# MS-6514

***Version 0B***
***05/21/2001 Update***

INTEL (R) Brookdale Chipset
Willamette/Northwood 478pin mPGA-B Processor Schematics


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**CPU:**

**Willamette/Northwood mPGA-478B Processor**

**System Brookdale Chipset:**

**INTEL MCH845 (North Bridge) +**
**INTEL ICH2 (South Bridge)**

**On Board Chipset:**

**BIOS -- FWH**
**AC'97 Codec -- AD1885**
**LPC Super I/O -- LPC47M142**
**Clock Generation -- CY28324**
**H/W Monitoring -- HECETA6 (Option)**

**Expansion Slots:**

**AGP2.0 SLOT (1.5V) * 1**
**PCI2.2 SLOT * 3**


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H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang


| | | |
|---|---|---|
| Title | COVER SHEET | |
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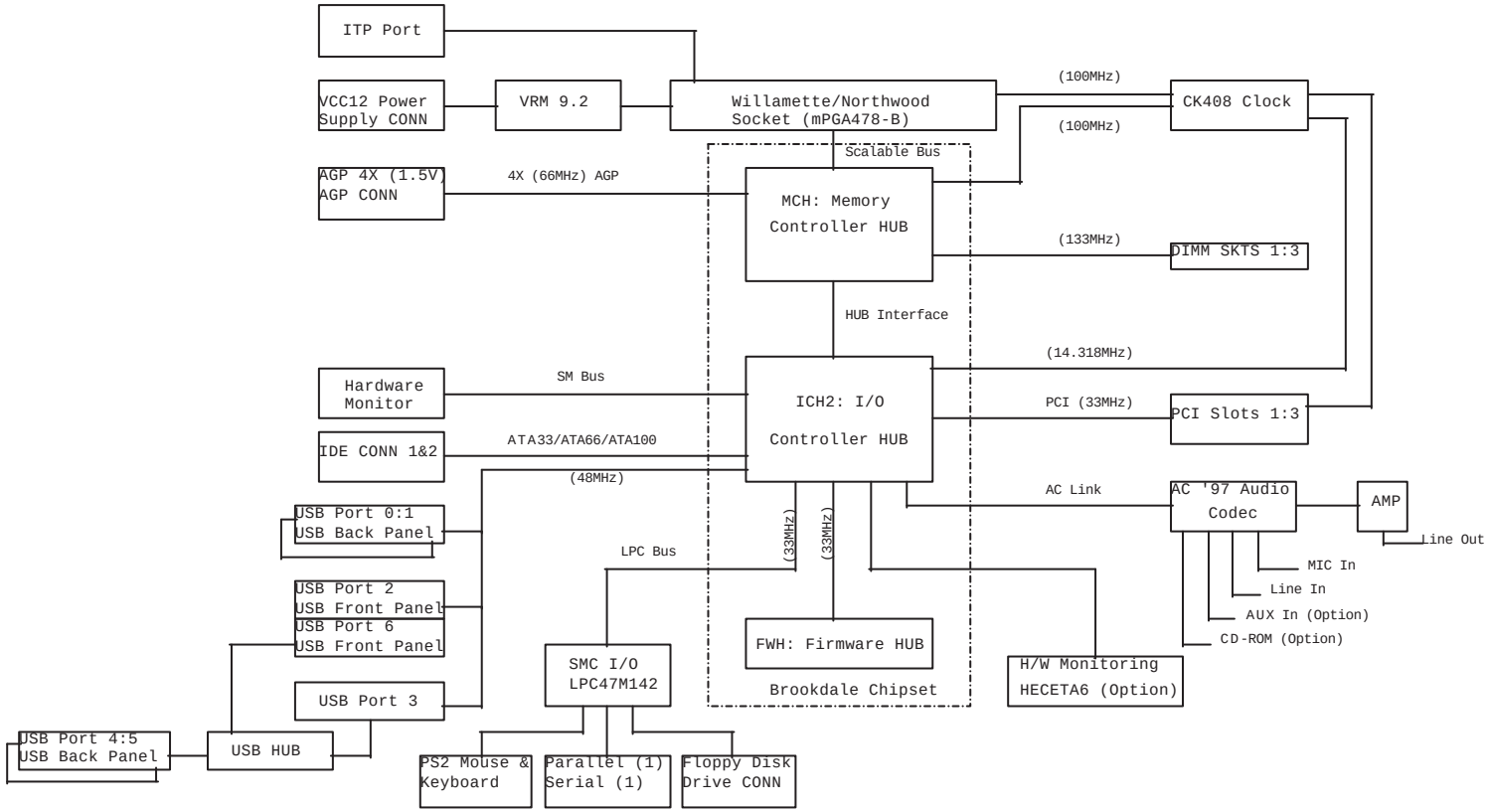


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H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang

Title: BLOCK DIAGRAM

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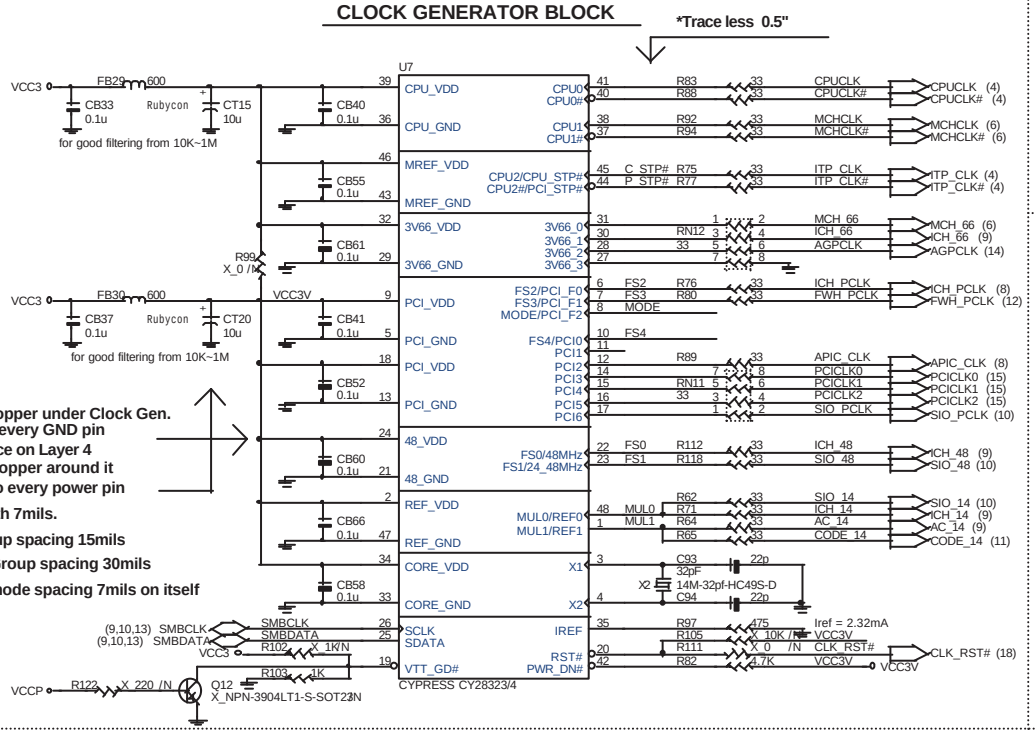
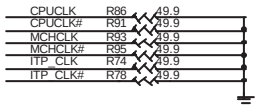
## CLOCK GENERATOR BLOCK



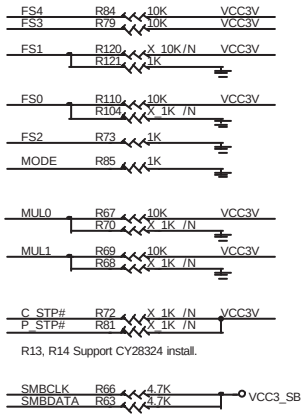

## Shut Source Termination Resistors



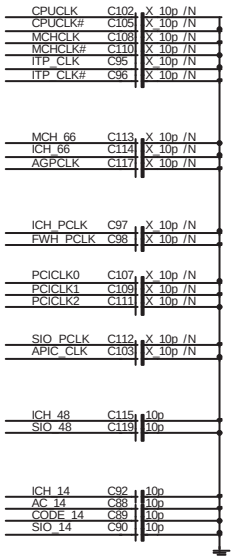

**Trace less 0.2"**

**49.9ohm for 50ohm M/B impedance**

## CLOCK STRAPPING RESISTORS




## Pull-Down Capacitors

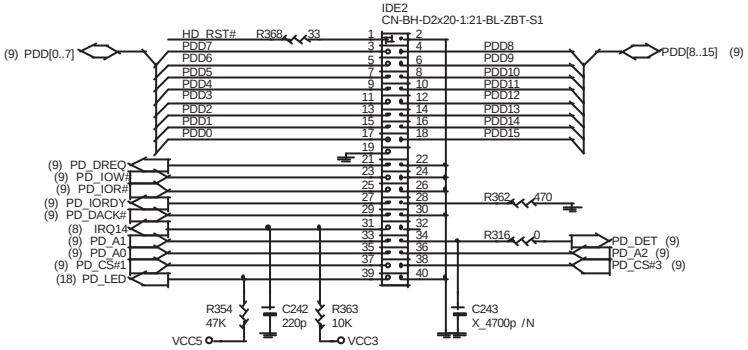



used only for EMI issue

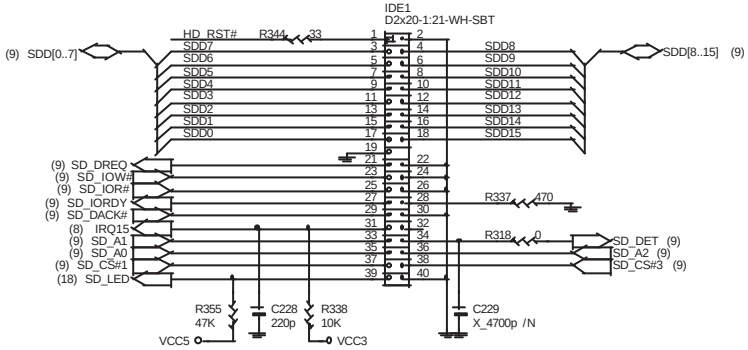
**Trace less 0.2"**

# ATA100 IDE CONNECTORS

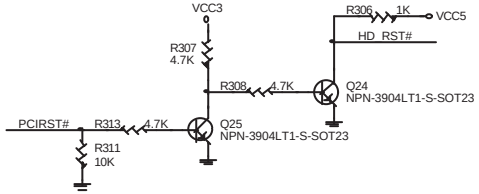
## PRIMARY IDE BLOCK




## SECONDARY IDE BLOCK




## RESET BLOCK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H/W Project Leader : Andy Chen

H/W Project Engineer : Prudence Wang

Title: CLOCK CY28324 & ATA100 IDE

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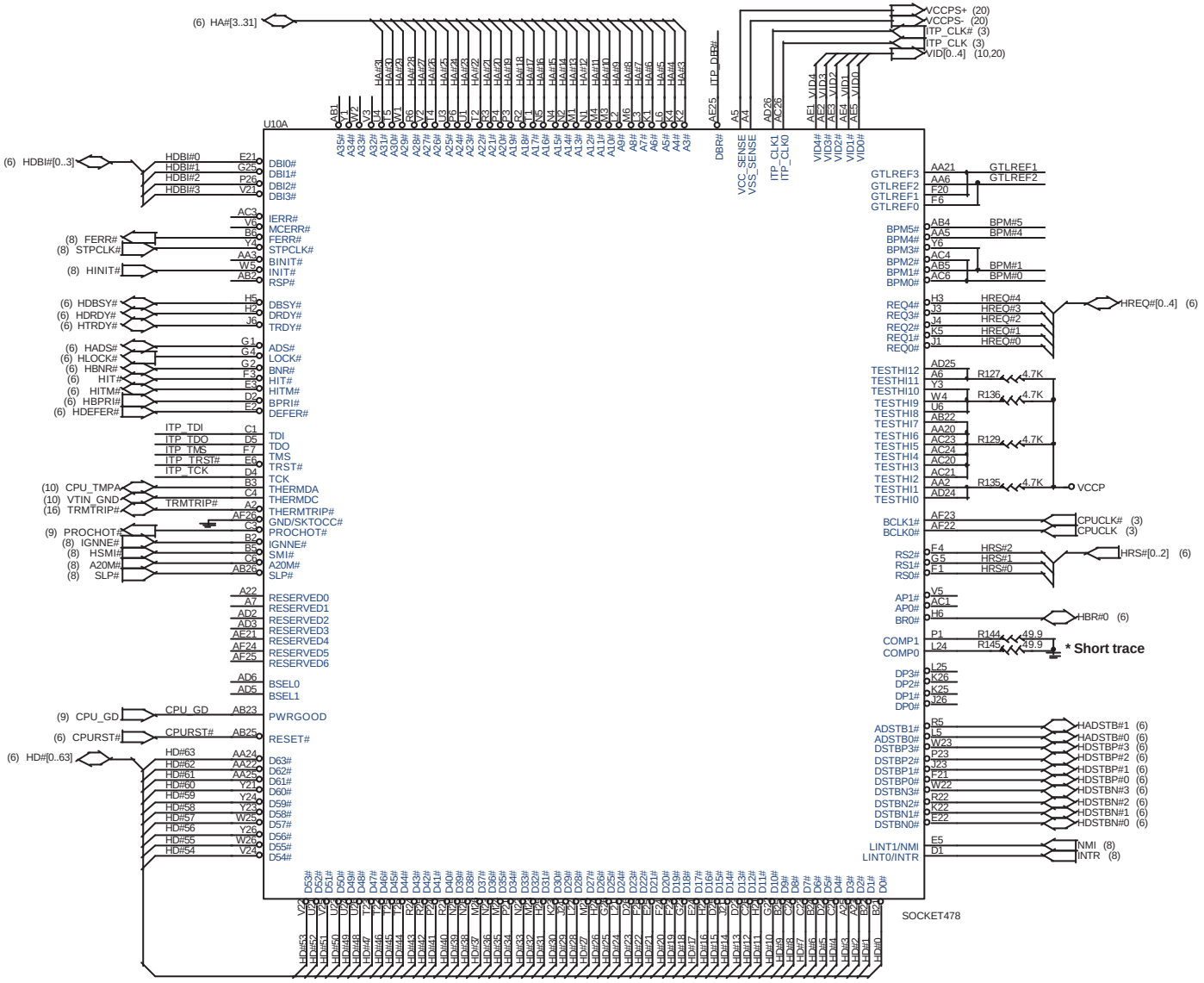
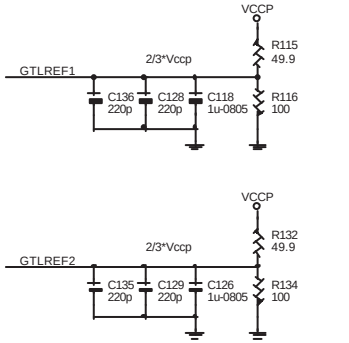
## CPU SIGNAL BLOCK



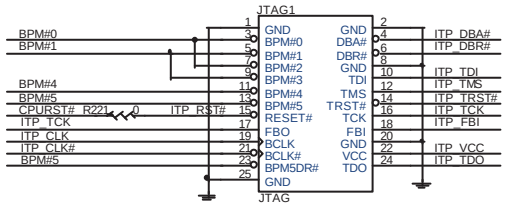

## CPU GTL REFERNCE VOLTAGE BLOCK

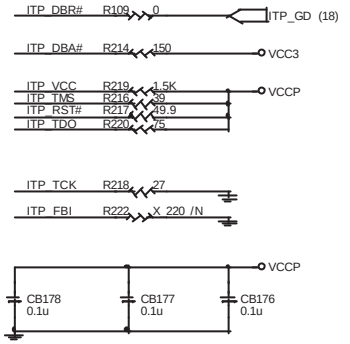



**Every pin put one 220pF cap near it.**

**Trace Width 15mils, Space 15mils.**

## CPU ITP BLOCK




**ALL COMPONENTS CLOSE TO CPU**

## CPU STRAPPING RESISTORS

**ALL COMPONENTS CLOSE TO CPU**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**MICRO-STAR**

H/W Project Leader : Andy Chen

H/W Project Engineer : Prudence Wang

| | | |
|---|---|---|
| Title | INTEL mPGA478-B CPU1 | |
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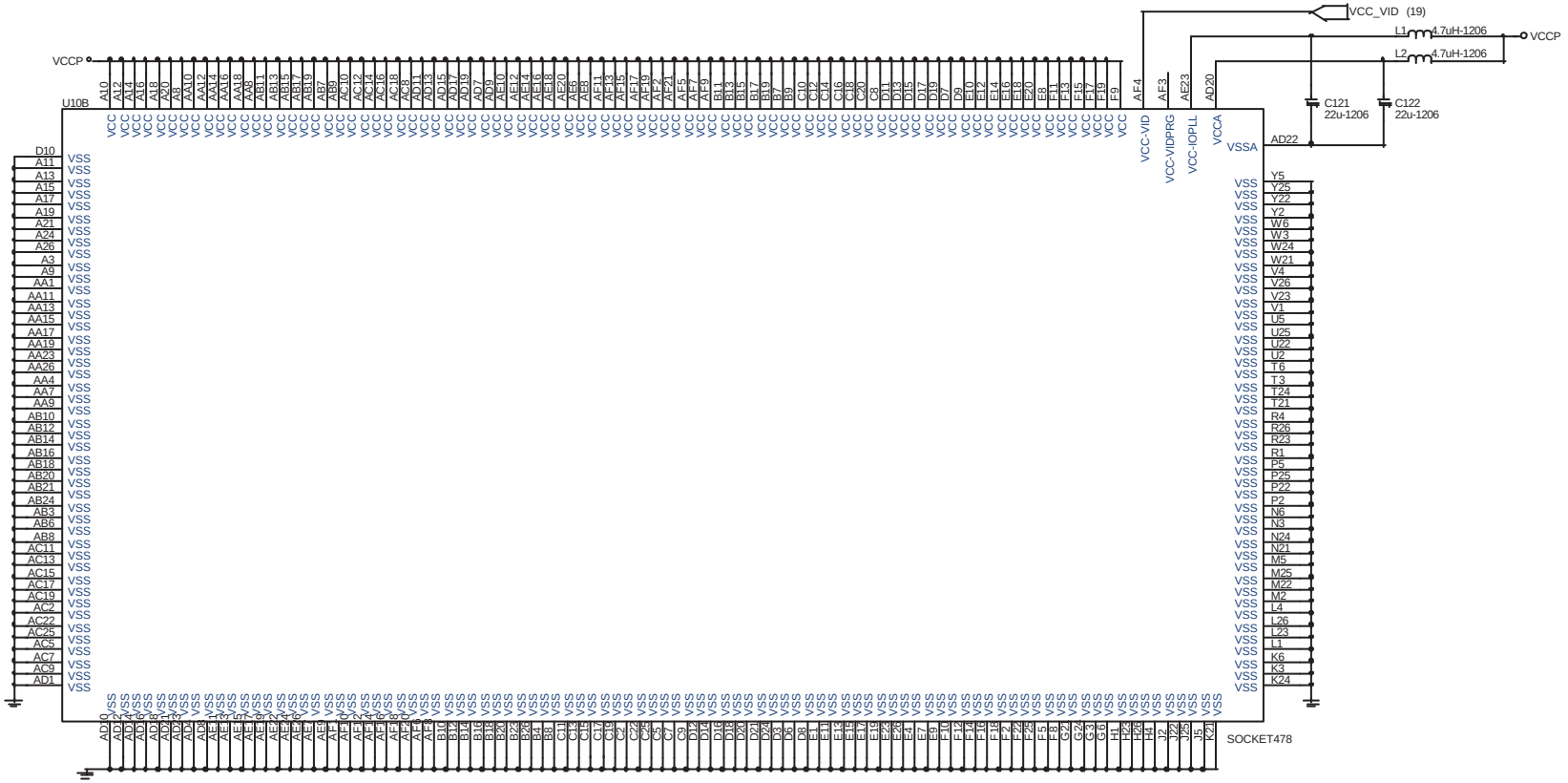
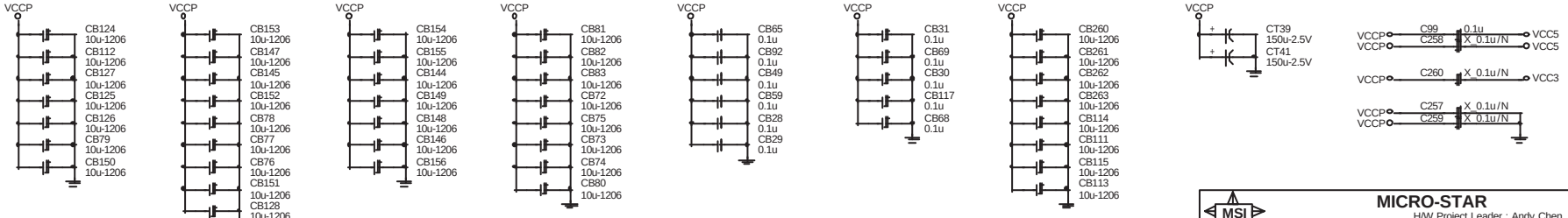
## CPU VOLTAGE BLOCK




## CPU DECOUPLING CAPACITORS




**PLACE CAPS WITHIN CPU CAVITY**

**PLACE CAPS WITHIN CPU CAVITY SOLDER**

| | | |
|---|---|---|
| MSI | **MICRO-STAR** H/W Project Leader : Andy Chen H/W Project Engineer : Prudence Wang | |
| Title | INTEL mPGA478-B CPU2 | |
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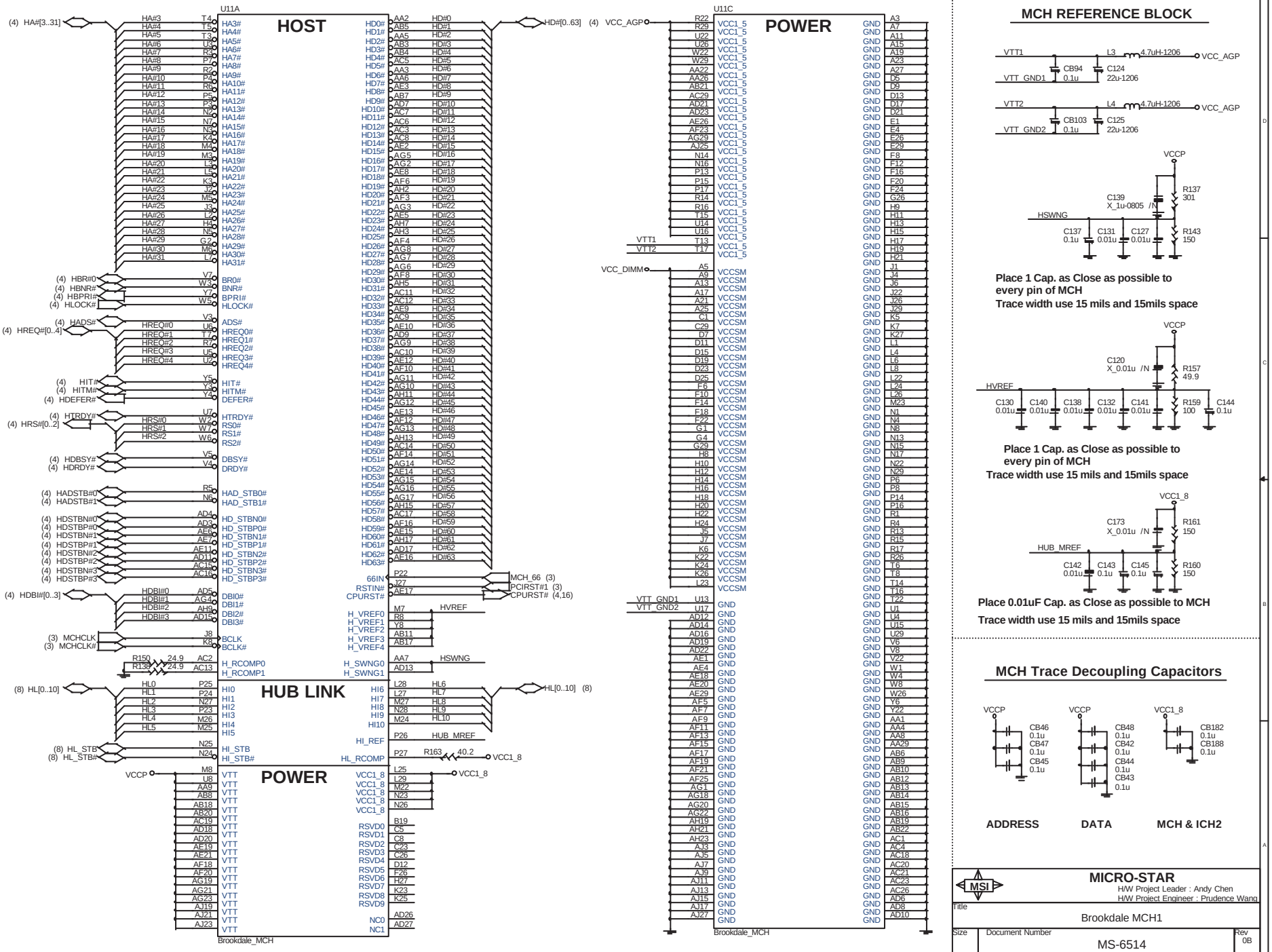


## MCH REFERENCE BLOCK




**Place 1 Cap. as Close as possible to every pin of MCH**
**Trace width use 15 mils and 15mils space**




**Place 1 Cap. as Close as possible to every pin of MCH**
**Trace width use 15 mils and 15mils space**




**Place 0.01uF Cap. as Close as possible to MCH**
**Trace width use 15 mils and 15mils space**

## MCH Trace Decoupling Capacitors




**ADDRESS** **DATA** **MCH & ICH2**

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**MICRO-STAR**

H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang

| | | |
|---|---|---|
| Title | Brookdale MCH1 | |
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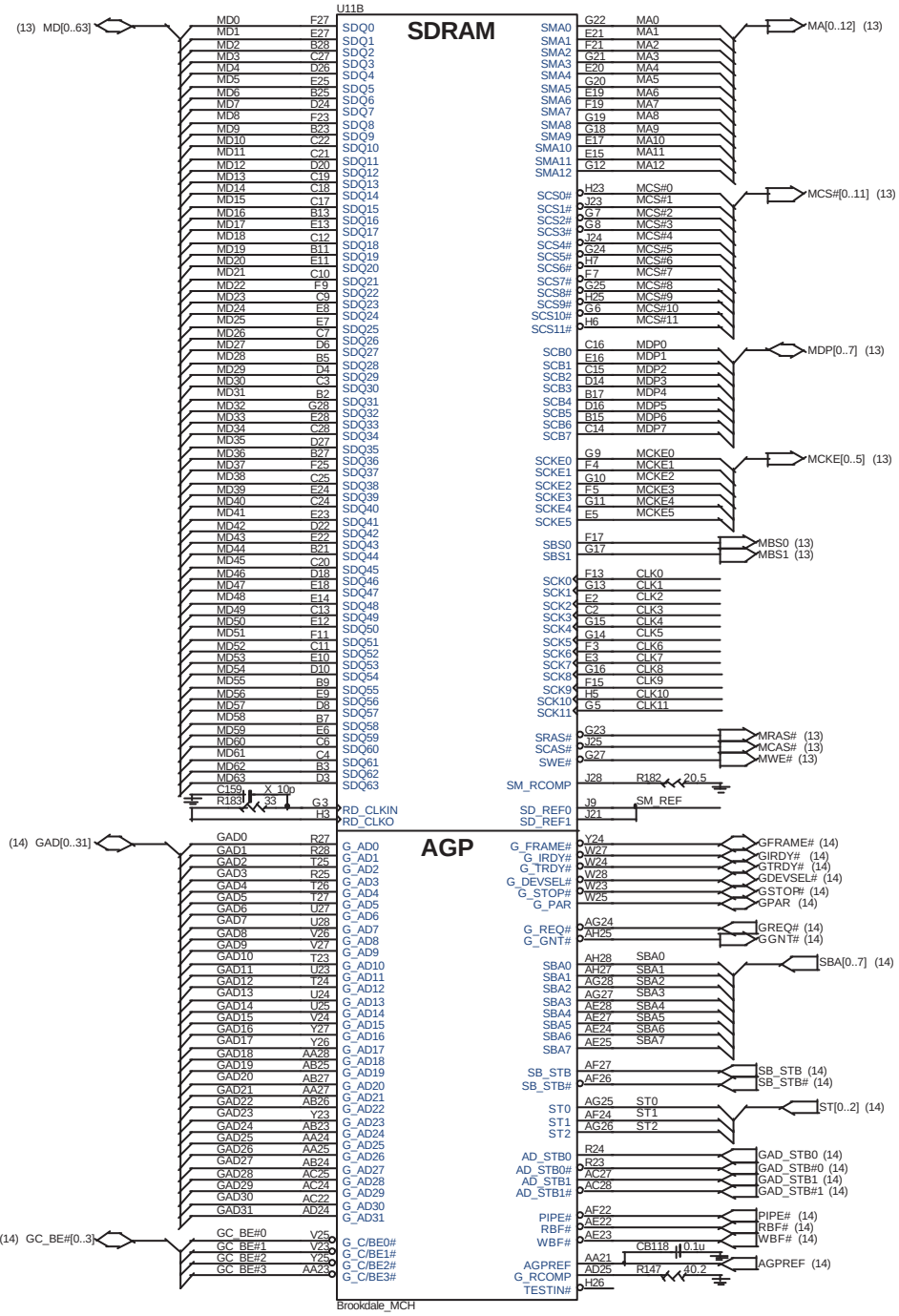
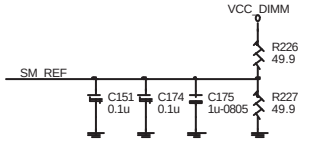
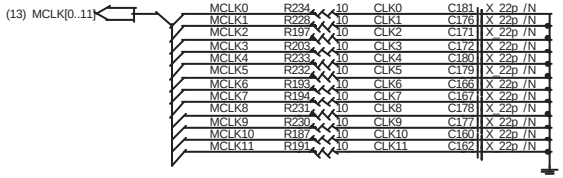


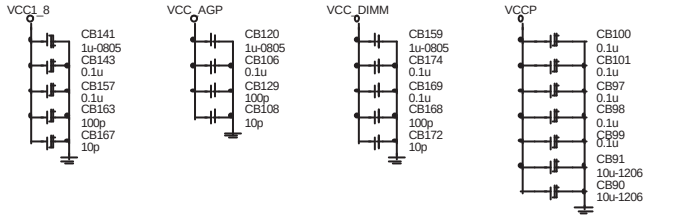

## MCH REFERENCE VOLTAGE

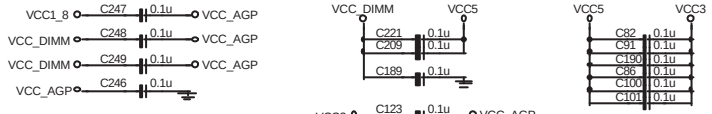



## MCH MEMORY CLOCK RC CIRCUITS

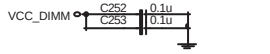



## MCH DECOUPLING CAPACITOR

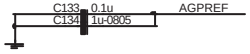



**Put MCH845 solder side**





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H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang

| | | |
|---|---|---|
| Title | Brookdale MCH2 & AGP SLOT | |
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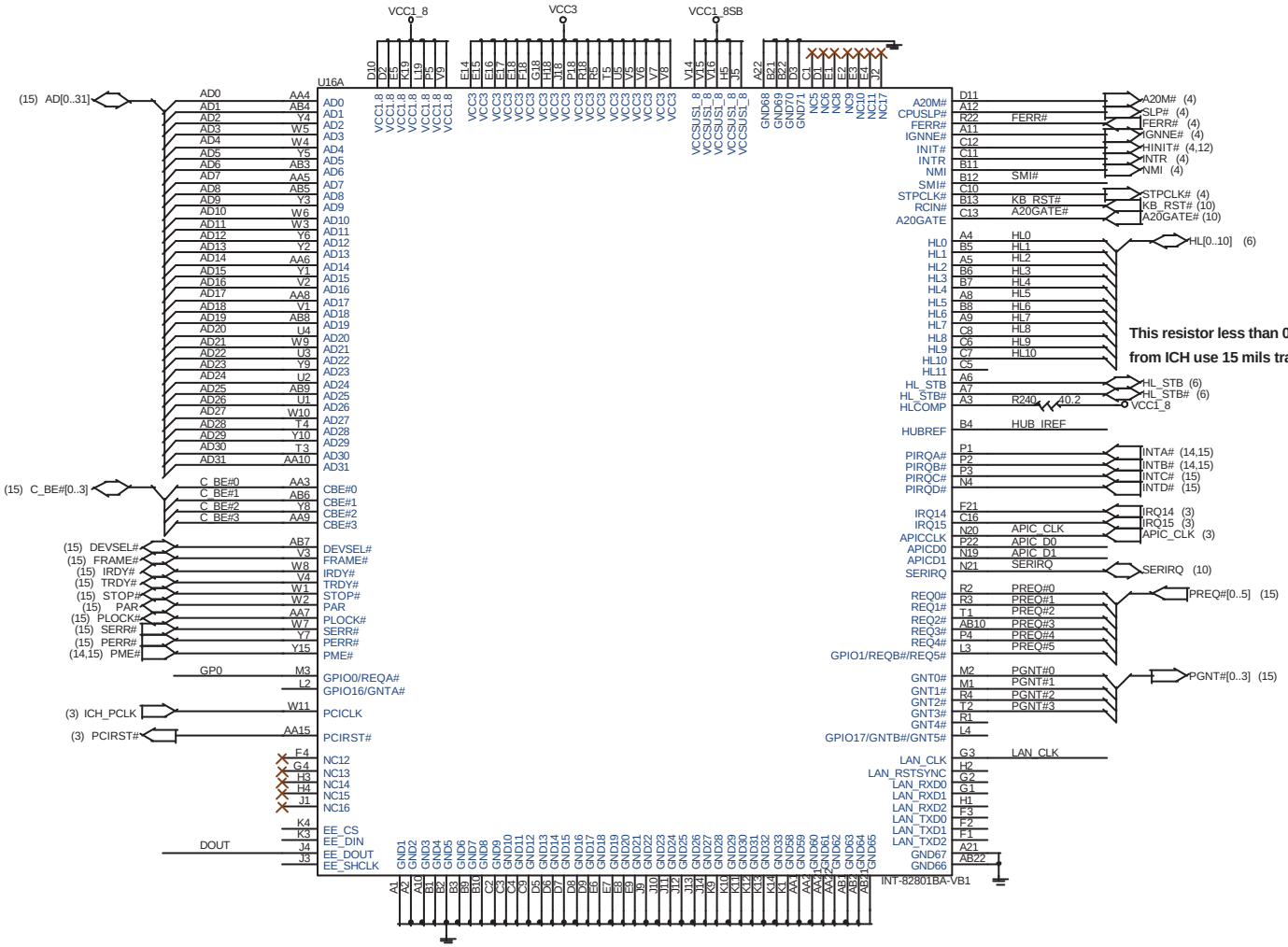
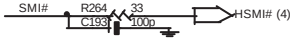
## ICH2 PCI / HUB LINK / CPU / LAN / INTERRUPT SIGNALS

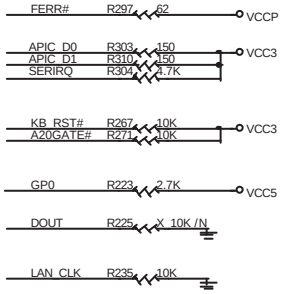



This resistor less than 0.5" from ICH use 15 mils trace

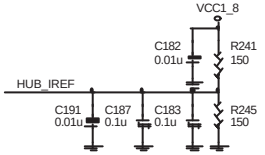
## ICH2 SMI# SIGNAL




## ICH2 STRAPPING RESISTORS



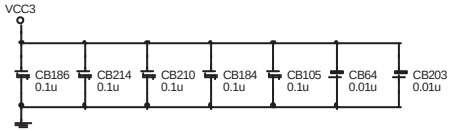

## ICH2 REFERENCE VOLTAGE



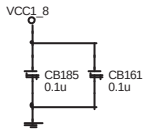

Place Cap. as Close as possible to ICH2

Trace width use 15 mils and 15mils space

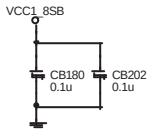
## ICH2 DECOUPLING CAPACITORS




Place one 0.1U/0.01U pair in each corner and 2 on opposite sides close to ICH2 if it fit




Distribute near the 1.8V power pin of the ICH2




Distribute near the VCC1_8SB Power pin of the ICH2

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**MICRO-STAR**

H/W Project Leader : Andy Chen

H/W Project Engineer : Prudence Wang

| | | |
|---|---|---|
| Title | Brookdale ICH2 PCI | |
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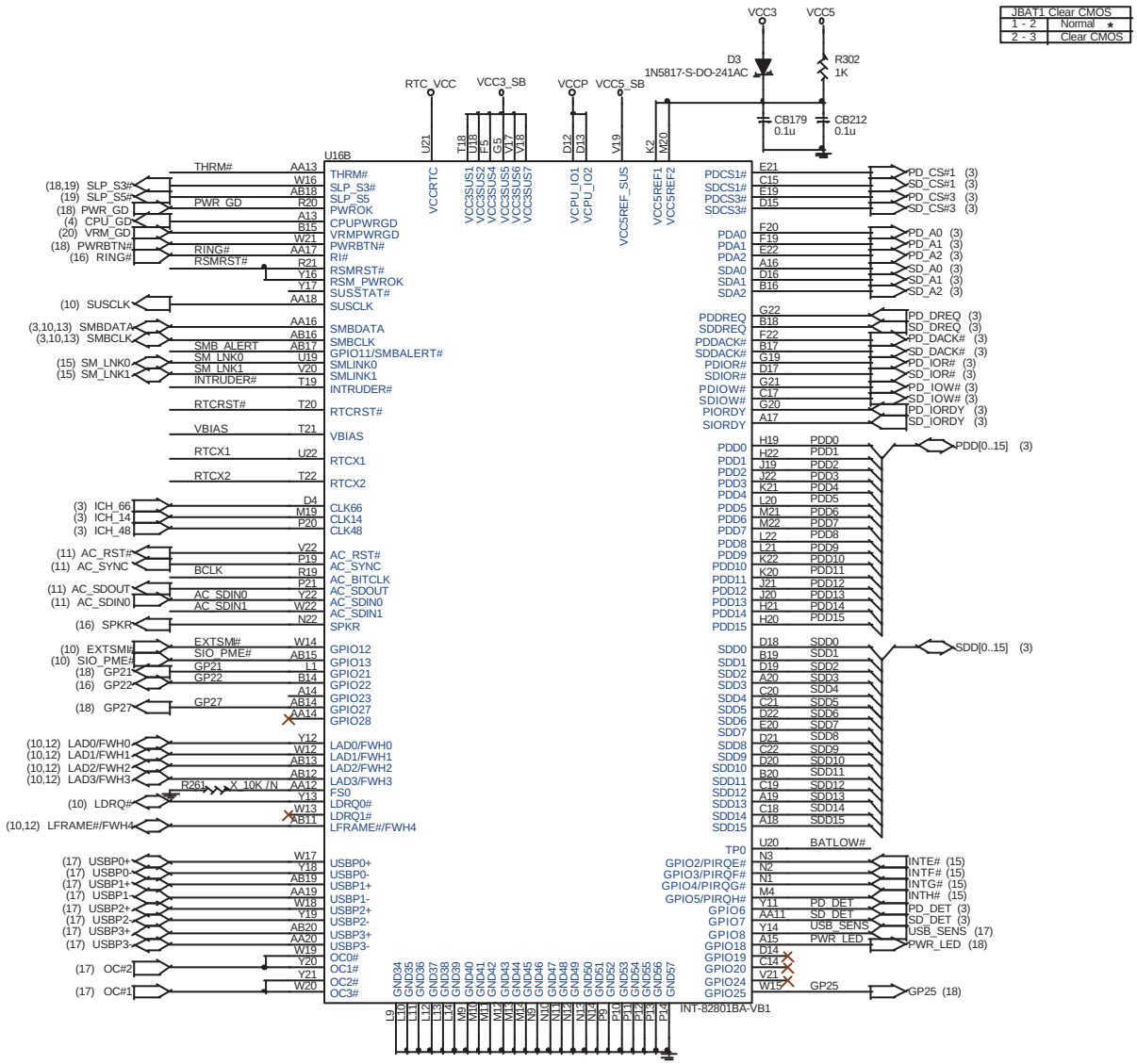
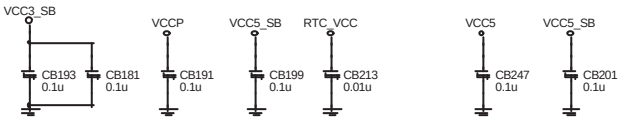
# ICH2 ASIC / RTC / AC'97 / GPIO / LPC / USB / IDE SIGNALS

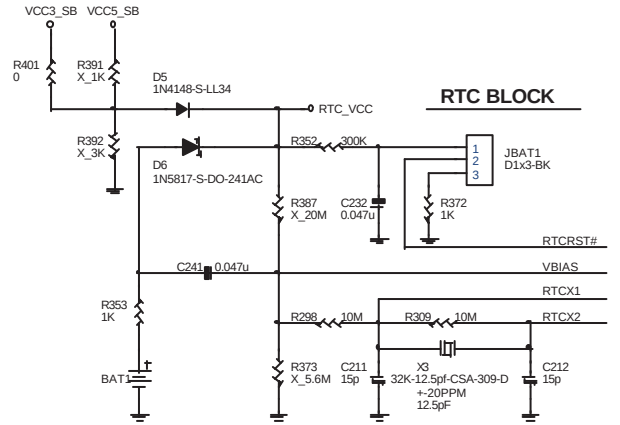



## ICH2 DECOUPLING CAPACITOR

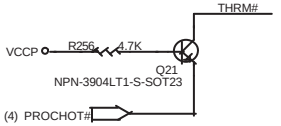



Distribute near the VCC3_SB power pin of the ICH

## RTC BLOCK

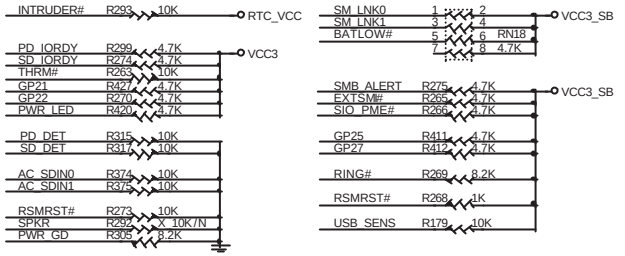



## PROCHOT BLOCK

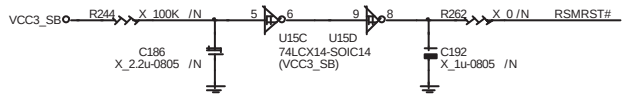



## CODEC CLOCK

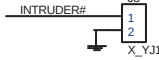

## ICH2 STRAPPING RESISTORS




## RESUME RESET CIRCUIT BLOCK




## INTERUDER




| | | |
|---|---|---|
| MSI | MICRO-STAR | H/W Project Leader : Andy Chen<br>H/W Project Engineer : Prudence Wang |
| Title | Brookdale ICH2 OTHER | |
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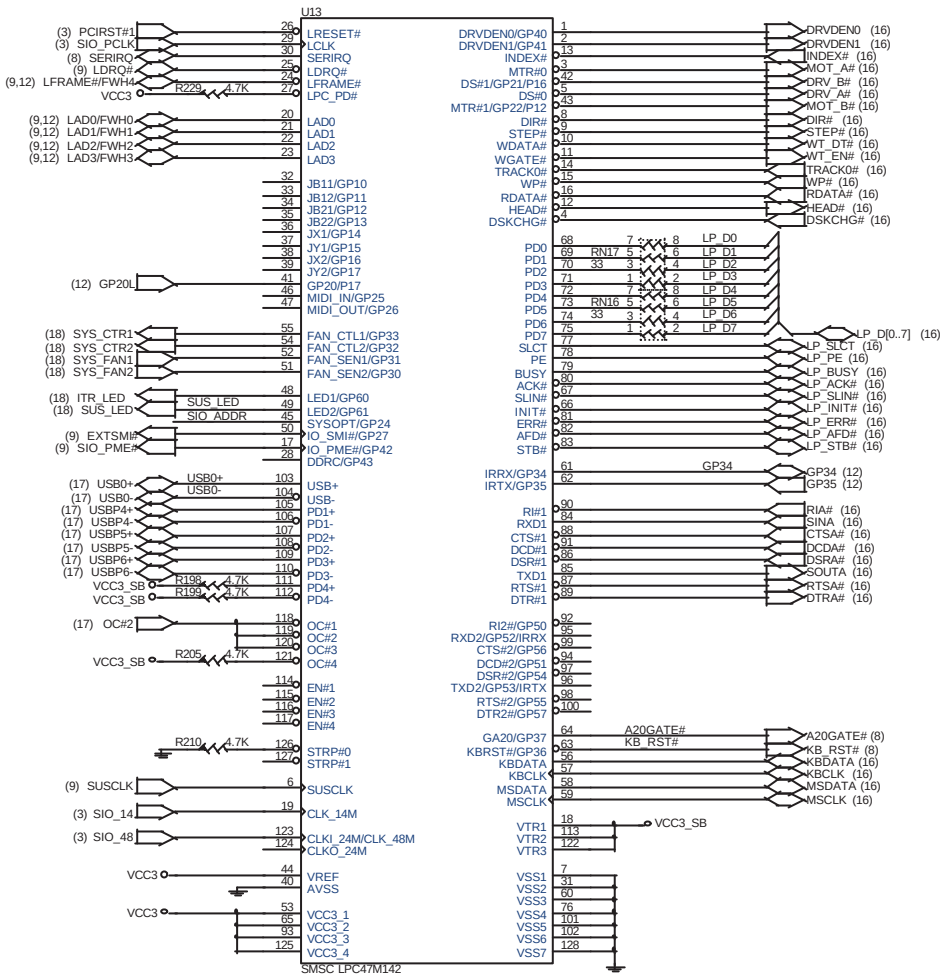
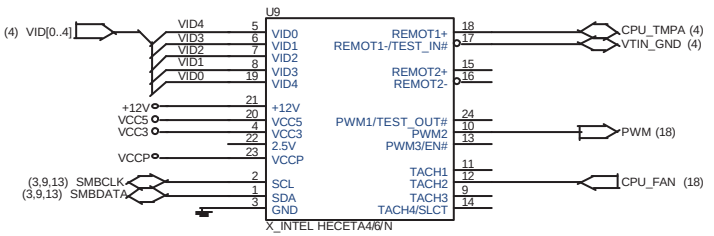
## LPC SUPER I/O LPC47M142

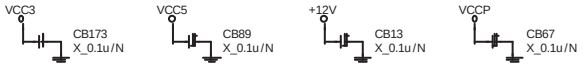



## H/W MONITOR -- INTEL HECETA6

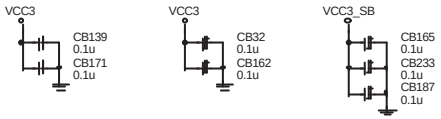



**ADDR.=101110XB**

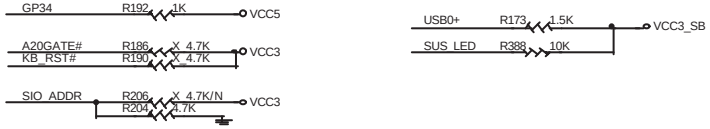
## H/W MONITOR DECOUPLING CAPACITORS




## LPC I/O DECOUPLING CAPACITORS




## LPC I/O STRAPPING RESISTOR




SYS_ADDR
H: 0x04E
L: 0x02E (DEFAULT)

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**MICRO-STAR**

H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang

Title: LPC I/O LPC47M142 & H/W MONITOR HECETA6

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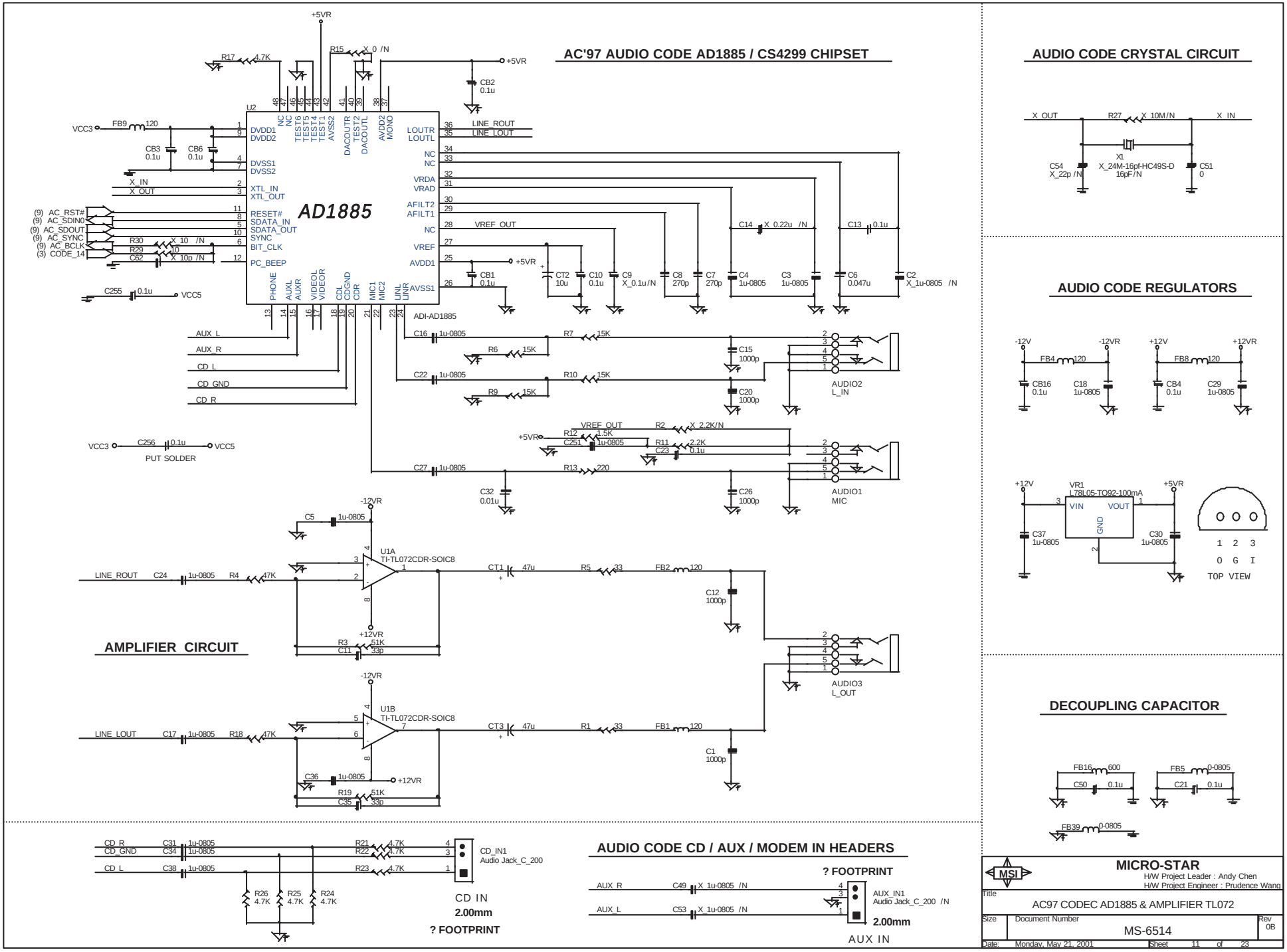
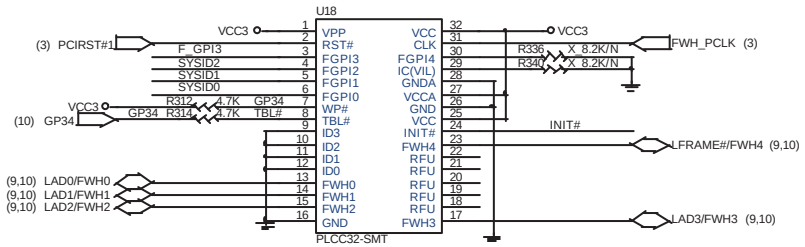
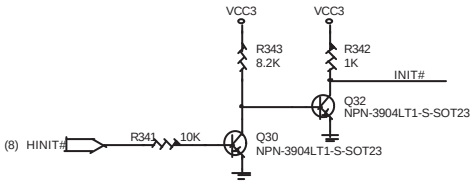

AC'97 AUDIO CODE AD1885 / CS4299 CHIPSET
AD1885
ADI-AD1885
AMPLIFIER CIRCUIT
PUT SOLDER
AUDIO CODE CRYSTAL CIRCUIT
AUDIO CODE REGULATORS
DECOUPLING CAPACITOR
AUDIO CODE CD / AUX / MODEM IN HEADERS
CD IN
2.00mm
? FOOTPRINT
AUX IN
MICRO-STAR
H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang
AC97 CODEC AD1885 & AMPLIFIER TL072
MS-6514
Monday, May 21, 2001

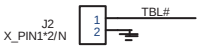
## Firware Hub (FWH)



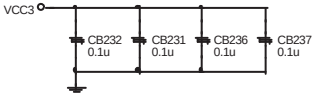

## FWH INIT Signal Voltage Translation Block



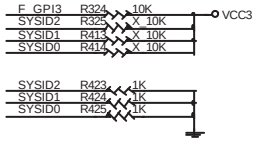

## BIOS Lock Mode Block



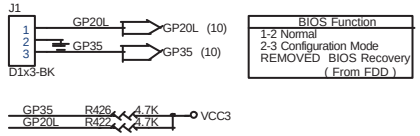

## FWH DECOUPLING CAPACITORS



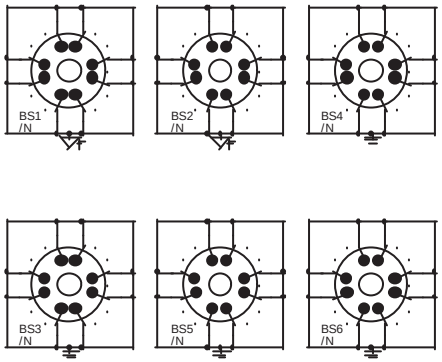

## FWH RESISTORS

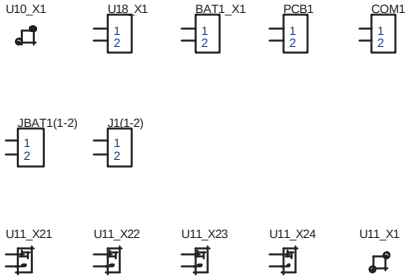



## BIOS Configuration Mode Block




## PCB OTHER COMPONENT




## SIMULATION TRACE


MICRO-STAR
H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang

| | | |
|---|---|---|
| Title | FWH & MANUAL | |
| Size | Document Number: MS-6514 | Rev: 0B |
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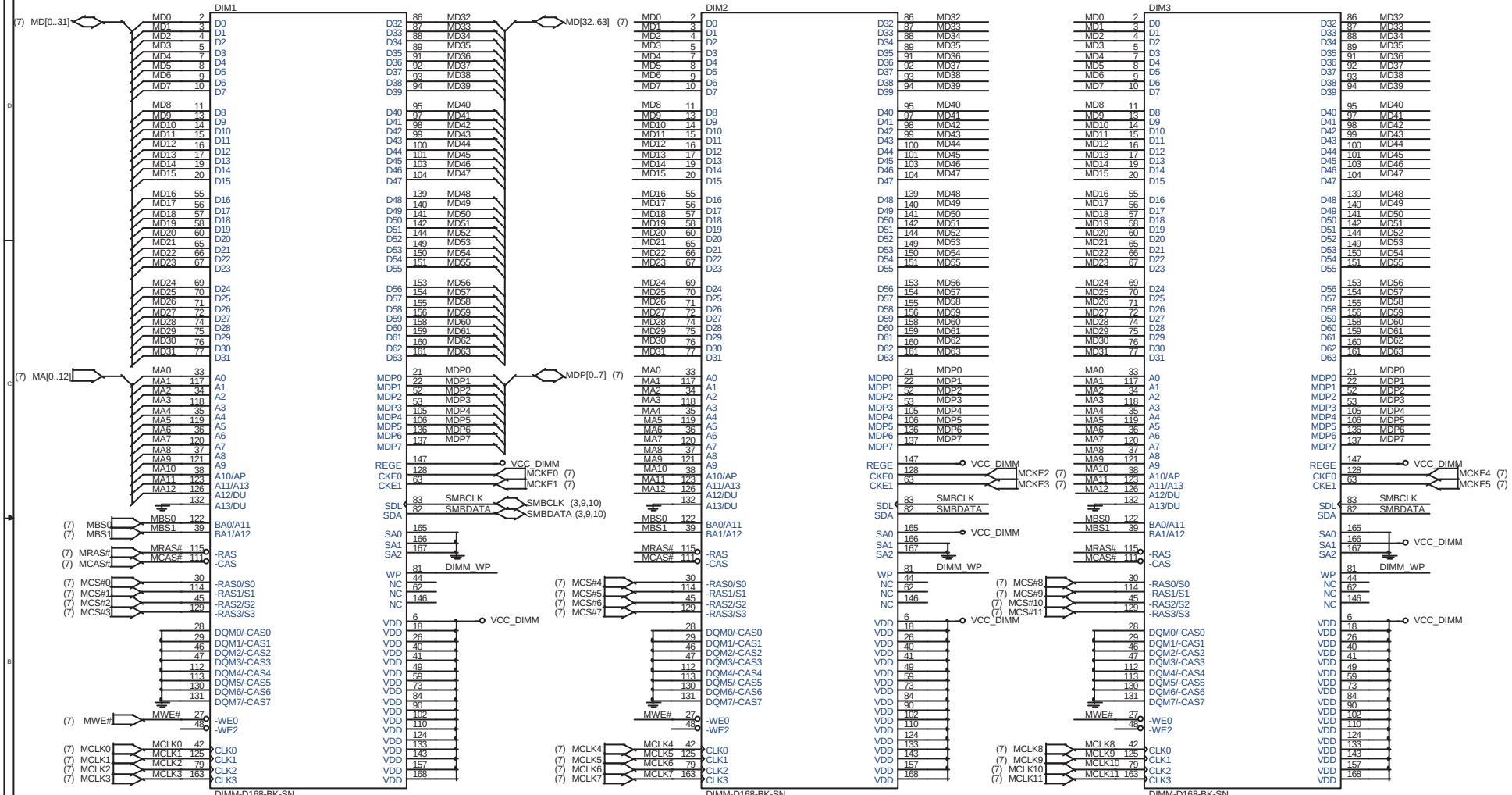
## DIMM1




**ADDR.=1010000B**

## DIMM2



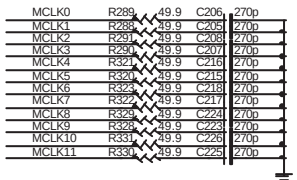

**ADDR.=1010001B**

## DIMM3

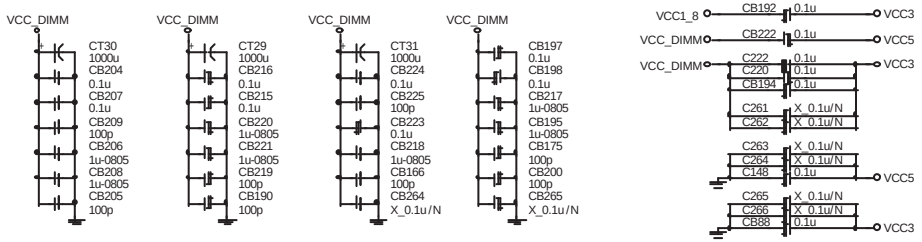



**ADDR.=1010010B**

## DIMM CLOCK




## DECOUPLING CAPACITORS




## DIMM SPD WE BLOCK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**MICRO-STAR**

H/W Project Leader : Andy Chen

H/W Project Engineer : Prudence Wang

| | | |
|---|---|---|
| Title | DIMM 1 & 2 & 3 | |
| Size | Document Number | Rev |
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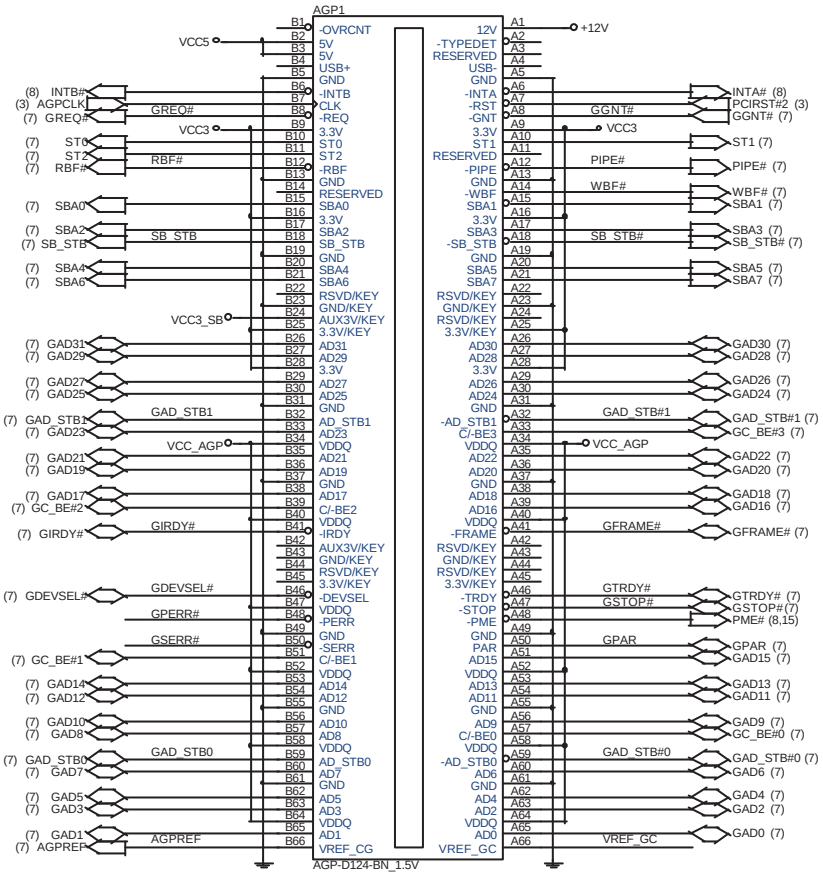
| Date: Monday, May 21, 2001 | Sheet 13 of 23 | |

## AGP 1.5V 2X/4X SLOT(AGP VER:2.0 COMPLY)

**VCC5 = 60mils trace / 15 mils space**

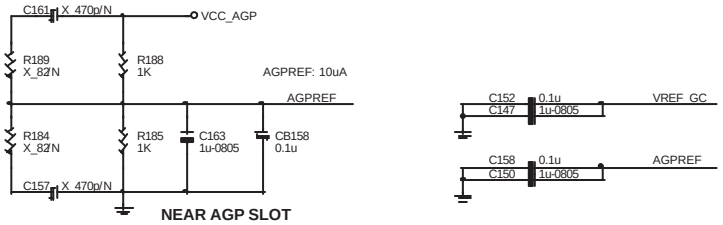



**INTA#**
**INTB#**

AGP Slot Imax

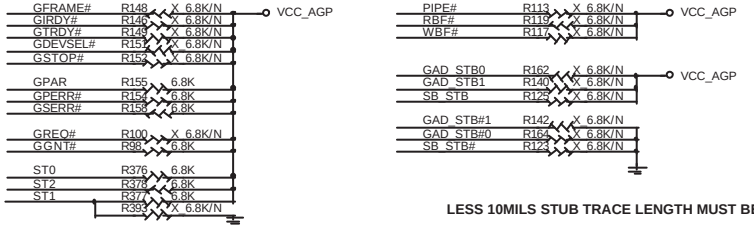
| | |
|---|---|
| VCCq | 8.0A |
| VCC3 | 6.0A |
| VCC12 | 1.0A |
| VCC5 | 2.0A |
| VCC3_SB | ?A |

## AGP SIGNAL REFERENCE CIRCUIT




**NEAR AGP SLOT**

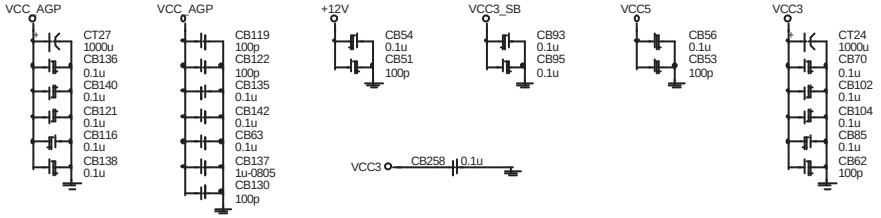
## AGP TERMINATION RESISTORS




**LESS 10MILS STUB TRACE LENGTH MUST BE FOLLOWING.**

**Place these resistors between PCI and AGP slot**

## AGP SLOT DECOUPLING CAPACITORS

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**MICRO-STAR**

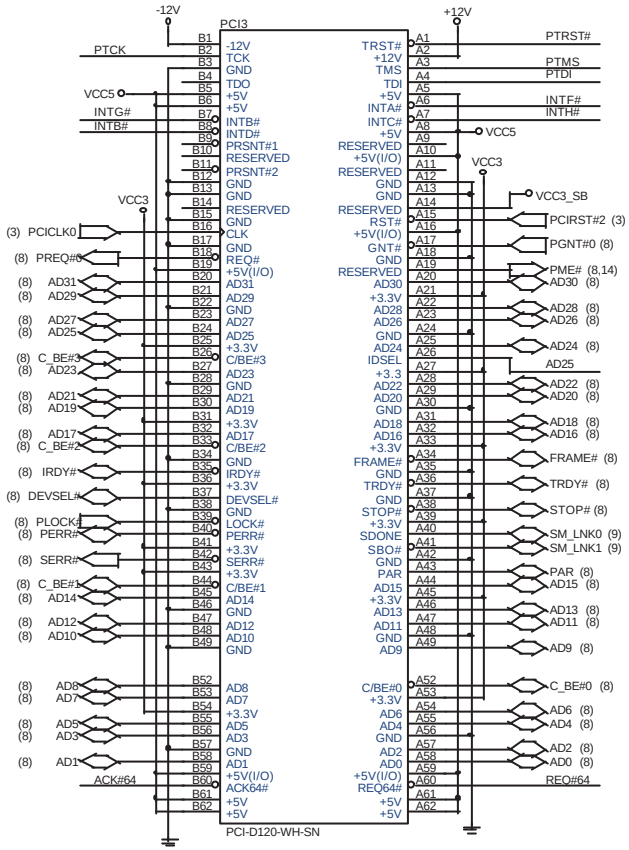
H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang

Title: AGP SLOT

Size | Document Number: MS-6514 | Rev: 0B

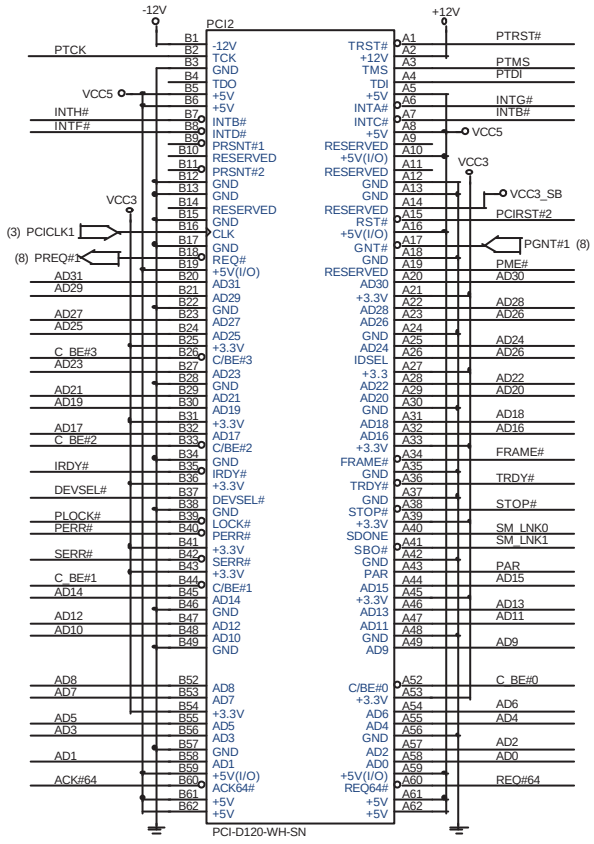
Date: Monday, May 21, 2001 | Sheet 14 of 23

## PCI SLOT 1 (PCI VER: 2.2 COMPLY)



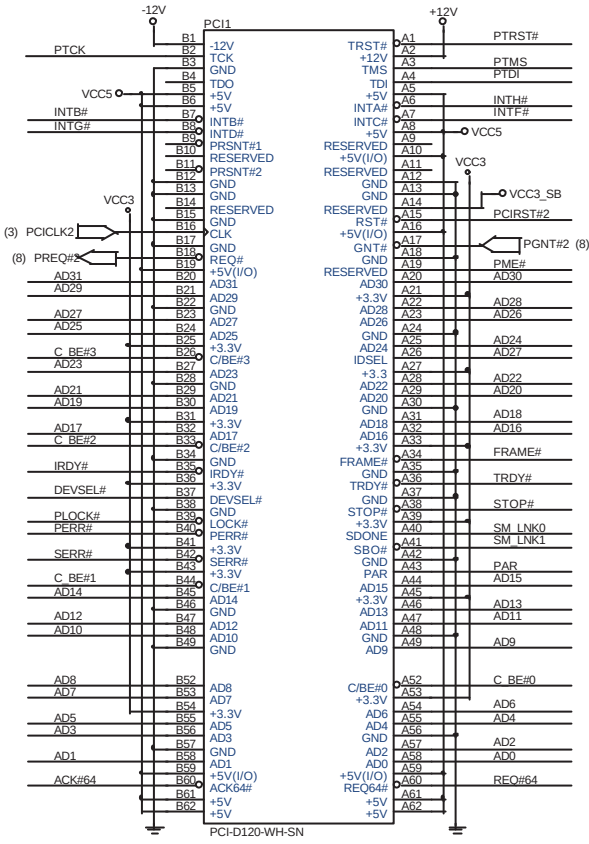

**IDSEL = AD25**
**MASTER = PREQ0**
**INTF#**

## PCI SLOT 2 (PCI VER: 2.2 COMPLY)



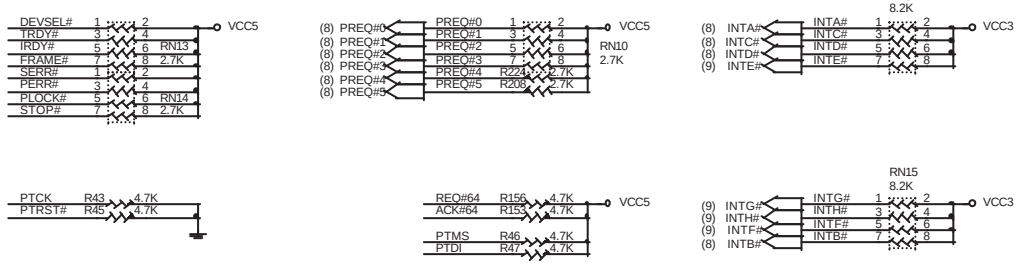

**IDSEL = AD26**
**MASTER = PREQ1**
**INTG#**

## PCI SLOT 3 (PCI VER: 2.2 COMPLY)

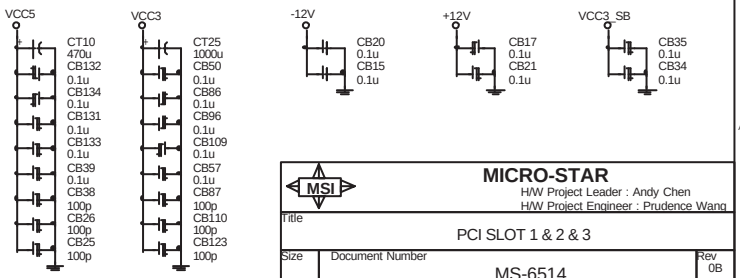



**IDSEL = AD27**
**MASTER = PREQ2**
**INTH#**

## PCI PULL-UP / DOWN RESISTORS




## PCI SLOT DECOUPLING CAPACITORS

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**MICRO-STAR**

H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang

| | | |
|---|---|---|
| Title | PCI SLOT 1 & 2 & 3 | |
| Size | Document Number: MS-6514 | Rev 0B |
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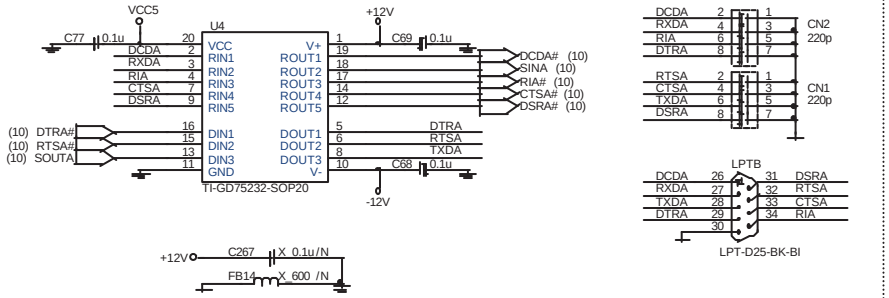
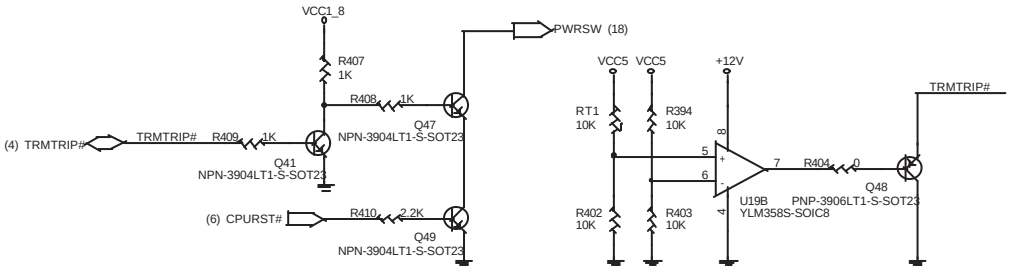
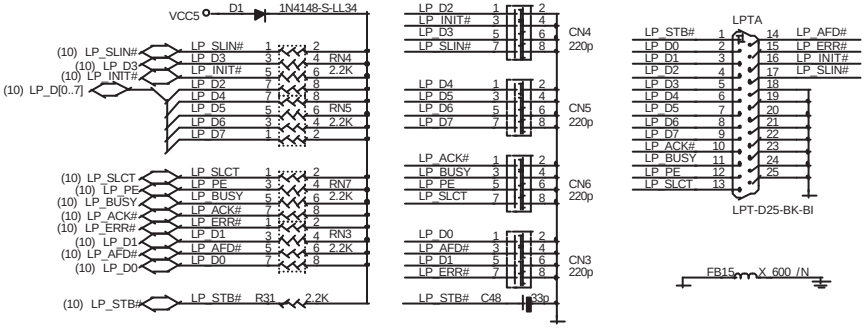
## SERIAL PORT 1



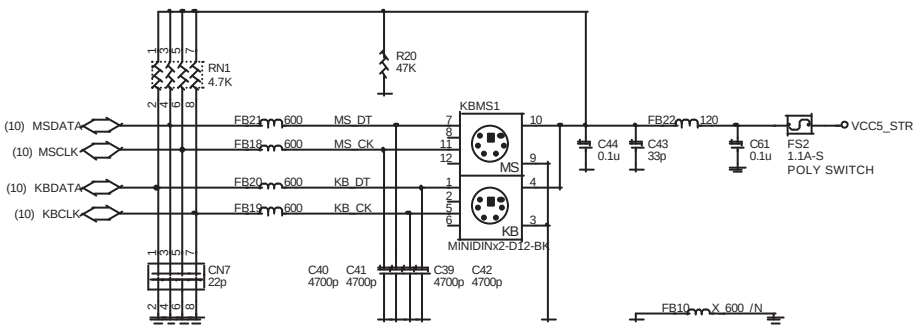

## THERMTRIP# CIRCUIT BLOCK




## PARALLAL PORT

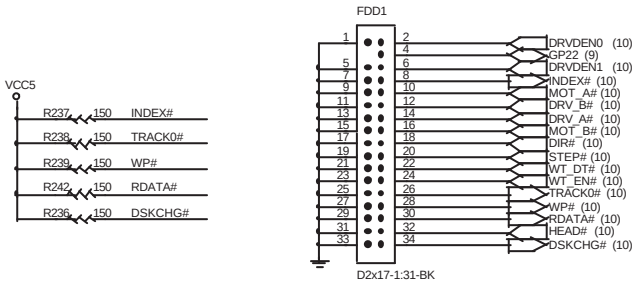



## PS2 KEYBOARD & MOUSE CONNECTOR

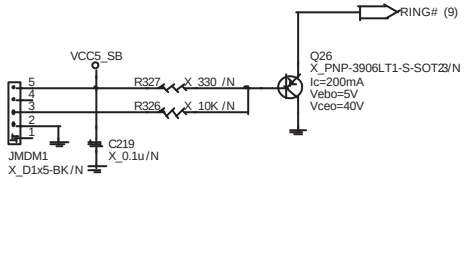



**PS. STANDARD**

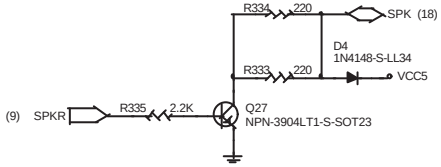
## FLOPPY CONNECTOR




## MODEM RING BLOCK




## SPEAKER




**MICRO-STAR**

H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang

| | | |
|---|---|---|
| Title | IO CONNECTOR | |
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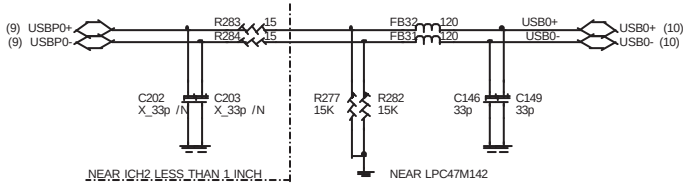
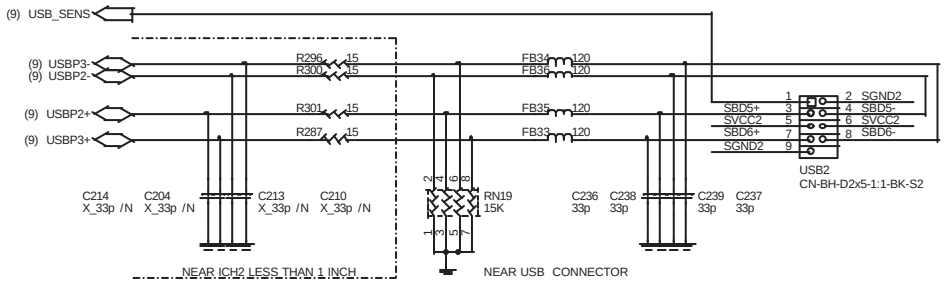
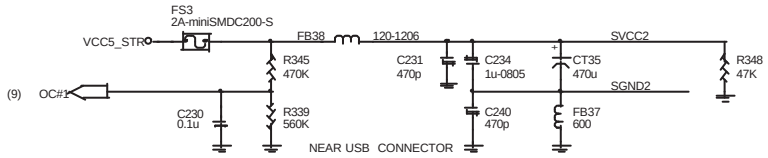
## SPARE USB SIGNAL



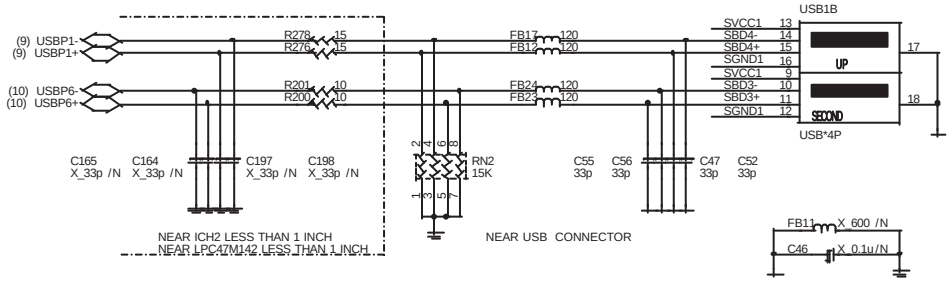

## FRONT PANEL USB CONNECTOR FOR USB PORT 5,6



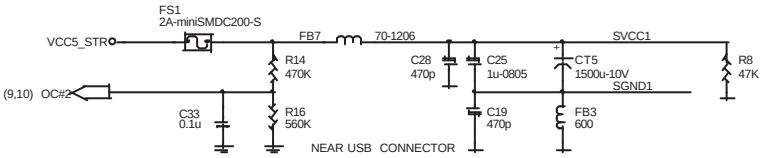

## POWER CIRCUIT FOR USB PORT 5,6




## REAR PANEL USB CONNECTOR FOR USB PORT 1,2

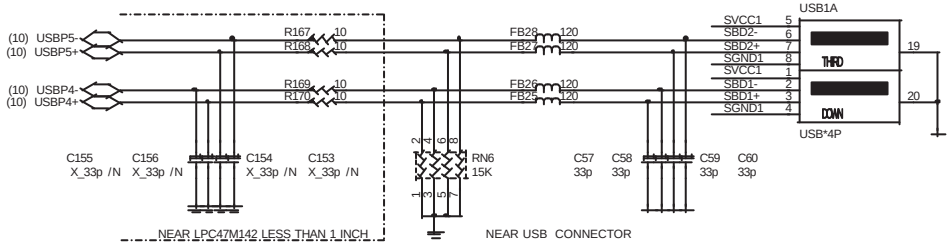


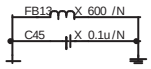

## POWER CIRCUIT FOR USB PORT 1,2,3,4





## REAR PANEL USB CONNECTOR FOR USB PORT 3,4




**RMOVED**

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**MICRO-STAR**

H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang

Title: USB HUB & USB CONNECTORS

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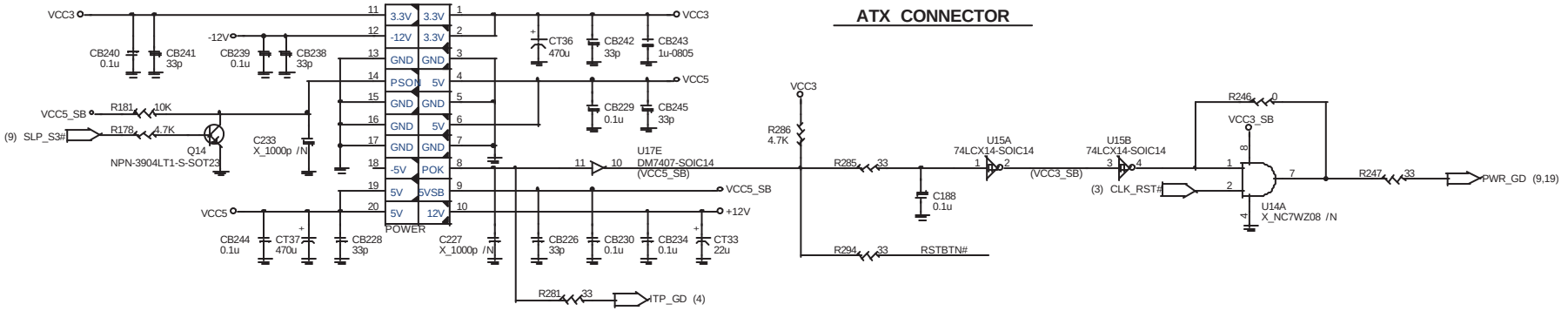
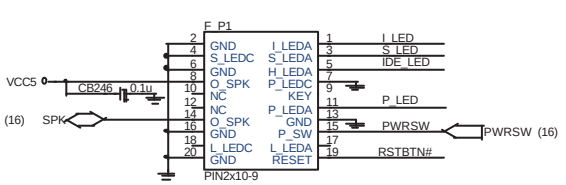
## ATX CONNECTOR



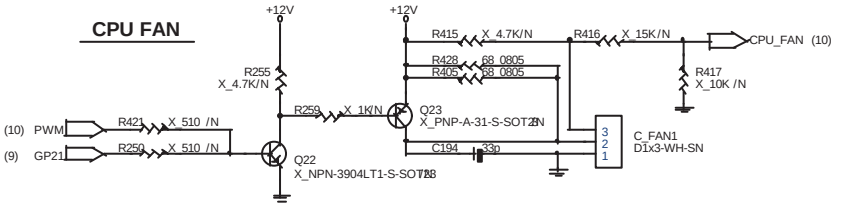

## FRONT PANEL HEADERS



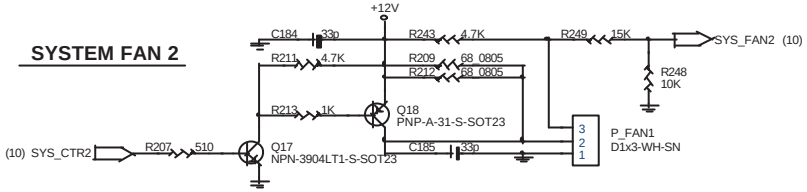

| STATE | S0 | S1 | S3 | S4/S5 |
|---|---|---|---|---|
| P_LED (Green) | BRIGHT | DARK | DARK | DARK |
| S_LED (Yellow) | DARK | BRIGHT | BRIGHT | DARK |
| L_LED (Option) | N/A | N/A | N/A | N/A |
| I_LED (Green) | Blinking | Blinking | DARK | DARK |

* GP25 default 1
*GP27 default 1
* ITR_LED default 1

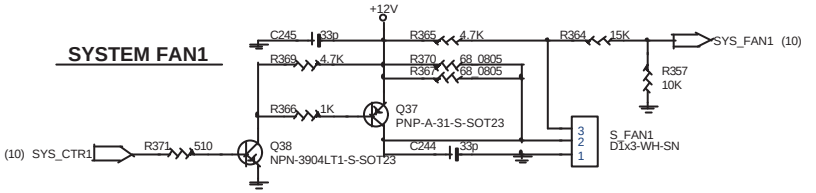
## CPU FAN



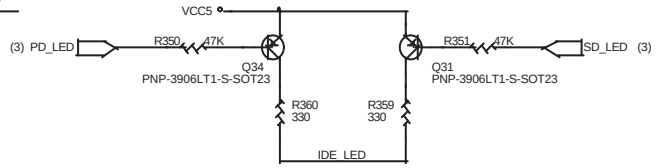

## SYSTEM FAN 2



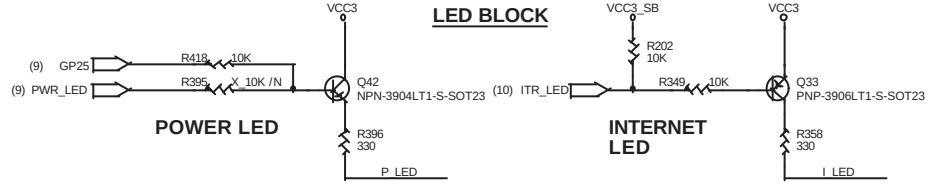

## SYSTEM FAN1



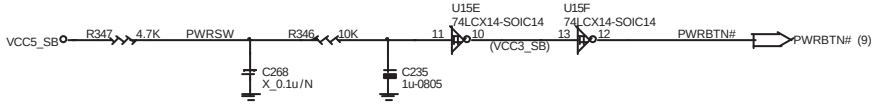

## IDE LED

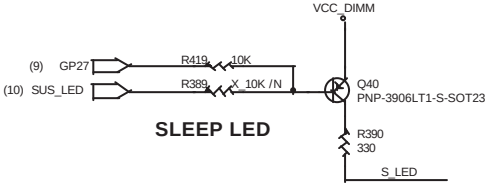



## LED BLOCK




## POWER BUTTON

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**MICRO-STAR**

H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang

Title: FRONT_PANEL & ATX CONNETOR & FAN

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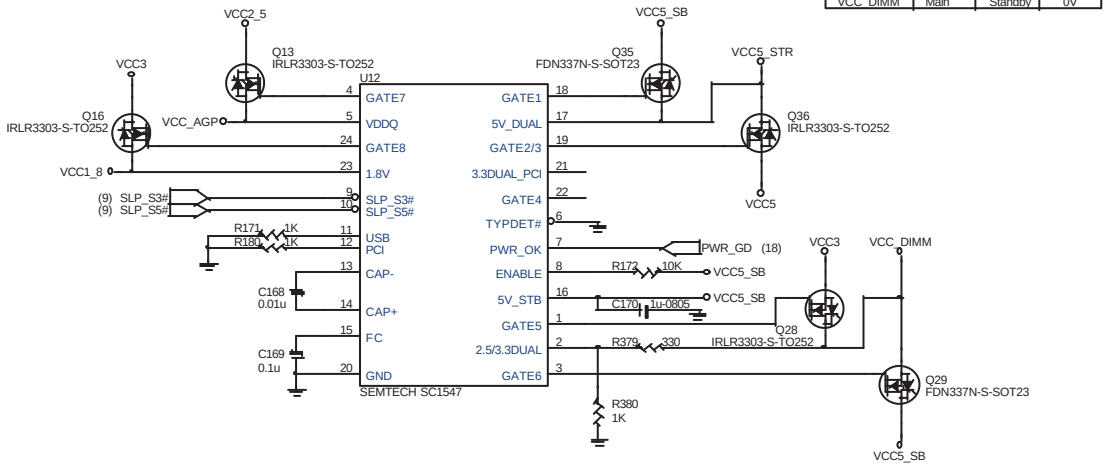
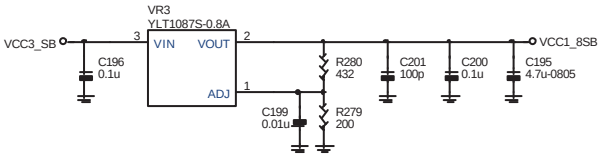
## POWER TRANSLATOR

| Power | S0 | S3 | S5 |
|---|---|---|---|
| VCC3_SB | Main | Standby | Standby |
| VCC5_STR | Main | Standby | 0V |
| VCC_DIMM | Main | Standby | 0V |



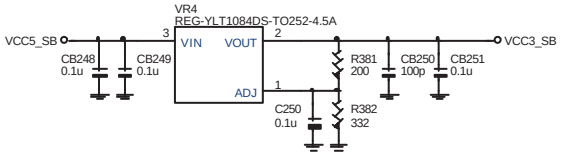

## 1.8V STANDBY POWER TRANSLATOR

**(40mils trace / 20 mils space)**

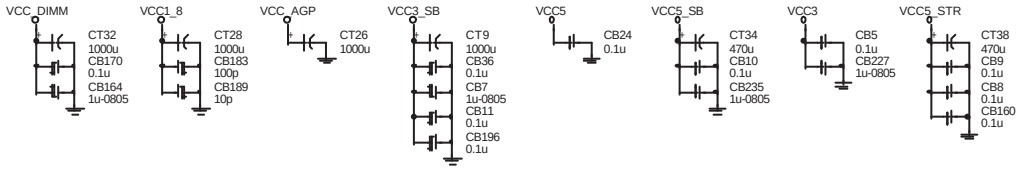



## 3.3V STANDBY POWER TRANSLATOR

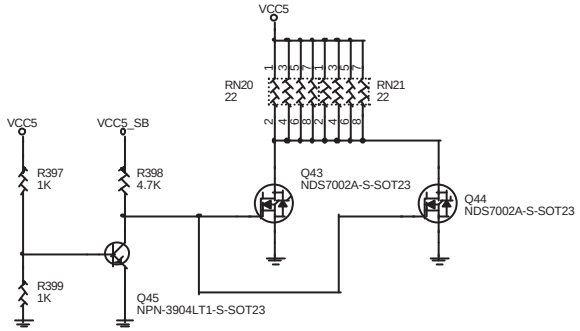
**(60mils trace / 20 mils space)**



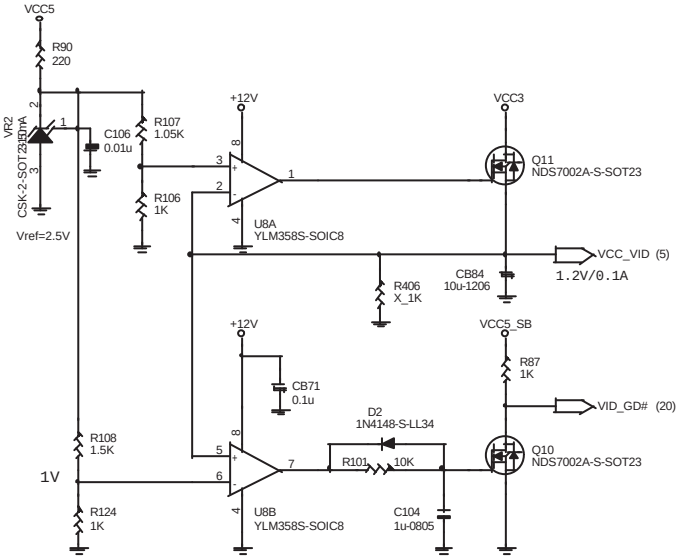

## REGULATORS OUTPUT DECOUPLING CAPACITORS



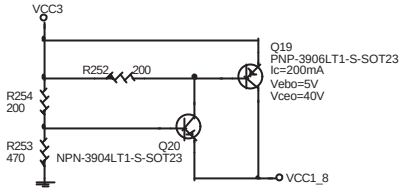

## VCC5 Discharge residual voltage on Power Off



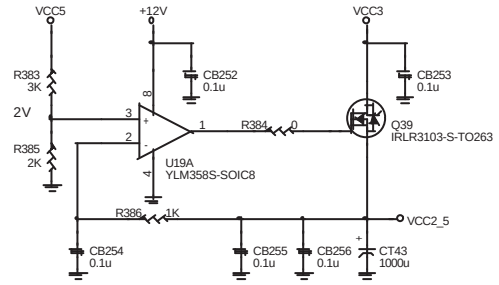

## CPU VID POWER GOOD BLOCK




## 1.8V/3.3V SEQUENCE CIRCUIT




## AGP POWER TRANSLATOR

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**MICRO-STAR**

H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang

Title: VOLTAGE REGULATOR

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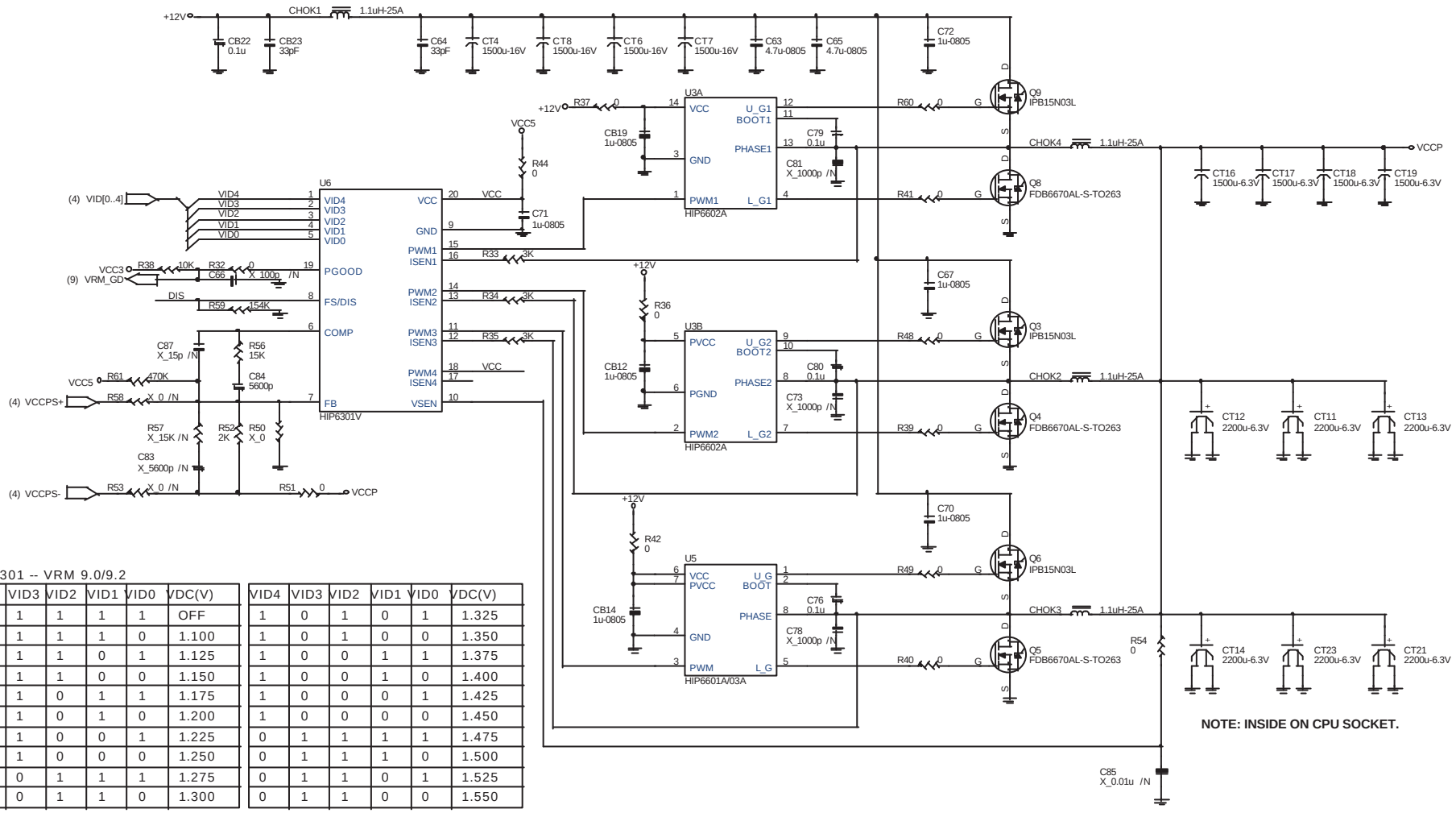


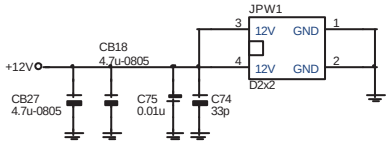

**NOTE: INSIDE ON CPU SOCKET.**

HIP6301 -- VRM 9.0/9.2

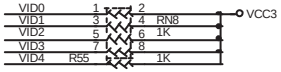
| VID4 | VID3 | VID2 | VID1 | VID0 | VDC(V) |
|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | 1 | OFF |
| 1 | 1 | 1 | 1 | 0 | 1.100 |
| 1 | 1 | 1 | 0 | 1 | 1.125 |
| 1 | 1 | 1 | 0 | 0 | 1.150 |
| 1 | 1 | 0 | 1 | 1 | 1.175 |
| 1 | 1 | 0 | 1 | 0 | 1.200 |
| 1 | 1 | 0 | 0 | 1 | 1.225 |
| 1 | 1 | 0 | 0 | 0 | 1.250 |
| 1 | 0 | 1 | 1 | 1 | 1.275 |
| 1 | 0 | 1 | 1 | 0 | 1.300 |

| VID4 | VID3 | VID2 | VID1 | VID0 | VDC(V) |
|---|---|---|---|---|---|
| 1 | 0 | 1 | 0 | 1 | 1.325 |
| 1 | 0 | 1 | 0 | 0 | 1.350 |
| 1 | 0 | 0 | 1 | 1 | 1.375 |
| 1 | 0 | 0 | 1 | 0 | 1.400 |
| 1 | 0 | 0 | 0 | 1 | 1.425 |
| 1 | 0 | 0 | 0 | 0 | 1.450 |
| 0 | 1 | 1 | 1 | 1 | 1.475 |
| 0 | 1 | 1 | 1 | 0 | 1.500 |
| 0 | 1 | 1 | 0 | 1 | 1.525 |
| 0 | 1 | 1 | 0 | 0 | 1.550 |

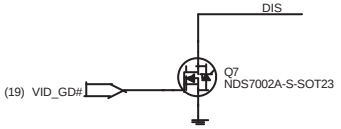
## ATX12V POWER CONNECTOR

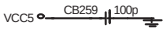



## VID PULL-UP RESISTORS




## PWM GOOD




MSI **MICRO-STAR**
H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang

Title: VRM9.2 INTERSIL HIP6301

Size | Document Number: MS-6514 | Rev: 0B

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# Jumper Setting & Connector Setting

| Jumper | Description | |
|---|---|---|
| J1 | BIOS function | |
| 1-2 | Normal | (Default) |
| 2-3 | Configuration Mode | |
| REMOVED | Recovery | |
| JBAT1 | Clear CMOS | |
| 1-2 | Normal | (Default) |
| 2-3 | Clear CMOS | |

| Rear Connector | Description |
|---|---|
| KBMS1 | PS/2 Keyboard and PS/2 mouse |
| USB1 | 4 Ports USB |
| COM1 | Serial Port |
| LPT | Parallel Port |
| L_OUT | Audio Line Out Phone Jack |
| L_IN | Audio Line In Phone Jack |
| MIC_IN | Audio Mic In Phone Jack |

| Slot | Description |
|---|---|
| AGP1 | AGP Slot |
| PCI1 | PCI Slot1 |
| PCI2 | PCI Slot2 |
| PCI3 | PCI Slot3 |

| Connector | Description |
|---|---|
| U3 | Intel mPGA478-B CPU |
| IDE1 | Primary IDE |
| IDE2 | Secondary IDE |
| JTAG | Intel Debug Port |
| BAT1 | Battery |
| CD_IN1 | CDROM Header (ATAPI) |
| U10 | BIOS |
| DIM1 | SDRAM DIMM1 |
| DIM2 | SDRAM DIMM2 |
| DIM3 | SDRAM DIMM3 |
| FDD1 | Floppy |
| USB3 | USB Internal Front Header |
| POWER | ATX Power |
| C_FAN | CPU Fan Header |
| S_FAN | System Fan Header |
| P_FAN | ATX PSU Fan Header |
| F_P1 | Front Panel |
| Pin1 | Email LED+ |
| Pin2,6,13,16,20 | GND |
| Pin3 | Suspend LED+ |
| Pin4 | Suspend LED- |
| Pin5 | Hard LED+ |
| Pin7 | Power LED- |
| Pin8 | Speaker+ |
| Pin9 | Key |
| Pin10,12 | NC |
| Pin11 | Power LED+ |
| Pin14 | Speaker- |
| Pin15 | Power Button |
| Pin17 | LAN LED+ |
| Pin18 | LAN LED- |
| Pin19 | Reset Button |
| JPW1 | ATX12V Power |

**POWER CONSUMPTION**

| | VCCP | VCC_AGP | VCC1_8 | VCC3_DIMM | VCC3 | VCC5 | VCC5_SB | +12V | -12V |
|---|---|---|---|---|---|---|---|---|---|
| CPU | 69.0A | 0 | 0 | 0 | 0 | 0 | 0 | NOTE4 | 0 |
| PMCH | 2.4A | NOTE1 | 0.2A | 2.0A | 0 | 0 | 0 | 0 | 0 |
| ICH2 | 0 | 0 | NOTE3 | 0 | NOTE3 | 0 | NOTE3 | 0 | 0 |
| CY28324 | 0 | 0 | 0 | 0 | ? | 0 | 0 | 0 | 0 |
| AD1885 | 0 | 0 | 0 | 0 | 21mA | 50mA | 0 | 0 | 0 |
| FWH -SST | 0 | 0 | 0 | 0 | 15mA | 0 | 0 | 0 | 0 |
| W83627HF | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 |
| HIP6301 | 0 | 0 | 0 | 0 | 0 | | | | 0 |
| HIP6602A | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 |
| HIP6601A | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 |
| SC1547 | 0 | 0 | 0 | 0 | 0 | 0 | | | 0 |
| DIMM | 0 | 0 | 0 | NOTE2 | 0 | | NOTE2 | 0 | 0 |
| AGP | 0 | 8.0A | 0 | 0 | 6.0A | 2.0A | ? | 1.0A | 0 |
| PCI | 0 | 0 | 0 | 0 | 7.6A | 5.0A | 0 | 500mA | 100mA |
| USB | 0 | 0 | 0 | 0 | 0 | | 0 | | 0 |
| USB HUB | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| FAN | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| TTL | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| AMPLIFIER | 0 | 0 | 0 | 0 | | | 0 | 0 | 0 |
| OTHER | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 |

NOTE1 --- MCH
VCC_AGP = VCC1_5 (1.5A) + VCC_AGP (0.37A)

NOTE2 --- DIMM
S0 STATE --- 2.0A * 3 = 6.0A ---> VCC3
S1/S3 STATE --- 200mA * 3 = 600mA ---> VCC3_SB
VCC3_SB --> 600mA*3.3V/5V=396mA --> VCC5_SB

NOTE3 --- ICH2

| Power | S0 | S1 | S3/S4/S5 |
|---|---|---|---|
| 1.8V | 300mA | 100mA | N/A |
| 1.8V_LAN | 36mA | 28mA | N/A |
| VCC1_8SB | 45mA | 30mA | 7mA |
| VCC3 | 410mA | 5mA | N/A |
| VCC3+562ET | 230mA | 210mA | N/A |
| VCC3_SB | 25mA | 0.6mA | N/A |

VCC3_SB =
VCC1_8SB =
VCC5_SB = VCC3_SB + VCC1_8SB

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**MICRO-STAR**
H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang

Title: JUMPER SETTING

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# GPIO Setting

## ICH2

| GPIO | Pin | Default | Directory |
|---|---|---|---|
| GPIO0/REQA# | M3 | GPI0 | Input |
| GPIO16/GNTA# | L2 | GPIO16 | Output |
| GPIO1/REQB#/REQ5# | L3 | REQ5# | Input |
| GPIO17/GNTA#/GNT5# | L4 | GNT5# | Output |
| GPIO11/SMBALERT# | AB17 | SMBALERT# | Input |
| GPIO12 | W14 | EXTSMI# | Input |
| GPIO13 | AB15 | SIO_PME# | Input |
| GPIO21 | L1 | CPU_FAN | Output |
| GPIO22 | B14 | FDD | Output |
| GPIO23 | A14 | NC | Output |
| GPIO27 | AB14 | Sleep LED | Output |
| GPIO28 | AA14 | NC | Output |
| GPIO2/PIRQE# | N3 | PIRQE# | Input |
| GPIO3/PIRQF# | N2 | PIRQF# | Input |
| GPIO4/PIRQG# | N1 | PIRQG# | Input |
| GPIO5/PIRQH# | M4 | PIRQH# | Input |
| GPIO6 | Y11 | PD_DET | Input |
| GPIO7 | AA11 | SD_DET | Input |
| GPIO8 | Y14 | USB_SENS | Input |
| GPIO18 | A15 | Power LED | Output |
| GPIO19 | D14 | NC | Output |
| GPIO20 | C14 | NC | Output |
| GPIO24 | V21 | NC | Output |
| GPIO25 | W15 | Power LED | Output |

## SIO

| GPIO | Pin | Default | Directory |
|---|---|---|---|
| JB11/GP10 | 32 | NC | Output |
| JB12/GP11 | 33 | NC | Output |
| JB21/GP12 | 34 | NC | Output |
| JB22/GP13 | 35 | NC | Output |
| JX1/GP14 | 36 | NC | Output |
| JY1/GP15 | 37 | NC | Output |
| JX2/GP16 | 38 | NC | Output |
| JY2/GP17 | 39 | NC | Output |
| GP20/P17 | 41 | GP20L | Input |
| MIDI_IN/GP25 | 46 | NC | Output |
| MIDI_OUT/GP26 | 47 | NC | Output |
| FAN_CTL1/GP33 | 55 | FAN_CTR1 | Output |
| FAN_CTL2/GP32 | 54 | FAN_CTR2 | Output |
| FAN_SEN1/GP31 | 52 | FAN_SEN1 | Input |
| FAN_SEN2/GP30 | 51 | FAN_SEN2 | Input |
| LED1/GP60 | 48 | PWR_LED | Output |
| LED2/GP61 | 49 | SUS_LED | Output |
| SYSOPT/GP24 | 45 | SIO_ADDR | Input |
| IO_SMI#/GP27 | 50 | EXTSMI# | Output |
| IO_PME#/GP42 | 17 | SIO_PME# | Output |
| DDRC/GP43 | 28 | NC | Output |
| KBRST#/GP36 | 63 | KB_RST# | Output |
| GA20/GP37 | 64 | A20GATE# | Output |
| DTR#2/GP57 | 100 | NC | Output |
| RTS#/GP55 | 98 | NC | Output |
| TXD2/GP53/IRTX | 96 | NC | Output |
| DSR#2/GP54 | 97 | NC | Output |
| DCD#2/GP51 | 94 | NC | Output |
| CTS#2/GP56 | 99 | NC | Output |
| RXD2/GP52/IRRX | 95 | NC | Output |
| RI#2/GP50 | 92 | NC | Output |
| IRTX/GP35 | 62 | GP35 | Output |
| IRRX/GP34 | 61 | FWH_WP | Output |


MICRO-STAR
H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang

Title: GPIO SETTING
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**Revision Initial ver: 0AE0 on 03/22/00**

Schematic Initial Revision 0AE0.

**Revision change list from ver: 0AE0 to ver: 0AE2 on 04/13/2001**

Sheet 1: Modify Cover Sheet description.
Sheet 2: Add H/W Monitoring Block.
Sheet 3: Removed two damping resistors on PD_LED and SD_LED.
Sheet 9: Remove one 1N5817 to support old SIO Vbat signal.
Sheet 10: Add GP35 signal to support P_LED signal on pin7 on F_P3.
Sheet 11: Add crystal circuits to support codec by option for customer request.
Sheet 17: Change USB1 all signals for customer request.
Sheet 18: Modify some block for customer request, detail list on below:
(1) Modify IDE_LED block to decrease LED current on no use.
(2) Modify PLED1 Block to decrease LED current on no use.
(3) Removed SUS_LED block to simply circuit.
(4) Modify ATX PSU FAN Block.
(5) Change P_LED from GP0 signal to GP35 signal for simple circuit.
Sheet 19: Change VCC5 to VCC5_SB on pin12 on U16.
Sheet 21: Modify Jumper and Connector description.
Sheet 22: Modify SIO GPIO Ports description.
Sheet 23: Add Revision 0AE2 changed item.

**Revision change list from ver: 0AE2 to ver: 0A on 04/17/2001**

Rename all components reference numbers.
Sheet 11: C37 change from GNDF to GND.

**Revision change list from ver: 0A to ver: 0A1 on 05/07/2001**

Sheet 3: Change CY28323 to CY23834, detail list on below:
(1) Removed R74,R75,R77,R78.
(2) Add R72,R81
Sheet 4: Remove ITP port, Removed JTAG1,R221,R109,R215,R219,R214,R216,R217,R220,R218,R222.
Sheet 5: Add SP cap on CT39,CT41.
Sheet 9: Add two pull down resistors on AC_SDIN0 and AC_SDIN1.
Sheet 10: Removed R165.
Sheet 14: Add three pull up resistors on ST0 , ST1 and ST2.
Sheet 19: Modify power function, detail list on below:
(1) Change VCC3_SB from Mosfet to LDO regulator.
(2) Add VCC2_5 to VCC_AGP.
Sheet 23: Add Revision 0A1 changed item.
Sheet 24: Add AGP power Circuit Update sheet.

**Revision change list from ver: 0A1 to ver: 0B on 05/12/2001**

Sheet 5: Removed two SP caps and add four 10uF caps.
Sheet 9: PLED change from GP22 on ICH2.
Sheet 18: SUS_LED add 2n3904.
Sheet 18: Modify components, detail description below:
(1) Add TRMTRIP# to PSON# on Power for support over temperature to shut down power supply.

**Revision change list from ver: 0B to ver: 0B1 on 05/15/2001**

Sheet 3: Add R74,R75,R77,R78 resistor for support ITP port..
Sheet 4: Add ITP port relational components.
Sheet 9: Modify components, detail description below:
(1) Change label from GP22 to PWR_LED.
(2) Add two divided resistors on RTC block from VCC5_SB, and add one resistor from VCC3_SB.
Sheet 10: Removed GP35 on pin62 on U13.
Sheet 15: Modify interrupt routing on PCI slots for customer request.
Sheet 16: Add RIA to RING# on com1for support S3 state wakeup.
Sheet 18: Modify components, detail description below:
(1) Add TRMTRIP# to PSON# on Power for support over temperature to shut down power supply.
(2) Add Power LED circuit, and modify SUS_LED power from VCC5 to VCC_DIMM.
(3) Removed two resistor on ATX FAN block, and change VCC5 to +12V.
(4) Change 2kohm to 330ohm on all LED blocks.
(5) Change all LED label to mit real state.
(6) Removed Speaker block to sheet16.
Sheet 19: Modify components, detail description below:
(1) Change VCC5 to VCC5_SB on VID_GD#.
(2) Change value on R383 and R385.

**Revision change list from ver: 0B1 to ver: 0B2 on 05/15/2001**

Sheet 18: Modify components, detail description below:
(1) Add one resistor to limit current on Q23.
(2) Modify THERMTRIP# circuit and driving PWRSW.
Sheet 19: Add one pull down resistor on VCC_VID.

**Revision change list from ver: 0B2 to ver: 0B on 05/16/2001**

Sheet 18: Modify Thermtrip circuit to use thermistor resistor on MOSFET Q4 bottom side.

**Revision change list from ver: 0B to ver: 0B on 05/17/2001**

Sheet 16: Move Speaker circuit to sheet18.
Sheet 18: Move Thermtrip circuit to sheet16, and modify it.

**Revision change list from ver: 0B to ver: 0B on 05/19/2001**

Sheet 9: Modify components, detail description below:
(1) Change label from PWR_LED to GP22, and connect to FDD pin 4.
(2) GP25,GP27,GP18 connect to LED.
(3) GP19,GP20 connect to configuration Jumper.
(4) LAN_WAKE change to USB_SENS.
(5) PD_DET and SD_DET connect to GP6 and GP7.
Sheet 10: GP34 connect to FWH write protect.
Sheet 15: Modify interrupt routing and IDSEL on PCI slots for customer request.
Sheet 16: Modify components, detail description below:
(1) Add RIA to RING# on com1for support S3 state wakeup.
(2) FDD cut pin3.
(3) Removed two resistor on ATX FAN block, and change VCC5 to +12V.
(4) Keyboard and mouse swap.
Sheet 17: USB_SENS on pin1 on USB2 connect to GP8 on ICH2.
Sheet 18: Modify components, detail description below:
(1) Change FAN to mit customer spec.
(2) Change LED to mit customer spec.
Sheet 22: Modify GPIO port description.

**Revision change list from ver: 0B to ver: 0B on 05/21/2001**

Sheet 10: Del R186 and R190,repeat.
Sheet 17: Modify components, detail description below:
(1) R276,R278 change from 10ohm to 15ohm.
(2) R169,R170 change from 15ohm to 10ohm.
Sheet 18: Add R405,R428 on CPU fAN, support always ON.
Sheet 21: Change Q3,Q6 and Q9 from FCB6030L ro 15N03.
Sheet 23: Modify Revision history.

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**MICRO-STAR**

H/W Project Leader : Andy Chen
H/W Project Engineer : Prudence Wang

Title: REVISION HISTORY - 1

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