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MS-6513

Version 0A
06/21/2001 Update

INTEL (R) Brookdale Chipset
Willamette/Northwood 478pin mPGA-B Processor Schematics

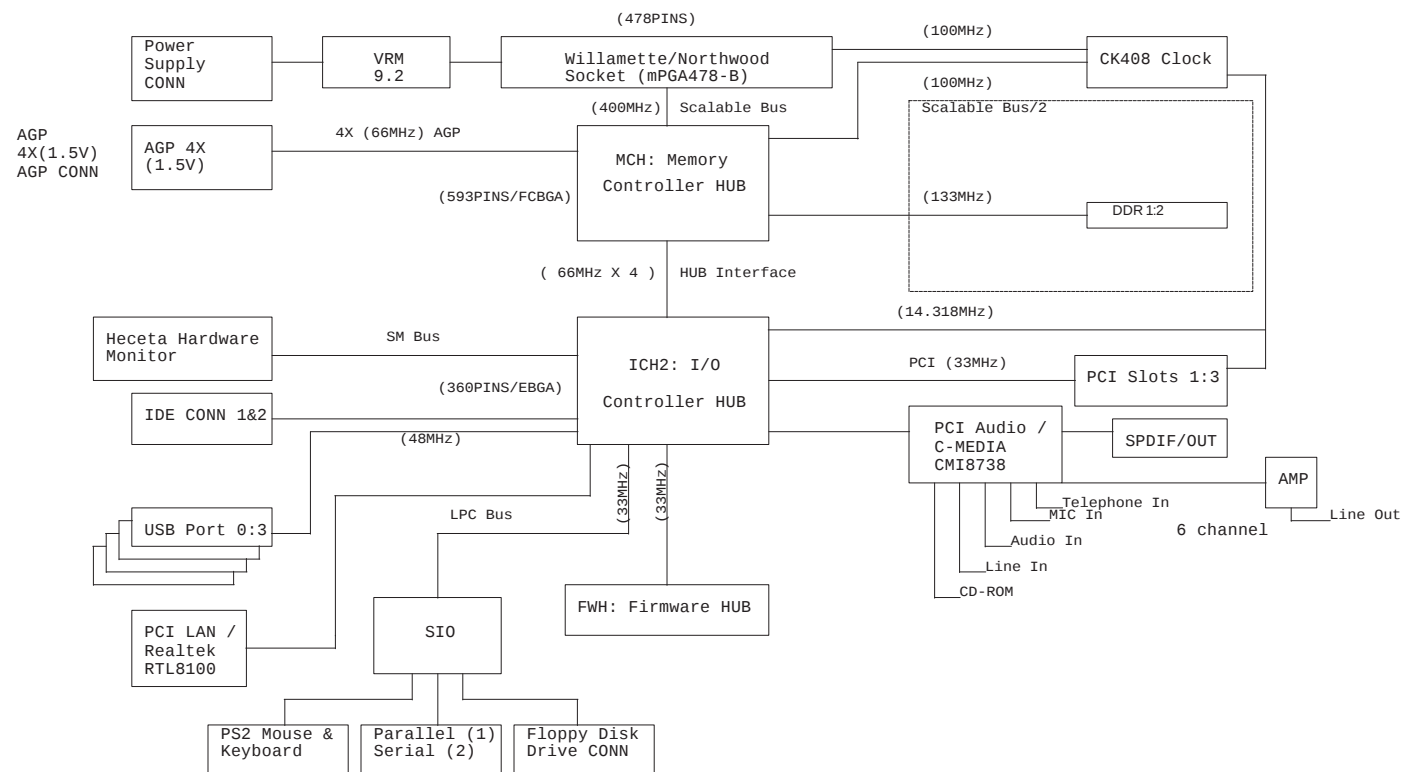
CPU:
Willamette/Northwood mPGA-478B Processor

System Brookdale Chipset:
INTEL MCH (North Bridge) +
INTEL ICH2 (South Bridge)

On Board Chipset:
BIOS -- FWH
LPC Super I/O -- W83627HF
Clock Generation -- CY28324
PCI SOUND -- C-MEDIA CMI8738

Expansion Slots:
AGP2.0 SLOT * 1
PCI2.2 SLOT * 3
PCI3 with two
masters

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General Purpose I/O Spec.

ICH2

GPIO Pin	Type	Function
GPIO 0	I	Non Connect
GPIO 1	I	Non Connect
GPIO 2~4	I	Not Implemented
GPIO 5	I	Non Connect
GPIO 6	I	Non Connect
GPIO 7	I	None
GPIO 8	I	LAN Wake Up
GPIO 9	I	AC'97 Serial Data In
GPIO 10	I	Non Connect
GPIO 11	I	Non Connect
GPIO 12	I	External SMI
GPIO 13	I	LPC PME
GPIO 14~15	I	Not Implemented
GPIO 16	O	Non Connect
GPIO 17	O	Non Connect
GPIO 18	O	Not Implemented
GPIO 19	O	Not Implemented
GPIO 20	O	Not Implemented
GPIO 21	O	Not Implemented
GPIO 22	O	Non
GPIO 23	OD	BIOS Locked/Unlocked
GPIO 24	O	Non
GPIO 25	O	Non
GPIO 26	O	Non
GPIO 27	I/O	Non
GPIO 28	I/O	non
GPIO 29~31	I/O	Not Implemented

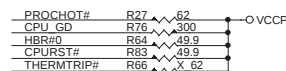
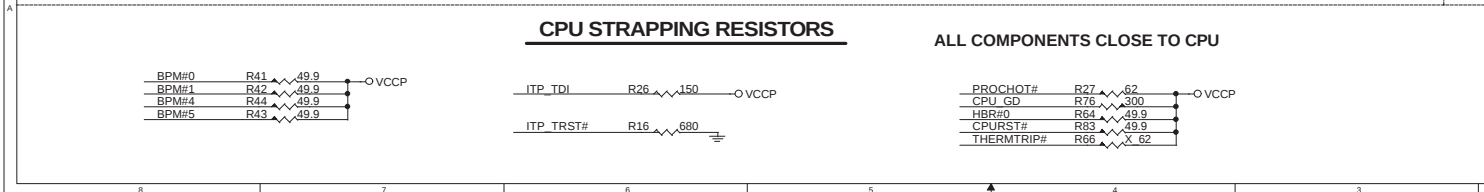
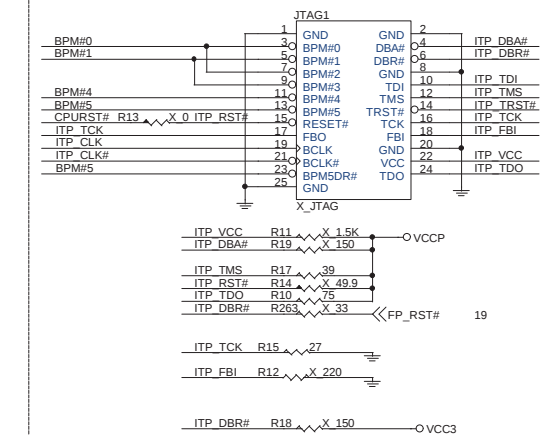
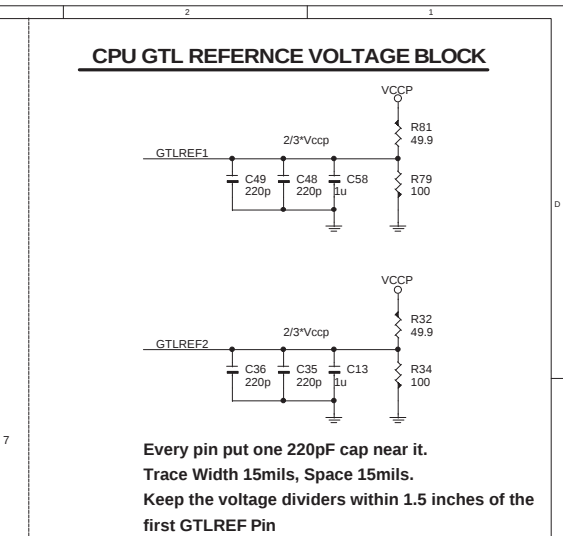
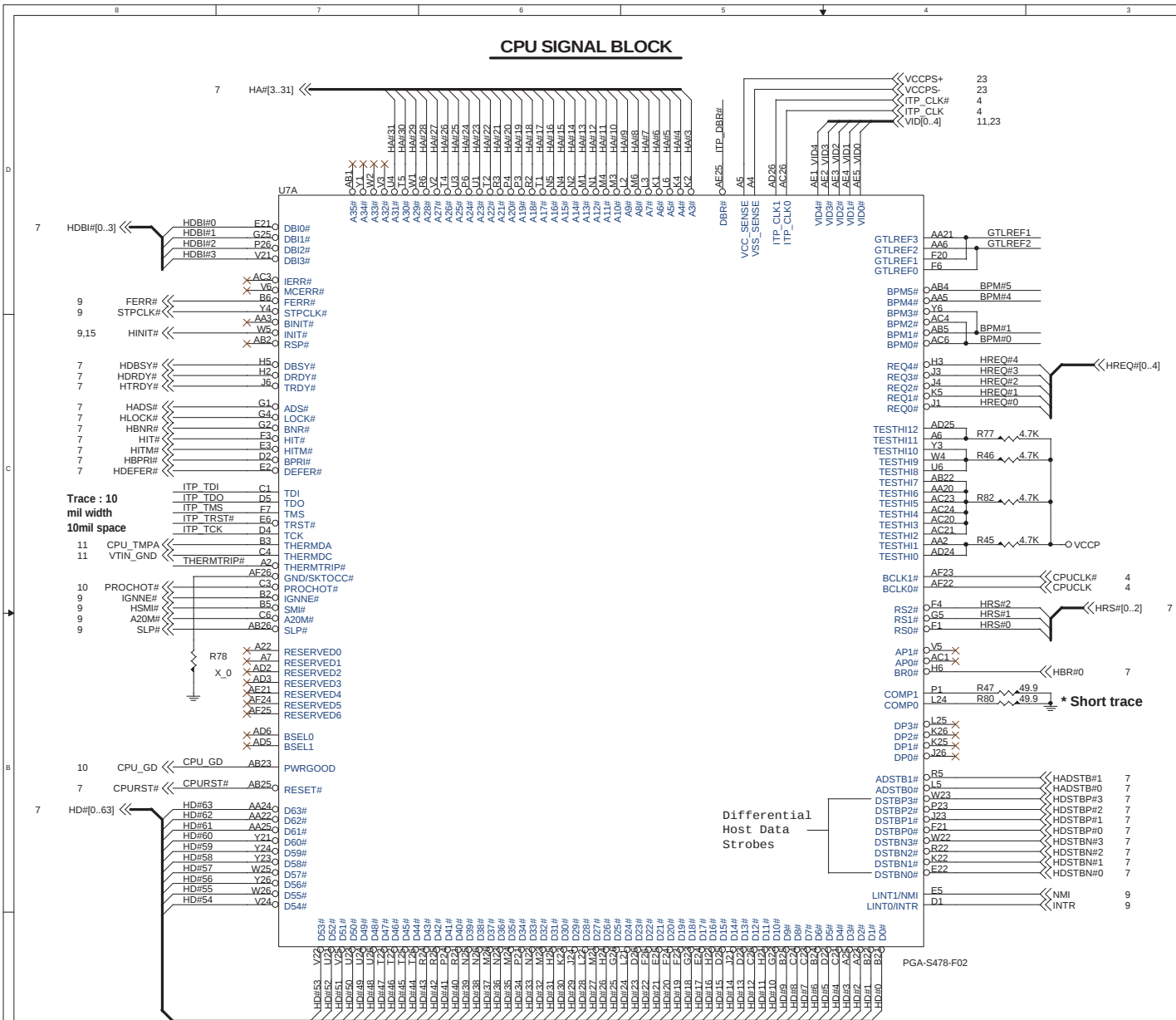
FWH

GPIO Pin	Type	Function
GPI 0	I	ATA IDE 1 Detect
GPI 1	I	ATA IDE 2 Detect
GPI 2	I	Reserved
GPI 3	I	Reserved

DLED-Super I/O

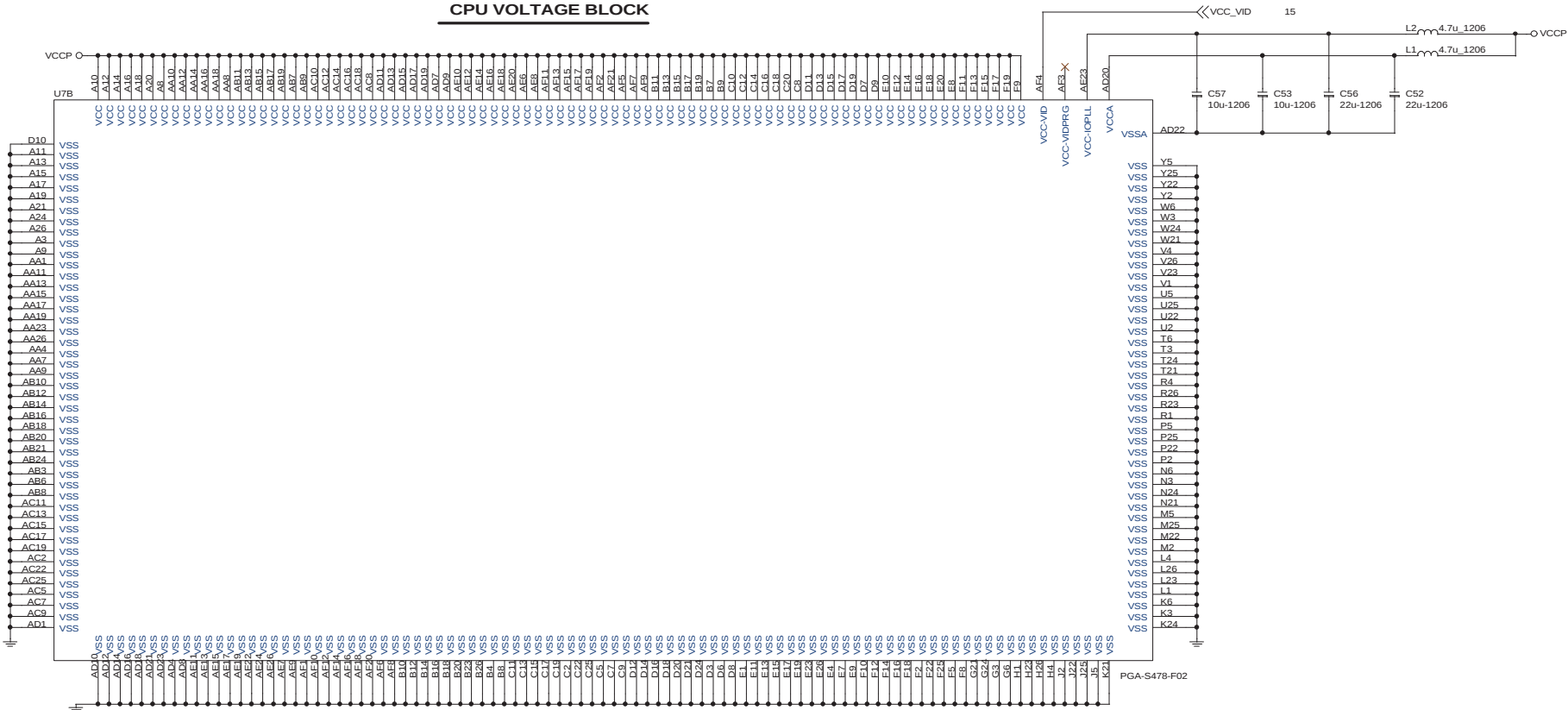
GPIO Pin	Type	Function
GP32	I/OD	Not Implemented
GP24	I/OD	Not Implemented
GP34	I/OD	Not Implemented
GP33	I/OD	Not Implemented

DEVICE	ICH INT Pin	IDSEL
PCI Slot 1	INTA# INTB# INTC# INTD#	AD16
PCI Slot 2	INTB# INTC# INTD# INTA#	AD17
PCI Slot 3	INTC# INTD# INTA# INTB#	AD18 AD19
PCI Audio	INTD#/INTE# INTA# INTB# INTC#	AD23
PCI Lan	INTC#/INTF# INTD# INTA# INTB#	AD22

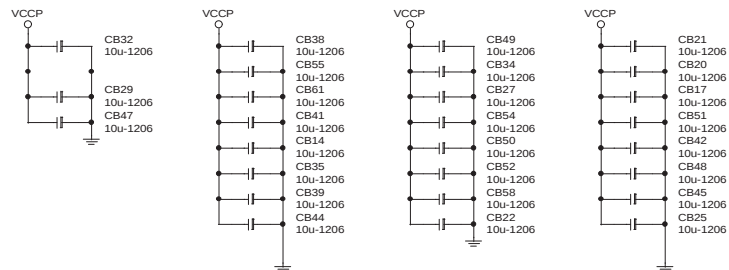


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CPU VOLTAGE BLOCK

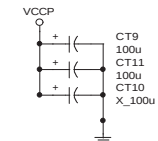


CPU DECOUPLING CAPACITORS



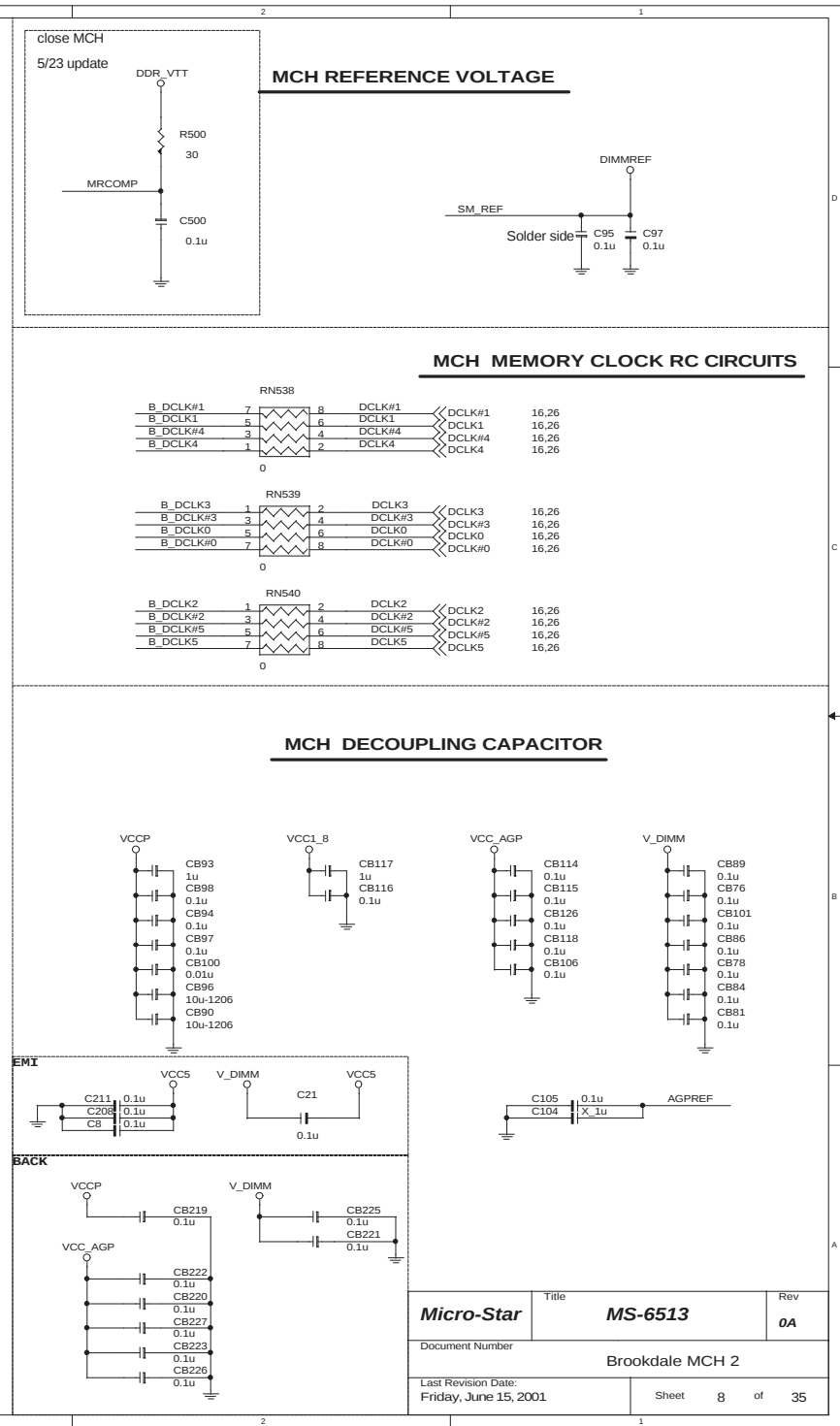
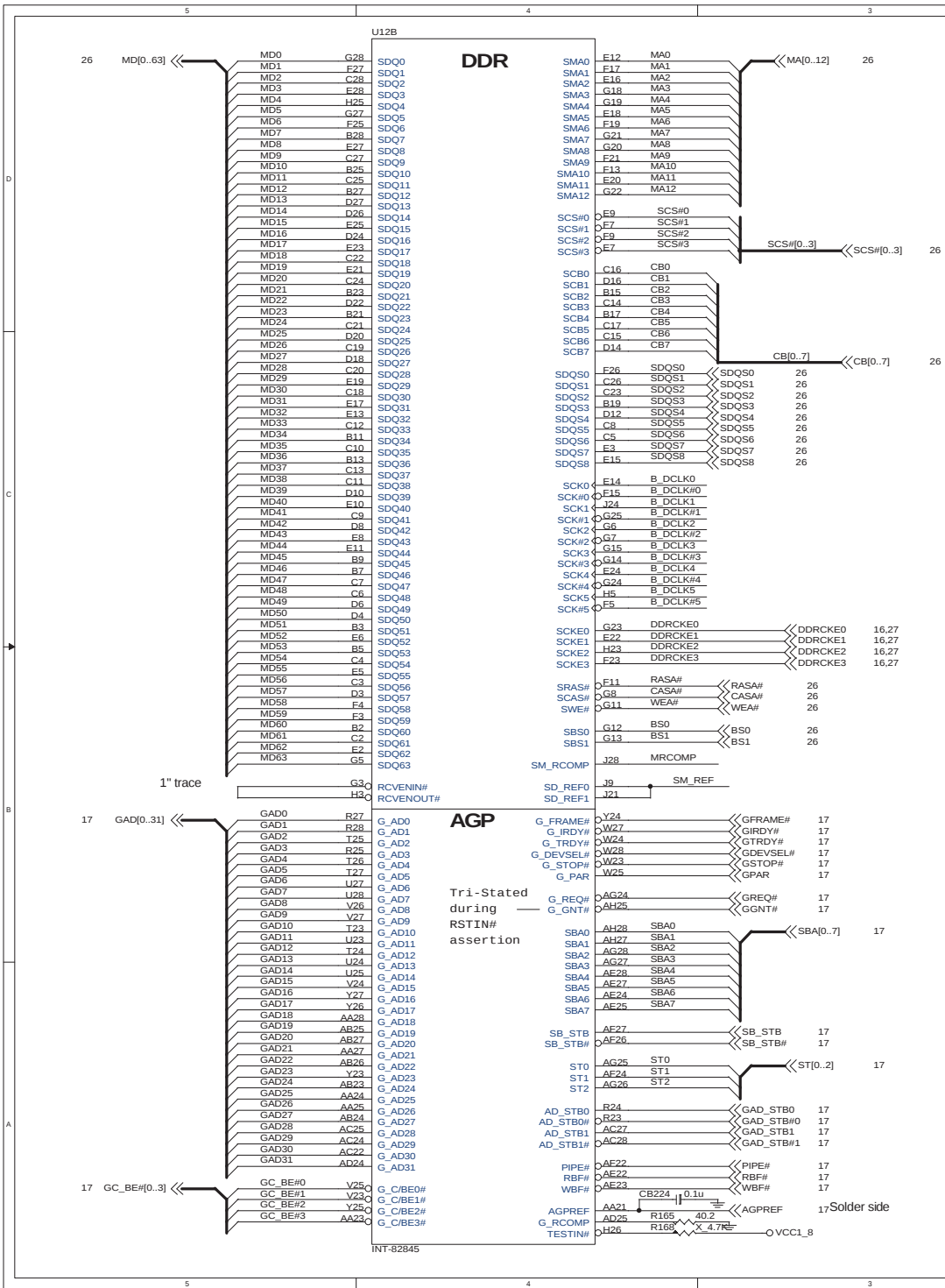
PLACE CAPS WITHIN CPU CAVITY

CPU DECOUPLING CAPACITORS

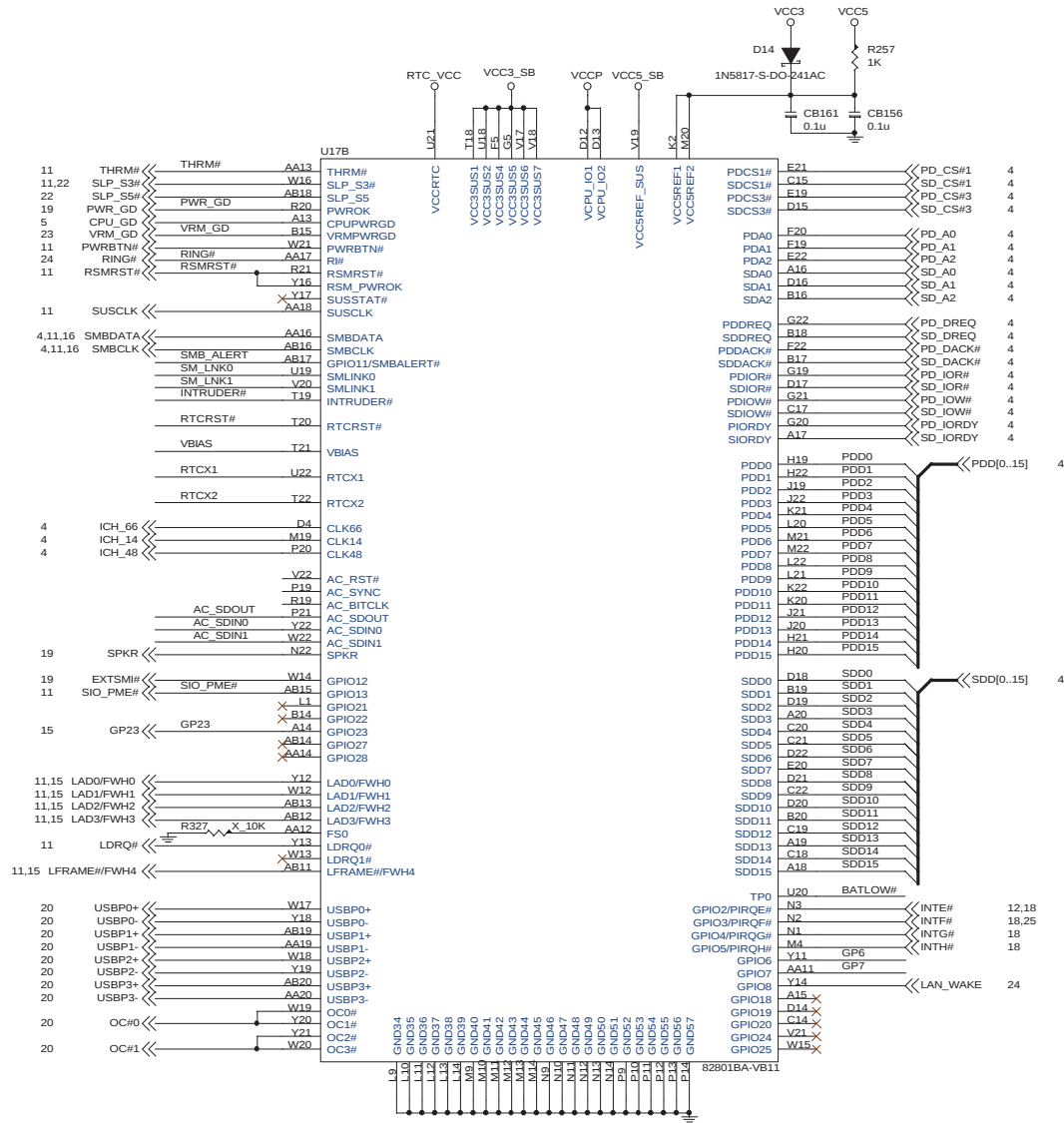


PLACE CAPS WITHIN CPU CAVITY SOLDER

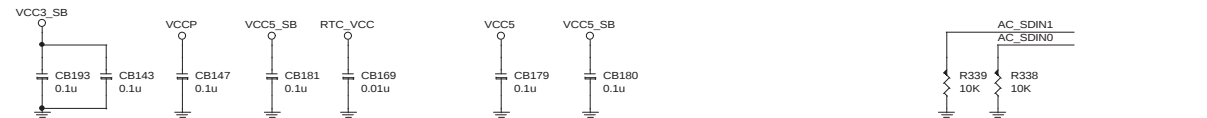
Micro-Star	Title	MS-6513	Rev
	Document Number	INTEL mPGA478-B CPU2	0A
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ICH2 ASIC / RTC / AC'97 / GPIO / LPC / USB / IDE SIGNALS

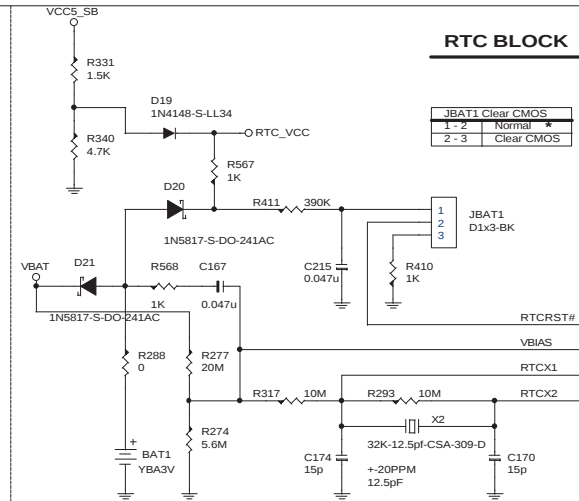


ICH2 DECOUPLING CAPACITOR

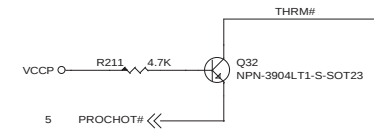


Distribute near the VCC3_SB power pin of the ICH

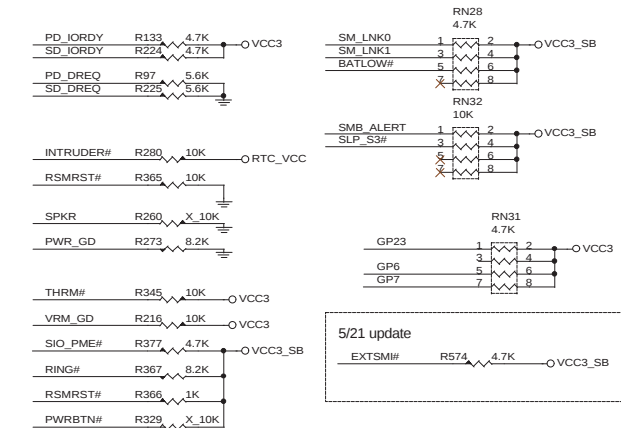
RTC BLOCK



PROCHOT BLOCK

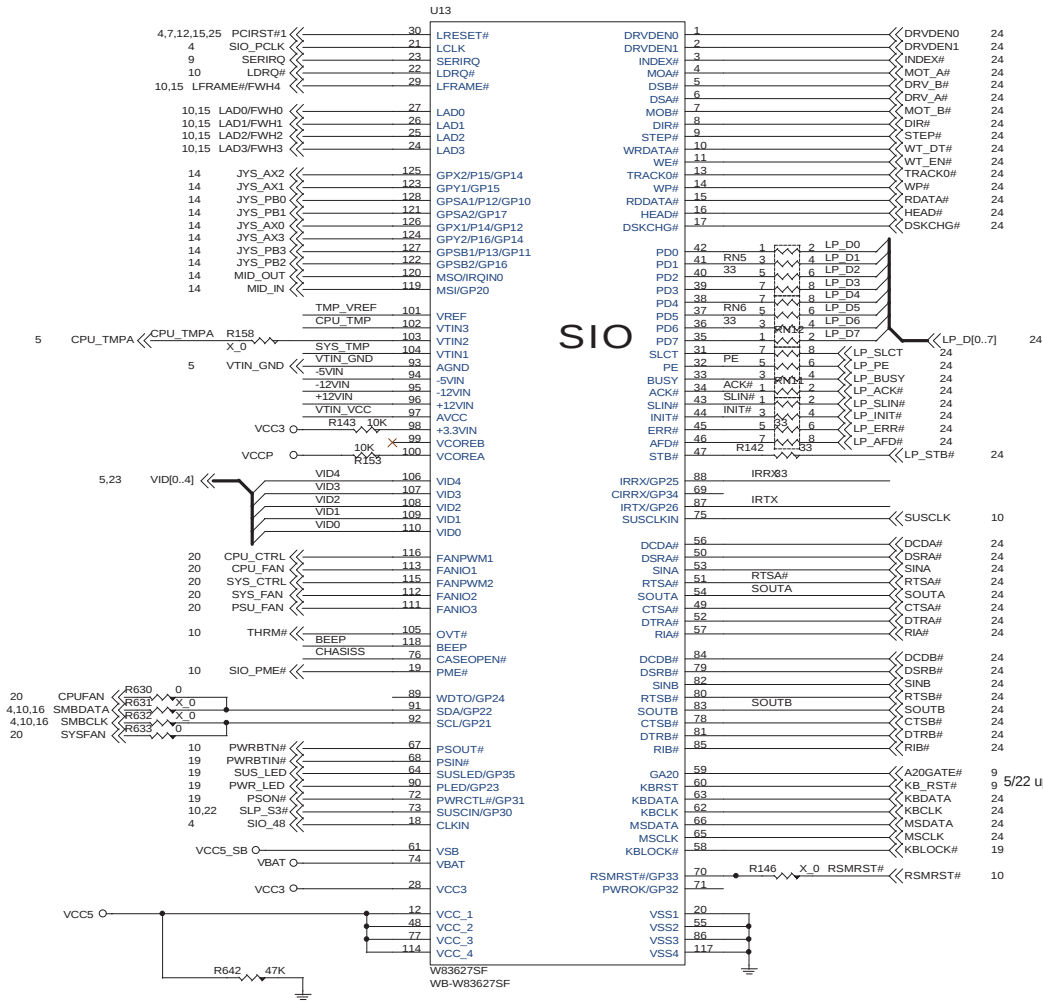


ICH2 STRAPPING RESISTORS

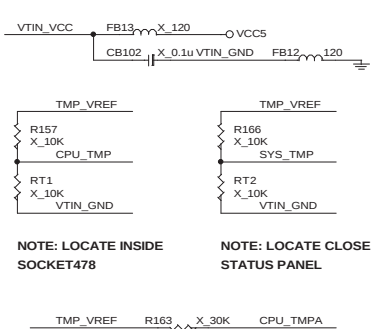


Micro-Star	Title	MS-6513	Rev	0A
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LPC SUPER I/O W83627HF

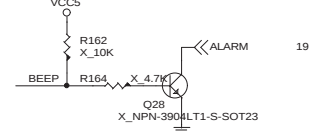


THERMAL RESISTOR BLOCK

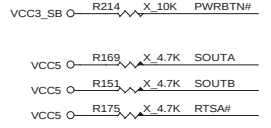


NOTE: LOCATE INSIDE SOCKET478
NOTE: LOCATE CLOSE STATUS PANEL

SPEAKER BLOCK

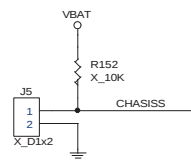


SUPER I/O STRAPPING RESISTOR

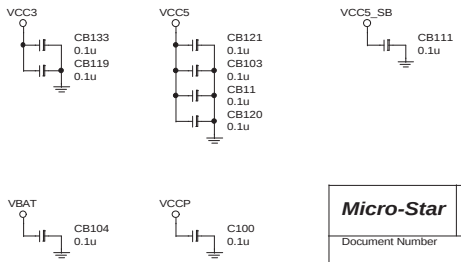


SOUTA	L: Disable KBC	H: Enable KBC
SOUTB	L: 24MHZ	H: 48MHZ
RTSA#	L: CFAD=2E	H: CFAD=4E
DTRA#	L: PNP Default	H: PNP no Default

CHASSIS INTRUSION HEADER

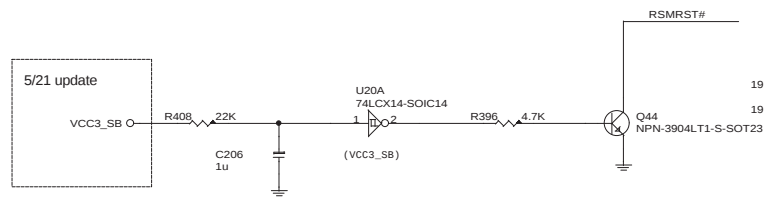


DECOUPLING CAPACITOR

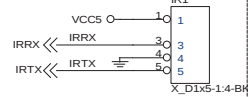


RESUME RESET CIRCUIT BLOCK

Stuff all for D Version bug

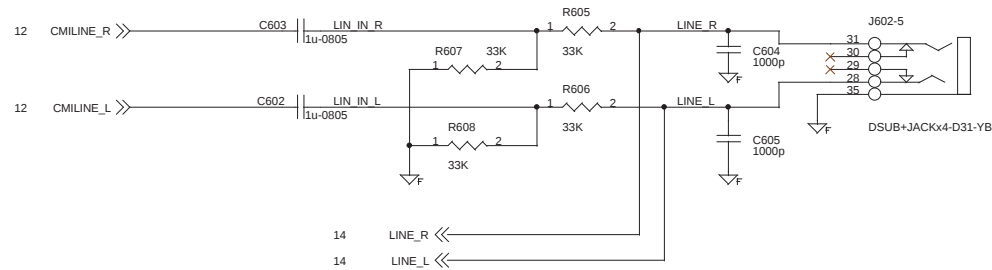


IR HEADER

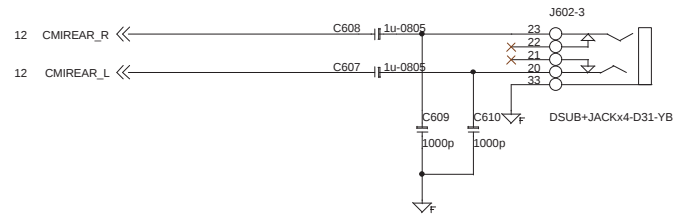


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LPC I/O W83627HF				
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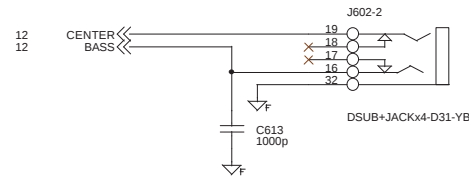
LINE-IN JACK



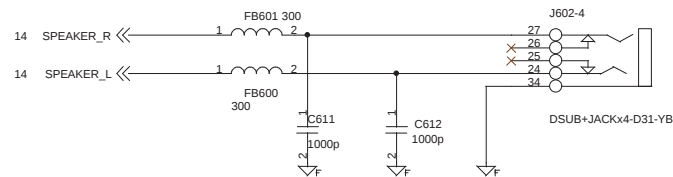
REAL JACK



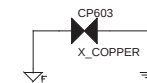
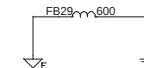
CENTER/BASS JACK



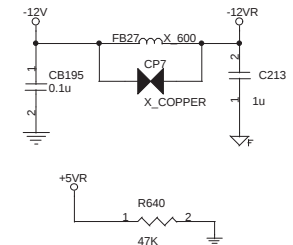
SPEAKER OUT JACK



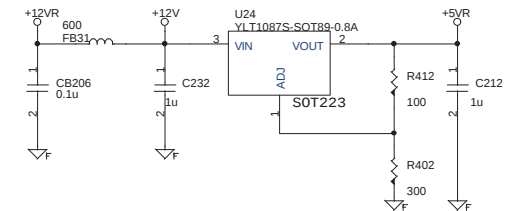
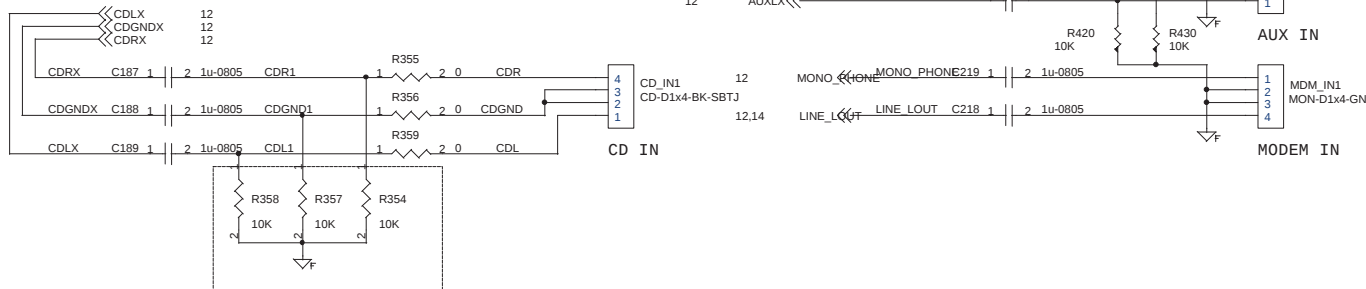
DECOUPLING CAPACITOR



AUDIO CODE REGULATORS

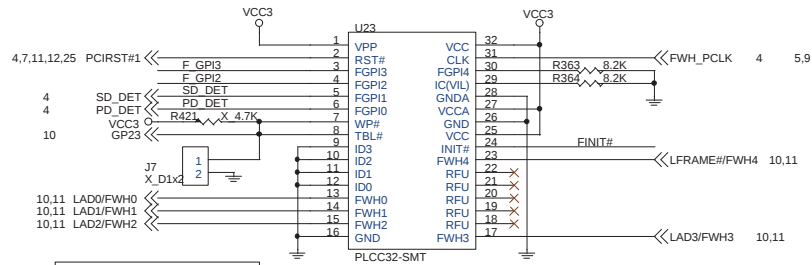


AUDIO CODE CD / AUX / MODEM IN HEADERS



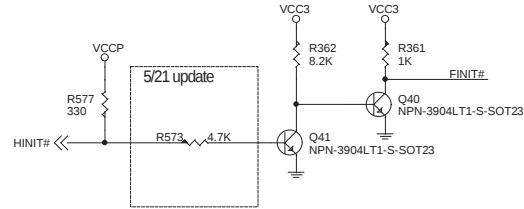
Micro-Star	Title MS-6513	Rev 0A
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Firmware Hub (FWH)

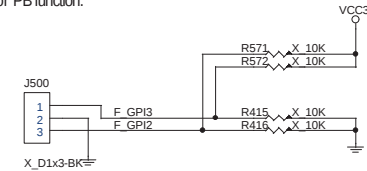


J7 BIOS Update	
SHORT	Locked
OPEN	Unlocked *

FWH INIT Signal Voltage Translation Block



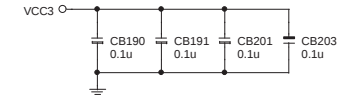
5/16 update
For PB function.



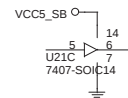
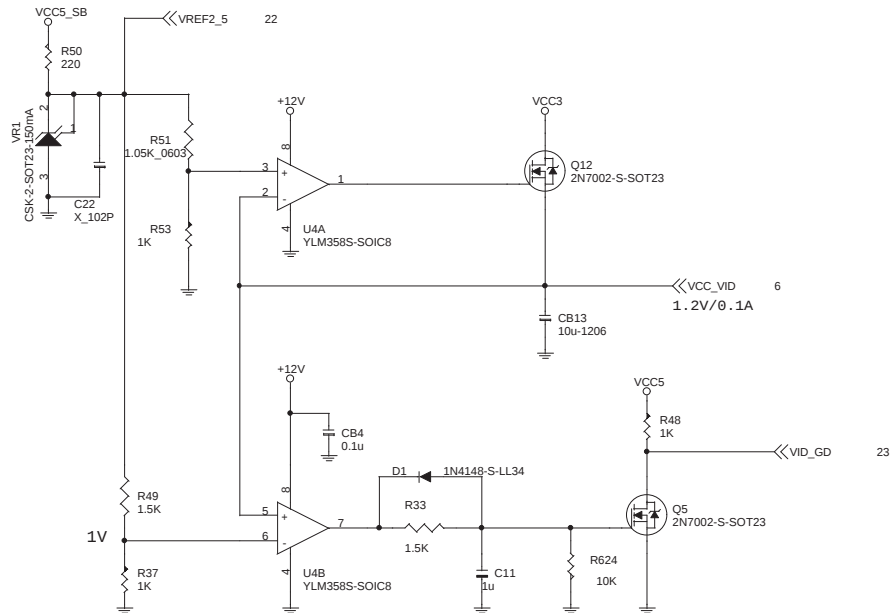
FWH RESISTORS



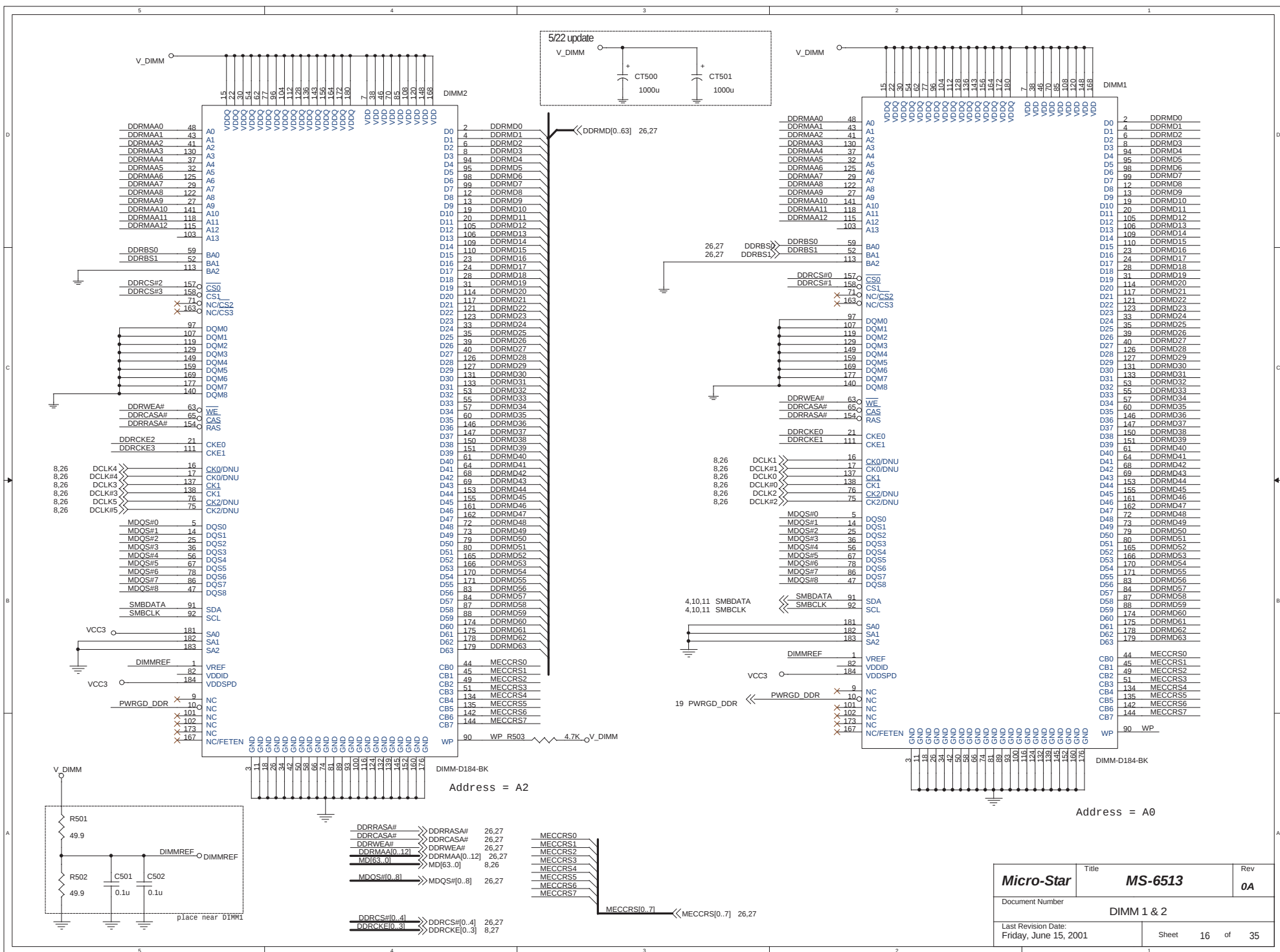
FWH DECOUPLING CAPACITORS



VCC_VID / VID_GOOD

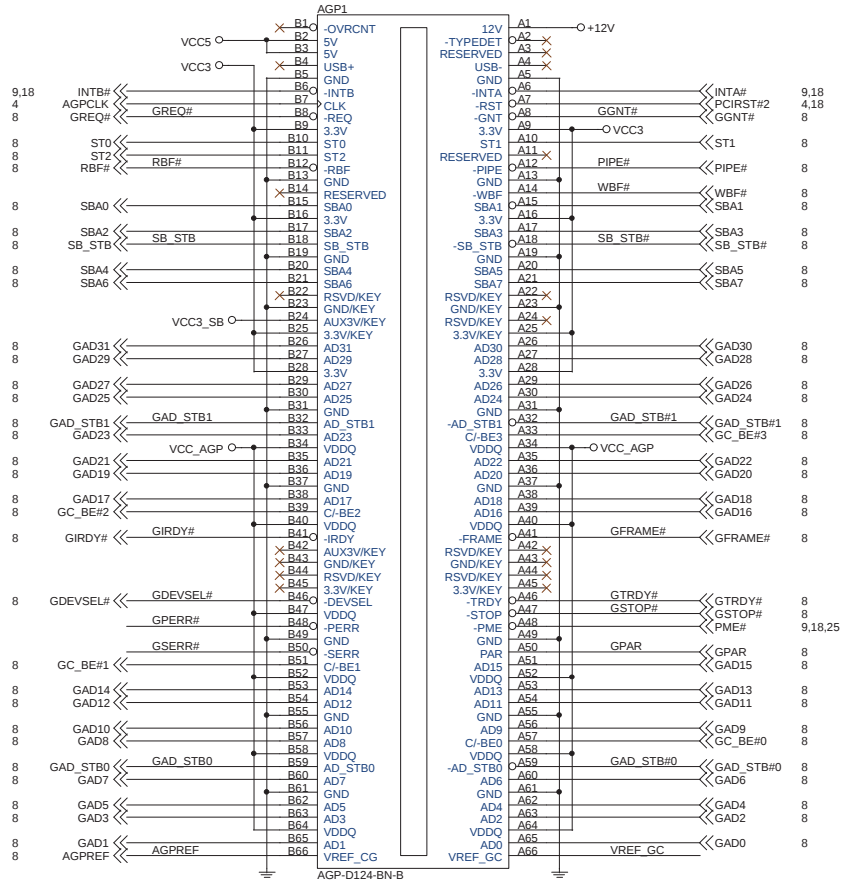


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FWH & AC'97 Enabled/Disabled control/VID				
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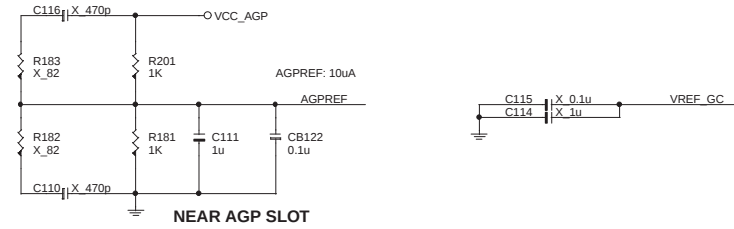


AGP UNIVERSAL 2X/4X SLOT(AGP VER:2.0 COMPLY)

VCC5 = 60mils trace / 15 mils space

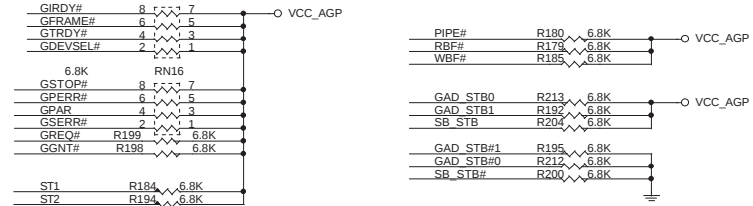


AGP SIGNAL REFERENCE CIRCUIT



NEAR AGP SLOT

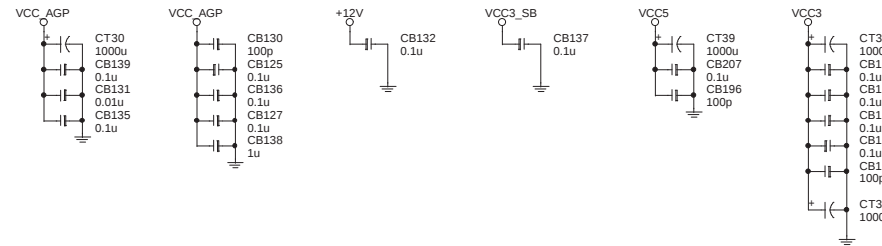
AGP TERMINATION RESISTORS



5/23 update
HI: SDRAM
LO:DDR

LESS 10MILS STUB TRACE LENGTH MUST BE FOLLOWING.
Place these resistors between PCI and AGP slot

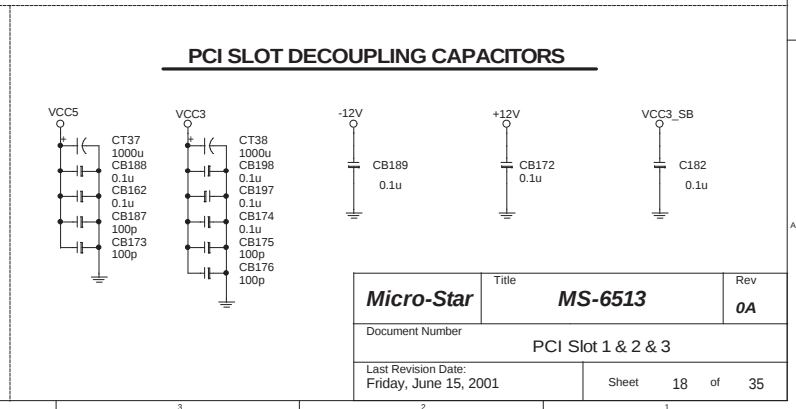
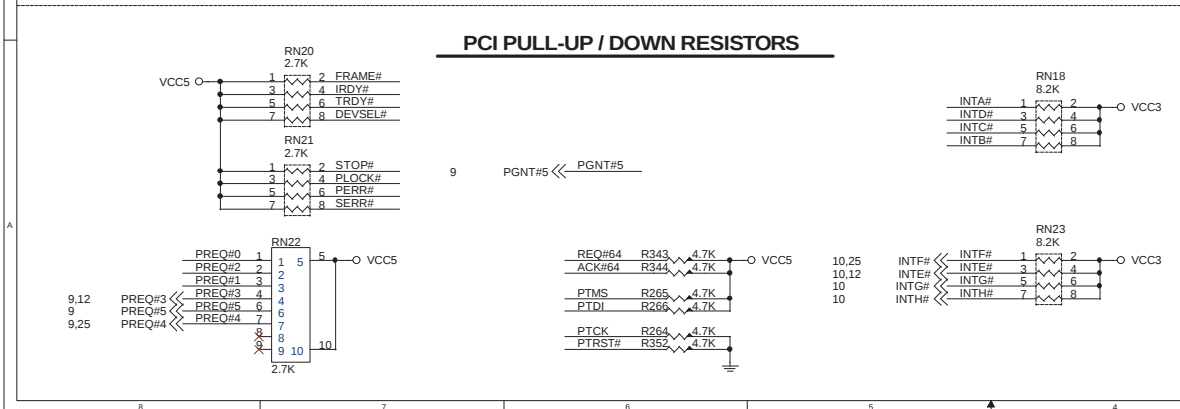
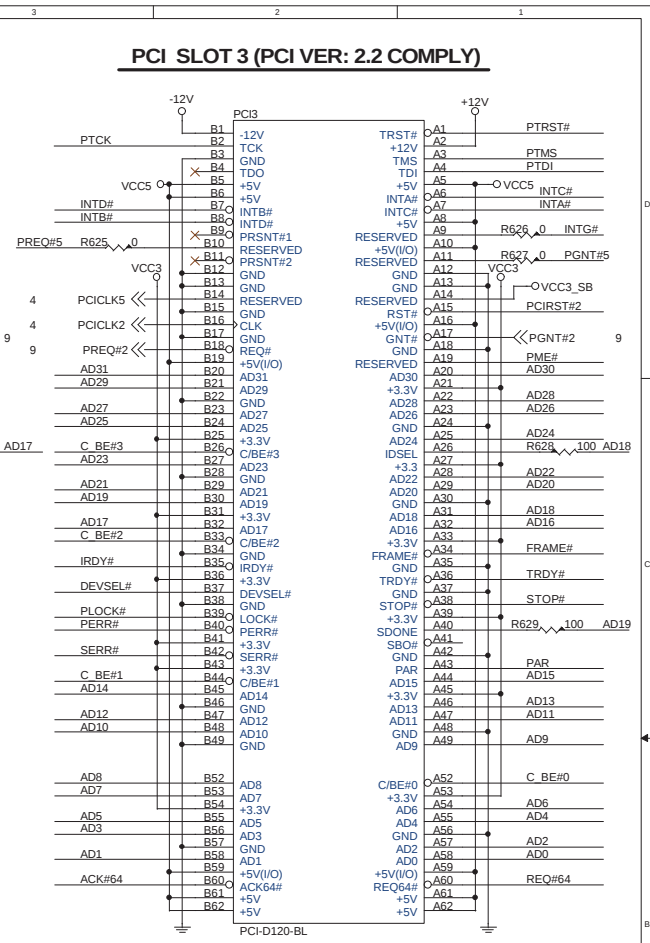
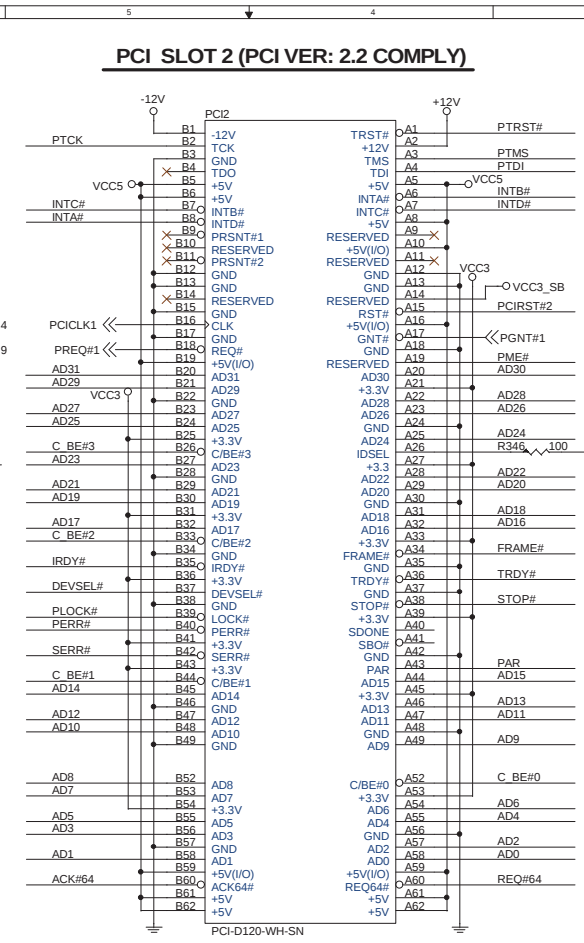
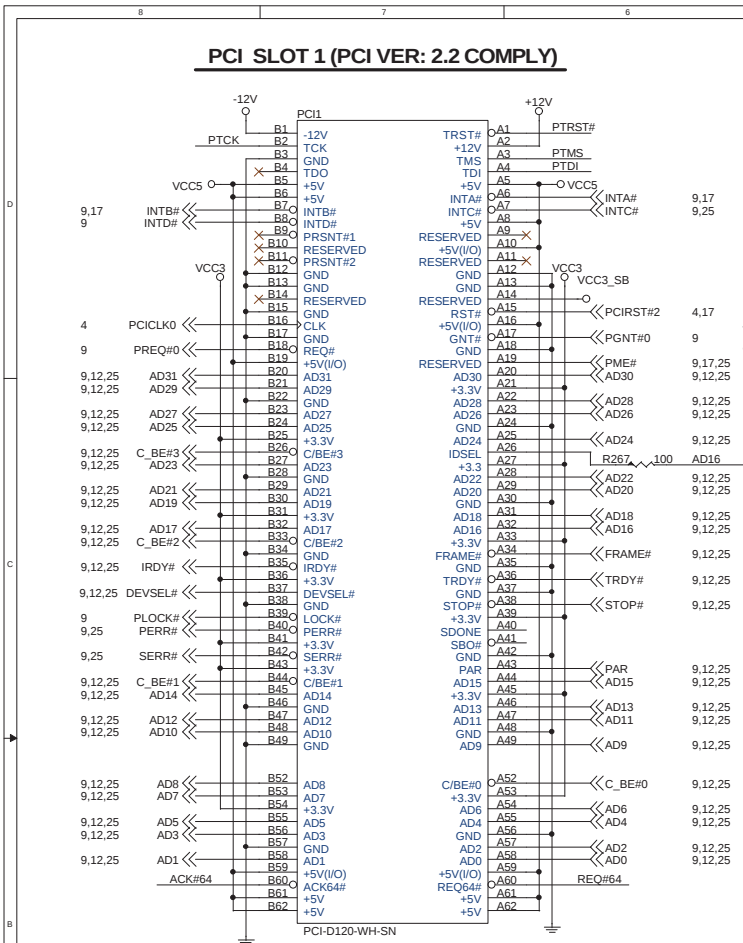
AGP SLOT DECOUPLING CAPACITORS



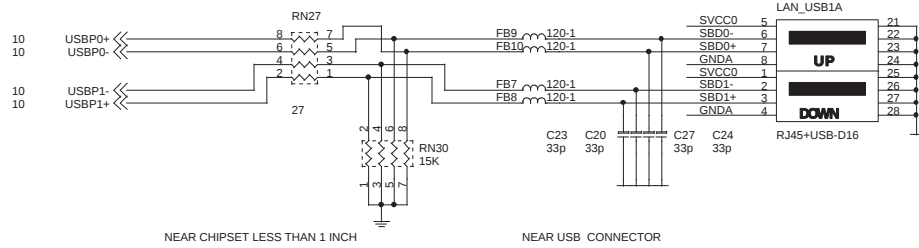
AGP Slot Imax
VCC AGP8.0A
VCC3 6.0A
VCC12 1.0A
VCC5 2.0A

INTA#
INTB#

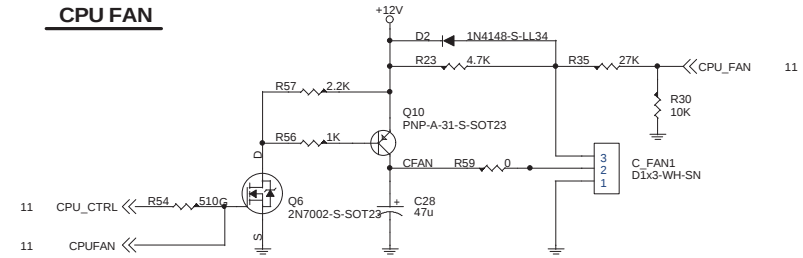
Micro-Star	Title MS-6513	Rev 0A
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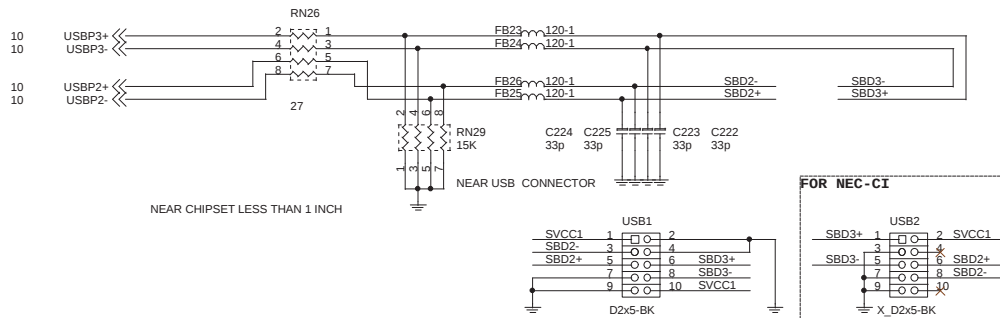
BACK PANEL USB CONNECTOR FOR USB PORT 0,1



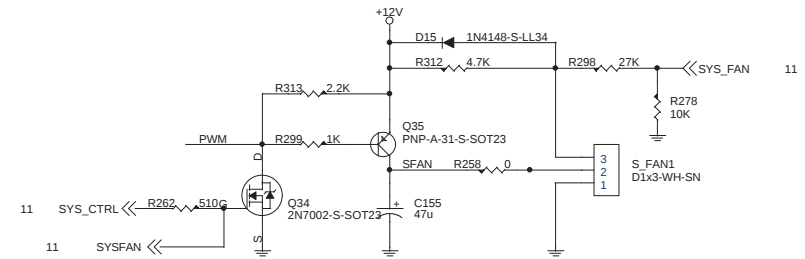
CPU FAN



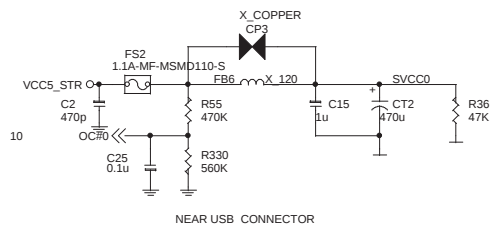
FRONT PANEL USB CONNECTOR FOR USB PORT 2,3



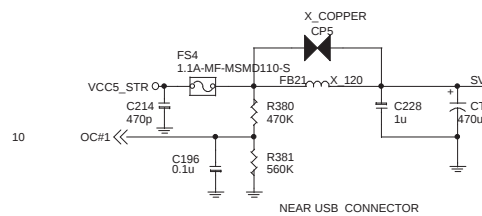
SYSTEM FAN



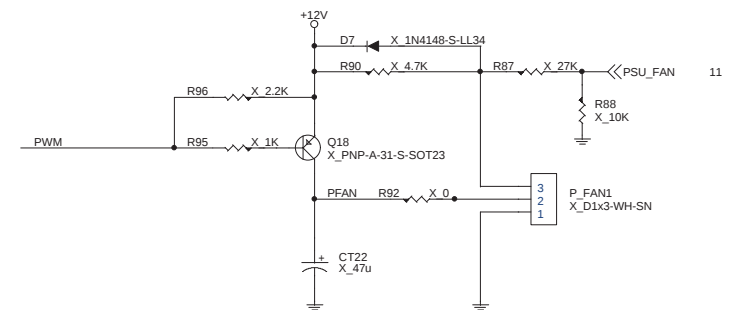
POWER CIRCUIT FOR USB PORT 0,1



POWER CIRCUIT FOR USB PORT 2,3



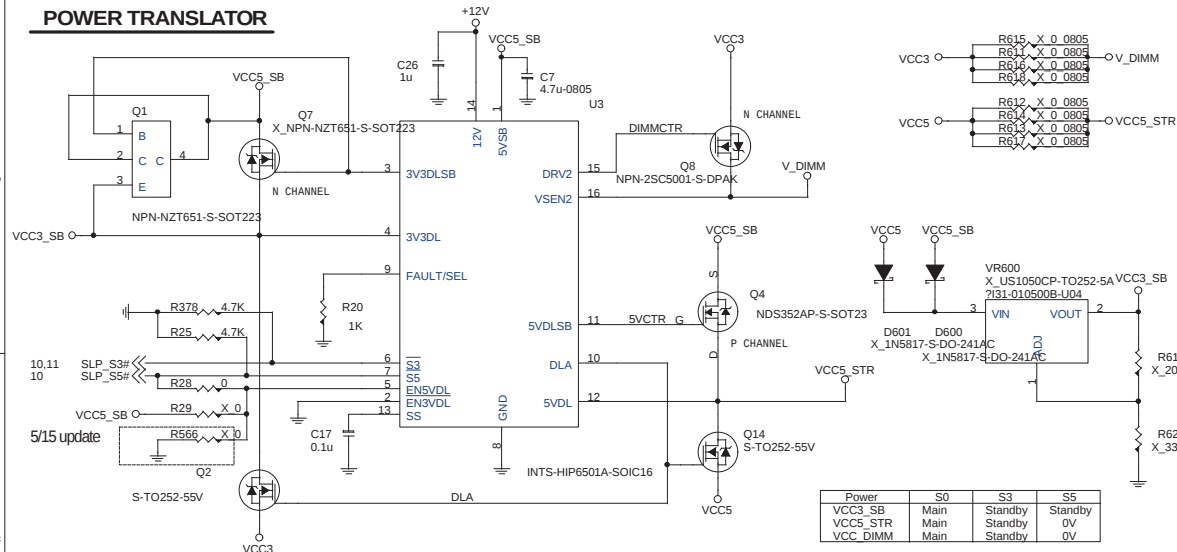
ATX PSU FAN ON/OFF CONTROL



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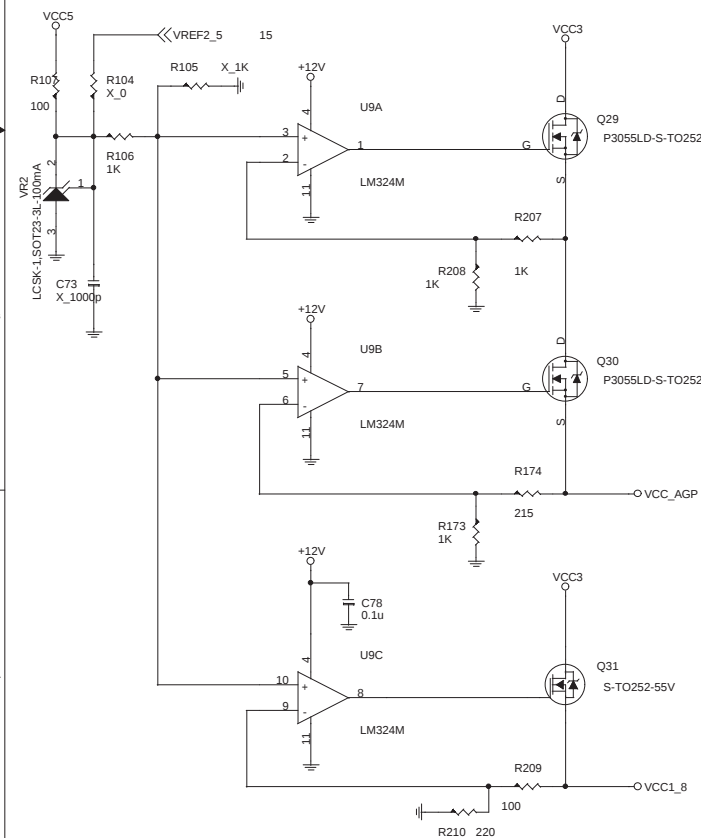
<i>Micro-Star</i>	Title	<i>MS-6513</i>	Rev
			<i>0A</i>
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RESERVED			
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POWER TRANSLATOR



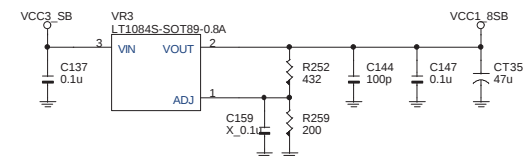
Power	S0	S3	S5
VCC3_SB	Main	Standby	Standby
VCC5_STR	Main	Standby	Standby
VCC_DIMM	Main	Standby	Standby

AGP 4X 1.5V POWER TRANSLATOR



1.8V STANDBY POWER TRANSLATOR

(40mils trace / 20 mils space)



POWER CONSUMPTION

	VCCP	VCC_AGP	VCC1_8	VCC3_DIMM	VCC3	VCC5	VCC5_SB	+12V	-12V
CPU	69.0A	0	0	2.0A	0	0	0	NOTE4	0
PMCH	2.4A	NOTE1	0.2A	2.0A	0	0	0	0	0
ICH2	0	0	NOTE3	0	NOTE3	0	NOTE3	0	0
CY28324	0	0	0	0	0	0	0	0	0
AD1885	0	0	0	0	0	0	0	0	0
FWH-SST	0	0	0	0	0	0	0	0	0
W83627HF	0	0	0	0	0	0	0	0	0
HIP6301	0	0	0	0	0	0	0	0	0
HIP6602A	0	0	0	0	0	0	0	0	0
HIP6601A	0	0	0	0	0	0	0	0	0
SC1547	0	0	0	0	0	0	0	0	0
DIMM	0	0	0	NOTE2	0	0	NOTE2	0	0
AGP	0	8.0A	0	0	6.0A	2.0A	0	1.0A	0
PCI	0	0	0	0	0	0	0	0	0
USB	0	0	0	0	0	0	0	0	0
USB HUB	0	0	0	0	0	0	0	0	0
FAN	0	0	0	0	0	0	0	0	0
TTL	0	0	0	0	0	0	0	0	0
AMPLIFIER	0	0	0	0	0	0	0	0	0
OTHER	0	0	0	0	0	0	0	0	0

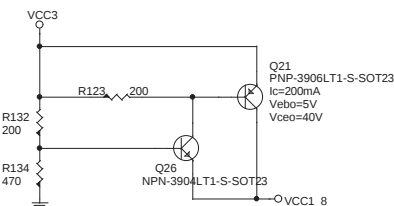
NOTE1 --- MCH
VCC_AGP = VCC1_5 (1.5A) + VCC_AGP (0.37A)

NOTE2 --- DIMM
S0 STATE --- 2.0A * 3 = 6.0A --> VCC3
S1/S3 STATE --- 200mA * 3 = 600mA --> VCC3_SB
VCC3_SB --> 600mA * 3.3V/5V = 396mA --> VCC5_SB

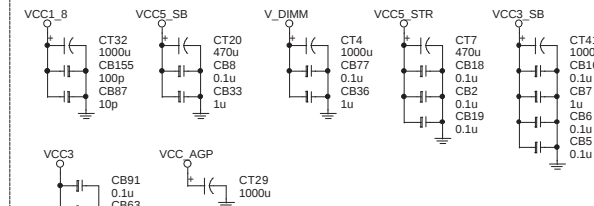
Power	S0	S1	S3/S4/S5
1.8V	300mA	100mA	N/A
1.8V LAN	36mA	28mA	N/A
VCC1_8SB	45mA	30mA	7mA
VCC3	410mA	5mA	N/A
VCC3+562ET	230mA	210mA	N/A
VCC3_SB	25mA	0.6mA	N/A

VCC3_SB =
VCC1_8SB =
VCC5_SB = VCC3_SB + VCC1_8SB

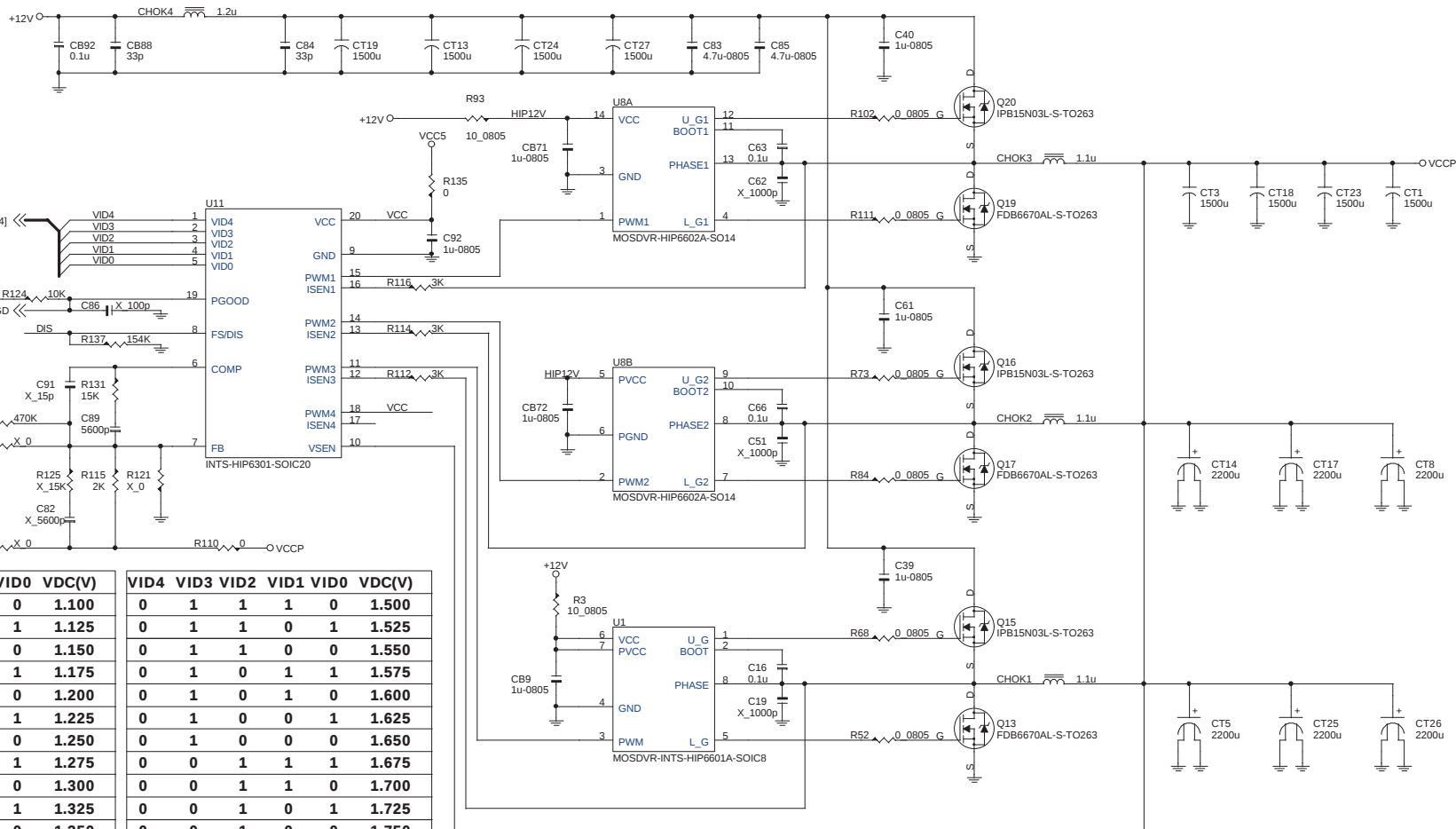
1.8V/3.3V SEQUENCE CIRCUIT



REGULATORS OUTPUT DECOUPLING CAPACITORS

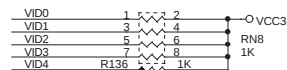


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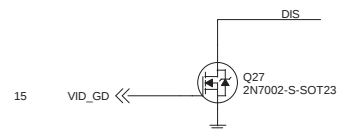
VID4	VID3	VID2	VID1	VID0	VDC(V)
1	1	1	1	0	1.100
1	1	1	0	1	1.125
1	1	1	0	0	1.150
1	1	0	1	1	1.175
1	1	0	1	0	1.200
1	1	0	0	1	1.225
1	1	0	0	0	1.250
1	0	1	1	1	1.275
1	0	1	1	0	1.300
1	0	1	0	1	1.325
1	0	1	0	0	1.350
1	0	0	1	1	1.375
1	0	0	1	0	1.400
1	0	0	0	1	1.425
1	0	0	0	0	1.450
0	1	1	1	1	1.475

VID PULL-UP RESISTORS

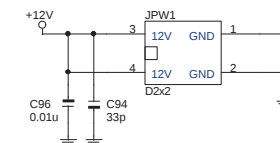


HIP6301V DON'T NEED PULL HIGH
HIP6301 NEED PULL HIGH

PWM GOOD



ATX12V POWER CONNECTOR



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3

SERIAL PORT 1



MODEM RING BLOCK



LAN WAKEUP BLOCK



SERIAL PORT 2



PS2 KEYBOARD & MOUSE CONNECTOR



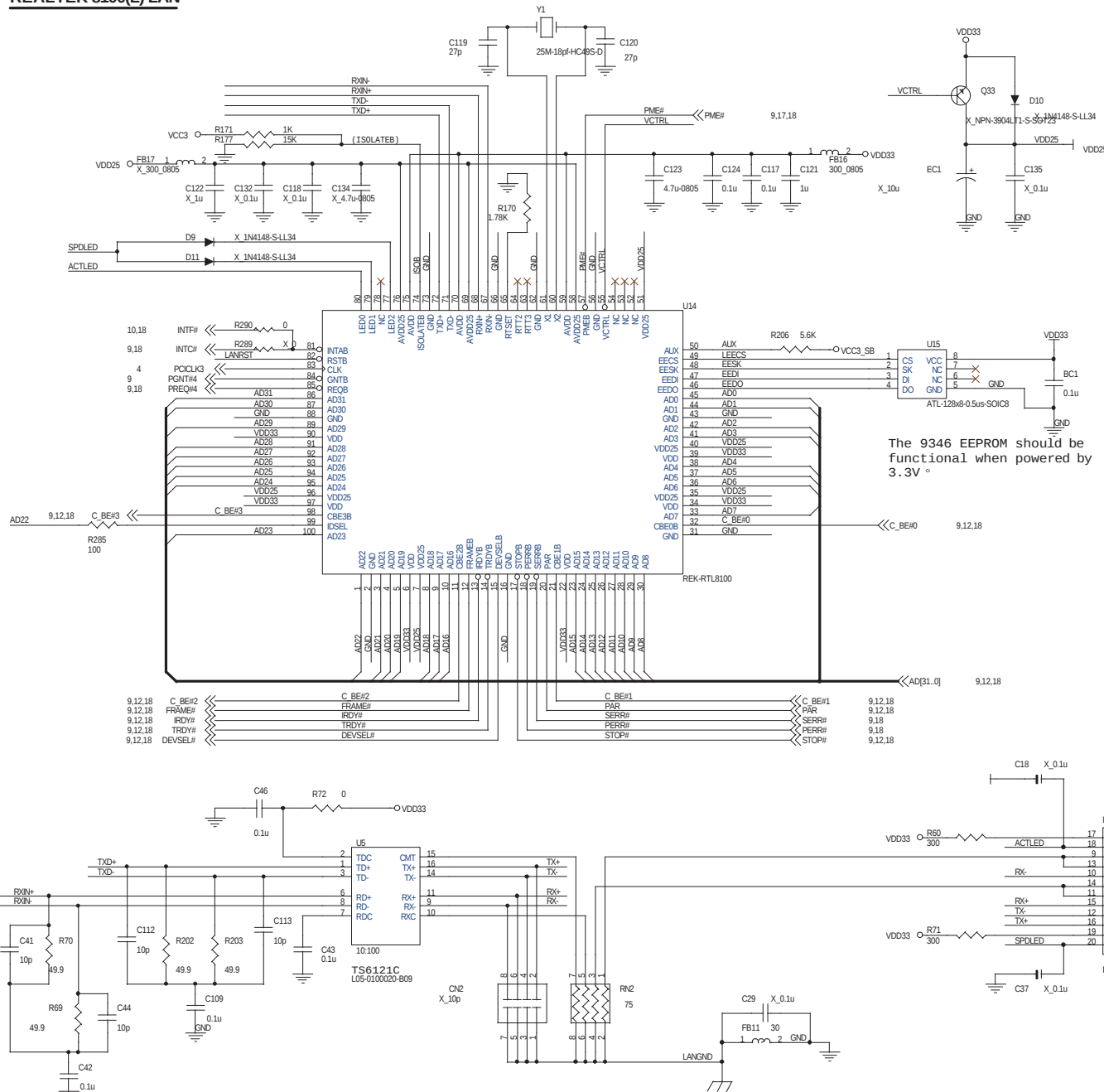
PARALLAL PORT



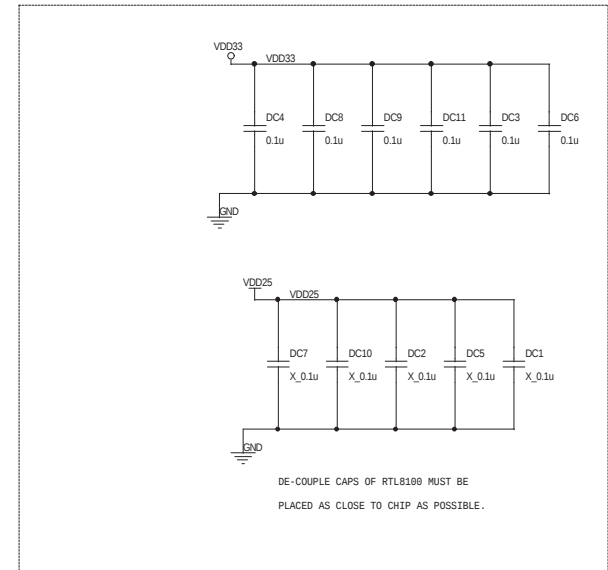
FLOPPY CONNECTOR



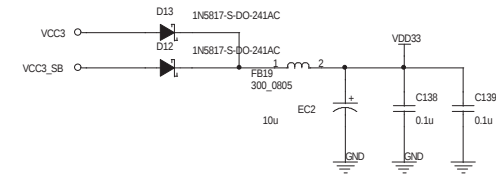
REALTEK 8100(L) LAN



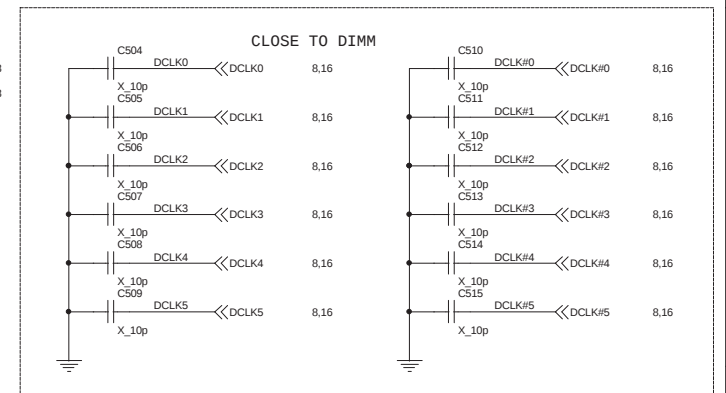
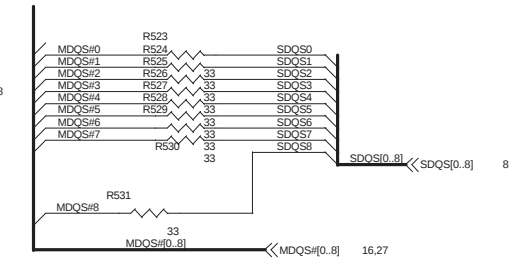
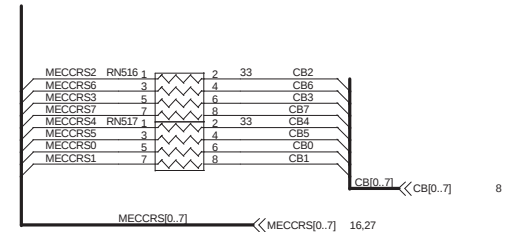
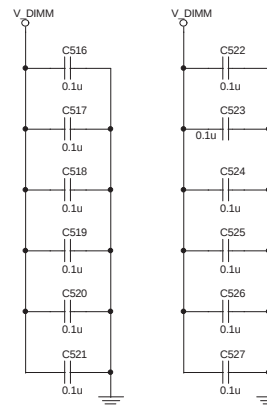
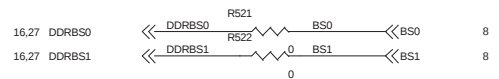
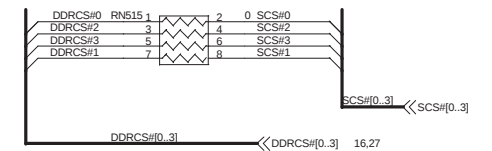
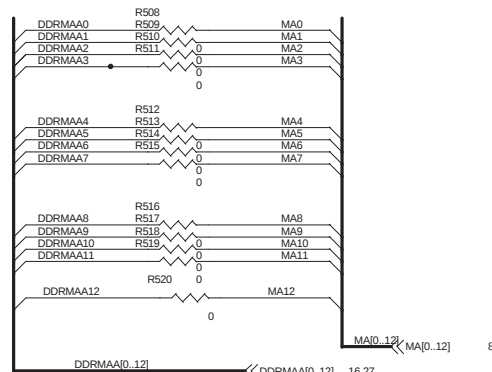
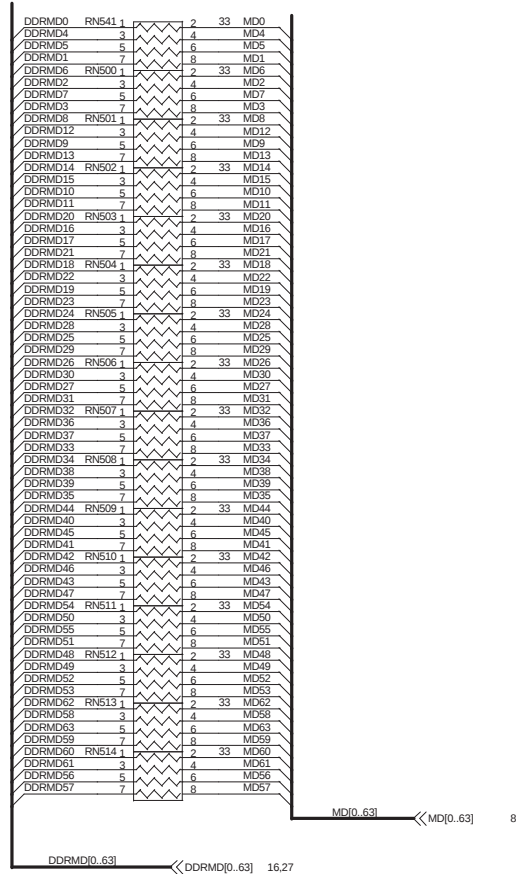
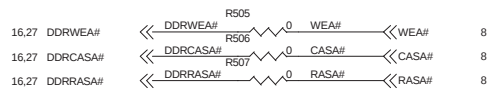
The 9346 EEPROM should be functional when powered by 3.3V °

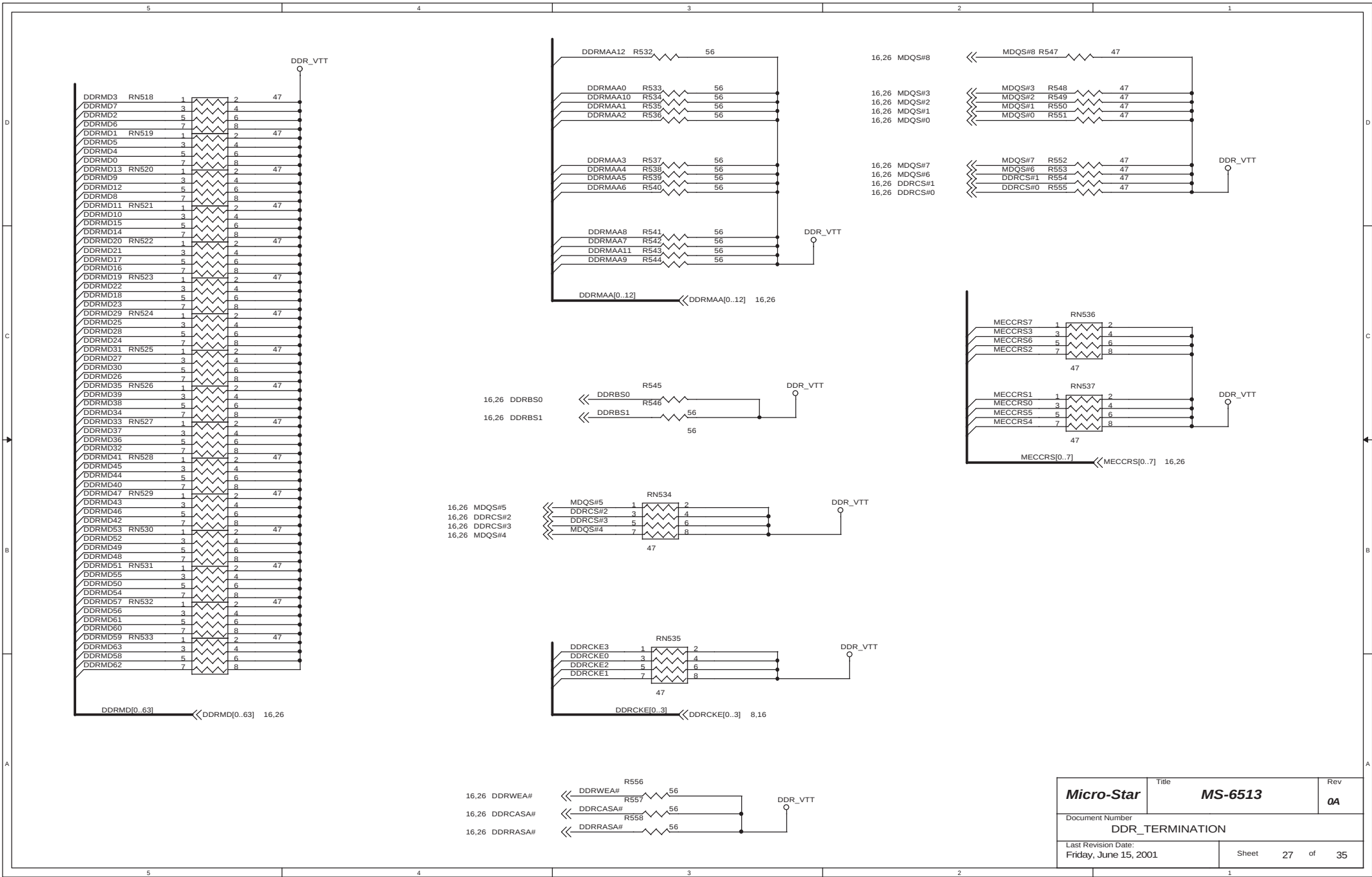


DE-COUPLE CAPS OF RTL8100 MUST BE PLACED AS CLOSE TO CHIP AS POSSIBLE.

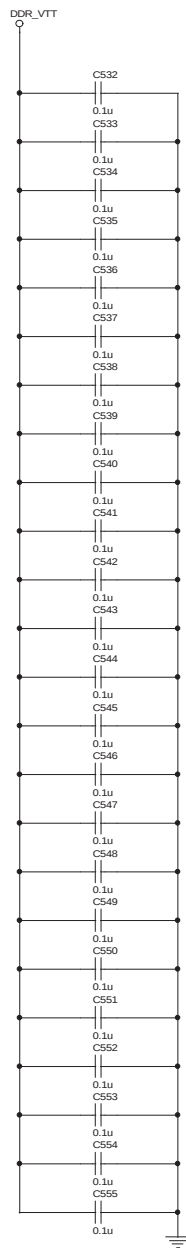
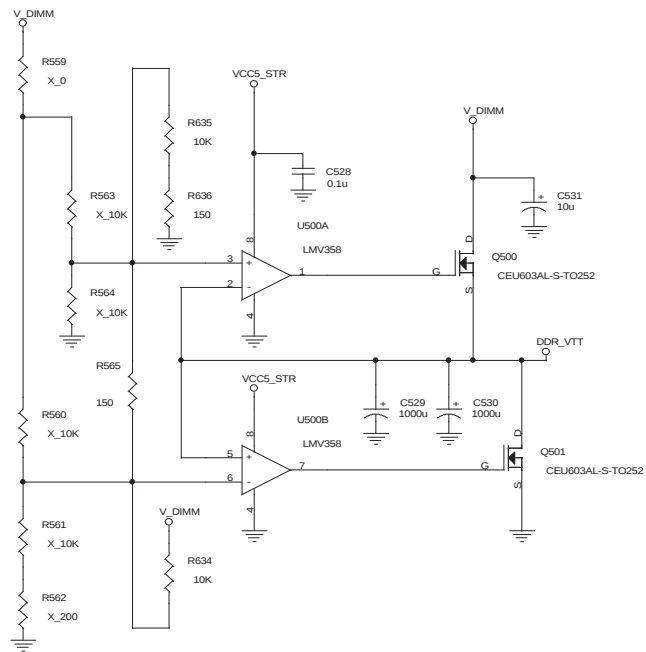


JLAN1/2	LAN SELECT
1-2	ENABLED
2-3	DISABLED





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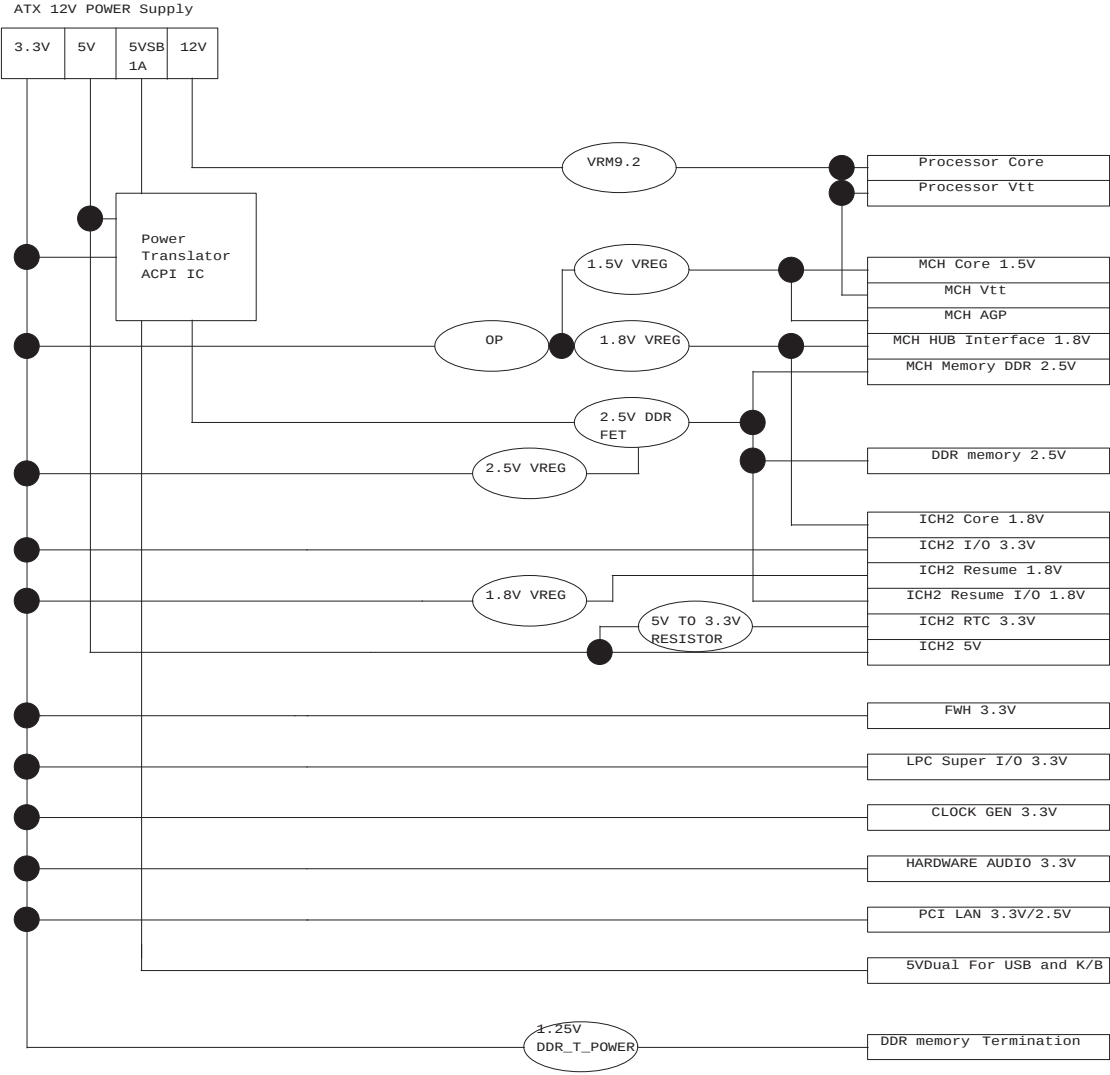
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DDR_T_POWER				
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Jumper Setting & Connector Setting

Jumper	Description	Connector	Description
J2	CHASSIS INTRUSION HEADER	U3	INTEL mPGA478-B CPU
J3	AUDIO REAR PHONE JACK (LINE_IN, LINE_OUT, MIC_IN)	IDE1	Primary
J4	AUDIO AUX HEADER	IDE2	Secondary
J5	AUDIO FRONT PANEL HEADPHONE JACK HEADER	DIM1	SDRAM DIMM1
J6	AUDIO INTERNAL SPEAKER HEADER (ATAPI)	DIM2	SDRAM DIMM2
J7	BIOS function	AGP1	AGP Slot
1-2	Normal (Default)	PCI1	PCI Slot1
2-3	Configuration Mode	PCI2	PCI Slot2
REMOVED	Recovery	PCI3	PCI Slot3
		COM1	Serial Port
		COM2	Serial Port
		LPT	Parallel Port
		FDD1	Floopy
JBAT1	CLEAR CMOS	JMDM1	MODEM RING HEADER
1-2	NORMAL (Default)	JWOL1	LAN WAKEUP HEADER
2-3	CLEAR CMOS	KBMS1	PS/2 Keyboard and PS/2 mouse
		C_FAN1	CPU FAN HEADER
CD_IN1	CDROM HEADER (ATAPI)	S_FAN	System FAN HEADER
MDM_IN1	TELEPHONY HEADER (ATAPI)	USB1	USB REAR CONNECTOR
		USB2	USB INTERNAL HEADER
		POWER	ATX Power
		JSMB1	SMBUS HEADER
		F_P1	Front Panel
		Pin1	Power of Hard LED
		Pin2	Power LED
		Pin3	Hard LED
		Pin4	Suspend LED
		Pin5,8,12,13	GND
		Pin6	Power Button
		Pin7	Reset Button
		Pin9	VCC
		P_FAN1	ATX FAN HEADER
		JPW1	ATX12V Power

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Power Delivery Map



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Pentium 4 Processor /Northwood mPGA 478

Source Synchronous Signal Group and the Associated Strobes

Signals	Associated Strobe
REQ[4:0],A[16:3]#	ADSTB0#
A[31:17]#	ADSTB1#
D[15:0]#,DBI0#	DSTBP0#,DSTBN0#
D[31:16]#,DBI1#	DSTBP1#,DSTBN1#
D[47:32]#,DBI2#	DSTBP2#,DSTBN2#
D[63:48]#,DBI3#	DSTBP3#,DSTBN3#

ADSTB0#
ADSTB1# should be +- 25mils

Signals	Length	Inaccuracy
Data	2.0" to 10.0"	+/- 100 mil
Address	2.0" to 10.0"	+/- 200 mil
Strobe	2.0" to 10.0"	+/- 25 mil
Clock	2.0" to 10.0"	Don't need

* Delta=(CPU_pkglen.net-CPUpkglen.strobe)+(CS_pkglen.net-CS_pkglen.strobe)

Trace : 7 mil width 13mil space

Miscellaneous Signals

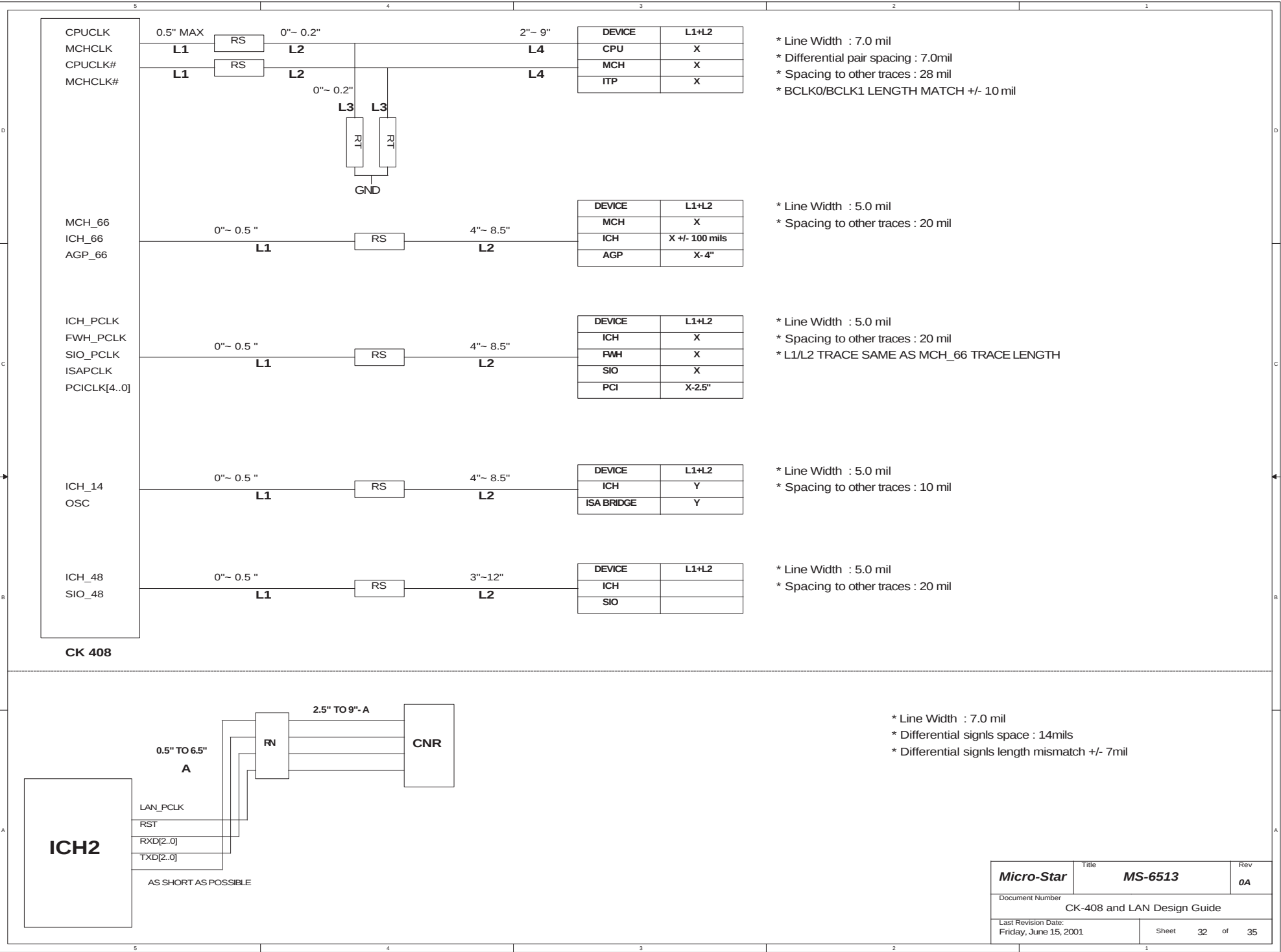
USB

- * USB Trace width : 9 mils
- * USB Trace Spacing : 25 mils
- * Differential USB Signlas Trace
Spacing : 18 mils
- * USB Power Trace must be 40mils width

AGP

1X Timing group	2X/4X Timing group	SIGNALS	Maximum Length	Width	Space	Dismatch Length	Relative to
AGPCLK PIPE# RBF# WBF# ST[2..0] GFRAME# GIRDY# GTRDY# GSTOP# GDEVSEL# GREQ# GNT# GPAR	SET#1 GAD[15..0] GC_BE#[1..0] GAD_STB0# SET#2 GAD[31..16] GC_BE#[3..2] GAD_STB1 GAD_STB1# SET#3 SBA[7..0] SB_STB SB_STB#	1X Timing group 2X/4X Timing group SET#1 2X/4X Timing group SET#2 2X/4X Timing group SET#3 2X/4X Timing group SET#1 2X/4X Timing group SET#2 2X/4X Timing group SET#3	7.5" 7.25" 7.25" 7.25" 6" 6" 6"	5 mil 5 mil 5 mil 5 mil 5 mil 5 mil 5 mil	5 mil 20 mil 20 mil 20 mil 15 mil 15 mil 15 mil	X +/- 0.125" +/- 0.125" +/- 0.125" +/- 0.25" +/- 0.25" +/- 0.25"	X GAD_STB0 GAD_STB0# GAD_STB1 GAD_STB1# SB_STB SB_STB# GAD_STB0 GAD_STB0# GAD_STB1 GAD_STB1# SB_STB SB_STB#

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SCK[0..2]
SCK#[0..2]
SCK[3..5]
SCK#[3..5]

Trace Width : 5 mils
Differential pair spacing : 7 mils.
Isolation spacing : 20 mils

A: 40 mils max
B+D: 2" ~ 6.5"
C+E: 2" ~ 7.0"

Length: SCK[0..2] = SCK#[0..2]
Length: SCK[3..5] = SCK#[3..5]

SDQ[0..63]
SCB[0..7]
SDQS[0..8]

Trace Width : 5 mils
Trace spacing : 12 mils

A: 2" ~ 5"
B: 0.5" MAX
C: 0.3" ~ 0.5"
D: 0.1" ~ 0.8"

Rs = 33 ohm +- 5%

RTT
DDR_VTT = 1.5V
Rtt = 47 ohm +- 5%

SDQ[0..7]	SDQS0
SDQ[8..15]	SDQS1
SDQ[16..23]	SDQS2
SDQ[24..31]	SDQS3
SDQ[32..39]	SDQS4
SDQ[40..47]	SDQS5
SDQ[48..55]	SDQS6
SDQ[56..63]	SDQS7
SCB[0..7]	SDQS8

Matching requirement is +- 25 mils to strobe

SMA[0..12]
SBS[0..1]
SRAS#
SCAS#
SWE#

Trace Width : 5 mils
Trace spacing : 12 mils

A: 40 mils max
B: 2" ~ 3.5"
C: 0.5" max
D: 0.3" ~ 0.5"
E: 0.1" ~ 0.8"

Rs = 0 ohm +- 5%

RTT
DDR_VTT = 1.5V
Rtt = 56 ohm +- 5%

$$\begin{aligned} \text{SCK}[0..2] \quad (A + B + D) &= \text{SMA}[0..12] \quad (A + B + C) + (1" \sim 4") \\ \text{SCK}\#[0..2] &= \text{SBS}[0..1] \\ \text{SCK}[3..5] \quad (A + C + E) &= \text{SMA}[0..12] \quad (A + B + C + D) + (1" \sim 4") \\ \text{SCK}\#[3..5] &= \text{SBS}[0..1] \end{aligned}$$

SCS#[0..1]
SCKE[0..1]

Trace Width : 5 mils
Trace spacing : 12 mils

A: 40 mils max
B: 2" ~ 3.5"
C: 0.5" max
D: 0.4" ~ 1.3"

Rs = 0 ohm +- 5%

RTT
DDR_VTT = 1.5V
Rtt = 47 ohm +- 5%

$$\begin{aligned} \text{SCK}[0..2] \quad (A + B + D) &= \text{SCS}\#[0..1] \quad (A + B + C) + (1" \sim 4") \\ \text{SCK}\#[0..2] &= \text{SCKE}[0..1] \\ \text{SCK}[3..5] \quad (A + C + E) &= \text{SCS}\#[2..3] \quad (A + B + C) + (1" \sim 4") \\ \text{SCK}\#[3..5] &= \text{SCKE}[2..3] \end{aligned}$$

SCS#[2..3]
SCKE[2..3]

Trace Width : 5 mils
Trace spacing : 12 mils

A: 40 mils max
B: 2" ~ 3.5"
C: 1.0" max
D: 0.1" ~ 0.8"

Rs = 0 ohm +- 5%

RTT
DDR_VTT = 1.5V
Rtt = 47 ohm +- 5%

RCVENIN#
RCVENOUT#

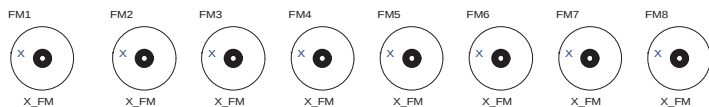
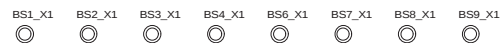
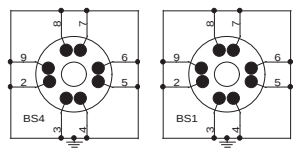
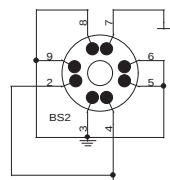
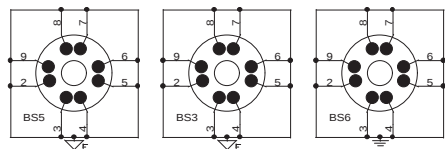
A: 40 mils max
B: exactly 1"

DIMM1 DIMM2

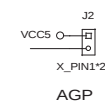
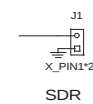
MCH

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PCB OTHER COMPONENT



SIMULATION TRACE

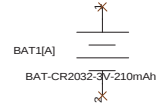


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JBAT1 Clear CMOS		
1 - 2	Normal	★
2 - 3	Clear CMOS	

JBAT1(1-2)
JC-D2-GN

BAT SOCKET



J7 BIOS Update	
SHORT	Locked
OPEN	Unlocked ★

J7(1)
X_JC-D2-GN

BIOS

U23(1)		
1	VPP	VCC
2	RST#	CLK
3	FGPI3	FGPI4
4	FGPI2	IC(VIL)
5	FGPI1	GNDA
6	FGPI0	VCCA
7	WP#	GND
8	TBL#	VCC
9	ID3	INIT#
10	ID2	FWH4
11	ID1	RFU
12	ID0	RFU
13	FWH0	RFU
14	FWH1	RFU
15	FWH2	RFU
16	GND	FWH3
17		
18		
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28		
29		
30		
31		
32		

SST-256K*9-33MHz-PLCC32

FRONT PANNEL BUZZER

F_P114-15
JC-D2-GN

JLAN1/2	LAN SELECT
1-2	ENABLED
2-3	DISABLED

JLAN1(1-2)
JC-D2-GN

PCB



Heat sink



Hooker



D1x3-1-2-BK



D1x3-1-2-BK



D1x3-1-2-BK



D1x3-1-2-BK

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