MS-6507E

Version 1.0
03/19/2002 Update

INTEL (R) Brookdale-E Chipset
Willamette/Northwood 478pin mPGA-B Processor Schematics

CPU:

Willamette/Northwood mPGA-478B Processor

System Brookdale-E Chipset:

INTEL MCH (North Bridge) +
INTEL ICH4 (South Bridge)

On Board Chipset:

BIOS -- FWH

LPC Super I/O -- W83627HF

Clock Generator -- CY28349

AC'97 Codec -- AvanceLogic AC201A/AC202A

Onboard Lan Chipset-- RealTek RTL8101L

Expansion Slots:

AGP2.0 SLOT * 1

PCI2.2 SLOT * 3 (PCI Slot 3 for Medion Option)

CNR1.2 SLOT * 1

ERP BOM	Function Description	
601-6507E-01S 601-6507E-020	MS-6507E 100 MSI Option:L	With LAN. MSI Standard
601-6507E-02S 601-6507E-010	MS-6507E 100 MSI Standard	Without LAN. MSI Standard
601-6507E-XXX		Medion SPEC.
	For Actebis:	With CNR,STR.W/O ISA,LAN. I/O with Shield.

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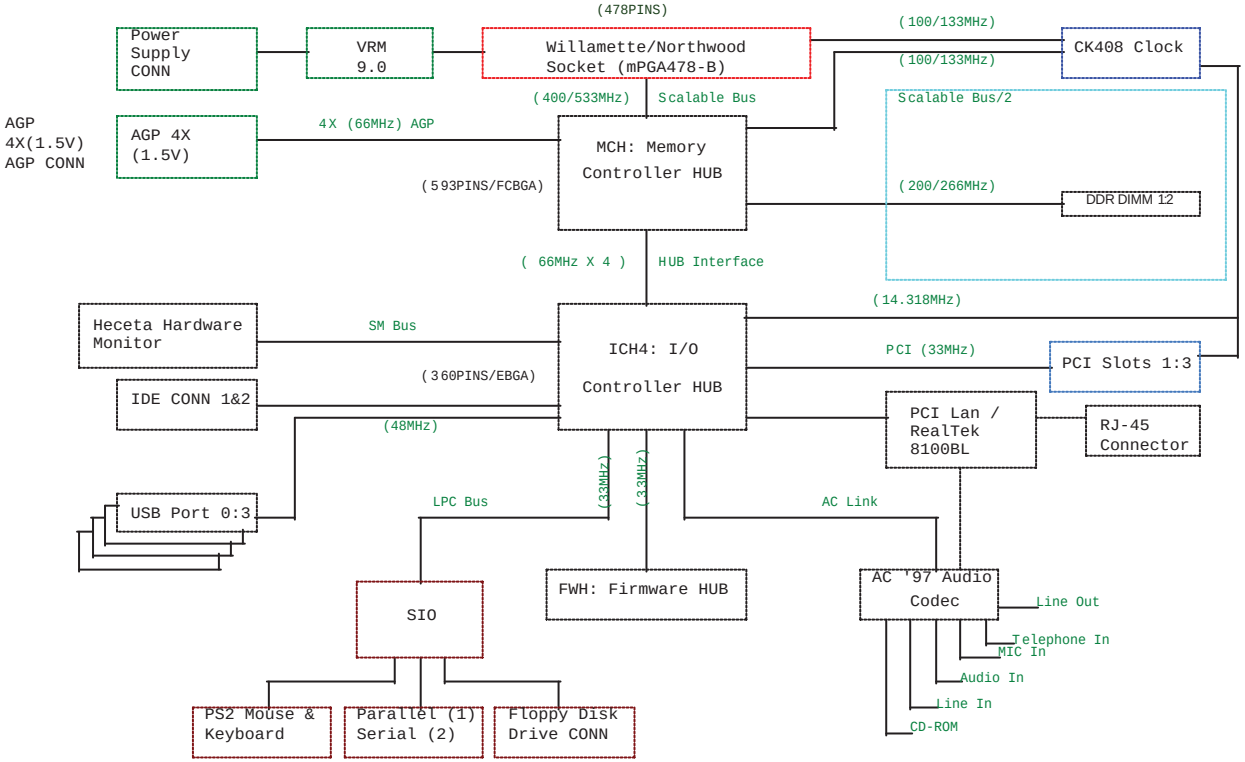

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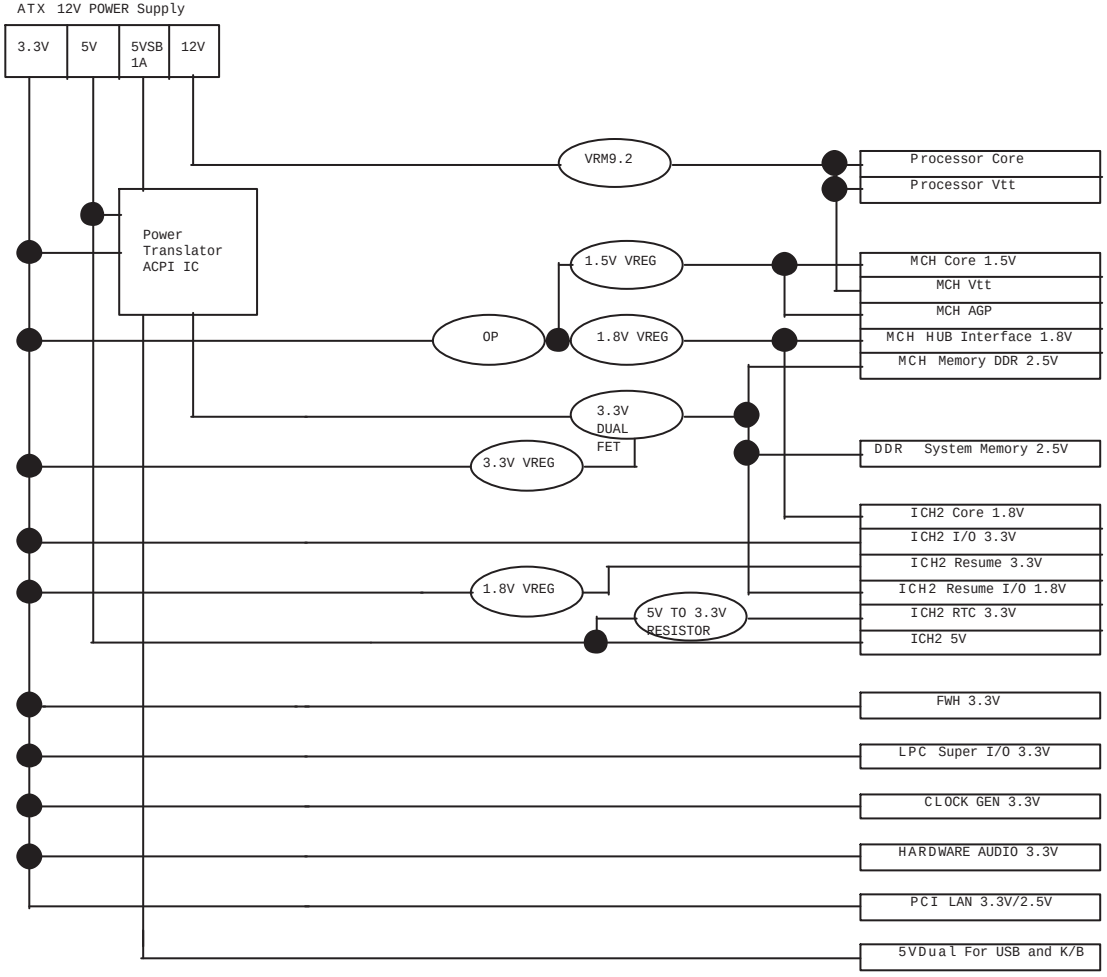
Power Delivery Map



POWER CONSUMPTION

	VCCP	VCC_AGP	VCC1_8	VCC3_DIMM	VCC3	VCC5	VCC5_SB	+12V	-12V
CPU	69.0A	0	0	0	0	0	0	NOTE4	0
MCH	2.4A	NOTE1	0.2A	2.0A	0	0	0	0	0
ICH4	0	0	NOTE3	0	NOTE3	0	NOTE3	0	0
ICS950213	0	0	0	0	0	0	0	0	0
ALC201A	0	0	0	0	0		0	0	0
FWH -SST	0	0	0	0			0		
W83627HF	0	0	0	0	0		0	0	0
L6917BD		0	0	0	0		0	0	0
DIMM	0	0	0	NOTE2	0		NOTE2	0	0
AGP	0	8.0A	0	0	6.0A	2.0A	?	1.0A	0
PCI	0	0	0	0		0	0	0	0
USB	0		0	0		0			0
USB HUB	0	0	0	0	0	0	0	0	0
FAN	0	0	0	0	0	0	0	0	0
TTL	0	0	0	0	0	0	0	0	0
AMPLIFIER	0	0	0	0			0	0	0
OTHER	0	0	0	0	0		0		

NOTE1 --- MCH
VCC_AGP = VCC1_5 (1.5A) + VCC_AGP (0.37A)

NOTE2 --- DIMM
S0 STATE --- 2.0A * 1 = 4.0A ---> V_DIMM
S1/S3 STATE --- 200mA * 2 = 400mA ---> V_DIMM
V_DIMM -->400mA*2.5V/3.3V=303mA --> VCC3_SB

NOTE3 --- ICH4

Power	S0	S1	S3/S4/S5
1.8V	132mA	99mA	N/A
VCC_AGP	550mA	266mA	N/A
VCC1_5SB	82mA	52mA	25mA
VCC3(I/O)	528mA	0.76mA	N/A
VCC3_SB	167mA	1mA	0.8mA / N/A

VCC3_SB =
VCC1_8SB =
VCC5_SB = VCC3_SB + VCC1_8SB

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General Purpose I/O Spec.

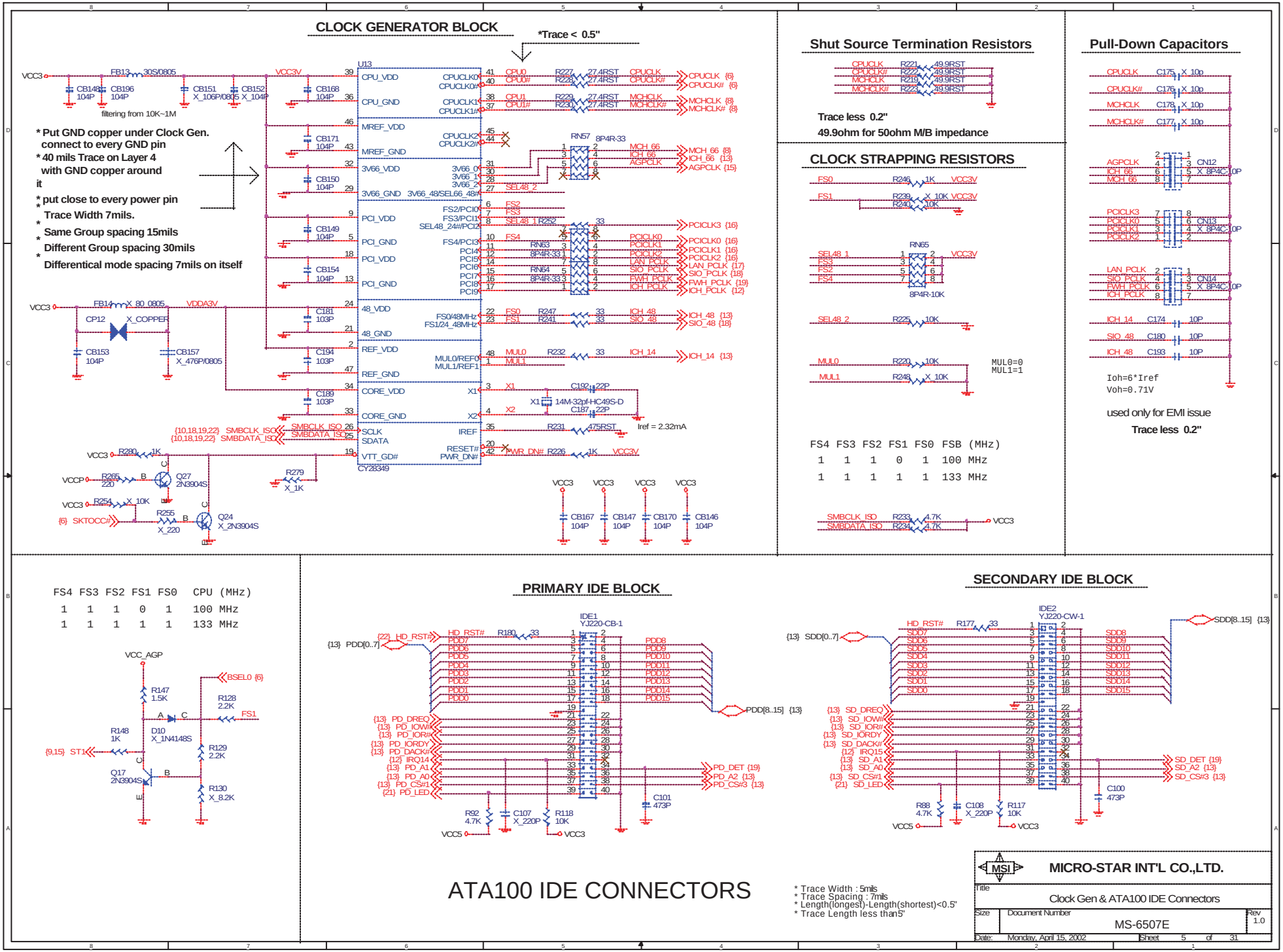
ICH4

GPIO Pin	Type	Function
GPIO 0	I	REQ#A
GPIO 1	I	REQ#5
GPIO 2	I	IRQE#
GPIO 3	I	IRQF#
GPIO 4	I	IRQG#
GPIO 5	I	IRQH#
GPIO 6~7	I	Not Implemented
GPIO 8	I	SIO_PME#
GPIO 9~10	I	Not Implemented
GPIO 11	I	External SMI
GPIO 12~13	I	Not Implemented
GPIO 14~15	I	Not Implemented
GPIO 16	O	Non Connect
GPIO 17	O	GNT#5
GPIO 18~21	O	Non Connect
GPIO 22	O/D	Non Connect
GPIO 23	O	BIOS Protect
GPIO 24~27	I/O	Non Connect
GPIO 28	I/O	LAN DISABLED(ICH4)
GPIO 29~47	I/O	Non Connect

FWH

GPIO Pin	Type	Function
GPI 0	I	ATA IDE 1 Detect
GPI 1	I	ATA IDE 2 Detect
GPI 2	I	Reserved
GPI 3	I	Reserved

DEVICE	ICH INT Pin	IDSEL	CLOCK
PCI Slot 1	INTA# INTB# INTC# INTD#	AD16	PCICLK0
PCI Slot 2	INTB# INTC# INTD# INTA#	AD17	PCICLK1
PCI Slot 3	INTC# INTD# INTA# INTB#	AD18	PCICLK2
PCI Slot 3	INTG#	AD19	PCICLK3
PCI Lan	INTD#/INTF#	AD29	LANPCLK


CLOCK GENERATOR BLOCK
*Trace < 0.5"
* Put GND copper under Clock Gen. connect to every GND pin
* 40 mils Trace on Layer 4 with GND copper around it
* put close to every power pin
* Trace Width 7mils.
* Same Group spacing 15mils
* Different Group spacing 30mils
* Differentical mode spacing 7mils on itself
filtering from 10K~1M
U13
CY28349
Iref = 2.32mA
Shut Source Termination Resistors
Trace less 0.2"
49.9ohm for 50ohm M/B impedance
CLOCK STRAPPING RESISTORS
FS4 FS3 FS2 FS1 FS0 FSB (MHz)
1 1 1 0 1 100 MHz
1 1 1 1 1 133 MHz
MUL0=0
MUL1=1
Pull-Down Capacitors
Ioh=6*Iref
Voh=0.71V
used only for EMI issue
Trace less 0.2"
FS4 FS3 FS2 FS1 FS0 CPU (MHz)
1 1 1 0 1 100 MHz
1 1 1 1 1 133 MHz
PRIMARY IDE BLOCK
SECONDARY IDE BLOCK
IDE1
YJ220-CB-1
IDE2
YJ220-CW-1
ATA100 IDE CONNECTORS
* Trace Width : 5mils
* Trace Spacing : 7mils
* Length(longest)-Length(shortest)<0.5"
* Trace Length less than5"
MICRO-STAR INT'L CO.,LTD.
Title
Clock Gen & ATA100 IDE Connectors
Size
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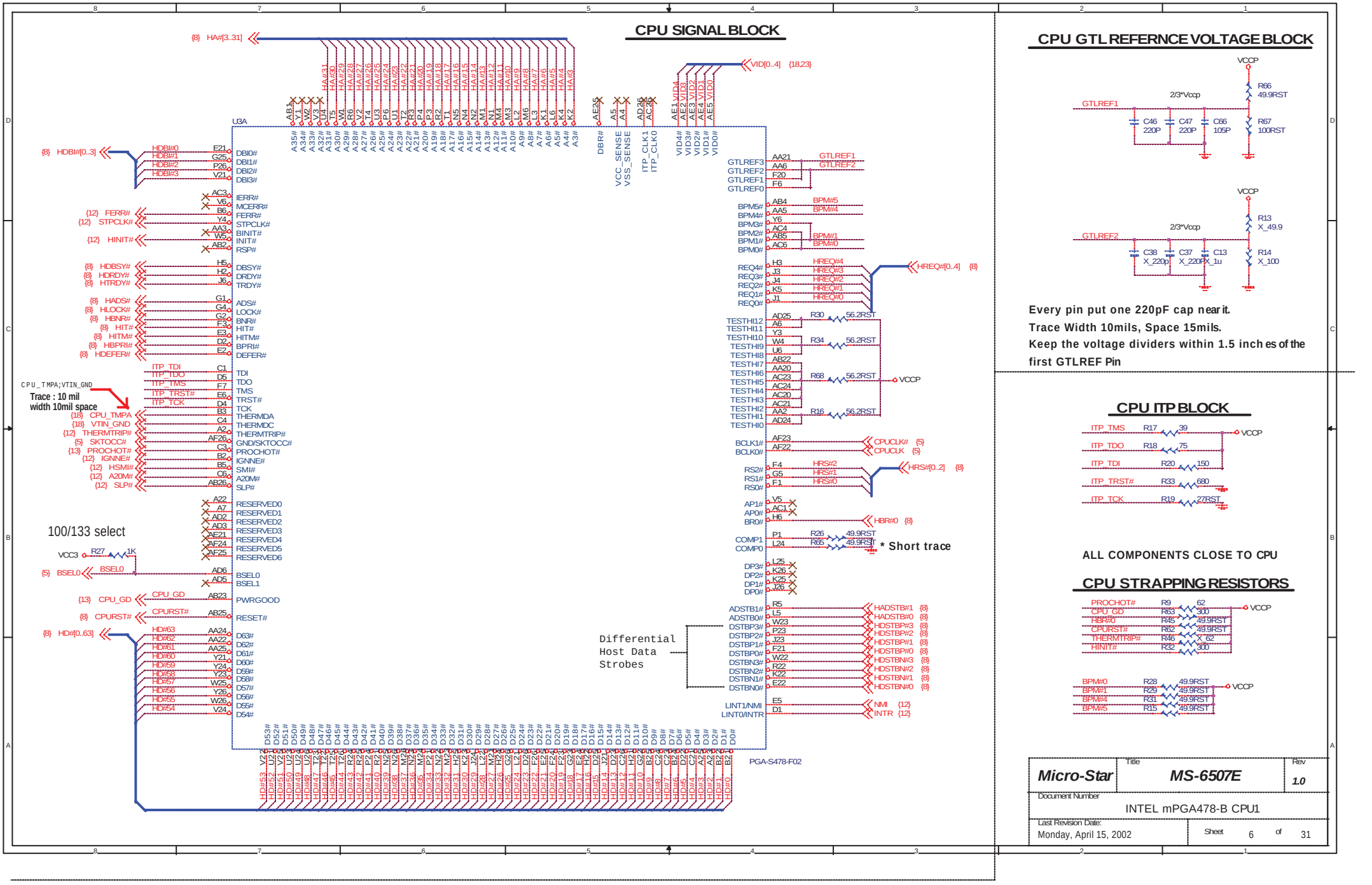
CPU SIGNAL BLOCK
CPU GTL REFERNCE VOLTAGE BLOCK
CPU ITP BLOCK
CPU STRAPPING RESISTORS
Every pin put one 220pF cap near it.
Trace Width 10mils, Space 15mils.
Keep the voltage dividers within 1.5 inch es of the first GTLREF Pin
ALL COMPONENTS CLOSE TO CPU
Trace : 10 mil width 10mil space
100/133 select
* Short trace
Differential Host Data Strobes
PGA-S478-F02
Micro-Star
MS-6507E
1.0
INTEL mPGA478-B CPU1
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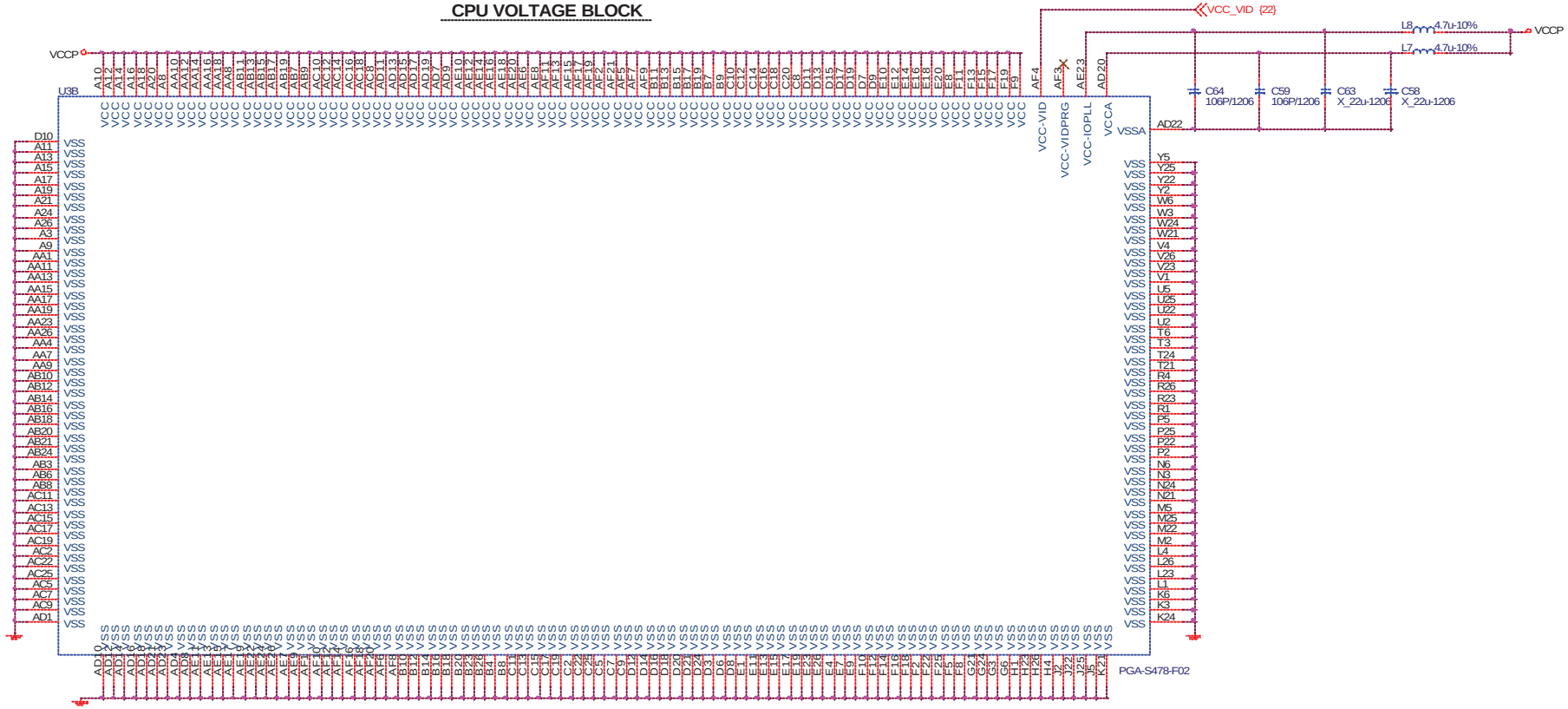
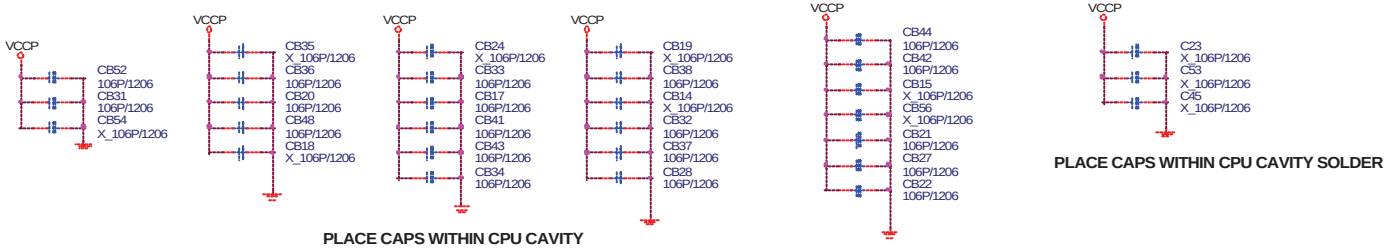
CPU VOLTAGE BLOCK



CPU DECOUPLING CAPACITORS



PLACE CAPS WITHIN CPU CAVITY

Reserve if necessary.

PLACE CAPS WITHIN CPU CAVITY SOLDER

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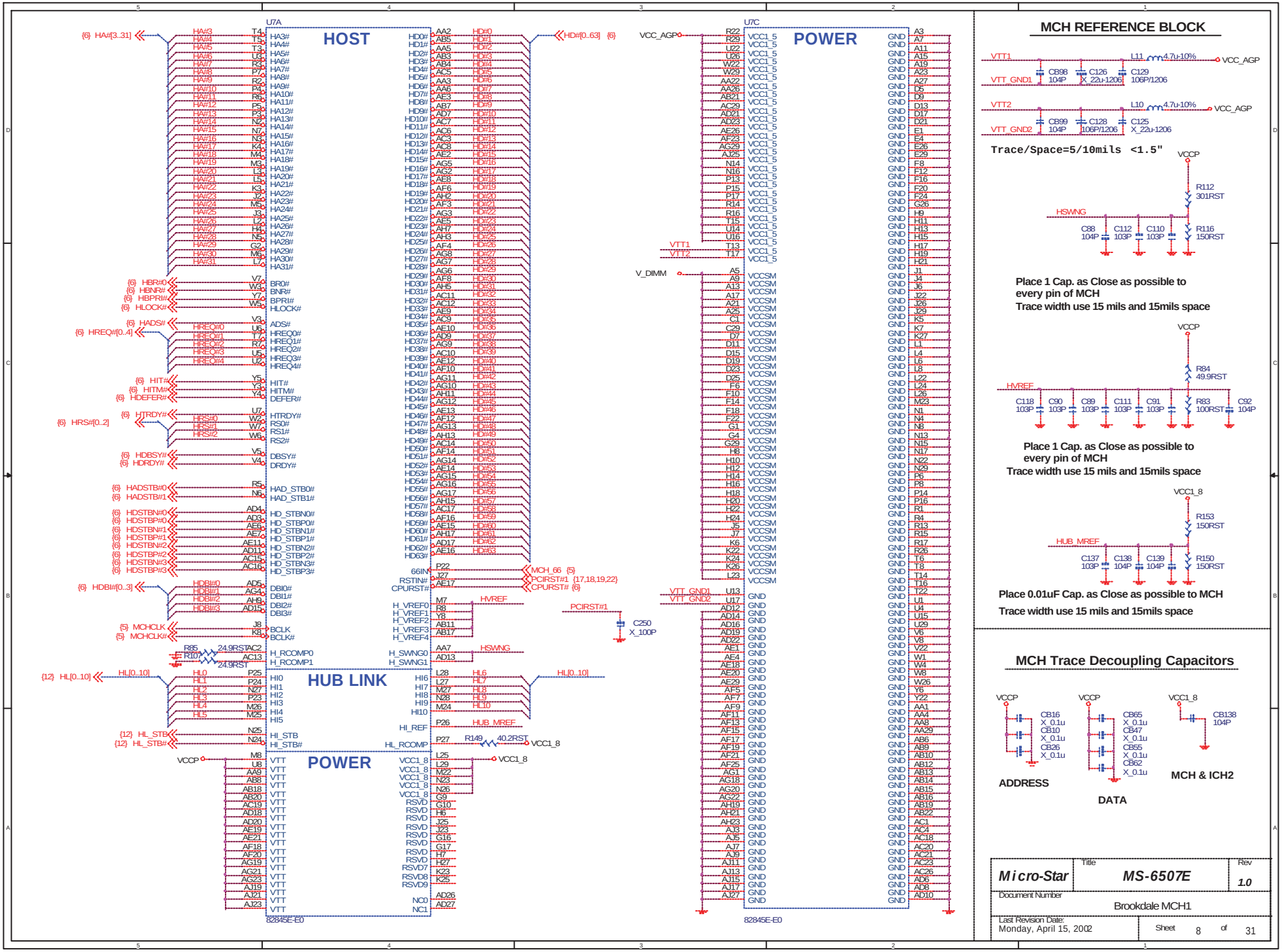

MCH REFERENCE BLOCK

Place 1 Cap. as Close as possible to every pin of MCH
Trace width use 15 mils and 15mils space

Place 1 Cap. as Close as possible to every pin of MCH
Trace width use 15 mils and 15mils space

Place 0.01uF Cap. as Close as possible to MCH
Trace width use 15 mils and 15mils space

MCH Trace Decoupling Capacitors

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1" trace

U7B

DDR

{11} MD[0..63]

MD0 G28 SDQ0
MD1 F27 SDQ1
MD2 C28 SDQ2
MD3 E28 SDQ3
MD4 H25 SDQ4
MD5 G27 SDQ5
MD6 F25 SDQ6
MD7 B28 SDQ7
MD8 E27 SDQ8
MD9 C27 SDQ9
MD10 B25 SDQ10
MD11 C25 SDQ11
MD12 B27 SDQ12
MD13 D27 SDQ13
MD14 D26 SDQ14
MD15 E25 SDQ15
MD16 D24 SDQ16
MD17 E23 SDQ17
MD18 C22 SDQ18
MD19 E21 SDQ19
MD20 C24 SDQ20
MD21 B23 SDQ21
MD22 D22 SDQ22
MD23 B21 SDQ23
MD24 C21 SDQ24
MD25 D20 SDQ25
MD26 C19 SDQ26
MD27 D18 SDQ27
MD28 C20 SDQ28
MD29 E19 SDQ29
MD30 C18 SDQ30
MD31 E17 SDQ31
MD32 E13 SDQ32
MD33 C12 SDQ33
MD34 B11 SDQ34
MD35 C10 SDQ35
MD36 B13 SDQ36
MD37 C13 SDQ37
MD38 C11 SDQ38
MD39 D10 SDQ39
MD40 E10 SDQ40
MD41 C9 SDQ41
MD42 D8 SDQ42
MD43 E8 SDQ43
MD44 E11 SDQ44
MD45 B9 SDQ45
MD46 B7 SDQ46
MD47 C7 SDQ47
MD48 C6 SDQ48
MD49 D6 SDQ49
MD50 D4 SDQ50
MD51 B3 SDQ51
MD52 E6 SDQ52
MD53 B5 SDQ53
MD54 C4 SDQ54
MD55 E5 SDQ55
MD56 C3 SDQ56
MD57 D3 SDQ57
MD58 F4 SDQ58
MD59 F3 SDQ59
MD60 B2 SDQ60
MD61 C2 SDQ61
MD62 E2 SDQ62
MD63 G5 SDQ63

SMA0 E12 DDRMA0
SMA1 F17 DDRMA1
SMA2 E16 DDRMA2
SMA3 G18 DDRMA3
SMA4 G19 DDRMA4
SMA5 E18 DDRMA5
SMA6 F19 DDRMA6
SMA7 G21 DDRMA7
SMA8 G20 DDRMA8
SMA9 F21 DDRMA9
SMA10 F13 DDRMA10
SMA11 E20 DDRMA11
SMA12 G22 DDRMA12

DDRMA[0..12] {10,11}

SCS#0 E9 CS#0
SCS#1 F7 CS#1
SCS#2 E9 CS#2
SCS#3 E7 CS#3

CS#[0..3]

SCB0 C16 CB0
SCB1 D16 CB1
SCB2 B15 CB2
SCB3 C14 CB3
SCB4 B17 CB4
SCB5 C17 CB5
SCB6 C15 CB6
SCB7 D14 CB7

CS#[0..3] {10,11}

CB[0..7]

CB[0..7] {11}

SDQS0 F26 SDQS0
SDQS1 C26 SDQS1
SDQS2 C23 SDQS2
SDQS3 B19 SDQS3
SDQS4 D12 SDQS4
SDQS5 C8 SDQS5
SDQS6 C5 SDQS6
SDQS7 E3 SDQS7
SDQS8 E15 SDQS8

SDQS[0..8] {11}

SCK0 E14 DCLK0
SCK#0 F15 DCLK#0
SCK1 J24 DCLK1
SCK#1 G25 DCLK#1
SCK2 G6 DCLK2
SCK#2 G7 DCLK#2
SCK3 G15 DCLK3
SCK#3 G14 DCLK#3
SCK4 E24 DCLK4
SCK#4 G24 DCLK#4
SCK5 H5 DCLK5
SCK#5 F5 DCLK#5

DCLK0 {10}
DCLK#0 {10}
DCLK1 {10}
DCLK#1 {10}
DCLK2 {10}
DCLK#2 {10}
DCLK3 {10}
DCLK#3 {10}
DCLK4 {10}
DCLK#4 {10}
DCLK5 {10}
DCLK#5 {10}

SCKE0 G23 DDRCKE0
SCKE1 F22 DDRCKE1
SCKE2 H23 DDRCKE2
SCKE3 F23 DDRCKE3

DDRCKE0 {10,11}
DDRCKE1 {10,11}
DDRCKE2 {10,11}
DDRCKE3 {10,11}

SRAS# F11 RASA#
SCAS# G8 CASA#
SWE# G11 WEA#

RASA# {10,11}
CASA# {10,11}
WEA# {10,11}

SBS0 G12 BS0
SBS1 G13 BS1

BS0 {10,11}
BS1 {10,11}

SM_RCOMP J28 MRCOMP

SD_REF0 J9 SM_REF
SD_REF1 J21

RCVENIN# C3
RCVENOUT# H3

1" Trace

AGP

{15} GAD[0..31]

GAD0 R27 G_AD0
GAD1 R28 G_AD1
GAD2 T25 G_AD2
GAD3 R25 G_AD3
GAD4 T26 G_AD4
GAD5 T27 G_AD5
GAD6 U27 G_AD6
GAD7 U28 G_AD7
GAD8 V26 G_AD8
GAD9 V27 G_AD9
GAD10 T23 G_AD10
GAD11 U23 G_AD11
GAD12 T24 G_AD12
GAD13 U24 G_AD13
GAD14 U25 G_AD14
GAD15 V24 G_AD15
GAD16 Y27 G_AD16
GAD17 Y26 G_AD17
GAD18 AA28 G_AD18
GAD19 AB25 G_AD19
GAD20 AB27 G_AD20
GAD21 AA27 G_AD21
GAD22 AB26 G_AD22
GAD23 Y23 G_AD23
GAD24 AB23 G_AD24
GAD25 AA24 G_AD25
GAD26 AA25 G_AD26
GAD27 AB24 G_AD27
GAD28 AC25 G_AD28
GAD29 AC24 G_AD29
GAD30 AC22 G_AD30
GAD31 AD24 G_AD31

{15} GC_BE#[0..3]

GC_BE#0 V25 G_C/BE0#
GC_BE#1 V23 G_C/BE1#
GC_BE#2 Y24 G_C/BE2#
GC_BE#3 AA23 G_C/BE3#

Tri-Stated during RSTIN# assertion

G_FRAME# Y24 GFRAME# {15}
G_IRDY# W27 GIRDY# {15}
G_TRDY# W24 GTRDY# {15}
G_DEVSEL# W28 GDEVSEL# {15}
G_STOP# W23 GSTOP# {15}
G_PAR W25 GPAR {15}

G_REQ# AG24 GREQ# {15}
G_GNT# AH25 GGNT# {15}

SBA0 AH28 SBA0
SBA1 AH27 SBA1
SBA2 AG28 SBA2
SBA3 AG27 SBA3
SBA4 AE28 SBA4
SBA5 AE27 SBA5
SBA6 AE24 SBA6
SBA7 AE25 SBA7

SBA[0..7] {15}

SB_STB AF27 SB_STB {15}
SB_STB# AF26 SB_STB# {15}

ST0 AG25 ST0
ST1 AF24 ST1
ST2 AG26 ST2

ST[0..2] {5,15}

AD_STB0 R24 GAD_STB0 {15}
AD_STB0# P22 GAD_STB#0 {15}
AD_STB1 AC27 GAD_STB1 {15}
AD_STB1# AC28 GAD_STB#1 {15}

PIPE# AF22 PIPE# {15}
RBF# AE22 RBF# {15}
WBF# AE23 WBF# {15}

CB209 X 0.1u 5020

AGPREF G_RCOMP AA21 AD25 R145 40.2R5 R144 4.7K H26 TESTIN# AGPREF {15}

VCC1_8

82845E-E0

MCH MEMORY CLOCK RC CIRCUITS

DDR_VTT
CB110 104P
R146 30
MRCOMP
C141 X_104P

MCH REFERENCE VOLTAGE

DIMMREF
SM_REF
C248 X_0.1u
C122 104P
5020

MCH DECOUPLING CAPACITOR

VCCP
CB88 104P
CB93 104P
CB95 103P
CB92 106P/1206
CB89 X_106P/1206

VCC1_8
CB108 104P
CB107 104P

VCC_AGP
CB109 104P
CB106 104P
CB112 104P
CB105 104P
CB97 104P

V_DIMM
CB91 104P
CB102 104P
CB96 104P
CB84 104P
CB77 104P
CB86 104P
CB81 104P

C136 104P
C135 103P
AGPREF

BACK

VCCP
CB203 X_0.1u 5020

VCC_AGP
CB207 X_0.1u 5020
CB205 X_0.1u 5020
CB211 X_0.1u 5020
CB206 X_0.1u 5020
CB210 X_0.1u 5020

V_DIMM
CB208 X_0.1u 5020
CB204 X_0.1u 5020

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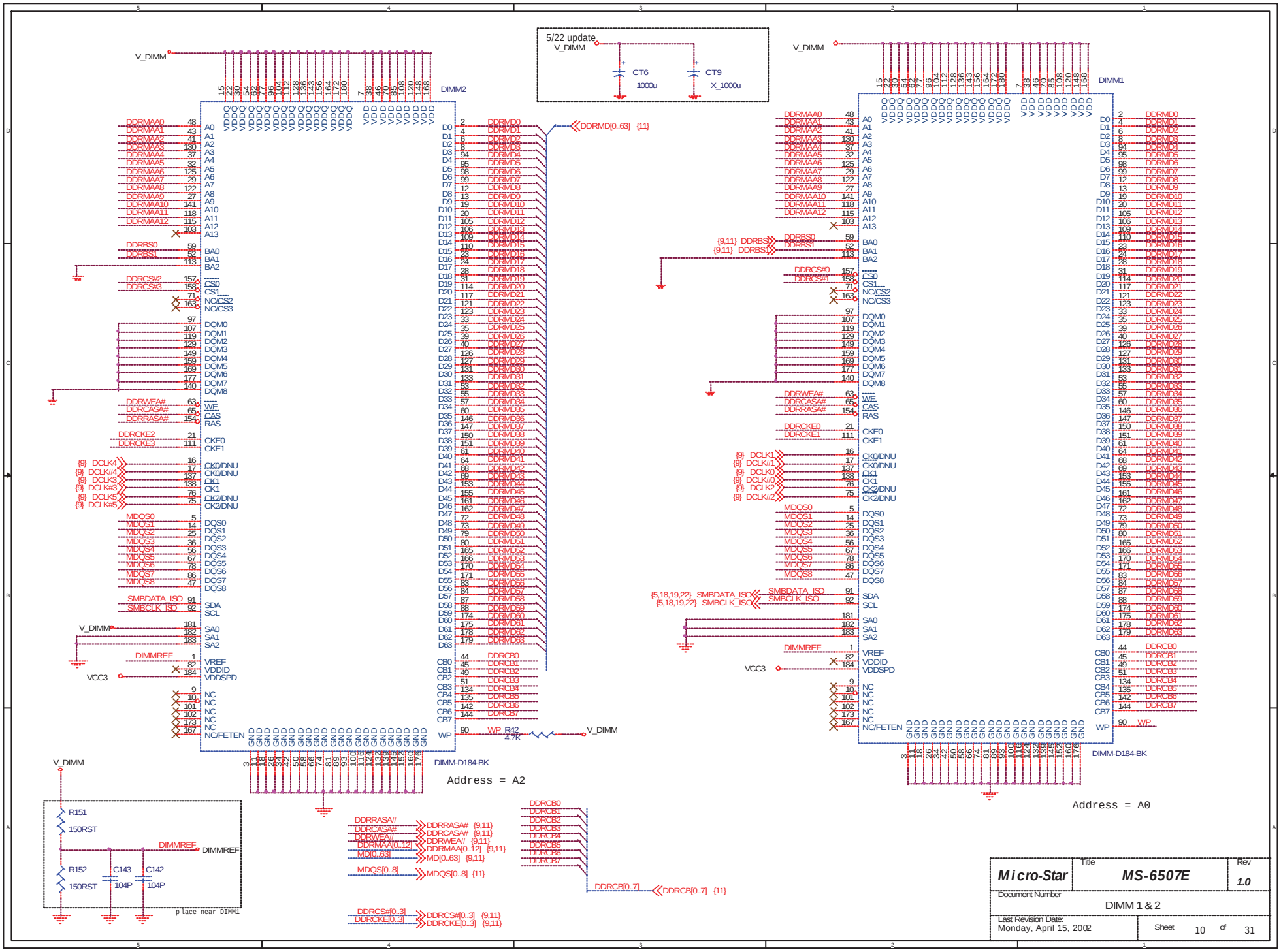
5/22 update
V_DIMM
CT6
1000u
CT9
X_1000u
DIMM2
DIMM1
DIMM-D184-BK
Address = A2
Address = A0
DDRDMD[0..63] {11}
DDRCB[0..7] {11}
DDRRASA# DDRRASA# {9,11}
DDRCASA# DDRCASA# {9,11}
DDRWEA# DDRWEA# {9,11}
DDRMAA[0..12] DDRMAA[0..12] {9,11}
MD[0..63] MD[0..63] {9,11}
MDQS[0..8] MDQS[0..8] {11}
DDRCS#[0..3] DDRCS#[0..3] {9,11}
DDRCKE[0..3] DDRCKE[0..3] {9,11}
R151
150RST
DIMMREF
R152
150RST
C143
104P
C142
104P
place near DIMM1
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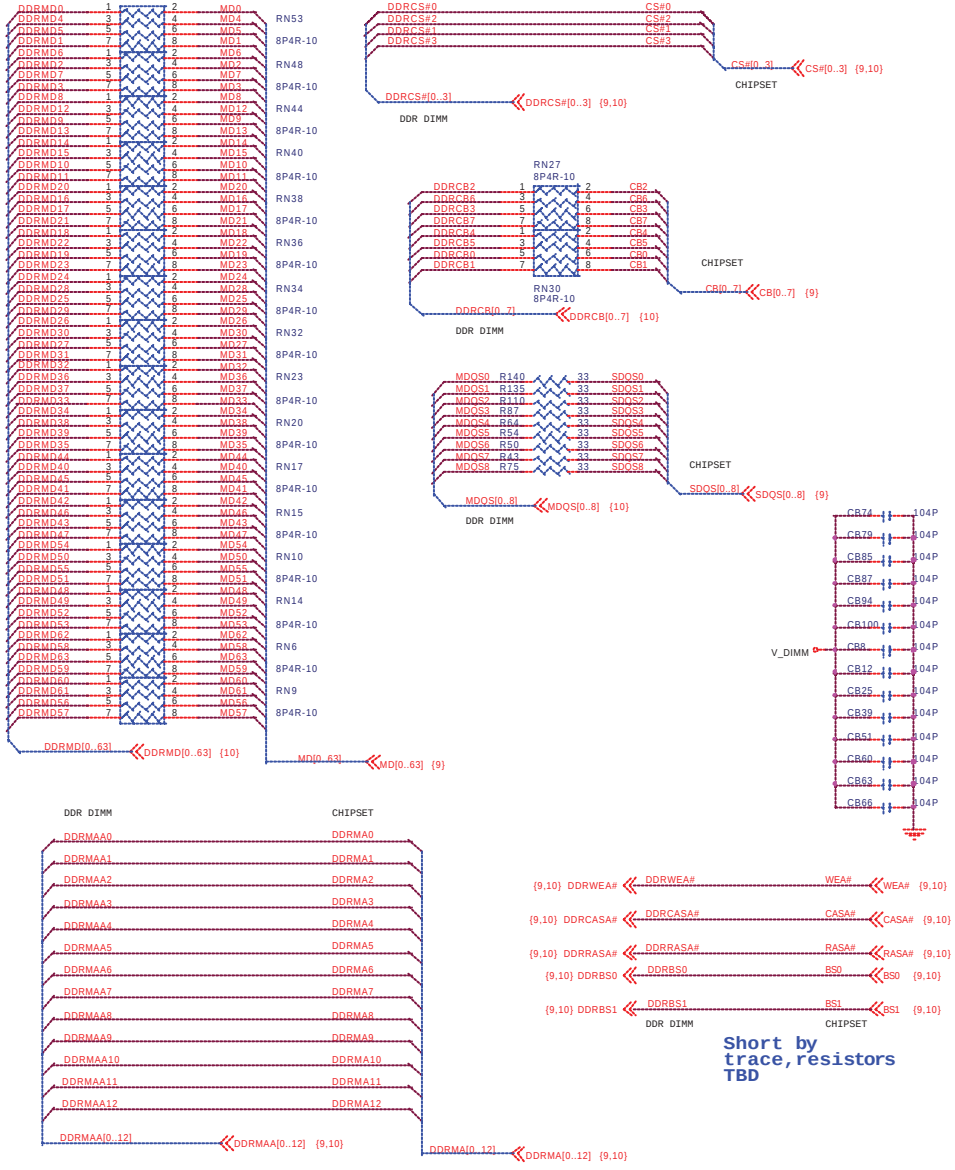
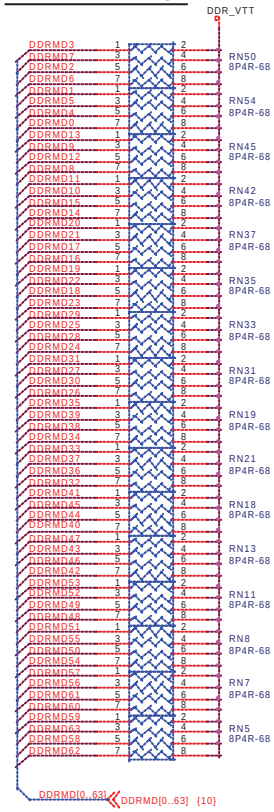
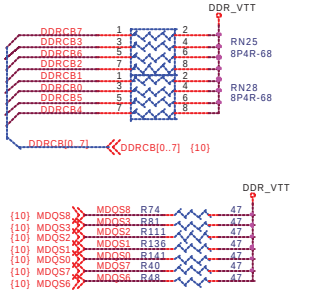
DDR DAMPING

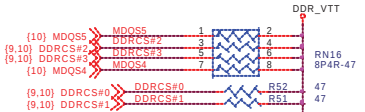


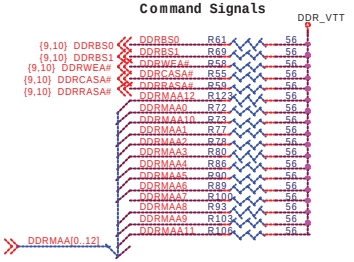
Short by trace,resistors TBD

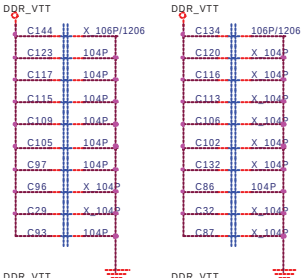
DDR TERMINATION

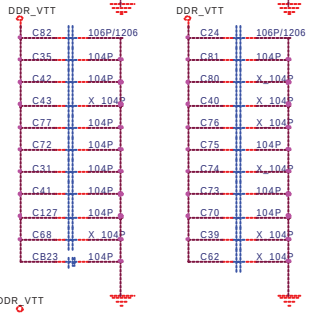


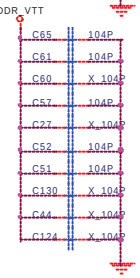












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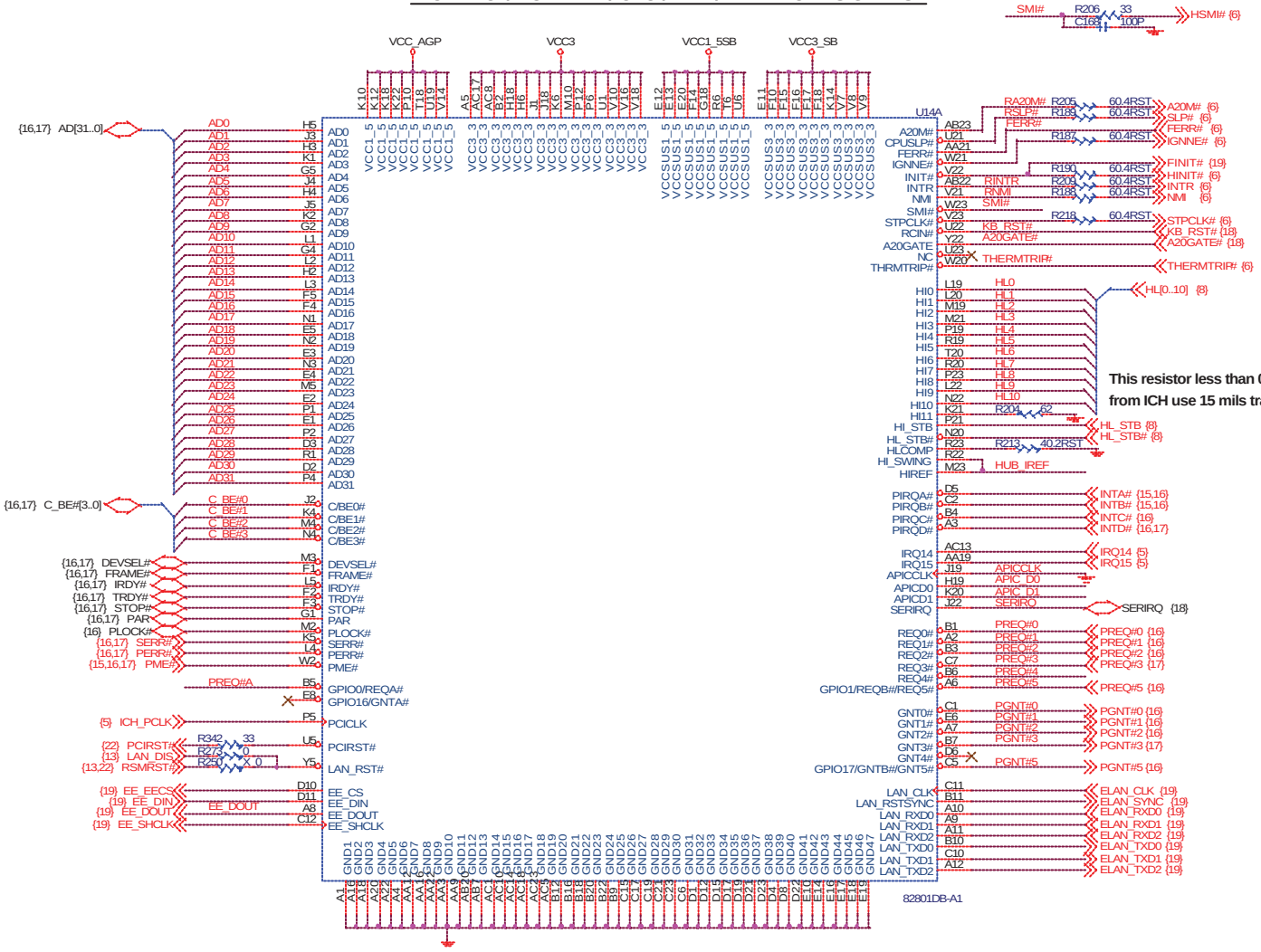
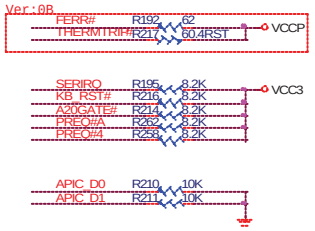
ICH4 PCI / HUB LINK / CPU / LAN / INTERRUPT SIGNALS



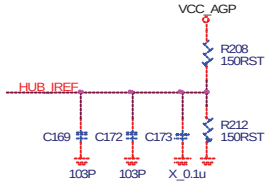
ICH4 STRAPPING RESISTORS

Reserved pull-down resistor for ICH4 reserved function straps.

ICH4 PULL-UP/DOWN RESISTORS



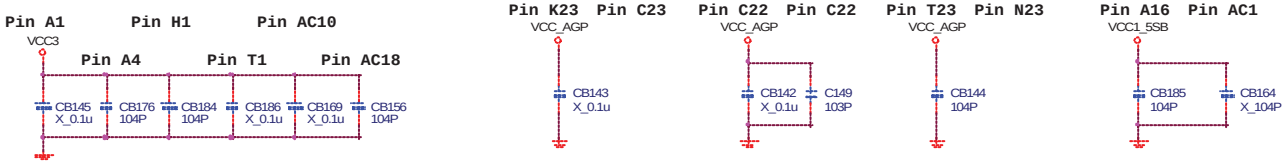
ICH4 REFERENCE VOLTAGE



Place Cap. as Close as possible to ICH4 < 0.25"
Trace width use 12 mils and 10mils space

ICH4 DECOUPLING CAPACITORS

Place one 0.1u close to ICH4 <100 mil



MSI MICRO-STAR INT'L CO.,LTD.

Title: ICH4 PCI & HI & LAN

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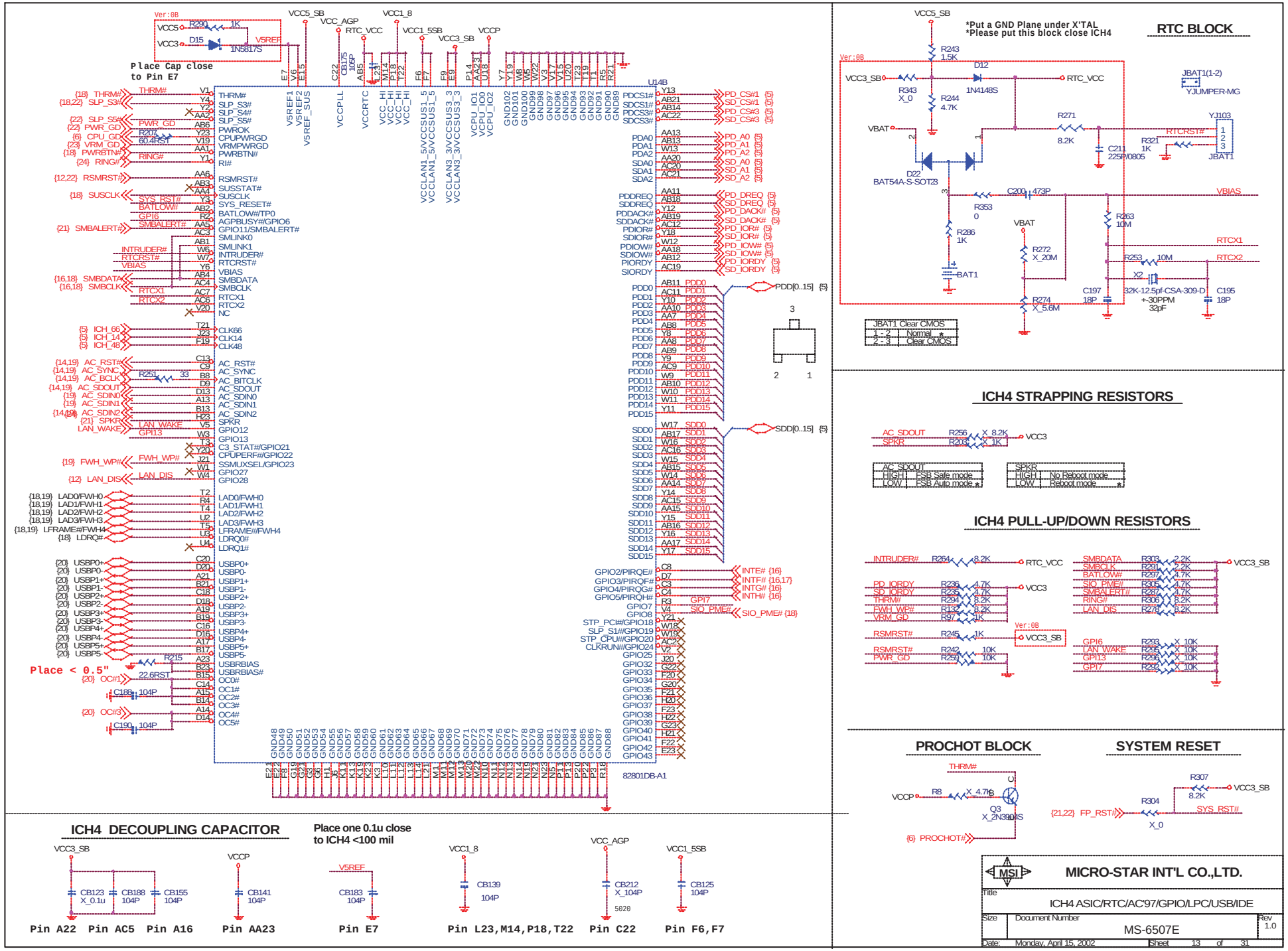
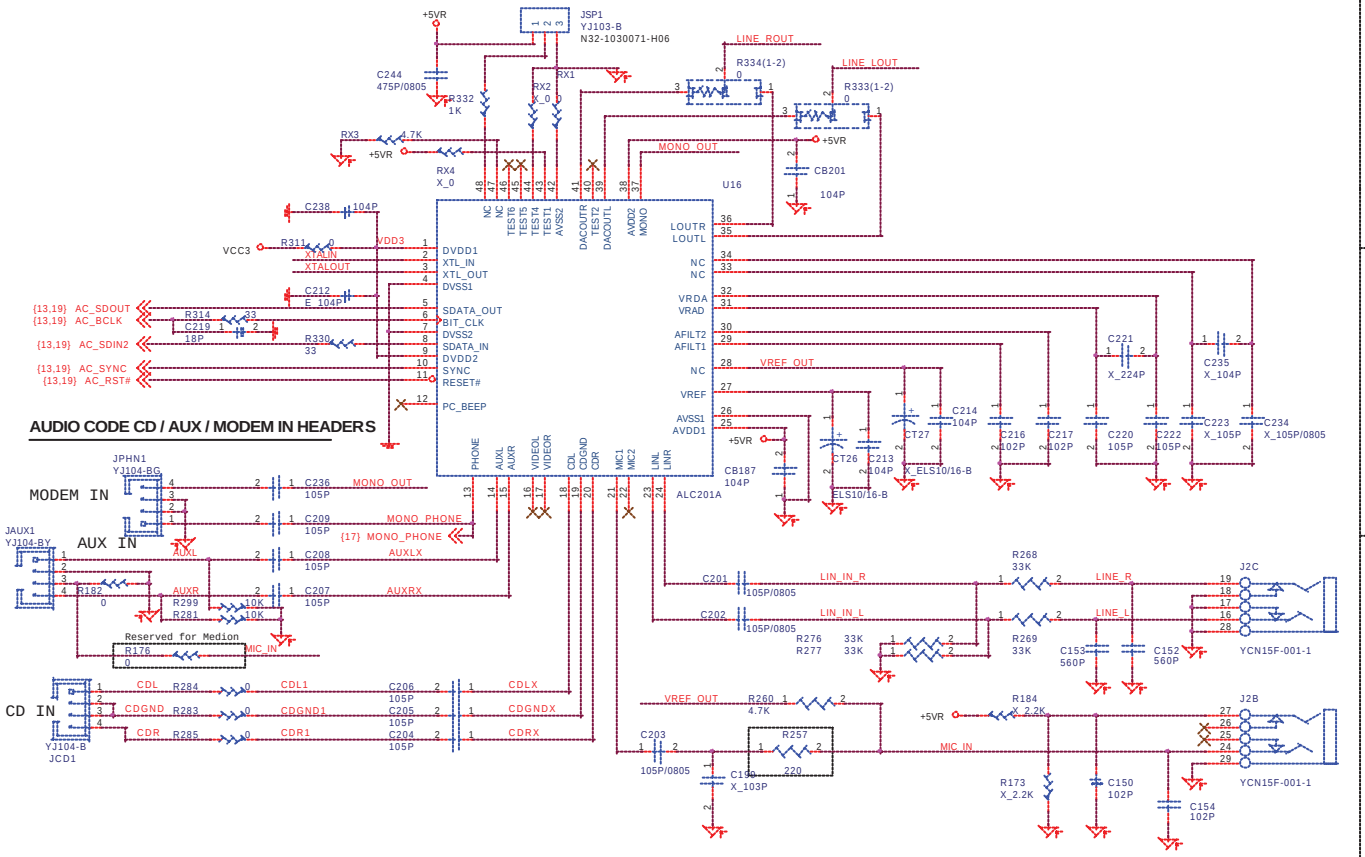
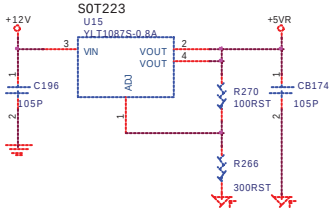

Place Cap close
to Pin E7
U14B
82801DB-A1
Place < 0.5"
RTC BLOCK
*Put a GND Plane under X'TAL
*Please put this block close ICH4
JBAT1 Clear CMOS
1 - 2 Normal *
2 - 3 Clear CMOS
ICH4 STRAPPING RESISTORS
AC_SDOUT
SPKR
HIGH FSB Safe mode
LOW FSB Auto mode *
HIGH No Reboot mode
LOW Reboot mode *
ICH4 PULL-UP/DOWN RESISTORS
PROCHOT BLOCK
SYSTEM RESET
ICH4 DECOUPLING CAPACITOR
Place one 0.1u close
to ICH4 <100 mil
Pin A22
Pin AC5
Pin A16
Pin AA23
Pin E7
Pin L23,M14,P18,T22
Pin C22
Pin F6,F7
MICRO-STAR INT'L CO.,LTD.
Title
ICH4 ASIC/RTC/AC'97/GPIO/LPC/USB/IDE
Size
Document Number
MS-6507E
Rev
1.0
Date: Monday, April 15, 2002
Sheet 13 of 31

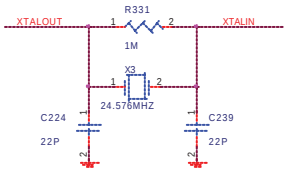
AC201A/AC202A AC97 CODEC



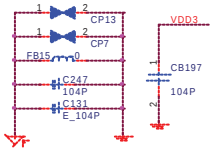
AUDIO CODE REGULATORS



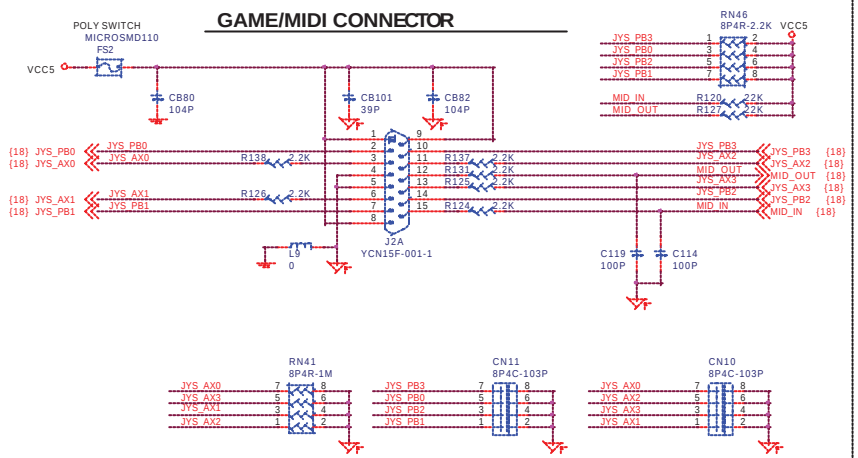
AUDIO CODE CRYSTAL CIRCUIT



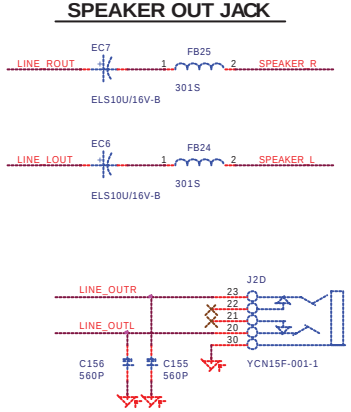
DECOUPLING CAPACITOR



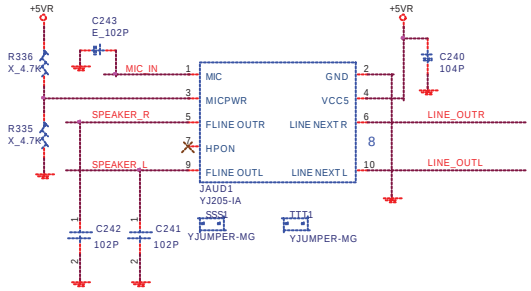
GAME/MIDI CONNECTOR



SPEAKER OUT JACK



Intel Front Audio Connector



Micro Star Restricted Secret

Title: AC97 CODEC AD1885	Rev: 1.0
Document Number: MS-6507E	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Monday, April 15, 2002
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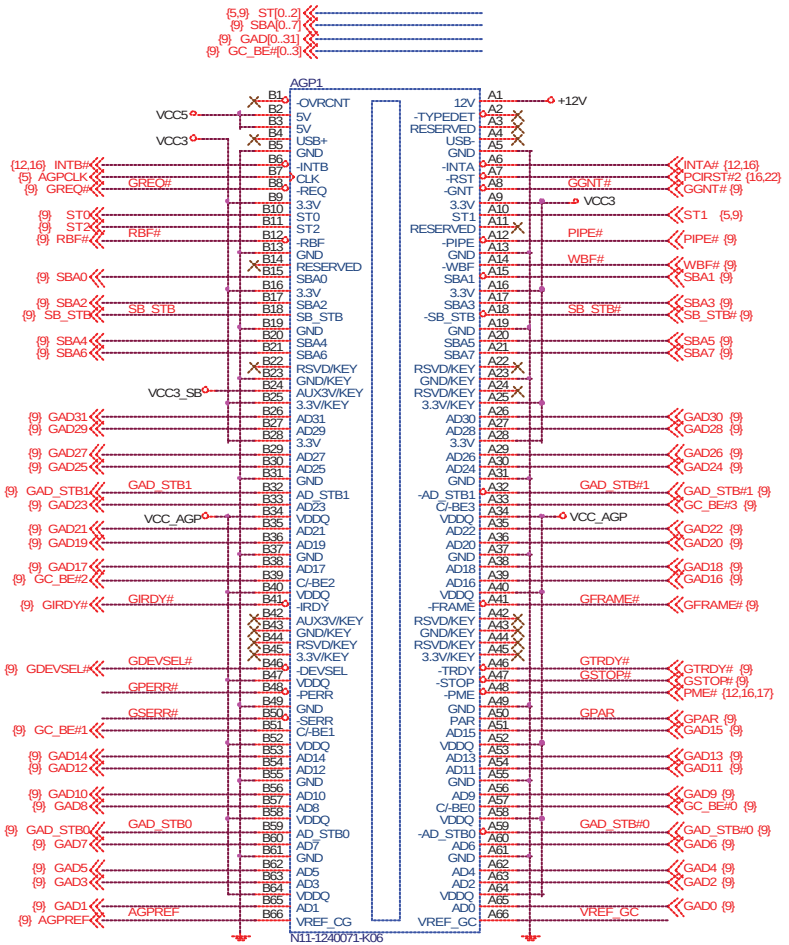
AGP UNIVERSAL 2X/4X SLOT(AGP VER:2.0 COMPLY)

VCC5 = 60mils trace / 15 mils space



VREF_GC:form the chipset to the graphics controller

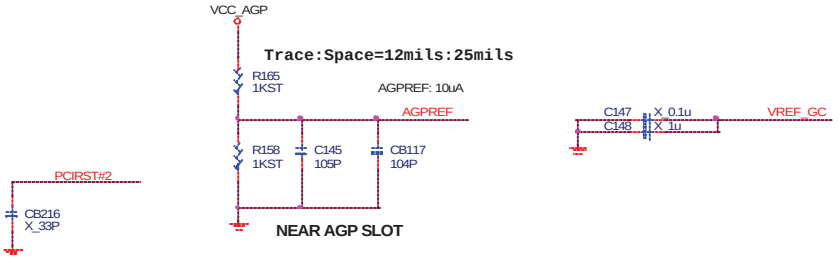
VREF_GC:form the graphics controller to the chipset

AGP Slot Imax

VCC_AGP 8.0A
VCC3 6.0A
VCC12 1.0A
VCC5 2.0A

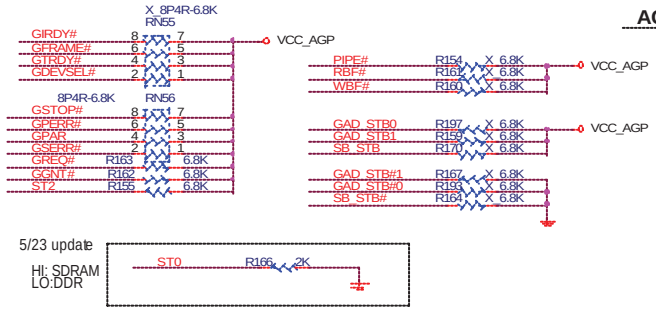
INTA#
INTB#

AGP SIGNAL REFERENCE CIRCUIT



NEAR AGP SLOT

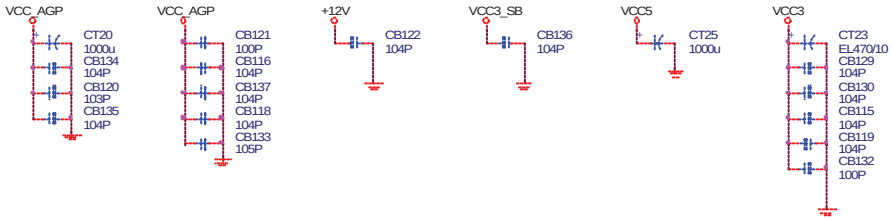
AGP TERMINATION RESISTORS



LESS 10MILS STUB TRACE LENGTH MUST BE FOLLOWING.

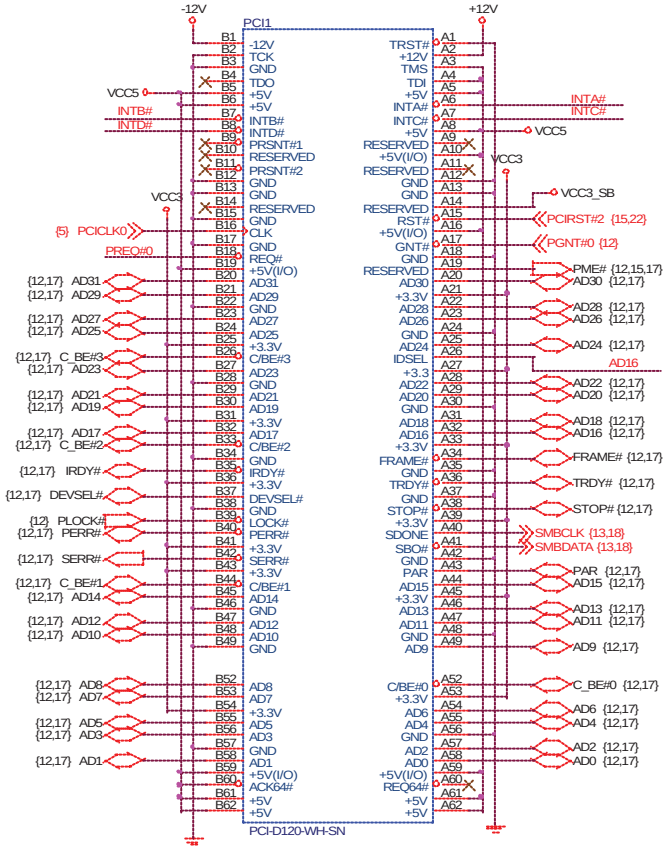
Place these resistors between PCI and AGP slot

AGP SLOT DECOUPLING CAPACITORS



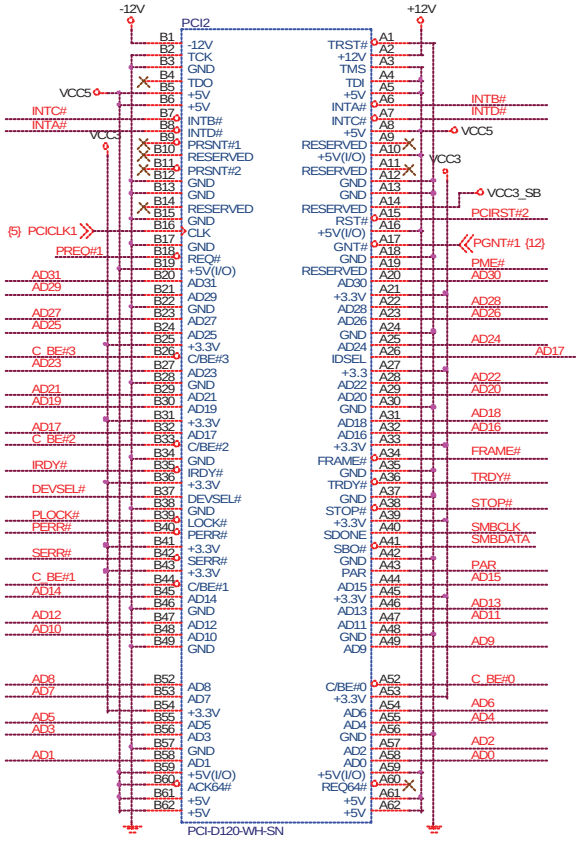
Micro-Star	Title: MS-6507E	Rev: 1.0
Document Number: AGP Slot		
Last Revision Date: Monday, April 15, 2002	Sheet 15 of 31	

PCI SLOT 1 (PCI VER: 2.2 COMPLY)



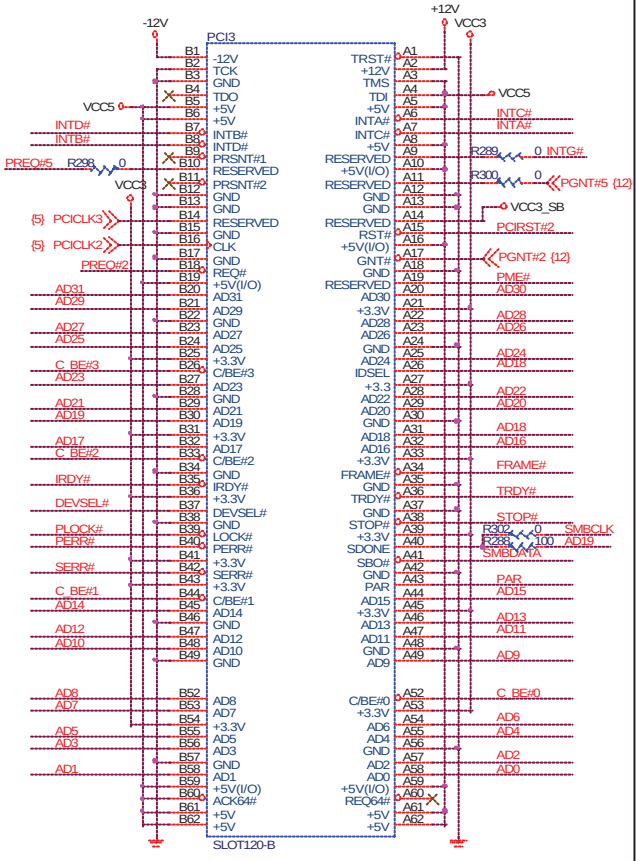
IDSEL = AD16
MASTER = PREQ0
INTA#

PCI SLOT 2 (PCI VER: 2.2 COMPLY)



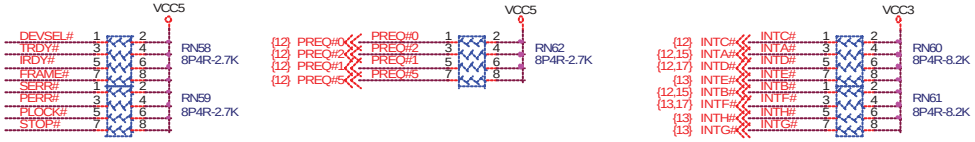
IDSEL = AD17
MASTER = PREQ1
INTB#

PCI SLOT 3 (PCI VER: 2.2 COMPLY)

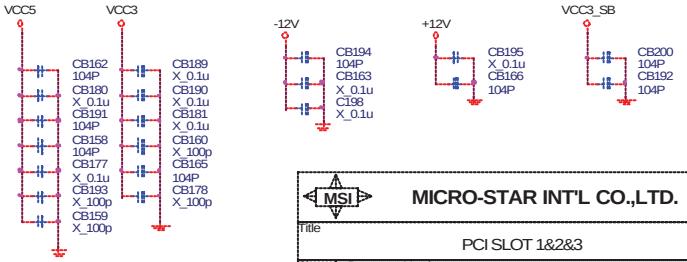


IDSEL = AD18
MASTER = PREQ2
INTC#

PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS

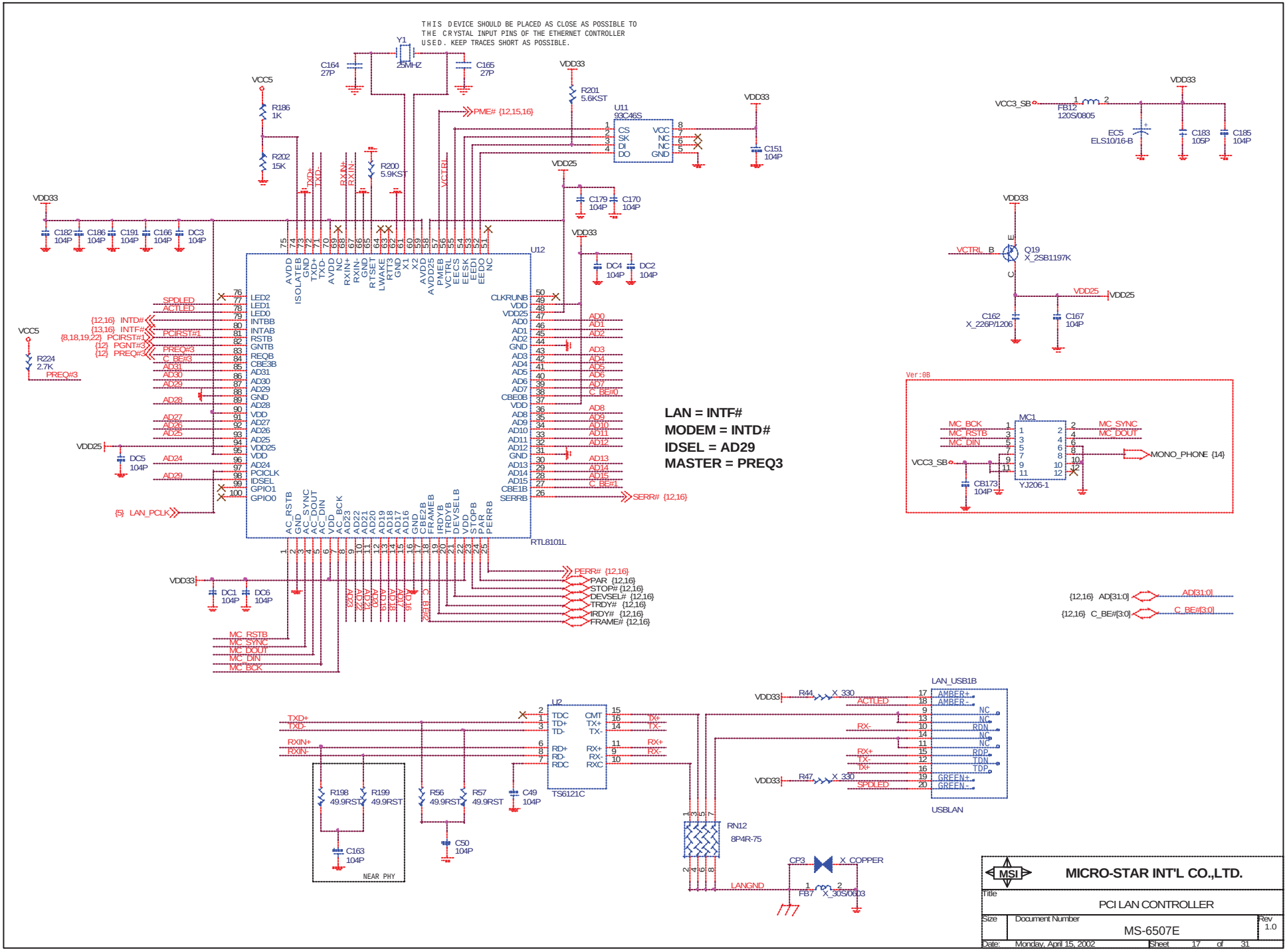


MSI **MICRO-STAR INT'L CO.,LTD.**

Title: PCI SLOT 1&2&3

Size | Document Number: MS-6507E | Rev: 1.0

Date: Monday, April 15, 2002 | Sheet 16 of 31


THIS DEVICE SHOULD BE PLACED AS CLOSE AS POSSIBLE TO THE CRYSTAL INPUT PINS OF THE ETHERNET CONTROLLER USED. KEEP TRACES SHORT AS POSSIBLE.
Y1
25MHZ
C164 27P
C165 27P
VCC5
R186 1K
R202 15K
R201 5.6KST
R200 5.9KST
U11 93C46S
CS SK DI DO VCC NC NC GND
PME# {12,15,16}
VCTRL
TXD+ TXD-
RXIN+ RXIN-
VDD33
VDD25
C179 104P
C170 104P
C182 104P
C186 104P
C191 104P
C166 104P
DC3 104P
DC4 104P
DC2 104P
C151 104P
U12
RTL8101L
AVDD ISOLATEB GND TXD+ TXD- AVDD NC RXIN+ RXIN- GND RTSET LWAKE RTI3 GND X1 X2 AVDD AVDD25 PMEB VCTRL EECS EESK EEDI EEDO NC
LED2 LED1 LED0 INTBB INTAB RSTB GNTB REQB CBE3B AD31 AD30 AD29 GND AD28 VDD AD27 AD26 AD25 VDD25 VDD AD24 PCICLK IDSEL GPIO1 GPIO0
CLKRUNB VDD VDD25 AD0 AD1 AD2 GND AD3 AD4 AD5 AD6 AD7 CBE0B VDD AD8 AD9 AD10 AD11 AD12 GND AD13 AD14 AD15 CBE1B SERRB
AC_RSTB GND AC_SYNC AC_SDOUT AC_DIN VDD AC_BCK AD23 AD22 AD21 AD20 AD19 AD18 AD17 AD16 GND CBE2B FRAMEB IRDYB TRDYB DEVSELB VDD STOPB PAR PERRB
SPDLED ACTLED
{12,16} INTD#
{13,16} INTF#
{8,18,19,22} PCIRST#1
{12} PGNT#3
{12} PREQ#3
PCIRST#1
PREQ#3
C_BE#3
AD31 AD30 AD29 AD28 AD27 AD26 AD25 AD24 AD29
R224 2.7K
PREQ#3
DC5 104P
{5} LAN_PCLK
SERR# {12,16}
PERR# {12,16}
PAR {12,16}
STOP# {12,16}
DEVSEL# {12,16}
TRDY# {12,16}
IRDY# {12,16}
FRAME# {12,16}
DC1 104P
DC6 104P
MC_RSTB
MC_SYNC
MC_DOUT
MC_DIN
MC_BCK
LAN = INTF#
MODEM = INTD#
IDSEL = AD29
MASTER = PREQ3
VCC3_SB
FB12 120S0805
EC5 ELS10/16-B
C183 105P
C185 104P
VCTRL_B
Q19 X_2SB1197K
C162 X_226P/1206
C167 104P
Ver:0B
MC1
MC_BCK MC_RSTB MC_DIN MC_SYNC MC_DOUT
MONO_PHONE {14}
CB173 104P
YJ206-1
{12,16} AD[31:0]
AD[31:0]
{12,16} C_BE#[3:0]
C_BE#[3:0]
U2
TS6121C
TDC TD+ TD- CMT TX+ TX- RD+ RD- RDC RX+ RX- RXC
TX+ TX- RX+ RX-
R198 49.9RST
R199 49.9RST
R56 49.9RST
R57 49.9RST
C49 104P
C50 104P
C163 104P
NEAR PHY
RN12 8P4R-75
LAN_USB1B
R44 X_330
R47 X_330
ACTLED
SPDLED
AMBER+ AMBER- NC NC RDN NC NC RDP TDN TDP GREEN+ GREEN-
USBLAN
CP3 X_COPPER
FB7 X_30S/0603
LANGND
MSI
MICRO-STAR INT'L CO.,LTD.
Title
PCI LAN CONTROLLER
Size
Document Number
MS-6507E
Rev 1.0
Date: Monday, April 15, 2002
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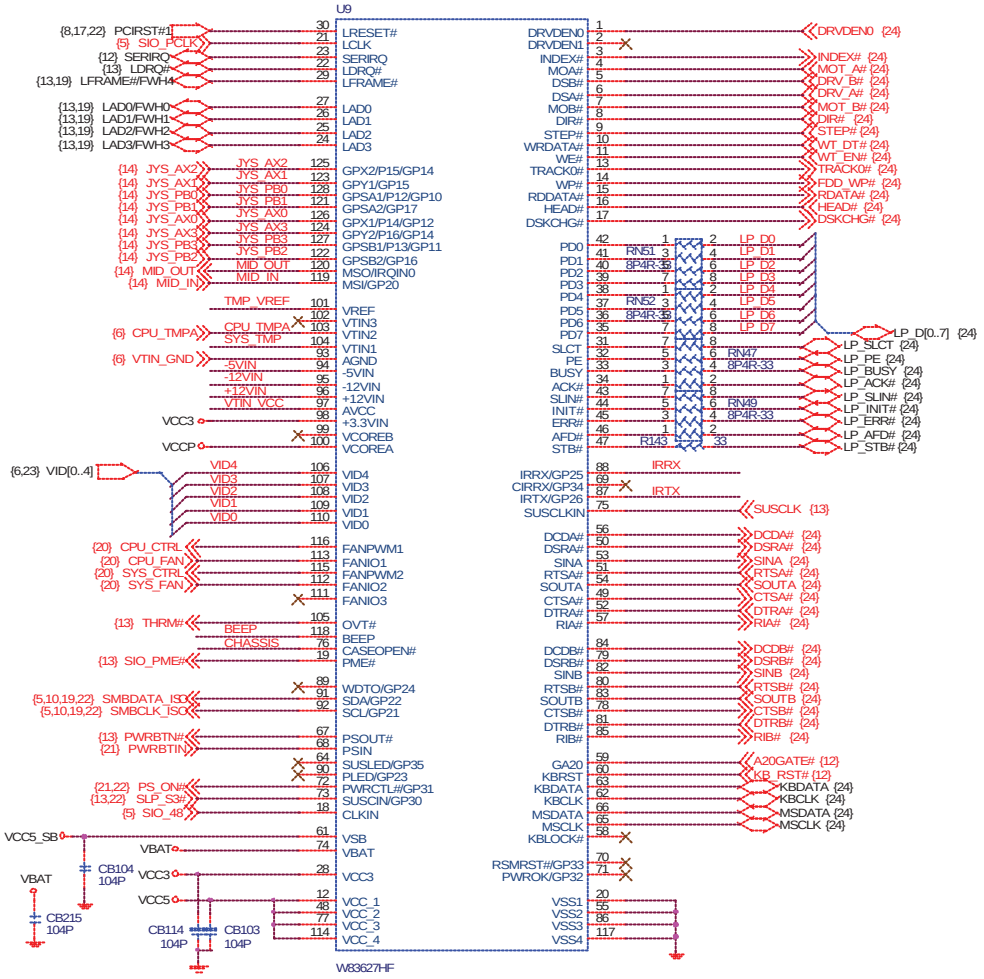
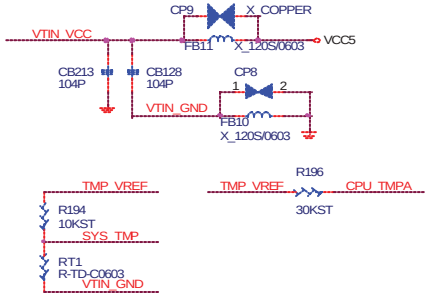
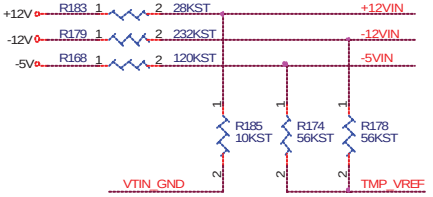
LPC SUPER I/O W83627HF

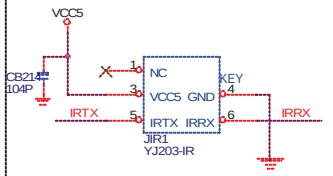


THERMAL RESISTOR BLOCK

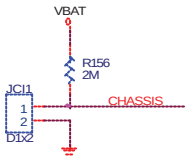




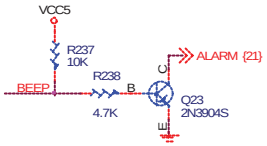
Intel Front IR Header



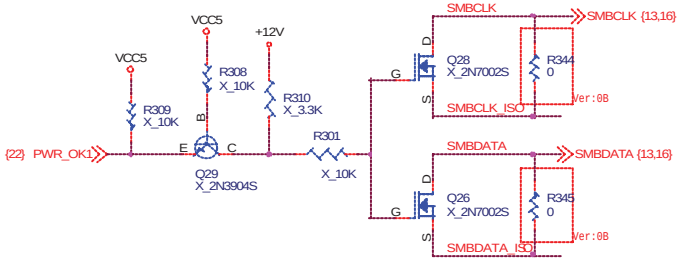
Chasiss Intrusion Header



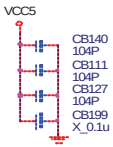
SPEAKER BLOCK



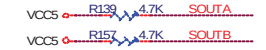
SMBus Isolation



LPC I/O DECOUPLING CAPACITORS



SUPER I/O STRAPPING RESISTOR



SOUTA	L: Disable KBC	H: Enable KBC
SOUTB	L: 24MHZ	H: 48MHZ
RTSA#	L: CFAD=2E	H: CFAD=4E
DTRA#	L: PNP Default	H: PNP no Default

MSI MICRO-STAR INT'L CO.,LTD.

Title: LPC IO & GAME PORT

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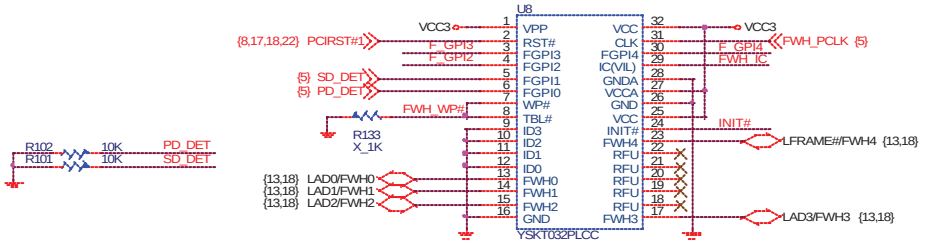
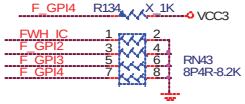
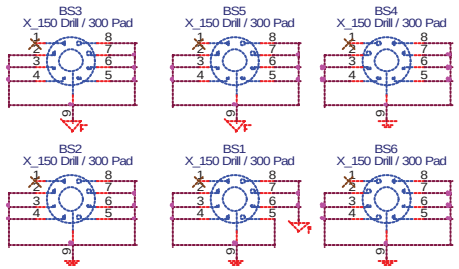
Firware Hub (FWH)



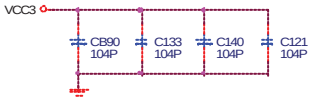
FWH RESISTORS



PCB Mounting Holes

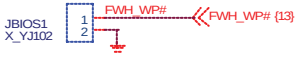


FWH DECOUPLING CAPACITORS



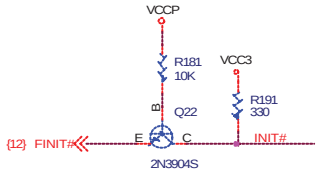
Place Cap. as Close to FWH< 350 mil

FWH write protect

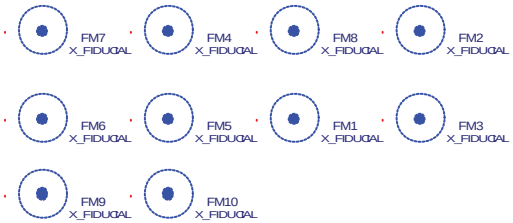


J7 BIOS Update	
SHORT	Locked
OPEN	Unlocked *

FWH INIT Signal Voltage Translation Block

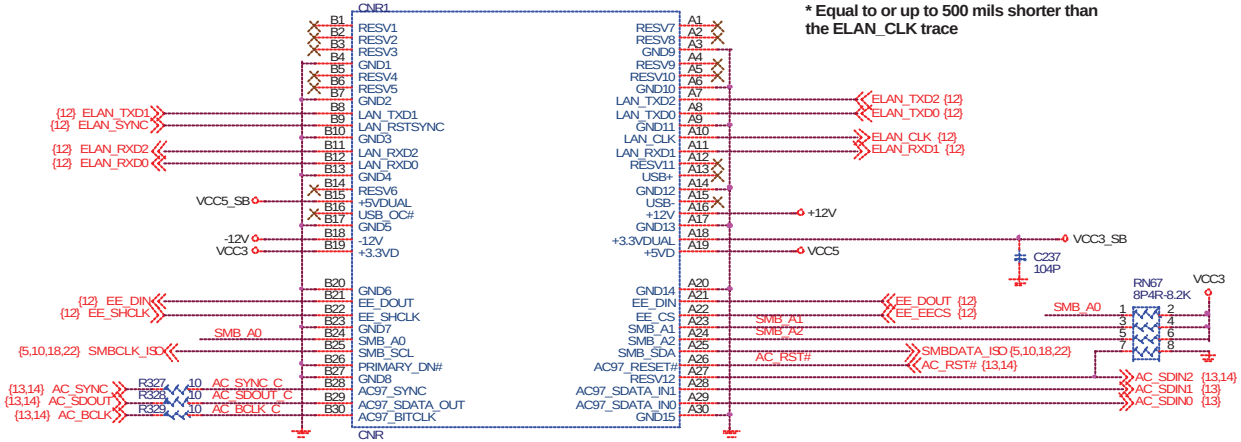


PCB Fiducials



SIMULATION TRACE

CNR RISER



*** LAN Trace width : 5 mils**

*** AC'97 Trace Spacing : 10 mils**

*** Maxium trace length < 9.5"**

*** Equal to or up to 500 mils shorter than the ELAN_CLK trace**

MSI **MICRO-STAR INT'L CO.,LTD.**

Title	FWH & CNR	
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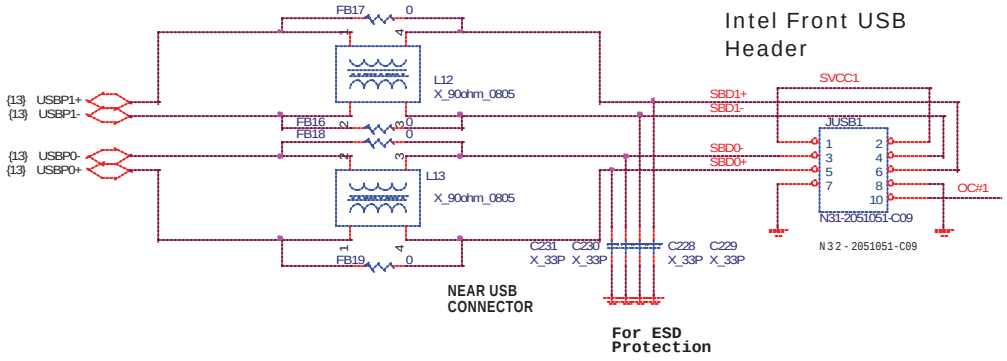
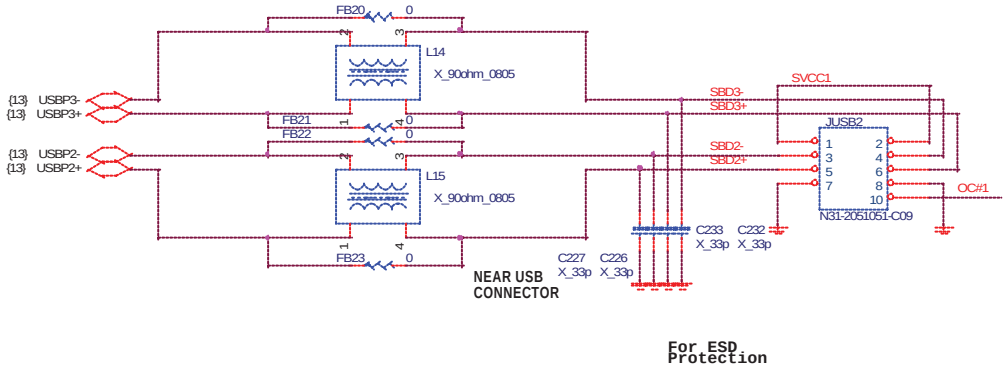
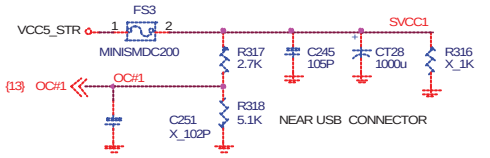
FRONT PANEL USB CONNECTOR FOR USB PORT 0,1



FRONT PANEL USB CONNECTOR FOR USB PORT 2,3

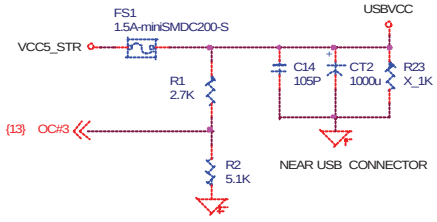


POWER CIRCUIT FOR USB PORT 0,1,2,3

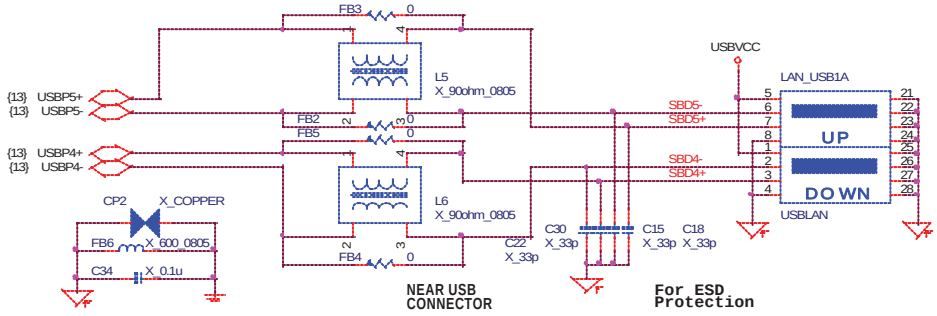


* USB Trace width : 7.5 mils
* USB Trace Spacing : 20 mils
* Differential USB Signlas Trace, Spacing : 18 mils
* USB Power Trace must be 40mils width

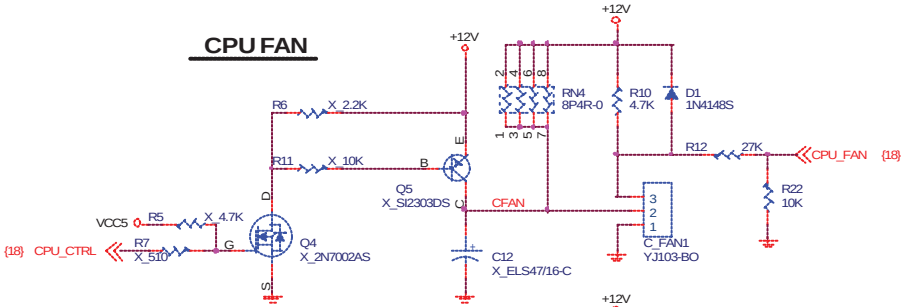
POWER CIRCUIT FOR USB PORT 4,5



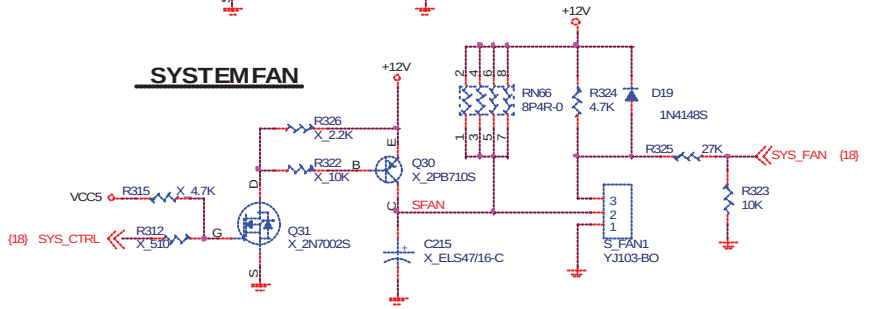
REAR PANEL USB CONNECTOR FOR USB PORT 4,5



CPU FAN



SYSTEM FAN



MSI **MICRO-STAR INT'L CO.,LTD.**

Title	USB CONNECTORS	
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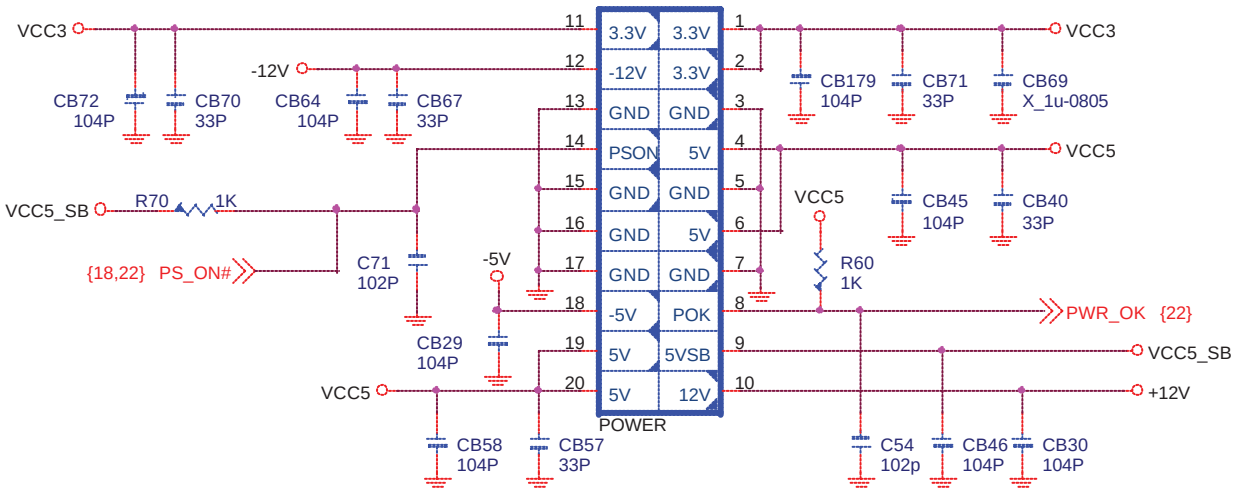
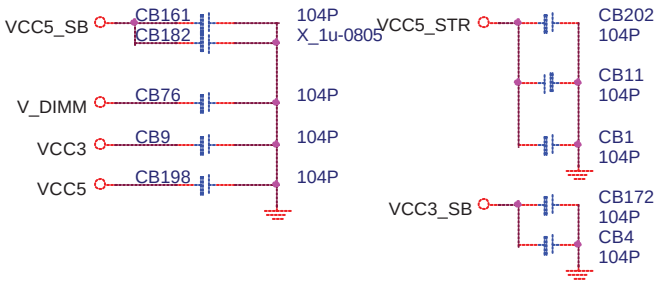
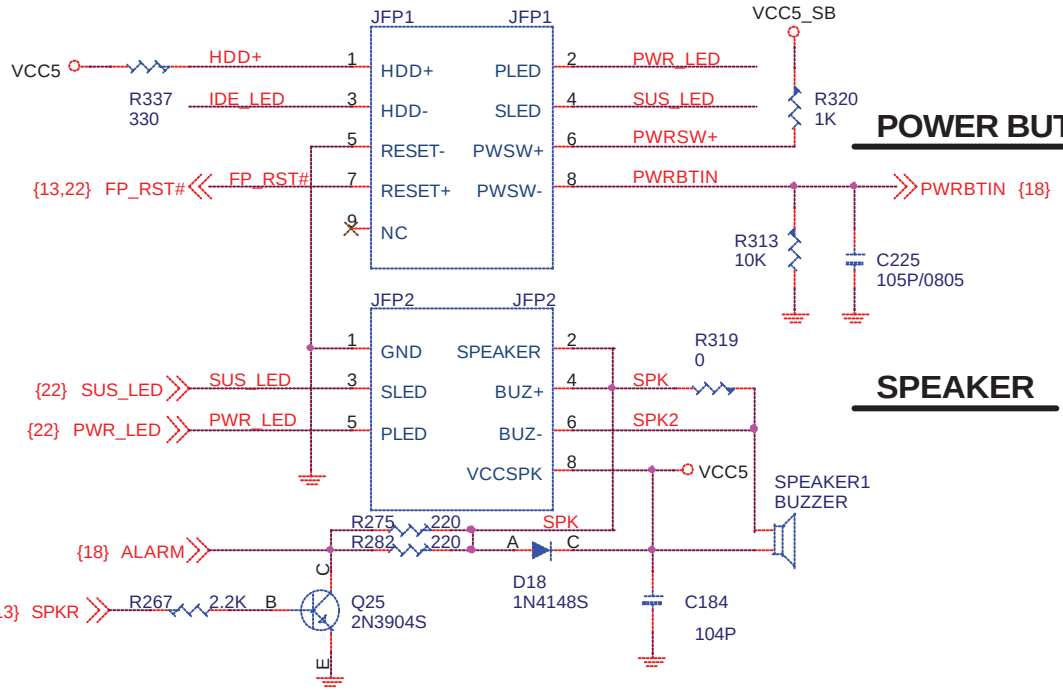
ATX CONNECTOR



REGULATORS OUTPUT DECOUPLING CAPACITORS

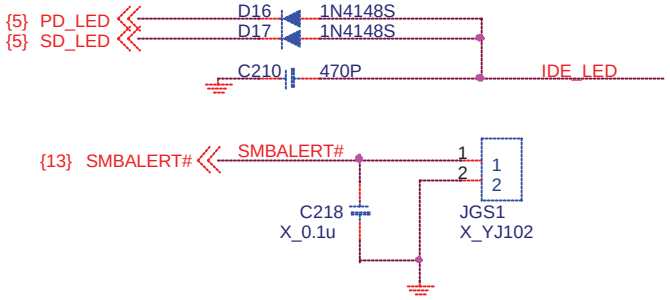


MSI/Intel Front Panel



POWER BUTTON

SPEAKER



MICRO-STAR INT'L CO.,LTD.	
Title	Front Panel & ATX Connector & FAN
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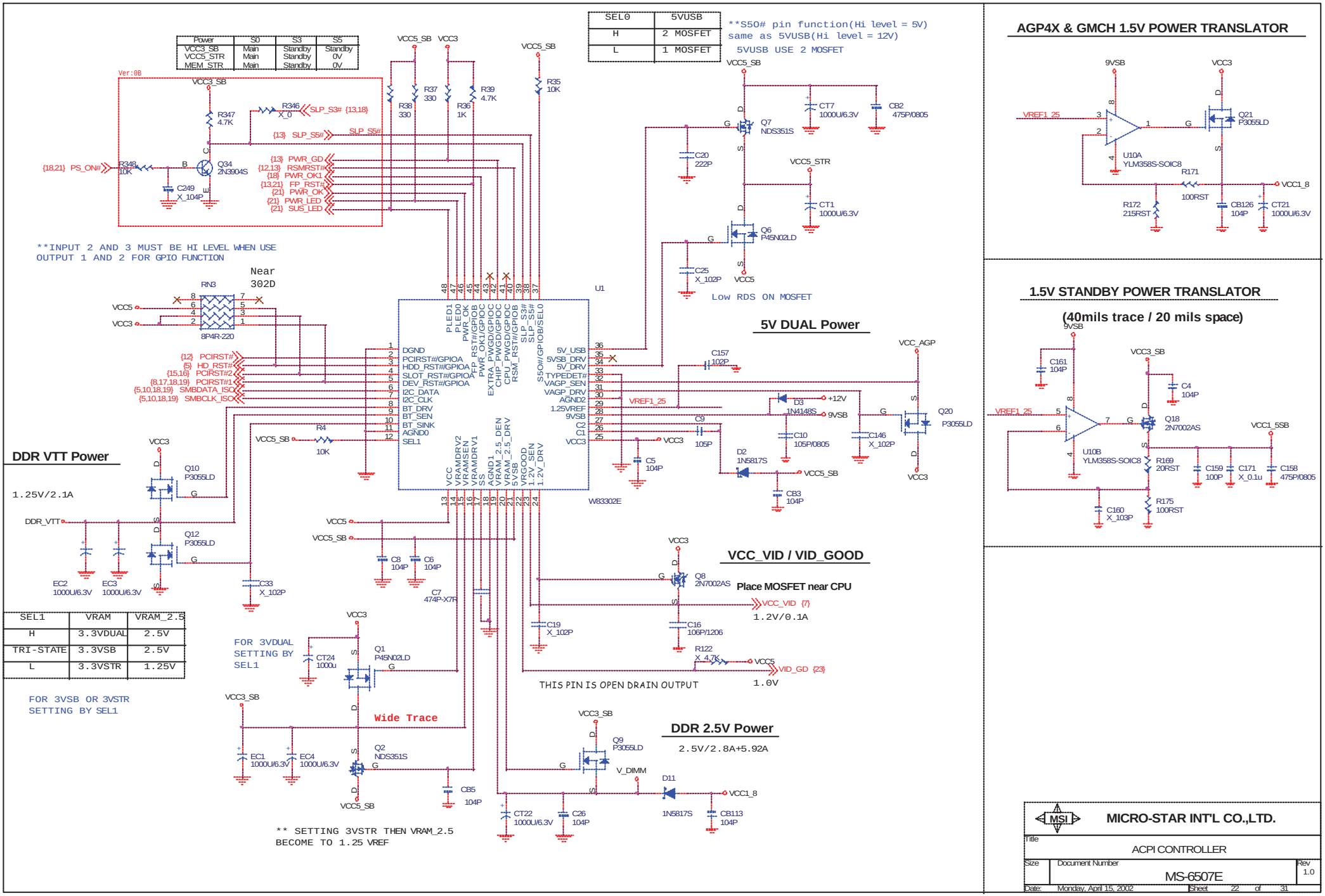
Power | S0 | S3 | S5
VCC3_SB | Main | Standby | Standby
VCC5_STR | Main | Standby | 0V
MEM_STR | Main | Standby | 0V
SEL0 | 5VUSB
H | 2 MOSFET
L | 1 MOSFET
**S5O# pin function(Hi level = 5V)
same as 5VUSB(Hi level = 12V)
5VUSB USE 2 MOSFET
Ver:0B
**INPUT 2 AND 3 MUST BE HI LEVEL WHEN USE
OUTPUT 1 AND 2 FOR GPIO FUNCTION
Near
302D
RN3
8P4R-220
Low RDS ON MOSFET
5V DUAL Power
W83302E
DDR VTT Power
1.25V/2.1A
VCC_VID / VID_GOOD
Place MOSFET near CPU
1.2V/0.1A
THIS PIN IS OPEN DRAIN OUTPUT
1.0V
DDR 2.5V Power
2.5V/2.8A+5.92A
Wide Trace
FOR 3VDUAL
SETTING BY
SEL1
FOR 3VSB OR 3VSTR
SETTING BY SEL1
SEL1 | VRAM | VRAM_2.5
H | 3.3VDUAL | 2.5V
TRI-STATE | 3.3VSB | 2.5V
L | 3.3VSTR | 1.25V
** SETTING 3VSTR THEN VRAM_2.5
BECOME TO 1.25 VREF
AGP4X & GMCH 1.5V POWER TRANSLATOR
U10A
YLM358S-SOIC8
1.5V STANDBY POWER TRANSLATOR
(40mils trace / 20 mils space)
U10B
YLM358S-SOIC8
MSI
MICRO-STAR INT'L CO.,LTD.
Title
ACPI CONTROLLER
Size
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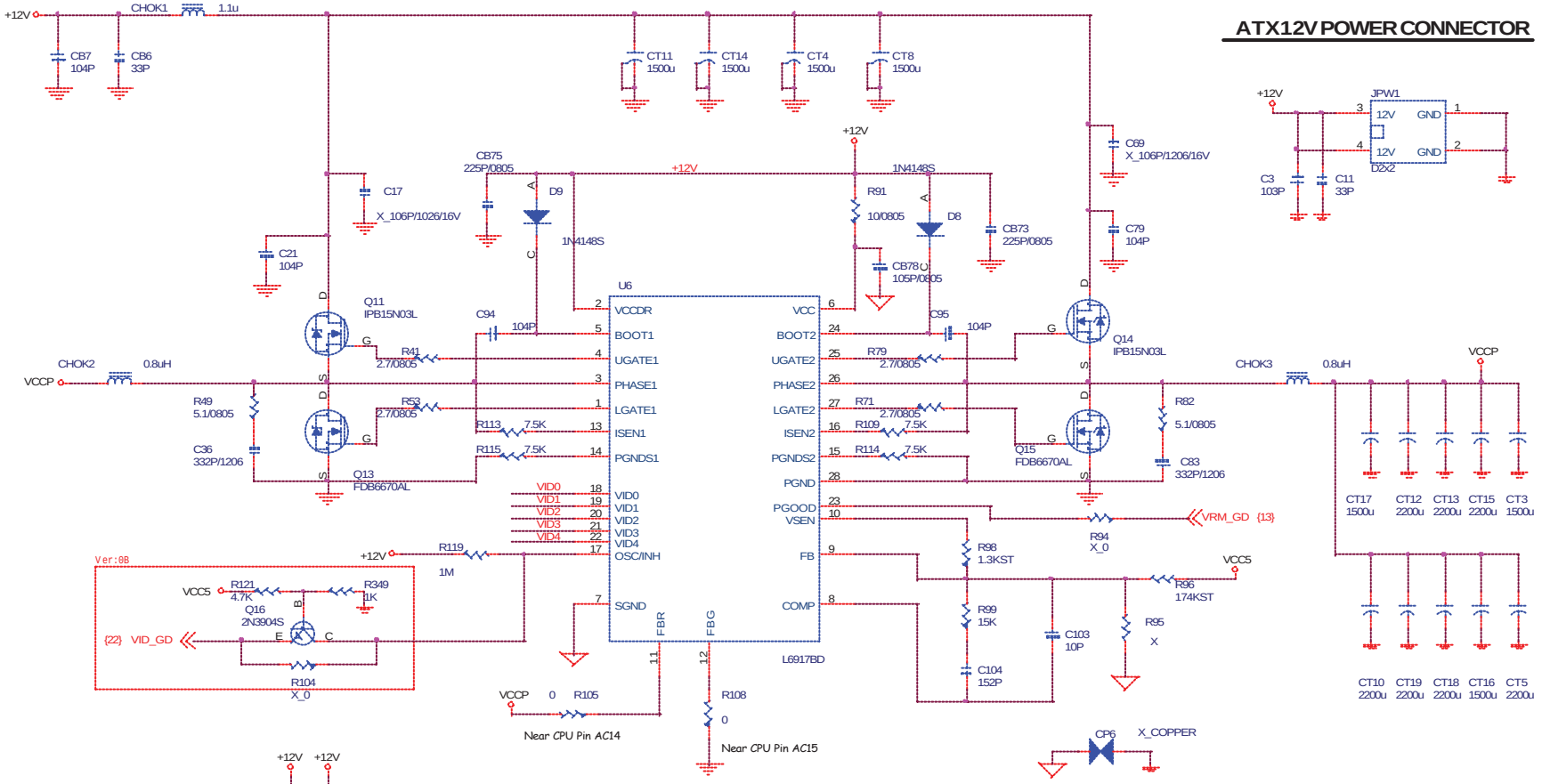
ATX12V POWER CONNECTOR



VID4	VID3	VID2	VID1	VID0	VDC(V)
1	1	1	1	0	1.100
1	1	1	0	1	1.125
1	1	1	0	0	1.150
1	1	0	1	1	1.175
1	1	0	1	0	1.200
1	1	0	0	1	1.225
1	1	0	0	0	1.250
1	0	1	1	1	1.275
1	0	1	1	0	1.300
1	0	1	0	1	1.325
1	0	1	0	0	1.350
1	0	0	1	1	1.375

VID4	VID3	VID2	VID1	VID0	VDC(V)
1	0	0	1	0	1.400
1	0	0	0	1	1.425
1	0	0	0	0	1.450
0	1	1	1	1	1.475
0	1	1	1	0	1.500
0	1	1	0	1	1.525
0	1	1	0	0	1.550
0	1	0	1	1	1.575
0	1	0	1	0	1.600
0	1	0	0	1	1.625
0	1	0	0	0	1.650
0	0	1	1	1	1.675

VID4	VID3	VID2	VID1	VID0	VDC(V)
0	0	1	1	0	1.700
0	0	1	0	1	1.725
0	0	1	0	0	1.750
0	0	0	1	1	1.775
0	0	0	1	0	1.800
0	0	0	0	1	1.825
0	0	0	0	0	1.850
1	1	1	1	1	OFF

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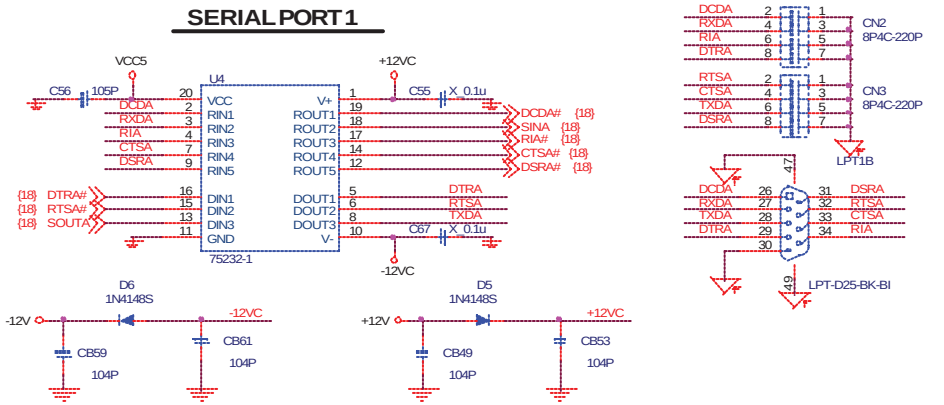
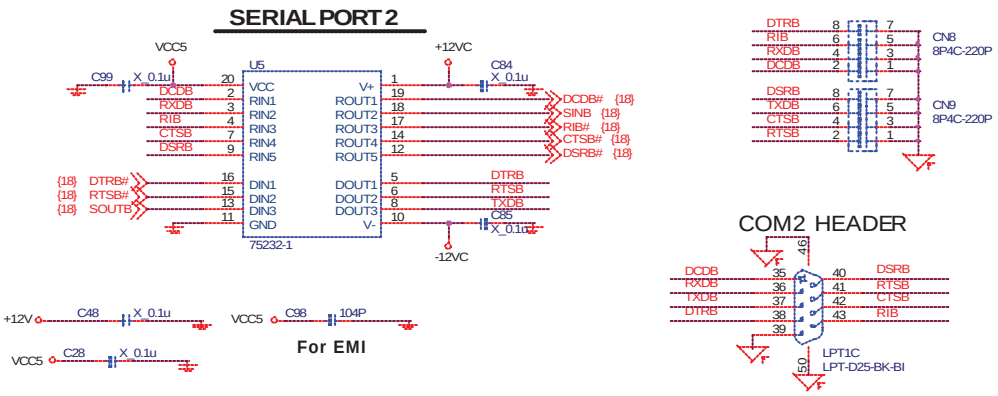
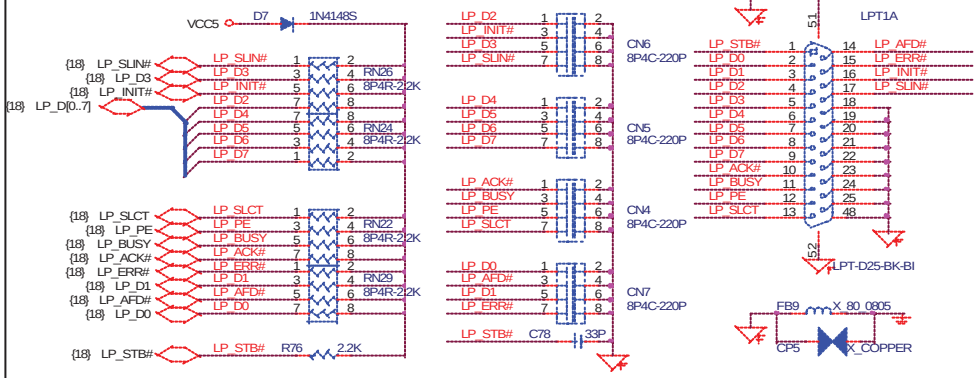
SERIAL PORT 1



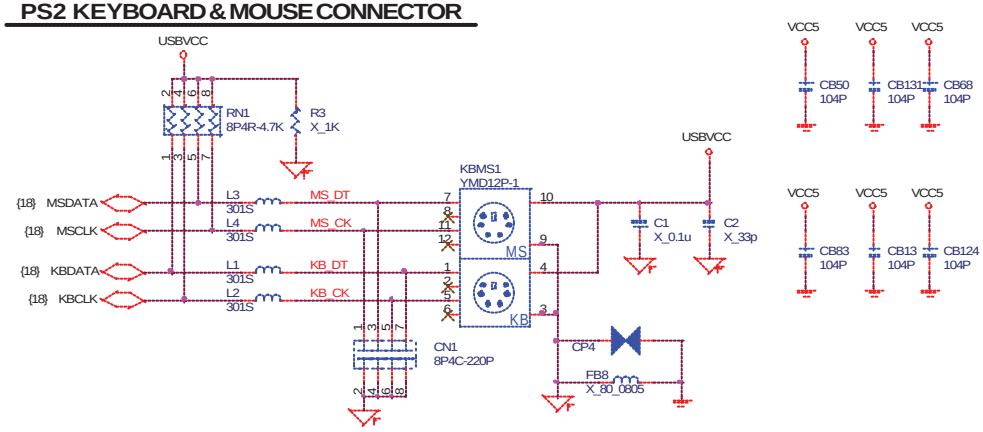
SERIAL PORT 2



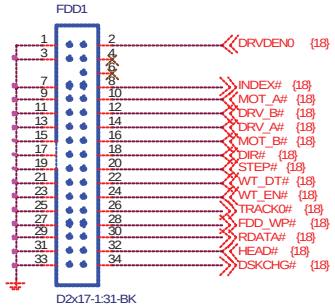
PARALLAL PORT



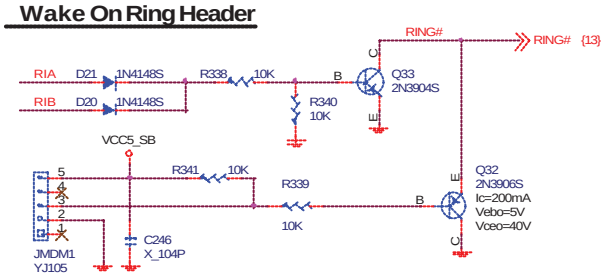
PS2 KEYBOARD & MOUSE CONNECTOR

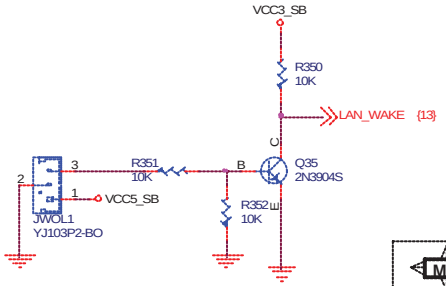


FLOPPY CONNECTOR



Wake On Ring Header





MSI **MICRO-STAR INT'L CO.,LTD.**

Title	I/O CONNECTORS	
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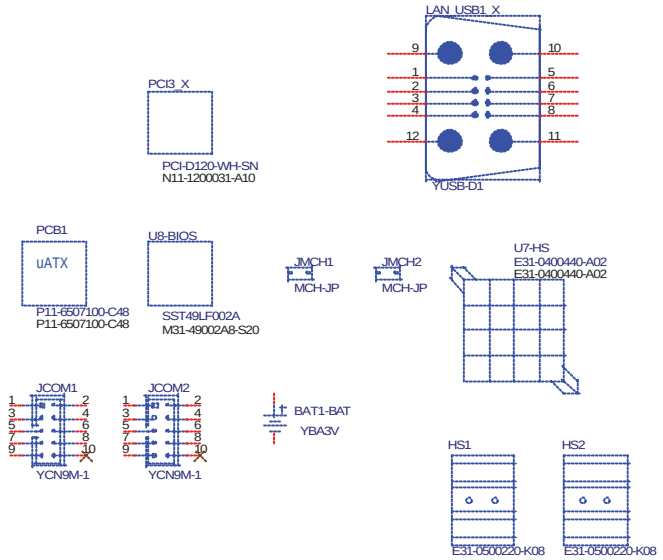
0B Revision History (Changes from Rev 0A)

Sheet	Desciption
22	Change MS5 SLP_S3# Singnal source from PS_ON#.
18	Add two Resistor between Q26 and Q28 Drain and Source.
23	Change CP6 PCBFootPrint from JP to NC.
17	Swap MC1 Pin.1 & Pin.2
13	Change RSMRST# Pull-Up to VCC3_SB. Change THERMTRIP# Damp R217 be a VCCP Pull-Up Resistor. Change RTC Block Circuit.
12	Add Damping Resistor on PCIRST# for decrease PCIRST# OverShoot and UnderShoot on MS5.

Jumper Setting & Connector Setting

Jumper	Description	
JAUDIO1	AUDIO FRONT PANEL HEADPHONE JACK HEADER	
JBAT1	CLEAR CMOS	
1-2	NORMAL	(Default)
2-3	CLEAR CMOS	

Connector	Description
U7	INTEL mPGA478-B CPU
PRIMAR1	Primary
SECON1	Secondary
DIMM1	SDRAM DIMM1
DIMM2	SDRAM DIMM2
AGP1	AGP Slot
PCI1	PCI Slot1
PCI2	PCI Slot2
PCI3	PCI Slot3(MEDION SPEC)
COM1	Serial Port
COM2	Serial Port
LPT1	Parallel Port
FDD1	Floopy
JMDM1	MODEM RING HEADER
KBMS1	PS/2 Keyboard and PS/2 mouse
C_FAN1	CPU FAN HEADER
LAN_USB1	LAN&USB REAR CONNECTOR
USB1	USB INTERNAL HEADER
USB2	USB INTERNAL HEADER
CONN1	ATX Power
JFP1	INTEL Front Panel
JFP2	MSI Front Panel
JPW1	ATX12V Power



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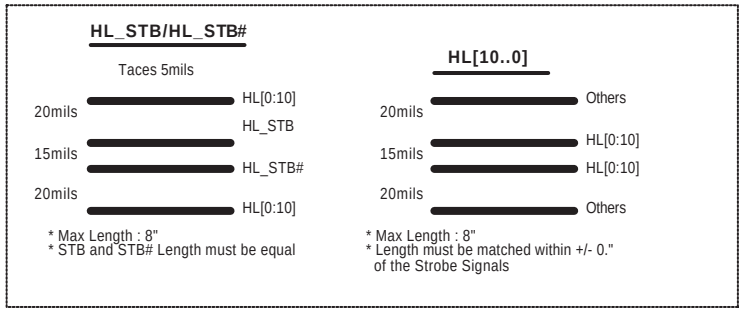
Pentium 4 Processor /Northwood mPGA 478

Source Synchronous Signal Group and the Associated Strobes

Signals	Associated Strobe
REQ[4:0],A[16:3]#	ADSTB0#
A[31:17]#	ADSTB1#
D[15:0]#,DBI0#	DSTBP0#,DSTBN0#
D[31:16]#,DBI1#	DSTBP1#,DSTBN1#
D[47:32]#,DBI2#	DSTBP2#,DSTBN2#
D[63:48]#,DBI3#	DSTBP3#,DSTBN3#

Signals	Length	Inaccuracy
Data	**2.0" to 10.0"**	+/- 100 mil
Address	**2.0" to 10.0"**	+/- 200 mil
Strobe	**2.0" to 10.0"**	+/- 25 mil
Clock	**2.0" to 10.0"**	Don't need

***** Delta=(CPU_pkglen.net-CPUpkglen.strobe)+(CS_pkglen.net-CS_pkglen.strobe)
Trace : 7 mil width 13mil space



Miscellaneous Signals

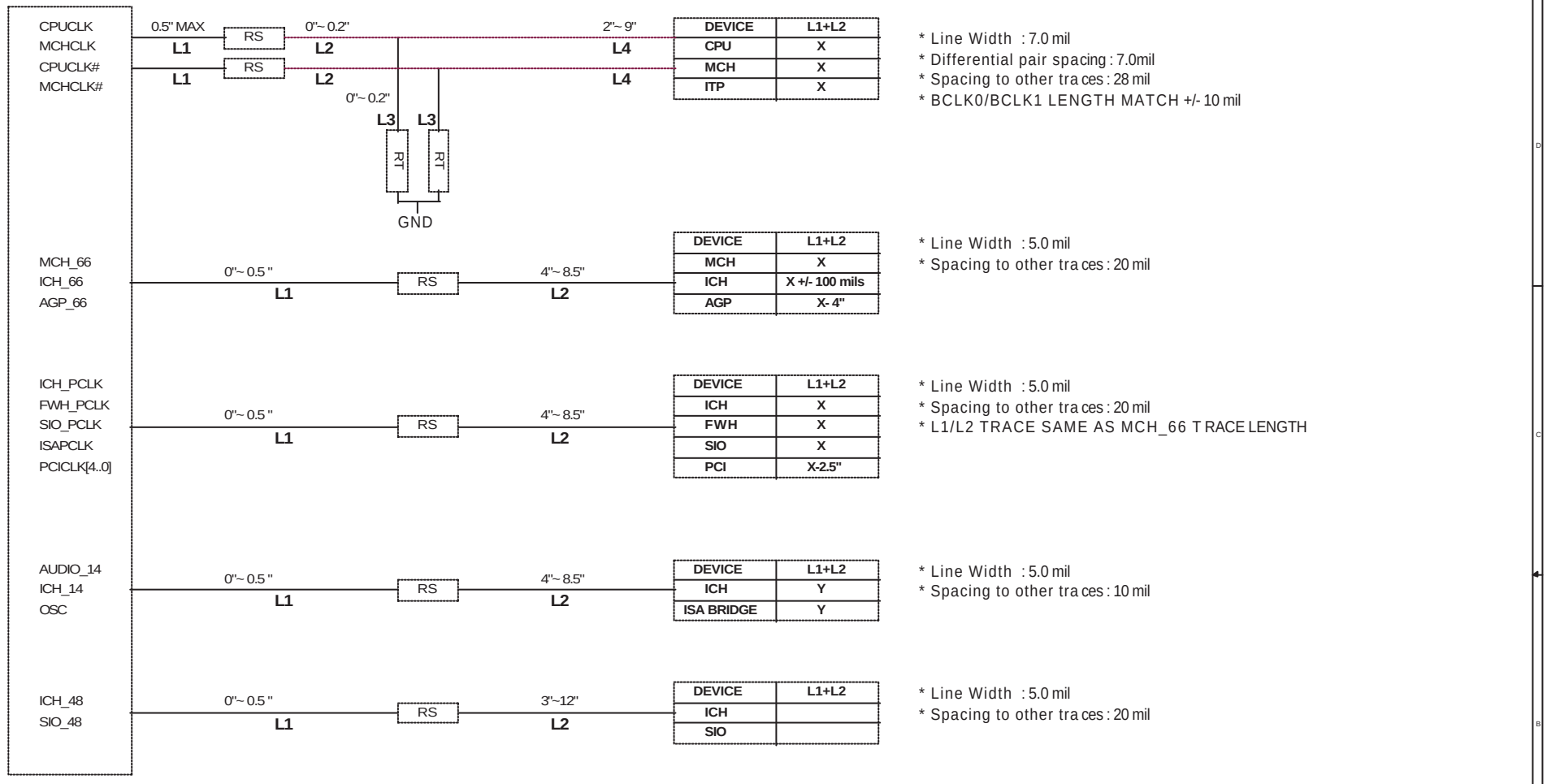
AGP

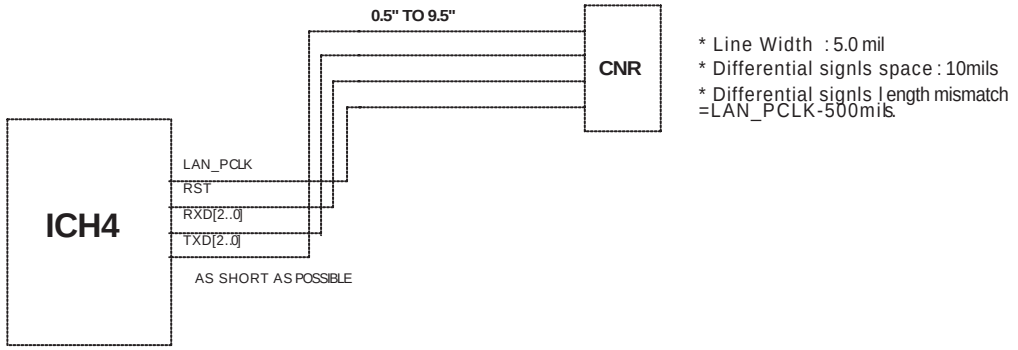
1X Timing group	2X/4X Timing group
AGPCLK PIPE# RBF# WBF# ST[2..0] GFRAME# GIRDY# GTRDY# GSTOP# GDEVSEL# GREQ# GGNT# GPAR	SET#1 GAD[15..0] GC_BE#[1..0] GAD_STB0 GAD_STB0# SET#2 GAD[31..16] GC_BE#[3..2] GAD_STB1 GAD_STB1# SET#3 SBA[7..0] SB_STB SB_STB#

SIGNALS	Maximum Length	Width	Space	Dismatch Length	Relative to
1X Timing group	7.5"	5 mil	5 mil	X	X
2X/4X Timing group SET#1	7.25"	5 mil	20 mil	+/- 0.125"	GAD_STB0 GAD_STB0#
2X/4X Timing group SET#2	7.25"	5 mil	20 mil	+/- 0.125"	GAD_STB1 GAD_STB1#
2X/4X Timing group SET#3	7.25"	5 mil	20 mil	+/- 0.125"	SB_STB SB_STB#
2X/4X Timing group SET#1	6"	5 mil	15 mil	+/- 0.25"	GAD_STB0 GAD_STB0#
2X/4X Timing group SET#2	6"	5 mil	15 mil	+/- 0.25"	GAD_STB1 GAD_STB1#
2X/4X Timing group SET#3	6"	5 mil	15 mil	+/- 0.25"	SB_STB SB_STB#

USB

- *** USB Trace width : 7.5 mils**
- *** Differential USB Signlas Trace Spacing : 7.5 mils**
- *** USB Trace Spacing with other signals: 20 mils**
- *** USB Power Trace must be 40mils width**





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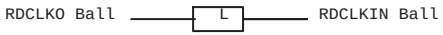
SDRAM Routing Guidelines

5.Feedback - RDCLKO,RDCLKIN routing rule

2 or 3 DIMM feedback layout guideline

Signal	Length	Width	Trace Spacing
Trace L	50 mils	7 mil	5 mil



DDR-SDRAM Routing Guidelines

1.DDR bus reference plane stack-up

PCB Layer	Description
Layer 1	Signal
Layer 2	Ground Flood
Layer 3	Ground
Layer 4	Power / Signal

***All the memory bus signals must be referenced to GND**

2.DDR signal groups

Group	Signals
Data	SDQ[63:0],SCB[7:0],SDQS[8:0]
Command	SMA[12:0],SBS[1:0],SRAS#,SCAS#,SWE#
Control	SCKE[3:0],SCS#[3:0]
Clock	SCK[5:0],SCK#[5:0]
Feedback	RCVENOUT#,RCVENIN#

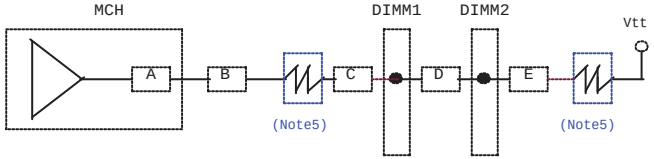
SDQS[8:0] were Data Strobes.

3.SDQ[63:0],SCB[7:0],SDQS[8:],SCK/SCK#[5:0]routing rule

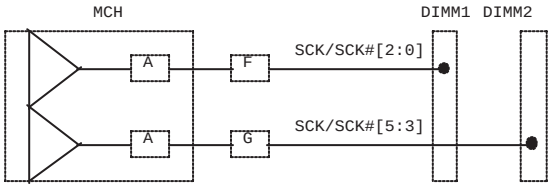
Signal	Length A	Length B	Length C	Length D	Length E	Width	Spacing	Routing Layer
SDQ[63:0] SCB[7:0] SQDS[8:0]	Package length	2.0" - 5.0"	Max = 0.5"	0.3' - 0.5"	0.1" - 0.8"	5 mil	(Note2)	Top
(Note1)	DIMM 1 = A + B + C = X DIMM 2 = A + B + C + D = X + D							
SCK/SCK#[2:0]	Package length	B+C+2"<= Length F <= B+C+1" 2.0" - 6.5"		None	None	5 mil	(Note4)	Bottom
	DIMM 1 = A + F = X + 1" to X + 2"							
SCK/SCK#[5:3] (Note3)	Package length	B+C+D+2"<= Length G <= B+C+D+1" 2.5" - 7.0"				5 mil	(Note4)	Bottom
	DIMM 2 = A + G = X + D + 1" to X + D + 2"							

*** Package length see Table - 4**

SDQ[63:0],SCB[7:0],SDQS[8:] layout guideline



SCK[5:0] layout guideline



Note1:Each data and strobe signal group must be length matching +/- 25 mils

SDQS[X] = +/- 25 mils SDQ[X]/SCB[X] group length

Signals	Associated Strobe
SDQ[7:0]	SDQ0
SDQ[15:8]	SDQ1
SDQ[23:16]	SDQ2
SDQ[31:17]	SDQ3
SDQ[39:32]	SDQ4
SDQ[47:40]	SDQ5
SDQ[55:48]	SDQ6
SDQ[63:56]	SDQ7
SCB[7:0]	SDQ8

Note2:Trace spacing normally = 12 mils and through between DIMM 2 pin = 7 mils, but breakout form MCH ball = 5 mils width with 7mils spacing for a max of 350mils

Note3:

- * SCK[X] length = SCK#[X] length
- * SCK/SCK#[2:0] routed to DIMM 0 are equal in length, and SCK/SCK#[5:3] routed to DIMM 1 are equal in 1ength

Note4:

- * Between the pair differential clock 2 signal trace spacing = 7 mils
- * Differential Trace with 2.5V copper flood spacing = 10 mils minimum
- * Serpentine spacing = 20 mils minimum
- * Differential signals breakout form MCH = 5 mil width with 7 mil differential spacing and 7 mil isolation spacing from another signal for a max of 350 mils

Note5:Data group signal can NOT placed within the same RPACK's(series and parallel resistor packs) as the command or control group signal

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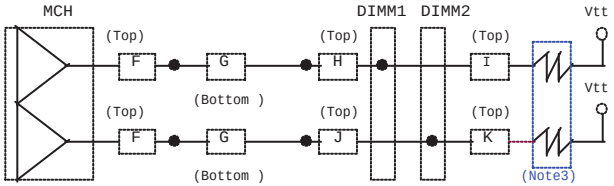
DDR-SDRAM Routing Guidelines

4.SCKE[3:0],SCS#[3:0] routing rule

DIMM 0					
Signal	Length F	Length G	Length H	Length I	Width
SCS#[1:0] SCKE[1:0] (Note1)	Max = 40 mils	2.0" - 3.5"	Max = 500 mils (Note2)	0.4" - 1.3"	5 mils
Total lenght	DIMM0 SCK/SCK#[2:0] length = X" DIMM0 SCS#/SCKE length = F + G + H = X"- 1"				

DIMM 1					
Signal	Length F	Length G	Length J	Length K	Width
SCS#[3:2] SCKE[3:2] (Note1)	Max = 40 mils	2.0" - 3.5"	Max = 1" (Note2)	0.1" - 0.8"	5 mils
Total lenght	DIMM1 SCK/SCK#[5:3] length = Y" DIMM1 SCS#/SCKE length = F + G + J = Y"- 1"				



Note1:

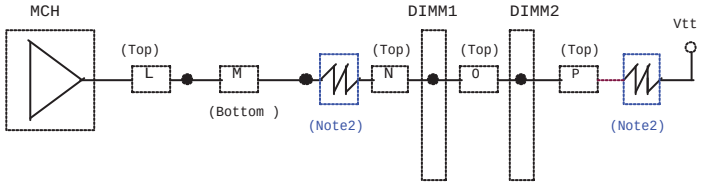
* Trace spacing normally = 12 mils and through between DIMM 2 pin or DIMM to Rtt = 7 mils, but breakout form MCH ball = 5 mils width with 7mils spacing for a max of 350mils
* Trace with 2.5V copper flood spacing = 7 mils minimum
* Isolation spacing form another group signal spacing = 20 mils minimum
* Control signals breakout form MCH = 5 mil width with 7 mil spacing for a max of 350 mils

Note2:This purpose prevent break form DIMM0 bottom size 2.5V copper flood to MCH power plane

Note3:Control group signal can NOT placed within the same parallel resistor packs as the command or data group signal

5.SMA[12:0],SBS[1:0],SRAS#,SCAS# routing rule

Signal	Length L	Length M	Length N	Length O	Length P	Width
SMA[12:0] SBS[1:0] SRAS# SCAS# (Note1)	Max = 40 mils	2.0" - 3.5"	Max = 500 mils	0.3" - 0.5"	0.1" - 0.8"	5 mils
DIMM 0 Total lenght	DIMM0 SCK/SCK#[2:0] length = X" Command signal length = L + M + N = X" - 1"					
DIMM 1 Total lenght	DIMM0 SCK/SCK#[5:3] length = Y" Command signal length = L + M + N + O = Y" - 1"					



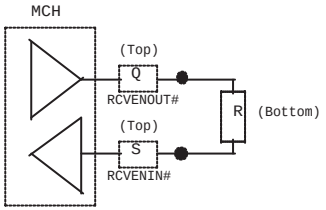
Note1:

* Trace spacing normally = 12 mils and through between DIMM 2 pin or DIMM to Rtt = 7 mils, but breakout form MCH ball = 5 mils width with 7mils spacing for a max of 350mils
* Trace with 2.5V copper flood spacing = 7 mils minimum
* Isolation spacing form another group signal spacing = 20 mils minimum
* Command signals breakout form MCH = 5 mil width with 7 mil spacing for a max of 350 mils

Note2:Command group signal can NOT placed within the same RPACK's(series and parallel resistor packs) as the data or control group signal

5.Feedback - RCVENOUT#,RCVENIN# routing rule

Signal	Length Q	Length R	Length S	Width
RCVENOUT# RCVENIN# (Note1)	40 mils	Equal 1"	40 mils	5 milS
Total Length	Q + R + S = 1080 mils			



Note1:

* Trace spacing = 12 mils
* Trace with 2.5V copper flood spacing = 7 mils minimum
* Isolation spacing form another group signal spacing = 10 mils minimum
* Command signals breakout form MCH = 5 mil width with 7 mil spacing for a max of 350 mils

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DDR Data Signals(1)		
Signal	MCH ball	Package length(")
SDQ0	G28	0.716
SDQ1	F27	0.699
SDQ2	C28	0.874
SDQ3	E28	0.754
SDQ4	H25	0.532
SDQ5	G27	0.666
SDQ6	F25	0.592
SDQ7	B28	0.892
SDQ8	E27	0.797
SDQ9	C27	0.833
SDQ10	B25	0.812
SDQ11	C25	0.753
SDQ12	B27	0.886
SDQ13	D27	0.867
SDQ14	D26	0.773
SDQ15	E25	0.645
SDQ16	D24	0.722
SDQ17	E23	0.602
SDQ18	C22	0.699
SDQ19	E21	0.566
SDQ20	C24	0.785
SDQ21	B23	0.781
SDQ22	D22	0.640
SDQ23	B21	0.711
SDQ24	C21	0.627
SDQ25	D20	0.555
SDQ26	C19	0.587
SDQ27	D18	0.522
SDQ28	C20	0.615
SDQ29	E19	0.487
SDQ30	C18	0.579
SDQ31	E17	0.521

DDR Data Signals(2)		
Signal	MCH ball	Package length(")
SDQ32	E13	0.432
SDQ33	C12	0.543
SDQ34	B11	0.596
SDQ35	C10	0.590
SDQ36	B13	0.639
SDQ37	C13	0.552
SDQ38	C11	0.588
SDQ39	D10	0.626
SDQ40	E10	0.533
SDQ41	C9	0.605
SDQ42	D8	0.587
SDQ43	E8	0.522
SDQ44	E11	0.523
SDQ45	B9	0.715
SDQ46	B7	0.706
SDQ47	C7	0.643
SDQ48	C6	0.700
SDQ49	D6	0.664
SDQ50	D4	0.760
SDQ51	B3	0.922
SDQ52	E6	0.640
SDQ53	B5	0.846
SDQ54	C4	0.810
SDQ55	E5	0.670
SDQ56	C3	0.859
SDQ57	D3	0.811
SDQ58	F4	0.723
SDQ59	F3	0.814
SDQ60	B2	0.949
SDQ61	C2	0.893
SDQ62	E2	0.865
SDQ63	G5	0.689

DDR ECC Signals		
Signal	MCH ball	Package length(")
SCB0	C16	0.570
SCB1	D16	0.526
SCB2	B15	0.623
SCB3	C14	0.533
SCB4	B17	0.621
SCB5	C17	0.583
SCB6	C15	0.540
SCB7	D14	0.503

DDR Data Strobe Signals		
Signal	MCH ball	Package length(")
SDQS0	F26	0.651
SDQS1	C26	0.775
SDQS2	C23	0.738
SDQS3	B19	0.636
SDQS4	D12	0.493
SDQS5	C8	0.596
SDQS6	C5	0.776
SDQS7	E3	0.821
SDQS8	E15	0.520

DDR Clock Signals		
Signal	MCH ball	Package length(")
SCK0	E14	0.453
SCK#0	F15	0.432
SCK1	J24	0.454
SCK#1	G25	0.587
SCK2	G6	0.551
SCK#2	G7	0.543
SCK3	G15	0.371
SCK#3	G14	0.349
SCK4	E24	0.610
SCK#4	G24	0.548
SCK5	H5	0.589
SCK#5	F5	0.693