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MS-6507

Version 5.0
11/20/2001 Update

INTEL (R) Brookdale Chipset
Willamette/Northwood 478pin mPGA-B Processor Schematics

CPU:

Willamette/Northwood mPGA-478B Processor

System Brookdale Chipset:

INTEL MCH (North Bridge) +
INTEL ICH2 (South Bridge)

On Board Chipset:

BIOS -- FWH

LPC Super I/O -- W83627HF

Clock Generation -- ICS950213AF

AC'97 Codec -- AvanceLogic AC201A/AC202A

Expansion Slots:

AGP2.0 SLOT * 1
PCI2.2 SLOT * 3
CNR 2.2 SLOT * 1

Micro-Star	Title: ***MS-6507***	Rev: ***5.0***
Document Number:	Cover Sheet	
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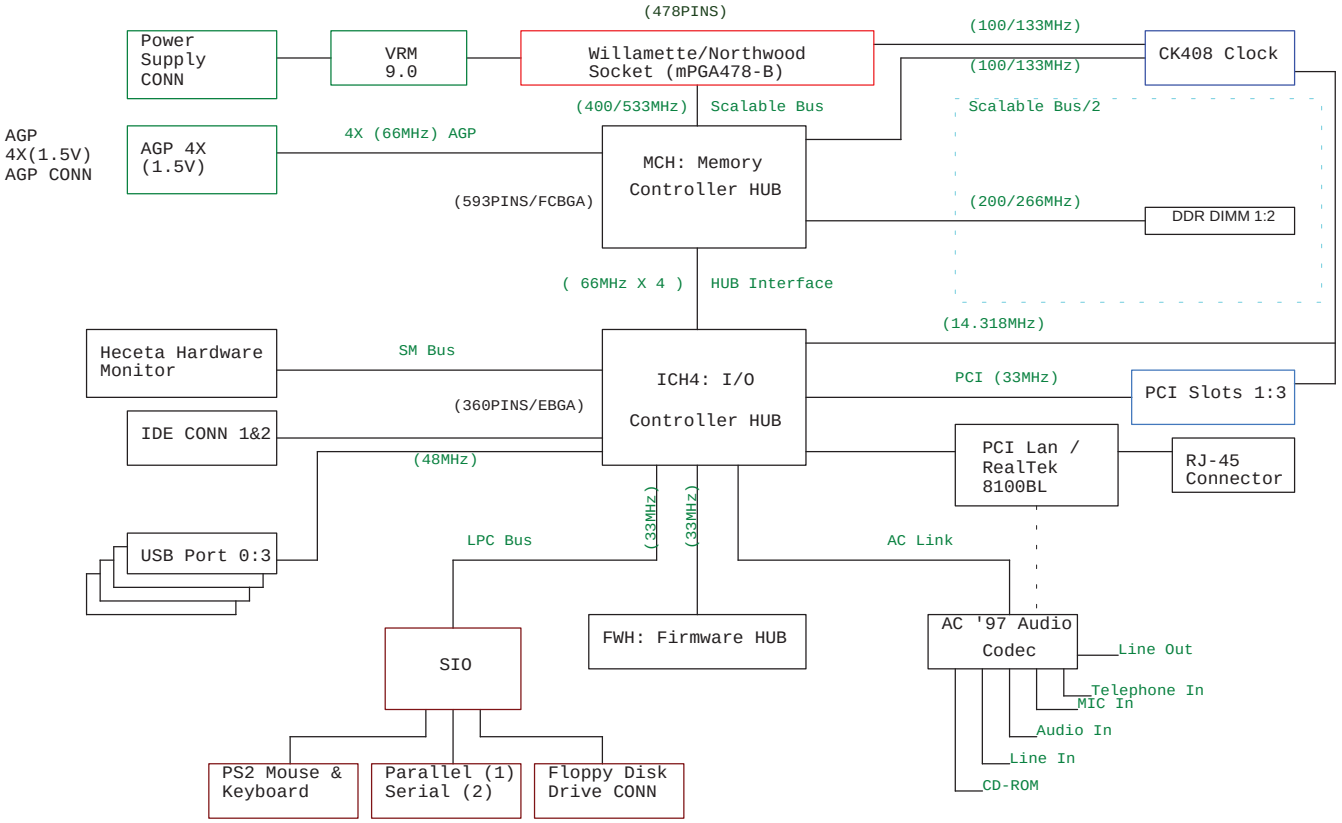

Micro-Star	Title: MS-6507	Rev: 5.0
Document Number:	Block Diagram	
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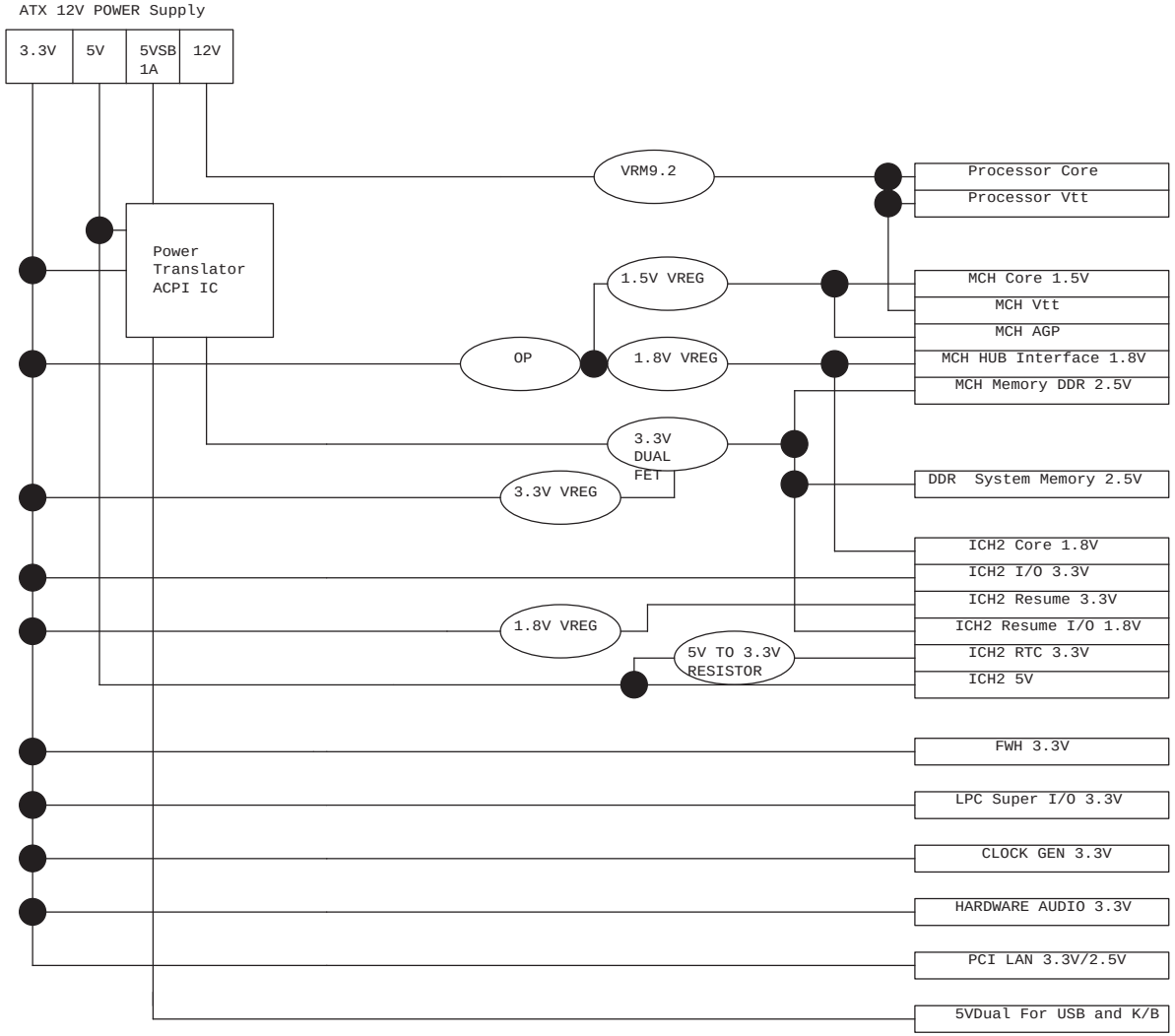
Power Delivery Map



POWER CONSUMPTION

	VCCP	VCC_AGP	VCC1_8	VCC3_DIMM	VCC3	VCC5	VCC5_SB	+12V	-12V
CPU	69.0A	0	0	0	0	0	0	NOTE4	0
PMCH	2.4A	NOTE1	0.2A	2.0A	0	0	0	0	0
ICH2	0	0	NOTE3	0	NOTE3	0	NOTE3	0	0
CY28324	0	0	0	0	0	0	0	0	0
AD1885	0	0	0	0	0		0	0	0
FWH -SST	0	0	0	0			0		
W83627HF	0	0	0	0	0		0	0	0
HIP6301		0	0	0	0		0	0	0
HIP6602A		0	0	0			0	0	0
HIP6601A	0	0	0	0	0	0	0	0	0
SC1547	0	0	0	0	0	0			0
DIMM	0	0	0	NOTE2	0		NOTE2	0	0
AGP	0	8.0A	0	0	6.0A	2.0A	?	1.0A	0
PCI	0	0	0	0		0	0	0	0
USB	0		0	0		0			0
USB HUB	0	0	0	0	0	0	0	0	0
FAN	0	0	0	0	0	0	0	0	0
TTL	0	0	0	0	0	0	0	0	0
AMPLIFIER	0	0	0	0			0	0	0
OTHER	0	0	0	0	0		0		

NOTE1 --- MCH
VCC_AGP = VCC1_5 (1.5A) + VCC_AGP (0.37A)

NOTE2 --- DIMM
S0 STATE --- 2.0A * 3 = 6.0A ---> VCC3
S1/S3 STATE --- 200mA * 3 = 600mA ---> VCC3_SB
VCC3_SB --> 600mA*3.3V/5V=396mA --> VCC5_SB

NOTE3 --- ICH2

Power	S0	S1	S3/S4/S5
1.8V	300mA	100mA	N/A
1.8V_LAN	36mA	28mA	N/A
VCC1_8SB	45mA	30mA	7mA
VCC3	410mA	5mA	N/A
VCC3+562ET	230mA	210mA	N/A
VCC3_SB	25mA	0.6mA	N/A

VCC3_SB =
VCC1_8SB =
VCC5_SB = VCC3_SB + VCC1_8SB

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Document Number: Power Delivery Map		
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General Purpose I/O Spec.

ICH4

GPIO Pin	Type	Function
GPIO 0	I	Non Connect
GPIO 1	I	Non Connect
GPIO 2~4	I	Not Implemented
GPIO 5	I	Non Connect
GPIO 6	I	AC97 Enabled/Disabled
GPIO 7	I	None
GPIO 8	I	LAN Wake Up
GPIO 9	I	AC'97 Serial Data In
GPIO 10	I	Non Connect
GPIO 11	I	Non Connect
GPIO 12	I	External SMI
GPIO 13	I	LPC PME
GPIO 14~15	I	Not Implemented
GPIO 16	O	Non Connect
GPIO 17	O	Non Connect
GPIO 18	O	Not Implemented
GPIO 19	O	Not Implemented
GPIO 20	O	Non
GPIO 21	O	Not Implemented
GPIO 22	O	Non
GPIO 23	OD	BIOS Locked/Unlocked
GPIO 24	O	Non
GPIO 25	O	Non
GPIO 26	O	Non
GPIO 27	I/O	Non
GPIO 28	I/O	Non
GPIO 29~31	I/O	Not Implemented

FWH

GPIO Pin	Type	Function
GPI 0	I	ATA IDE 1 Detect
GPI 1	I	ATA IDE 2 Detect
GPI 2	I	Reserved
GPI 3	I	Reserved

DEVICE	ICH INT Pin	IDSEL
PCI Slot 1	INTA# INTB# INTC# INTD#	AD16
PCI Slot 2	INTB# INTC# INTD# INTA#	AD17
PCI Slot 3	INTC# INTD# INTA# INTB#	AD18
PCI Lan	INTC#/INTF#	AD29

Micro-Star	Title: MS-6507	Rev: 5.0
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CLOCK GENERATOR BLOCK

*Trace less 0.5"

for good filtering from 10K~1M

CP1 X_COPPER, FB1 X_0/0805, CB1 104P, CT1 Rubycon, CB2 105P, X_ELS10U/16V-B, VCC3, VCC3_C

for good filtering from 10K~1M

CP2 X_COPPER, FB2 X_0/0805, CB6 104P, CT2 Rubycon, CB7 105P, X_ELS10U/16V-B, R9 X_0, VCC3V

U1 ICS950213AF

Pin	Signal	Pin	Signal
39	CPU_VDD	41	CPU0
		40	CPU0#
36	CPU_GND	38	CPU1
		37	CPU1#
46	MREF_VDD	45	3VMREF/CPU_STP#
		44	3VMREF#/PCI_STP#
43	MREF_GND		
32	3V66_VDD	31	3V66_0
		30	3V66_1
		28	3V66_2
29	3V66_GND	27	3V66_3
9	PCI_VDD	6	FS2/PCI_F0
		7	FS3/PCI_F1
		8	MODE/PCI_F2
5	PCI_GND	10	FS4/PCI0
		11	PCI1
18	PCI_VDD	12	PCI2
		14	PCI3
		15	PCI4
13	PCI_GND	16	PCI5
		17	PCI6
24	48_VDD	22	FS0/48MHz
		23	FS1/24_48MHz
21	48_GND		
2	REF_VDD	48	MUL0/REF0
		1	MUL1/REF1
47	REF_GND		
34	CORE_VDD	3	X1
33	CORE_GND	4	X2
26	SCLK	35	IREF
25	SDATA		
19	VTT_GD#	20	RST#
		42	PWR_DN#

CB3 104P, CB4 104P, CB5 104P, CB8 104P, CB9 104P, CB10 104P, CB11 104P, CB12 104P

VCC3_C

*Put GND copper under Clock Gen.
connect to every GND pin
* 40 mils Trace on Layer 4
with GND copper around it
* put close to every power pin
* Trace Width 7mils.
* Same Group spacing 15mils
* Different Group spacing 30mils
* Different mode spacing 7mils on itself

R3 33 CPUCLK → CPUCLK {6}
R5 33 CPUCLK# → CPUCLK# {6}
R7 47 MCHCLK → MCHCLK {8}
R8 47 MCHCLK# → MCHCLK# {8}
C_STP, P_STP
RN1 8P4R-33: MCH_66, ICH_66, AGPCLK → MCH_66 {8}, ICH_66 {13}, AGPCLK {15}
RN2 8P4R-33: FS2, FS3, MODE → ICH_PCLK, FWH_PCLK, SIO_PCLK → ICH_PCLK {12}, FWH_PCLK {19}, SIO_PCLK {18}
FS4
R14 33 PCICLK5 → PCICLK5 {16}
PCICLK0 → PCICLK0 {16}
RN3 8P4R-33: PCICLK1, PCICLK2, PCICLK3 → PCICLK1 {16}, PCICLK2 {16}, PCICLK3 {17}
R19 33 FS0 → ICH_48 {13}
R20 33 FS1 → SIO_48 {18}
R22 33 MUL0 → ICH_14
R24 33 MUL1 → AUDIO_14 → ICH_14 {13}, AUDIO_14 {14}
C6 18P, X1 14.318MHZ/32PF, C7 18P
R29 475RST
R32 X_0, R35 4.7K, CRST# → FP_RST# → FP_RST# {13,21,22}, VCC3V
R34 X_1K VTT_GD# → SMBCLK, SMBDATA → {10,18,19,22} SMBCLK, {10,18,19,22} SMBDATA

R30 10K VTT_GD#, VCC3
Q1 2N3904S, R36 220, VCCP
R39 X, Q2 X_2N3904S, {6} SKTOCC#

Shut Source Termination Resistors

CPUCLK R1 49.9RST
CPUCLK# R2 49.9RST
MCHCLK R4 49.9RST
MCHCLK# R6 49.9RST

Trace less 0.2"
49.9ohm for 50ohm M/B impedance

CLOCK STRAPPING RESISTORS

FS4 R10 10K VCC3V
FS3 R11 10K VCC3V
FS1 R12 10K VCC3V, R13 X_10K
FS0 R15 10K VCC3V, R16 X_10K
FS2 R17 10K, R18 X_10K VCC3V
MODE R21 X_10K

MUL0=0 MUL0=1
Ioh=6*Iref
Voh=0.71V

MUL0 R23 X_10K VCC3V, R25 10K
MUL1 R26 10K VCC3V, R27 X_10K
CRST# R28 10K VCC3V
SMBCLK R31 1K, SMBDATA R33 1K → VCC3
C_STP R37 X_1K VCC3V, P_STP R38 X_1K

Pull-Down Capacitors

CN1 X_8P4C-10P: MCH_66, ICH_66, AGPCLK
CN2 X_8P4C-10P: SIO_PCLK, FWH_PCLK, ICH_PCLK
CN3 X_8P4C-10P: PCICLK0, PCICLK1, PCICLK2, PCICLK3
PCICLK4 C1 X_10P
PCICLK5 C2 10P
AUDIO_14 C3 10P
ICH_48 C4 X_10P
SIO_48 C5 10P
ICH_14 C8 10P

used only for EMI issue
Trace less 0.2"

ATA100 IDE CONNECTORS

PRIMARY IDE BLOCK

IDE2 YJ220-CB-1
R41 4.7K, R43 33, HD_RST# {22}
PDD0–PDD15 {13} PDD[0..7], PDD[8..15] {13}
PDDREQ, PDIOW#, PDIOR#, PDIORDY, PDDACK#, IRQ14, PDA1, PDA0, PDCS#1, PD_LED {21}
R45 470, R49 33
PD_DET {19}, PDA2 {13}, PDCS#3 {13}
R55 8.2K VCC5, C11 47P, R53 10K VCC3, C12 X_473P

SECONDARY IDE BLOCK

IDE1 YJ220-CW-1
R40 4.7K, R42 33, HD_RST#
SDD0–SDD15 {13} SDD[0..7], SDD[8..15] {13}
SDDREQ, SDIOW#, SDIOR#, SDIORDY, SDDACK#, IRQ15, SDA1, SDA0, SDCS#1, SD_LED {21}
R44 470
SD_DET {19}, SDA2 {13}, SDCS#3 {13}
R48 33
R54 8.2K VCC5, C9 47P, R50 10K VCC3, C10 X_473P

VCC_AGP
R46 1K, BSEL0 {6}
R47 8.2K, FS1
R51 6.8K, {9,15} ST1
D1 1N4148S, R52 R/0603
Q3 2N3904S, R56 R/0603

VCC3
CB13 104P, CB14 104P, CB15 104P, CB16 104P

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	Document Number: Clock CY28323/4 & ATA100 IDE		
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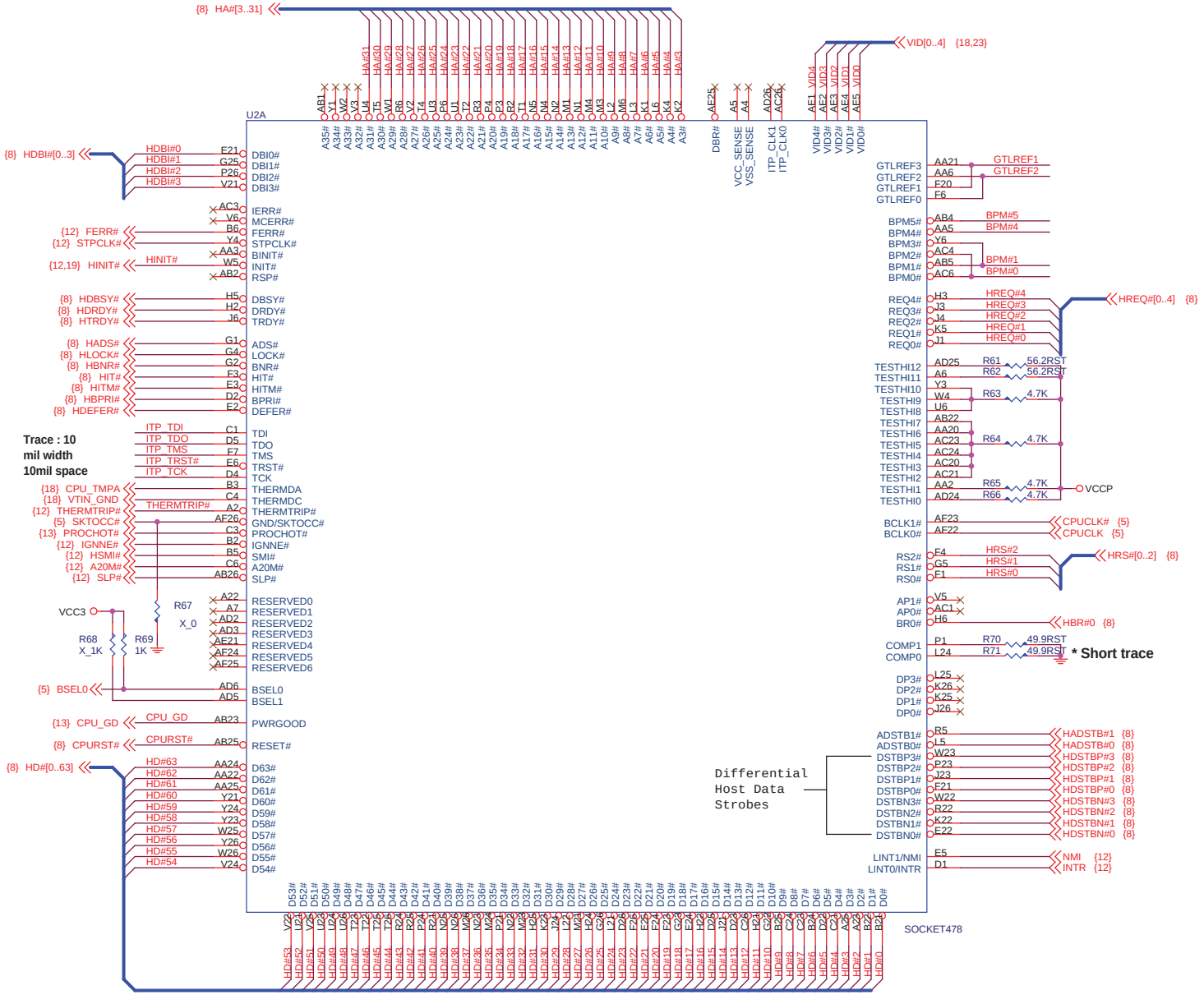
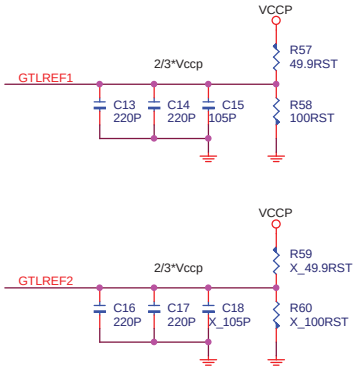
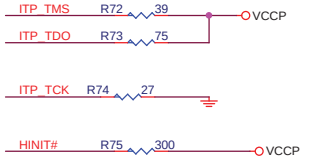
CPU SIGNAL BLOCK



CPU GTL REFERNCE VOLTAGE BLOCK

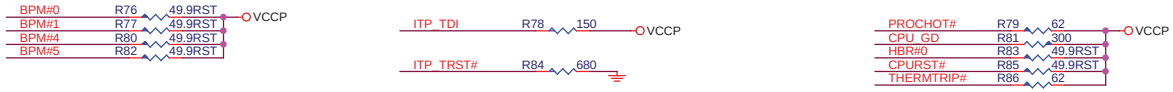


Every pin put one 220pF cap near it.
Trace Width 15mils, Space 15mils.
Keep the voltage dividers within 1.5 inches of the first GTLREF Pin



CPU STRAPPING RESISTORS

ALL COMPONENTS CLOSE TO CPU



Micro-Star	Title: MS-6507	Rev: 5.0
Document Number: INTEL mPGA478-B CPU1		
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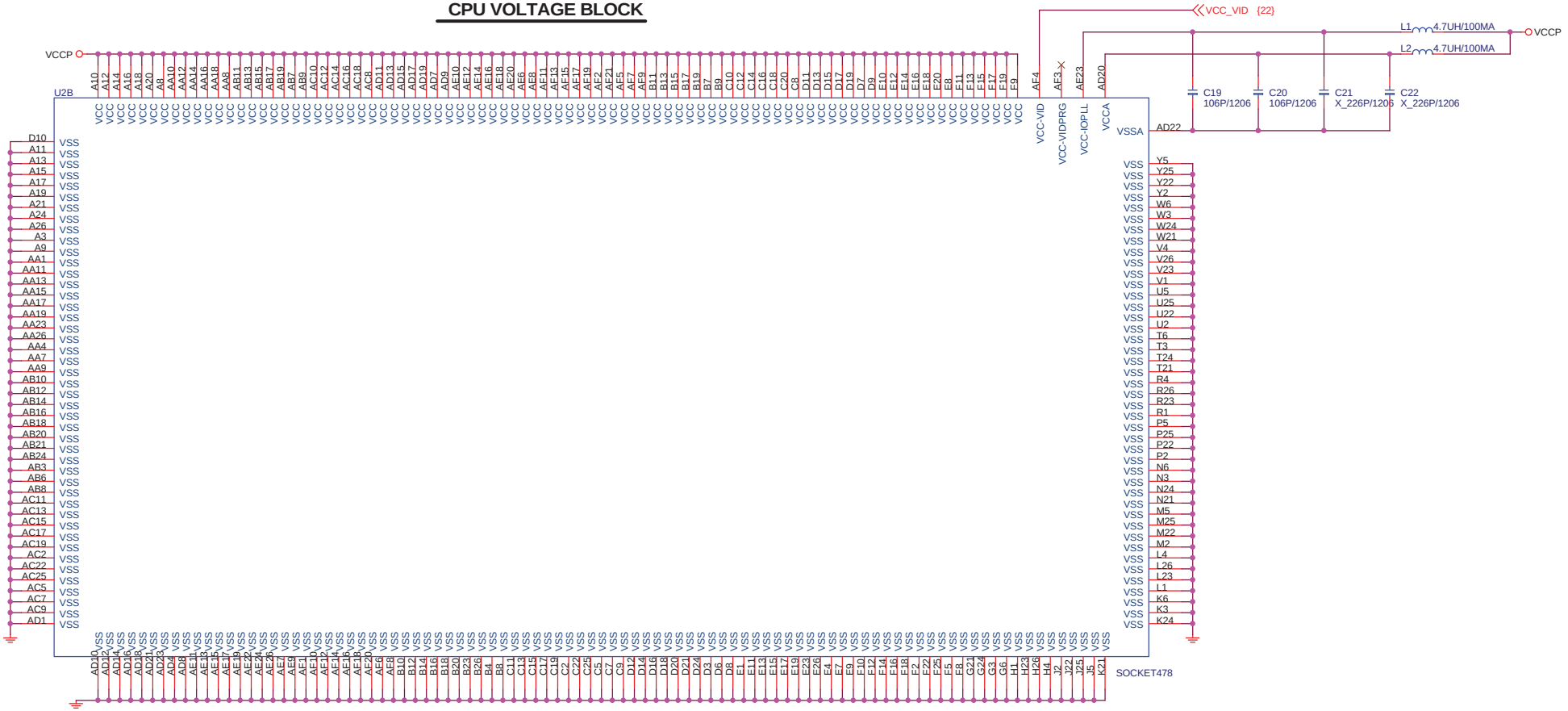
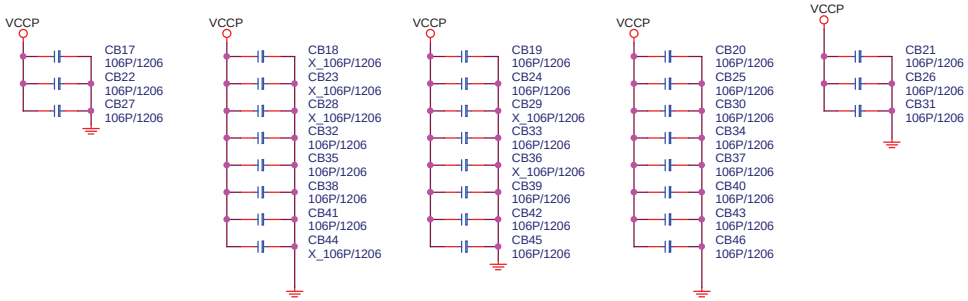
CPU VOLTAGE BLOCK



CPU DECOUPLING CAPACITORS



PLACE CAPS WITHIN CPU CAVITY

Micro-Star	Title: MS-6507	Rev: 5.0
Document Number: INTEL mPGA478-B CPU2		
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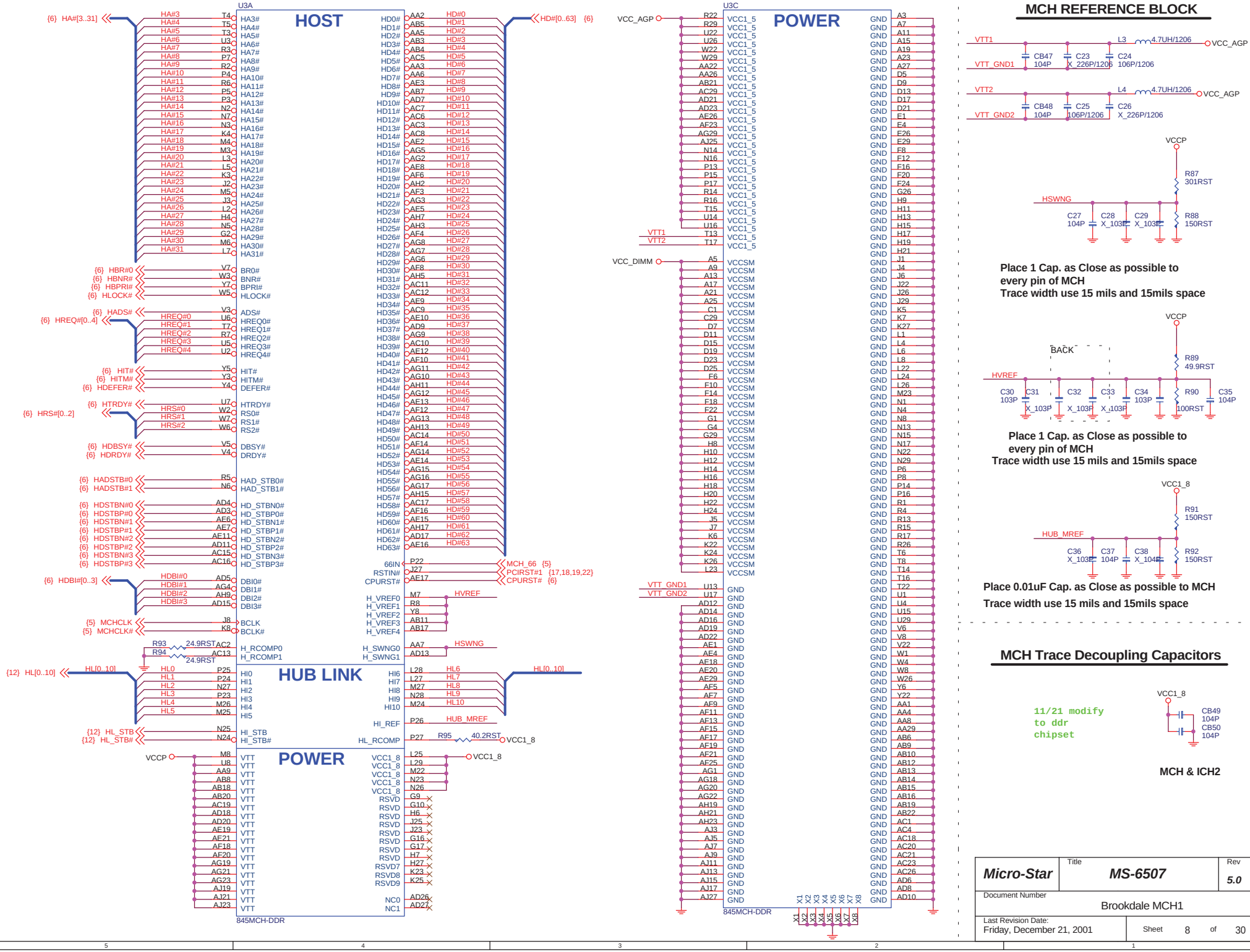
U3A
HOST
HA#3
HA4#
HA5#
HA6#
HA#7
HA#8
HA#9
HA10#
HA11#
HA12#
HA13#
HA14#
HA15#
HA16#
HA17#
HA18#
HA19#
HA20#
HA21#
HA22#
HA23#
HA24#
HA25#
HA26#
HA27#
HA28#
HA29#
HA30#
HA31#
BR0#
BNR#
BPRI#
HLOCK#
ADS#
HREQ0#
HREQ1#
HREQ2#
HREQ3#
HREQ4#
HIT#
HITM#
DEFER#
HTRDY#
RS0#
RS1#
RS2#
DBSY#
DRDY#
HAD_STB0#
HAD_STB1#
HD_STBN0#
HD_STBP0#
HD_STBN1#
HD_STBP1#
HD_STBN2#
HD_STBP2#
HD_STBN3#
HD_STBP3#
DBI0#
DBI1#
DBI2#
DBI3#
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BCLK#
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H_RCOMP1
HD0#
HD1#
HD2#
HD3#
HD4#
HD5#
HD6#
HD7#
HD8#
HD9#
HD10#
HD11#
HD12#
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HD61#
HD62#
HD63#
66IN
RSTIN#
CPURST#
H_VREF0
H_VREF1
H_VREF2
H_VREF3
H_VREF4
H_SWNG0
H_SWNG1
HUB LINK
HI0
HI1
HI2
HI3
HI4
HI5
HI_STB
HI_STB#
HI6
HI7
HI8
HI9
HI10
HI_REF
HL_RCOMP
POWER
VTT
VCC1_8
RSVD
RSVD7
RSVD8
RSVD9
NC0
NC1
845MCH-DDR
U3C
POWER
VCC1_5
VCCSM
GND
VTT1
VTT2
VTT_GND1
VTT_GND2
845MCH-DDR
MCH REFERENCE BLOCK
VTT1
VTT_GND1
CB47 104P
C23 X_226P/1206
C24 106P/1206
L3 4.7UH/1206
VCC_AGP
VTT2
VTT_GND2
CB48 104P
C25 106P/1206
C26 X_226P/1206
L4 4.7UH/1206
VCCP
R87 301RST
HSWNG
C27 104P
C28 X_103P
C29 X_103P
R88 150RST
Place 1 Cap. as Close as possible to every pin of MCH
Trace width use 15 mils and 15mils space
BACK
HVREF
R89 49.9RST
C30 103P
C31 X_103P
C32 X_103P
C33 X_103P
C34 103P
R90 100RST
C35 104P
Place 1 Cap. as Close as possible to every pin of MCH
Trace width use 15 mils and 15mils space
VCC1_8
R91 150RST
HUB_MREF
C36 X_103P
C37 104P
C38 X_104P
R92 150RST
Place 0.01uF Cap. as Close as possible to MCH
Trace width use 15 mils and 15mils space
MCH Trace Decoupling Capacitors
11/21 modify to ddr chipset
VCC1_8
CB49 104P
CB50 104P
MCH & ICH2
Micro-Star
Title
MS-6507
Rev
5.0
Document Number
Brookdale MCH1
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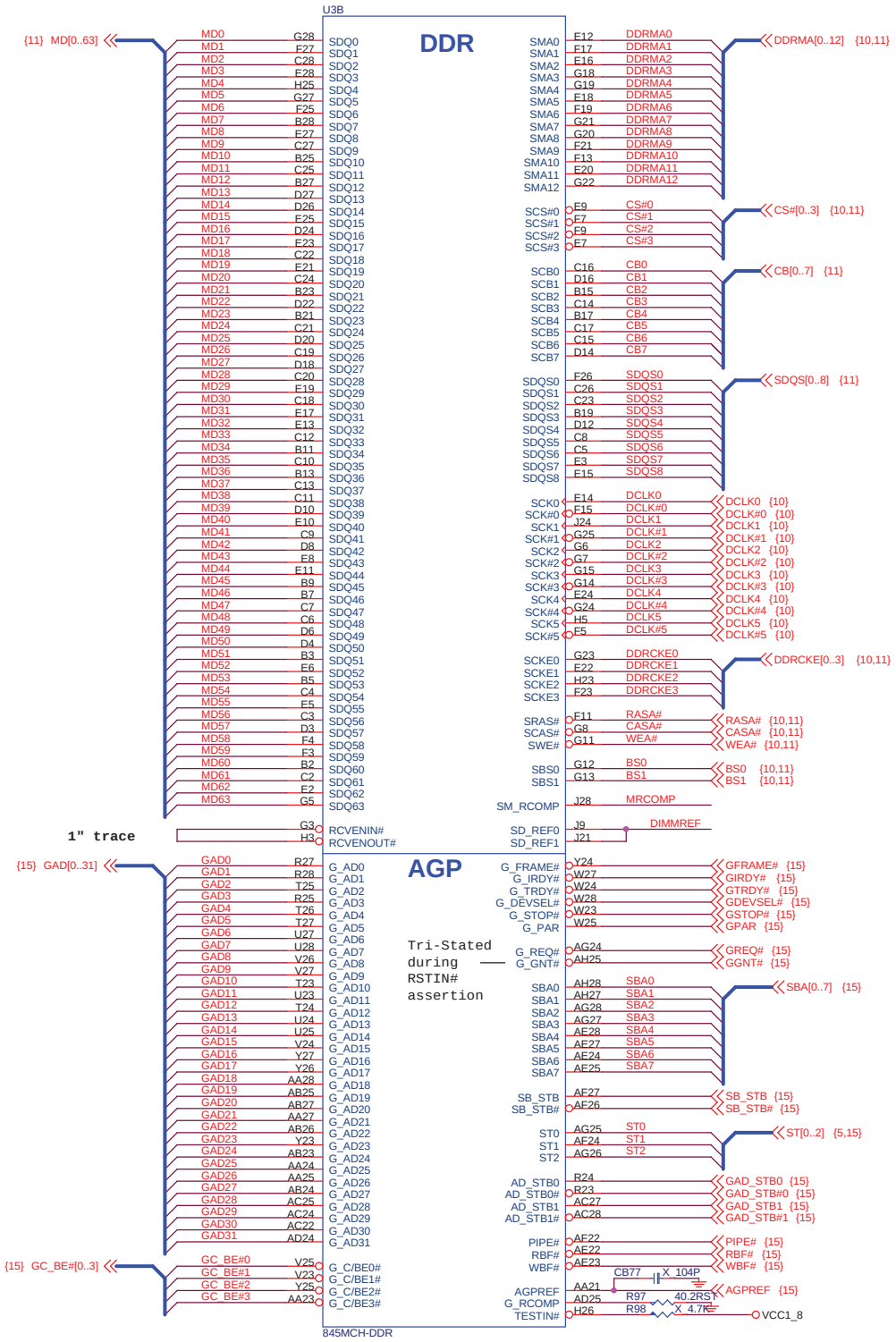
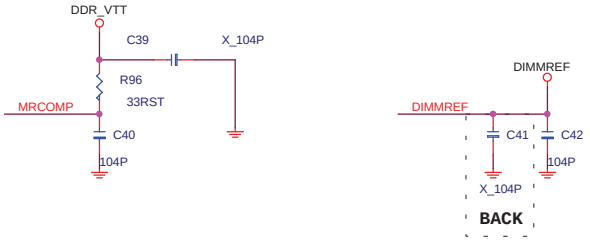
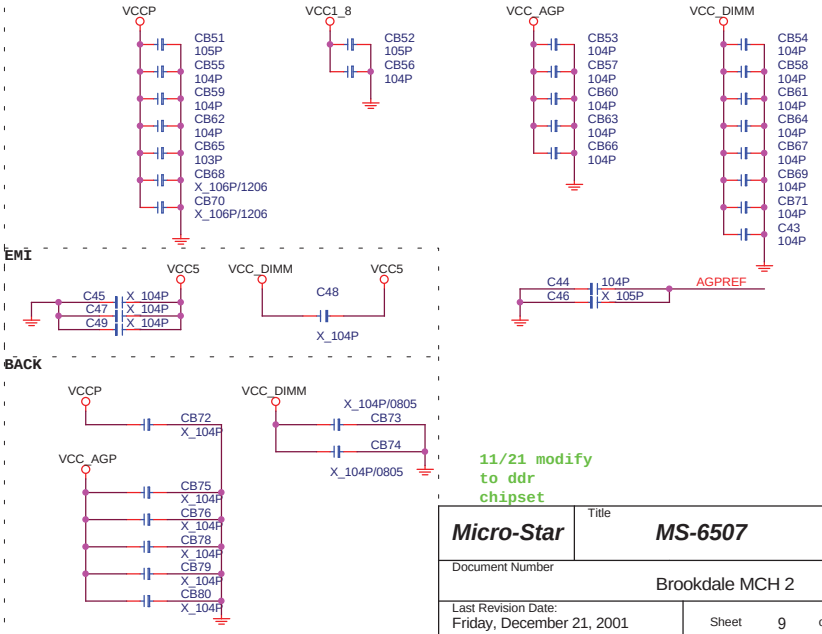


MCH REFERENCE VOLTAGE



MCH DECOUPLING CAPACITOR



Micro-Star	Title: MS-6507	Rev: 5.0
Document Number: Brookdale MCH 2		
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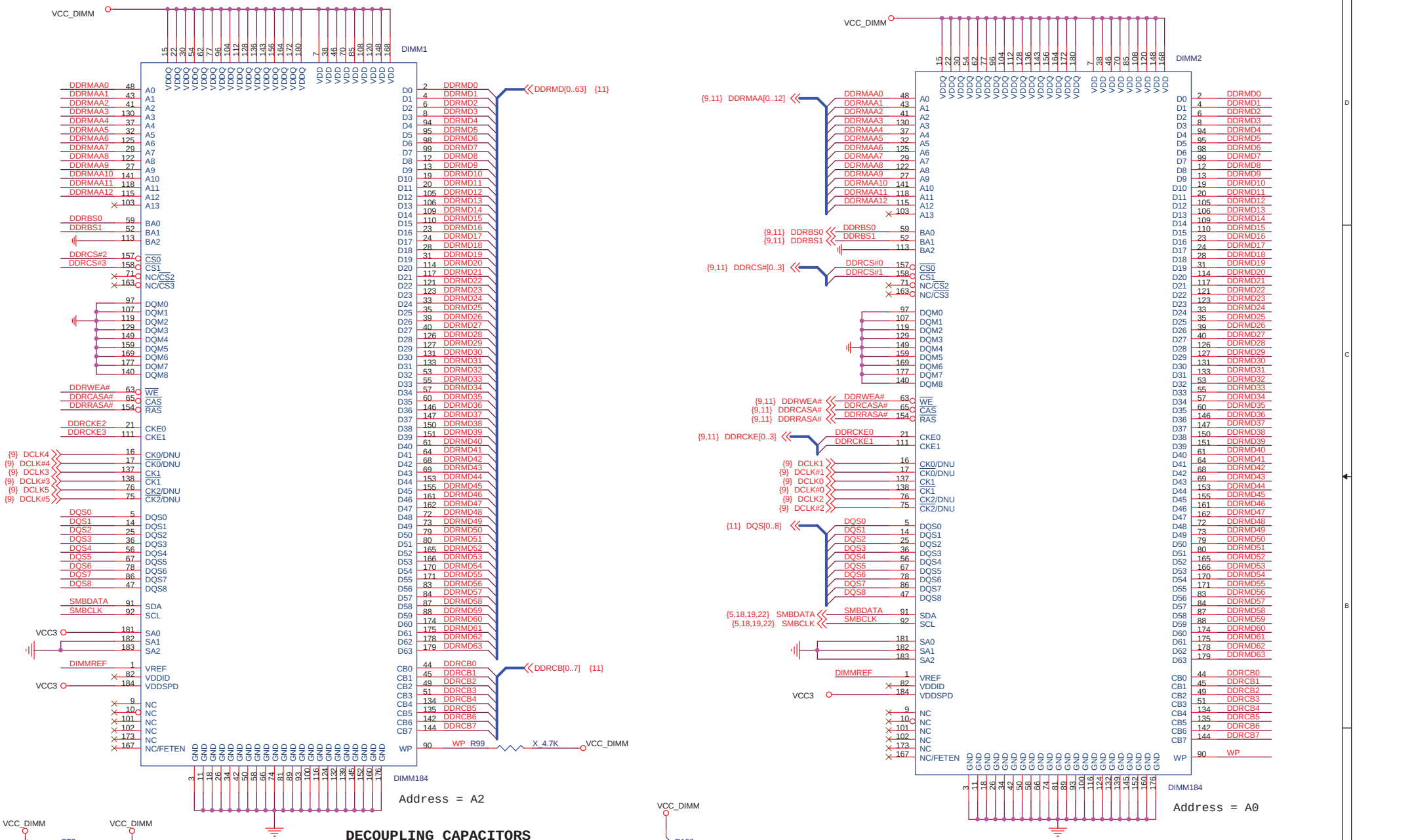
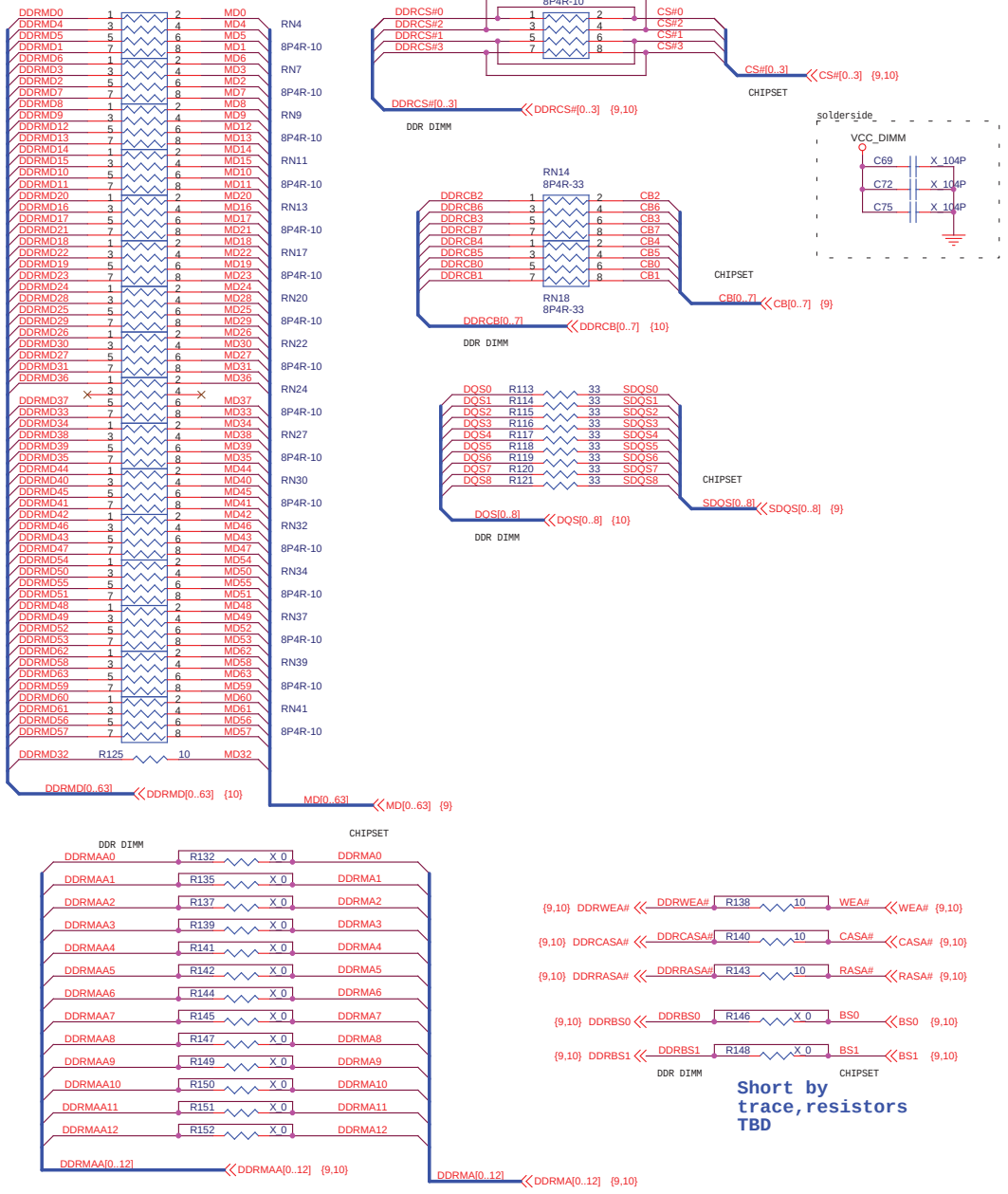
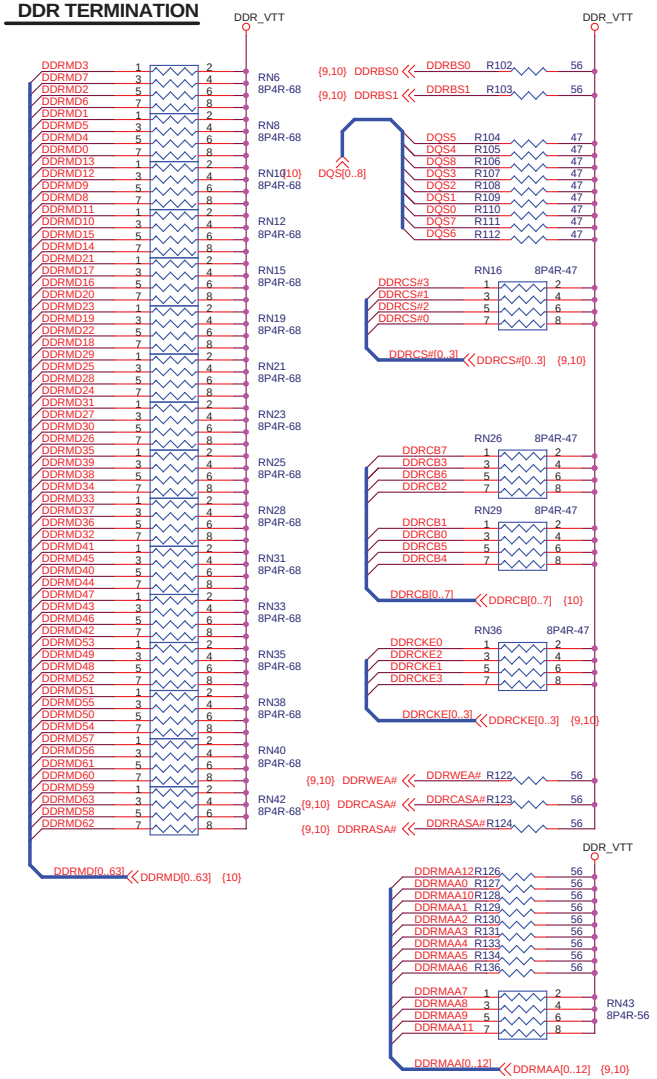

VCC_DIMM
DIMM1
DDRMAA0
DDRMAA1
DDRMAA2
DDRMAA3
DDRMAA4
DDRMAA5
DDRMAA6
DDRMAA7
DDRMAA8
DDRMAA9
DDRMAA10
DDRMAA11
DDRMAA12
DDRBS0
DDRBS1
DDRCS#2
DDRCS#3
DQM0
DQM1
DQM2
DQM3
DQM4
DQM5
DQM6
DQM7
DQM8
DDRWEA#
DDRCASA#
DDRRASA#
DDRCKE2
DDRCKE3
{9} DCLK4
{9} DCLK#4
{9} DCLK3
{9} DCLK#3
{9} DCLK5
{9} DCLK#5
DQS0
DQS1
DQS2
DQS3
DQS4
DQS5
DQS6
DQS7
DQS8
SMBDATA
SMBCLK
VCC3
DIMMREF
VDDSPD
NC/FETEN
DDRMD[0..63] {11}
DDRCB[0..7] {11}
WP R99
X_4.7K
DIMM184
Address = A2
VCC_DIMM
DIMM2
{9,11} DDRMAA[0..12]
{9,11} DDRBS0
{9,11} DDRBS1
{9,11} DDRCS#[0..3]
{9,11} DDRWEA#
{9,11} DDRCASA#
{9,11} DDRRASA#
{9,11} DDRCKE[0..3]
{9} DCLK1
{9} DCLK#1
{9} DCLK0
{9} DCLK#0
{9} DCLK2
{9} DCLK#2
{11} DQS[0..8]
{5,18,19,22} SMBDATA
{5,18,19,22} SMBCLK
Address = A0
DECOUPLING CAPACITORS
CT3
1000U/6.3V-TEAPC
CB81 104P
CB83 104P
CB85 100P
CB88 105P
CB91 105P
CB94 100P
CB82 X_104P
CB84 104P
CB86 X_105P
CB89 105P
CB92 X_100P
CB95 X_100P
C50 X_104P
CB87 X_104P
CB90 104P
C53 104P
CB93 104P
C54 104P
CB96 104P
R100 150
R101 150
C51 104P
C52 104P
DIMMREF
place near DIMM1
11/21 modify
Micro-Star
Title
MS-6507
Rev
5.0
Document Number
DDR DIMM 1 & 2
Last Revision Date:
Friday, December 21, 2001
Sheet 10 of 30

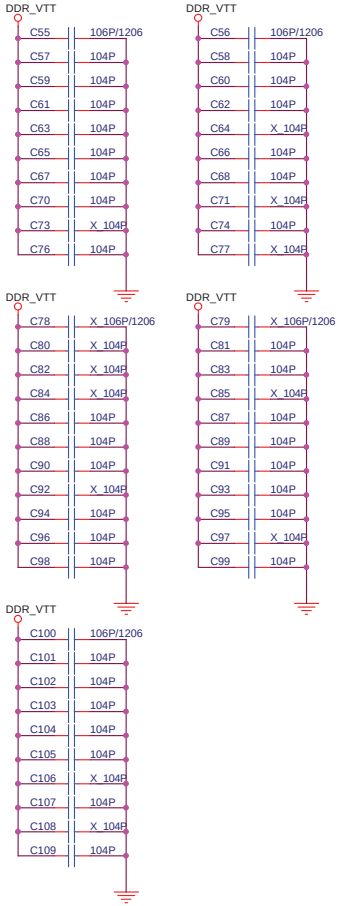
DDR DAMPING



Short by trace,resistors TBD

DDR TERMINATION





Micro-Star	Title: MS-6507	Rev: 5.0
Document Number: DDR DAMPING		
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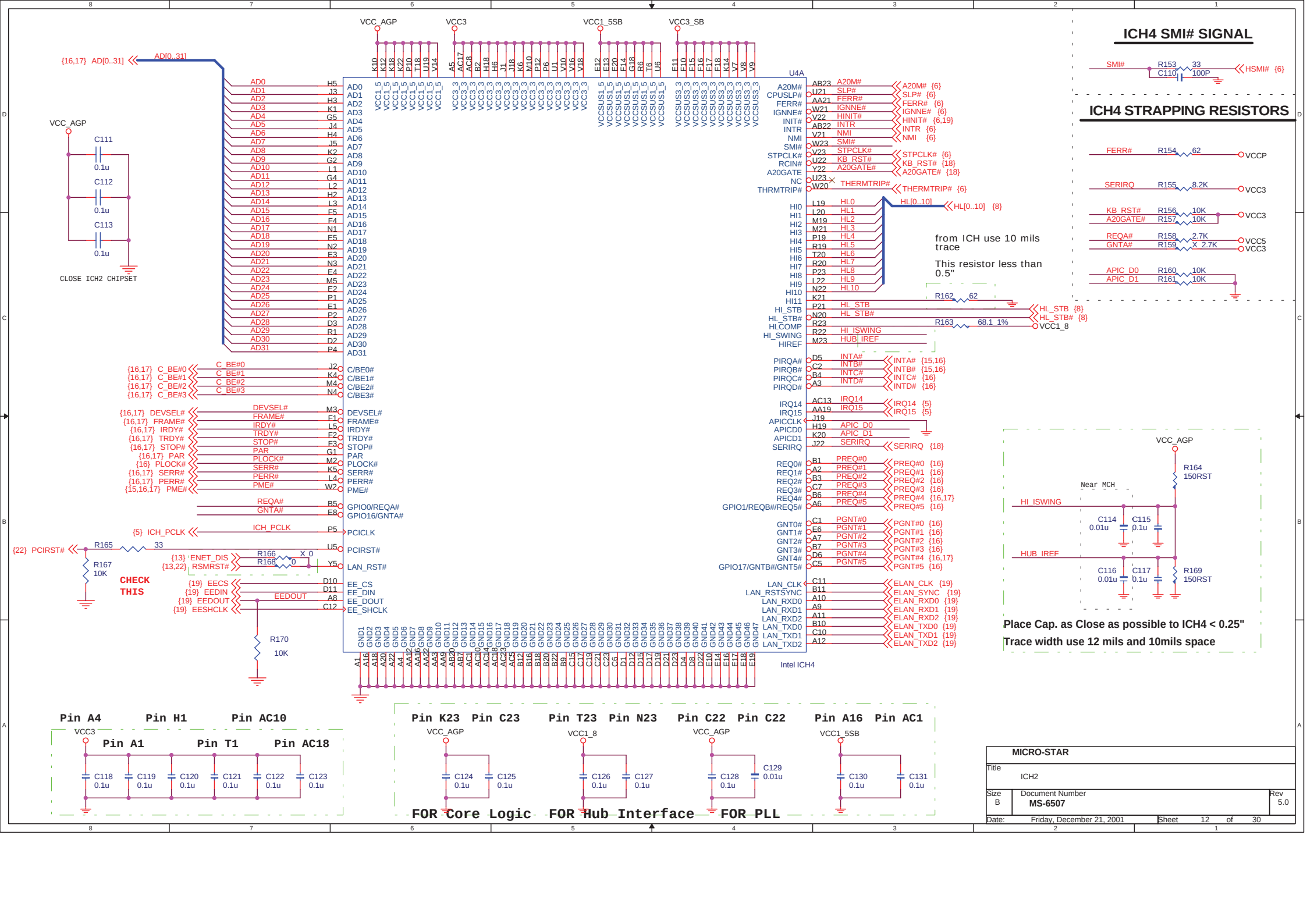
ICH4 SMI# SIGNAL
SMI#
R153 33
C110 100P
HSMI# {6}
ICH4 STRAPPING RESISTORS
FERR# R154 62 VCCP
SERIRQ R155 8.2K VCC3
KB_RST# R156 10K
A20GATE# R157 10K
VCC3
REQA# R158 2.7K
GNTA# R159 X 2.7K
VCC5
VCC3
APIC_D0 R160 10K
APIC_D1 R161 10K
U4A
Intel ICH4
from ICH use 10 mils trace
This resistor less than 0.5"
R162 62
R163 68.1 1%
VCC1_8
HL_STB {8}
HL_STB# {8}
HL[0..10] {8}
THERMTRIP# {6}
A20M# {6}
SLP# {6}
FERR# {6}
IGNNE# {6}
HINIT# {6,19}
INTR {6}
NMI {6}
STPCLK# {6}
KB_RST# {18}
A20GATE# {18}
INTA# {15,16}
INTB# {15,16}
INTC# {16}
INTD# {16}
IRQ14 {5}
IRQ15 {5}
APIC_D0
APIC_D1
SERIRQ {18}
PREQ#0 {16}
PREQ#1 {16}
PREQ#2 {16}
PREQ#3 {16}
PREQ#4 {16,17}
PREQ#5 {16}
PGNT#0 {16}
PGNT#1 {16}
PGNT#2 {16}
PGNT#3 {16}
PGNT#4 {16,17}
PGNT#5 {16}
ELAN_CLK {19}
ELAN_SYNC {19}
ELAN_RXD0 {19}
ELAN_RXD1 {19}
ELAN_RXD2 {19}
ELAN_TXD0 {19}
ELAN_TXD1 {19}
ELAN_TXD2 {19}
VCC_AGP
VCC3
VCC1_5SB
VCC3_SB
{16,17} AD[0..31]
AD[0..31]
VCC_AGP
C111 0.1u
C112 0.1u
C113 0.1u
CLOSE ICH2 CHIPSET
{16,17} C_BE#0
{16,17} C_BE#1
{16,17} C_BE#2
{16,17} C_BE#3
{16,17} DEVSEL#
{16,17} FRAME#
{16,17} IRDY#
{16,17} TRDY#
{16,17} STOP#
{16,17} PAR
{16} PLOCK#
{16,17} SERR#
{16,17} PERR#
{15,16,17} PME#
REQA#
GNTA#
{5} ICH_PCLK
{22} PCIRST#
R165 33
R167 10K
{13} ENET_DIS
{13,22} RSMRST#
R166 X 0
R168 0
CHECK THIS
{19} EECS
{19} EEDIN
{19} EEDOUT
{19} EESHCLK
EEDOUT
R170 10K
Near MCH
R164 150RST
C114 0.01u
C115 0.1u
C116 0.01u
C117 0.1u
R169 150RST
HI_ISWING
HUB_IREF
Place Cap. as Close as possible to ICH4 < 0.25"
Trace width use 12 mils and 10mils space
Pin A4 Pin H1 Pin AC10
Pin A1 Pin T1 Pin AC18
C118 0.1u
C119 0.1u
C120 0.1u
C121 0.1u
C122 0.1u
C123 0.1u
Pin K23 Pin C23
Pin T23 Pin N23
Pin C22 Pin C22
Pin A16 Pin AC1
C124 0.1u
C125 0.1u
C126 0.1u
C127 0.1u
C128 0.1u
C129 0.01u
C130 0.1u
C131 0.1u
FOR Core Logic
FOR Hub Interface
FOR PLL
MICRO-STAR
Title ICH2
Size B
Document Number MS-6507
Rev 5.0
Date: Friday, December 21, 2001
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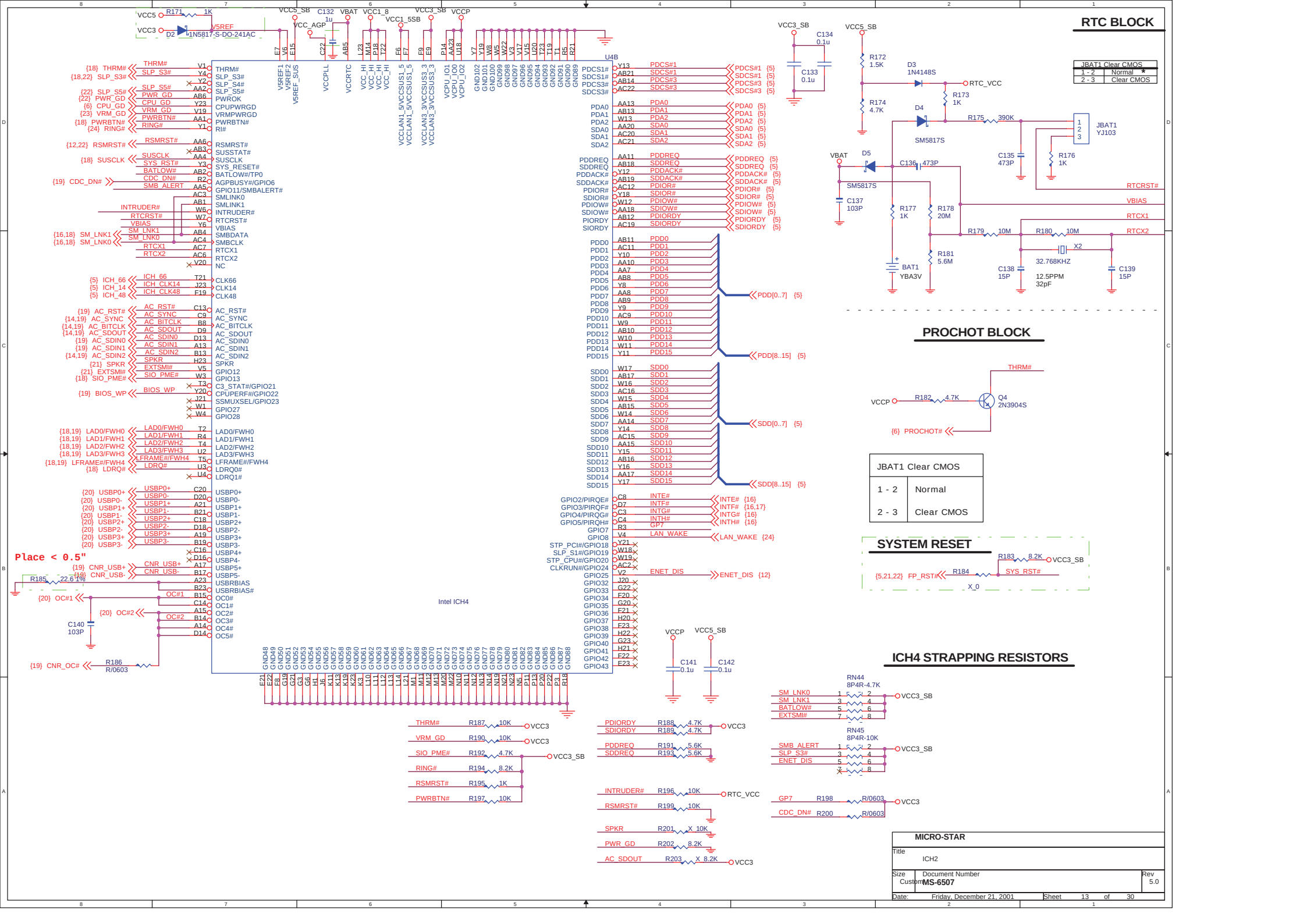
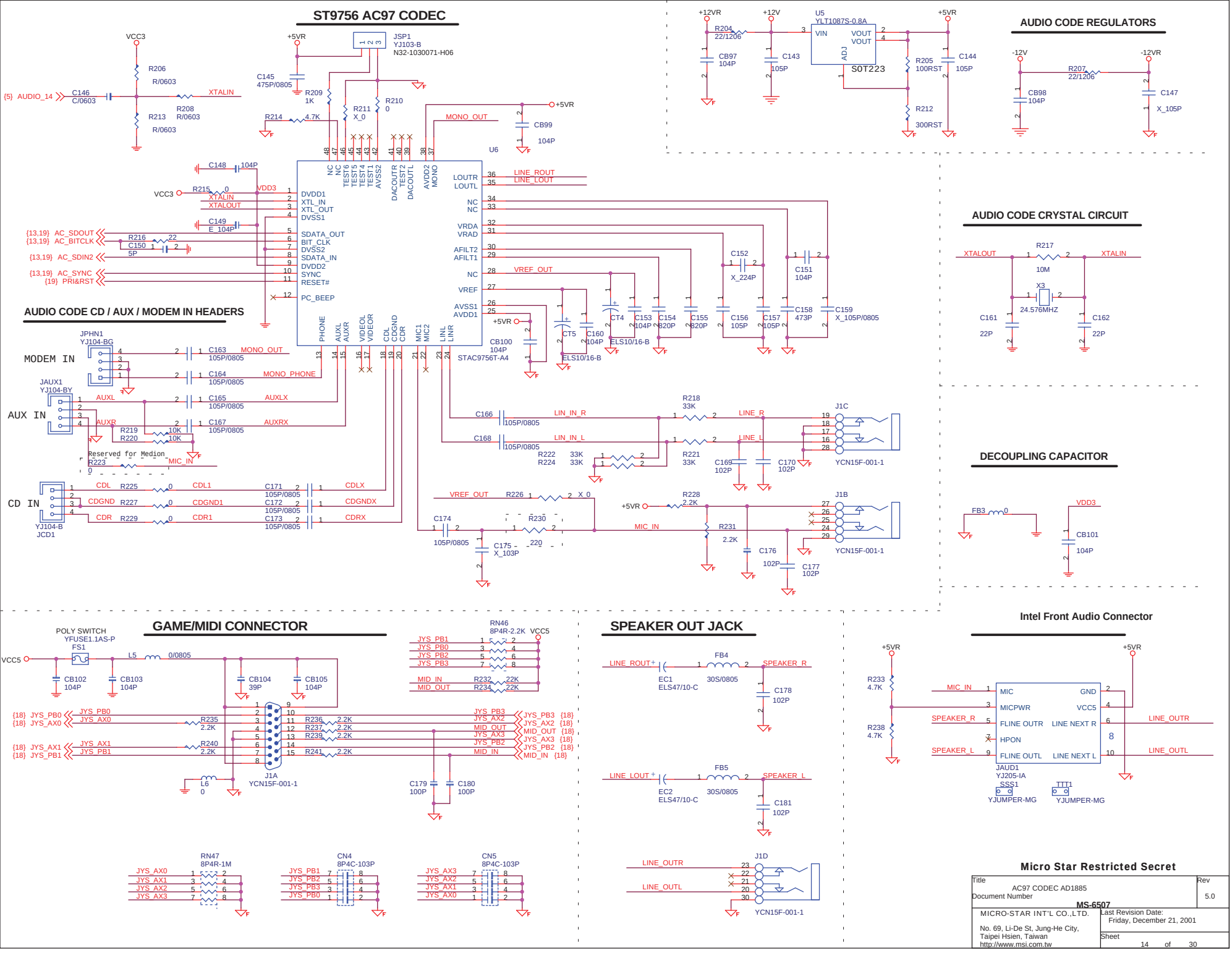

RTC BLOCK
JBAT1 Clear CMOS
1 - 2 Normal *
2 - 3 Clear CMOS
PROCHOT BLOCK
JBAT1 Clear CMOS
1 - 2 Normal
2 - 3 Clear CMOS
SYSTEM RESET
ICH4 STRAPPING RESISTORS
Intel ICH4
Place < 0.5"
MICRO-STAR
Title ICH2
Size Custom
Document Number MS-6507
Rev 5.0
Date: Friday, December 21, 2001
Sheet 13 of 30


ST9756 AC97 CODEC
AUDIO CODE REGULATORS
AUDIO CODE CRYSTAL CIRCUIT
AUDIO CODE CD / AUX / MODEM IN HEADERS
DECOUPLING CAPACITOR
GAME/MIDI CONNECTOR
SPEAKER OUT JACK
Intel Front Audio Connector
Micro Star Restricted Secret
AC97 CODEC AD1885
MS-6507
5.0
MICRO-STAR INT'L CO.,LTD.
No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan
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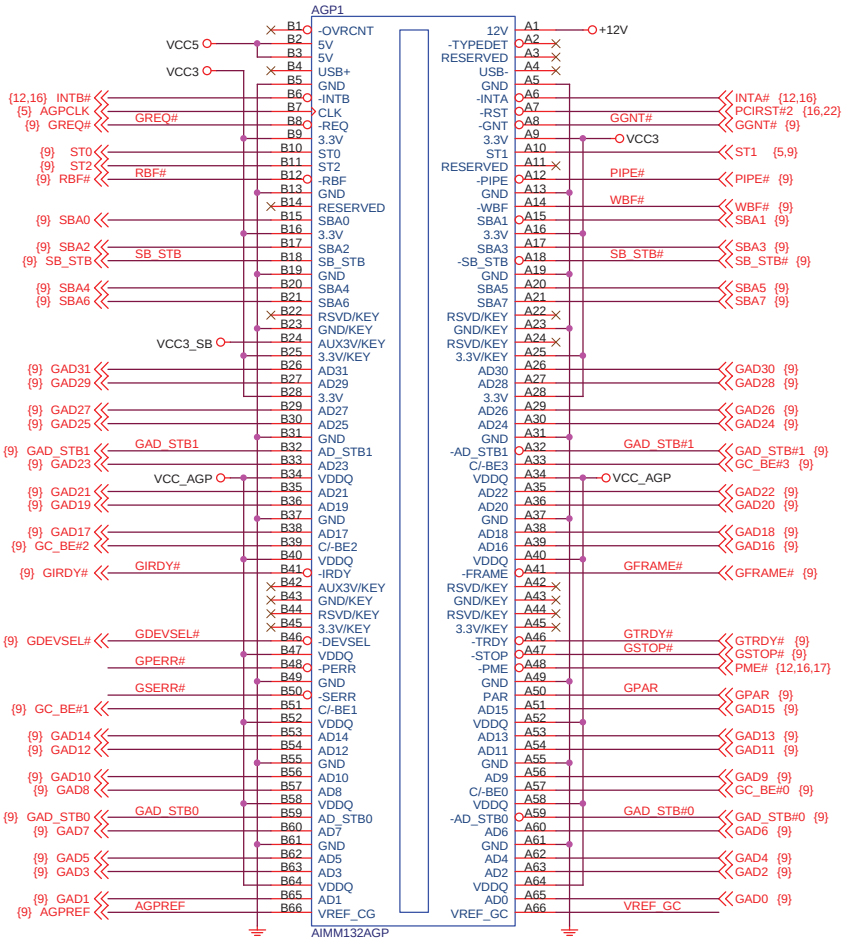
{5,9} ST[0..2]
{9} GAD[0..31]
{9} SBA[0..7]
{9} GC_BE#[0..3]

AGP UNIVERSAL 2X/4X SLOT(AGP VER:2.0 COMPLY)

VCC5 = 60mils trace / 15 mils space



VREF_GC:form the chipset to the graphics controller

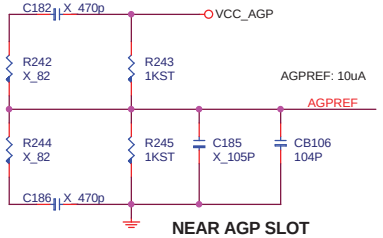
AGP Slot Imax

VCC_AGP 8.0A
VCC3 6.0A
VCC12 1.0A
VCC5 2.0A

VREF_GC:form the graphics controller to the chipset

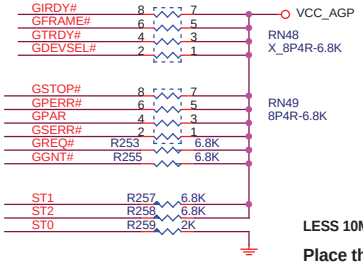
INTA#
INTB#

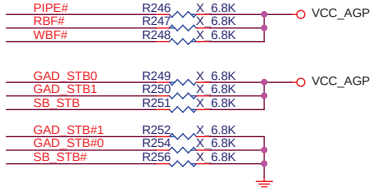
AGP SIGNAL REFERENCE CIRCUIT



NEAR AGP SLOT

AGP TERMINATION RESISTORS

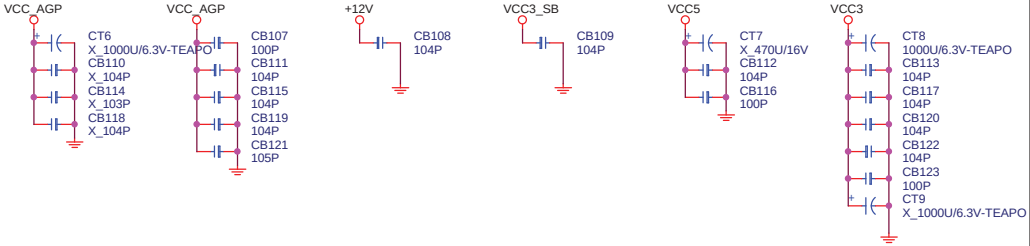




LESS 10MILS STUB TRACE LENGTH MUST BE FOLLOWING.

Place these resistors between PCI and AGP slot

AGP SLOT DECOUPLING CAPACITORS



Micro-Star	Title: MS-6507	Rev: 5.0
Document Number: AGP Slot		
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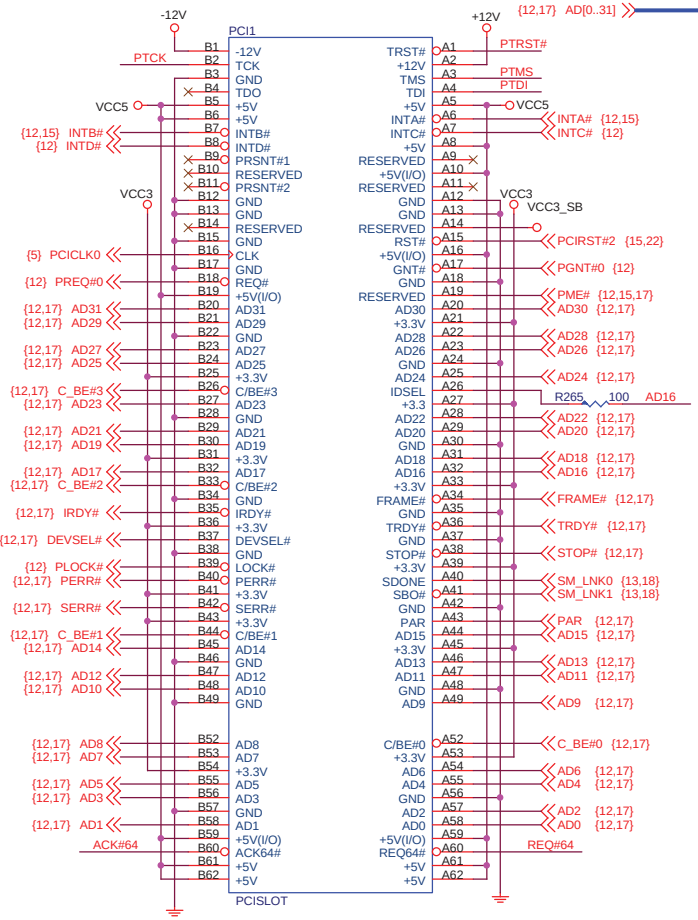
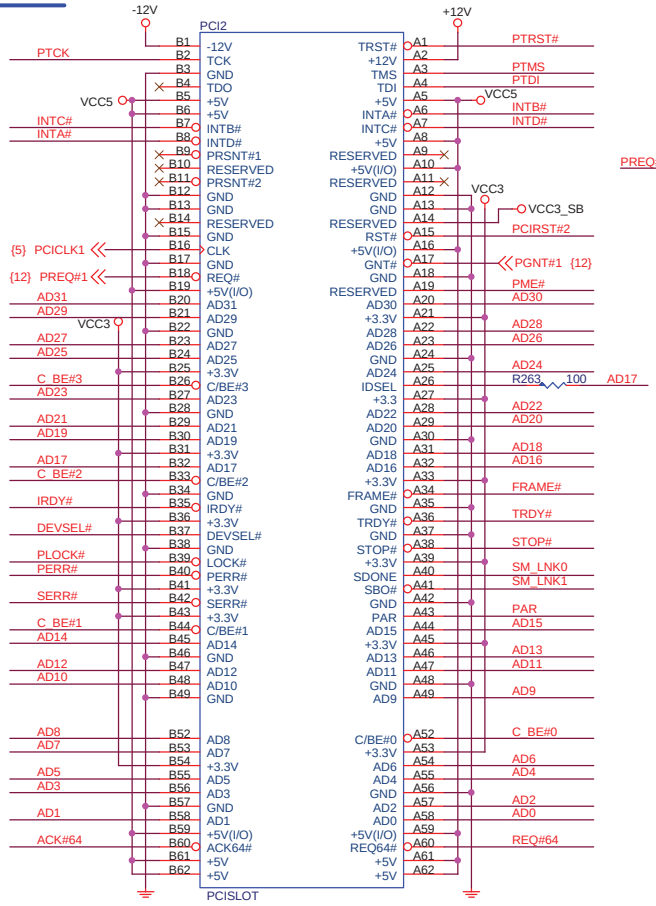
PCI SLOT 1 (PCI VER: 2.2 COMPLY)



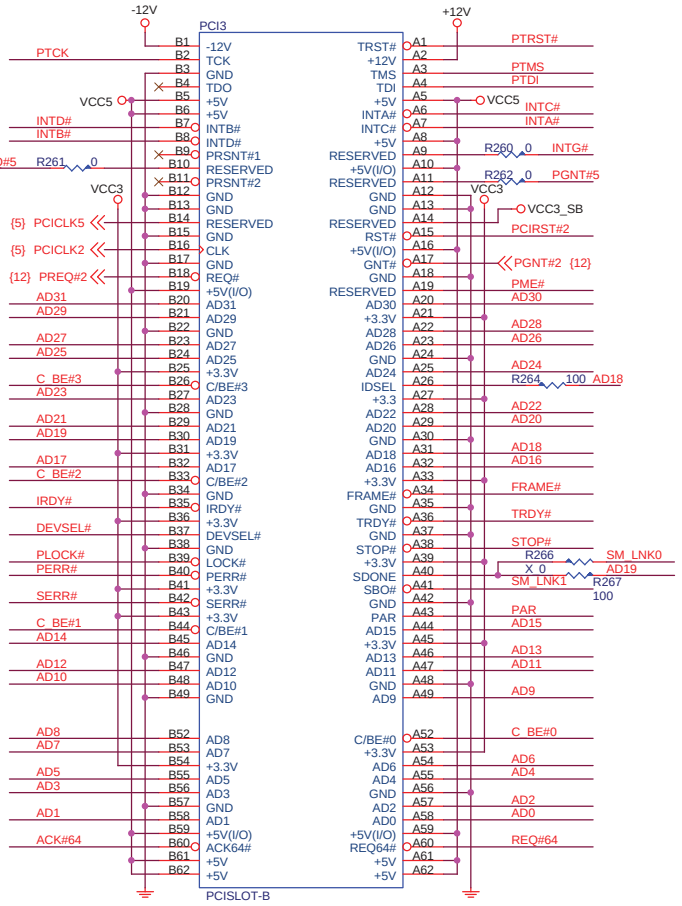
IDSEL = AD16
MASTER = PREQ0
INTA#

PCI SLOT 2 (PCI VER: 2.2 COMPLY)



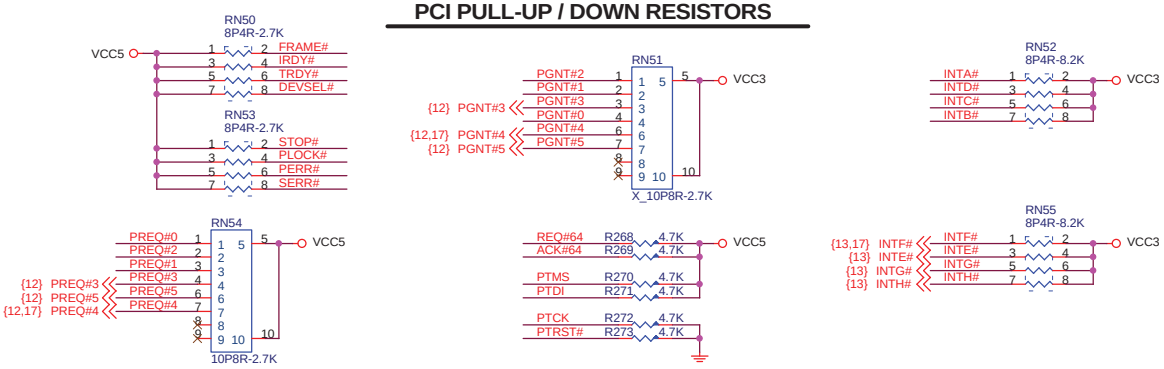
IDSEL = AD17
MASTER = PREQ1
INTB#

PCI SLOT 3 (PCI VER: 2.2 COMPLY)

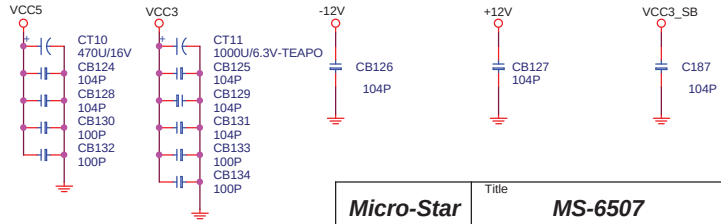


IDSEL = AD18
MASTER = PREQ2
INTC#

PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS



Micro-Star	Title: MS-6507	Rev: 5.0
Document Number: PCI Slot 1 & 2 & 3		
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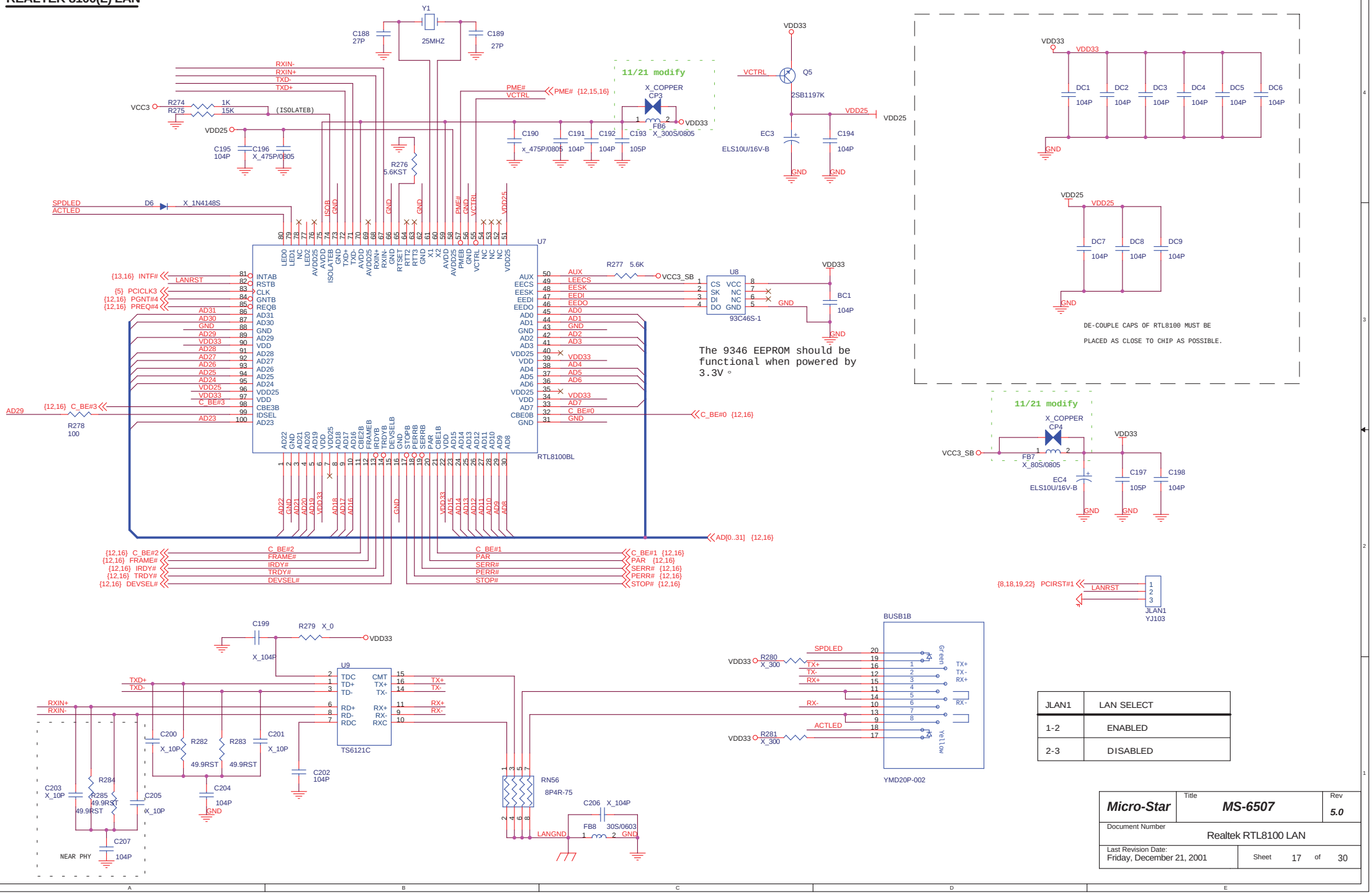
REALTEK 8100(L) LAN



JLAN1	LAN SELECT
1-2	ENABLED
2-3	DISABLED

Micro-Star	Title: MS-6507	Rev: 5.0
Document Number: Realtek RTL8100 LAN		
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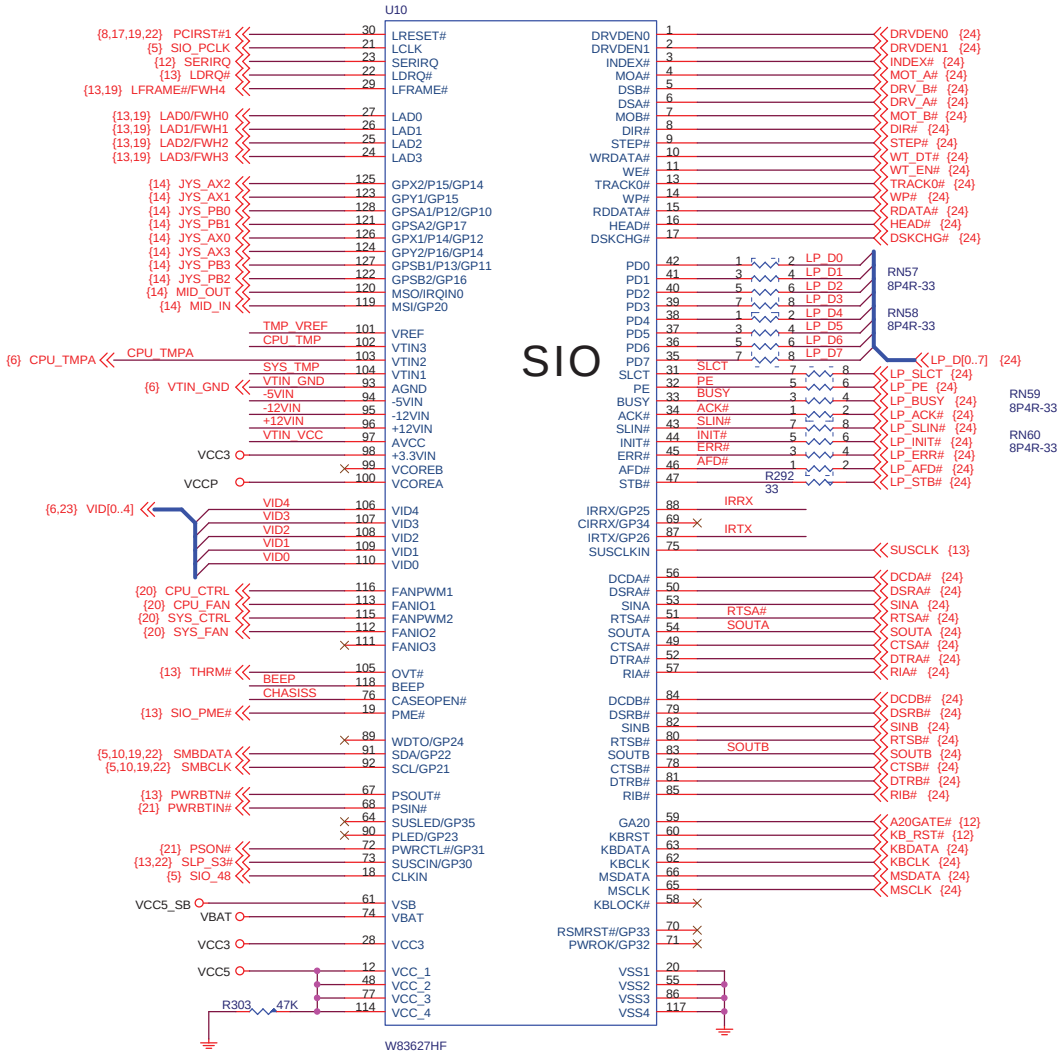
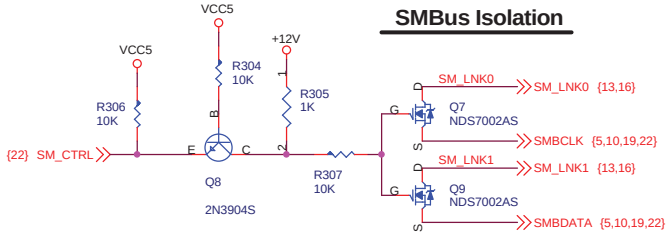
Hardware Monitor

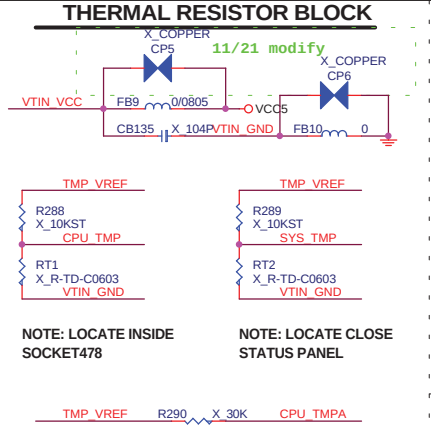
LPC SUPER I/O W83627HF



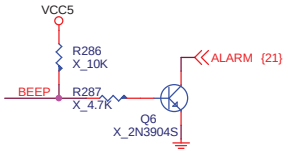
SMBus Isolation



THERMAL RESISTOR BLOCK

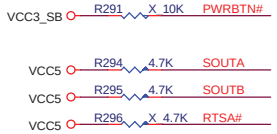


SPEAKER BLOCK



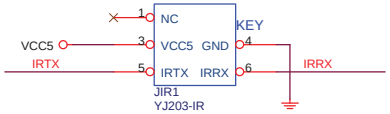
CHASISS INTRUSION HEADER

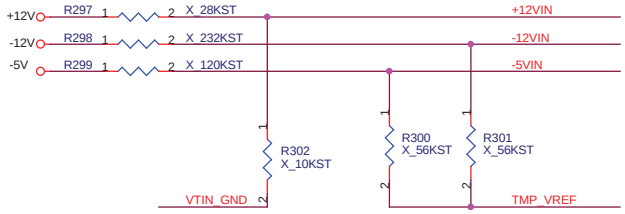
SUPER I/O STRAPPING RESISTOR



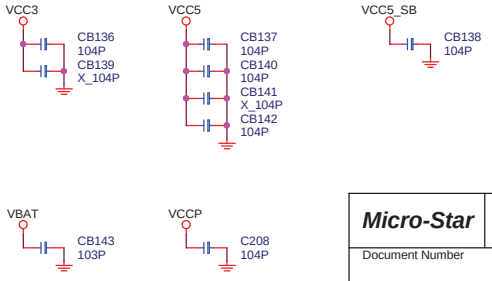
SOUTA	L: Disable KBC	H: Enable KBC
SOUTB	L: 24MHZ	H: 48MHZ
RTSA#	L: CFAD=2E	H: CFAD=4E
DTRA#	L: PNP Default	H: PNP no Default

Intel IR Connector





DECOUPLING CAPACITOR



Micro-Star	Title: MS-6507		Rev: 5.0
Document Number: LPC I/O W83627HF			
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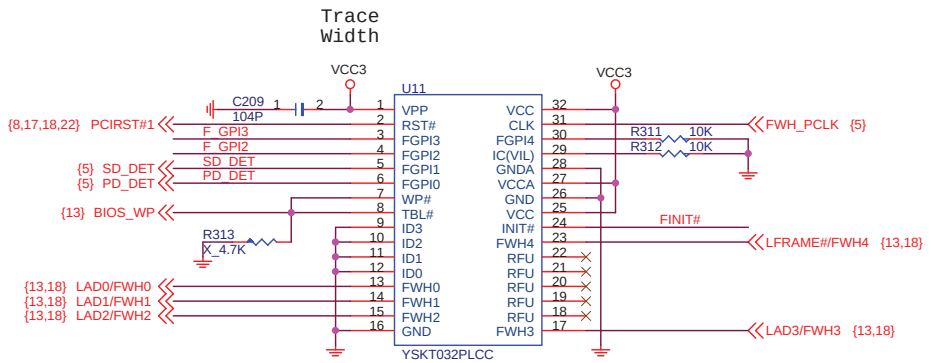
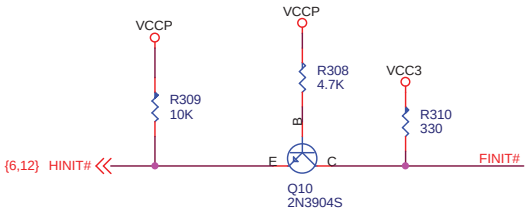
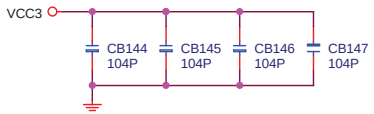
Firware Hub (FWH)



FWH INIT Signal Voltage Translation Block

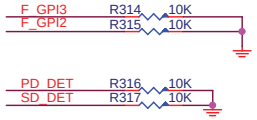


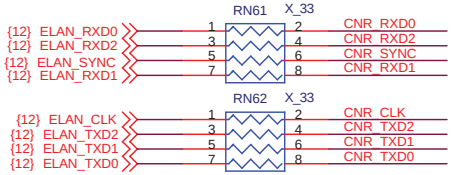
FWH DECOUPLING CAPACITORS



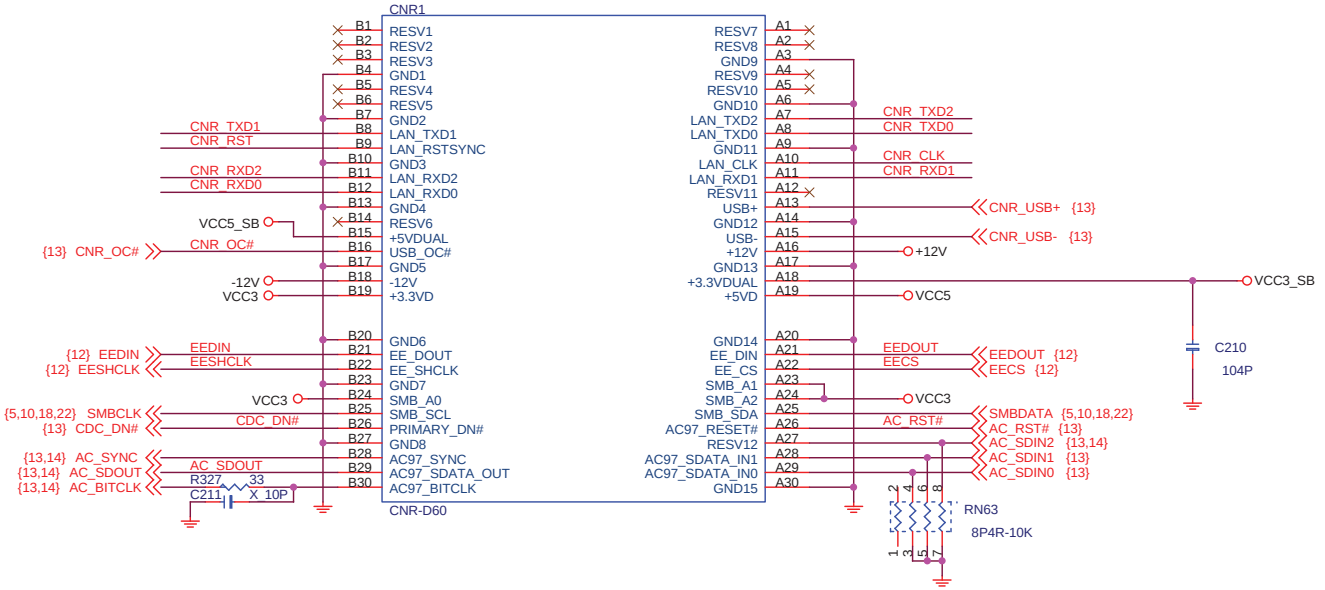
Near ICH4

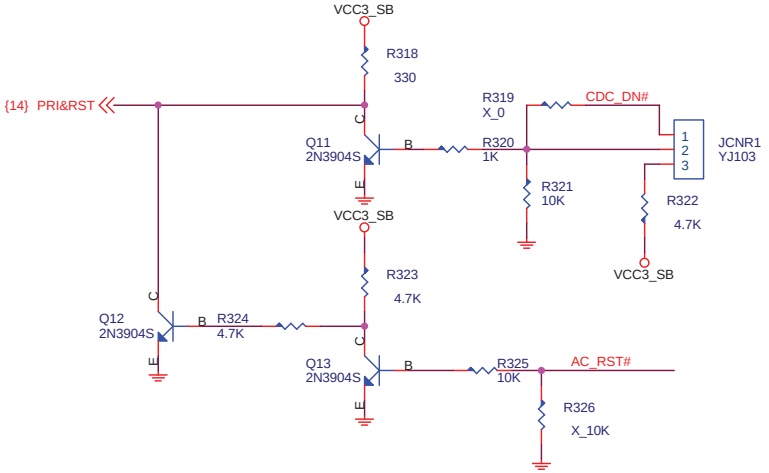
FWH RESISTORS





CNR RISER

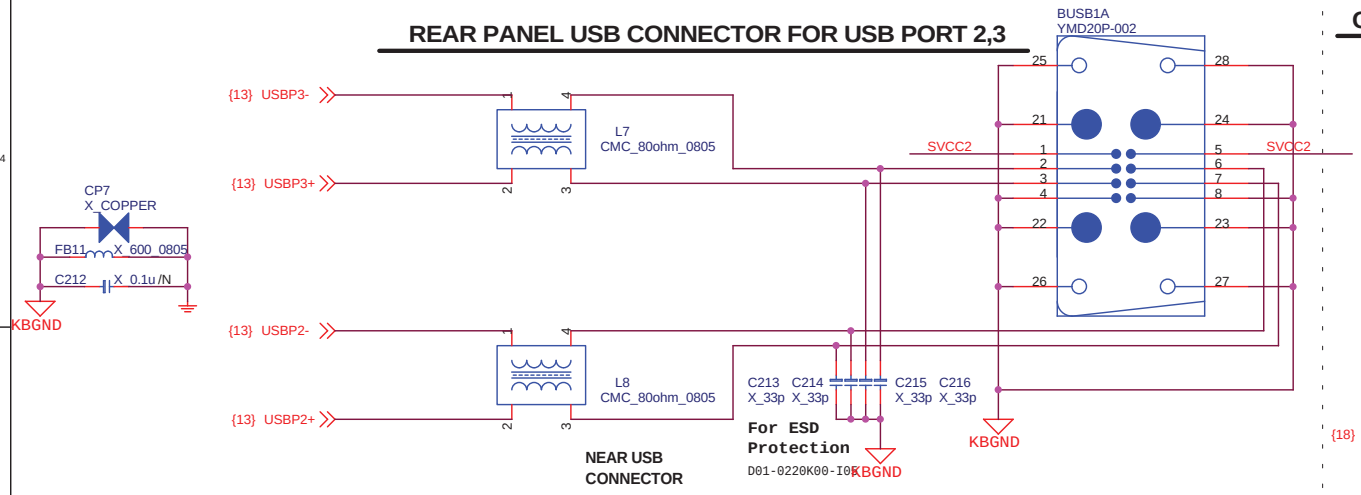




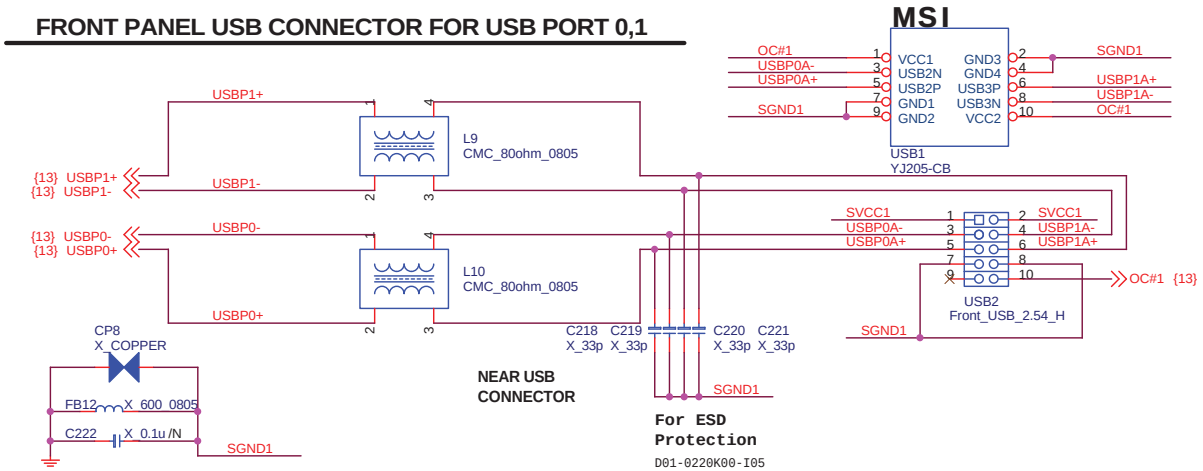
Micro Star Restricted Secret

Title: FWH & CNR & AC'97 Control	Rev: 5.0
Document Number: MS-6507	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Friday, December 21, 2001 Sheet 19 of 30

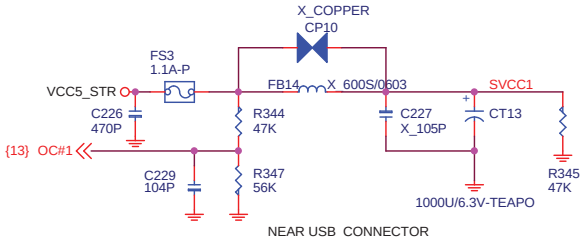
REAR PANEL USB CONNECTOR FOR USB PORT 2,3



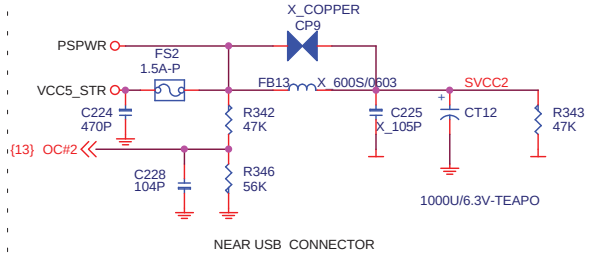
FRONT PANEL USB CONNECTOR FOR USB PORT 0,1



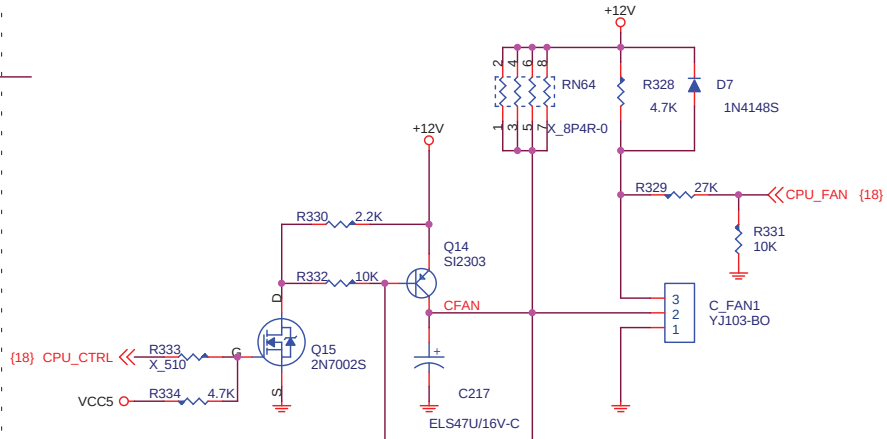
POWER CIRCUIT FOR USB PORT 0,1



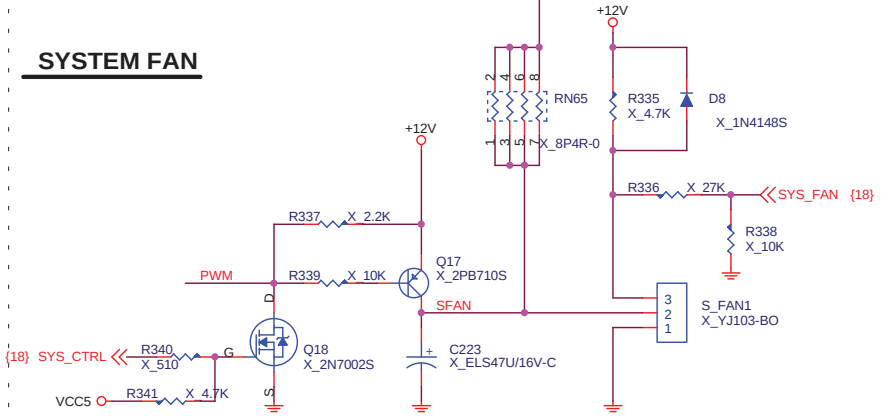
POWER CIRCUIT FOR USB PORT 2, 3



CPU FAN



SYSTEM FAN



Micro-Star	Title: MS-6507	Rev: 5.0
Document Number: USB & FAN Connectors		
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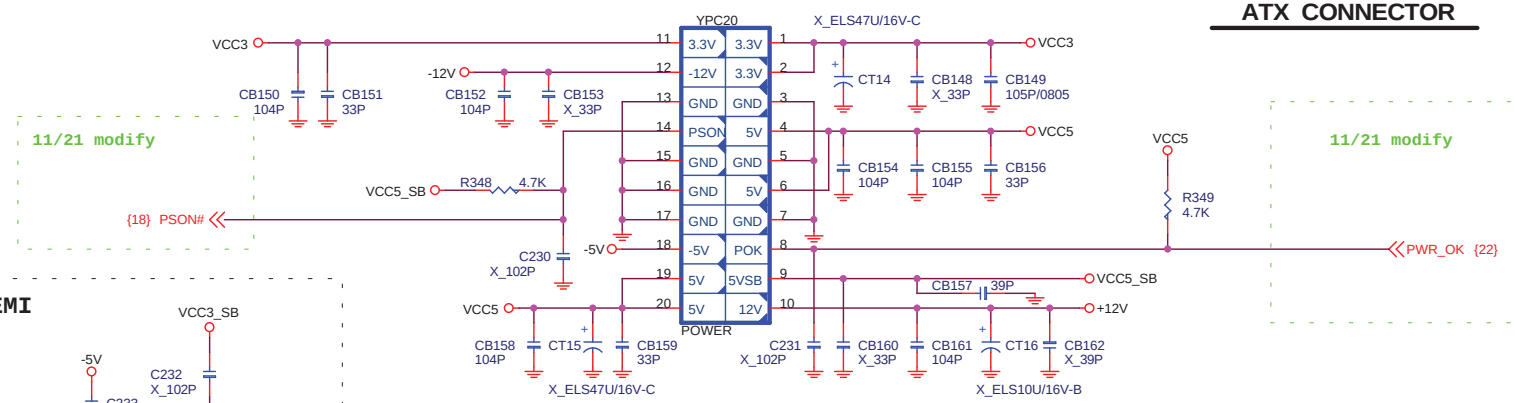
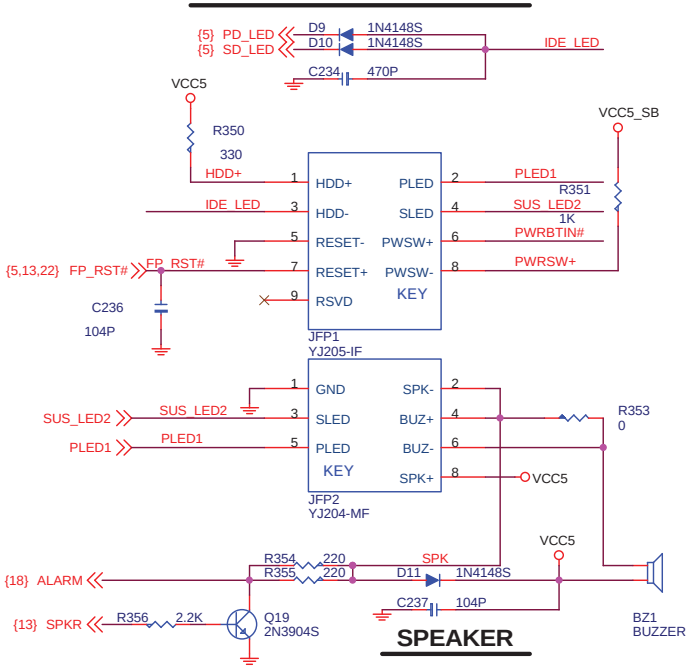
ATX CONNECTOR



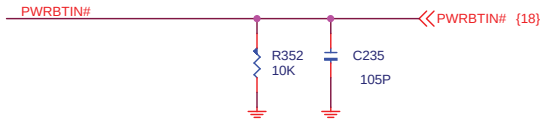
EMI

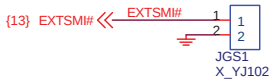
Brookdale FRONT PANEL-M



SPEAKER

POWER BUTTON





Micro-Star	Title: MS-6507	Rev: 5.0
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REGULATORS OUTPUT DECOUPLING CAPACITORS

POWER Bulk Decuping	470UF	1000UF
VCC_DIMM		2
VCC_AGP		2
VCC5	2	
VCC3		3
VCC5_STR	2	
DDR_VTT		2
VCC1_8		1
VCC3_SB		2
VCC5_SB		2

**S50# pin function(Hi level = 5V)
same as 5VUSB(Hi level = 12V)

SEL0	5VUSB
H	2 MOSFET
L	1 MOSFET

5VUSB USE 2 MOSFET

For 5VDUAL

Low RDS ON MOSFET

For AGP

For DDR VTT

For P4-1.2V

For DDR

For MuTIOL

DUAL LAYOUT

Reserved

THIS PIN IS OPEN DRAIN OUTPUT

SEL1	VRAM	VRAM_2.5
H	3.3VDUAL	2.5V
TRI-STATE	3.3VSB	2.5V
L	3.3VSTR	1.25V

FOR 3VSB OR 3VSTR
SETTING BY SEL1

FOR 3VDUAL ** SETTING 3VSTR THEN VRAM_2.5
SETTING BY BECOME TO 1.25 VREF
SEL1

Get Close.

1.8V STANDBY POWER TRANSLATOR

(40mils trace / 20 mils space)

1.8V POWER TRANSLATOR

11/21 modify

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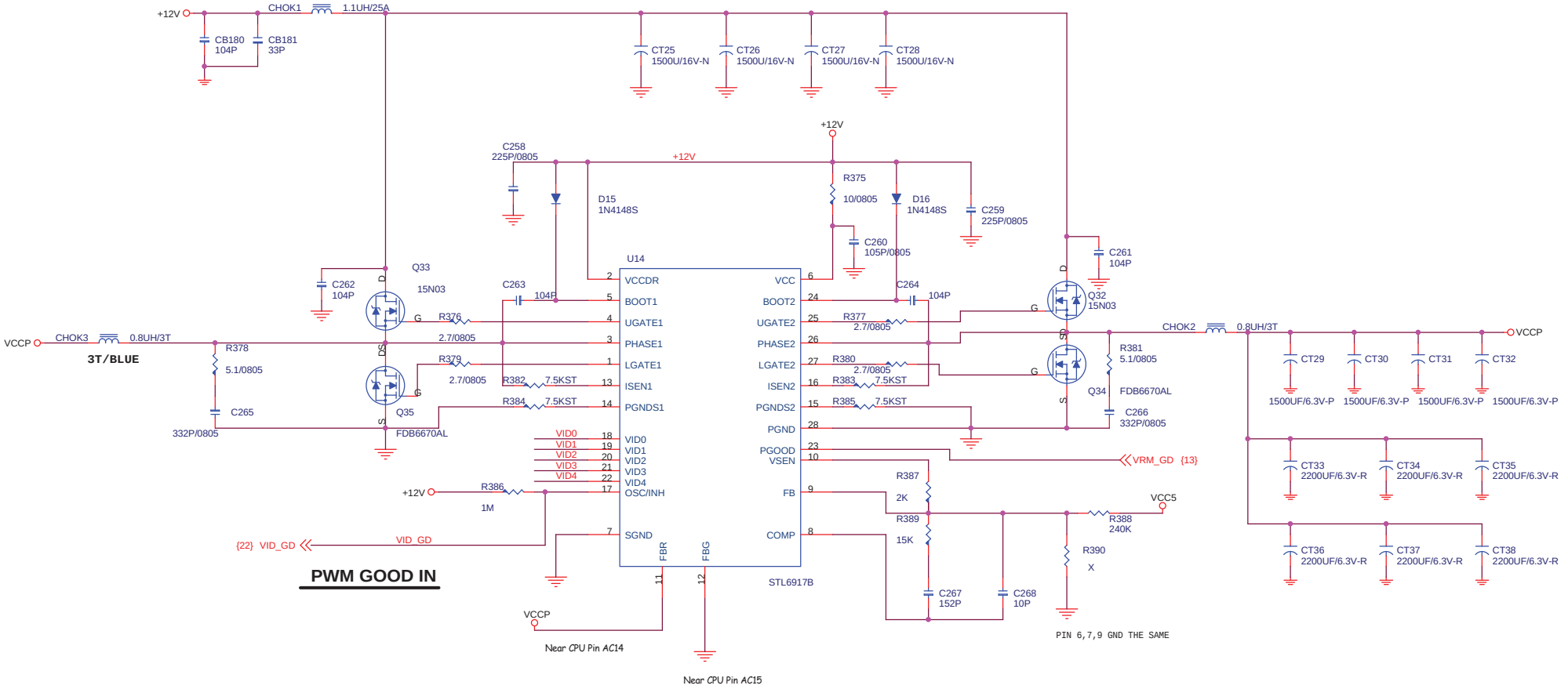
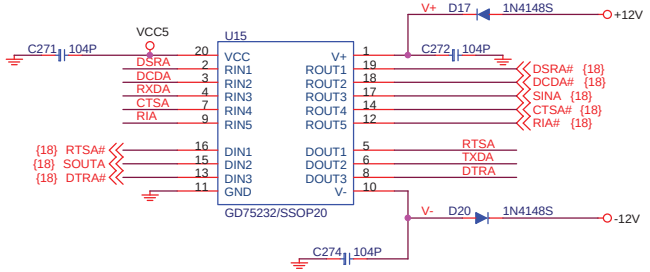
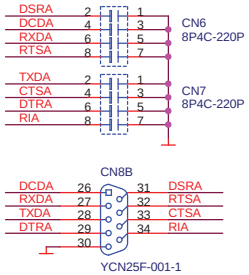


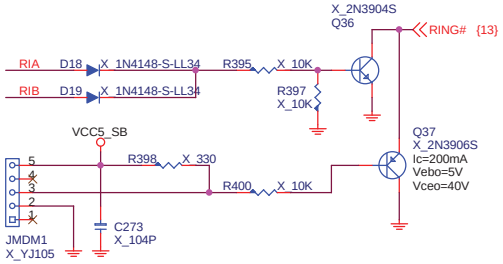
Micro-Star	Title: MS-6507	Rev: 5.0
Document Number: VRM 9.0		
Last Revision Date: Friday, December 21, 2001	Sheet 23 of 30	

SERIAL PORT 1

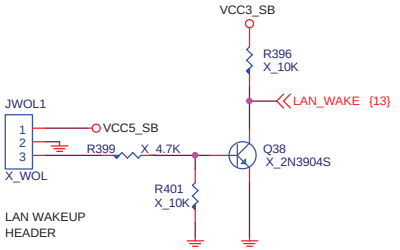




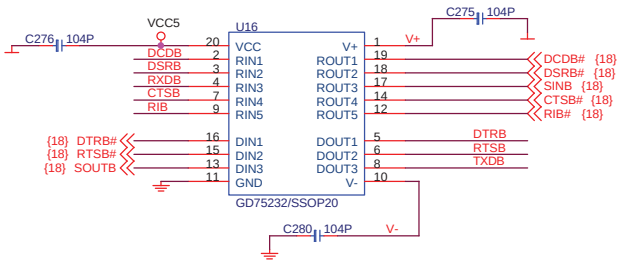
MODEM RING BLOCK

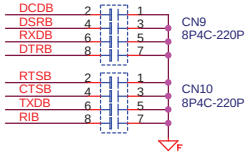


LAN WAKEUP BLOCK

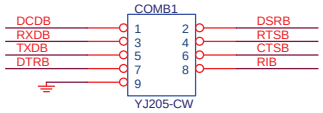


SERIAL PORT 2

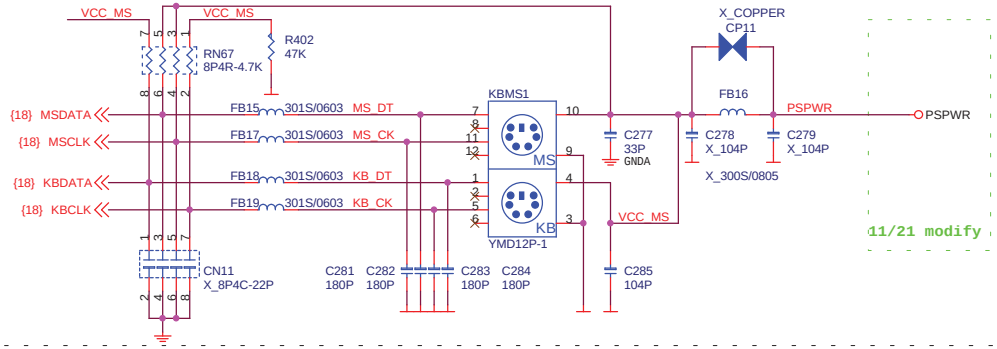




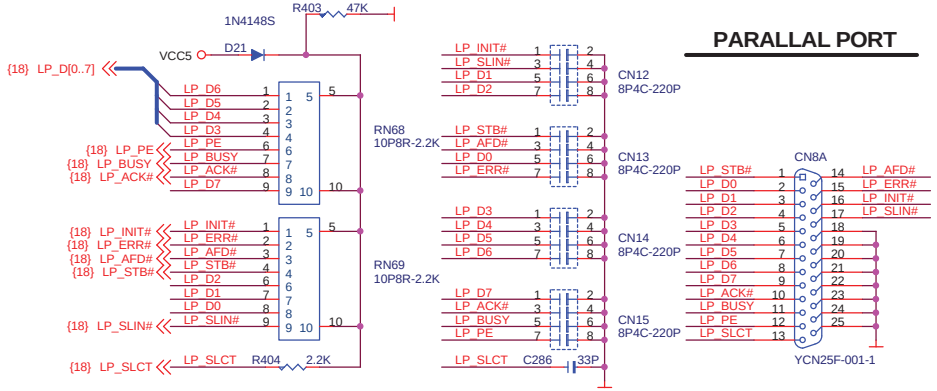
COM2 HEADER



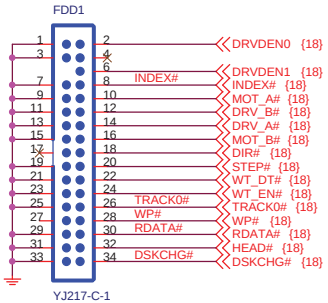
PS2 KEYBOARD & MOUSE CONNECTOR



PARALLAL PORT



FLOPPY CONNECTOR



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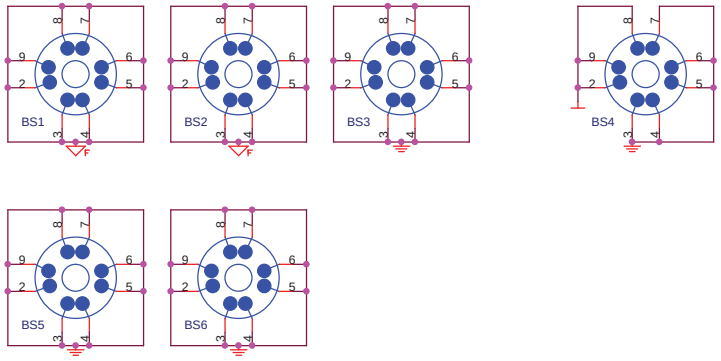
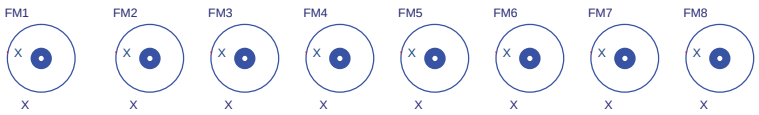
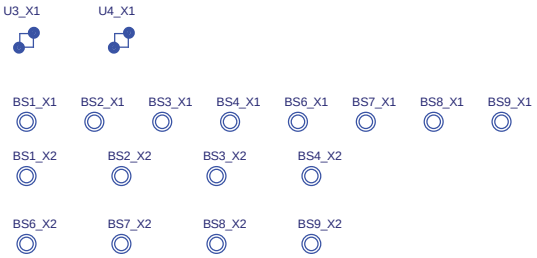
Jumper Setting & Connector Setting

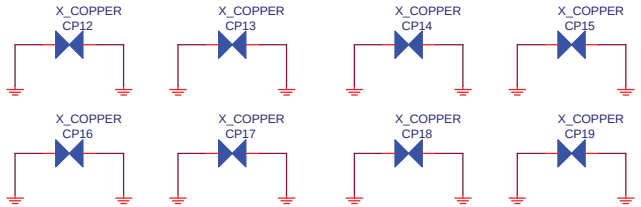
Jumper	Description	
JAUDIO1	AUDIO FRONT PANEL HEADPHONE JACK HEADER	
JBAT1	CLEAR CMOS	
1-2	NORMAL	(Default)
2-3	CLEAR CMOS	
CD_IN1	CDROM HEADER (ATAPI)	
USB1	EXTERNAL USB	
J11/12	CENTER/SUBWOOFER SELECT	
JLAN1	ONBOARD LAN ENABLE/DISABLE	
COMB1	EXTERNAL COMB	

Connector	Description
U7	INTEL mPGA478-B CPU
IDE1	Primary
IDE2	Secondary
DIM1	SDRAM DIMM1
DIM2	SDRAM DIMM2
AGP1	AGP Slot
PCI1	PCI Slot1
PCI2	PCI Slot2
PCI3	PCI Slot3(MEDION SPEC)
COM1	Serial Port
COMB1	Serial Port
LPT	Parallel Port
FDD1	Floopy
JMDM1	MODEM RING HEADER
JWOL1	LAN WAKEUP HEADER
KBMS1	PS/2 Keyboard and PS/2 mouse
C_FAN1	CPU FAN HEADER
USB	USB REAR CONNECTOR
USB1	USB INTERNAL HEADER
POWER	ATX Power
F_P1	Front Panel
JPW1	ATX12V Power









SIMULATION TRACE

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Pentium 4 Processor /Northwood mPGA 478

Source Synchronous Signal Group and the Associated Strobes

Signals	Associated Strobe
REQ[4:0],A[16:3]#	ADSTB0#
A[31:17]#	ADSTB1#
D[15:0]#,DBI0#	DSTBP0#,DSTBN0#
D[31:16]#,DBI1#	DSTBP1#,DSTBN1#
D[47:32]#,DBI2#	DSTBP2#,DSTBN2#
D[63:48]#,DBI3#	DSTBP3#,DSTBN3#

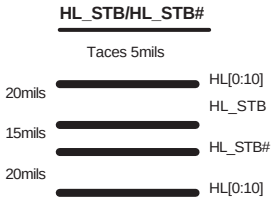
Signals	Length	Inaccuracy
Data	**2.0" to 10.0"**	+/- 100 mil
Address	**2.0" to 10.0"**	+/- 200 mil
Strobe	**2.0" to 10.0"**	+/- 25 mil
Clock	**2.0" to 10.0"**	Don't need

***** Delta=(CPU_pkglen.net-CPUpkglen.strobe)+(CS_pkglen.net-CS_pkglen.strobe)
Trace : 7 mil width 13mil space

Miscellaneous Signals

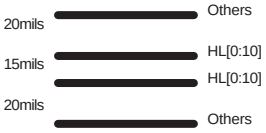
HL_STB/HL_STB#

Taces 5mils



* Max Length : 8"
* STB and STB# Length must be equal

HL[10..0]



* Max Length : 8"
* Length must be matched within +/- 0."
of the Strobe Signals

USB

*** USB Trace width : 9 mils**
*** USB Trace Spacing : 25 mils**
*** Differential USB Signlas Trace Spacing : 18 mils**
*** USB Power Trace must be 40mils width**

AGP

1X Timing group	2X/4X Timing group
AGPCLK PIPE# RBF# WBF# ST[2..0] GFRAME# GIRDY# GTRDY# GSTOP# GDEVSEL# GREQ# GGNT# GPAR	__SET#1__ GAD[15..0] GC_BE#[1..0] GAD_STB0 GAD_STB0# __SET#2__ GAD[31..16] GC_BE#[3..2] GAD_STB1 GAD_STB1# __SET#3__ SBA[7..0] SB_STB SB_STB#

SIGNALS	Maximum Length	Width	Space	Dismatch Length	Relative to
1X Timing group	7.5"	5 mil	5 mil	X	X
2X/4X Timing group SET#1	7.25"	5 mil	20 mil	+/- 0.125"	GAD_STB0 GAD_STB0#
2X/4X Timing group SET#2	7.25"	5 mil	20 mil	+/- 0.125"	GAD_STB1 GAD_STB1#
2X/4X Timing group SET#3	7.25"	5 mil	20 mil	+/- 0.125"	SB_STB SB_STB#
2X/4X Timing group SET#1	6"	5 mil	15 mil	+/- 0.25"	GAD_STB0 GAD_STB0#
2X/4X Timing group SET#2	6"	5 mil	15 mil	+/- 0.25"	GAD_STB1 GAD_STB1#
2X/4X Timing group SET#3	6"	5 mil	15 mil	+/- 0.25"	SB_STB SB_STB#

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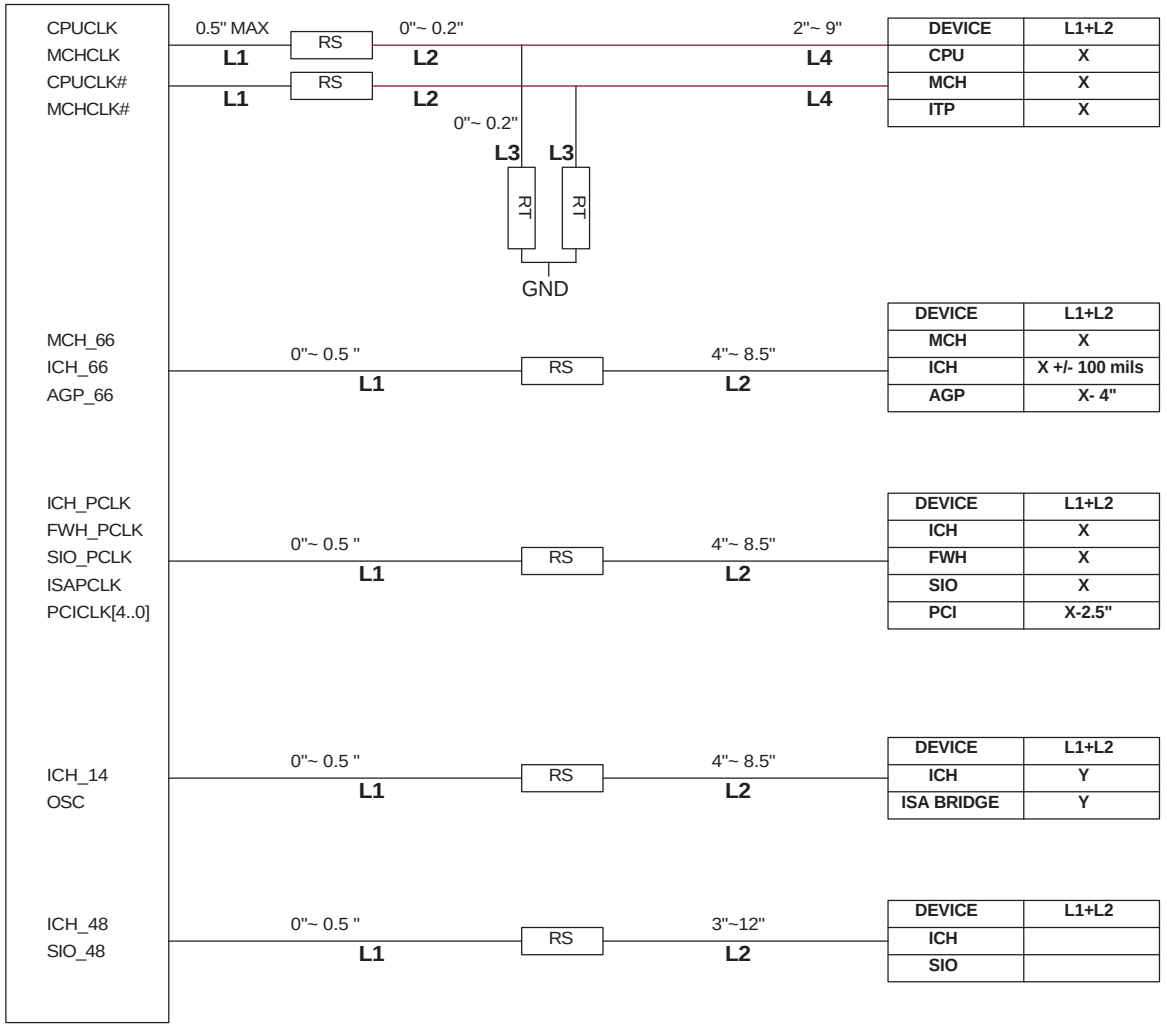


DEVICE	L1+L2
CPU	X
MCH	X
ITP	X

* Line Width : 7.0 mil
* Differential pair spacing : 7.0mil
* Spacing to other traces : 28 mil
* BCLK0/BCLK1 LENGTH MATCH +/- 10 mil

DEVICE	L1+L2
MCH	X
ICH	X +/- 100 mils
AGP	X- 4"

* Line Width : 5.0 mil
* Spacing to other traces : 20 mil

DEVICE	L1+L2
ICH	X
FWH	X
SIO	X
PCI	X-2.5"

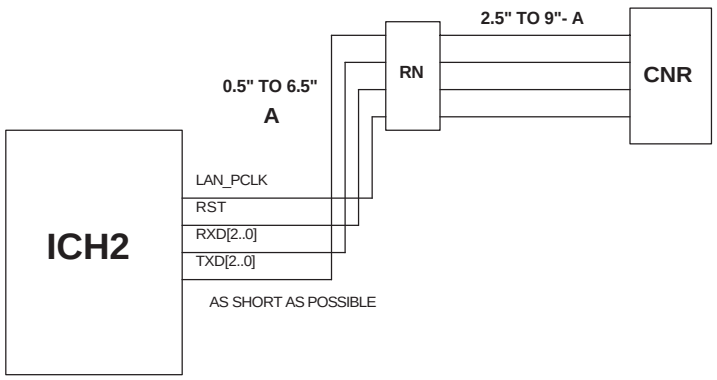
* Line Width : 5.0 mil
* Spacing to other traces : 20 mil
* L1/L2 TRACE SAME AS MCH_66 TRACE LENGTH

DEVICE	L1+L2
ICH	Y
ISA BRIDGE	Y

* Line Width : 5.0 mil
* Spacing to other traces : 10 mil

DEVICE	L1+L2
ICH	
SIO	

* Line Width : 5.0 mil
* Spacing to other traces : 20 mil



* Line Width : 7.0 mil
* Differential signls space : 14mils
* Differential signls length mismatch +/- 7mil

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SDRAM Routing Guidelines

5.Feedback - RDCLKO,RDCLKIN routing rule

2 or 3 DIMM feedback layout guideline

Signal	Length	Width	Trace Spacing
Trace L	50 mils	7 mil	5 mil

DDR-SDRAM Routing Guidelines

1.DDR bus reference plane stack-up

PCB Layer	Description
Layer 1	Signal
Layer 2	Ground Flood
Layer 3	Ground
Layer 4	Power / Signal

***All the memory bus signals must be referenced to GND**

2.DDR signal groups

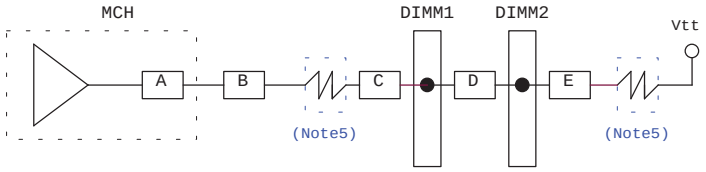
Group	Signals
Data	SDQ[63:0],SCB[7:0],SDQS[8:0]
Command	SMA[12:0],SBS[1:0],SRAS#,SCAS#,SWE#
Control	SCKE[3:0],SCS#[3:0]
Clock	SCK[5:0],SCK#[5:0]
Feedback	RCVENOUT#,RCVENIN#

3.SDQ[63:0],SCB[7:0],SDQS[8:],SCK/SCK#[5:0]routing rule

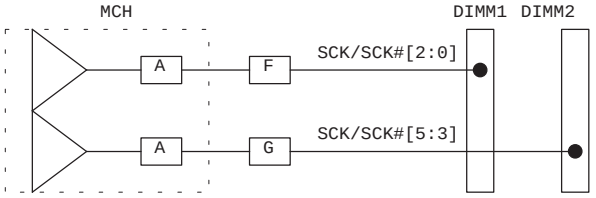
Signal	Length A	Length B	Length C	Length D	Length E	Width	Spacing	Routing Layer
SDQ[63:0] SCB[7:0] SQDS[8:0]	Package length	2.0" - 5.0"	Max = 0.5"	0.3' - 0.5"	0.1" - 0.8"	5 mil	(Note2)	Top
(Note1)	DIMM 1 = A + B + C = X DIMM 2 = A + B + C + D = X + D							
SCK/SCK#[2:0]	Package length	B+C+2"<= Length F <= B+C+1" 2.0" - 6.5"		None	None	5 mil	(Note4)	Bottom
	DIMM 1 = A + F =X + 1" to X + 2"							
SCK/SCK#[5:3] (Note3)	Package length	B+C+D+2"<=Length G <= B+C+D+1" 2.5" - 7.0"				5 mil	(Note4)	Bottom
	DIMM 2 = A + G =X + D + 1" to X + D + 2"							

*** Package length see Table - 4**

SDQ[63:0],SCB[7:0],SDQS[8:] layout guideline



SCK[5:0] layout guideline



Note1:Each data and strobe signal group must be length matching +/- 25 mils

SDQS[X] = +/- 25 mils SDQ[X]/SCB[X] group length

Signals	Associated Strobe
SDQ[7:0]	SDQ0
SDQ[15:8]	SDQ1
SDQ[23:16]	SDQ2
SDQ[31:17]	SDQ3
SDQ[39:32]	SDQ4
SDQ[47:40]	SDQ5
SDQ[55:48]	SDQ6
SDQ[63:56]	SDQ7
SCB[7:0]	SDQ8

Note2:Trace spacing normally = 12 mils and through between DIMM 2 pin = 7 mils, but breakout form MCH ball = 5 mils width with 7mils spacing for a max of 350mils

Note3:

- * SCK[X] length = SCK#[X] length
- * SCK/SCK#[2:0] routed to DIMM 0 are equal in length, and SCK/SCK#[5:3] routed to DIMM 1 are equal in 1length

Note4:

- * Between the pair differential clock 2 signal trace spacing = 7 mils
- * Differential Trace with 2.5V copper flood spacing = 10 mils minimum
- * Serpentine spacing = 20 mils minimum
- * Differential signals breakout form MCH = 5 mil width with 7 mil differential spacing and 7 mil isolation spacing from another signal for a max of 350 mils

Note5:Data group signal can NOT placed within the same RPACK's(series and parallel resistor packs) as the command or control group signal

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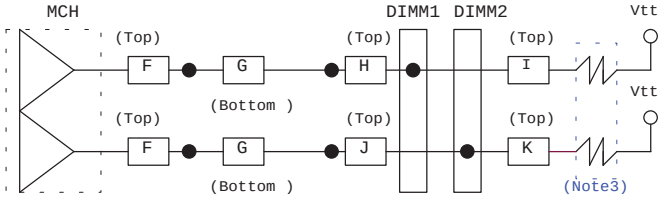
DDR-SDRAM Routing Guidelines

4.SCKE[3:0],SCS#[3:0] routing rule

DIMM 0					
Signal	Length F	Length G	Length H	Length I	Width
SCS#[1:0] SCKE[1:0] (Note1)	Max = 40 mils	2.0" - 3.5"	Max = 500 mils (Note2)	0.4" - 1.3"	5 mils
Total lenght	DIMM0 SCK/SCK#[2:0] length = X" DIMM0 SCS#/SCKE length = F + G + H =X"- 1"				

DIMM 1					
Signal	Length F	Length G	Length J	Length K	Width
SCS#[3:2] SCKE[3:2] (Note1)	Max = 40 mils	2.0" - 3.5"	Max = 1" (Note2)	0.1" - 0.8"	5 mils
Total lenght	DIMM1 SCK/SCK#[5:3] length = Y" DIMM1 SCS#/SCKE length = F + G + J =Y"- 1"				



Note1:

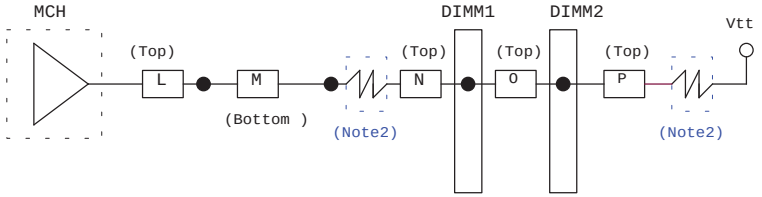
* Trace spacing normally = 12 mils and through between DIMM 2 pin or DIMM to Rtt = 7 mils, but breakout form MCH ball = 5 mils width with 7mils spacing for a max of 350mils
* Trace with 2.5V copper flood spacing = 7 mils minimum
* Isolation spacing form another group signal spacing = 20 mils minimum
* Control signals breakout form MCH = 5 mil width with 7 mil spacing for a max of 350 mils

Note2:This purpose prevent break form DIMM0 bottom size 2.5V copper flood to MCH power plane

Note3:Control group signal can NOT placed within the same parallel resistor packs as the command or data group signal

5.SMA[12:0],SBS[1:0],SRAS#,SCAS# routing rule

Signal	Length L	Length M	Length N	Length O	Length P	Width
SMA[12:0] SBS[1:0] SRAS# SCAS# (Note1)	Max = 40 mils	2.0" - 3.5"	Max = 500 mils	0.3" - 0.5"	0.1" - 0.8"	5 mils
DIMM 0 Total lenght	DIMM0 SCK/SCK#[2:0] length = X" Command signal length = L + M + N = X" - 1"					
DIMM 1 Total lenght	DIMM0 SCK/SCK#[5:3] length = Y" Command signal length = L + M + N + O = Y" - 1"					



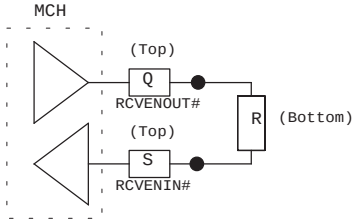
Note1:

* Trace spacing normally = 12 mils and through between DIMM 2 pin or DIMM to Rtt = 7 mils, but breakout form MCH ball = 5 mils width with 7mils spacing for a max of 350mils
* Trace with 2.5V copper flood spacing = 7 mils minimum
* Isolation spacing form another group signal spacing = 20 mils minimum
* Command signals breakout form MCH = 5 mil width with 7 mil spacing for a max of 350 mils

Note2:Command group signal can NOT placed within the same RPACK's(series and parallel resistor packs) as the data or control group signal

5.Feedback - RCVENOUT#,RCVENIN# routing rule

Signal	Length Q	Length R	Length S	Width
RCVENOUT# RCVENIN# (Note1)	40 mils	Equal 1"	40 mils	5 milS
Total Length	Q + R + S = 1080 mils			



Note1:

* Trace spacing = 12 mils
* Trace with 2.5V copper flood spacing = 7 mils minimum
* Isolation spacing form another group signal spacing = 10 mils minimum
* Command signals breakout form MCH = 5 mil width with 7 mil spacing for a max of 350 mils

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Table - 4

DDR Data Signals(1)		
Signal	MCH ball	Package length(")
SDQ0	G28	0.716
SDQ1	F27	0.699
SDQ2	C28	0.874
SDQ3	E28	0.754
SDQ4	H25	0.532
SDQ5	G27	0.666
SDQ6	F25	0.592
SDQ7	B28	0.892
SDQ8	E27	0.797
SDQ9	C27	0.833
SDQ10	B25	0.812
SDQ11	C25	0.753
SDQ12	B27	0.886
SDQ13	D27	0.867
SDQ14	D26	0.773
SDQ15	E25	0.645
SDQ16	D24	0.722
SDQ17	E23	0.602
SDQ18	C22	0.699
SDQ19	E21	0.566
SDQ20	C24	0.785
SDQ21	B23	0.781
SDQ22	D22	0.640
SDQ23	B21	0.711
SDQ24	C21	0.627
SDQ25	D20	0.555
SDQ26	C19	0.587
SDQ27	D18	0.522
SDQ28	C20	0.615
SDQ29	E19	0.487
SDQ30	C18	0.579
SDQ31	E17	0.521

DDR Data Signals(2)		
Signal	MCH ball	Package length(")
SDQ32	E13	0.432
SDQ33	C12	0.543
SDQ34	B11	0.596
SDQ35	C10	0.590
SDQ36	B13	0.639
SDQ37	C13	0.552
SDQ38	C11	0.588
SDQ39	D10	0.626
SDQ40	E10	0.533
SDQ41	C9	0.605
SDQ42	D8	0.587
SDQ43	E8	0.522
SDQ44	E11	0.523
SDQ45	B9	0.715
SDQ46	B7	0.706
SDQ47	C7	0.643
SDQ48	C6	0.700
SDQ49	D6	0.664
SDQ50	D4	0.760
SDQ51	B3	0.922
SDQ52	E6	0.640
SDQ53	B5	0.846
SDQ54	C4	0.810
SDQ55	E5	0.670
SDQ56	C3	0.859
SDQ57	D3	0.811
SDQ58	F4	0.723
SDQ59	F3	0.814
SDQ60	B2	0.949
SDQ61	C2	0.893
SDQ62	E2	0.865
SDQ63	G5	0.689

DDR ECC Signals		
Signal	MCH ball	Package length(")
SCB0	C16	0.570
SCB1	D16	0.526
SCB2	B15	0.623
SCB3	C14	0.533
SCB4	B17	0.621
SCB5	C17	0.583
SCB6	C15	0.540
SCB7	D14	0.503

DDR Data Strobe Signals		
Signal	MCH ball	Package length(")
SDQS0	F26	0.651
SDQS1	C26	0.775
SDQS2	C23	0.738
SDQS3	B19	0.636
SDQS4	D12	0.493
SDQS5	C8	0.596
SDQS6	C5	0.776
SDQS7	E3	0.821
SDQS8	E15	0.520

DDR Clock Signals		
Signal	MCH ball	Package length(")
SCK0	E14	0.453
SCK#0	F15	0.432
SCK1	J24	0.454
SCK#1	G25	0.587
SCK2	G6	0.551
SCK#2	G7	0.543
SCK3	G15	0.371
SCK#3	G14	0.349
SCK4	E24	0.610
SCK#4	G24	0.548
SCK5	H5	0.589
SCK#5	F5	0.693

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