Last Schematic Update Date:
06/01/2001

MS-6506 *Version 0A*

INTEL (R) Brookdale Chipset
Willamette/Northwood 478pin mPGA-B Processor Schematics

FormFactor : Flex-ATX (22.4 X 19.2mm) for NEC-CI

CPU:

Willamette/Northwood mPGA-478B Processor

System Brookdale Chipset:

INTEL MCH (North Bridge) +
INTEL ICH2 (South Bridge)

On Board Chipset:

BIOS -- FWH

LPC Super I/O -- W83627HF

Clock Generation -- ICS950208

Expansion Slots:

AGP2.0 SLOT * 1
PCI2.2 SLOT * 2
CNR SLOT * 1

ERP BOM	Function Description	
601-6506-A10	MS-6506 Ver:0A	With AGP,CNR,STR. NEC-CI Led.

Title	Rev
Cover Sheet	0A
Document Number: MS-6506	
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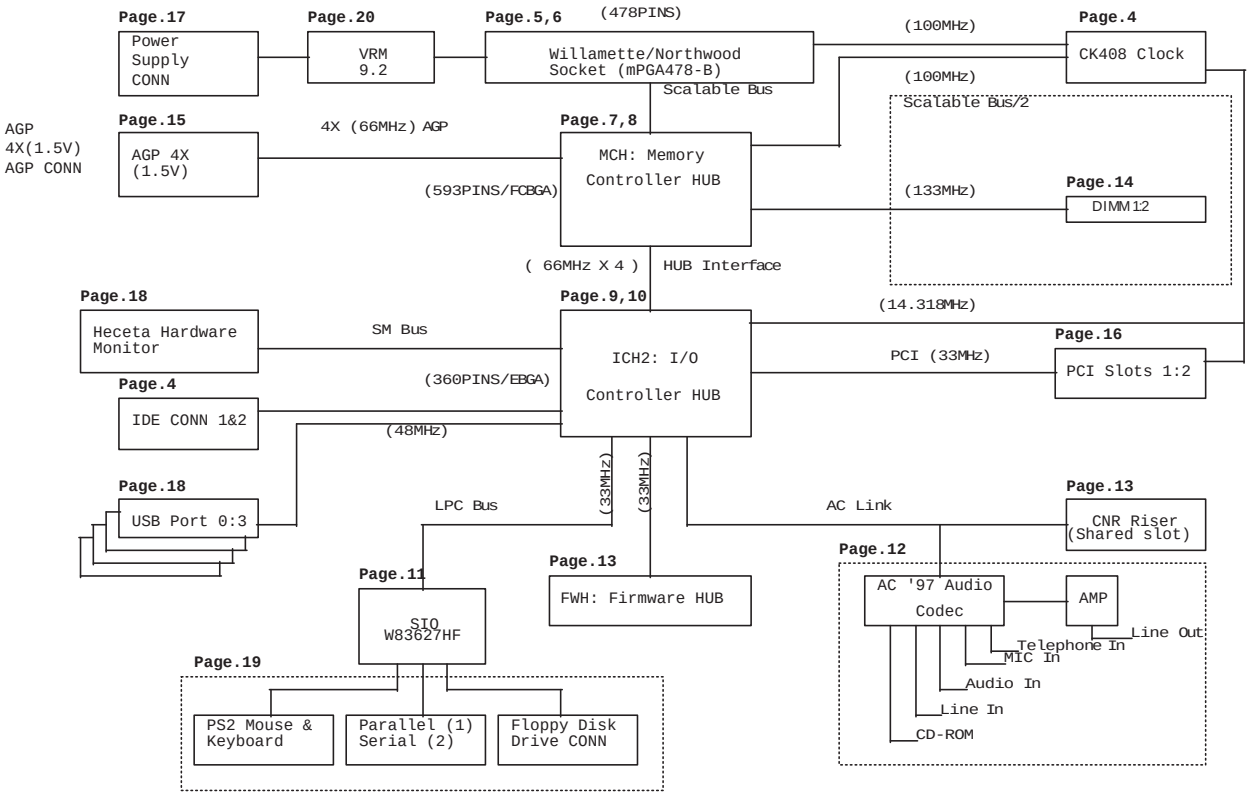

Micro Star Restricted Secret

Title: Block Diagram	Rev: 0A
Document Number: MS-6506	
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General Purpose I/O Spec.

ICH2

GPIO Pin	Type	Function
GPIO 0	I	REQ#A
GPIO 1	I	PREQ#5
GPIO 2	I	INTE#
GPIO 3	I	INTF#
GPIO 4	I	INTG#
GPIO 5	I	INTH#
GPIO 6	I	AC97 Enabled/Disabled
GPIO 7	I	None
GPIO 8	I	Non Connect
GPIO 9	I	AC'97 Serial Data In
GPIO 10	I	Non Connect
GPIO 11	I	Non Connect
GPIO 12	I	External SMI
GPIO 13	I	LPC PME
GPIO 14~15	I	Not Implemented
GPIO 16	O	Non Connect
GPIO 17	O	Non Connect
GPIO 18	O	Not Implemented
GPIO 19	O	Not Implemented
GPIO 20	O	Non
GPIO 21	O	Vpp Programming Control
GPIO 22	O	Not Implemented
GPIO 23	OD	BIOS Locked/Unlocked
GPIO 24	O	Non
GPIO 25	O	Non
GPIO 26	O	Non
GPIO 27	I/O	Non
GPIO 28	I/O	non
GPIO 29~31	I/O	Not Implemented

FWH

GPIO Pin	Type	Function
GPI 0	I	ATA IDE 1 Detect
GPI 1	I	ATA IDE 2 Detect
GPI 2	I	Auto Recovery
GPI 3	I	Reserved

DEVICE	ICH INT Pin	IDSEL
PCI Slot 1	INTA# INTB# INTC# INTD#	AD16
PCI Slot 2	INTF# INTG# INTH# INTE#	AD17

Title: GPIO Spec.	Rev: 0A
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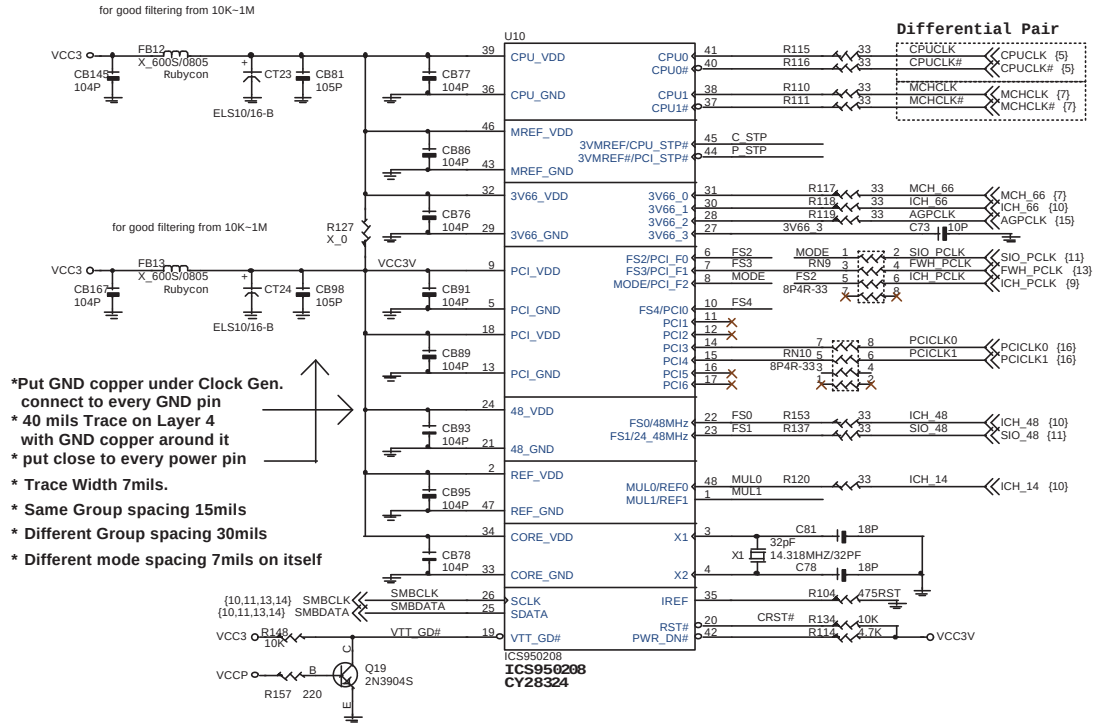
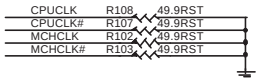
CLOCK GENERATOR BLOCK

*Trace less 0.5"



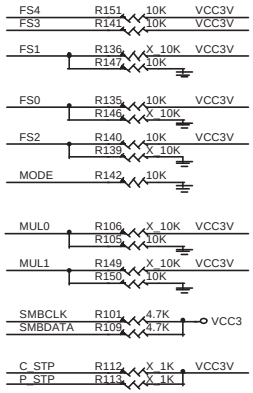
Shut Source Termination Resistors



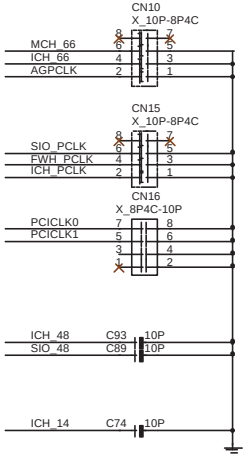
Trace less 0.2"

49.9ohm for 50ohm M/B impedance

CLOCK STRAPPING RESISTORS



Pull-Down Capacitors

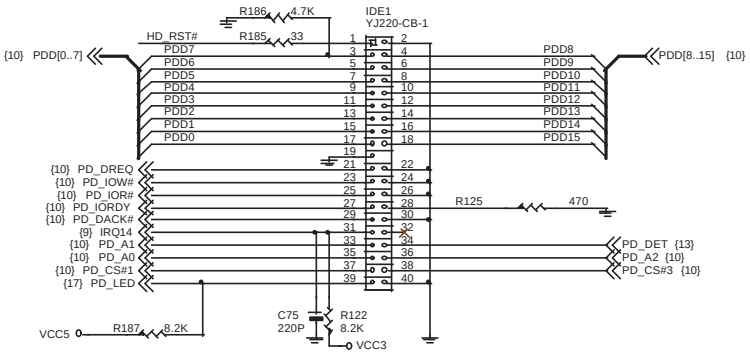


used only for EMI issue

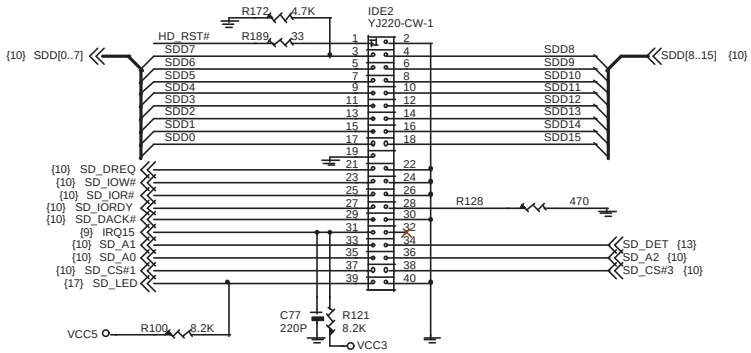
Trace less 0.2"

ATA100 IDE CONNECTORS

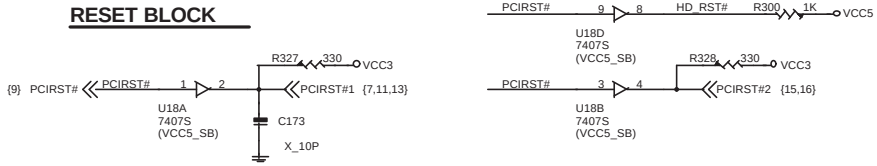
PRIMARY IDE BLOCK



SECONDARY IDE BLOCK



RESET BLOCK



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Title: Clock CY28323/4 & ATA100 IDE	Rev: 0A
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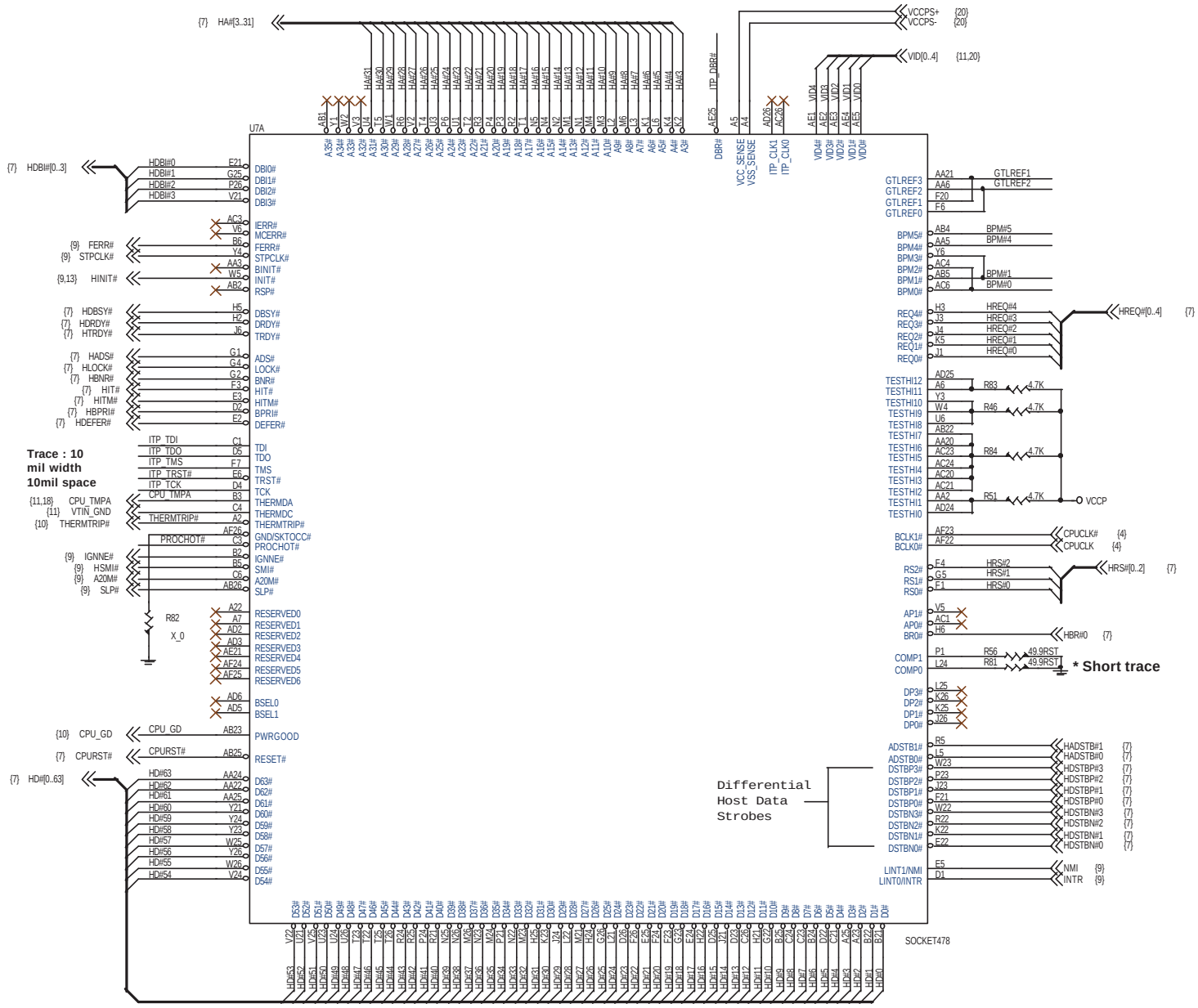
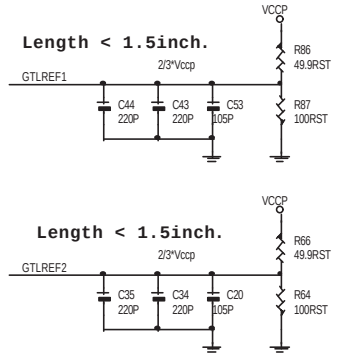
CPU SIGNAL BLOCK

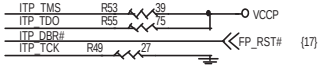


CPU GTL REFERNCE VOLTAGE BLOCK



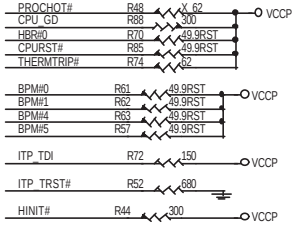
Every pin put one 220pF cap near it.
Trace Width 15mils, Space 15mils.
Keep the voltage dividers within 1.5 inches of the first GTLREF Pin

CPU ITP BLOCK



CPU STRAPPING RESISTORS

ALL COMPONENTS CLOSE TO CPU



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Title: INTEL mPGA478-B CPU1	Rev: 0A
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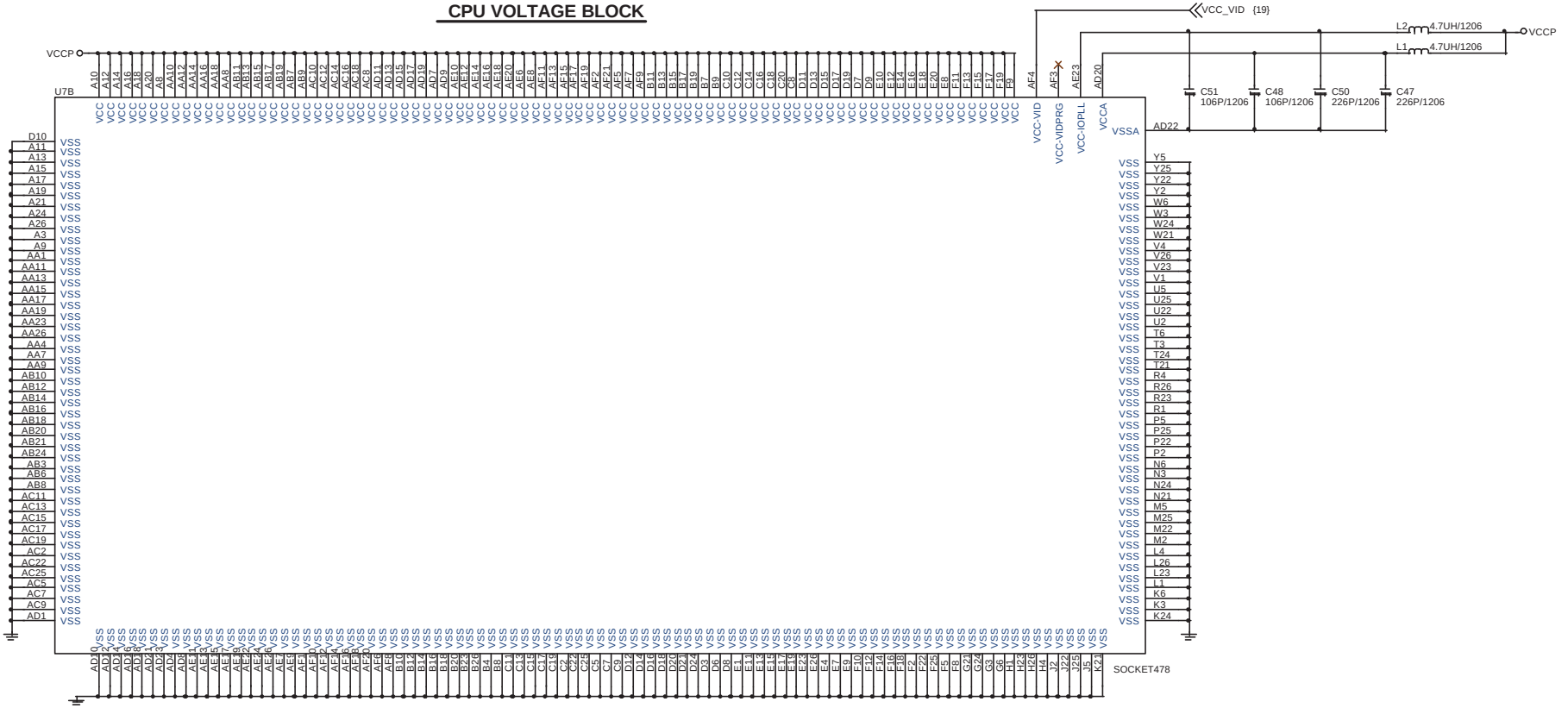
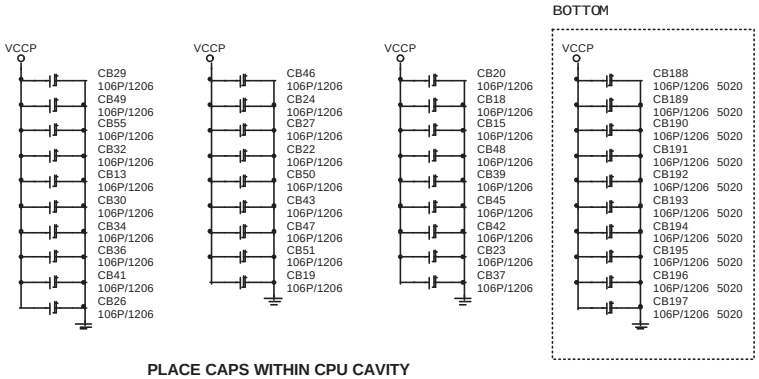
CPU VOLTAGE BLOCK



CPU DECOUPLING CAPACITORS



PLACE CAPS WITHIN CPU CAVITY

CPU DECOUPLING CAPACITORS

PLACE CAPS WITHIN CPU CAVITY SOLDER

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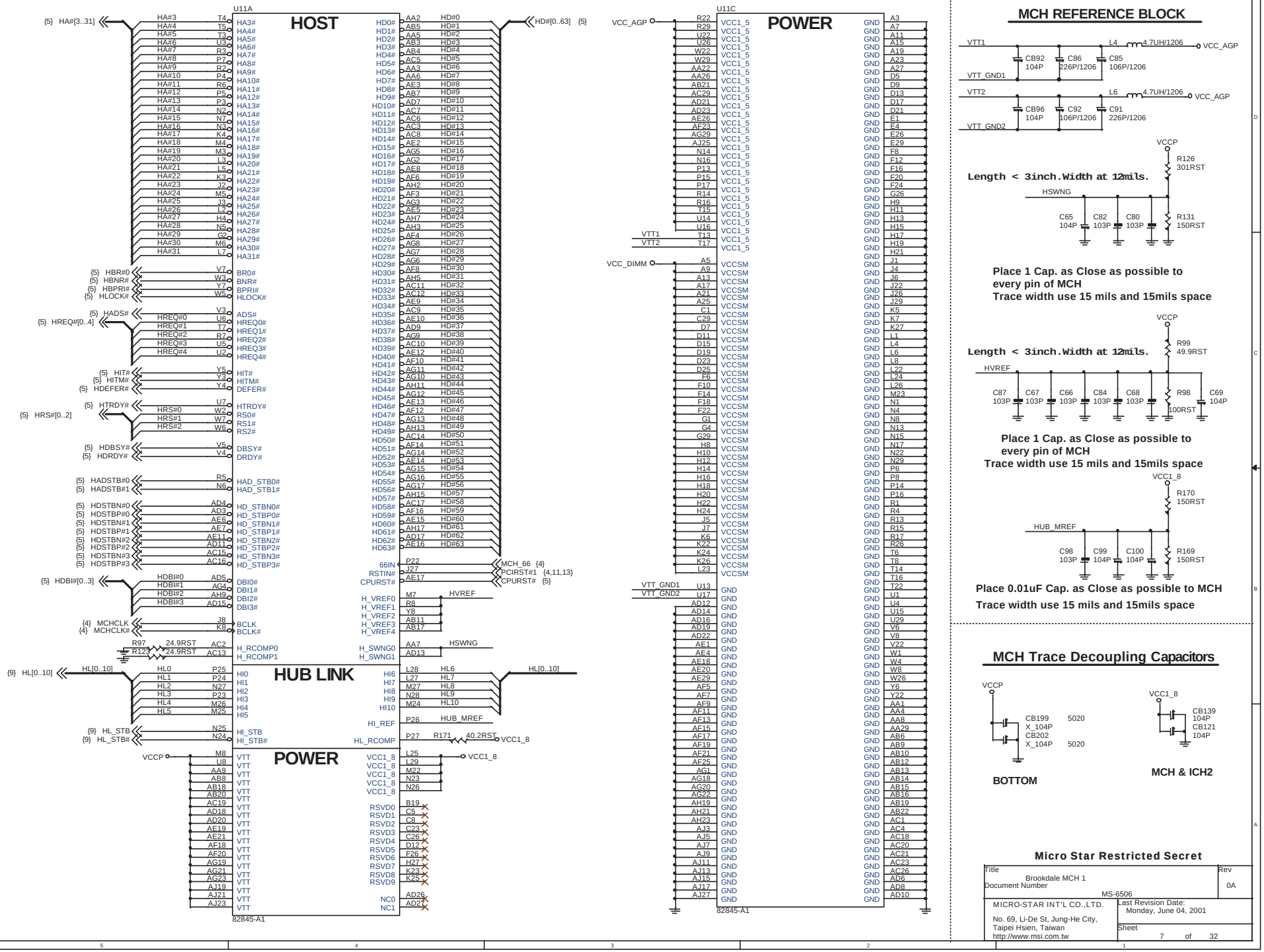

MCH REFERENCE BLOCK

Length < 3inch.Width at 12mils.

Place 1 Cap. as Close as possible to every pin of MCH
Trace width use 15 mils and 15mils space

Length < 3inch.Width at 12mils.

Place 1 Cap. as Close as possible to every pin of MCH
Trace width use 15 mils and 15mils space

Place 0.01uF Cap. as Close as possible to MCH
Trace width use 15 mils and 15mils space

MCH Trace Decoupling Capacitors

BOTTOM

MCH & ICH2

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Title: Brookdale MCH 1	Rev: 0A
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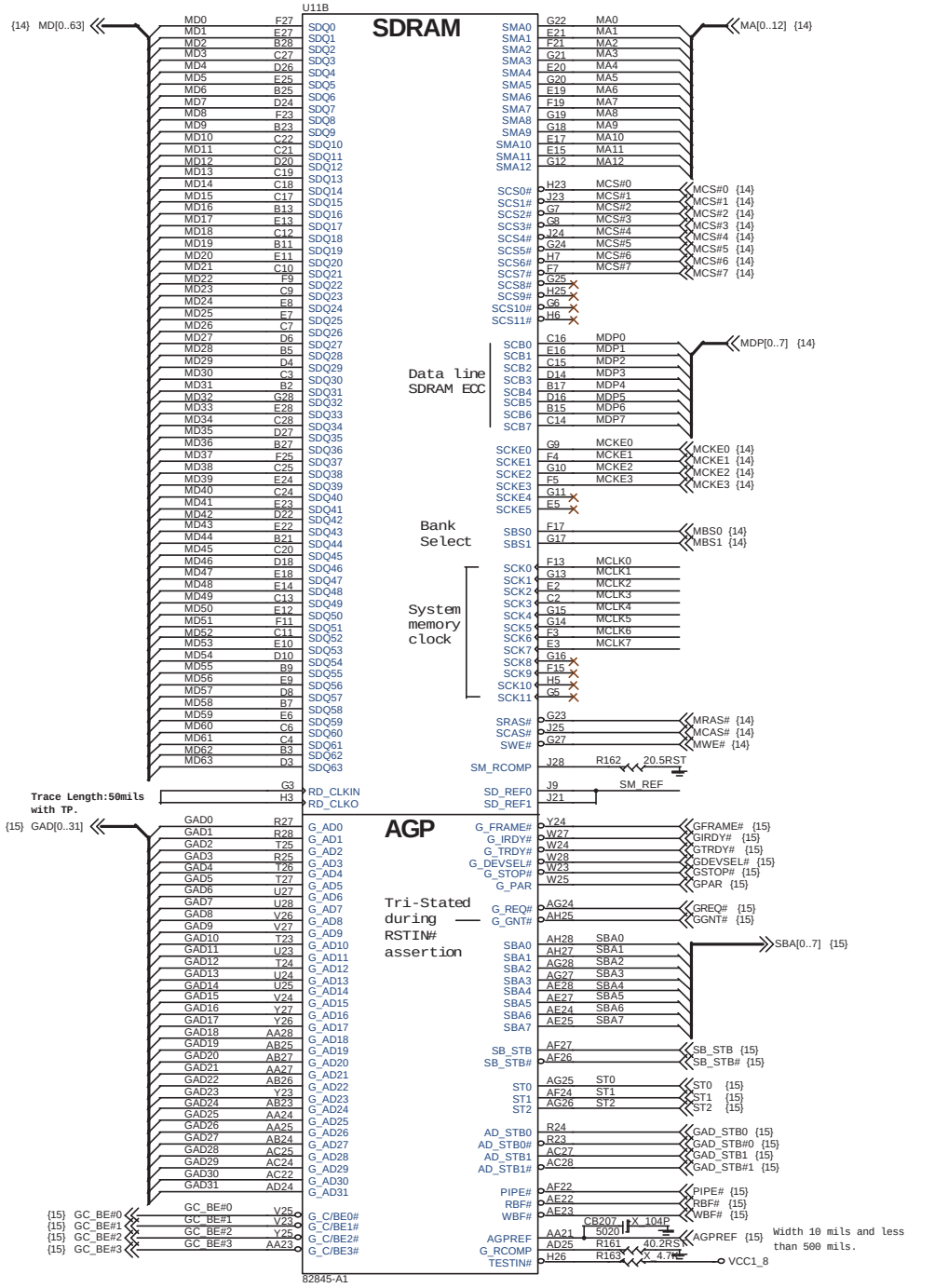
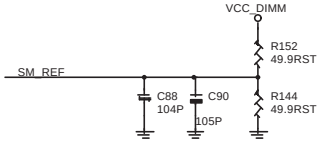
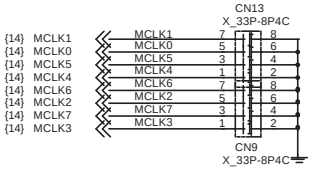


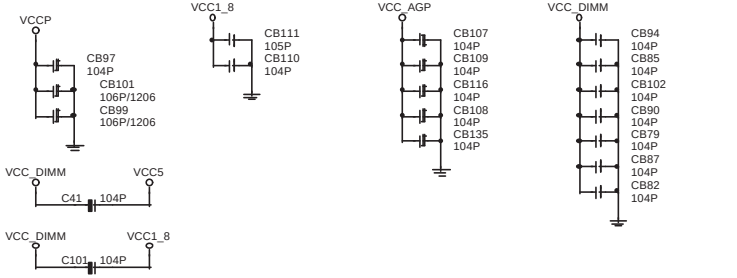
MCH REFERENCE VOLTAGE



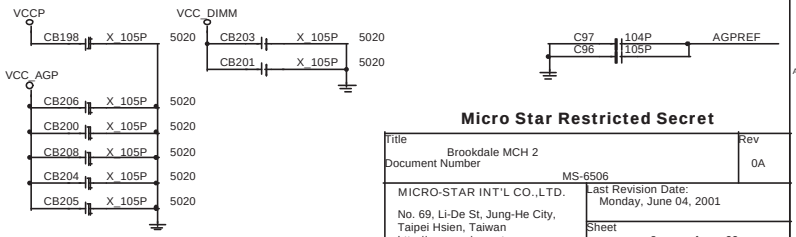
MCH MEMORY CLOCK RC CIRCUITS



MCH DECOUPLING CAPACITOR



BACK



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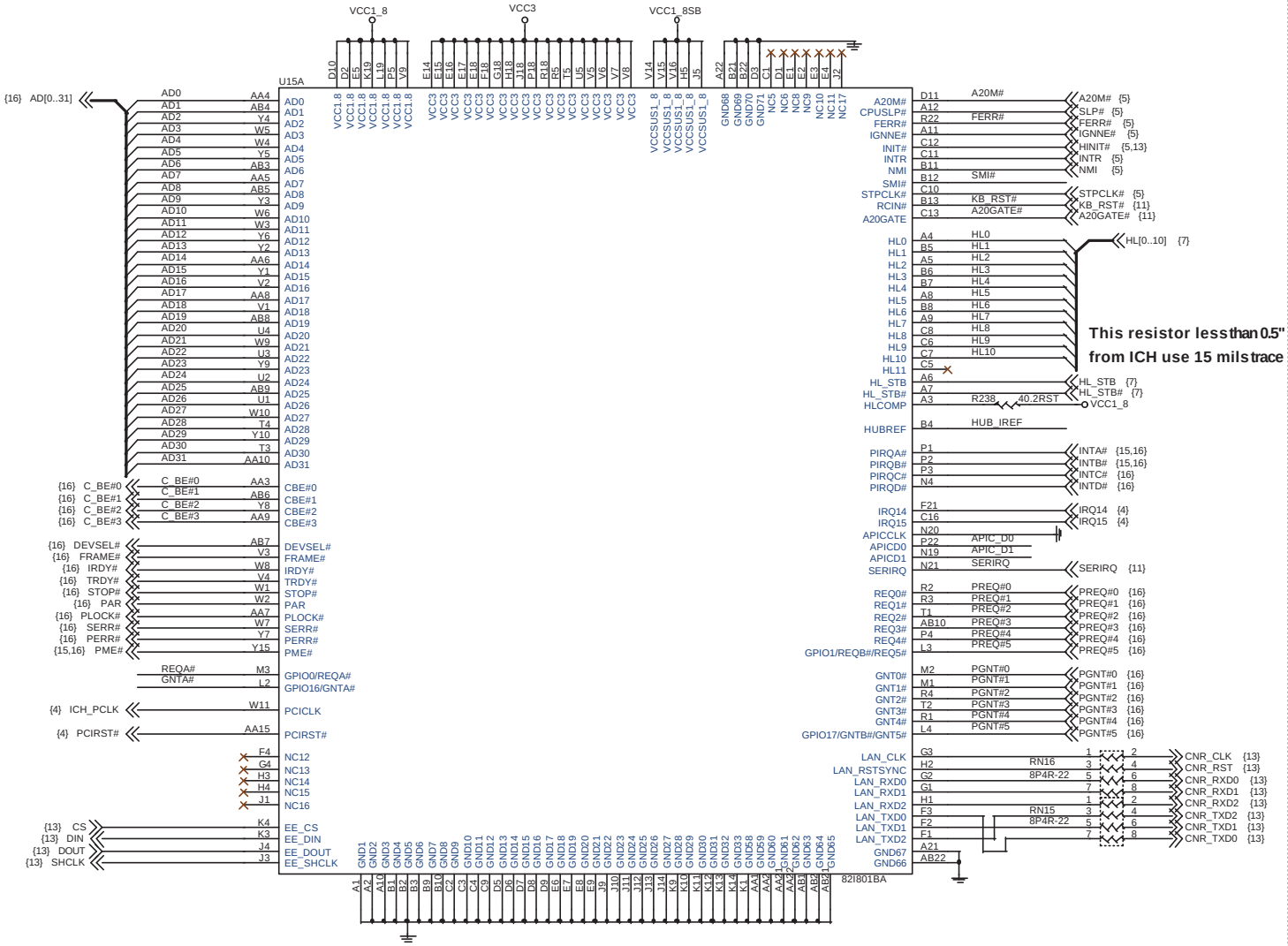
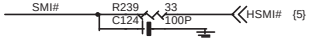
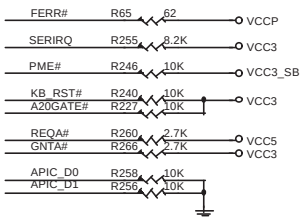
ICH2 PCI / HUB LINK / CPU / LAN / INTERRUPT SIGNALS



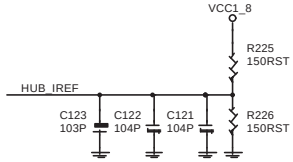
ICH2 SMI# SIGNAL



ICH2 STRAPPING RESISTORS

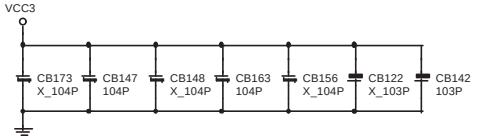


ICH2 REFERENCE VOLTAGE

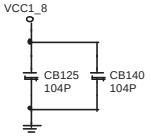


Place Cap. as Close as possible to ICH2
Trace width use 15 mils and 15mils space

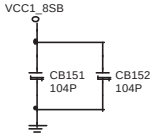
ICH2 DECOUPLING CAPACITORS



Place one 0.1U/0.01U pair in each corner and 2 on opposite sides close to ICH2 if it fit



Distribute near the 1.8V power pin of the ICH2



Distribute near the VCC1_8SB Power pin of the ICH2

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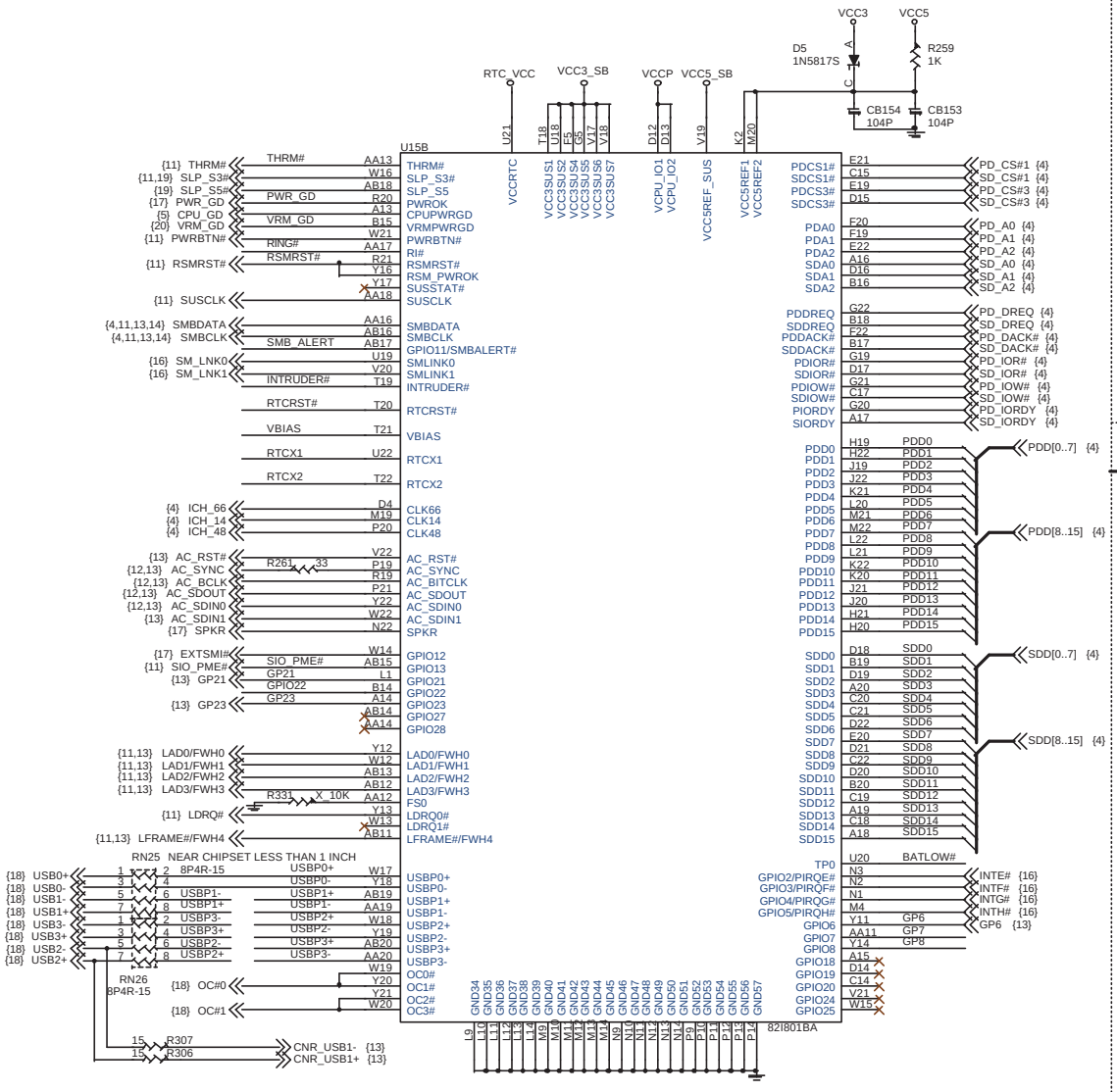
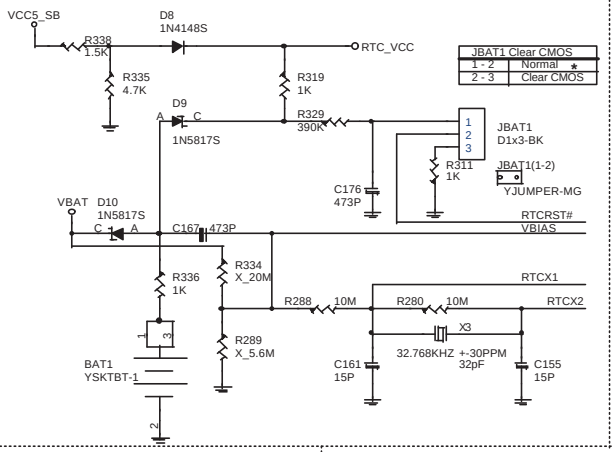
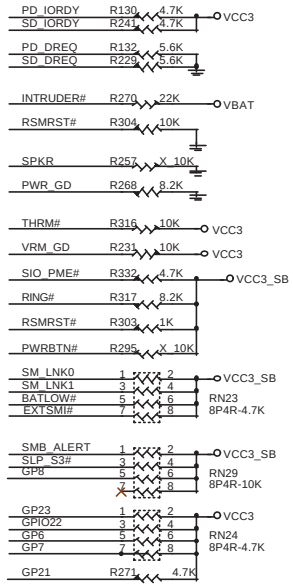
ICH2 ASIC / RTC / AC'97 / GPIO / LPC / USB / IDE SIGNALS



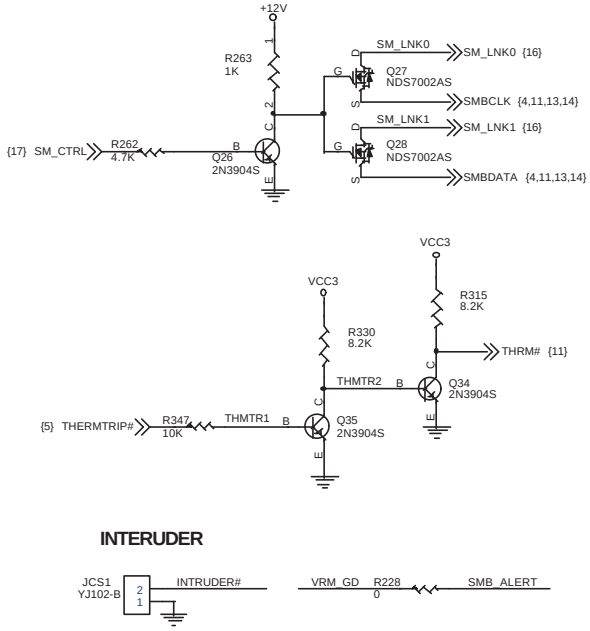
RTC BLOCK



ICH2 STRAPPING RESISTORS

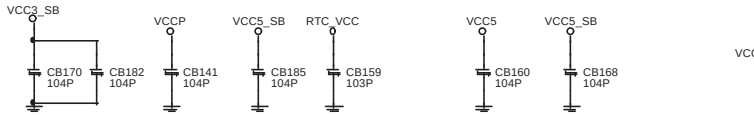


NEC-CI AOL2 Function



INTERUDER

ICH2 DECOUPLING CAPACITOR



Distribute near the VCC3_SB power pin of the ICH

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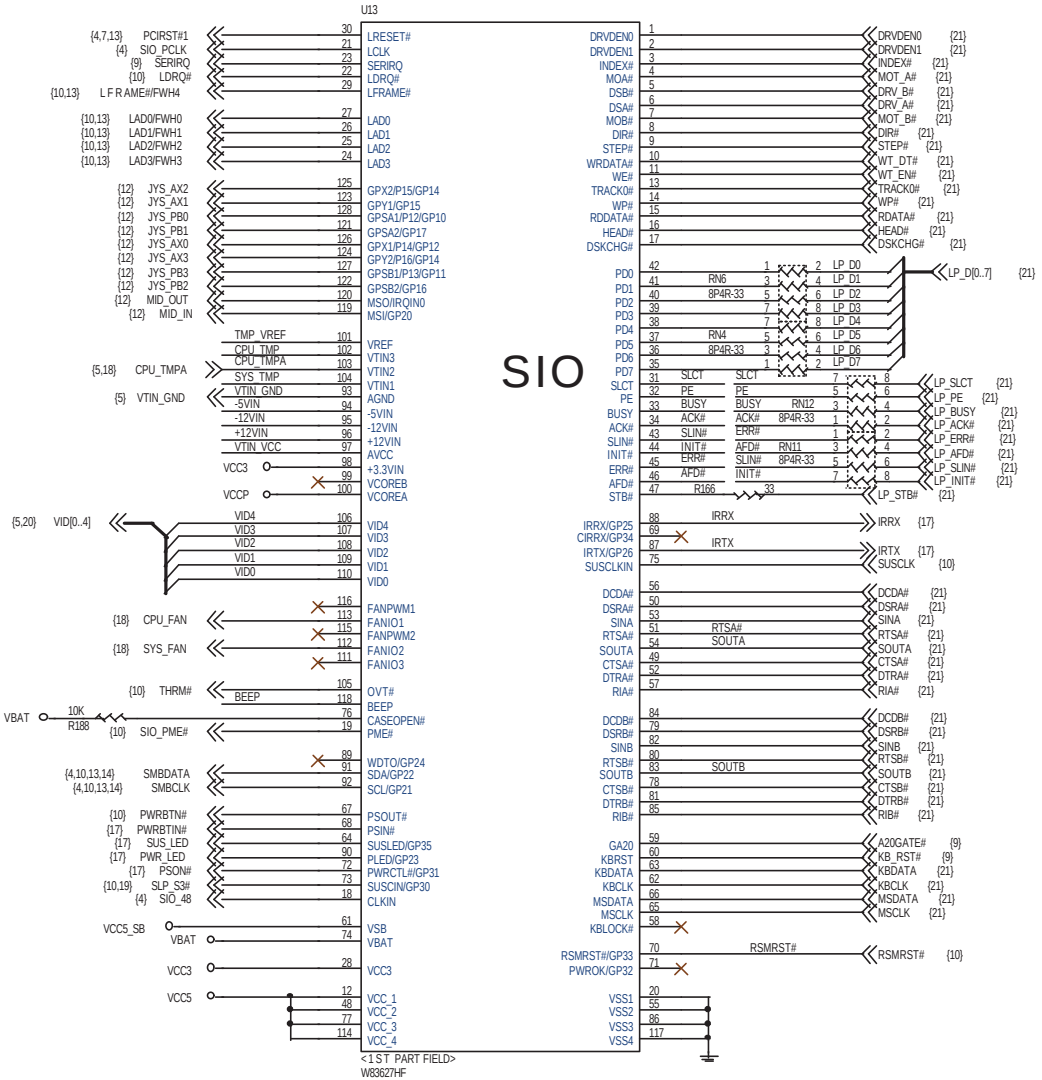
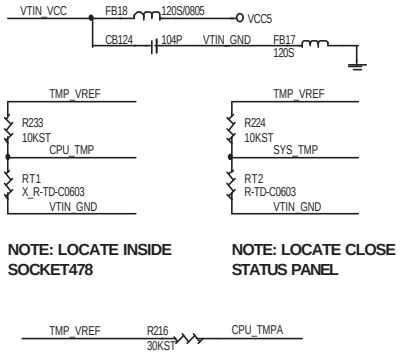
LPC SUPER I/O W83627HF



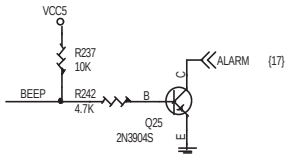
THERMAL RESISTOR BLOCK



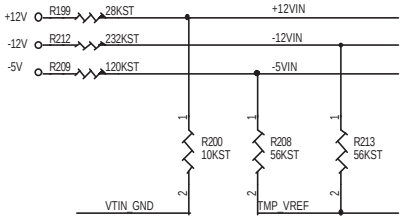
NOTE: LOCATE INSIDE SOCKET478

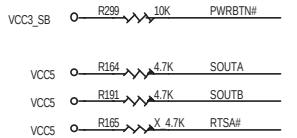
NOTE: LOCATE CLOSE STATUS PANEL

SPEAKER BLOCK



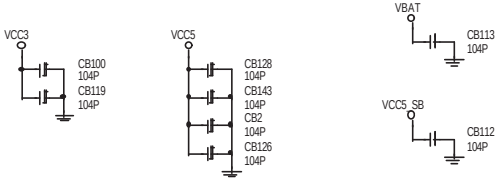
SUPER I/O STRAPPING RESISTOR





SOUTA	L: Disable KBC	H: Enable KBC
SOUTB	L: 24MHZ	H: 48MHZ
RTSA#	L: CFAD=2E	H: CFAD=4E
DTRA#	L: PNP Default	H: PNP no Default

DECOUPLING CAPACITOR



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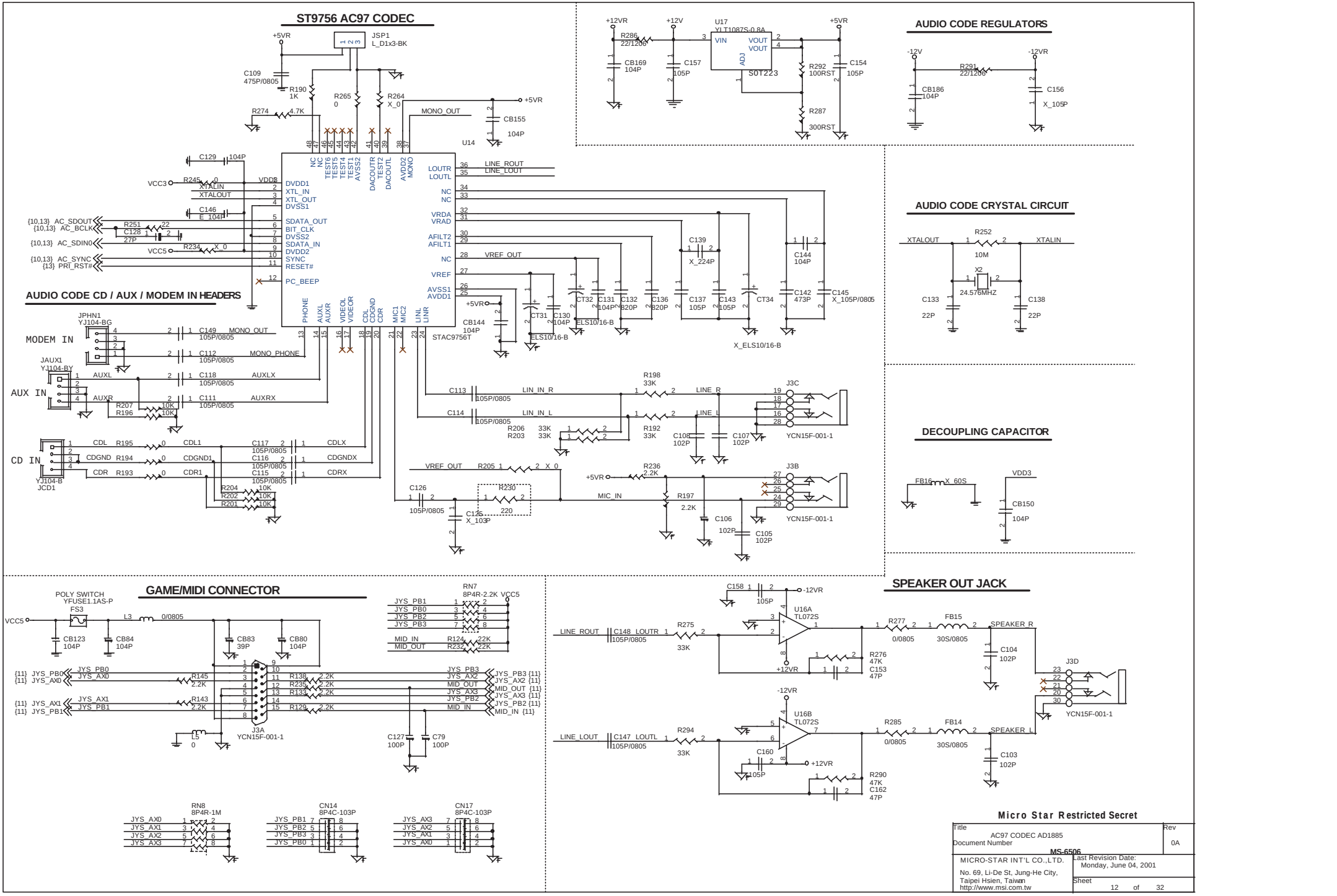
ST9756 AC97 CODEC
AUDIO CODE REGULATORS
AUDIO CODE CRYSTAL CIRCUIT
AUDIO CODE CD / AUX / MODEM IN HEADERS
DECOUPLING CAPACITOR
GAME/MIDI CONNECTOR
SPEAKER OUT JACK
U14
STAC9756T
U17
YLT1087S-0.8A
SOT223
U16A
TL072S
U16B
TL072S
JSP1
L_D1x3-BK
JPHN1
YJ104-BG
JAUX1
YJ104-BY
JCD1
YJ104-B
J3A
YCN15F-001-1
J3B
J3C
J3D
FS3
POLY SWITCH
YFUSE1.1AS-P
RN7
8P4R-2.2K
RN8
8P4R-1M
CN14
8P4C-103P
CN17
8P4C-103P
MODEM IN
AUX IN
CD IN
Micro Star Restricted Secret
AC97 CODEC AD1885
MS-6506
0A
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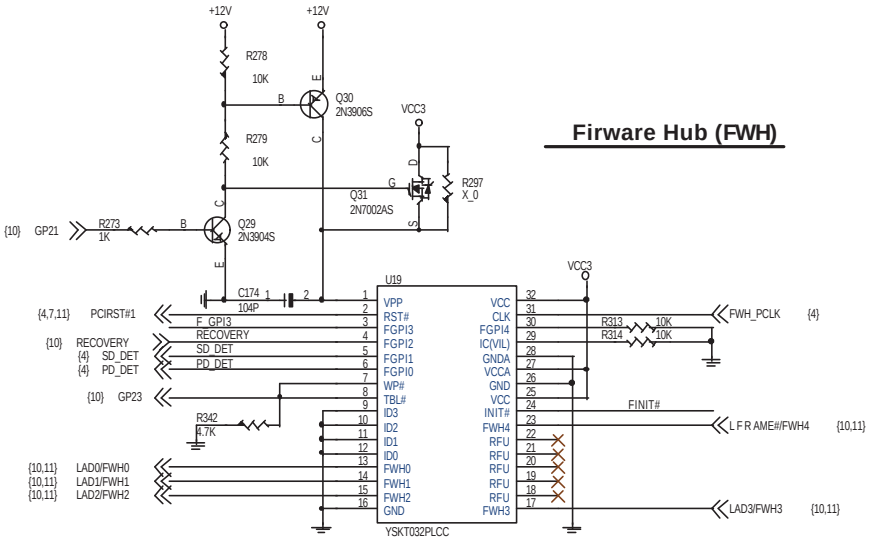
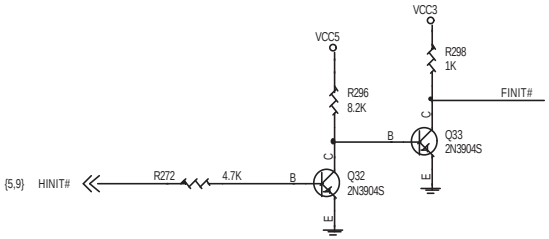
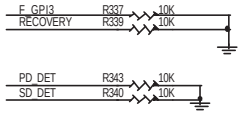
Firware Hub (FWH)



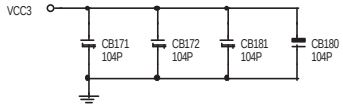
FWH INIT Signal Voltage Translation Block



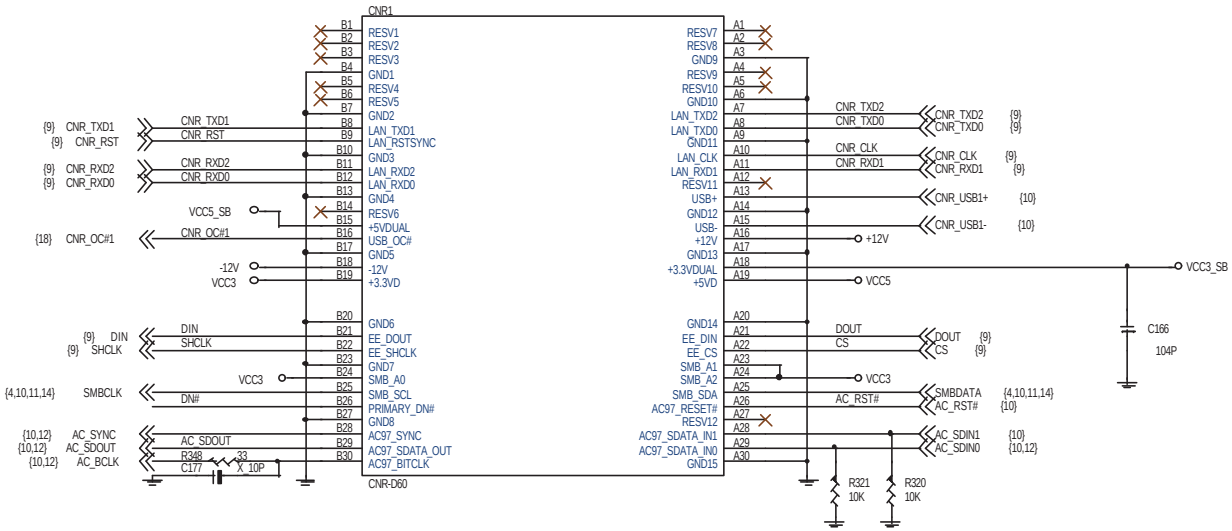
FWH RESISTORS

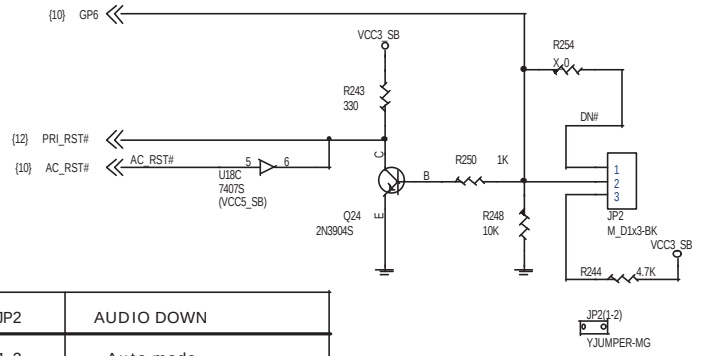


FWH DECOUPLING CAPACITORS



CNR RISER





JP2	AUDIO DOWN
1-2	Auto mode
2-3	Disabled onboard audio codec

Micro Star Restricted Secret

Title: FWH & CNR & AC'97 Control		Rev: 0A
Document Number: MS-6506		
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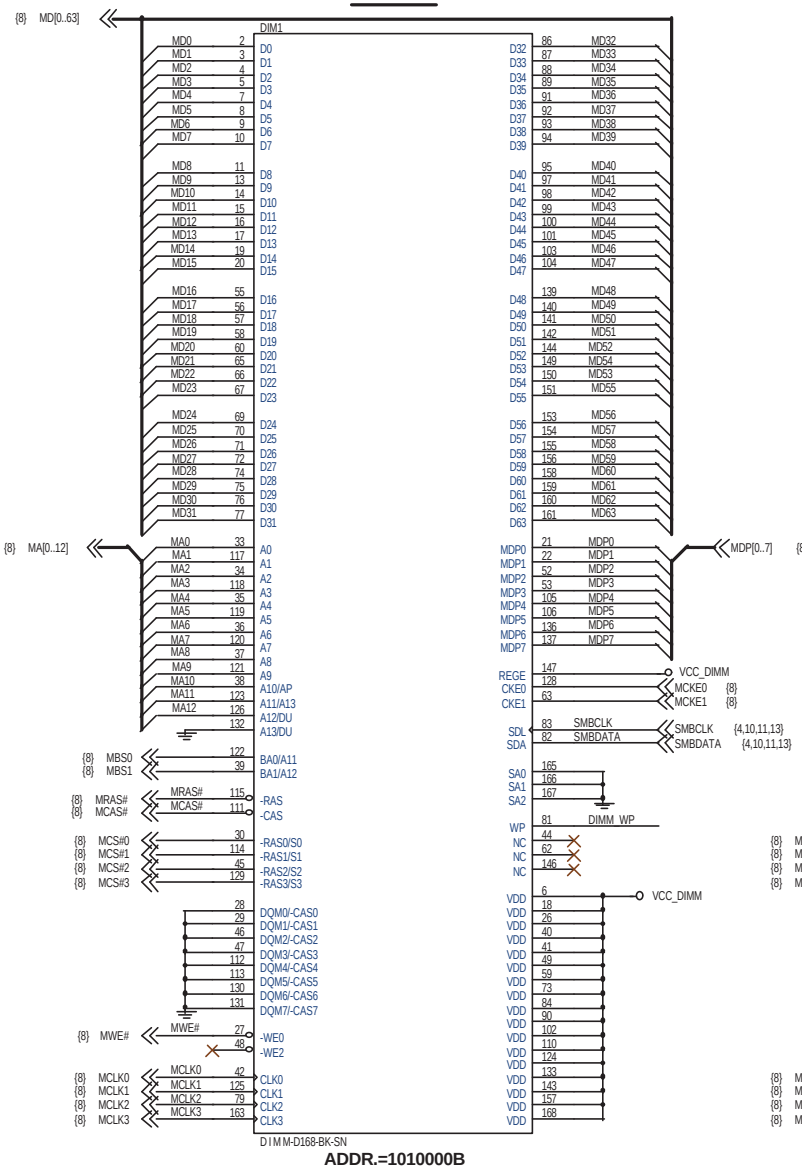
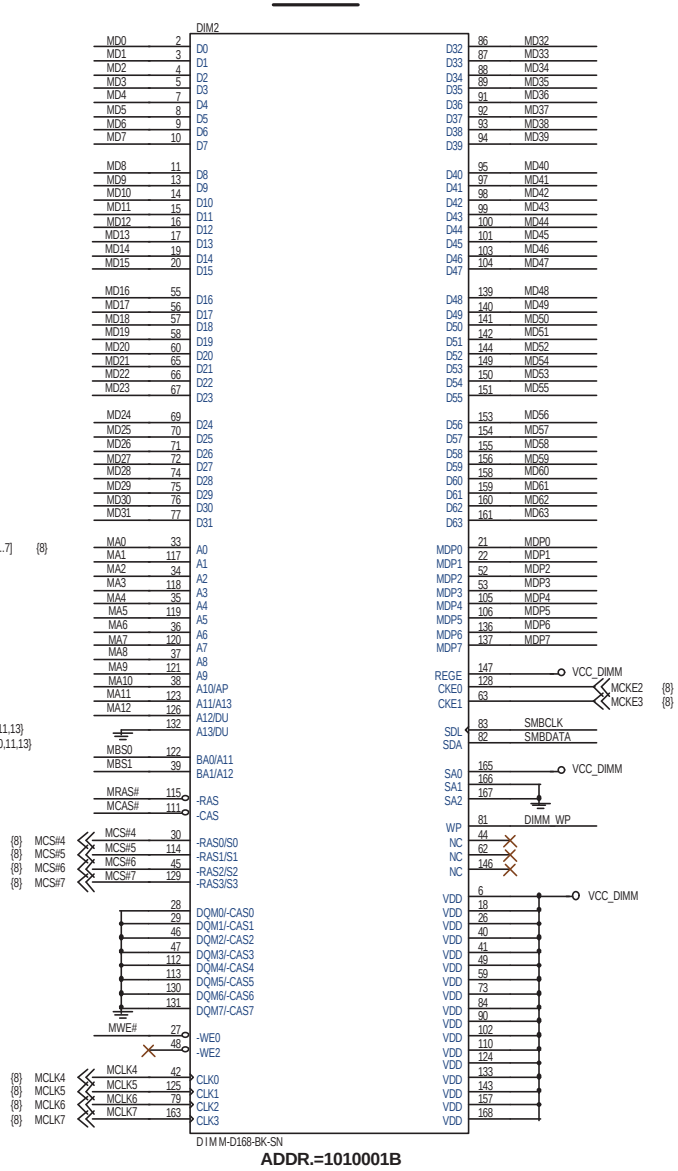
DIMM1



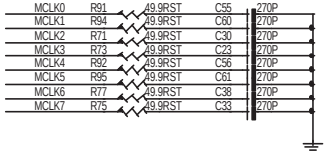
ADDR.=1010000B

DIMM2

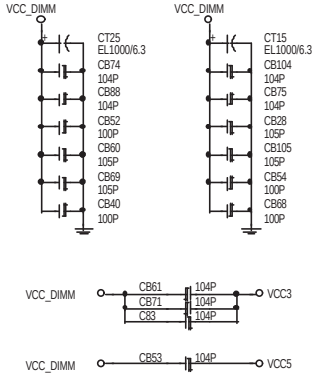


ADDR.=1010001B

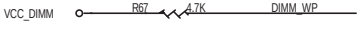
DIMM CLOCK



DECOUPLING CAPACITORS



DIMM SPD WE BLOCK



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Title: DIMM 1 & 2	Rev: 0A
Document Number: MS-6506	
MICRO-STAR INT'L CO.,LTD.	Last Revision Date: Monday, June 04, 2001
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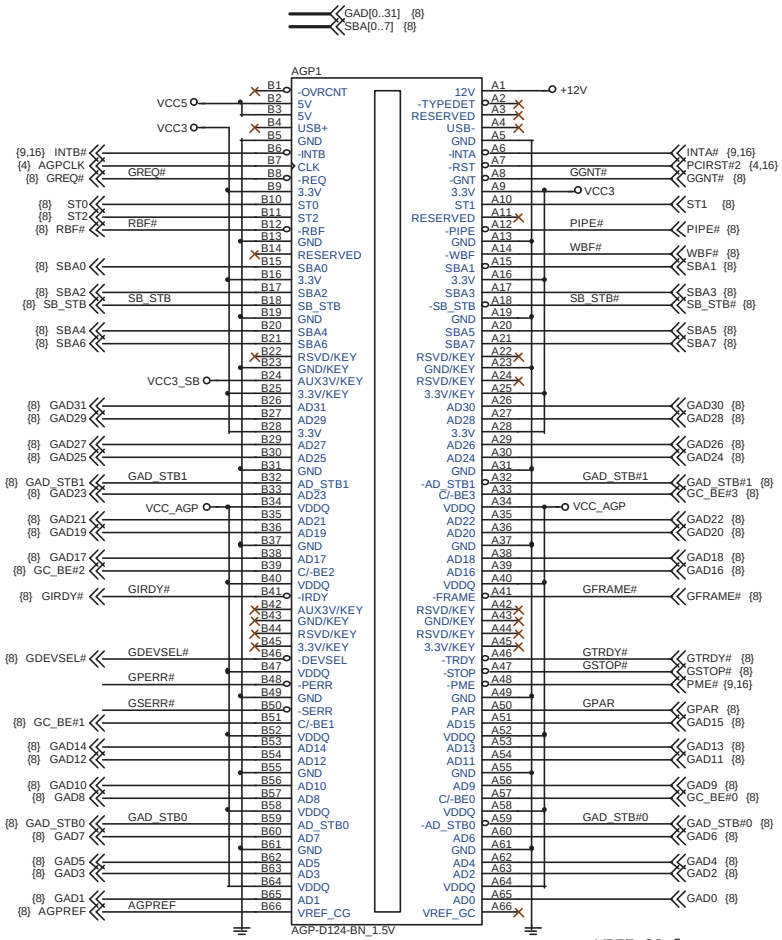
AGP UNIVERSAL 2X/4X SLOT(AGP VER:2.0 COMPLY)

VCC5 = 60mils trace / 15 mils space



VREF_GC:form the chipset to the graphics controller

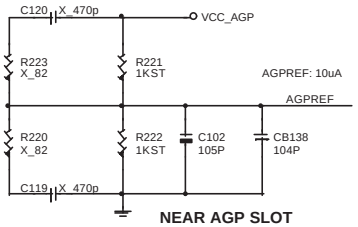
VREF_GC:form the graphics controller to the chipset

AGP Slot Imax

VCC_AGP 8.0A
VCC3 6.0A
VCC12 1.0A
VCC5 2.0A

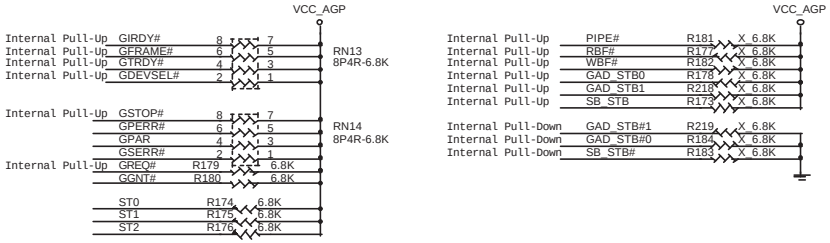
INTA#
INTB#

AGP SIGNAL REFERENCE CIRCUIT



NEAR AGP SLOT

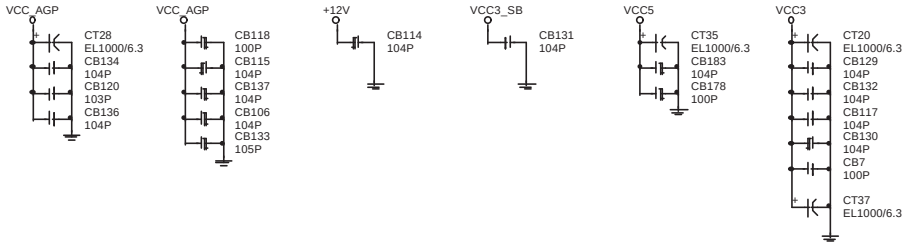
AGP TERMINATION RESISTORS



LESS 10MILS STUB TRACE LENGTH MUST BE FOLLOWING.

Place these resistors between PCI and AGP slot

AGP SLOT DECOUPLING CAPACITORS



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Title: AGP SLOT	Rev: 0A
Document Number: MS-6506	
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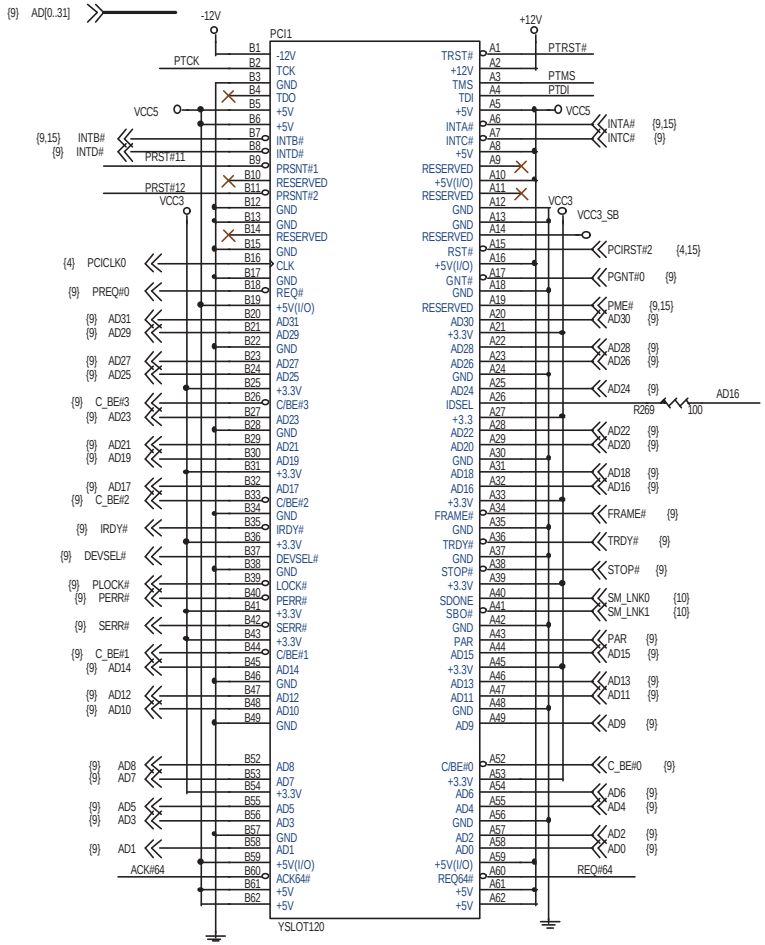
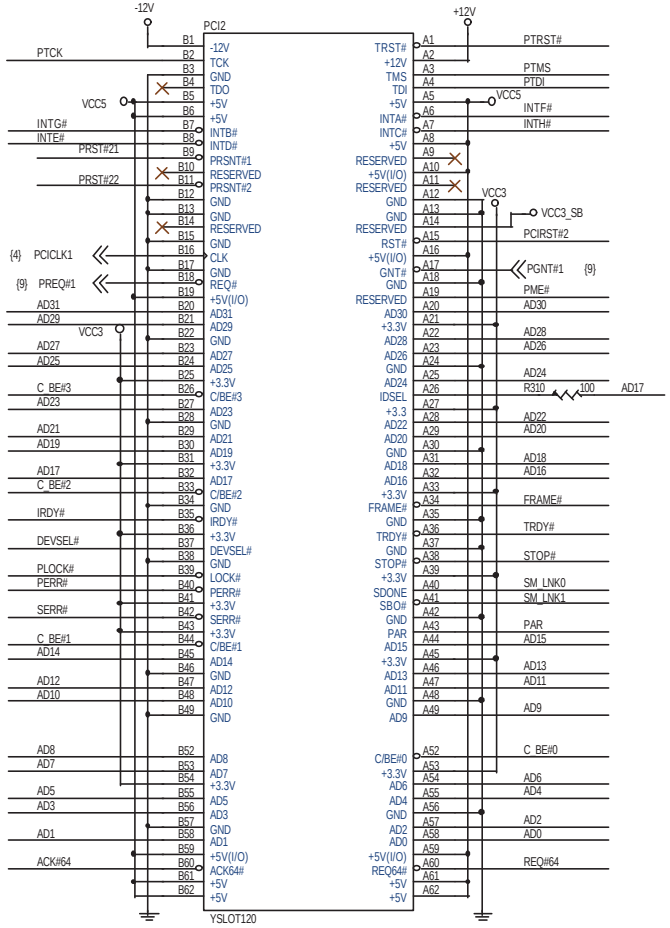
PCI SLOT 1 (PCI VER: 2.2 COMPLY)



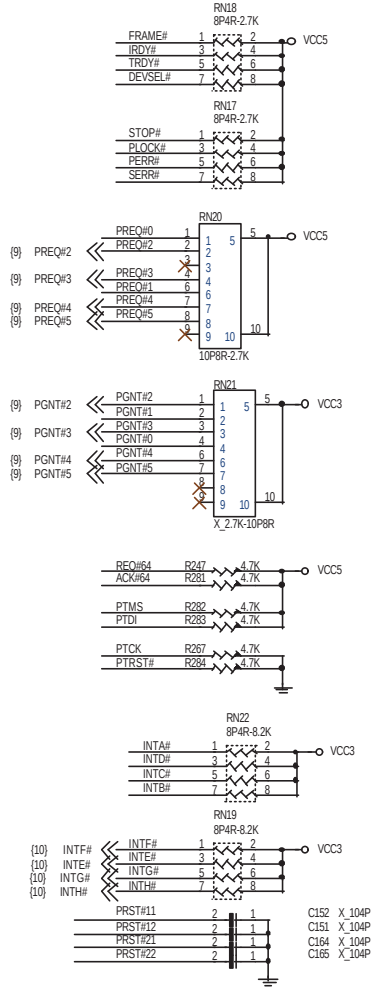
IDSEL = AD16
MASTER = PREQ0
INTA#

PCI SLOT 2 (PCI VER: 2.2 COMPLY)

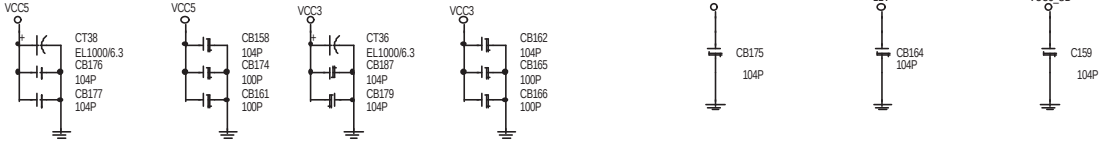


IDSEL = AD17
MASTER = PREQ1
INTE#

PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS



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Title: PCI Slot 1 & 2 & 3	Rev: 0A
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MICRO-STAR INT'L CO.,LTD.	Last Revision Date: Monday, June 04, 2001
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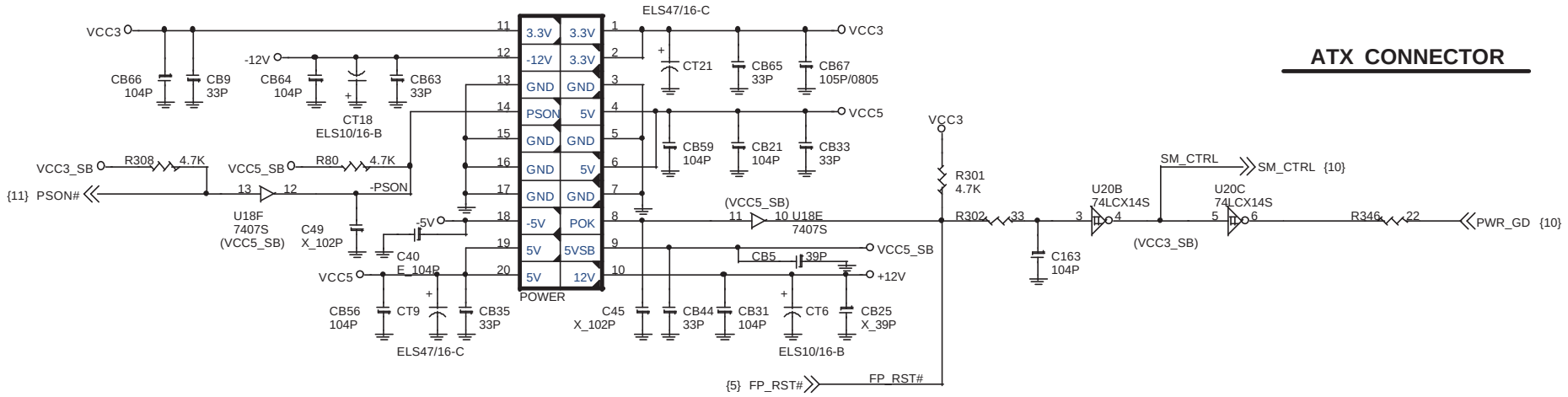
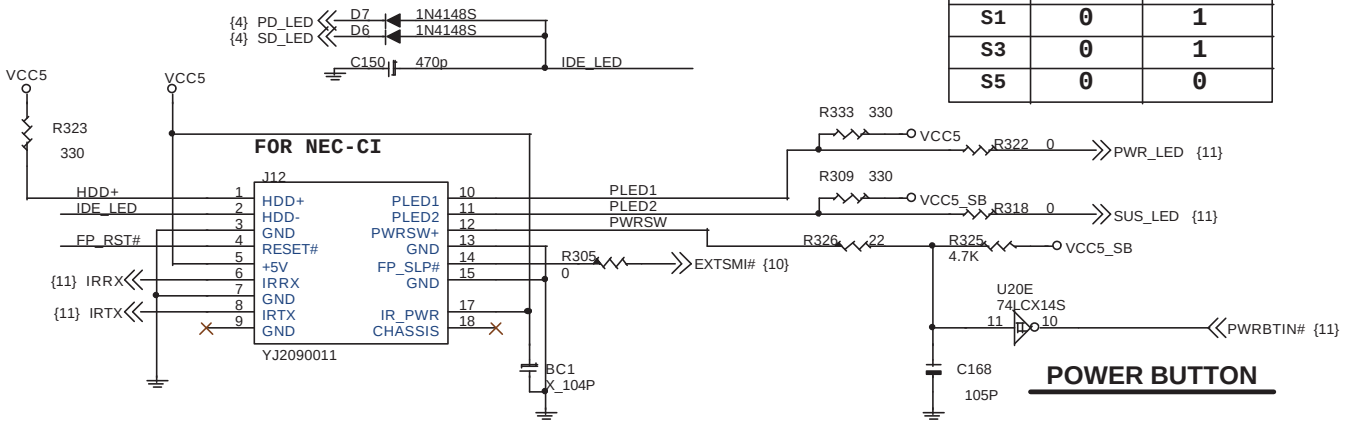


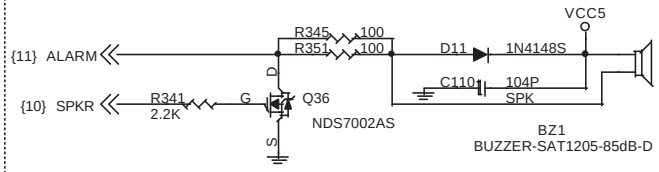
Brookdale FRONT PANEL-M



	PLED	SUSLED
S0	1	0
S1	0	1
S3	0	1
S5	0	0

POWER BUTTON

SPEAKER



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Title: Front Panel & Connector	Rev: 0A
Document Number: MS-6506	
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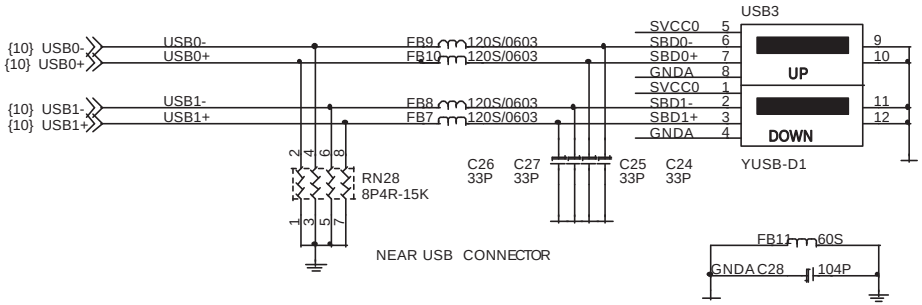
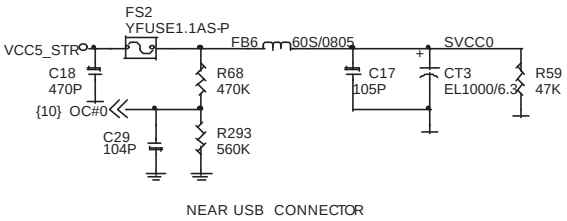
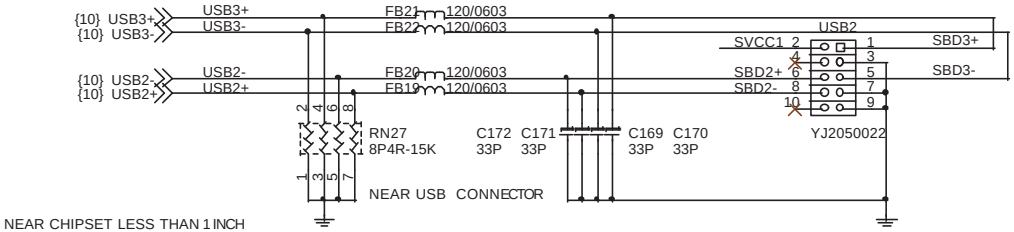
BACK PANEL USB CONNECTOR FOR USB PORT 0,1



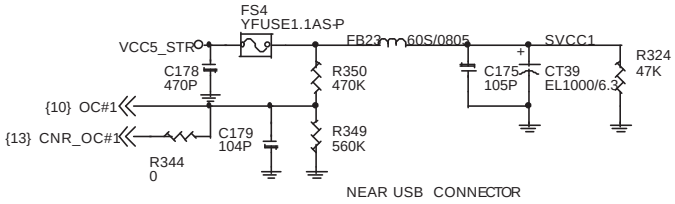
POWER CIRCUIT FOR USB PORT 0,1



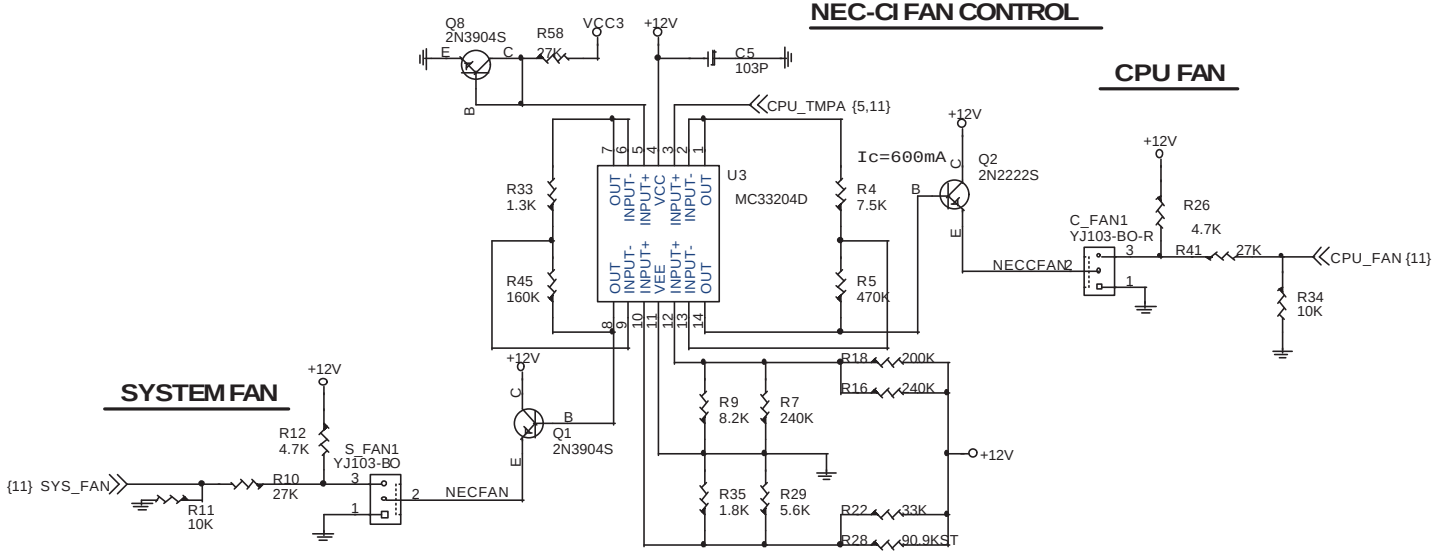
FRONT PANEL USB CONNECTOR FOR USB PORT 2,3



POWER CIRCUIT FOR USB PORT 2, 3



NEC-CI FAN CONTROL



Micro Star Restricted Secret

Title: USB & FAN Connectors	Rev: 0A
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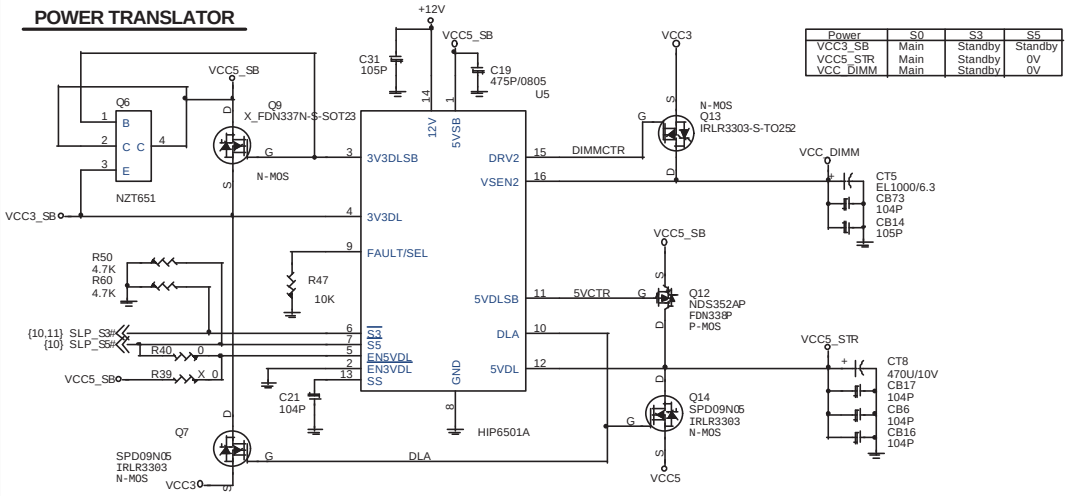
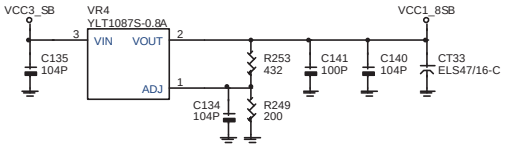
POWER TRANSLATOR



Power	S0	S3	S5
VCC3_SB	Main	Standby	Standby
VCC5_STR	Main	Standby	0V
VCC_DIMM	Main	Standby	0V

1.8V STANDBY POWER TRANSLATOR

(40mils trace / 20 mils space)



NOTE1 --- MCH
VCC_AGP = VCC1_5 (1.5A) + VCC_AGP (0.37A)

NOTE2 --- DIMM
S0 STATE --- 2.0A * 3 = 6.0A ---> VCC3
S1/S3 STATE --- 200mA * 3 = 600mA ---> VCC3_SB
VCC3_SB --> 600mA*3.3V/5V=396mA -->VCC5_SB

NOTE3 --- ICH2

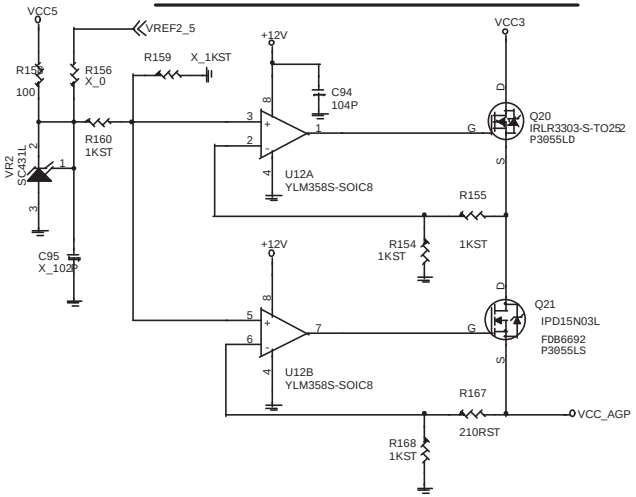
Power	S0	S1	S3/S4/S5
1.8V	300mA	100mA	N/A
1.8V_LAN	36mA	28mA	N/A
VCC1_8SB	45mA	30mA	7mA
VCC3	410mA	5mA	N/A
VCC3+562ET	230mA	210mA	N/A
VCC3_SB	25mA	0.6mA	N/A

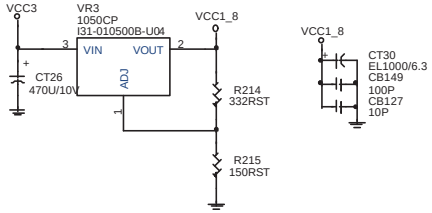
VCC3_SB =
VCC1_8SB=
VCC5_SB = VCC3_SB + VCC1_8SB

POWER CONSUMPTION

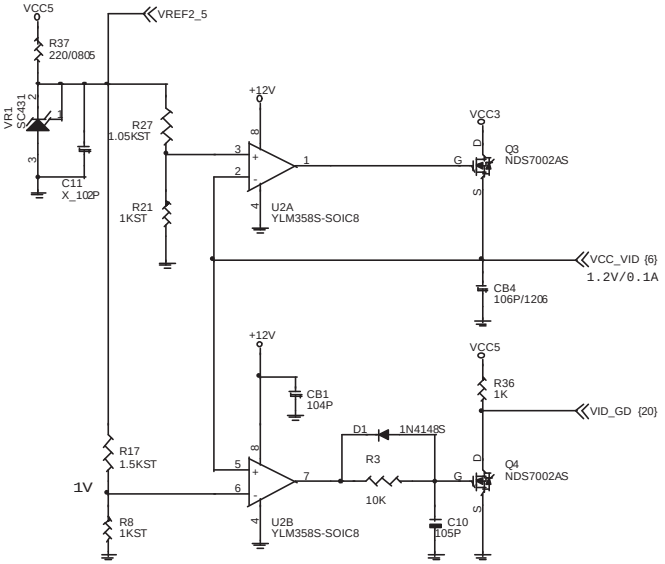
	VCCP	VCC_AGP	VCC1_8	VCC3_DIMM	VCC3	VCC5	VCC5_SB	+12V	-12V
CPU	69.0A	0	0	0	0	0	0	NOTE4	0
PMCH	2.4A	NOTE1	0.2A	2.0A	0	0	0	0	0
ICH2	0	0	NOTE3	0	NOTE3	0	NOTE3	0	0
CY28324	0	0	0	0	0	0	0	0	0
AD1885	0	0	0	0	0		0	0	0
FWH -SST	0	0	0	0			0		
W83627HF	0	0	0	0	0		0	0	0
HIP6301		0	0	0	0		0	0	0
HIP6602A		0	0	0			0	0	0
HIP6601A	0	0	0	0	0	0	0	0	0
SC1547	0	0	0	0	0	0			0
DIMM	0	0	0	NOTE2	0		NOTE2	0	0
AGP	0	8.0A	0	0	6.0A	2.0A	?	1.0A	0
PCI	0	0	0	0		0	0	0	0
USB	0		0	0		0			0
USB HUB	0	0	0	0	0	0	0	0	0
FAN	0	0	0	0	0	0	0	0	0
TTL	0	0	0	0	0	0	0	0	0
AMPLIFIER	0	0	0	0			0	0	0
OTHER	0	0	0	0	0		0		

AGP 4X 1.5V POWER TRANSLATOR

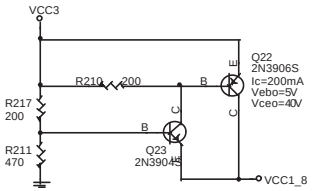




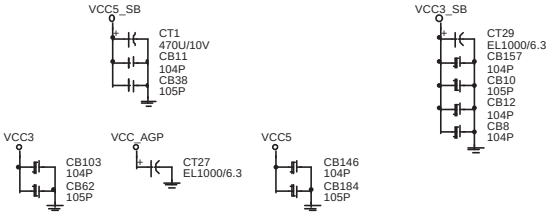
VCC_VID / VID_GOOD



1.8V/3.3V SEQUENCE CIRCUIT



REGULATORS OUTPUT DECOUPLING CAPACITORS



Micro Star Restricted Secret

Title: Voltage Regulator	Rev: 0A
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MICRO-STAR INT'L CO.,LTD.	Last Revision Date: Monday, June 04, 2001
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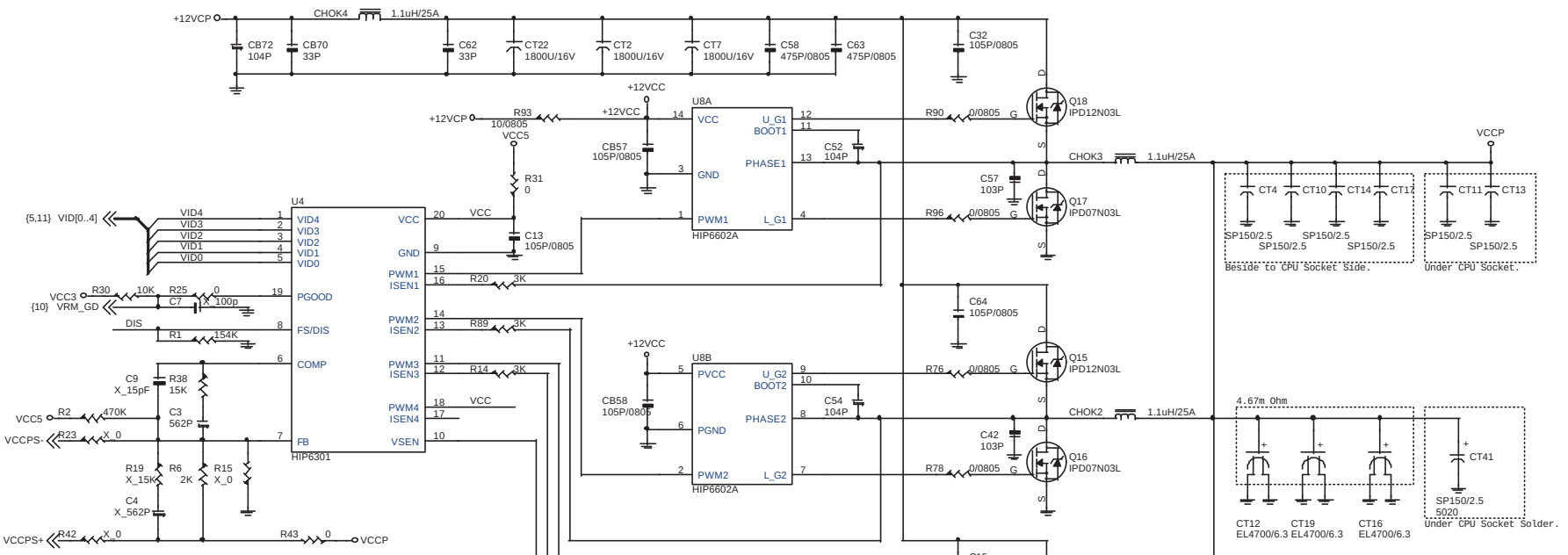
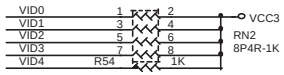


VID4	VID3	VID2	VID1	VID0	VDC(V)
1	1	1	1	0	1.100
1	1	1	0	1	1.125
1	1	1	0	0	1.150
1	1	0	1	1	1.175
1	1	0	1	0	1.200
1	1	0	0	1	1.225
1	1	0	0	0	1.250
1	0	1	1	1	1.275
1	0	1	1	0	1.300
1	0	1	0	1	1.325
1	0	1	0	0	1.350
1	0	0	1	1	1.375
1	0	0	1	0	1.400
1	0	0	0	1	1.425
1	0	0	0	0	1.450
0	1	1	1	1	1.475

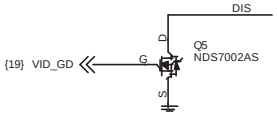
VID4	VID3	VID2	VID1	VID0	VDC(V)
0	1	1	1	0	1.500
0	1	1	0	1	1.525
0	1	1	0	0	1.550
0	1	0	1	1	1.575
0	1	0	1	0	1.600
0	1	0	0	1	1.625
0	1	0	0	0	1.650
0	0	1	1	1	1.675
0	0	1	1	0	1.700
0	0	1	0	1	1.725
0	0	1	0	0	1.750
0	0	0	1	1	1.775
0	0	0	1	0	1.800
0	0	0	0	1	1.825
0	0	0	0	0	1.850
1	1	1	1	1	OFF

VID PULL-UP RESISTORS

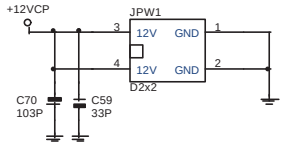
HIP6301V DON'T NEED PULL HIGH
HIP6301 NEED PULL HIGH



PWM GOOD



ATX12V POWER CONNECTOR



Micro Star Restricted Secret

Title: VRM 9.0	Rev: 0A
Document Number: MS-6506	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Monday, June 04, 2001
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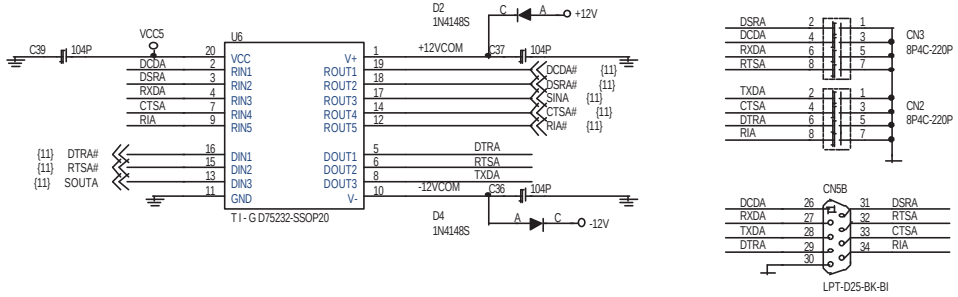
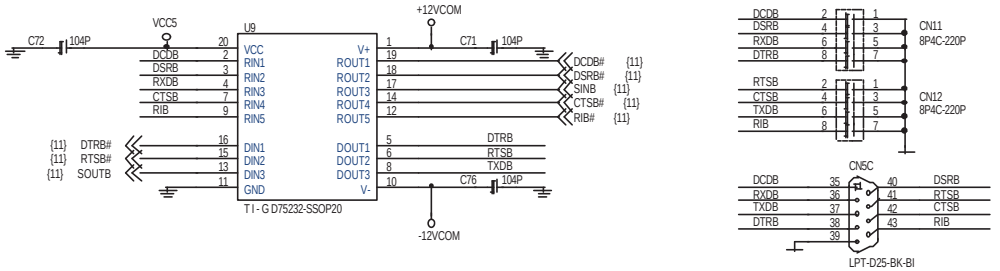
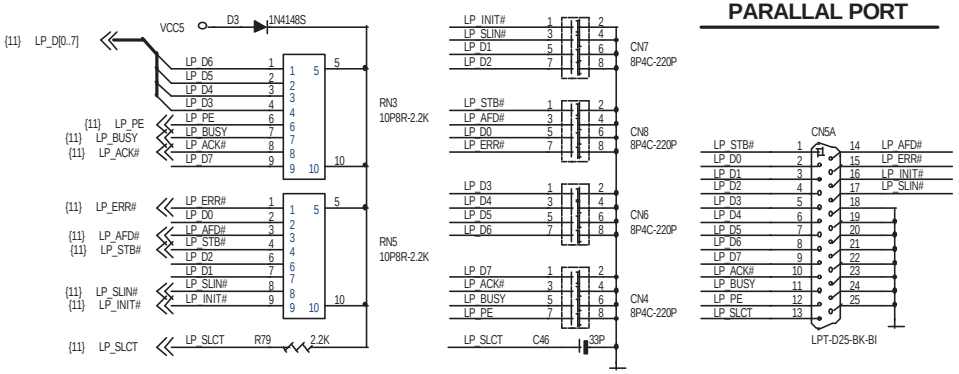
SERIAL PORT 1



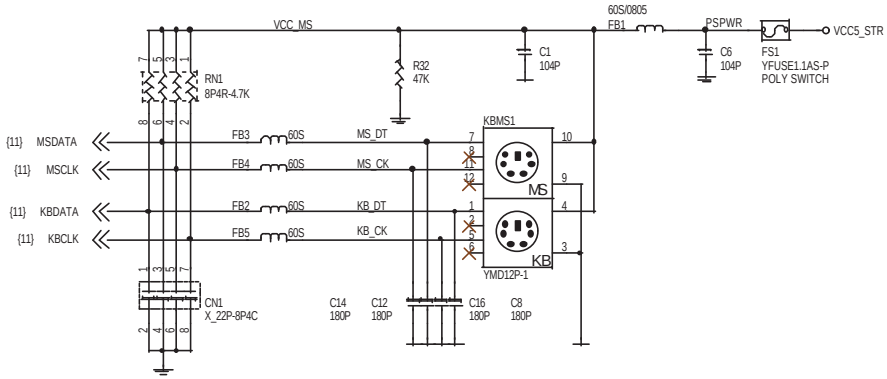
SERIAL PORT 2



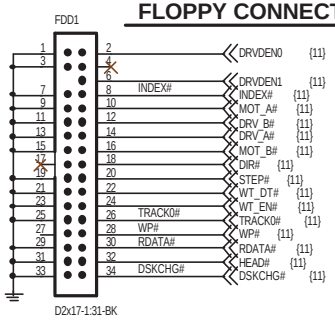
PARALLAL PORT



PS2 KEYBOARD & MOUSE CONNECTOR



FLOPPY CONNECTOR



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Title: IO Connector	Rev: 0A
Document Number: MS-6506	
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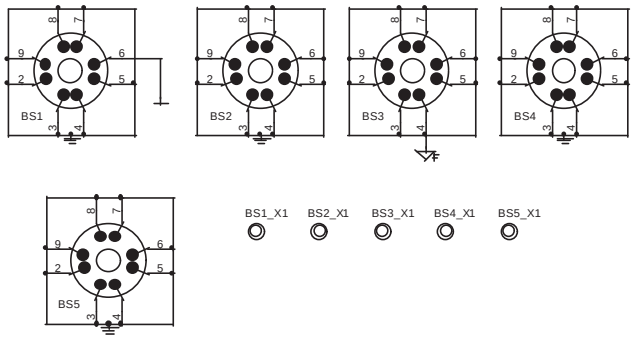
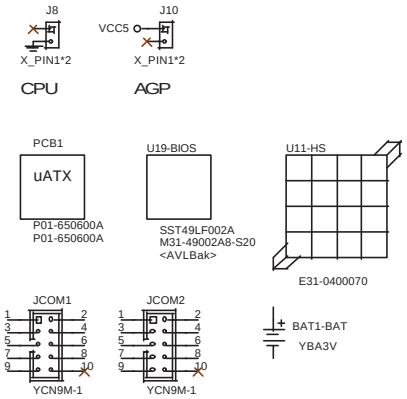
PCB OTHER COMPONENT



BS1_X1 BS2_X1 BS3_X1 BS4_X1 BS5_X1

SIMULATION TRACE



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Jumper Setting & Connector Setting

Jumper	Description
J3	AUDIO REAR PHONE JACK (LINE_IN, LINE_OUT, MIC_IN)

JP3	BIOS function	
1-2	Normal	(Default)
2-3	Configuration Mode	
REMOVED	Recovery	

JBAT1	CLEAR CMOS	
1-2	NORMAL	(Default)
2-3	CLEAR CMOS	

JAUX1	AUDIO AUX HEADER
JCD1	CDROM HEADER (ATAPI)
JPHN1	TELEPHONY HEADER (ATAPI)

JP1	CNR RISER CODEC SELECT HEADER	
1-2	ENABLE ONBOARD AC'97	(Default)
2-3	DISBALE ONBARD AC'97	

Connector	Description
U3	INTEL mPGA478-B CPU
IDE1	Primary
IDE2	Secondary
DIM1	SDRAM DIMM1
DIM2	SDRAM DIMM2
AGP1	AGP Slot
PCI1	PCI Slot1
PCI2	PCI Slot2
COM1	Serial Port
COM2	Serial Port
LPT	Parallel Port
FDD1	Floopy
JCS1	Chassis Instruction
KBMS1	PS/2 Keyboard and PS/2 mouse
C_FAN1	CPU FAN HEADER
S_FAN	System FAN HEADER
USB1	USB REAR CONNECTOR
USB2	USB INTERNAL HEADER
POWER	ATX Power
F_P1	Front Panel
Pin1	Power of Hard LED
Pin2	Power LED
Pin3	Hard LED
Pin4	Suspend LED
Pin5,8,12,13	GND
Pin6	Power Button
Pin7	Reset Button
Pin9	VCC
P_FAN1	ATX FAN HEADER
JPW1	ATX12V Power
JSP1	SPDIF Connector

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Pentium 4 Processor /Northwood mPGA 478

Source Synchronous Signal Group and the Associated Strobes

Signals	Associated Strobe
REQ[4:0],A[16:3]#	ADSTB0#
A[31:17]#	ADSTB1#
D[15:0]#,DBI0#	DSTBP0#,DSTBN0#
D[31:16]#,DBI1#	DSTBP1#,DSTBN1#
D[47:32]#,DBI2#	DSTBP2#,DSTBN2#
D[63:48]#,DBI3#	DSTBP3#,DSTBN3#

Signals	Length	Inaccuracy
Data	**2.0" to 10.0"**	+/- 100 mil
Address	**2.0" to 10.0"**	+/- 200 mil
Strobe	**2.0" to 10.0"**	+/- 25 mil
Clock	**2.0" to 10.0"**	Don't need

* Delta=(CPU_pkglen.net-CPUpkglen.strobe)+(CS_pkglen.net-CS_pkglen.strobe)
Trace : 7 mil width 13mil space

Miscellaneous Signals

HL_STB/HL_STB#

Taces 5mils

20mils — HL[0:10]

HL_STB

15mils — HL_STB#

20mils — HL[0:10]

* Max Length : 8"
* STB and STB# Length must be equal

HL[10..0]

20mils — Others

HL[0:10]

15mils — HL[0:10]

20mils — Others

* Max Length : 8"
* Length must be matched within +/- 0." of the Strobe Signals

USB

*** USB Trace width : 9 mils**

*** USB Trace Spacing : 25 mils**

*** Differential USB Signlas Trace Spacing : 18 mils**

*** USB Power Trace must be 40mils width**

AGP

1X Timing group	2X/4X Timing group
AGPCLK PIPE# RBF# WBF# ST[2..0] GFRAME# GIRDY# GTRDY# GSTOP# GDEVSEL# GREQ# GGNT# GPAR	SET#1 GAD[15..0] GC_BE#[1.0] GAD_STB0 GAD_STB0# SET#2 GAD[31..16] GC_BE#[3.2] GAD_STB1 GAD_STB1# SET#3 SBA[7..0] SB_STB SB_STB#

SIGNALS	Maximum Length	Width	Space	Dismatch Length	Relative to
1X Timing group	7.5"	5 mil	5 mil	X	X
2X/4X Timing group SET#1	7.25"	5 mil	20 mil	+/- 0.125"	GAD_STB0 GAD_STB0#
2X/4X Timing group SET#2	7.25"	5 mil	20 mil	+/- 0.125"	GAD_STB1 GAD_STB1#
2X/4X Timing group SET#3	7.25"	5 mil	20 mil	+/- 0.125"	SB_STB SB_STB#
2X/4X Timing group SET#1	6'	5 mil	15 mil	+/- 0.25"	GAD_STB0 GAD_STB0#
2X/4X Timing group SET#2	6'	5 mil	15 mil	+/- 0.25"	GAD_STB1 GAD_STB1#
2X/4X Timing group SET#3	6'	5 mil	15 mil	+/- 0.25"	SB_STB SB_STB#

Title: Revision History - 1	Rev: 0A
Document Number: MS-6506	
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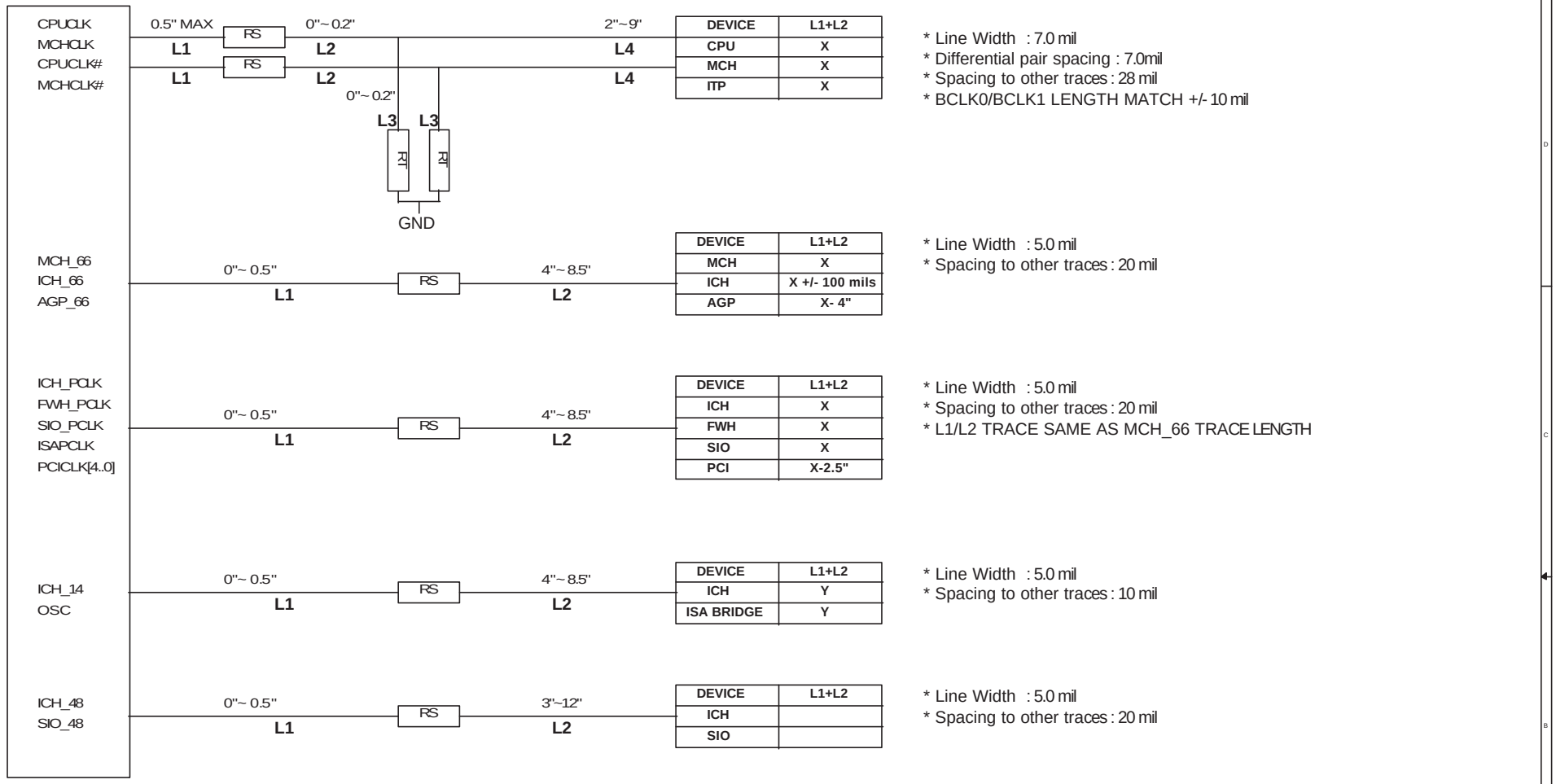


DEVICE	L1+L2
CPU	X
MCH	X
ITP	X

* Line Width : 7.0 mil
* Differential pair spacing : 7.0mil
* Spacing to other traces : 28 mil
* BCLK0/BCLK1 LENGTH MATCH +/- 10 mil

DEVICE	L1+L2
MCH	X
ICH	X +/- 100 mils
AGP	X- 4"

* Line Width : 5.0 mil
* Spacing to other traces : 20 mil

DEVICE	L1+L2
ICH	X
FWH	X
SIO	X
PCI	X-2.5"

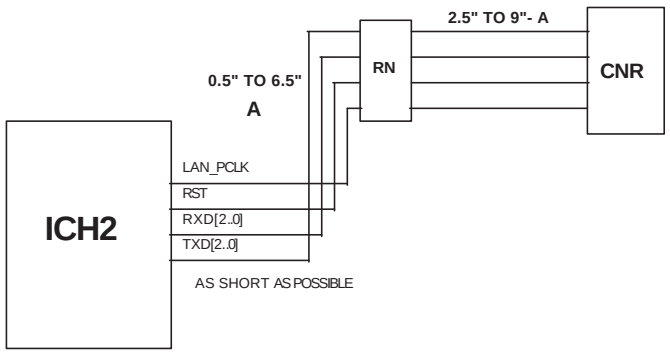
* Line Width : 5.0 mil
* Spacing to other traces : 20 mil
* L1/L2 TRACE SAME AS MCH_66 TRACE LENGTH

DEVICE	L1+L2
ICH	Y
ISA BRIDGE	Y

* Line Width : 5.0 mil
* Spacing to other traces : 10 mil

DEVICE	L1+L2
ICH	
SIO	

* Line Width : 5.0 mil
* Spacing to other traces : 20 mil



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Document Number: MS-6506	
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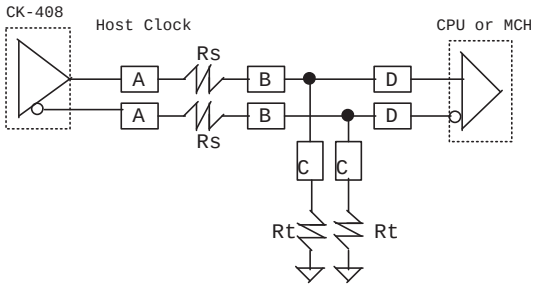
Clock Routing Guidelines

1.CPU and MCH differential host bus clock routing rule

Signal	Length A	Length B	Length C	Length D	Width	Spacing
CPUCLK, CPUCLK# MCHCLK, MCHCLK# (Note1)	Max = 0.5"	0.0" - 0.2"	0.0" - 0.2"	2" - 9"	7 mils	7 mils (Note2)
CPU clock trace length	CPU clock length = A + B + D =X"					
MCH clock trace length	MCH clock length = A + B + D =(X"+0.4") to (X"+0.6")					



Note1:

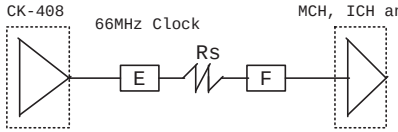
* The clk and clk# length matching +/-10mil of a differential clock pair
* A differential clock pair do not split up,must be keep 7mils spacing and reference to GND

Note2:

* Differential pair spacing = 7 mils
* Spacing to other trace = 28 - 35 mils

2.MCH,ICH and AGP 66MHz clock routing rule

Signal	Length E	Length F	Width	Spacing
MCH_66CLK ICH_66CLK (Note1)	0.0" - 0.5"	4.0" - 8.5" = Y"	5 mils	20 mils
AGPCLK (Note2)	0.0" - 0.5"	Y" - 4"		
MCH or ICH clock trace length	MCH or ICH clock length = E + F = Y"			
AGP clock trace length	AGP clock length = E + F = Y" - 4"			

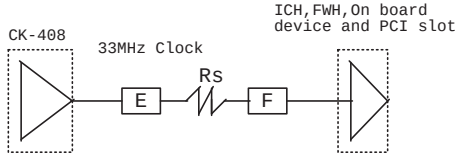


Note1: MCH with ICH clock trace match = +/- 100 mils

Note2: AGP clock trace length less than MCH or ICH clock trace length = 4" +/- 100 mils

3.ICH,FWH,On board device and PCI slot 33MHz clock routing rule

Signal	Length E	Length F	Width	Spacing
ICH_PCLK FWH_PCLK DEV_PCLK (Note1)	0.0" - 0.5"	4.0" - 8.5" = Y"	5 mils	15 mils
SLOT_PCLK (Note2)	0.0" - 0.5"	Y" - 2.6"		
ICH or DEV PCI clock trace length	ICH,FWH or DEV PCI clock length = E + F = Y"			
Slot PCI clock trace length	Slot PCI clock length = E + F = Y" - 2.6"			



Note1:33MHz trace length must be match with 66MHz of all the on board device = +/- 100 mils

Note2: Slot PCI clock trace length less than ICH PCI clock trace length = 2.6" +/- 100 mils

4.ICH and SIO 14MHz clock routing rule

Signal	Length E	Length F	Width	Spacing
ICH_14CLK SIO_14CLK	0.0" - 0.5"	0" - 18"	5 mils	10 mils

5.ICH and SIO 48MHz clock routing rule

Signal	Length E	Length F	Width	Spacing
ICH_48CLK SIO_48CLK	0.0" - 0.5"	3" - 12"	5 mils	15 mils

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MCH Routing Guidelines

1.HVREF,HSWNG and HRCOMP signal layout

Signal	Max. Length	Width	Clearance
HVREF	3"	12 mil	10 mil
HSWNG	3"	12 mil	10 mil
HRCOMP	0.5"	10 mil	7 mil

SDRAM Routing Guidelines

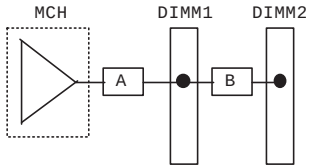
1.SDQ[63:0],SCB[7:0] routing rule

2DIMM Layout Guideline

Signal	Length A	Length B	Width	Trace Spacing	Group Spacing
SDQ[63:0] SCB[7:0]	2.0" - 4.0"	0.4" - 0.6"	5 mil	12 mil	12 mil

Breakout CHIP routing rule

Width/spacing	Max. Length
5 mil / 5 mil	0.5"
5 mil / 8 mil	1.5"



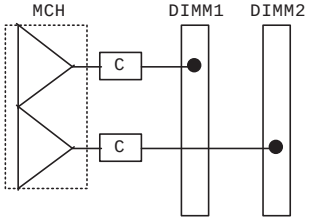
2.SCS#[7:0],SCKE[3:0] routing rule

2DIMM Layout Guideline

Signal	Length C	Width	Trace Spacing	Group Spacing
SCS#[7:0]	3.0" - 4.0"	5 mil	12 mil	12 mil
SCKE[5:0]	3.0" - 4.0"	10 mil	12 mil	12 mil

Breakout CHIP routing rule

Width/spacing	Max. Length
5 mil / 5 mil	0.5"



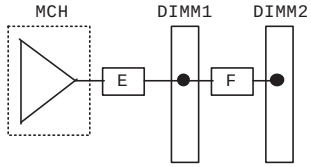
3.SMA[12:0],SBS[1:0],SRAS#,SCAS#,SWE# routing rule

2DIMM Layout Guideline

Signal	Length E	Length F	Width	Trace Spacing	Group Spacing
SMA[12:0] SBS[1:0] SRAS# SCAS# SWE#	2.0" - 3.0"	0.4" - 0.6"	5 mil	10 mil	12 mil

2DIMM Breakout CHIP routing rule

Width/spacing	Max. Length
5 mil / 5 mil	0.5"
5 mil / 8 mil	1.5"



4.SCK[0:7] routing rule

2DIMM Layout Guideline

Signal	Length G	Length H	Length I	Length J	Length K	Width	Trace Spacing	Group Spacing
SCK[7:0]	See Table-3	0.0" - 1.0"	0.0" - 0.25"	4.0" - 5.0"	0.0" - 1.5"	7 mil	15 mil	15 mil

2DIMM Total Length Limits

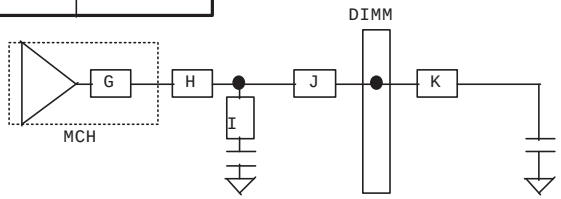
MCH package length G + Length H + Length J = Total length
G + H + J = 5.3"+/- 50mils

Table - 3

SCK Signal	Package Trace Length(")
SCK0	0.404
SCK1	0.353
SCK2	0.865
SCK3	0.893
SCK4	0.371
SCK5	0.349
SCK6	0.814
SCK7	0.821
SCK8	0.483
SCK9	0.432
SCK10	0.589
SCK11	0.689

Breakout CHIP routing rule

Width/spacing	Max. Length
7 mil / 5 mil	0.5"
7 mil / 10 mil	1.0"



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Norminal 4-layer Board Stackup

1.Board spec.

Description	Target Value	notes
Micro-stripline Er	4.2 - 4.5	
Trace Thickness	1.3 - 1.42 mils	Note1
Board Thickness	62 mils	
Material	FR4	
Fab Construction	4 layer	

Note1: Thickness after plating

2.Board each layer thickness .

Description	Target Value	Tolerance(+/- mils)
(Layer 1) Top layer	1.4 mil	See notes 1
Perpreg	4.0 mil	0.3
(Layer 2) Power layer	1.4 mil	0.2
Core	48 mil	5
(layer 3) Ground layer	1.4 mil	0.2
Perpreg	4.0 mil	0.3
(layer 4) Bottom layer	1.4 mil	See notes 1

Note1: Final plating thickness from 1.3 - 1.42 mils

3.Via Stack

Description	Target Value
Via Pad	26 mil
Via Anti-Pad	40 mil
Via Finiched hole	14 mil
Signal Pad(BGA)	20 mil

4.CPU GTL+ bus impedance = 50 Ohm(7mil trace width)

5.CPU asynchronous GTL+,AGP,Memory and Hub-link bus impedance = 60 Ohm(5mil trace width)

CPU Routing Guidelines

1.CPU data or address synchronous signal groups and the associate strobe

Signals	Associated Strobe
REQ[4:0]#,A[16:3]#	ADSTB0#
A[31:17]#	ADSTB1#
D[15:0]#,DBI0#	DSTBP0#,DSTBN0#
D[31:16]#,DBI1#	DSTBP1#,DSTBN1#
D[47:32]#,DBI2#	DSTBP2#,DSTBN2#
D[63:48]#,DBI3#	DSTBP3#,DSTBN3#

***All the system bus signals must be referenced to GND**

2.CPU connect to MCH address layout guideline

Signal	PCB length	Total length	Width	Spacing	Length match
REQ[4:0]# A[16:3]# ADSTB0# (Note1)	2" - 10" (Note2)	See Table -1	5 mils	13 mils (Note3)	+/- 200 mils (Note4)
A[31:17]# ADSTB1# (Note1)	2" - 10" (Note2)	See Table -1	5 mils	13 mils (Note3)	+/- 200 mils (Note4)

Note1:This group all the signals keep same length

Note2:This trace length is pin to pin length

Note3:Trace edge to edge spacing greater than 3:1 versus trace to reference plane height ratio

Note4:This group other signal trace lengtn match = ADSTB# +/- 200 mils

3. CPU connect to MCH data layout guideline

Signal	PCB length	Total length	Width	Spacing	Length match
D[15:0]# DBI0# DSTBP0# DSTBN0# (Note1)	2" - 10" (Note2)	See Table -1	5 mils	13 mils (Note3)	+/- 100 mils +/- 25 mils (Note4)
D[31:16]# DBI1# DSTBP1# DSTBN1# (Note1)	2" - 10" (Note2)	See Table -1	5 mils	13 mils (Note3)	+/- 100 mils +/- 25 mils (Note4)
D[47:32]# DBI2# DSTBP2# DSTBN2# (Note1)	2" - 10" (Note2)	See Table -1	5 mils	13 mils (Note3)	+/- 100 mils +/- 25 mils (Note4)
D[63:48]# DBI3# DSTBP3# DSTBN3# (Note1)	2" - 10" (Note2)	See Table -1	5 mils	13 mils (Note3)	+/- 100 mils +/- 25 mils (Note4)

Note1:This group all the signals keep same length

Note2:This trace length is pin to pin length

Note3:Trace edge to edge spacing greater than 3:1 versus trace to reference plane height ratio

Note4:

* Each group DSTBPn/p# signals pad to pad length match = +/- 25 mils
* This group other signal trace lengtn match = DSTBn/p# +/- 100 mils

Table - 1

CPU package length + PCB trace length + MCH package length = Total length					
L1	+	L2	+	L3	= Total L4

7.Keep the voltage divider with in 1.5 inches of GTLREF pin.and do not allow the GTLREF routing to splits or discontinuities power plane.

8.CPU Asynchronous GTL+ bus connect to ICH2 trace length

Signal Name	Trace Spacing	Trace Length	Pull-up Resistor
FERR#	7 MIL	1"-12"	62 Ohm +/- 5%
PROCHHOT#	7 MIL	1"-17"	62 Ohm +/- 5%
THERMTRIP#	7 MIL	1"-17"	62 Ohm +/- 5%
A20M#	7 MIL	1"-12"	None
IGNNE#	7 MIL	1"-12"	None
LINT[1:0]	7 MIL	1"-12"	None
SLP#	7 MIL	1"-12"	None
SMI#	7 MIL	1"-12"	None
STPCLK#	7 MIL	1"-12"	None
INIT#	7 MIL	1"-17"	None
PWRGOOD	7 MIL	1"-12"	300 Ohm +/- 5%

9.CPU BCLK,BCLK# should be routed as a differential pair with 7 mil trace and 7 mil spacing between them,2.5" to 10" pin to pin common clock lengths, and 25 mil spacing away form all the signal or clock.

10.DBSY#,DRDY#,TRDY#,ADS#,LOCK#,BNR#,HIT#,HITM#,BPRI#,DEFER#,BR0#,RESET# and RS[2:0]# CPU signal trace length around 2.5" to 10"

Title: CPU Bus Layout Guigeline	Rev: 0A
Document Number: MS-6506	
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Norminal 4-layer Board Stackup

1.Board spec.

Description	Target Value	notes
Micro-stripline Er	4.2 - 4.5	
Trace Thickness	1.3 - 1.42 mils	Note1
Board Thickness	62 mils	
Material	FR4	
Fab Construction	4 layer	

Note1: Thickness after plating

2.Board each layer thickness .

Description	Target Value	Tolerance(+/- mils)
(Layer 1) Top layer	1.4 mil	See notes 1
Perpreg	4.0 mil	0.3
(Layer 2) Power layer	1.4 mil	0.2
Core	48 mil	5
(layer 3) Ground layer	1.4 mil	0.2
Perpreg	4.0 mil	0.3
(layer 4) Bottom layer	1.4 mil	See notes 1

Note1: Final plating thickness from 1.3 - 1.42 mils

3.Via Stack

Description	Target Value
Via Pad	26 mil
Via Anti-Pad	40 mil
Via Finiched hole	14 mil
Signal Pad(BGA)	20 mil

4.CPU GTL+ bus impedance = 50 Ohm(7mil trace width)

5.CPU asynchronous GTL+,AGP,Memory and Hub-link bus impedance = 60 Ohm(5mil trace width)

CPU Routing Guidelines

1.CPU data synchronous signal groups and the associate strobe

Signals	Associated Strobe
REQ[4:0]#,A[16:3]#	ADSTB0#
A[31:17]#	ADSTB1#
D[15:0]#,DBI0#	DSTBP0#,DSTBN0#
D[31:16]#,DBI1#	DSTBP1#,DSTBN1#
D[47:32]#,DBI2#	DSTBP2#,DSTBN2#
D[63:48]#,DBI3#	DSTBP3#,DSTBN3#

***All the system bus signals must be referenced to GND**

2.Trace edge to edge spacing greater than 3:1(about 12 mils) versus trace to GND plane height ratio

3.2" - 10" from pin to pin and each data signal group should be routed to same length within +/-100 mils of the associated strobes.Additional CPU,MCH internal trcae length(see Table-1)must be included.The calculation trace length follow (Table-2).

4.A pair data strobe should be routed to the same length within +/- 25mils, if one strobe switch layers, and another switch layer in the same manner.Additional CPU,MCH internal trace length(See Table-1)must be inculded.The calculation trace length follow (Table-2)

5.2" - 10" from pin to pin and each address signal group should be routed to same length within +/-200 mils of the associated strobes.Additional CPU,MCH internal trcae length(see Table-1)must be included.The calculation trace length follow (Table-2).

6.Internal adderss strobe trace length(See Table-1) of CPU,MCH must be inculded.The calculation trace length follow (Table-2)

Table - 1

CPU package length + PCB trace length + MCH package length = Total length					
L1	+	L2	+	L3	= Total L4

7.Keep the voltage divider with in 1.5 inches of GTLREF pin.and do not allow the GTLREF routing to splits or discontinuities power plane.

8.CPU Asynchronous GTL+ bus connect to ICH2 trace length

Signal Name	Trace Spacing	Trace Length	Pull-up Resistor
FERR#	7 MIL	1"-12"	62 Ohm +/- 5%
PROCHHOT#	7 MIL	1"-17"	62 Ohm +/- 5%
THERMTRIP#	7 MIL	1"-17"	62 Ohm +/- 5%
A20M#	7 MIL	1"-12"	None
IGNNE#	7 MIL	1"-12"	None
LINT[1:0]	7 MIL	1"-12"	None
SLP#	7 MIL	1"-12"	None
SMI#	7 MIL	1"-12"	None
STPCLK#	7 MIL	1"-12"	None
INIT#	7 MIL	1"-17"	None
PWRGOOD	7 MIL	1"-12"	300 Ohm +/- 5%

9.CPU BCLK,BCLK# should be routed as a differential pair with 7 mil trace and 7 mil spacing between them,2.5" to 10" pin to pin common clock lengths, and 25 mil spacing away form all the signal or clock.

10.DBSY#,DRDY#,TRDY#,ADS#,LOCK#,BNR#,HIT#,HITM#,BPRI#,DEFER#,BR0#,RESET# and RS[2:0]# CPU signal trace length around 2.5" to 10"

Signal	CPU ball	CPU length(")	MCH ball	MCH length(")
Address Group 0				
ADSTB#0	L5	0.210	R5	0.530
A#3	K2	0.368	T4	0.518
A#4	K4	0.265	T5	0.434
A#5	L6	0.155	T3	0.728
A#6	K1	0.415	U3	0.577
A#7	L3	0.304	R3	0.551
A#8	M6	0.144	P7	0.359
A#9	L2	0.372	R2	0.643
A#10	M3	0.327	P4	0.533
A#11	M4	0.246	R6	0.397
A#12	N1	0.394	P5	0.463
A#13	M1	0.408	P3	0.576
A#14	N2	0.349	N2	0.660
A#15	N4	0.241	N7	0.407
A#16	N5	0.198	N3	0.570
REQ#0	J1	0.427	U6	0.402
REQ#1	K5	0.207	T7	0.350
REQ#2	J4	0.270	R7	0.393
REQ#3	J3	0.337	U5	0.475
REQ#4	H3	0.356	U3	0.599
Address Group 1				
ADSTB#1	R5	0.214	N6	0.438
A#17	T1	0.470	K4	0.550
A#18	R2	0.404	M4	0.580
A#19	P3	0.303	M3	0.648
A#20	P4	0.246	L3	0.604
A#21	R3	0.334	L5	0.521
A#22	T2	0.388	K3	0.624
A#23	U1	0.458	J2	0.685
A#24	P6	0.156	M5	0.509
A#25	U3	0.379	J3	0.636
A#26	T4	0.281	L2	0.648
A#27	V2	0.417	H4	0.634
A#28	R6	0.166	N5	0.472
A#29	W1	0.493	G2	0.792
A#30	T5	0.217	M6	0.449
A#31	U4	0.285	L7	0.365

Signal	CPU ball	CPU length(")	MCH ball	MCH length(")
Data Group 0				
DSTBN#0	E22	0.338	AD4	0.759
DSTBP#0	F21	0.326	AD3	0.801
D#0	B21	0.414	AA2	0.649
D#1	B22	0.475	AB5	0.564
D#2	A23	0.538	AA5	0.531
D#3	A25	0.608	AB3	0.678
D#4	C21	0.386	AB4	0.628
D#5	D22	0.386	AC5	0.635
D#6	B24	0.535	AA3	0.623
D#7	C23	0.464	AA6	0.468
D#8	C24	0.515	AE3	0.802
D#9	B25	0.590	AB7	0.495
D#10	G22	0.274	AD7	0.609
D#11	H21	0.203	AC7	0.548
D#12	C26	0.589	AC6	0.579
D#13	D23	0.462	AC3	0.709
D#14	J21	0.183	AC8	0.590
D#15	D25	0.550	AE2	0.856
DBI#0	E21	0.309	AD5	0.637
Data Group 1				
DSTBN#1	K22	0.301	AE6	0.693
DSTBP#1	J23	0.306	AE7	0.638
D#16	H22	0.272	AG5	0.845
D#17	E24	0.480	AG2	0.904
D#18	G23	0.358	AE8	0.663
D#19	F23	0.418	AF6	0.759
D#20	F24	0.443	AH2	0.965
D#21	E25	0.508	AF3	0.798
D#22	F26	0.513	AG3	0.898
D#23	D26	0.597	AE5	0.709
D#24	L21	0.176	AH7	0.863
D#25	G26	0.524	AH3	0.904
D#26	H24	0.412	AF4	0.794
D#27	M21	0.171	AG8	0.789
D#28	L22	0.245	AG7	0.785
D#29	J24	0.401	AG6	0.785
D#30	K23	0.313	AF8	0.711
D#31	H25	0.473	AH5	0.892
DBI#1	G25	0.458	AG4	0.888

Signal	CPU ball	CPU length(")	MCH ball	MCH length(")
Data Group 2				
DSTBN#2	K22	0.252	AE11	0.595
DSTBP#2	J23	0.266	AD11	0.532
D#32	M23	0.300	AC11	0.514
D#33	N22	0.226	AC12	0.565
D#34	P21	0.178	AE9	0.652
D#35	M24	0.371	AC9	0.566
D#36	N23	0.271	AE10	0.605
D#37	M26	0.454	AD9	0.635
D#38	N26	0.437	AG9	0.724
D#39	N25	0.383	AC10	0.543
D#40	R21	0.165	AE12	0.558
D#41	P24	0.343	AF10	0.666
D#42	R25	0.381	AG11	0.703
D#43	R24	0.329	AG10	0.705
D#44	T26	0.420	AH11	0.754
D#45	T25	0.380	AG12	0.669
D#46	T22	0.221	AE13	0.563
D#47	T23	0.279	AF12	0.596
DBI#2	P26	0.441	AH9	0.775
Data Group 3				
DSTBN#3	W22	0.298	AC15	0.443
DSTBP#3	W23	0.300	AC16	0.395
D#48	U26	0.419	AG13	0.668
D#49	U24	0.324	AH13	0.712
D#40	U23	0.270	AC14	0.412
D#51	V25	0.384	AF14	0.548
D#52	U21	0.167	AG14	0.621
D#53	V22	0.252	AE14	0.520
D#54	V24	0.341	AG15	0.612
D#55	W26	0.447	AG16	0.610
D#56	Y26	0.454	AG17	0.619
D#57	W25	0.426	AH15	0.703
D#58	Y23	0.336	AC17	0.339
D#59	Y24	0.386	AF16	0.580
D#60	Y21	0.222	AE15	0.534
D#61	AA25	0.426	AH17	0.672
D#62	AA22	0.268	AD17	0.419
D#63	AA24	0.394	AE16	0.503
DBI#3	V21	0.202	AD15	0.431

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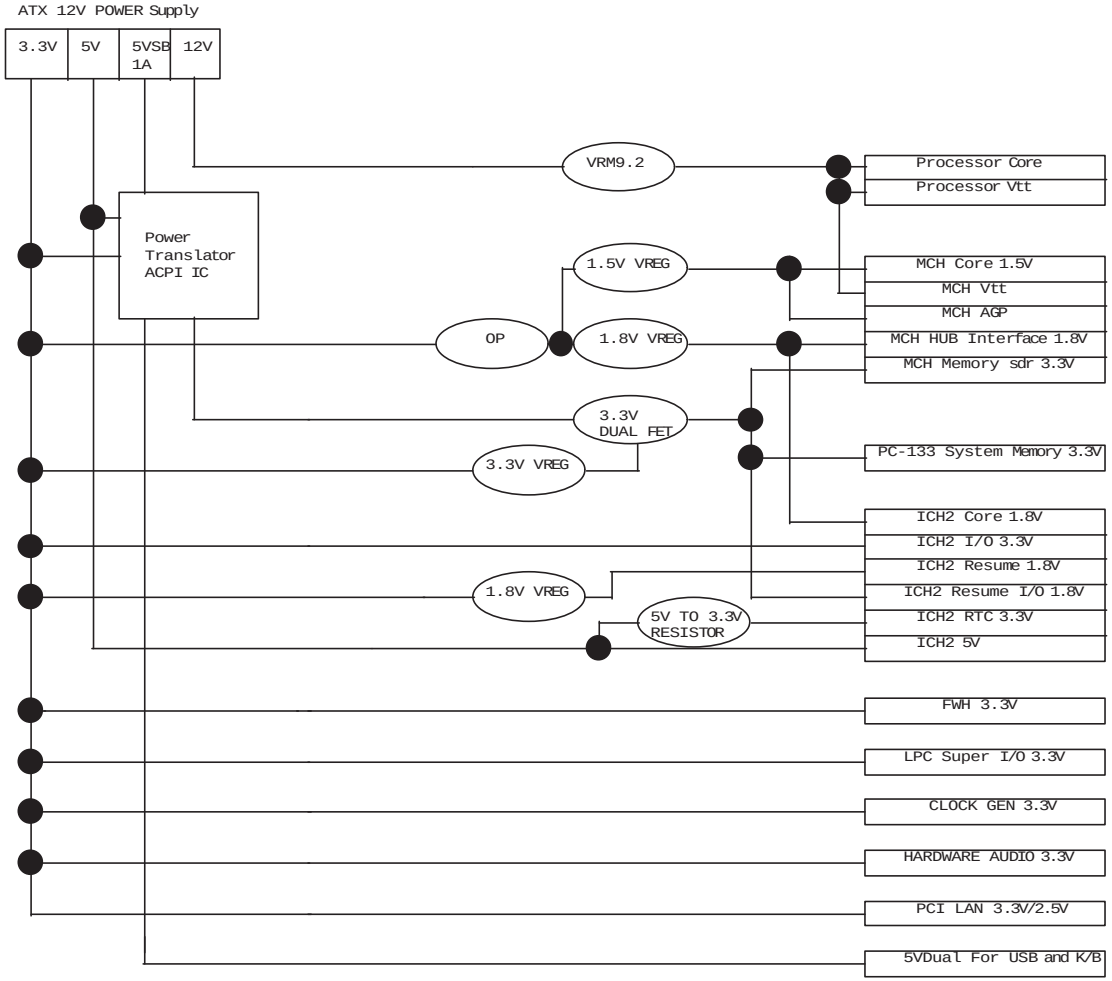
Power Delivery Map



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0A Revision History

05/22	05	**GTLREF[0:3] just reference to one Reference Voltage GTLREF1.**
05/22	10	**Remove Processor Hot Block. Add GPIO21 for Flash Vpp Programing Voltage Control.**
05/22	13	**Change U10 Vpp Circuit for 12V Programming.**
05/23	04	**Remove ITPCLK/ITPCLK#.**
05/23	05	**Restore GTLREF[0,2] reference to GTLREF2 and GTLREF[1,3] to GTLREF1. For Layout Consideration**
05/29	13	**Add Q92 for Vpp Programing Control Logic.**
05/31	12	**Reserved C109 & R190 for SPDIF Noise Considerarion.**
06/01	X	**Rename Schematics file.**

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