MS-6501 ATX Version 0C

Last Update 11/12/2001

CPU:

Dual AMD Socket-462 Processors

System Chipset:

AMD 762(North Bridge)
AMD 768 (South Bridge)

Expansion Slots:

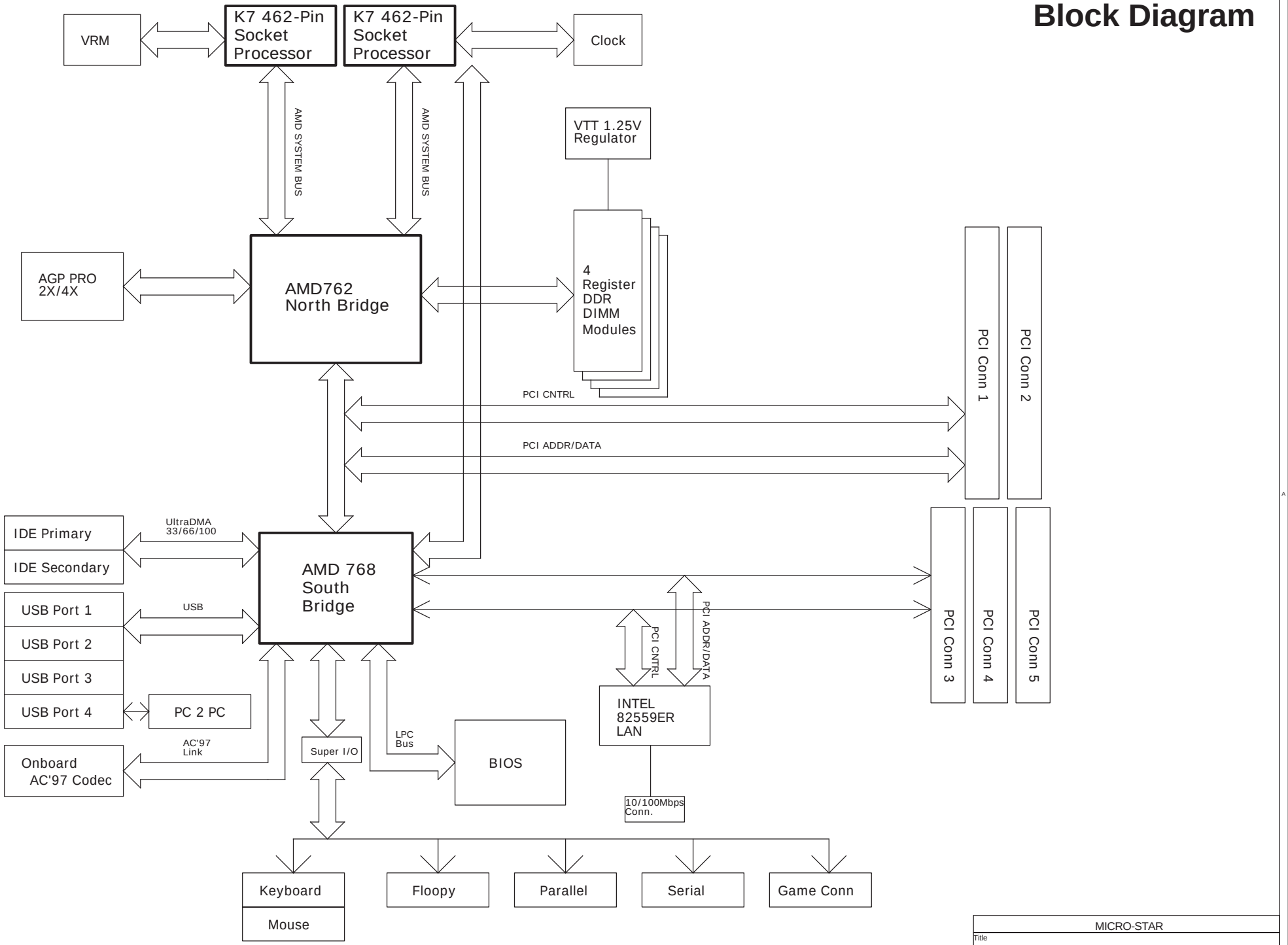
AGP-Pro SLOT * 1
PCI2.2 PCI/64/66 SLOT * 2
PCI2.2 PCI/32/33 SLOT * 3

On Board:

LAN 82559ER
AC97 Codec
PC 2 PC

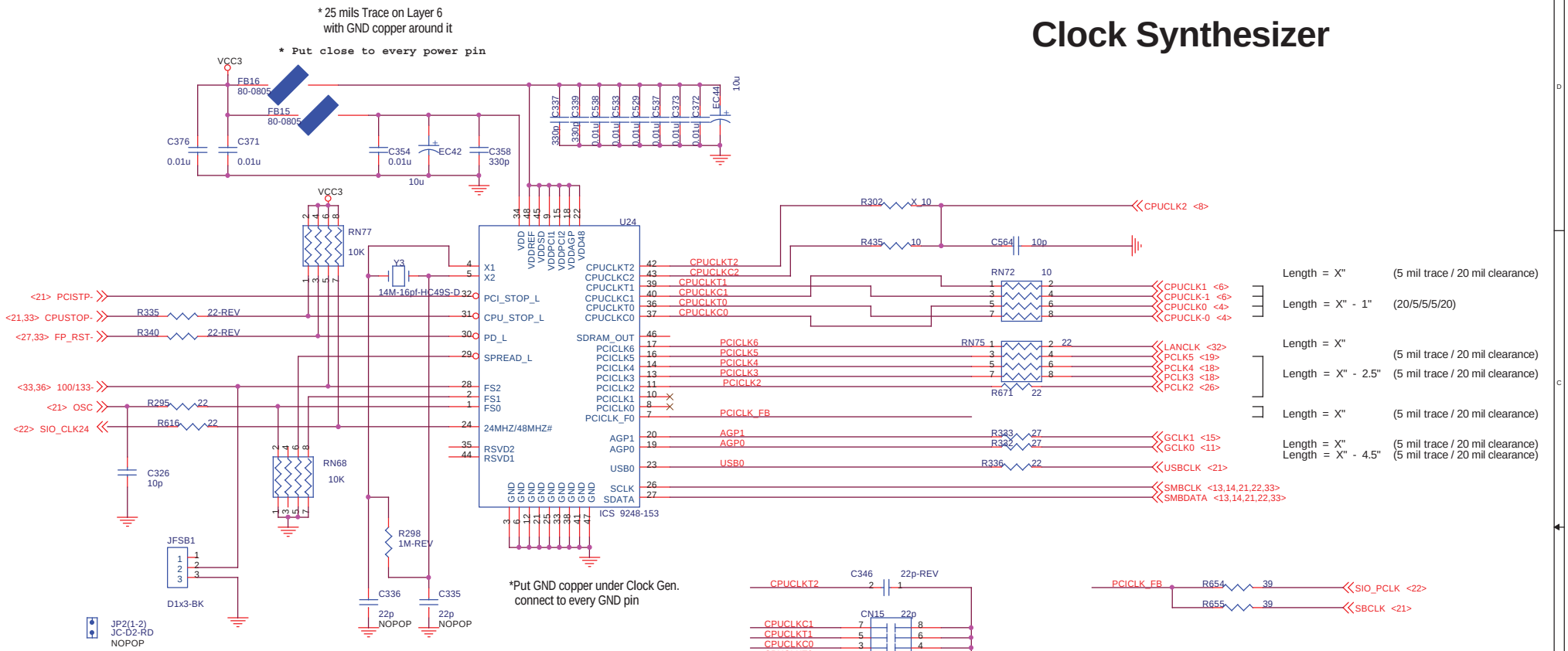
MICRO-STAR		
Title: Cover Sheet		
Size: Custom	Document Number: MS-6501	Rev: 0C
Date: Tuesday, November 20, 2001	Sheet 1 of 41	

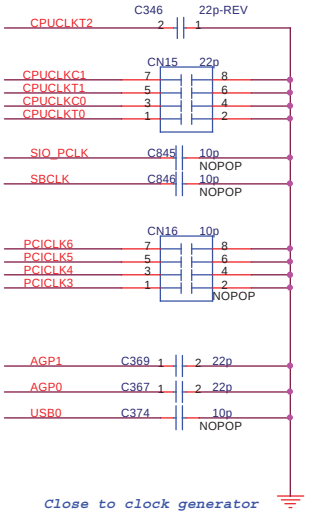
Block Diagram



MICRO-STAR		
Title: Block Diagram		
Size: Custom	Document Number: MS-6501	Rev: 0C
Date: Tuesday, November 20, 2001	Sheet 2 of 41	

Clock Synthesizer





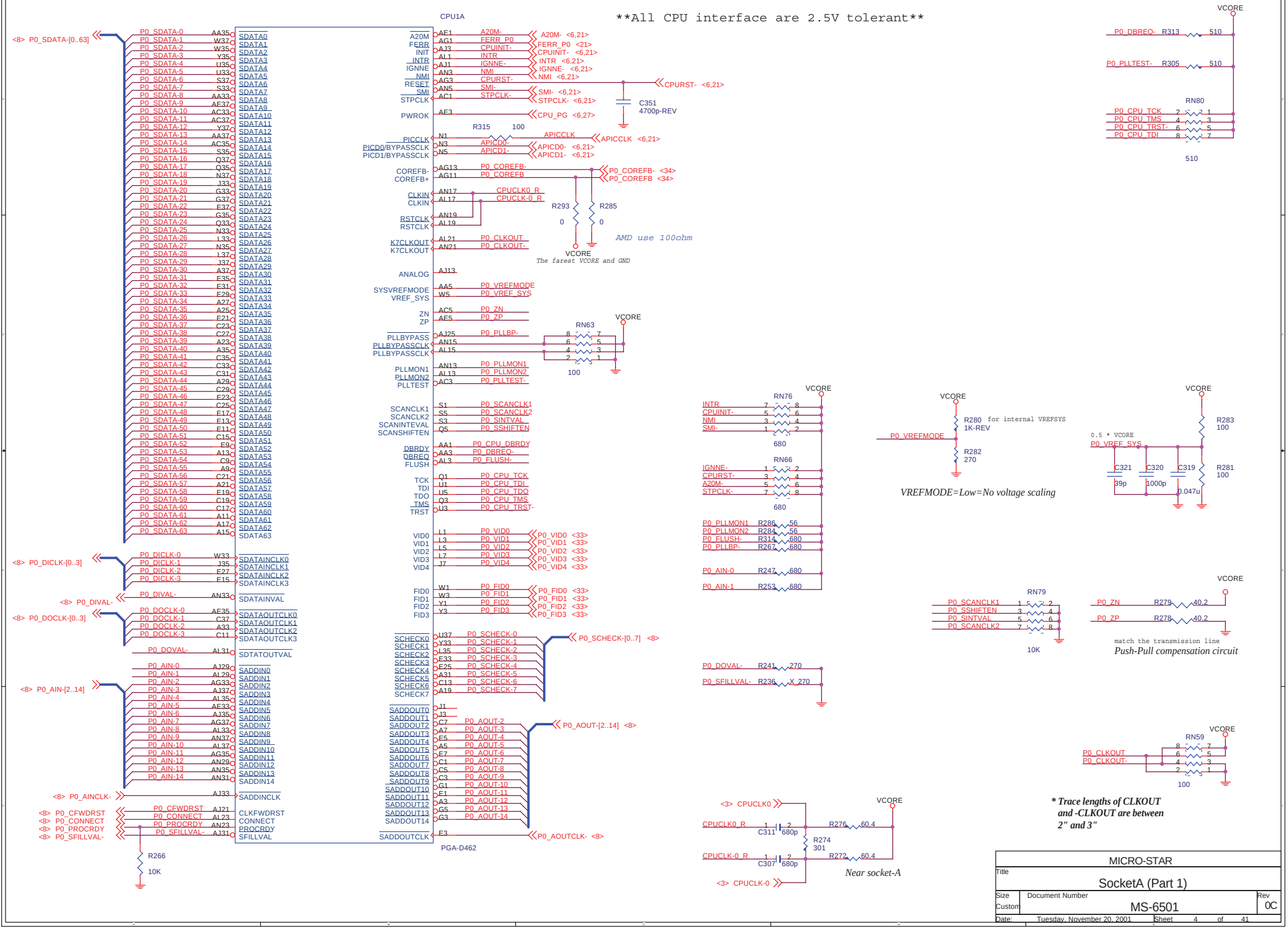
	WIDTH/SPACE		LENGTH
CPUCLK0&CPUCLK0#:	5/20	5 FOR DIFF. PAIR	X-1 INCH
CPUCLK1&CPUCLK1#:	5/20	5 FOR DIFF. PAIR	X-1 INCH
CPUCLK2&GCLK0	5/20		X
GCLK1	5/20		X-4.5
NBCLK&SBCLK	5/20		X
PCICLK GROUP	5/20		X-2.5

* X MEANS THE SHORTEST LENGTH FOR MAINTAIN PROPAGATION DELAY

* CPUCLK1'S TERMINATION CKT MUST BE PLACED NEAR TO NB

FS2	FS1	FS0	CPU SDRAM	PCI	AGP
0	0	0	133.3	33.3	66.7
0	0	1	95.0	31.67	63.33
0	1	0	100.99	33.66	67.33
0	1	1	115.0	38.33	76.67
1	0	0	100.7	33.57	67.13
1	0	1	103.0	34.33	66.6
1	1	0	105.0	35.00	60.0
1	1	1	110.0	36.67	66.6

MICRO-STAR		
Title	Clock Synthesizer	
Size: Custom	Document Number: MS-6501	Rev: 0C
Date: Tuesday, November 20, 2001	Sheet 3 of 41	


All CPU interface are 2.5V tolerant
CPU1A
PGA-D462
<8> P_SDATA-[0..63]
P_SDATA-0 AA35 SDATA0
P_SDATA-1 W37 SDATA1
P_SDATA-2 W35 SDATA2
P_SDATA-3 Y35 SDATA3
P_SDATA-4 U35 SDATA4
P_SDATA-5 U33 SDATA5
P_SDATA-6 S37 SDATA6
P_SDATA-7 S33 SDATA7
P_SDATA-8 AA33 SDATA8
P_SDATA-9 AE37 SDATA9
P_SDATA-10 AC33 SDATA10
P_SDATA-11 AC37 SDATA11
P_SDATA-12 Y37 SDATA12
P_SDATA-13 AA37 SDATA13
P_SDATA-14 AC35 SDATA14
P_SDATA-15 S35 SDATA15
P_SDATA-16 Q37 SDATA16
P_SDATA-17 Q35 SDATA17
P_SDATA-18 N37 SDATA18
P_SDATA-19 J33 SDATA19
P_SDATA-20 G33 SDATA20
P_SDATA-21 G37 SDATA21
P_SDATA-22 E37 SDATA22
P_SDATA-23 G35 SDATA23
P_SDATA-24 Q33 SDATA24
P_SDATA-25 N33 SDATA25
P_SDATA-26 L33 SDATA26
P_SDATA-27 N35 SDATA27
P_SDATA-28 L37 SDATA28
P_SDATA-29 J37 SDATA29
P_SDATA-30 A37 SDATA30
P_SDATA-31 E35 SDATA31
P_SDATA-32 E31 SDATA32
P_SDATA-33 E29 SDATA33
P_SDATA-34 A27 SDATA34
P_SDATA-35 A25 SDATA35
P_SDATA-36 E21 SDATA36
P_SDATA-37 C23 SDATA37
P_SDATA-38 C27 SDATA38
P_SDATA-39 A23 SDATA39
P_SDATA-40 A35 SDATA40
P_SDATA-41 C35 SDATA41
P_SDATA-42 C33 SDATA42
P_SDATA-43 C31 SDATA43
P_SDATA-44 A29 SDATA44
P_SDATA-45 C29 SDATA45
P_SDATA-46 E23 SDATA46
P_SDATA-47 C25 SDATA47
P_SDATA-48 E17 SDATA48
P_SDATA-49 E13 SDATA49
P_SDATA-50 E11 SDATA50
P_SDATA-51 C15 SDATA51
P_SDATA-52 E9 SDATA52
P_SDATA-53 A13 SDATA53
P_SDATA-54 C9 SDATA54
P_SDATA-55 A9 SDATA55
P_SDATA-56 C21 SDATA56
P_SDATA-57 A21 SDATA57
P_SDATA-58 E19 SDATA58
P_SDATA-59 C19 SDATA59
P_SDATA-60 C17 SDATA60
P_SDATA-61 A11 SDATA61
P_SDATA-62 A17 SDATA62
P_SDATA-63 A15 SDATA63
<8> P_DICLK-[0..3]
P_DICLK-0 W33 SDATAINCLK0
P_DICLK-1 J35 SDATAINCLK1
P_DICLK-2 E27 SDATAINCLK2
P_DICLK-3 E15 SDATAINCLK3
<8> P_DIVAL-
P_DIVAL- AN33 SDATAINVAL
<8> P_DOCLK-[0..3]
P_DOCLK-0 AE35 SDATAOUTCLK0
P_DOCLK-1 C37 SDATAOUTCLK1
P_DOCLK-2 A33 SDATAOUTCLK2
P_DOCLK-3 C11 SDATAOUTCLK3
P_DOVAL- AL31 SDTATOUTVAL
<8> P_AIN-[2..14]
P_AIN-0 AJ29 SADDIN0
P_AIN-1 AL29 SADDIN1
P_AIN-2 AG33 SADDIN2
P_AIN-3 AJ37 SADDIN3
P_AIN-4 AL35 SADDIN4
P_AIN-5 AE33 SADDIN5
P_AIN-6 AJ35 SADDIN6
P_AIN-7 AG37 SADDIN7
P_AIN-8 AL33 SADDIN8
P_AIN-9 AN37 SADDIN9
P_AIN-10 AL37 SADDIN10
P_AIN-11 AG35 SADDIN11
P_AIN-12 AN29 SADDIN12
P_AIN-13 AN35 SADDIN13
P_AIN-14 AN31 SADDIN14
<8> P_AINCLK-
AJ33 SADDINCLK
<8> P_CFWDRST
<8> P_CONNECT
<8> P_PROCRDY
<8> P_SFILLVAL-
P_CFWDRST AJ21 CLKFWDRST
P_CONNECT AL23 CONNECT
P_PROCRDY AN23 PROCRDY
P_SFILLVAL- AJ31 SFILLVAL
R266
10K
A20M AE1 A20M- A20M- <6,21>
FERR AG1 FERR_P0 FERR_P0 <21>
INIT AJ3 CPUINIT- CPUINIT- <6,21>
INTR AL1 INTR INTR <6,21>
IGNNE AJ1 IGNNE- IGNNE- <6,21>
NMI AN3 NMI NMI <6,21>
RESET AG3 CPURST- CPURST- <6,21>
SMI AN5 SMI- SMI- <6,21>
STPCLK AC1 STPCLK- STPCLK- <6,21>
PWROK AE3 CPU_PG <6,27>
C351 4700p-REV
R315 100
PICCLK N1 APICCLK APICCLK <6,21>
PICD0/BYPASSCLK N3 APICD0- APICD0- <6,21>
PICD1/BYPASSCLK N5 APICD1- APICD1- <6,21>
COREFB- AG13 P0_COREFB- P0_COREFB- <34>
COREFB+ AG11 P0_COREFB P0_COREFB <34>
CLKIN AN17 CPUCLK0_R CPUCLK0_R
CLKIN AL17 CPUCLK0_R CPUCLK0_R
RSTCLK AN19 RSTCLK
RSTCLK AL19 RSTCLK
R293 0
R285 0
AMD use 100ohm
K7CLKOUT AL21 P0_CLKOUT
K7CLKOUT AN21 P0_CLKOUT-
VCORE
The farest VCORE and GND
ANALOG AJ13
SYSVREFMODE AA5 P0_VREFMODE
VREF_SYS W5 P0_VREF_SYS
ZN AC5 P0_ZN
ZP AE5 P0_ZP
RN63
PLLBYPASS AJ25 P0_PLLBP-
PLLBYPASSCLK AN15
PLLBYPASSCLK AL15
100
PLLMON1 AN13 P0_PLLMON1
PLLMON2 AL13 P0_PLLMON2
PLLTEST AC3 P0_PLLTEST-
SCANCLK1 S1 P0_SCANCLK1
SCANCLK2 S5 P0_SCANCLK2
SCANINTEVAL S3 P0_SINTVAL
SCANSHIFTEN Q5 P0_SSHIFTEN
DBRDY AA1 P0_CPU_DBRDY
DBREQ AA3 P0_DBREQ-
FLUSH AL3 P0_FLUSH-
TCK Q1 P0_CPU_TCK
TDI U1 P0_CPU_TDI
TDO U5 P0_CPU_TDO
TMS Q3 P0_CPU_TMS
TRST U3 P0_CPU_TRST-
VID0 I1 P0_VID0 P0_VID0 <33>
VID1 I3 P0_VID1 P0_VID1 <33>
VID2 I5 P0_VID2 P0_VID2 <33>
VID3 I7 P0_VID3 P0_VID3 <33>
VID4 J7 P0_VID4 P0_VID4 <33>
FID0 W1 P0_FID0 P0_FID0 <33>
FID1 W3 P0_FID1 P0_FID1 <33>
FID2 Y1 P0_FID2 P0_FID2 <33>
FID3 Y3 P0_FID3 P0_FID3 <33>
SCHECK0 U37 P0_SCHECK-0
SCHECK1 Y33 P0_SCHECK-1
SCHECK2 L35 P0_SCHECK-2
SCHECK3 E33 P0_SCHECK-3
SCHECK4 E25 P0_SCHECK-4
SCHECK5 A31 P0_SCHECK-5
SCHECK6 C13 P0_SCHECK-6
SCHECK7 A19 P0_SCHECK-7
P0_SCHECK-[0..7] <8>
SADDOUT0 J1
SADDOUT1 J3
SADDOUT2 C7 P0_AOUT-2
SADDOUT3 A7 P0_AOUT-3
SADDOUT4 E5 P0_AOUT-4
SADDOUT5 A5 P0_AOUT-5
SADDOUT6 E7 P0_AOUT-6
SADDOUT7 C1 P0_AOUT-7
SADDOUT8 C5 P0_AOUT-8
SADDOUT9 C3 P0_AOUT-9
SADDOUT10 G1 P0_AOUT-10
SADDOUT11 E1 P0_AOUT-11
SADDOUT12 A3 P0_AOUT-12
SADDOUT13 G5 P0_AOUT-13
SADDOUT14 G3 P0_AOUT-14
P0_AOUT-[2..14] <8>
SADDOUTCLK E3 P0_AOUTCLK- <8>
VCORE
P0_DBREQ- R313 510
P0_PLLTEST- R305 510
RN80
P0_CPU_TCK
P0_CPU_TMS
P0_CPU_TRST-
P0_CPU_TDI
510
RN76
INTR
CPUINIT-
NMI
SMI-
680
RN66
IGNNE-
CPURST-
A20M-
STPCLK-
680
P0_PLLMON1 R286 56
P0_PLLMON2 R284 56
P0_FLUSH- R314 680
P0_PLLBP- R267 680
P0_AIN-0 R247 680
P0_AIN-1 R253 680
P0_DOVAL- R241 270
P0_SFILLVAL- R236 270
P0_VREFMODE
R280 for internal VREFSYS 1K-REV
R282 270
VREFMODE=Low=No voltage scaling
0.5 * VCORE
P0_VREF_SYS
R283 100
C321 39p
C320 1000p
C319 0.047u
R281 100
RN79
P0_SCANCLK1
P0_SSHIFTEN
P0_SINTVAL
P0_SCANCLK2
10K
P0_ZN R279 40.2
P0_ZP R278 40.2
match the transmission line
Push-Pull compensation circuit
RN59
P0_CLKOUT
P0_CLKOUT-
100
* Trace lengths of CLKOUT and -CLKOUT are between 2" and 3"
<3> CPUCLK0
CPUCLK0_R C311 680p
CPUCLK0_R C307 680p
R276 60.4
R274 301
R272 60.4
<3> CPUCLK0
Near socket-A
MICRO-STAR
Title
SocketA (Part 1)
Size Custom
Document Number MS-6501
Rev 0C
Date: Tuesday, November 20, 2001
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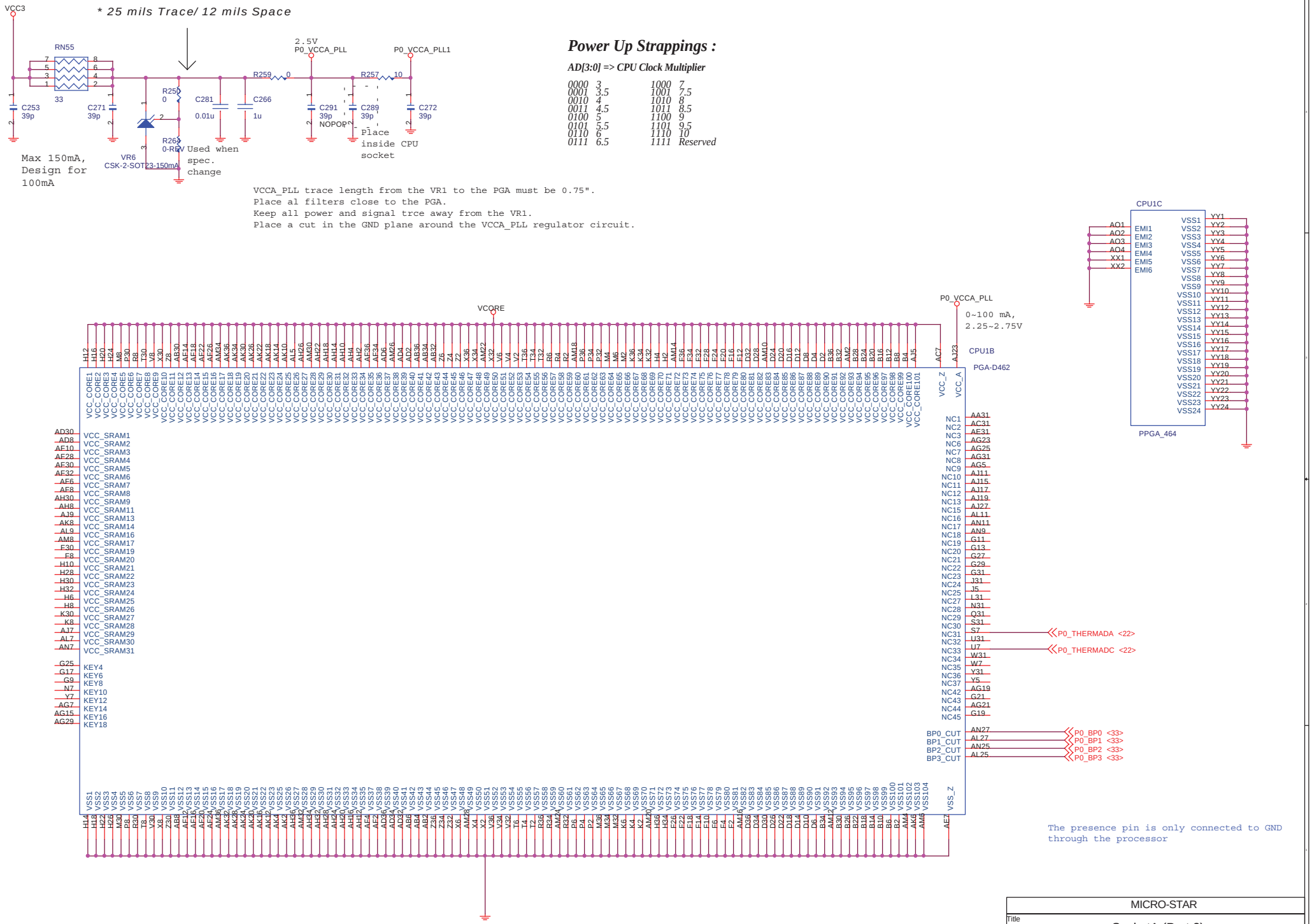
* 25 mils Trace/ 12 mils Space
VCC3
RN55
33
C253 39p
C271 39p
R250 0
R263 0-R/V
VR6 CSK-2-SOT23-150mA
C281 0.01u
C266 1u
R259 0
2.5V
P0_VCCA_PLL
C291 39p NOPOP
C289 39p
R257 10
P0_VCCA_PLL1
C272 39p
Place inside CPU socket
Used when spec. change
Max 150mA, Design for 100mA
Power Up Strappings :
AD[3:0] => CPU Clock Multiplier
0000 3
0001 3.5
0010 4
0011 4.5
0100 5
0101 5.5
0110 6
0111 6.5
1000 7
1001 7.5
1010 8
1011 8.5
1100 9
1101 9.5
1110 10
1111 Reserved
VCCA_PLL trace length from the VR1 to the PGA must be 0.75".
Place al filters close to the PGA.
Keep all power and signal trce away from the VR1.
Place a cut in the GND plane around the VCCA_PLL regulator circuit.
CPU1C
PPGA_464
VCORE
P0_VCCA_PLL
0~100 mA, 2.25~2.75V
CPU1B
PGA-D462
P0_THERMADA <22>
P0_THERMADC <22>
P0_BP0 <33>
P0_BP1 <33>
P0_BP2 <33>
P0_BP3 <33>
The presence pin is only connected to GND through the processor
MICRO-STAR
Title
SocketA (Part 2)
Size Custom
Document Number MS-6501
Rev 0C
Date: Tuesday, November 20, 2001
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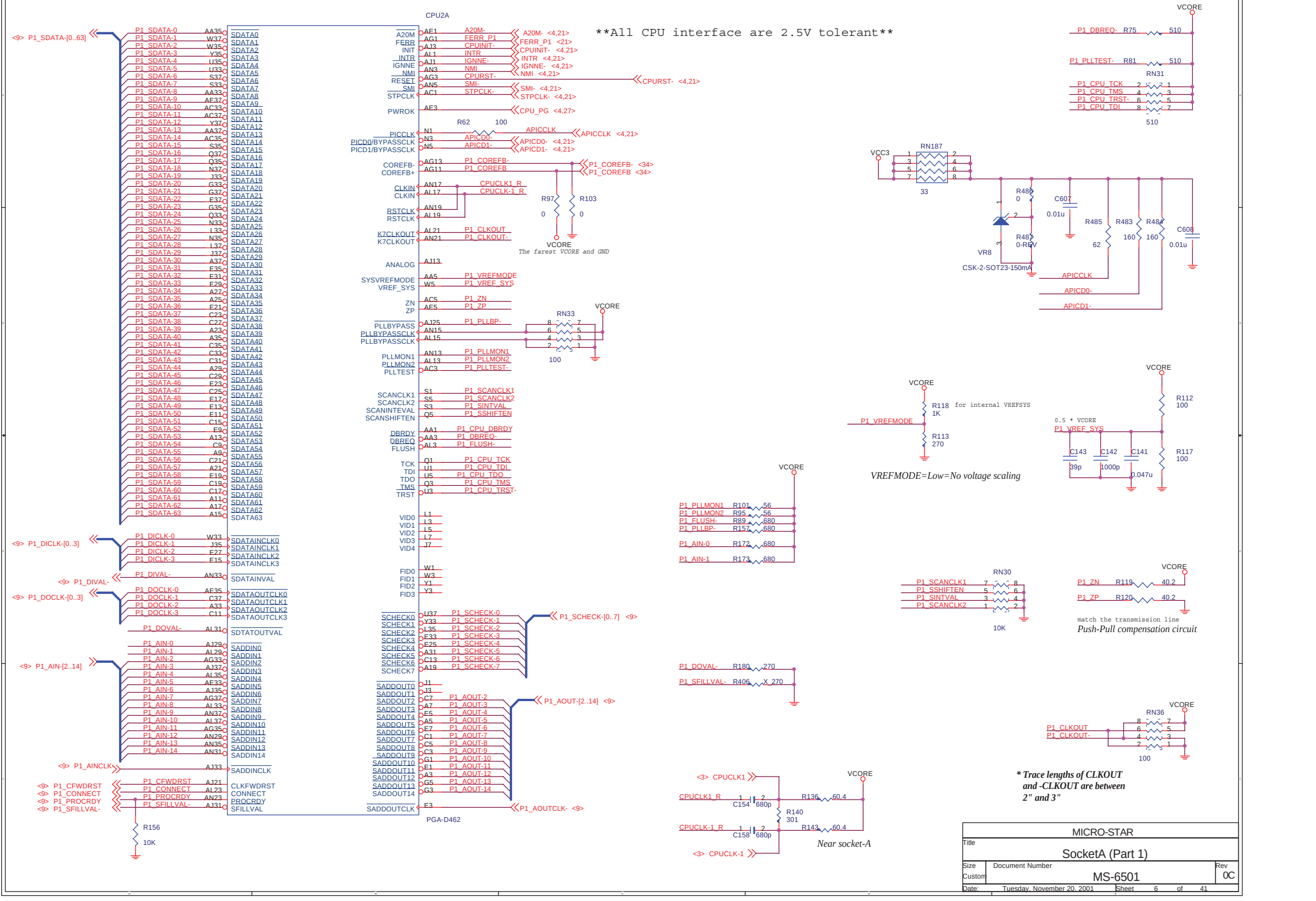
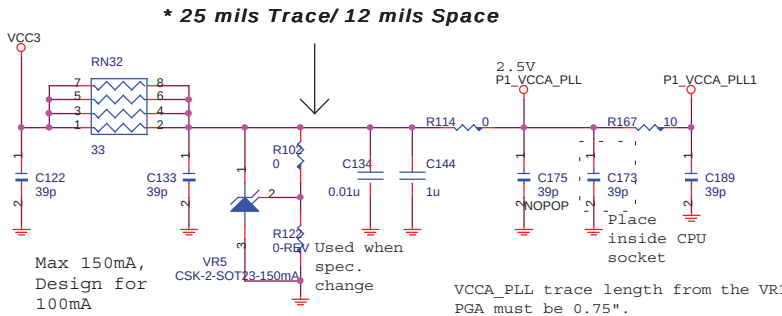

CPU2A
All CPU interface are 2.5V tolerant
PGA-D462
The farest VCORE and GND
Near socket-A
VREFMODE=Low=No voltage scaling
Push-Pull compensation circuit
* Trace lengths of CLKOUT and -CLKOUT are between 2" and 3"
CSK-2-SOT23-150mA
for internal VREFSYS
match the transmission line
MICRO-STAR
SocketA (Part 1)
MS-6501
Size Custom
Document Number
Rev 0C
Date: Tuesday, November 20, 2001
Sheet 6 of 41



VCCA_PLL trace length from the VR1 to the PGA must be 0.75".

Place al filters close to the PGA.

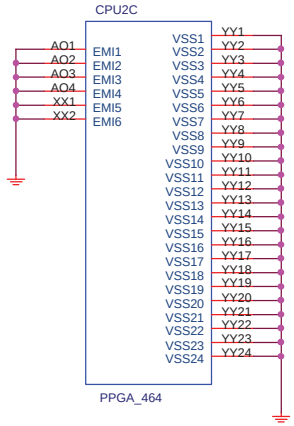
Keep all power and signal trce away from the VR1.

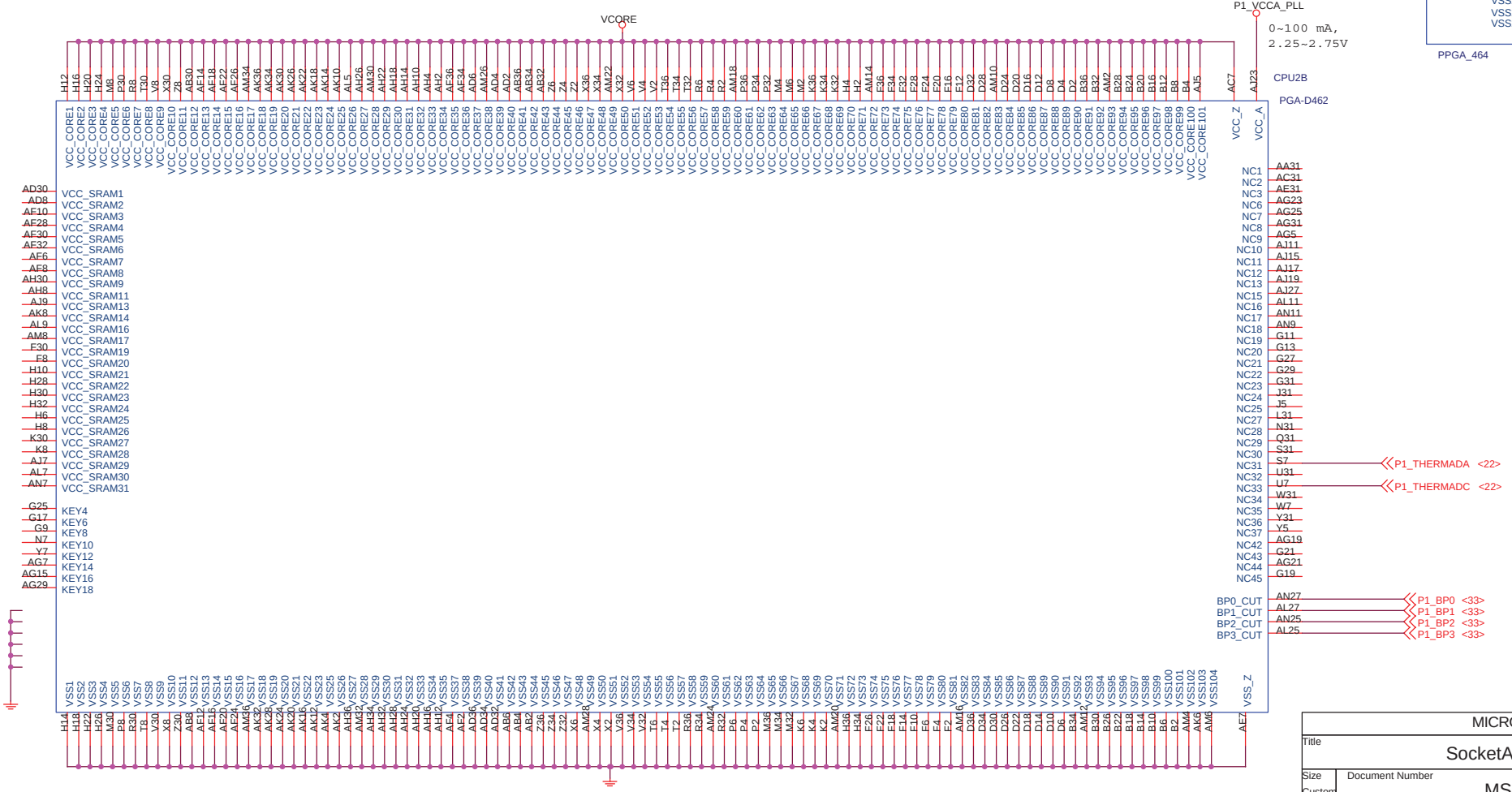
Place a cut in the GND plane around the VCCA_PLL regulator circuit.

Power Up Strappings :

AD[3:0] => CPU Clock Multiplier

0000	*3*	*1000*	*7*
0001	*3.5*	*1001*	*7.5*
0010	*4*	*1010*	*8*
0011	*4.5*	*1011*	*8.5*
0100	*5*	*1100*	*9*
0101	*5.5*	*1101*	*9.5*
0110	*6*	*1110*	*10*
0111	*6.5*	*1111*	*Reserved*





MICRO-STAR			
Title: SocketA (Part 2)			
Size: Custom	Document Number: MS-6501		Rev: 0C
Date: Tuesday, November 20, 2001	Sheet 7 of 41		

AMD-762
System Bus 0

U23A

BELONG TO CLKFWD GROUP[SADDIN] MATCH W/IN +/-50MILS OF GROUP 5/10, CLK:5/20

BELONG TO CLKFWD GROUP[SADDOUT] MATCH W/IN +/-50MILS OF GROUP 5/10, CLK:5/20

BELONG TO CLKFWD GROUP;MATCHED TO INDIVIDUAL CLKFWD GROUP

RESPECTIVELY.[SDATA0], [SDATA1], [SDATA2],[SDATA3] W/IN+/-50MILS OF GROUP

<4> P0_CFWDRST	P0_CFWDRST	AC5	P0_CLKFWDRST
<4> P0_CONNECT	P0_CONNECT	AC4	P0_CONNECT
<4> P0_PROCRDY	P0_PROCRDY	AC6	P0_PROCRDY
<3> CPUCLK2	CPUCLK2	AH20	SYSCLK
<4> P0_AIN-[2..14]	P0_AIN-2	Y4	P0_SADDIN2#
	P0_AIN-3	AA2	P0_SADDIN3#
	P0_AIN-4	AA6	P0_SADDIN4#
	P0_AIN-5	Y5	P0_SADDIN5#
	P0_AIN-6	AA4	P0_SADDIN6#
	P0_AIN-7	AA3	P0_SADDIN7#
	P0_AIN-8	AA5	P0_SADDIN8#
	P0_AIN-9	AB3	P0_SADDIN9#
	P0_AIN-10	AB5	P0_SADDIN10#
	P0_AIN-11	Y6	P0_SADDIN11#
	P0_AIN-12	AD1	P0_SADDIN12#
	P0_AIN-13	AC3	P0_SADDIN13#
	P0_AIN-14	AC1	P0_SADDIN14#
<4> P0_AINCLK-	P0_AINCLK-	AA7	P0_SADDINCLK#
<4> P0_AOUT-[2..14]	P0_AOUT-2	G1	P0_SADDOUT2#
	P0_AOUT-3	H2	P0_SADDOUT3#
	P0_AOUT-4	G3	P0_SADDOUT4#
	P0_AOUT-5	F4	P0_SADDOUT5#
	P0_AOUT-6	H4	P0_SADDOUT6#
	P0_AOUT-7	E1	P0_SADDOUT7#
	P0_AOUT-8	F3	P0_SADDOUT8#
	P0_AOUT-9	F2	P0_SADDOUT9#
	P0_AOUT-10	F5	P0_SADDOUT10#
	P0_AOUT-11	G5	P0_SADDOUT11#
	P0_AOUT-12	F1	P0_SADDOUT12#
	P0_AOUT-13	E2	P0_SADDOUT13#
	P0_AOUT-14	D1	P0_SADDOUT14#
<4> P0_AOUTCLK-	P0_AOUTCLK-	E3	P0_SADDOUTCLK#
<4> P0_SCHECK-[0..7]	P0_SCHECK-0	V7	P0_SCHECK0#
	P0_SCHECK-1	V8	P0_SCHECK1#
	P0_SCHECK-2	P8	P0_SCHECK2#
	P0_SCHECK-3	T1	P0_SCHECK3#
	P0_SCHECK-4	N7	P0_SCHECK4#
	P0_SCHECK-5	N1	P0_SCHECK5#
	P0_SCHECK-6	J3	P0_SCHECK6#
	P0_SCHECK-7	K3	P0_SCHECK7#
<4> P0_DICLK-[0..3]	P0_DICLK-0	U5	P0_SDATAINCLK0#
	P0_DICLK-1	R1	P0_SDATAINCLK1#
	P0_DICLK-2	M1	P0_SDATAINCLK2#
	P0_DICLK-3	H3	P0_SDATAINCLK3#
<4> P0_DIVAL-	P0_DIVAL-	AB1	P0_SDATAINVALID#
<4> P0_DOCLK-[0..3]	P0_DOCLK-0	W5	P0_SDATAOUTCLK0#
	P0_DOCLK-1	R8	P0_SDATAOUTCLK1#
	P0_DOCLK-2	N5	P0_SDATAOUTCLK2#
	P0_DOCLK-3	H1	P0_SDATAOUTCLK3#
<4> P0_SFILLVAL-		J8	P0_SYSFILLVALID#
			P0_VREF AC2 P0_S2K_VREF

P0_SDATA0#	W3	P0_SDATA-0
P0_SDATA1#	V4	P0_SDATA-1
P0_SDATA2#	V3	P0_SDATA-2
P0_SDATA3#	V5	P0_SDATA-3
P0_SDATA4#	V6	P0_SDATA-4
P0_SDATA5#	U4	P0_SDATA-5
P0_SDATA6#	U3	P0_SDATA-6
P0_SDATA7#	U8	P0_SDATA-7
P0_SDATA8#	Y1	P0_SDATA-8
P0_SDATA9#	Y3	P0_SDATA-9
P0_SDATA10#	AA1	P0_SDATA-10
P0_SDATA11#	Y7	P0_SDATA-11
P0_SDATA12#	W1	P0_SDATA-12
P0_SDATA13#	W7	P0_SDATA-13
P0_SDATA14#	Y2	P0_SDATA-14
P0_SDATA15#	U6	P0_SDATA-15
P0_SDATA16#	U7	P0_SDATA-16
P0_SDATA17#	R7	P0_SDATA-17
P0_SDATA18#	R6	P0_SDATA-18
P0_SDATA19#	R5	P0_SDATA-19
P0_SDATA20#	R3	P0_SDATA-20
P0_SDATA21#	R4	P0_SDATA-21
P0_SDATA22#	R2	P0_SDATA-22
P0_SDATA23#	U2	P0_SDATA-23
P0_SDATA24#	T7	P0_SDATA-24
P0_SDATA25#	V1	P0_SDATA-25
P0_SDATA26#	T5	P0_SDATA-26
P0_SDATA27#	V2	P0_SDATA-27
P0_SDATA28#	T3	P0_SDATA-28
P0_SDATA29#	U1	P0_SDATA-29
P0_SDATA30#	P6	P0_SDATA-30
P0_SDATA31#	P1	P0_SDATA-31
P0_SDATA32#	P2	P0_SDATA-32
P0_SDATA33#	P4	P0_SDATA-33
P0_SDATA34#	M8	P0_SDATA-34
P0_SDATA35#	M6	P0_SDATA-35
P0_SDATA36#	L3	P0_SDATA-36
P0_SDATA37#	L7	P0_SDATA-37
P0_SDATA38#	M4	P0_SDATA-38
P0_SDATA39#	L6	P0_SDATA-39
P0_SDATA40#	P7	P0_SDATA-40
P0_SDATA41#	P5	P0_SDATA-41
P0_SDATA42#	N3	P0_SDATA-42
P0_SDATA43#	P3	P0_SDATA-43
P0_SDATA44#	M5	P0_SDATA-44
P0_SDATA45#	M7	P0_SDATA-45
P0_SDATA46#	L5	P0_SDATA-46
P0_SDATA47#	M3	P0_SDATA-47
P0_SDATA48#	K7	P0_SDATA-48
P0_SDATA49#	J6	P0_SDATA-49
P0_SDATA50#	J7	P0_SDATA-50
P0_SDATA51#	K5	P0_SDATA-51
P0_SDATA52#	J4	P0_SDATA-52
P0_SDATA53#	J2	P0_SDATA-53
P0_SDATA54#	H6	P0_SDATA-54
P0_SDATA55#	H5	P0_SDATA-55
P0_SDATA56#	M2	P0_SDATA-56
P0_SDATA57#	L4	P0_SDATA-57
P0_SDATA58#	L2	P0_SDATA-58
P0_SDATA59#	L1	P0_SDATA-59
P0_SDATA60#	K1	P0_SDATA-60
P0_SDATA61#	H7	P0_SDATA-61
P0_SDATA62#	J5	P0_SDATA-62
P0_SDATA63#	J1	P0_SDATA-63

P0_SDATA-[0..63] <4>

AMD-AMD762

VCC2_5
R408 100
CPUCLK2
R410 150

Put these two res. very close to N.B.

U3_X
NB FAN

+12V
NBFAN1
2
1
D1x2-WH

VCORE
R248 100
Set S2K_VREF to 50% of VCORE
P0_S2K_VREF
C265 0.047u
C270 0.039u
R251 100

MICRO-STAR

Title	North Bridge AMD762-CPU0	
Size B	Document Number MS-6501	Rev 0C
Date: Tuesday, November 20, 2001	Sheet 8 of 41	

AMD-762
System Bus 1

U23B

BELONG TO CLKFWD GROUP[SADDIN] MATCH W/IN +/-50MILS OF GROUP 5/10, CLK:5/20

BELONG TO CLKFWD GROUP[SADDOUT] MATCH W/IN +/-50MILS OF GROUP 5/10, CLK:5/20

BELONG TO CLKFWD GROUP;MATCHED TO INDIVIDUAL CLKFWD GROUP

RESPECTIVELY.[SDATA0], [SDATA1], [SDATA2],[SDATA3] W/IN+/-50MILS OF GROUP

<6> P1_CFWDRST — P1_CFWDRST — AL19 — P1_CLKFWDRST
<6> P1_CONNECT — P1_CONNECT — AJ19 — P1_CONNECT
<6> P1_PROCRDY — P1_PROCRDY — AE19 — P1_PROCRDY

<6> P1_AIN-[2..14]

P1_AIN-2	AG17	P1_SADDIN2#
P1_AIN-3	AH18	P1_SADDIN3#
P1_AIN-4	AL18	P1_SADDIN4#
P1_AIN-5	AL17	P1_SADDIN5#
P1_AIN-6	AF17	P1_SADDIN6#
P1_AIN-7	AG16	P1_SADDIN7#
P1_AIN-8	AG18	P1_SADDIN8#
P1_AIN-9	AD17	P1_SADDIN9#
P1_AIN-10	AK18	P1_SADDIN10#
P1_AIN-11	AK17	P1_SADDIN11#
P1_AIN-12	AG19	P1_SADDIN12#
P1_AIN-13	AE18	P1_SADDIN13#
P1_AIN-14	AF18	P1_SADDIN14#

<6> P1_AINCLK- — P1_AINCLK- — AJ18 — P1_SADDINCLK#

<6> P1_AOUT-[2..14]

P1_AOUT-2	AJ2	P1_SADDOUT2#
P1_AOUT-3	AK3	P1_SADDOUT3#
P1_AOUT-4	AE3	P1_SADDOUT4#
P1_AOUT-5	AG3	P1_SADDOUT5#
P1_AOUT-6	AF3	P1_SADDOUT6#
P1_AOUT-7	AD7	P1_SADDOUT7#
P1_AOUT-8	AJ3	P1_SADDOUT8#
P1_AOUT-9	AF2	P1_SADDOUT9#
P1_AOUT-10	AD5	P1_SADDOUT10#
P1_AOUT-11	AD6	P1_SADDOUT11#
P1_AOUT-12	AF1	P1_SADDOUT12#
P1_AOUT-13	AH1	P1_SADDOUT13#
P1_AOUT-14	AG2	P1_SADDOUT14#

<6> P1_AOUTCLK- — P1_AOUTCLK- — AG1 — P1_SADDOUTCLK#

<6> P1_SCHECK-[0..7]

P1_SCHECK-0	AG14	P1_SCHECK0#
P1_SCHECK-1	AL15	P1_SCHECK1#
P1_SCHECK-2	AH12	P1_SCHECK2#
P1_SCHECK-3	AJ10	P1_SCHECK3#
P1_SCHECK-4	AL9	P1_SCHECK4#
P1_SCHECK-5	AG8	P1_SCHECK5#
P1_SCHECK-6	AF6	P1_SCHECK6#
P1_SCHECK-7	AL7	P1_SCHECK7#

<6> P1_DICLK-[0..3]

P1_DICLK-0	AE15	P1_SDATAINCLK0#
P1_DICLK-1	AD12	P1_SDATAINCLK1#
P1_DICLK-2	AJ8	P1_SDATAINCLK2#
P1_DICLK-3	AK5	P1_SDATAINCLK3#

<6> P1_DIVAL- — P1_DIVAL- — AE17 — P1_SDATAINVALID#

<6> P1_DOCLK-[0..3]

P1_DOCLK-0	AH15	P1_SDATAOUTCLK0#
P1_DOCLK-1	AH11	P1_SDATAOUTCLK1#
P1_DOCLK-2	AG9	P1_SDATAOUTCLK2#
P1_DOCLK-3	AJ4	P1_SDATAOUTCLK3#

<6> P1_SFILLVAL- — P1_SFILLVAL- — AL20 — P1_SYSFILLVALID#

P1_SDATA0#	AE14	P1_SDATA-0
P1_SDATA1#	AJ14	P1_SDATA-1
P1_SDATA2#	AE16	P1_SDATA-2
P1_SDATA3#	AD14	P1_SDATA-3
P1_SDATA4#	AJ15	P1_SDATA-4
P1_SDATA5#	AL14	P1_SDATA-5
P1_SDATA6#	AK15	P1_SDATA-6
P1_SDATA7#	AE13	P1_SDATA-7
P1_SDATA8#	AL16	P1_SDATA-8
P1_SDATA9#	AD15	P1_SDATA-9
P1_SDATA10#	AG15	P1_SDATA-10
P1_SDATA11#	AF15	P1_SDATA-11
P1_SDATA12#	AJ16	P1_SDATA-12
P1_SDATA13#	AH17	P1_SDATA-13
P1_SDATA14#	AJ17	P1_SDATA-14
P1_SDATA15#	AH14	P1_SDATA-15
P1_SDATA16#	AF14	P1_SDATA-16
P1_SDATA17#	AE12	P1_SDATA-17
P1_SDATA18#	AF12	P1_SDATA-18
P1_SDATA19#	AK12	P1_SDATA-19
P1_SDATA20#	AJ11	P1_SDATA-20
P1_SDATA21#	AE11	P1_SDATA-21
P1_SDATA22#	AG11	P1_SDATA-22
P1_SDATA23#	AF11	P1_SDATA-23
P1_SDATA24#	AK14	P1_SDATA-24
P1_SDATA25#	AL13	P1_SDATA-25
P1_SDATA26#	AL12	P1_SDATA-26
P1_SDATA27#	AG13	P1_SDATA-27
P1_SDATA28#	AJ13	P1_SDATA-28
P1_SDATA29#	AG12	P1_SDATA-29
P1_SDATA30#	AJ12	P1_SDATA-30
P1_SDATA31#	AL11	P1_SDATA-31
P1_SDATA32#	AG7	P1_SDATA-32
P1_SDATA33#	AF9	P1_SDATA-33
P1_SDATA34#	AK11	P1_SDATA-34
P1_SDATA35#	AL10	P1_SDATA-35
P1_SDATA36#	AK8	P1_SDATA-36
P1_SDATA37#	AL8	P1_SDATA-37
P1_SDATA38#	AH8	P1_SDATA-38
P1_SDATA39#	AK9	P1_SDATA-39
P1_SDATA40#	AE10	P1_SDATA-40
P1_SDATA41#	AE9	P1_SDATA-41
P1_SDATA42#	AD11	P1_SDATA-42
P1_SDATA43#	AG10	P1_SDATA-43
P1_SDATA44#	AJ9	P1_SDATA-44
P1_SDATA45#	AH9	P1_SDATA-45
P1_SDATA46#	AF8	P1_SDATA-46
P1_SDATA47#	AJ7	P1_SDATA-47
P1_SDATA48#	AF4	P1_SDATA-48
P1_SDATA49#	AG5	P1_SDATA-49
P1_SDATA50#	AF5	P1_SDATA-50
P1_SDATA51#	AK6	P1_SDATA-51
P1_SDATA52#	AH4	P1_SDATA-52
P1_SDATA53#	AJ5	P1_SDATA-53
P1_SDATA54#	AL4	P1_SDATA-54
P1_SDATA55#	AH3	P1_SDATA-55
P1_SDATA56#	AE8	P1_SDATA-56
P1_SDATA57#	AE7	P1_SDATA-57
P1_SDATA58#	AG6	P1_SDATA-58
P1_SDATA59#	AL6	P1_SDATA-59
P1_SDATA60#	AJ6	P1_SDATA-60
P1_SDATA61#	AE5	P1_SDATA-61
P1_SDATA62#	AH6	P1_SDATA-62
P1_SDATA63#	AL5	P1_SDATA-63

P1_SDATA-[0..63] <6>

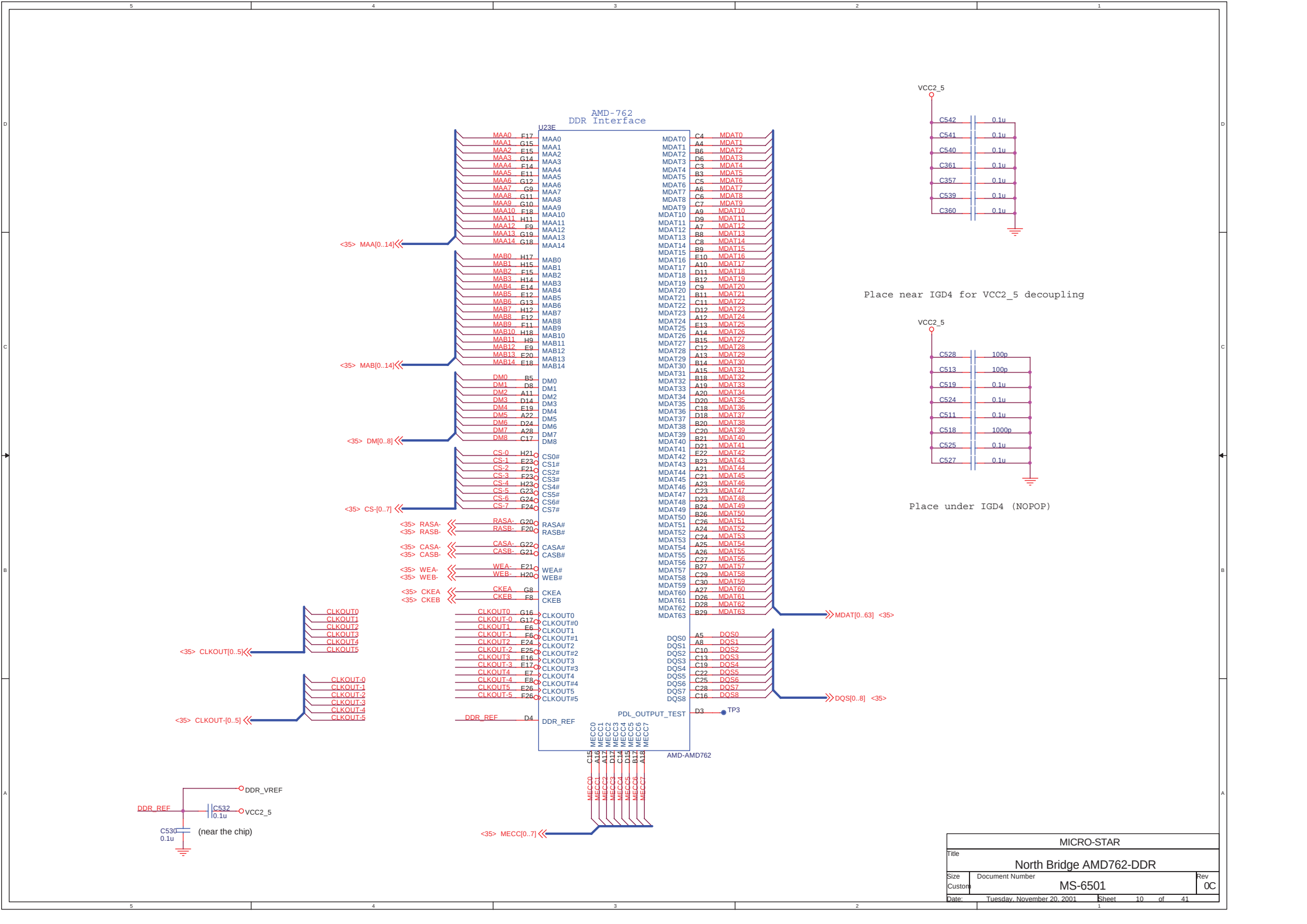
P1_VREF — AB7 — P1_S2K_VREF

AMD-AMD762

Set S2K_VREF to 50% of VCORE

VCORE
R242 100
P1_S2K_VREF
C261 0.047u
C250 0.039u
R244 100

MICRO-STAR		
Title: North Bridge AMD762-CPU1		
Size: B	Document Number: MS-6501	Rev: 0C
Date: Tuesday, November 20, 2001	Sheet 9 of 41	


AMD-762
DDR Interface
U23E
MAA0 F17
MAA1 G15
MAA2 E15
MAA3 G14
MAA4 F14
MAA5 E11
MAA6 G12
MAA7 G9
MAA8 G11
MAA9 G10
MAA10 F18
MAA11 H11
MAA12 F9
MAA13 G19
MAA14 G18
<35> MAA[0..14]
MAB0 H17
MAB1 H15
MAB2 F15
MAB3 H14
MAB4 E14
MAB5 E12
MAB6 G13
MAB7 H12
MAB8 F12
MAB9 F11
MAB10 H18
MAB11 H9
MAB12 E9
MAB13 E20
MAB14 E18
<35> MAB[0..14]
DM0 B5
DM1 D8
DM2 A11
DM3 D14
DM4 E19
DM5 A22
DM6 D24
DM7 A28
DM8 C17
<35> DM[0..8]
CS-0 H21
CS-1 E23
CS-2 F21
CS-3 F23
CS-4 H23
CS-5 G23
CS-6 G24
CS-7 F24
<35> CS-[0..7]
<35> RASA-
<35> RASB-
RASA- G20
RASB- F20
<35> CASA-
<35> CASB-
CASA- G22
CASB- G21
<35> WEA-
<35> WEB-
WEA- F21
WEB- H20
<35> CKEA
<35> CKEB
CKEA G8
CKEB F8
CLKOUT0 G16
CLKOUT-0 G17
CLKOUT1 E6
CLKOUT-1 F6
CLKOUT2 E24
CLKOUT-2 E25
CLKOUT3 E16
CLKOUT-3 E17
CLKOUT4 E7
CLKOUT-4 E8
CLKOUT5 E26
CLKOUT-5 E26
DDR_REF D4
MDAT0 C4
MDAT1 A4
MDAT2 B6
MDAT3 D6
MDAT4 C3
MDAT5 B3
MDAT6 C5
MDAT7 A6
MDAT8 C6
MDAT9 C7
MDAT10 A9
MDAT11 D9
MDAT12 A7
MDAT13 B8
MDAT14 C8
MDAT15 B9
MDAT16 E10
MDAT17 A10
MDAT18 D11
MDAT19 B12
MDAT20 C9
MDAT21 B11
MDAT22 C11
MDAT23 D12
MDAT24 A12
MDAT25 E13
MDAT26 A14
MDAT27 B15
MDAT28 C12
MDAT29 A13
MDAT30 B14
MDAT31 A15
MDAT32 B18
MDAT33 A19
MDAT34 A20
MDAT35 D20
MDAT36 C18
MDAT37 D18
MDAT38 B20
MDAT39 C20
MDAT40 B21
MDAT41 D21
MDAT42 E22
MDAT43 B23
MDAT44 A21
MDAT45 C21
MDAT46 A23
MDAT47 C23
MDAT48 D23
MDAT49 B24
MDAT50 B26
MDAT51 C26
MDAT52 A24
MDAT53 C24
MDAT54 A25
MDAT55 A26
MDAT56 C27
MDAT57 B27
MDAT58 C29
MDAT59 C30
MDAT60 A27
MDAT61 D26
MDAT62 D28
MDAT63 B29
MDAT[0..63] <35>
DQS0 A5
DQS1 A8
DQS2 C10
DQS3 C13
DQS4 C19
DQS5 C22
DQS6 C25
DQS7 C28
DQS8 C16
DQS[0..8] <35>
PDL_OUTPUT_TEST D3
TP3
AMD-AMD762
MECC0 C15
MECC1 A16
MECC2 A17
MECC3 D17
MECC4 C14
MECC5 D15
MECC6 B17
MECC7 A18
<35> MECC[0..7]
CLKOUT0
CLKOUT1
CLKOUT2
CLKOUT3
CLKOUT4
CLKOUT5
<35> CLKOUT[0..5]
CLKOUT-0
CLKOUT-1
CLKOUT-2
CLKOUT-3
CLKOUT-4
CLKOUT-5
<35> CLKOUT-[0..5]
DDR_VREF
DDR_REF
C532
0.1u
VCC2_5
C530
0.1u
(near the chip)
VCC2_5
C542 0.1u
C541 0.1u
C540 0.1u
C361 0.1u
C357 0.1u
C539 0.1u
C360 0.1u
Place near IGD4 for VCC2_5 decoupling
VCC2_5
C528 100p
C513 100p
C519 0.1u
C524 0.1u
C511 0.1u
C518 1000p
C525 0.1u
C527 0.1u
Place under IGD4 (NOPOP)
MICRO-STAR
Title
North Bridge AMD762-DDR
Size
Custom
Document Number
MS-6501
Rev
0C
Date: Tuesday, November 20, 2001
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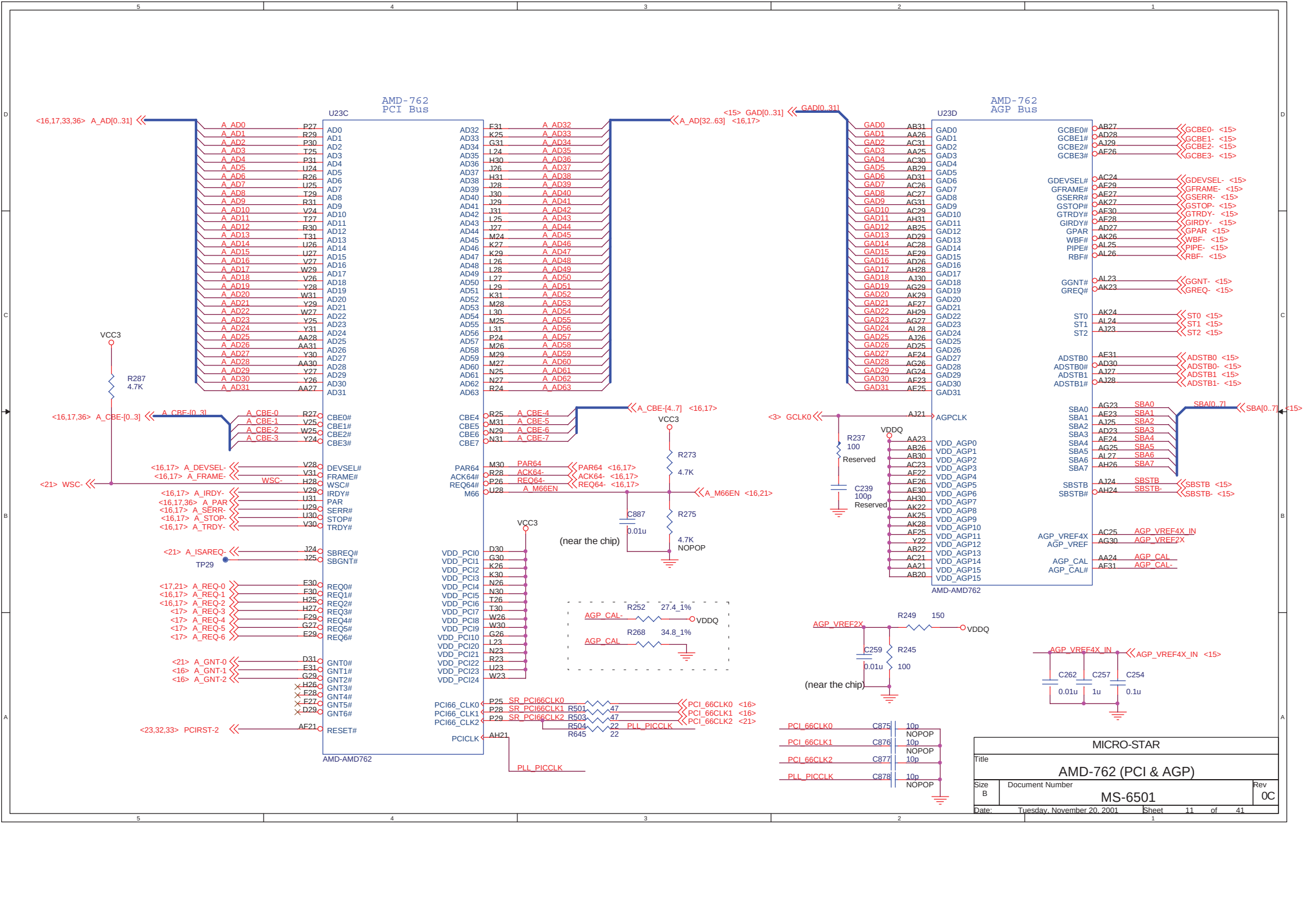
AMD-762
PCI Bus
U23C
AMD-AMD762
AMD-762
AGP Bus
U23D
AMD-AMD762
MICRO-STAR
AMD-762 (PCI & AGP)
MS-6501
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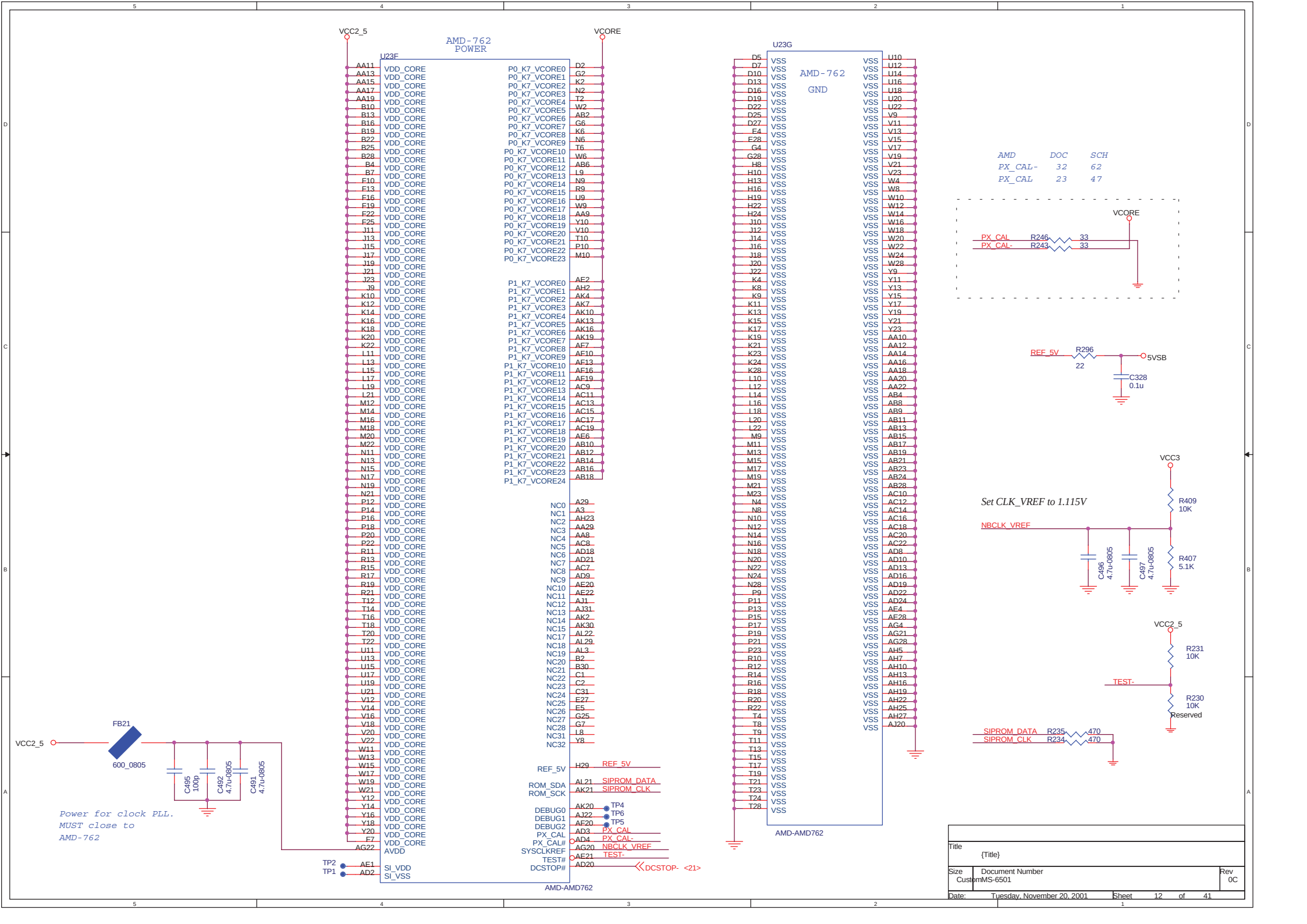
AMD-762
POWER
U23F
VCC2_5
VCORE
AMD-AMD762
U23G
AMD-762
GND
AMD-AMD762
AMD DOC SCH
PX_CAL- 32 62
PX_CAL 23 47
PX_CAL
PX_CAL-
R246
R243
33
33
REF_5V
R296
22
5VSB
C328
0.1u
VCC3
Set CLK_VREF to 1.115V
NBCLK_VREF
R409
10K
R407
5.1K
C496
4.7u-0805
C497
4.7u-0805
VCC2_5
R231
10K
TEST-
R230
10K
Reserved
SIPROM_DATA
SIPROM_CLK
R235
R234
470
470
FB21
600_0805
C495
100p
C492
4.7u-0805
C491
4.7u-0805
Power for clock PLL.
MUST close to
AMD-762
TP2
TP1
SI_VDD
SI_VSS
REF_5V
ROM_SDA
ROM_SCK
DEBUG0
DEBUG1
DEBUG2
PX_CAL
PX_CAL#
SYSCLKREF
TEST#
DCSTOP#
TP4
TP6
TP5
DCSTOP- <21>
Title
{Title}
Size
CustomMS-6501
Document Number
Rev
0C
Date:
Tuesday, November 20, 2001
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12
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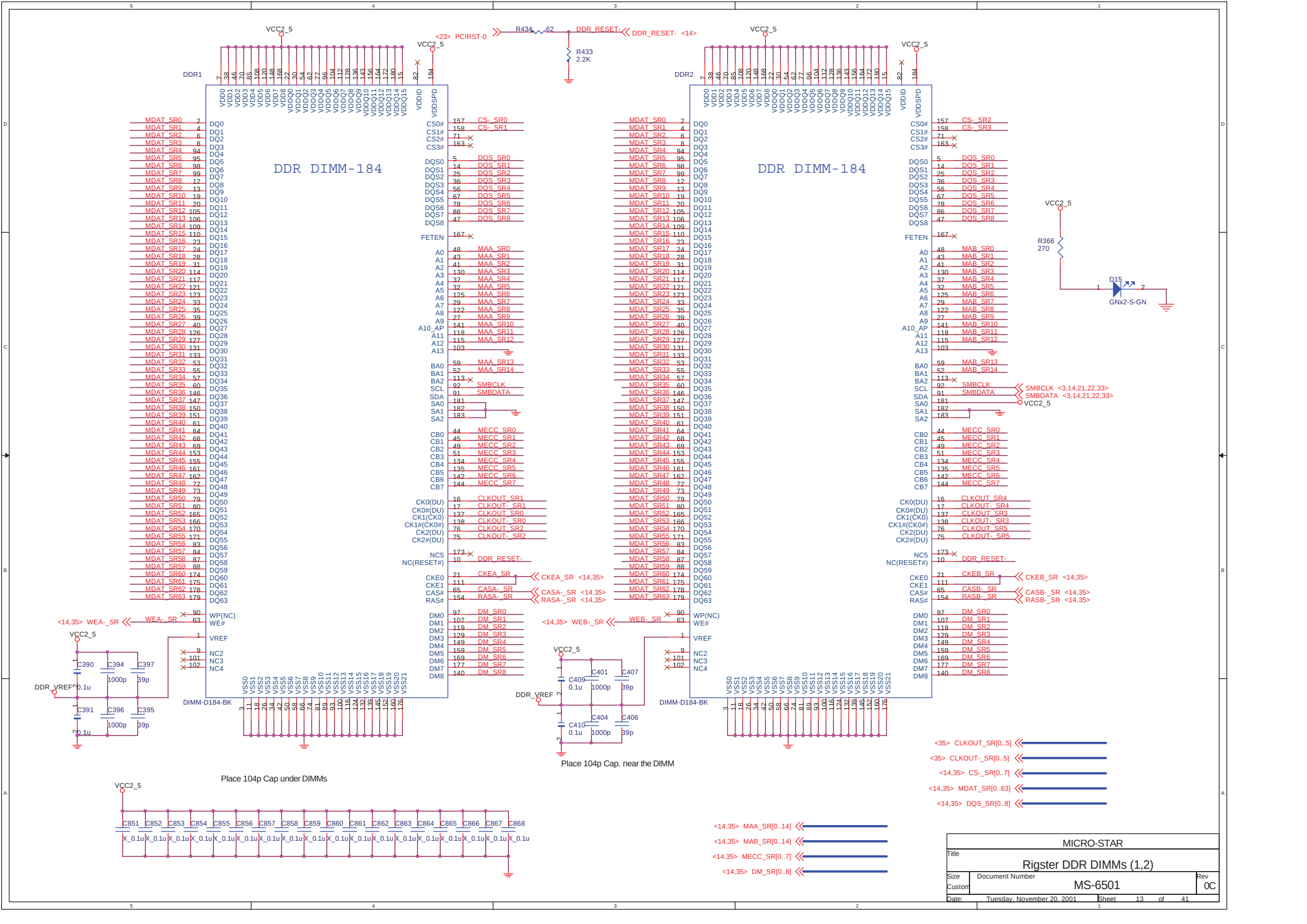
41



MICRO-STAR		
Title	Rigster DDR DIMMs (1,2)	
Size: Custom	Document Number: MS-6501	Rev: 0C
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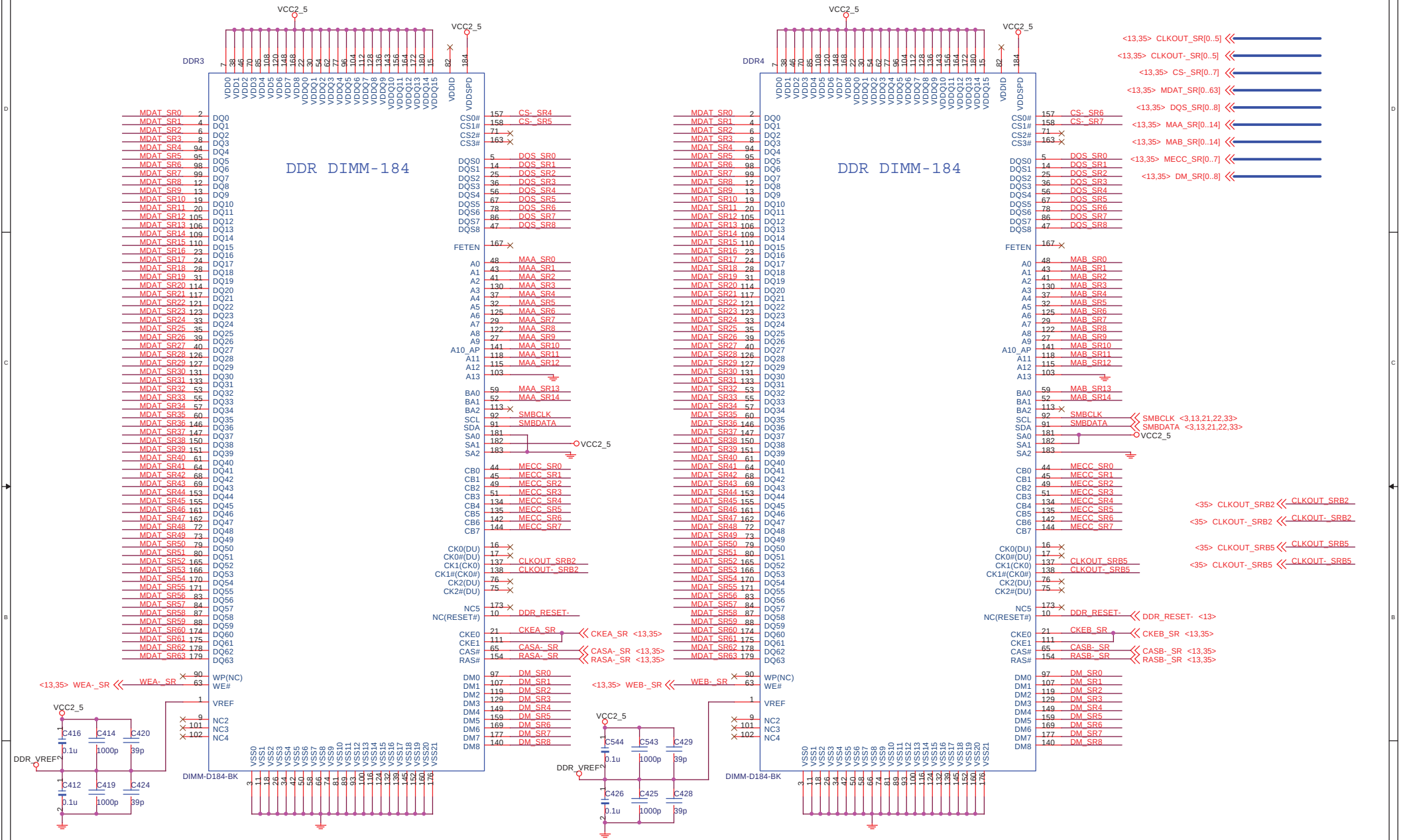
DDR3
DDR4
DDR DIMM-184
VCC2_5
DIMM-D184-BK
Place 104p Cap. near the DIMM
MICRO-STAR
Rigster DDR DIMMs (3,4)
MS-6501
0C
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AGP Pro Connector

AGP Pro Imax
VCC3 7.6A
VCC12 9.2A

AGP1-1
AGP LABEL

<11> GAD[0..31] GAD[0..31]
<11> SBA[0..7] SBA[0..7]

AGP1

D1	VCC3_3_J	VCC3_3_A	C1
D2	VCC3_3_K	GND_A	C2
D3	VCC3_3_L	VCC3_3_B	C3
D4	VCC3_3_M	GND_B	C4
D5	VCC3_3_N	GND_C	C5
D6	VCC3_3_O	GND_D	C6
D7	VCC3_3_P	GND_E	C7
D8	VCC3_3_Q	GND_F	C8
D9	PRSNT#2	RESV_A	C9
D10	PRSNT#1	RESV_B	C10
	KEY		
B1	AGP_OVRCNT#	VCC_12V_A	A1
B2	5V_A	TYPEDET#	A2
B3	5V_B	RESV_C	A3
B4	AGP_USB+	AGP_USB-	A4
B5	GND_Q	GND_G	A5
B6	INTB#	INTA#	A6
B7	AGPCLK_CONN	RST#	A7
B8	REQ#	GNT#	A8
B9	VCC3_3_R	VCC3_3_E	A9
B10	ST0	ST1	A10
B11	ST2	RESV_D	A11
B12	RBF#	PIPE#	A12
B13	GND_R	GND_H	A13
B14	RESV_L	WBF#	A14
B15	SBA0	SBA1	A15
B16	VCC3_3_S	VCC3_3_F	A16
B17	SBA2	SBA3	A17
B18	SB_STB	SB_STB#	A18
B19	GND_S	GND_I	A19
B20	SBA4	SBA5	A20
B21	SBA6	SBA7	A21
B22	RESV_M	RESV_E	A22
B23	GND_T	GND_J	A23
B24	3_3AUX_1	RESV_F	A24
B25	VCC3_3_T	VCC3_3_G	A25
B26	GAD31	GAD30	A26
B27	GAD29	GAD28	A27
B28	VCC3_3_U	VCC3_3_H	A28
B29	GAD27	GAD26	A29
B30	GAD25	GAD24	A30
B31	GND_U	GND_K	A31
B32	AD_STB1	AD_STB1#	A32
B33	GAD23	C/BE#3	A33
B34	VDDQ_F	VDDQ_A	A34
B35	GAD21	GAD22	A35
B36	GAD19	GAD20	A36
B37	GND_V	GND_L	A37
B38	GAD17	GAD18	A38
B39	C/BE#2	GAD16	A39
B40	VDDQ_G	VDDQ_B	A40
B41	IRDY#	FRAME#	A41
B42	3_3AUX_2	RESV_G	A42
B43	GND_W	GND_M	A43
B44	RESV_N	RESV_H	A44
B45	VCC3_3_V	VCC3_3_I	A45
B46	DEVSEL#	TRDY#	A46
B47	VDDQ_H	STOP#	A47
B48	PERR#	PME#	A48
B49	GND_X	GND_N	A49
B50	SERR#	PAR	A50
B51	C/BE#1	GAD15	A51
B52	VDDQ_I	VDDQ_C	A52
B53	GAD14	GAD13	A53
B54	GAD12	GAD11	A54
B55	GND_Y	GND_O	A55
B56	GAD10	GAD9	A56
B57	GAD8	C/BE#0	A57
B58	VDDQ_J	VDDQ_D	A58
B59	AD_STB0	AD_STB0#	A59
B60	GAD7	GAD6	A60
B61	GND_Z	GND_P	A61
B62	GAD5	GAD4	A62
B63	GAD3	GAD2	A63
B64	VDDQ_K	VDDQ_E	A64
B65	GAD1	GAD0	A65
B66	VREFCG	VREFGC	A66
	KEY		
F1	RESV_O	RESV_I	E1
F2	RESV_P	RESV_J	E2
F3	GND_AA	VCC_12V_B	E3
F4	GND_BB	VCC_12V_C	E4
F5	GND_CC	VCC_12V_D	E5
F6	GND_DD	VCC_12V_E	E6
F7	GND_EE	VCC_12V_F	E7
F8	GND_FF	VCC_12V_G	E8
F9	GND_GG	VCC_12V_H	E9
F10	GND_HH	VCC_12V_I	E10
F11	GND_II	VCC_12V_J	E11
F12	GND_JJ	VCC_12V_K	E12
F13	GND_KK	VCC_12V_L	E13
F14	GND_LL	VCC_12V_M	E14

CARD-D180

<18,19,21> PIRQC-
<3> GCLK1
<11> GREQ-
<11> ST0
<11> ST2
<11> RBF-
<11> SBSTB
<11> ADSTB1
<11> GCBE2-
<11> GIRDY-
<11> GDEVSEL-
<11> GSERR-
<11> GCBE1-
<11> ADSTB0

GREQ- ST0 ST2 RBF- SBA0 SBA2 SBA4 SBA6 3VDUAL GAD31 GAD29 GAD27 GAD25 GAD23 GAD21 GAD19 GAD17 GCBE2- GIRDY- GDEVSEL- GPERR- GSERR- GCBE1- GAD14 GAD12 GAD10 GAD8 GAD7 GAD5 GAD3 GAD1 VREF4X_OUT

TYPEDET- PIRQB- <18,19,21,32> PCIRST-1 <16,18,19,22,23,26> GGNT- <11> ST1 <11> PIPE- <11> WBF- <11> SBA1 SBA3 SBA5 SBA7 GAD30 GAD28 GAD26 GAD24 GAD22 GAD20 GAD18 GAD16 GFRAME- <11> GTRDY- <11> GSTOP- <11> PME- <18,19,21,32> GPAR <11> GAD15 GAD13 GAD11 GAD9 GCBE0- <11> GAD6 GAD4 GAD2 GAD0 AGP_VREF4X_IN <11>

TYPEDET- <36> SBSTB- <11> ADSTB1- <11> GCBE3- <11> ADSTB0- <11>

Near the AGP connector

RN35 8.2K: WBF- RBF- PIPE- GREQ-
RN42 8.2K: GDEVSEL- GTRDY- GIRDY- GFRAME-
RN44 8.2K: GSERR- GPAR GPERR- GSTOP-
RN37 8.2K: SBA2 SBA0 SBA3 SBA1
RN41 8.2K: SBA6 SBA4 SBA7 SBA5

ADSTB0 R229 8.2K
ADSTB1 R208 8.2K
SBSTB R170 8.2K
ADSTB0- R239 8.2K
ADSTB1- R196 8.2K
SBSTB- R159 8.2K

+12V C904 VDDQ
4.7u-0805

VDDQ C888 106P
VDDQ C889 106P
Near EC34
Near EC63

VCC3
EC18 1000u/6.3V
EC95 1000u/6.3V
EC96 1000u/6.3V

VDDQ
EC63 1000u/6.3V
EC34 2200u/6.3V
EC29 1000u/6.3V
R163 2.55K-1%
Q40 N-IPD20N03L-S-TO252
C879 1000p
R164 1K +12V
VR4 LCSK-1_SOT23-3L-100mA
C178 X_0.1u
VCC3
C224 0.1u
EC25 1000u/6.3V
R90 1K
R166 10K-1%
TYPEDET-
R96 4.7K
Q19 NPN-3904LT1-S-SOT23

+12V
C299 0.1u
EC37 470u

+12V
J4 D2x2
C590 4.7u-1206
C589 4.7u-1206

VDDQ
C280 560p
R258 1K
R255 75
VREF4X_OUT
C587 0.1u NOPOP
R263 1K
R260 75
C292 560p
Place close to N/B

TYPEDET#	VDDQ
Low	1.5V
High	3.3V

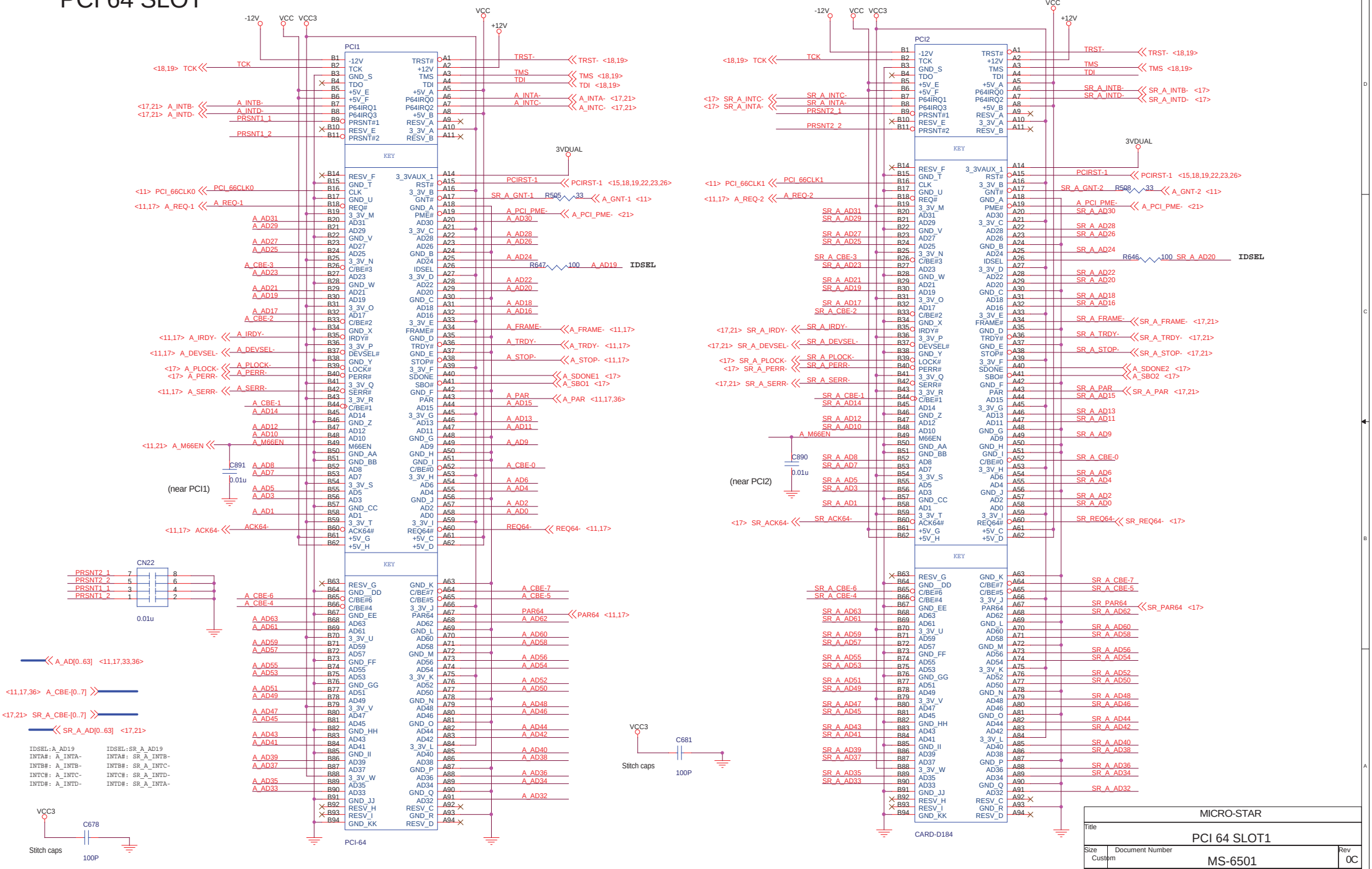
MICRO-STAR

Title: AGP PRO CONNECTOR

Size: Custom | Document Number: MS-6501 | Rev: 0C

Date: Tuesday, November 20, 2001 | Sheet 15 of 41

PCI 64 SLOT


PCI1
PCI2
PCI-64
CARD-D184
CN22
(near PCI1)
(near PCI2)
-12V
VCC
VCC3
+12V
3VDUAL
KEY
IDSEL
R647 100 A_AD19
R646 100 SR_A_AD20
R505 33 SR_A_GNT-1
R508 33 SR_A_GNT-2
C891 0.01u
C890 0.01u
C678 100P
C681 100P
Stitch caps
IDSEL:A_AD19
INTA#: A_INTA-
INTB#: A_INTB-
INTC#: A_INTC-
INTD#: A_INTD-
IDSEL:SR_A_AD19
INTA#: SR_A_INTB-
INTB#: SR_A_INTC-
INTC#: SR_A_INTD-
INTD#: SR_A_INTA-
MICRO-STAR
PCI 64 SLOT1
MS-6501
Custom
0C
Tuesday, November 20, 2001
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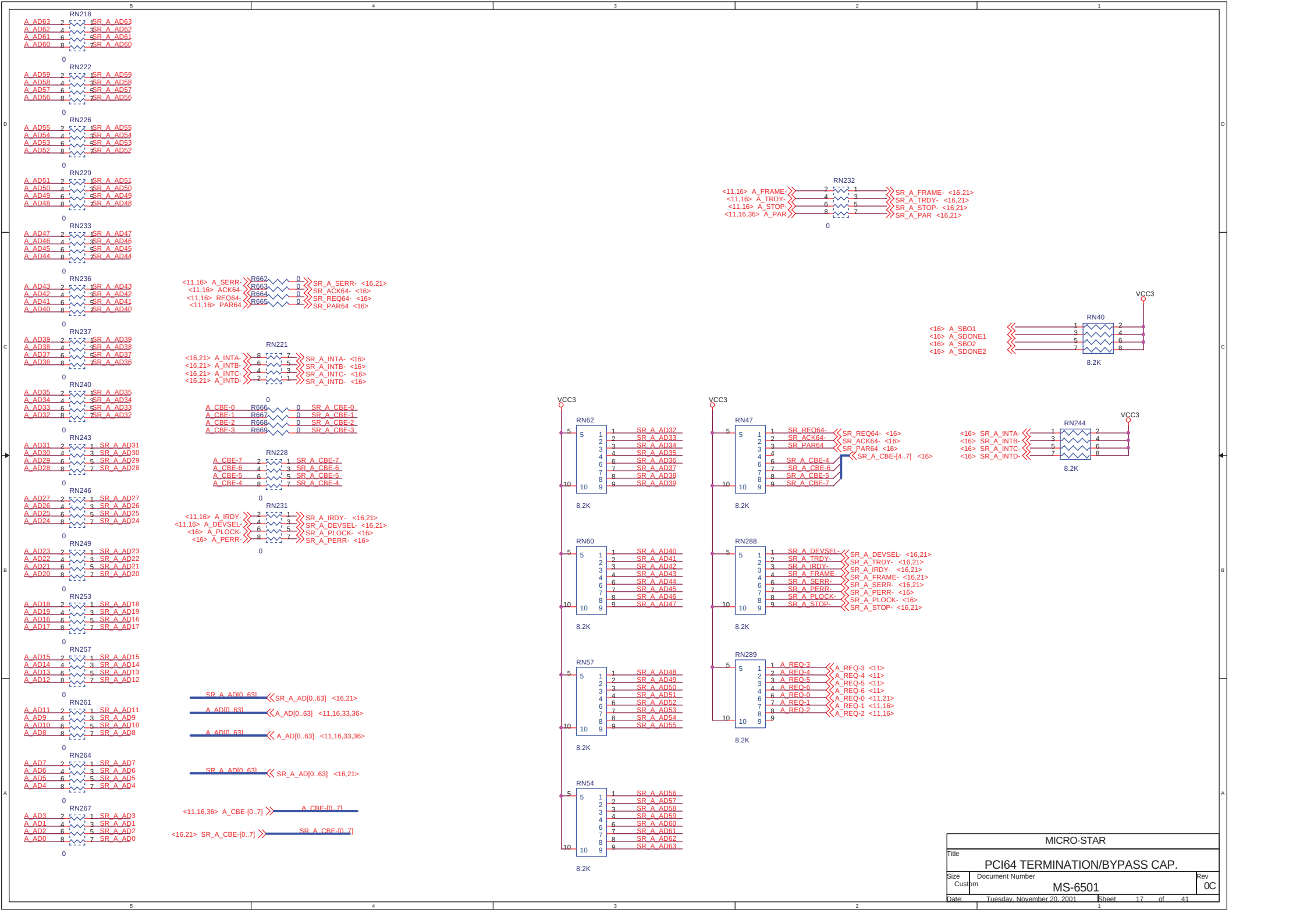
RN218
A_AD63 SR_A_AD63
A_AD62 SR_A_AD62
A_AD61 SR_A_AD61
A_AD60 SR_A_AD60
RN222
A_AD59 SR_A_AD59
A_AD58 SR_A_AD58
A_AD57 SR_A_AD57
A_AD56 SR_A_AD56
RN226
A_AD55 SR_A_AD55
A_AD54 SR_A_AD54
A_AD53 SR_A_AD53
A_AD52 SR_A_AD52
RN229
A_AD51 SR_A_AD51
A_AD50 SR_A_AD50
A_AD49 SR_A_AD49
A_AD48 SR_A_AD48
RN233
A_AD47 SR_A_AD47
A_AD46 SR_A_AD46
A_AD45 SR_A_AD45
A_AD44 SR_A_AD44
RN236
A_AD43 SR_A_AD43
A_AD42 SR_A_AD42
A_AD41 SR_A_AD41
A_AD40 SR_A_AD40
RN237
A_AD39 SR_A_AD39
A_AD38 SR_A_AD38
A_AD37 SR_A_AD37
A_AD36 SR_A_AD36
RN240
A_AD35 SR_A_AD35
A_AD34 SR_A_AD34
A_AD33 SR_A_AD33
A_AD32 SR_A_AD32
RN243
A_AD31 SR_A_AD31
A_AD30 SR_A_AD30
A_AD29 SR_A_AD29
A_AD28 SR_A_AD28
RN246
A_AD27 SR_A_AD27
A_AD26 SR_A_AD26
A_AD25 SR_A_AD25
A_AD24 SR_A_AD24
RN249
A_AD23 SR_A_AD23
A_AD22 SR_A_AD22
A_AD21 SR_A_AD21
A_AD20 SR_A_AD20
RN253
A_AD18 SR_A_AD18
A_AD19 SR_A_AD19
A_AD16 SR_A_AD16
A_AD17 SR_A_AD17
RN257
A_AD15 SR_A_AD15
A_AD14 SR_A_AD14
A_AD13 SR_A_AD13
A_AD12 SR_A_AD12
RN261
A_AD11 SR_A_AD11
A_AD9 SR_A_AD9
A_AD10 SR_A_AD10
A_AD8 SR_A_AD8
RN264
A_AD7 SR_A_AD7
A_AD6 SR_A_AD6
A_AD5 SR_A_AD5
A_AD4 SR_A_AD4
RN267
A_AD3 SR_A_AD3
A_AD1 SR_A_AD1
A_AD2 SR_A_AD2
A_AD0 SR_A_AD0
<11,16> A_SERR- R662 0 SR_A_SERR- <16,21>
<11,16> ACK64- R663 0 SR_ACK64- <16>
<11,16> REQ64- R664 0 SR_REQ64- <16>
<11,16> PAR64 R665 0 SR_PAR64 <16>
RN221
<16,21> A_INTA-
<16,21> A_INTB-
<16,21> A_INTC-
<16,21> A_INTD-
SR_A_INTA- <16>
SR_A_INTB- <16>
SR_A_INTC- <16>
SR_A_INTD- <16>
A_CBE-0 R666 0 SR_A_CBE-0
A_CBE-1 R667 0 SR_A_CBE-1
A_CBE-2 R668 0 SR_A_CBE-2
A_CBE-3 R669 0 SR_A_CBE-3
RN228
A_CBE-7 SR_A_CBE-7
A_CBE-6 SR_A_CBE-6
A_CBE-5 SR_A_CBE-5
A_CBE-4 SR_A_CBE-4
RN231
<11,16> A_IRDY- SR_A_IRDY- <16,21>
<11,16> A_DEVSEL- SR_A_DEVSEL- <16,21>
<16> A_PLOCK- SR_A_PLOCK- <16>
<16> A_PERR- SR_A_PERR- <16>
SR_A_AD[0..63] SR_A_AD[0..63] <16,21>
A_AD[0..63] A_AD[0..63] <11,16,33,36>
A_AD[0..63] A_AD[0..63] <11,16,33,36>
SR_A_AD[0..63] SR_A_AD[0..63] <16,21>
<11,16,36> A_CBE-[0..7] A_CBE-[0..7]
<16,21> SR_A_CBE-[0..7] SR_A_CBE-[0..7]
RN232
<11,16> A_FRAME-
<11,16> A_TRDY-
<11,16> A_STOP-
<11,16,36> A_PAR
SR_A_FRAME- <16,21>
SR_A_TRDY- <16,21>
SR_A_STOP- <16,21>
SR_A_PAR <16,21>
VCC3
RN40
<16> A_SBO1
<16> A_SDONE1
<16> A_SBO2
<16> A_SDONE2
8.2K
RN62
SR_A_AD32
SR_A_AD33
SR_A_AD34
SR_A_AD35
SR_A_AD36
SR_A_AD37
SR_A_AD38
SR_A_AD39
8.2K
RN47
SR_REQ64- SR_REQ64- <16>
SR_ACK64- SR_ACK64- <16>
SR_PAR64 SR_PAR64 <16>
SR_A_CBE-[4..7] <16>
SR_A_CBE-4
SR_A_CBE-6
SR_A_CBE-5
SR_A_CBE-7
8.2K
RN244
<16> SR_A_INTA-
<16> SR_A_INTB-
<16> SR_A_INTC-
<16> SR_A_INTD-
8.2K
RN60
SR_A_AD40
SR_A_AD41
SR_A_AD42
SR_A_AD43
SR_A_AD44
SR_A_AD45
SR_A_AD46
SR_A_AD47
8.2K
RN288
SR_A_DEVSEL-
SR_A_TRDY-
SR_A_IRDY-
SR_A_FRAME-
SR_A_SERR-
SR_A_PERR-
SR_A_PLOCK-
SR_A_STOP-
SR_A_DEVSEL- <16,21>
SR_A_TRDY- <16,21>
SR_A_IRDY- <16,21>
SR_A_FRAME- <16,21>
SR_A_SERR- <16,21>
SR_A_PERR- <16>
SR_A_PLOCK- <16>
SR_A_STOP- <16,21>
8.2K
RN57
SR_A_AD48
SR_A_AD49
SR_A_AD50
SR_A_AD51
SR_A_AD52
SR_A_AD53
SR_A_AD54
SR_A_AD55
8.2K
RN289
A_REQ-3
A_REQ-4
A_REQ-5
A_REQ-6
A_REQ-0
A_REQ-1
A_REQ-2
A_REQ-3 <11>
A_REQ-4 <11>
A_REQ-5 <11>
A_REQ-6 <11>
A_REQ-0 <11,21>
A_REQ-1 <11,16>
A_REQ-2 <11,16>
8.2K
RN54
SR_A_AD56
SR_A_AD57
SR_A_AD58
SR_A_AD59
SR_A_AD60
SR_A_AD61
SR_A_AD62
SR_A_AD63
8.2K
MICRO-STAR
Title
PCI64 TERMINATION/BYPASS CAP.
Size Custom
Document Number MS-6501
Rev 0C
Date: Tuesday, November 20, 2001
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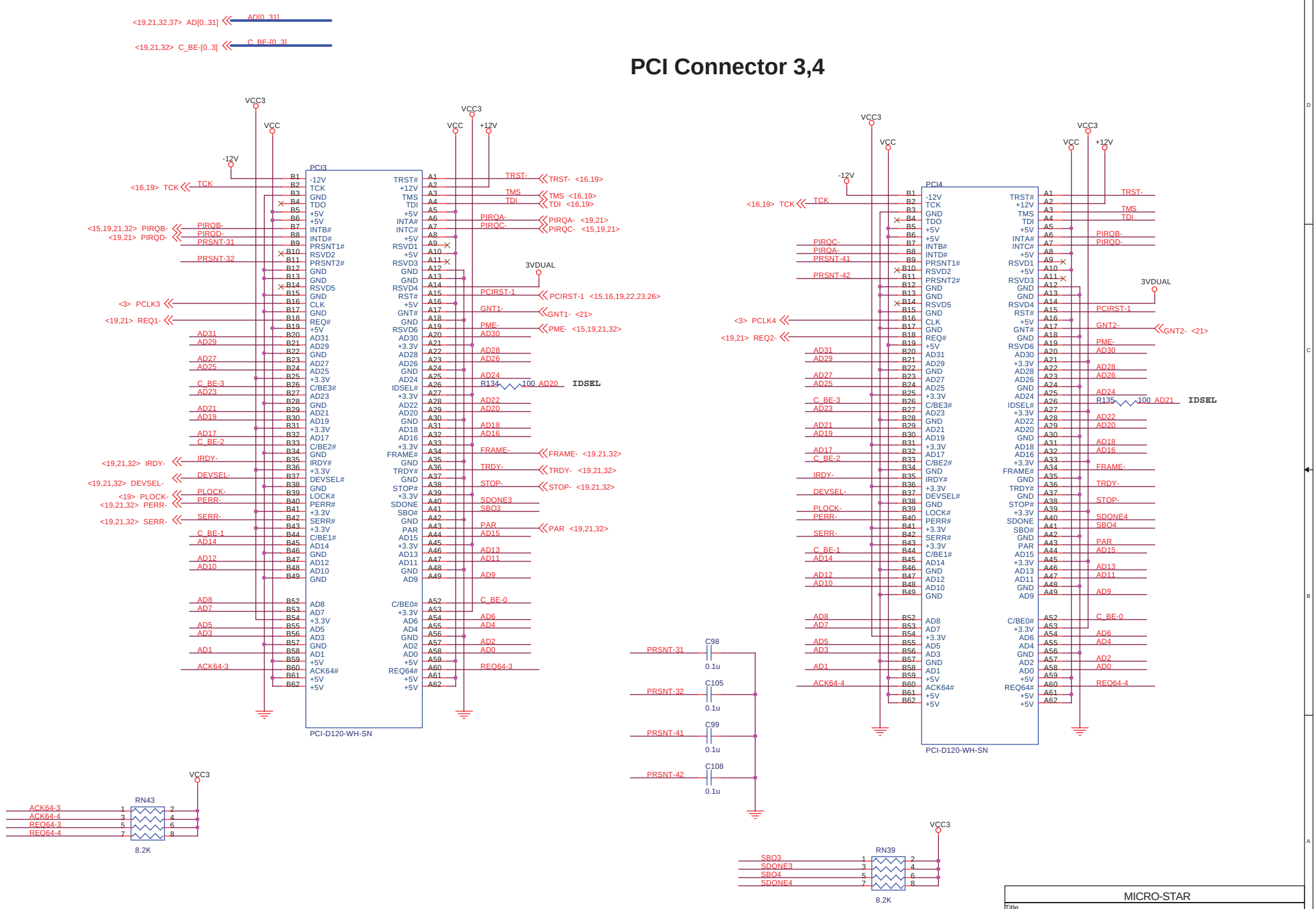
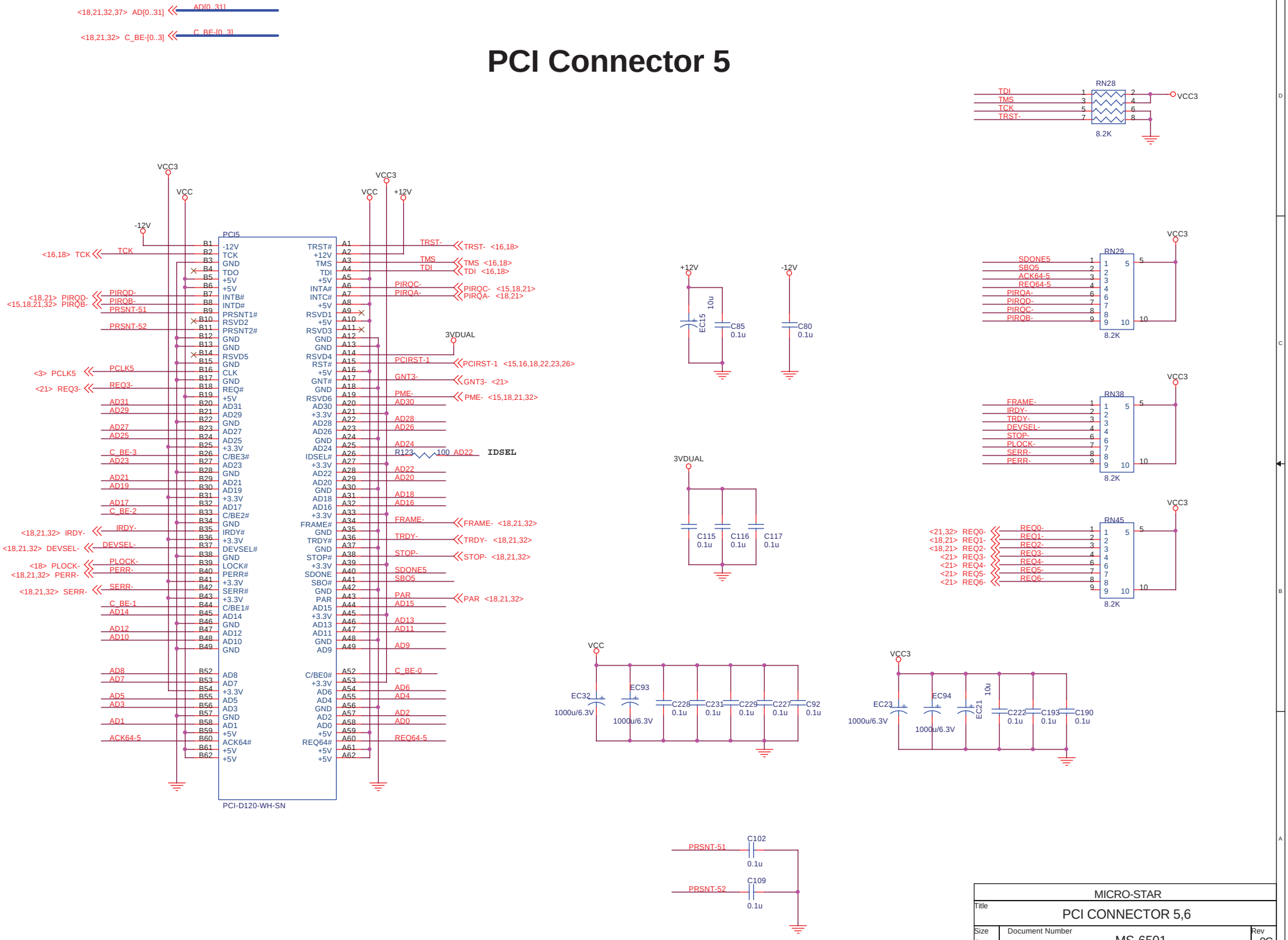
PCI Connector 3,4



PCI Connector 5



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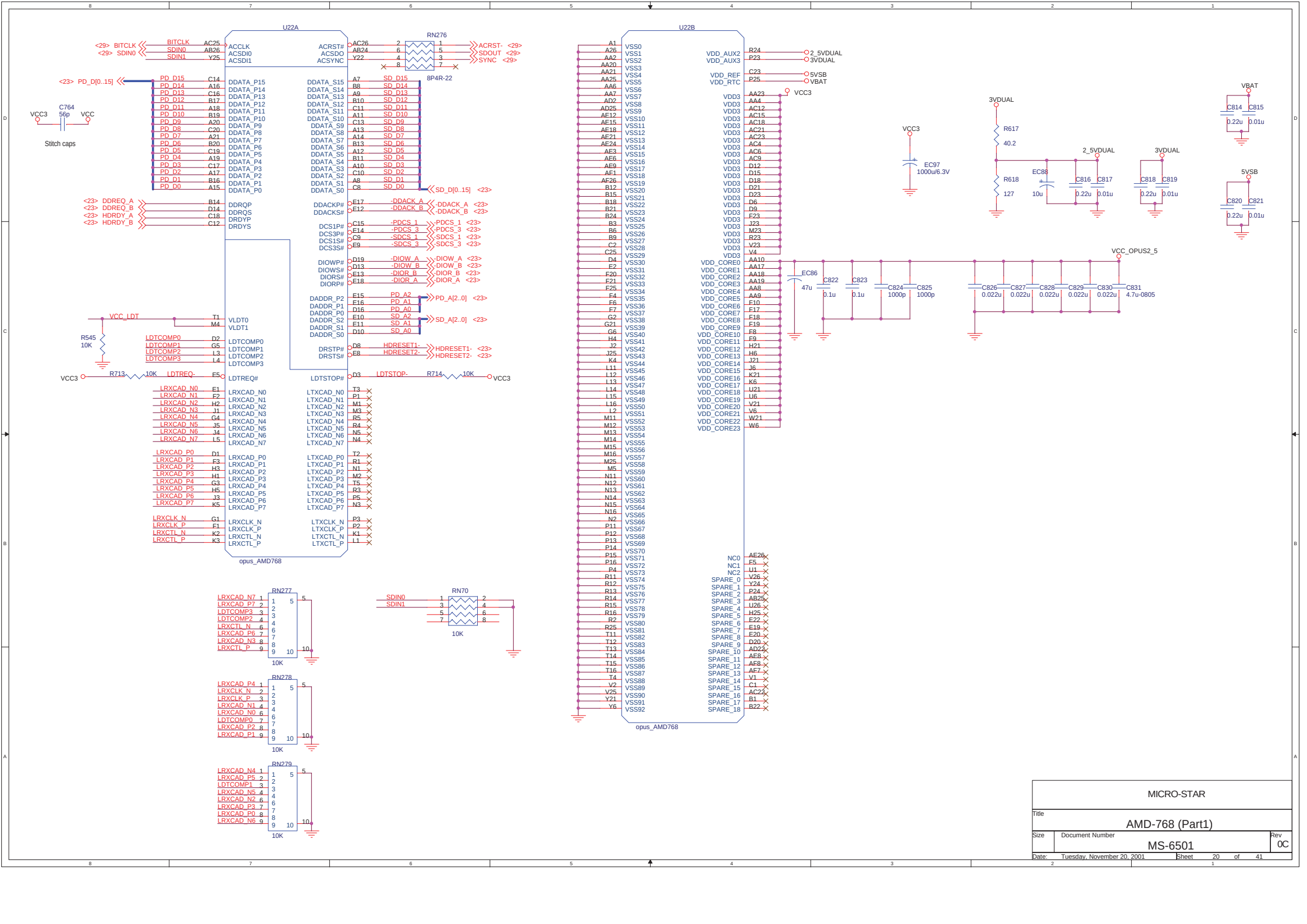
Title	PCI CONNECTOR 5,6	
Size: Custom	Document Number: MS-6501	Rev: 0C
Date: Tuesday, November 20, 2001	Sheet 19 of 41	


U22A
BITCLK
SDIN0
SDIN1
ACCLK
ACSDI0
ACSDI1
ACSDO
ACSYNC
ACRST#
RN276
8P4R-22
ACRST-
SDOUT
SYNC
PD_D[0..15]
DDATA_P0
DDATA_P1
DDATA_P2
DDATA_P3
DDATA_P4
DDATA_P5
DDATA_P6
DDATA_P7
DDATA_P8
DDATA_P9
DDATA_P10
DDATA_P11
DDATA_P12
DDATA_P13
DDATA_P14
DDATA_P15
DDATA_S0
DDATA_S1
DDATA_S2
DDATA_S3
DDATA_S4
DDATA_S5
DDATA_S6
DDATA_S7
DDATA_S8
DDATA_S9
DDATA_S10
DDATA_S11
DDATA_S12
DDATA_S13
DDATA_S14
DDATA_S15
SD_D[0..15]
C764
56p
Stitch caps
DDREQ_A
DDREQ_B
HDRDY_A
HDRDY_B
DDRQP
DDRQS
DRDYP
DRDYS
DDACKP#
DDACKS#
-DDACK_A
-DDACK_B
DCS1P#
DCS3P#
DCS1S#
DCS3S#
-PDCS_1
-PDCS_3
-SDCS_1
-SDCS_3
DIOWP#
DIOWS#
DIORS#
DIORP#
-DIOW_A
-DIOW_B
-DIOR_A
-DIOR_B
DRSTP#
DRSTS#
HDRESET1-
HDRESET2-
DADDR_P0
DADDR_P1
DADDR_P2
DADDR_S0
DADDR_S1
DADDR_S2
PD_A[2..0]
SD_A[2..0]
VCC_LDT
VLDT0
VLDT1
R545
10K
LDTCOMP0
LDTCOMP1
LDTCOMP2
LDTCOMP3
R713
LDTREQ-
LDTREQ#
LDTSTOP#
LDTSTOP-
R714
LRXCAD_N0
LRXCAD_N1
LRXCAD_N2
LRXCAD_N3
LRXCAD_N4
LRXCAD_N5
LRXCAD_N6
LRXCAD_N7
LRXCAD_P0
LRXCAD_P1
LRXCAD_P2
LRXCAD_P3
LRXCAD_P4
LRXCAD_P5
LRXCAD_P6
LRXCAD_P7
LTXCAD_N0
LTXCAD_N1
LTXCAD_N2
LTXCAD_N3
LTXCAD_N4
LTXCAD_N5
LTXCAD_N6
LTXCAD_N7
LTXCAD_P0
LTXCAD_P1
LTXCAD_P2
LTXCAD_P3
LTXCAD_P4
LTXCAD_P5
LTXCAD_P6
LTXCAD_P7
LRXCLK_N
LRXCLK_P
LRXCTL_N
LRXCTL_P
LTXCLK_N
LTXCLK_P
LTXCTL_N
LTXCTL_P
opus_AMD768
RN277
RN278
RN279
RN70
10K
U22B
VSS0
VSS1
VSS2
VSS3
VSS4
VSS5
VSS6
VSS7
VSS8
VSS9
VSS10
VSS11
VSS12
VSS13
VSS14
VSS15
VSS16
VSS17
VSS18
VSS19
VSS20
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VSS48
VSS49
VSS50
VSS51
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VSS53
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VSS64
VSS65
VSS66
VSS67
VSS68
VSS69
VSS70
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VSS75
VSS76
VSS77
VSS78
VSS79
VSS80
VSS81
VSS82
VSS83
VSS84
VSS85
VSS86
VSS87
VSS88
VSS89
VSS90
VSS91
VSS92
VDD_AUX2
VDD_AUX3
VDD_REF
VDD_RTC
2_5VDUAL
3VDUAL
5VSB
VBAT
VDD3
VDD_CORE0
VDD_CORE1
VDD_CORE2
VDD_CORE3
VDD_CORE4
VDD_CORE5
VDD_CORE6
VDD_CORE7
VDD_CORE8
VDD_CORE9
VDD_CORE10
VDD_CORE11
VDD_CORE12
VDD_CORE13
VDD_CORE14
VDD_CORE15
VDD_CORE16
VDD_CORE17
VDD_CORE18
VDD_CORE19
VDD_CORE20
VDD_CORE21
VDD_CORE22
VDD_CORE23
NC0
NC1
NC2
SPARE_0
SPARE_1
SPARE_2
SPARE_3
SPARE_4
SPARE_5
SPARE_6
SPARE_7
SPARE_8
SPARE_9
SPARE_10
SPARE_11
SPARE_12
SPARE_13
SPARE_14
SPARE_15
SPARE_16
SPARE_17
SPARE_18
R617
40.2
R618
127
EC88
10u
EC97
1000u/6.3V
EC86
47u
C822
0.1u
C823
0.1u
C824
1000p
C825
1000p
C826
0.022u
C827
0.022u
C828
0.022u
C829
0.022u
C830
0.022u
C831
4.7u-0805
C814
0.22u
C815
0.01u
C816
0.22u
C817
0.01u
C818
0.22u
C819
0.01u
C820
0.22u
C821
0.01u
VCC_OPUS2_5
MICRO-STAR
AMD-768 (Part1)
MS-6501
Rev
0C
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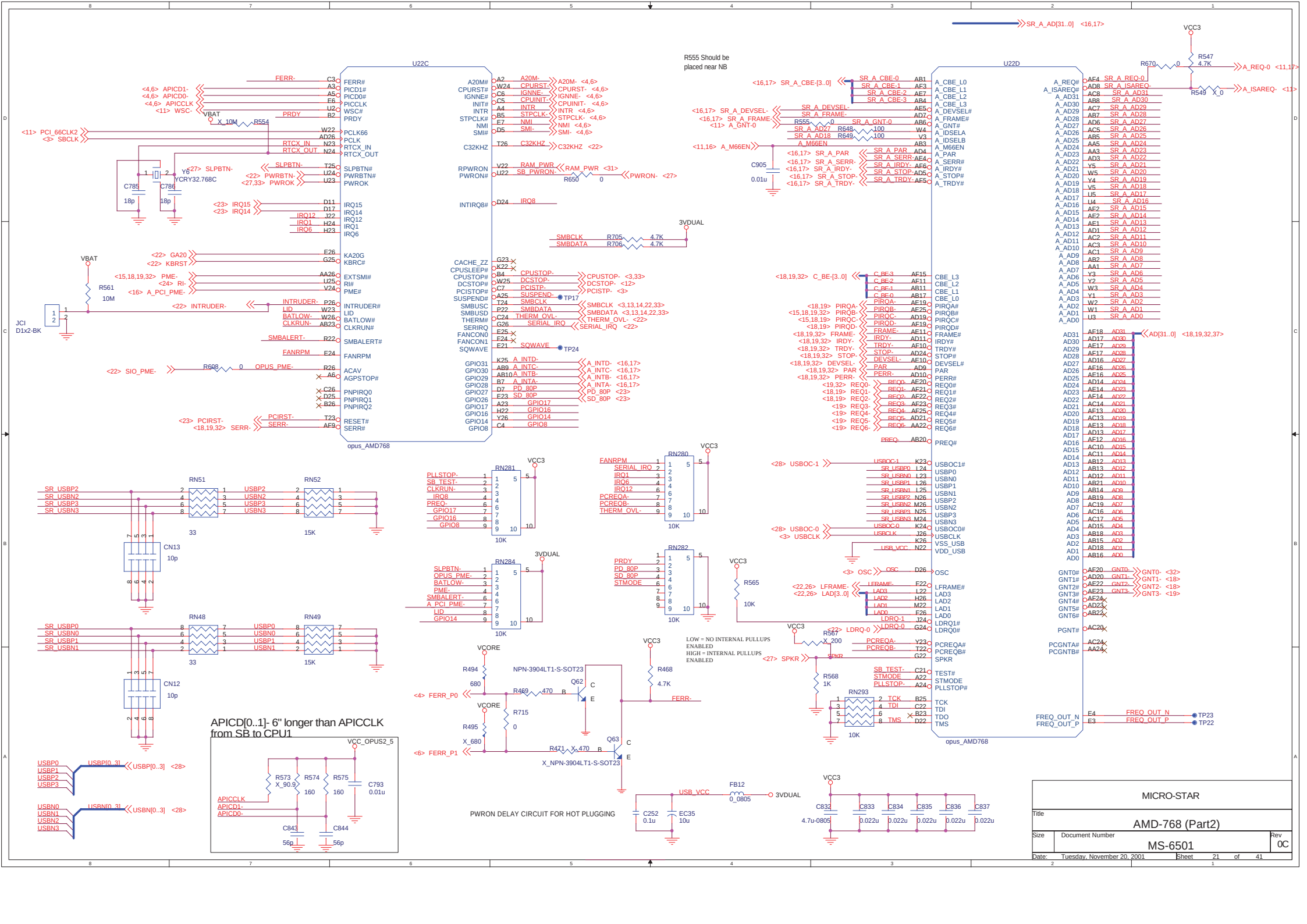
U22C
U22D
opus_AMD768
R555 Should be placed near NB
SR_A_AD[31..0] <16,17>
VCC3
3VDUAL
VBAT
JCI D1x2-BK
RN51
RN52
RN48
RN49
RN280
RN281
RN282
RN284
RN293
CN13
CN12
10p
33
15K
10K
LOW = NO INTERNAL PULLUPS ENABLED
HIGH = INTERNAL PULLUPS ENABLED
APICD[0..1]- 6" longer than APICCLK from SB to CPU1
VCC_OPUS2_5
PWRON DELAY CIRCUIT FOR HOT PLUGGING
NPN-3904LT1-S-SOT23
X_NPN-3904LT1-S-SOT23
MICRO-STAR
AMD-768 (Part2)
MS-6501
Rev 0C
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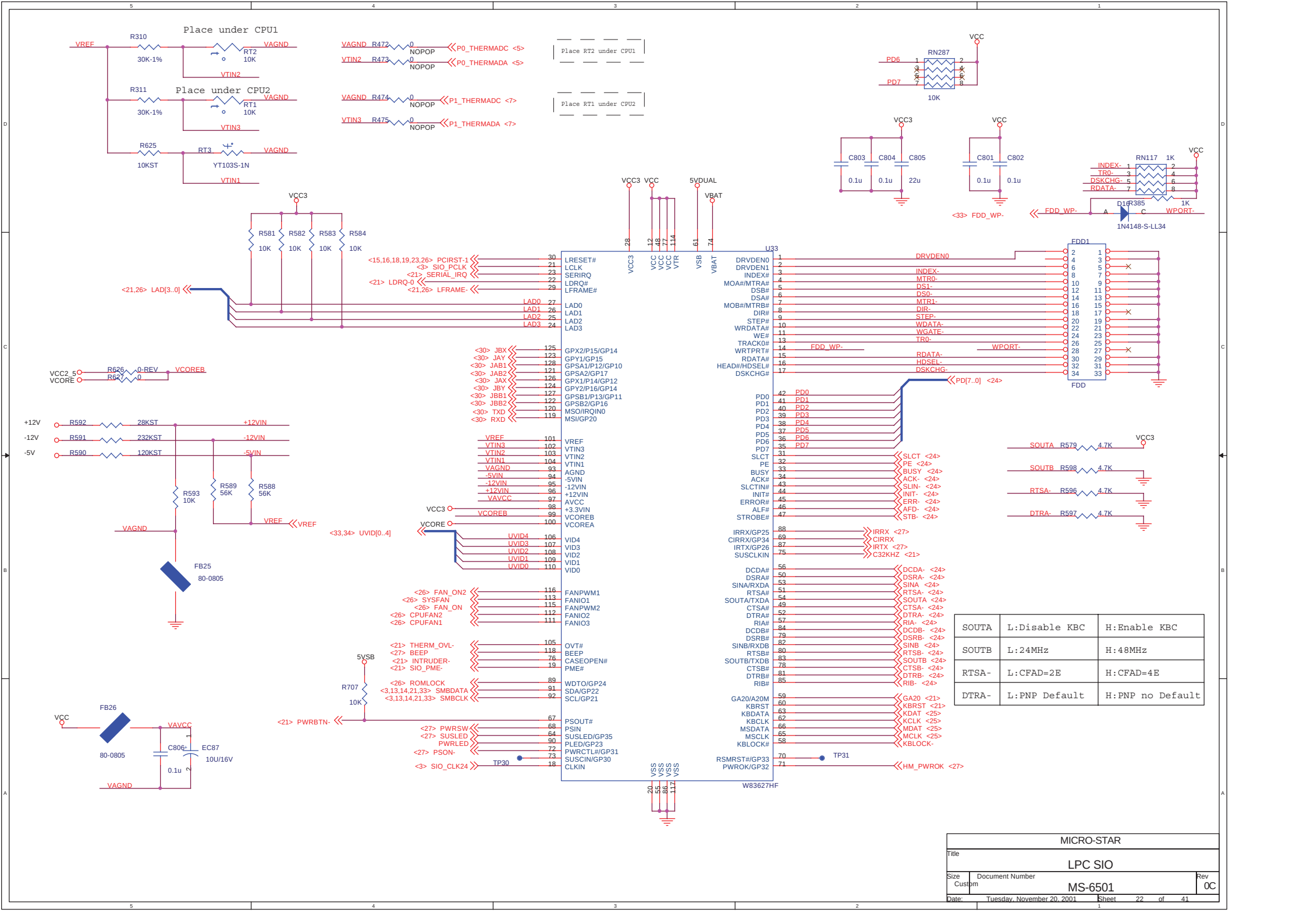
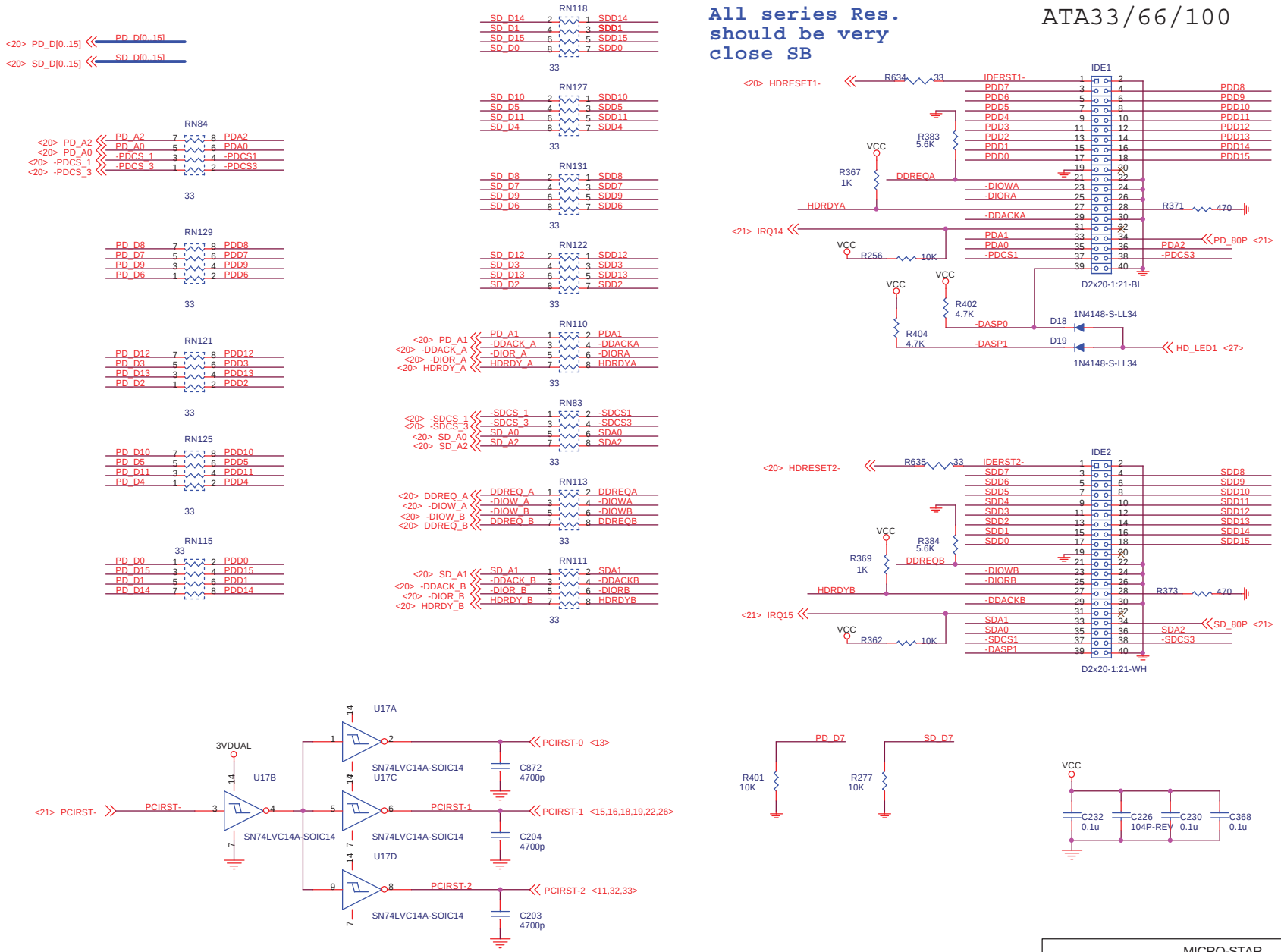


SOUTA	L:Disable KBC	H:Enable KBC
SOUTB	L:24MHz	H:48MHz
RTSA-	L:CFAD=2E	H:CFAD=4E
DTRA-	L:PNP Default	H:PNP no Default

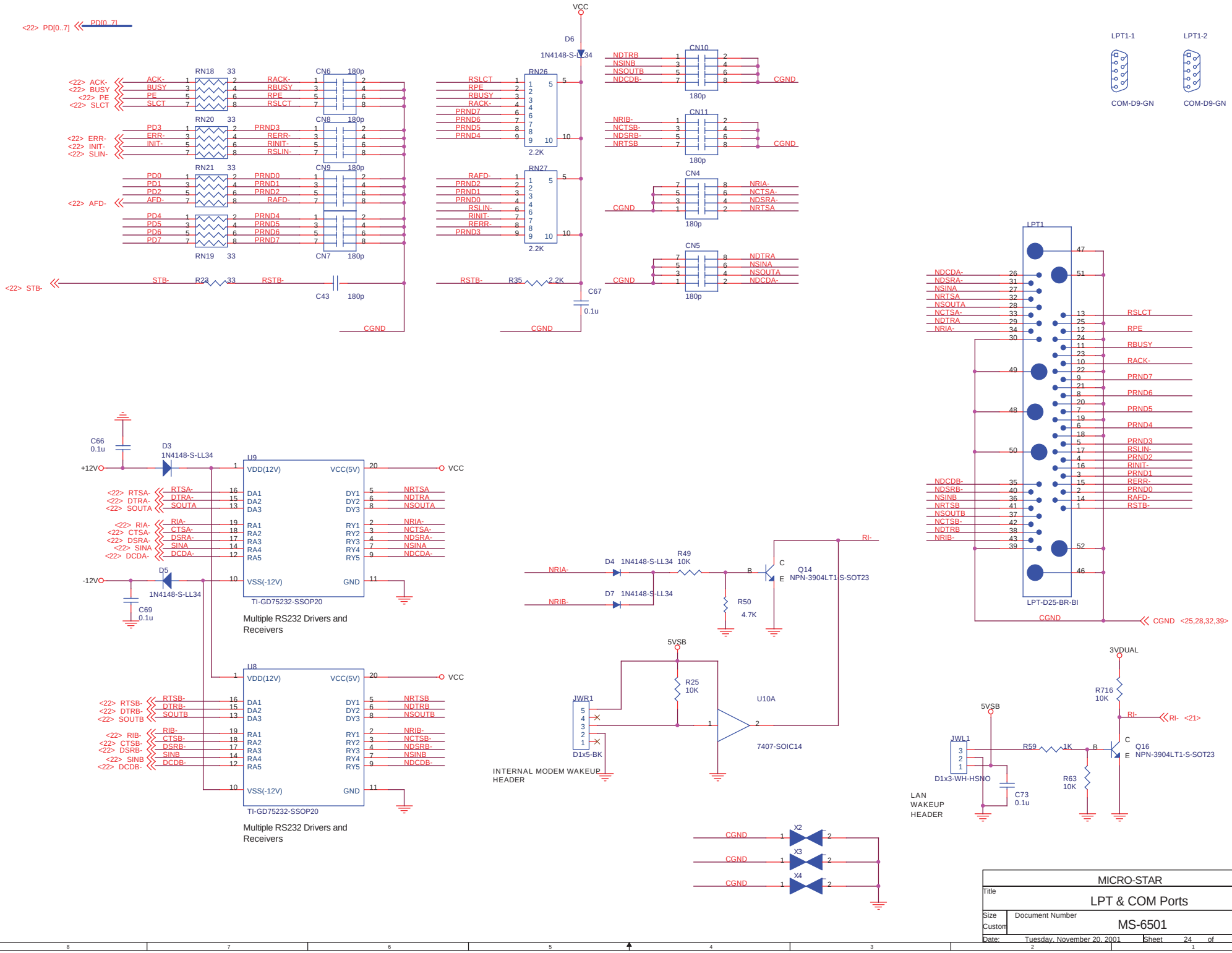
MICRO-STAR		
Title	LPC SIO	
Size: Custom	Document Number: MS-6501	Rev: 0C
Date: Tuesday, November 20, 2001	Sheet 22 of 41	

ATA33/66/100

All series Res. should be very close SB



MICRO-STAR		
Title: ATA33/66 Connectors		
Size: Custom	Document Number: MS-6501	Rev: 0C
Date: Tuesday, November 20, 2001	Sheet 23 of 41	


PD[0..7]
RN18 33
RN20 33
RN21 33
RN19 33
CN6 180p
CN8 180p
CN9 180p
CN7 180p
ACK-
BUSY
PE
SLCT
PD3
ERR-
INIT-
SLIN-
PD0
PD1
PD2
AFD-
PD4
PD5
PD6
PD7
RACK-
RBUSY
RPE
RSLCT
RERR-
RINIT-
RSLIN-
PRND0
PRND1
PRND2
RAFD-
PRND4
PRND5
PRND6
PRND7
STB-
R23 33
C43 180p
CGND
VCC
D6
1N4148-S-LL34
RN26
RN27
2.2K
R35 2.2K
C67
0.1u
CN10
CN11
CN4
CN5
180p
NDTRB
NSINB
NSOUTB
NDCDB-
NRIB-
NCTSB-
NDSRB-
NRTSB
NRIA-
NCTSA-
NDSRA-
NRTSA
NDTRA
NSINA
NSOUTA
NDCDA-
LPT1-1
LPT1-2
COM-D9-GN
LPT1
LPT-D25-BR-BI
C66
0.1u
D3
1N4148-S-LL34
+12V
-12V
D5
C69
0.1u
U9
U8
VDD(12V)
VCC(5V)
VSS(-12V)
GND
DA1
DA2
DA3
RA1
RA2
RA3
RA4
RA5
DY1
DY2
DY3
RY1
RY2
RY3
RY4
RY5
TI-GD75232-SSOP20
Multiple RS232 Drivers and Receivers
D4 1N4148-S-LL34
D7 1N4148-S-LL34
R49 10K
R50 4.7K
Q14
NPN-3904LT1-S-SOT23
5VSB
R25 10K
JWR1
D1x5-BK
U10A
7407-SOIC14
INTERNAL MODEM WAKEUP HEADER
3VDUAL
R716 10K
JWL1
D1x3-WH-HSNO
R59 1K
R63 10K
C73 0.1u
Q16
LAN WAKEUP HEADER
X2
X3
X4
MICRO-STAR
LPT & COM Ports
MS-6501
0C
Tuesday, November 20, 2001
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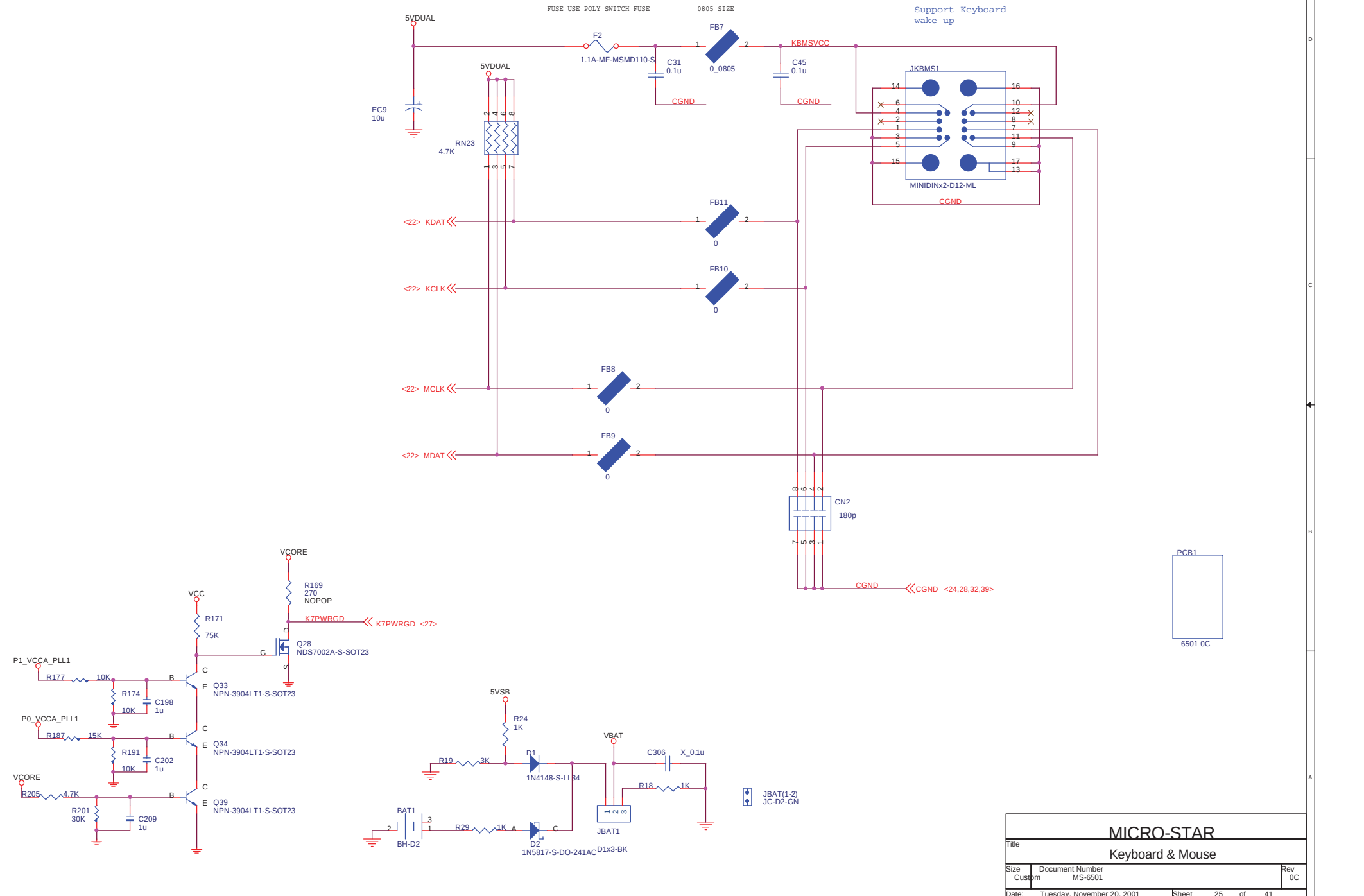
FUSE USE POLY SWITCH FUSE
0805 SIZE
Support Keyboard wake-up
5VDUAL
F2
1.1A-MF-MSMD110-S
FB7
0_0805
KBMSVCC
C31 0.1u
C45 0.1u
CGND
EC9 10u
RN23 4.7K
JKBMS1
MINIDINx2-D12-ML
FB11
FB10
FB8
FB9
<22> KDAT
<22> KCLK
<22> MCLK
<22> MDAT
CN2 180p
CGND <24,28,32,39>
PCB1
6501 0C
VCORE
R169 270 NOPOP
K7PWRGD
K7PWRGD <27>
VCC
R171 75K
Q28 NDS7002A-S-SOT23
P1_VCCA_PLL1
R177 10K
R174 10K
C198 1u
Q33 NPN-3904LT1-S-SOT23
P0_VCCA_PLL1
R187 15K
R191 10K
C202 1u
Q34 NPN-3904LT1-S-SOT23
VCORE
R205 4.7K
R201 30K
C209 1u
Q39 NPN-3904LT1-S-SOT23
5VSB
R24 1K
R19 3K
D1 1N4148-S-LL34
VBAT
C306 X_0.1u
R18 1K
JBAT1
JBAT(1-2) JC-D2-GN
BAT1
BH-D2
R29 1K
D2 1N5817-S-DO-241AC
D1x3-BK
MICRO-STAR
Title
Keyboard & Mouse
Size Custom
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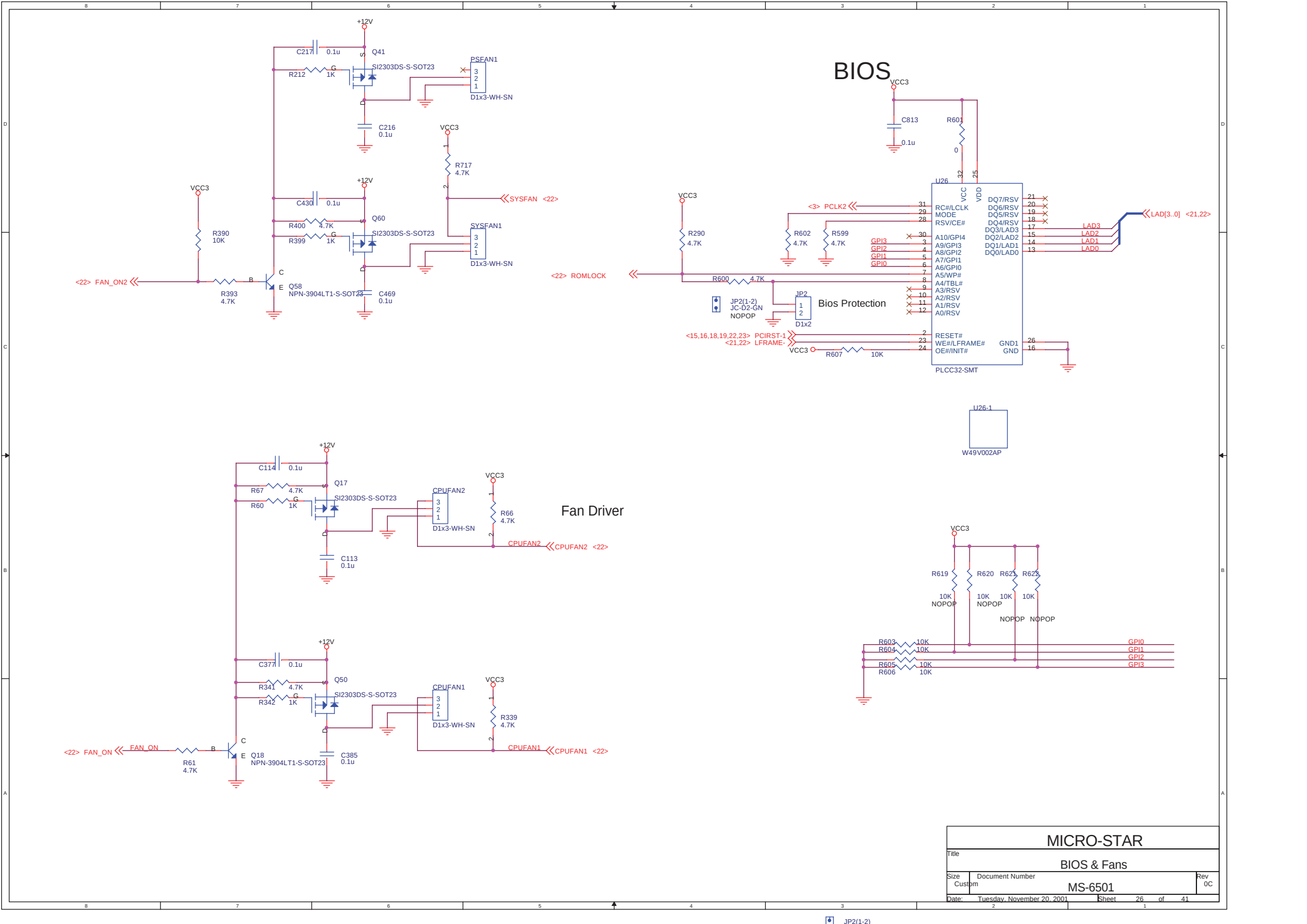
BIOS
Fan Driver
Bios Protection
+12V
VCC3
C217 0.1u
Q41
SI2303DS-S-SOT23
R212 1K
PSFAN1
D1x3-WH-SN
C216 0.1u
R717 4.7K
SYSFAN <22>
C430 0.1u
R400 4.7K
R399 1K
Q60
SYSFAN1
R390 10K
<22> FAN_ON2
R393 4.7K
Q58
NPN-3904LT1-S-SOT23
C469 0.1u
<22> ROMLOCK
C813 0.1u
R601 0
U26
PCLK2
RC#/LCLK
MODE
RSV/CE#
A10/GPI4
A9/GPI3
A8/GPI2
A7/GPI1
A6/GPI0
A5/WP#
A4/TBL#
A3/RSV
A2/RSV
A1/RSV
A0/RSV
RESET#
WE#/LFRAME#
OE#/INIT#
DQ7/RSV
DQ6/RSV
DQ5/RSV
DQ4/RSV
DQ3/LAD3
DQ2/LAD2
DQ1/LAD1
DQ0/LAD0
GND1
GND
PLCC32-SMT
LAD[3..0] <21,22>
LAD3
LAD2
LAD1
LAD0
R290 4.7K
R602 4.7K
R599 4.7K
R600 4.7K
GPI3
GPI2
GPI1
GPI0
JP2(1-2)
JC-D2-GN
NOPOP
JP2
D1x2
<15,16,18,19,22,23> PCIRST-1
<21,22> LFRAME-
R607 10K
U26-1
W49V002AP
C114 0.1u
Q17
R67 4.7K
R60 1K
CPUFAN2
R66 4.7K
CPUFAN2 <22>
C113 0.1u
C377 0.1u
Q50
R341 4.7K
R342 1K
CPUFAN1
R339 4.7K
CPUFAN1 <22>
<22> FAN_ON
FAN_ON
R61 4.7K
Q18
NPN-3904LT1-S-SOT23
C385 0.1u
R619 10K NOPOP
R620 10K NOPOP
R621 10K
R622 10K
NOPOP NOPOP
R603 10K
R604 10K
R605 10K
R606 10K
GPI0
GPI1
GPI2
GPI3
MICRO-STAR
Title
BIOS & Fans
Size
Custom
Document Number
MS-6501
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0C
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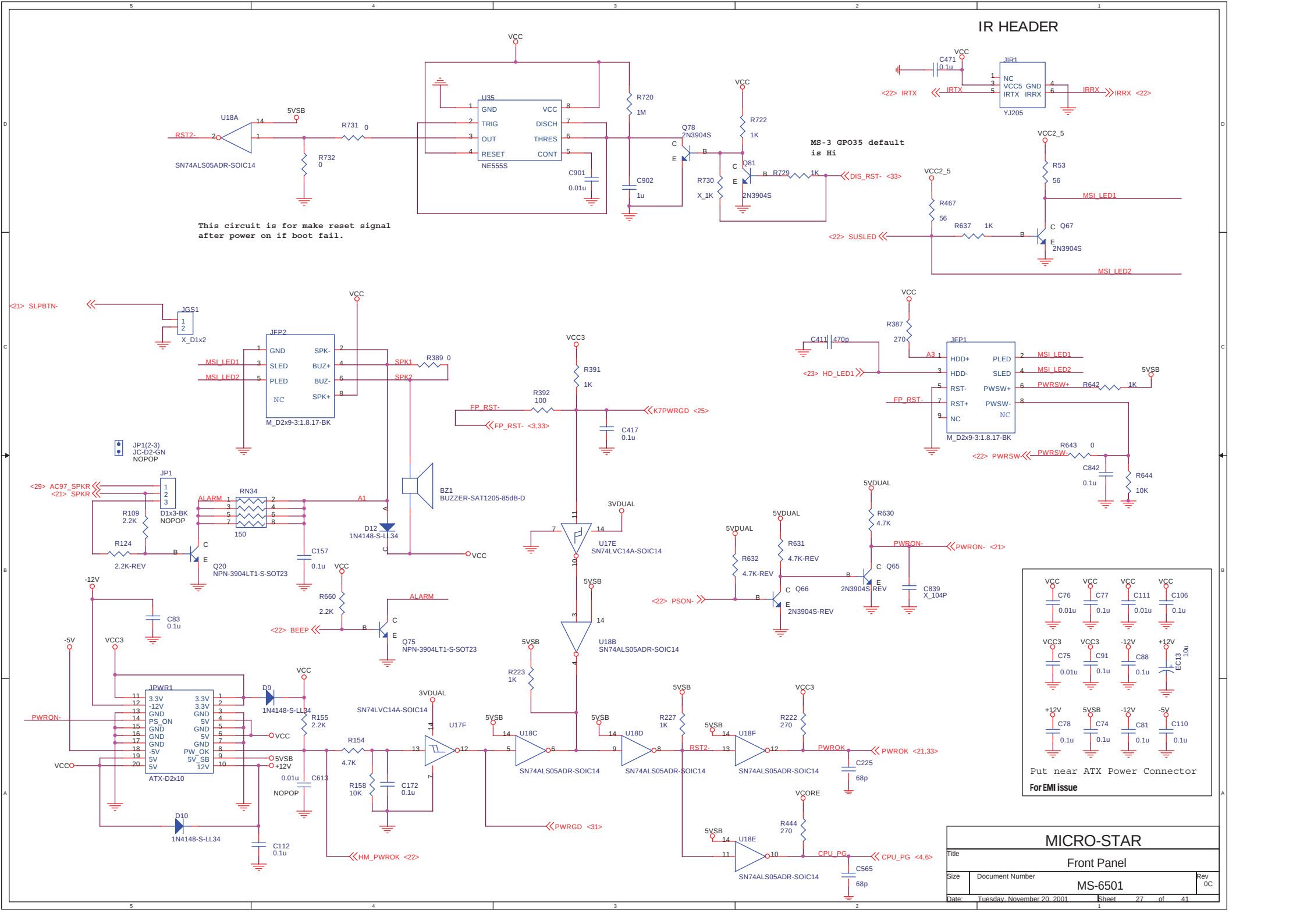
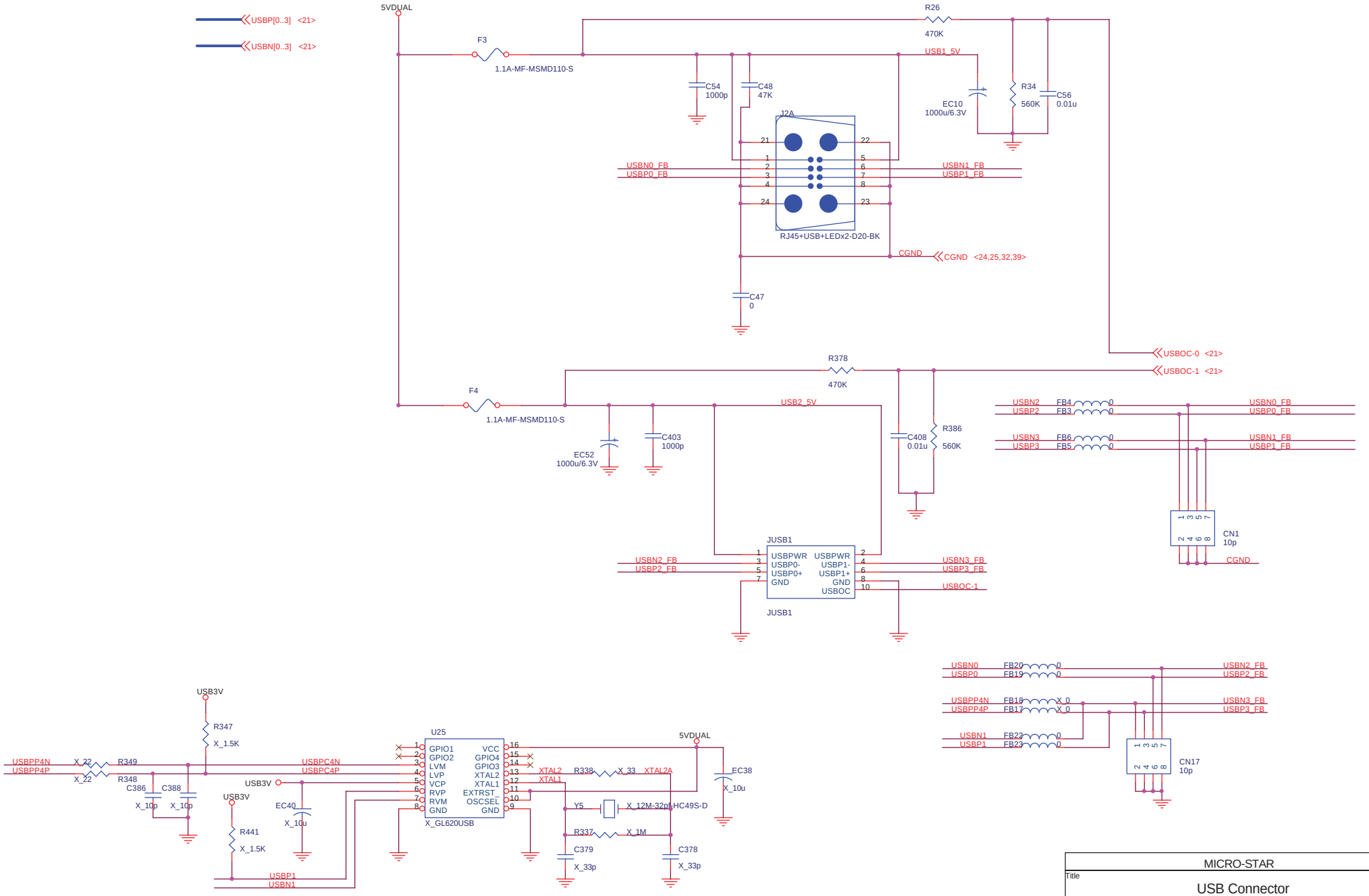
IR HEADER



MICRO-STAR		
Title	Front Panel	
Size	Document Number MS-6501	Rev 0C
Date: Tuesday, November 20, 2001	Sheet 27 of 41	



MICRO-STAR		
Title	USB Connector	
Size: Custom	Document Number: MS-6501	Rev: 0C
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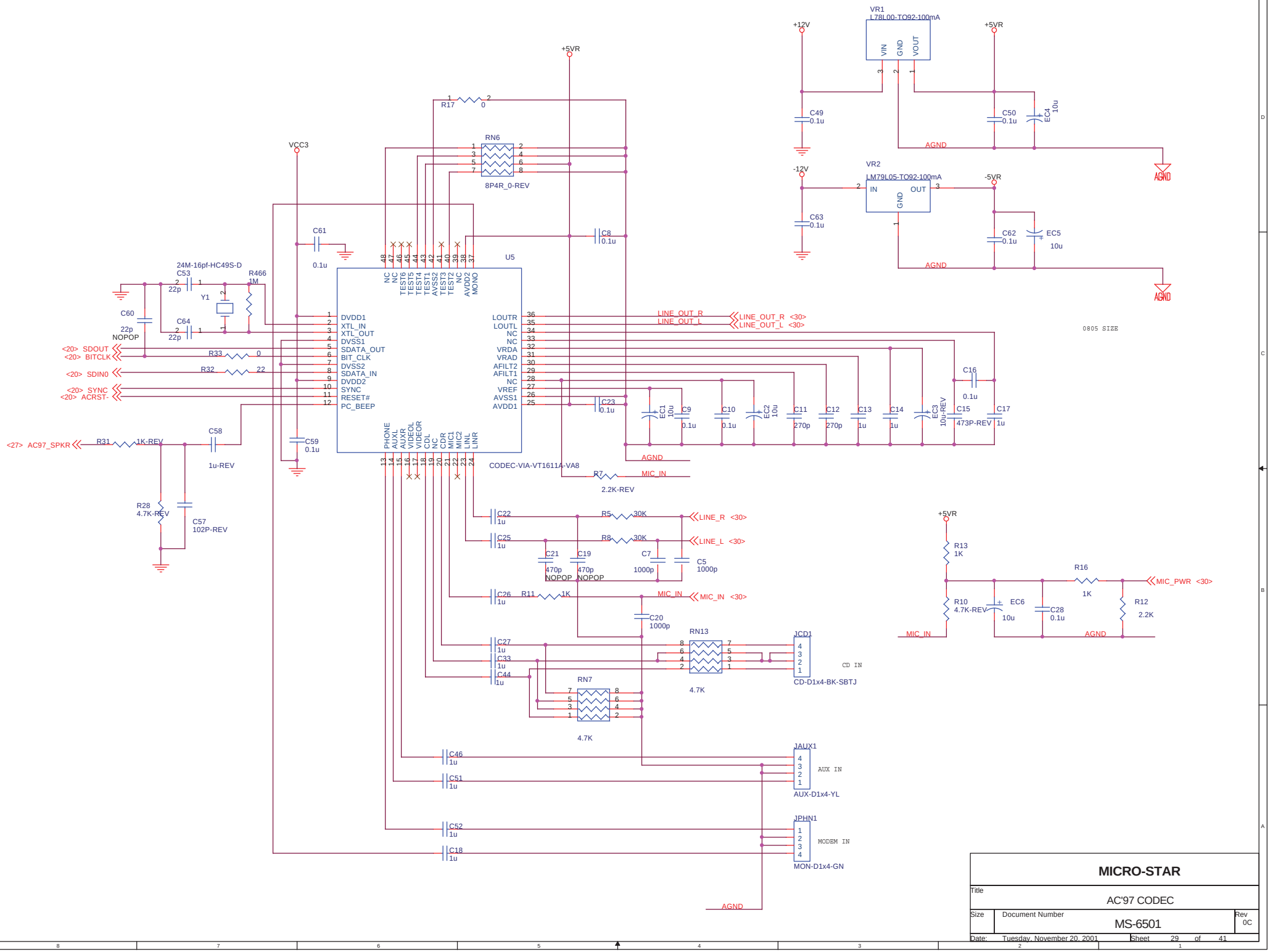
VR1
L78L00-TO92-100mA
VIN
GND
VOUT
+12V
+5VR
C49
0.1u
C50
0.1u
EC4
10u
AGND
VR2
LM79L05-TO92-100mA
IN
GND
OUT
-12V
-5VR
C63
0.1u
C62
0.1u
EC5
10u
+5VR
R17
0
RN6
8P4R_0-REV
VCC3
C61
0.1u
C8
0.1u
U5
24M-16pf-HC49S-D
C53
22p
C64
22p
Y1
R466
1M
C60
22p
NOPOP
<20> SDOUT
<20> BITCLK
<20> SDIN0
<20> SYNC
<20> ACRST-
R33
0
R32
22
DVDD1
XTL_IN
XTL_OUT
DVSS1
SDATA_OUT
BIT_CLK
DVSS2
SDATA_IN
DVDD2
SYNC
RESET#
PC_BEEP
LOUTR
LOUTL
VRDA
VRAD
AFILT2
AFILT1
VREF
AVSS1
AVDD1
LINE_OUT_R
LINE_OUT_L
LINE_OUT_R <30>
LINE_OUT_L <30>
0805 SIZE
C16
0.1u
C15
473P-REV
C17
1u
EC1
10u
EC2
10u
EC3
10u-REV
C9
0.1u
C10
0.1u
C11
270p
C12
270p
C13
1u
C14
1u
C23
0.1u
AGND
MIC_IN
R7
2.2K-REV
CODEC-VIA-VT1611A-VA8
C59
0.1u
<27> AC97_SPKR
R31
1K-REV
C58
1u-REV
R28
4.7K-REV
C57
102P-REV
C22
1u
C25
1u
R5
30K
R8
30K
LINE_R <30>
LINE_L <30>
C21
470p
NOPOP
C19
470p
NOPOP
C7
1000p
C5
1000p
C26
1u
R11
1K
MIC_IN <30>
C20
1000p
C27
1u
C33
1u
C44
1u
RN13
4.7K
JCD1
CD-D1x4-BK-SBTJ
CD IN
RN7
4.7K
C46
1u
C51
1u
JAUX1
AUX-D1x4-YL
AUX IN
C52
1u
C18
1u
JPHN1
MON-D1x4-GN
MODEM IN
+5VR
R13
1K
R16
1K
MIC_PWR <30>
R10
4.7K-REV
EC6
10u
C28
0.1u
R12
2.2K
MIC_IN
AGND
MICRO-STAR
Title
AC'97 CODEC
Size
Document Number
MS-6501
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0C
Date:
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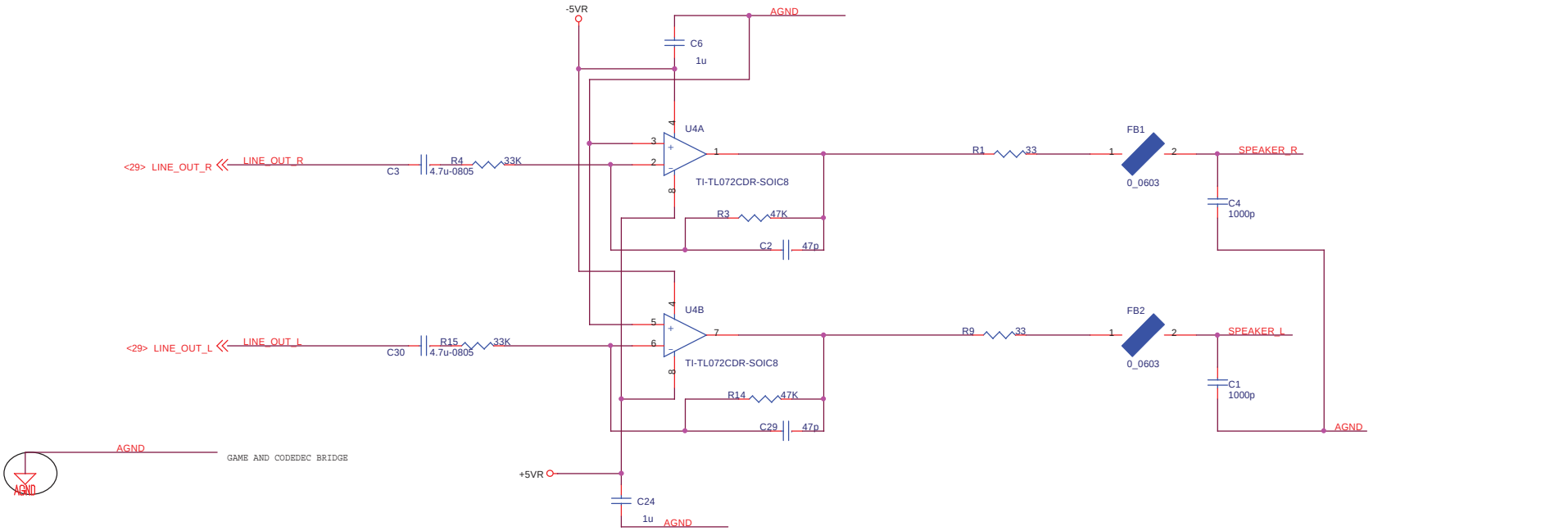
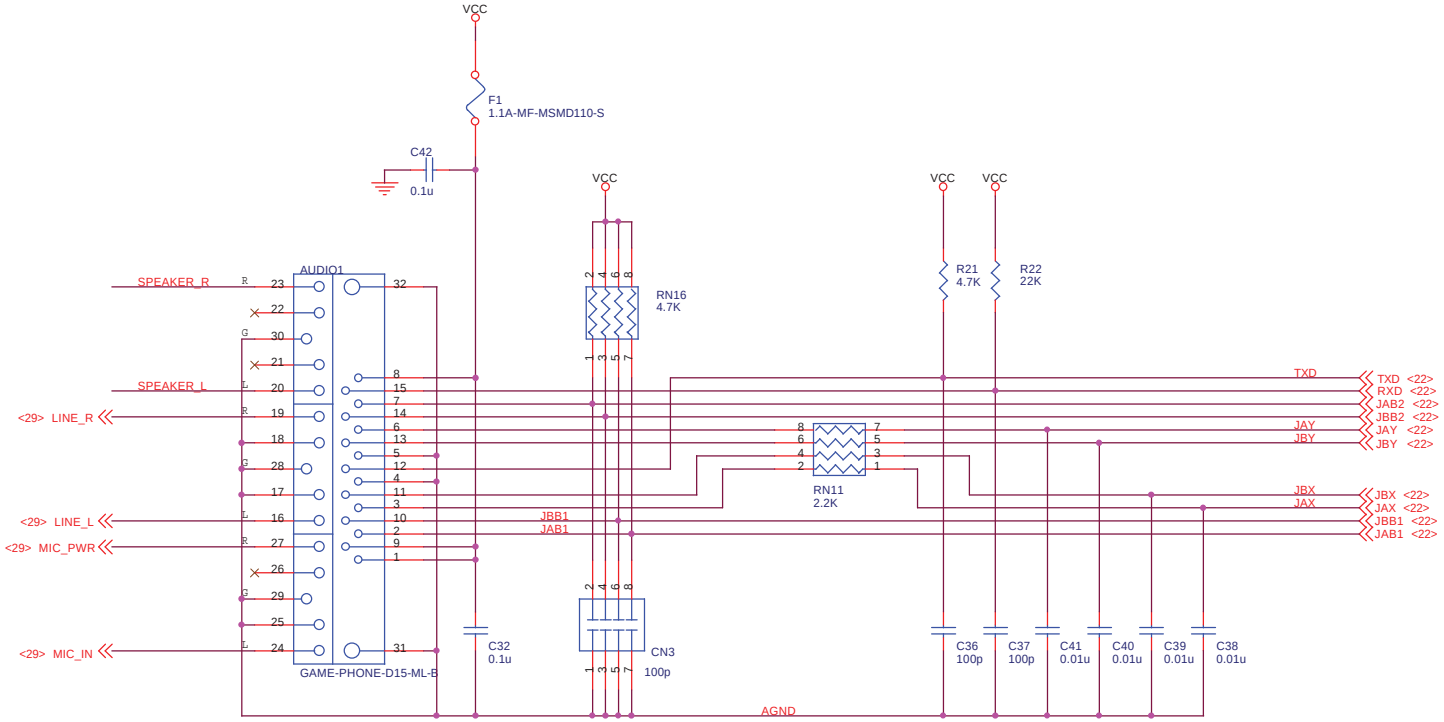
41





MICRO-STAR

Title: Audio/Game Port

Size: Custom | Document Number: MS-6501 | Rev: 0C

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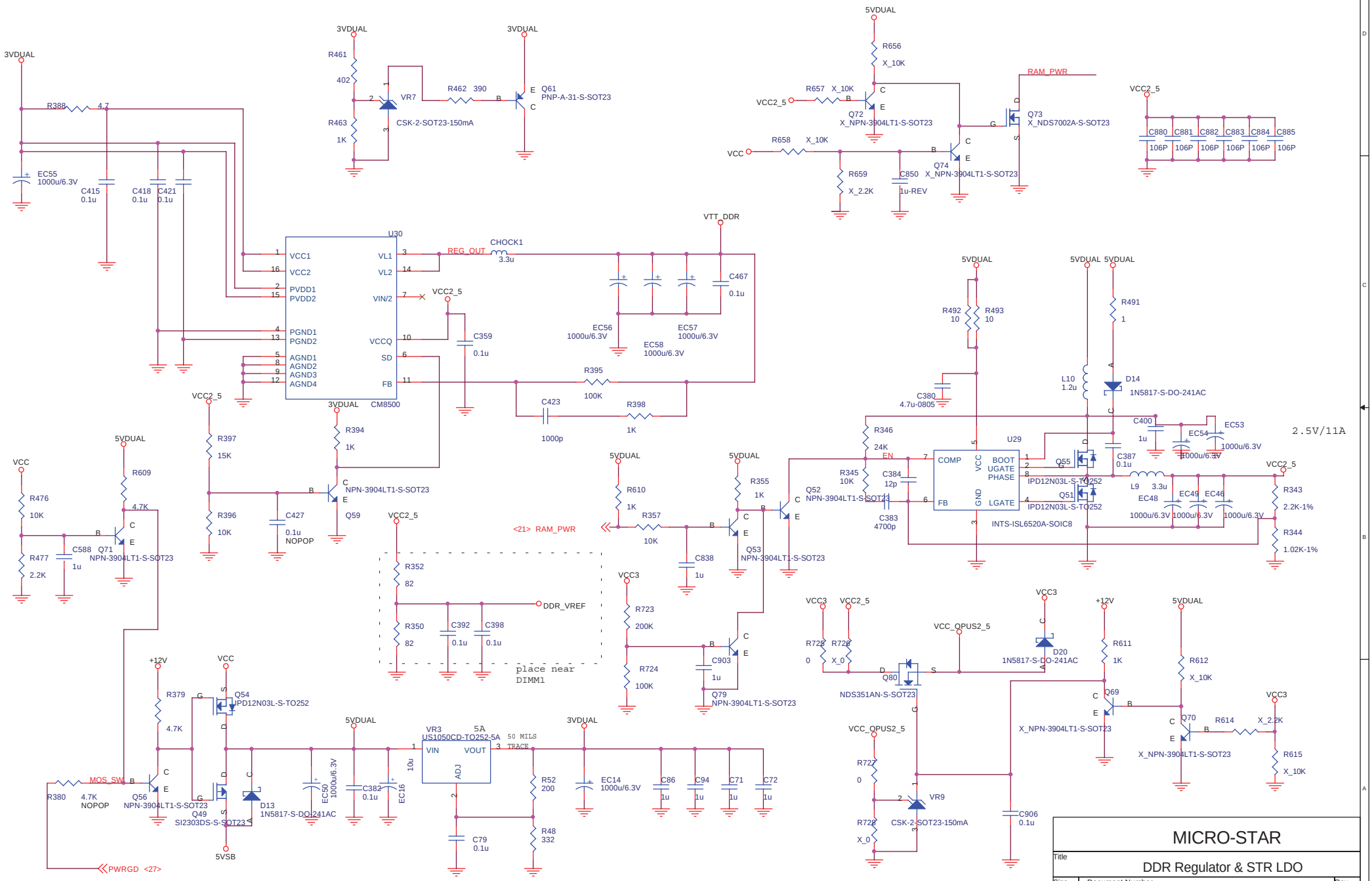
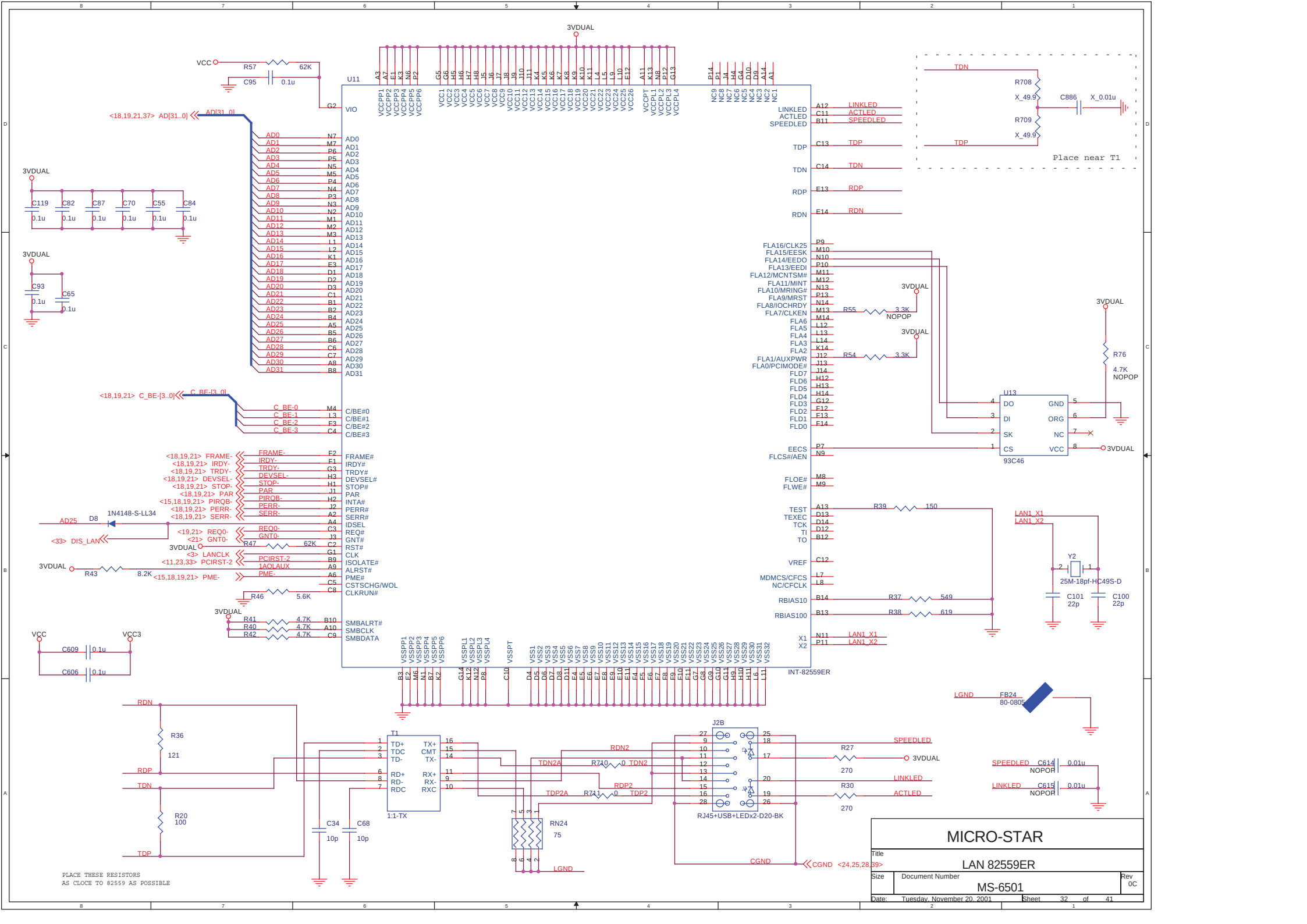
DDR Regulator & STR LDO




3VDUAL
VCC
R57
62K
C95
0.1u
U11
G2
VIO
<18,19,21,37> AD[31..0]
AD[31..0]
AD0 N7
AD1 M7
AD2 P6
AD3 P5
AD4 N5
AD5 M5
AD6 P4
AD7 N4
AD8 P3
AD9 N3
AD10 N2
AD11 M1
AD12 M2
AD13 M3
AD14 L1
AD15 L2
AD16 K1
AD17 E3
AD18 D1
AD19 D2
AD20 D3
AD21 C1
AD22 B1
AD23 B2
AD24 B4
AD25 A5
AD26 B5
AD27 B6
AD28 C6
AD29 C7
AD30 A8
AD31 B8
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
AD16
AD17
AD18
AD19
AD20
AD21
AD22
AD23
AD24
AD25
AD26
AD27
AD28
AD29
AD30
AD31
C119 0.1u
C82 0.1u
C87 0.1u
C70 0.1u
C55 0.1u
C84 0.1u
C93 0.1u
C65 0.1u
<18,19,21> C_BE-[3..0]
C_BE-[3..0]
C_BE-0 M4
C_BE-1 L3
C_BE-2 F3
C_BE-3 C4
C/BE#0
C/BE#1
C/BE#2
C/BE#3
<18,19,21> FRAME-
<18,19,21> IRDY-
<18,19,21> TRDY-
<18,19,21> DEVSEL-
<18,19,21> STOP-
<18,19,21> PAR
<15,18,19,21> PIRQB-
<18,19,21> PERR-
<18,19,21> SERR-
FRAME- F2
IRDY- F1
TRDY- G3
DEVSEL- H3
STOP- H1
PAR J1
PIRQB- H2
PERR- J2
SERR- A2
FRAME#
IRDY#
TRDY#
DEVSEL#
STOP#
PAR
INTA#
PERR#
SERR#
IDSEL
REQ#
GNT#
RST#
CLK
ISOLATE#
ALRST#
PME#
CSTSCHG/WOL
CLKRUN#
AD25
D8
1N4148-S-LL34
<33> DIS_LAN
<19,21> REQ0-
<21> GNT0-
REQ0- C3
GNT0- J3
R47
62K
3VDUAL
<3> LANCLK
<11,23,33> PCIRST-2
LANCLK G1
PCIRST-2 B9
1AOLAUX A9
3VDUAL
R43
8.2K
<15,18,19,21> PME-
PME- A6
R46
5.6K
C5
C8
3VDUAL
R41 4.7K
R40 4.7K
R42 4.7K
SMBALRT# B10
SMBCLK A10
SMBDATA C9
VCC
VCC3
C609 0.1u
C606 0.1u
INT-82559ER
LINKLED A12
ACTLED C11
SPEEDLED B11
TDP C13
TDN C14
RDP E13
RDN E14
LINKLED
ACTLED
SPEEDLED
TDP
TDN
RDP
RDN
FLA16/CLK25 P9
FLA15/EESK M10
FLA14/EEDO N10
FLA13/EEDI P10
FLA12/MCNTSM# M11
FLA11/MINT M12
FLA10/MRING# N13
FLA9/MRST P13
FLA8/IOCHRDY N14
FLA7/CLKEN M13
FLA6 M14
FLA5 L12
FLA4 L13
FLA3 L14
FLA2 K14
FLA1/AUXPWR J12
FLA0/PCIMODE# J13
FLD7 J14
FLD6 H12
FLD5 H13
FLD4 H14
FLD3 G12
FLD2 F12
FLD1 F13
FLD0 F14
R55 3.3K NOPOP
R54 3.3K
EECS P7
FLCS#/AEN N9
FLOE# M8
FLWE# M9
TEST A13
TEXEC D13
TCK D14
TI D12
TO B12
VREF C12
MDMCS/CFCS L7
NC/CFCLK L8
RBIAS10 B14
RBIAS100 B13
R39 150
R37 549
R38 619
X1 N11
X2 P11
LAN1_X1
LAN1_X2
TDN
R708
X_49.9
C886
X_0.01u
R709
X_49.9
TDP
Place near T1
U13
DO
DI
SK
CS
GND
ORG
NC
VCC
93C46
R76
4.7K
NOPOP
Y2
25M-18pf-HC49S-D
C101 22p
C100 22p
LGND
FB24
80-0805
T1
TD+
TDC
TD-
RD+
RD-
RDC
TX+
CMT
TX-
RX+
RX-
RXC
1:1-TX
RDN2
TDN2A
R740 0 TDN2
RDP2
TDP2A
R741 0 TDP2
RN24
75
J2B
RJ45+USB+LEDx2-D20-BK
SPEEDLED
LINKLED
ACTLED
R27
270
R30
270
3VDUAL
C614 0.01u
NOPOP
C615 0.01u
NOPOP
R36
121
R20
100
C34 10p
C68 10p
CGND
<CGND> <24,25,28,39>
LGND
PLACE THESE RESISTORS
AS CLOCE TO 82559 AS POSSIBLE
MICRO-STAR
Title
LAN 82559ER
Size
Document Number
MS-6501
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0C
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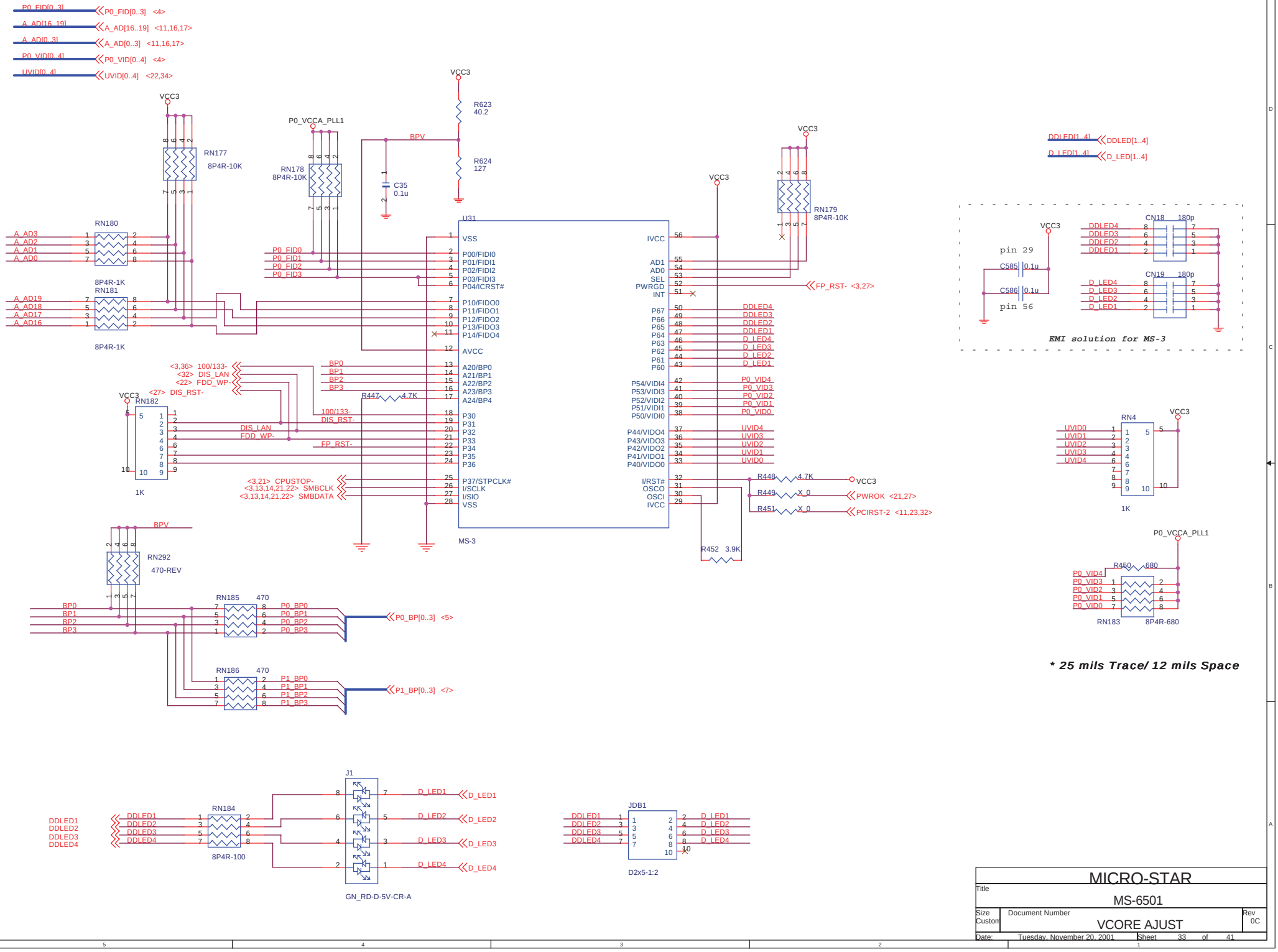
P0_FID[0..3] P0_FID[0..3] <4>
A_AD[16..19] A_AD[16..19] <11,16,17>
A_AD[0..3] A_AD[0..3] <11,16,17>
P0_VID[0..4] P0_VID[0..4] <4>
UVID[0..4] UVID[0..4] <22,34>
VCC3
RN177 8P4R-10K
P0_VCCA_PLL1
RN178 8P4R-10K
BPV
C35 0.1u
R623 40.2
R624 127
RN180
A_AD3 A_AD2 A_AD1 A_AD0
8P4R-1K
RN181
A_AD19 A_AD18 A_AD17 A_AD16
8P4R-1K
U31
VSS
P00/FIDI0 P01/FIDI1 P02/FIDI2 P03/FIDI3 P04/ICRST#
P10/FIDO0 P11/FIDO1 P12/FIDO2 P13/FIDO3 P14/FIDO4
AVCC
A20/BP0 A21/BP1 A22/BP2 A23/BP3 A24/BP4
P30 P31 P32 P33 P34 P35 P36
P37/STPCLK#
I/SCLK
I/SIO
VSS
IVCC
AD1 AD0 SEL PWRGD INT
P67 P66 P65 P64 P63 P62 P61 P60
P54/VIDI4 P53/VIDI3 P52/VIDI2 P51/VIDI1 P50/VIDI0
P44/VIDO4 P43/VIDO3 P42/VIDO2 P41/VIDO1 P40/VIDO0
I/RST#
OSCO
OSCI
IVCC
MS-3
RN179 8P4R-10K
FP_RST- <3,27>
DDLED4 DDLED3 DDLED2 DDLED1 D_LED4 D_LED3 D_LED2 D_LED1
P0_VID4 P0_VID3 P0_VID2 P0_VID1 P0_VID0
UVID4 UVID3 UVID2 UVID1 UVID0
<3,36> 100/133-
<32> DIS_LAN
<22> FDD_WP-
<27> DIS_RST-
RN182
1K
R447 4.7K
100/133-
DIS_RST-
DIS_LAN
FDD_WP-
FP_RST-
<3,21> CPUSTOP-
<3,13,14,21,22> SMBCLK
<3,13,14,21,22> SMBDATA
R448 4.7K
R449 X_0
R451 X_0
R452 3.9K
PWROK <21,27>
PCIRST-2 <11,23,32>
RN292 470-REV
RN185 470
RN186 470
P0_BP[0..3] <5>
P1_BP[0..3] <7>
J1
GN_RD-D-5V-CR-A
RN184
8P4R-100
JDB1
D2x5-1:2
DDLED[1..4]
D_LED[1..4]
CN18 180p
CN19 180p
pin 29
pin 56
C585 0.1u
C586 0.1u
EMI solution for MS-3
RN4
1K
RN183 8P4R-680
R450 680
* 25 mils Trace/ 12 mils Space
MICRO-STAR
Title
MS-6501
Size Custom
Document Number
VCORE AJUST
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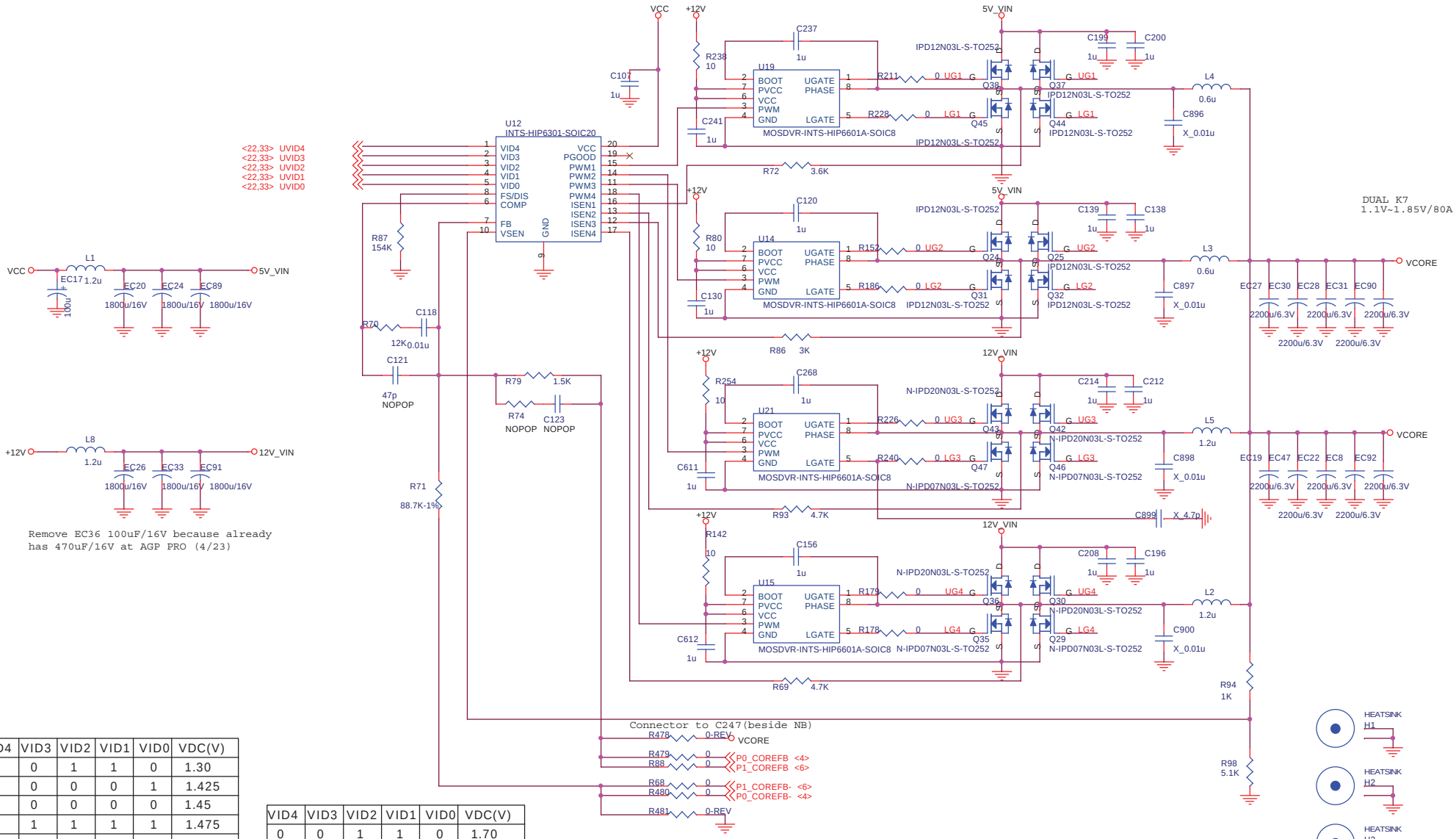
Voltage Regular Module

All N-Channel MOSFET use TO-252



VID4	VID3	VID2	VID1	VID0	VDC(V)
1	0	1	1	0	1.30
1	0	0	0	1	1.425
1	0	0	0	0	1.45
0	1	1	1	1	1.475
0	1	1	1	0	1.500
0	1	1	0	1	1.525
0	1	1	0	0	1.550
0	1	0	1	1	1.575
0	1	0	1	0	1.600
0	1	0	0	1	1.625
0	1	0	0	0	1.650
0	0	1	1	1	1.675
0	0	1	1	0	1.700

VID4	VID3	VID2	VID1	VID0	VDC(V)
0	0	1	1	0	1.70
0	0	1	0	1	1.725
0	0	1	0	0	1.75
0	0	0	1	1	1.775
0	0	0	1	0	1.80
0	0	0	0	1	1.825
0	0	0	0	0	1.85
1	1	1	1	1	NO CPU

Design for 45A @+/- 100 mV

Title	MICRO-STAR MS-6501
Size: Custom	Document Number: VRM
Rev	0C
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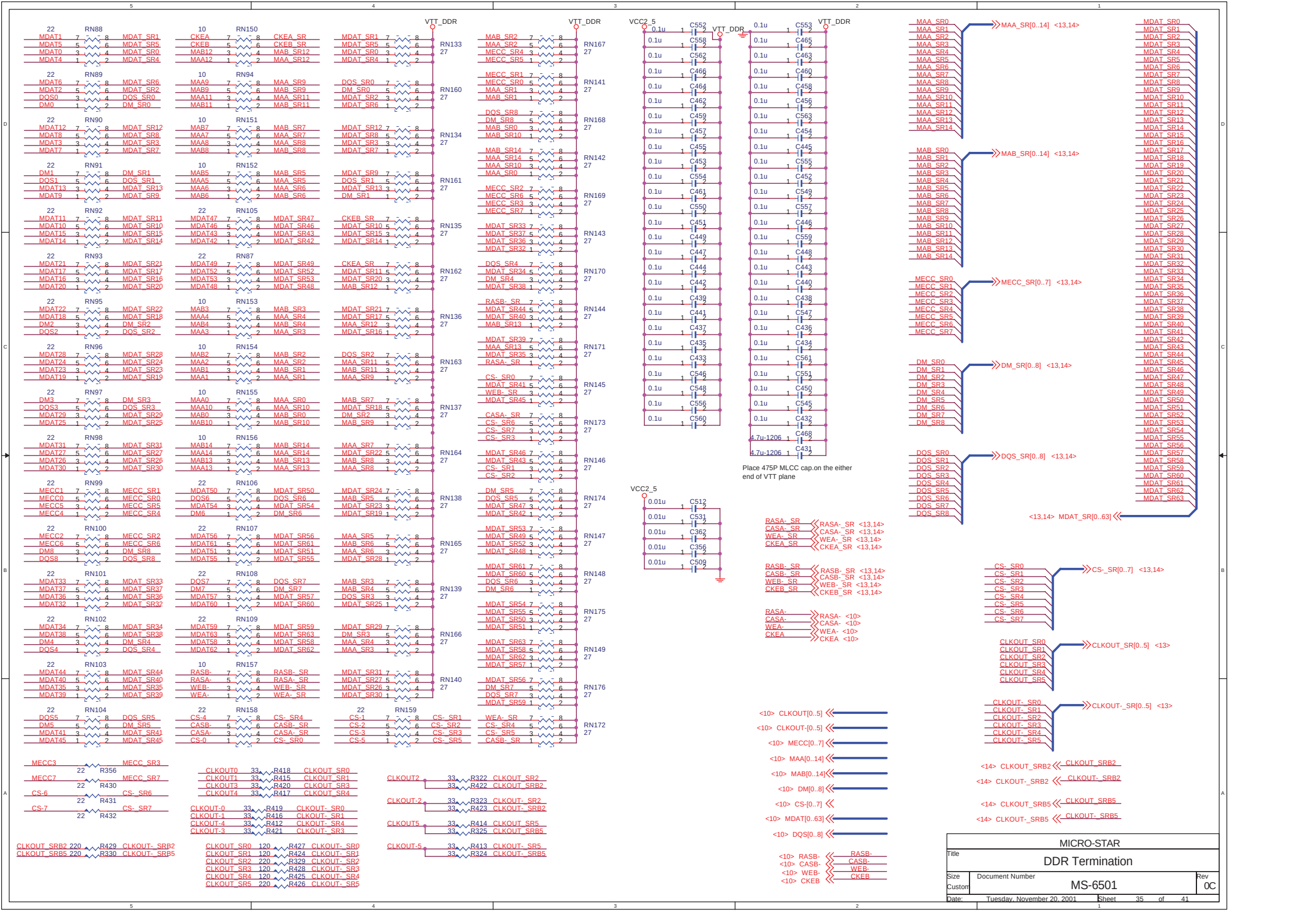
VTT_DDR
VCC2_5
RN88
RN89
RN90
RN91
RN92
RN93
RN95
RN96
RN97
RN98
RN99
RN100
RN101
RN102
RN103
RN104
RN150
RN94
RN151
RN152
RN105
RN87
RN153
RN154
RN155
RN156
RN106
RN107
RN108
RN109
RN157
RN158
RN159
RN133
RN160
RN168
RN134
RN142
RN161
RN135
RN143
RN162
RN170
RN136
RN144
RN171
RN137
RN145
RN163
RN173
RN164
RN146
RN138
RN174
RN165
RN147
RN139
RN148
RN166
RN175
RN149
RN140
RN176
RN172
RN167
RN141
RN169
C552
C553
C558
C465
C562
C463
C466
C460
C464
C458
C462
C456
C459
C563
C457
C454
C455
C445
C453
C555
C554
C452
C461
C549
C550
C557
C451
C446
C449
C559
C447
C448
C444
C443
C442
C440
C439
C438
C441
C547
C437
C436
C435
C434
C433
C561
C546
C551
C548
C450
C556
C545
C560
C432
C468
C431
4.7u-1206
0.1u
0.01u
C512
C531
C362
C356
C509
Place 475P MLCC cap.on the either end of VTT plane
MAA_SR[0..14] <13,14>
MAB_SR[0..14] <13,14>
MECC_SR[0..7] <13,14>
DM_SR[0..8] <13,14>
DQS_SR[0..8] <13,14>
MDAT_SR[0..63] <13,14>
RASA-_SR
CASA-_SR
WEA-_SR
CKEA_SR
RASB-_SR
CASB-_SR
WEB-_SR
CKEB_SR
RASA- <10>
CASA- <10>
WEA- <10>
CKEA <10>
CS-_SR[0..7] <13,14>
CLKOUT_SR[0..5] <13>
CLKOUT-_SR[0..5] <13>
CLKOUT_SRB2
CLKOUT-_SRB2
CLKOUT_SRB5
CLKOUT-_SRB5
<10> CLKOUT[0..5]
<10> CLKOUT-[0..5]
<10> MECC[0..7]
<10> MAA[0..14]
<10> MAB[0..14]
<10> DM[0..8]
<10> CS-[0..7]
<10> MDAT[0..63]
<10> DQS[0..8]
<10> RASB-
<10> CASB-
<10> WEB-
<10> CKEB
MECC3
MECC7
CS-6
CS-7
R356
R430
R431
R432
CLKOUT0
CLKOUT1
CLKOUT3
CLKOUT4
R418
R415
R420
R417
CLKOUT2
CLKOUT-2
CLKOUT5
CLKOUT-5
R322
R422
R323
R423
R414
R325
R413
R324
CLKOUT-0
CLKOUT-1
CLKOUT-4
CLKOUT-3
R419
R416
R412
R421
CLKOUT_SRB2 220
CLKOUT-_SRB5 220
R429
R330
CLKOUT_SR0
CLKOUT_SR1
CLKOUT_SR2
CLKOUT_SR3
CLKOUT_SR4
CLKOUT_SR5
R427
R424
R329
R428
R425
R426
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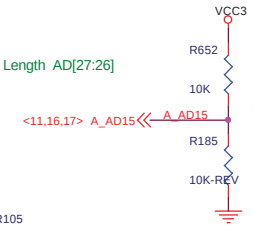
A_AD[11:10] CPU0 Physical S2K Bus Length

00 - Short non-slotA
01 - Single Slot A or "close"
10 - Far dual Slot A
11 - Farthest possible Slot A

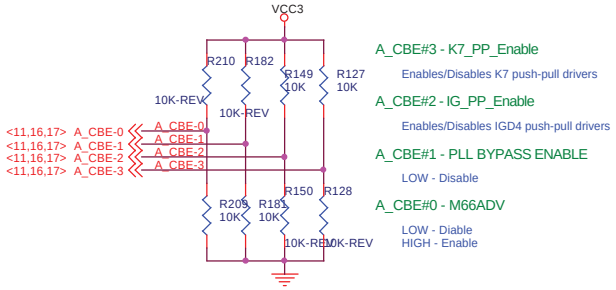
A_AD[27:26] CPU1 Physical S2K Bus Length AD[27:26]

00 - Short non-slotA
01 - Single Slot A or "close"
10 - Far dual Slot A
11 - Farthest possible Slot A



A_AD[15] 66MHz PCI

LOW -> Disable 66MHz PCI Mode
HIGH -> Enable 66MHz PCI Mode



A_CBE#3 - K7_PP_Enable

Enables/Disables K7 push-pull drivers

A_CBE#2 - IG_PP_Enable

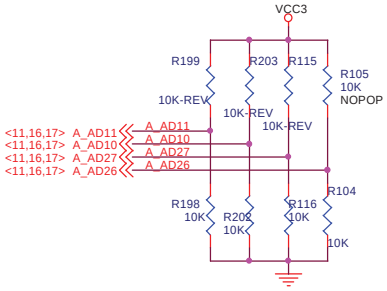
Enables/Disables IGD4 push-pull drivers

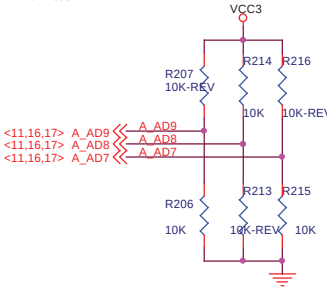
A_CBE#1 - PLL BYPASS ENABLE

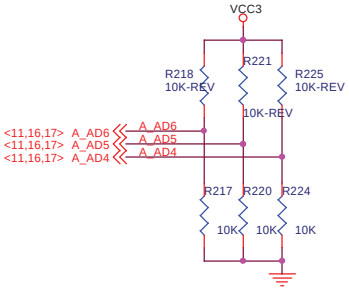
LOW - Disable

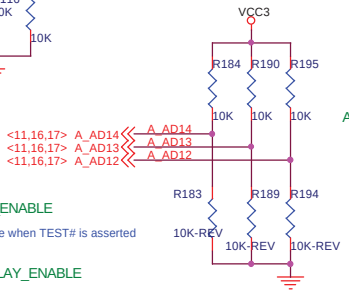
A_CBE#0 - M66ADV

LOW - Diable
HIGH - Enable









A_AD[14:12] AGP CLock Mux[2:0]

Selects input APLL clock mux for PLL test mode.
Refer to Ch. 11 of IGD4 Differences Document

A_AD[9] Bypass_PLLs

Enables PLL bypass mode when TEST# is asserted.

A_AD[8] Outclk_Delay_Enable

Enables K7 OUTCLK delay. Default is disabled.

A_AD[7:5] SysClock_Mux[2:0]

Selects input SPLL clock mux for PLL test mode.
Refer to Ch. 11 of IGD4 Differences Document

A_AD[4] IGD4 Threshhold Range Select for S2k Cells is

Low - Threshold sense set to between 0.6V and 1.0V.
High - S2k Threshold sense set to between 1.0V and 1.4V.

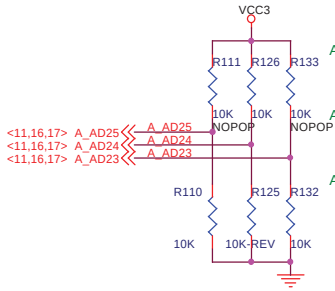
A_AD[31:30] CLK SPEED

L L ---> 100 Mhz (DEFAULT)

L H ---> 66 Mhz

H L ---> RESERVED

H H ---> 133 MHz



A_AD[25] TRISTATE_ENABLE

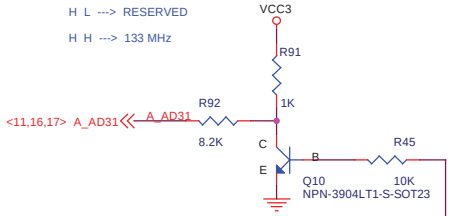
Enables board test mode when TEST# is asserted

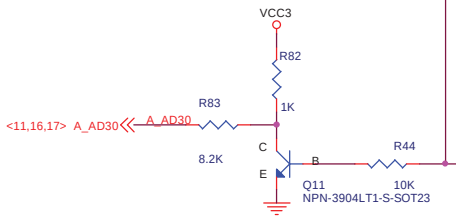
A_AD[24] INCLK_DELAY_ENABLE

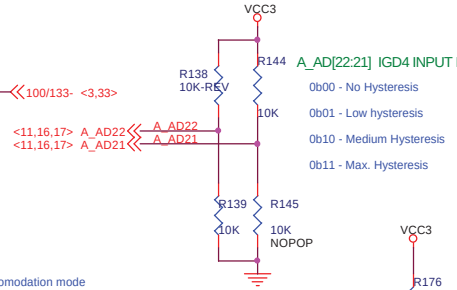
Enables IGD4 INCLK delay

A_AD[23] NAND_TREE_ENABLE

Enables NAND tree test mode when TEST# is asserted

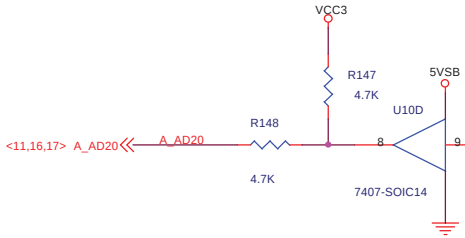






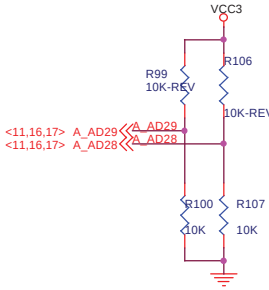
A_AD[22:21] IGD4 INPUT HYSTERISIS OF OUTCLKS

0b00 - No Hysteresis
0b01 - Low hysteresis
0b10 - Medium Hysteresis
0b11 - Max. Hysteresis



A_AD[20] AGP TYPEDET

LOW - AGP Card with VDD_AGP = 1.5V installed
HIGH - AGP Card with VDD_AGP = 3.3V installed

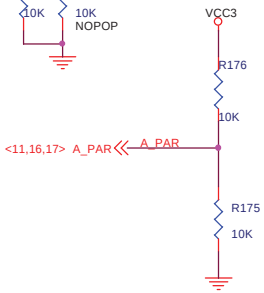


A_AD[29] Disable Divider

LOW - disable large skew accomodation mode
HIGH - enable large skew accomodation mode

A_AD[28] SysClk Threshold

LOW - Senses input thresholds between 0.6V and 1.0V.
HIGH - Senses input thresholds between 1.0V and 1.4V.



A pullup on A_PAR will put IGD4 into clock test mode when TEST# is low

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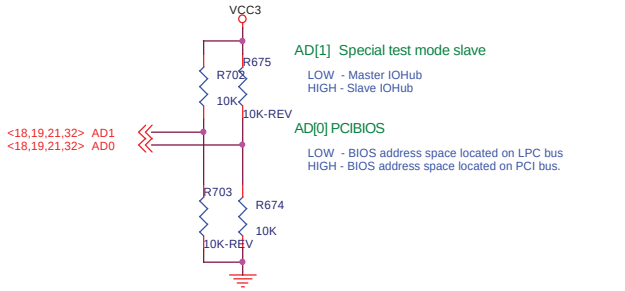


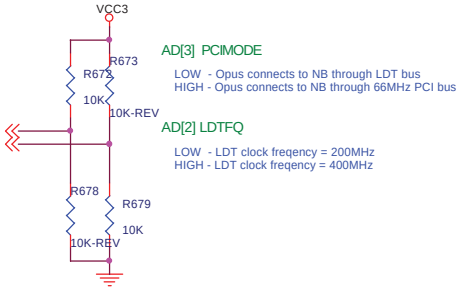
<18,19,21,32> AD1
<18,19,21,32> AD0

AD[1] Special test mode slave

LOW - Master IOHub
HIGH - Slave IOHub

AD[0] PCIBIOS

LOW - BIOS address space located on LPC bus
HIGH - BIOS address space located on PCI bus.



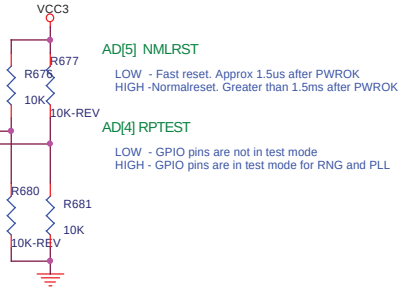
<18,19,21,32> AD3
<18,19,21,32> AD2

AD[3] PCIMODE

LOW - Opus connects to NB through LDT bus
HIGH - Opus connects to NB through 66MHz PCI bus

AD[2] LDTFQ

LOW - LDT clock freqency = 200MHz
HIGH - LDT clock freqency = 400MHz



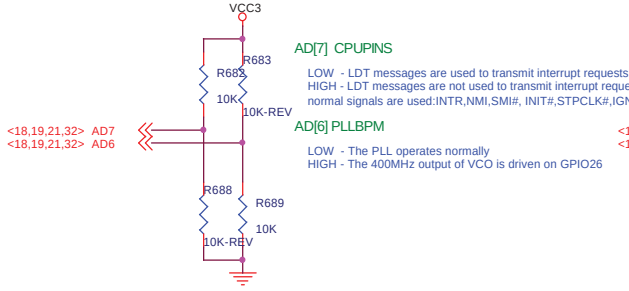
<18,19,21,32> AD5
<18,19,21,32> AD4

AD[5] NMLRST

LOW - Fast reset. Approx 1.5us after PWROK
HIGH -Normalreset. Greater than 1.5ms after PWROK

AD[4] RPTEST

LOW - GPIO pins are not in test mode
HIGH - GPIO pins are in test mode for RNG and PLL



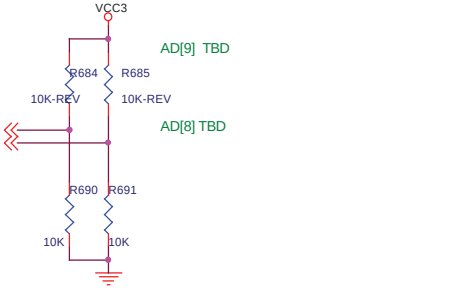
<18,19,21,32> AD7
<18,19,21,32> AD6

AD[7] CPUPINS

LOW - LDT messages are used to transmit interrupt requests
HIGH - LDT messages are not used to transmit interrupt requests. Instead ,the normal signals are used:INTR,NMI,SMI#, INIT#,STPCLK#,IGNNE#,etc.

AD[6] PLLBPM

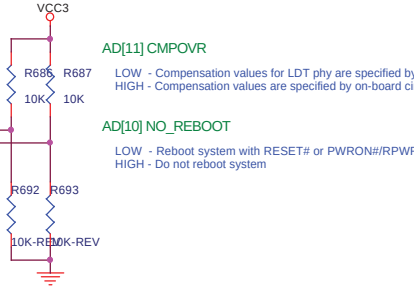
LOW - The PLL operates normally
HIGH - The 400MHz output of VCO is driven on GPIO26



<18,19,21,32> AD9
<18,19,21,32> AD8

AD[9] TBD

AD[8] TBD



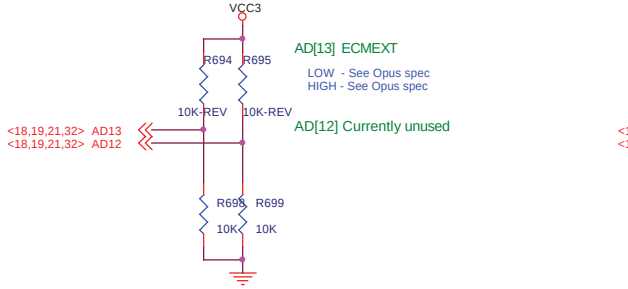
<18,19,21,32> AD11
<18,19,21,32> AD10

AD[11] CMPOVR

LOW - Compensation values for LDT phy are specified by register values
HIGH - Compensation values are specified by on-board circuitry

AD[10] NO_REBOOT

LOW - Reboot system with RESET# or PWRON#/RPWRON signals
HIGH - Do not reboot system

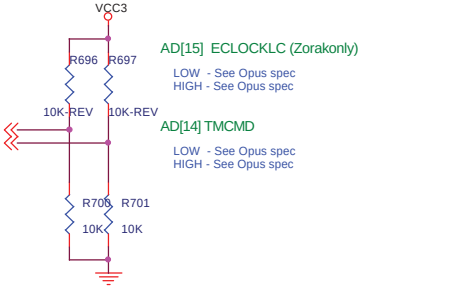


<18,19,21,32> AD13
<18,19,21,32> AD12

AD[13] ECMEXT

LOW - See Opus spec
HIGH - See Opus spec

AD[12] Currently unused



<18,19,21,32> AD15
<18,19,21,32> AD14

AD[15] ECLOCKLC (Zorakonly)

LOW - See Opus spec
HIGH - See Opus spec

AD[14] TMCMD

LOW - See Opus spec
HIGH - See Opus spec

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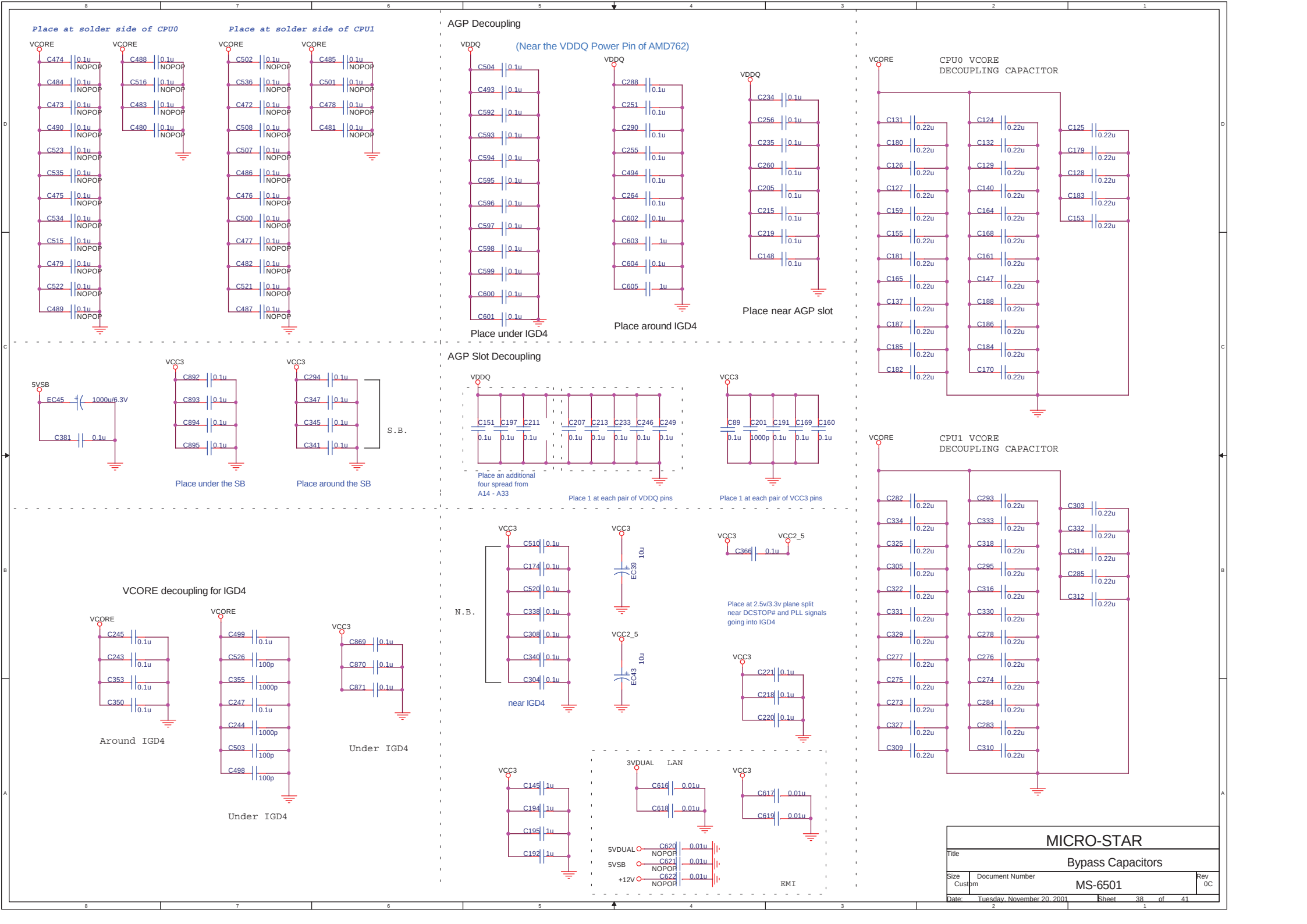
Place at solder side of CPU0
Place at solder side of CPU1
VCORE
C474 0.1u NOPOP
C484 0.1u NOPOP
C473 0.1u NOPOP
C490 0.1u NOPOP
C523 0.1u NOPOP
C535 0.1u NOPOP
C475 0.1u NOPOP
C534 0.1u NOPOP
C515 0.1u NOPOP
C479 0.1u NOPOP
C522 0.1u NOPOP
C489 0.1u NOPOP
C488 0.1u NOPOP
C516 0.1u NOPOP
C483 0.1u NOPOP
C480 0.1u NOPOP
C502 0.1u NOPOP
C536 0.1u NOPOP
C472 0.1u NOPOP
C508 0.1u NOPOP
C507 0.1u NOPOP
C486 0.1u NOPOP
C476 0.1u NOPOP
C500 0.1u NOPOP
C477 0.1u NOPOP
C482 0.1u NOPOP
C521 0.1u NOPOP
C487 0.1u NOPOP
C485 0.1u NOPOP
C501 0.1u NOPOP
C478 0.1u NOPOP
C481 0.1u NOPOP
AGP Decoupling
VDDQ
(Near the VDDQ Power Pin of AMD762)
C504 0.1u
C493 0.1u
C592 0.1u
C593 0.1u
C594 0.1u
C595 0.1u
C596 0.1u
C597 0.1u
C598 0.1u
C599 0.1u
C600 0.1u
C601 0.1u
Place under IGD4
C288 0.1u
C251 0.1u
C290 0.1u
C255 0.1u
C494 0.1u
C264 0.1u
C602 0.1u
C603 1u
C604 0.1u
C605 1u
Place around IGD4
C234 0.1u
C256 0.1u
C235 0.1u
C260 0.1u
C205 0.1u
C215 0.1u
C219 0.1u
C148 0.1u
Place near AGP slot
CPU0 VCORE
DECOUPLING CAPACITOR
C131 0.22u
C180 0.22u
C126 0.22u
C127 0.22u
C159 0.22u
C155 0.22u
C181 0.22u
C165 0.22u
C137 0.22u
C187 0.22u
C185 0.22u
C182 0.22u
C124 0.22u
C132 0.22u
C129 0.22u
C140 0.22u
C164 0.22u
C168 0.22u
C161 0.22u
C147 0.22u
C188 0.22u
C186 0.22u
C184 0.22u
C170 0.22u
C125 0.22u
C179 0.22u
C128 0.22u
C183 0.22u
C153 0.22u
5VSB
EC45 1000u/6.3V
C381 0.1u
VCC3
C892 0.1u
C893 0.1u
C894 0.1u
C895 0.1u
Place under the SB
C294 0.1u
C347 0.1u
C345 0.1u
C341 0.1u
S.B.
Place around the SB
AGP Slot Decoupling
VDDQ
C151 0.1u
C197 0.1u
C211 0.1u
C207 0.1u
C213 0.1u
C233 0.1u
C246 0.1u
C249 0.1u
Place an additional four spread from A14 - A33
Place 1 at each pair of VDDQ pins
VCC3
C89 0.1u
C201 1000p
C191 0.1u
C169 0.1u
C160 0.1u
Place 1 at each pair of VCC3 pins
CPU1 VCORE
DECOUPLING CAPACITOR
C282 0.22u
C334 0.22u
C325 0.22u
C305 0.22u
C322 0.22u
C331 0.22u
C329 0.22u
C277 0.22u
C275 0.22u
C273 0.22u
C327 0.22u
C309 0.22u
C293 0.22u
C333 0.22u
C318 0.22u
C295 0.22u
C316 0.22u
C330 0.22u
C278 0.22u
C276 0.22u
C274 0.22u
C284 0.22u
C283 0.22u
C310 0.22u
C303 0.22u
C332 0.22u
C314 0.22u
C285 0.22u
C312 0.22u
VCORE decoupling for IGD4
VCORE
C245 0.1u
C243 0.1u
C353 0.1u
C350 0.1u
Around IGD4
C499 0.1u
C526 100p
C355 1000p
C247 0.1u
C244 1000p
C503 100p
C498 100p
Under IGD4
VCC3
C869 0.1u
C870 0.1u
C871 0.1u
Under IGD4
N.B.
C510 0.1u
C174 0.1u
C520 0.1u
C338 0.1u
C308 0.1u
C340 0.1u
C304 0.1u
near IGD4
EC39 10u
EC43 10u
VCC2_5
C366 0.1u
Place at 2.5v/3.3v plane split near DCSTOP# and PLL signals going into IGD4
C221 0.1u
C218 0.1u
C220 0.1u
C145 1u
C194 1u
C195 1u
C192 1u
3VDUAL
LAN
C616 0.01u
C618 0.01u
5VDUAL
5VSB
+12V
C620 NOPOP 0.01u
C621 NOPOP 0.01u
C622 NOPOP 0.01u
C617 0.01u
C619 0.01u
EMI
MICRO-STAR
Title
Bypass Capacitors
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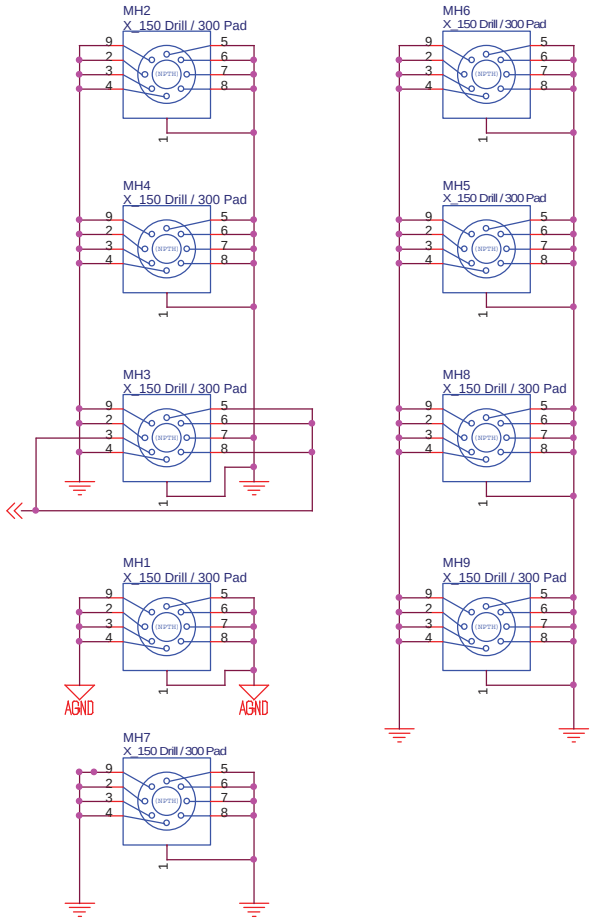
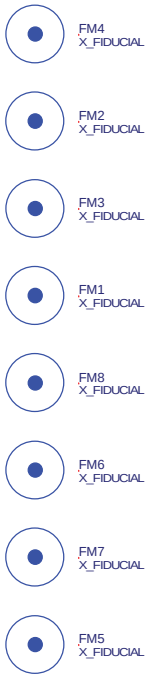
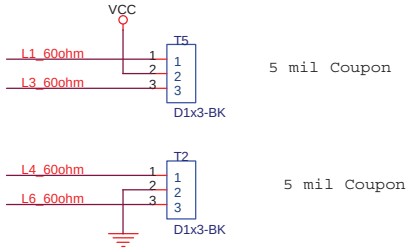
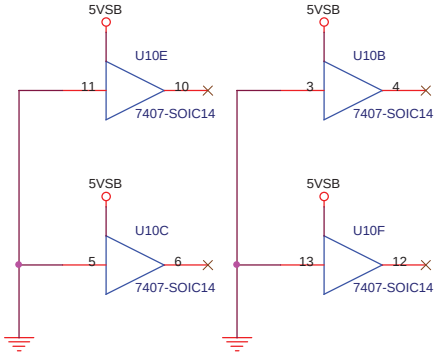
MOUNTING HOLES



FIDUCIALS







MICRO-STAR		
Title: Mounting Hole		
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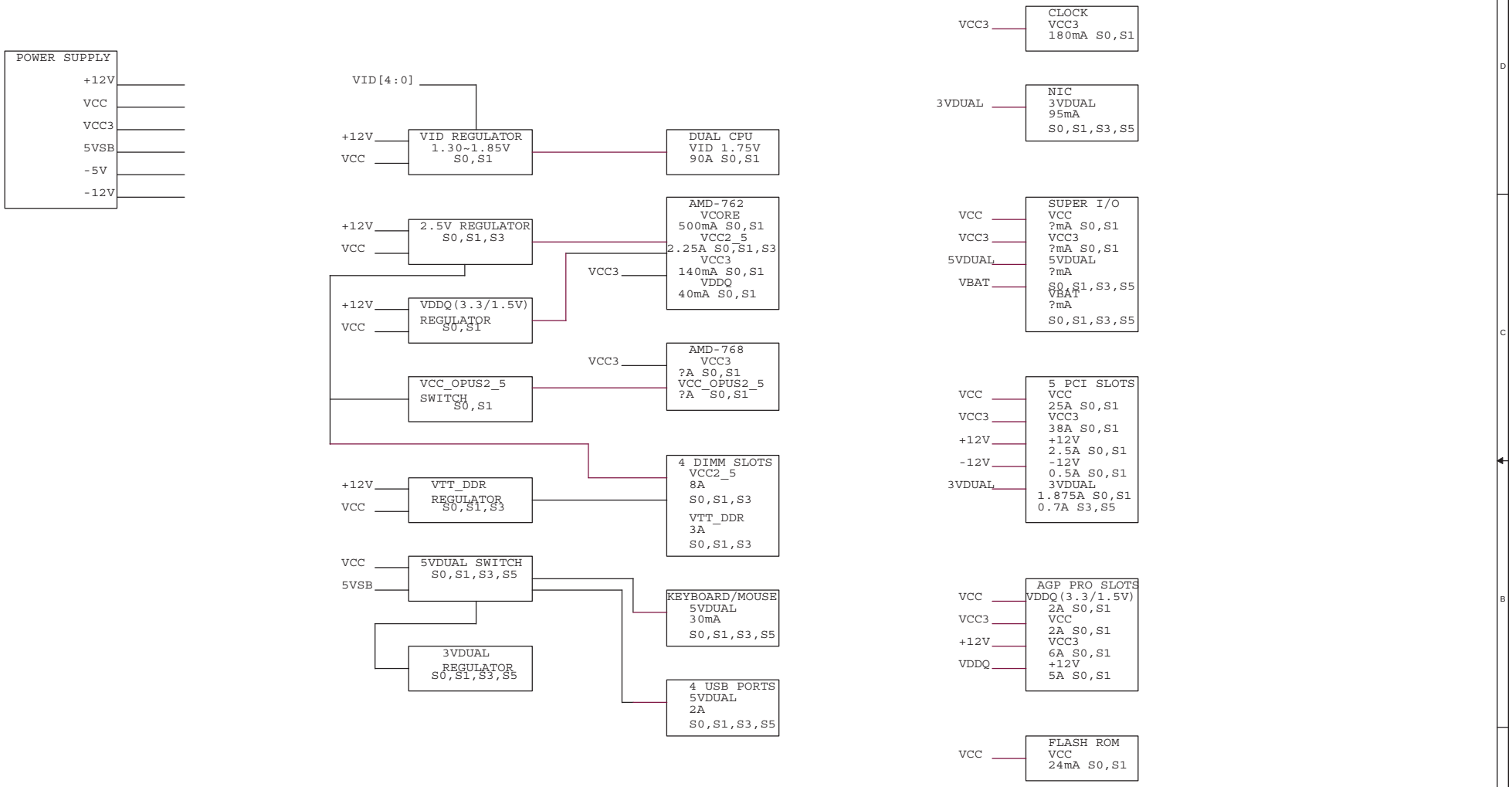

MICRO-STAR		
Title: Power Map		
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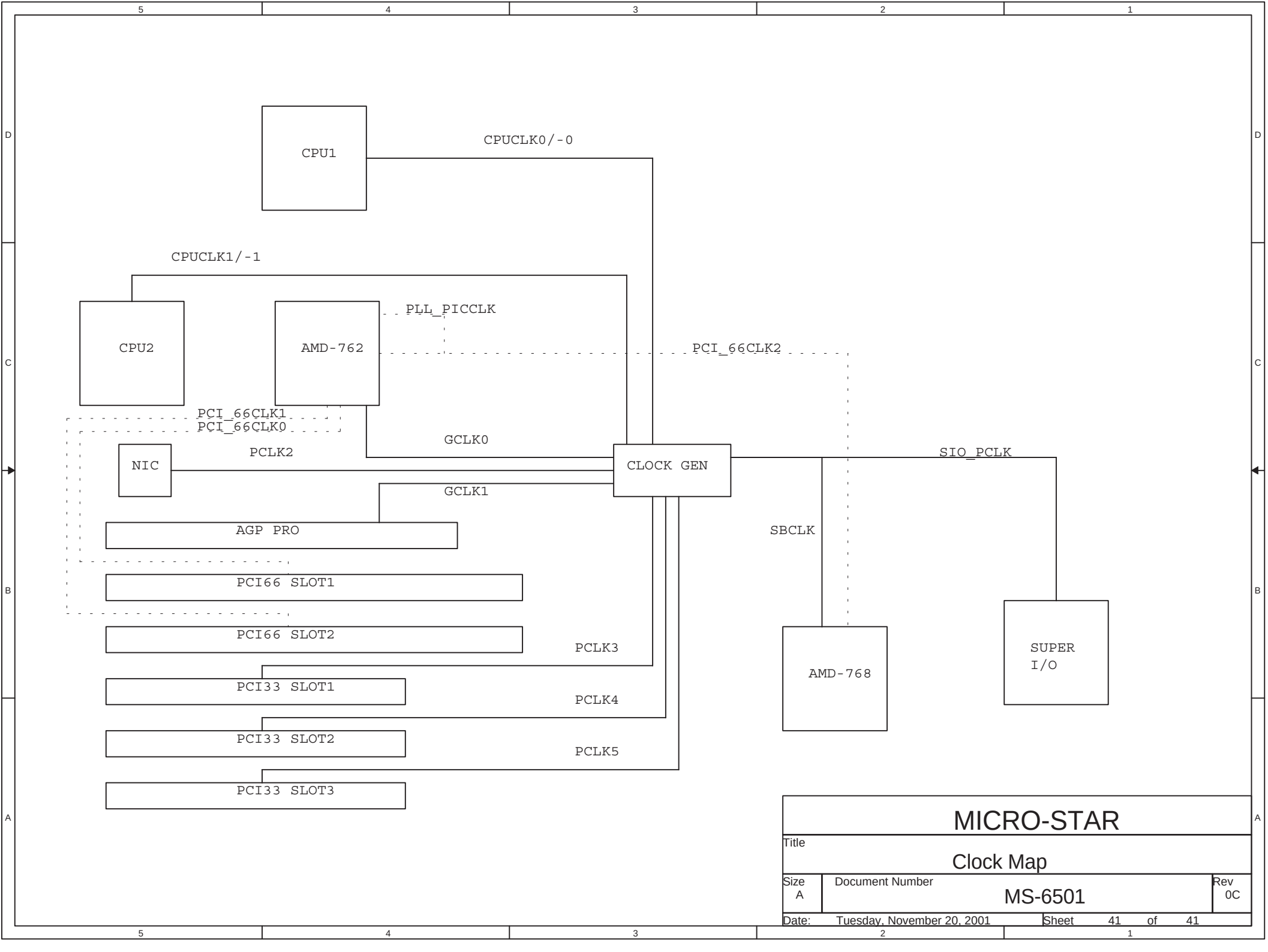

MICRO-STAR

Title: Clock Map

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