MS-6399

Version 1.0
07/23/2001 Update

INTEL (R) Brookdale Chipset
Willamette/Northwood 478pin mPGA-B Processor Schematics

CPU:

Willamette/Northwood mPGA-478B Processor

System Brookdale Chipset:

INTEL MCH (North Bridge) +
INTEL ICH2 (South Bridge)

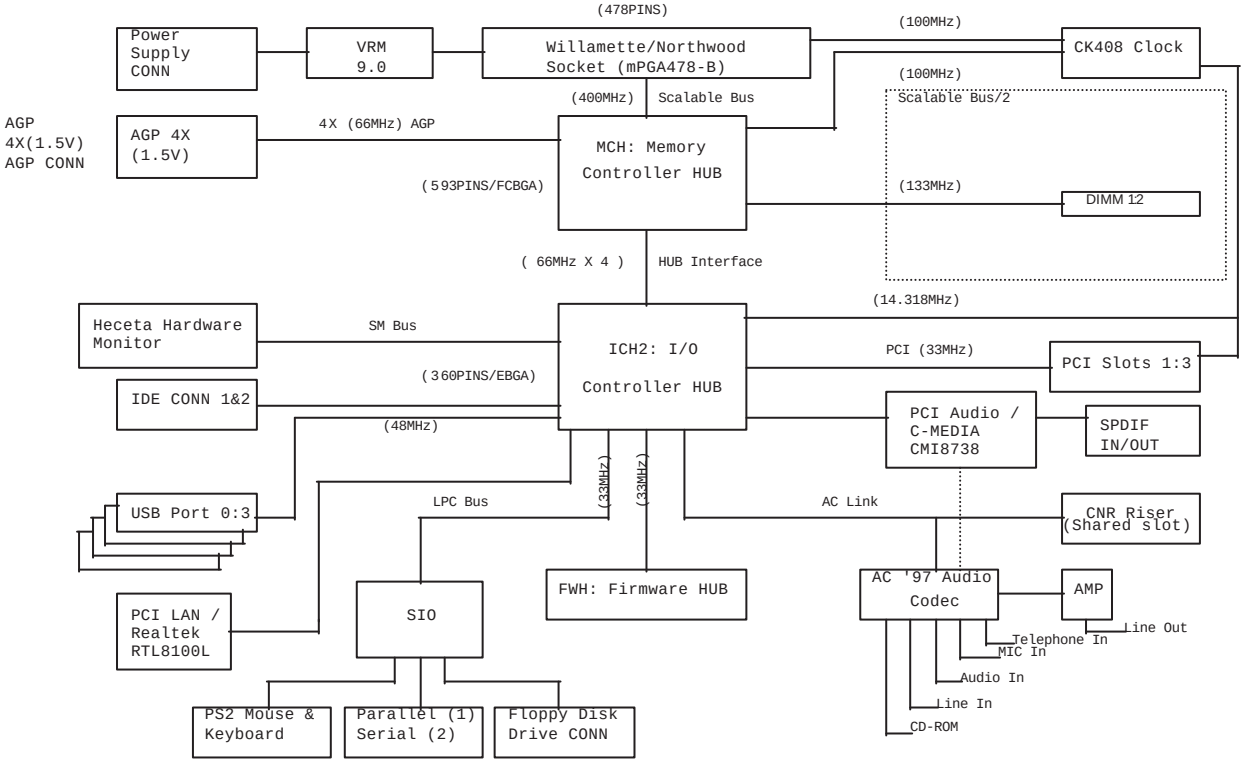
On Board Chipset:

BIOS -- FWH
LPC Super I/O -- W83627HF
Clock Generation -- CY28324
PCI SOUND -- C-MEDIA CMI8738

Expansion Slots:

AGP2.0 SLOT * 1
PCI2.2 SLOT * 3

Micro-Star	Title: *MS-6399*	Rev: *1.0*
Document Number: Cover Sheet		
Last Revision Date: Monday, July 23, 2001	Sheet 1 of 31	



Micro-Star	Title: MS-6399	Rev: 1.0
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General Purpose I/O Spec.

ICH2

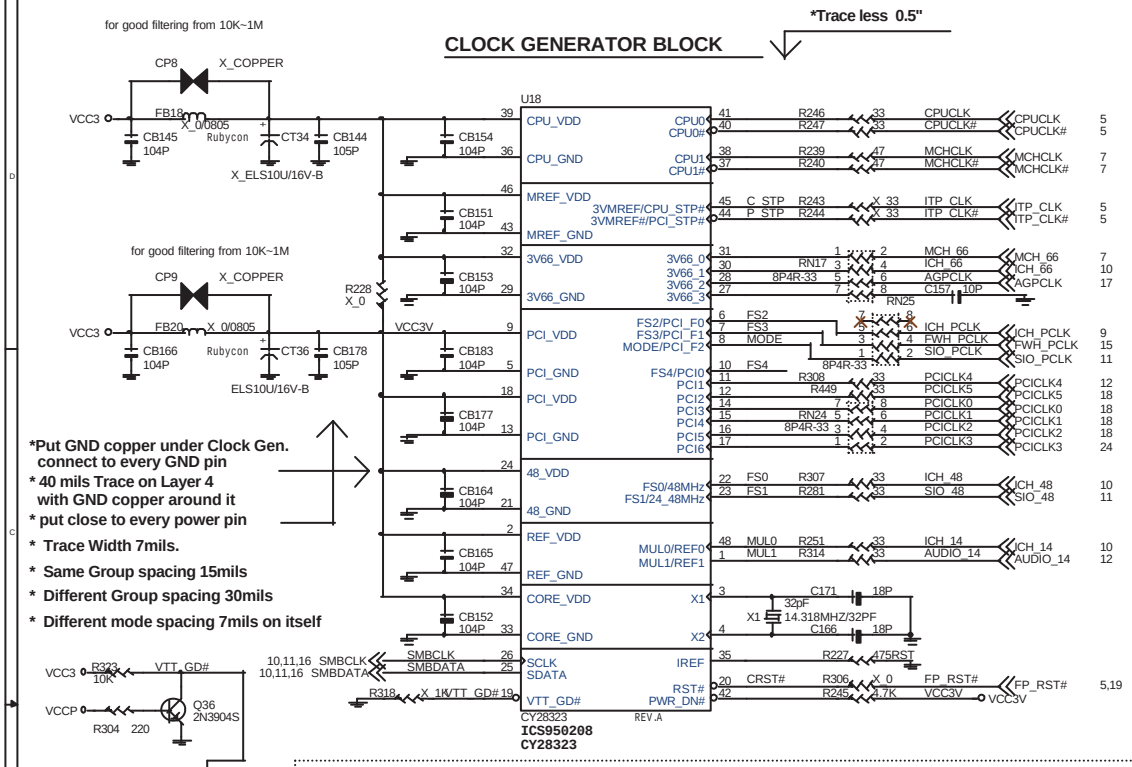
GPIO Pin	Type	Function
GPIO 0	I	Non Connect
GPIO 1	I	Non Connect
GPIO 2~4	I	Not Implemented
GPIO 5	I	Non Connect
GPIO 6	I	AC97 Enabled/Disabled
GPIO 7	I	None
GPIO 8	I	LAN Wake Up
GPIO 9	I	AC'97 Serial Data In
GPIO 10	I	Non Connect
GPIO 11	I	Non Connect
GPIO 12	I	External SMI
GPIO 13	I	LPC PME
GPIO 14~15	I	Not Implemented
GPIO 16	O	Non Connect
GPIO 17	O	Non Connect
GPIO 18	O	Not Implemented
GPIO 19	O	Not Implemented
GPIO 20	O	Non
GPIO 21	O	Not Implemented
GPIO 22	O	Non
GPIO 23	OD	BIOS Locked/Unlocked
GPIO 24	O	Non
GPIO 25	O	Non
GPIO 26	O	Non
GPIO 27	I/O	Non
GPIO 28	I/O	Non
GPIO 29~31	I/O	Not Implemented

FWH

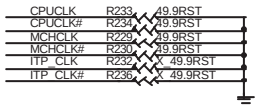
GPIO Pin	Type	Function
GPI 0	I	ATA IDE 1 Detect
GPI 1	I	ATA IDE 2 Detect
GPI 2	I	Reserved
GPI 3	I	Reserved

DEVICE	ICH INT Pin	IDSEL
PCI Slot 1	INTA# INTB# INTC# INTD#	AD16
PCI Slot 2	INTB# INTC# INTD# INTA#	AD17
PCI Slot 3	INTC# INTD# INTA# INTB#	AD18
PCI Audio	INTD#/INTE# INTA# INTB# INTC#	AD23
PCI Lan	INTC#/INTF# INTD# INTA# INTB#	AD22

CLOCK GENERATOR BLOCK



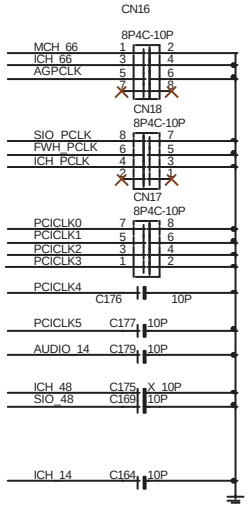
Shut Source Termination Resistors



Trace less 0.2"

49.9ohm for 50ohm M/B impedance

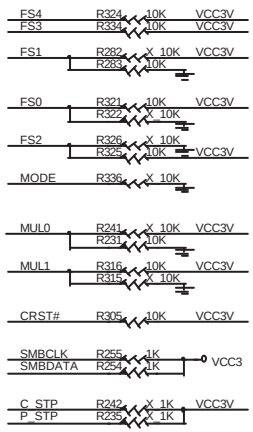
Pull-Down Capacitors



used only for EMI issue

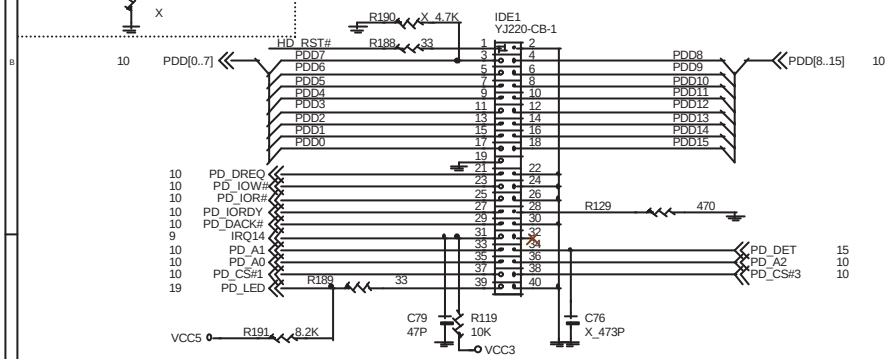
Trace less 0.2"

CLOCK STRAPPING RESISTORS

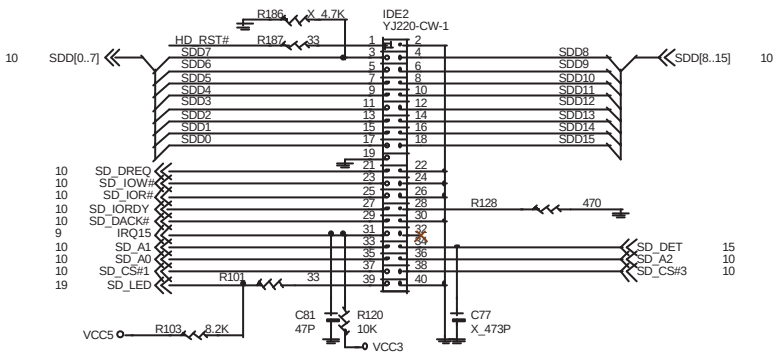


ATA100 IDE CONNECTORS

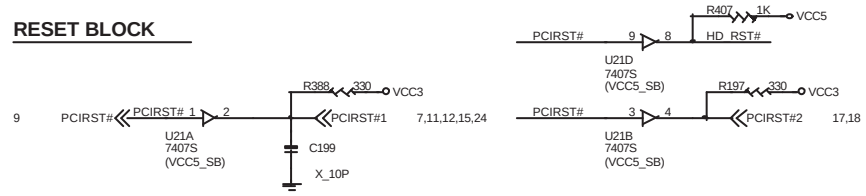
PRIMARY IDE BLOCK



SECONDARY IDE BLOCK



RESET BLOCK



Micro-Star	Title: MS-6399	Rev: 1.0
Document Number: Clock CY28323/4 & ATA100 IDE		
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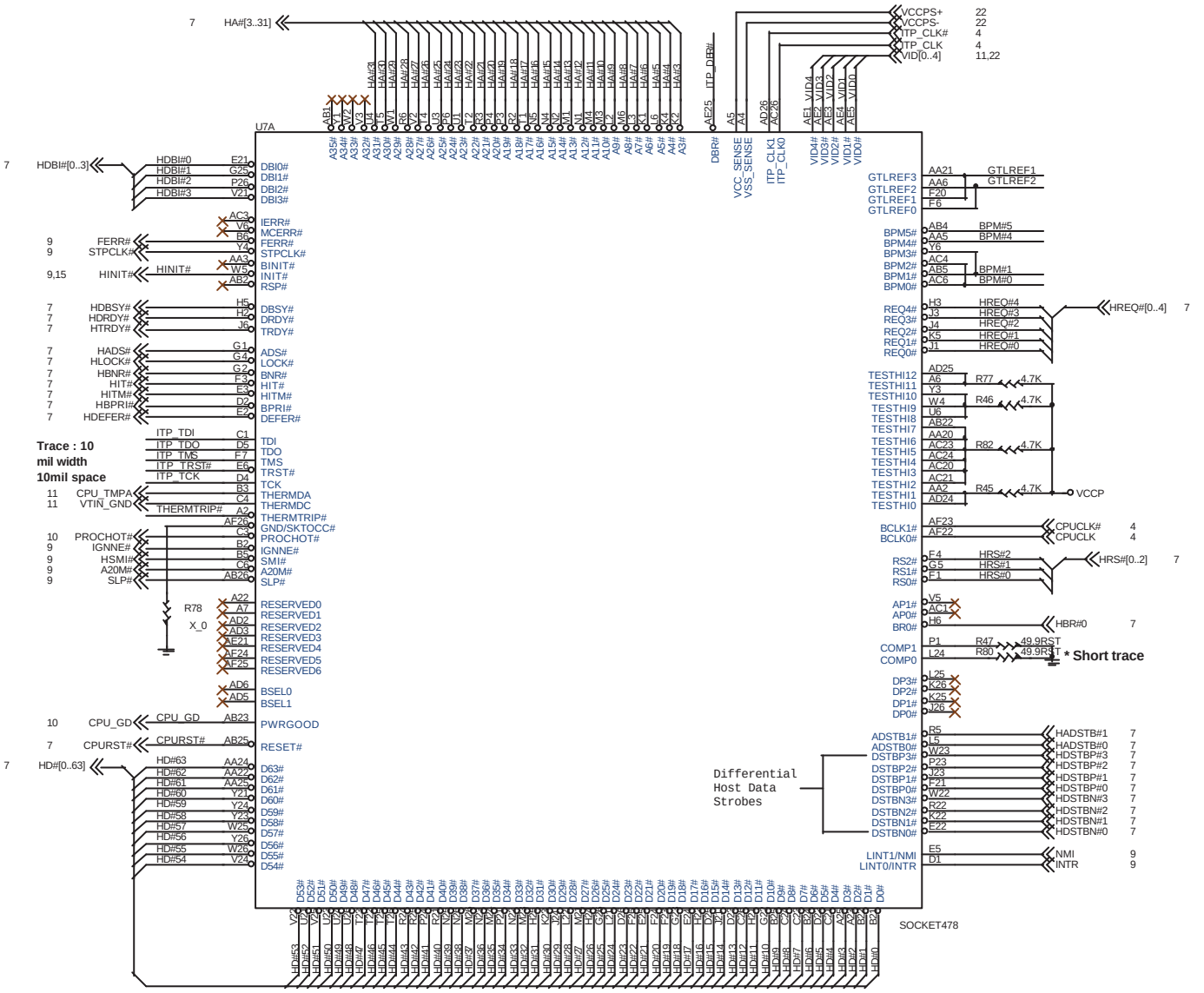
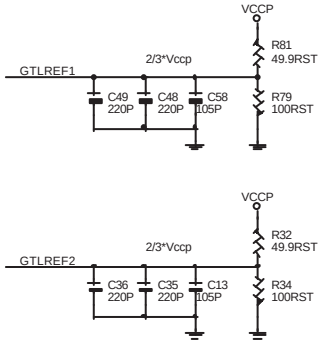
CPU SIGNAL BLOCK

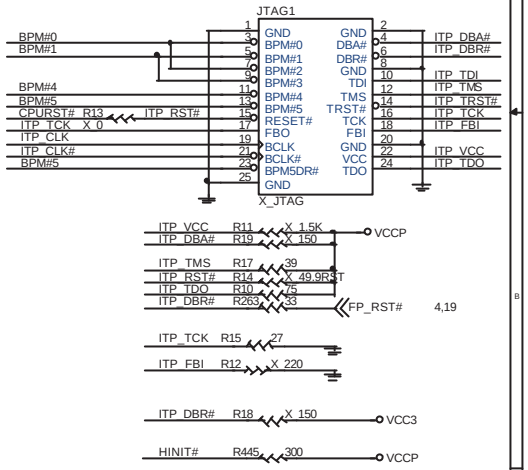


CPU GTL REFERNCE VOLTAGE BLOCK



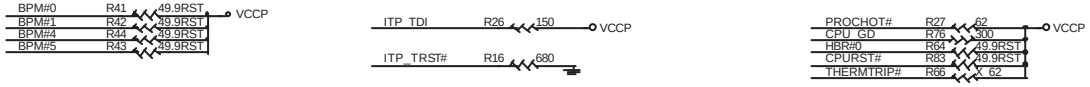
Every pin put one 220pF cap near it.
Trace Width 15mils, Space 15mils.
Keep the voltage dividers within 1.5 inches of the first GTLREF Pin

CPU ITP BLOCK



NO USE ITP COMPORENTS LIST:
1.JTAG1 NC
2.R13 NC
3.R11 NC
4.R14 NC
5.R263 NC
6.R18 NC

CPU STRAPPING RESISTORS



Micro-Star	Title: MS-6399		Rev: 0B
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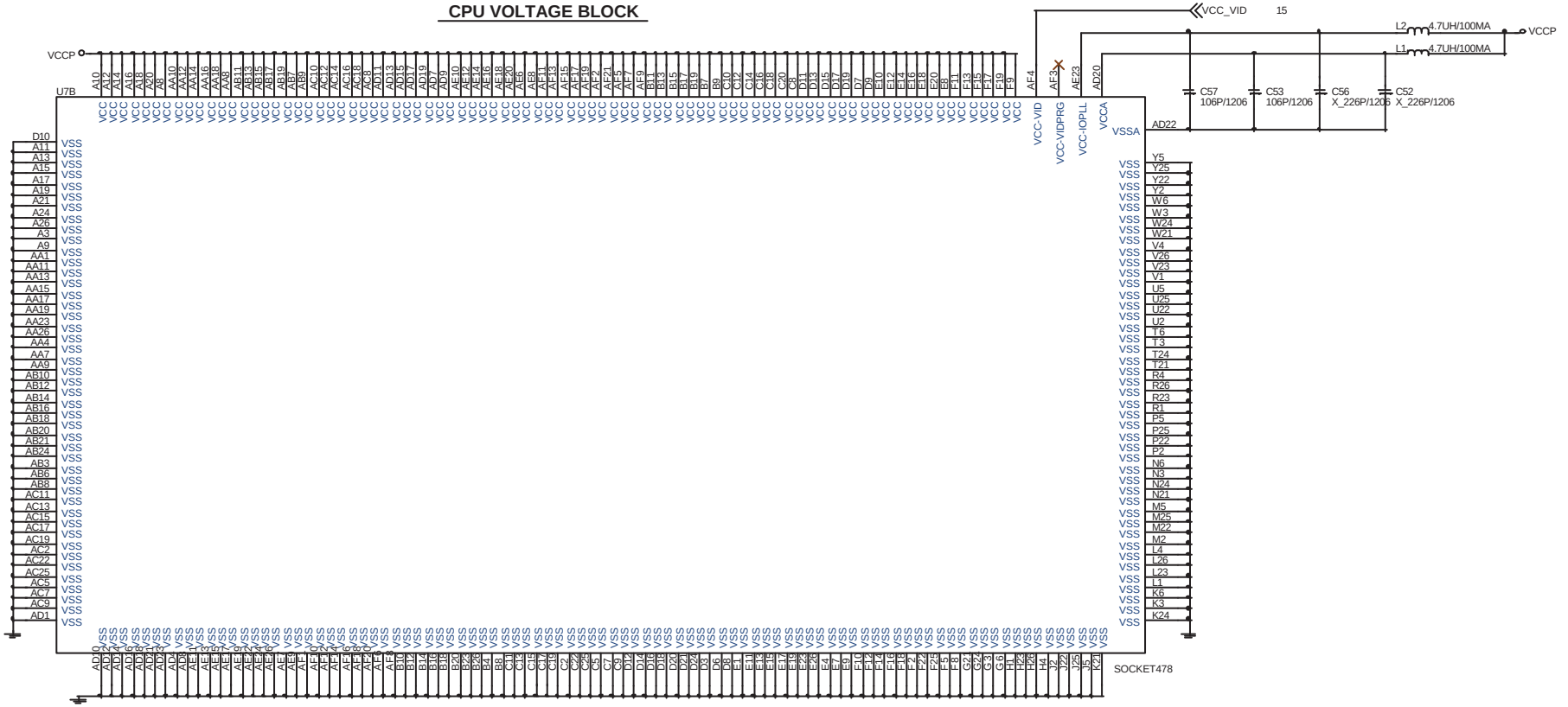
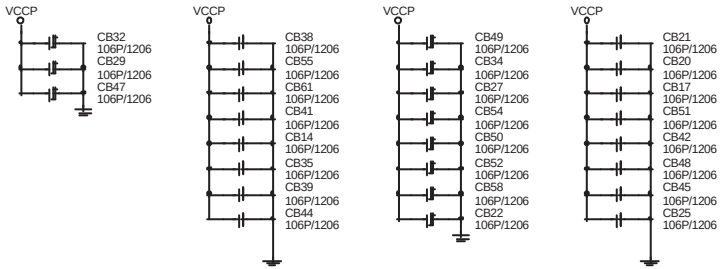
CPU VOLTAGE BLOCK

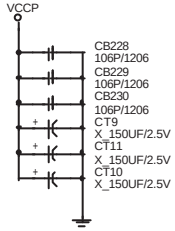


CPU DECOUPLING CAPACITORS



PLACE CAPS WITHIN CPU CAVITY

CPU DECOUPLING CAPACITORS



PLACE CAPS WITHIN CPU CAVITY SOLDER

Micro-Star	Title: MS-6399	Rev: 1.0
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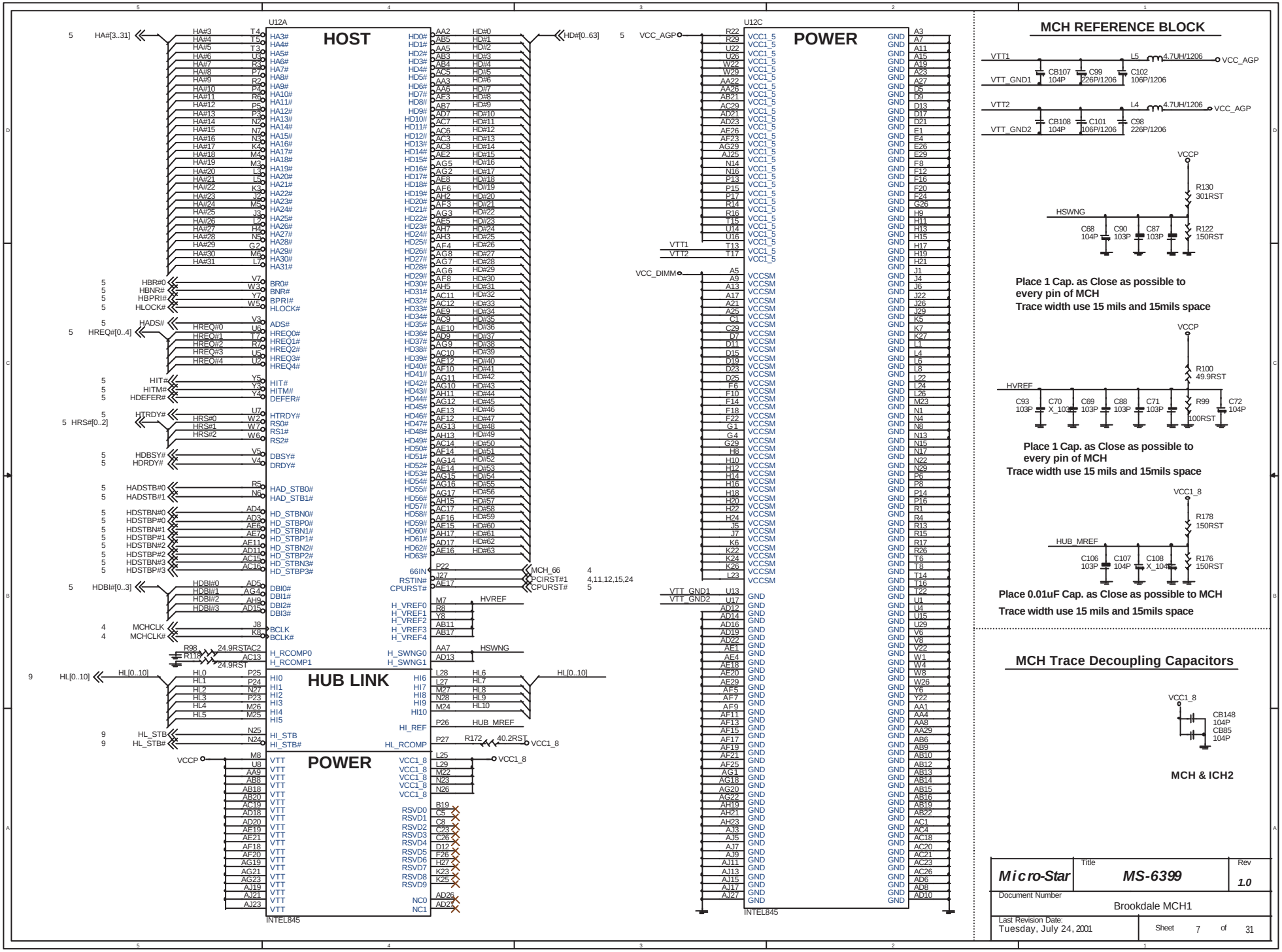
U12A
HOST
HA#[3..31]
HA#3
HA#4
HA#5
HA#6
HA#7
HA#8
HA#9
HA#10
HA#11
HA#12
HA#13
HA#14
HA#15
HA#16
HA#17
HA#18
HA#19
HA#20
HA#21
HA#22
HA#23
HA#24
HA#25
HA#26
HA#27
HA#28
HA#29
HA#30
HA#31
HBR#0
HBNR#
HBPRI#
HLOCK#
HADS#
HREQ#[0..4]
HREQ#0
HREQ#1
HREQ#2
HREQ#3
HREQ#4
HIT#
HITM#
HDEFER#
HTRDY#
HRS#[0..2]
HRS#0
HRS#1
HRS#2
HDBSY#
HDRDY#
HADSTB#0
HADSTB#1
HDSTBN#0
HDSTBP#0
HDSTBN#1
HDSTBP#1
HDSTBN#2
HDSTBP#2
HDSTBN#3
HDSTBP#3
HDBI#[0..3]
HDBI#0
HDBI#1
HDBI#2
HDBI#3
MCHCLK
MCHCLK#
R98 24.9RSTAC2
R119 24.9RST
BR0#
BNR#
BPRI#
HLOCK#
ADS#
HREQ0#
HREQ1#
HREQ2#
HREQ3#
HREQ4#
HIT#
HITM#
DEFER#
HTRDY#
RS0#
RS1#
RS2#
DBSY#
DRDY#
HAD_STB0#
HAD_STB1#
HD_STBN0#
HD_STBP0#
HD_STBN1#
HD_STBP1#
HD_STBN2#
HD_STBP2#
HD_STBN3#
HD_STBP3#
DBI0#
DBI1#
DBI2#
DBI3#
BCLK
BCLK#
H_RCOMP0
H_RCOMP1
HD[0..63]
HD#0
HD#1
HD#2
HD#3
HD#4
HD#5
HD#6
HD#7
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HD#9
HD#10
HD#11
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HD#58
HD#59
HD#60
HD#61
HD#62
HD#63
66IN
RSTIN#
CPURST#
H_VREF0
H_VREF1
H_VREF2
H_VREF3
H_VREF4
H_SWNG0
H_SWNG1
HVREF
HSWNG
MCH_66
PCIRST#1
CPURST#
4
4,11,12,15,24
5
HUB LINK
HL[0..10]
HL0
HL1
HL2
HL3
HL4
HL5
HI0
HI1
HI2
HI3
HI4
HI5
HI6
HI7
HI8
HI9
HI10
HI_REF
HI_STB
HI_STB#
HL_RCOMP
HUB_MREF
40.2RST
POWER
VCCP
VTT
VCC1_8
RSVD0
RSVD1
RSVD2
RSVD3
RSVD4
RSVD5
RSVD6
RSVD7
RSVD8
RSVD9
NC0
NC1
INTEL845
U12C
POWER
VCC_AGP
VCC_DIMM
VTT1
VTT2
VTT_GND1
VTT_GND2
VCC1_5
VCCSM
GND
INTEL845
MCH REFERENCE BLOCK
VTT1
VTT_GND1
CB107 104P
C99 226P/1206
C102 106P/1206
L5 4.7UH/1206
VCC_AGP
VTT2
VTT_GND2
CB108 104P
C101 106P/1206
C98 226P/1206
L4 4.7UH/1206
VCCP
R130 301RST
HSWNG
C68 104P
C90 103P
C87 103P
R122 150RST
Place 1 Cap. as Close as possible to every pin of MCH
Trace width use 15 mils and 15mils space
R100 49.9RST
HVREF
C93 103P
C70 X_103P
C69 103P
C88 103P
C71 103P
R99 100RST
C72 104P
Place 1 Cap. as Close as possible to every pin of MCH
Trace width use 15 mils and 15mils space
VCC1_8
R178 150RST
HUB_MREF
C106 103P
C107 104P
C108 X_104P
R176 150RST
Place 0.01uF Cap. as Close as possible to MCH
Trace width use 15 mils and 15mils space
MCH Trace Decoupling Capacitors
VCC1_8
CB148 104P
CB85 104P
MCH & ICH2
Micro-Star
Title
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Document Number
Brookdale MCH1
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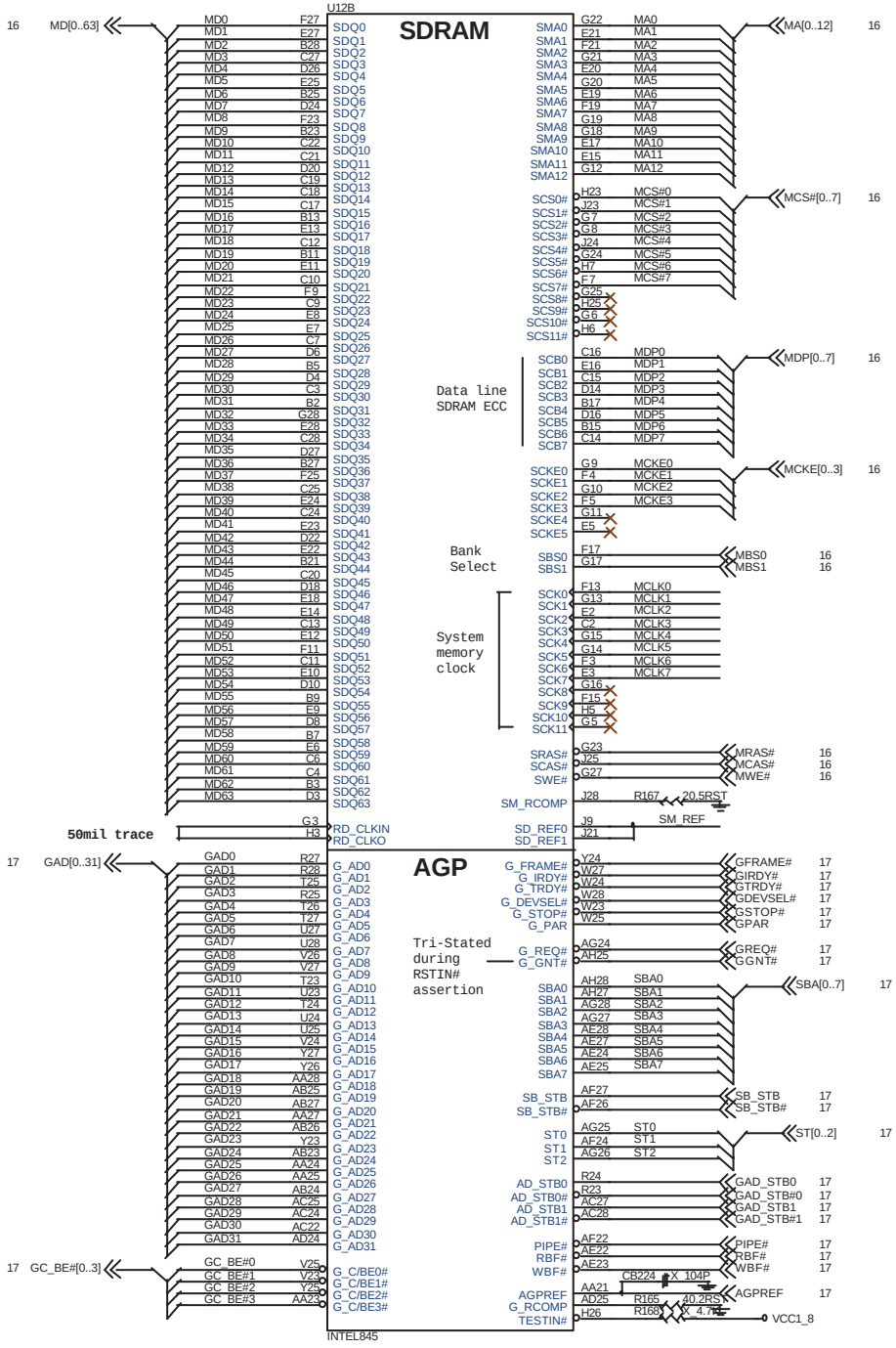
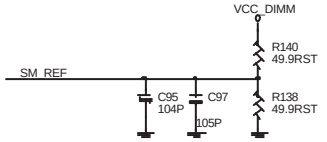
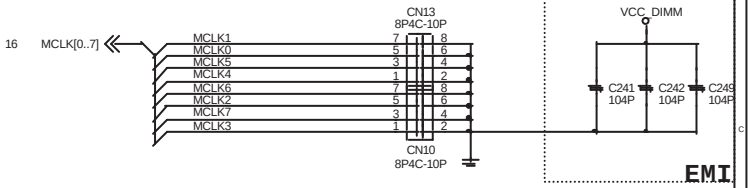


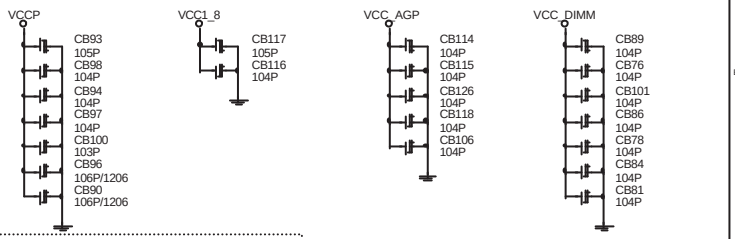
MCH REFERENCE VOLTAGE



MCH MEMORY CLOCK RC CIRCUITS



MCH DECOUPLING CAPACITOR



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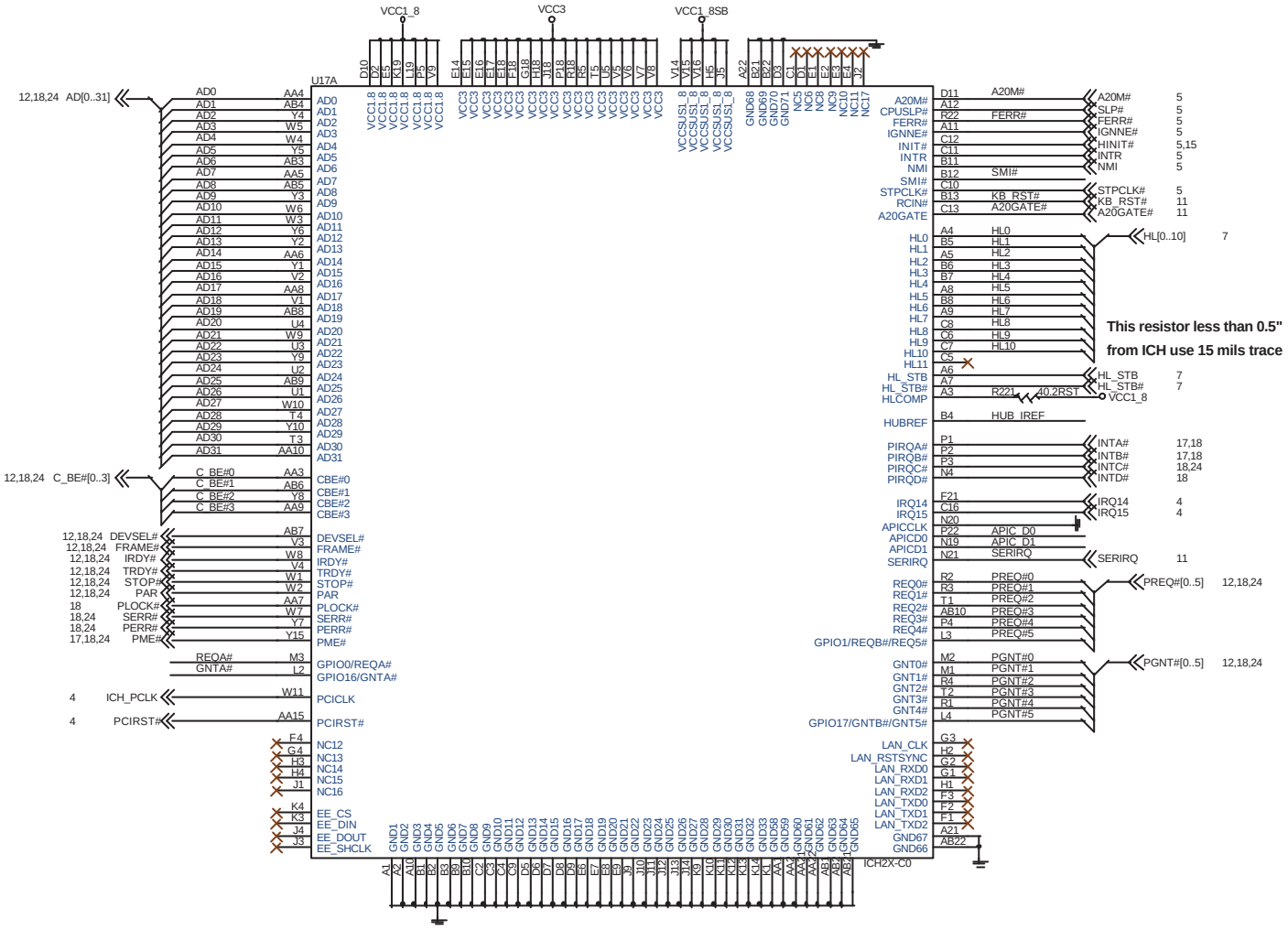
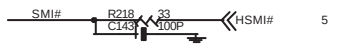
ICH2 PCI / HUB LINK / CPU / LAN / INTERRUPT SIGNALS

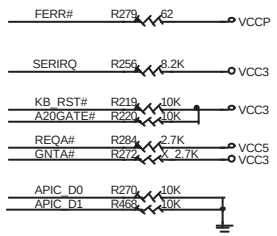


This resistor less than 0.5" from ICH use 15 mils trace

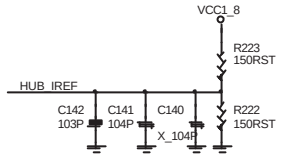
ICH2 SMI# SIGNAL



ICH2 STRAPPING RESISTORS

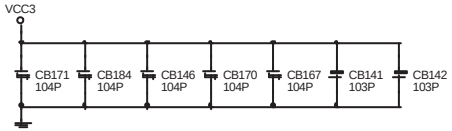


ICH2 REFERENCE VOLTAGE

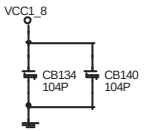


Place Cap. as Close as possible to ICH2
Trace width use 15 mils and 15mils space

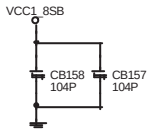
ICH2 DECOUPLING CAPACITORS



Place one 0.1U/0.01U pair in each corner and 2 on opposite sides close to ICH2 if it fit



Distribute near the 1.8V power pin of the ICH2



Distribute near the VCC1_8SB Power pin of the ICH2

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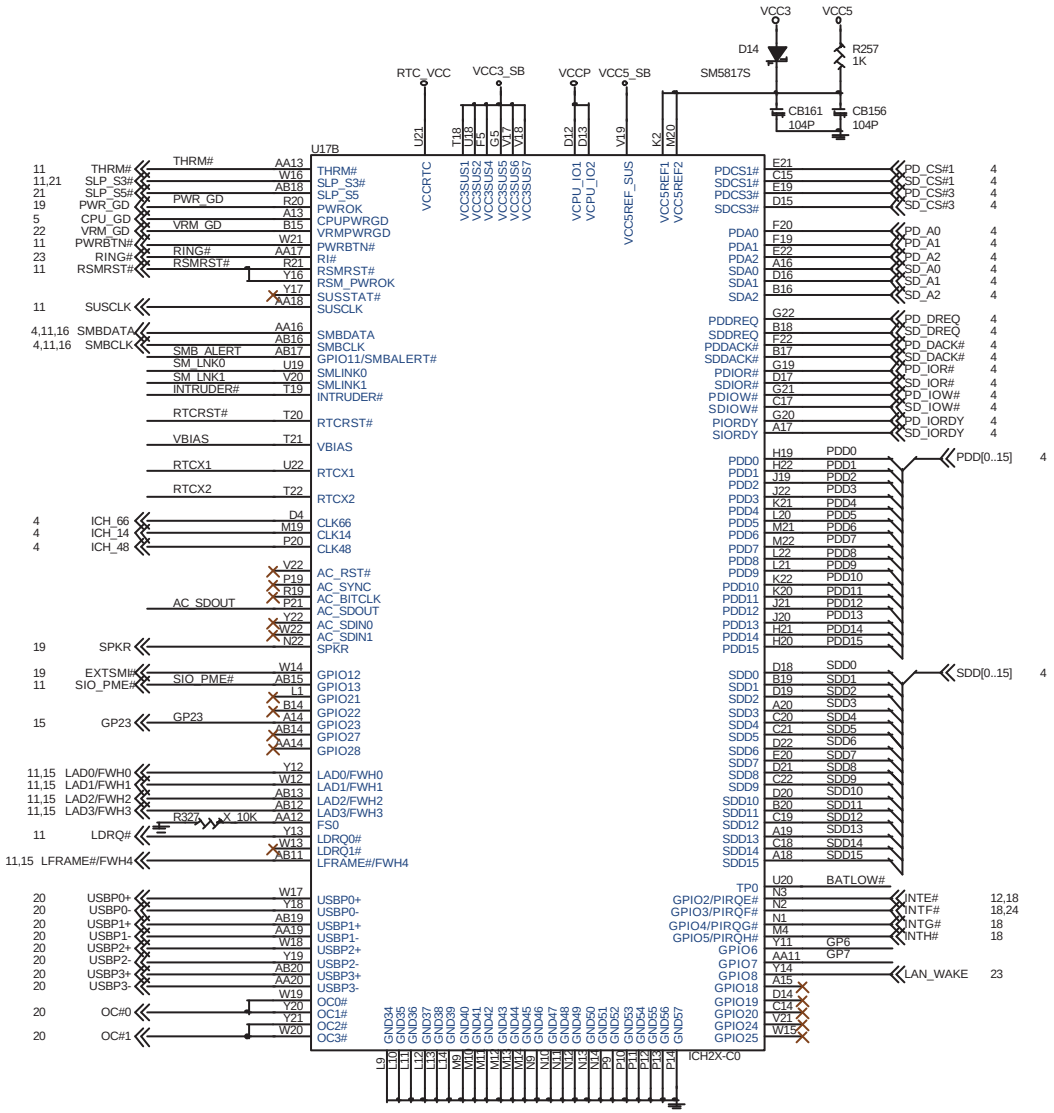
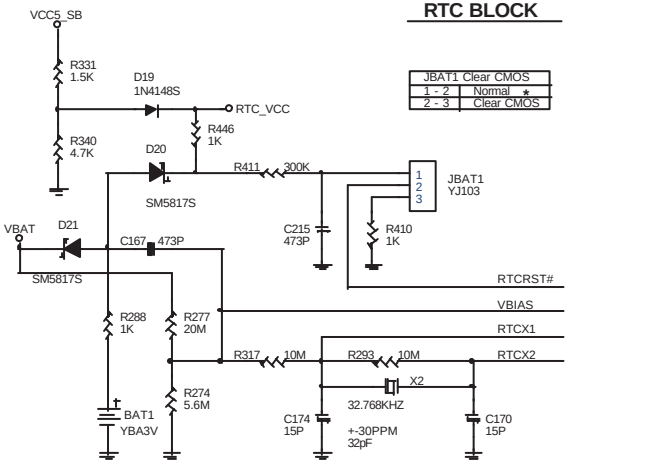
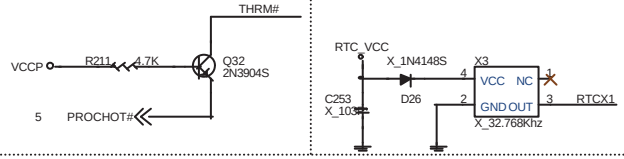
ICH2 ASIC / RTC / AC'97 / GPIO / LPC / USB / IDE SIGNALS



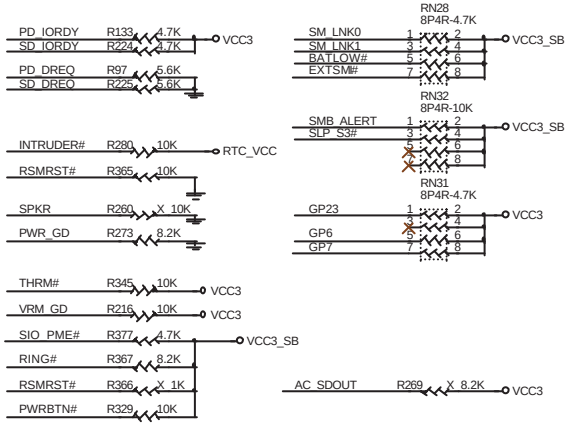
RTC BLOCK



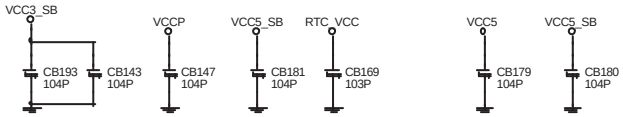
PROCHOT BLOCK



ICH2 STRAPPING RESISTORS



ICH2 DECOUPLING CAPACITOR



Distribute near the VCC3_SB power pin of the ICH

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	Document Number: Brookdale ICH2 Other	
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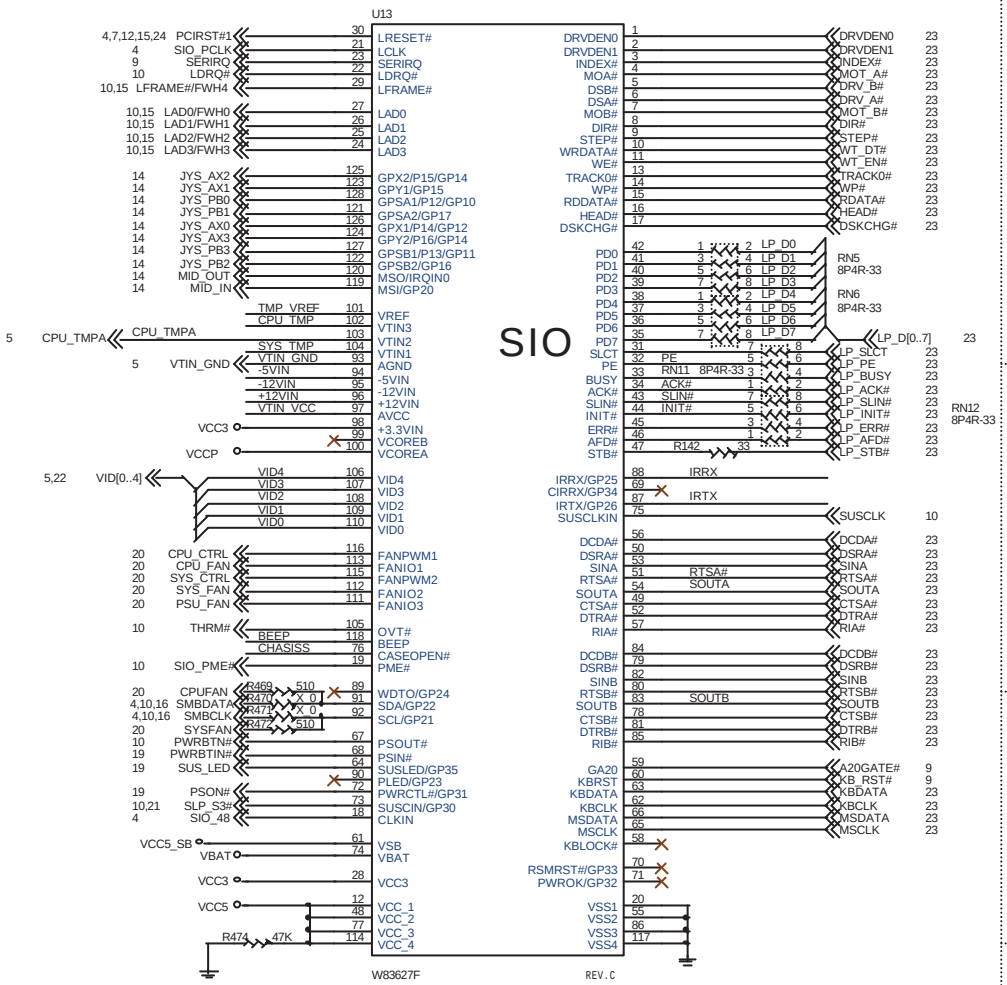
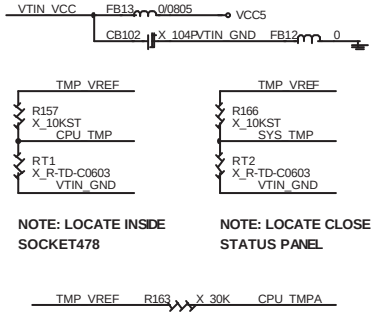
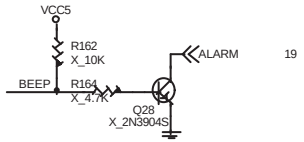
LPC SUPER I/O W83627HF



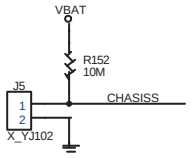
THERMAL RESISTOR BLOCK



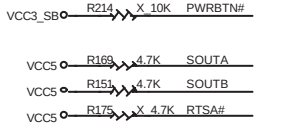
SPEAKER BLOCK



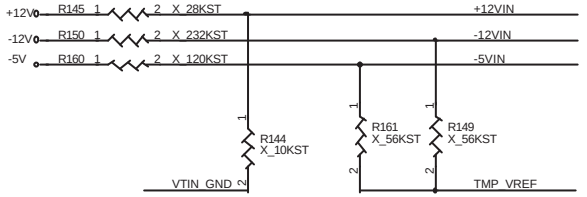
CHASISS INTRUSION HEADER



SUPER I/O STRAPPING RESISTOR

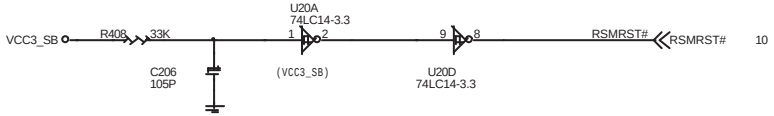


SOUTA	L: Disable KBC	H: Enable KBC
SOUTB	L: 24MHZ	H: 48MHZ
RTSA#	L: CFAD=2E	H: CFAD=4E
DTRA#	L: PNP Default	H: PNP no Default

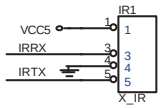


RESUME RESET CIRCUIT BLOCK

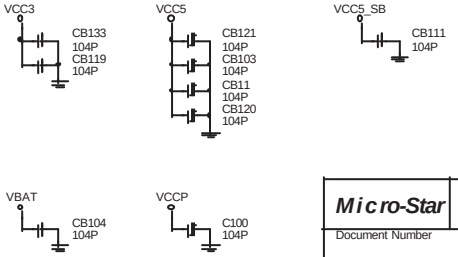
Stuff all for D Version bug



IR HEADER



DECOUPLING CAPACITOR



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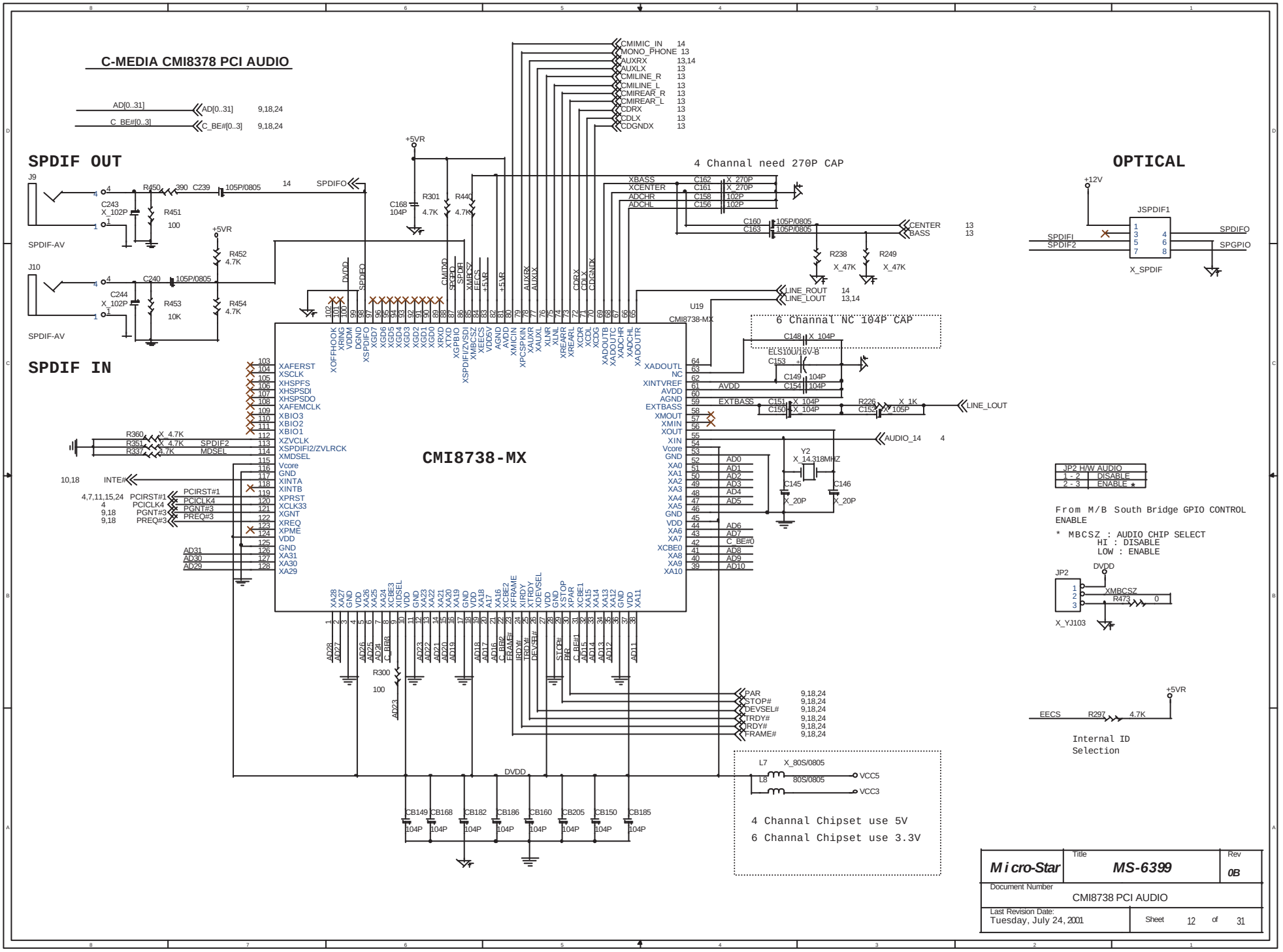
C-MEDIA CMI8378 PCI AUDIO
SPDIF OUT
SPDIF IN
OPTICAL
CMI8738-MX
4 Channal need 270P CAP
6 Channal NC 104P CAP
From M/B South Bridge GPIO CONTROL ENABLE
* MBCSZ : AUDIO CHIP SELECT
HI : DISABLE
LOW : ENABLE
Internal ID Selection
4 Channal Chipset use 5V
6 Channal Chipset use 3.3V
Micro-Star
MS-6399
0B
CMI8738 PCI AUDIO
Tuesday, July 24, 2001
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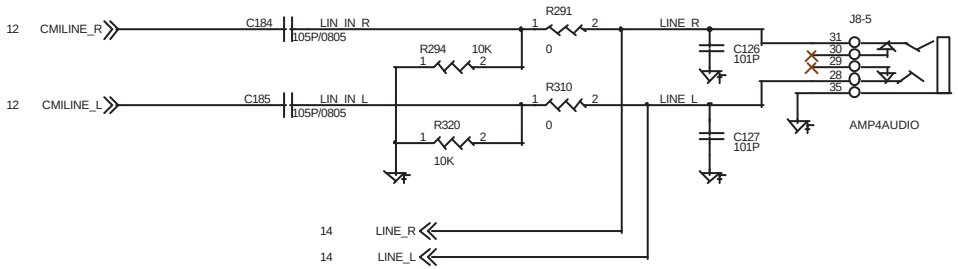
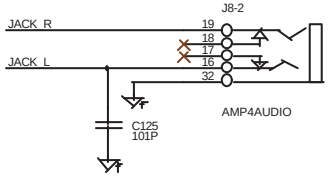
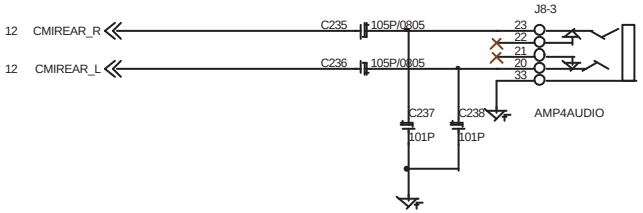
LINE-IN JACK



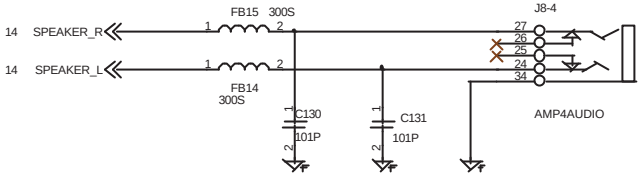
CENTER/BASS JACK



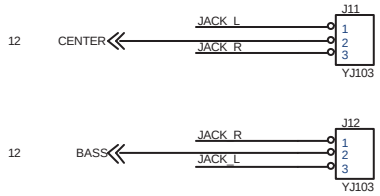
REAL JACK



SPEAKER OUT JACK

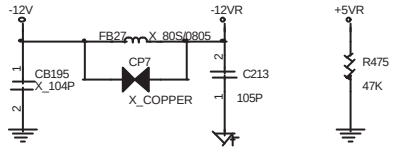


Support Creative Labs!

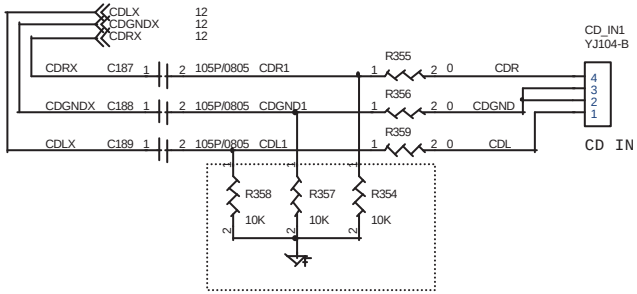


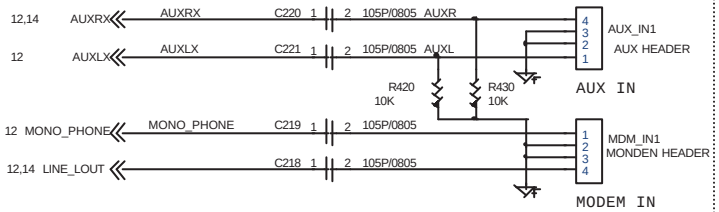
J11	J12	Connection Scheme
1-2	1-2	Mode1 Center to left Channel/Subwoofer to right channel
*2-3	2-3	Mode2 Center to right Channel/Subwoofer to left channel

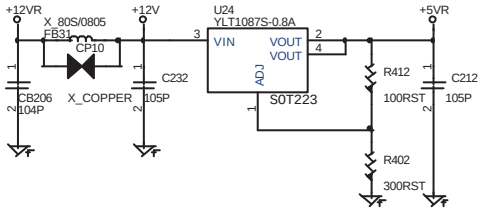
AUDIO CODE REGULATORS



AUDIO CODE CD / AUX / MODEM IN HEADERS







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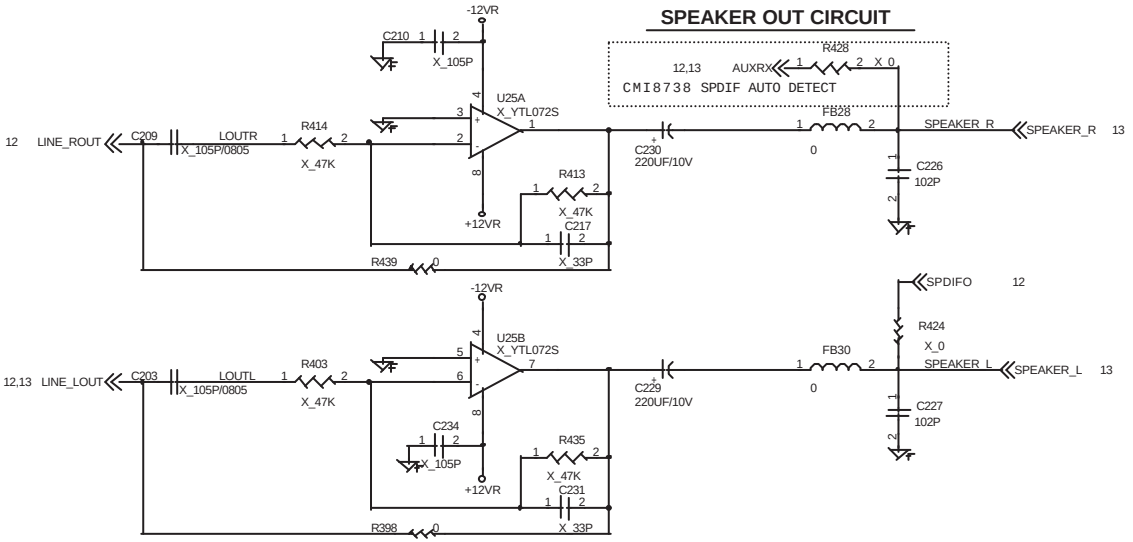
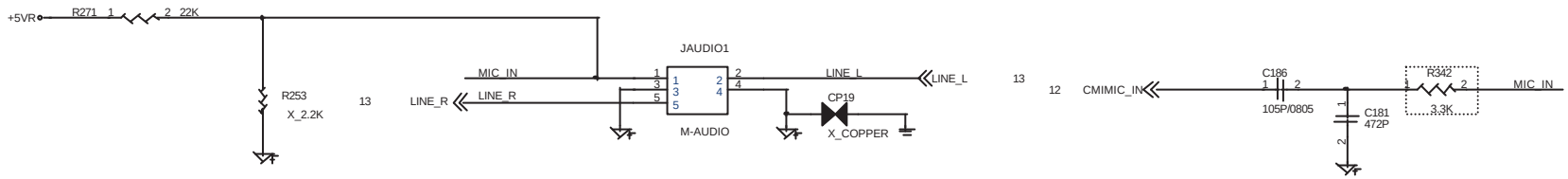
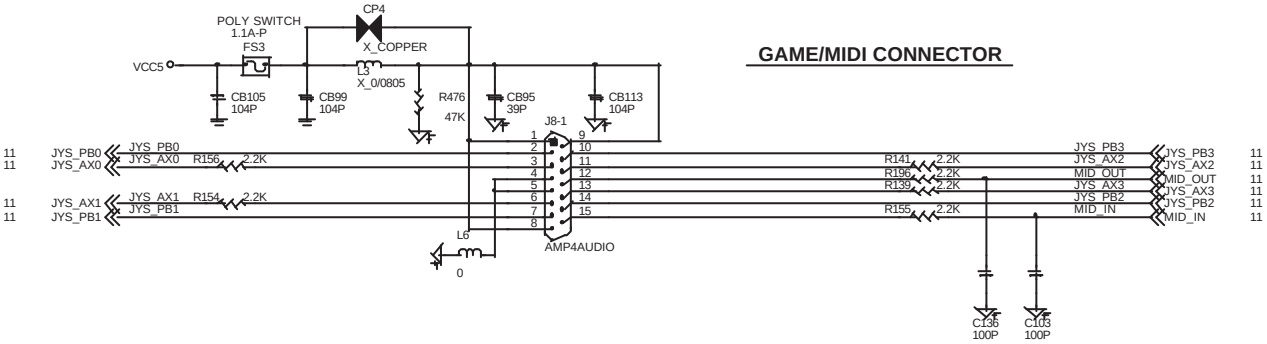
SPEAKER OUT CIRCUIT

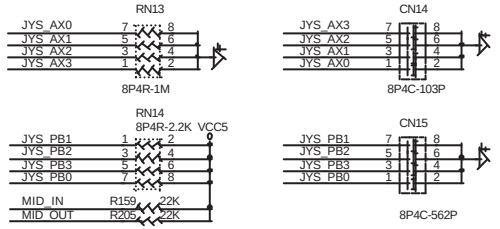


FOR MSI INTERNAL HEADER



GAME/MIDI CONNECTOR





Micro-Star	Title: MS-6399	Rev: 1.0
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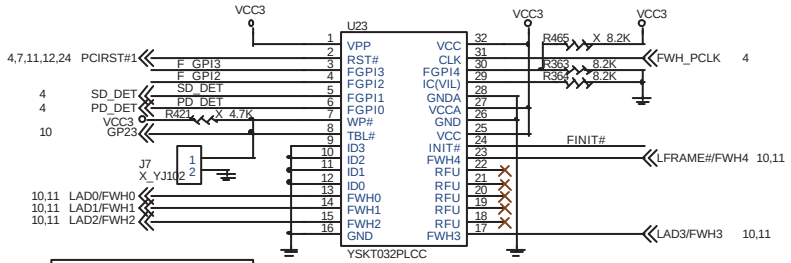
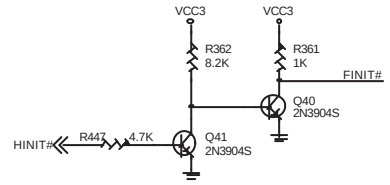
Firware Hub (FWH)

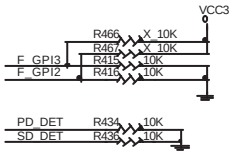


J7 BIOS Update	
SHORT	Locked
OPEN	Unlocked *

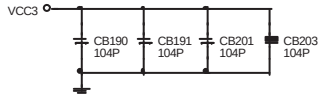
FWH INIT Signal Voltage Translation Block



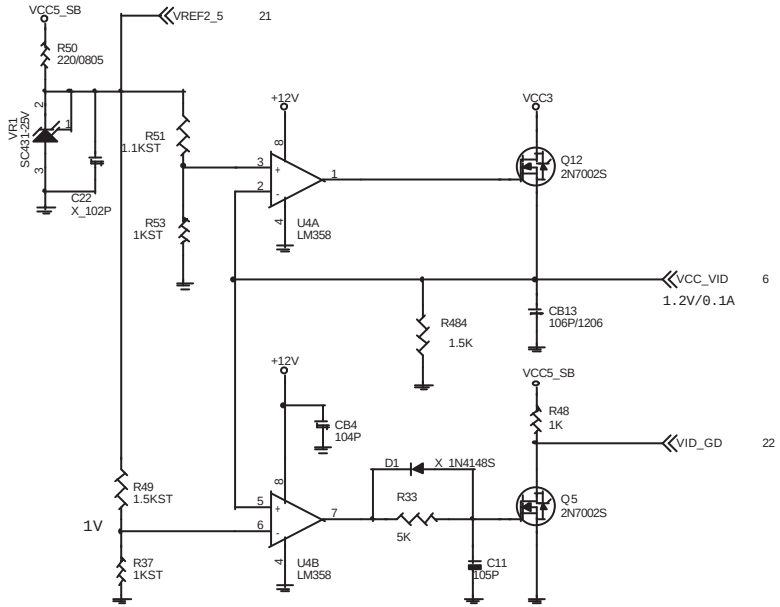
FWH RESISTORS



FWH DECOUPLING CAPACITORS



VCC_VID / VID_GOOD



Micro-Star	Title: MS-6399	Rev: 1.0
Document Number: FWH & VID		
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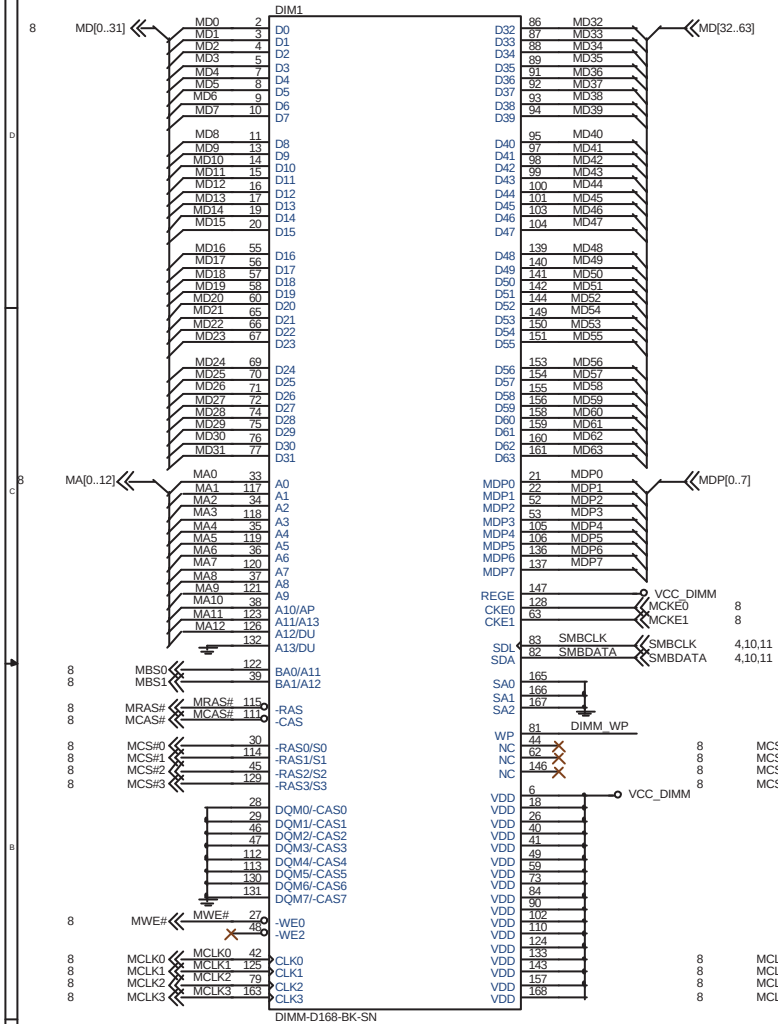
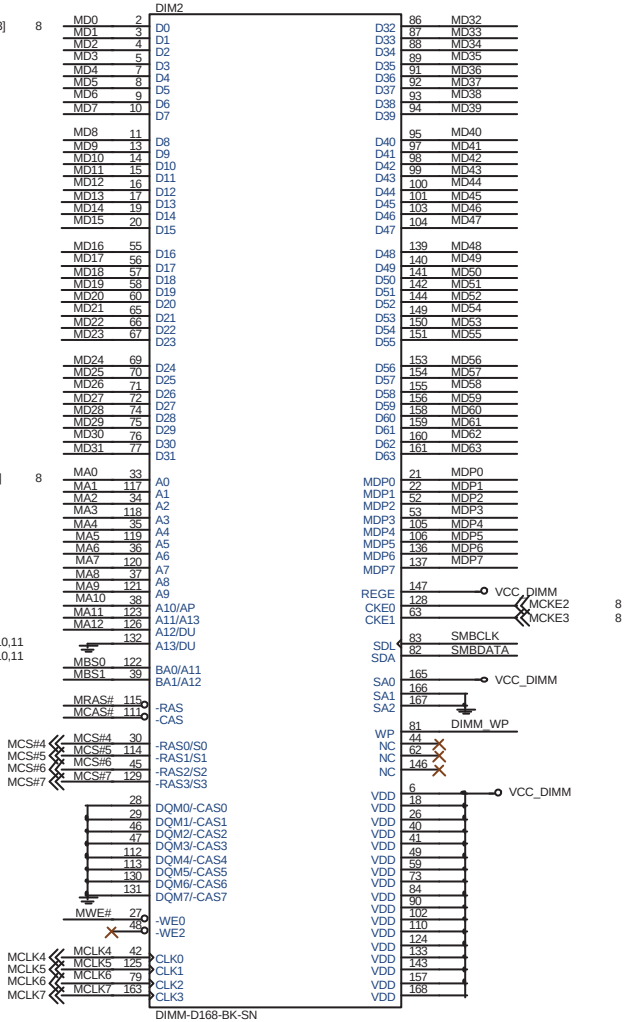
DIMM1



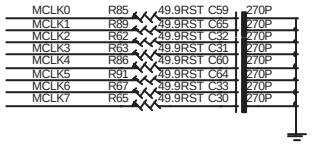
ADDR.=1010000B

DIMM2

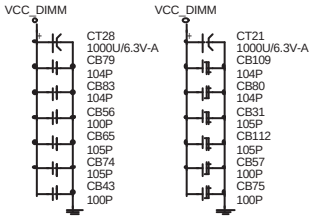


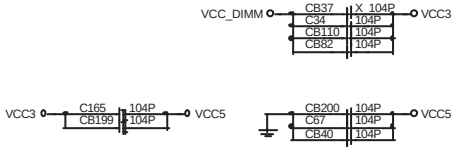
ADDR.=1010001B

DIMM CLOCK



DECOUPLING CAPACITORS





DIMM SPD WE BLOCK

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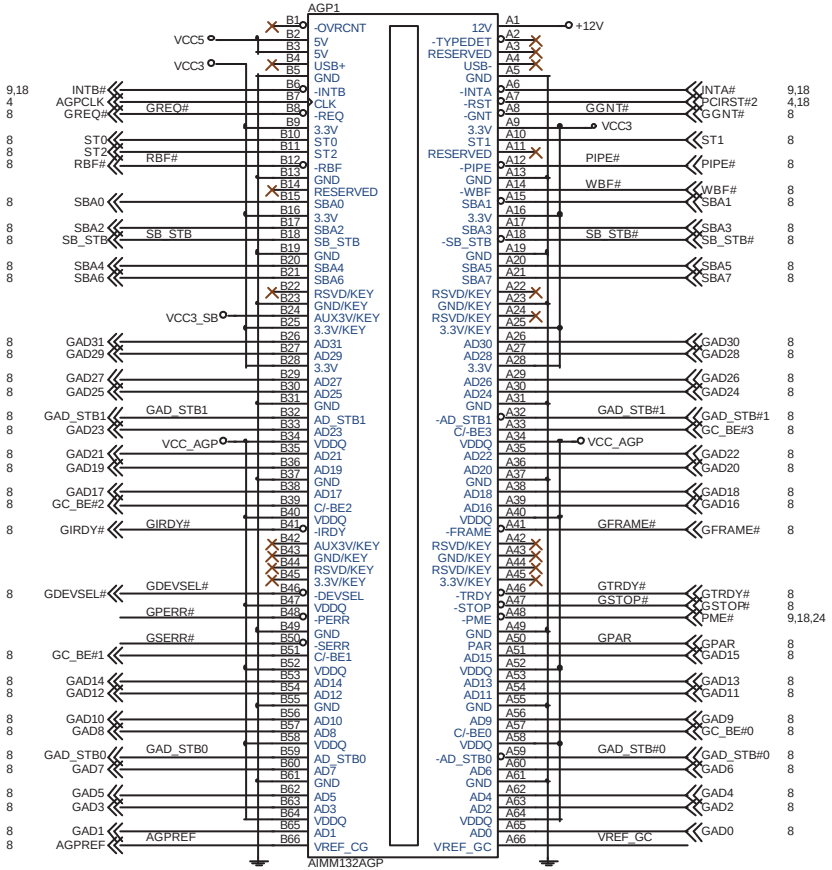
AGP UNIVERSAL 2X/4X SLOT(AGP VER:2.0 COMPLY)

VCC5 = 60mils trace / 15 mils space



VREF_GC:form the chipset to the graphics controller

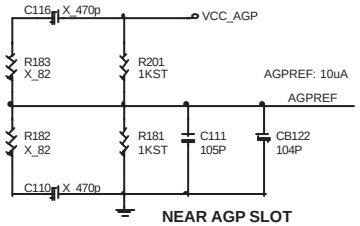
VREF_GC:form the graphics controller to the chipset

AGP Slot Imax

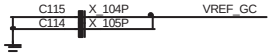
VCC_AGP 8.0A
VCC3 6.0A
VCC12 1.0A
VCC5 2.0A

INTA#
INTB#

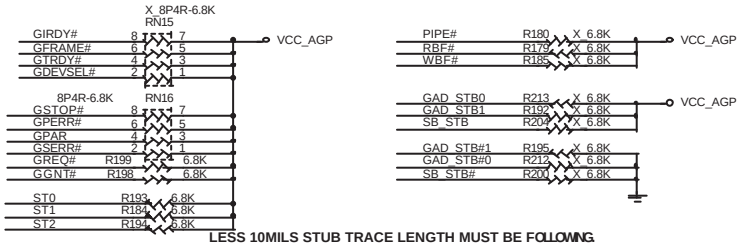
AGP SIGNAL REFERENCE CIRCUIT



NEAR AGP SLOT



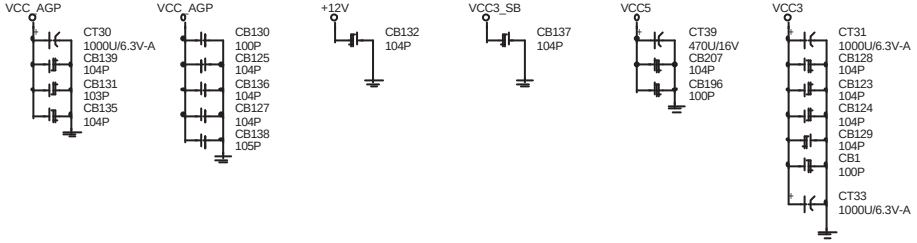
AGP TERMINATION RESISTORS



LESS 10MILS STUB TRACE LENGTH MUST BE FOLLOWING.

Place these resistors between PCI and AGP slot

AGP SLOT DECOUPLING CAPACITORS



Micro-Star	Title: MS-6399		Rev: 1.0
Document Number: AGP Slot			
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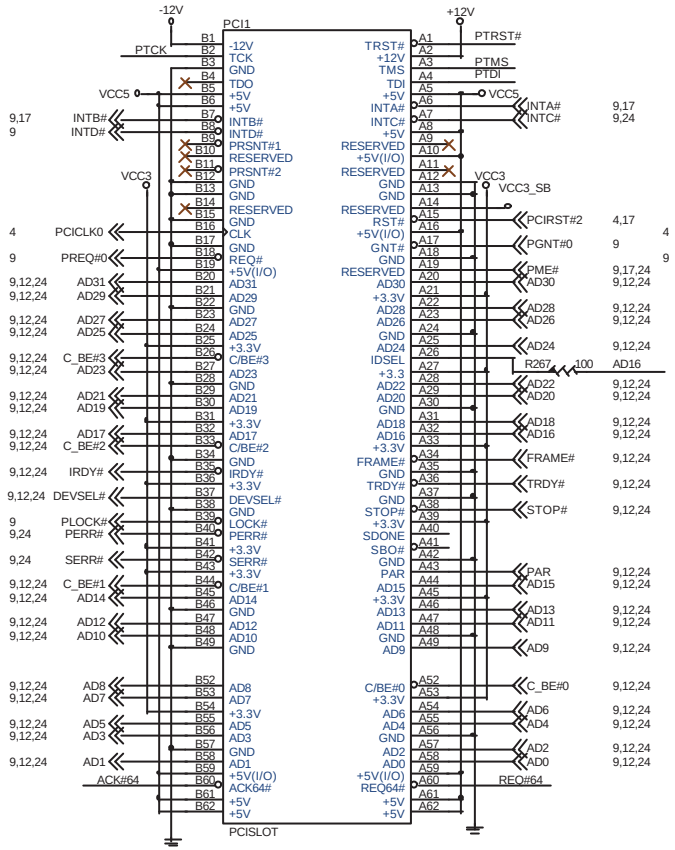
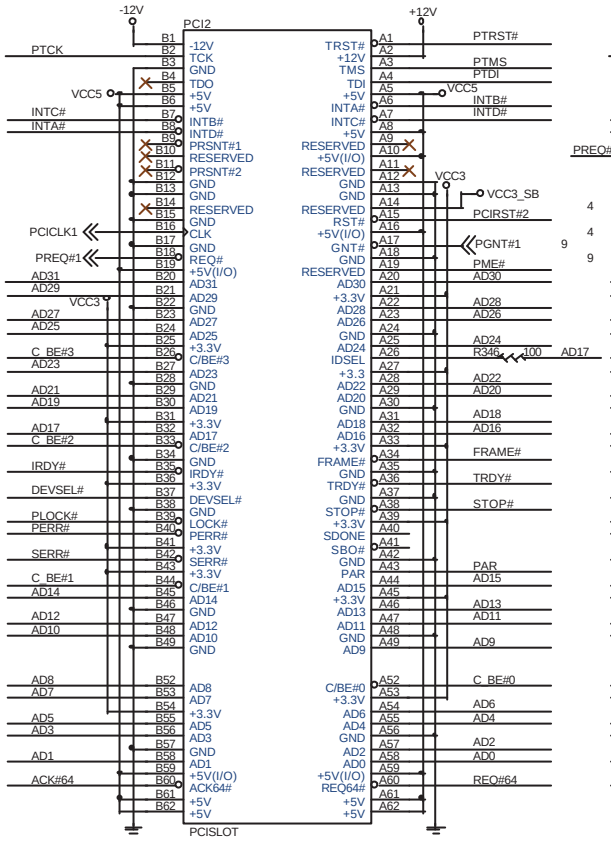
PCI SLOT 1 (PCI VER: 2.2 COMPLY)



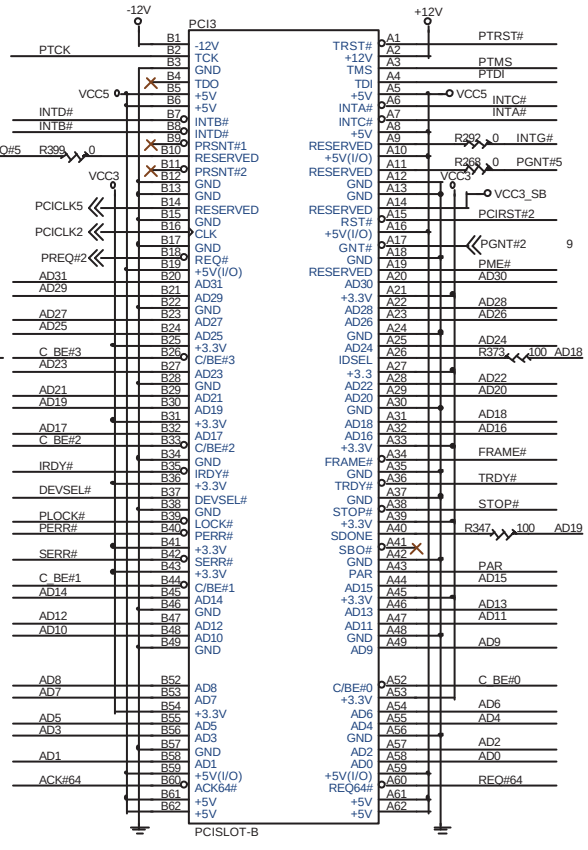
IDSEL = AD16
MASTER = PREQ0
INTA#

PCI SLOT 2 (PCI VER: 2.2 COMPLY)



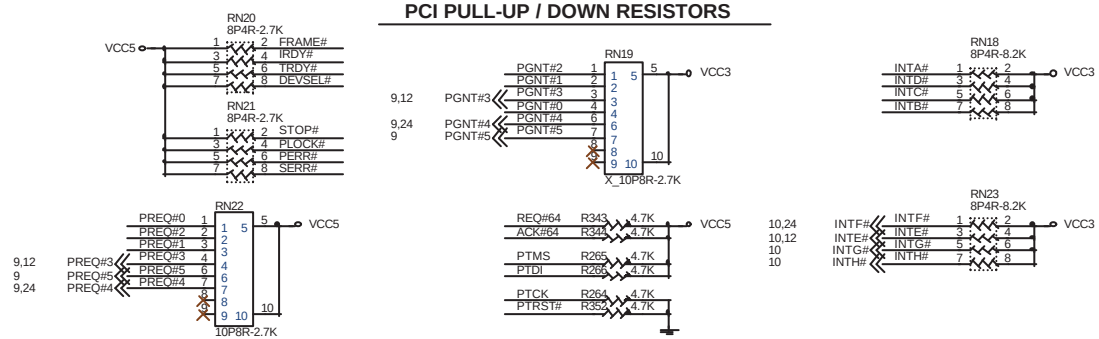
IDSEL = AD17
MASTER = PREQ1
INTB#

PCI SLOT 3 (PCI VER: 2.2 COMPLY)

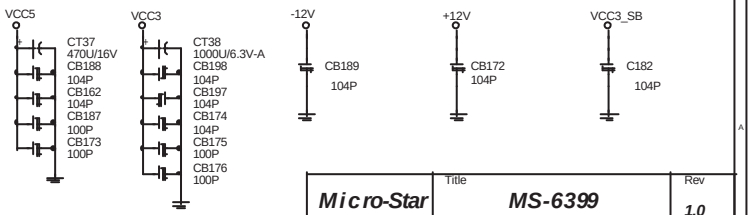


IDSEL = AD18
MASTER = PREQ2
INTC#

PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS



Micro-Star	Title: MS-6399	Rev: 1.0
Document Number: PCI Slot 1 & 2 & 3		
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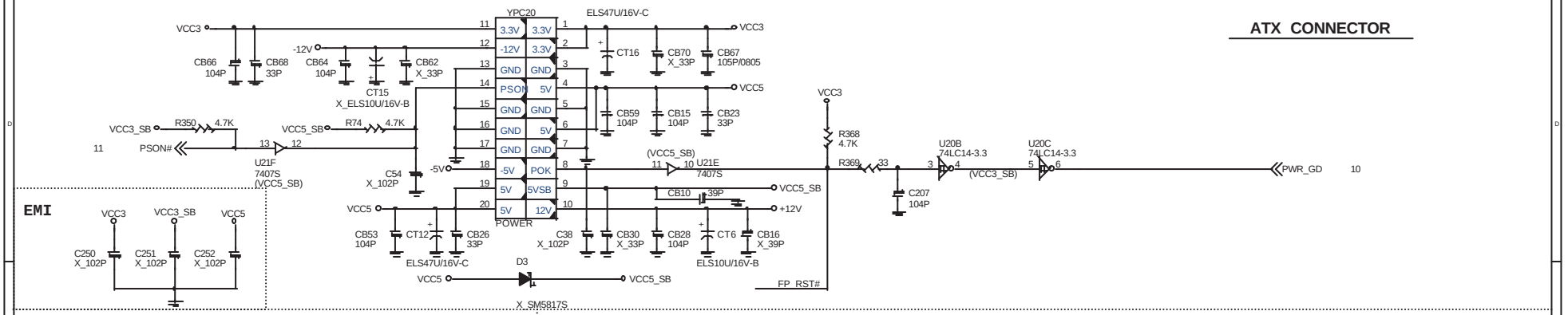

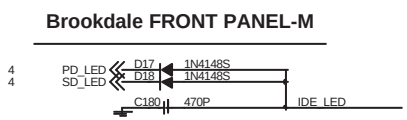

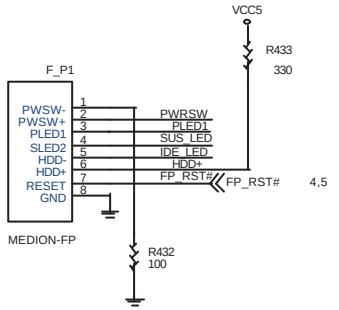

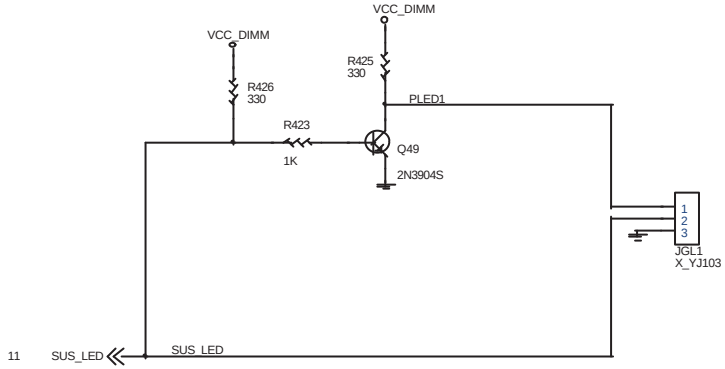

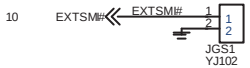

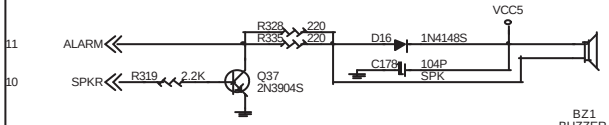

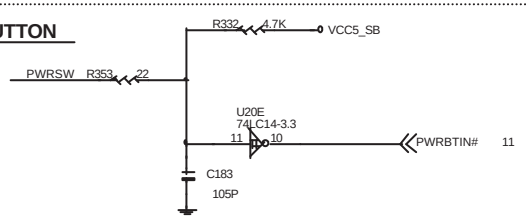

Micro-Star	Title: MS-6399	Rev: 1.0
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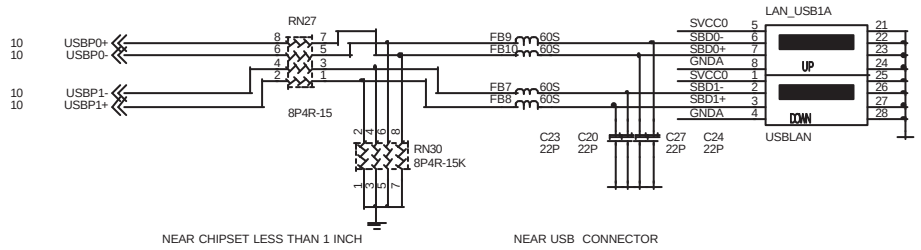
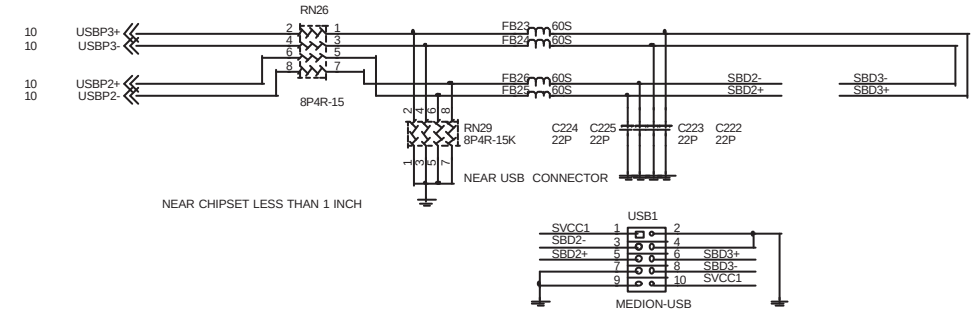
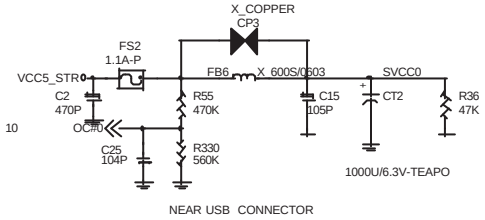
BACK PANEL USB CONNECTOR FOR USB PORT 0,1



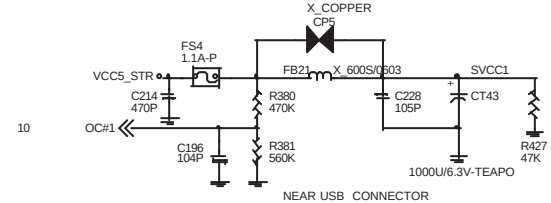
FRONT PANEL USB CONNECTOR FOR USB PORT 2,3



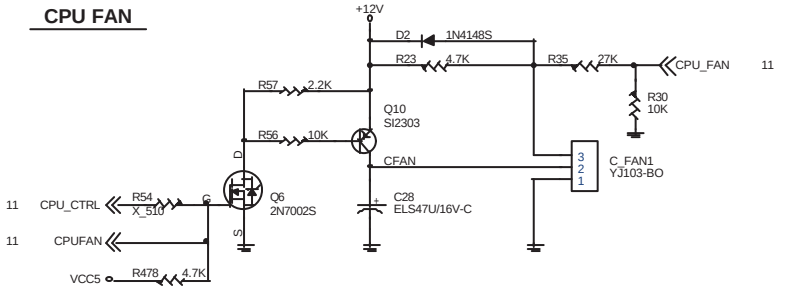
POWER CIRCUIT FOR USB PORT 0,1



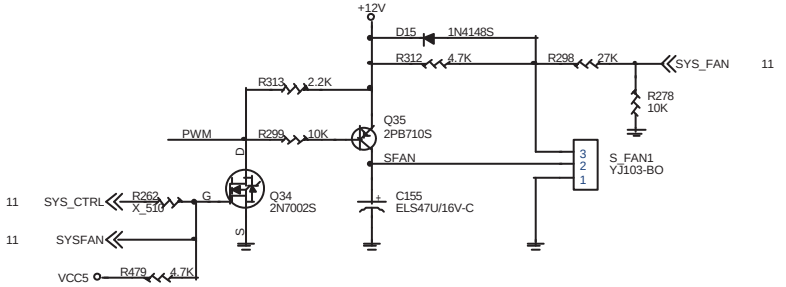
POWER CIRCUIT FOR USB PORT 2, 3



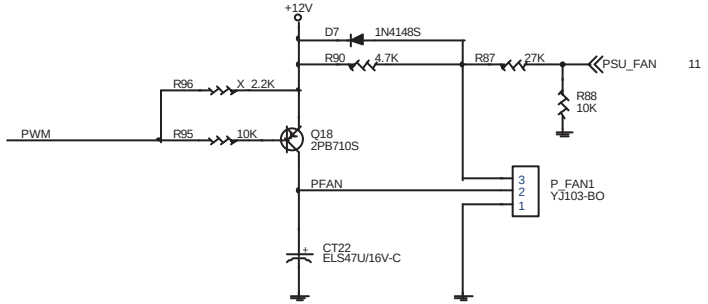
CPU FAN



SYSTEM FAN



ATX PSU FAN ON/OFF CONTROL



Micro-Star	Title: MS-6399	Rev: 1.0
Document Number: USB & FAN Connectors		
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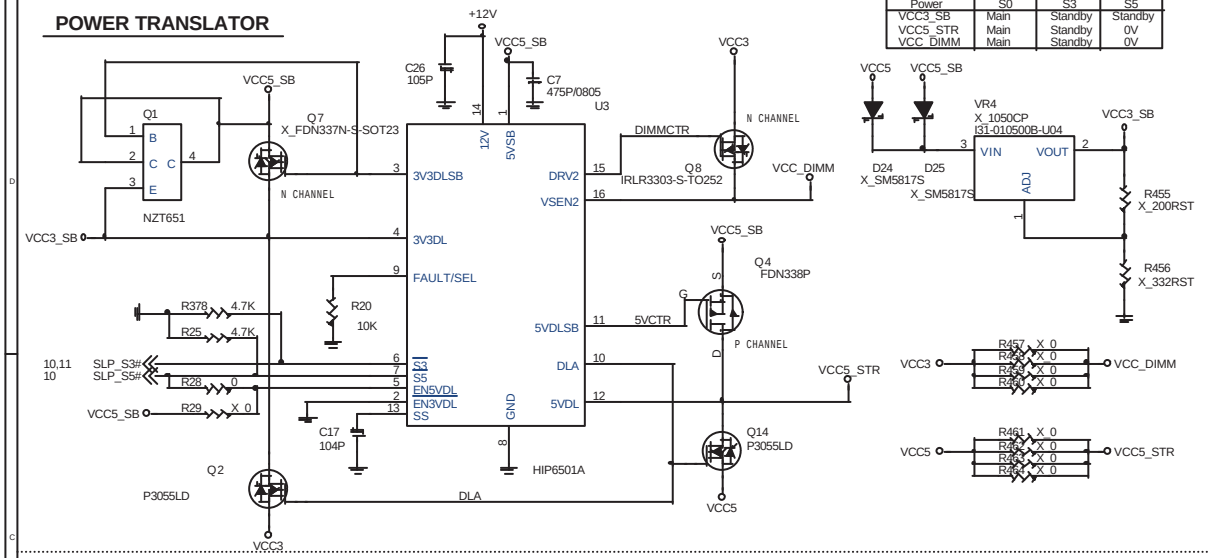
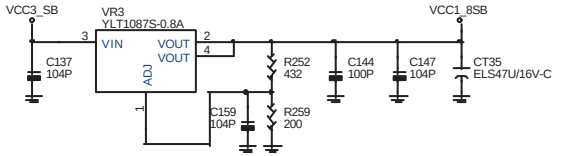
POWER TRANSLATOR



Power	S0	S3	S5
VCC3_SB	Main	Standby	Standby
VCC5_STR	Main	Standby	0V
VCC_DIMM	Main	Standby	0V

1.8V STANDBY POWER TRANSLATOR

(40mils trace / 20 mils space)



POWER CONSUMPTION

	VCCP	VCC_AGP	VCC1_8	VCC3_DIMM	VCC3	VCC5	VCC5_SB	+12V	-12V
CPU	69.0A	0	0	0	0	0	0	NOTE4	0
PMCH	2.4A	NOTE1	0.2A	2.0A	0	0	0	0	0
ICH2	0	0	NOTE3	0	NOTE3	0	NOTE3	0	0
CY28324	0	0	0	0	0	0	0	0	0
AD1885	0	0	0	0	0		0	0	0
FWH -SST	0	0	0	0			0		
W83627HF	0	0	0	0	0		0	0	0
HIP6301		0	0	0	0		0	0	0
HIP6602A		0	0	0			0	0	0
HIP6601A	0	0	0	0	0	0	0	0	0
SC1547	0	0	0	0	0	0			0
DIMM	0	0	0	NOTE2	0		NOTE2	0	0
AGP	0	8.0A	0	0	6.0A	2.0A	?	1.0A	0
PCI	0	0	0	0		0	0	0	0
USB	0		0	0		0			0
USB HUB	0	0	0	0	0	0	0	0	0
FAN	0	0	0	0	0	0	0	0	0
TTL	0	0	0	0	0	0	0	0	0
AMPLIFIER	0	0	0	0			0	0	0
OTHER	0	0	0	0	0		0		

NOTE1 --- MCH
VCC_AGP = VCC1_5 (1.5A) + VCC_AGP (0.37A)

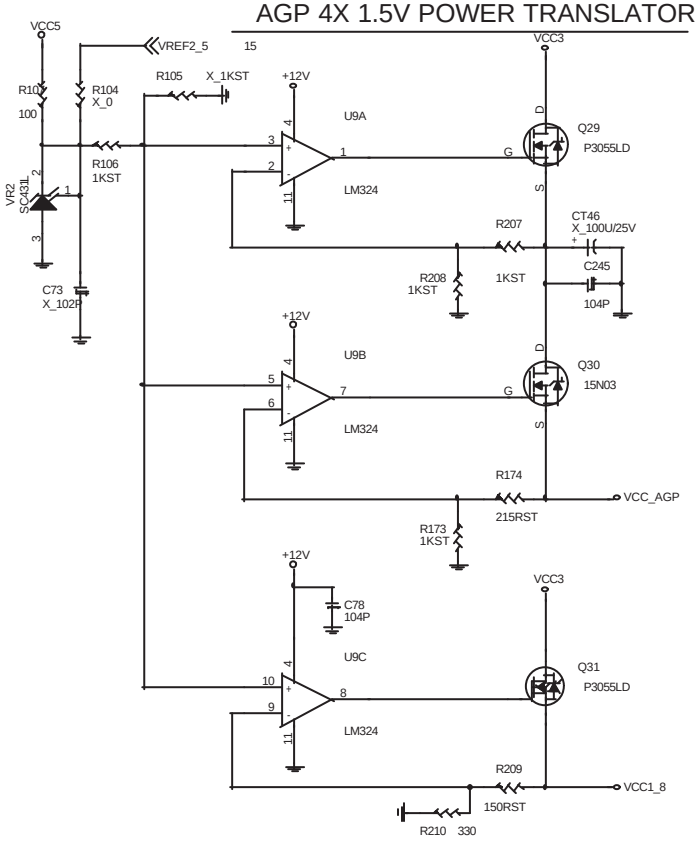
NOTE2 --- DIMM
S0 STATE --- 2.0A * 3 = 6.0A ---> VCC3
S1/S3 STATE --- 200mA * 3 = 600mA ---> VCC3_SB
VCC3_SB --> 600mA*3.3V/5V=396mA --> VCC5_SB

NOTE3 --- ICH2

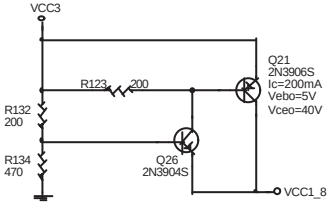
Power	S0	S1	S3/S4/S5
1.8V	300mA	100mA	N/A
1.8V_LAN	36mA	28mA	N/A
VCC1_8SB	45mA	30mA	7mA
VCC3	410mA	5mA	N/A
VCC3+562ET	230mA	210mA	N/A
VCC3_SB	25mA	0.6mA	N/A

VCC3_SB =
VCC1_8SB =
VCC5_SB = VCC3_SB + VCC1_8SB

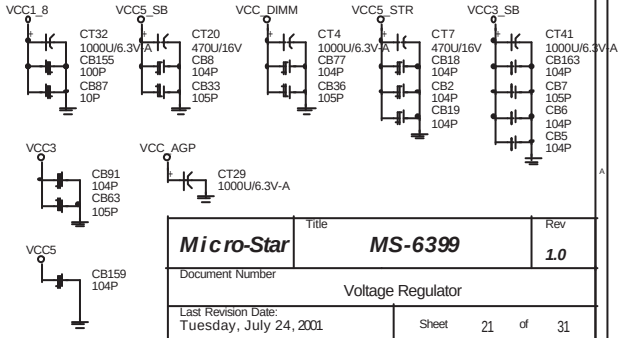
AGP 4X 1.5V POWER TRANSLATOR



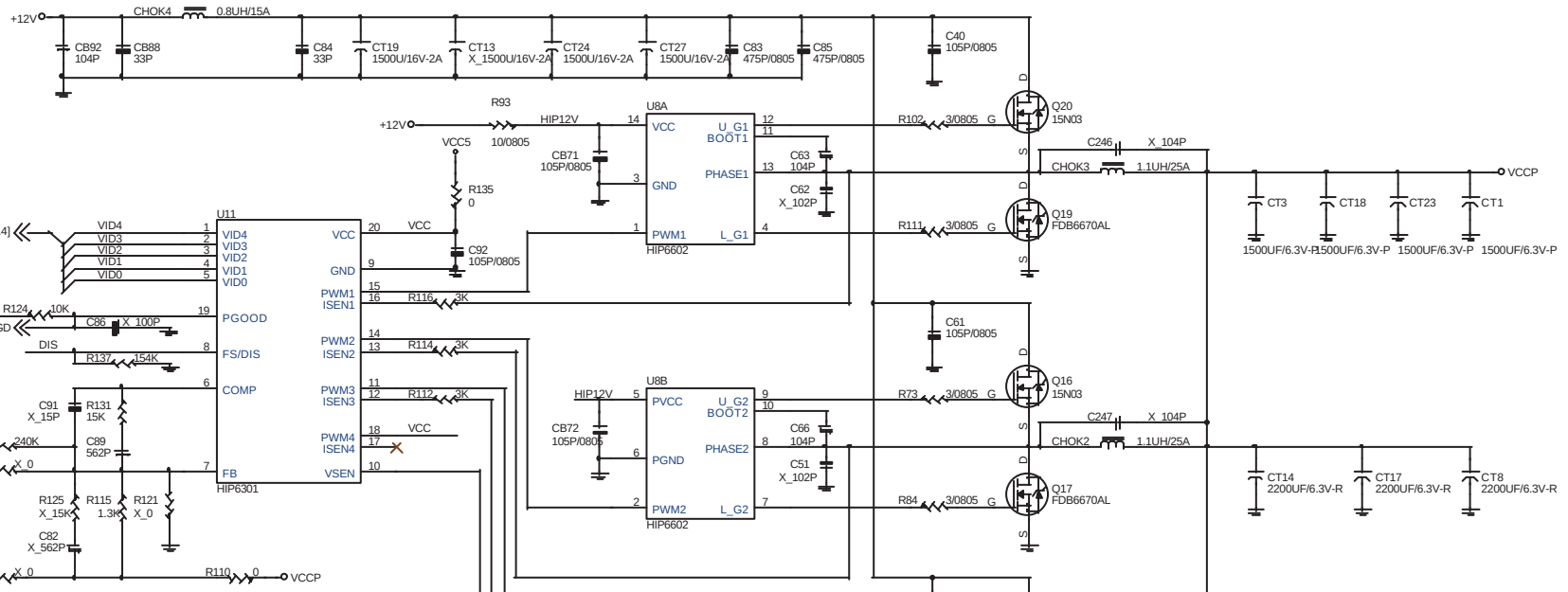
1.8V/3.3V SEQUENCE CIRCUIT



REGULATORS OUTPUT DECOUPLING CAPACITORS



Micro-Star	Title: MS-6399	Rev: 1.0
	Document Number: Voltage Regulator	
	Last Revision Date: Tuesday, July 24, 2001	Sheet 21 of 31



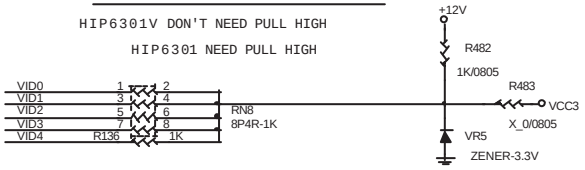
VID4	VID3	VID2	VID1	VID0	VDC(V)
1	1	1	1	0	1.100
1	1	1	0	1	1.125
1	1	1	0	0	1.150
1	1	0	1	1	1.175
1	1	0	1	0	1.200
1	1	0	0	1	1.225
1	1	0	0	0	1.250
1	0	1	1	1	1.275
1	0	1	1	0	1.300
1	0	1	0	1	1.325
1	0	1	0	0	1.350
1	0	0	1	1	1.375
1	0	0	1	0	1.400
1	0	0	0	1	1.425
1	0	0	0	0	1.450
0	1	1	1	1	1.475

VID4	VID3	VID2	VID1	VID0	VDC(V)
0	1	1	1	0	1.500
0	1	1	0	1	1.525
0	1	1	0	0	1.550
0	1	0	1	1	1.575
0	1	0	1	0	1.600
0	1	0	0	1	1.625
0	1	0	0	0	1.650
0	0	1	1	1	1.675
0	0	1	1	0	1.700
0	0	1	0	1	1.725
0	0	1	0	0	1.750
0	0	0	1	1	1.775
0	0	0	1	0	1.800
0	0	0	0	1	1.825
0	0	0	0	0	1.850
1	1	1	1	1	OFF

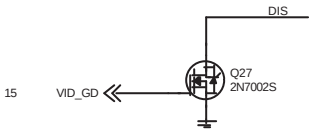
VID PULL-UP RESISTORS

HIP6301V DON'T NEED PULL HIGH

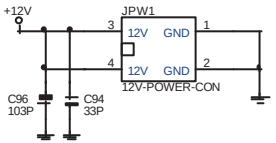
HIP6301 NEED PULL HIGH



PWM GOOD



ATX12V POWER CONNECTOR



Micro-Star	Title: MS-6399	Rev: 1.0
Document Number: VRM 9.2		
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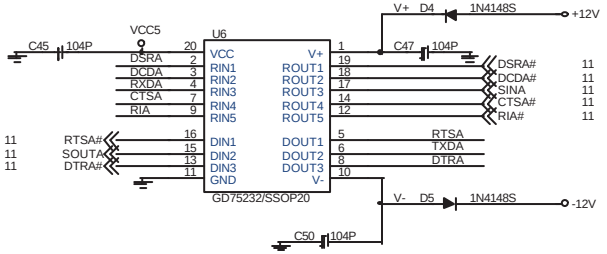
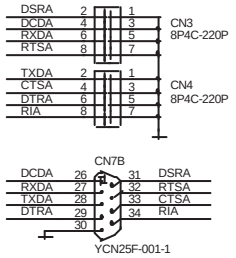
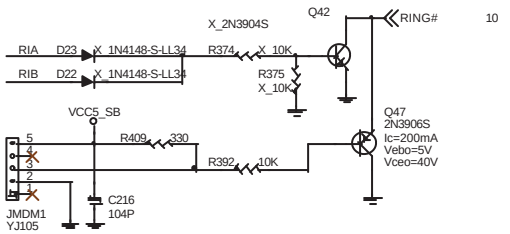
SERIAL PORT 1

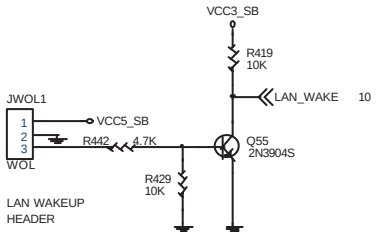




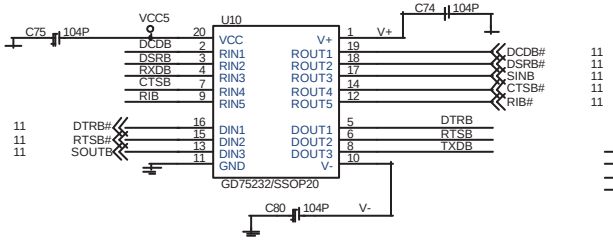
MODEM RING BLOCK

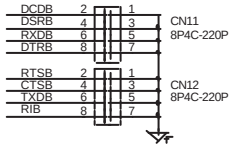


LAN WAKEUP BLOCK

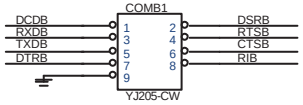


SERIAL PORT 2

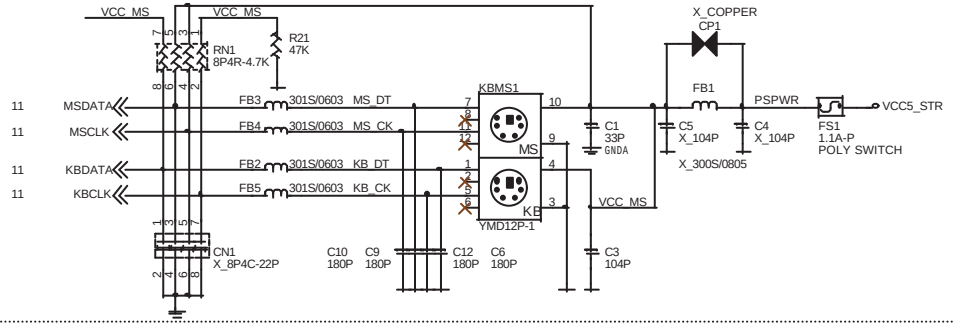




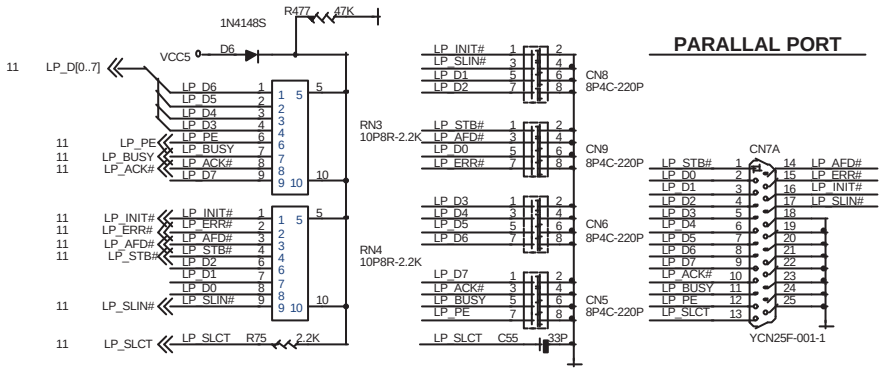
COM2 HEADER



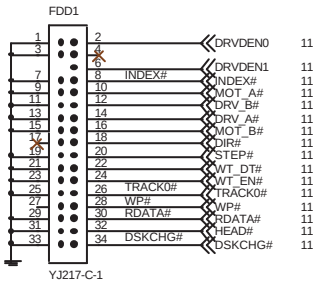
PS2 KEYBOARD & MOUSE CONNECTOR



PARALLAL PORT



FLOPPY CONNECTOR



Micro-Star	Title: MS-6399		Rev: 1.0
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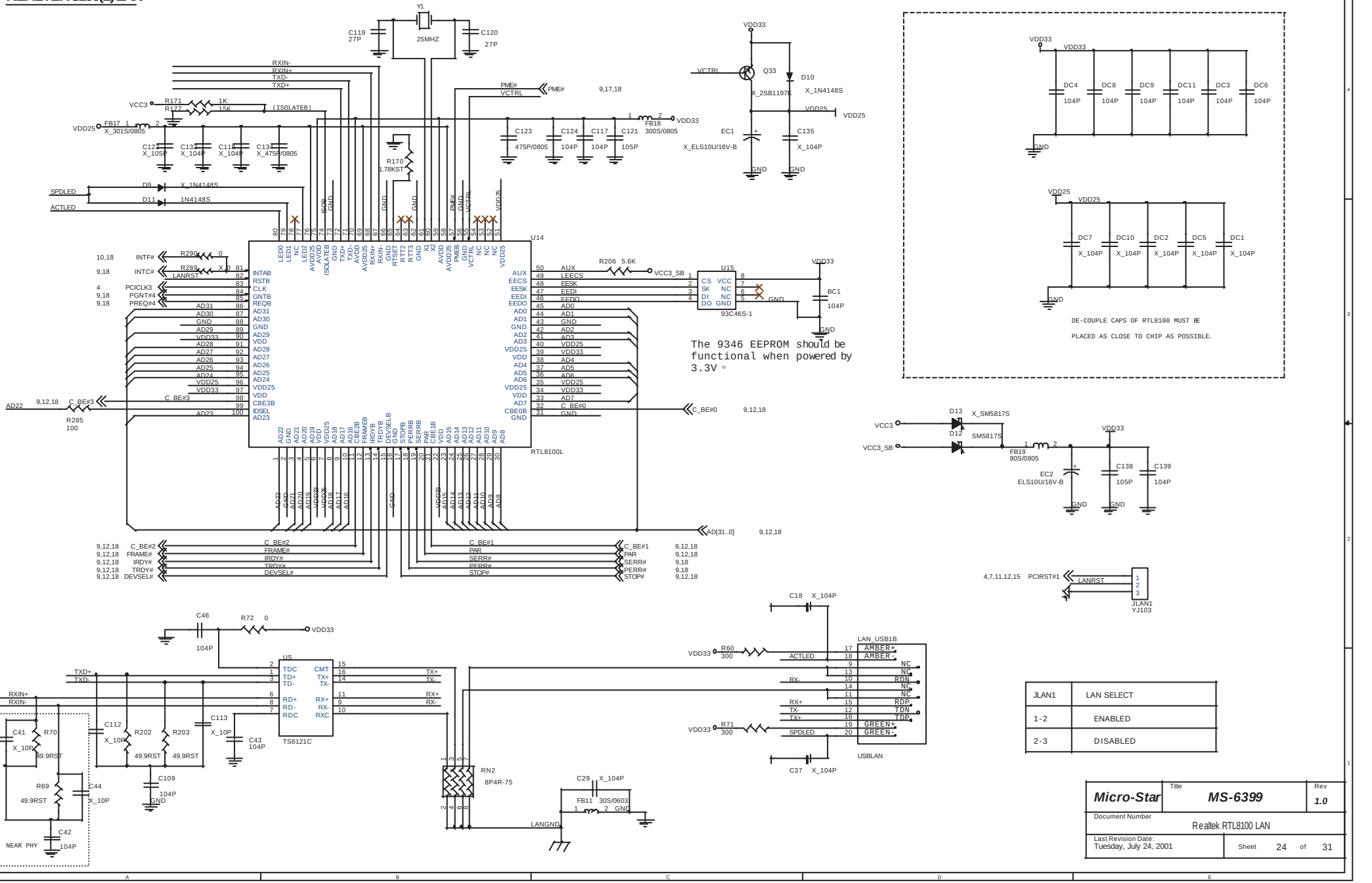
REALTEK 8100(L) LAN



JLAN1	LAN SELECT
1-2	ENABLED
2-3	DISABLED

Micro-Star	Title: MS-6399	Rev: 1.0
Document Number: Realtek RTL8100 LAN		
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Jumper Setting & Connector Setting

Jumper	Description	
J1	INTERUDER HEADER	
J2	CHASISS INTRUSION HEADER	
J3	AUDIO REAR PHONE JACK (LINE_IN, LINE_OUT, MIC_IN)	
J4	AUDIO AUX HEADER	
J5	AUDIO FRONT PANEL HEADPHONE JACK HEADER	
J6	AUDIO INTERNAL SPEAKER HEADER (ATAPI)	
J7	BIOS function	
1-2	Normal	(Default)
2-3	Configuration Mode	
REMOVED	Recovery	
JBAT1	CLEAR CMOS	
1-2	NORMAL	(Default)
2-3	CLEAR CMOS	
IR1	IR HEADER	
CD_IN1	CDROM HEADER (ATAPI)	
MDM_IN1	TELEPHONY HEADER (ATAPI)	
JP1	CNR RISER CODEC SELECT HEADER	
1-2	AUTO MODE	(Default)
2-3	PRIMARY AUDIO CODEC ONBOARD	

Connector	Description
U3	INTEL mPGA478-B CPU
IDE1	Primary
IDE2	Secondary
DIM1	SDRAM DIMM1
DIM2	SDRAM DIMM2
AGP1	AGP Slot
PCI1	PCI Slot1
PCI2	PCI Slot2
PCI3	PCI Slot3
COM1	Serial Port
COM2	Serial Port
LPT	Parallel Port
FDD1	Floopy
JMDM1	MODEM RING HEADER
JWOL1	LAN WAKEUP HEADER
KBMS1	PS/2 Keyboard and PS/2 mouse
C_FAN1	CPU FAN HEADER
S_FAN	System FAN HEADER
USB1	USB REAR CONNECTOR
USB2	USB INTERNAL HEADER
POWER	ATX Power
JSMB1	SMBUS HEADER
F_P1	Front Panel
Pin1	Power of Hard LED
Pin2	Power LED
Pin3	Hard LED
Pin4	Suspend LED
Pin5,8,12,13	GND
Pin6	Power Button
Pin7	Reset Button
Pin9	VCC
P_FAN1	ATX FAN HEADER
JPW1	ATX12V Power

Micro-Star	Title: MS-6399	Rev: 0A
Document Number: JUMPER SETTING		
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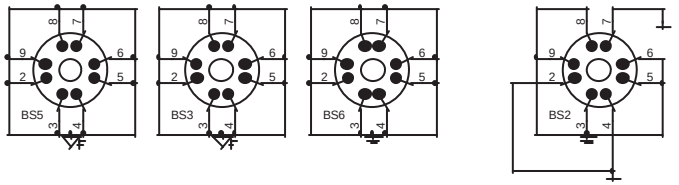
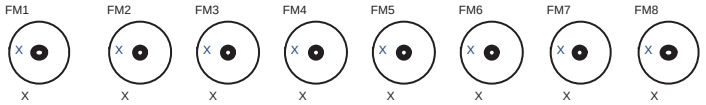
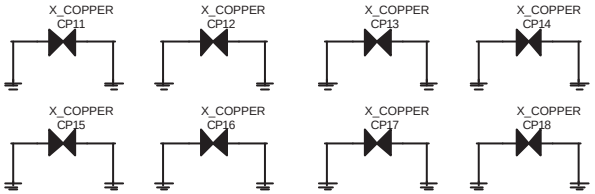
PCB OTHER COMPONENT







SIMULATION TRACE

Micro-Star	Title: MS-6399	Rev: 0A
Document Number: MANUAL		
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Pentium 4 Processor /Northwood mPGA 478

Source Synchronous Signal Group and the Associated Strobes

Signals	Associated Strobe
REQ[4:0],A[16:3]#	ADSTB0#
A[31:17]#	ADSTB1#
D[15:0]#,DBI0#	DSTBP0#,DSTBN0#
D[31:16]#,DBI1#	DSTBP1#,DSTBN1#
D[47:32]#,DBI2#	DSTBP2#,DSTBN2#
D[63:48]#,DBI3#	DSTBP3#,DSTBN3#

Signals	Length	Inaccuracy
Data	**2.0" to 10.0"**	+/- 100 mil
Address	**2.0" to 10.0"**	+/- 200 mil
Strobe	**2.0" to 10.0"**	+/- 25 mil
Clock	**2.0" to 10.0"**	Don't need

***** Delta=(CPU_pkglen.net-CPUpkglen.strobe)+(CS_pkglen.net-CS_pkglen.strobe)
Trace : 7 mil width 13mil space

Miscellaneous Signals

HL_STB/HL_STB#

Taces 5mils

20mils — HL[0:10]
HL_STB
15mils — HL_STB#
20mils — HL[0:10]

* Max Length : 8"
* STB and STB# Length must be equal

HL[10..0]

20mils — Others
15mils — HL[0:10]
HL[0:10]
20mils — Others

* Max Length : 8"
* Length must be matched within +/- 0." of the Strobe Signals

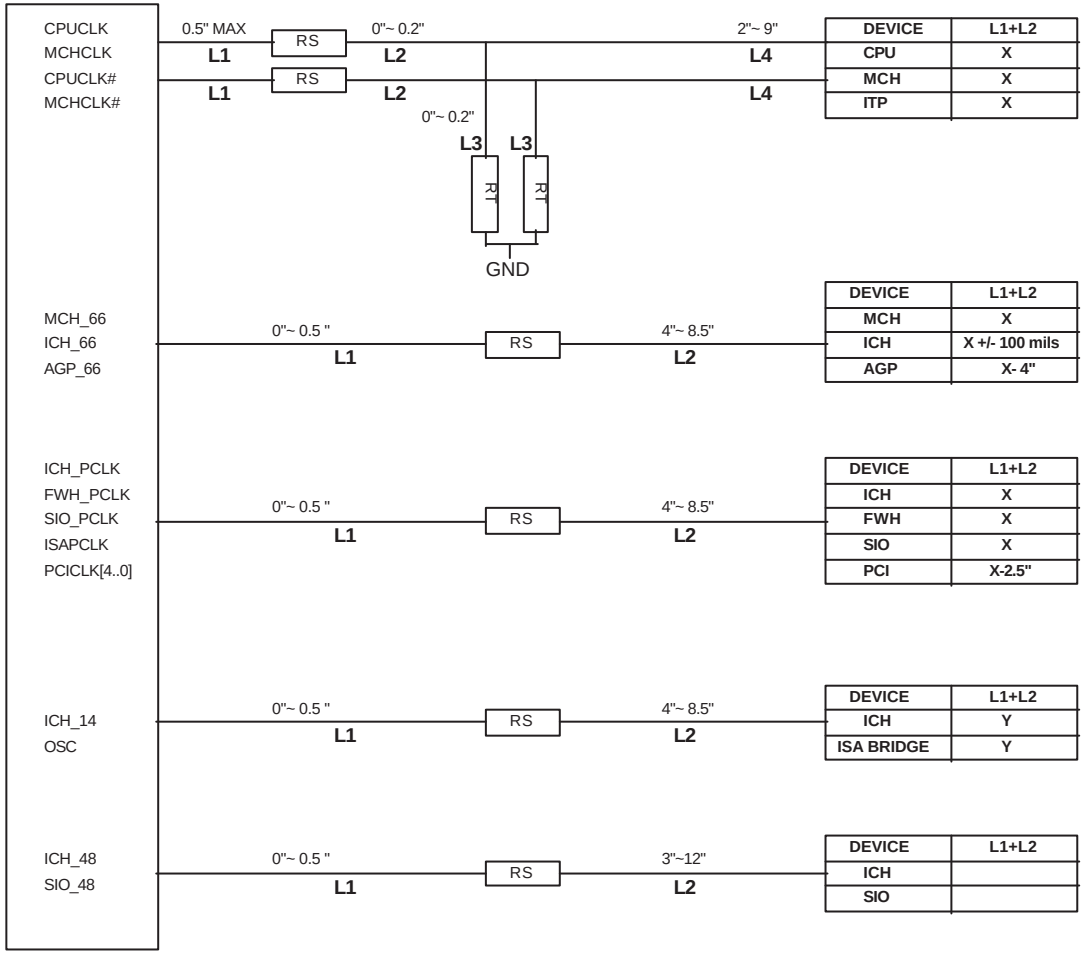
USB

*** USB Trace width : 9 mils**
*** USB Trace Spacing : 25 mils**
*** Differential USB Signlas Trace Spacing : 18 mils**
*** USB Power Trace must be 40mils width**

AGP

1X Timing group	2X/4X Timing group
AGPCLK PIPE# RBF# WBF# ST[2..0] GFRAME# GIRDY# GTRDY# GSTOP# GDEVSEL# GREQ# GGNT# GPAR	SET#1 GAD[15..0] GC_BE#[1..0] GAD_STB0 GAD_STB0# SET#2 GAD[31..16] GC_BE#[3..2] GAD_STB1 GAD_STB1# SET#3 SBA[7..0] SB_STB SB_STB#

SIGNALS	Maximum Length	Width	Space	Dismatch Length	Relative to
1X Timing group	7.5"	5 mil	5 mil	X	X
2X/4X Timing group SET#1	7.25"	5 mil	20 mil	+/- 0.125"	GAD_STB0 GAD_STB0#
2X/4X Timing group SET#2	7.25"	5 mil	20 mil	+/- 0.125"	GAD_STB1 GAD_STB1#
2X/4X Timing group SET#3	7.25"	5 mil	20 mil	+/- 0.125"	SB_STB SB_STB#
2X/4X Timing group SET#1	6"	5 mil	15 mil	+/- 0.25"	GAD_STB0 GAD_STB0#
2X/4X Timing group SET#2	6"	5 mil	15 mil	+/- 0.25"	GAD_STB1 GAD_STB1#
2X/4X Timing group SET#3	6"	5 mil	15 mil	+/- 0.25"	SB_STB SB_STB#



DEVICE	L1+L2
CPU	X
MCH	X
ITP	X

* Line Width : 7.0 mil
* Differential pair spacing : 7.0mil
* Spacing to other traces : 28 mil
* BCLK0/BCLK1 LENGTH MATCH +/- 10 mil

DEVICE	L1+L2
MCH	X
ICH	X +/- 100 mils
AGP	X- 4"

* Line Width : 5.0 mil
* Spacing to other traces : 20 mil

DEVICE	L1+L2
ICH	X
FWH	X
SIO	X
PCI	X-2.5"

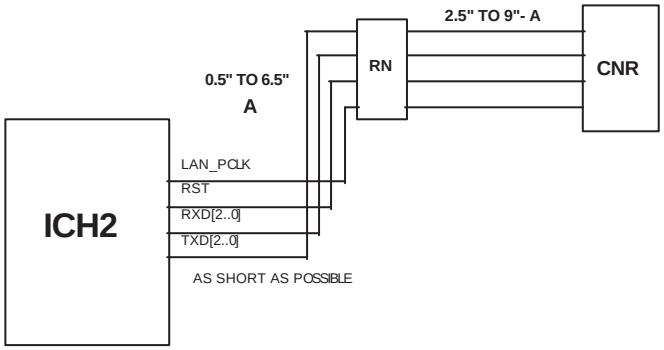
* Line Width : 5.0 mil
* Spacing to other traces : 20 mil
* L1/L2 TRACE SAME AS MCH_66 TRACE LENGTH

DEVICE	L1+L2
ICH	Y
ISA BRIDGE	Y

* Line Width : 5.0 mil
* Spacing to other traces : 10 mil

DEVICE	L1+L2
ICH	
SIO	

* Line Width : 5.0 mil
* Spacing to other traces : 20 mil



* Line Width : 7.0 mil
* Differential signls space : 14mils
* Differential signls length mismatch +/- 7mil

Micro-Star	Title: MS-6399	Rev: 0A
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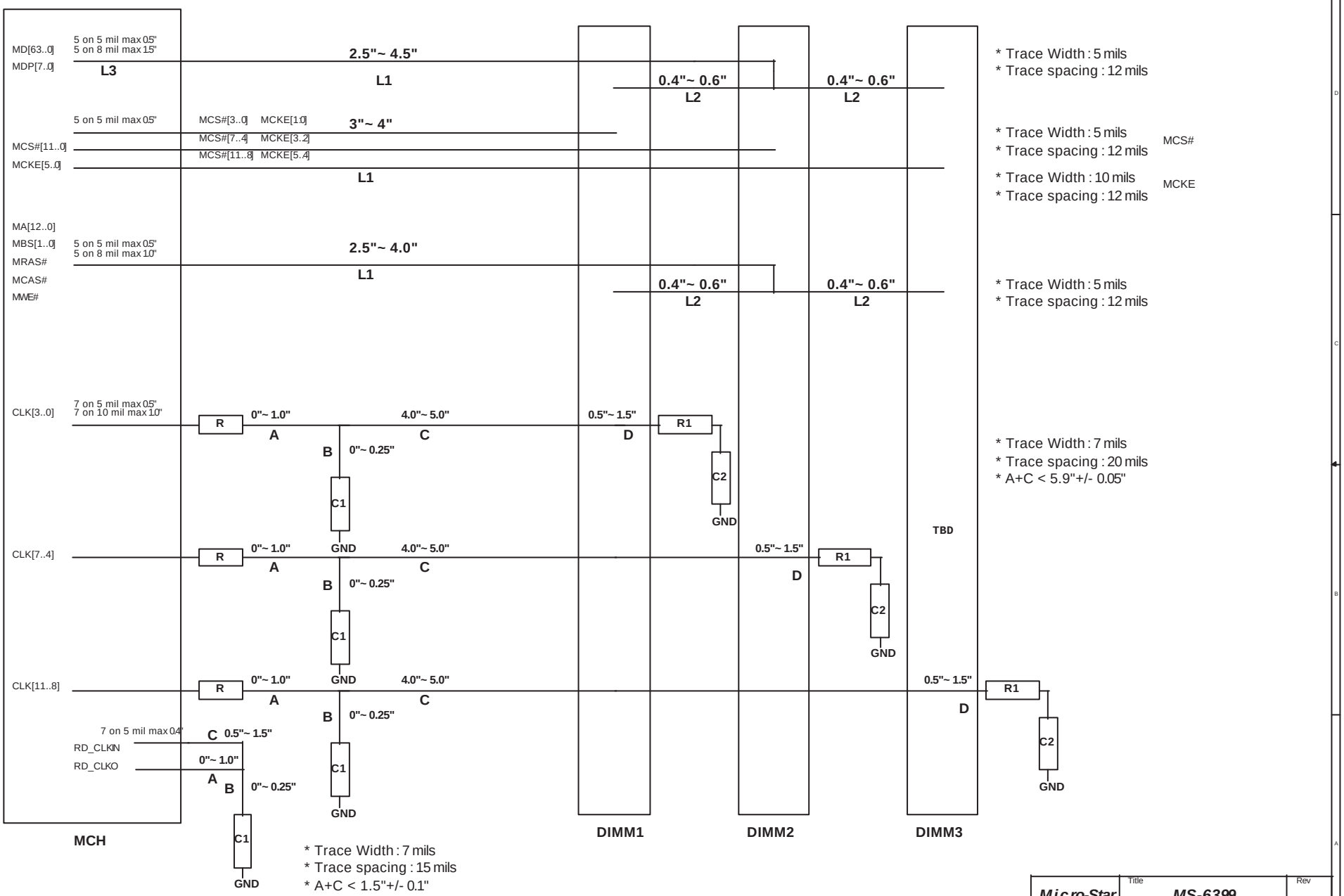
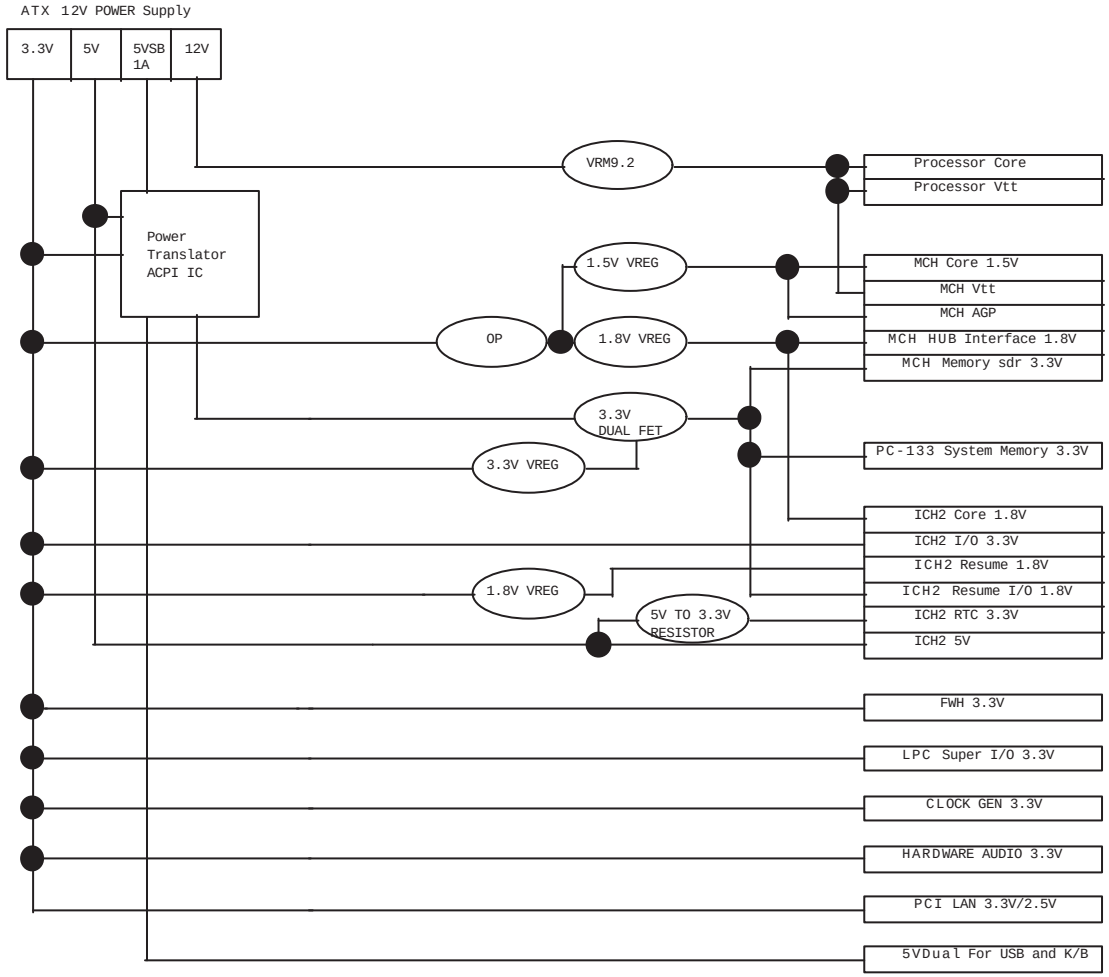


Micro-Star	Title: MS-6399	Rev: 0A
Document Number: PC133 DIMM DG		
Last Revision Date: Monday, May 28, 2001	Sheet 29 of 31	

Power Delivery Map



Micro-Star	Title: MS-6399	Rev: 0A
Document Number: Power Delivery Map		
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JBAT1 Clear CMOS	
1 - 2	Normal *
2 - 3	Clear CMOS

JBAT1(1-2)
YJUMPER-MG

BAT SOCKET

BAT1[A]
YSKTBT

JP2 H/W AUDIO	
1 - 2	DISABLE
2 - 3	ENABLE *

X_JP2(2-3)
YJUMPER-MG

J7 BIOS Update	
SHORT	Locked
OPEN	Unlocked *

J7(1)
X_YJUMPER-MG

BIOS

U23[1]

1			32
2	VPP	VCC	31
3	RST#	CLK	30
4	FGPI3	FGPI4	29
5	FGPI2	IC(VIL)	28
6	FGPI1	GNDA	27
7	FGPI0	VCCA	26
8	WP#	GND	25
9	TBL#	VCC	24
10	ID3	INIT#	23
11	ID2	FWH4	22
12	ID1	RFU	21
13	ID0	RFU	20
14	FWH0	RFU	19
15	FWH1	RFU	18
16	FWH2	RFU	17
	GND	FWH3	

SST49LF002A

FRONT PANNEL BUZZER

F_P114-15
X_YJUMPER-MG

JLAN1	LAN SELECT
1-2	ENABLED
2-3	DISABLED

JLAN1(1-2)
YJUMPER-MG

J11	J12	Connection Scheme
1-2	1-2	Mode1 Center to left Channel/Subwoofer to right channel
* 2-3	2-3	Mode2 Center to right Channel/Subwoofer to left channel

J11(2-3)
YJUMPER-MG

J12(2-3)
YJUMPER-MG

MS6399 PCB

PCB
MS-6399-100

COM1
YCN9M-1

X_U12-A
845-MCH-PIN

X_U12-B
845-MCH-PIN

X_U12-C
845-MCH-PIN

X_U12-D
845-MCH-PIN

X_U12
845-MCH-H

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