MS-6394 100

Single Intel PGA 370 Processor (Cu , Cu-T & Tualatin)
ServerWorks LC-T + CSB5 Chipset
National Semiconductor PC97417 LPC IO Chip

Title: Cover Sheet		Rev: 100
Document Number		
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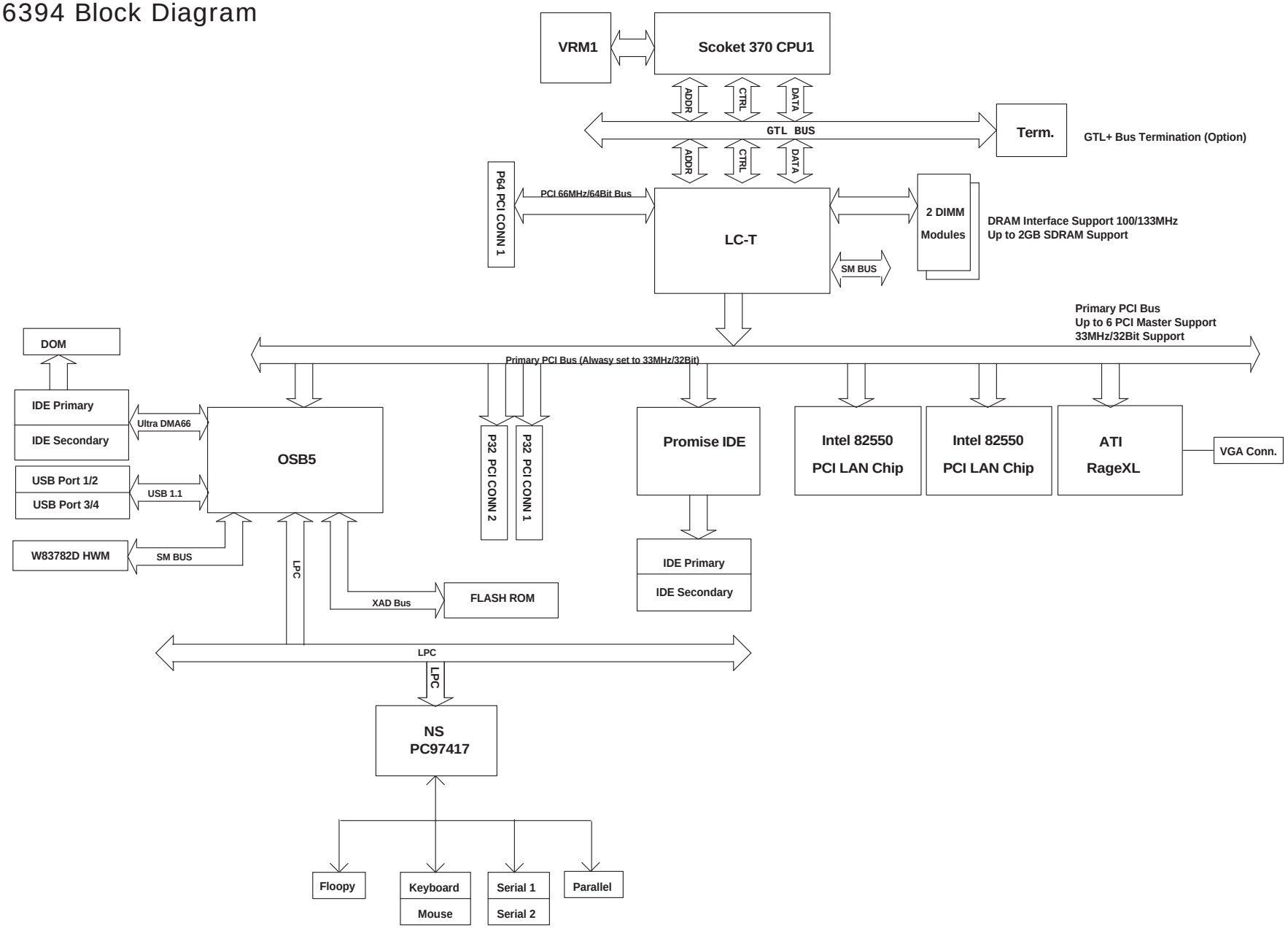
BLOCK DIAGRAM

MS6394 Block Diagram



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Title: Block Diagram		Rev: 100
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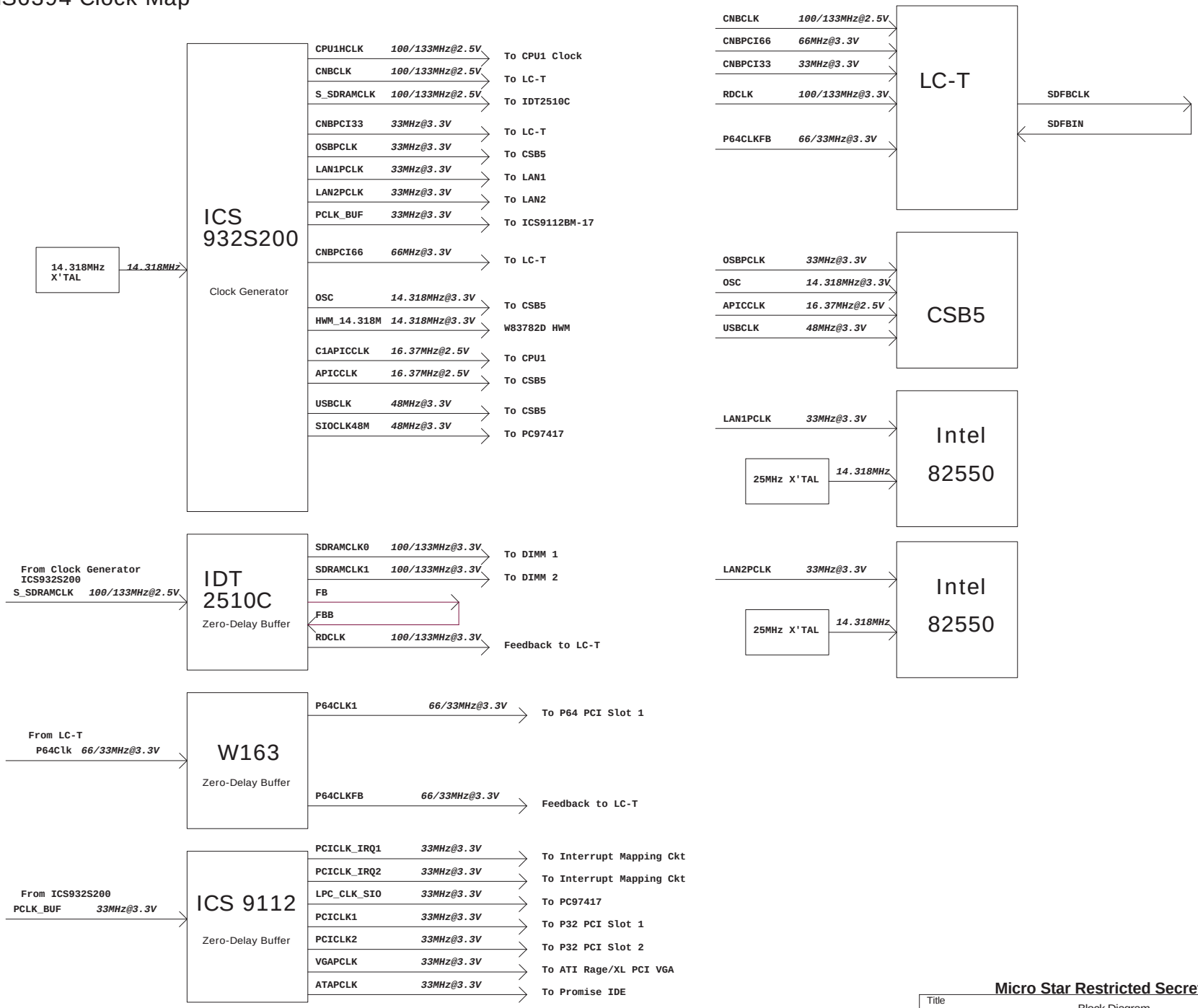
MS6394 Clock Map



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Title: Block Diagram		Rev: 100
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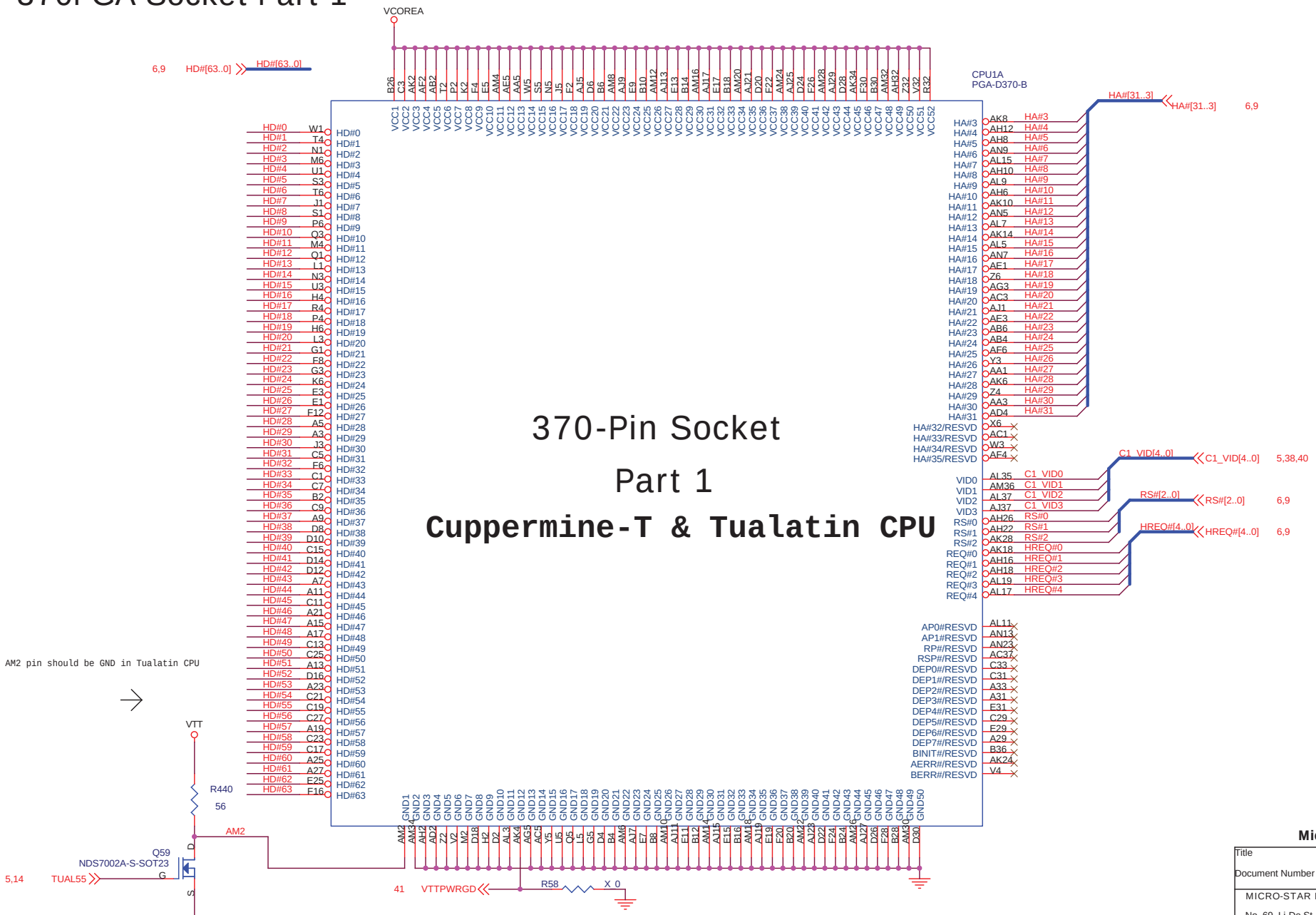
370PGA Socket Part 1



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Title	370-pin Socket : Part 1	Rev 100
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370PGA Socket Part 2

Intel Tualatin 1.33GHz (133MhzFSB) :

Vcore=1.425V@18.7A
Vtt=1.25V@2.3A
Vcccmos15=1.5V@250mA
Vcccmos18=1.8V@1mA
Vcore(state)=-0.080 to +0.040
Isgnt=TBD

370-Pin Socket Part 2

CPU1B
PGA-D370-B

Place 0603 package near VCMOS processor pin.

For Cu-T/Tualatin Only
Not backward compatible

For Future Compatible

PWRGD_CPU0 is 1.8V Signal

CLKREF Should be 1.25V for both Cu-T & Tualatin, But RCC set this resistor value to 100 Ohm.

DETECT VTT = Tualatin
GND = CuMine

GTLREF Generation Circuit

Use 0603 Packages and distribute within 500 miles of processor GTLREF inputs (1 cap for every 2 inputs)

CMOSREF Generation Circuit

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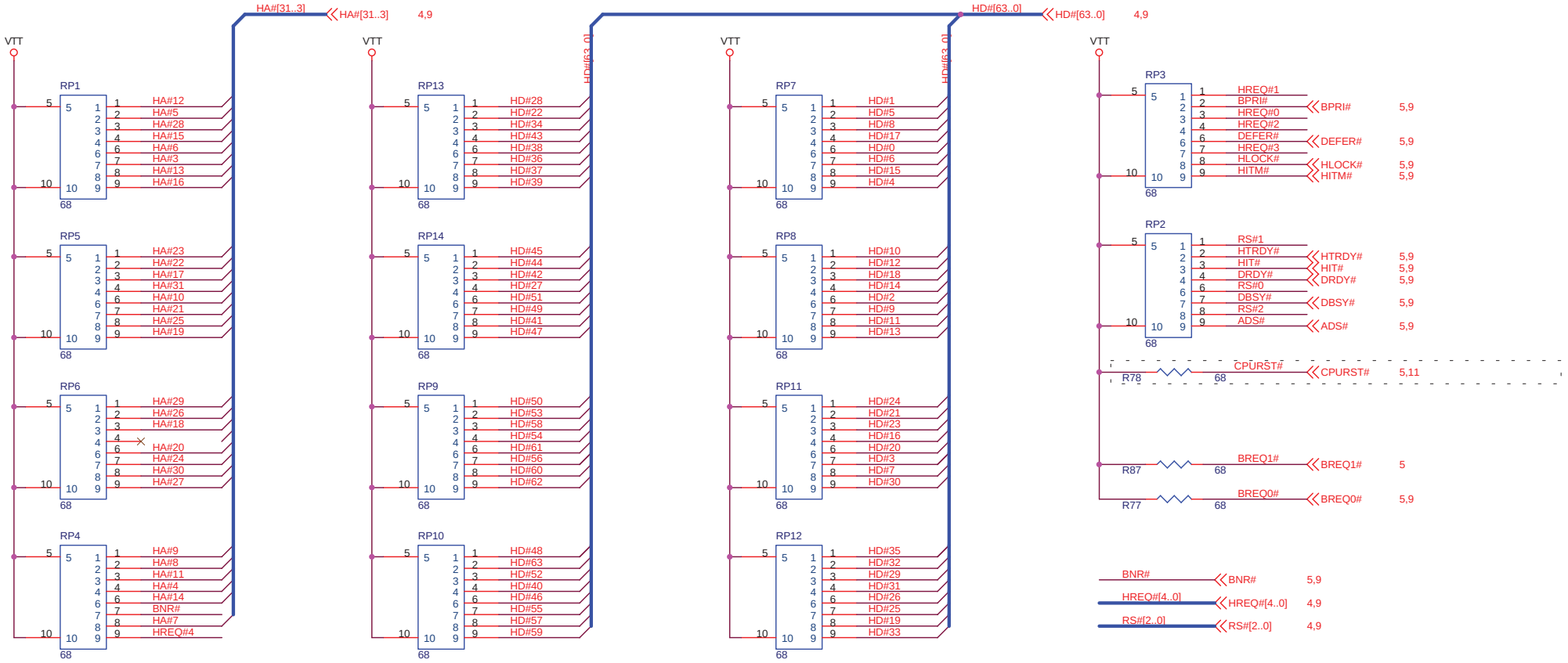
AGTL Termination



In RCC Reference Design without the GTL+ Bus termination. For signal quality issue we implement termination in our design.Put the termination inside the CPU2 socket.

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Title	AGTL Termination	Rev 100
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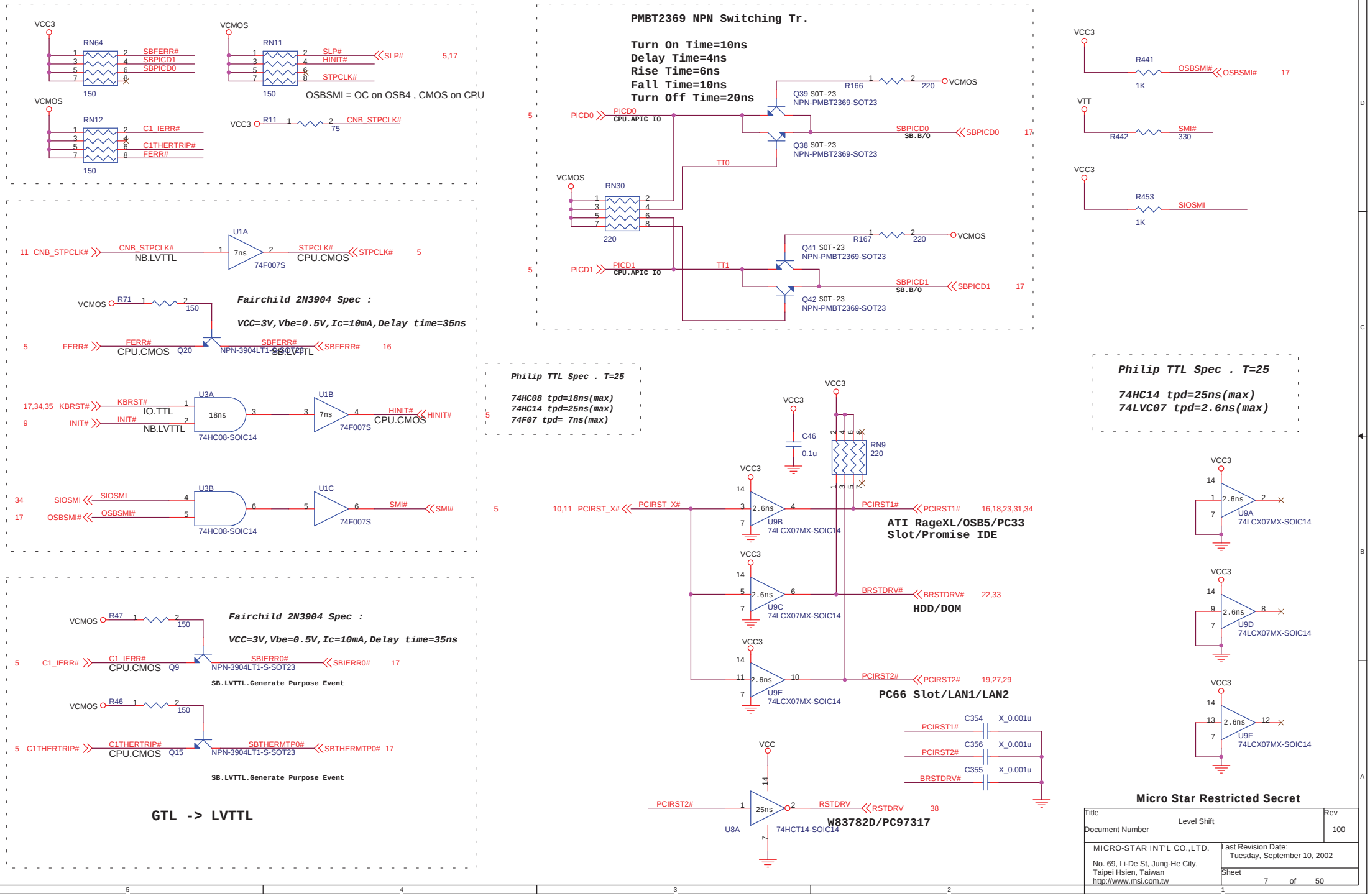

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Title	Level Shift	Rev 100
Document Number		
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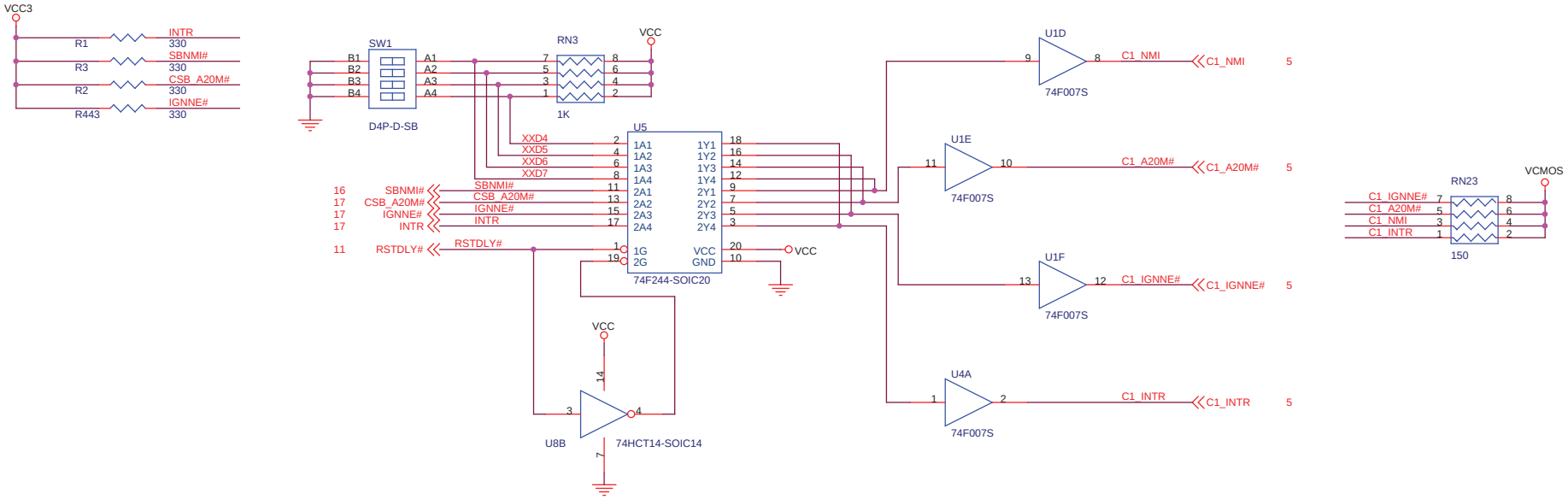

CPU FRACTION TABLE :

LINT[1]	LINT[0]	IGNNE#	A20M#	Fraction
0	0	0	0	2
0	0	0	1	4
0	0	1	0	3/11
0	0	1	1	5
0	1	0	0	2.5
0	1	0	1	4.5/8.5
0	1	1	0	3.5/11.5
0	1	1	1	5.5/9.5
1	0	0	0	6/10
1	0	0	1	8
1	0	1	0	7
1	0	1	1	Reserved
1	1	0	0	6.5/10.5
1	1	0	1	1.5
1	1	1	0	7.5
1	1	1	1	2

Title: Jumpless	Rev: 100
Document Number:	
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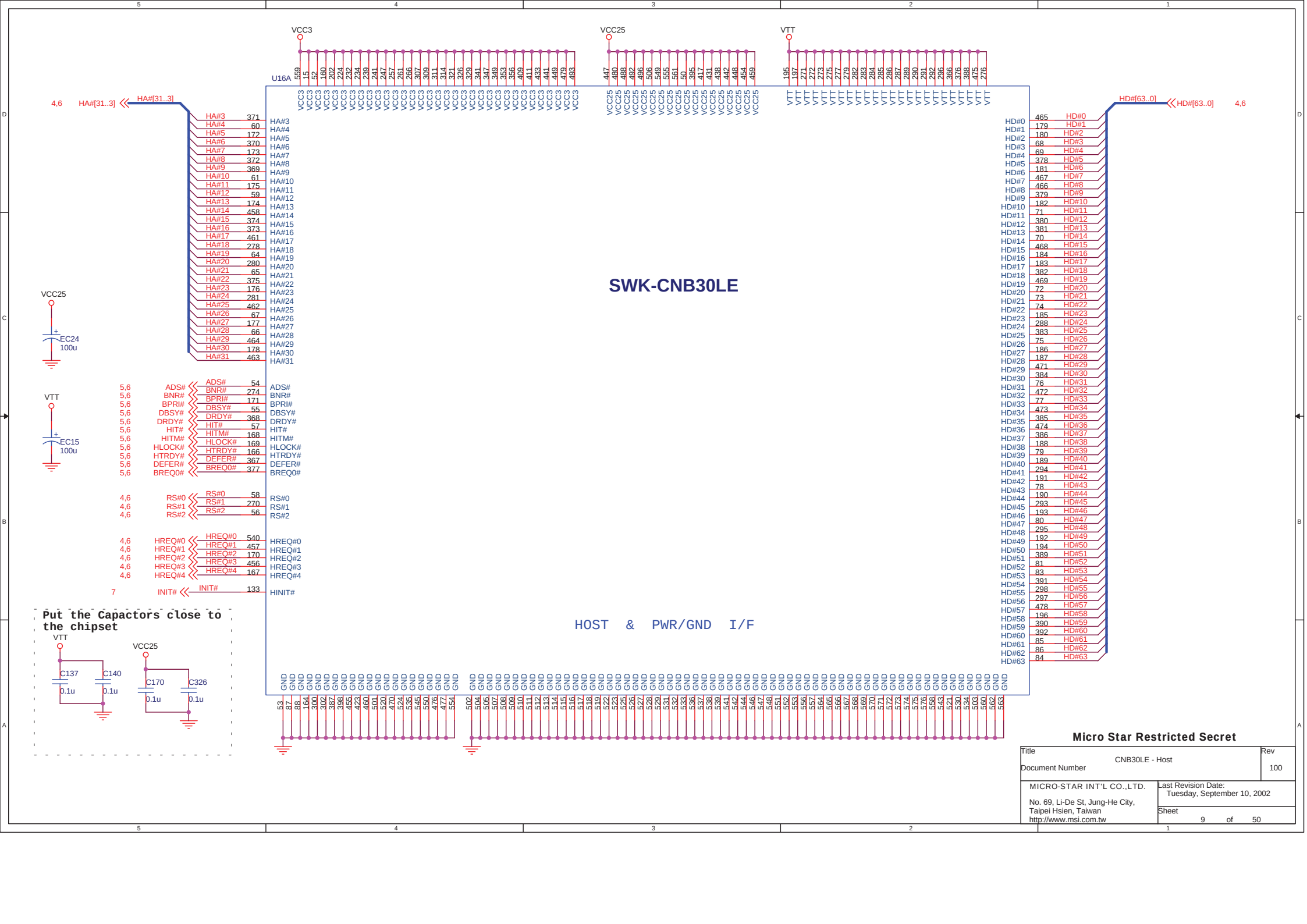
SWK-CNB30LE
HOST & PWR/GND I/F
U16A
VCC3
VCC25
VTT
HA#[31..3]
HD#[63..0]
ADS#
BNR#
BPRI#
DBSY#
DRDY#
HIT#
HITM#
HLOCK#
HTRDY#
DEFER#
BREQ0#
RS#0
RS#1
RS#2
HREQ#0
HREQ#1
HREQ#2
HREQ#3
HREQ#4
INIT#
HINIT#
EC24
100u
EC15
100u
Put the Capactors close to the chipset
C137
C140
C170
C326
0.1u
Micro Star Restricted Secret
Title
CNB30LE - Host
Document Number
100
Rev
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Power Comsuption of CNB30LE :

2.5V - 600mA for Core Logic
1.5V - 1.0A for GTL buffer
3.3V - 1.8A for Both PCI bus and Memory Bus

SDRDCLK — C110 10p

DLLRST# SCL SDA → DLLRST# SCL SDA 17,44 12,13,17,38 12,13,17,38

SDFBCLK R102 33 SDFBIN

SDRDCLK R108 22 RDCLK → RDCLK 14

U16C

DPLLRST# 89 | SCL 18 | SDA 338 | SDCLK 365 | SDFBIN 269 | SDRDCLK 453

12 AMA[12..0] → AMA[12..0]

AMA0	435	A_MA0
AMA1	434	A_MA1
AMA2	437	A_MA2
AMA3	436	A_MA3
AMA4	35	A_MA4
AMA5	253	A_MA5
AMA6	252	A_MA6
AMA7	36	A_MA7
AMA8	254	A_MA8
AMA9	149	A_MA9
AMA10	150	A_MA10
AMA11	256	A_MA11
AMA12	37	A_MA12

12 ABA0 ABA1

ABA0	255	A_BA0
ABA1	39	A_BA1

12 ARAS# ACAS# AWE# ACKE

ARAS#	251	A_RAS#
ACAS#	32	A_CAS#
AWE#	346	A_WE#
ACKE	27	A_CKE
	29	A_MUXSEL

13 BMA[12..0] → BMA[12..0]

BMA0	146	B_MA0
BMA1	147	B_MA1
BMA2	440	B_MA2
BMA3	34	B_MA3
BMA4	148	B_MA4
BMA5	351	B_MA5
BMA6	352	B_MA6
BMA7	151	B_MA7
BMA8	354	B_MA8
BMA9	38	B_MA9
BMA10	152	B_MA10
BMA11	258	B_MA11
BMA12	355	B_MA12

13 BBA0 BBA1

BBA0	444	B_BA0
BBA1	357	B_BA1

13 BRAS# BCAS# BWE# BCKE

BRAS#	33	B_RAS#
BCAS#	439	B_CAS#
BWE#	144	B_WE#
BCKE	141	B_CKE
	28	B_MUXSEL

12 CS#0 CS#1 13 CS#2 13 CS#3

CS#0	41	CS#0
CS#1	154	CS#1
CS#2	443	CS#2
CS#3	259	CS#3
CS#4	153	CS#4
CS#5	40	CS#5
CS#6	348	CS#6
CS#7	145	CS#7

TP1 TP2 TP3 TP4

M66EN_IN 107 → TEST1/M66EN

VCC3 R126 R180 X_2.2K 2.2K TMODE# 408 → TESTMODE#

350 → TEST2

SWK-CNB30LE

MEMEORY I/F

MD[63..0] → MD[63..0] 12,13

MD0	21	MD0
MD1	134	MD1
MD2	240	MD2
MD3	23	MD3
MD4	24	MD4
MD5	242	MD5
MD6	138	MD6
MD7	243	MD7
MD8	339	MD8
MD9	340	MD9
MD10	142	MD10
MD11	245	MD11
MD12	246	MD12
MD13	143	MD13
MD14	343	MD14
MD15	344	MD15
MD16	146	MD16
MD17	156	MD17
MD18	44	MD18
MD19	262	MD19
MD20	45	MD20
MD21	263	MD21
MD22	46	MD22
MD23	264	MD23
MD24	450	MD24
MD25	47	MD25
MD26	451	MD26
MD27	161	MD27
MD28	452	MD28
MD29	162	MD29
MD30	267	MD30
MD31	268	MD31
MD32	19	MD32
MD33	20	MD33
MD34	22	MD34
MD35	135	MD35
MD36	136	MD36
MD37	137	MD37
MD38	25	MD38
MD39	26	MD39
MD40	139	MD40
MD41	140	MD41
MD42	244	MD42
MD43	30	MD43
MD44	430	MD44
MD45	342	MD45
MD46	250	MD46
MD47	31	MD47
MD48	43	MD48
MD49	358	MD49
MD50	157	MD50
MD51	359	MD51
MD52	158	MD52
MD53	360	MD53
MD54	159	MD54
MD55	361	MD55
MD56	265	MD56
MD57	362	MD57
MD58	48	MD58
MD59	363	MD59
MD60	49	MD60
MD61	364	MD61
MD62	163	MD62
MD63	51	MD63

MECC0 MECC1 MECC2 MECC3 MECC4 MECC5 MECC6 MECC7

248 432 445 155 249 345 42 260

MECC7	MECC7	12,13
MECC6	MECC6	12,13
MECC5	MECC5	12,13
MECC4	MECC4	12,13
MECC3	MECC3	12,13
MECC2	MECC2	12,13
MECC1	MECC1	12,13
MECC0	MECC0	12,13

By Datasheet Check List :

TEST1 should be pull-dwon1K
TEST2 should be pull-up 2.2K - 4.7K to 3.3V
TESTMODE# should be pull-up 2.2K - 4.7K to 3.3V

VCC25 — R154 1K — DLLRST#

VCC3 — R176 X_2.7K — SCL

VCC3 — R172 X_2.7K — SDA

Put the Capactors on the solder side

VCC25: C333 1u, C322 1u
VTT: C327 1u, C102 1u

Put the Capactors on the solder side

VCC3: C328 0.1u, C330 0.1u, C334 0.1u
VCC25: C331 0.1u
VTT: C321 0.1u

Put the Capactors on the solder side

VCC3: C324 0.1u, C323 0.1u, C329 1u, C332 1u

Put the Capactors on the corner of chipset

VCC3: C124 0.1u, C100 0.1u, C157 0.1u, C190 0.1u
VCC3: C104 1u, C159 1u, C182 1u, C132 1u

M66EN_IN to latch at PCIRESET to configure the DPLL to generate 33MHz or 66MHz out on PCICLK_O

L = 33MHz
H = 66MHz

7,11 PCIRST_X# → U2A 74HCT14-SOIC14

Q36 NDS7002A-S-SOT23

19 M66EN → R331 2.2K → VCC3

M66EN_IN → R184 X_2.2K → VCC3

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Title	CNB30LE - Memory	Rev 100
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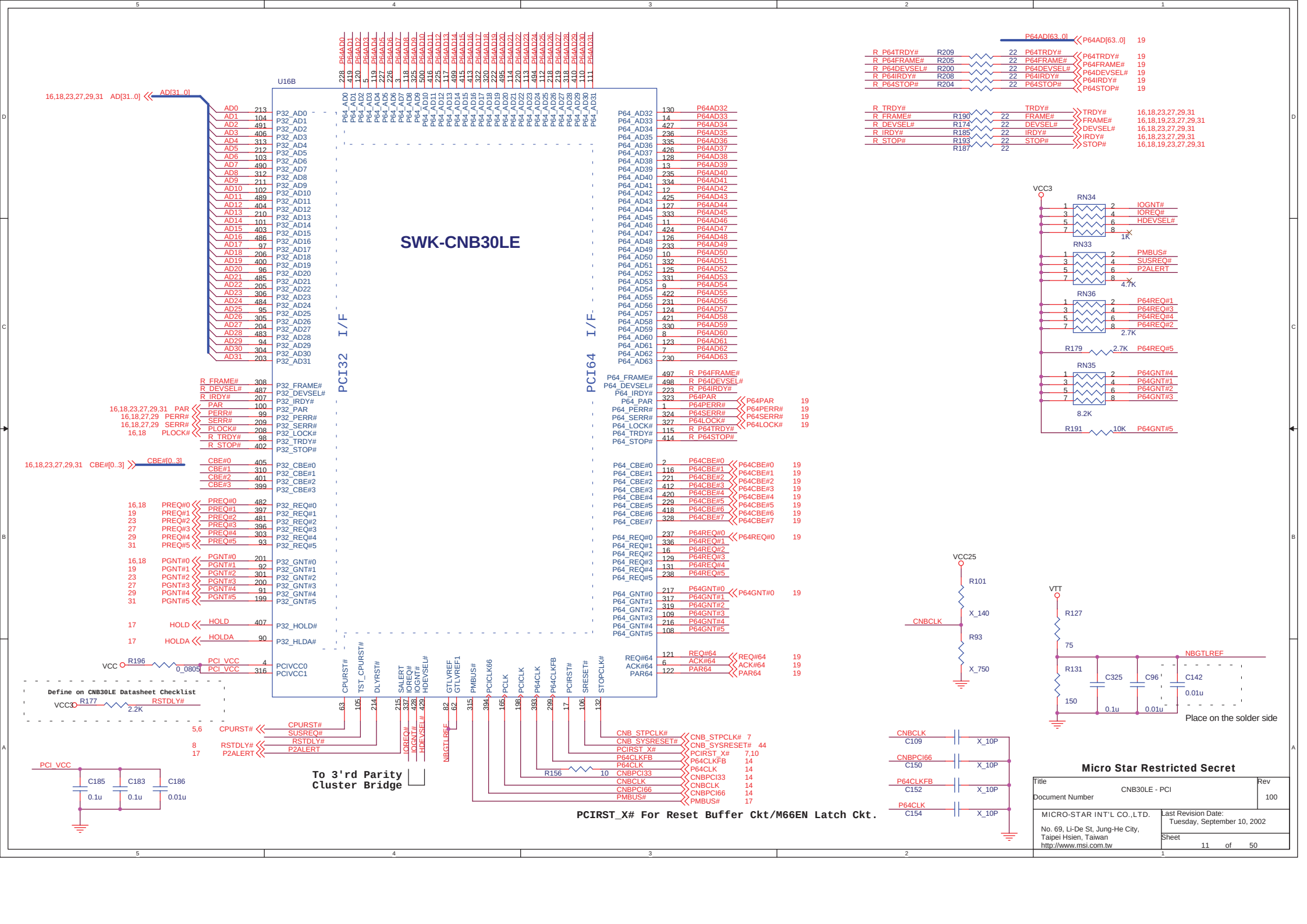
SWK-CNB30LE
U16B
PCI32 I/F
PCI64 I/F
P32_AD0
P32_AD1
P32_AD2
P32_AD3
P32_AD4
P32_AD5
P32_AD6
P32_AD7
P32_AD8
P32_AD9
P32_AD10
P32_AD11
P32_AD12
P32_AD13
P32_AD14
P32_AD15
P32_AD16
P32_AD17
P32_AD18
P32_AD19
P32_AD20
P32_AD21
P32_AD22
P32_AD23
P32_AD24
P32_AD25
P32_AD26
P32_AD27
P32_AD28
P32_AD29
P32_AD30
P32_AD31
P32_FRAME#
P32_DEVSEL#
P32_IRDY#
P32_PAR
P32_PERR#
P32_SERR#
P32_LOCK#
P32_TRDY#
P32_STOP#
P32_CBE#0
P32_CBE#1
P32_CBE#2
P32_CBE#3
P32_REQ#0
P32_REQ#1
P32_REQ#2
P32_REQ#3
P32_REQ#4
P32_REQ#5
P32_GNT#0
P32_GNT#1
P32_GNT#2
P32_GNT#3
P32_GNT#4
P32_GNT#5
P32_HOLD#
P32_HLDA#
PCIVCC0
PCIVCC1
P64_AD32
P64_AD33
P64_AD34
P64_AD35
P64_AD36
P64_AD37
P64_AD38
P64_AD39
P64_AD40
P64_AD41
P64_AD42
P64_AD43
P64_AD44
P64_AD45
P64_AD46
P64_AD47
P64_AD48
P64_AD49
P64_AD50
P64_AD51
P64_AD52
P64_AD53
P64_AD54
P64_AD55
P64_AD56
P64_AD57
P64_AD58
P64_AD59
P64_AD60
P64_AD61
P64_AD62
P64_AD63
P64_FRAME#
P64_DEVSEL#
P64_IRDY#
P64_PAR
P64_PERR#
P64_SERR#
P64_LOCK#
P64_TRDY#
P64_STOP#
P64_CBE#0
P64_CBE#1
P64_CBE#2
P64_CBE#3
P64_CBE#4
P64_CBE#5
P64_CBE#6
P64_CBE#7
P64_REQ#0
P64_REQ#1
P64_REQ#2
P64_REQ#3
P64_REQ#4
P64_REQ#5
P64_GNT#0
P64_GNT#1
P64_GNT#2
P64_GNT#3
P64_GNT#4
P64_GNT#5
REQ#64
ACK#64
PAR64
CPURST#
TST_CPURST#
DLYRST#
SALERT
IOREQ#
IOGNT#
HDEVSEL#
GTLVREF
GTLVREF1
PMBUS#
PCICLK66
PCLK
PCICLK
P64CLK
P64CLKFB
PCIRST#
SRESET#
STOPCLK#
CPURST#
SUSREQ#
RSTDLY#
P2ALERT
RSTDLY#
2.2K
R177
VCC3
R196
0_0805
VCC
PCI_VCC
Define on CNB30LE Datasheet Checklist
To 3'rd Parity Cluster Bridge
CNB_STPCLK#
CNB_SYSRESET#
PCIRST_X#
P64CLKFB
P64CLK
CNBPCI33
CNBCLK
CNBPCI66
PMBUS#
R156
10
PCIRST_X# For Reset Buffer Ckt/M66EN Latch Ckt.
C185
C183
C186
0.1u
0.1u
0.01u
R_P64TRDY#
R_P64FRAME#
R_P64DEVSEL#
R_P64IRDY#
R_P64STOP#
R209
R205
R200
R208
R204
R_TRDY#
R_FRAME#
R_DEVSEL#
R_IRDY#
R_STOP#
R190
R174
R185
R193
R187
RN34
RN33
RN36
RN35
IOGNT#
IOREQ#
HDEVSEL#
PMBUS#
SUSREQ#
P2ALERT
P64REQ#1
P64REQ#3
P64REQ#4
P64REQ#2
P64GNT#4
P64GNT#1
P64GNT#2
P64GNT#3
1K
4.7K
2.7K
8.2K
R179
R191
10K
P64GNT#5
VCC25
VTT
CNBCLK
X_140
R93
X_750
R101
R127
75
R131
150
C325
C96
C142
0.1u
0.01u
0.01u
NBGTLREF
Place on the solder side
CNBCLK
C109
CNBPCI66
C150
P64CLKFB
C152
P64CLK
C154
X_10P
Micro Star Restricted Secret
Title
CNB30LE - PCI
Document Number
Rev
100
MICRO-STAR INT'L CO.,LTD.
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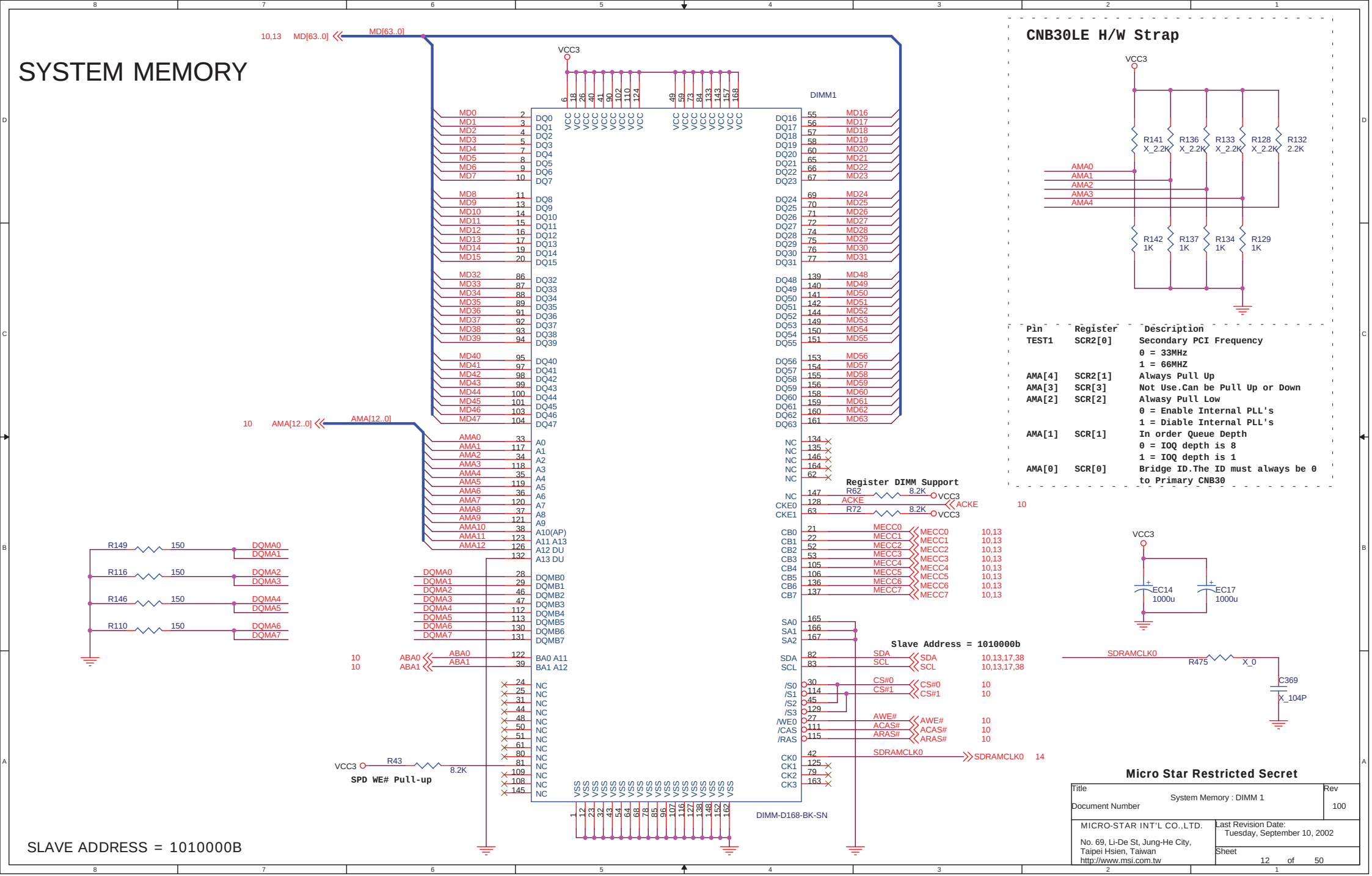
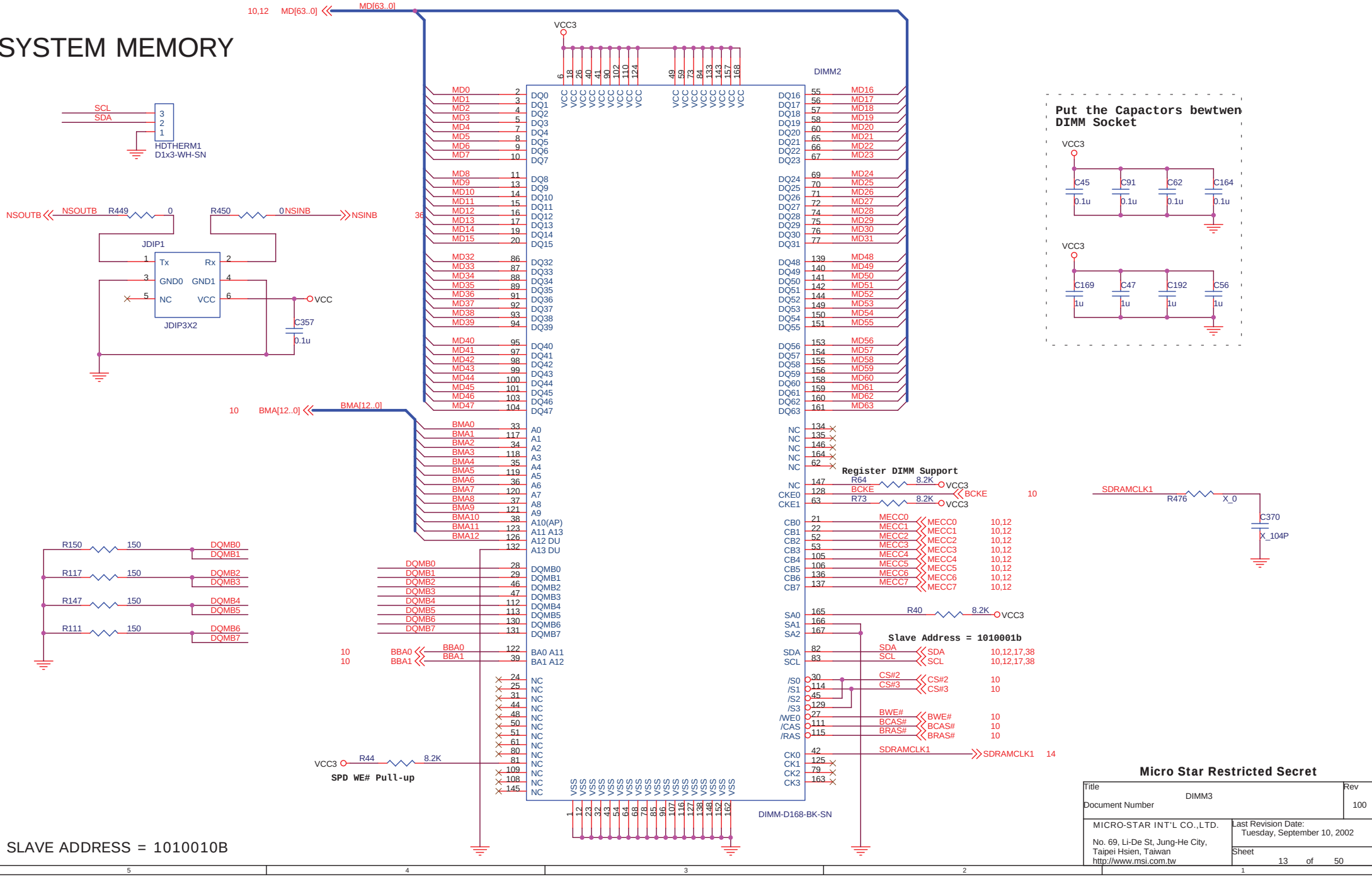
SYSTEM MEMORY



SYSTEM MEMORY



SLAVE ADDRESS = 1010010B

Micro Star Restricted Secret

Title	DIMM3	Rev 100
Document Number		

MICRO-STAR INT'L CO.,LTD.
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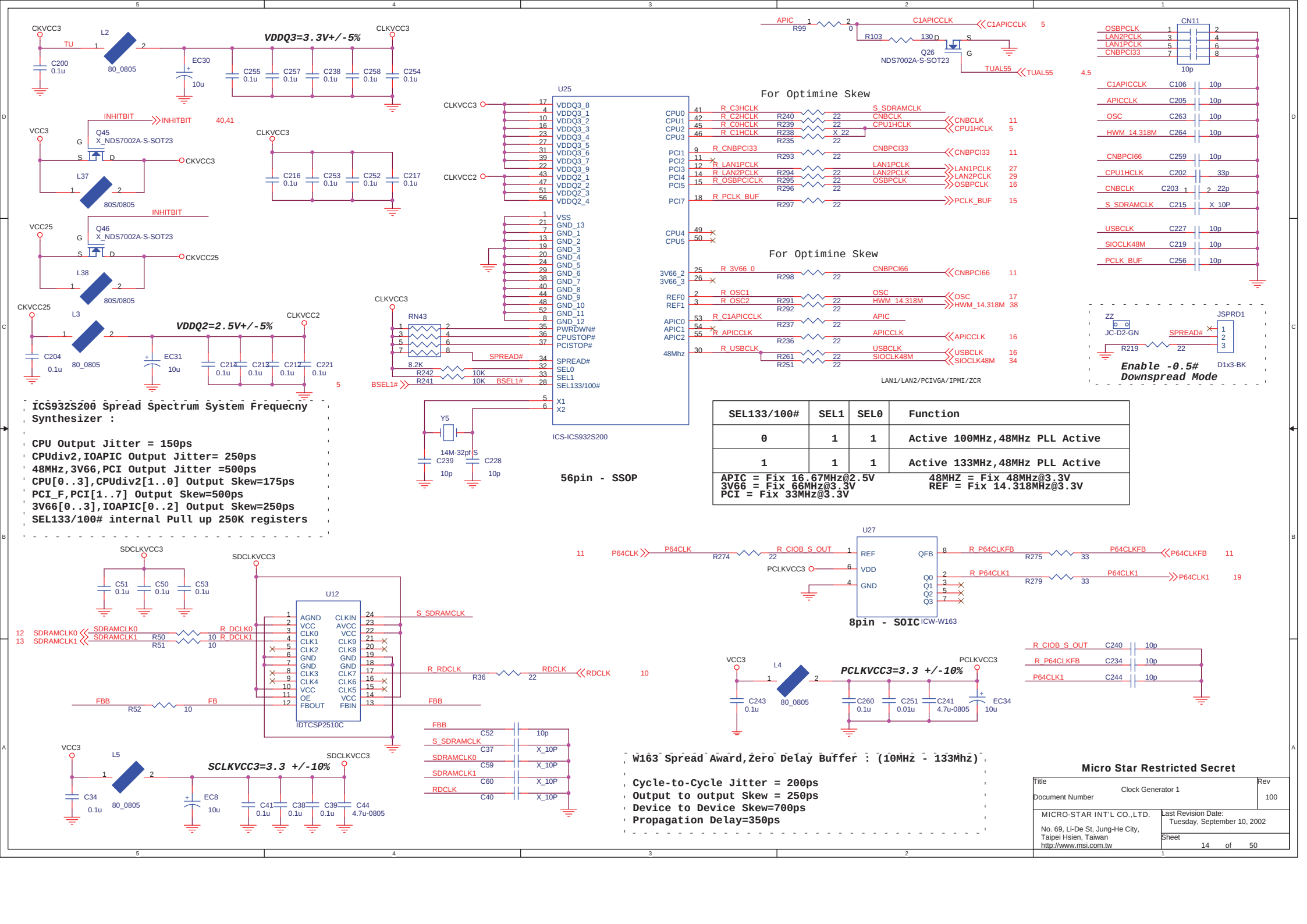

ICS932S200 Spread Spectrum System Frequecny Synthesizer :

CPU Output Jitter = 150ps
CPUdiv2,IOAPIC Output Jitter= 250ps
48MHz,3V66,PCI Output Jitter =500ps
CPU[0..3],CPUdiv2[1..0] Output Skew=175ps
PCI_F,PCI[1..7] Output Skew=500ps
3V66[0..3],IOAPIC[0..2] Output Skew=250ps
SEL133/100# internal Pull up 250K registers

SEL133/100#	SEL1	SEL0	Function
0	1	1	Active 100MHz,48MHz PLL Active
1	1	1	Active 133MHz,48MHz PLL Active

APIC = Fix 16.67MHz@2.5V　　48MHZ = Fix 48MHz@3.3V
3V66 = Fix 66MHz@3.3V　　REF = Fix 14.318MHz@3.3V
PCI = Fix 33MHz@3.3V

W163 Spread Award,Zero Delay Buffer : (10MHz - 133Mhz)

Cycle-to-Cycle Jitter = 200ps
Output to output Skew = 250ps
Device to Device Skew=700ps
Propagation Delay=350ps

Micro Star Restricted Secret

Title	Clock Generator 1	Rev 100
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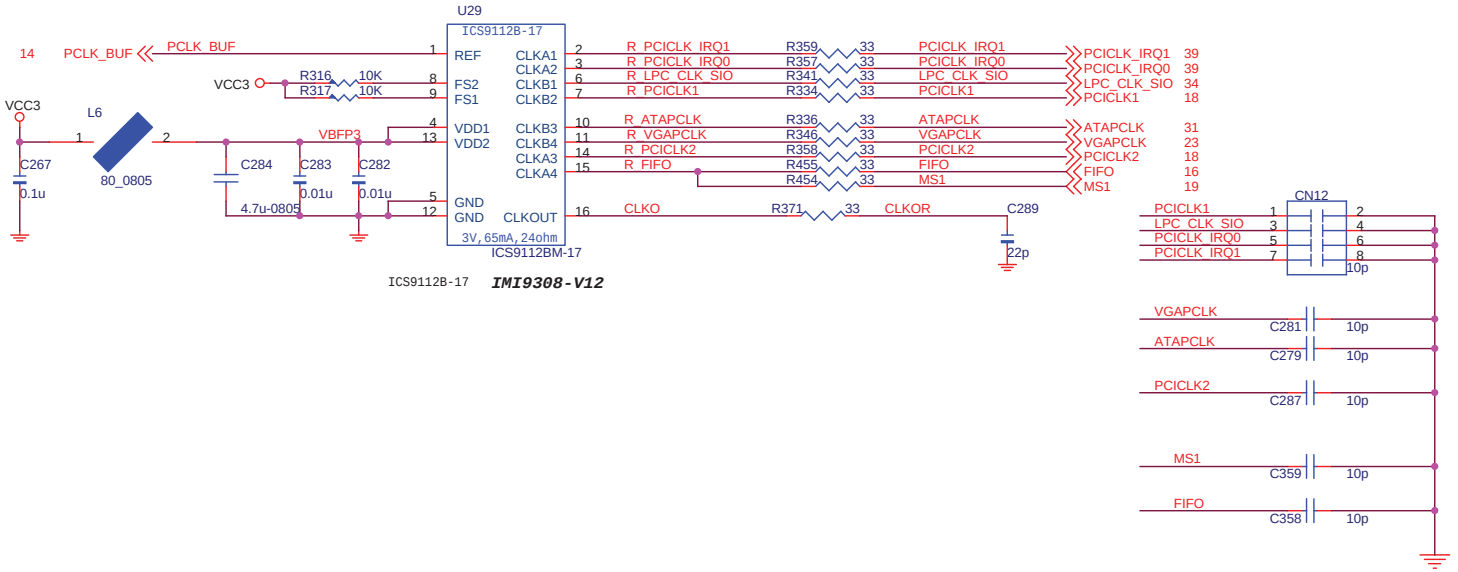
Clock Generator 2



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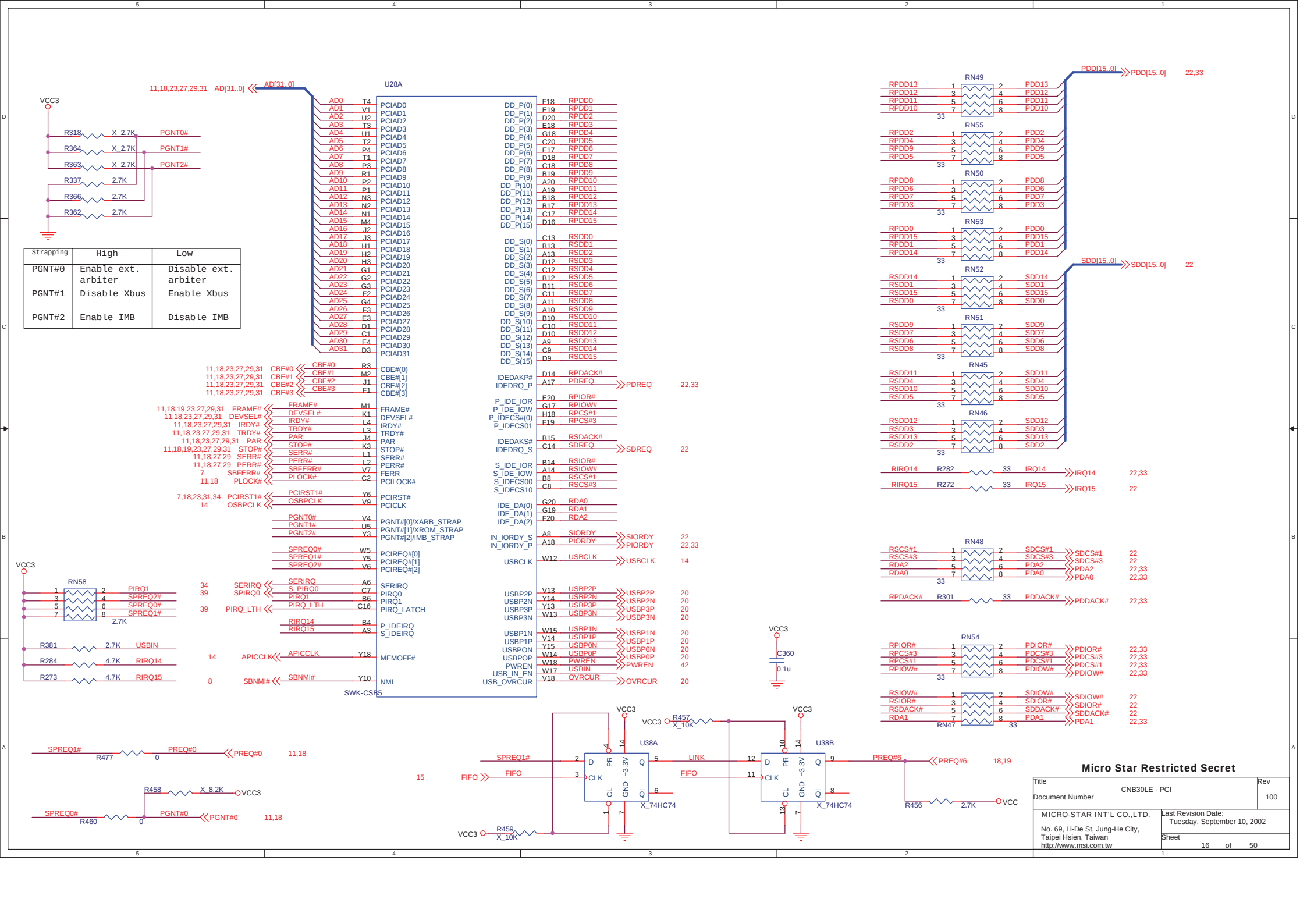
VCC3
R318 X_2.7K PGNT0#
R364 X_2.7K PGNT1#
R363 X_2.7K PGNT2#
R337 2.7K
R366 2.7K
R362 2.7K
Strapping | High | Low
PGNT#0 | Enable ext. arbiter | Disable ext. arbiter
PGNT#1 | Disable Xbus | Enable Xbus
PGNT#2 | Enable IMB | Disable IMB
11,18,23,27,29,31 AD[31..0]
AD[31..0]
U28A
PCIAD0 PCIAD1 PCIAD2 PCIAD3 PCIAD4 PCIAD5 PCIAD6 PCIAD7 PCIAD8 PCIAD9 PCIAD10 PCIAD11 PCIAD12 PCIAD13 PCIAD14 PCIAD15 PCIAD16 PCIAD17 PCIAD18 PCIAD19 PCIAD20 PCIAD21 PCIAD22 PCIAD23 PCIAD24 PCIAD25 PCIAD26 PCIAD27 PCIAD28 PCIAD29 PCIAD30 PCIAD31
DD_P(0) DD_P(1) DD_P(2) DD_P(3) DD_P(4) DD_P(5) DD_P(6) DD_P(7) DD_P(8) DD_P(9) DD_P(10) DD_P(11) DD_P(12) DD_P(13) DD_P(14) DD_P(15)
DD_S(0) DD_S(1) DD_S(2) DD_S(3) DD_S(4) DD_S(5) DD_S(6) DD_S(7) DD_S(8) DD_S(9) DD_S(10) DD_S(11) DD_S(12) DD_S(13) DD_S(14) DD_S(15)
RPDD0 RPDD1 RPDD2 RPDD3 RPDD4 RPDD5 RPDD6 RPDD7 RPDD8 RPDD9 RPDD10 RPDD11 RPDD12 RPDD13 RPDD14 RPDD15
RSDD0 RSDD1 RSDD2 RSDD3 RSDD4 RSDD5 RSDD6 RSDD7 RSDD8 RSDD9 RSDD10 RSDD11 RSDD12 RSDD13 RSDD14 RSDD15
11,18,23,27,29,31 CBE#0 CBE#1 CBE#2 CBE#3
CBE#(0) CBE#[1] CBE#[2] CBE#[3]
11,18,19,23,27,29,31 FRAME#
11,18,23,27,29,31 DEVSEL#
11,18,23,27,29,31 IRDY#
11,18,23,27,29,31 TRDY#
11,18,23,27,29,31 PAR
11,18,19,23,27,29,31 STOP#
11,18,23,27,29 SERR#
11,18,23,27,29 PERR#
7 SBFERR#
11,18 PLOCK#
FRAME# DEVSEL# IRDY# TRDY# PAR STOP# SERR# PERR# FERR PCILOCK#
7,18,23,31,34 PCIRST1#
14 OSBPCLK
PCIRST# PCICLK
PGNT0# PGNT1# PGNT2#
PGNT#[0]/XARB_STRAP
PGNT#[1]/XROM_STRAP
PGNT#[2]/IMB_STRAP
SPREQ0# SPREQ1# SPREQ2#
PCIREQ#[0] PCIREQ#[1] PCIREQ#[2]
IDEDAKP# IDEDRQ_P
P_IDE_IOR P_IDE_IOW P_IDECS#(0) P_IDECS01
IDEDAKS# IDEDRQ_S
S_IDE_IOR S_IDE_IOW S_IDECS00 S_IDECS10
IDE_DA(0) IDE_DA(1) IDE_DA(2)
IN_IORDY_S IN_IORDY_P
USBCLK
RPDACK# PDREQ RPIOW# RPCS#1 RPCS#3 RDA0 RDA2 SIORDY PIORDY SDREQ RSIOR# RSIOW# RSCS#1 RSCS#3 RSDACK#
PDREQ 22,33
SDREQ 22
SIORDY 22
PIORDY 22,33
USBCLK 14
VCC3
RN58
PIRQ1 SPREQ2# SPREQ0# SPREQ1#
2.7K
34 SERIRQ
39 SPIRQ0
39 PIRQ_LTH
SERIRQ S_PIRQ0 PIRQ1 PIRQ_LTH
RIRQ14 RIRQ15
P_IDEIRQ S_IDEIRQ
R381 2.7K USBIN
R284 4.7K RIRQ14
R273 4.7K RIRQ15
14 APICCLK
APICCLK MEMOFF#
8 SBNMI#
SBNMI# NMI
SWK-CSB5
USBP2P USBP2N USBP3P USBP3N
USBP1N USBP1P USBP0N USBP0P PWREN USB_IN_EN USB_OVRCUR
USBP2P USBP2N USBP3P USBP3N
USBP1N USBP1P USBP0N USBP0P PWREN USBIN OVRCUR
20 20 20 20 20 20 42 20
VCC3 C360 0.1u
RN49 RPDD13 RPDD12 RPDD11 RPDD10 PDD13 PDD12 PDD11 PDD10
RN55 RPDD2 RPDD4 RPDD9 RPDD5 PDD2 PDD4 PDD9 PDD5
RN50 RPDD8 RPDD6 RPDD7 RPDD3 PDD8 PDD6 PDD7 PDD3
RN53 RPDD0 RPDD15 RPDD1 RPDD14 PDD0 PDD15 PDD1 PDD14
PDD[15..0] PDD[15..0] 22,33
RN52 RSDD14 RSDD1 RSDD15 RSDD0 SDD14 SDD1 SDD15 SDD0
RN51 RSDD9 RSDD7 RSDD6 RSDD8 SDD9 SDD7 SDD6 SDD8
RN45 RSDD11 RSDD4 RSDD10 RSDD5 SDD11 SDD4 SDD10 SDD5
RN46 RSDD12 RSDD3 RSDD13 RSDD2 SDD12 SDD3 SDD13 SDD2
SDD[15..0] SDD[15..0] 22
RIRQ14 R282 33 IRQ14 IRQ14 22,33
RIRQ15 R272 33 IRQ15 IRQ15 22
RN48 RSCS#1 RSCS#3 RDA2 RDA0 SDCS#1 SDCS#3 PDA2 PDA0
RPDACK# R301 33 PDDACK# PDDACK# 22,33
RN54 RPIOR# RPCS#3 RPCS#1 RPIOW# PDIOR# PDCS#3 PDCS#1 PDIOW#
RN47 RSIOW# RSIOR# RSDACK# RDA1 SDIOW# SDIOR# SDDACK# PDA1
SPREQ1# R477 0 PREQ#0 PREQ#0 11,18
R458 X_8.2K VCC3
SPREQ0# R460 0 PGNT#0 PGNT#0 11,18
15 FIFO
VCC3 R457 X_10K
VCC3 R459 X_10K
U38A U38B
SPREQ1# FIFO LINK PREQ#6
D PR +3.3V Q CLK CL GND QI
X_74HC74
PREQ#6 PREQ#6 18,19
R456 2.7K VCC
Micro Star Restricted Secret
Title CNB30LE - PCI
Document Number
Rev 100
MICRO-STAR INT'L CO.,LTD.
No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan
http://www.msi.com.tw
Last Revision Date: Tuesday, September 10, 2002
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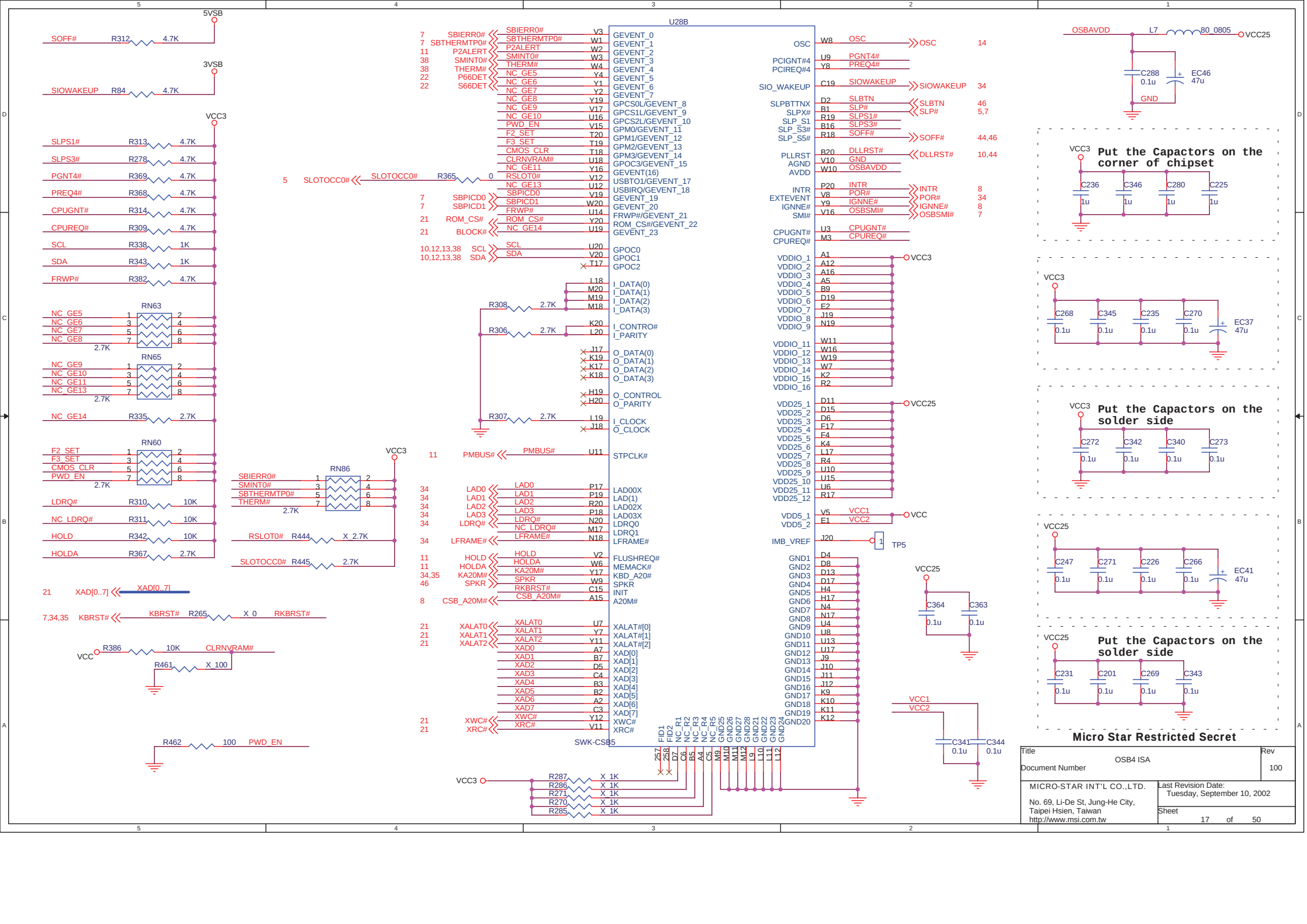
U28B
SWK-CSB5
Put the Capactors on the corner of chipset
Put the Capactors on the solder side
Put the Capactors on the solder side
Micro Star Restricted Secret
Title
OSB4 ISA
Document Number
Rev
100
MICRO-STAR INT'L CO.,LTD.
No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan
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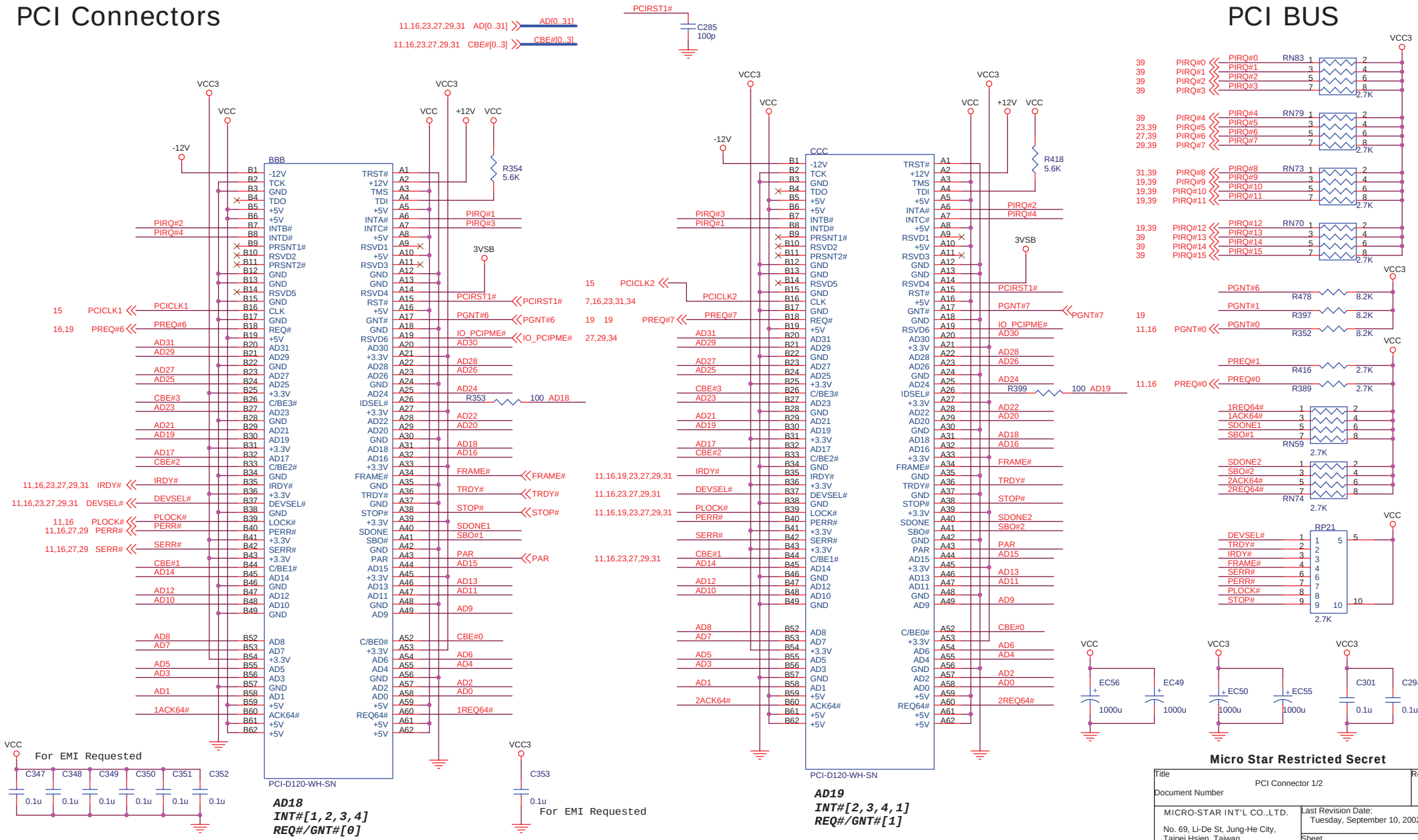
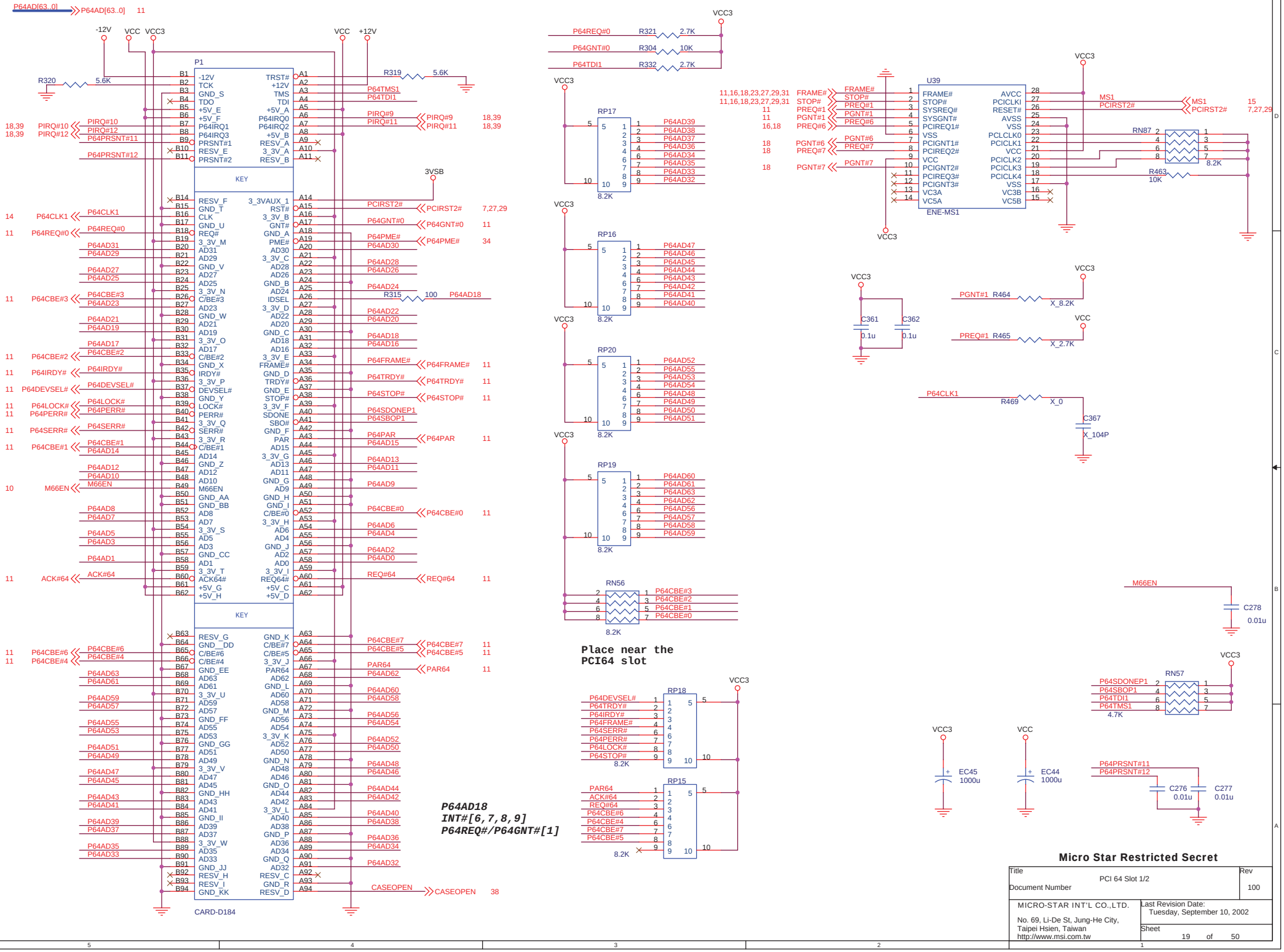
PCI Connectors



PCI BUS

Micro Star Restricted Secret

Title	PCI Connector 1/2	Rev 100
Document Number		
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Tuesday, September 10, 2002 Sheet 18 of 50


P64AD[63..0]
P64AD[63..0] 11
P1
CARD-D184
KEY
R320 5.6K
R319 5.6K
3VSB
P64PRSNT#12
P64PRSNT#11
PIRQ#10
PIRQ#12
P64CLK1
P64REQ#0
P64CBE#3
P64CBE#2
P64CBE#1
P64CBE#6
P64CBE#4
P64IRDY#
P64DEVSEL#
P64LOCK#
P64PERR#
P64SERR#
M66EN
ACK#64
P64PRSNT#1
P64PRSNT#2
P64REQ#0 R321 2.7K
P64GNT#0 R304 10K
P64TDI1 R332 2.7K
RP17
RP16
RP20
RP19
RN56
8.2K
Place near the PCI64 slot
RP18
RP15
P64AD18
INT#[6,7,8,9]
P64REQ#/P64GNT#[1]
CASEOPEN
U39
ENE-MS1
R463 10K
RN87 8.2K
R464 X_8.2K
R465 X_2.7K
R469 X_0
C361 0.1u
C362 0.1u
C367 X_104P
C278 0.01u
RN57 4.7K
EC45 1000u
EC44 1000u
C276 0.01u
C277 0.01u
Micro Star Restricted Secret
Title PCI 64 Slot 1/2
Document Number 100
Rev
MICRO-STAR INT'L CO.,LTD.
No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan
http://www.msi.com.tw
Last Revision Date: Tuesday, September 10, 2002
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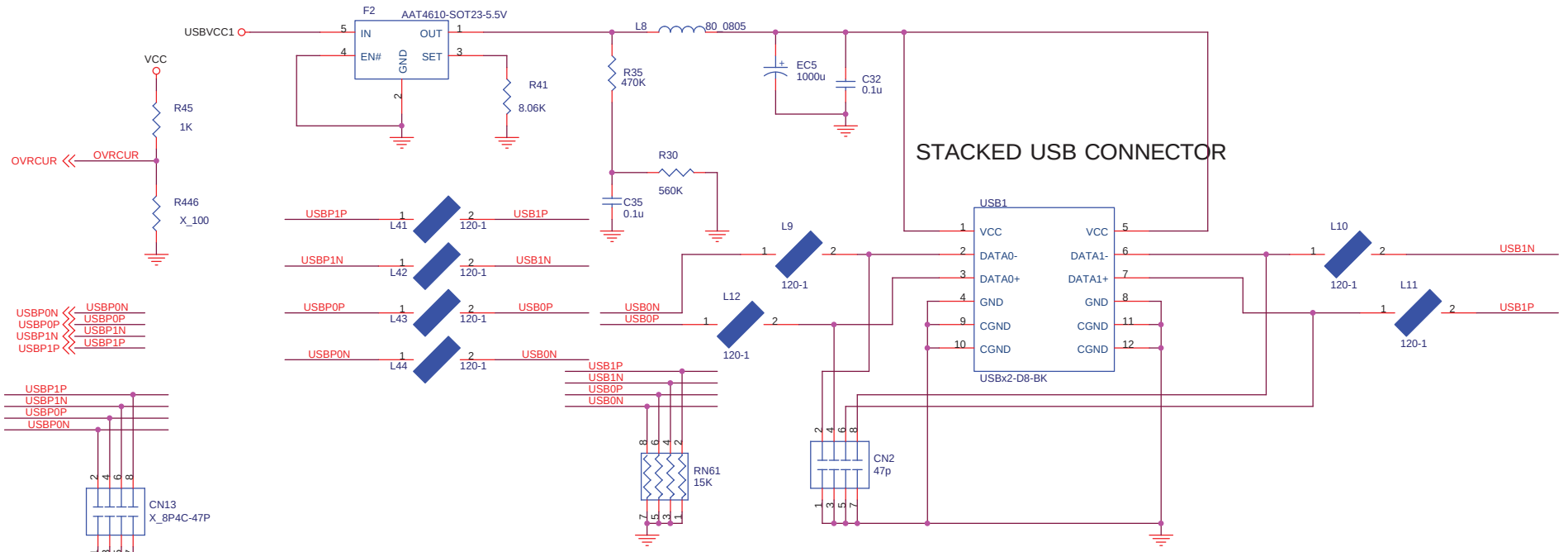
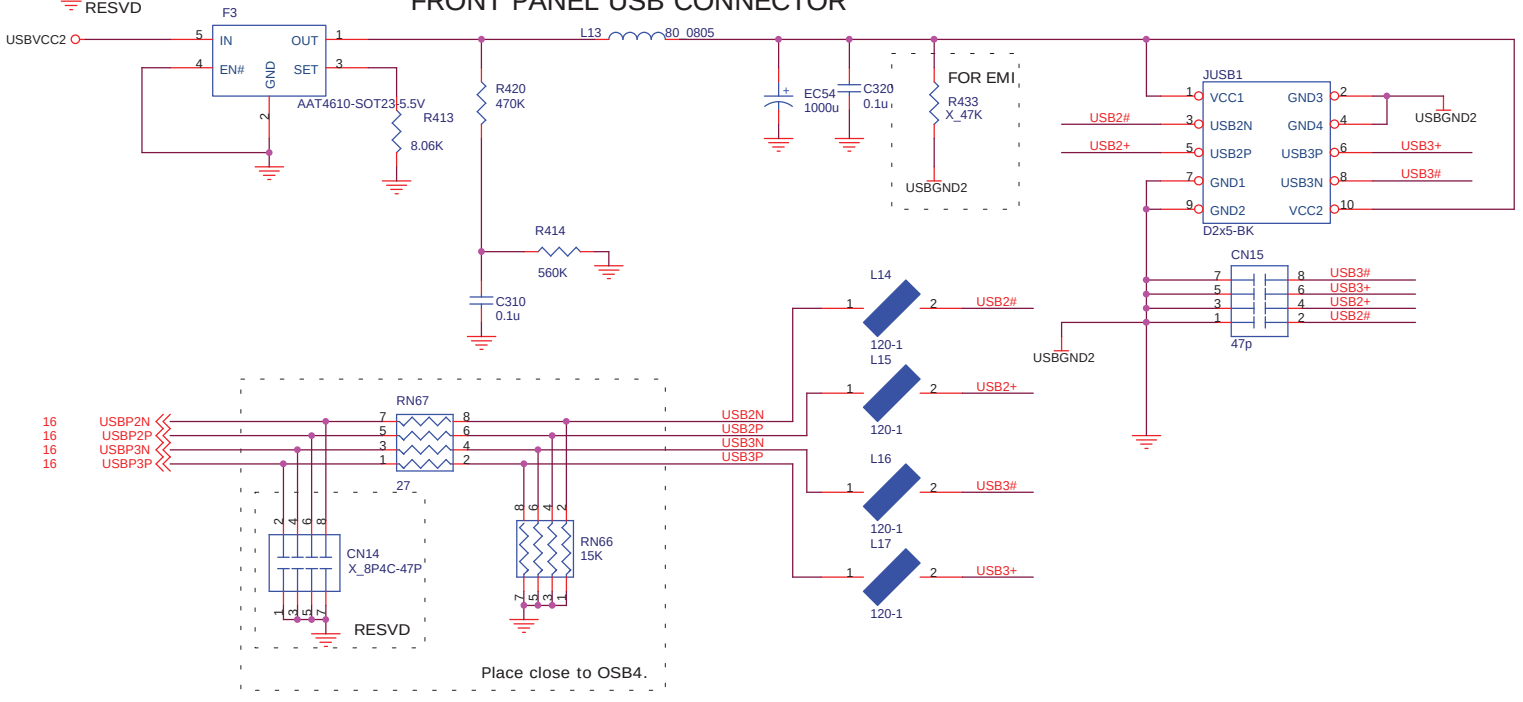
USB Connectors



FRONT PANEL USB CONNECTOR



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Title	USB Connectors	Rev 100
Document Number		
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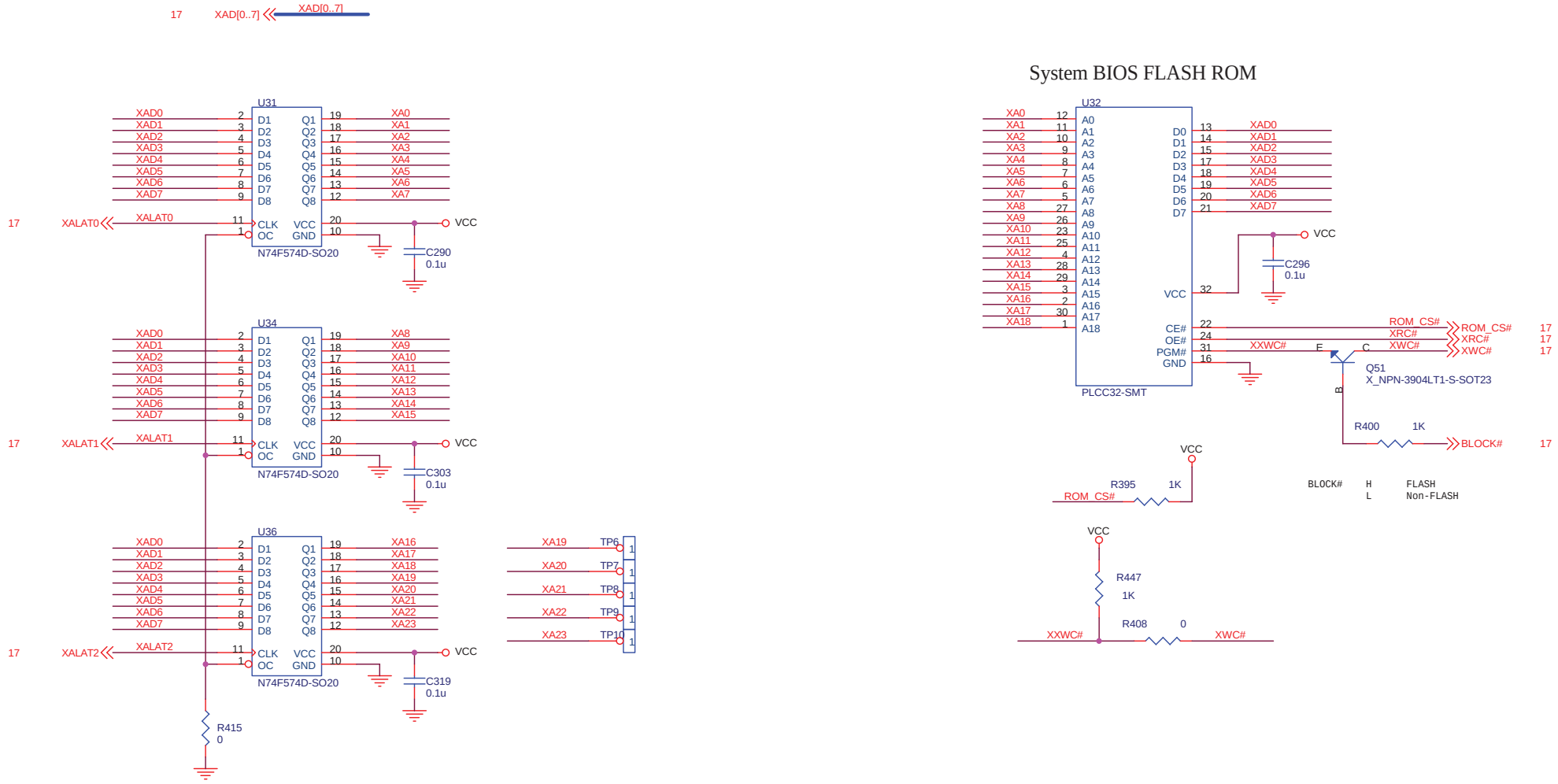


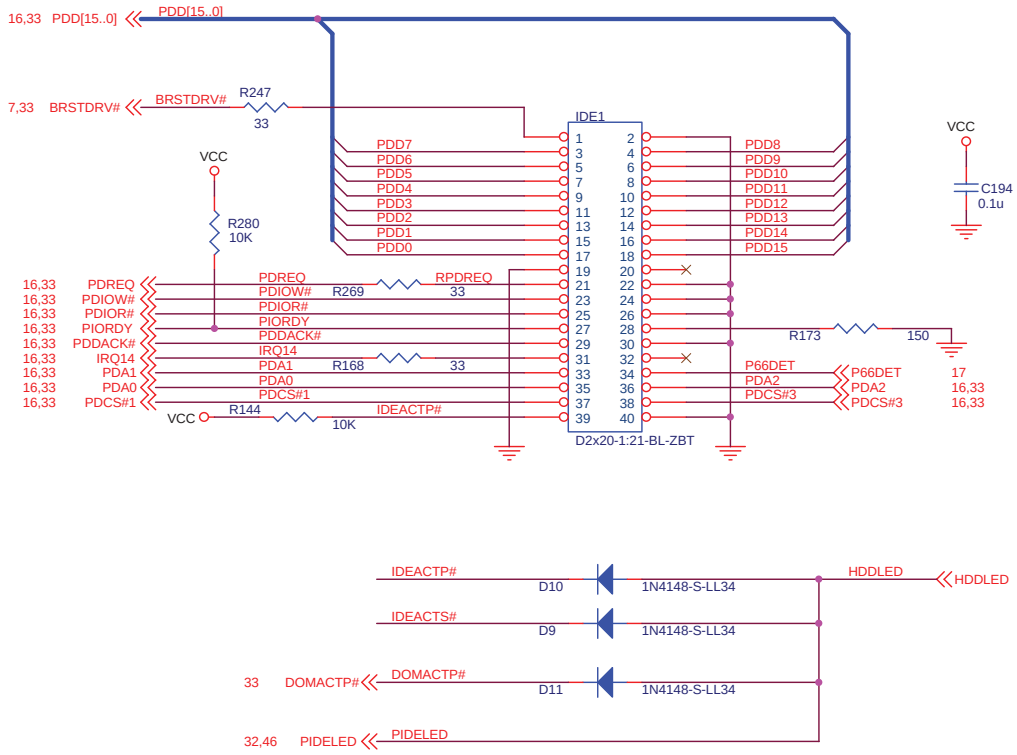
System BIOS FLASH ROM

Micro Star Restricted Secret

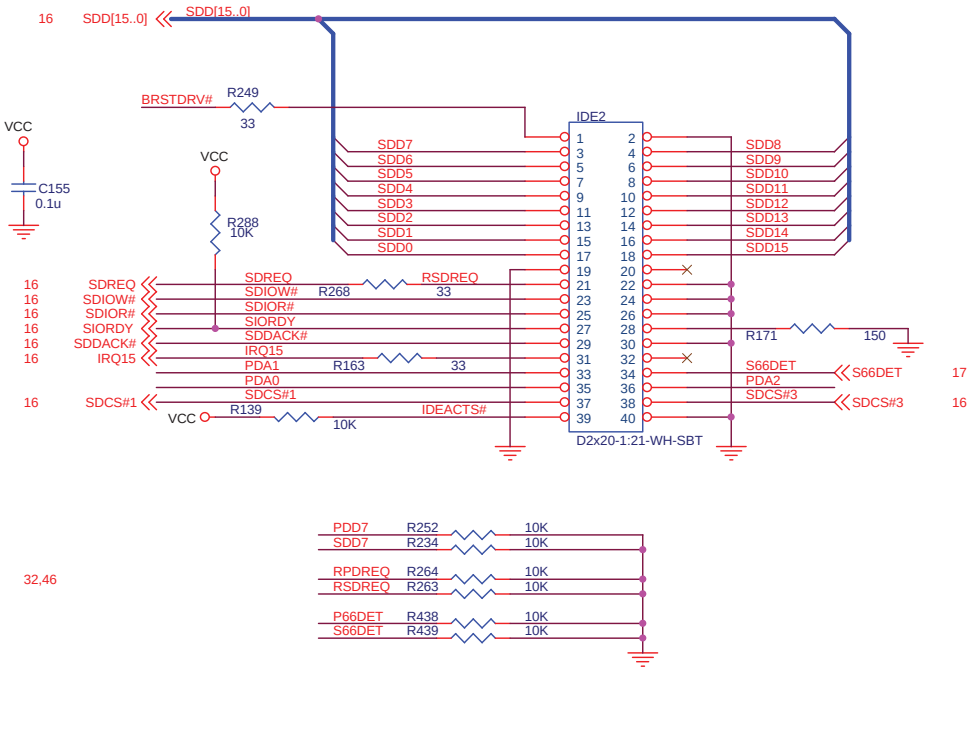
Title	Flash ROM & XAD Ckt	Rev 100
Document Number		
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Tuesday, September 10, 2002 Sheet 21 of 50

ATA100 IDE CONNECTORS

PRIMARY IDE CONN.



SECONDARY IDE CONN.



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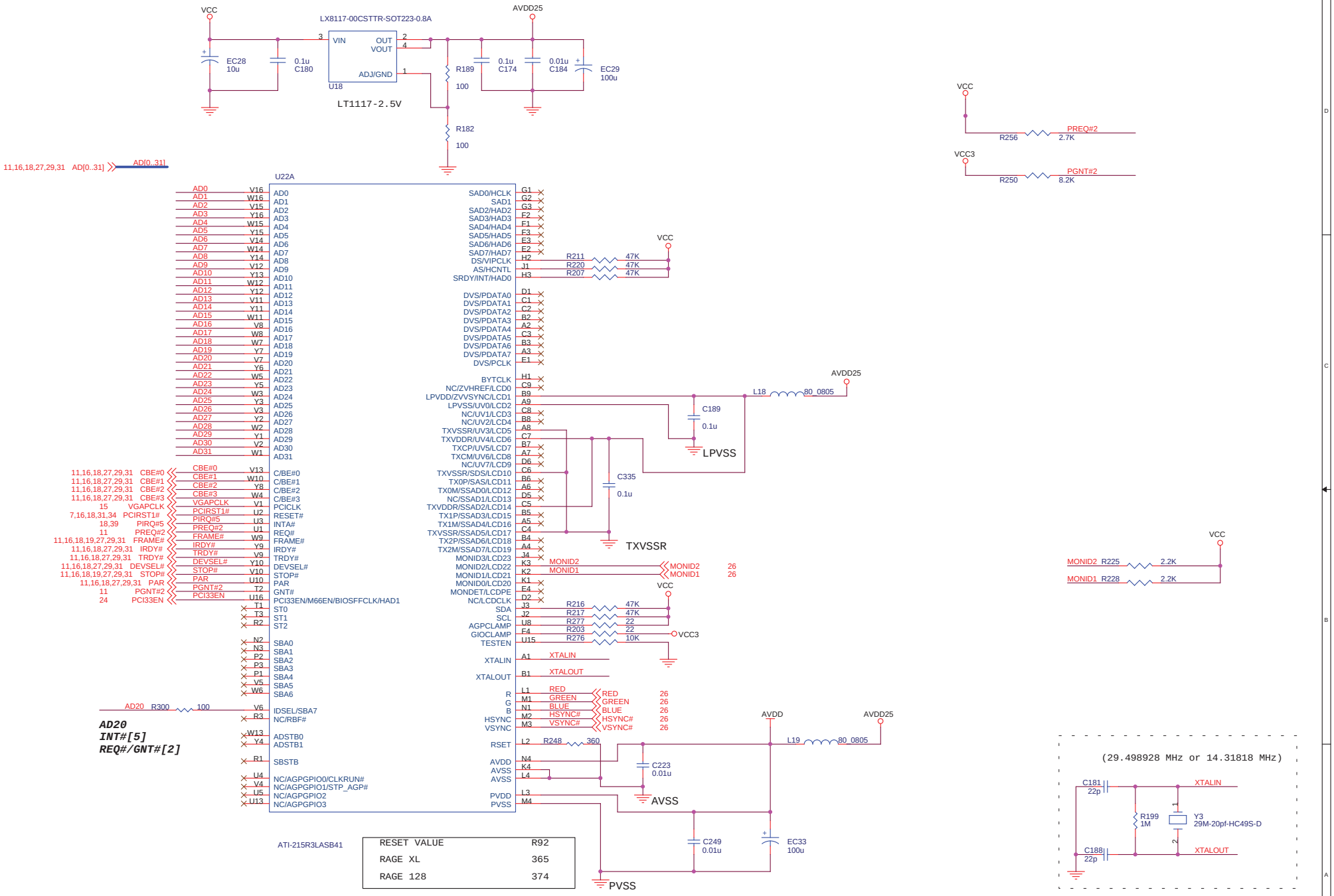
Title	ATA 66 IDE Connectors	Rev 100
Document Number		
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Tuesday, September 10, 2002
		Sheet 22 of 50


VCC
LX8117-00CSTTR-SOT223-0.8A
AVDD25
EC28 10u
0.1u C180
VIN
OUT
VOUT
ADJ/GND
U18
LT1117-2.5V
R189 100
0.1u C174
0.01u C184
EC29 100u
R182 100
11,16,18,27,29,31 AD[0..31]
AD[0..31]
U22A
AD0 V16
AD1 W16
AD2 V15
AD3 Y16
AD4 W15
AD5 Y15
AD6 V14
AD7 W14
AD8 Y14
AD9 V12
AD10 Y13
AD11 W12
AD12 Y12
AD13 V11
AD14 Y11
AD15 W11
AD16 V8
AD17 W8
AD18 W7
AD19 Y7
AD20 V7
AD21 Y6
AD22 W5
AD23 Y5
AD24 W3
AD25 Y3
AD26 V3
AD27 Y2
AD28 W2
AD29 Y1
AD30 V2
AD31 W1
CBE#0 V13
CBE#1 W10
CBE#2 Y8
CBE#3 W4
VGAPCLK V1
PCIRST1# U2
PIRQ#5 U3
PREQ#2 U1
FRAME# W9
IRDY# Y9
TRDY# V9
DEVSEL# Y10
STOP# V10
PAR U10
PGNT#2 T2
PCI33EN U16
T1
T3
R2
N2
N3
P2
P3
P1
V5
W6
V6
R3
W13
Y4
R1
U4
V4
U5
U13
C/BE#0
C/BE#1
C/BE#2
C/BE#3
PCICLK
RESET#
INTA#
REQ#
FRAME#
IRDY#
TRDY#
DEVSEL#
STOP#
PAR
GNT#
PCI33EN/M66EN/BIOSFFCLK/HAD1
ST0
ST1
ST2
SBA0
SBA1
SBA2
SBA3
SBA4
SBA5
SBA6
IDSEL/SBA7
NC/RBF#
ADSTB0
ADSTB1
SBSTB
NC/AGPGPIO0/CLKRUN#
NC/AGPGPIO1/STP_AGP#
NC/AGPGPIO2
NC/AGPGPIO3
SAD0/HCLK G1
SAD1 G2
SAD2/HAD2 G3
SAD3/HAD3 F2
SAD4/HAD4 F1
SAD5/HAD5 F3
SAD6/HAD6 F5
SAD7/HAD7 E2
DS/VIPCLK H2
AS/HCNTL J1
SRDY/INT/HAD0 H3
DVS/PDATA0 D1
DVS/PDATA1 C1
DVS/PDATA2 C2
DVS/PDATA3 B2
DVS/PDATA4 A2
DVS/PDATA5 C3
DVS/PDATA6 B3
DVS/PDATA7 A3
DVS/PCLK E1
BYTCLK H1
NC/ZVHREF/LCD0 C9
LPVDD/ZVVSYNC/LCD1 B9
LPVSS/UV0/LCD2 A9
NC/UV1/LCD3 C8
NC/UV2/LCD4 B8
TXVSSR/UV3/LCD5 A8
TXVDDR/UV4/LCD6 C7
TXCP/UV5/LCD7 B7
TXCM/UV6/LCD8 A7
NC/UV7/LCD9 D6
TXVSSR/SDS/LCD10 C6
TX0P/SAS/LCD11 B6
TX0M/SSAD0/LCD12 A6
NC/SSAD1/LCD13 D5
TXVDDR/SSAD2/LCD14 C5
TX1P/SSAD3/LCD15 B5
TX1M/SSAD4/LCD16 A5
TXVSSR/SSAD5/LCD17 C4
TX2P/SSAD6/LCD18 B4
TX2M/SSAD7/LCD19 A4
MONID3/LCD23 J4
MONID2/LCD22 K3
MONID1/LCD21 K2
MONID0/LCD20 K1
MONDET/LCDPE E4
NC/LCDCLK D2
SDA J3
SCL J2
AGPCLAMP U8
GIOCLAMP F4
TESTEN U15
XTALIN A1
XTALOUT B1
R L1
G M1
B N1
HSYNC M2
VSYNC M3
RSET L2
AVDD N4
AVSS K4
AVSS L4
PVDD L3
PVSS M4
R211 47K
R220 47K
R207 47K
R216 47K
R217 47K
R277 22
R203 22
R276 10K
R248 360
C189 0.1u
C335 0.1u
C223 0.01u
C249 0.01u
EC33 100u
L18 80_0805
L19 80_0805
LPVSS
TXVSSR
AVSS
PVSS
AVDD
AVDD25
VCC3
MONID2 26
MONID1 26
RED 26
GREEN 26
BLUE 26
HSYNC# 26
VSYNC# 26
AD20 R300 100
AD20
INT#[5]
REQ#/GNT#[2]
VCC
R256 PREQ#2 2.7K
VCC3
R250 PGNT#2 8.2K
MONID2 R225 2.2K
MONID1 R228 2.2K
(29.498928 MHz or 14.31818 MHz)
C181 22p
C188 22p
R199 1M
Y3 29M-20pf-HC49S-D
XTALIN
XTALOUT
ATI-215R3LASB41
RESET VALUE R92
RAGE XL 365
RAGE 128 374
Micro Star Restricted Secret
Title ATI Rage XL 1/4
Rev 100
Document Number
MICRO-STAR INT'L CO.,LTD.
No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan
http://www.msi.com.tw
Last Revision Date: Tuesday, September 10, 2002
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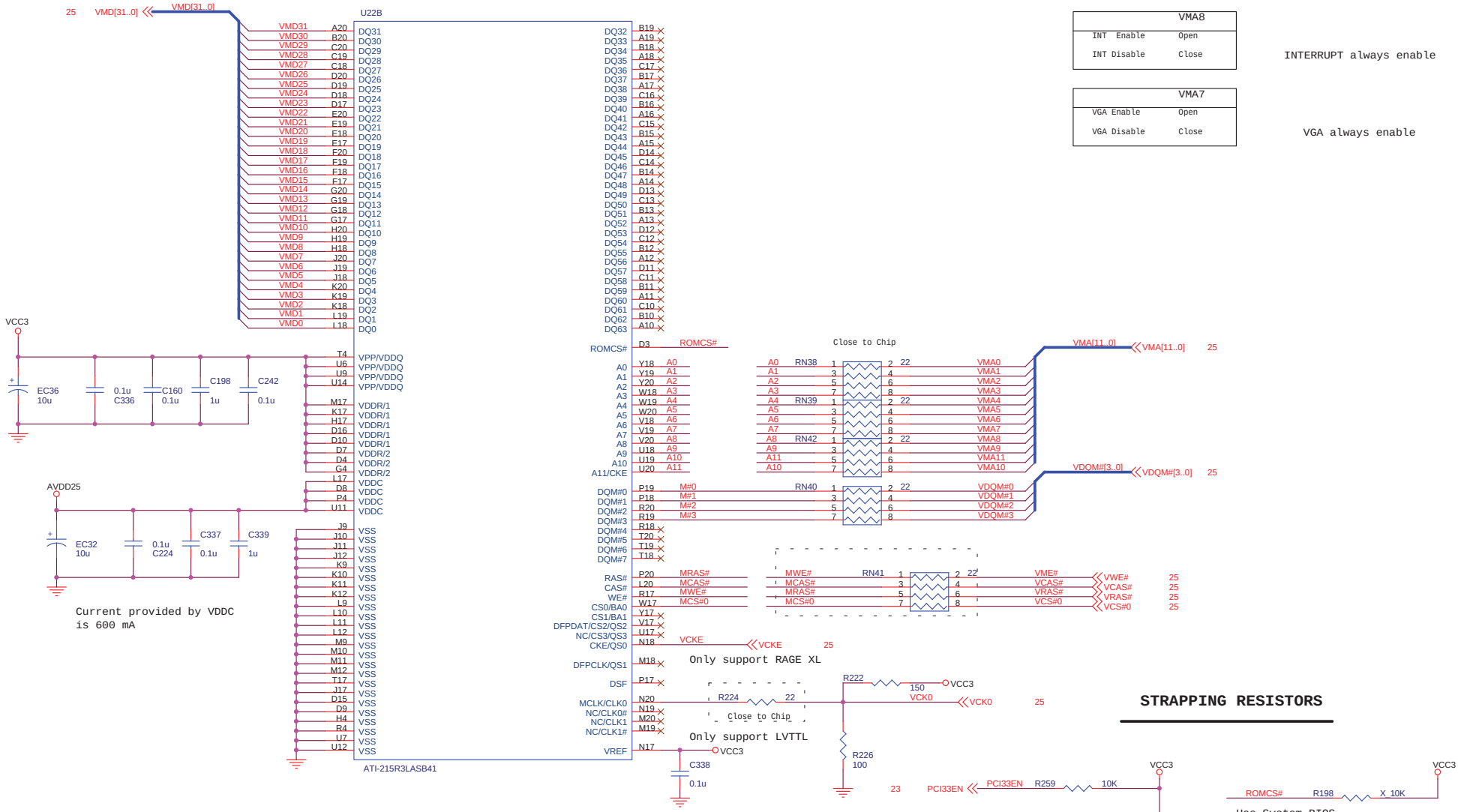

VMA8	
INT Enable	Open
INT Disable	Close

INTERRUPT always enable

VMA7	
VGA Enable	Open
VGA Disable	Close

VGA always enable

	VMA0 Bus Clock Select	VMA6 Bus Type	PCI33EN
PCI 33MHz / 3.3V	1	0	1
PCI 33MHz / 5V	1	1	1
PCI 66MHz	0	1	0
AGP 1/2X	0	0	0
AGP Test Mode	1	Don't care	0

Read BIOS straps	Close
Don't Read BIOS	Open

VMA5	
IDSEL Enable	Open
IDSEL Disable	Close

VDDR	I/O power for Memory & muitimedia
VDDP	Power for PCI or AGP Interface
VDDC	Graphic controllor power
AVDD	Analog DAC Power - 2.5 V
PVDD	Phase Lock Loop Power - 2.5 V

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Title	ATI Rage XL 2/4
Document Number	100
Rev	
MICRO-STAR INT'L CO.,LTD.	Last Revision Date: Tuesday, September 10, 2002
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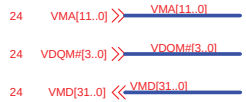
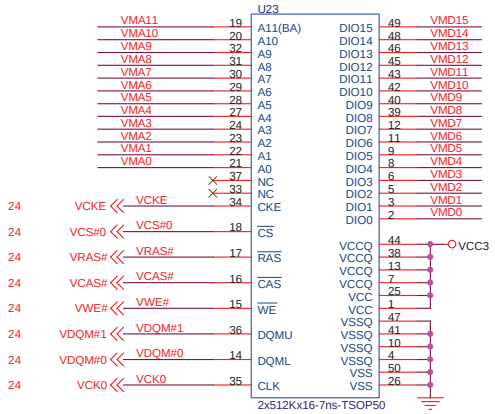
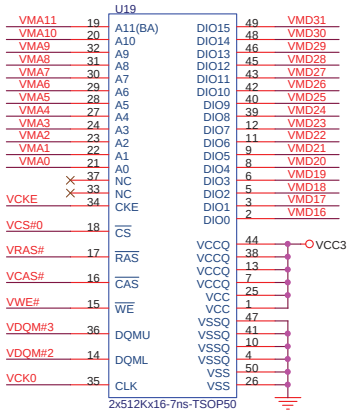
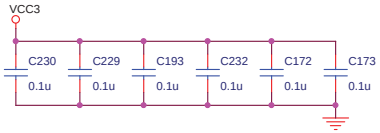
4MBytes SDRAM 16Mbit 512Kx16x2









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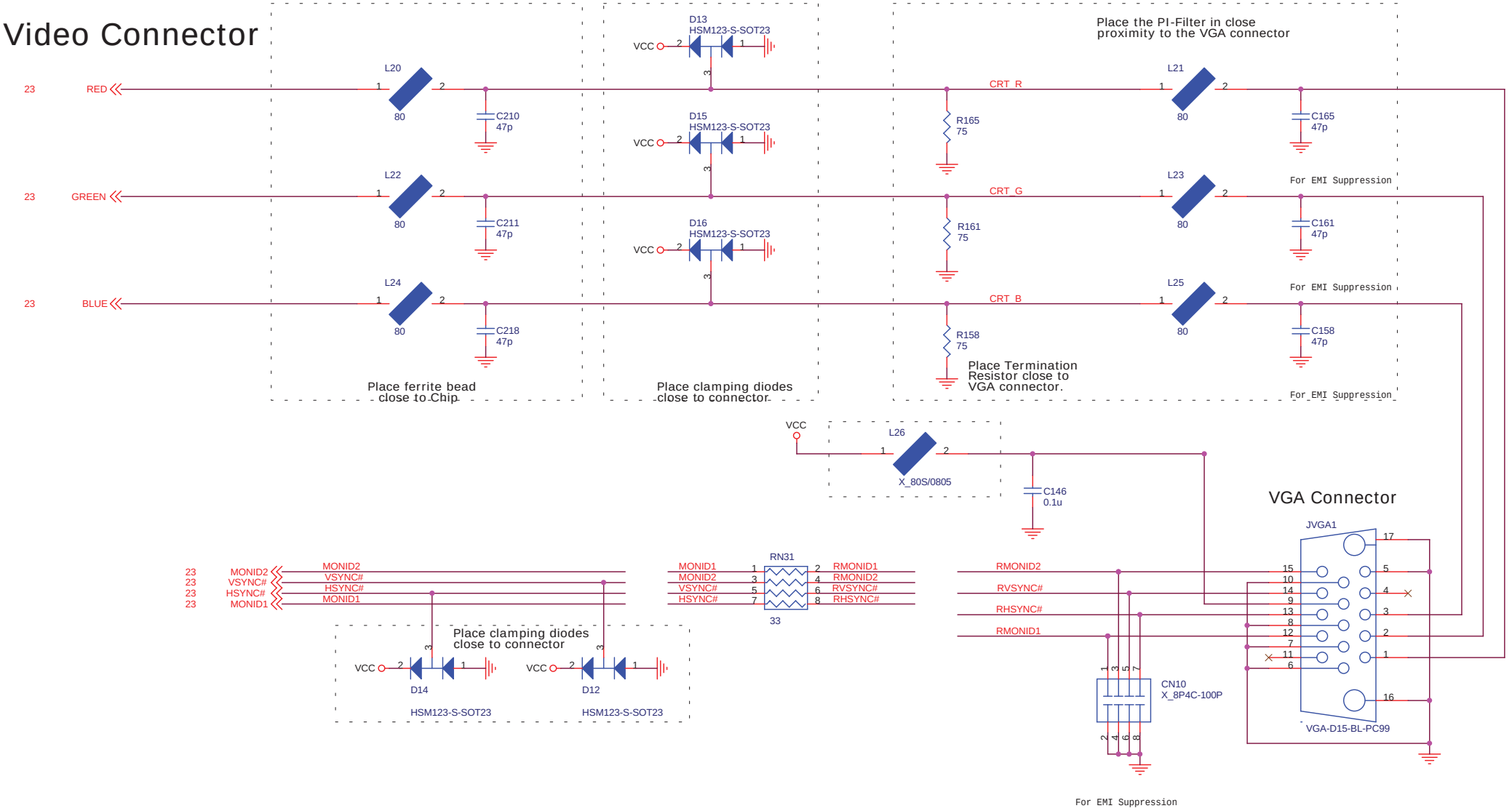
Title: ATI Rage XL 3/4	Rev: 100
Document Number	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, September 10, 2002 Sheet 25 of 50

Video Connector



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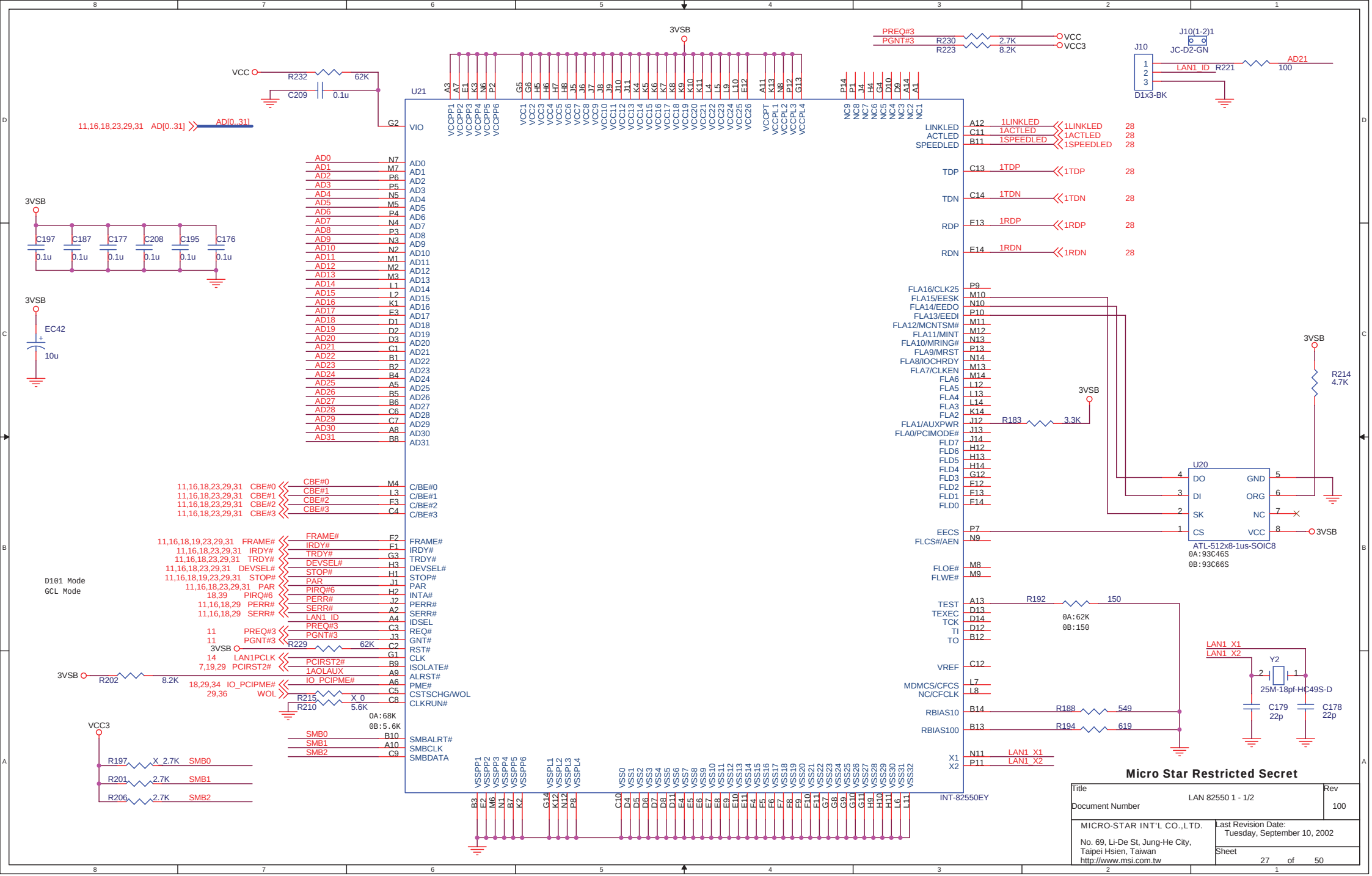
Title	ATI Rage XL /44	Rev 100
Document Number		
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Tuesday, September 10, 2002 Sheet 26 of 50


U21
INT-82550EY
VIO
AD[0..31]
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
AD16
AD17
AD18
AD19
AD20
AD21
AD22
AD23
AD24
AD25
AD26
AD27
AD28
AD29
AD30
AD31
CBE#0
CBE#1
CBE#2
CBE#3
C/BE#0
C/BE#1
C/BE#2
C/BE#3
FRAME#
IRDY#
TRDY#
DEVSEL#
STOP#
PAR
INTA#
PERR#
SERR#
IDSEL
REQ#
GNT#
RST#
CLK
ISOLATE#
ALRST#
PME#
CSTSCHG/WOL
CLKRUN#
SMBALRT#
SMBCLK
SMBDATA
LINKLED
ACTLED
SPEEDLED
TDP
TDN
RDP
RDN
FLA16/CLK25
FLA15/EESK
FLA14/EEDO
FLA13/EEDI
FLA12/MCNTSM#
FLA11/MINT
FLA10/MRING#
FLA9/MRST
FLA8/IOCHRDY
FLA7/CLKEN
FLA6
FLA5
FLA4
FLA3
FLA2
FLA1/AUXPWR
FLA0/PCIMODE#
FLD7
FLD6
FLD5
FLD4
FLD3
FLD2
FLD1
FLD0
EECS
FLCS#/AEN
FLOE#
FLWE#
TEST
TEXEC
TCK
TI
TO
VREF
MDMCS/CFCS
NC/CFCLK
RBIAS10
RBIAS100
X1
X2
3VSB
VCC
VCC3
R232 62K
C209 0.1u
C197 C187 C177 C208 C195 C176 0.1u
EC42 10u
R229 62K
R202 8.2K
R215 X_0
R210 5.6K
0A:68K
0B:5.6K
R197 X_2.7K SMB0
R201 2.7K SMB1
R206 2.7K SMB2
PREQ#3
PGNT#3
R230 2.7K
R223 8.2K
J10(1-2)1
J10
JC-D2-GN
D1x3-BK
LAN1_ID R221 100
AD21
R183 3.3K
R214 4.7K
U20
DO
DI
SK
CS
GND
ORG
NC
VCC
ATL-512x8-1us-SOIC8
0A:93C46S
0B:93C66S
R192 150
0A:62K
0B:150
R188 549
R194 619
LAN1_X1
LAN1_X2
Y2
25M-18pf-HC49S-D
C179 22p
C178 22p
D101 Mode
GCL Mode
LAN1PCLK
PCIRST2#
1AOLAUX
IO_PCIPME#
WOL
Micro Star Restricted Secret
Title
LAN 82550 1 - 1/2
Document Number
100
Rev
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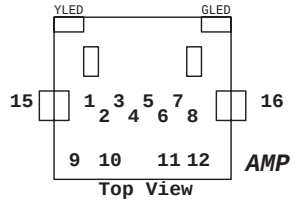
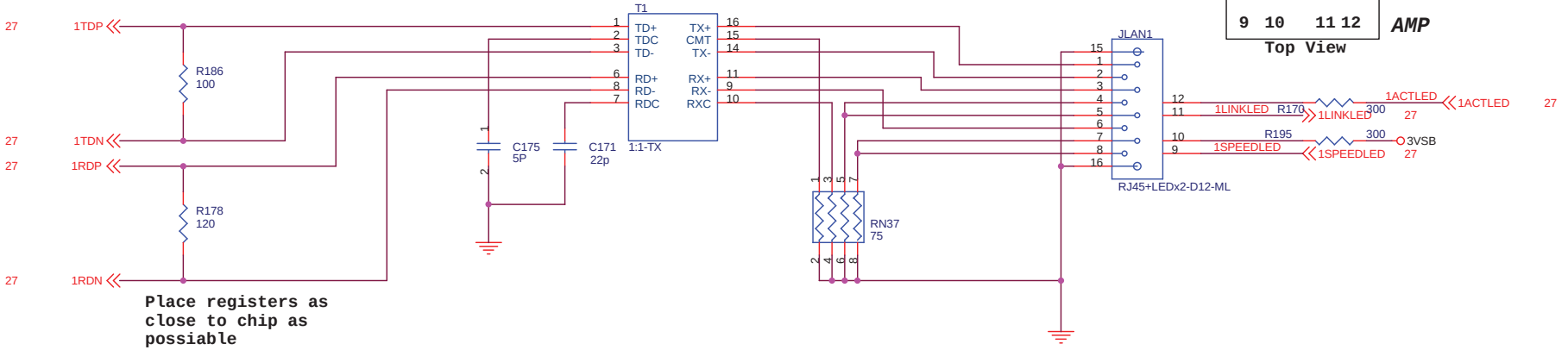
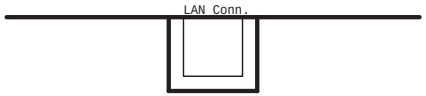
FLOAT PLANE(CONNECT TO
CHASSIS GROUND BY 1500P CAP)



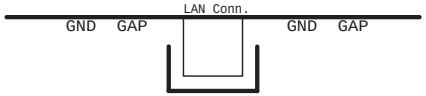


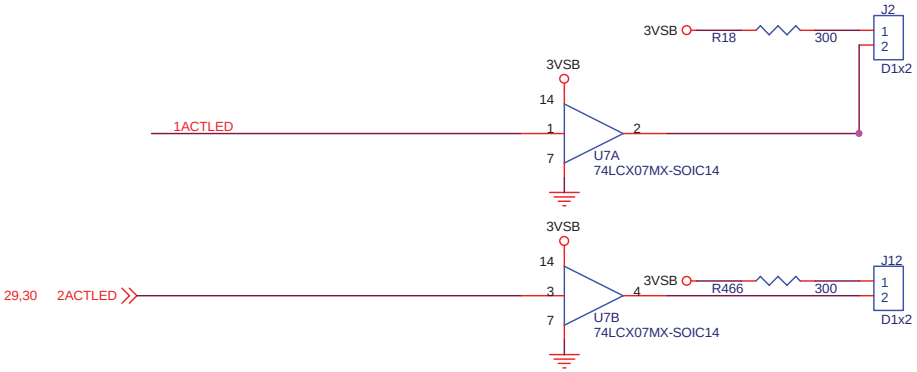
Place registers as close to chip as possiable

Component Side



Gnd





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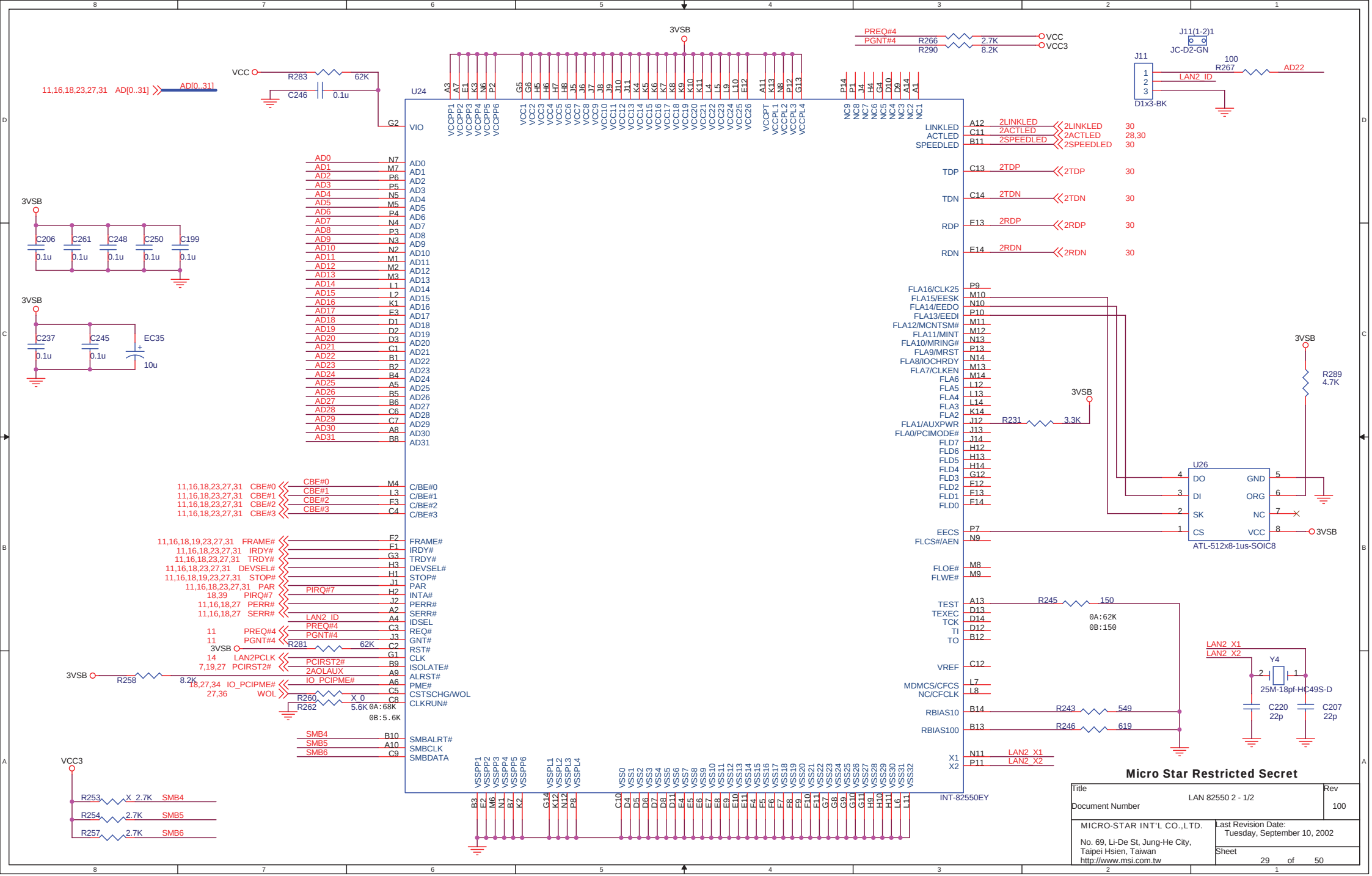
U24
INT-82550EY
3VSB
VCC
VCC3
AD[0..31]
11,16,18,23,27,31 AD[0..31]
R283 62K
C246 0.1u
PREQ#4
PGNT#4
R266 2.7K
R290 8.2K
J11(1-2)1
JC-D2-GN
J11
R267 100
AD22
LAN2_ID
D1x3-BK
LINKLED
ACTLED
SPEEDLED
2LINKLED
2ACTLED
2SPEEDLED
TDP
TDN
RDP
RDN
2TDP
2TDN
2RDP
2RDN
C206 0.1u
C261 0.1u
C248 0.1u
C250 0.1u
C199 0.1u
C237 0.1u
C245 0.1u
EC35 10u
FLA16/CLK25
FLA15/EESK
FLA14/EEDO
FLA13/EEDI
FLA12/MCNTSM#
FLA11/MINT
FLA10/MRING#
FLA9/MRST
FLA8/IOCHRDY
FLA7/CLKEN
FLA6
FLA5
FLA4
FLA3
FLA2
FLA1/AUXPWR
FLA0/PCIMODE#
FLD7
FLD6
FLD5
FLD4
FLD3
FLD2
FLD1
FLD0
R231 3.3K
R289 4.7K
U26
DO
DI
SK
CS
GND
ORG
NC
VCC
ATL-512x8-1us-SOIC8
EECS
FLCS#/AEN
FLOE#
FLWE#
TEST
TEXEC
TCK
TI
TO
VREF
MDMCS/CFCS
NC/CFCLK
RBIAS10
RBIAS100
R245 150
0A:62K
0B:150
R243 549
R246 619
X1
X2
LAN2_X1
LAN2_X2
Y4
25M-18pf-HC49S-D
C220 22p
C207 22p
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
AD16
AD17
AD18
AD19
AD20
AD21
AD22
AD23
AD24
AD25
AD26
AD27
AD28
AD29
AD30
AD31
CBE#0
CBE#1
CBE#2
CBE#3
11,16,18,23,27,31 CBE#0
11,16,18,23,27,31 CBE#1
11,16,18,23,27,31 CBE#2
11,16,18,23,27,31 CBE#3
11,16,18,19,23,27,31 FRAME#
11,16,18,23,27,31 IRDY#
11,16,18,23,27,31 TRDY#
11,16,18,23,27,31 DEVSEL#
11,16,18,19,23,27,31 STOP#
11,16,18,23,27,31 PAR
18,39 PIRQ#7
11,16,18,27 PERR#
11,16,18,27 SERR#
PIRQ#7
LAN2_ID
PREQ#4
PGNT#4
11 PREQ#4
11 PGNT#4
R281 62K
3VSB
14 LAN2PCLK
7,19,27 PCIRST2#
PCIRST2#
2AOLAUX
18,27,34 IO_PCIPME#
27,36 WOL
IO_PCIPME#
R258 8.2K
R260 X_0
R262 5.6K
0A:68K
0B:5.6K
SMB4
SMB5
SMB6
R253 X_2.7K
R254 2.7K
R257 2.7K
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Title
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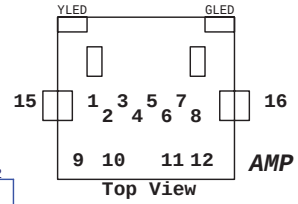
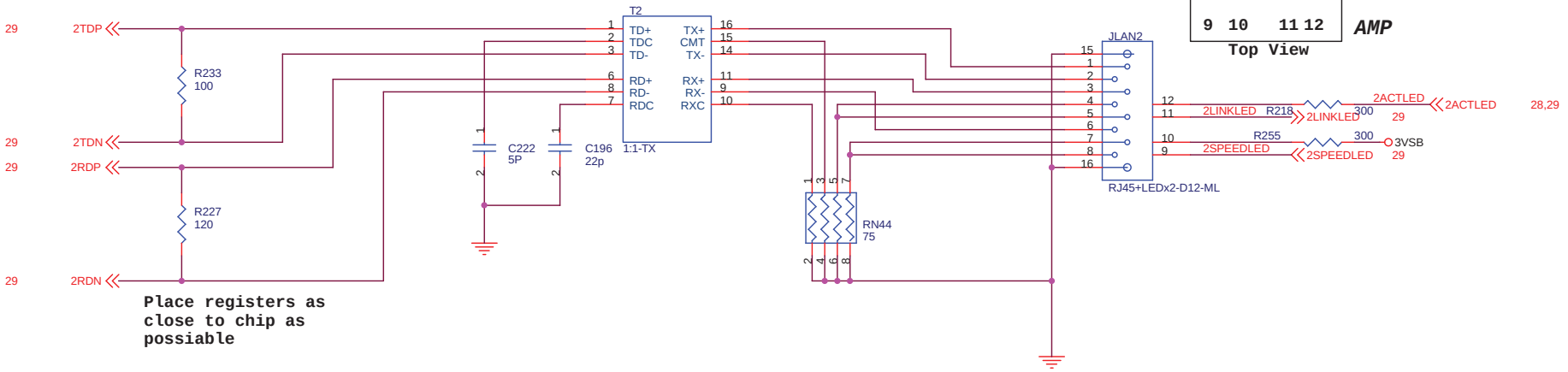
FLOAT PLANE(CONNECT TO
CHASSIS GROUND BY 1500P CAP)





Place registers as close to chip as possiable

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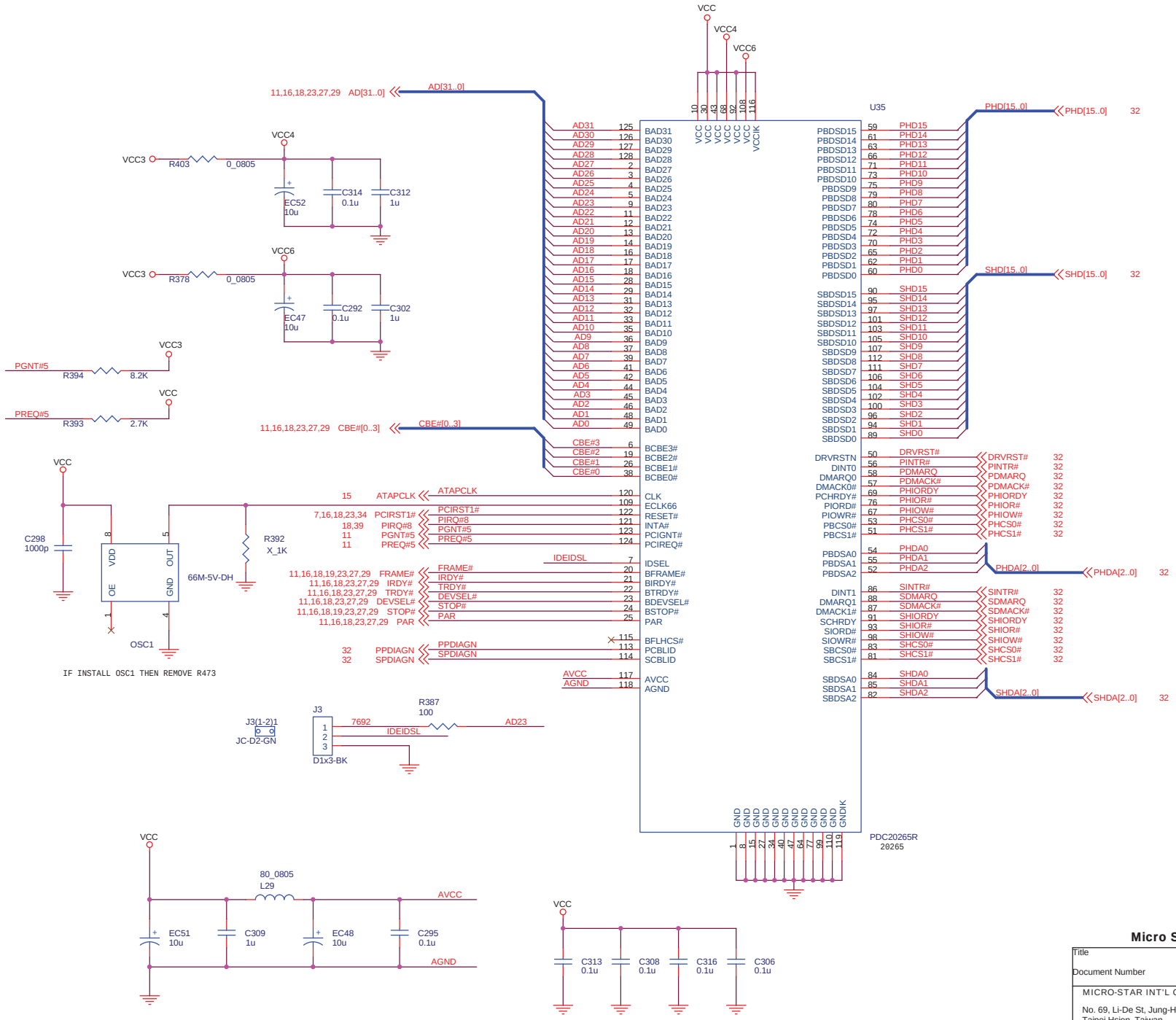
VCC
VCC4
VCC6
11,16,18,23,27,29 AD[31..0]
AD[31..0]
U35
PHD[15..0]
SHD[15..0]
VCC3
R403 0_0805
EC52 10u
C314 0.1u
C312 1u
R378 0_0805
EC47 10u
C292 0.1u
C302 1u
PGNT#5
R394 8.2K
PREQ#5
R393 2.7K
11,16,18,23,27,29 CBE#[0..3]
CBE#[0..3]
C298 1000p
R392 X_1K
66M-5V-DH
OSC1
IF INSTALL OSC1 THEN REMOVE R473
J3
J3(1-2)1
JC-D2-GN
D1x3-BK
R387 100
7692
IDEIDSL
AD23
80_0805
L29
EC51 10u
C309 1u
EC48 10u
C295 0.1u
AVCC
AGND
C313 0.1u
C308 0.1u
C316 0.1u
C306 0.1u
PDC20265R
20265
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Primose IDE 1/2
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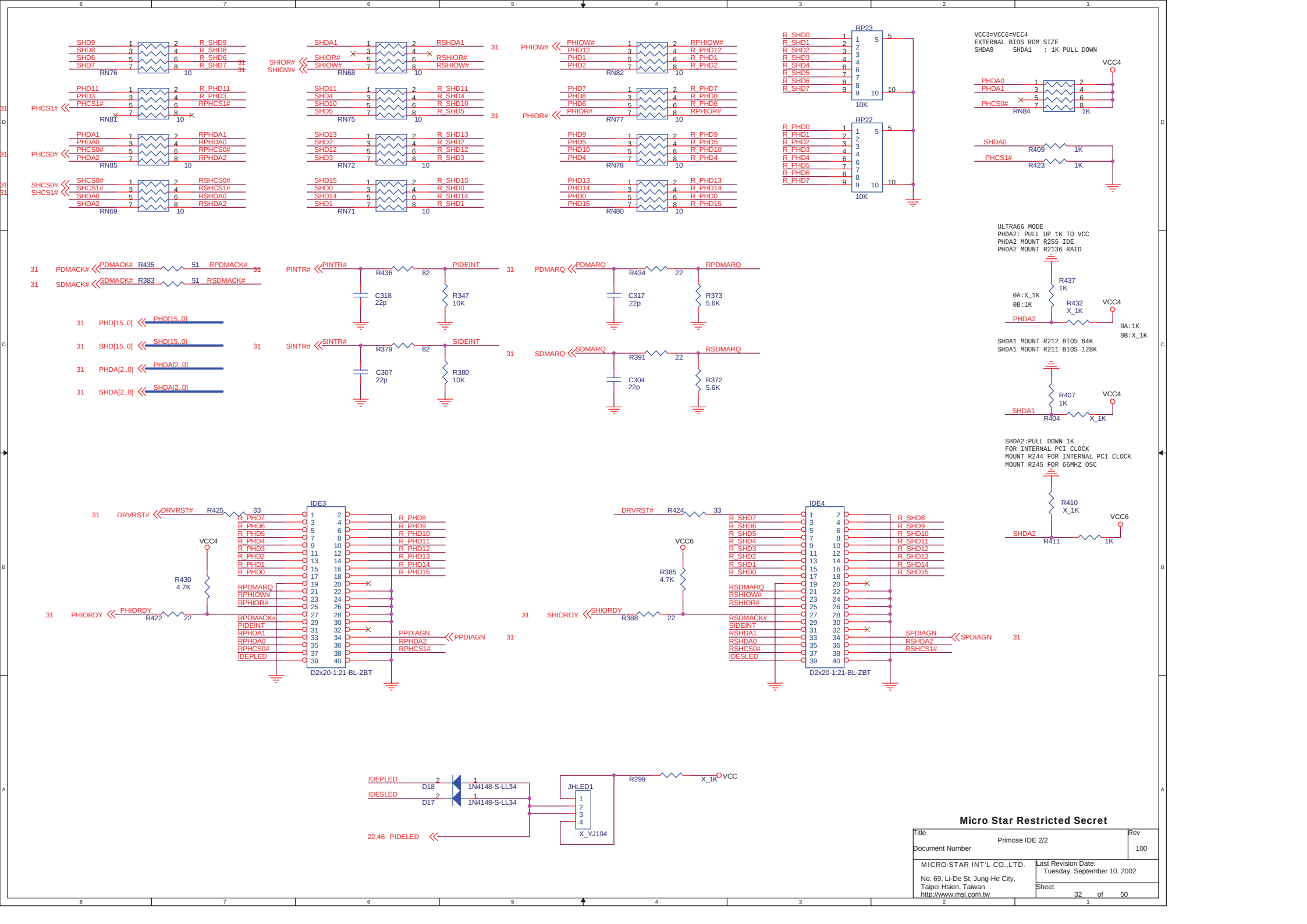

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Title: Primose IDE 2/2	Rev: 100
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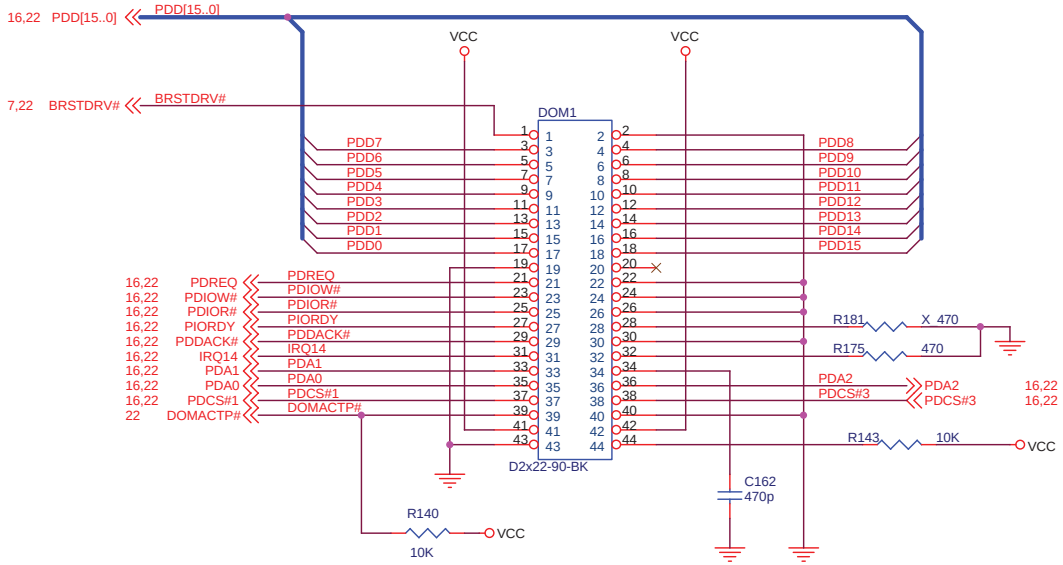
Disk On Module

Share with Primary IDE



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Title: Disk On Module	Rev: 100
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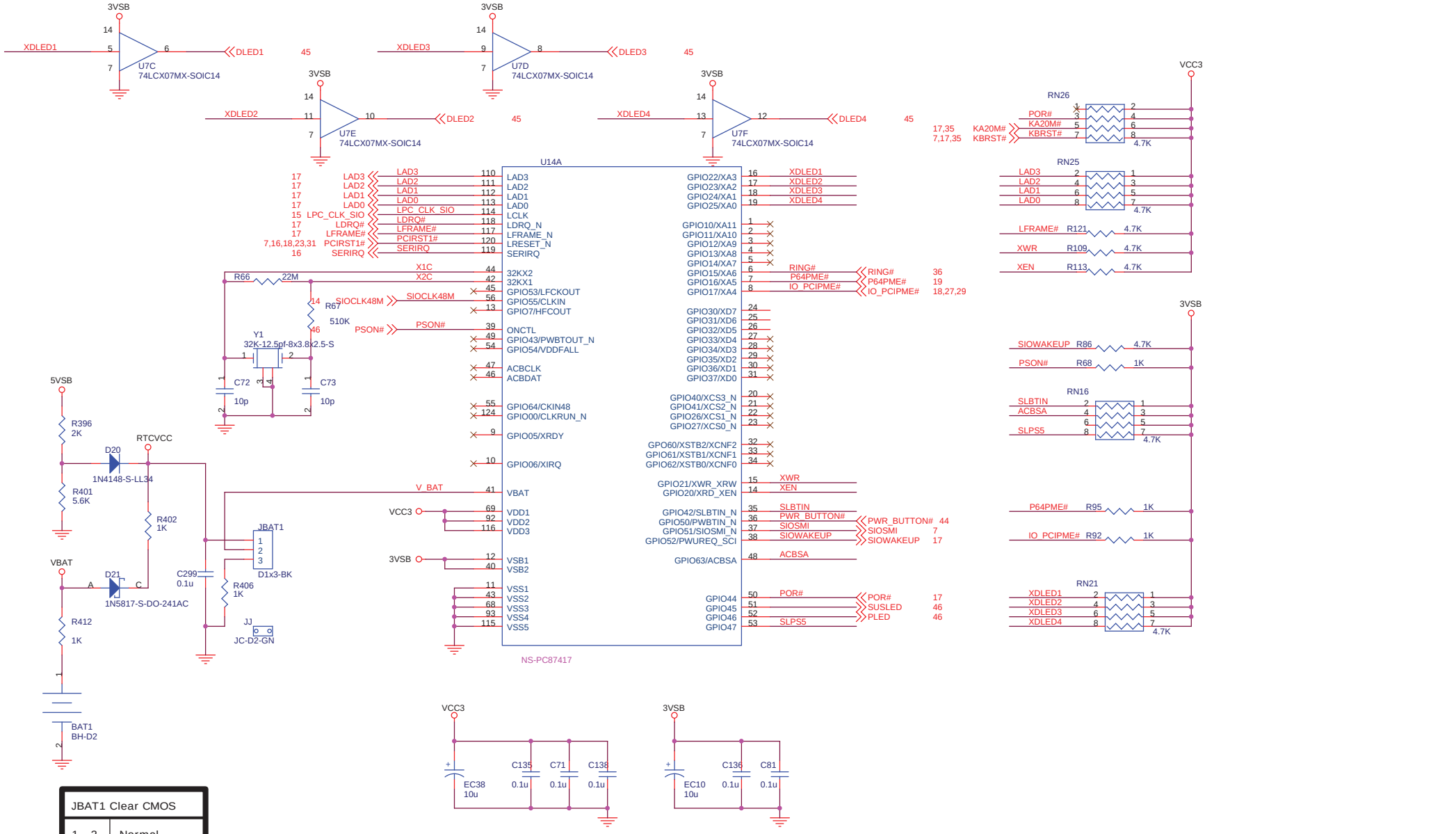
U7C 74LCX07MX-SOIC14
U7D 74LCX07MX-SOIC14
U7E 74LCX07MX-SOIC14
U7F 74LCX07MX-SOIC14
U14A
NS-PC87417
RN26
RN25
RN16
RN21
JBAT1 Clear CMOS
1 - 2 Normal
2 - 3 Clear CMOS
Micro Star Restricted Secret
NS PC97317 IO
MICRO-STAR INT'L CO.,LTD.
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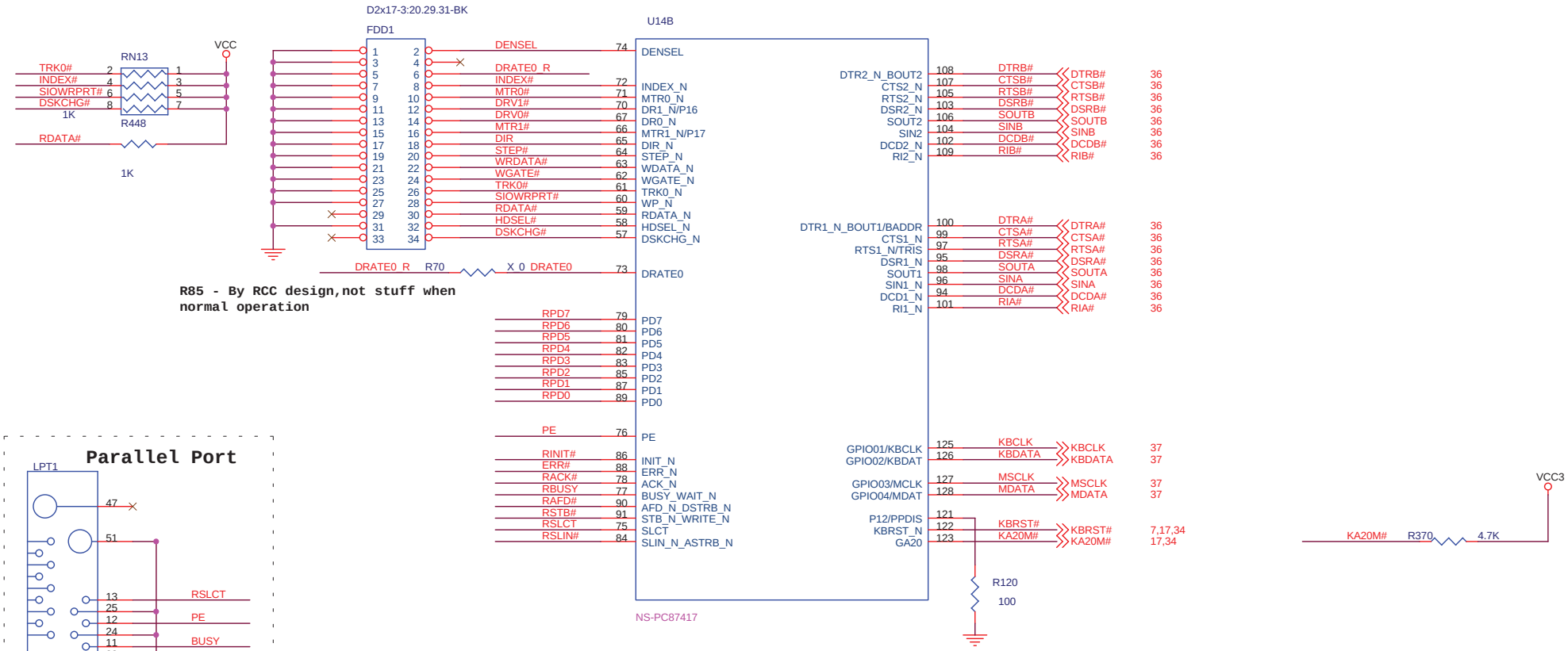
D2x17-3:20.29.31-BK
FDD1
U14B
RN13
VCC
TRK0#
INDEX#
SIOWRPRT#
DSKCHG#
1K
R448
RDATA#
1K
DENSEL
DRATE0_R
INDEX#
MTR0#
DRV1#
DRV0#
MTR1#
DIR
STEP#
WRDATA#
WGATE#
TRK0#
SIOWRPRT#
RDATA#
HDSEL#
DSKCHG#
DRATE0_R
R70
X_0_DRATE0
R85 - By RCC design,not stuff when
normal operation
INDEX_N
MTR0_N
DR1_N/P16
DR0_N
MTR1_N/P17
DIR_N
STEP_N
WDATA_N
WGATE_N
TRK0_N
WP_N
RDATA_N
HDSEL_N
DSKCHG_N
DRATE0
RPD7
RPD6
RPD5
RPD4
RPD3
RPD2
RPD1
RPD0
PD7
PD6
PD5
PD4
PD3
PD2
PD1
PD0
PE
RINIT#
ERR#
RACK#
RBUSY
RAFD#
RSTB#
RSLCT
RSLIN#
INIT_N
ERR_N
ACK_N
BUSY_WAIT_N
AFD_N_DSTRB_N
STB_N_WRITE_N
SLCT
SLIN_N_ASTRB_N
DTR2_N_BOUT2
CTS2_N
RTS2_N
DSR2_N
SOUT2
SIN2
DCD2_N
RI2_N
DTRB#
CTSB#
RTSB#
DSRB#
SOUTB
SINB
DCDB#
RIB#
DTR1_N_BOUT1/BADDR
CTS1_N
RTS1_N/TRIS
DSR1_N
SOUT1
SIN1_N
DCD1_N
RI1_N
DTRA#
CTSA#
RTSA#
DSRA#
SOUTA
SINA
DCDA#
RIA#
GPIO01/KBCLK
GPIO02/KBDAT
GPIO03/MCLK
GPIO04/MDAT
P12/PPDIS
KBRST_N
GA20
KBCLK
KBDATA
MSCLK
MDATA
KBRST#
KA20M#
R120
100
NS-PC87417
VCC3
KA20M#
R370
4.7K
Parallel Port
LPT1
LPT-D25-BR-BI
RSLCT
PE
BUSY
ACK#
PD7
PD6
PD5
PD4
PD3
SLIN#
PD2
RINIT#
PD1
ERR#
PD0
AFD#
STB#
RN18
RN22
RN27
33
ACK#
R59
RACK#
C63
180p
CN7
CN5
CN6
RN17
RN20
RN24
4.7K
RSLIN#
R122
Micro Star Restricted Secret
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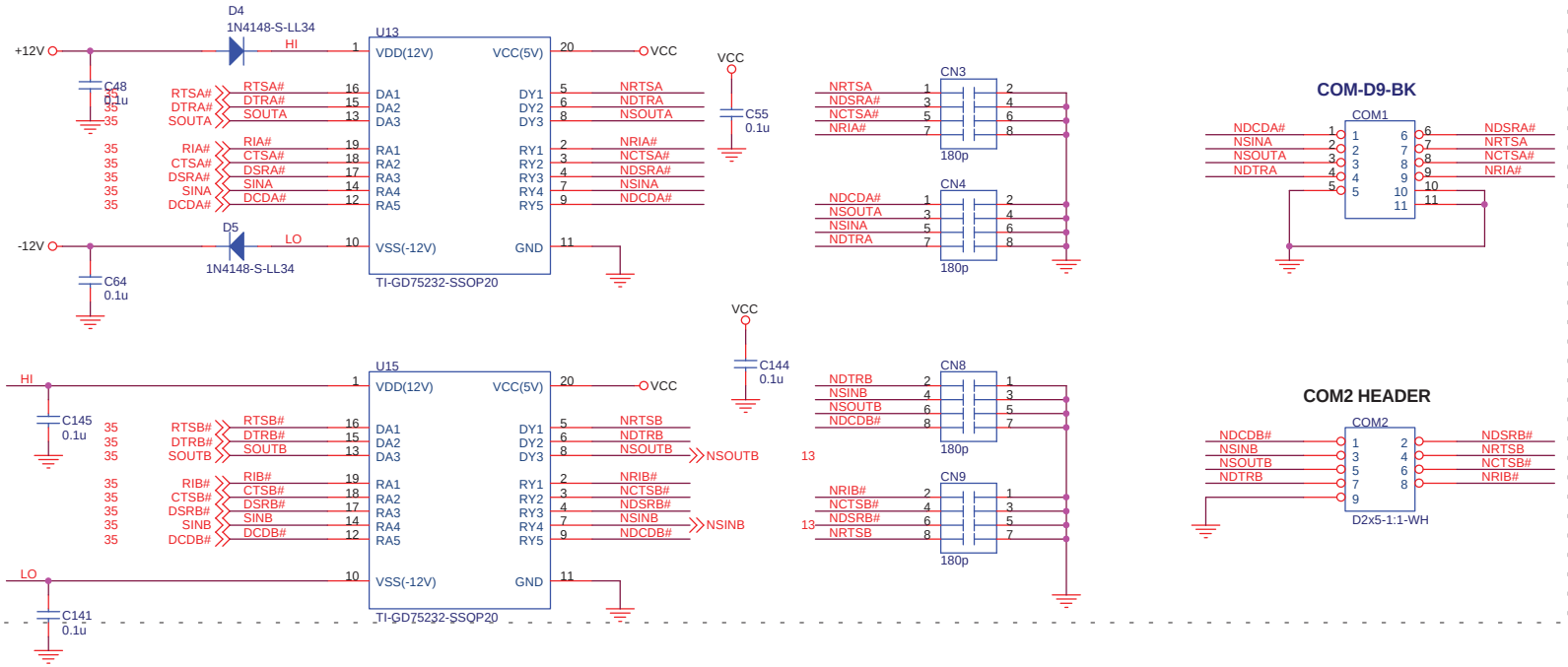
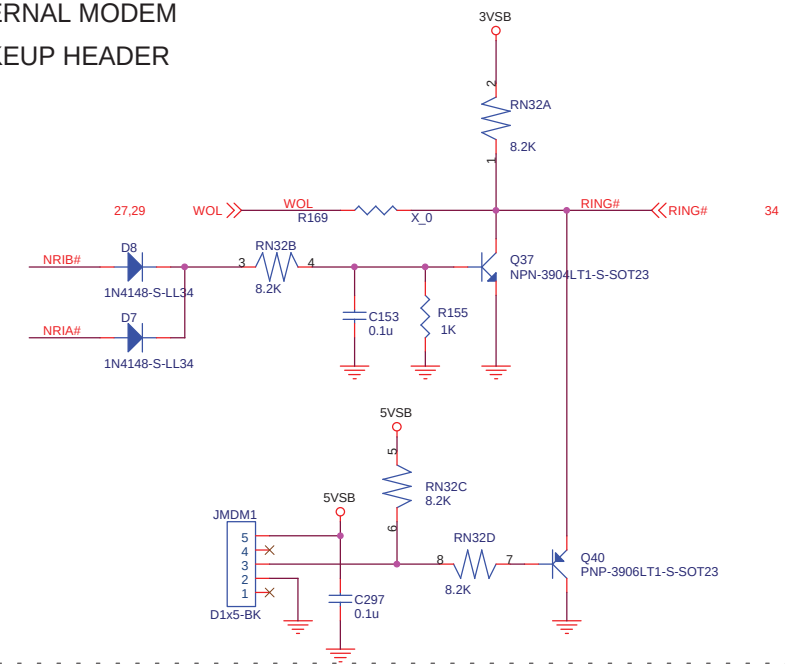
Serial Port



INTERNAL MODEM

WAKEUP HEADER



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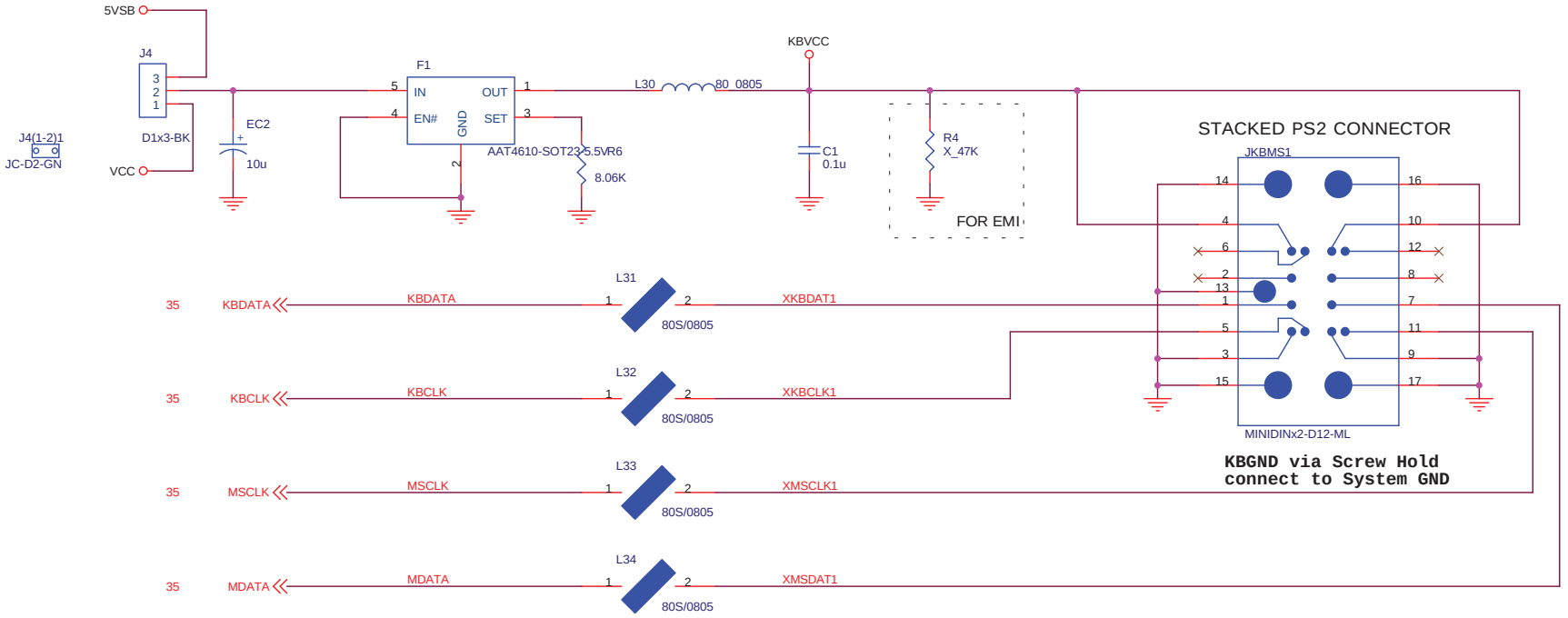
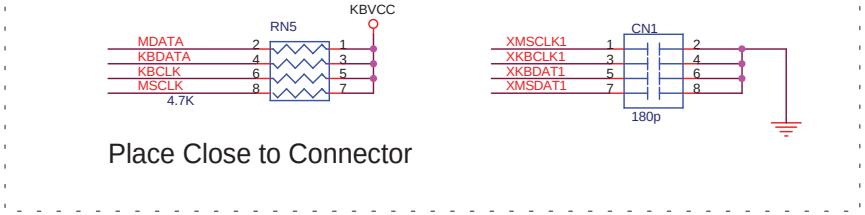
Keyboard/Mouse Ports





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Title: Keyboard/Mouse Ports	Rev: 100
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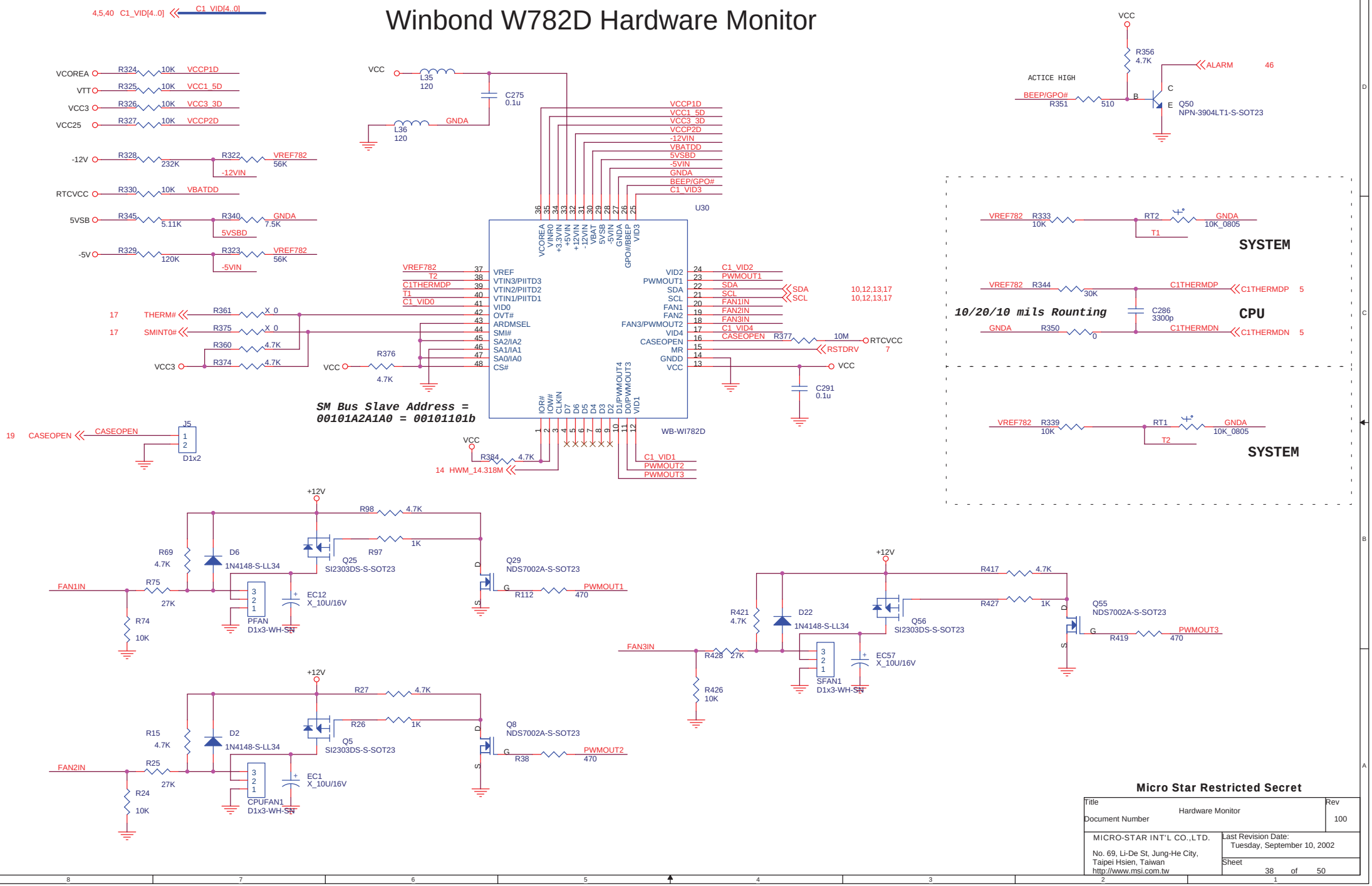
Winbond W782D Hardware Monitor



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Title	Hardware Monitor	Rev 100
Document Number		
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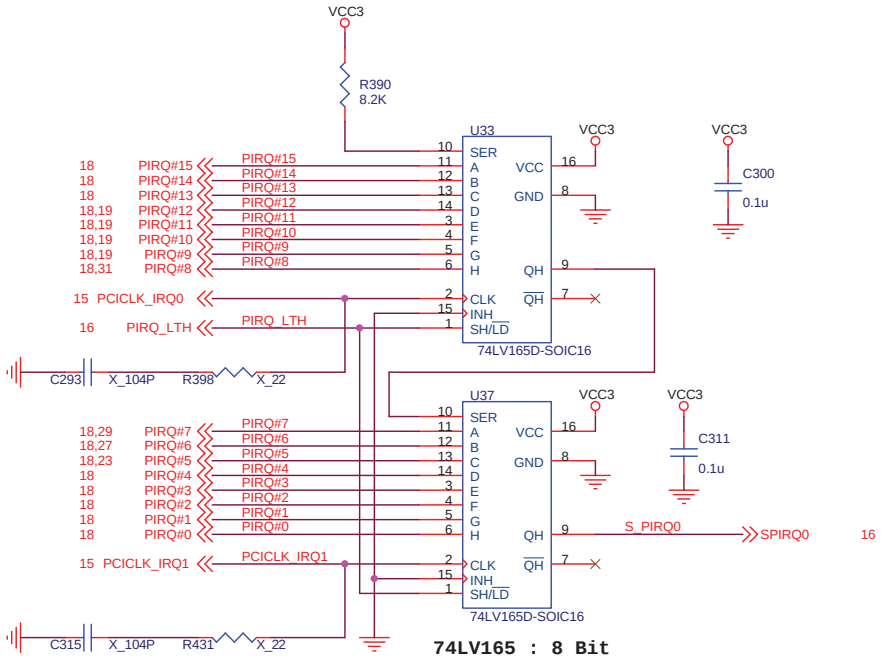

74LV165 : 8 Bit parallel-in/Serial-out shift register

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Title: Interrupt Mapping Ckt	Rev: 100
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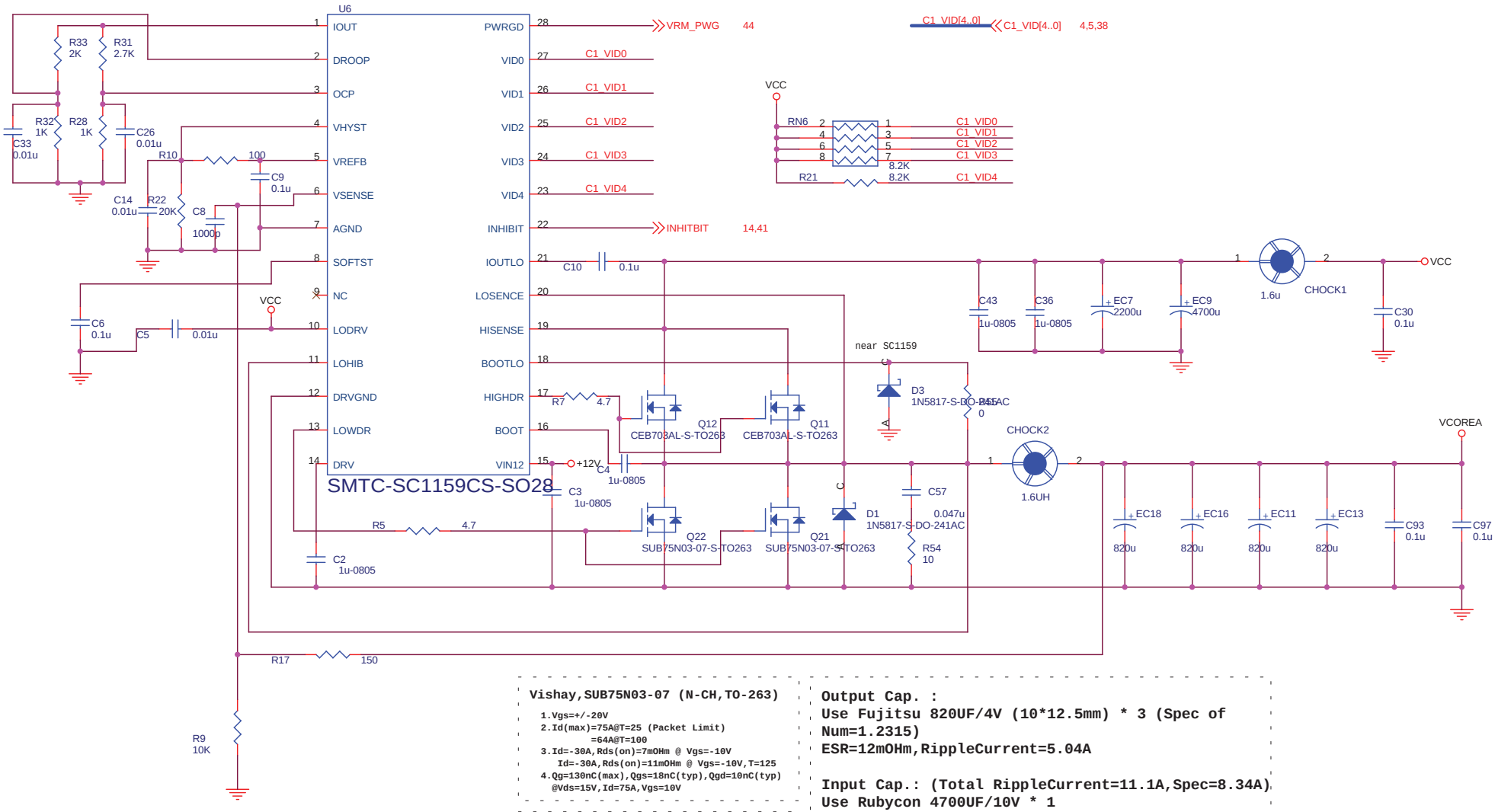

Vishay,SUB75N03-07 (N-CH,TO-263)

1. Vgs=+/-20V
2. Id(max)=75A@T=25 (Packet Limit)
   =64A@T=100
3. Id=-30A,Rds(on)=7mOHm @ Vgs=-10V
   Id=-30A,Rds(on)=11mOHm @ Vgs=-10V,T=125
4. Qg=130nC(max),Qgs=18nC(typ),Qgd=10nC(typ)
   @Vds=15V,Id=75A,Vgs=10V

CET,CEB703AL (N-CH,TO-263)

1. Vgs=+/-20V
2. Id(max)=40A@T=125-Pulse
3. Id=-25A,Rds(on)=17mOHm @ Vgs=-10V
   Id=-10A,Rds(on)=30mOHm @ Vgs=-4.5
4. Qg=50nC(max),Qgs=6nC(typ),Qgd=7nC(typ)
   @Vds=10V,Id=25A,Vgs=10V

Output Cap. :
Use Fujitsu 820UF/4V (10*12.5mm) * 3 (Spec of Num=1.2315)
ESR=12mOHm,RippleCurrent=5.04A

Input Cap.: (Total RippleCurrent=11.1A,Spec=8.34A)
Use Rubycon 4700UF/10V * 1
ESR=15mOHm,RippleCurrent=3.4A (25mm)
Use Lelon 1500UF/10V (20mm) * 1
ESR=22mOHm,RippleCurrent=2.15A

To meet Cuppermine 1.133GHz CPU Transient Spec.
The spec as follow :
Vcore=1.7V,Imax=22A,Istpgnt=2.5A
Vtran(min)=-0.110V,Vtran(max)=+0.080V
Iripple(input)=8.34A

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Document Number		

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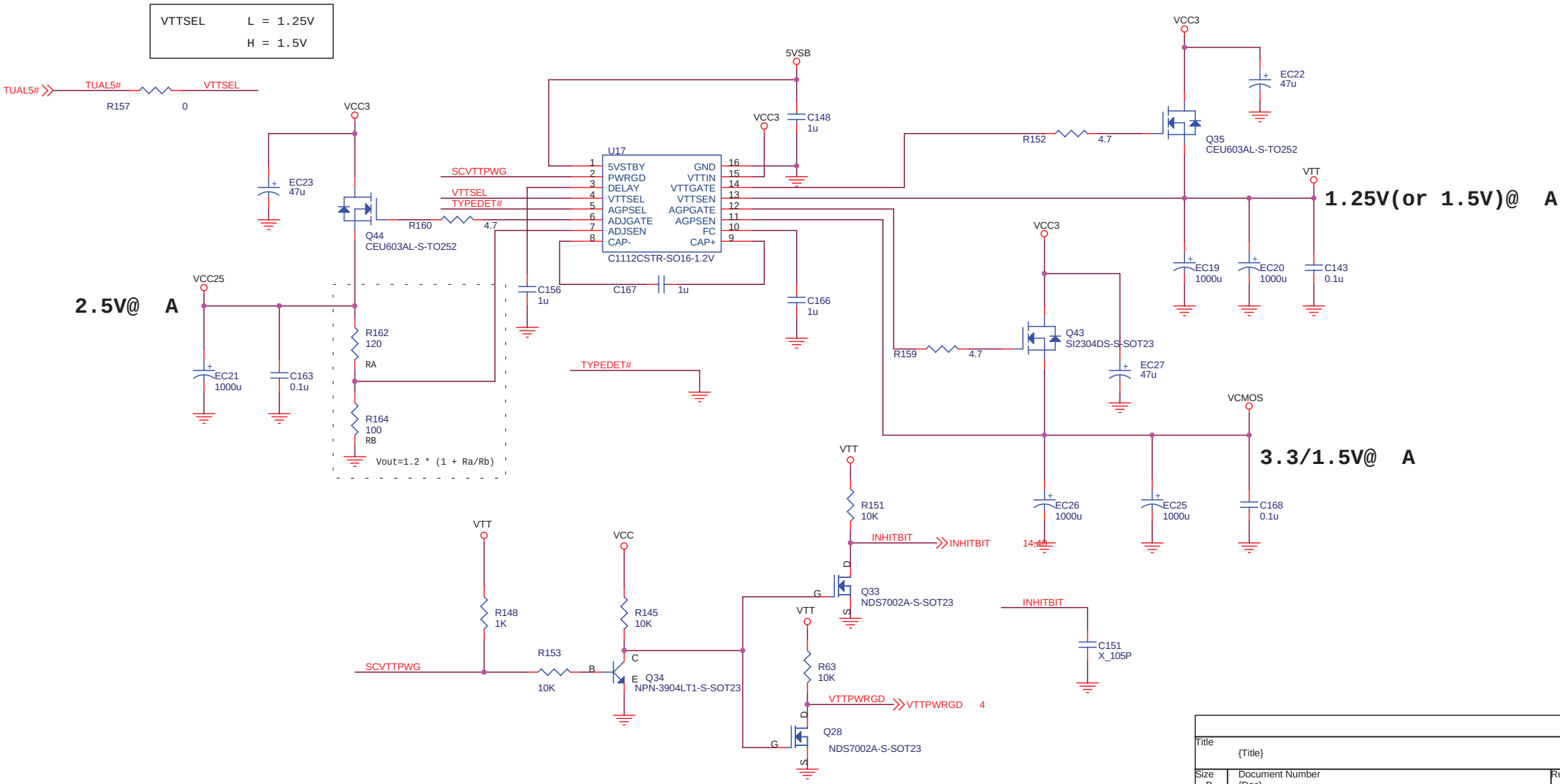

Title	{Title}		
Size B	Document Number {Doc}		Rev 100
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Voltage Regulators

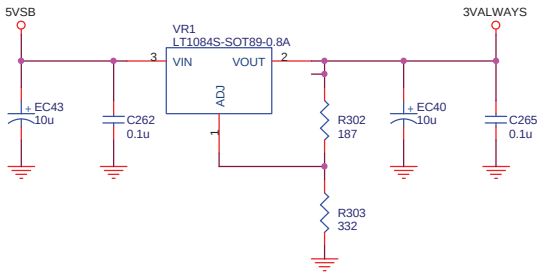
SI2303DS (P-CH,SOT-23) Spec :

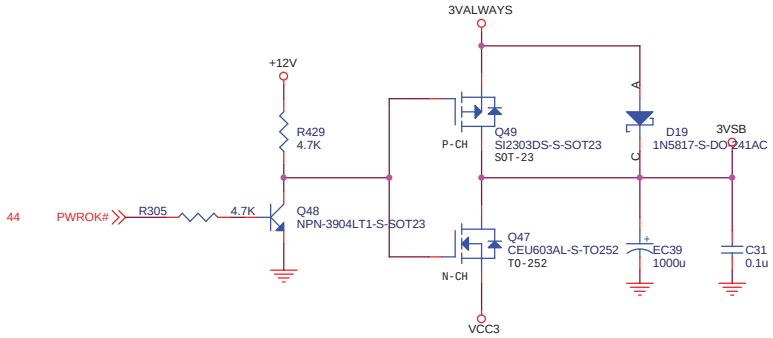
1.Vgs=+/-20V
2.Id=-1.7A,Rds(on)=210mOHm @ Vgs=-10V,T=25
Id=-1.3A,Rds(on)=460mOHm @ Vgs=-4.5

CET,CEU73AL (P-CH,TO-252)

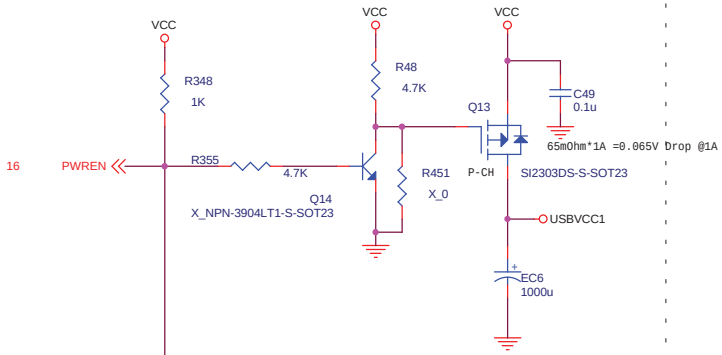
1.Vgs=+/-20V
2.Id(max)=240A@T=125-Pulse
3.Id=-25A,Rds(on)=22mOHm @ Vgs=-10V
Id=-10A,Rds(on)=40mOHm @ Vgs=-4.5
4.Qg=40nC(max),Qgs=6nC(typ),Qgd=2nC(typ)
@Vds=10V,Id=25A,Vgs=10V

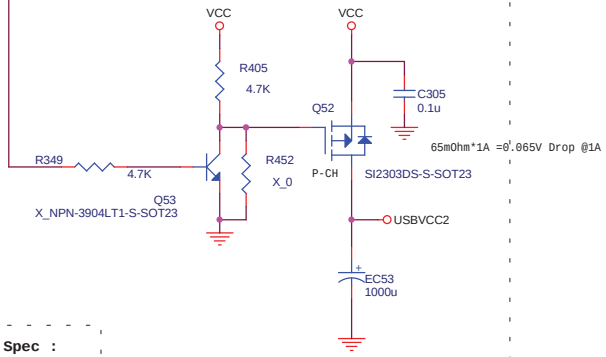
VCC 3SBY Voltage Regulator





USB Power Control





IRLML6402 (P-CH,SOT-23) Spec :

1.Vgs=+/-12V
2.Id=-3.7A,Rds(on)=65mOHm @ Vgs=-4.5V,T=25
Id=-2.2A,Rds(on)=135mOHm @ Vgs=-2.5,T=25

Micro Star Restricted Secret

Title	System Voltage Regulators	Rev
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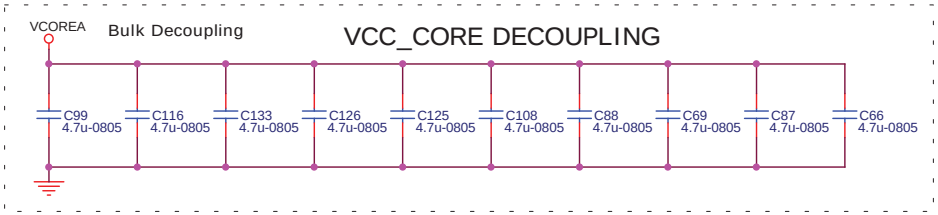
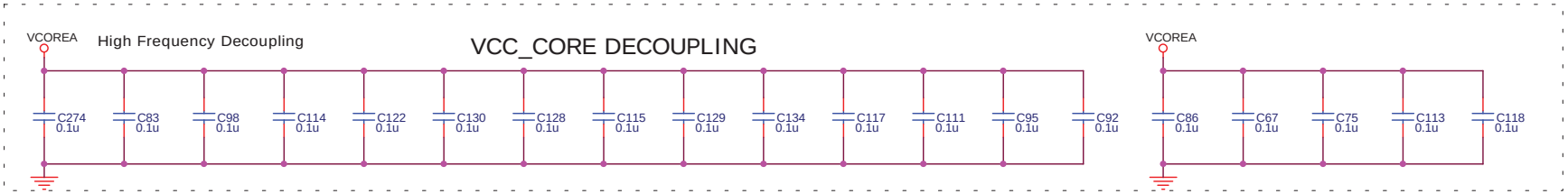
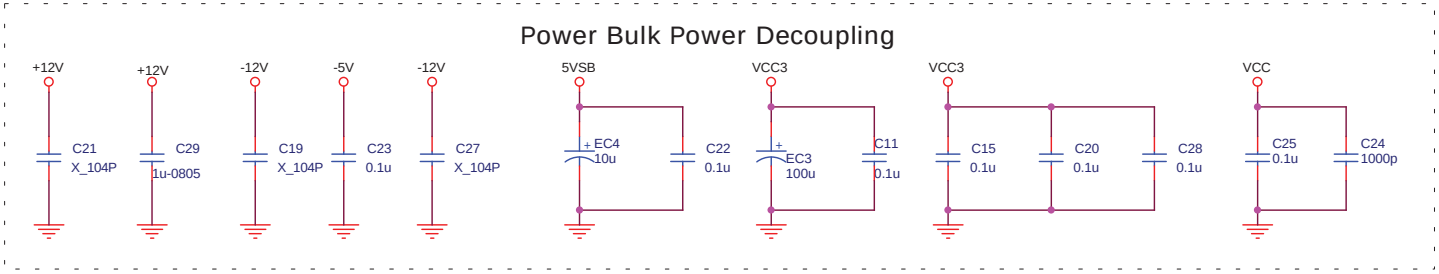
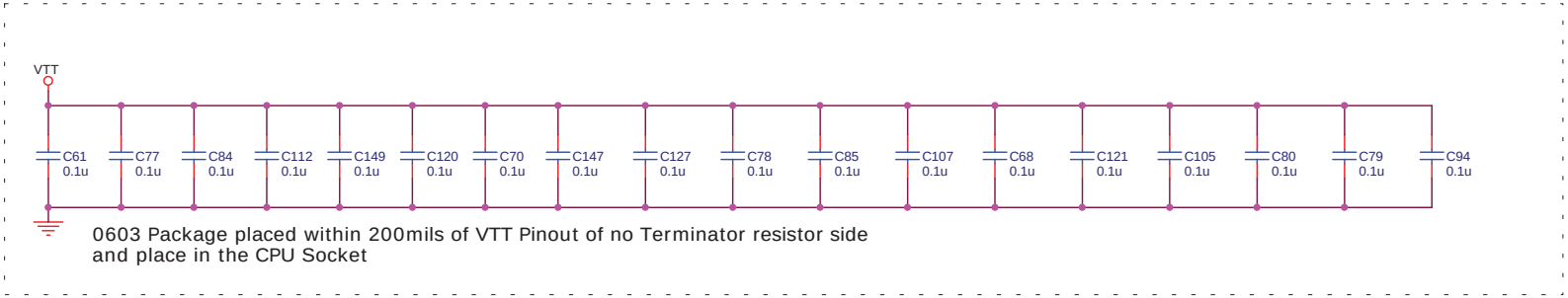
370-pin Socket Decoupling









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Title: VRM Decoupling	Rev: 100
Document Number:	
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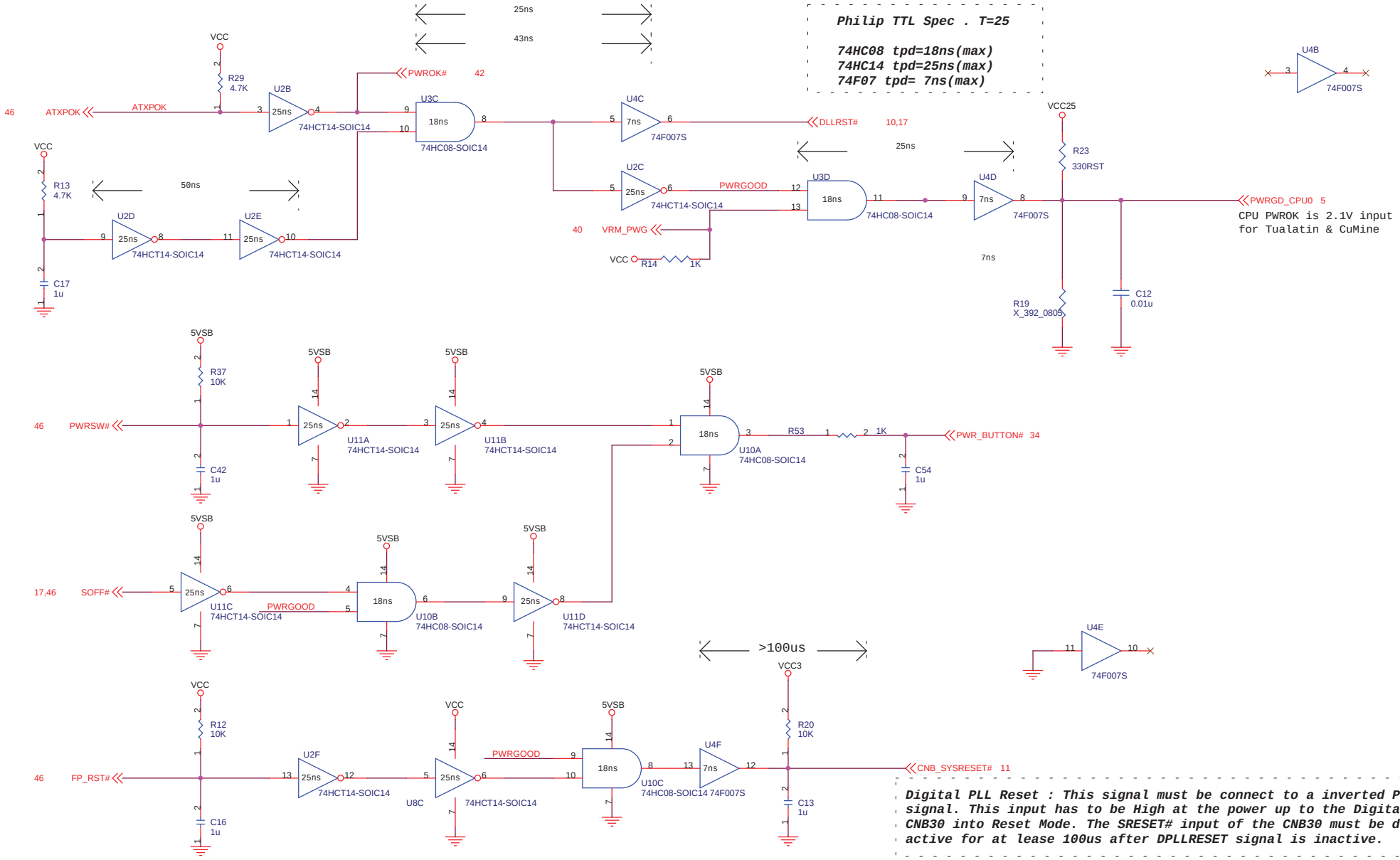

Micro Star Restricted Secret

Title	Power OK / Reset	Rev
Document Number		100
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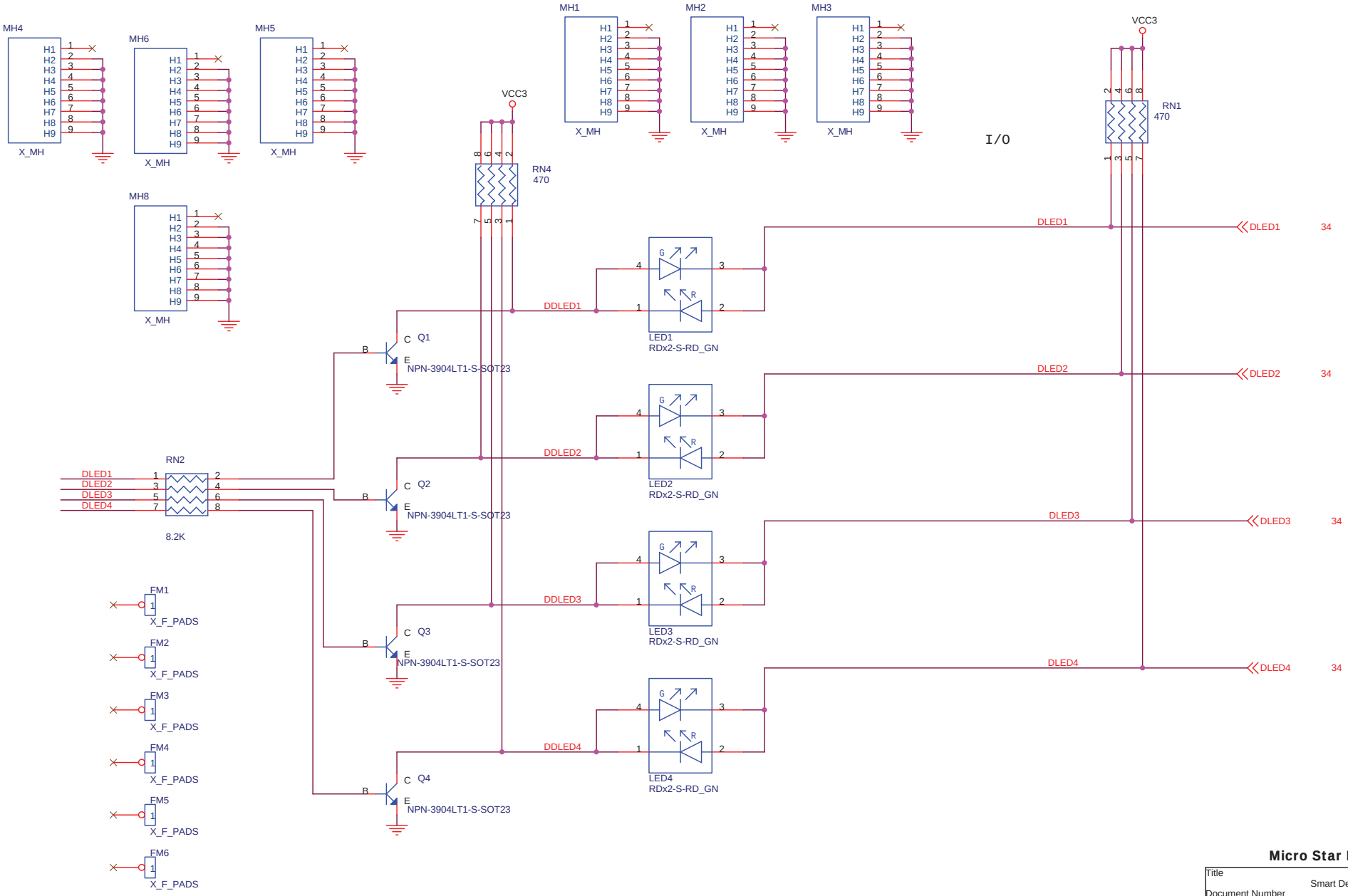

Micro Star Restricted Secret

Title: Smart Debug LED	Rev: 100
Document Number	
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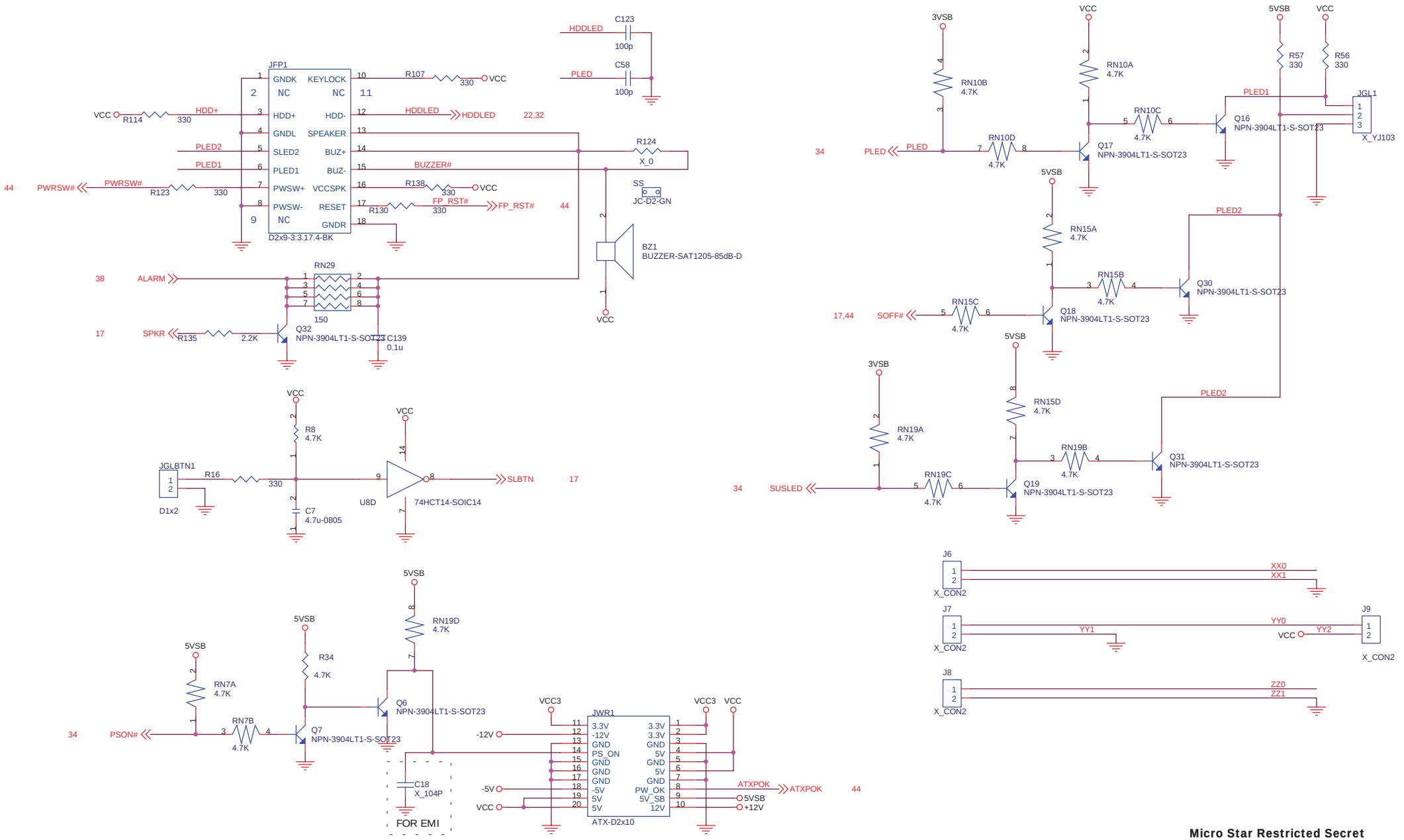

Micro Star Restricted Secret

Title	Front Panel and ATX Power Connector
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General Spec.

PCI Config.

DEVICE	ICH INT Pin	IDSEL	CLOCK	PIN OUT	R#/G#
PCI SLOT1	INT#1 INT#2 INT#3 INT#4	AD18	PCICLK1		0
PCI SLOT2	INT#2 INT#3 INT#4 INT#1	AD19	PCICLK2		1
CSB5	INT#0 (USB) INT#1 INT#2 INT#3		SBPCLK		X
ATI Rage (VGA)	INT#5	AD20	VGACLK		2
LAN 1	INT#6	AD21	LAN1PCLK		3
LAN 2	INT#7	AD22	LAN2PCLK		4
Promise IDE Raid	INT#8	AD23	IDEPCLK		5
PCI66 SLOT1	INT#9 INT#10 INT#11 INT#12	P64AD18	P64CLK1		64R/G# 0

*AD26 = Check on ASUS board
**AD19 = Check on RCC reference schematic

NS PC97317

GPIO Pin	Type	Function	Pin Number
GPIO 22	I/O	Pull Up to 3VSB through 4.7K ohms (DLED1)	16
GPIO 23	I/O	Pull Up to 3VSB through 4.7K ohms (DLED2)	17
GPIO 24	I/O	Pull Up to 3VSB through 4.7K ohms (DLED3)	18
GPIO 25	I/O	Pull Up to 3VSB through 4.7K ohms (DLED4)	19
GPIO 15	I/O	RING#	24
GPIO 16	I/O	P64PME# PCI64 Bus PME# Event	25
GPIO 17	I/O	IO_PCIPME# PCI32 Bus PME# Event	26
GPIO 20	I/O	XEN Only 4.7K VCC3 Pull-High	15
GPIO 21	I/O	XWR Only 4.7K VCC3 Pull-High	14
GPIO 42	I/O	SLBTIN Only 4.7K 3VSB Pull-High	35
GPIO 50	I/O	Power Button	36
GPIO 51	I/O	SMI# EVENT	37
GPIO 52	I/O	SIOWAKE-UP Only 4.7K 3VSB Pull-High	38
GPIO 63	I/O	Only 3VSB Pull-High	48
GPIO 44	I/O	POR - External Event	50
GPIO 45	I/O	Suspend LED	51
GPIO 46	I/O	Power & Green LED	52
GPIO 47	I/O	Only 3VSB Pull-High	53

DRAM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	1010000B	DCLK0
DIMM 2	1010001B	DCLK1

W83782D	00101101B
82550	11001000B

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General Spec.

CSB5 General Purpose Event List

Pin	Event	Orginal Signal	MS6394 implement
V3	GEVENT_0	ACPI General Purpose Event	CPU SERR# Event
W1	GEVENT_1	ACPI General Purpose Event	CPU ThermTrip# Event
W2	GEVENT_2	ACPI General Purpose Event	P2ALERT
W3	GEVENT_3	ACPI General Purpose Event	SMIINT0# W83782 SMI Event
W4	GEVENT_4	ACPI General Purpose Event	Therm# W83782 Thermal Event
Y4	GEVENT_5	No Use	
Y1	GEVENT_6	No Use	
Y2	GEVENT_7	No Use	
Y19	GEVENT_8	No Use	
V17	GEVENT_9	No Use	
U16	GEVENT_10	No Use	
V15	GEVENT_11	No Use	
T20	GEVENT_12	No Use	
T19	GEVENT_13	No Use	
T18	GEVENT_14	General Purpose Event	CMOS Clear
U18	GEVENT_15	General Purpose Event	Clear NVRAM #
Y16	GEVENT_16	No Use	
V12	GEVENT_17	General Purpose Event	CPU Present Detect
U12	GEVENT_18	No Use	
V19	GEVENT_19	General Purpose Event	IOAPIC
W20	GEVENT_20	General Purpose Event	IOAPIC
U14	GEVENT_21	No Use	
Y20	GEVENT_22	General Purpose Event	FOR BIOS CS# Function
U19	GEVENT_23	General Purpose Event	FOR BIOS Write Protect Function
U20	GPOC 0	General Purpose Event	SMBus Clock
V20	GPOC 1	General Purpose Event	SMBus Data
T17	GPOC 2	No Use	

Gevent 23	
H	Flash
L	non Flash

CNB30LE DRAM Support List

Generation	Depth	Size/Row
16M 2-Banks SDRAM	11/9	16MB
	11/10	32MB
64M 2-Banks SDRAM	13/10	128MB
64M 4-Banks SDRAM	12/8	32MB
	12/9	64MB
	12/10	128MB
	13/10	256MB**
	12/9	64MB
128M 4-Banks SDRAM	12/10	128MB**
	13/10	256MB**
	*12/11	256MB
256M 4-Banks SDRAM	13/8	64MB
	13/9	128MB
	13/10	256MB
	13/11	512MB
	*12/10	128MB

*Not List in CNB30LE"Table2. MA Mapping for Row and Column Address for SDRAM"
** Not List in CNB30LE "Table 1. Support SDRAMs" table

TTL Gate Count List :

TTL	Num.	Locate (Free Gate)
74F07	3	U10(1),U6(0),U1(0)
74F08	2	U58-5VSB(2)
74F244	2	U7(0),U9(0)
74HC08	1	U2(0)
74HC14	3	U5(1),U16(0),U57-5VSB(2)
74HC273	1	U8(0)
74LVC07	1	U3(0)

Intel PC SDRAM Register DIMM Spec :

Type	PLL	Support
64MByte 72bit ECC SDRAM	Non	No
64MByte 72bit ECC SDRAM	Yes	Yes
72bit ECC Stacked SDRAM (2 Rows)	Yes	Yes
256MB using 16M*4 (64Mbit) SDRAMs		
512MB using 32M*4 (128Mbit) SDRAMs		
1GB using 64M*4 (256Mbit) SDRAMs		
72bit ECC Unstacked SDRAM (1 Row)	Yes	Yes
128MB using 16M*4 (64Mbit) SDRAMs		
256MB using 32M*4 (128Mbit) SDRAMs		
512MB using 64M*4 (256Mbit) SDRAMs		

Note :
1.With PLL = CK0 -> PLL , CK1,CK2,CK3 Terminated
2.Register Signal :
S0#/S2# (Chip Selset)
DOMB[0..7] (DQ Mask)
BA[0..1] (Bank Select)
A[0..12] (Address)
RAS# (Row Address Strobe)
CAS# (Column Address Strobe)
CKE0 (Clock Enable)
WE# (Write Enable)

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General Spec.

Power Button Event Ckt :

From Panel — **PWRSW#** Active : Low

From CSB5 — **SOFF#** Active : Low

From Power OK Ckt — **PWRGOOD** Active : High

→ **PWR_BUTTON#** Active : Low — To PC97417

Panel Reset Button Event Ckt :

From Panel — **FP_RST#** Active : Low

From Power OK Ckt — **PWRGOOD** Active : High

→ **CNB_SYSRESET#** To HE-WS
Active : Low
System Reset : This is a reset input to CNB30. This signal resets any of the current operations and put the whole device in intial state.

System Reset Map :

From CSB5 — **PCIRST_X#** Active : Low

- → **PCIRST#** Active : Low — To HE-WS,CIOB,AGP Pro Slot
- → **RSTDRV** Active : High — To W83782D
- → **BRSTDRV#** Active : Low — To IDE Connector,PC97417

From CIOB20 — **P64PCIRST1_X#** Active : Low → **P64PCIRST1#** Active : Low — To ATI Rage XL/PCI32 Slot1/PCI32 Slot2/LAN1/LAN2

From CIOB20 — **P64PCIRST2_X#** Active : Low → **P64PCIRST2#** Active : Low — To PCI64 Slot1/PCI64 Slot2

System Power OK Architecture :

From ATX Power — **ATX Power OK** Active : High

OnBoard RC-Delay — **VCC RC-Delay Reset** Active : High

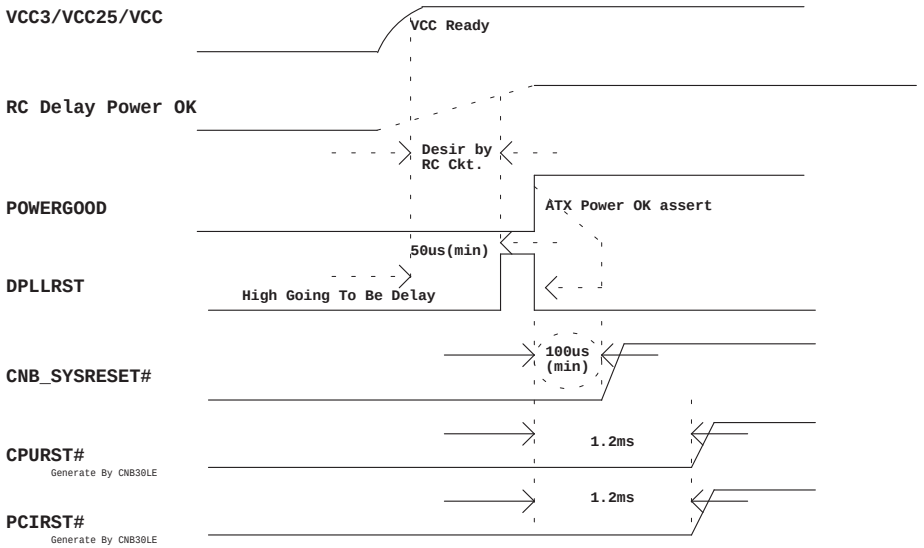
→ **DLLRST#** Active : High — To HE-WS,CIOB,CSB5

Digital PLL Reset : This signal must be connect to a inverted Power Good signal. This input has to be High at the power up to the Digital PLL in CNB30 into Reset Mode. The SRESET# input of the CNB30 must be driven active for at lease 100us after DPLLRESET signal is inactive.

→ **PWRGOOD** Active : High
- → **PWRGD_CPU0** — To CPU 0
- → **PWRGD_CPU1** — To CPU 1

From VRM Module — **VRM_PWG** Active : High

Reset Timing :



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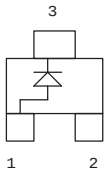
BAS70



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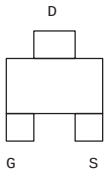

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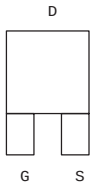

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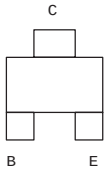
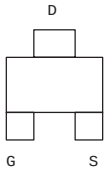


NDS351



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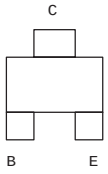
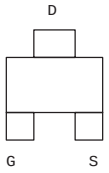
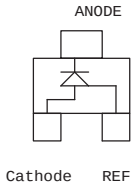


Si2303



LM431



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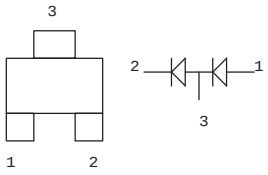

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U32_X
MXIC-4M-PLCC32

PCB
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BAT1_X
BAT-B-CR2032-P-3V-220mAh

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