Last Schematic Update Date: 03/01/2001

MS-6378 *Version 1.0*

CPU: AMD Socket-462 Processor

System Chipset: VIA KLE133(North)
+ 686B (South)

Expansion: PCI * 3
CNR * 1

On Board Device:

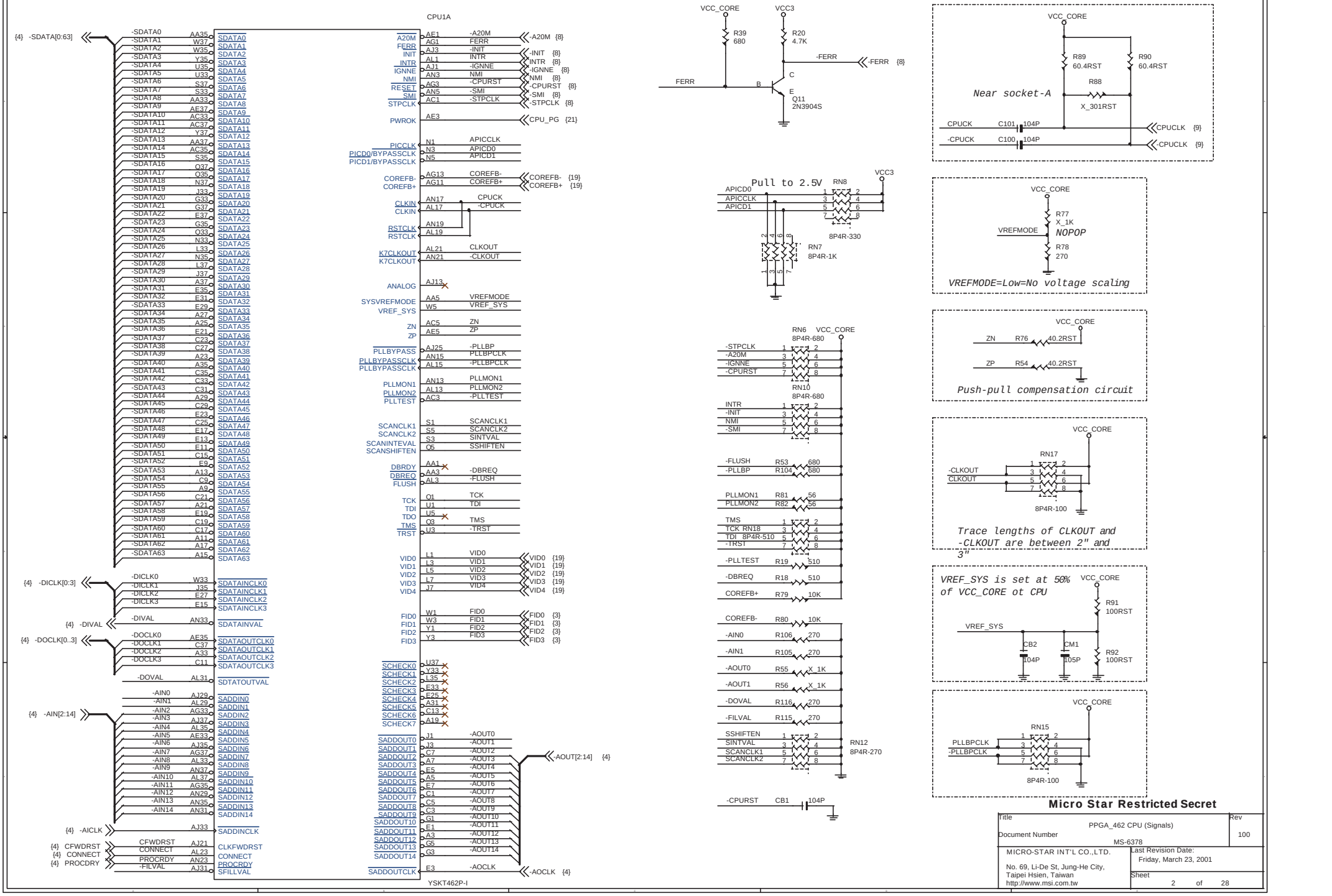
AC97 Codec ALC100P

Optional: ISA * 1

ERP BOM	Function Description
601-6378-04S	MSI Standard: With CNR. W/O ISA,LAN,STR.
601-6378-03S	MSI Option:A With ISA,LAN,CNR. W/O STR.
601-6378-05S	For Legend: With ISA,CNR,STR.W/O Lan. Special Request:Legend SPEC.
601-6378-010 from 04S	MSI Standard: With CNR,STR. W/O ISA,LAN.
601-6378-020 from 03S	MSI Option:A With ISA,LAN,CNR,STR.

	For Actebis: w/o ISA,w/o LAN. Special Request:I/O with Shield.

Title: Cover Page		Rev: 100
Document Number: MS-6378		
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Friday, March 23, 2001	
	Sheet 1 of 28	


CPU1A
YSKT462P-I
Pull to 2.5V
RN8
8P4R-330
RN7
8P4R-1K
RN6
8P4R-680
RN10
8P4R-680
RN12
8P4R-270
RN17
8P4R-100
RN15
8P4R-100
Near socket-A
NOPOP
VREFMODE=Low=No voltage scaling
Push-pull compensation circuit
Trace lengths of CLKOUT and -CLKOUT are between 2" and 3"
VREF_SYS is set at 50% of VCC_CORE ot CPU
Micro Star Restricted Secret
PPGA_462 CPU (Signals)
MS-6378
MICRO-STAR INT'L CO.,LTD.
No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan
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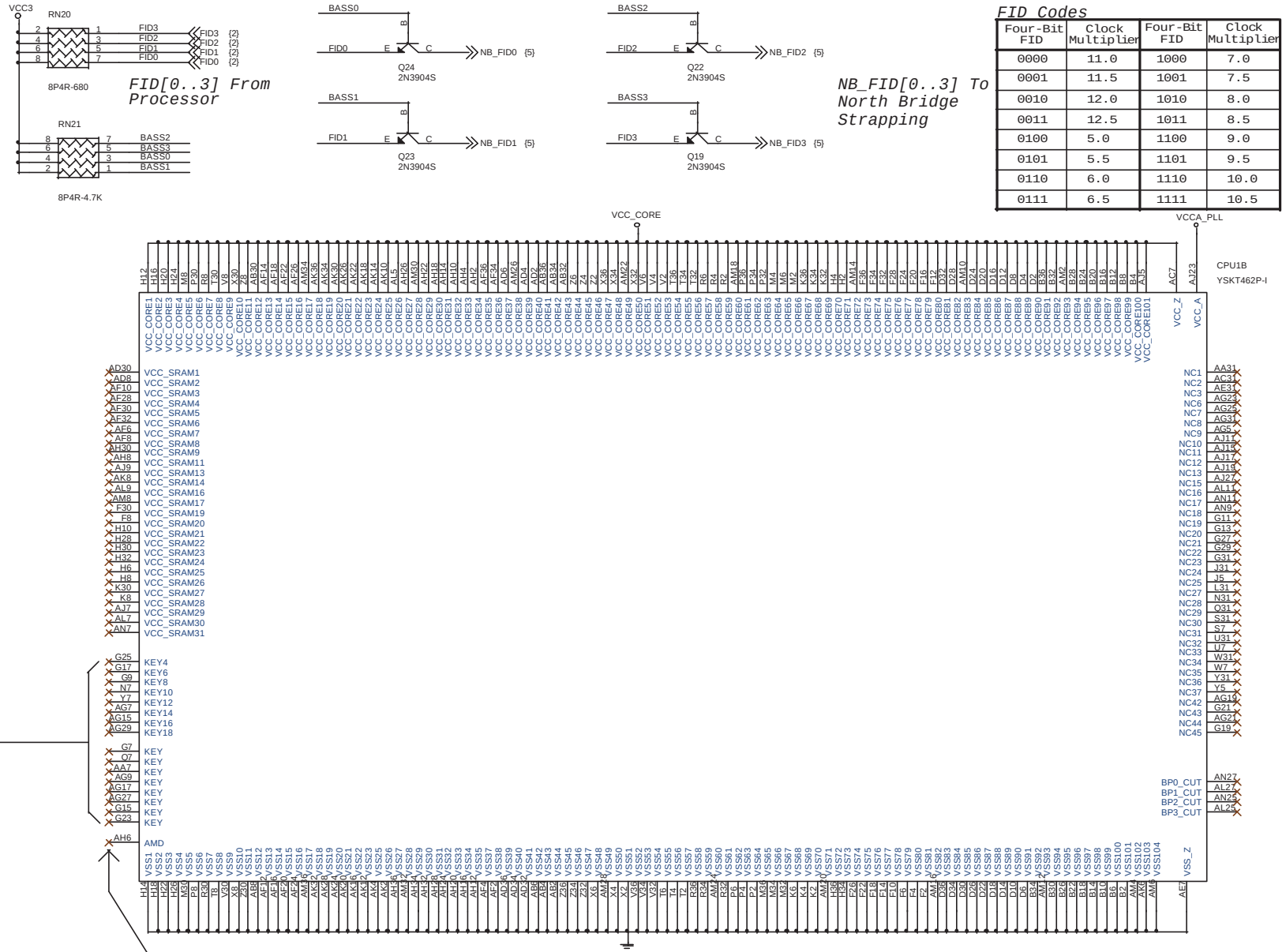

FID Codes

Four-Bit FID	Clock Multiplier	Four-Bit FID	Clock Multiplier
0000	11.0	1000	7.0
0001	11.5	1001	7.5
0010	12.0	1010	8.0
0011	12.5	1011	8.5
0100	5.0	1100	9.0
0101	5.5	1101	9.5
0110	6.0	1110	10.0
0111	6.5	1111	10.5

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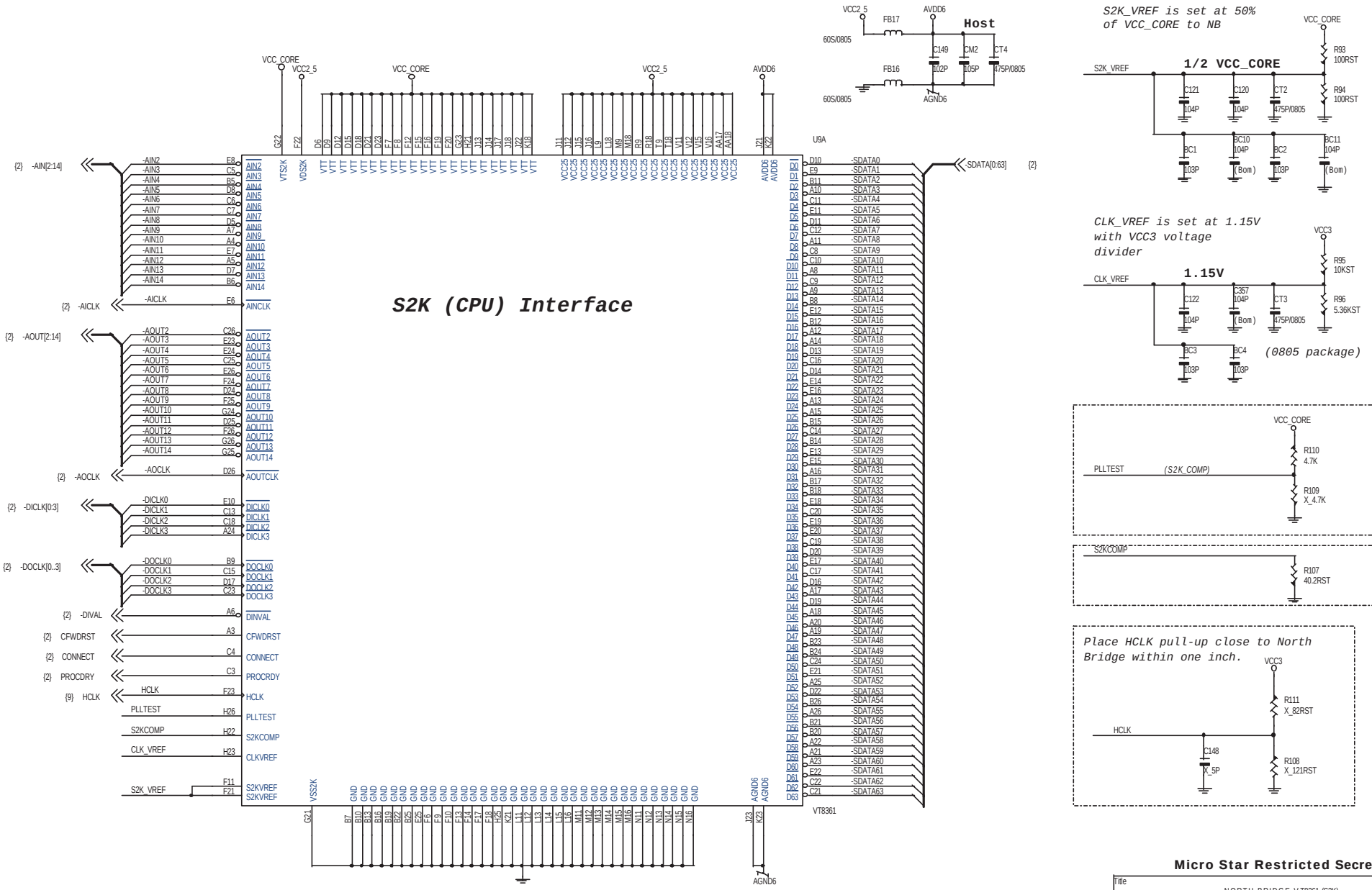
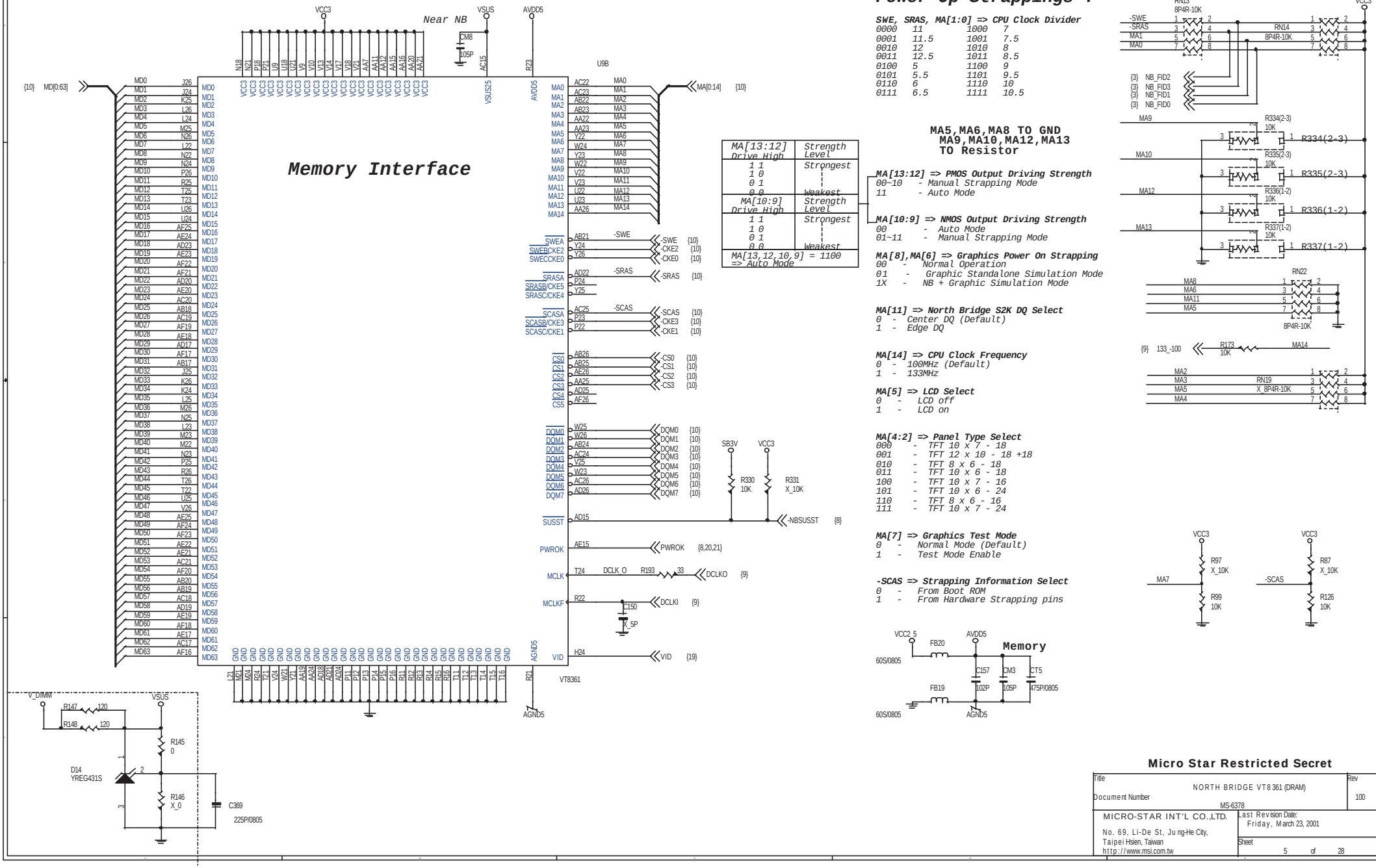
Title	PPGA_462 CPU (Power & Ground)	Rev 100
Document Number	MS-6378	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Friday, March 23, 2001	Sheet 3 of 28


S2K (CPU) Interface
U9A
VT8361
Host
FB17
FB16
60S/0805
C149
102P
CM2
105P
CT4
475P/0805
AVDD6
AGND6
VCC2_5
VCC_CORE
S2K_VREF is set at 50% of VCC_CORE to NB
1/2 VCC_CORE
R93 100RST
R94 100RST
C121 104P
C120 104P
CT2 475P/0805
BC1 103P
BC10 104P (Bom)
BC2 103P
BC11 104P (Bom)
CLK_VREF is set at 1.15V with VCC3 voltage divider
VCC3
1.15V
R95 10KST
R96 5.36KST
C122 104P
C357 104P (Bom)
CT3 475P/0805
BC3 103P
BC4 103P
(0805 package)
PLLTEST
(S2K_COMP)
R110 4.7K
R109 X_4.7K
S2KCOMP
R107 40.2RST
Place HCLK pull-up close to North Bridge within one inch.
HCLK
R111 X_82RST
C148 X_5P
R108 X_121RST
-AIN2
-AIN3
-AIN4
-AIN5
-AIN6
-AIN7
-AIN8
-AIN9
-AIN10
-AIN11
-AIN12
-AIN13
-AIN14
-AICLK
-AOUT2
-AOUT3
-AOUT4
-AOUT5
-AOUT6
-AOUT7
-AOUT8
-AOUT9
-AOUT10
-AOUT11
-AOUT12
-AOUT13
-AOUT14
-AOCLK
-DICLK0
-DICLK1
-DICLK2
-DICLK3
-DOCLK0
-DOCLK1
-DOCLK2
-DOCLK3
-DIVAL
CFWDRST
CONNECT
PROCRDY
HCLK
PLLTEST
S2KCOMP
CLK_VREF
S2K_VREF
-SDATA[0:63]
Micro Star Restricted Secret
Title
NORTH BRIDGE VT8361 (S2K)
Document Number
MS-6378
Rev
100
MICRO-STAR INT'L CO.,LTD.
No. 69, Li-De St, Ju ng-He City, Taipei Hsien, Taiwan
http://www.msi.com.tw
Last Revision Date:
Friday, March 23, 2001
Sheet
4 of 28



Power Up Strappings :

SWE, SRAS, MA[1:0] => CPU Clock Divider

0000	11	1000	7
0001	11.5	1001	7.5
0010	12	1010	8
0011	12.5	1011	8.5
0100	5	1100	9
0101	5.5	1101	9.5
0110	6	1110	10
0111	6.5	1111	10.5

MA5,MA6,MA8 TO GND
MA9,MA10,MA12,MA13
TO Resistor

MA[13:12] => PMOS Output Driving Strength
00~10 - Manual Strapping Mode
11 - Auto Mode

MA[10:9] => NMOS Output Driving Strength
00 - Auto Mode
01~11 - Manual Strapping Mode

MA[8],MA[6] => Graphics Power On Strapping
00 - Normal Operation
01 - Graphic Standalone Simulation Mode
1X - NB + Graphic Simulation Mode

MA[11] => North Bridge S2K DQ Select
0 - Center DQ (Default)
1 - Edge DQ

MA[14] => CPU Clock Frequency
0 - 100MHz (Default)
1 - 133MHz

MA[5] => LCD Select
0 - LCD off
1 - LCD on

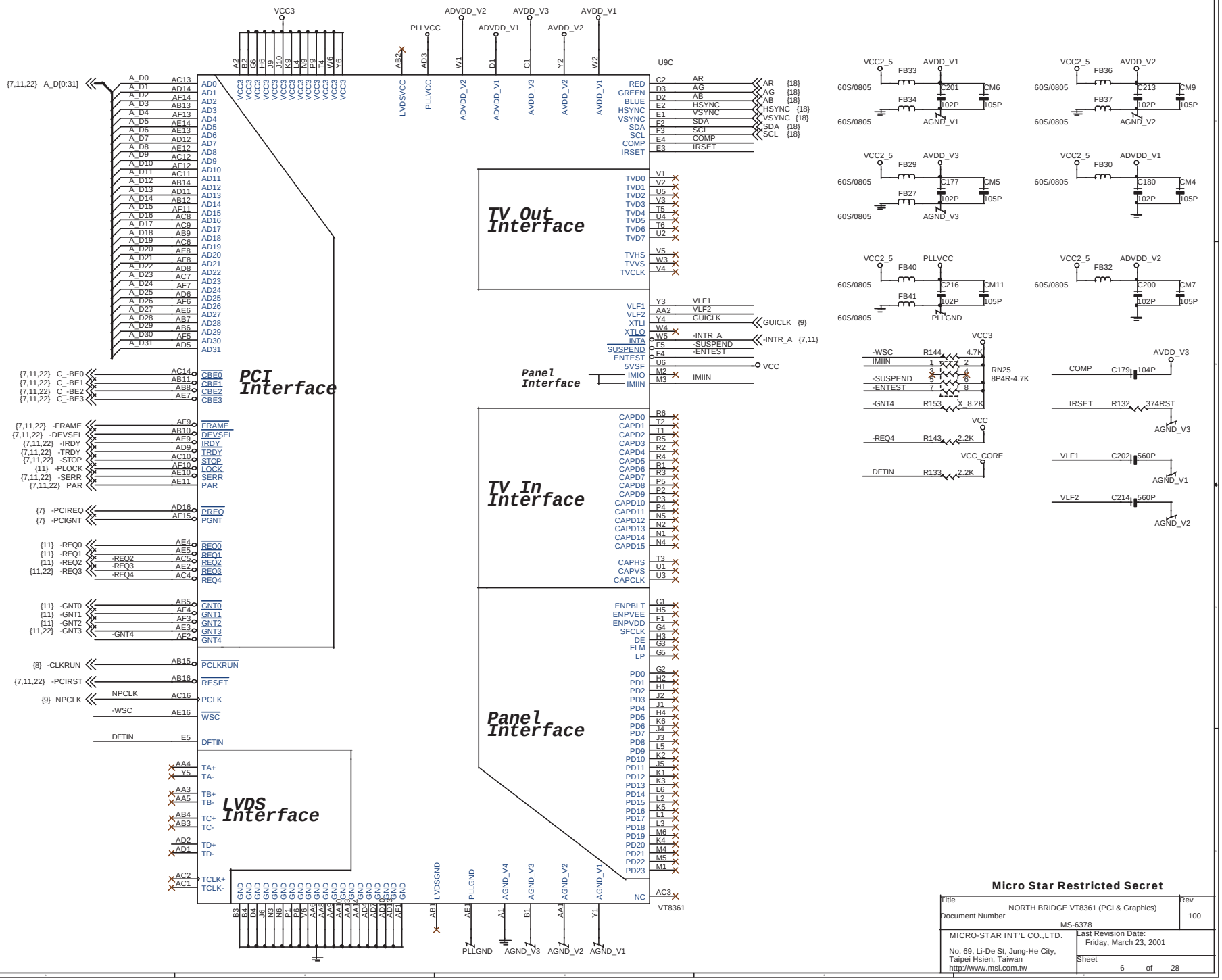
MA[4:2] => Panel Type Select
000 - TFT 10 x 7 - 18
001 - TFT 12 x 10 - 18 +18
010 - TFT 8 x 6 - 18
011 - TFT 10 x 6 - 18
100 - TFT 10 x 7 - 16
101 - TFT 10 x 6 - 24
110 - TFT 8 x 6 - 16
111 - TFT 10 x 7 - 24

MA[7] => Graphics Test Mode
0 - Normal Mode (Default)
1 - Test Mode Enable

-SCAS => Strapping Information Select
0 - From Boot ROM
1 - From Hardware Strapping pins

Micro Star Restricted Secret

Title	NORTH BRIDGE VT8361 (DRAM)	Rev 100
Document Number	MS-6378	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Ju ng-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Friday, March 23, 2001	Sheet 5 of 28


PCI Interface
TV Out Interface
TV In Interface
Panel Interface
LVDS Interface
Panel Interface
U9C
VT8361
{7,11,22} A_D[0:31]
A_D0
A_D1
A_D2
A_D3
A_D4
A_D5
A_D6
A_D7
A_D8
A_D9
A_D10
A_D11
A_D12
A_D13
A_D14
A_D15
A_D16
A_D17
A_D18
A_D19
A_D20
A_D21
A_D22
A_D23
A_D24
A_D25
A_D26
A_D27
A_D28
A_D29
A_D30
A_D31
{7,11,22} C_-BE0
{7,11,22} C_-BE1
{7,11,22} C_-BE2
{7,11,22} C_-BE3
{7,11,22} -FRAME
{7,11,22} -DEVSEL
{7,11,22} -IRDY
{7,11,22} -TRDY
{7,11,22} -STOP
{11} -PLOCK
{7,11,22} -SERR
{7,11,22} PAR
{7} -PCIREQ
{7} -PCIGNT
{11} -REQ0
{11} -REQ1
{11} -REQ2
{11,22} -REQ3
-REQ2
-REQ3
-REQ4
{11} -GNT0
{11} -GNT1
{11} -GNT2
{11,22} -GNT3
-GNT4
{8} -CLKRUN
{7,11,22} -PCIRST
{9} NPCLK
-WSC
DFTIN
RED
GREEN
BLUE
HSYNC
VSYNC
SDA
SCL
COMP
IRSET
AR {18}
AG {18}
AB {18}
HSYNC {18}
VSYNC {18}
SDA {18}
SCL {18}
TVD0
TVD1
TVD2
TVD3
TVD4
TVD5
TVD6
TVD7
TVHS
TVVS
TVCLK
VLF1
VLF2
XTLI
XTLO
INTA
SUSPEND
ENTEST
5VSF
IMIO
IMIIN
GUICLK {9}
-INTR_A {7,11}
-SUSPEND
-ENTEST
VCC
CAPD0
CAPD1
CAPD2
CAPD3
CAPD4
CAPD5
CAPD6
CAPD7
CAPD8
CAPD9
CAPD10
CAPD11
CAPD12
CAPD13
CAPD14
CAPD15
CAPHS
CAPVS
CAPCLK
ENPBLT
ENPVEE
ENPVDD
SFCLK
DE
FLM
LP
PD0
PD1
PD2
PD3
PD4
PD5
PD6
PD7
PD8
PD9
PD10
PD11
PD12
PD13
PD14
PD15
PD16
PD17
PD18
PD19
PD20
PD21
PD22
PD23
NC
TA+
TA-
TB+
TB-
TC+
TC-
TD+
TD-
TCLK+
TCLK-
VCC3
PLLVCC
ADVDD_V2
ADVDD_V3
ADVDD_V1
AVDD_V3
AVDD_V2
AVDD_V1
LVDSVCC
LVDSGND
PLLGND
AGND_V4
AGND_V3
AGND_V2
AGND_V1
VCC2_5
FB33
FB34
FB36
FB37
FB29
FB27
FB30
FB40
FB41
FB32
C201
C213
C177
C180
C216
C200
102P
105P
CM6
CM9
CM5
CM4
CM11
CM7
60S/0805
-WSC
IMIIN
-SUSPEND
-ENTEST
-GNT4
-REQ4
DFTIN
RN25
8P4R-4.7K
R144 4.7K
R153 8.2K
R143 2.2K
R133 2.2K
VCC_CORE
COMP
IRSET
VLF1
VLF2
C179 104P
R132 374RST
C202 560P
C214 560P
Micro Star Restricted Secret
Title
NORTH BRIDGE VT8361 (PCI & Graphics)
Rev
100
Document Number
MS-6378
MICRO-STAR INT'L CO.,LTD.
No. 69, Li-De St, Jung-He City,
Taipei Hsien, Taiwan
http://www.msi.com.tw
Last Revision Date:
Friday, March 23, 2001
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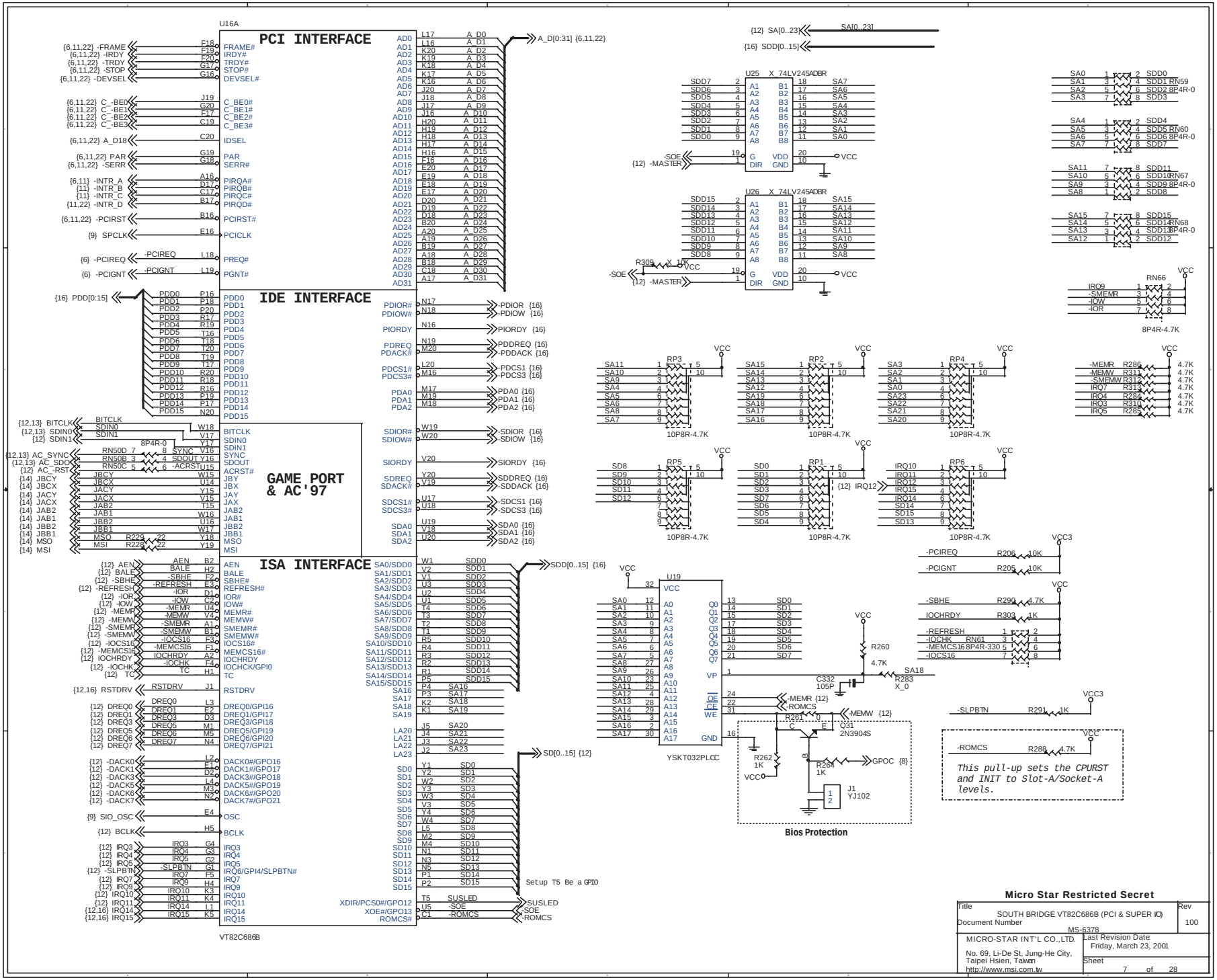
PCI INTERFACE
IDE INTERFACE
GAME PORT & AC'97
ISA INTERFACE
VT82C686B
U16A
Bios Protection
Micro Star Restricted Secret
Title
SOUTH BRIDGE VT82C686B (PCI & SUPER IO)
Document Number
MS-6378
Rev
100
MICRO-STAR INT'L CO.,LTD.
No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan
http://www.msi.com.tw
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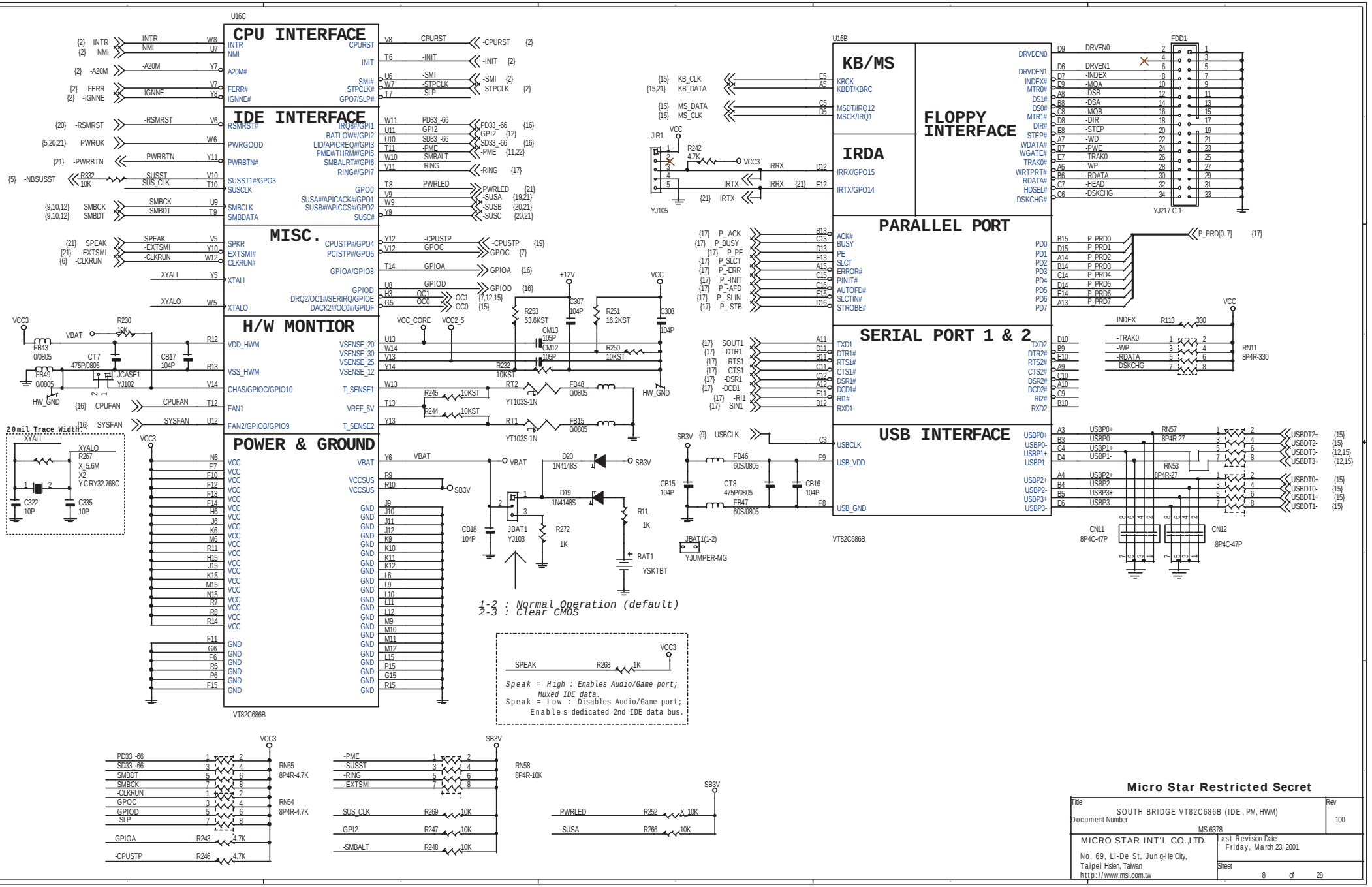
This pull-up sets the CPURST and INIT to Slot-A/Socket-A levels.


CPU INTERFACE
IDE INTERFACE
MISC.
H/W MONTIOR
POWER & GROUND
KB/MS
IRDA
FLOPPY INTERFACE
PARALLEL PORT
SERIAL PORT 1 & 2
USB INTERFACE
VT82C686B
U16C
U16B
FDD1
YJ217-C-1
YJ105
JIR1
JBAT1
YJ103
BAT1
YSKTBT
YJUMPER-MG
JCASE1
YJ102
CN11
CN12
8P4C-47P
RN11
8P4R-330
RN53
RN57
8P4R-27
RN54
RN55
RN58
8P4R-4.7K
8P4R-10K
20mil Trace Width
1-2 : Normal Operation (default)
2-3 : Clear CMOS
Speak = High : Enables Audio/Game port; Muxed IDE data.
Speak = Low : Disables Audio/Game port; Enables dedicated 2nd IDE data bus.
Micro Star Restricted Secret
SOUTH BRIDGE VT82C686B (IDE, PM, HWM)
MS-6378
MICRO-STAR INT'L CO.,LTD.
No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan
http://www.msi.com.tw
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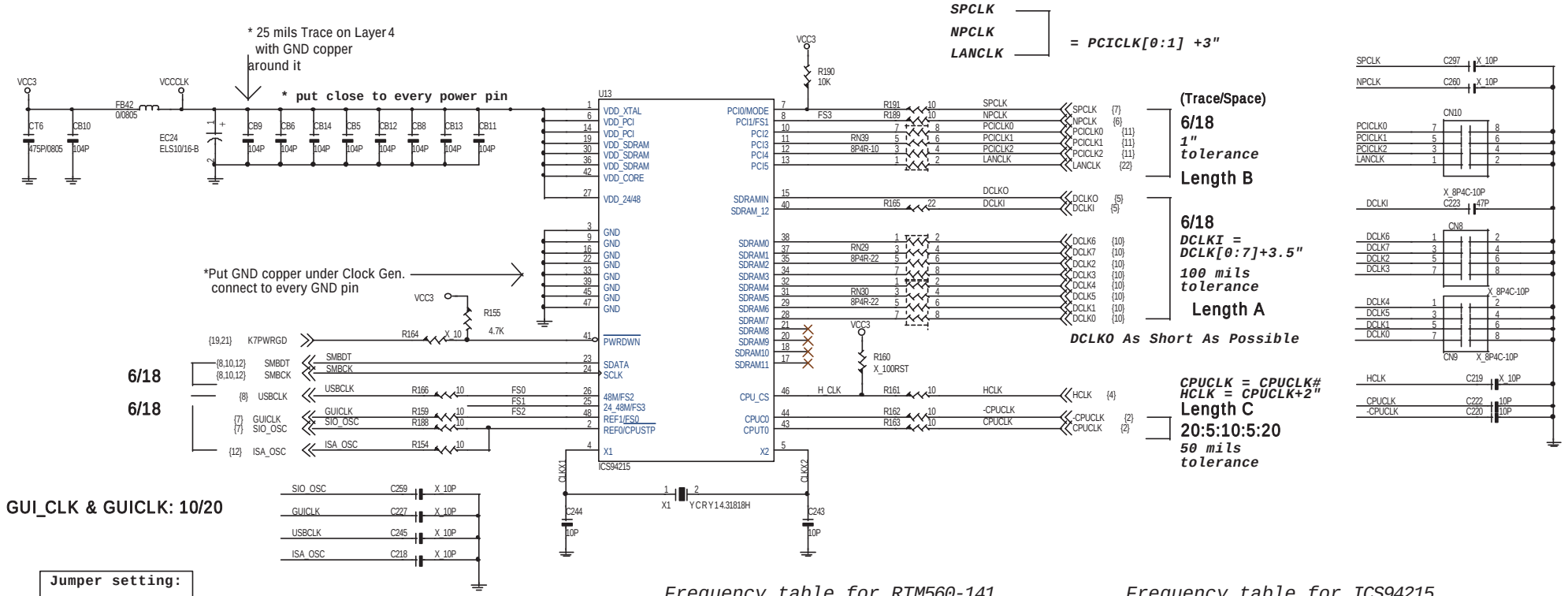

Frequency table for RTM560-141

FS3-0 4	FS3-0 3	FS3-0 2	FS3-0 1	CPU	PCI	CPU/PCI	Spread Spectrum
OFF	OFF	OFF	OFF	133.3	33.3	4	+/- 5%
OFF	OFF	OFF	ON	75	37.5	2	+/- 5%
OFF	OFF	ON	OFF	100.2	33.3	3	+/- 5%
OFF	OFF	ON	ON	66.8	33.4	2	+/- 5%
OFF	ON	OFF	OFF	79	39.5	2	OFF
OFF	ON	OFF	ON	110	36.7	3	OFF
OFF	ON	ON	OFF	115	38.3	3	OFF
OFF	ON	ON	ON	120	30	4	OFF
ON	OFF	OFF	OFF	133.3	33.3	4	OFF
ON	OFF	OFF	ON	83	27.7	3	OFF
ON	OFF	ON	OFF	100.2	33.3	3	OFF
ON	OFF	ON	ON	66.8	33.4	2	OFF
ON	ON	OFF	OFF	124	31	4	OFF
ON	ON	OFF	ON	129	32.3	4	OFF
ON	ON	ON	OFF	138	34.5	4	OFF
ON	ON	ON	ON	143	35.8	4	OFF

Frequency table for ICS94215

FS3-0 3	FS3-0 2	FS3-0 1	FS3-0 0	CPU	PCI	CPU/PCI
1	1	1	1	133.3	33.3	4
1	1	1	0	117	39	3
1	1	0	1	115	38.33	3
1	1	0	0	113	37.67	3
1	0	1	1	111	37.00	3
1	0	1	0	110	36.67	3
1	0	0	1	109	36.33	3
1	0	0	0	107	35.67	3
0	1	1	1	100	33.33	4
0	1	1	0	105	35.00	3
0	1	0	1	103	34.33	3
0	1	0	0	100.9	33.57	3
0	0	1	1	102	34	3
0	0	1	0	101	33.67	3
0	0	0	1	95	31.67	3
0	0	0	0	90	30	3

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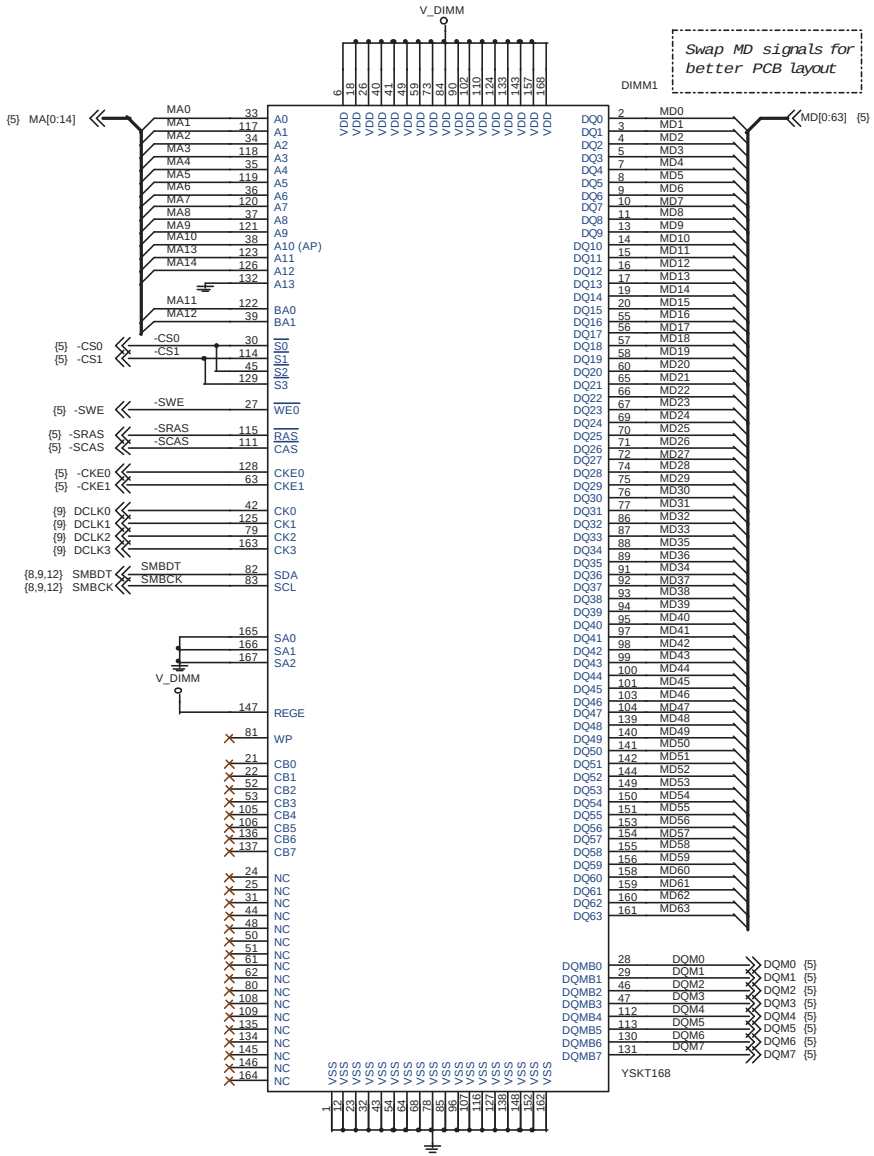
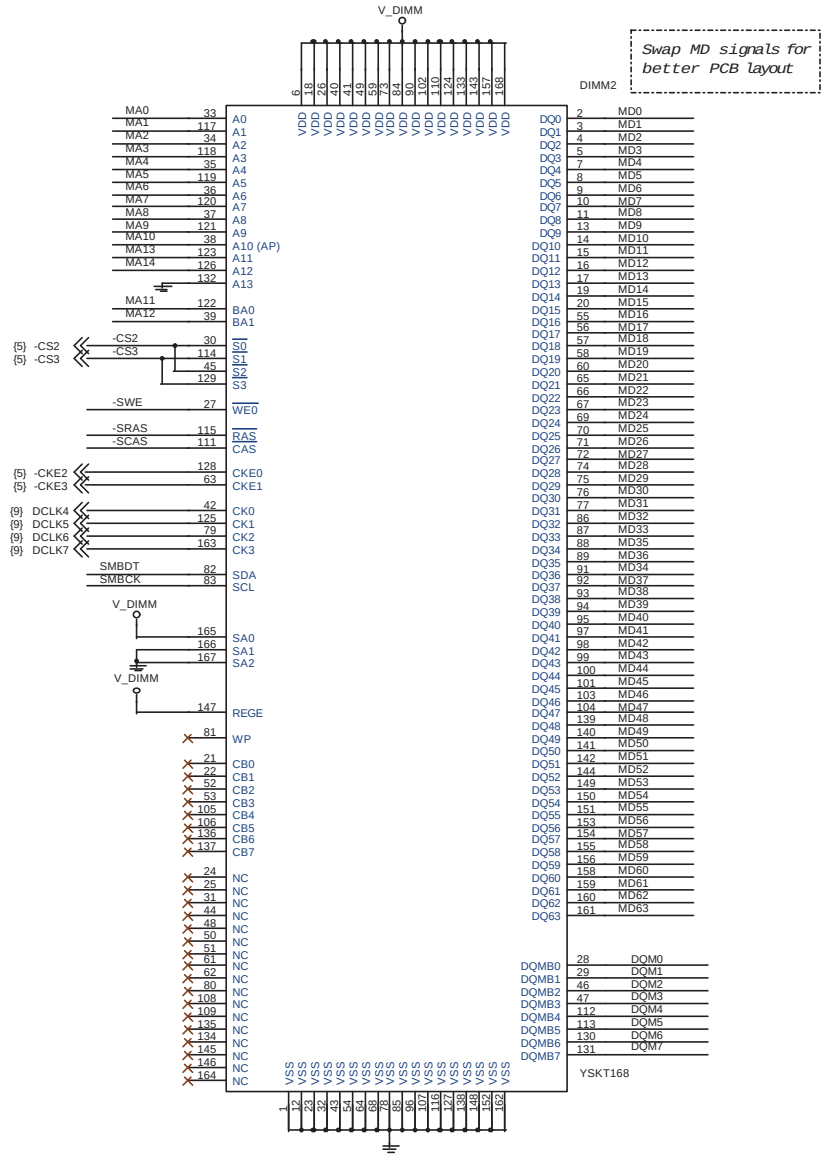
Title: CLOCK SYNTHESIZER		Rev: 100
Document Number: MS-6378		
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Friday, March 23, 2001	Sheet 9 of 28





Micro Star Restricted Secret

Title	SDRAM (DIMM1 AND DIMM2)	Rev
Document Number	MS-6378	100
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Friday, March 23, 2001	
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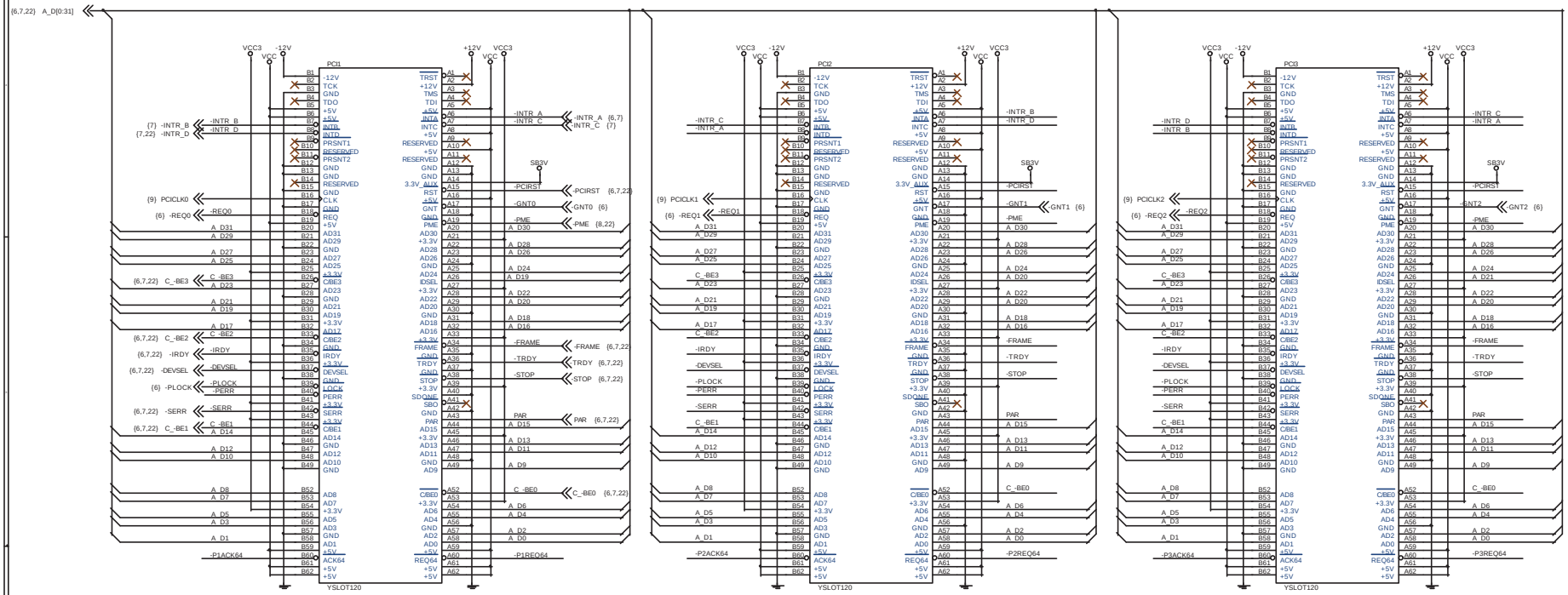
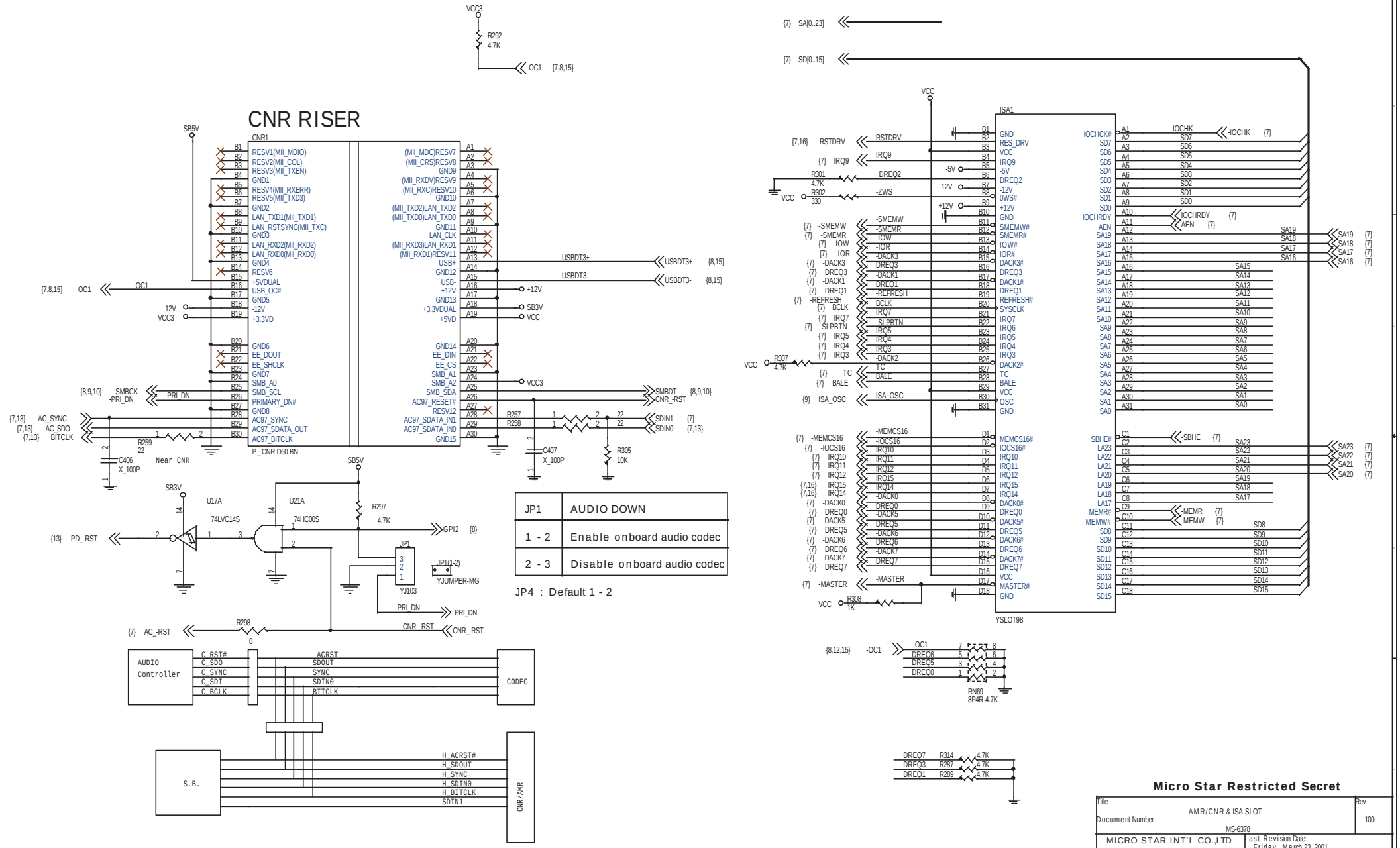


Micro Star Restricted Secret

Title	PCI1&2&3 SLOTS	Rev
Document Number	MS-6378	100
MICRO-STAR INT'L CO.,LTD.	Last Revision Date: Friday, March 23, 2001	
No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Sheet 11 of 28	

CNR RISER

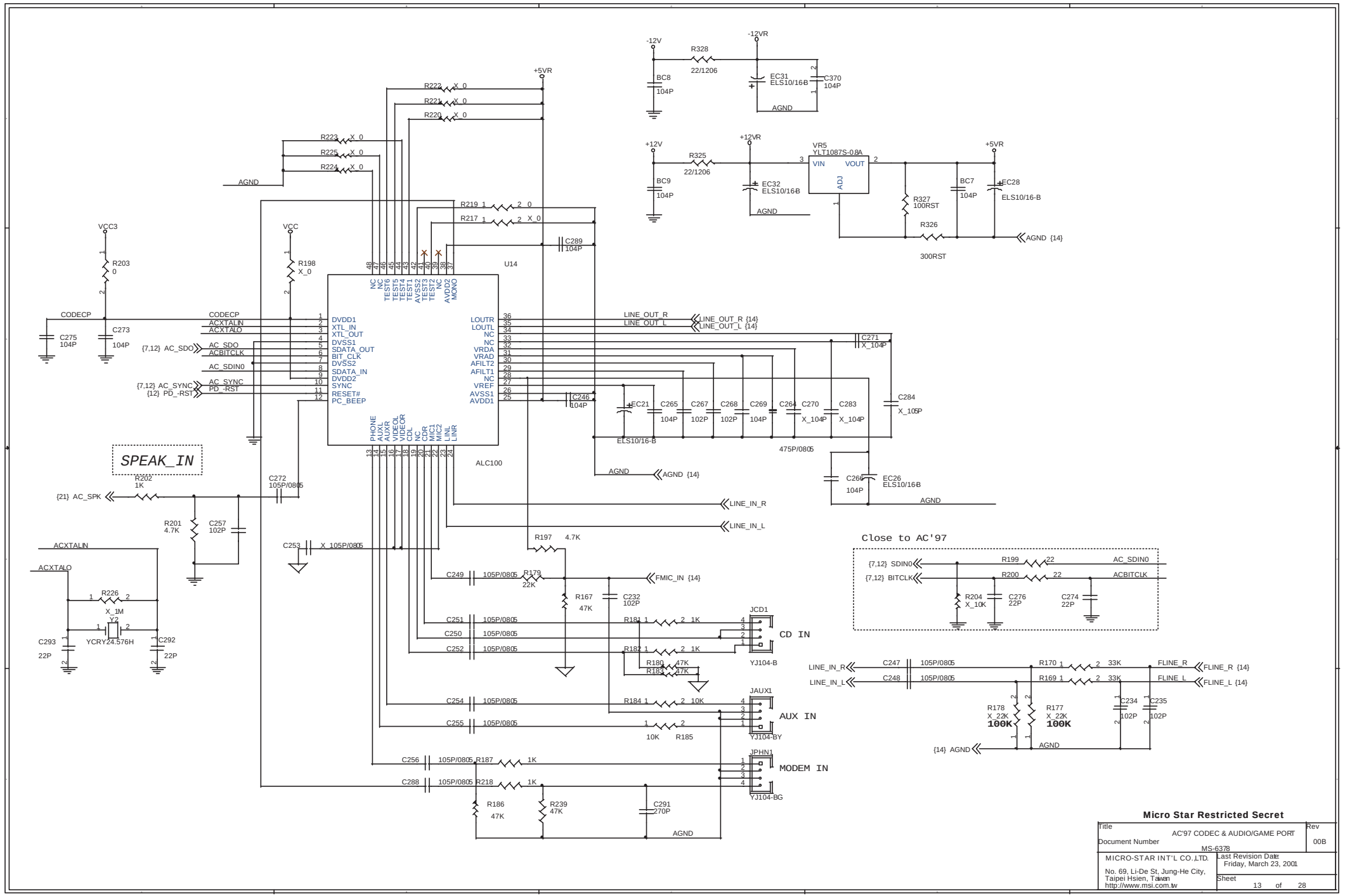


JP1	AUDIO DOWN
1 - 2	Enable onboard audio codec
2 - 3	Disable onboard audio codec

JP4 : Default 1 - 2

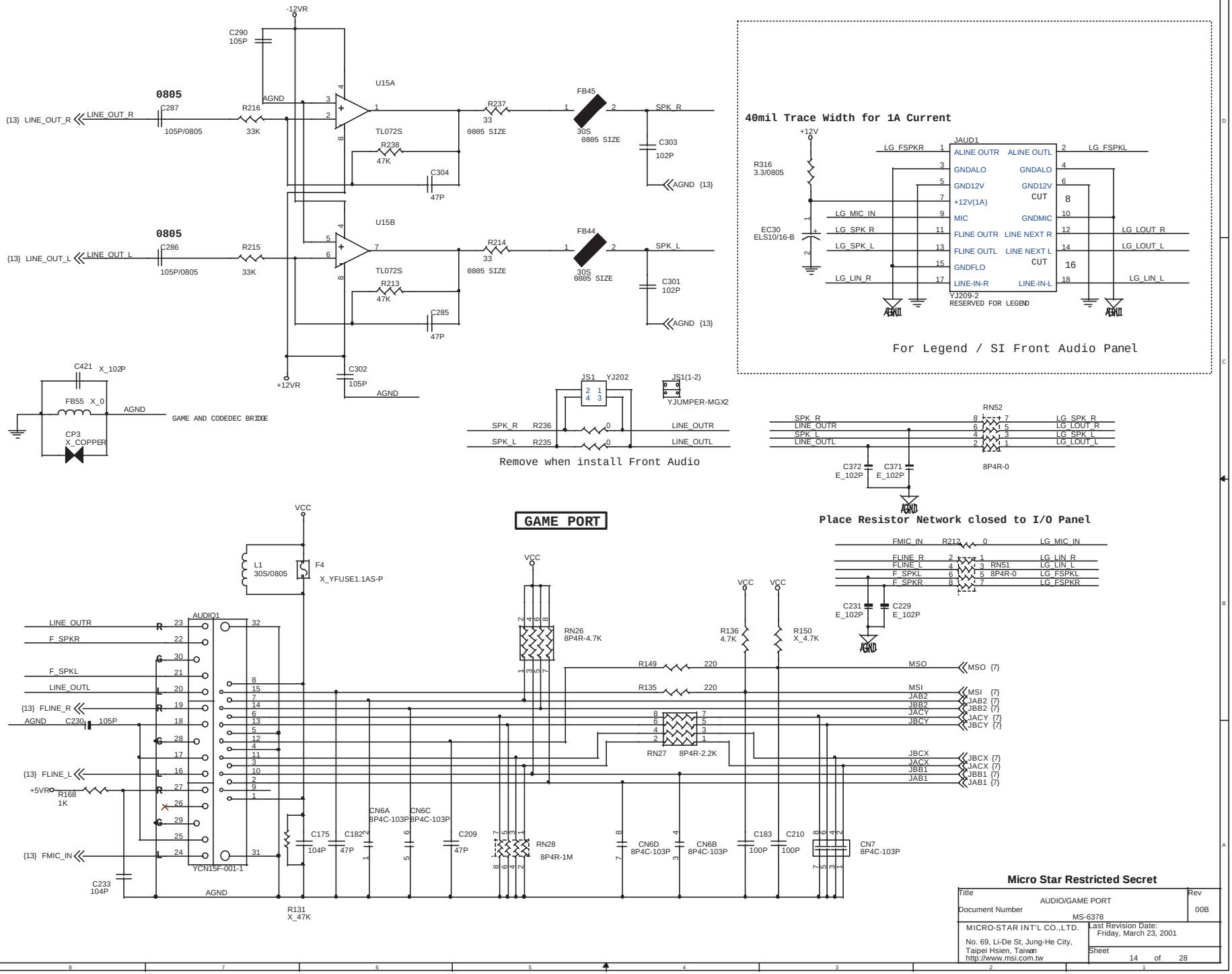
Micro Star Restricted Secret

Title	AMR/CNR & ISA SLOT	Rev
Document Number	MS-6378	100
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Friday, March 23, 2001	
	Sheet 12 of 28	



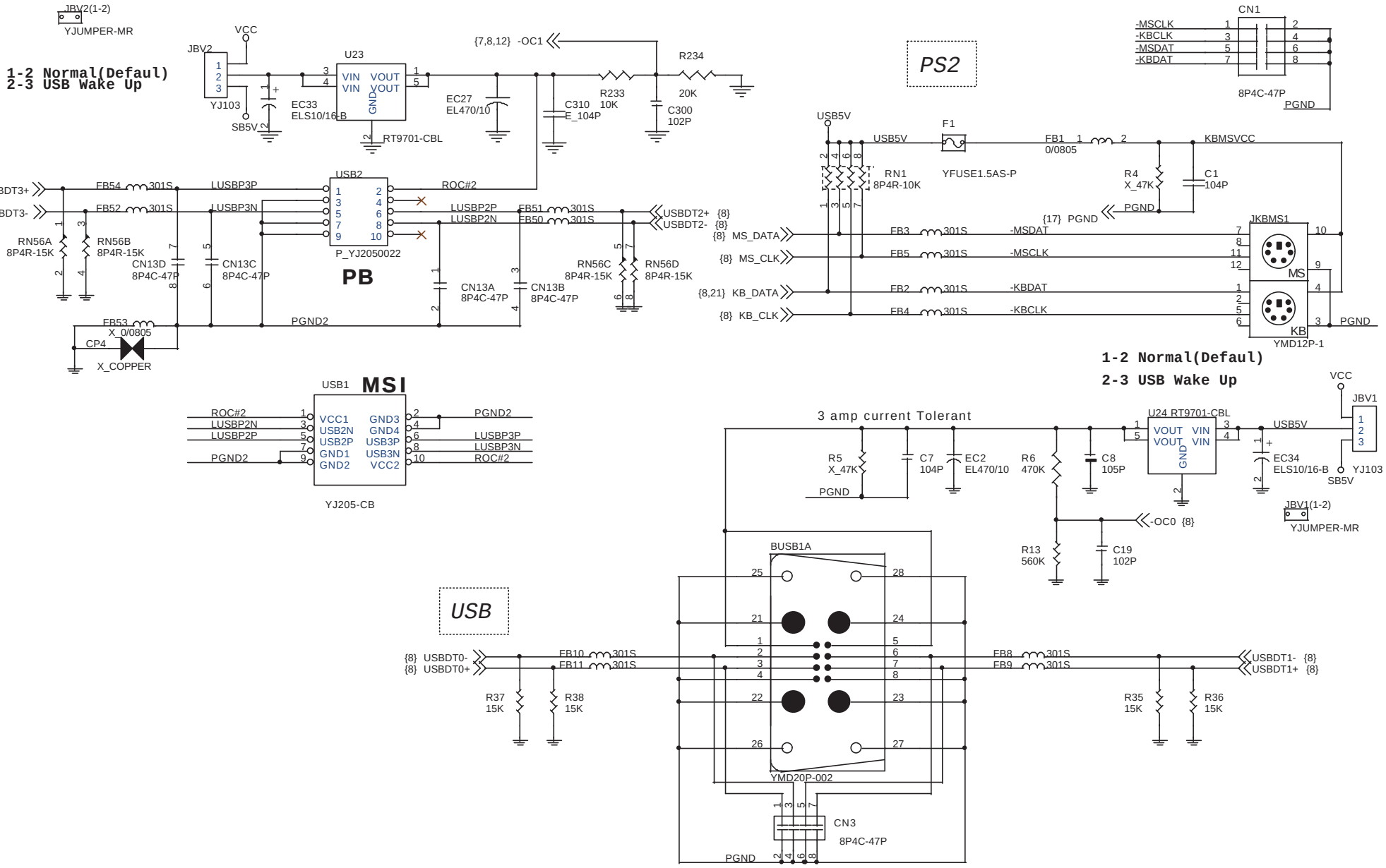
Micro Star Restricted Secret

Title	AC'97 CODEC & AUDIO/GAME PORT	Rev 00B
Document Number	MS-6378	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Friday, March 23, 2001	
	Sheet 13 of 28	



Micro Star Restricted Secret

Title	AUDIO/GAME PORT	Rev
Document Number	MS-6378	00B
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Friday, March 23, 2001	
	Sheet 14 of 28	


JBV2(1-2)
YJUMPER-MR
1-2 Normal(Defaul)
2-3 USB Wake Up
JBV2
YJ103
SB5V
VCC
U23
EC33
ELS10/16-B
RT9701-CBL
{7,8,12} -OC1
EC27
EL470/10
C310
E_104P
R233
10K
R234
20K
C300
102P
PS2
CN1
-MSCLK
-KBCLK
-MSDAT
-KBDAT
8P4C-47P
PGND
USB5V
F1
YFUSE1.5AS-P
FB1
0/0805
KBMSVCC
RN1
8P4R-10K
R4
X_47K
C1
104P
{17} PGND
JKBMS1
MS
KB
YMD12P-1
{8,12} USBDT3+
{8,12} USBDT3-
FB54 301S
FB52 301S
LUSBP3P
LUSBP3N
USB2
P_YJ2050022
ROC#2
LUSBP2P
LUSBP2N
FB51 301S
FB50 301S
USBDT2+ {8}
USBDT2- {8}
PB
RN56A
8P4R-15K
RN56B
8P4R-15K
CN13D
8P4C-47P
CN13C
8P4C-47P
CN13A
8P4C-47P
CN13B
8P4C-47P
RN56C
8P4R-15K
RN56D
8P4R-15K
FB53
X_0/0805
CP4
X_COPPER
PGND2
{8} MS_DATA
{8} MS_CLK
{8,21} KB_DATA
{8} KB_CLK
FB3 301S
FB5 301S
FB2 301S
FB4 301S
-MSDAT
-MSCLK
-KBDAT
-KBCLK
1-2 Normal(Defaul)
2-3 USB Wake Up
MSI
USB1
ROC#2
LUSBP2N
LUSBP2P
PGND2
VCC1
USB2N
USB2P
GND1
GND2
GND3
GND4
USB3P
USB3N
VCC2
PGND2
LUSBP3P
LUSBP3N
ROC#2
YJ205-CB
3 amp current Tolerant
U24 RT9701-CBL
R5
X_47K
C7
104P
EC2
EL470/10
R6
470K
C8
105P
R13
560K
C19
102P
-OC0 {8}
USB5V
EC34
ELS10/16-B
YJ103
SB5V
JBV1
JBV1(1-2)
YJUMPER-MR
USB
BUSB1A
YMD20P-002
CN3
8P4C-47P
{8} USBDT0-
{8} USBDT0+
FB10 301S
FB11 301S
FB8 301S
FB9 301S
USBDT1- {8}
USBDT1+ {8}
R37
15K
R38
15K
R35
15K
R36
15K
Micro Star Restricted Secret
Title
KB/MOUSE & USB CONNECTORS
Rev
00B
Document Number
MS-6378
MICRO-STAR INT'L CO.,LTD.
No. 69, Li-De St, Jung-He City,
Taipei Hsien, Taiwan
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Last Revision Date:
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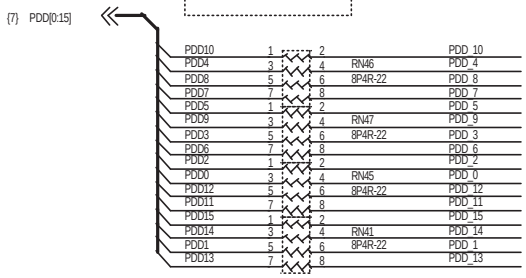
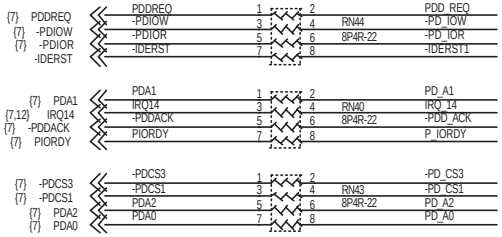
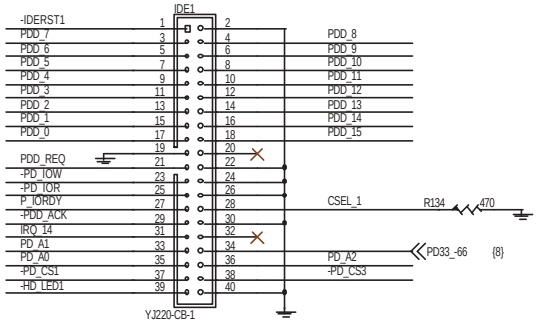
PRIMARY

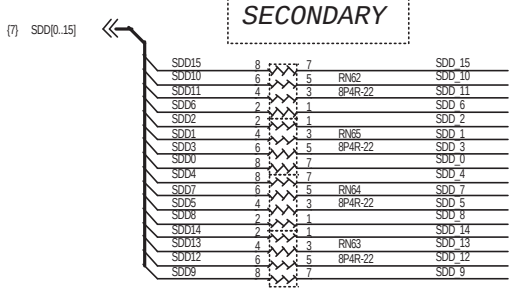


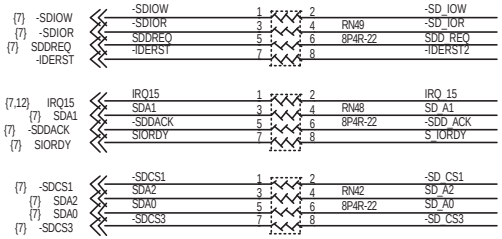


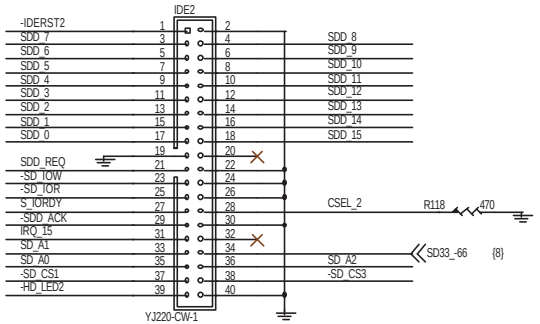


These resistor should be placed near South Bridge <1"

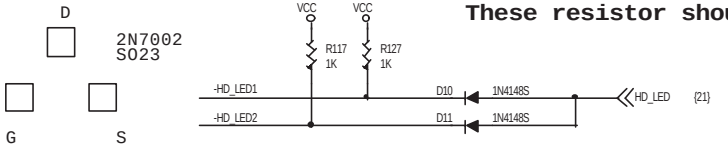
SECONDARY

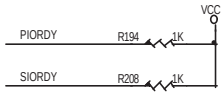




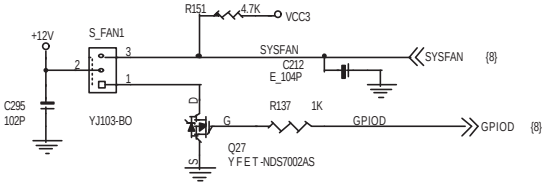


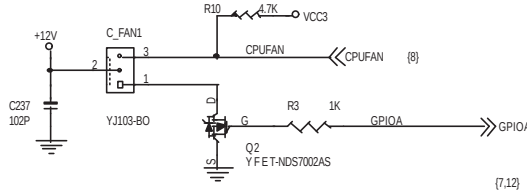
These resistor should be placed near South Bridge <1"



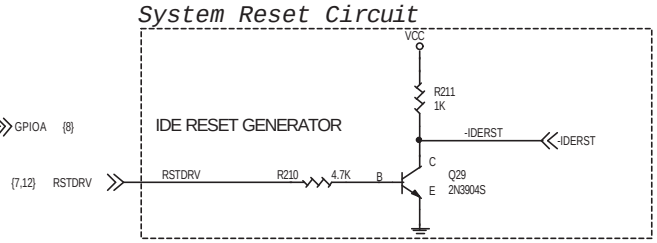


FAN





System Reset Circuit



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Title	IDE1 & IDE2 CON NECTORS	Rev 00B
Document Number	MS-6378	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Friday, March 23, 2001	
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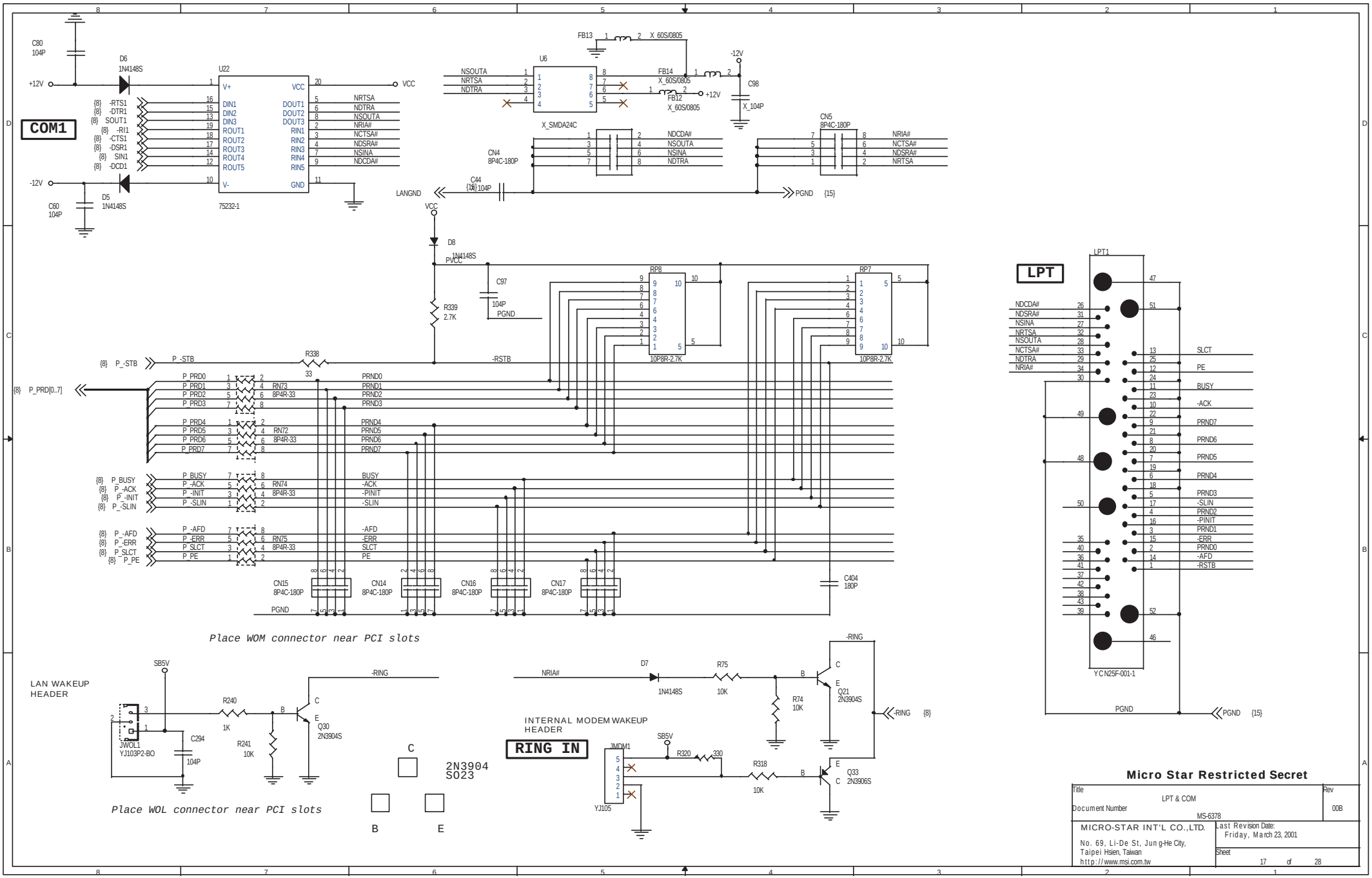
COM1
U22
75232-1
U6
LPT
LPT1
YCN25F-001-1
RP8
RP7
10P8R-2.7K
CN4
CN5
CN14
CN15
CN16
CN17
Place WOM connector near PCI slots
LAN WAKEUP HEADER
JWOL1
YJ103P2-BO
Place WOL connector near PCI slots
INTERNAL MODEM WAKEUP HEADER
RING IN
1MDM1
YJ105
2N3904
S023
B
C
E
Micro Star Restricted Secret
Title
LPT & COM
Document Number
MS-6378
Rev
00B
MICRO-STAR INT'L CO.,LTD.
No. 69, Li-De St, Jung-He City,
Taipei Hsien, Taiwan
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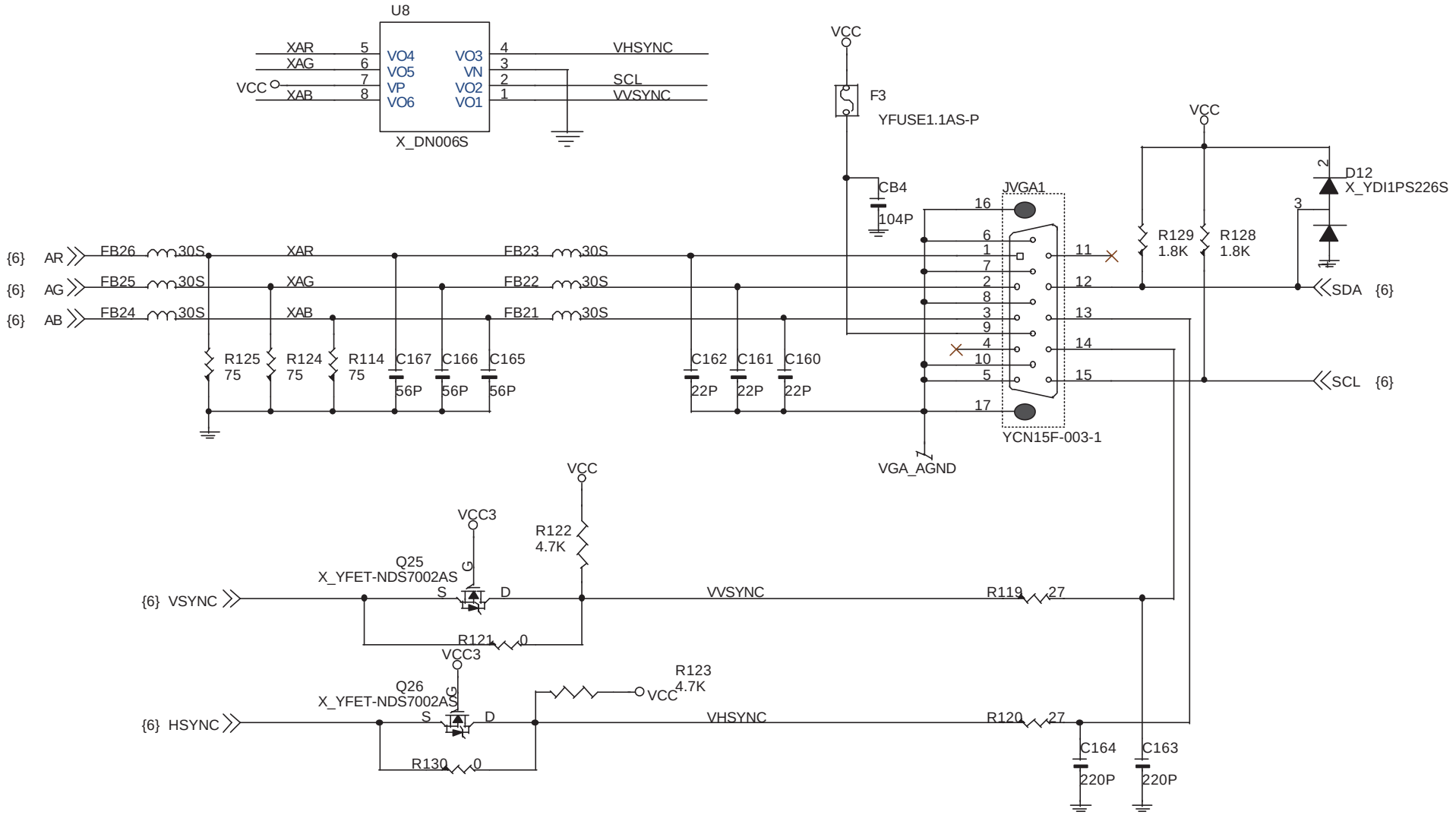

Trace Note:
1.The 5V traces should be 20 mils to VGA/DFP

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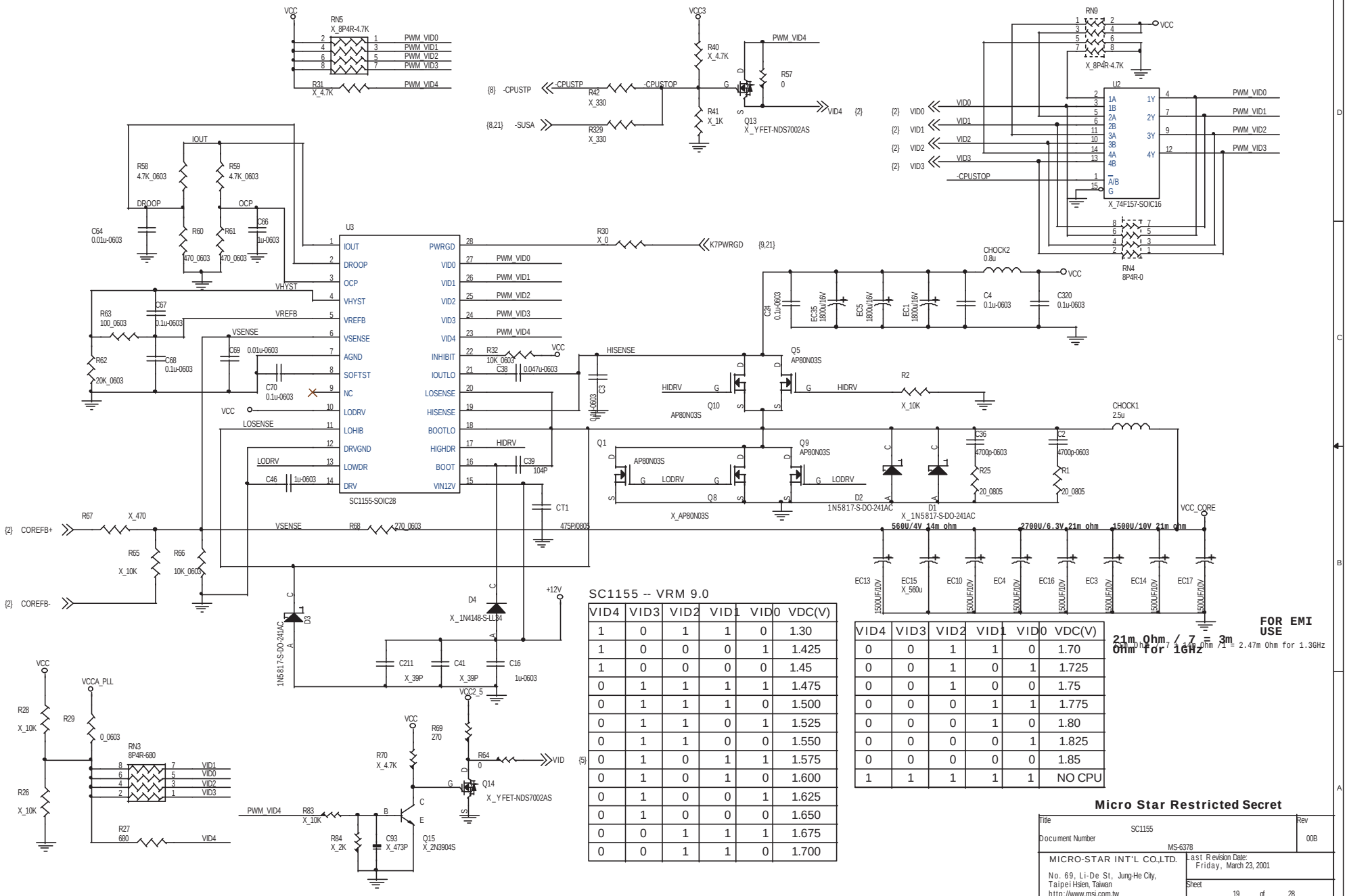
Title: VGA Connector	Rev: 00B
Document Number: MS-6378	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Friday, March 23, 2001 Sheet 18 of 28



SC1155 -- VRM 9.0

VID4	VID3	VID2	VID1	VID0	VDC(V)
1	0	1	1	0	1.30
1	0	0	0	1	1.425
1	0	0	0	0	1.45
0	1	1	1	1	1.475
0	1	1	1	0	1.500
0	1	1	0	1	1.525
0	1	1	0	0	1.550
0	1	0	1	1	1.575
0	1	0	1	0	1.600
0	1	0	0	1	1.625
0	1	0	0	0	1.650
0	0	1	1	1	1.675
0	0	1	1	0	1.700

VID4	VID3	VID2	VID1	VID0	VDC(V)
0	0	1	1	0	1.70
0	0	1	0	1	1.725
0	0	1	0	0	1.75
0	0	0	1	1	1.775
0	0	0	1	0	1.80
0	0	0	0	1	1.825
0	0	0	0	0	1.85
1	1	1	1	1	NO CPU

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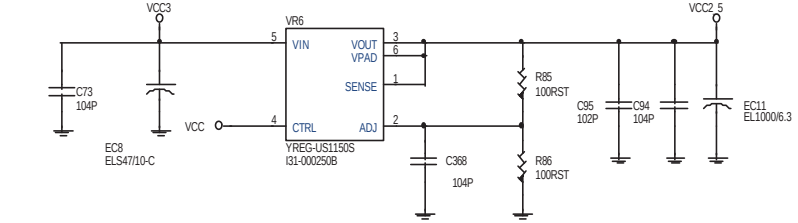
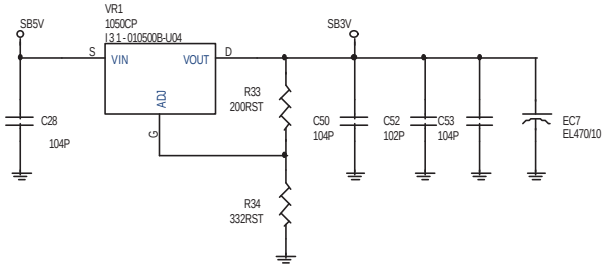
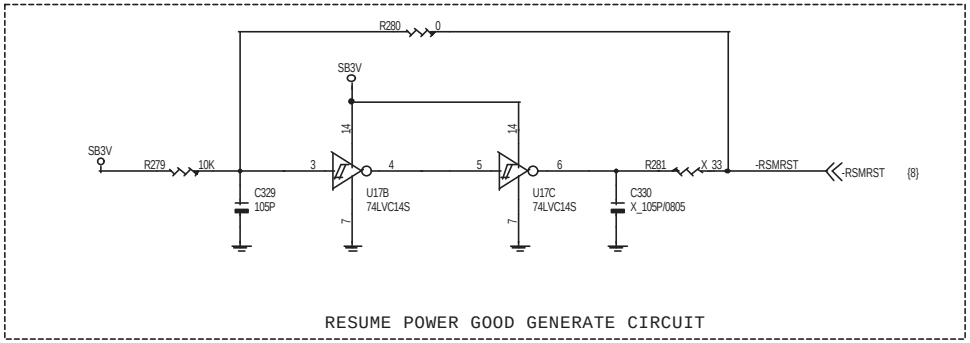
Title: SC1155		Rev: 00B
Document Number: MS-6378		
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Friday, March 23, 2001	Sheet 19 of 28

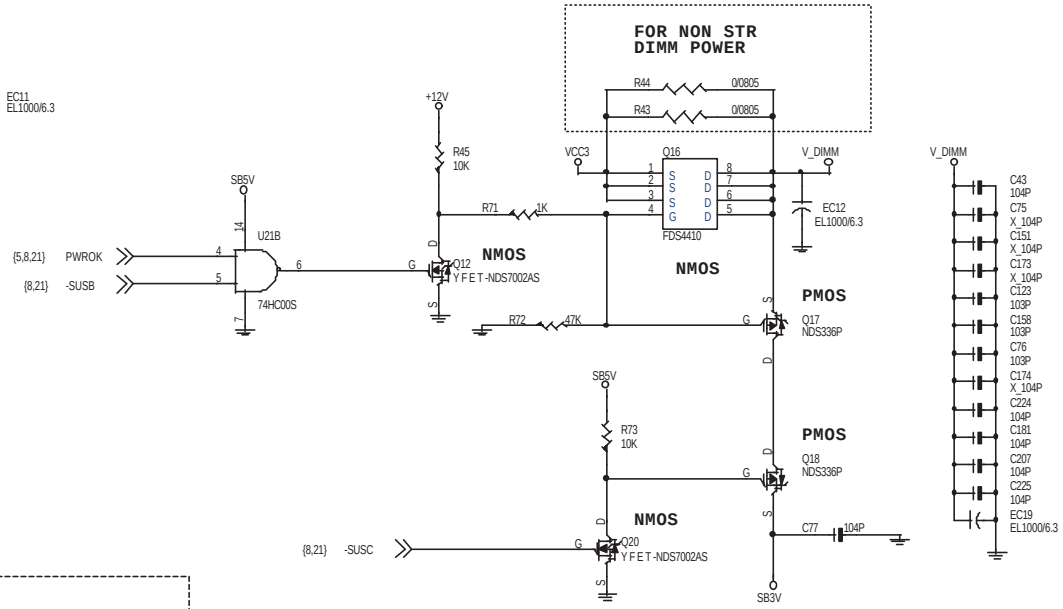




UP TO 60MILS TRACE WIDTH TO PCI SLOT TO MINIMUM VOLTAGE DROOP



RESUME POWER GOOD GENERATE CIRCUIT



ACPI S3 (SUSPEND TO RAM) POWER CIRCUIT

2.5V Supply to VCC25 power balls of NB (locate near North Bridge)

Micro Star Restricted Secret

Title: ACPI STR POWER		Rev: 00B
Document Number: MS-6378		
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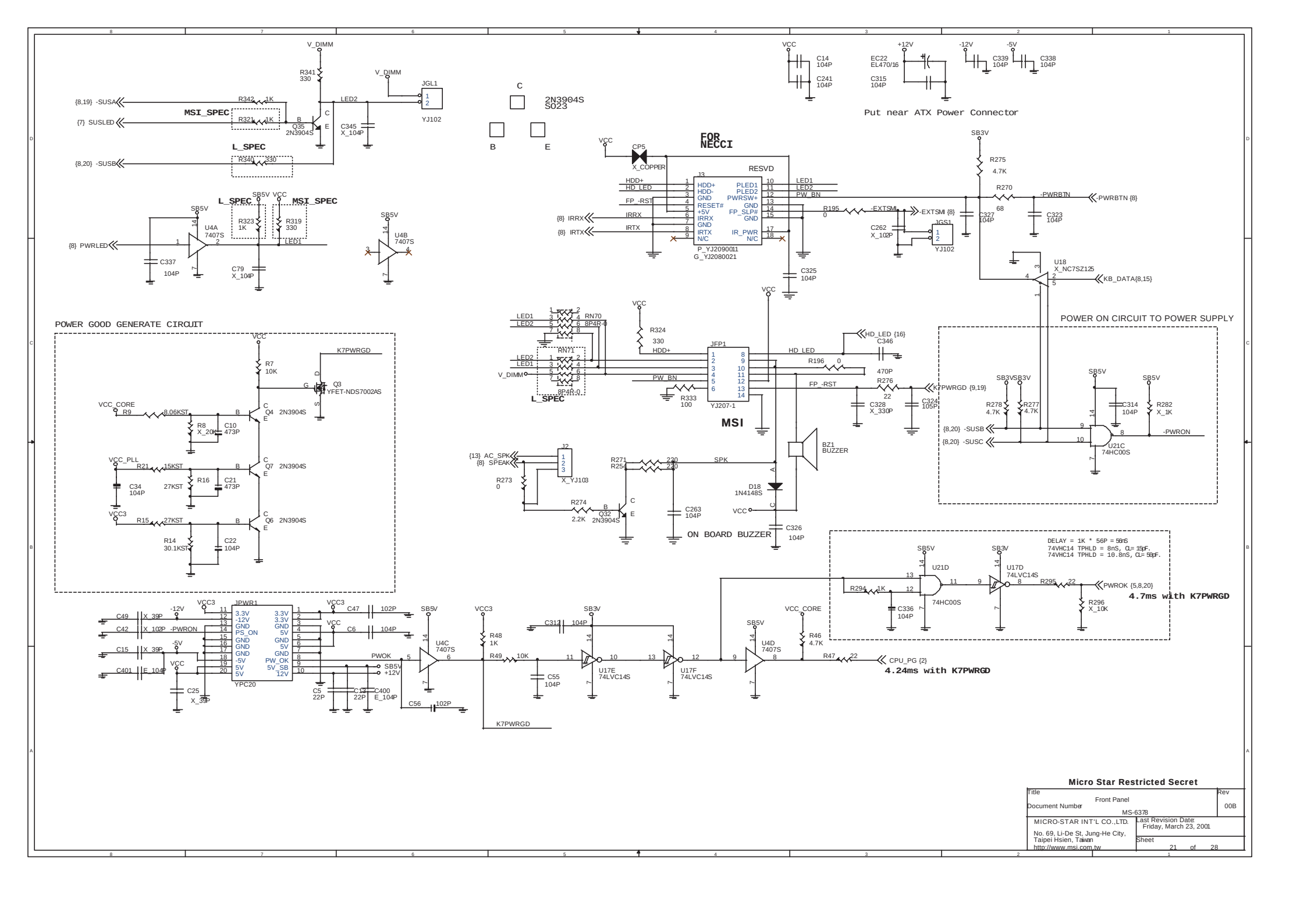
V_DIMM
R341 330
V_DIMM
JGL1
{8,19} -SUSA
R342 1K
LED2
MSI_SPEC
{7} SUSLED
R321 1K
Q35 2N3904S
C345 X_104P
YJ102
L_SPEC
{8,20} -SUSB
R340 330
SB5V VCC MSI_SPEC
L_SPEC
SB5V
R323 1K
R319 330
U4A 7407S
LED1
{8} PWRLED
C337 104P
C79 X_104P
SB5V
U4B 7407S
C
2N3904S
S023
B
E
Put near ATX Power Connector
VCC
C14 104P
C241 104P
+12V
EC22 EL470/16
C315 104P
-12V
C339 104P
-5V
C338 104P
FOR NECCI
VCC
CP5
X_COPPER
RESVD
J3
HDD+
HD_LED
FP_-RST
{8} IRRX
IRRX
{8} IRTX
IRTX
HDD+
HDD-
GND
RESET#
+5V
IRRX
GND
IRTX
N/C
PLED1
PLED2
PWRSW+
GND
FP_SLP#
GND
IR_PWR
N/C
LED1
LED2
PW_BN
P_YJ2090011
G_YJ2080021
R195 0
-EXTSMI
-EXTSMI {8}
C262 X_102P
JGS1
YJ102
SB3V
R275 4.7K
R270 68
-PWRBTN
-PWRBTN {8}
C327 104P
C323 104P
C325 104P
U18 X_NC7SZ125
KB_DATA{8,15}
POWER ON CIRCUIT TO POWER SUPPLY
POWER GOOD GENERATE CIRCUIT
VCC
R7 10K
K7PWRGD
Q3 YFET-NDS7002AS
VCC_CORE
R9 8.06KST
Q4 2N3904S
R8 X_20K
C10 473P
VCC_PLL
R21 15KST
Q7 2N3904S
C34 104P
27KST
R16
C21 473P
VCC3
R15 27KST
Q6 2N3904S
R14 30.1KST
C22 104P
VCC
RN70 8P4R-0
LED1
LED2
RN71 8P4R-0
V_DIMM
R324 330
HDD+
PW_BN
R333 100
JFP1
YJ207-1
L_SPEC
MSI
HD_LED {16}
C346 470P
HD_LED
R196 0
FP_-RST
R276 22
C328 X_330P
C324 105P
K7PWRGD {9,19}
SB3V SB3V
R278 4.7K
R277 4.7K
SB5V SB5V
C314 104P
R282 X_1K
{8,20} -SUSB
{8,20} -SUSC
U21C 74HC00S
-PWRON
{13} AC_SPK
{8} SPEAK
J2
X_YJ103
R273 0
R271 220
R254 220
SPK
BZ1 BUZZER
D18 1N4148S
R274 2.2K
Q32 2N3904S
C263 104P
ON BOARD BUZZER
C326 104P
DELAY = 1K * 56P = 56nS
74VHC14 TPHLD = 8nS, CL= 15pF.
74VHC14 TPHLD = 10.8nS, CL= 50pF.
SB5V SB3V
U21D
74HC00S
U17D 74LVC14S
R294 1K
R295 22
PWROK {5,8,20}
4.7ms with K7PWRGD
C336 104P
R296 X_10K
JPWR1
YPC20
-12V
-PWRON
-5V
VCC
C49 X_39P
C42 X_102P
C15 X_39P
C401 E_104P
C25 X_39P
VCC3
C47 102P
C6 104P
C5 22P
C12 22P
C400 E_104P
PWOK
SB5V
+12V
U4C 7407S
C56 102P
K7PWRGD
R48 1K
R49 10K
C55 104P
C312 104P
U17E 74LVC14S
U17F 74LVC14S
U4D 7407S
VCC_CORE
R46 4.7K
R47 22
CPU_PG {2}
4.24ms with K7PWRGD
Micro Star Restricted Secret
Title
Front Panel
Rev
00B
Document Number
MS-6378
MICRO-STAR INT'L CO.,LTD.
No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan
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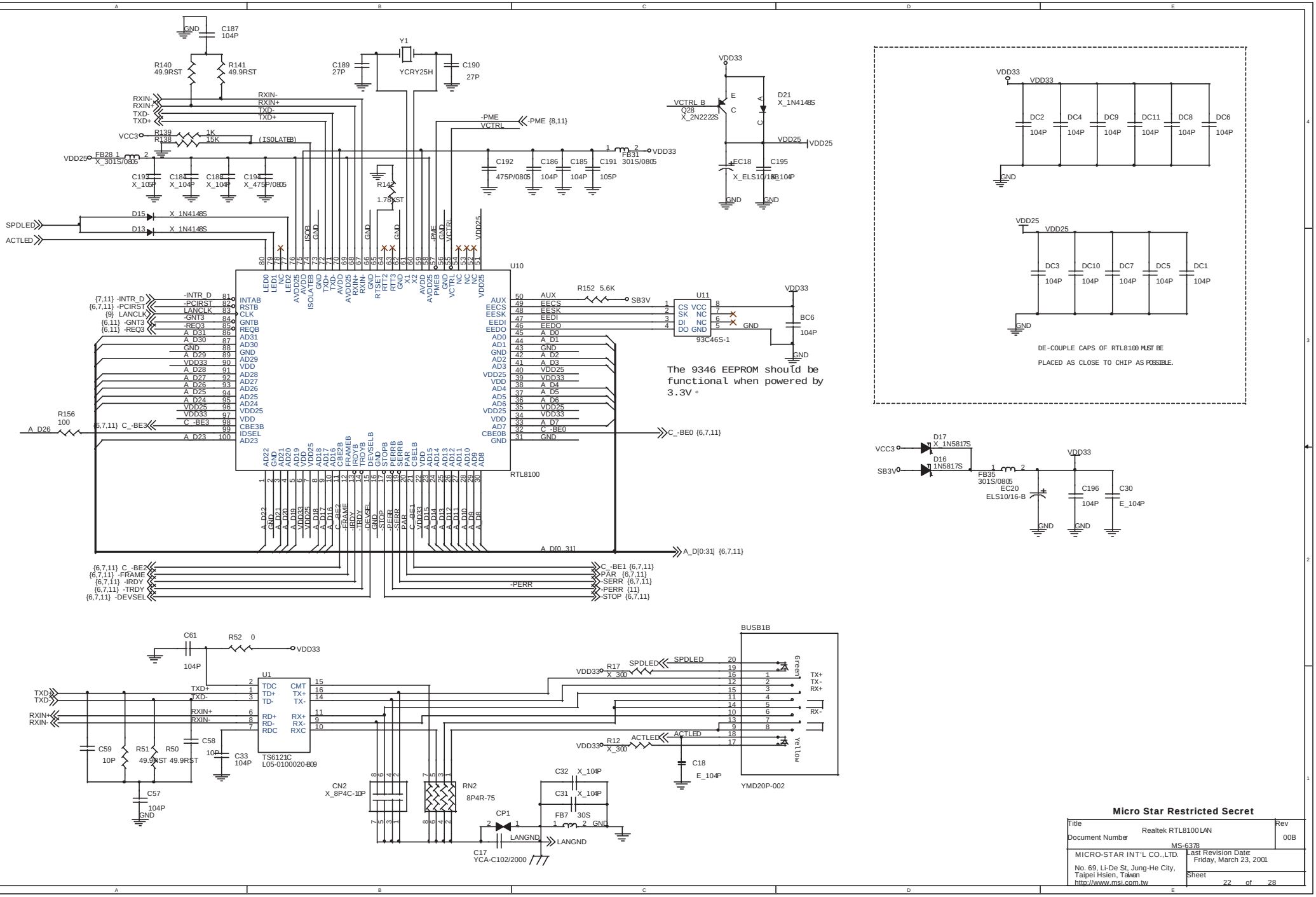
U10
RTL8100
U11
93C46S-1
U1
TS6121C
L05-0100020-B09
BUSB1B
YMD20P-002
CN2
X_8P4C-10P
RN2
8P4R-75
CP1
C17
YCA-C102/2000
Y1
YCRY25H
The 9346 EEPROM should be functional when powered by 3.3V。
DE-COUPLE CAPS OF RTL8100 MUST BE
PLACED AS CLOSE TO CHIP AS POSSIBLE.
Micro Star Restricted Secret
Realtek RTL8100 LAN
MS-6378
MICRO-STAR INT'L CO.,LTD.
No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan
http://www.msi.com.tw
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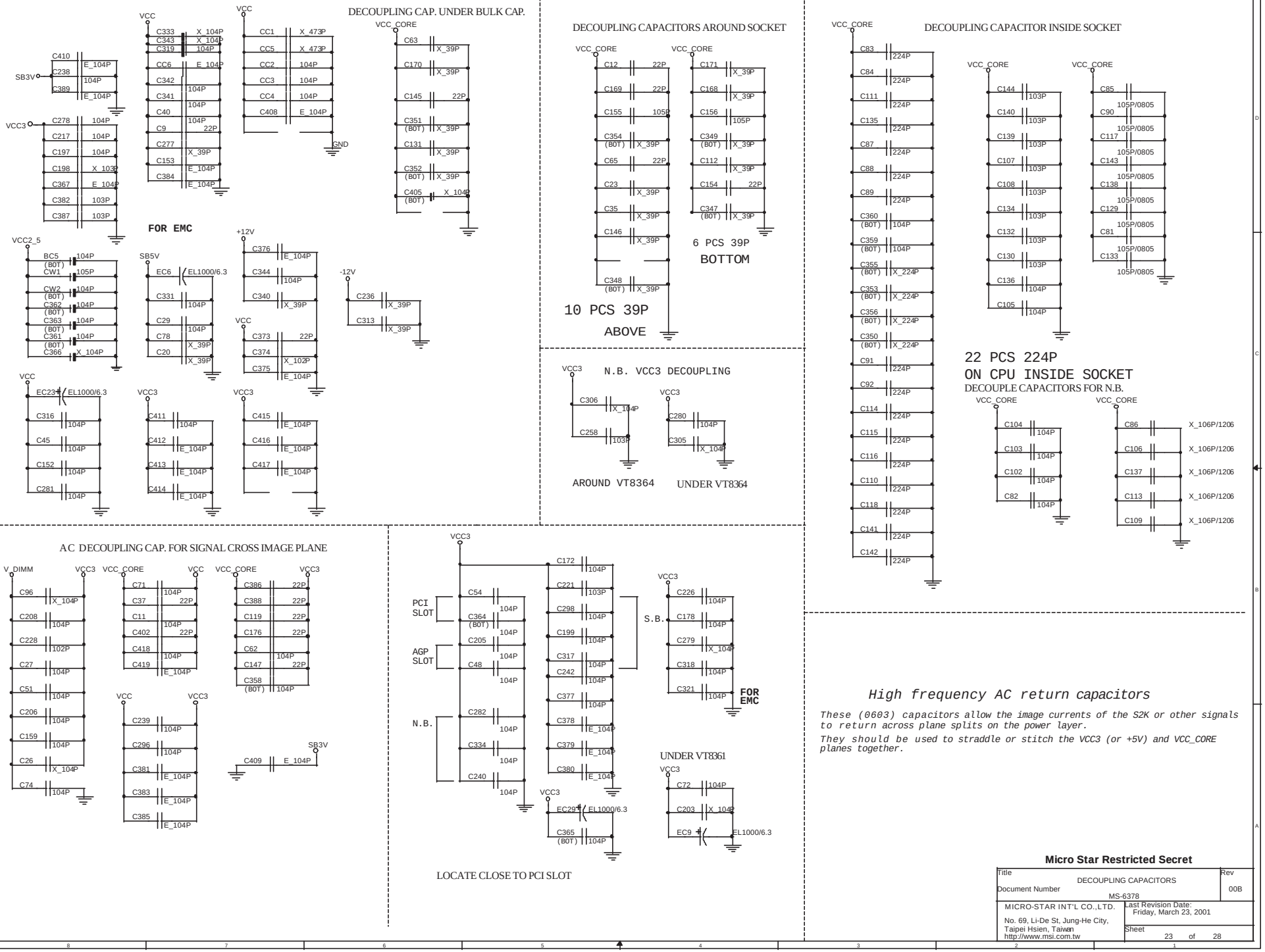
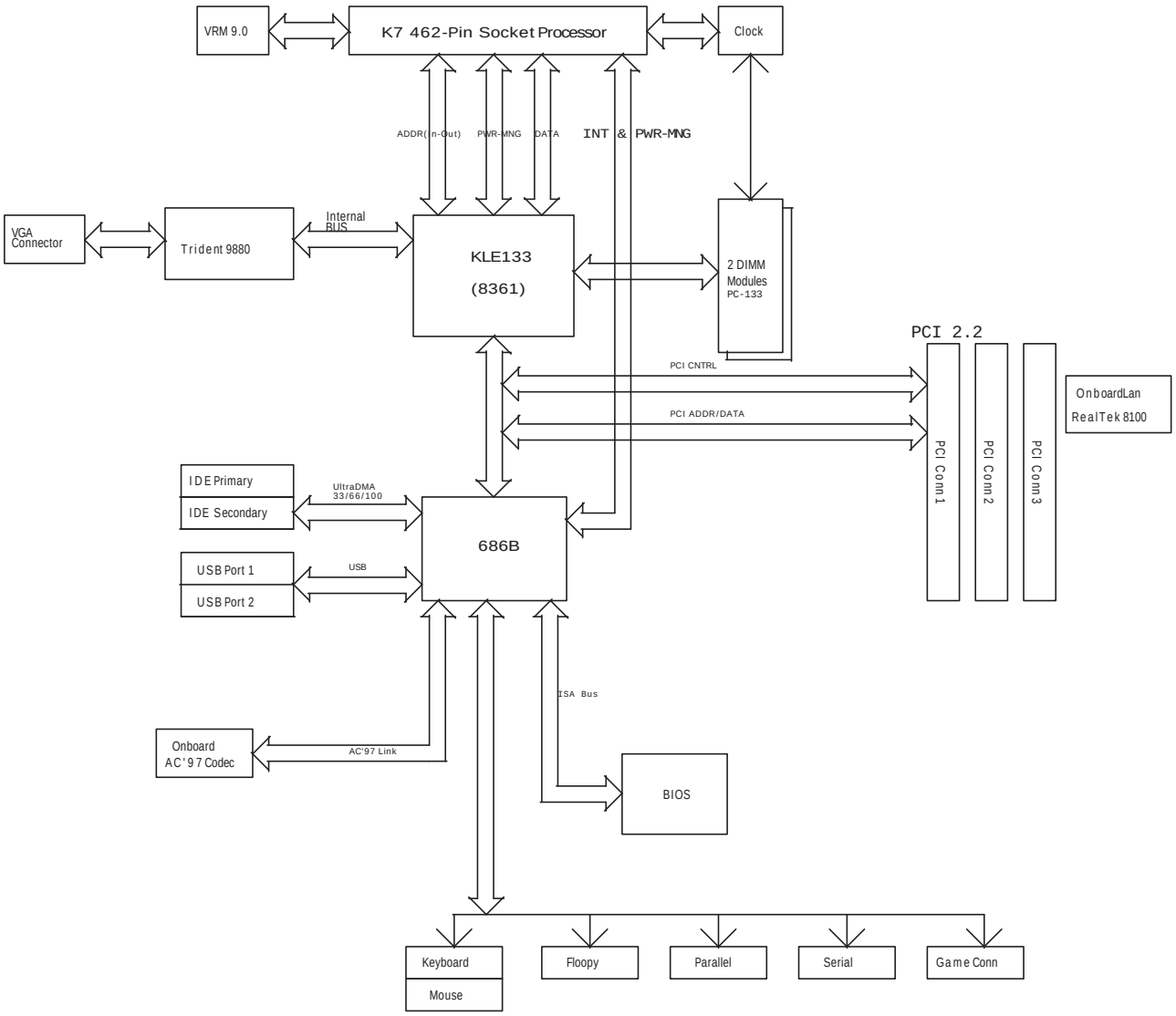


Micro Star Restricted Secret

Title	DECOUPLING CAPACITORS	Rev 00B
Document Number	MS-6378	
MICRO-STAR INT'L CO.,LTD.	Last Revision Date: Friday, March 23, 2001	
No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Sheet 23 of 28	

Block Diagram



Micro Star Restricted Secret

Title	BLOCK DIAGRAM	Rev 100
Document Number	MS-6378	
MICRO-STAR INT'L CO.,LTD.	Last Revision Date: Friday, February 23, 2001	
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-DACK5

General Purpose I/O Spec.

VIA686A GPIO Pin	Pin Out	Function	Default
GPIO 0	T8	PWRLED	
GPIO 1	V9	-SUSA	
GPIO 2	W9	-SUSB	
GPIO 3	V10	-SUSST	
GPIO 4	Y12	-CPUSTP	
GPIO 5	V12	GPOC(BIOS Protect)	
GPIO 7	T7	-SLP	
GPIO 8	T14	GPOA(CpuFanControl)	
GPIO 9	U12	SYSFAN	
GPIO 10	V14	Chassis Instruction	
GPIO 11	U8	GPIOD(SysFanControl)	
GPIO 12	T5	Suspend Led	
GPIO 13	U5	-SOE	
GPIO 14	E12	IRTX	
GPIO 15	D12	IRRX	
GPIO 16	L2	-DACK0	
GPIO 17	E1	-DACK1	
GPIO 18	D2	-DACK3	
GPIO 19	L4	-DACK5	
GPIO 20	M3	-DACK6	
GPIO 21	N2	-DACK7	
GPIO 22	Y15	JAY	
GPIO 23	V15	JAX	
GPIO 24	H3	-USBOC1	
GPIO 25	G5	-USBOC0	

H/W Monitor

GPIO Pin	Pin Out	Function
VSENS1	U13	Voltage Sense Vcore
VSENS2	V13	Voltage Sense 2.5V
VSENS3	W14	Voltage Sense 5V
VSENS4	Y14	Voltage Sense 12V
VREF	T13	Voltage Reference
TSENS1	W13	CPU Temperature Sense
TSENS2	Y13	Syetem Temperature Sense
FAN1	T12	CPU FAN Speed Monitor
FAN2	U12	Power FAN Speed Monitor

DEVICE	INT Pin	IDSEL	PCI REQ/GNT
PCI Slot 1	INTA#	AD19	REQ#0/GNT#0
PCI Slot 2	INTB#	AD20	REQ#1/GNT#1
PCI Slot 3	INTC#	AD21	REQ#2/GNT#2
RTL8100 LAN	INTD#	AD26	REQ#3/GNT#3
VIA686A		AD18	PREQ# /PGNT#
VT8361	INTA#		

Power State	-RSMRST	-SUSST	-SUSA	-SUSB	-SUSC
On	1	1	1	1	1
POS	1	1	0	1	1
STR	1	1	0	0	1
STD/ Soft-off	1	1	0	0	0
Delay 4 Sec.	1	0	0	0	0
Mechanical off	0	1	0	0	0

0B Revision History (Changes from Rev 0A)

7	To fix schematics Error on BIOS Data Siganls.
12	Remove AMR Slot.
13	Change Codec Power for Cost Down.
20	Change VCC2_5 Power from 1084DS to US1150.
3	Change RN20 & RN21 Power form VCCA_PLL to VCC3.
5	Add C369 on VSUS Signals.
17	U5 Siganls Error Fix.
19	Change Output Capacitor from 2700uF/6.3V to 1500uF/10V for Cost Down.

0C Revision History (Changes from Rev 0B)

15	USB1 PinOut Error Fix. Change USB Power from Fuse to Hi-Side MOS(U23&U24). Add Capacitor on USB Power Input.
22	Add a Diode D21 between VDD33 and VDD25
17	JWOL1 Connector Siganls Error Fix.(Swap Pin.1&3.)
21	Change R322 & R319 Power from SB3V to SB5V.
8	Add a Resistor between SB -SUSST and NB -NBSUSST. Add a Pull-Up Resistor to SB3V and VCC3 on -NBSUSST.
8	R230 Change Power from VCC3 to VBAT.
6	Remove FB38,FB39,C215,CM10.
9	Remove R192,EC25 and U13.27 direct connector to VCCCLK. Remove U12,R157 and R158.
5	Change Strap Resistor for VIA Recommend.
17	Change U7 to Resistor and Capacitor Network.

1.0 Revision History (Changes from Rev 0C)

7	Change XBUS Buffer from 16LCX245 SSOP48 to 74LV245 SSOP20.(Cost Down)
21	Change LED Control Schematics.
19	Add Input Capacitor for future reserved.
8	Change D18,D19 from 1N5817S to 1N4148S aviod leakage current.

Title	History I	Rev
Document Number	MS-6378	00B
MICRO-STAR INT'L CO.,LTD.	Last Revision Date: Thursday, March 22, 2001	
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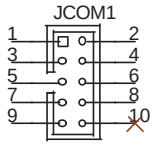
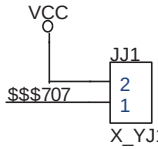
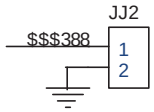
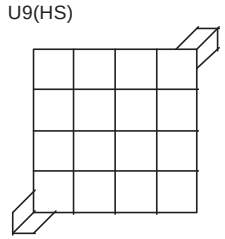
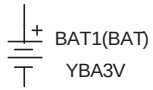
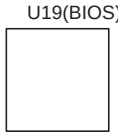


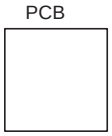






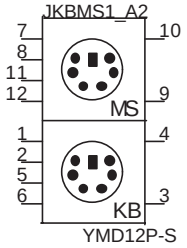


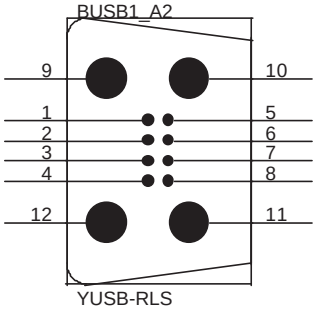




For A2 Customer Requirement Component:

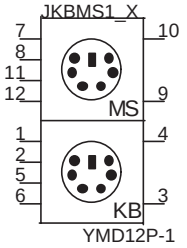
For A2 : N56-12F0041-F02.

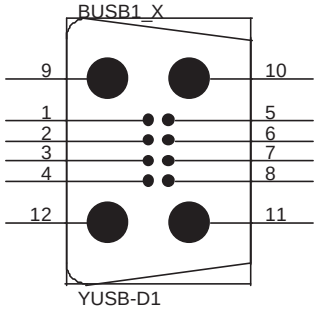




For A2 : N53-08M0031-F02.

For msi Standard Component:





Micro Star Restricted Secret

Title: Packing	Rev: 00B
Document Number: MS-6378	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Friday, March 23, 2001 Sheet 27 of 28

Trace type	Trace width(mils)	Spacing(mils)
singal	5	10
clock	X	X
power	30	20
USB clock as short as possible or less than 9"		

Clock trace	Desired length	Allowable range	Singals	
Clockgen-->CPU	Lcpu	1"~9"	CPUCLK,-CPUCLK	**20:5:5:5:20**
Clockgen-->NB	Lcpu+2"	1"~9"	HCLK	**6:18**
Clockgen-->SDCLK[0:7]	Lsd	1"~4"	DCLK[0:7]	**6:18**
Clockgen-->NB(DCLKI)	Lsd+3"	5"~8"	DCLKI	**6:18**
NB-->Clockgen(DCLKO)	Ldout	1"~8"	DCLKO	**6:18**
Clockgen-->NB(GUICLK)	Lgout	1"~8"	GUICLK	**10:20**
				6:18
Clockgen-->VT836X(NB)	Lpci+3"	4"~15"	NPCLK	**6:18**
Clockgen-->SB	Lpci+3"	4"~15"	SPCLK	**6:18**
Clockgen-->PCI1	Lpci	1"~12"	PCICLK0	**6:18**
Clockgen-->PCI2	Lpci	1"~12"	PCICLK1	**6:18**
Clockgen-->PCI3	Lpci	1"~12"	PCICLK2	**6:18**
Clockgen-->LANCLK	Lpci	1"~12"	LANCLK	**6:18**

Signals	Desired length	Allowable range	Allowable range
MA[0:14]	L2	2"~4"	
MD[0:63]	L2	2"~4"	
-CAS[0:7]	L2	2"~4"	
-SWE	L2	2"~4"	
-SRAS	L2	2"~4"	
-SCAS	L2	2"~4"	
-RAS[0:1]	L2	2"~4"	
-RAS[2:3]	L2		2"~4"
-CKE[0:1]	L3	2"~4.5"	
-CKE[2:3]	L3		2"~4.5"

LAN TX/RX Differential Pair Signals

GuideLine:

1.Trace Width 8mil,Spacing between signals 10mil,Minimum separation between TX/RX 40mils.
2.TX Pair Terminal Resistors closed to Transformer,RX Pair Terminal Resistors closed to Chipset.

USB Differential Pair Signals

GuideLine:

1.Trace Width 8mil,Spacing between signals 12mil,Minimum separation between TX/RX 20mils.
2.Differential Pair Trace Length within +/- 50mil.

Socket-A S2K Clock Forwarded Singal Groups

Guideline:

1.The singal trace mismatch should be less than 100 mils between longest one and shortest one within the same group.

2.5 mil trace width.

3.15 mil minimum clearance to other signals at least.(20 mil recommended)

4.Maintain 50 mil minimum clearance to its own serpentine segment.

5.Pull-up resistors must be kept with 1" of the VT836X chip

Group Name	Signals in Group	Clocks for Group	Allowable range
Data 0	-SDATA[0:15]	-DICLK0,-DOCLK0	0.01"~6"
Data 1	-SDATA[16:31]	-DICLK1,-DOCLK1	0.01"~6"
Data 2	-SDATA[32:47]	-DICLK2,-DOCLK2	0.01"~6"
Data 3	-SDATA[48:63]	-DICLK3,-DOCLK3	0.01"~6"
Address IN	-AIN[2:14],-DIVAL	-AINCLK	0.01"~6"
Address OUT	-AOUT[2:14]	-AOCLK	0.01"~6"

Ultra DMA/66 Guide-line	Signals	Before termination resisor	After termination resisor to IDE connect
1.IDE signals is in a minimum of 5 mil wide and 10 mils between two adjacent traces. 2.Data and strobe lines should be routed as a bus.The total trace length of these signals should be short than 4.5".The maximum trace length difference among them must be less than 1".Other lines should be as short as possible.	-IDERST1,-IDERST2,-PDIOW,-SDIOW ,-PDIOR,-SDIOR,-PDDACK,-SDDACK ,-PDCS1,-SDCS1,-PDCS3,-SDCS3 ,PDA[0:2],SDA[0:2],PDD[0:15] ,SDD[0:15]	L6<1"	L7<3.5"
	IRQ14,IRQ15,PIORDY,SIORDY ,PD33_-66,SD33_-66,PDDREQ ,SDDREQ	L7<3.5"	L6<1"