

MS-6377 100

Intel PGA 370 Processor ServerWorks CNB30LE + OSB4 Chipset National Semiconductor PC97317 IO Chip

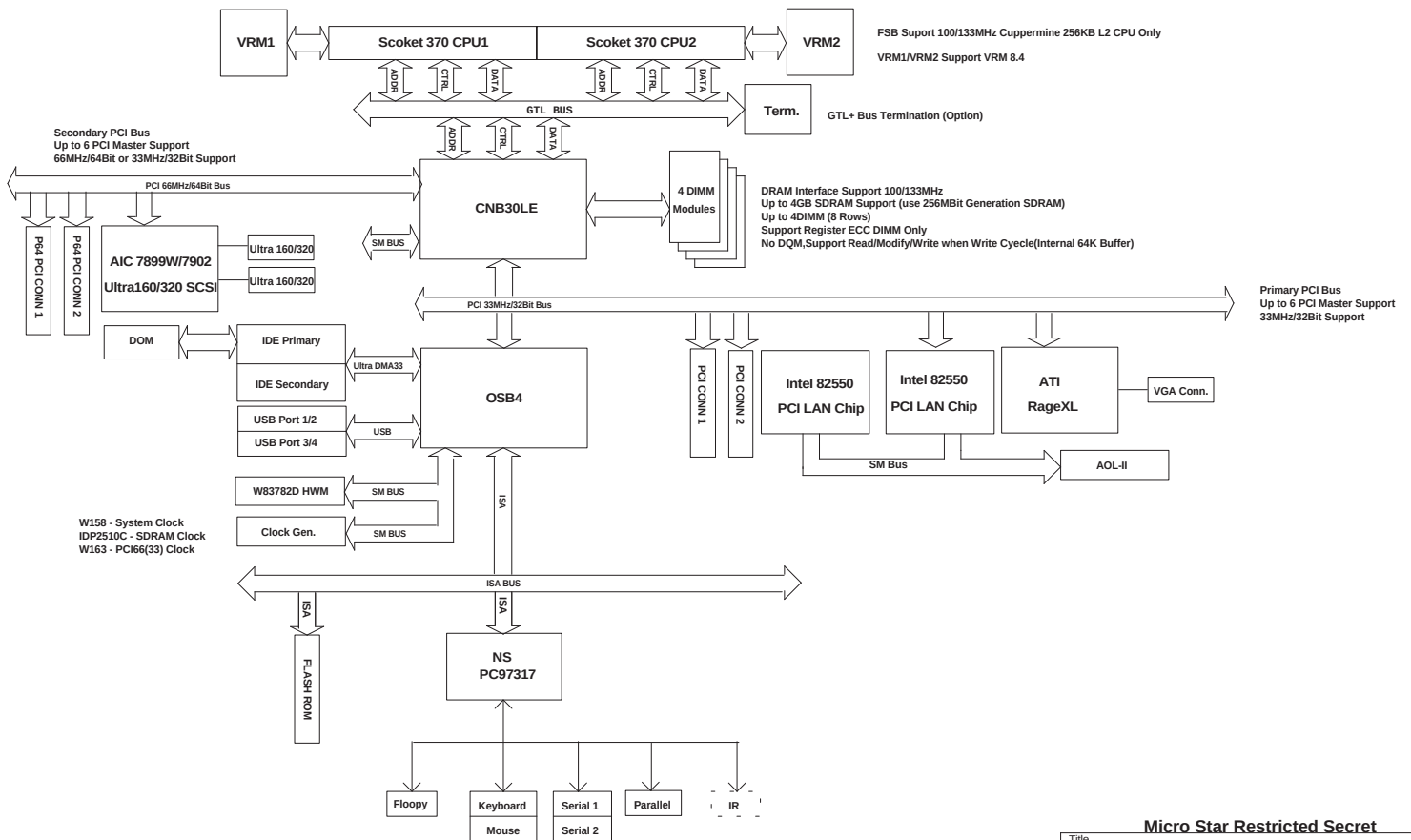
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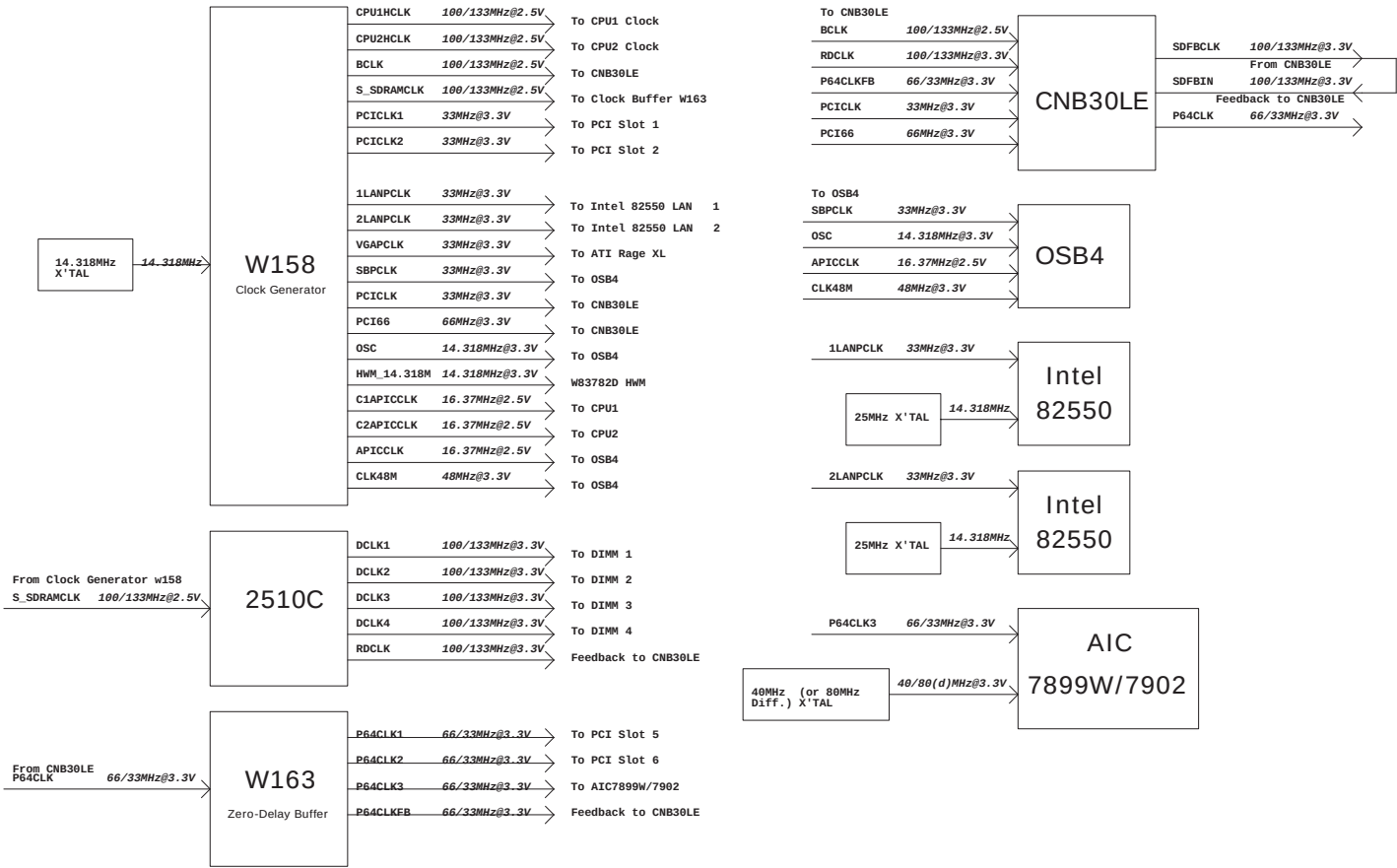
BLOCK DIAGRAM



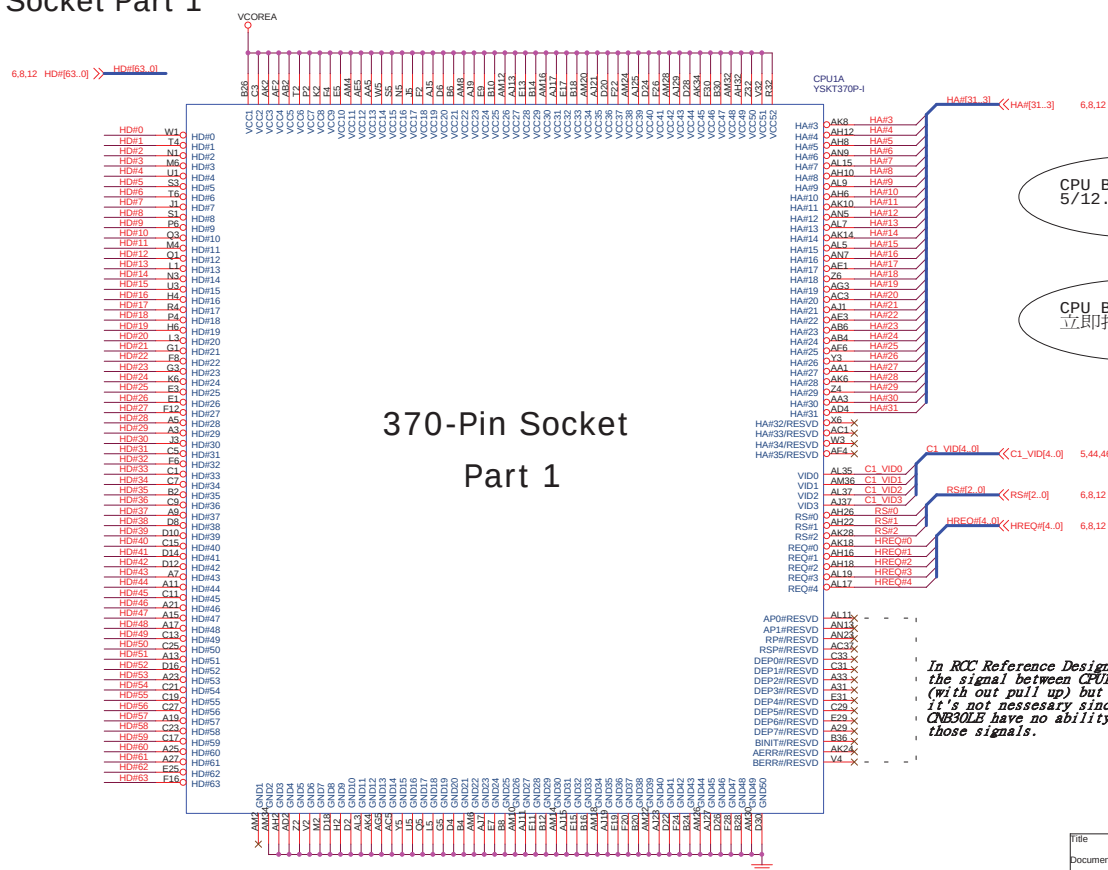
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Title		Block Diagram		Rev
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MS6377 Clock Map



370PGA Socket Part 1



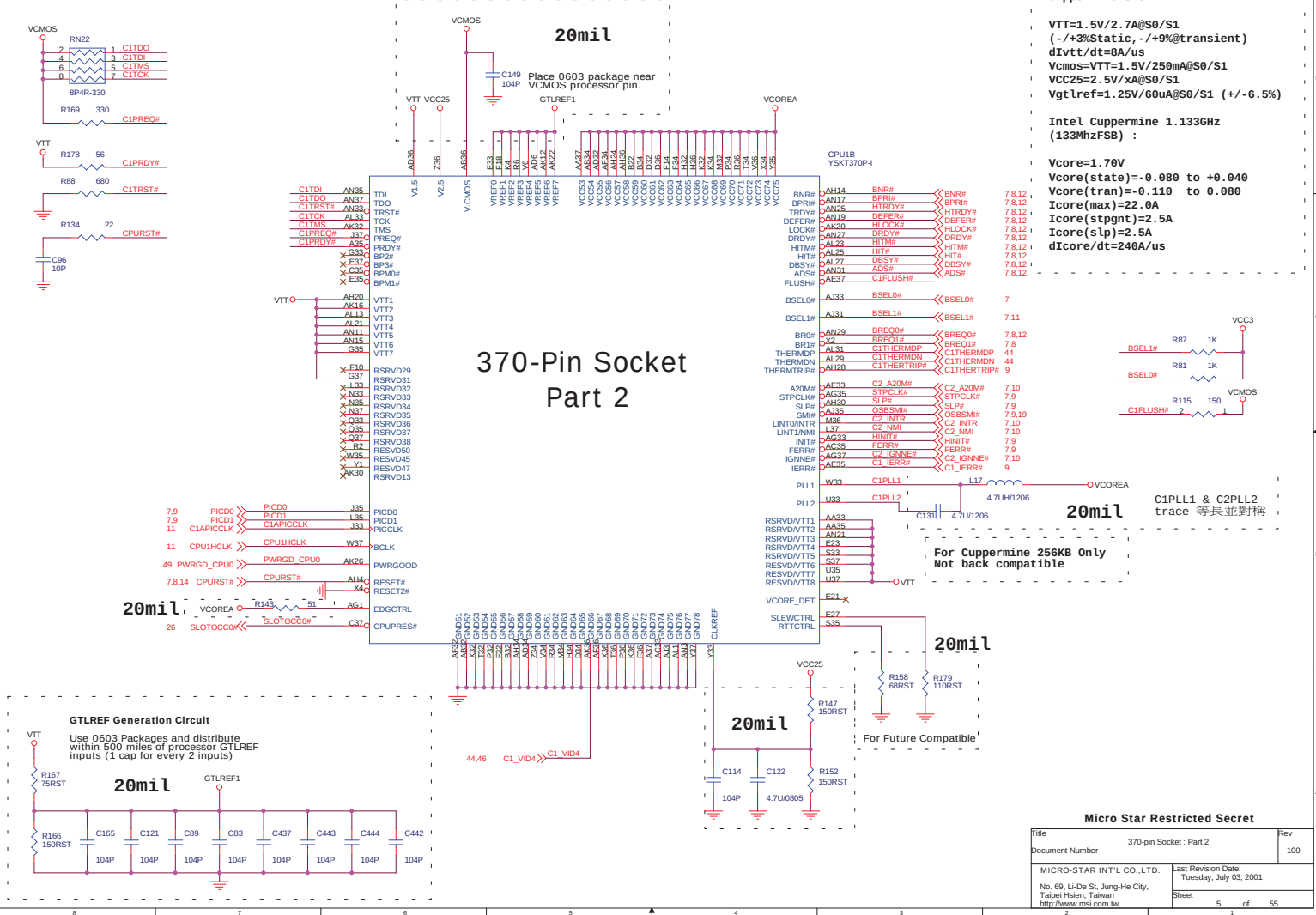
CPU BUS trace/space
5/12.5 mil (1: 2.5)

CPU BUS 出 CHIP 後
立即打 VIA 至各 CPU

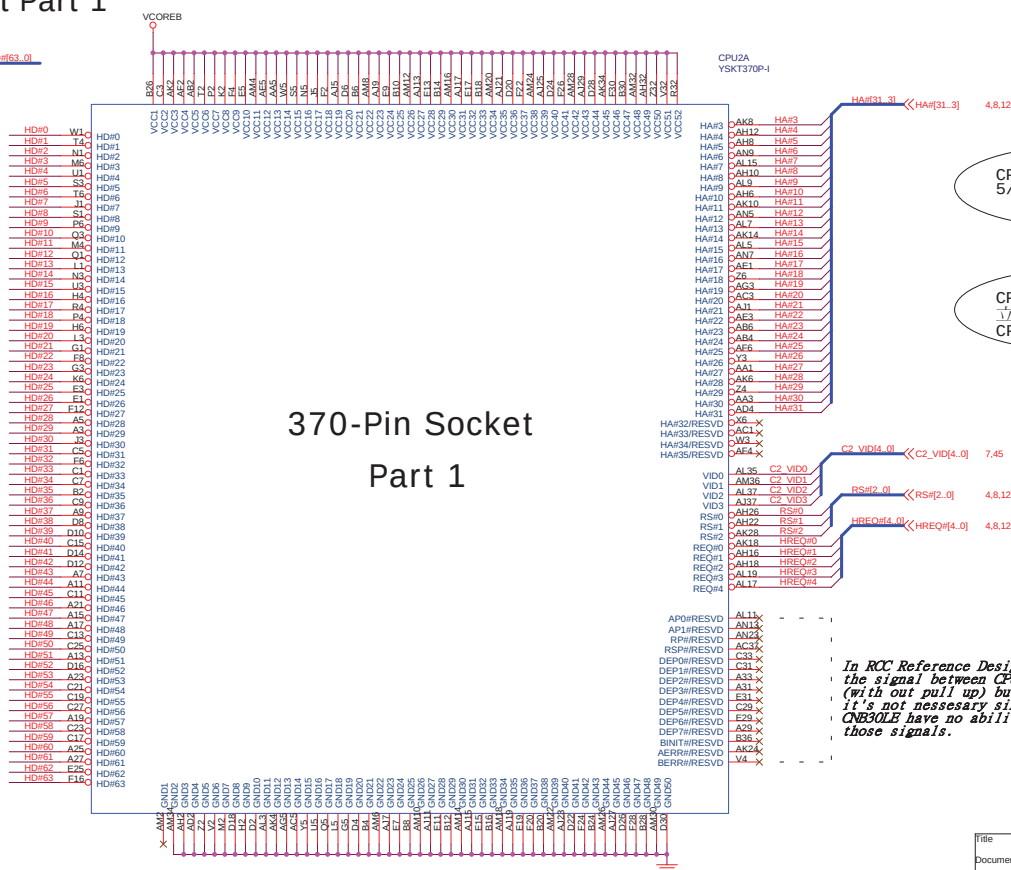
In ROC Reference Design connect all the signal between CPU1 and CPU2 (with out pull up) but we think it's not nesessary since the CNB30LE have no ability to process those signals.

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370PGA Socket Part 2

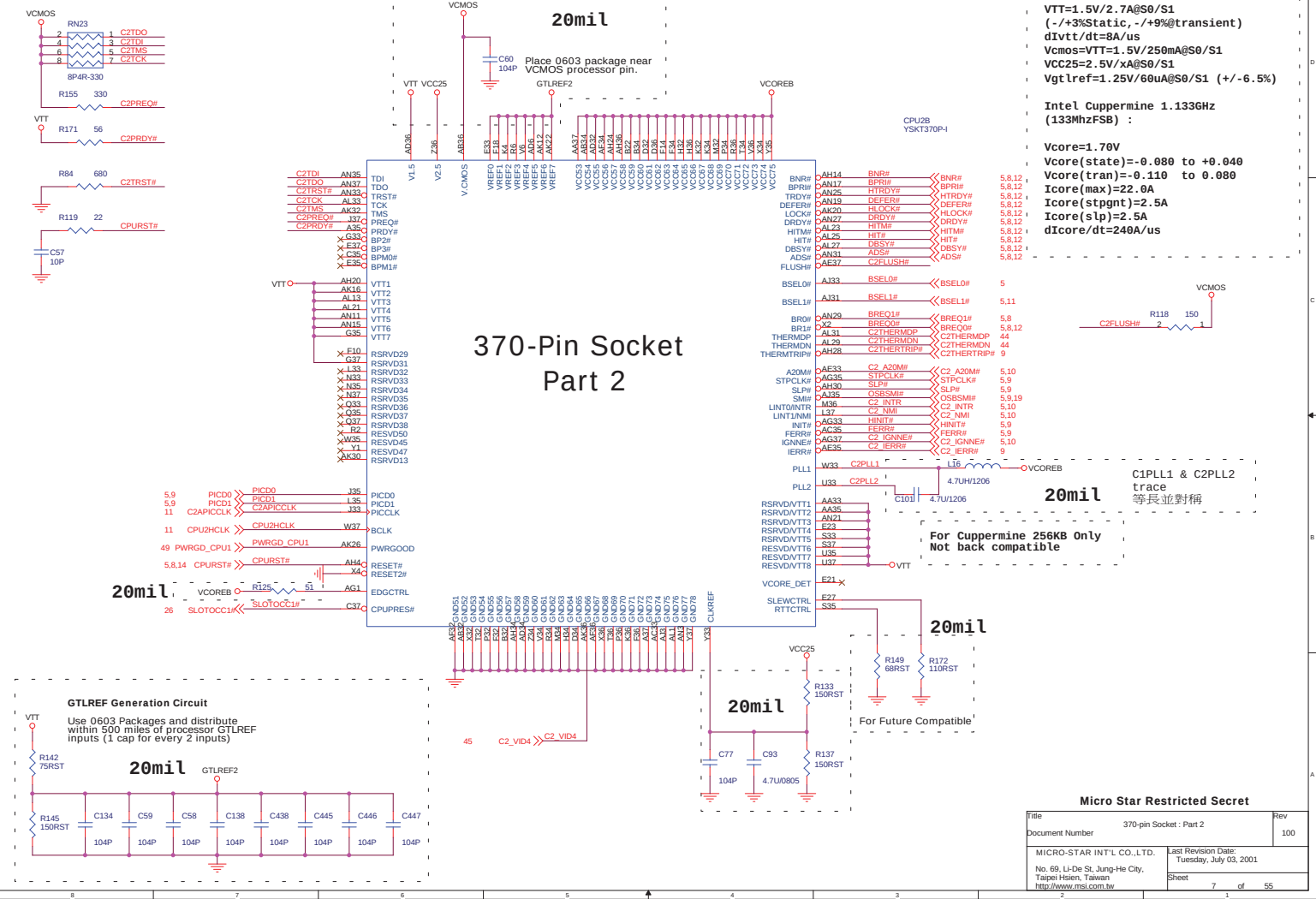


370PGA Socket Part 1

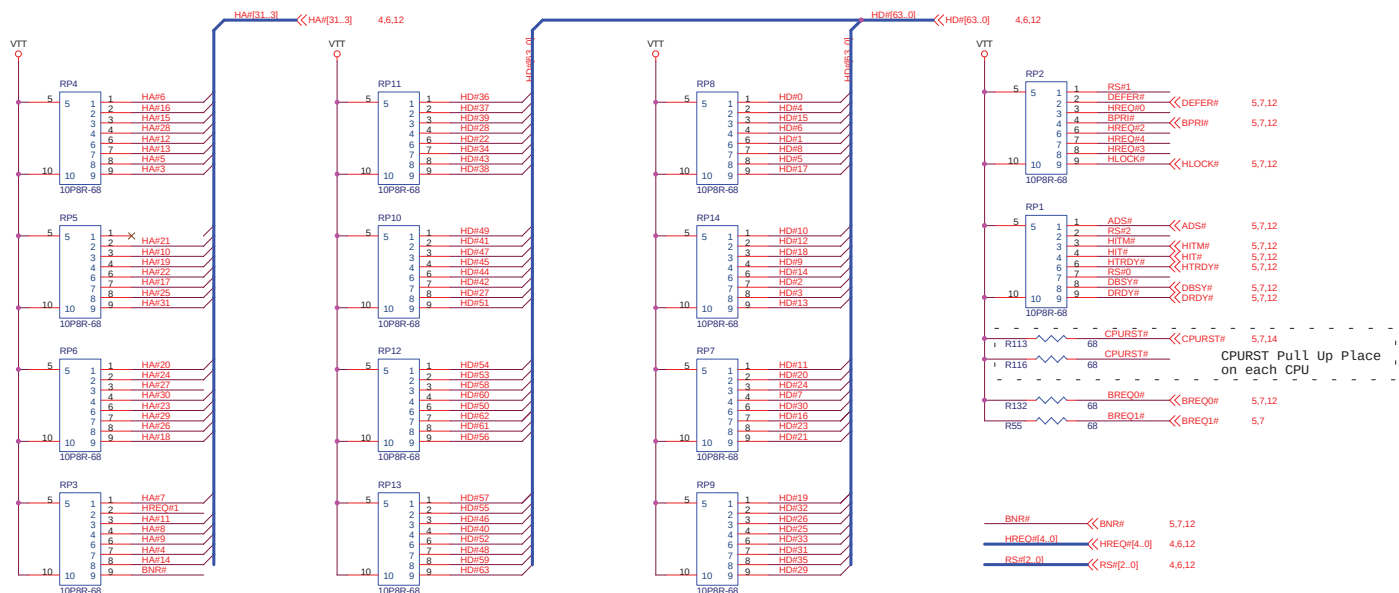


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370PGA Socket Part 2



AGTL Termination



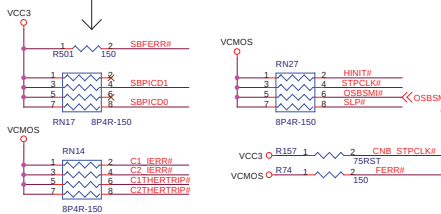
In RCC Reference Design without the GIL+ Bus termination. For signal quality issue we implement termination in our design. Put the termination inside the CPU2 socket.

一顆排阻放一顆電容

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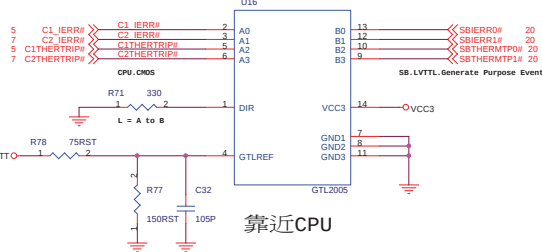
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靠近SB



Philip TTL Spec . T=25
74HC08 tpd=18ns(max)
74HC14 tpd=25ns(max)
74F07 tpd=7ns(max)

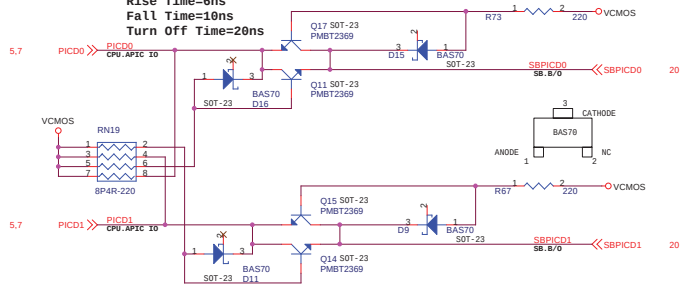
GT1 -> LVTTT



靠近CPU

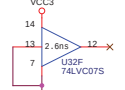
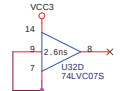
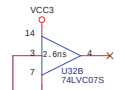
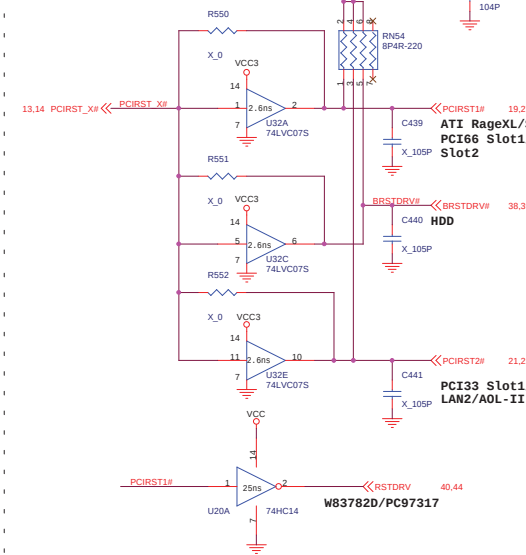
PMBT2369 NPN Switching Tr.

Turn On Time=10ns
Delay Time=4ns
Rise Time=6ns
Fall Time=10ns
Turn Off Time=20ns



VCC3

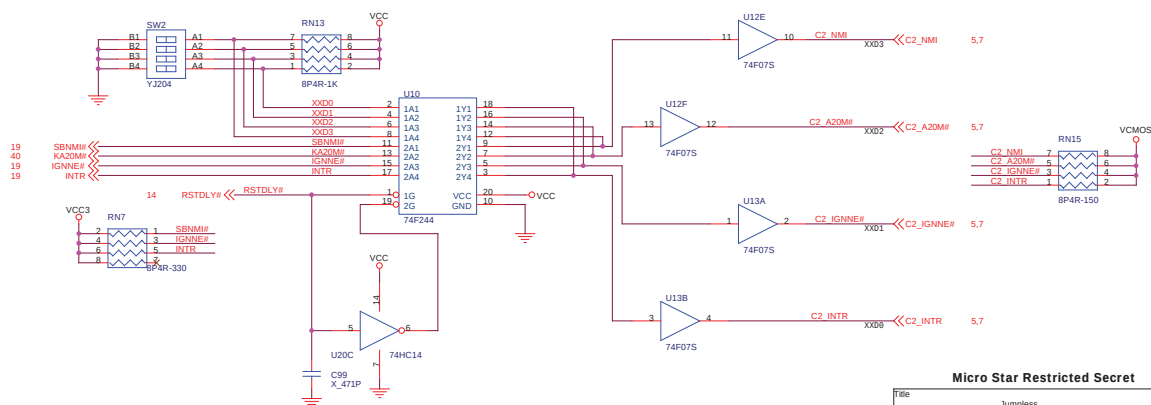
Philip TTL Spec . T=25
74HC14 tpd=25ns(max)
74LVC07 tpd=2.6ns(max)



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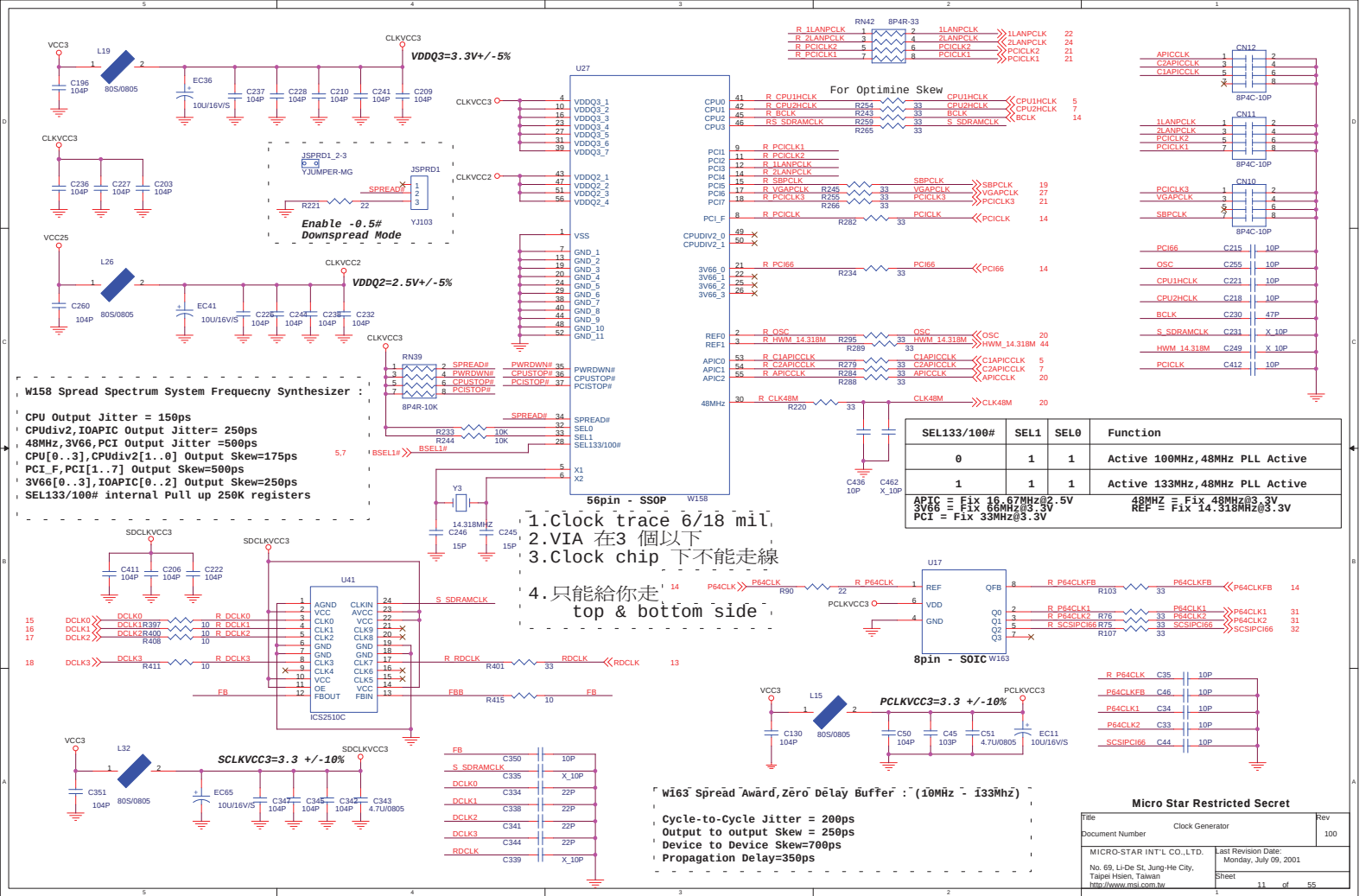
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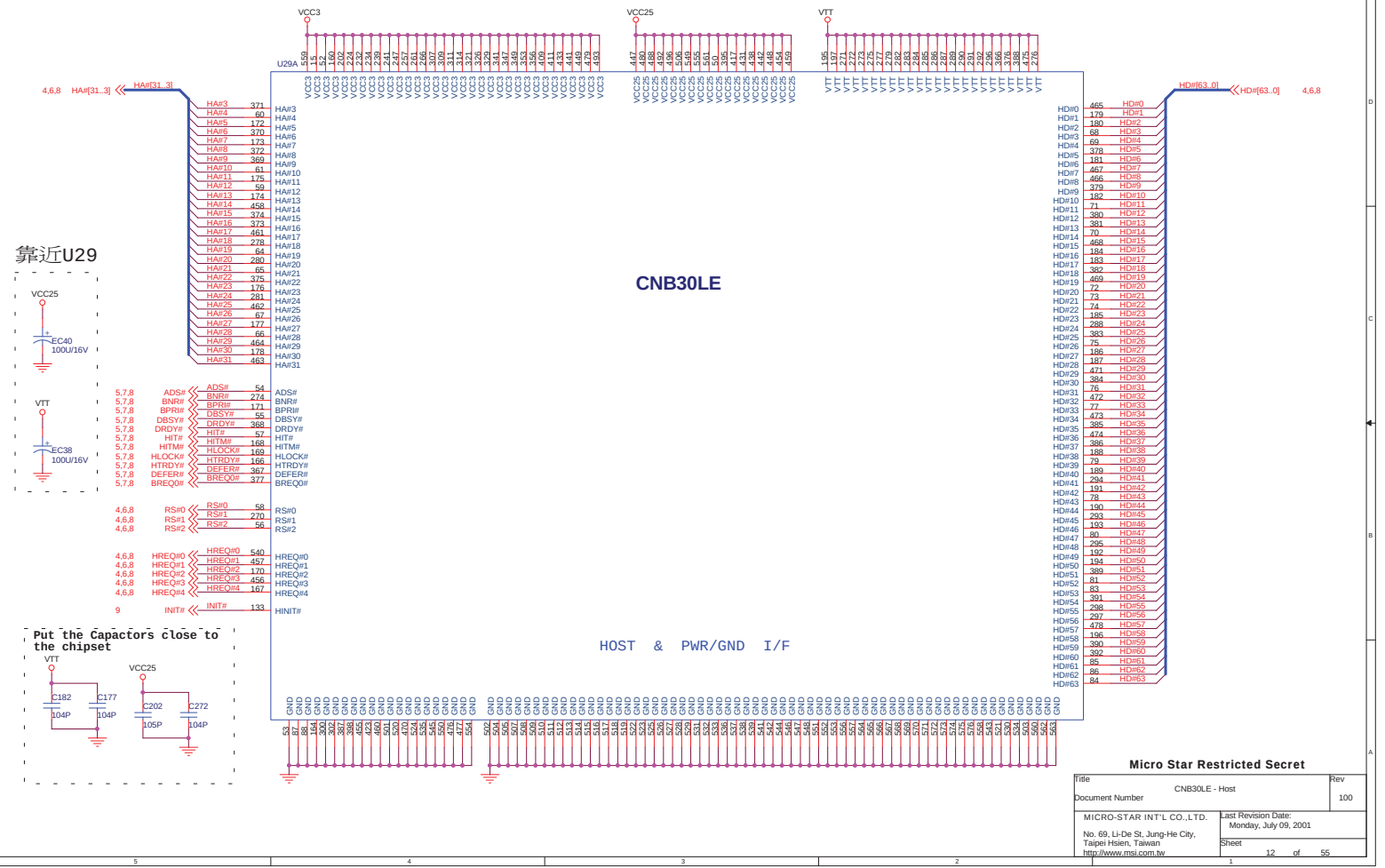
A1	A2	A3	A3	
LINT1	A20M#	IGNNE#	LINT0	Ratio
0	0	0	0	2
0	0	0	1	2.5
0	0	1	0	3 / 11
0	0	1	1	3.5/11.5
0	1	0	0	4
0	1	0	1	4.5/8.5
0	1	1	0	5
0	1	1	1	5.5/9.5
1	0	0	0	6 /10
1	0	0	1	6.5/10.5
1	0	1	0	7
1	0	1	1	7.5
1	1	0	0	8
1	1	0	1	1.5
1	1	1	0	Reserved
1	1	1	1	2



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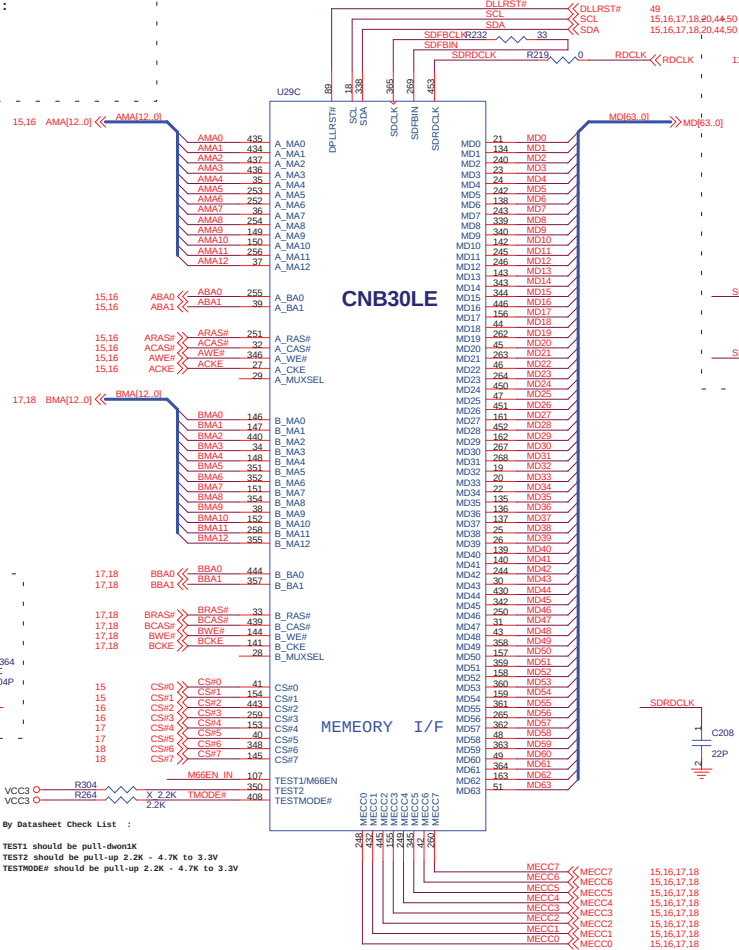




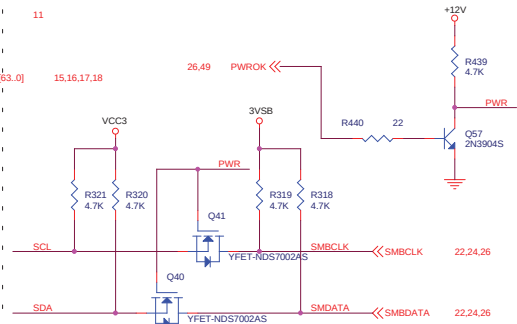
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Power Consumption of CNB30LE

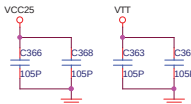
2.5V - 600mA for Core Logic
1.5V - 1.0A for GTL buffer
3.3V - 1.8A for Both PCI bus
and Memory Bus



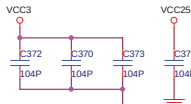
SM Bus Translation



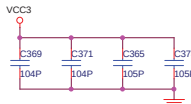
Put the Capacitors on the solder side



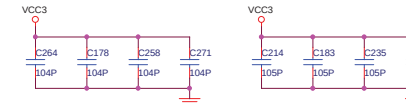
Put the Capacitors on the solder side



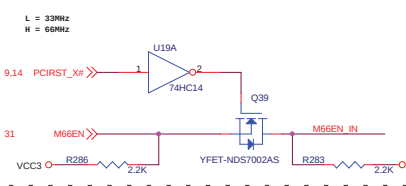
Put the Capacitors on the solder side



Put the Capacitors on the corner of the chipset

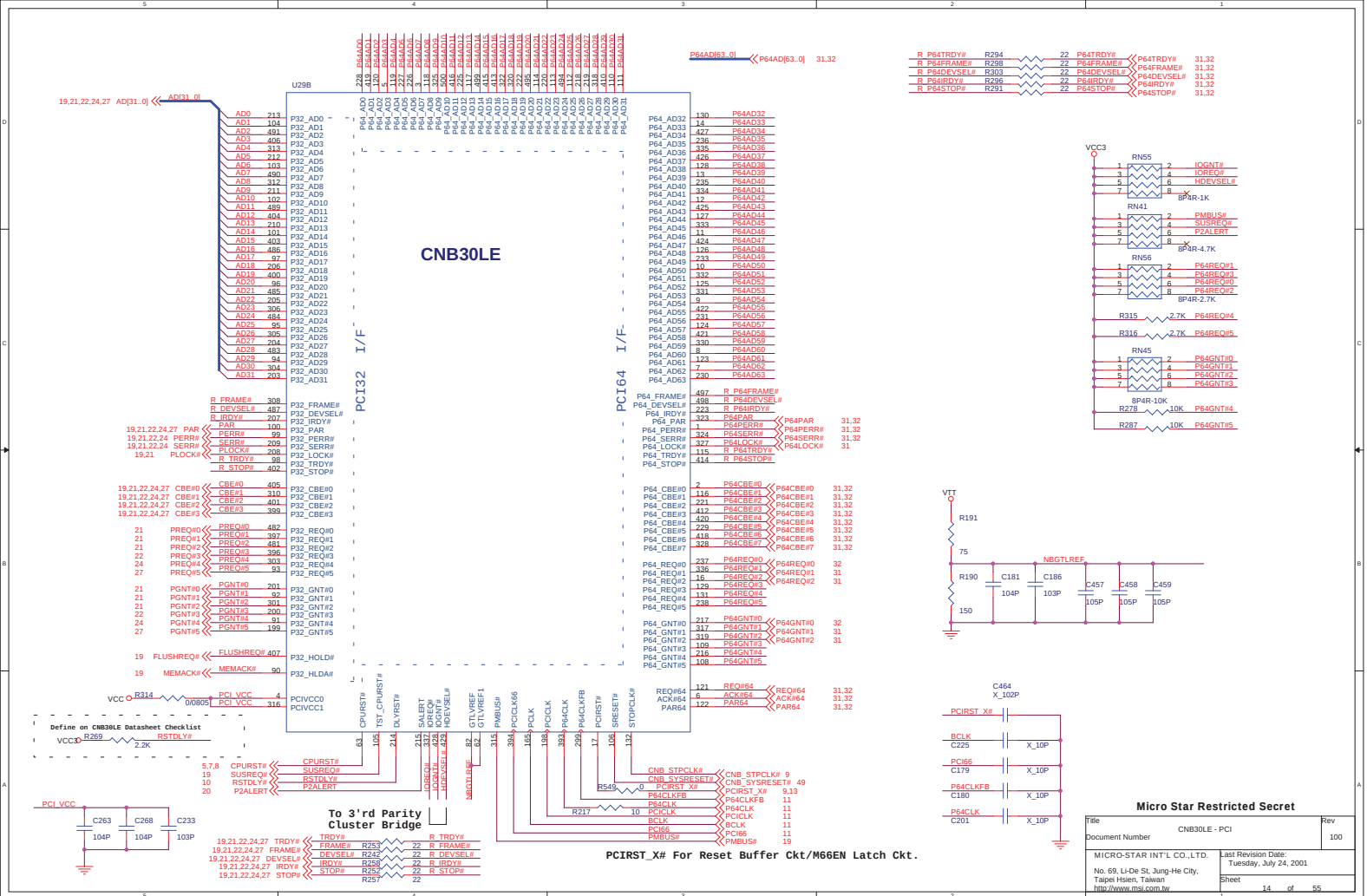


M66EN_IN to latch at PCIRESET to configure the DPLL to generate 33MHz or 66MHz out on PCICLK_0



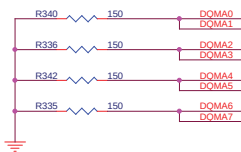
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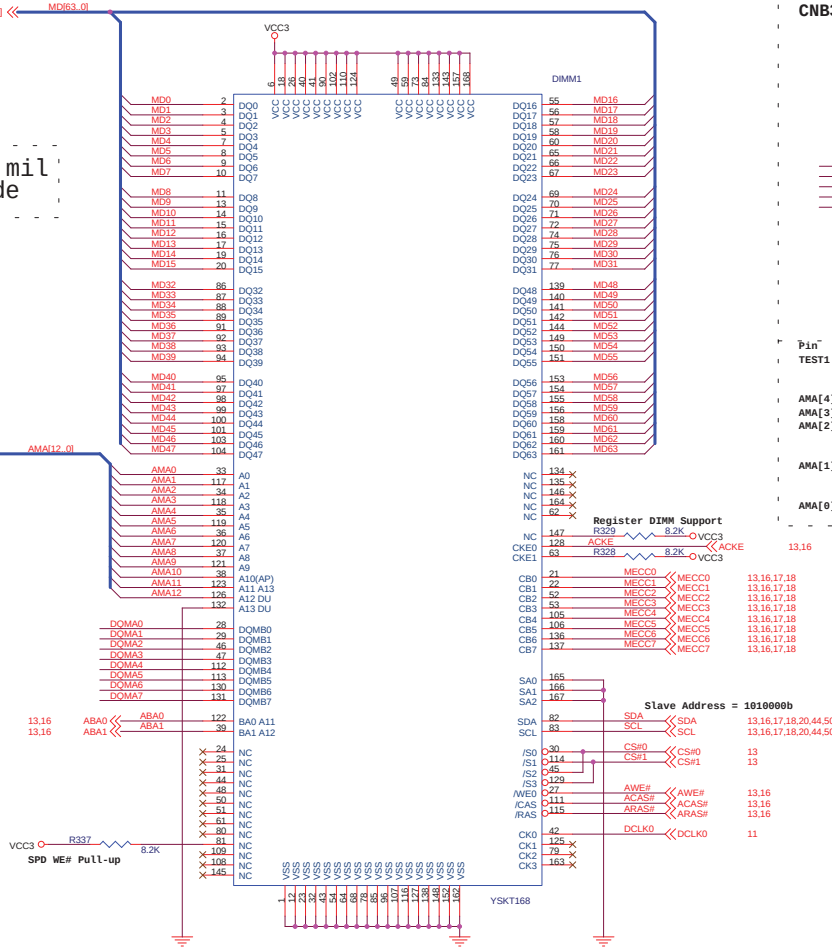


SYSTEM MEMORY

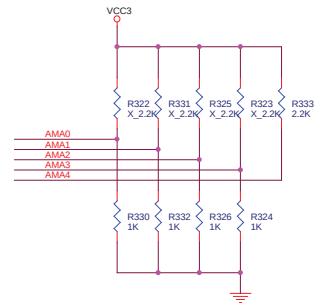
Memory BUS trace 5/10 mil
Only TOP or BOTTOM side



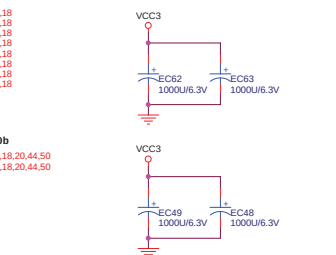
SLAVE ADDRESS = 1010000B



CNB30LE H/W Strap



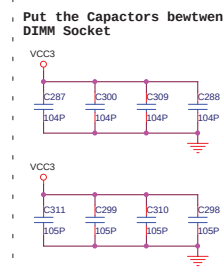
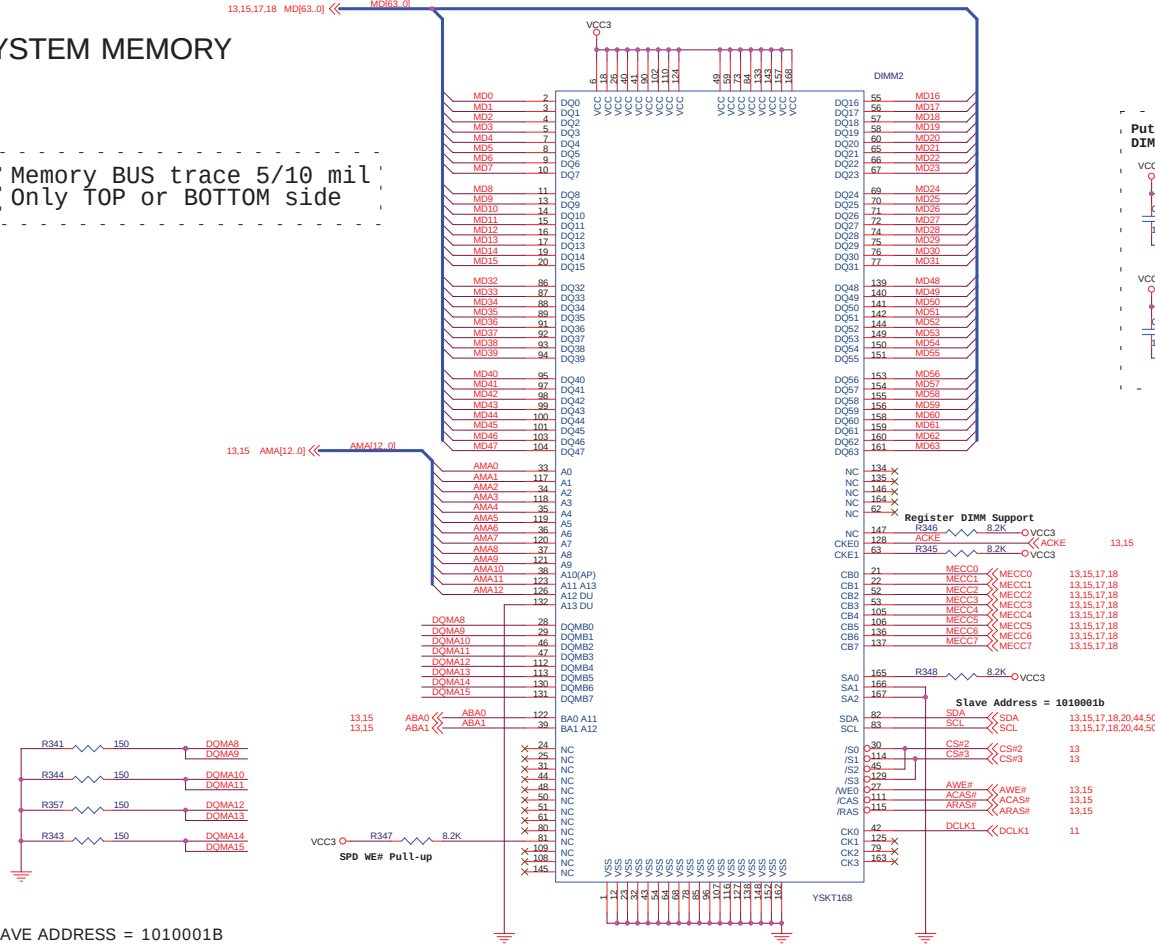
Pin	Register	Description
TEST1	SCR2[0]	Secondary PCI Frequency 0 = 33MHz 1 = 66MHz
AMA[4]	SCR2[1]	Always Pull Up
AMA[3]	SCR[3]	Not Use.Can be Pull Up or Down
AMA[2]	SCR[2]	Always Pull Low 0 = Enable Internal PLL's 1 = Disable Internal PLL's
AMA[1]	SCR[1]	In order Queue depth 0 = IOQ depth is 8 1 = IOQ depth is 1
AMA[0]	SCR[0]	Bridge ID.The ID must always be 0 to Primary CNB30



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SYSTEM MEMORY

Memory BUS trace 5/10 mil
Only TOP or BOTTOM side



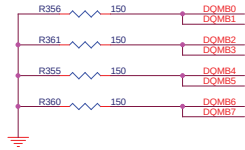
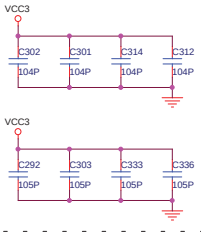
SLAVE ADDRESS = 1010001B

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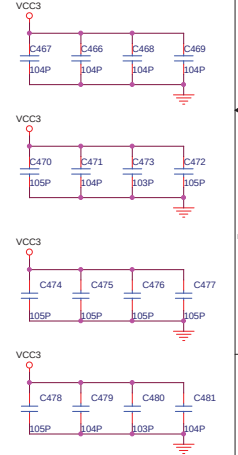
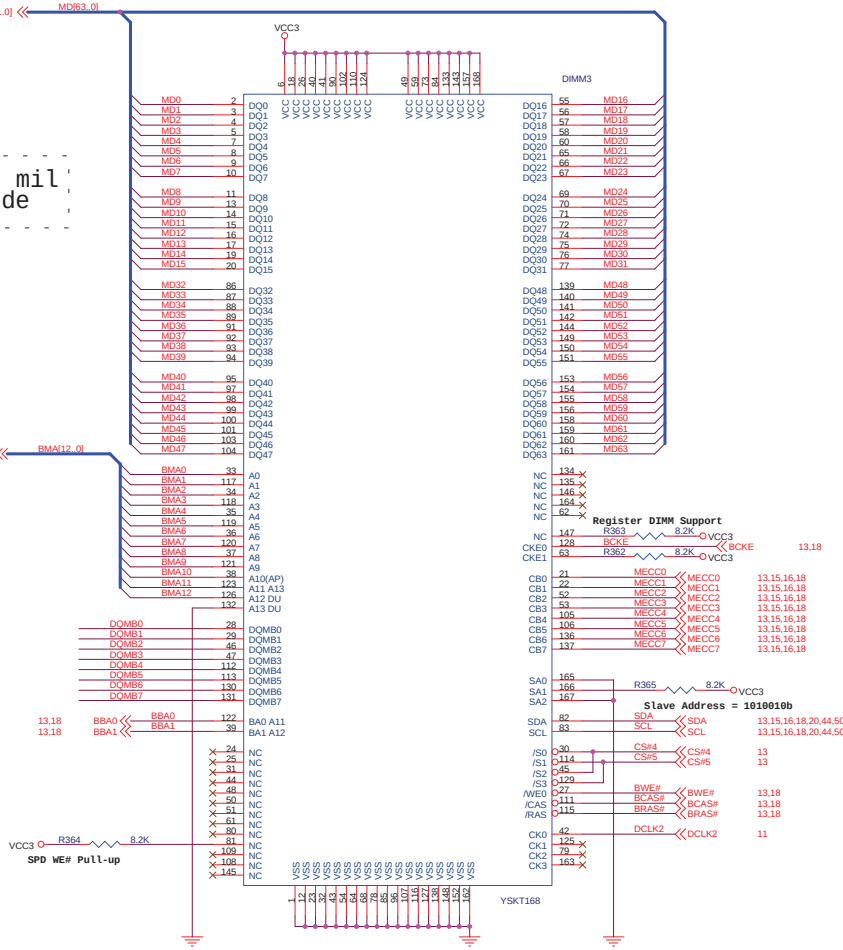
SYSTEM MEMORY

Memory BUS trace 5/10 mil
Only TOP or BOTTOM side

Put the Capacitors bewtween
DIMM Socket



SLAVE ADDRESS = 1010010B

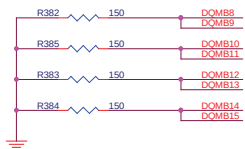


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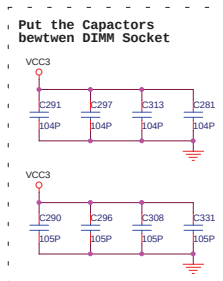
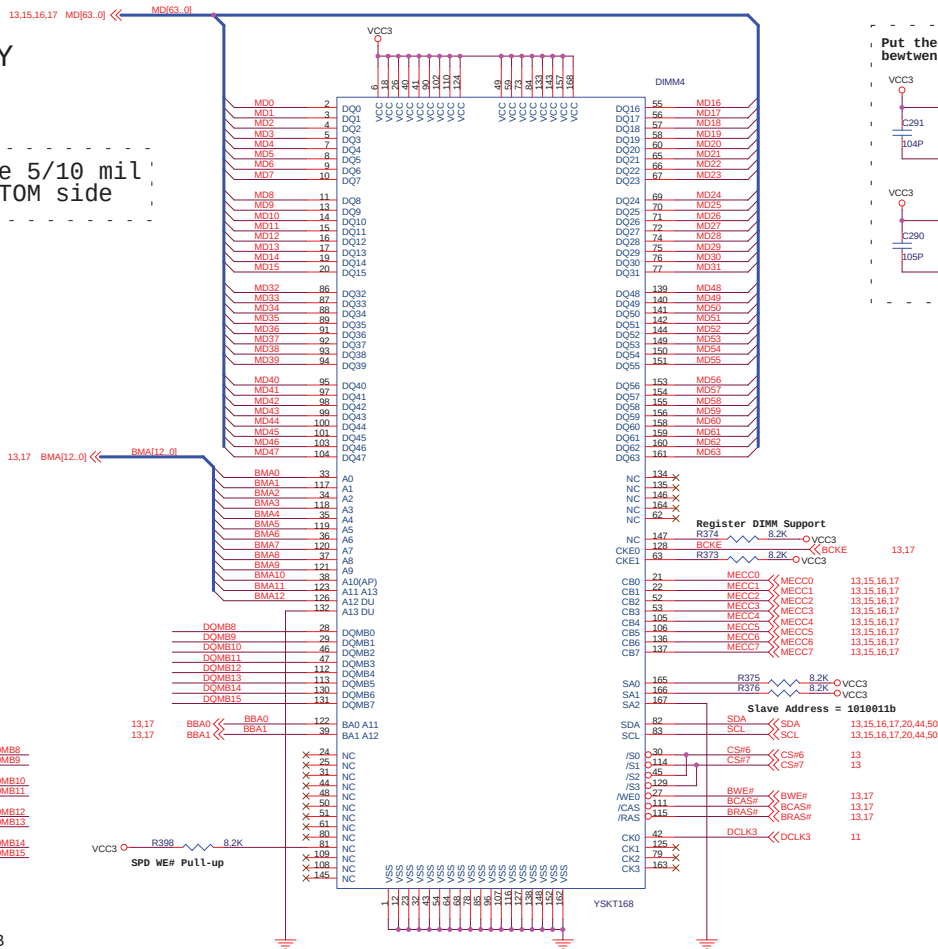
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SYSTEM MEMORY

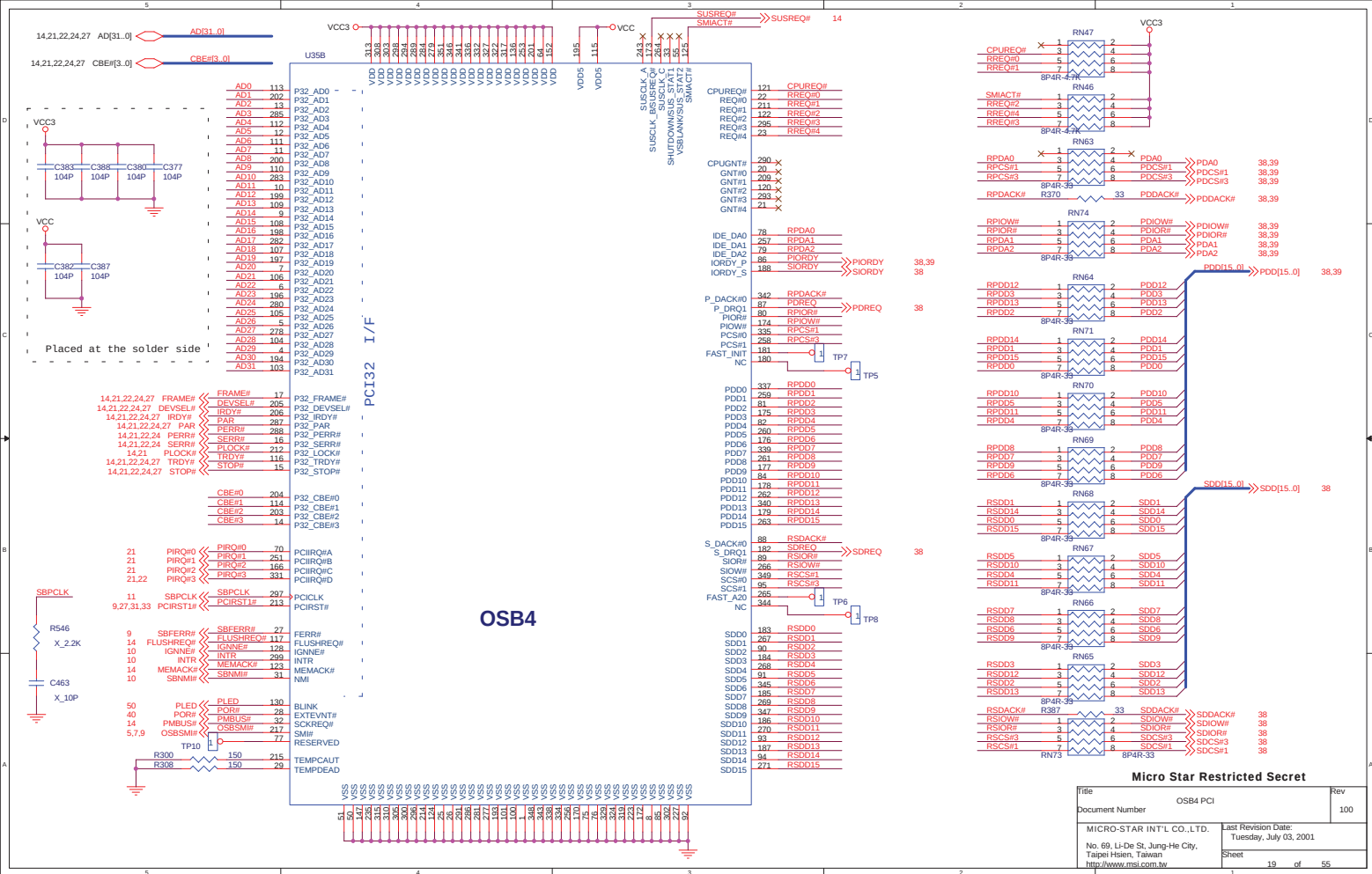
Memory BUS trace 5/10 mil
Only TOP or BOTTOM side

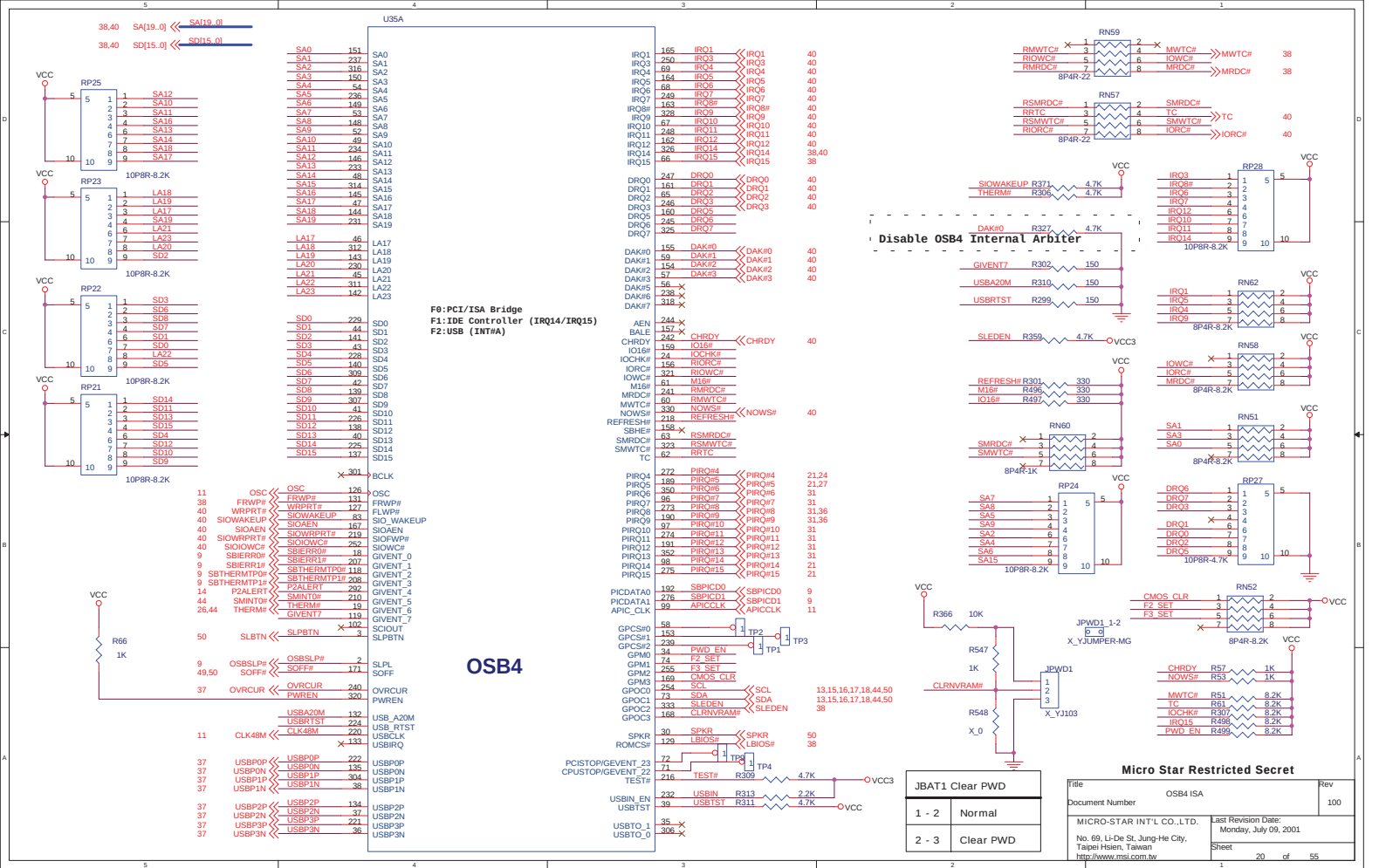


SLAVE ADDRESS = 1010011B



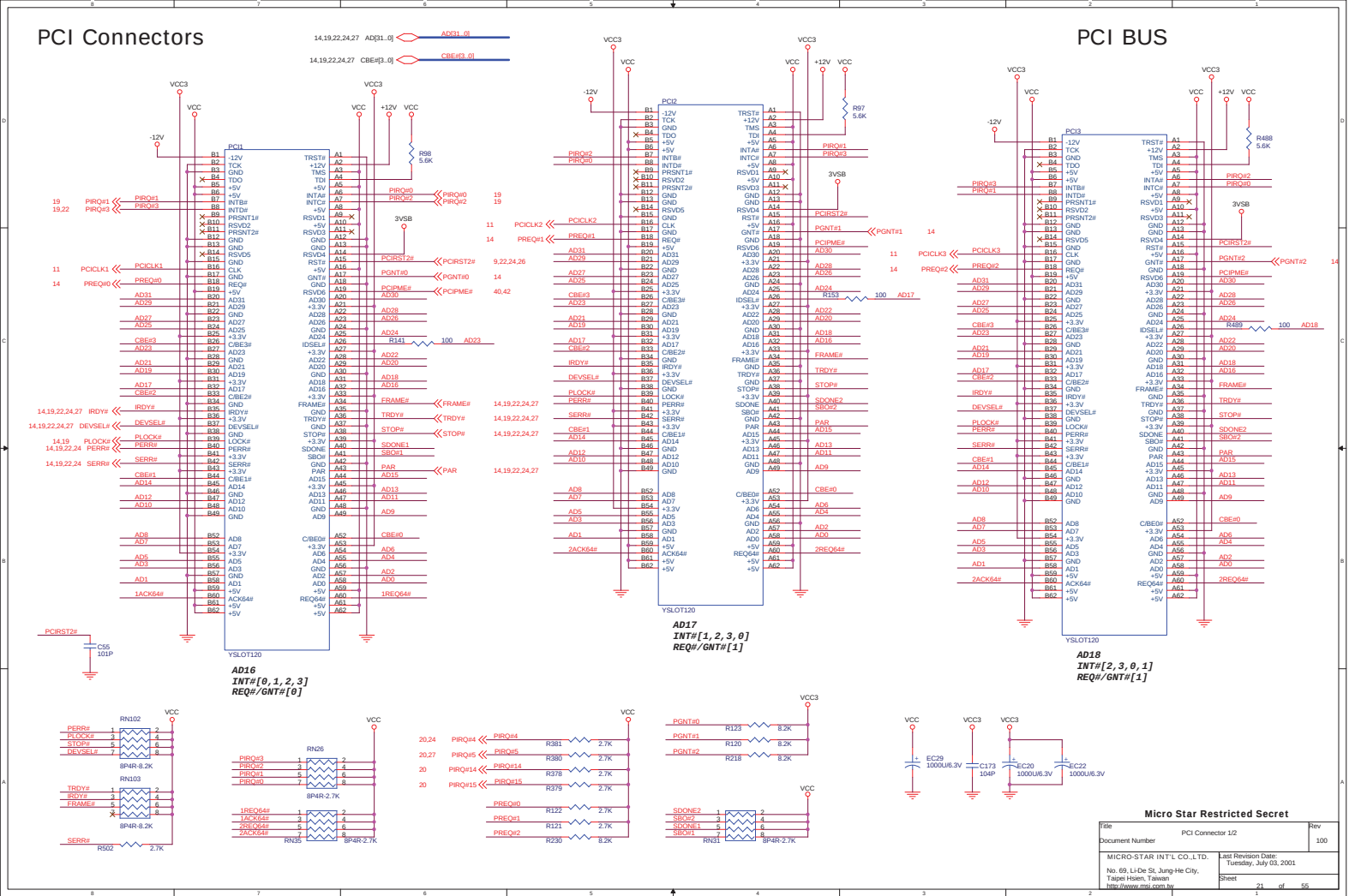
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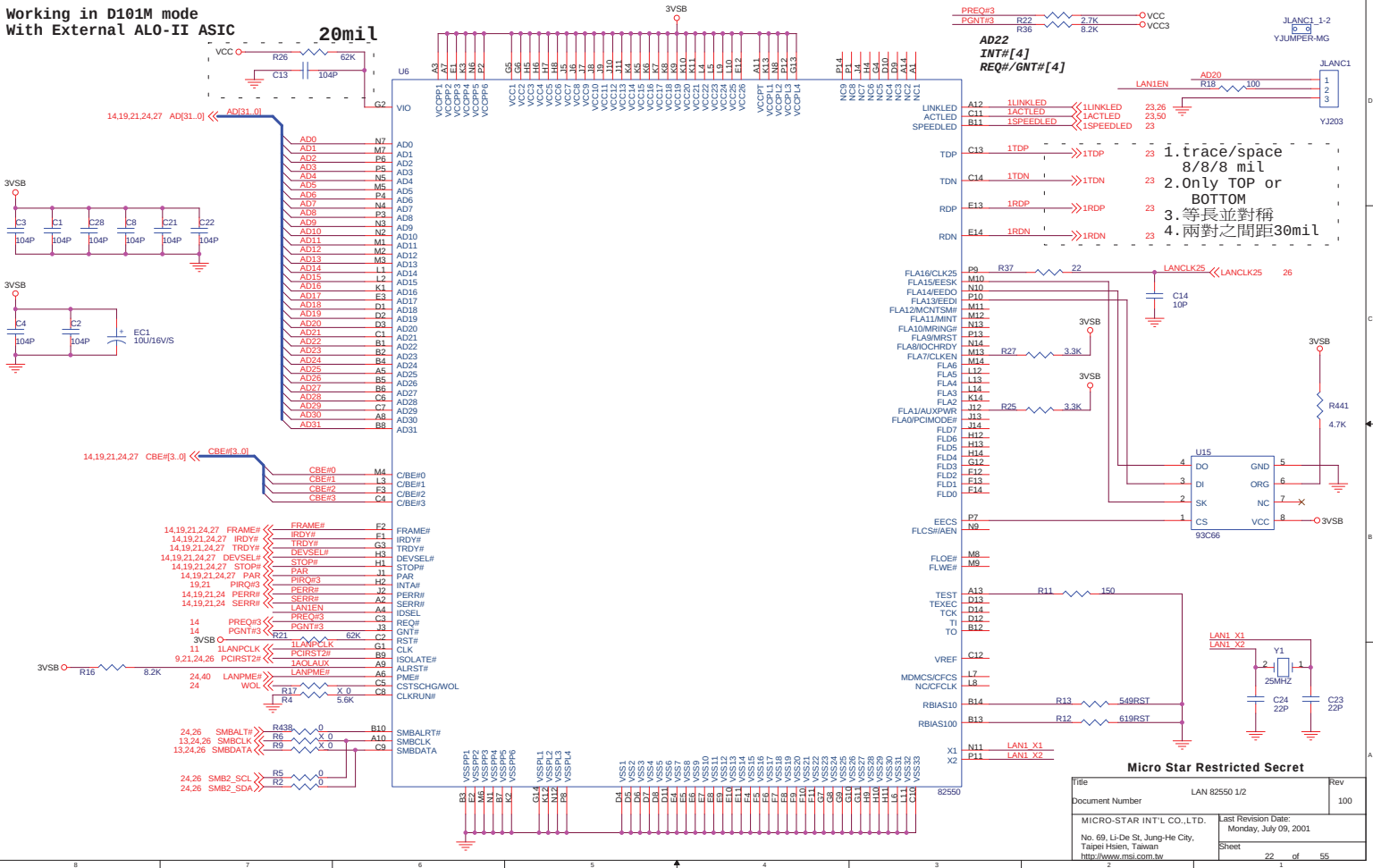


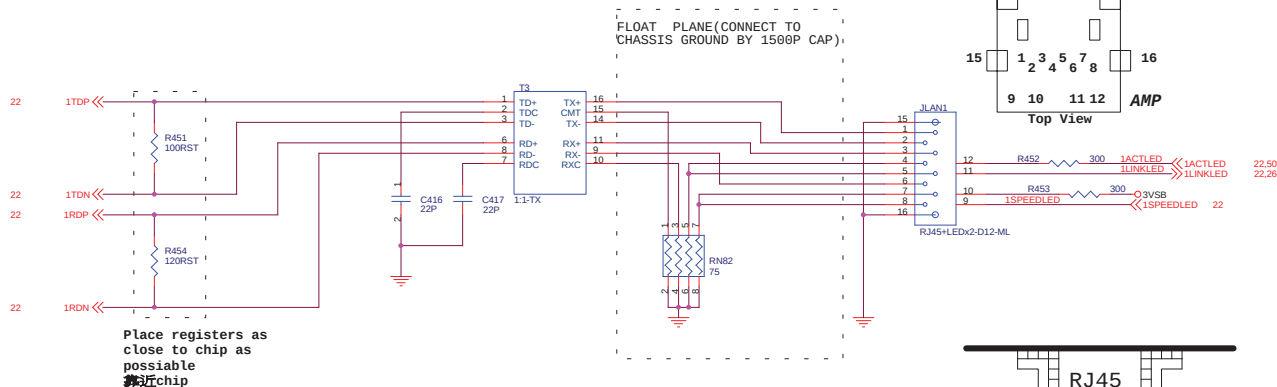
PCI Connectors

PCI BUS



Working in D101M mode
With External ALO-II ASIC

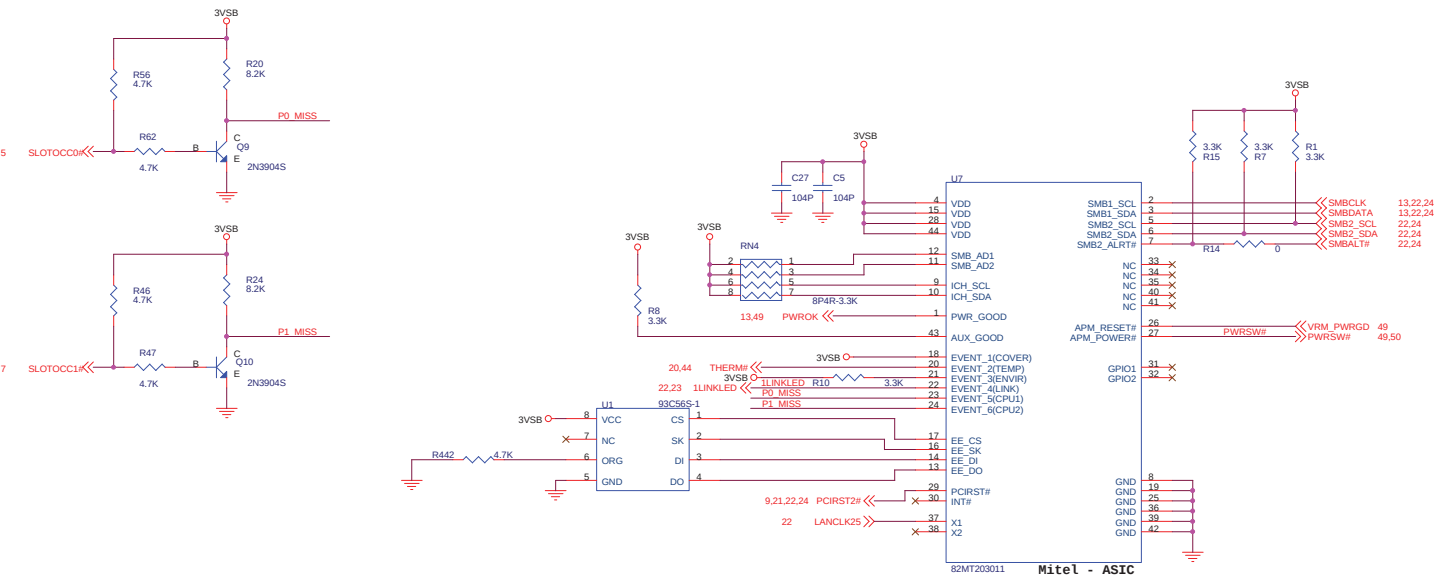




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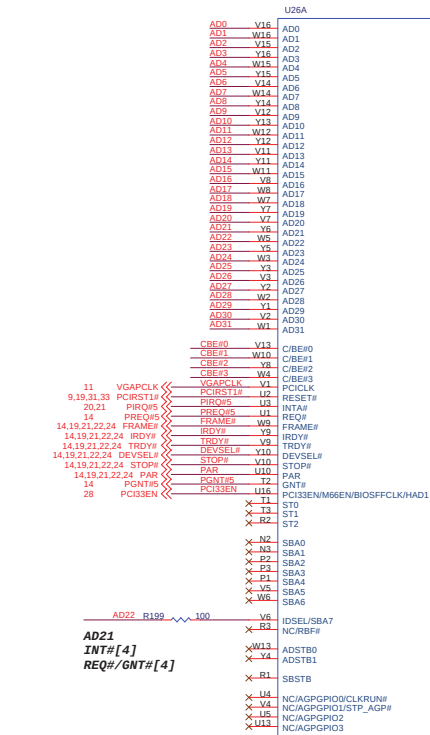
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AlertOnLAN 2

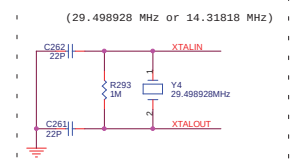
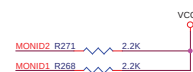
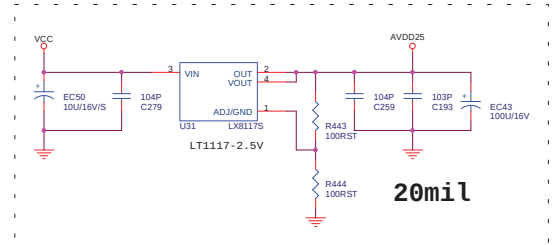


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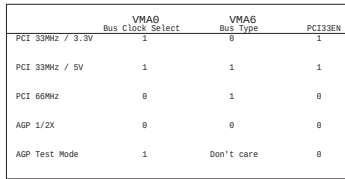
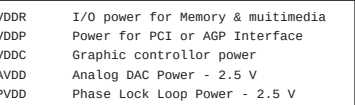
14,19,21,22,24 AD[31:0] << AD[31:0]
14,19,21,22,24 CBE[3:0] << CBE[3:0]



RESET VALUE	R92
RAGE XL	365
RAGE 128	374



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INTERRUPT always enable

VGA always enable

ROMCS# R285

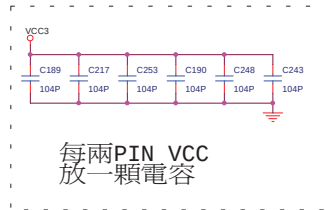
Use System BIOS

VMA5	
IDSEL Enable	Open
IDSEL Disable	Close

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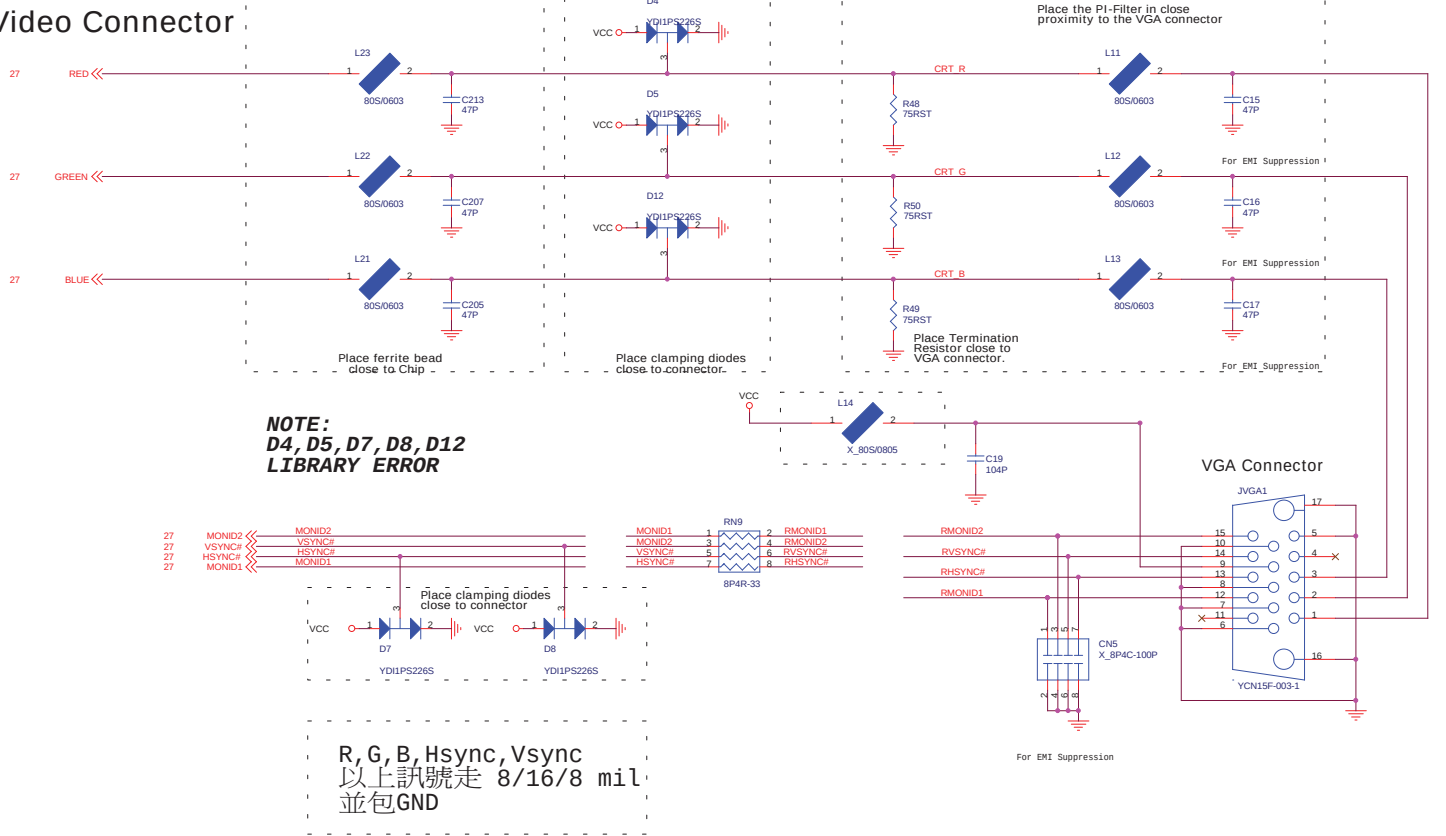
4MBytes SDRAM 16Mbit 512Kx16x2



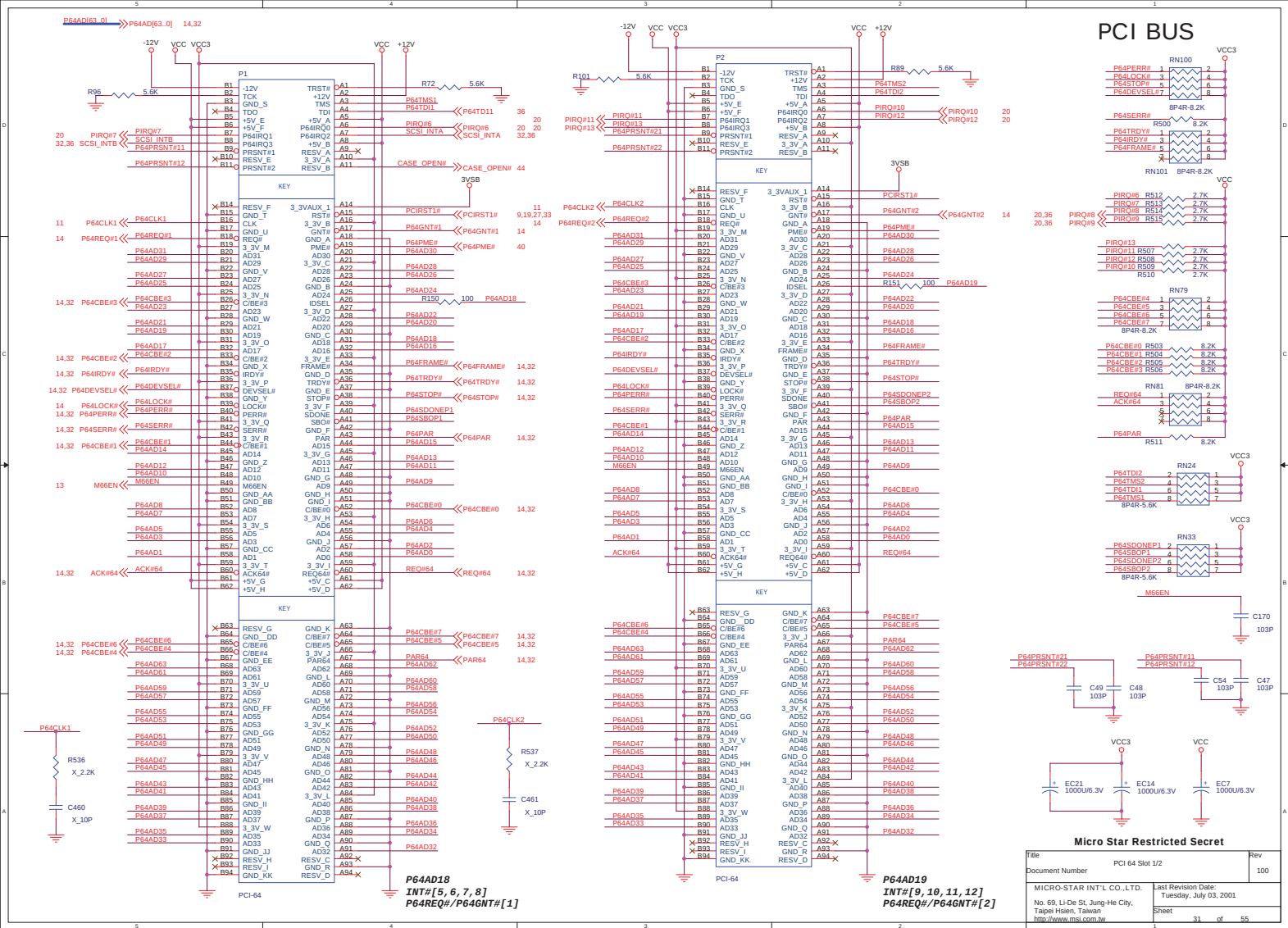
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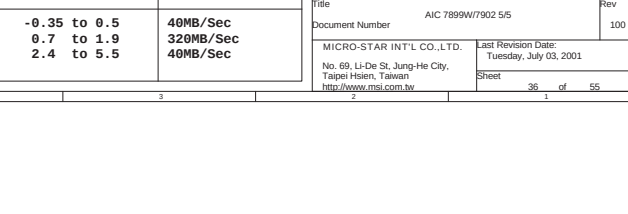
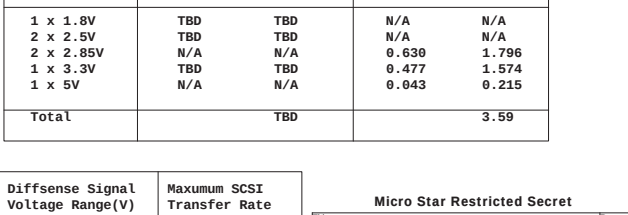
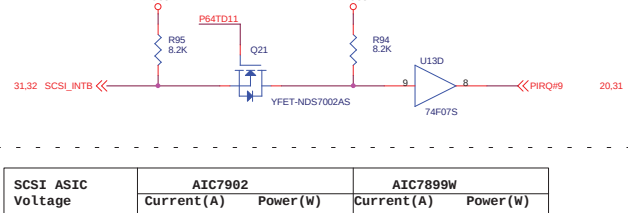
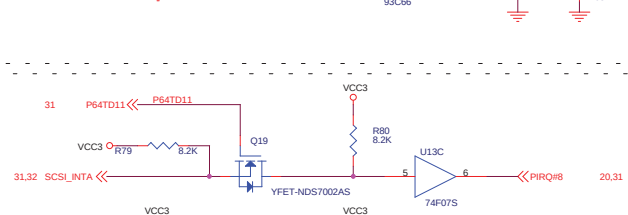
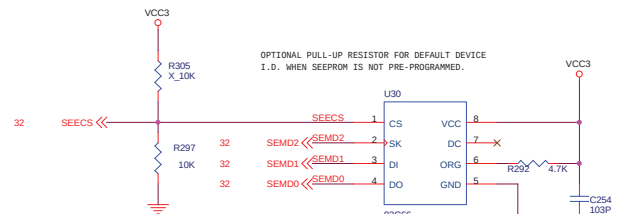
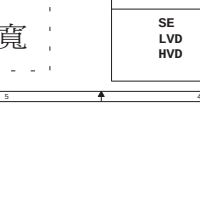
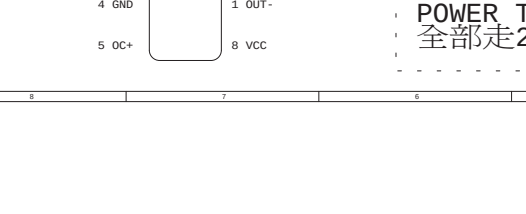
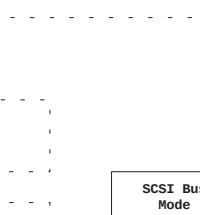
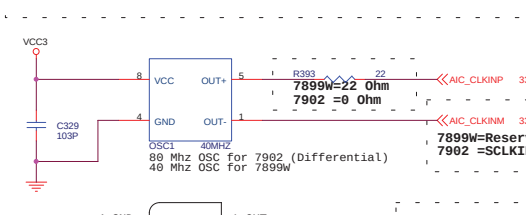
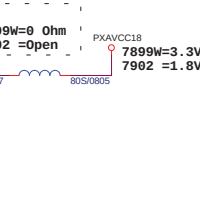
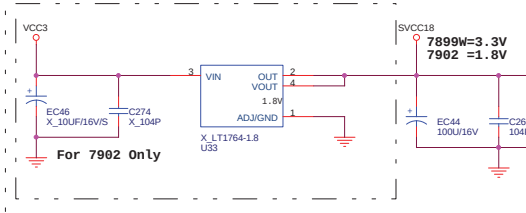
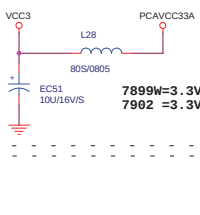
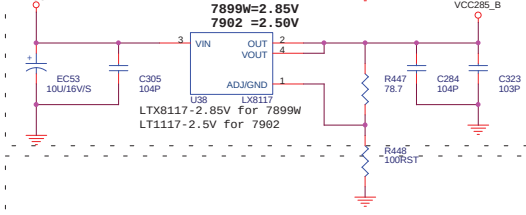
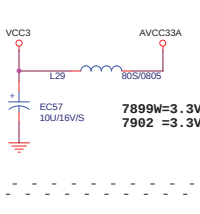
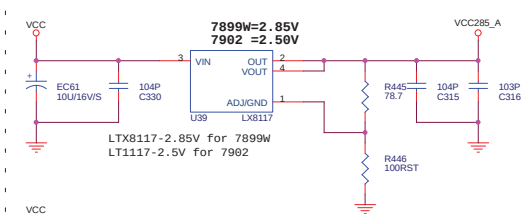
Title	ATI Rage XL 3/4	Rev
Document Number		100
MICRO-STAR INT'L CO.,LTD.		Last Revision Date:
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Video Connector



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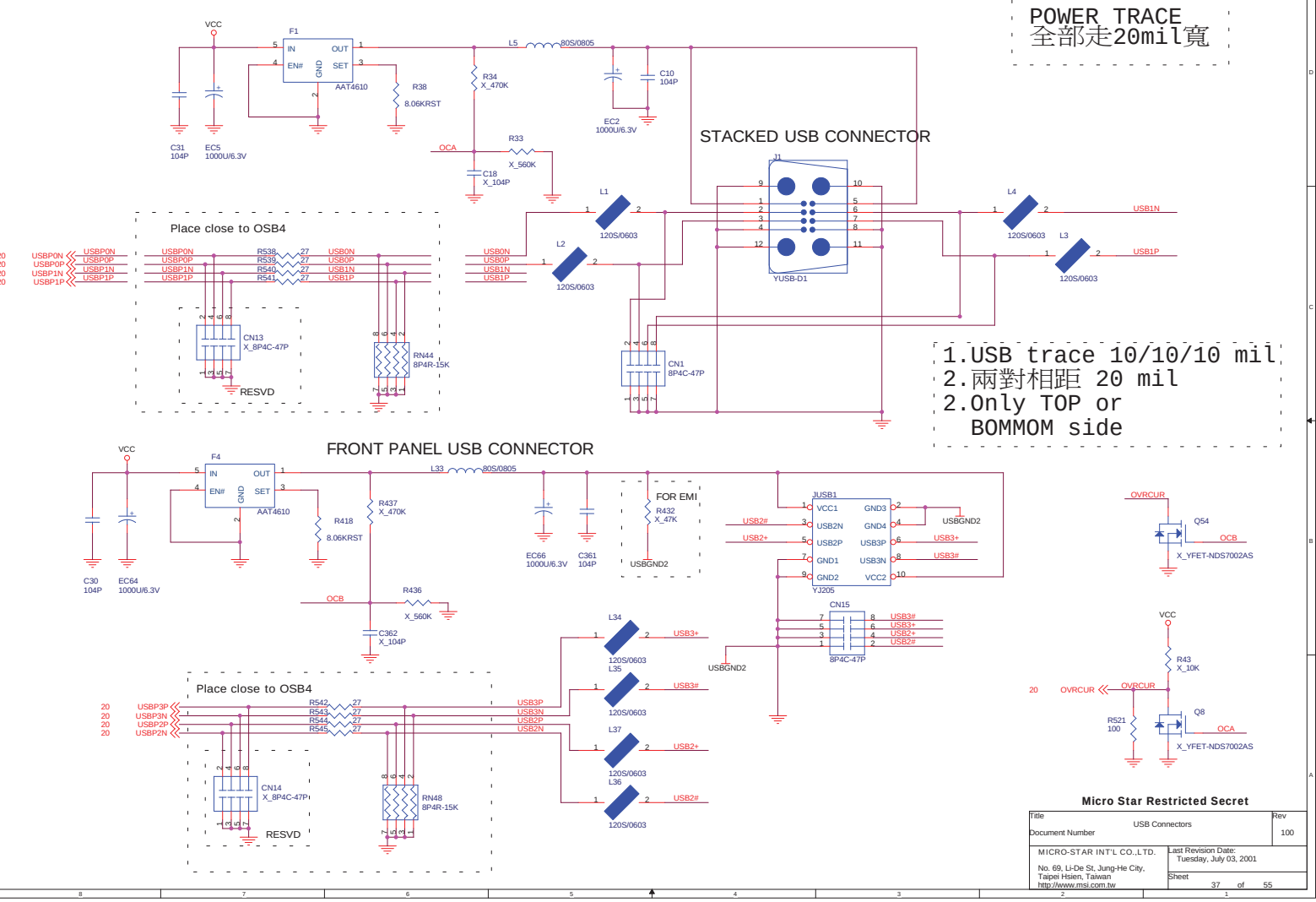
SCSI ASIC Voltage	AIC7902		AIC7899W	
	Current(A)	Power(W)	Current(A)	Power(W)
1 x 1.8V	TBD	TBD	N/A	N/A
2 x 2.5V	TBD	TBD	N/A	N/A
2 x 2.85V	N/A	N/A	0.639	1.796
1 x 3.3V	TBD	TBD	0.477	1.574
1 x 5V	N/A	N/A	0.043	0.215
Total		TBD		3.59

SCSI Bus Mode	DiffSense Signal Voltage Range(V)	Maximum SCSI Transfer Rate
SE	-0.35 to 0.5	40MB/Sec
LVD	0.7 to 1.9	320MB/Sec
HVD	2.4 to 5.5	40MB/Sec

Micro Star Restricted Secret		
Title	AIC 7899W/7902 5/5	Rev 100
Document Number		
MICRO-STAR INT'L CO.,LTD.		Last Revision Date: Tuesday, July 03, 2001
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http://www.msi.com.tw		

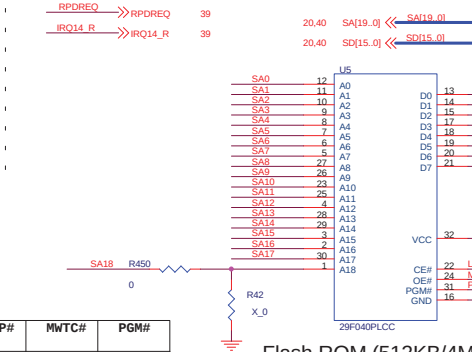
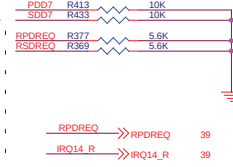
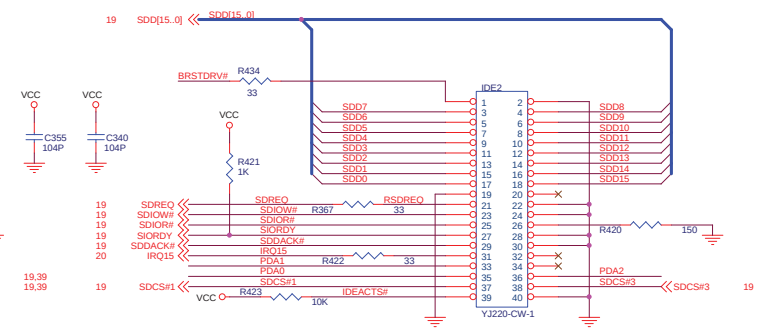
POWER TRACE
全部走20mil寬

USB Connectors

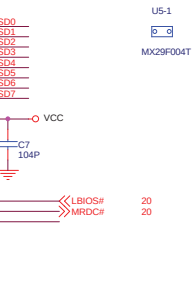


PRIMARY IDE CONN.

1.IDE 同一channel等長
2.trace spec 5/7/5 mil



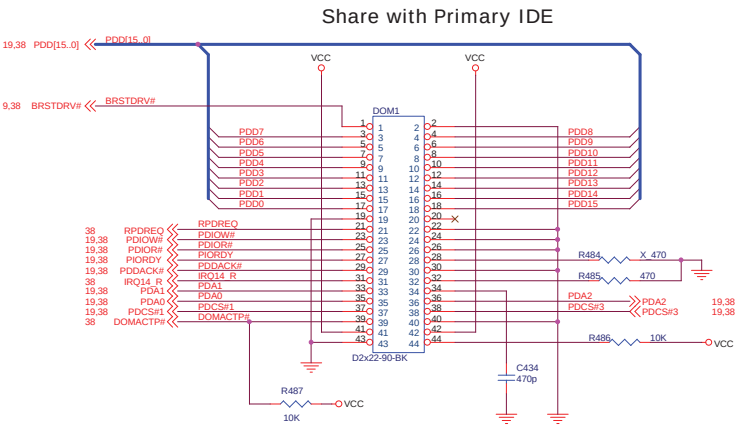
FRWP#	MWTC#	PGM#
L	L	L
L	H	H
H	L	H
H	H	H



Flash ROM (512KB/4M)

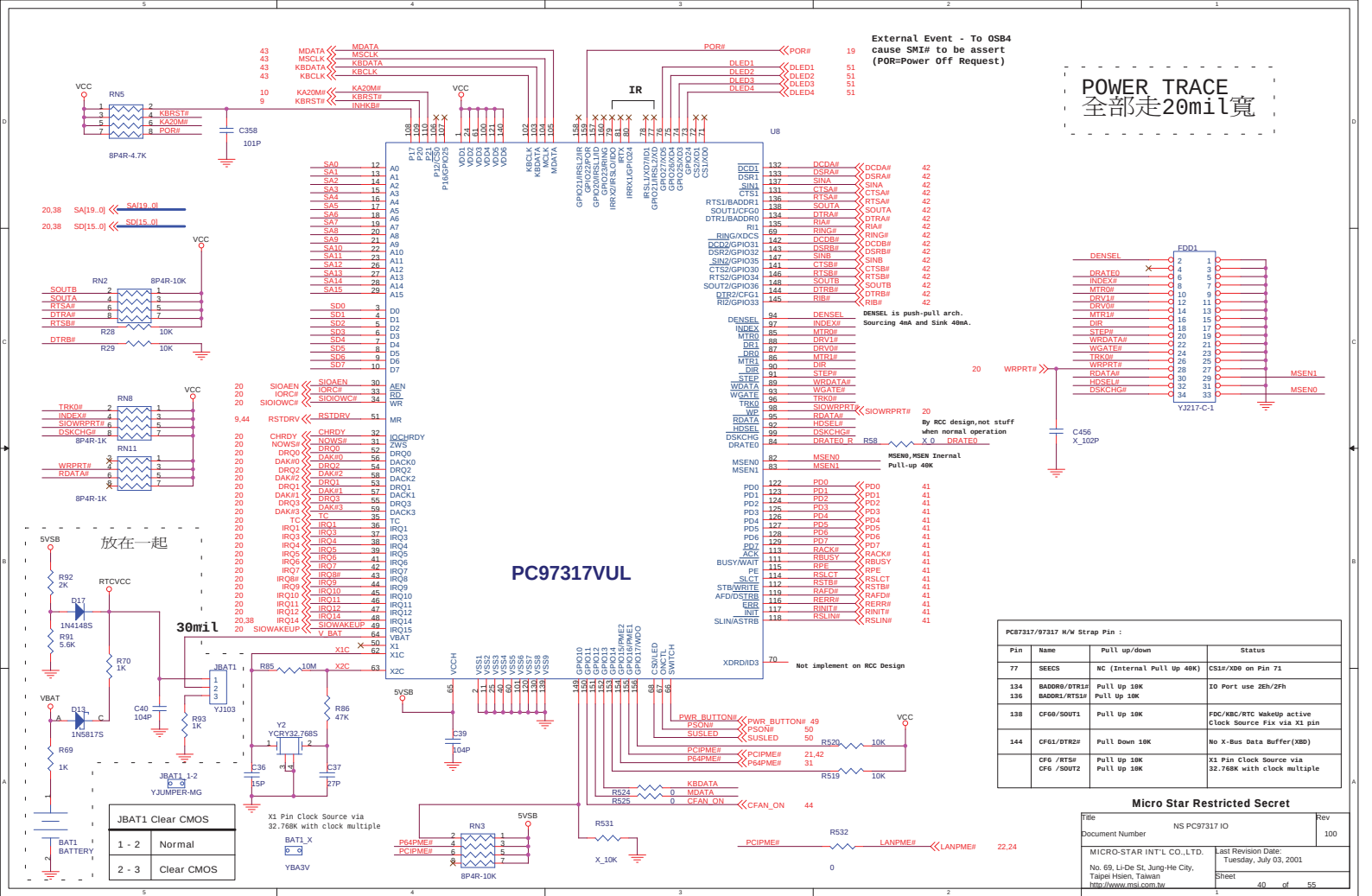
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Title	ATA 66 IDE Connectors	Rev
Document Number		100
MICRO-STAR INT'L CO.,LTD.	Last Revision Date: Tuesday, July 03, 2001	
No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Sheet 38 of 55	

Disk On Module

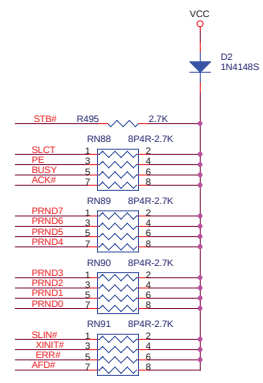
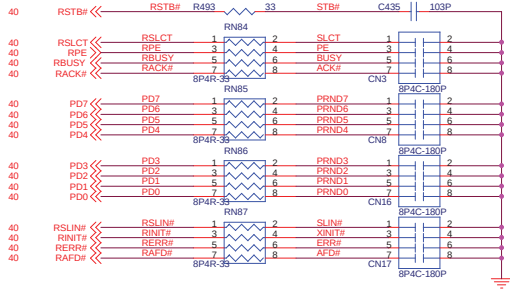
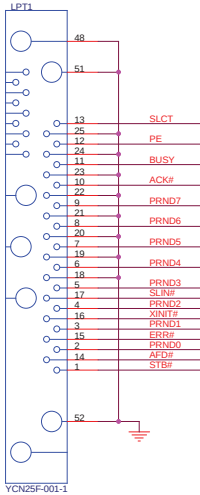


Micro Star Restricted Secret

Title		Rev
Disk On Module		100
Document Number		
MICRO-STAR INT'L CO.,LTD.		Last Revision Date:
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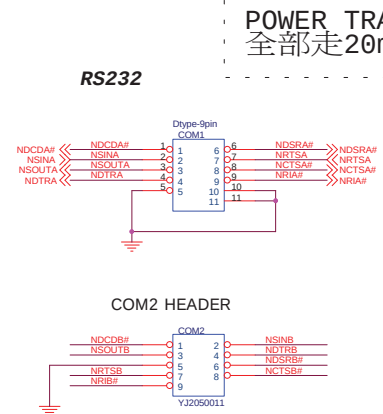
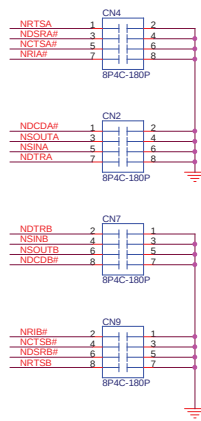
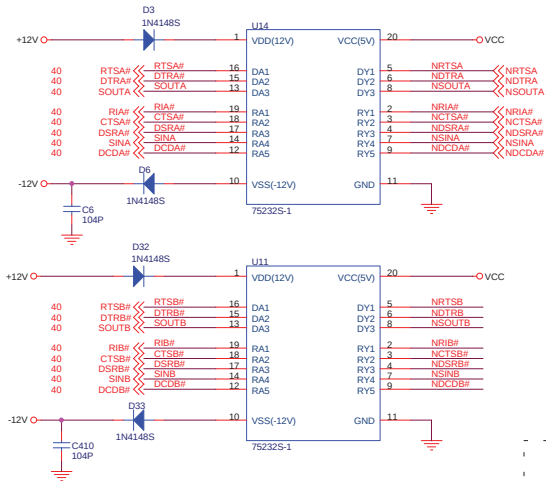
Parallel Port Header



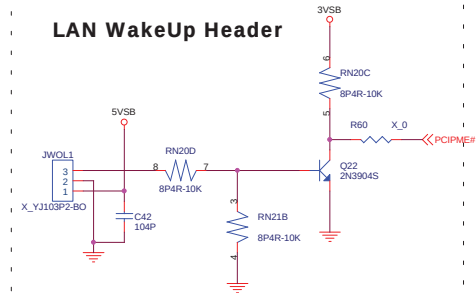
Micro Star Restricted Secret

Title	Parallel Port Header	Rev
Document Number		100
MICRO-STAR INT'L CO.,LTD.	Last Revision Date:	
No. 69, Li-De St, Jung-He City,	Tuesday, July 03, 2001	
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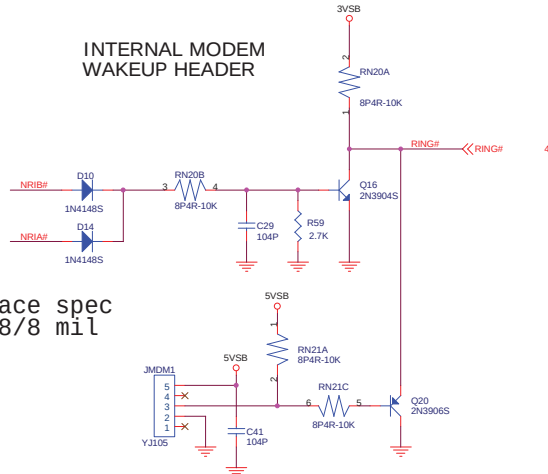
Serial Port/COM Headers



LAN WakeUp Header



INTERNAL MODEM WAKEUP HEADER



trace spec
8/8/8 mil

POWER TRACE
全部走20mil寬

RS232

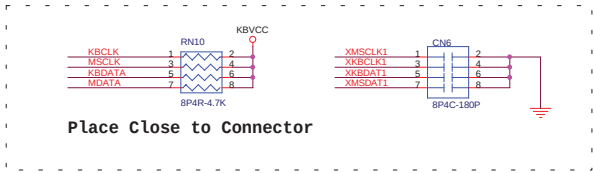
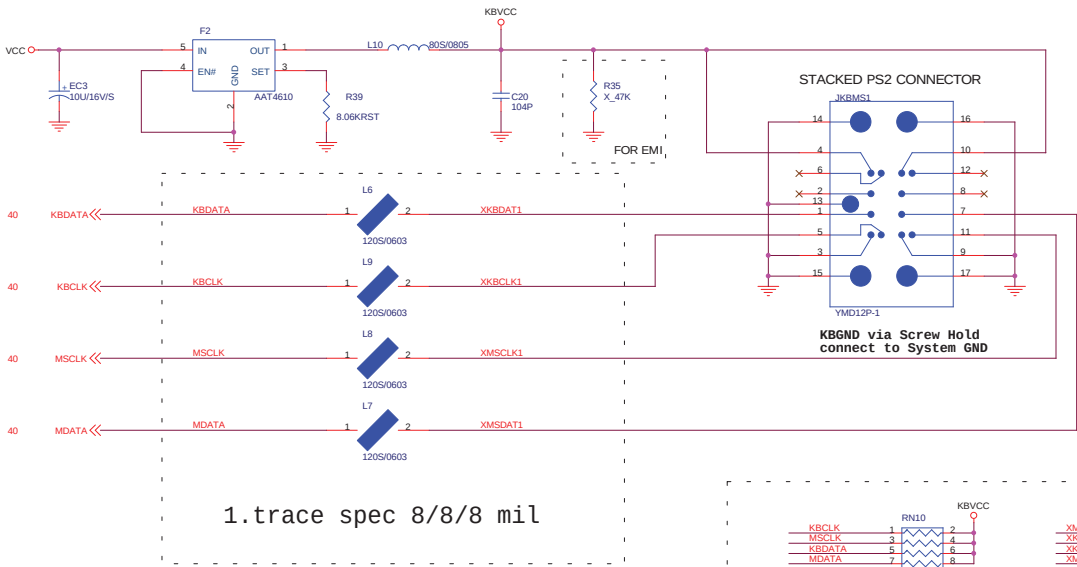
COM2 HEADER

Micro Star Restricted Secret

Title	Serial Port Header	Rev
Document Number		100
MICRO-STAR INT'L CO., LTD.		Last Revision Date:
No. 69, Li-De St. Jung-He City,		Tuesday, July 24, 2001
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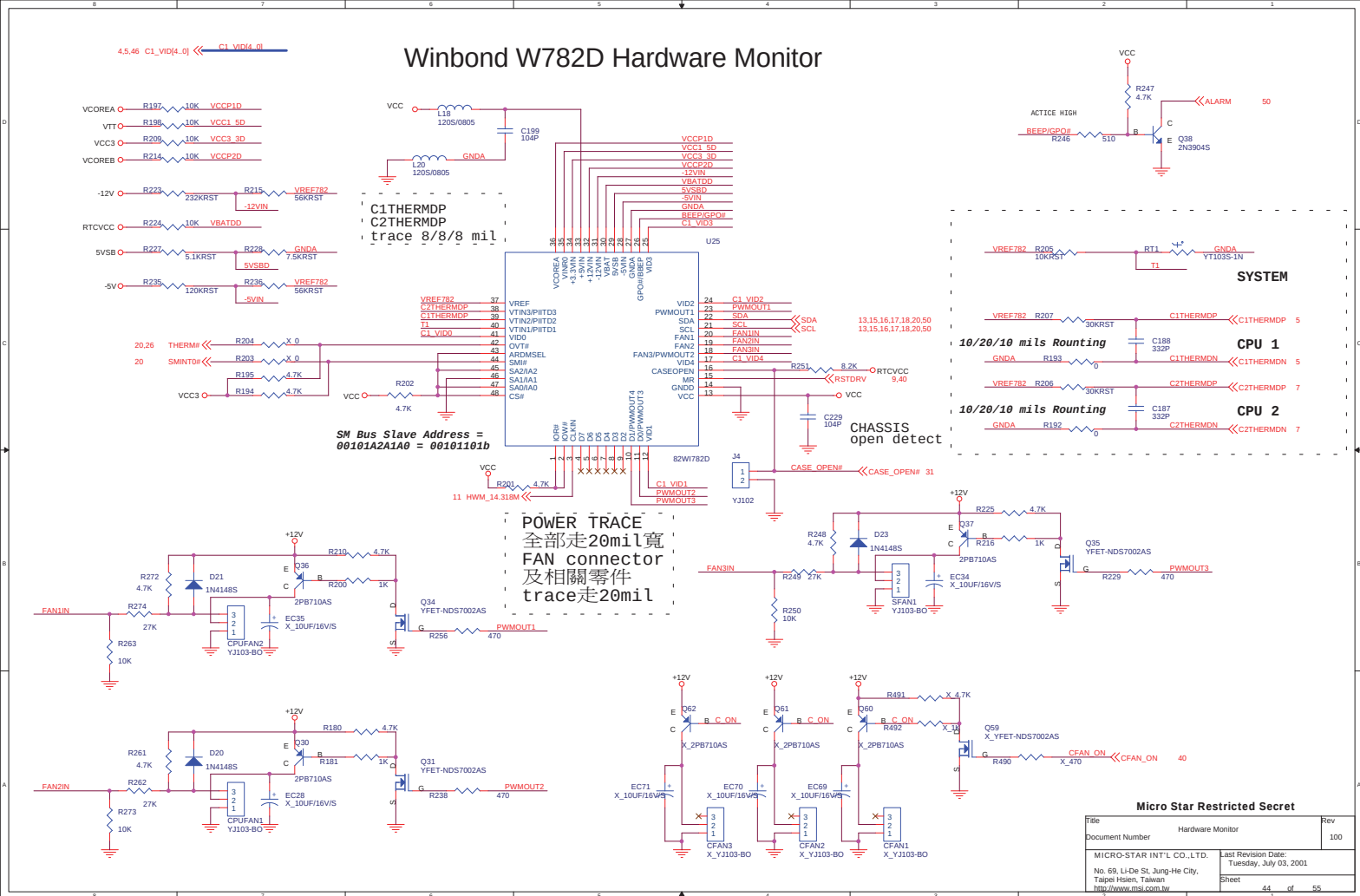
Keyboard/Mouse Ports

POWER TRACE
全部走20mil寬

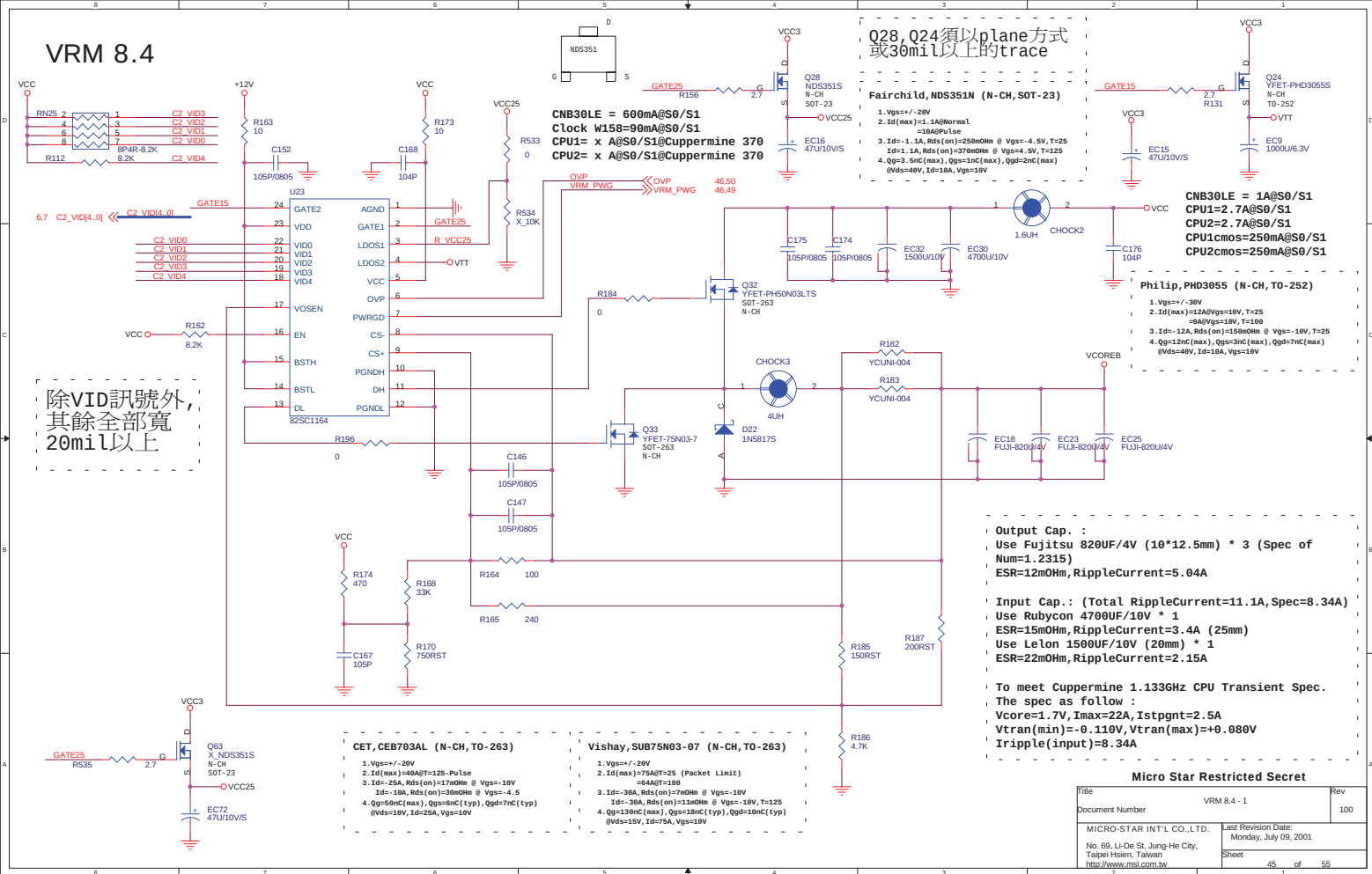


Micro Star Restricted Secret		
Title	Keyboard/Mouse Ports	Rev
Document Number		100
MICRO-STAR INT'L CO.,LTD.		Last Revision Date:
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Winbond W782D Hardware Monitor

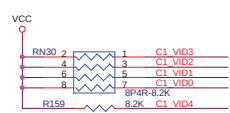


VRM 8.4



除VID訊號外，其餘全部寬20mil以上

4.544 C1_VID[4:0] << C1_VID[4:0]

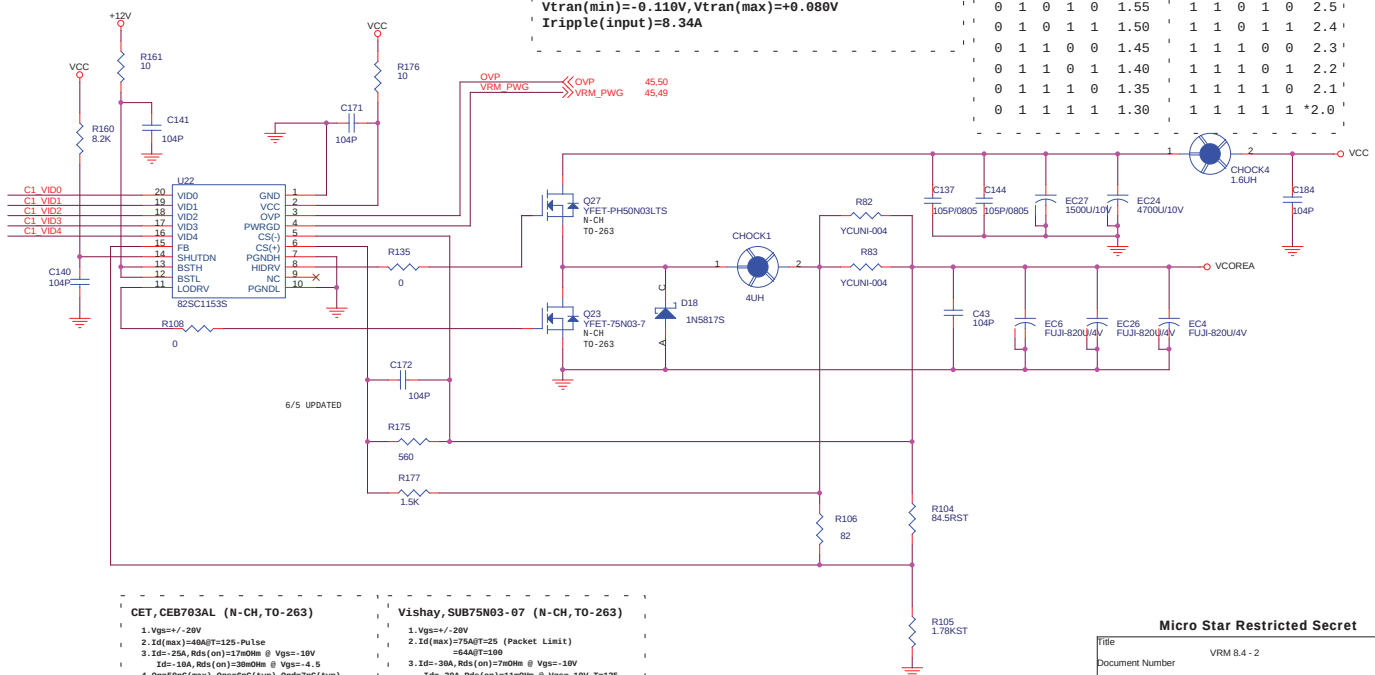


Output Cap. :
Use Fujitsu 820UF/4V (10*12.5mm) * 3 (Spec of Num=1.2315)
ESR=12mOHm, RippleCurrent=5.04A

Input Cap.: (Total RippleCurrent=11.1A, Spec=8.34A)
Use Rubycon 4700UF/10V * 1
ESR=15mOHm, RippleCurrent=3.4A (25mm)
Use LeIon 1500UF/10V (20mm) * 1
ESR=22mOHm, RippleCurrent=2.15A

To meet Coppermine 1.133GHz CPU Transient Spec.
The spec as follow :
Vcore=1.7V, I_{max}=22A, Istpgnt=2.5A
V_{tran}(min)=-0.110V, V_{tran}(max)=+0.080V
I_{ripple}(input)=8.34A

D4	D3	D2	D1	D0	Vs	D4	D3	D2	D1	D0	Vs
0	0	0	0	0	2.05	1	0	0	0	0	3.5
0	0	0	0	1	2.00	1	0	0	0	1	3.4
0	0	0	1	0	1.95	1	0	0	1	0	3.3
0	0	0	1	1	1.90	1	0	0	1	1	3.2
0	0	1	0	0	1.85	1	0	1	0	0	3.1
0	0	1	0	1	1.80	1	0	1	0	1	3.0
0	0	1	1	0	1.75	1	0	1	1	0	2.9
0	0	1	1	1	1.70	1	0	1	1	1	2.8
0	1	0	0	0	1.65	1	1	0	0	0	2.7
0	1	0	0	1	1.60	1	1	0	0	1	2.6
0	1	0	1	0	1.55	1	1	0	1	0	2.5
0	1	0	1	1	1.50	1	1	0	1	1	2.4
0	1	1	0	0	1.45	1	1	1	0	0	2.3
0	1	1	0	1	1.40	1	1	1	0	1	2.2
0	1	1	1	0	1.35	1	1	1	1	0	2.1
0	1	1	1	1	1.30	1	1	1	1	1	2.0

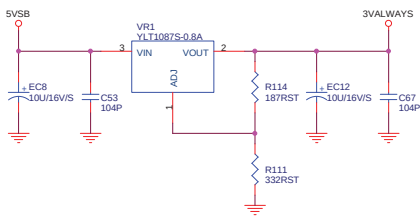


CET, CEB703AL (N-CH, TO-263)	Vishay, SUB75N03-07 (N-CH, TO-263)
1. V _{gs} =+/-20V	1. V _{gs} =+/-20V
2. I _d (max)=48A @ T=125-Pulse	2. I _d (max)=75A @ T=25 (Packet Limit)
3. I _d =25A, R _{ds} (on)=17mOHm @ V _{gs} =10V	3. I _d =30A, R _{ds} (on)=7mOHm @ V _{gs} =10V
I _d =18A, R _{ds} (on)=30mOHm @ V _{gs} =4.5	I _d =30A, R _{ds} (on)=11mOHm @ V _{gs} =10V, T=125
4. Q _g =50nC (max.), Q _{gs} =0nC (typ), Q _{gd} =7nC (typ)	4. Q _g =130nC (max.), Q _{gs} =10nC (typ), Q _{gd} =10nC (typ)
@V _{ds} =10V, I _d =25A, V _{gs} =10V	@V _{ds} =10V, I _d =75A, V _{gs} =10V

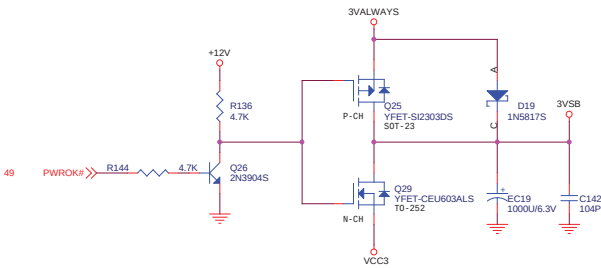
Micro Star Restricted Secret		
File	VRM 8.4 - 2	Rev
Document Number		100
MICRO-STAR INT'L CO., LTD.		Last Revision Date:
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Voltage Regulators

VCC 3SBY Voltage Regulator



以plane方式走線



SI2303DS (P-CH, SOT-23) Spec :

- 1. Vgs=+/-20V
- 2. Id(max)=240A/T=125-Pu1sc
- 3. Id=-1.7A, Rds(on)=210mOhm @ Vgs=-10V, T=25
- Id=-1.3A, Rds(on)=460mOhm @ Vgs=-4.5

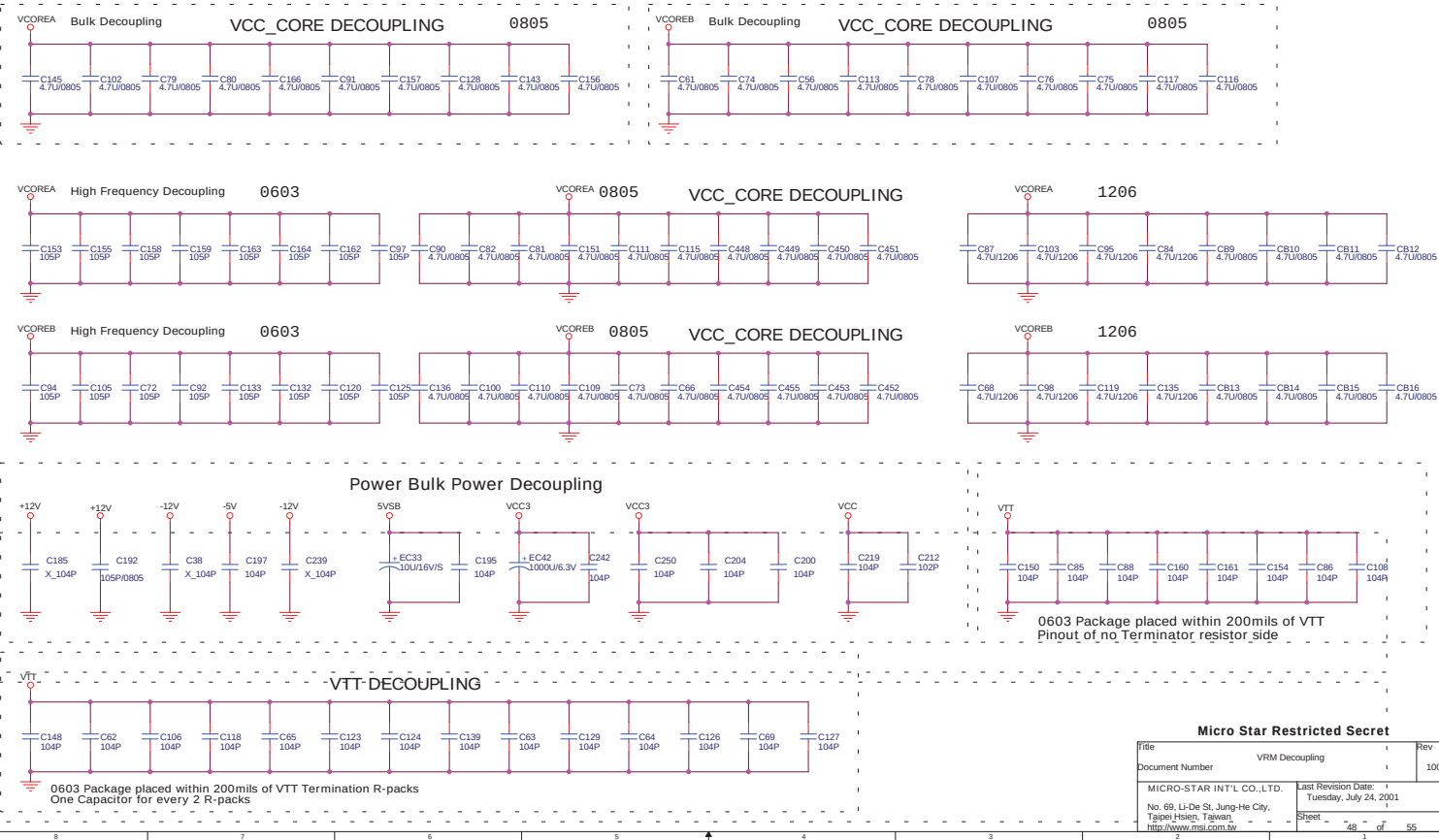
CET, CEU73AL (P-CH, T0-252)

- 1. Vgs=+/-20V
- 2. Id(max)=240A/T=125-Pu1sc
- 3. Id=-25A, Rds(on)=22mOhm @ Vgs=-10V
- Id=-18A, Rds(on)=40mOhm @ Vgs=-4.5
- 4. Qg=48nC(max), Qgs=6nC(typ), Qgd=2nC(typ)
- @Vgs=10V, Lf=25A, Vgs=10V

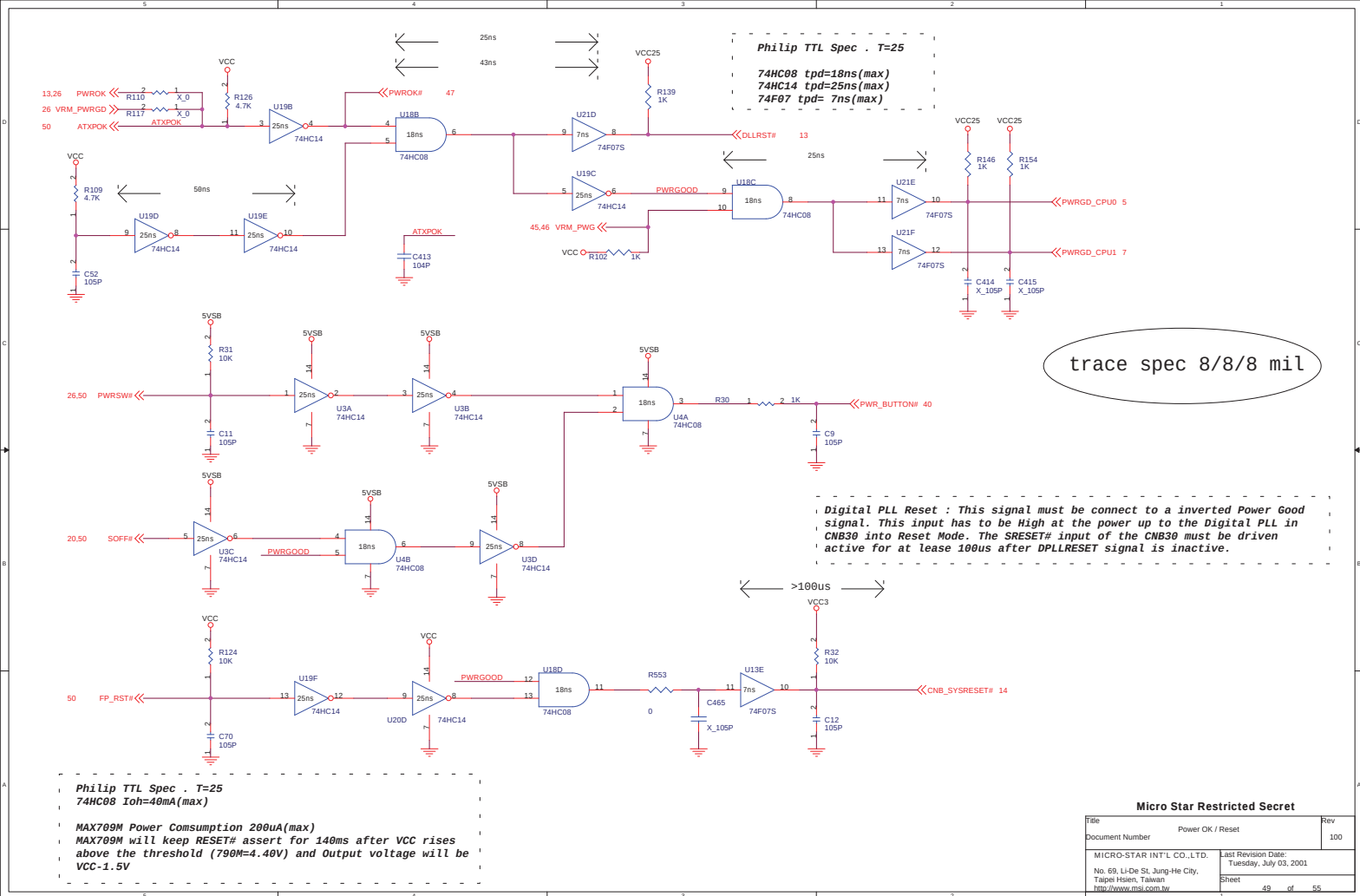
Micro Star Restricted Secret

Title	System Voltage Regulators	Rev
Document Number		100
MICRO-STAR INT'L CO., LTD.	Last Revision Date:	
No. 69, Li-De St, Jung-He City,	Tuesday, July 03, 2001	
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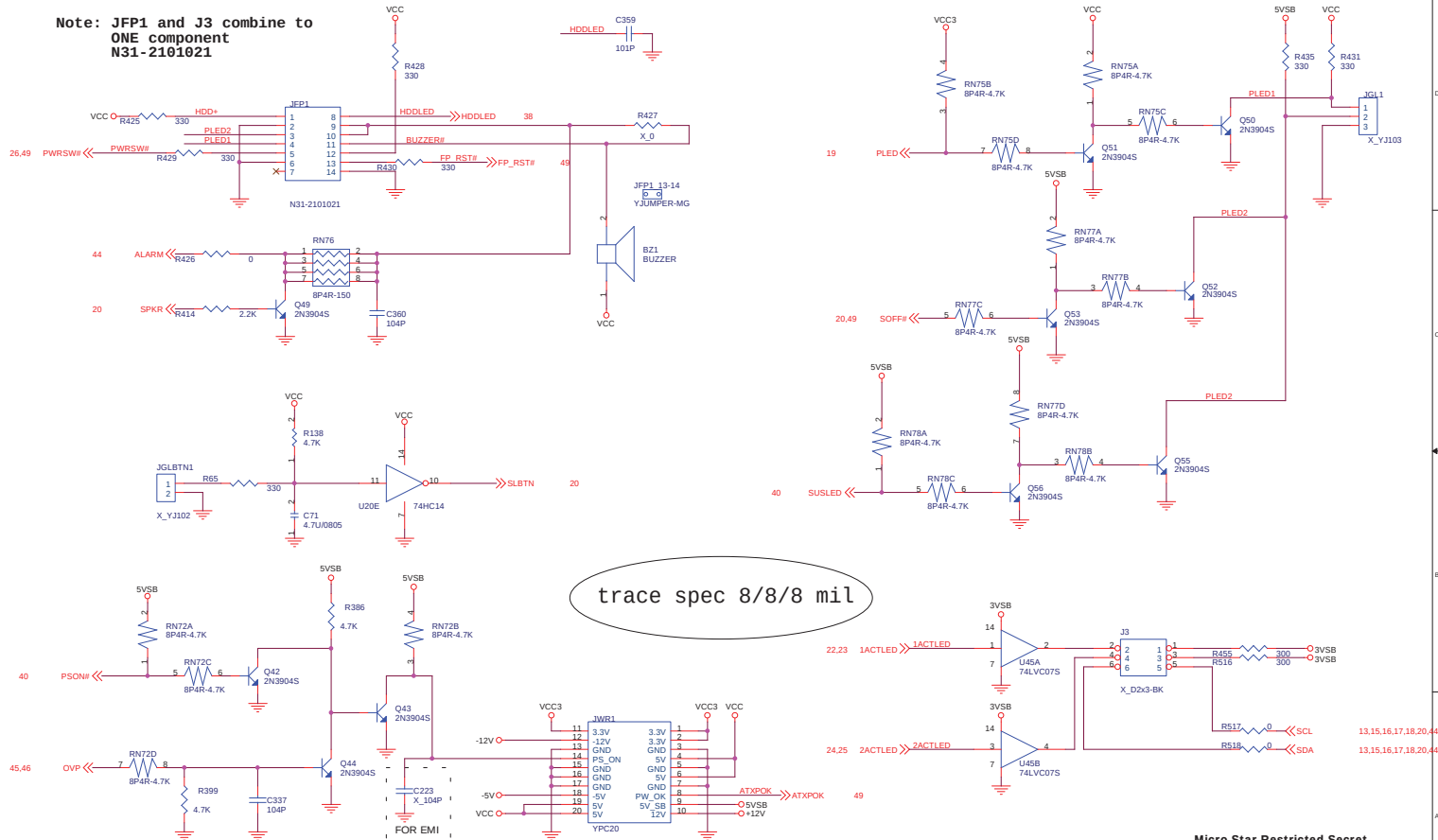
370-pin Socket Decoupling

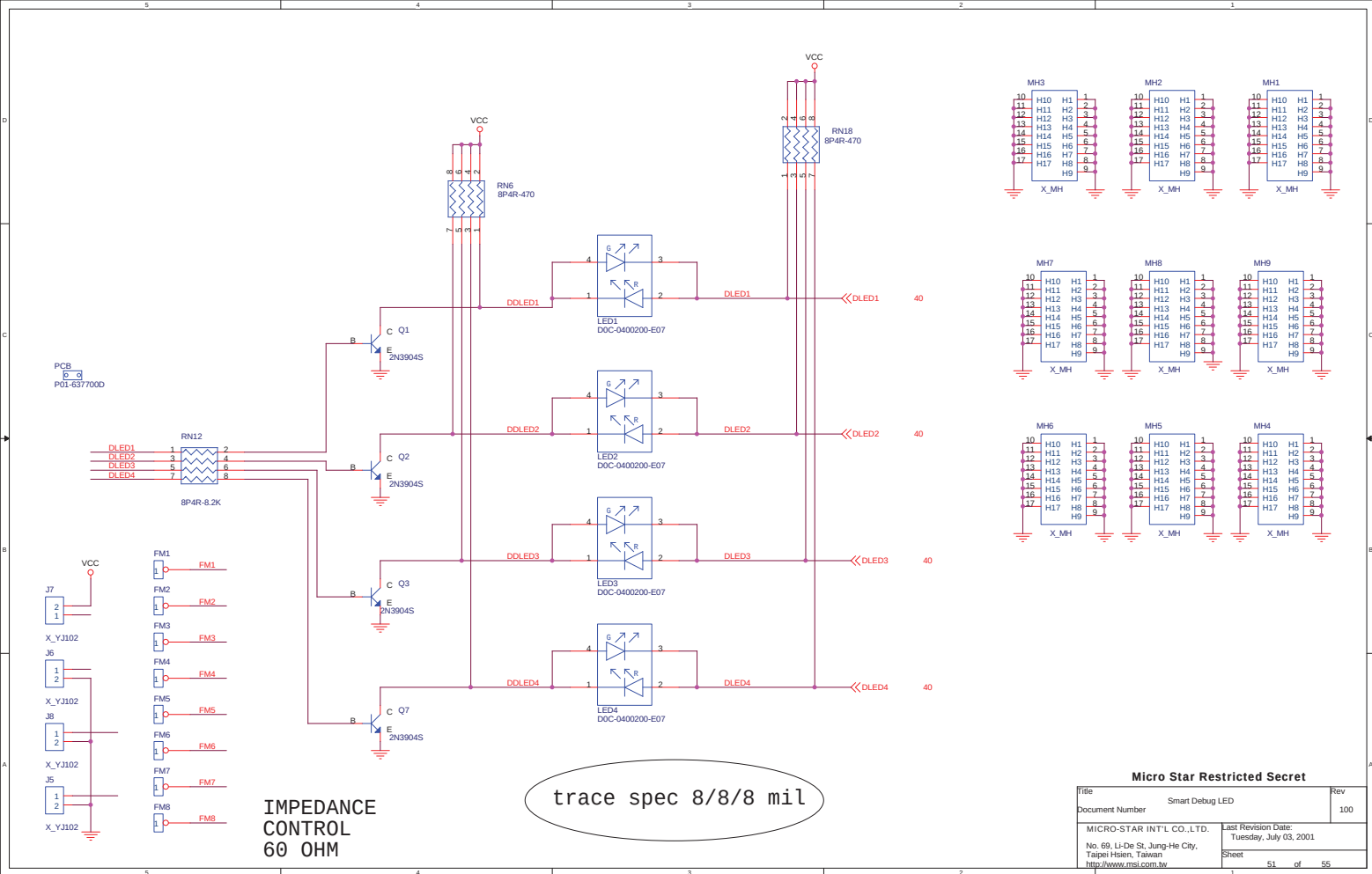


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Title	VRM Decoupling	Rev
Document Number		100
MICRO-STAR INT'L CO.,LTD.		Last Revision Date: Tuesday, July 24, 2001
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Note: JFP1 and J3 combine to
ONE component
N31-2101021





General Spec.

PCI Config.

DEVICE	ICH INT Pin	IDSEL	CLOCK	PIN OUT	R# /G#
PCI SLOT1	INT#0 INT#1 INT#2 INT#3	AD23	PCICLK1		0
PCI SLOT2	INT#1 INT#2 INT#3 INT#0	AD17	PCICLK2		1
PCI SLOT3	INT#2 INT#3 INT#0 INT#1	AD18	PCICLK3		2
OSB4	INT#0 (USB) INT#1 INT#2 INT#3	*AD26 **AD19	SBPCLK		X
LAN 1	INT#3	AD20	1LANPCLK		3
LAN 2	INT#4	AD21	2LANPCLK		4
ATI VGA	INT#5	AD22			5
SCSI	INT#8(I) INT#9(I)	P64AD17	SCSI PCI66		0
PCI66 SLOT5	INT#6 INT#7 INT#8(I) INT#9(I)	P64AD18	P64CLK1		1
PCI66 SLOT6	INT#10 INT#11 INT#12 INT#13	P64AD19	P64CLK2		2

*AD26 = Check on ASUS board
**AD19 = Check on RCC
reference schematic

NS PC97317

GPIO Pin	Type	Function	Pin Number
GPIO 24	I/O	DLED4	73
GPIO 25	I/O	DLED3	74
GPIO 26	I/O	DLED2	75
GPIO 27	I/O	DLED1	76
GPIO 10	I/O	LAN PME# Event	149
GPIO 11	I/O	CFAN_ON	150
GPIO 12	I/O	MOUSE WAKE UP EVENT	151
GPIO 13	I/O	KEYBOARD WAKE UP EVENT	152
GPIO 14	I/O	Pull Up to 5V with 10K ohm	153
GPIO 15	I/O	PCI64 Bus PME# Event	154
GPIO 16	I/O	PCI32 Bus PME# Event	155
GPIO 17	I/O	Pull Up to 5V through 10K ohm	156
CS0/LED	I/O	Suspend LED	68
CS1/XD0	I/O	NC	71
GPIO22/POR	I/O	POR - External Event	159
P17	I/O	Pull Up to 5V with 4.7K ohm	108
P18	I/O	KB Reset#	109
P19	I/O	A20 Mask	110

DRAM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	1010000B	DCLK0
DIMM 2	1010001B	DCLK1
DIMM 3	1010010B	DCLK2
DIMM 4	1010011B	DCLK3

W83782D	01011010B(5A)
82550	11001000B

Micro Star Restricted Secret

Title	General Spec.		Rev
Document Number			100
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-Hsi City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Tuesday, July 03, 2001	
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General Spec.

ROSB General Purpose Event List			
Pin	Event	Orginal Signal	MS6377 Implement
V1_18	GEVENT_0	ACPI General Purpose Event	CPU 1 SERR# Event
U3_207	GEVENT_1	ACPI General Purpose Event	CPU 2 SERR# Event
W2_118	GEVENT_2	ACPI General Purpose Event	CPU 1 THERMTRIP# Event
V3_208	GEVENT_3	ACPI General Purpose Event	CPU 2 THERMTRIP# Event
W4_292	GEVENT_4	ACPI General Purpose Event	P2ALERT
Y3_210	GEVENT_5	ACPI General Purpose Event	SMINT0#,W83782D SMI Event)
W1_19	GEVENT_6	ACPI General Purpose Event	THERM#,W83782D Thermer Evvent)
Y2_119	GEVENT_7	ACPI General Purpose Event	Not Use. Pull Down
W26_58	GEVENT_8	General Purpose Chip Select 0	Not Use. NC.
W25_153	GEVENT_9	General Purpose Chip Select 1	Not Use. NC.
Y24_239	GEVENT_10	General Purpose Chip Select 2	Not Use. NC.
AF9_34	GEVENT_11	GP#0	Not Use. PULL-HIGH.
C26_74	GEVENT_12	General Purpose Port	Not Use. PULL-HIGH.
C24_255	GEVENT_13	General Purpose Port	Not Use. PULL-HIGH.
C25_169	GEVENT_14	General Purpose Port	Not Use. PULL-HIGH.
D26_168	GEVENT_15	GP for Backplane	Not Use. PULL-HIGH. (CLRNVRAM#)
AC14_306	GEVENT_16	USB Test Mode Enable	Not Use. NC.
AF10_35	GEVENT_17	USB Test Mode Select 1	Not Use. NC.
AE11_133	GEVENT_18	USB Interrupt	Not Use. NC.
E25_167	GEVENT_19	Super IO Address Enable	SIOAEN.Super IO Address Enable
G24_252	GEVENT_20	Super IO Write/Previously MIDCLK	SIOWC#.Super IO Write Command
AE9_131	GEVENT_21	Flash ROM Write	FRWP#.Flash ROM Write Protect
F26_71	GEVENT_22	CPU Stop CLK	Not Use. NC.
E26_72	GEVENT_23	PCI Stop CLK /Previously MIDIN	Not Use. NC.
AE8_130	BLINK	BLINK	POWER LED (PLED1)
C1_3	SLPBTN	SLPBTN	SLEEP BUTTON
Program on OSB 2.4.4.39 to 2.4.4.50 : GPEConfiguration /Input Level/Status Register			

PC97317 POR#,SCI,ONCTL# Generation	
POR# Generator :	
* SMI Command ACPI Global Lock Release Sleep Enable Select Rising/Falling/High/Low(GPIO12, GPIO13, P12) Select Rising/Falling/High/Low(PME1, PME2, IRRX1, IRRX2, GPIO10) Switch Off Event(SWITCH#) MS-6377 Implement :	
GP010 : GP012 : GP013 : GP015/PME2 : P64PME# GP016/PME1 : PCIPME# P12/CS0# : NC IRRX1 : NC IRRX2 : NC	
* SCI Generator :	
RTC Alarm Power Management Timer Switch Off Event(SWITCH#) BIOS Global Lock Release Select Rising/Falling/High/Low(GPIO12, GPIO13, P12) Select Rising/Falling/High/Low(PME1, PME2, IRRX1, IRRX2, GPIO10) Pulse/Tran Select(RING#,RI1#,RI2#) MATCH	
* ONCTL# Generator :	
RTC Alarm Fail Safe Timer Select Rising/Falling/High/Low(GPIO12, GPIO13, P12) Select Rising/Falling/High/Low(PME1, PME2, IRRX1, IRRX2, GPIO10) Switch Off Event(SWITCH#) Switch On Event(SWITCH#) Pulse/Tran Select(RING#,RI1#,RI2#) MATCH	

CNB30LE DRAM Support List		
Generation	Depth	Size/Row
16M 2-Banks SDRAM	11/9	16MB
	11/10	32MB
64M 2-Banks SDRAM	13/10	128MB
64M 4-Banks SDRAM	12/9	32MB
	12/9	64MB
	12/10	128MB
	13/10	256MB**
	12/9	64MB
128M 4-Banks SDRAM	12/10	128MB**
	13/10	256MB**
	*12/11	256MB
256M 4-Banks SDRAM	13/8	64MB
	13/9	128MB
	13/10	256MB
	13/11	512MB
	*12/10	128MB
*Not List in CNB30LE"Table2. MA Mapping for Row and Column Address for SDRAM" ** Not List in CNB30LE "Table 1. Support SDRAMs" table		
TTL Gate Count List :		
TTL	Num.	Locate (Free Gate)
74F07	3	U10(1),U6(0),U1(0)
74F08	2	U58-5VSB(2)
74F244	2	U7(0),U9(0)
74HC08	1	U2(0)
74HC14	3	U5(1),U16(0),U57-5VSB(2)
74HC273	1	U8(0)
74LVC07	1	U3(0)

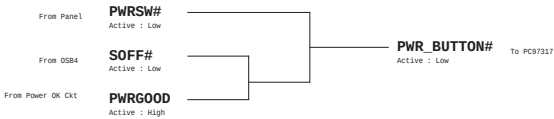
Intel PC SDRAM Register DIMM Spec :		
Type	PLL	Support
64MByte 72bit ECC SDRAM	Non	No
64MByte 72bit ECC SDRAM	Yes	Yes
72bit ECC Stacked SDRAM (2 Rows)	Yes	Yes
256MB using 16M*4 (64Mbit) SDRAMs		
512MB using 32M*4 (128Mbit) SDRAMs		
1GB using 64M*4 (256Mbit) SDRAMs		
72bit ECC Unstacked SDRAM (1 Row)	Yes	Yes
128MB using 16M*4 (64Mbit) SDRAMs		
256MB using 32M*4 (128Mbit) SDRAMs		
512MB using 64M*4 (256Mbit) SDRAMs		
Note : 1.With PLL = CK0 -> PLL , CK1,CK2,CK3 Terminated 2.Register Signal : S0#/S2# (Chip Selset) D0MB[0..7] (DQ Mask) BA[0..1] (Bank Select) A[0..12] (Address) RAS# (Row Address Strobe) CAS# (Column Address Strobe) CKE0 (Clock Enable) WE# (Write Enable)		

Micro Star Restricted Secret

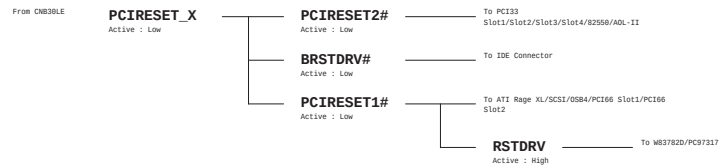
Title	Genreal Spec.		Rev
Document Number			100
MICRO-STAR INT'L CO.,LTD. No. 69 Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, July 03, 2001		
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General Spec.

Power Button Event Ckt :



System Reset Map :



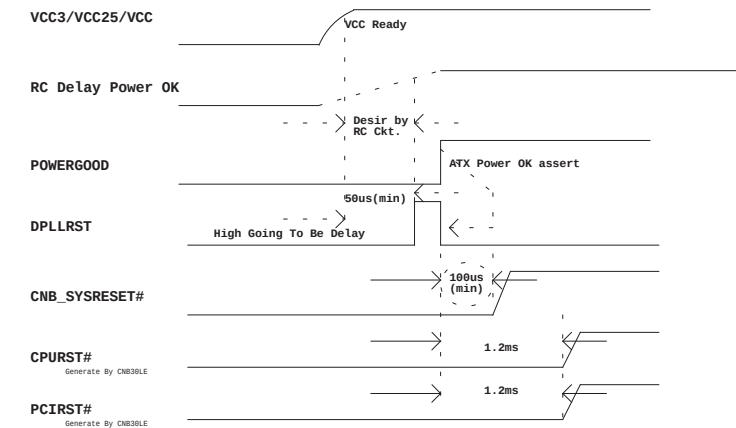
Panel Reset Button Event Ckt :



System Power OK Architecture :



Reset Timing :

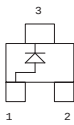


Micro Star Restricted Secret

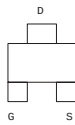
Title	Genreal Spec.	Rev
Document Number		100
MICRO-STAR INT'L CO.,LTD. No. 69 Li-De St, Jung-He City, Taiper Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, July 03, 2001	
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BAS70



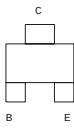
2N7002



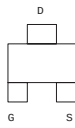
CEU603



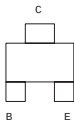
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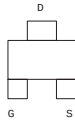
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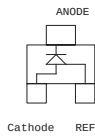
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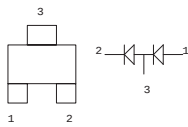
Si2303



LM431



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