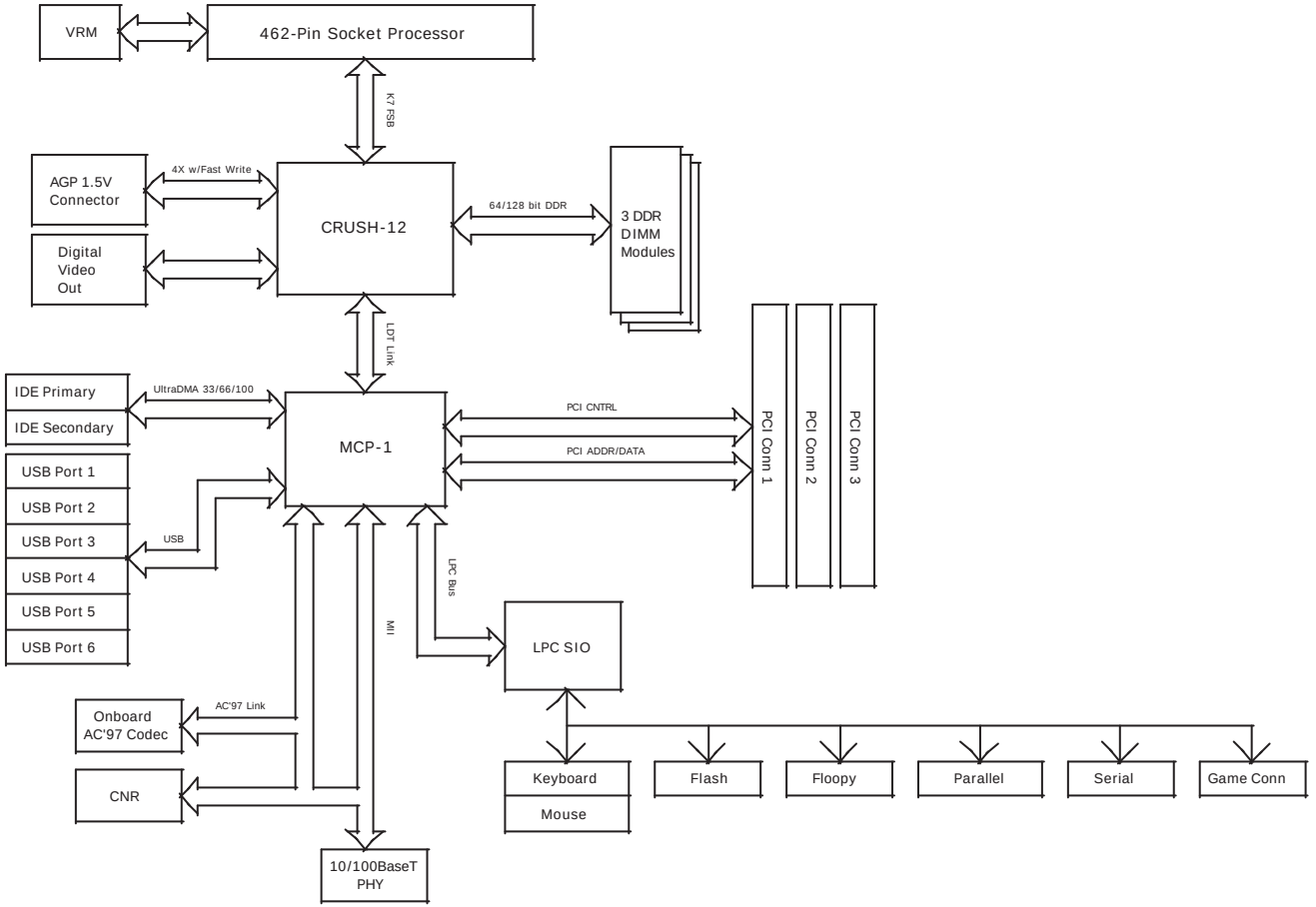
MS-6367 micro-ATX

Revision 0.0D

AMD Socket A Processor
nVIDIA CRUSH-12/MCP-1 Chipset
Winbond 83627HF-AW LPC I/O

Title: Cover Sheet		Rev: 00D
Document Number: MS-6367		
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Monday, September 03, 2001	Sheet 1 of 50

Block Diagram



Title	Block Diagram	Rev
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General Spec.

MCP-1

GPIO Pin	Type	Function
GPIO 0	I/O	PCI_REQ#4 (multifunction pin)
GPIO 1	I/O	PCI_GNT#4 (multifunction pin)
GPIO 2	I/O	PCI_PERR# (multifunction pin)
GPIO 3	I	PCI_IRQ#E (multifunction pin)
GPIO 4	I	MII_RXER (multifunction pin)
GPIO 5	I	Pull up through 8.2K ohms (LPC_DRQ#1)
GPIO 6	I	USB_OC1# (multifunction pin)
GPIO 7	I	USB_OC2# (multifunction pin)
GPIO 8	I	USB_OC2# (multifunction pin)
GPIO 9	I	USB_OC2# (multifunction pin)
GPIO 10	I	USB_OC2# (multifunction pin)
GPIO 11	I	AC_SDIN1
GPIO 12	I	A20GATE (multifuntion pin)
GPIO 13	O	SPDIF (multifuntion pin)
GPIO 14	I/O	CNR Detected
GPIO 15	I/O	CRUSH Fan Contrl (multifunction pin)
GPIO 16	I/O	Pull Up to 3.3V through 1K ohms (BIOS protect)
GPIO 17	I/O	Pull up through 8.2K ohms (PRDY#)
GPIO 18	I/O	NC(CPUSLP#)
GPIO 19	I/O	SLPBTN# (multifunction pin)
GPIO 20	I/O	SLP_S1# (multifunction pin)
GPIO 21	I/O	EXTSMI# (multifunction pin)
GPIO 22	I/O	THERM# (multifuntion pin)
GPIO 23	I/O	Pull up through 10M ohms to 1.2V(INTRUDER#)
GPIO 24	I/O	RI# (multifuntion pin)
GPIO 25	I/O	KBRST# (multifuntion pin)
SPIO 0	I/O	SM_CLK0 (multifuntion pin)
SPIO 1	I/O	SM_DATA0 (multifuntion pin)
SPIO 2	I/O	SM_CLK1 (multifuntion pin)
SPIO 3	I/O	SM_DATA1 (multifuntion pin)
SPIO 4	I/O	DDC_CLK (multifuntion pin)
SPIO 5	I/O	DDC_DATA (multifuntion pin)
SPIO 6	I	Pull up through 4.7K ohms (SMB_ALERT#)

BIOS Protect Config.	
BIOS Un_Protected	1
BIOS Protected	0

SPDIF output control Config.	
Analog output	1(default)
SPDIF output	0

STR Control Config.	GPIO23
Power Off	1
Power On / Disable	1
Before Enter S3	0

PCI Config.

DEVICE	MCP1 INT Pin	REQ# / GNT#	IDSEL	CLOCK	CLK GEN PIN OUT
PCI Slot 1	INTA# INTB# INTC# INTD#	PCI_REQ#0 PCI_GNT#0	AD16	PCICLK0	MCP1/AB20 (PCI_CLK0)
PCI Slot 2	INTB# INTC# INTD# INTA#	PCI_REQ#1 PCI_GNT#1	AD17	PCICLK1	MCP1/AB18 (PCI_CLK1)
PCI Slot 3	INTC# INTD# INTA# INTB#	PCI_REQ#2 PCI_GNT#2	AD18	PCICLK2	MCP1/AB12 (PCI_CLK2)
PCI Slot 4 (RESVD)	INTE#	PCI_REQ#3 PCI_GNT#3	AD19	PCICLK4	MCP1/AB6 (PCI_CLK4)

LPC

GPIO Pin	Type	Function
GPIO 24	I/O	SPDIF output control.
GPIO 32	I/O	Secondary IDE ATA66/100 detection (ATADET1)
GPIO 33	I/O	Primary IDE ATA66/100 detection (ATADET0)

LPC Flash ROM

GPIO Pin	Type	Function
GPI 0	I	Pull down through 8.2K ohms (unused)
GPI 1	I	Pull down through 8.2K ohms (unused)
GPI 2	I	Pull down through 8.2K ohms (unused)
GPI 3	I	Pull down through 8.2K ohms (unused)
GPI 4	I	Pull down through 8.2K ohms (unused)

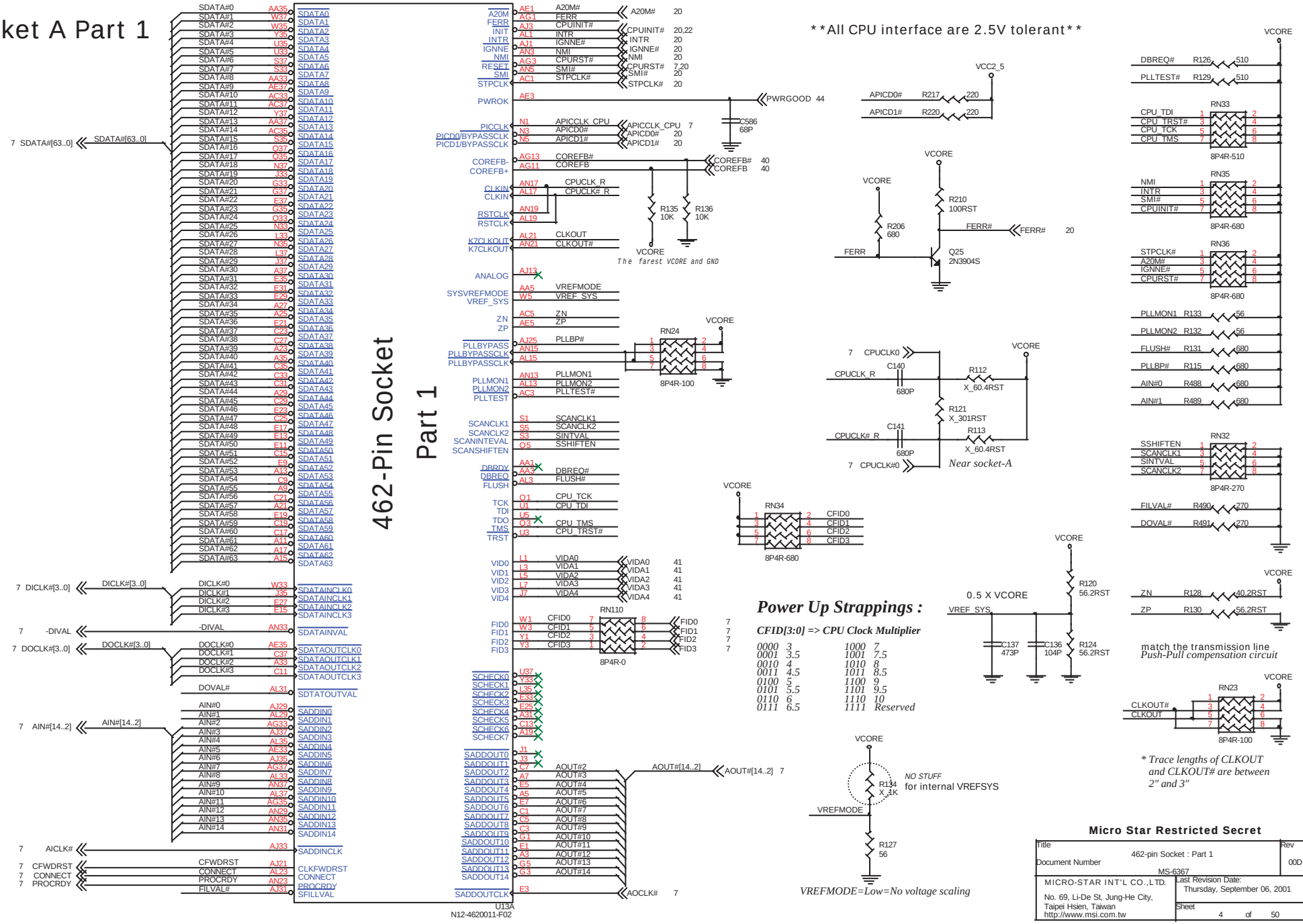
DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	1010000B	MCLK_A0/MCLK_A0# MCLK_A1/MCLK_A1# MCLK_A2/MCLK_A2#
DIMM 2	1010001B	MCLK_B0/MCLK_B0# MCLK_B2/MCLK_B2# MCLK_B4/MCLK_B4#
DIMM 3	1010010B	MCLK_B1/MCLK_B1# MCLK_B3/MCLK_B3# MCLK_B5/MCLK_B5#

SMBUS Config.

DEVICE	ADDRESS
LPC IO	0101101B
MII EEPROM	1010011B
CNR	1010100B

Socket A Part 1



All CPU interface are 2.5V tolerant

Power Up Strappings :

CFID[3:0] => CPU Clock Multiplier

0000	3	1000	7
0001	3.5	1001	7.5
0010	4	1010	8
0011	4.5	1011	8.5
0100	5	1100	9
0101	5.5	1101	9.5
0110	6	1110	10
0111	6.5	1111	Reserved

Near socket-A

match the transmission line
Push-Pull compensation circuit

** Trace lengths of CLKOUT and CLKOUT# are between 2" and 3"*

NO STUFF
for internal VREFSYS

VREFMODE=Low=No voltage scaling

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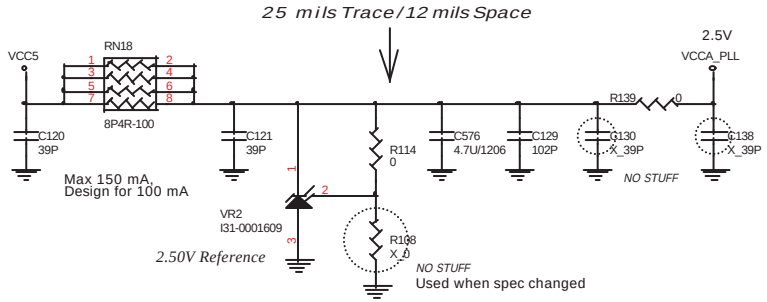
Socket A Part 2

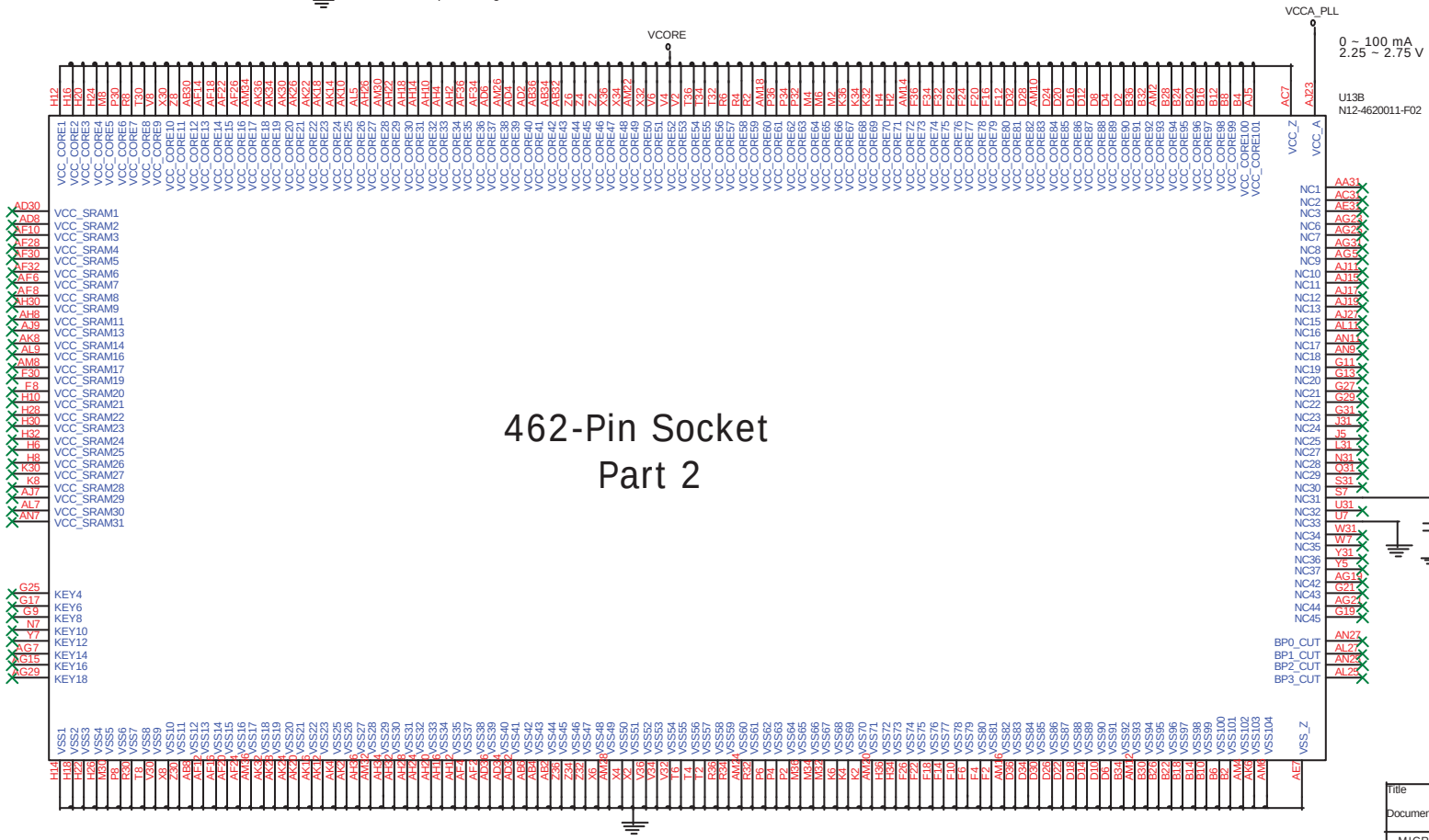


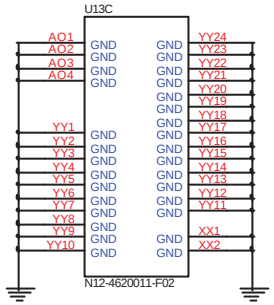
VCCA_PLL trace length from the regulator to the PGA must less be 0.75"

Place all filters close to the PGA

Keep all power and signal trace away from the regulator

Place a cut in GND plane around the VCCA_PLL regulator circuit





For 1.5GHz CPU Fan Holes

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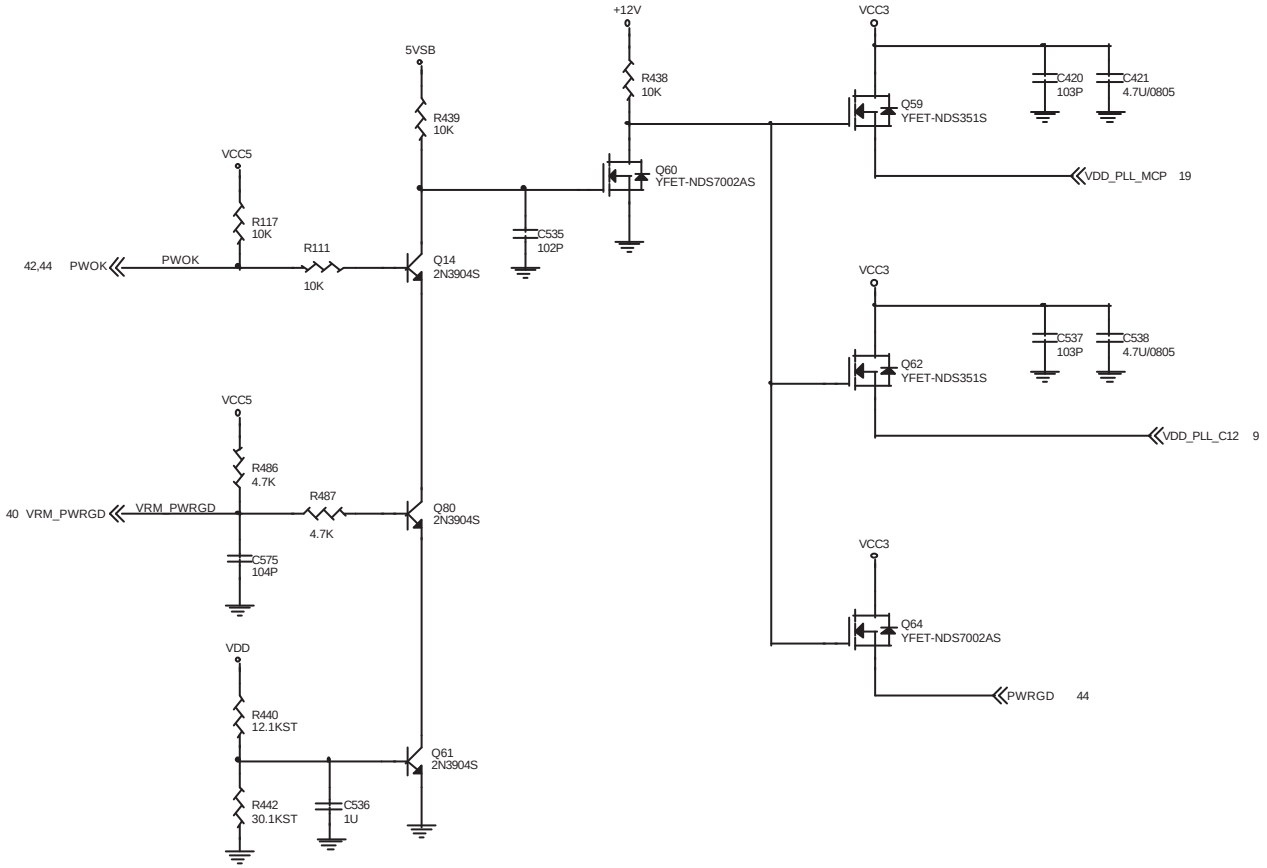
PLL Delay



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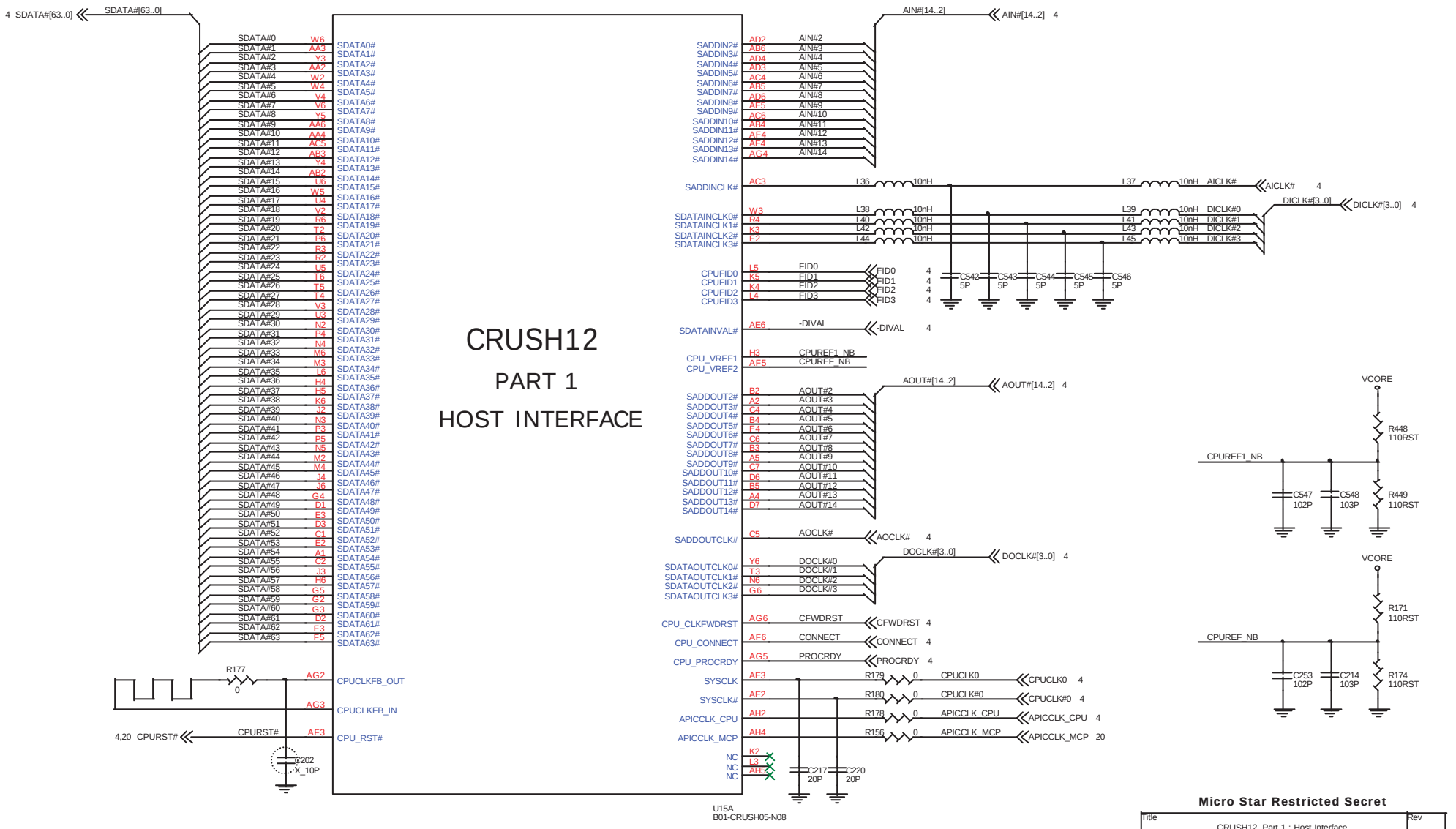
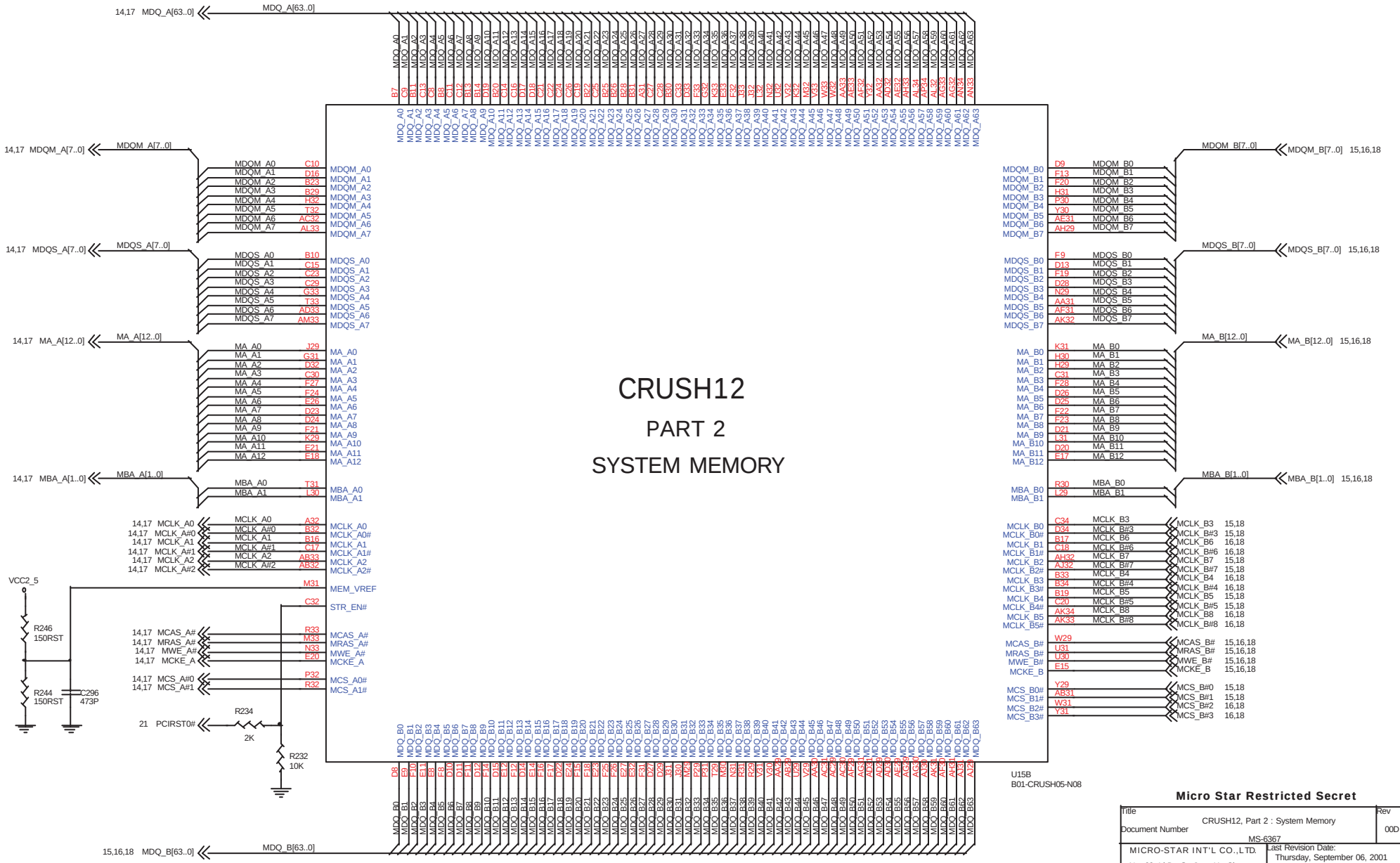
CRUSH12, Part 1 : Host Interface



CRUSH12, Part 2 : Memory Interface



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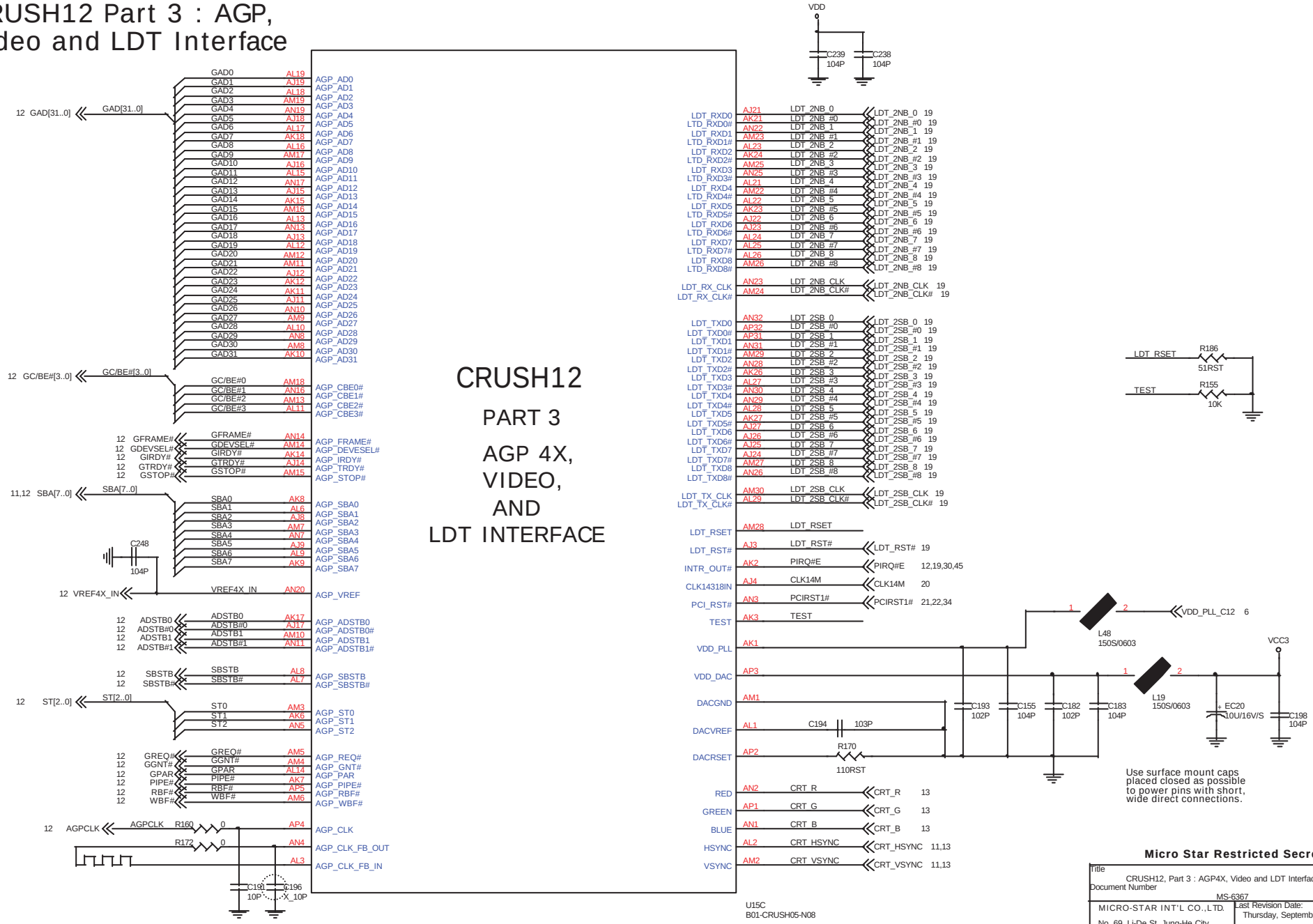
CRUSH12 Part 3 : AGP, Video and LDT Interface



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Title: CRUSH12, Part 3 : AGP4X, Video and LDT Interface	Rev: 00D
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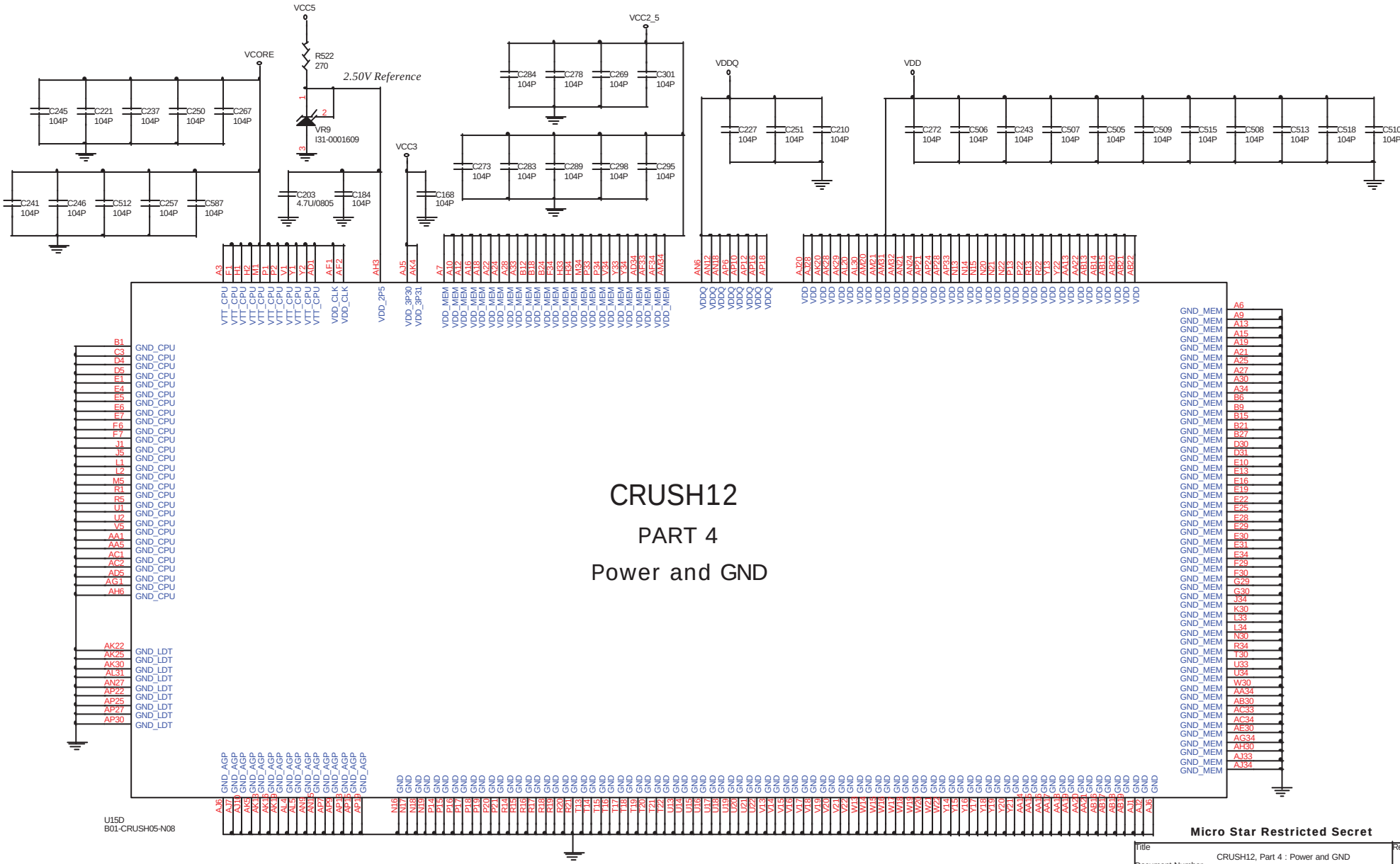
CRUSH Part 4 : Power and GND



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Title	CRUSH12, Part 4 : Power and GND	Rev 00D
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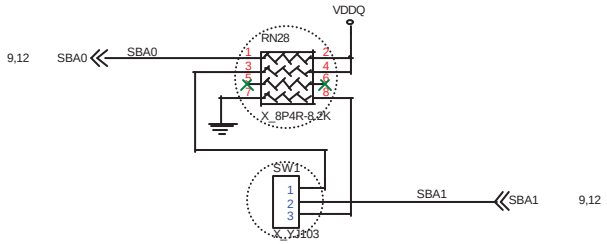
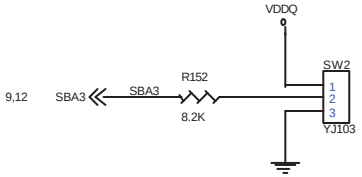
CRUSH12 Strapping Pin



AGP signals SBA[1:0] specify the CPU FSB clock frequency.

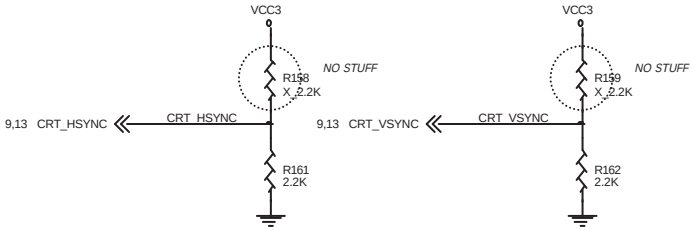
Host Freq.	SBA1	SBA0
66MHz	0	0
100MHz	0	1
RESERVE	1	0
133MHz	1	1



AGP signal SBA3 determine whether to use the USER defined ROm table or the "SAFE' mode ROM table.

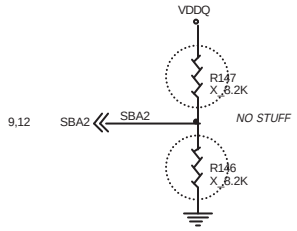
0 = "SAFE" mode table
1 = USER defined table

FSB Mode	SBA3
SAFE	0
AUTO	1



Function		LDT internal terminations		CPU Type strapping	
		Enable	Disable	Intel	AMD
HSYNC	Buffered	0	1	X	X
	Non-Buffered	0*	1	X	X
VSYNC	Buffered	X	X	1	0
	Non-Buffered	X	X	1	0*

Use 10K pu/pd if VSYNC/HSYNC are buffered;
use 2.2K if VSYNC/HSYNC are un-buffered.
* Default



AGP signal SBA2 determine if the CPU FSB frequency should be set based upon the SBA[1:0] straps or those stored in the ROM table.

0 = Use values stored in ROM tables.
1 = AUTO detect by reading SBA[1:0]

FSB Set.	SBA2
ROM	0
AUTO	1

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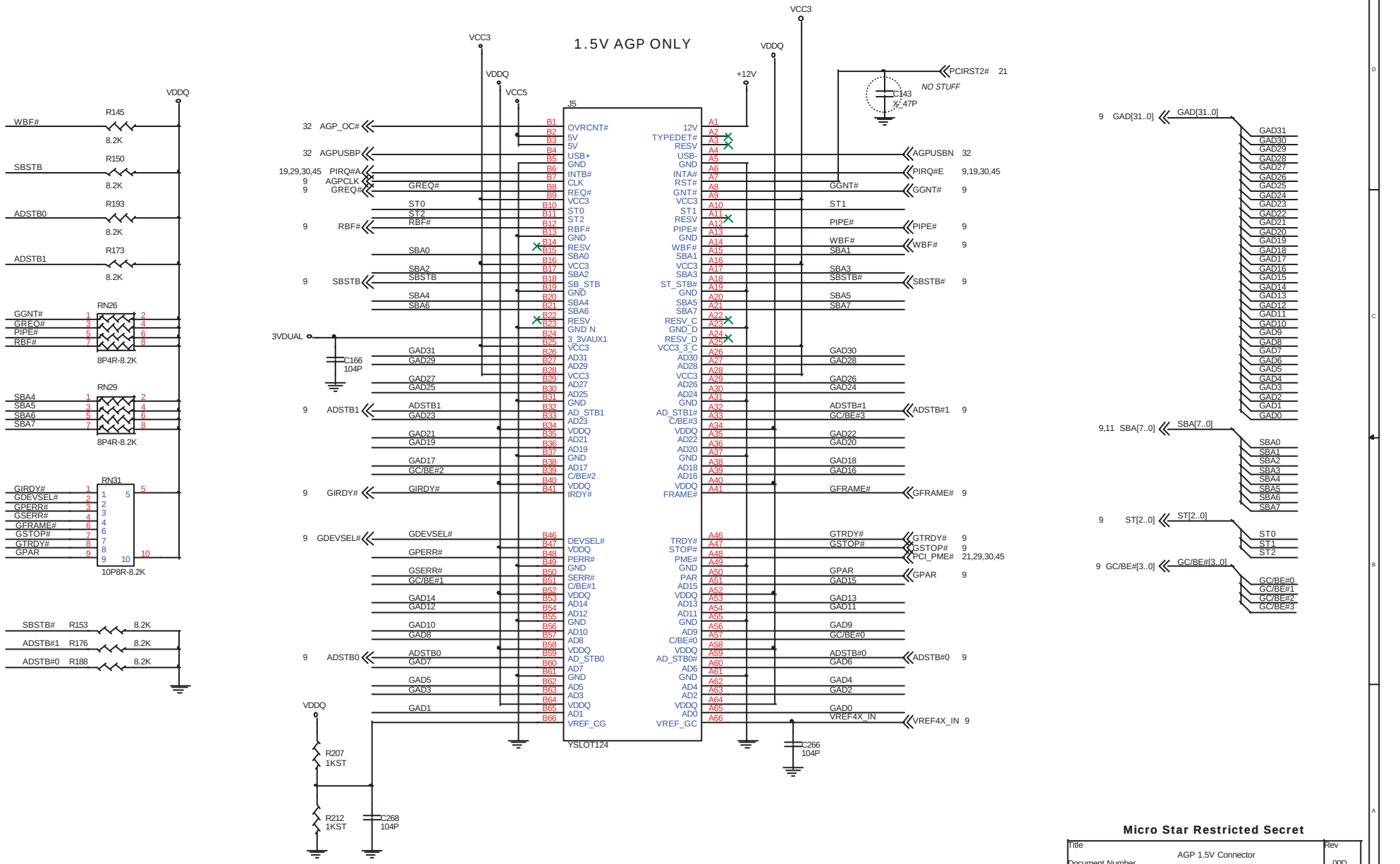
AGP 1.5V Connector



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Title	AGP 1.5V Connector	Rev 00D
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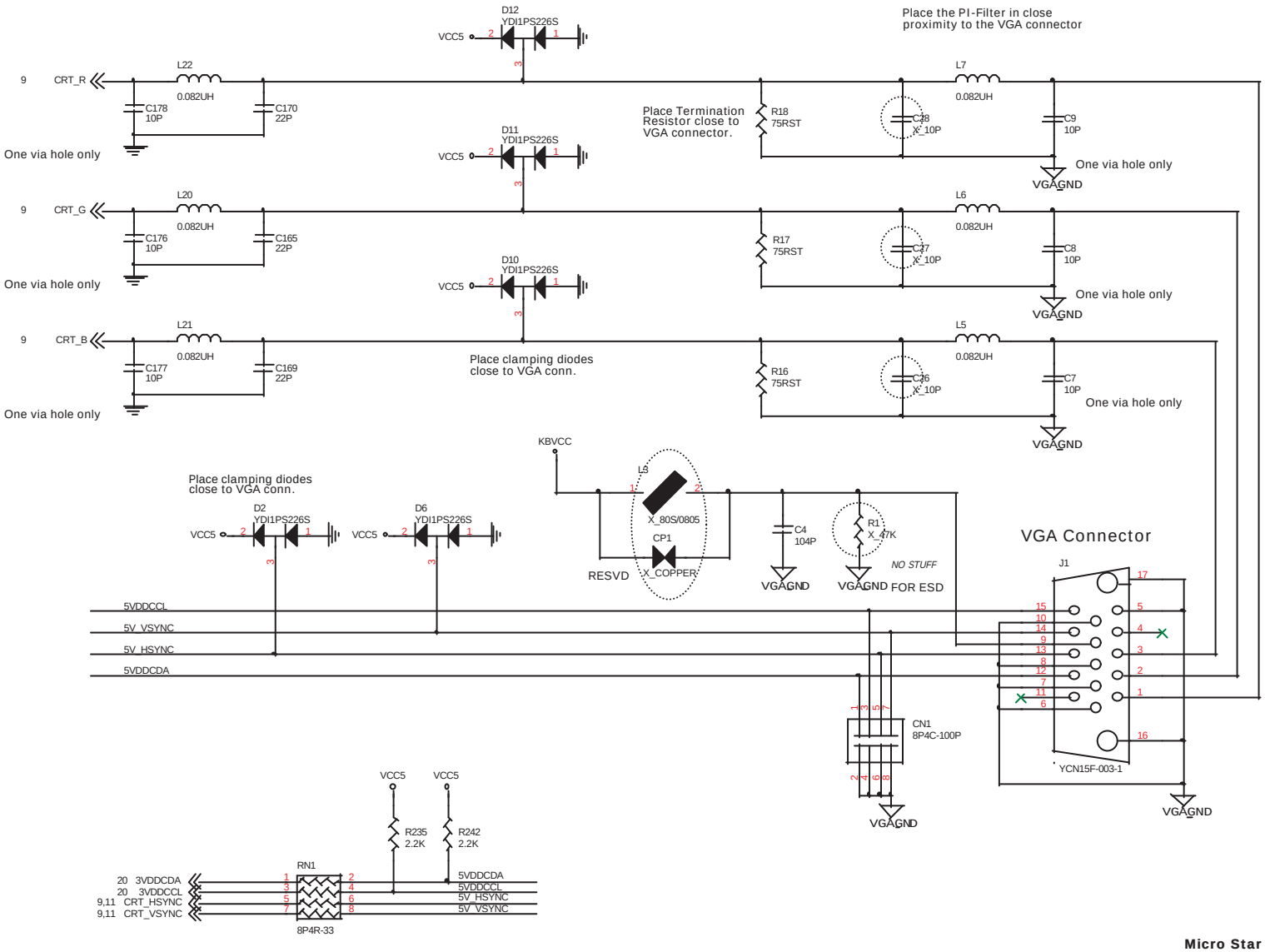
Video Connector



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Title	Video Connector	Rev
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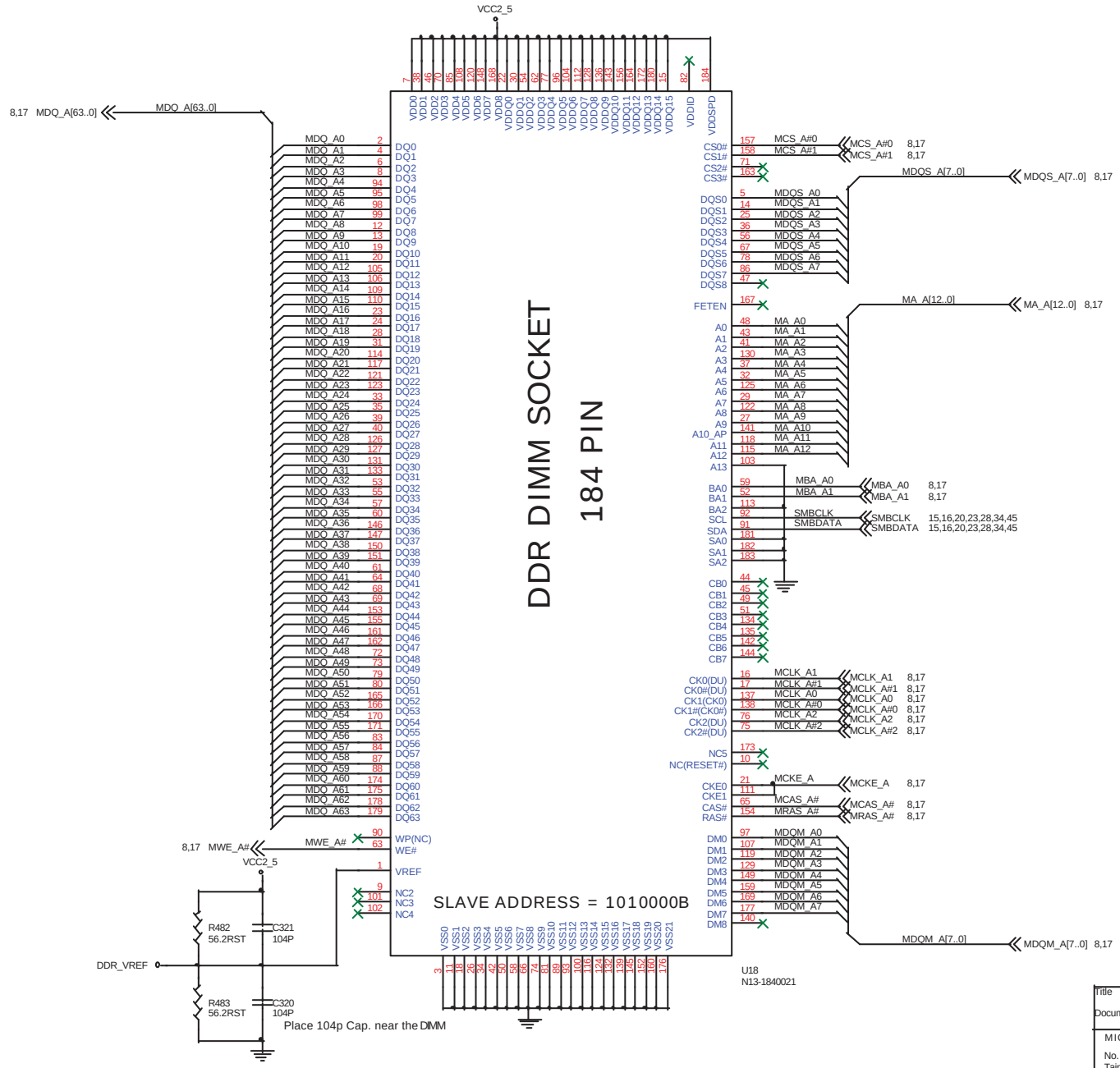
SYSTEM MEMORY



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Title	System Memory : DDR DIMM 1	Rev 00D
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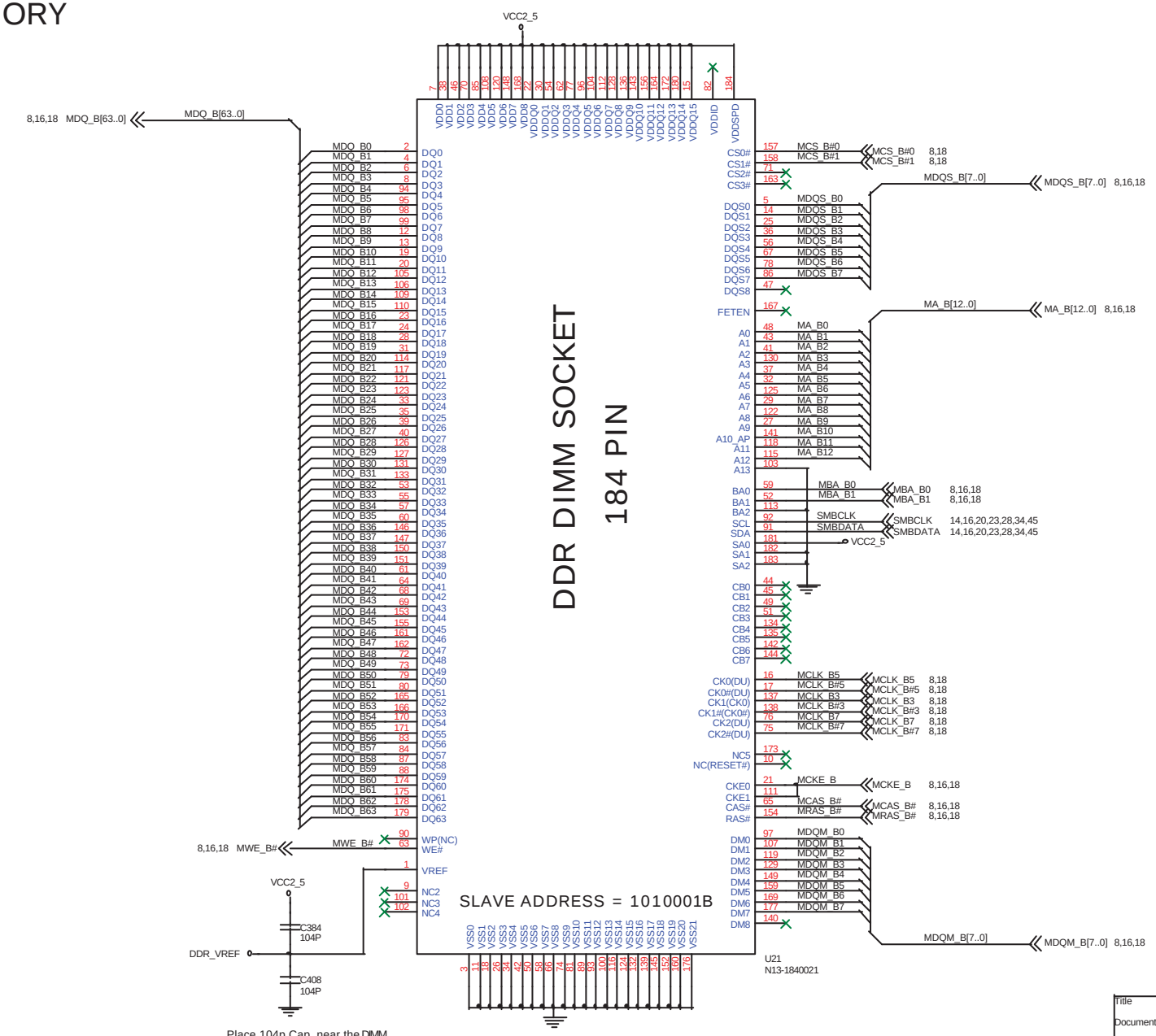
SYSTEM MEMORY



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Title	System Memory : DDR DIMM 3	Rev 00D
Document Number	MS-6367	
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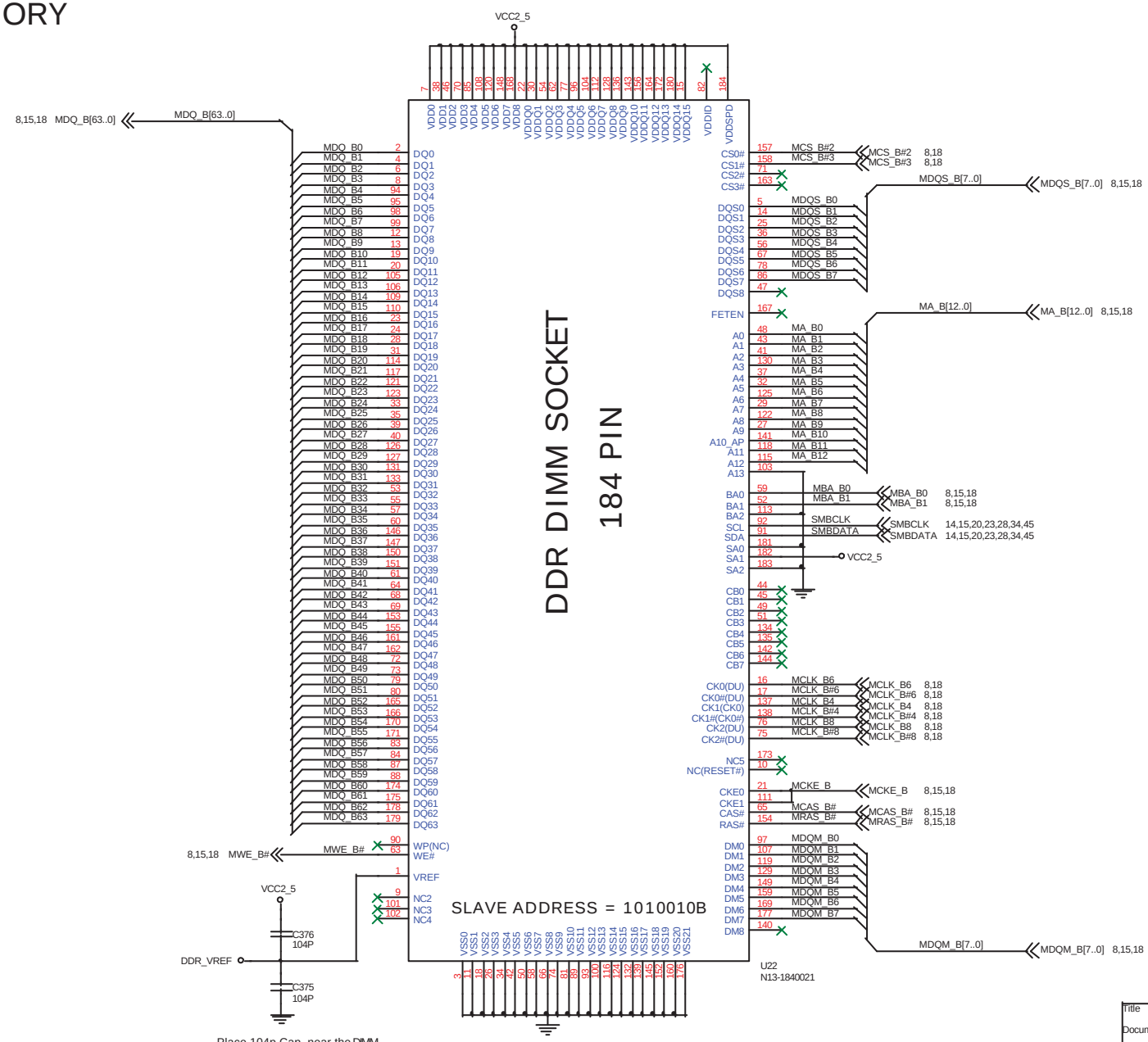
SYSTEM MEMORY



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Title	System Memory : DDR DIMM 2	Rev 00D
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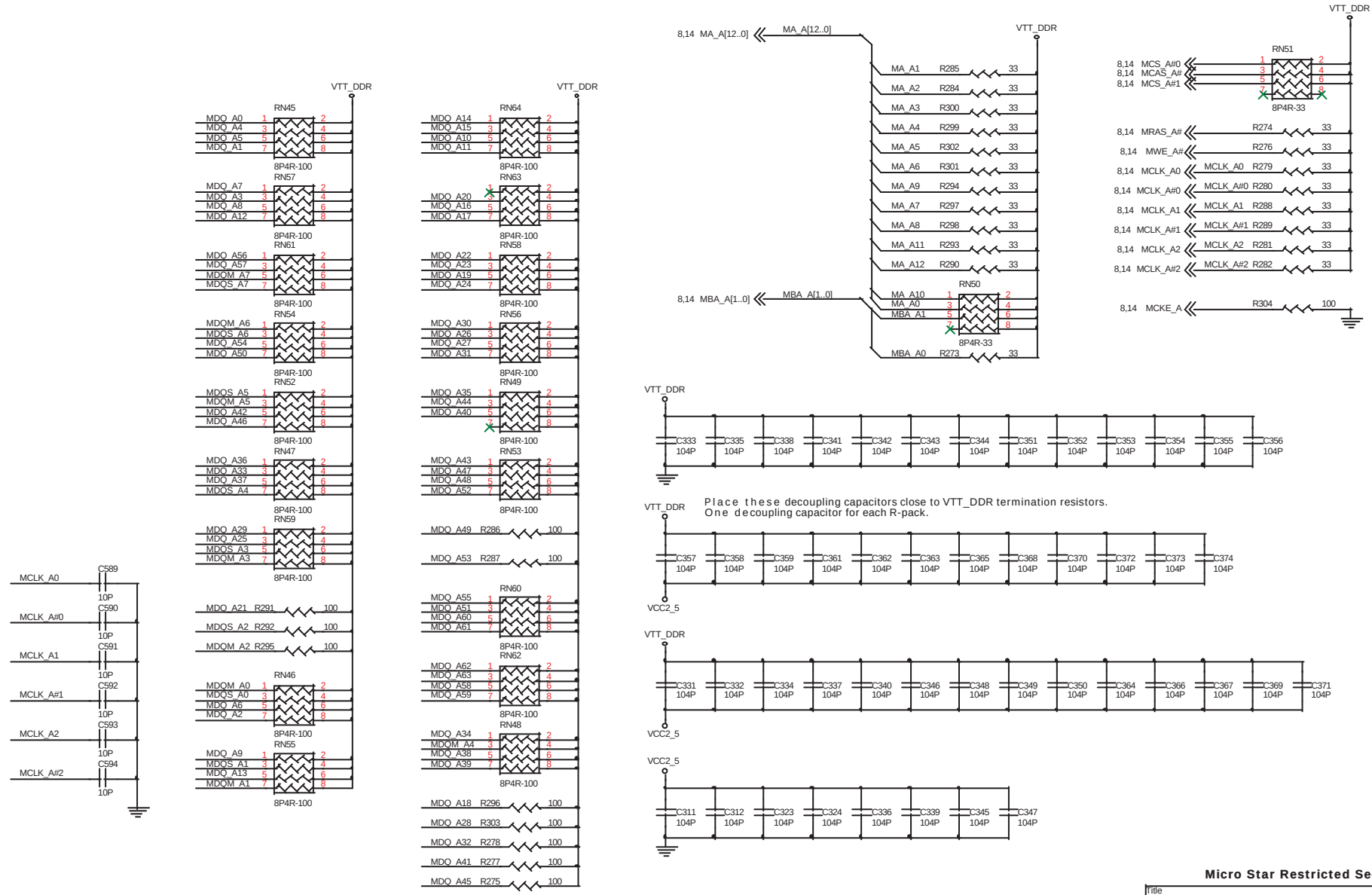
DDR Terminations



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Title	DDR Terminations Bank 0	Rev 00D
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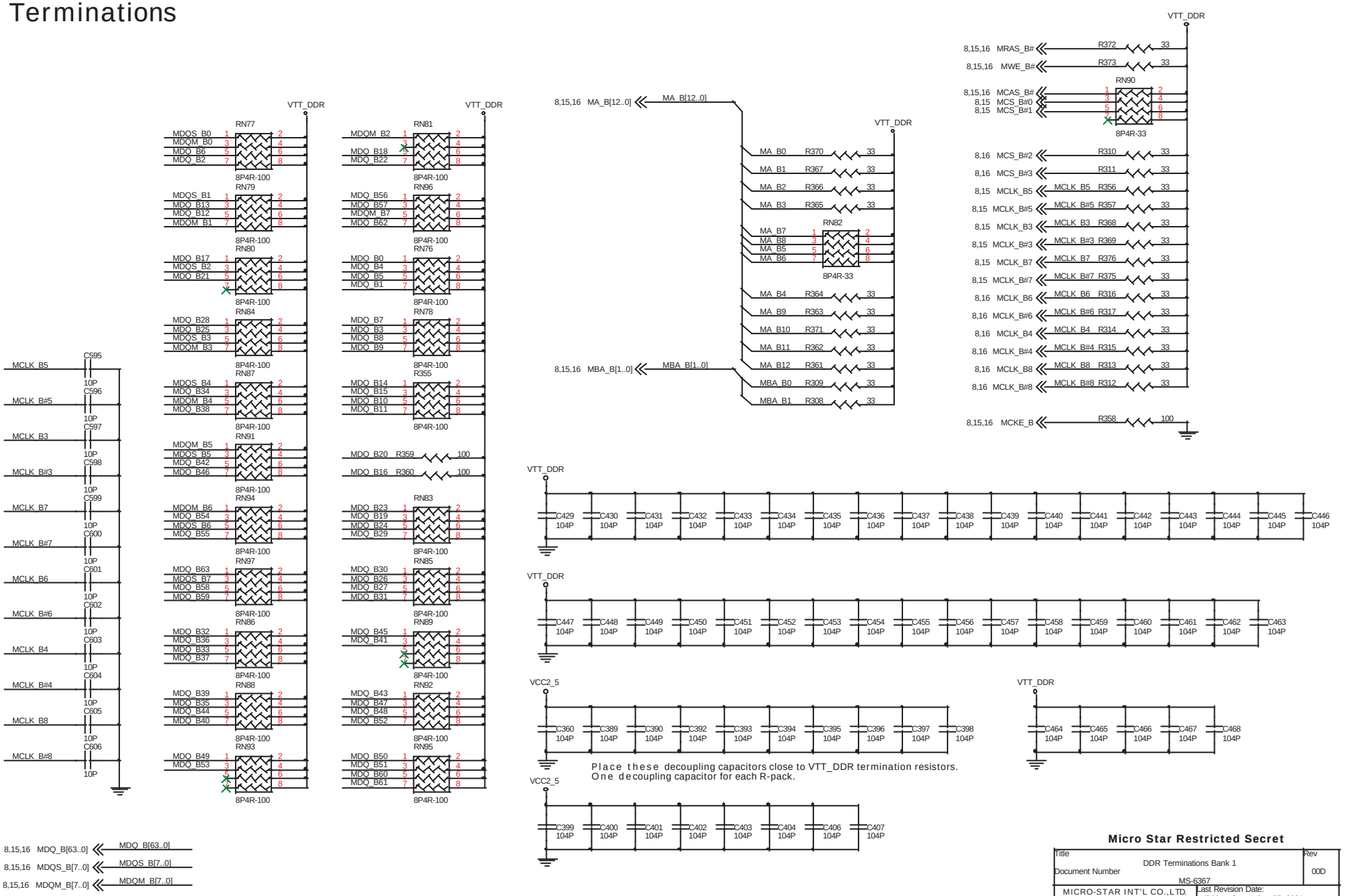
DDR Terminations



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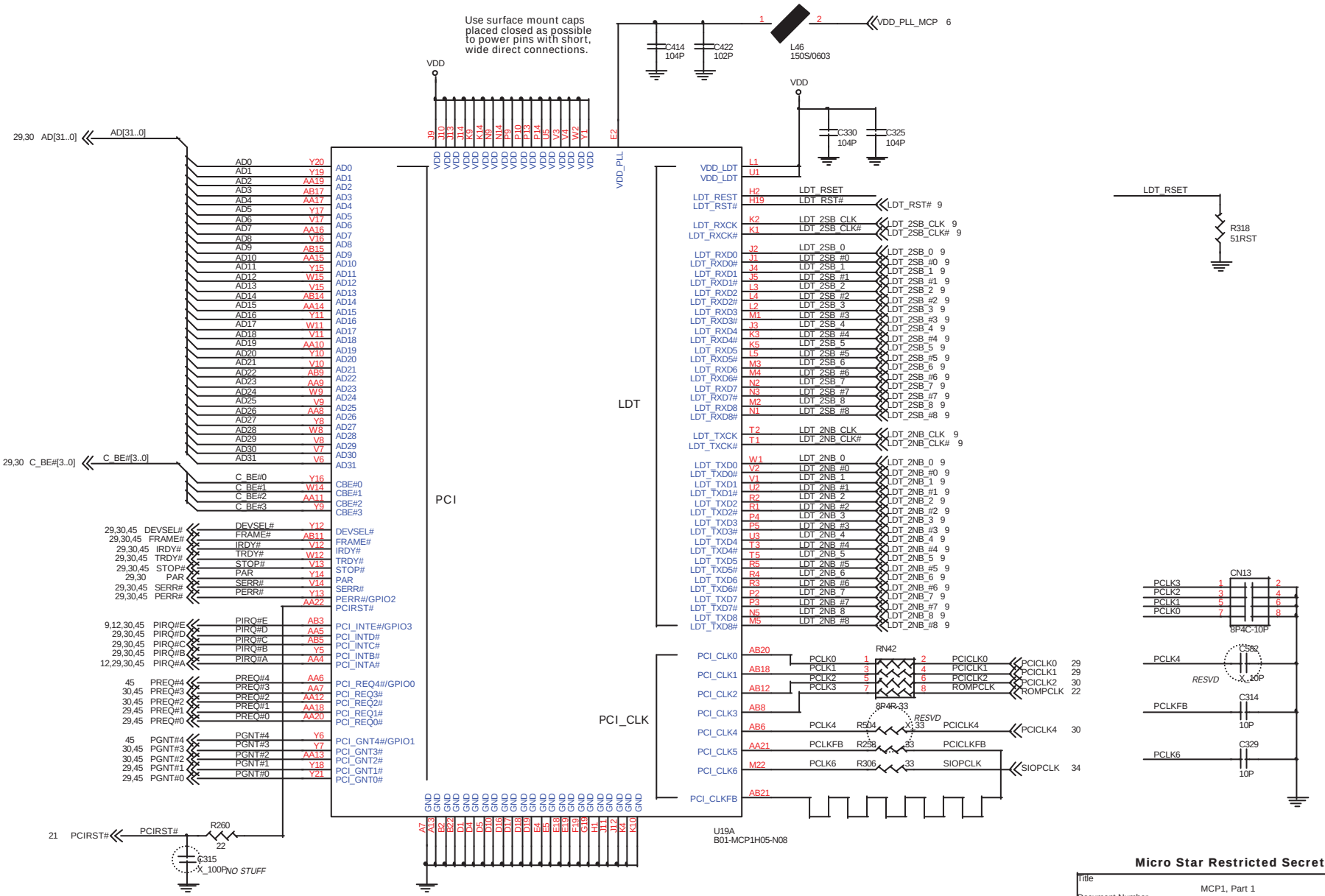
MCP1, Part 1



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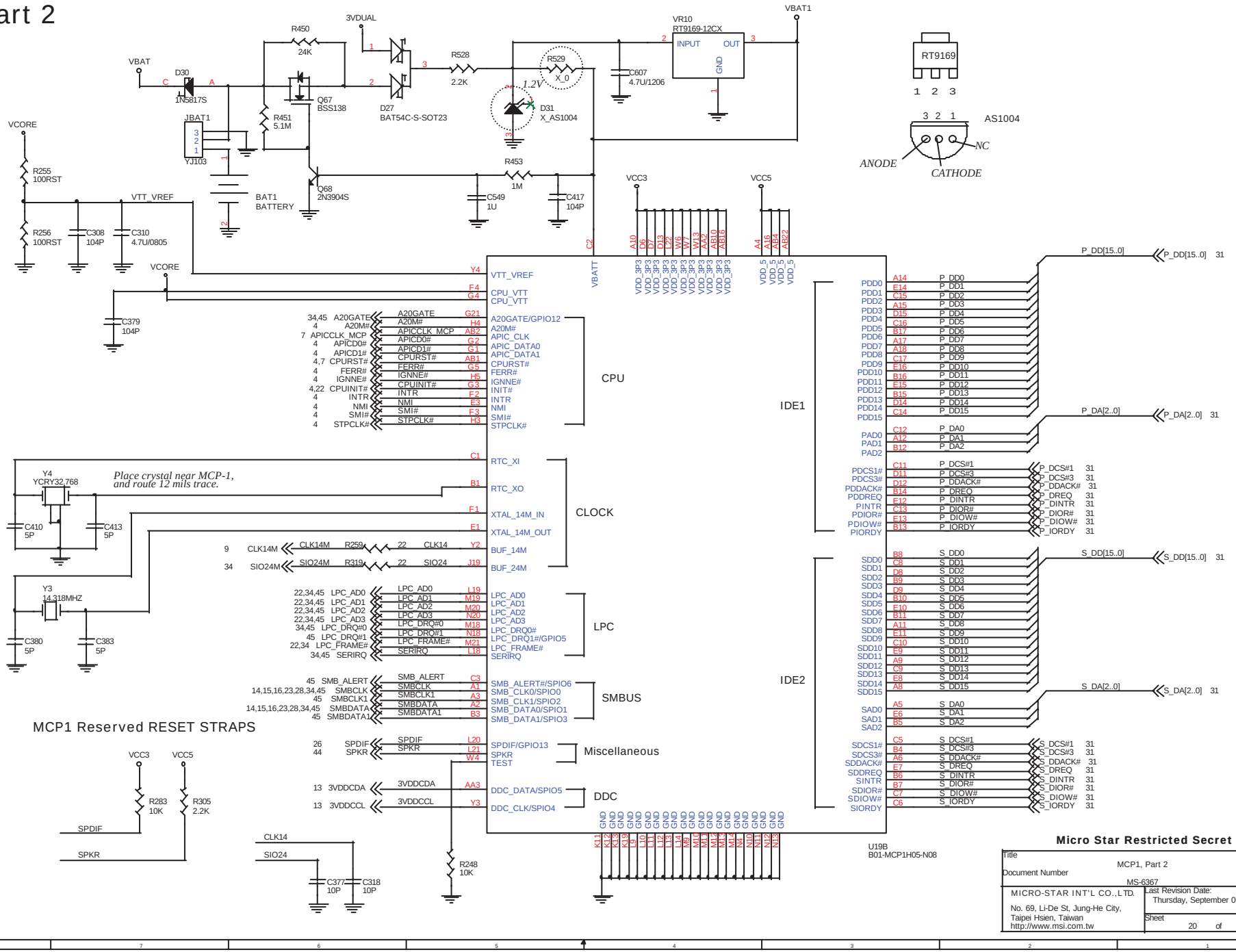
MCP1, Part 2


3VDUAL
VBAT1
VR10
RT9169-12CX
INPUT
OUT
GND
RT9169
1 2 3
AS1004
ANODE
NC
CATHODE
VBAT
D30
1N5817S
R450
24K
Q67
BSS138
D27
BAT54C-S-SOT23
R528
2.2K
R529
X_0
1.2V
D31
X_AS1004
C607
4.7U/1206
JBAT1
YJ103
R451
5.1M
BAT1
BATTERY
Q68
2N3904S
R453
1M
C549
1U
C417
104P
VCORE
R255
100RST
R256
100RST
VTT_VREF
C308
104P
C310
4.7U/0805
C379
104P
VCC3
VCC5
VBATT
VTT_VREF
CPU_VTT
A20GATE/GPIO12
A20M#
APIC_CLK
APIC_DATA0
APIC_DATA1
CPURST#
FERR#
IGNNE#
INIT#
INTR
NMI
SMI#
STPCLK#
CPU
RTC_XI
RTC_XO
XTAL_14M_IN
XTAL_14M_OUT
BUF_14M
BUF_24M
CLOCK
Y4
YCRY32.768
Place crystal near MCP-1,
and route 12 mils trace.
C410
5P
C413
5P
Y3
14.318MHZ
C380
5P
C383
5P
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LPC_DRQ0#
LPC_DRQ1#/GPIO5
LPC_FRAME#
SERIRQ
LPC
SMB_ALERT#/SPIO6
SMB_CLK0/SPIO0
SMB_CLK1/SPIO2
SMB_DATA0/SPIO1
SMB_DATA1/SPIO3
SMBUS
SPDIF/GPIO13
SPKR
TEST
Miscellaneous
DDC_DATA/SPIO5
DDC_CLK/SPIO4
DDC
MCP1 Reserved RESET STRAPS
R283
10K
R305
2.2K
SPDIF
SPKR
R248
10K
C377
10P
C318
10P
CLK14
SIO24
IDE1
IDE2
P_DD[15..0]
P_DA[2..0]
S_DD[15..0]
S_DA[2..0]
U19B
B01-MCP1H05-N08
Micro Star Restricted Secret
Title
MCP1, Part 2
Rev
00D
Document Number
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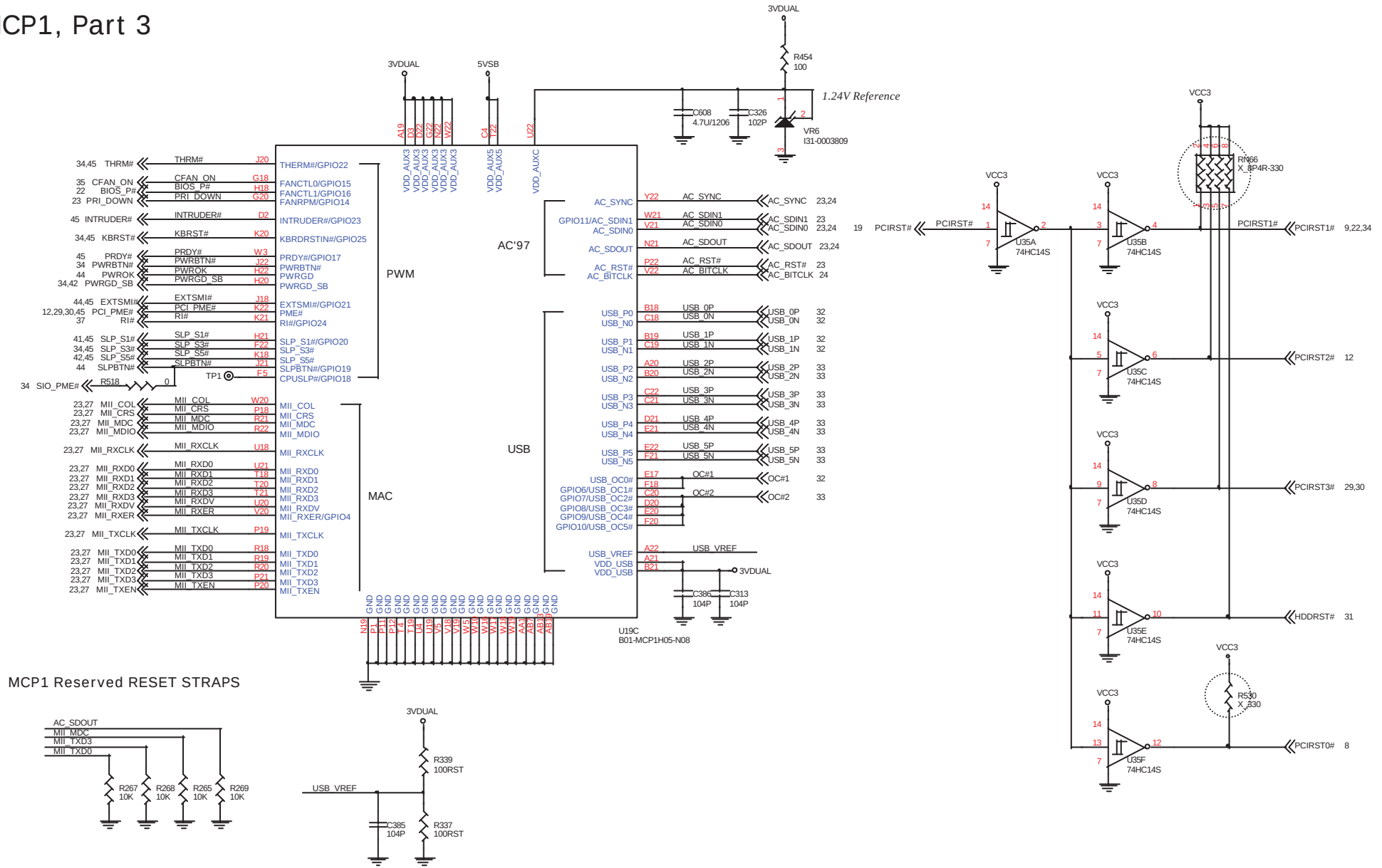
MCP1, Part 3



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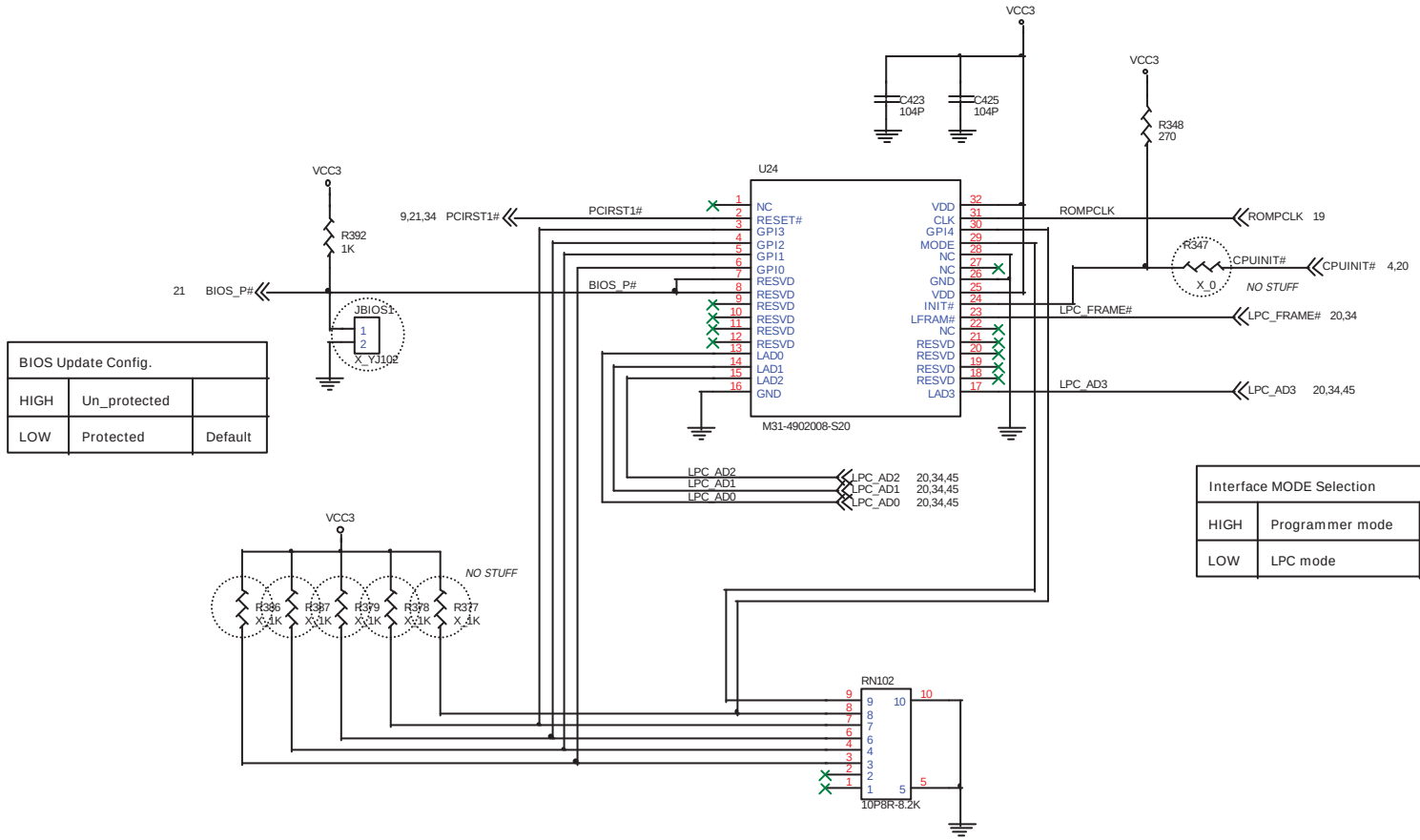
Flash ROM



BIOS Update Config.		
HIGH	Un_protected	
LOW	Protected	Default

Interface MODE Selection		
HIGH	Programmer mode	
LOW	LPC mode	Default

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Title: Flash ROM		Rev: 00D
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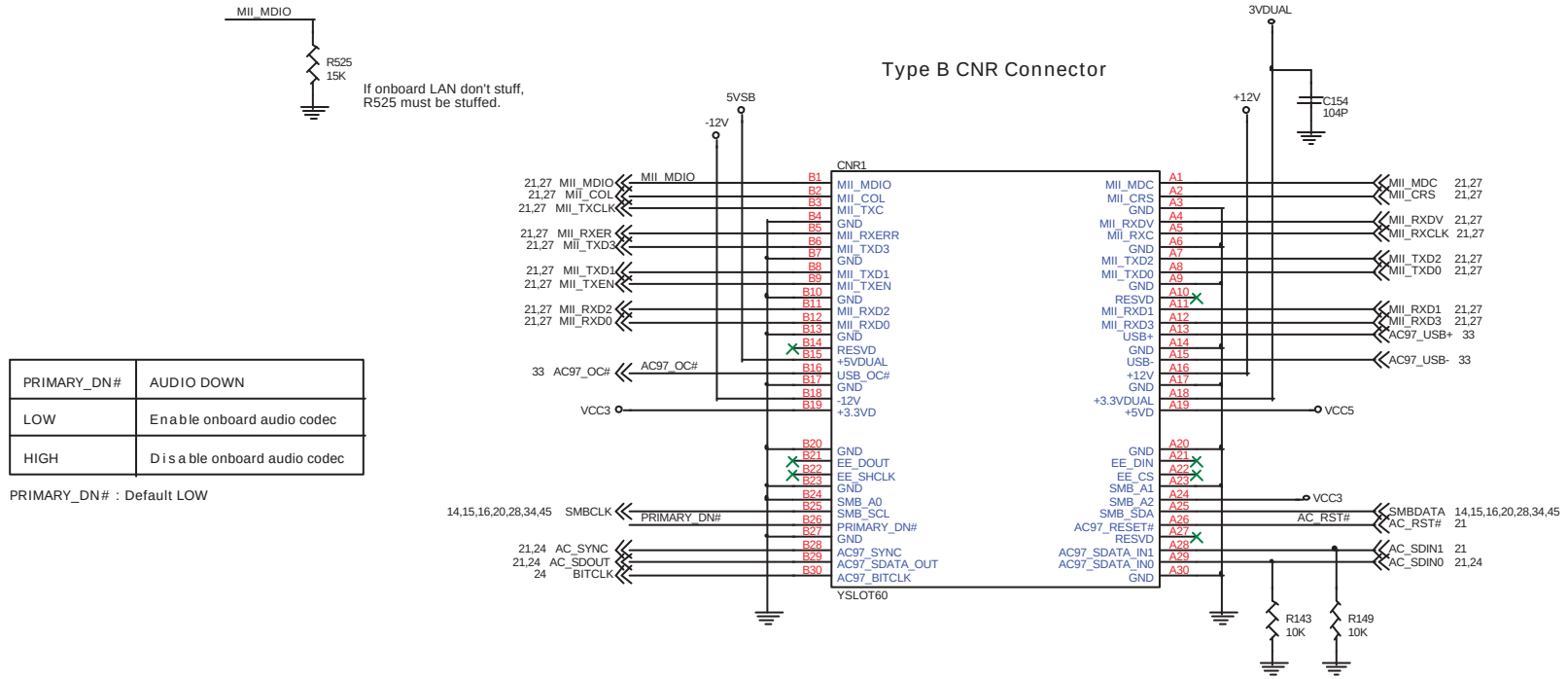
Comm. Networking Riser



PRIMARY_DN#	AUDIO DOWN
LOW	Enable onboard audio codec
HIGH	Disable onboard audio codec

PRIMARY_DN# : Default LOW

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Title	Communication Networking Riser	Rev 00D
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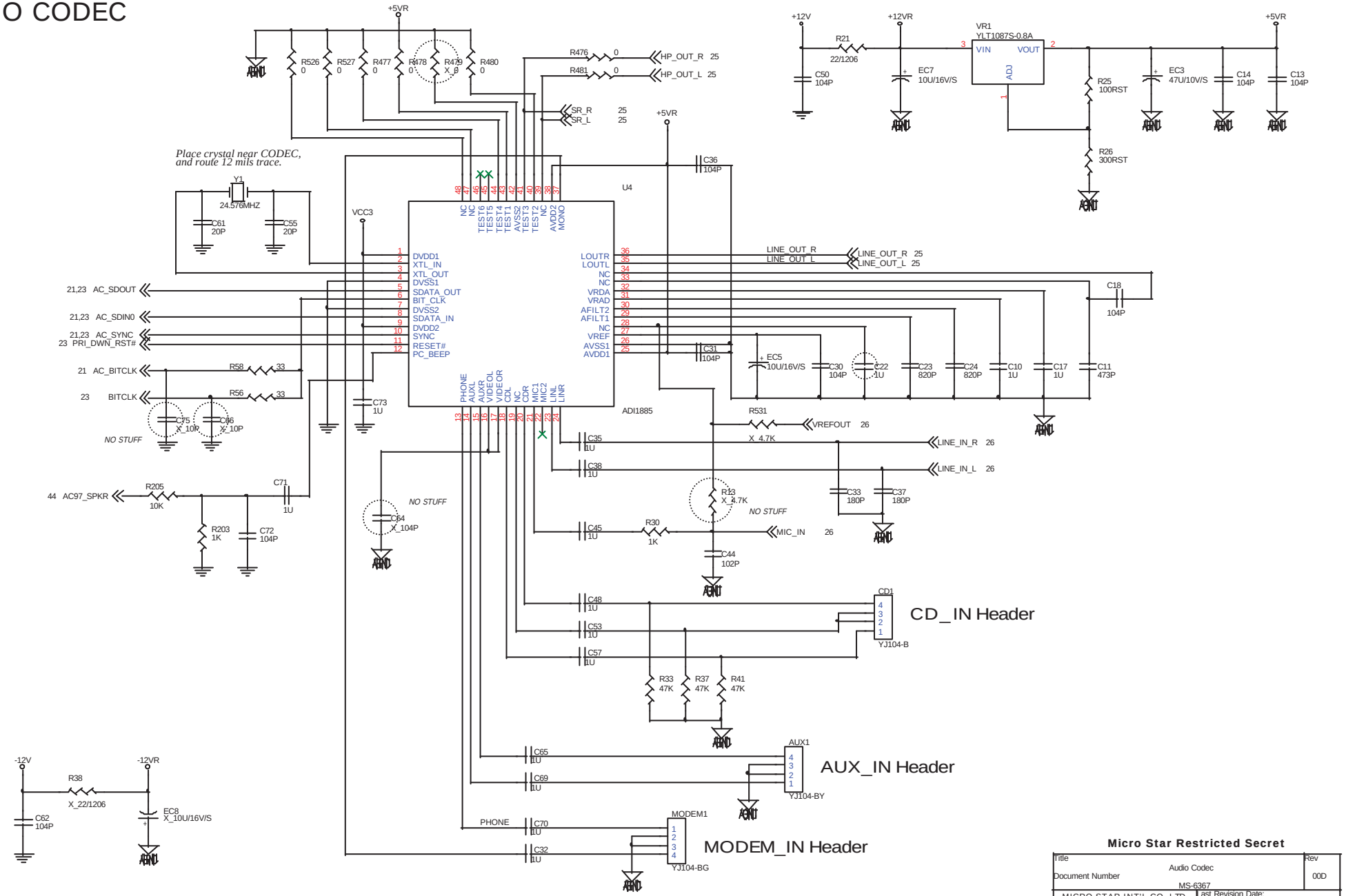
AUDIO CODEC



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Title	Audio Codec	Rev 00D
Document Number	MS-6367	
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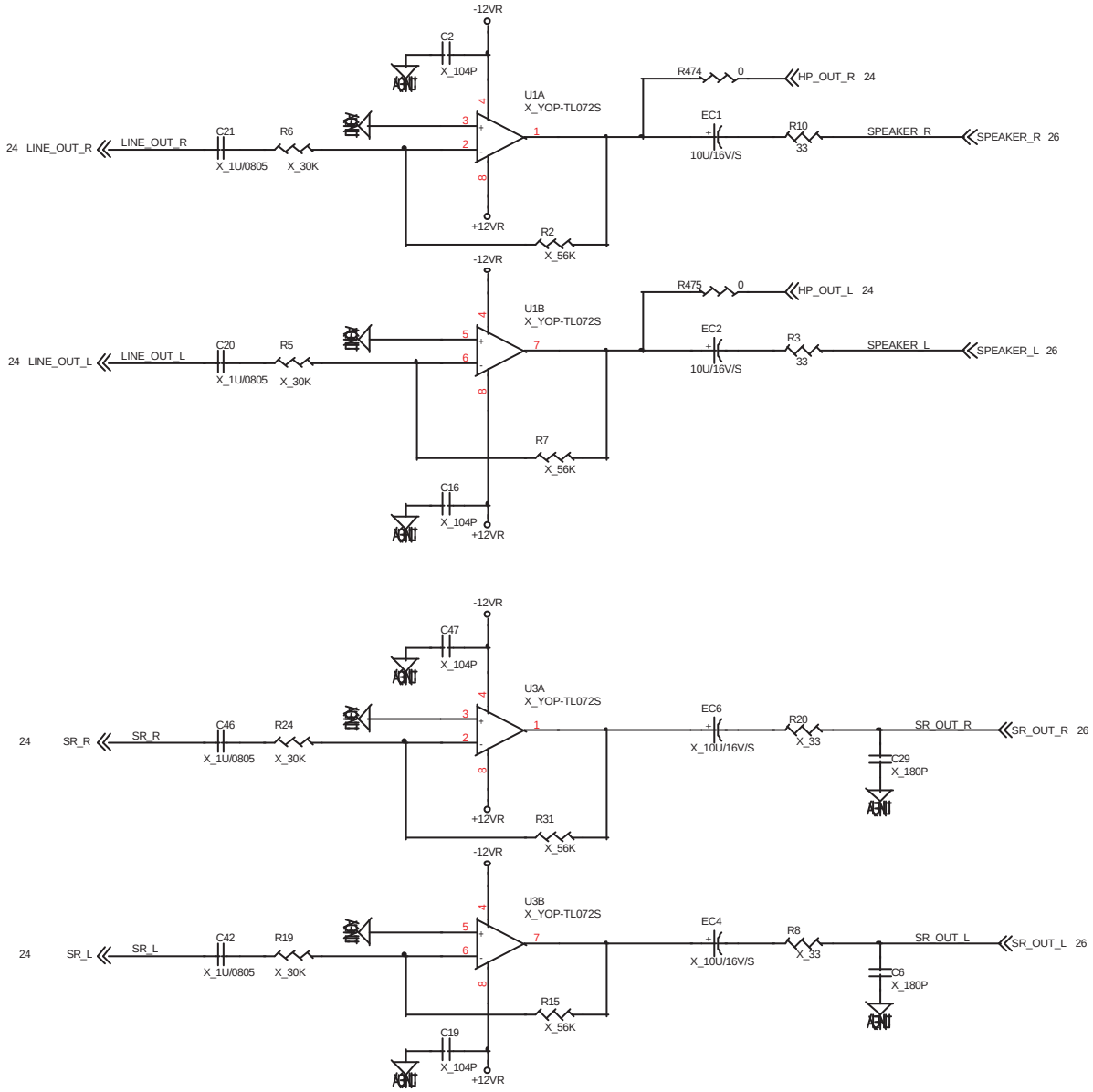
Audio Amplifier



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Title	Audio Amplifier	Rev
Document Number	MS-6367	00D
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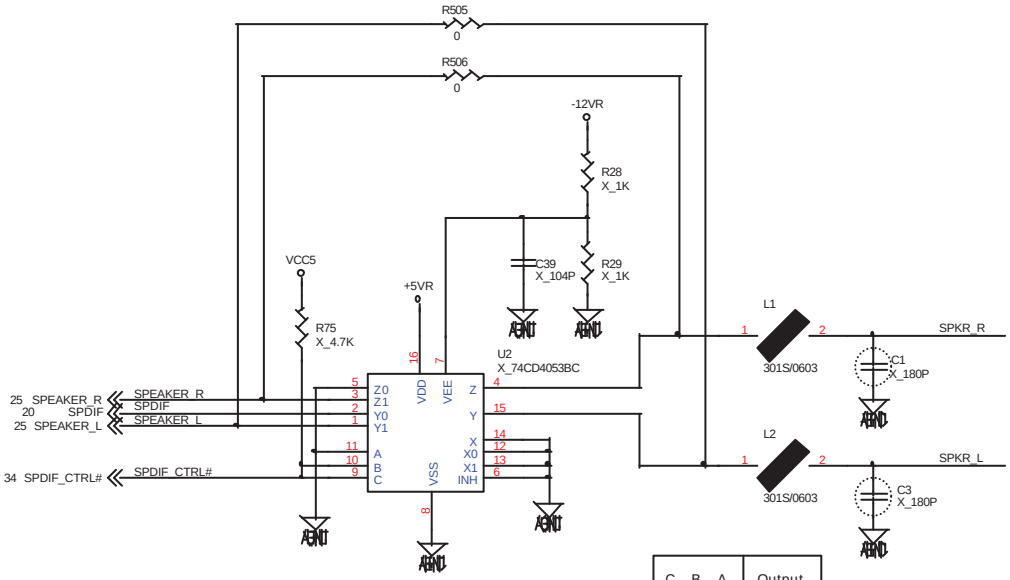
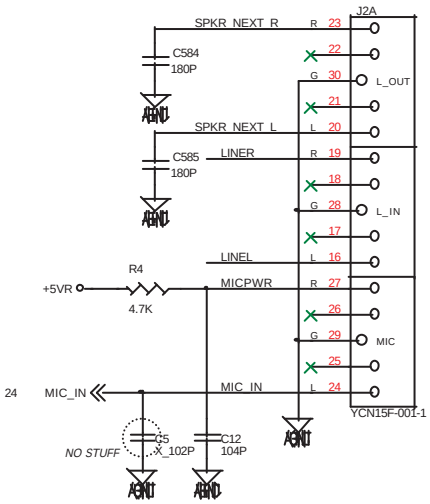
Audio Connector

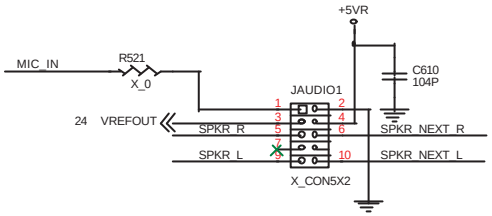


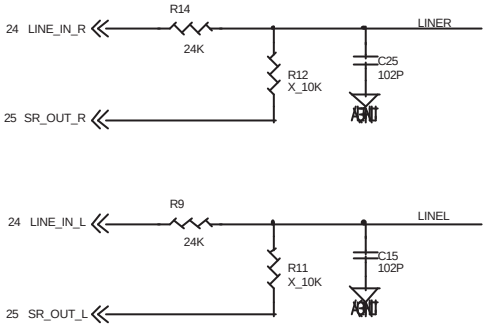
C	B	A	Output
1	1	0	Y1,Z1
0	0	0	Y0,Z0

Audio Connector

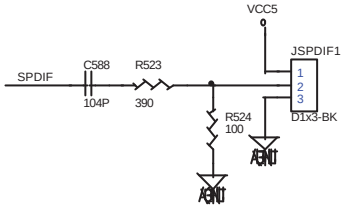


Intel Front Audio Header





SPDIF Header



Place this header near CNR and CODEC.

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Title	Audio Connector	Rev 00D
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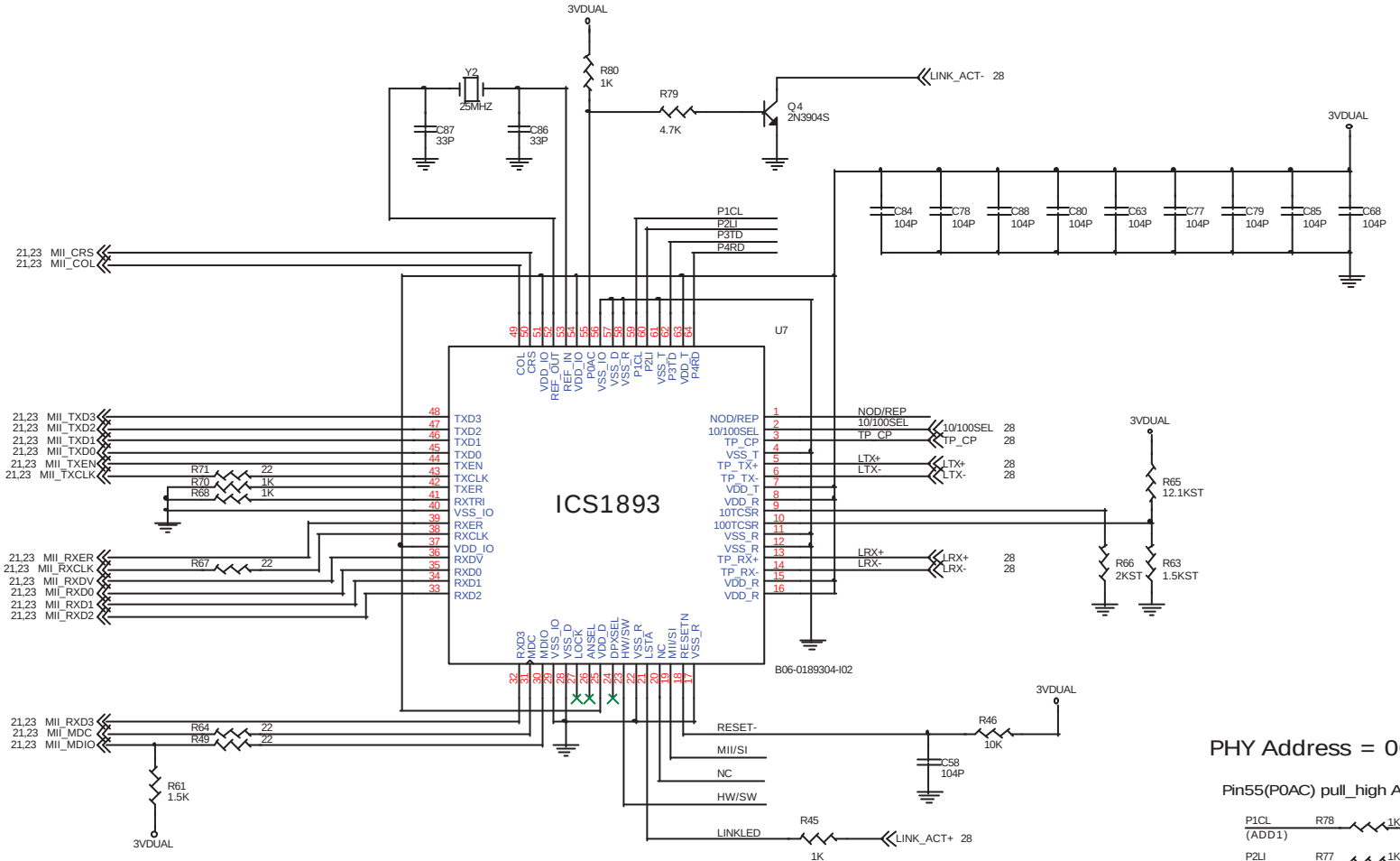
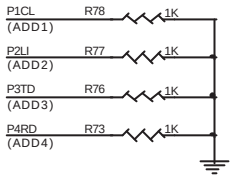
LAN



PHY Address = 00001

Pin55(P0AC) pull_high ADD0 = 1



1.HW/SW=1
Set as SW mode

2.MII/SI=0
MII Enable

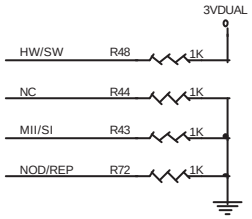
3.NOD/REP=0
NODE Operation

In SW mode:

Pin2 (10/100SEL) is output now
is 10MHz or 100MHz
Low(0) is 10 Base-T, High(1) is 100Base-T

Pin24 (DPXSEL) is output now
is Half or Full
Low(0) is Half-Duplex, High(1) is Full Duplex

Pin26 (ANSEL) is output, show Auto-Negotiation
is Enable or Disable
Low(0) is Disable, High(1) is Enable



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Title	LAN	Rev 00D
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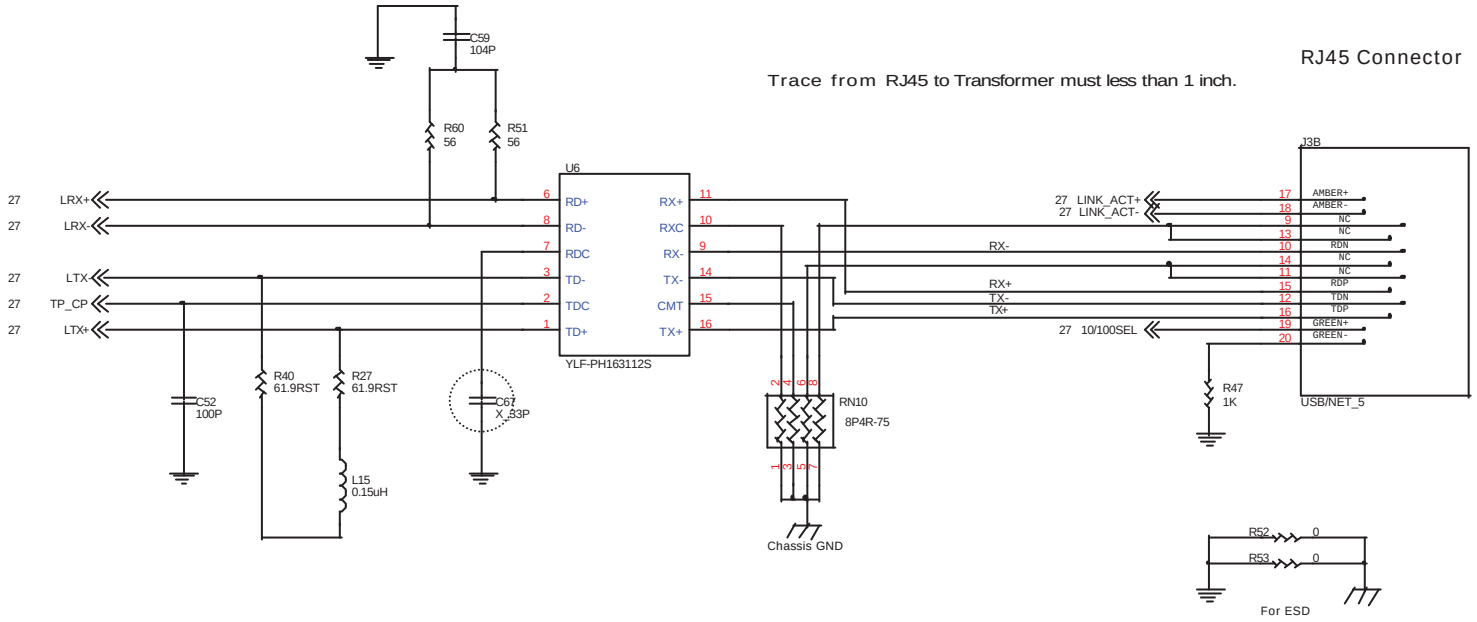
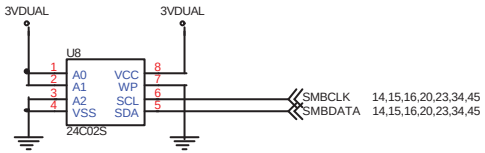
LAN Connector



EEPROM



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Title	LAN Connector	Rev
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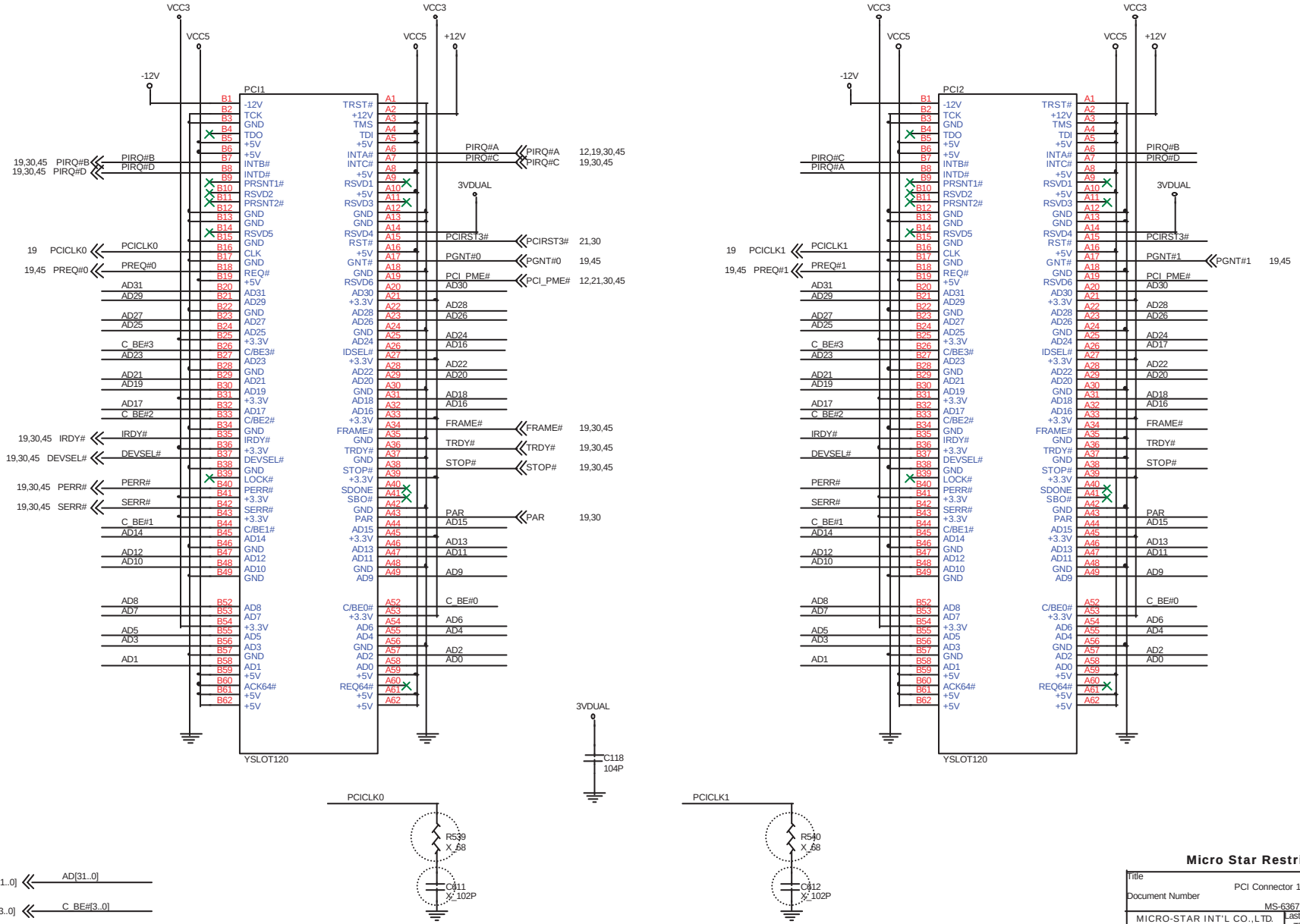
PCI Connectors



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Title	PCI Connector 1 & 2	Rev 00D
Document Number	MS-6367	
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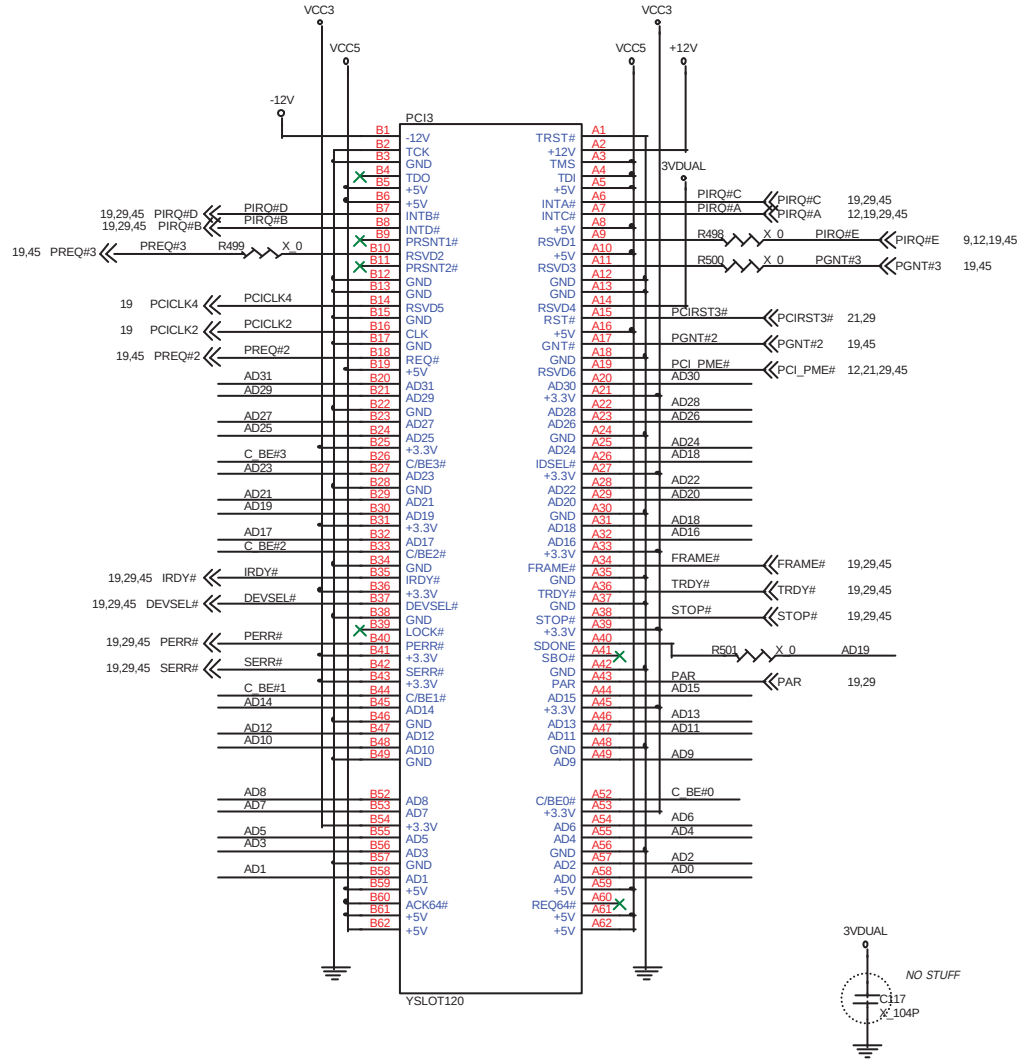
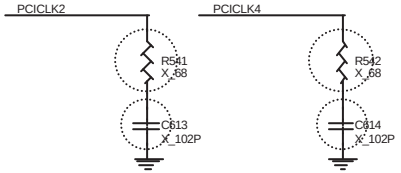
PCI Connectors





19,29 AD[31..0] — AD[31..0]

19,29 C_BE#[3..0] — C_BE#[3..0]

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Title	PCI Connector 3	Rev 00D
Document Number	MS-6367	
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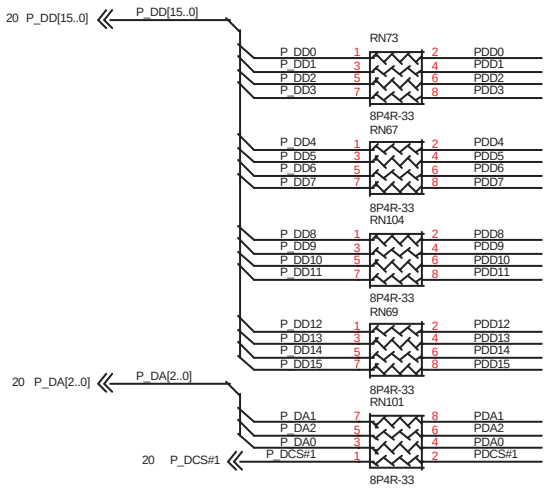
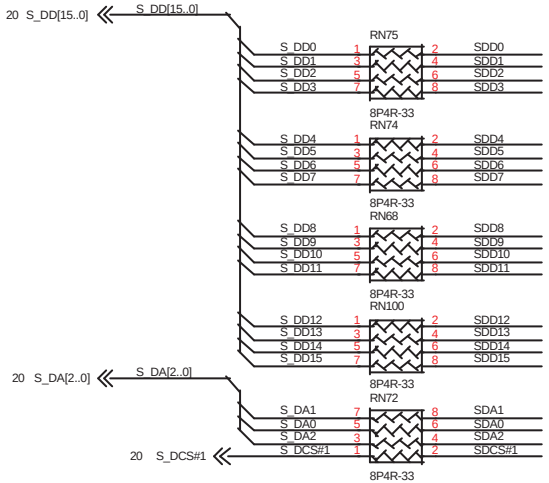
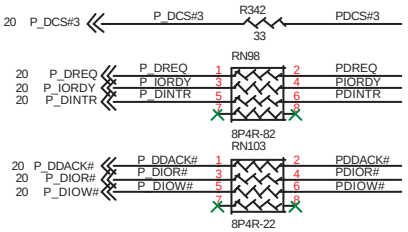
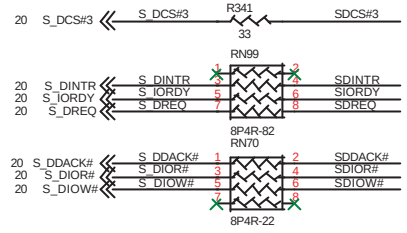
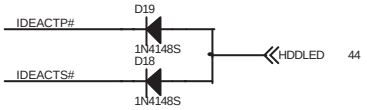
ATA100 IDE CONNECTORS



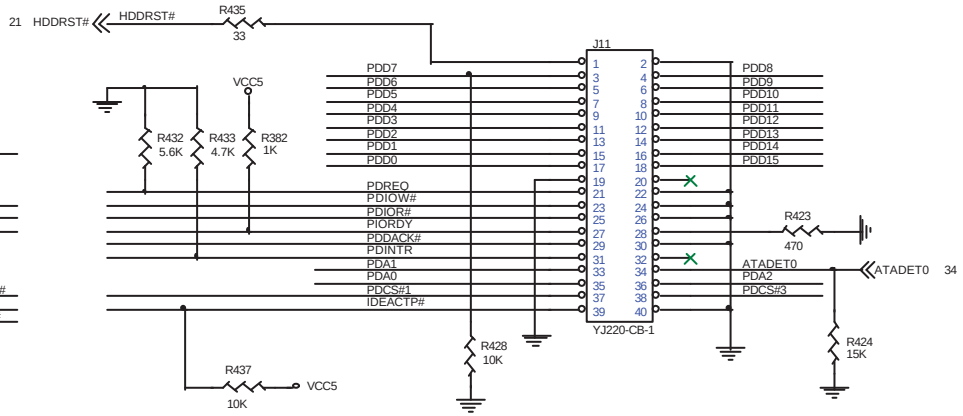




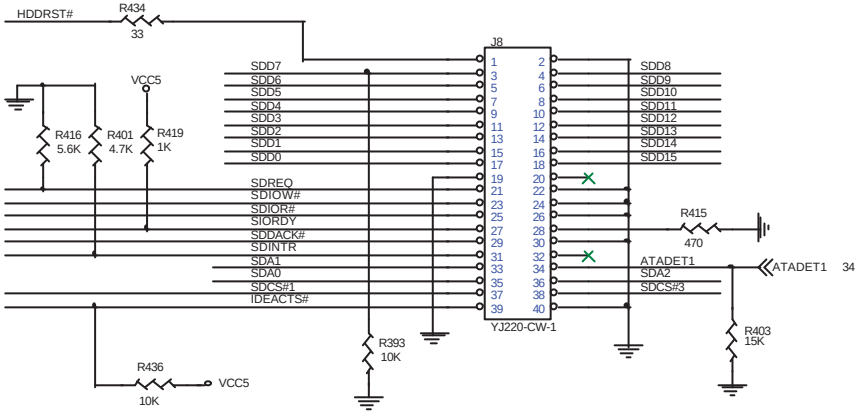




PRIMARY IDE CONN.



SECONDARY IDE CONN.



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Title	ATA 100 IDE Connectors	Rev
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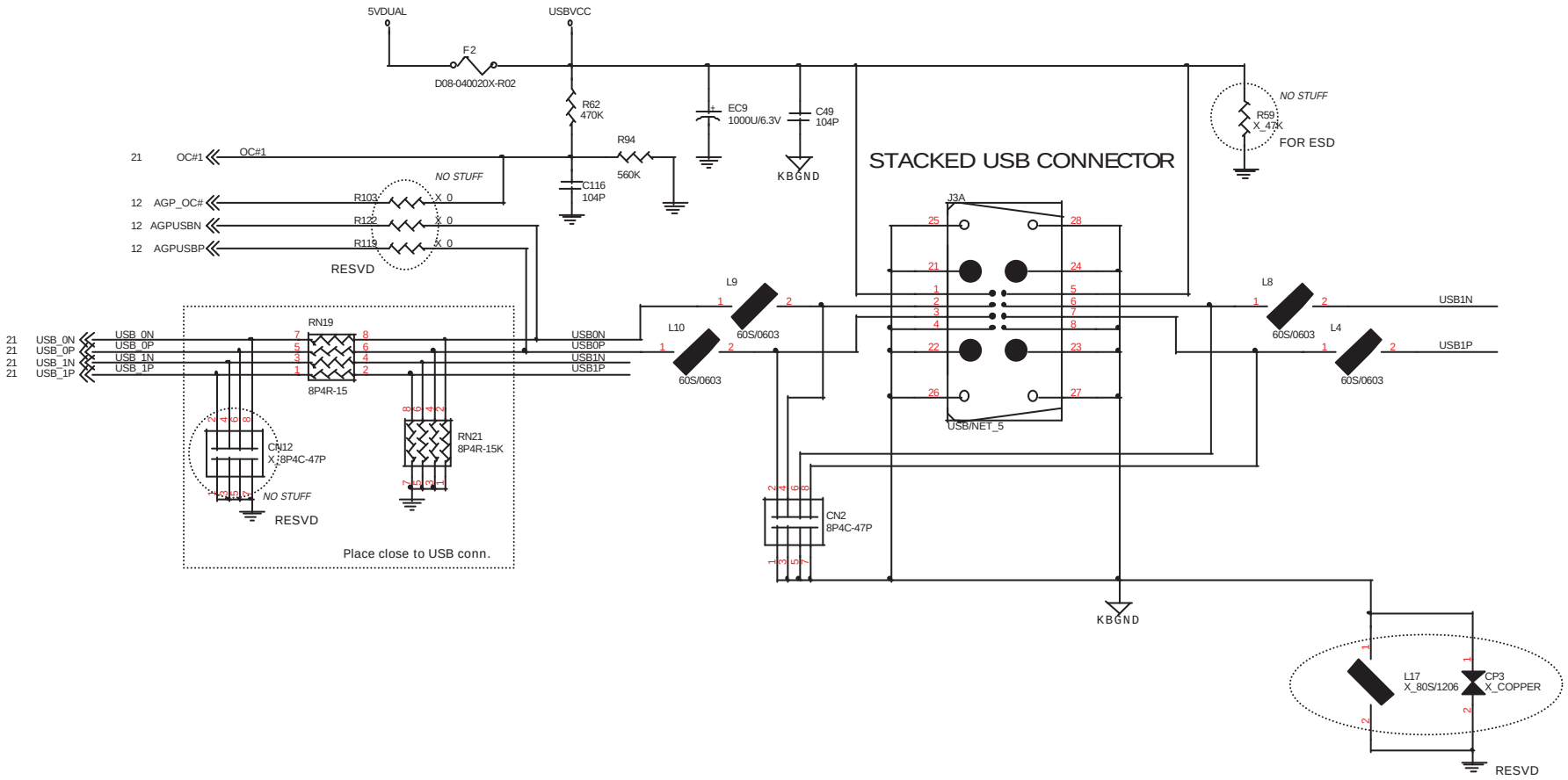
USB Rear Connectors



Micro Star Restricted Secret

Title	USB Rear Connectors	Rev 00D
Document Number	MS-6367	
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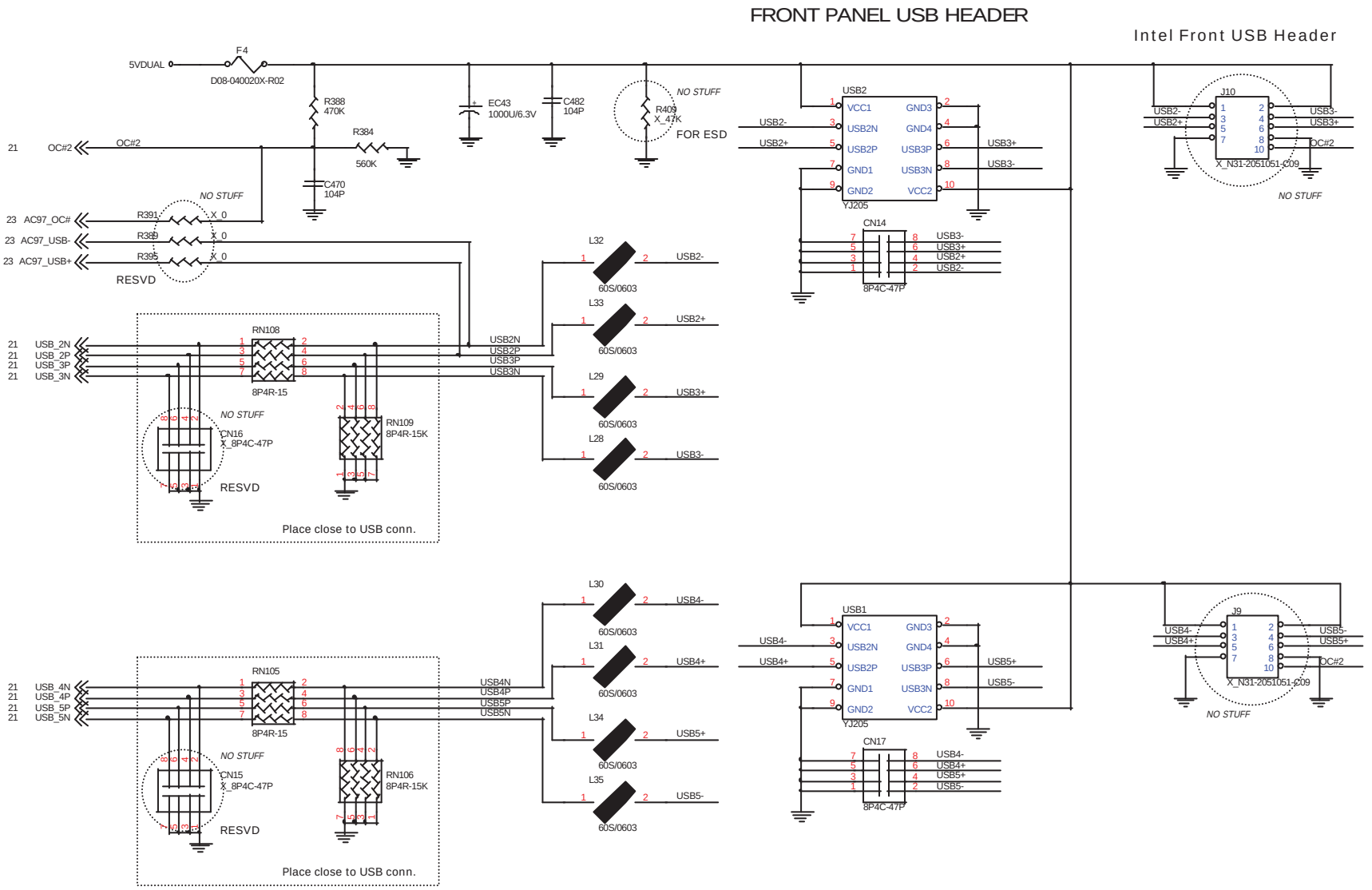
USB Front Connectors



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Title	USB Connectors	Rev 00D
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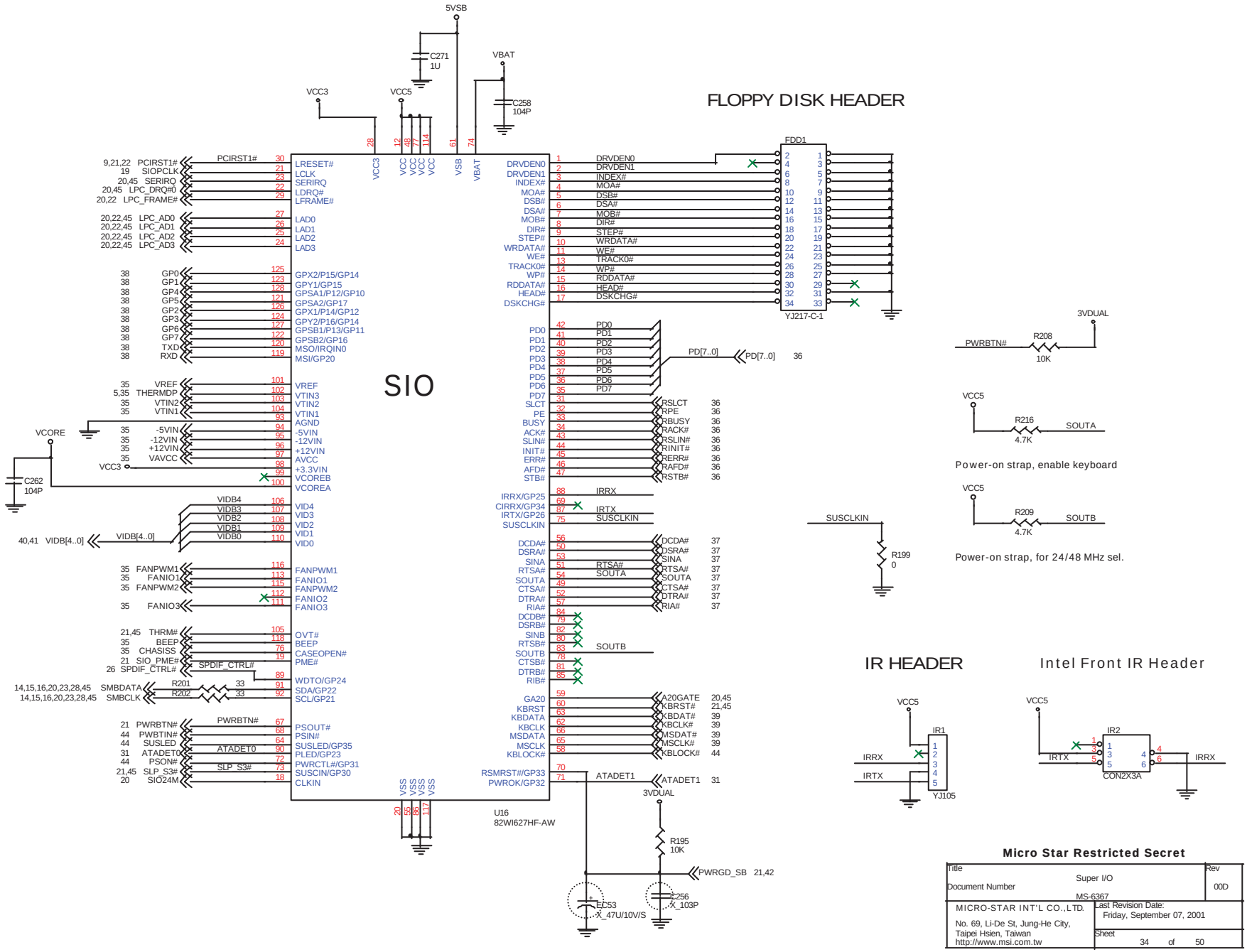
Super I/O



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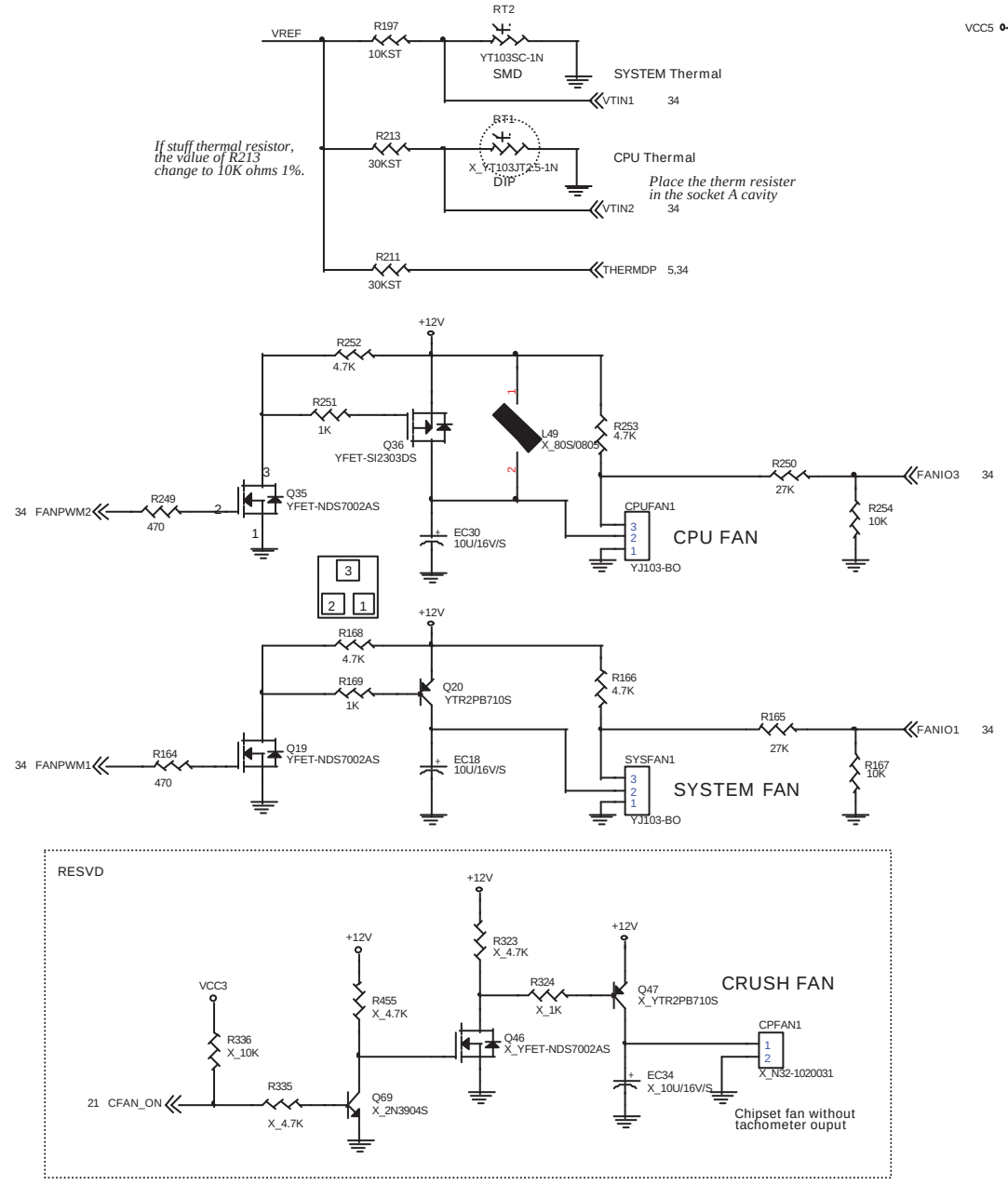
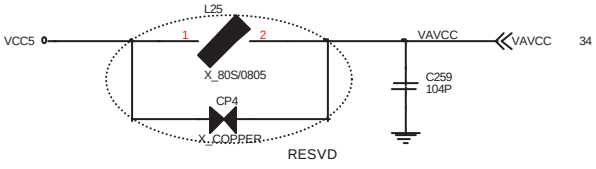
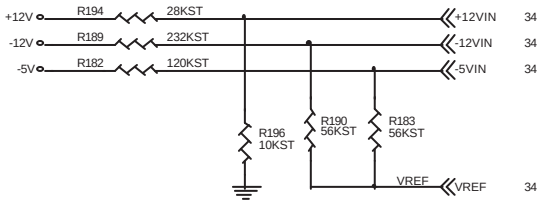
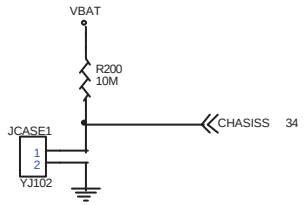
Hardware Monitor

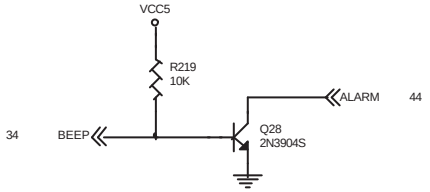






Chasiss Intrusion Header





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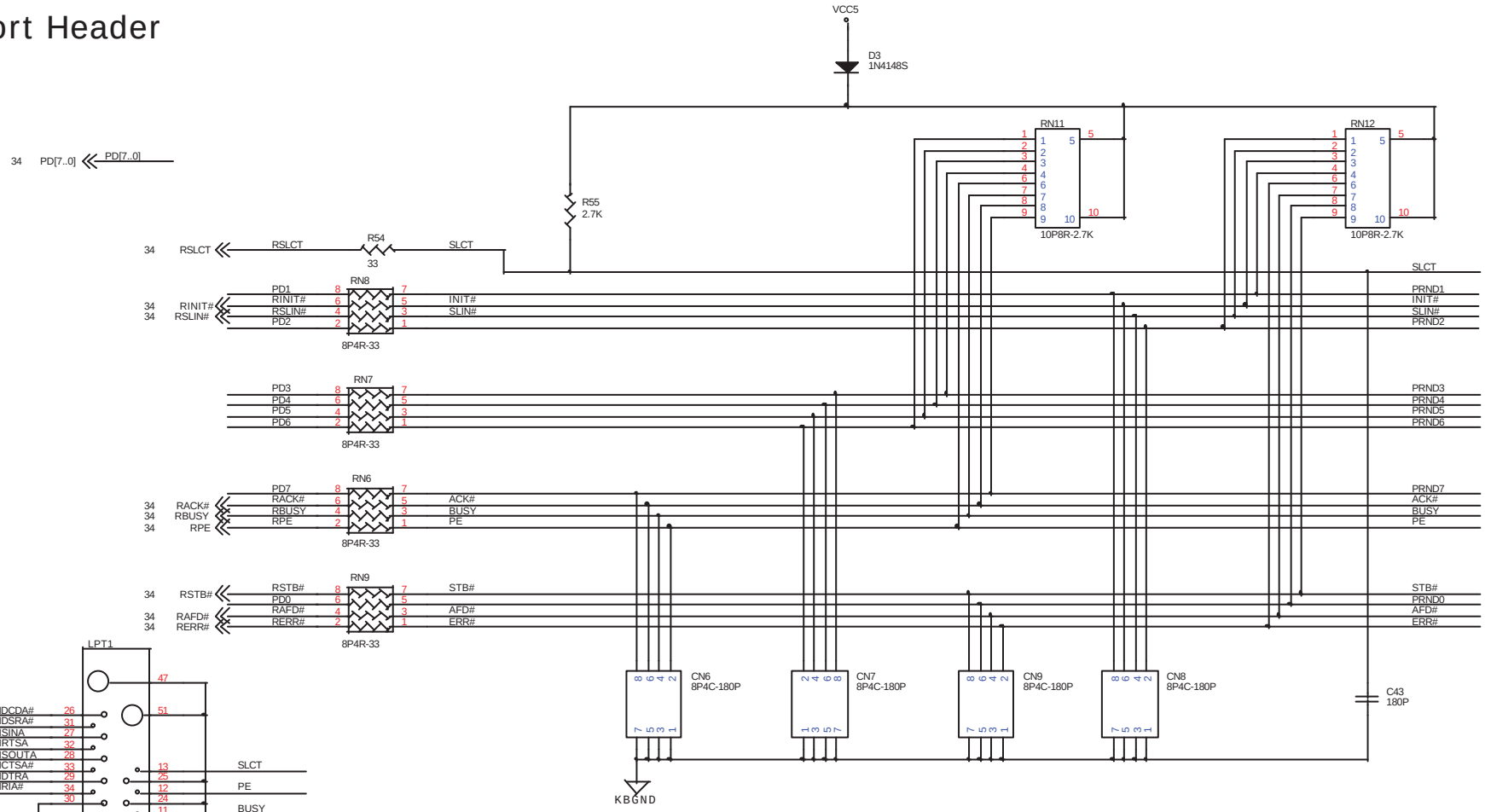
Parallel Port Header



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Title	Parallel Port Header	Rev 00D
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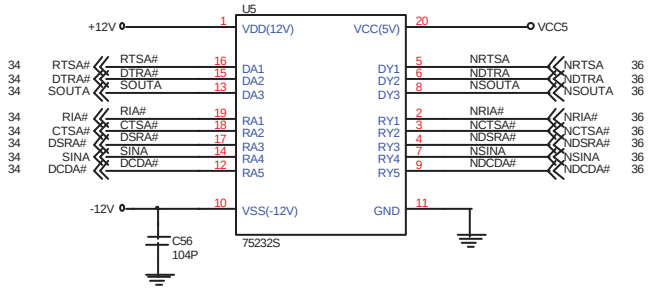
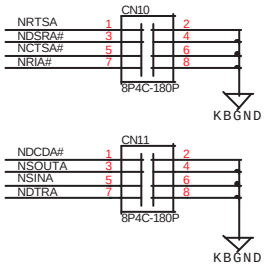
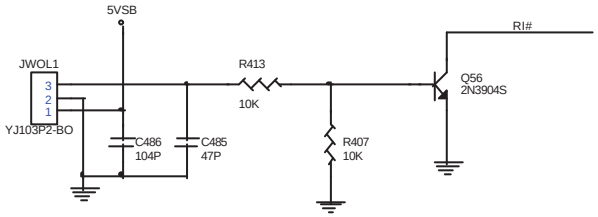
Serial Port/COM Headers

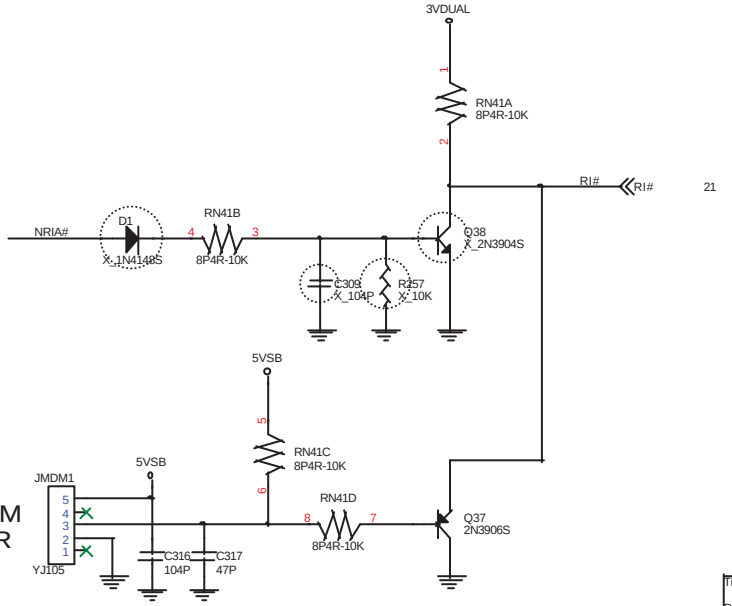




LAN WAKEUP HEADER



INTERNAL MODEM WAKEUP HEADER



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Title	Serial Port Header	Rev
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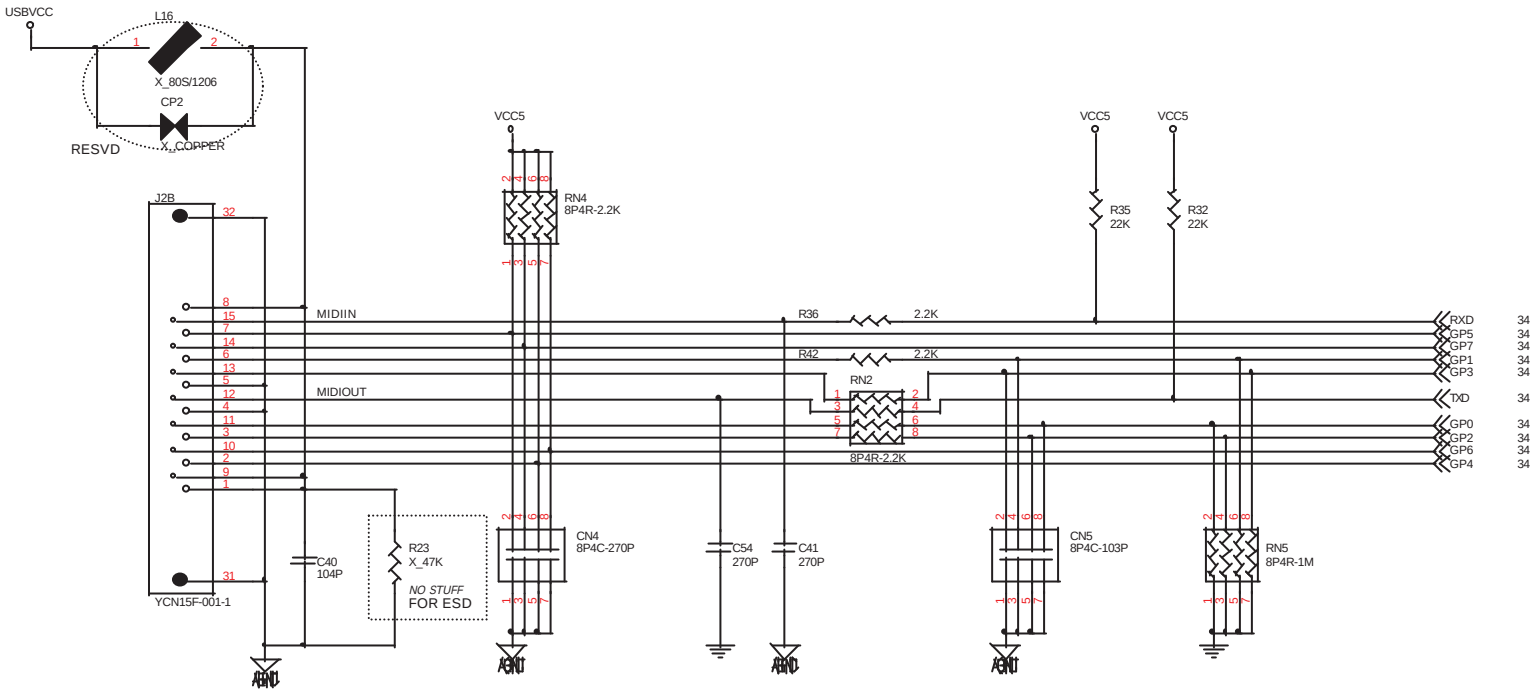
Game Port



GAME PORT HEADER

Micro Star Restricted Secret

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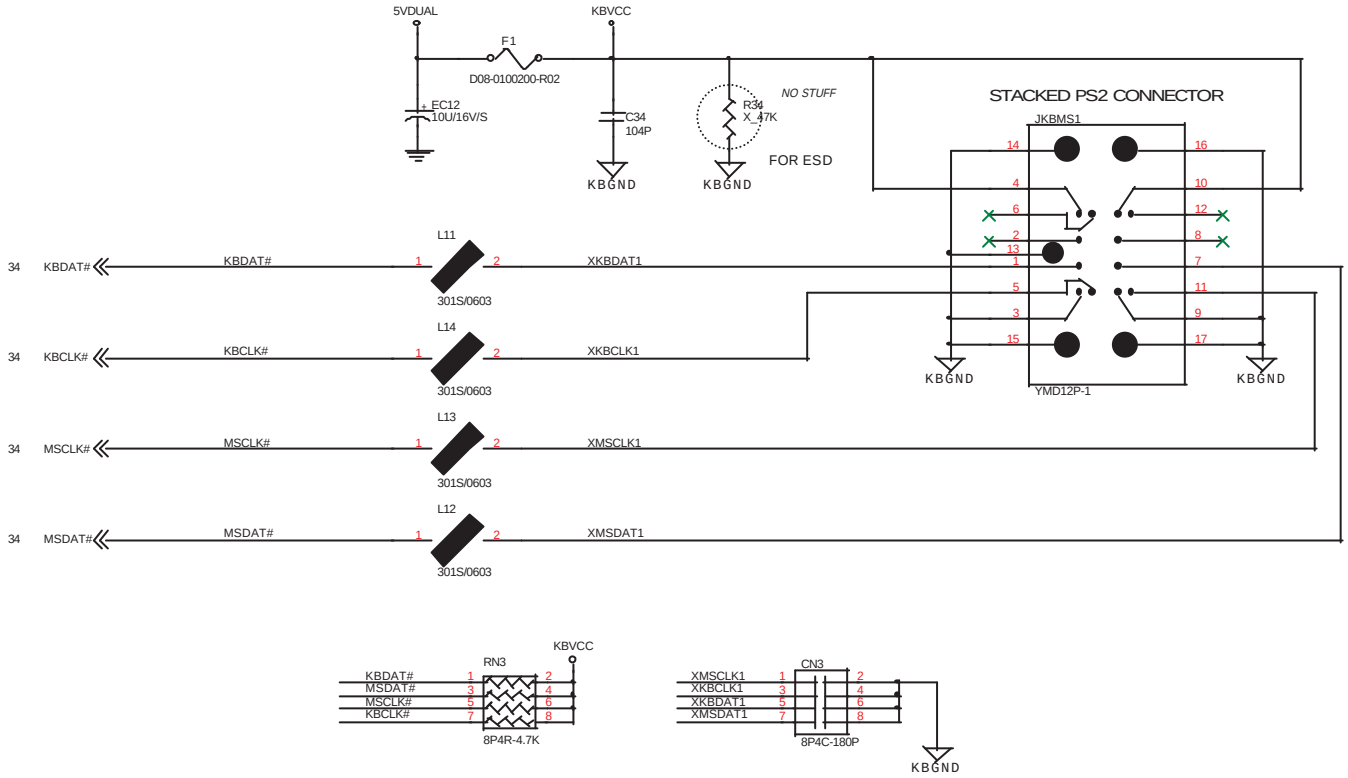
Keyboard/Mouse Ports



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Title	Keyboard/Mouse Ports	Rev
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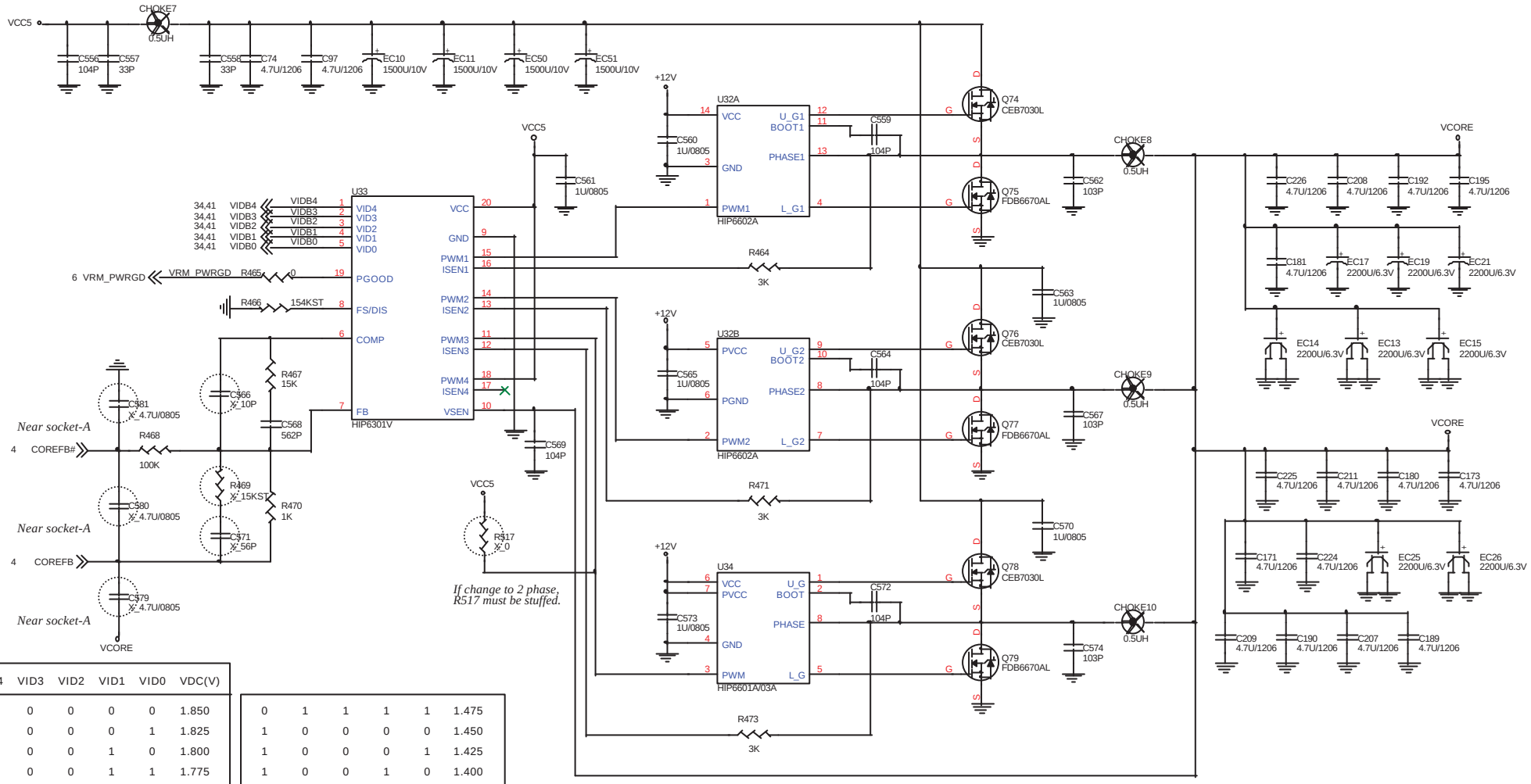
VRM 9.0



VID4	VID3	VID2	VID1	VID0	VDC(V)
0	0	0	0	0	1.850
0	0	0	0	1	1.825
0	0	0	1	0	1.800
0	0	0	1	1	1.775
0	0	1	0	0	1.750
0	0	1	0	1	1.725
0	0	1	1	0	1.700
0	0	1	1	1	1.675
0	1	0	0	0	1.650
0	1	0	0	1	1.625
0	1	0	1	0	1.600
0	1	0	1	1	1.575
0	1	1	0	0	1.550
0	1	1	0	1	1.525
0	1	1	1	0	1.500

0	1	1	1	1	1.475
1	0	0	0	0	1.450
1	0	0	0	1	1.425
1	0	0	1	0	1.400
1	0	0	1	1	1.375
1	0	1	0	0	1.350
1	0	1	0	1	1.325
1	0	1	1	0	1.300
1	0	1	1	1	1.275
1	1	0	0	0	1.250
1	1	0	0	1	1.225
1	1	0	1	0	1.200
1	1	0	1	1	1.175
1	1	1	0	0	1.150
1	1	1	1	1	NoCPU

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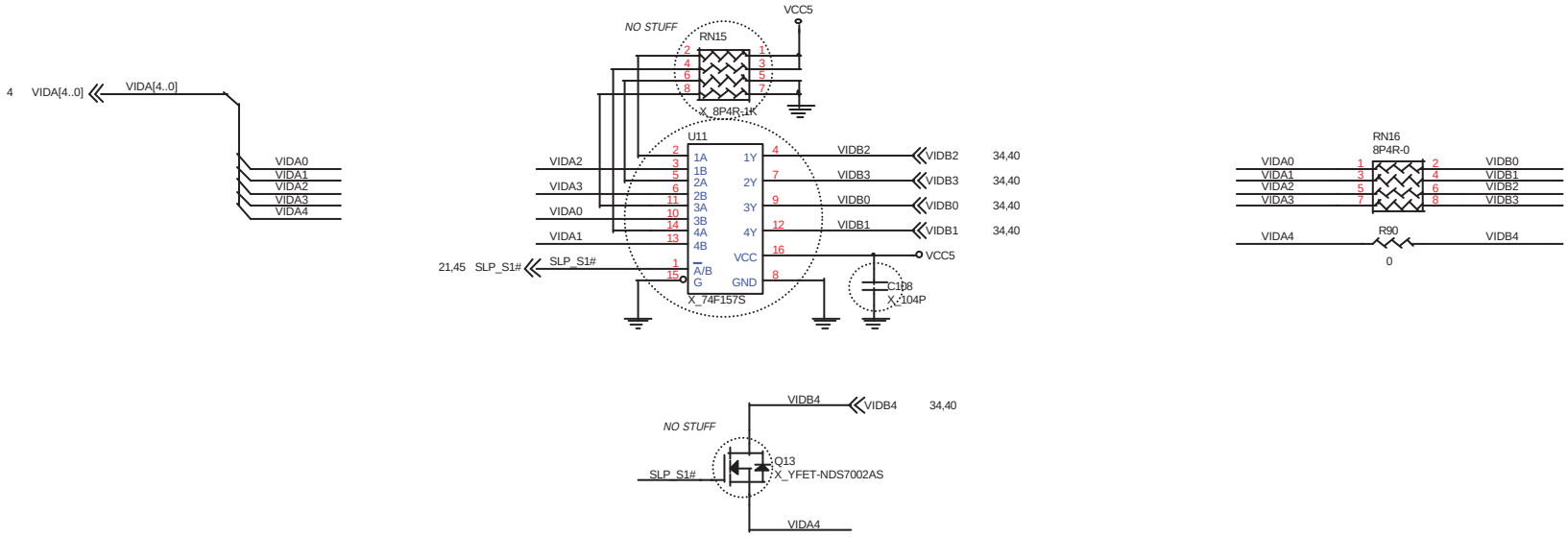
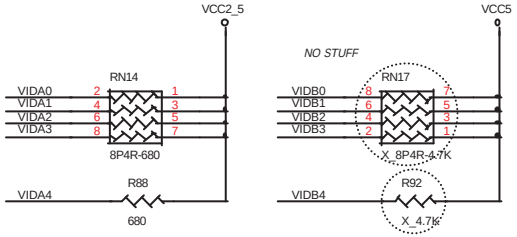
Vcore Setting





Micro Star Restricted Secret

Title: Vcore Setting		Rev: 00D
Document Number: MS-6367		
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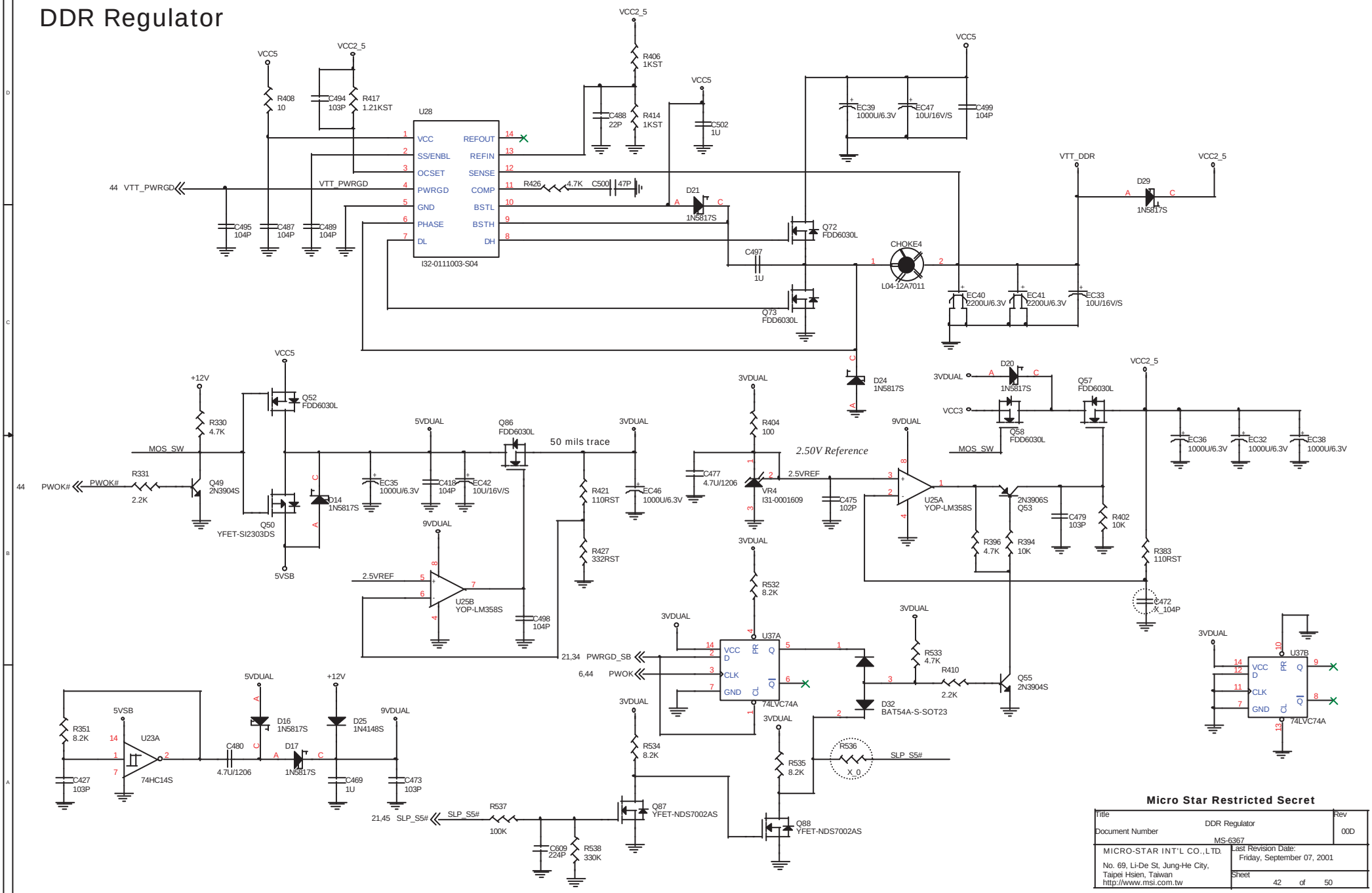
DDR Regulator



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Title	DDR Regulator	Rev
Document Number	MS-6367	00D
MICRO-STAR INT'L CO.,LTD.	Last Revision Date:	Friday, September 07, 2001
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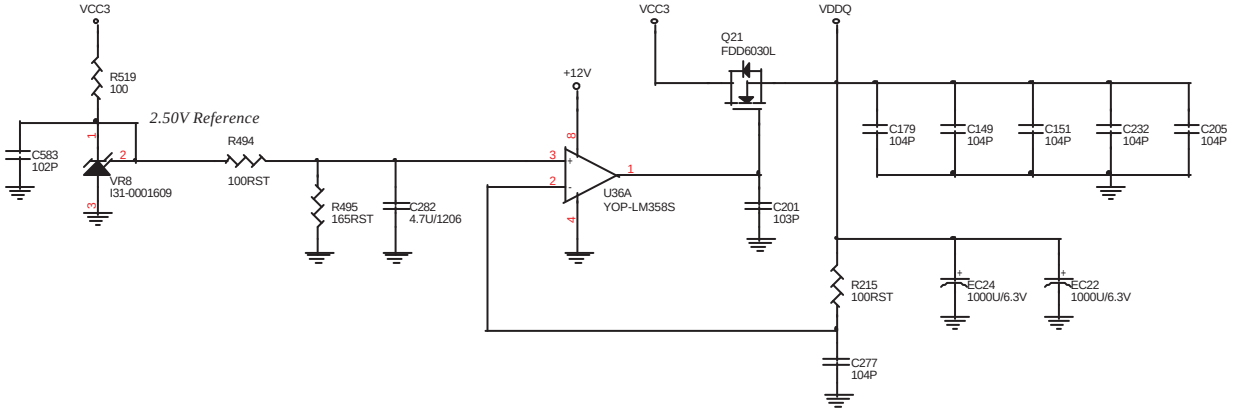
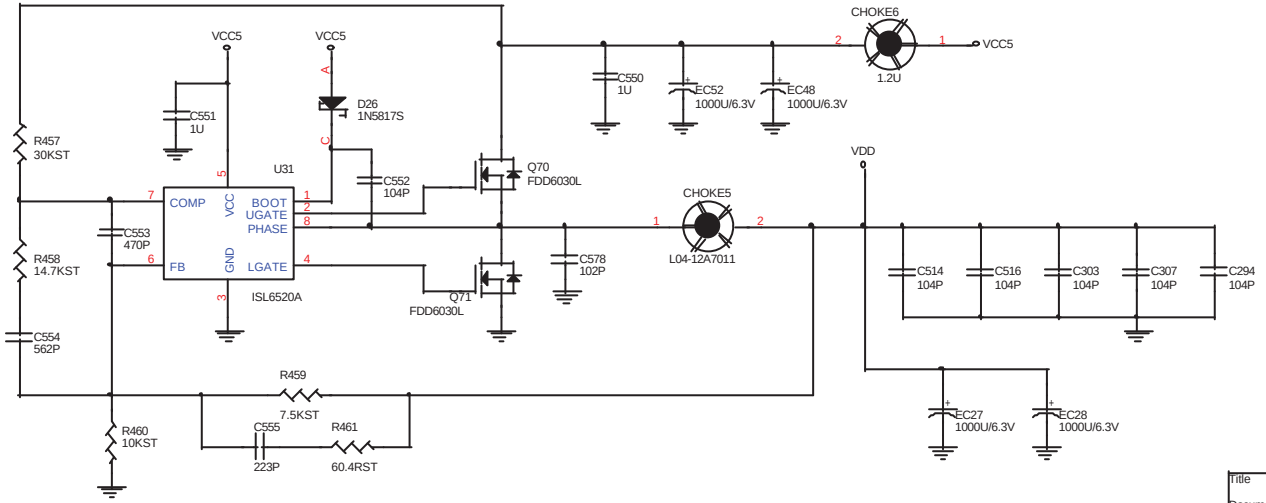
Voltage Regulators

AGP VDDQ 1.5 Voltage Regulator



VCC 1.3 Voltage Regulator



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Title	System Voltage Regulators	Rev 00D
Document Number	MS-6367	
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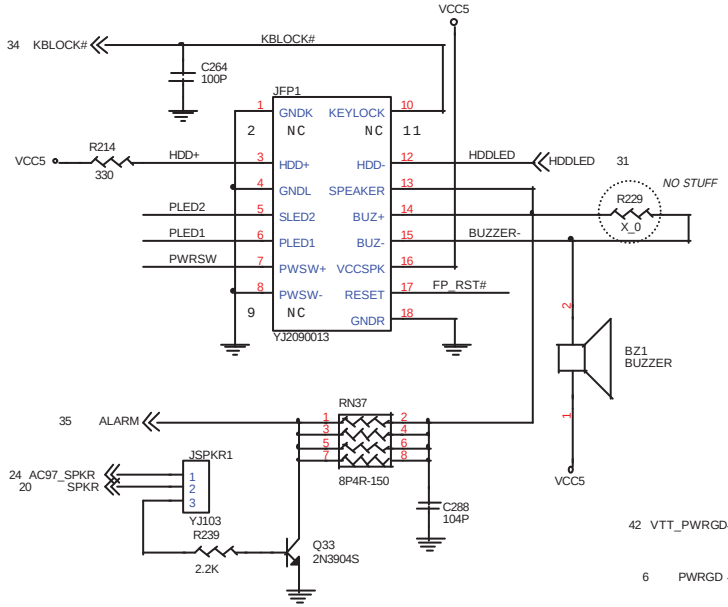
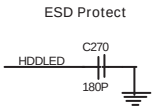
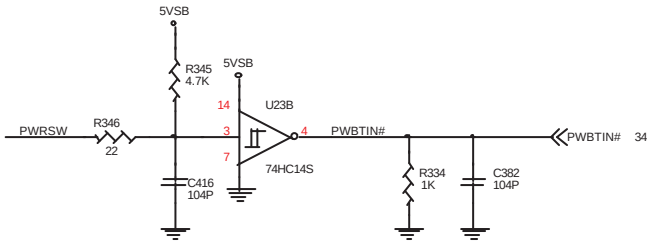
Front Panel and Power Connector

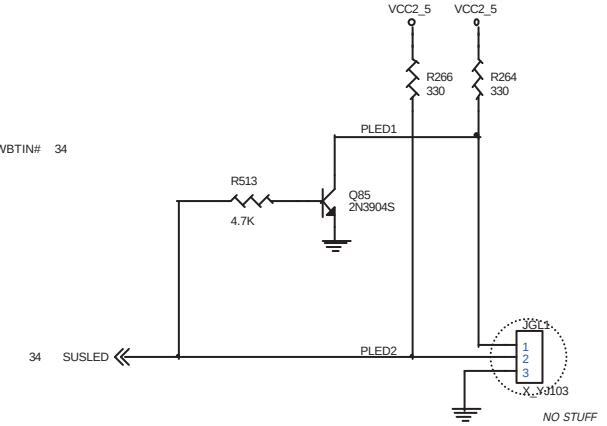
MSI Standard Front Panel Header



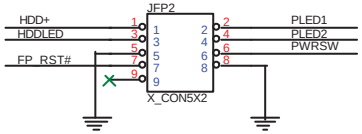
ESD Protect

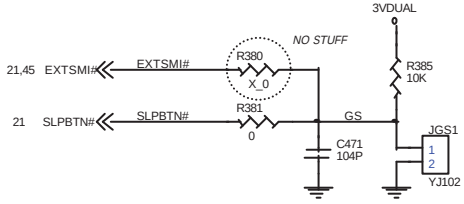


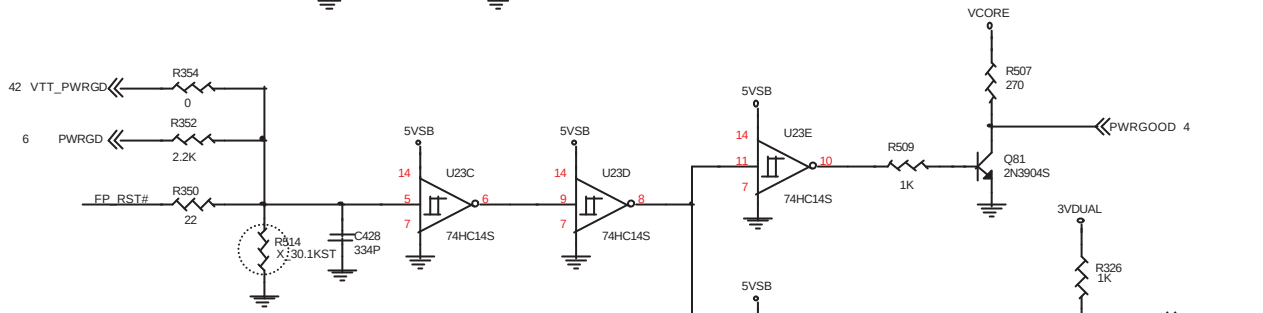


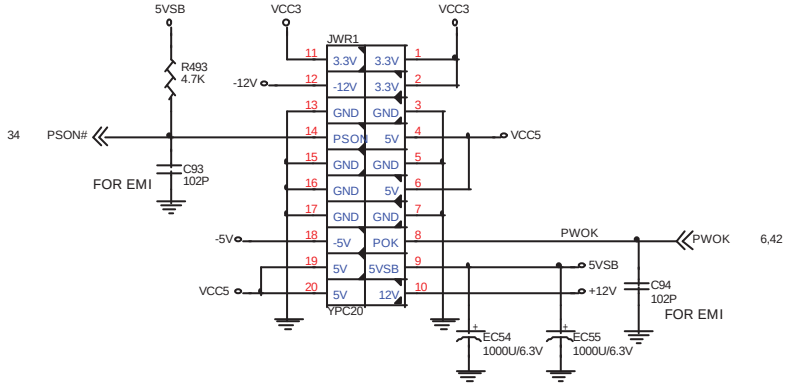


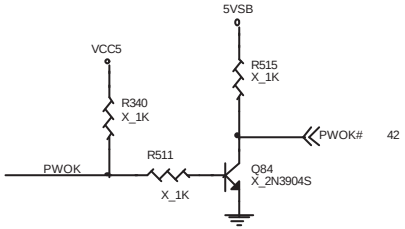
Intel Front Panel Header











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Title	Front Panel and ATX Power Connector	Rev 00D
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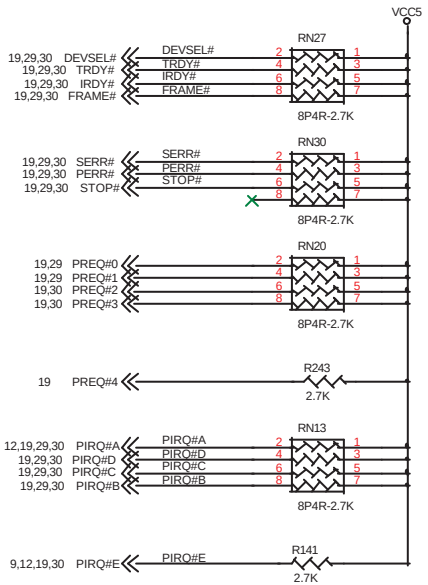
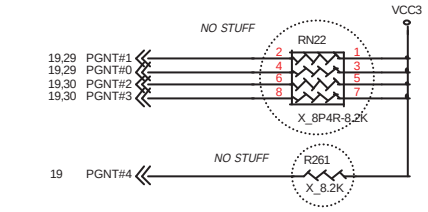
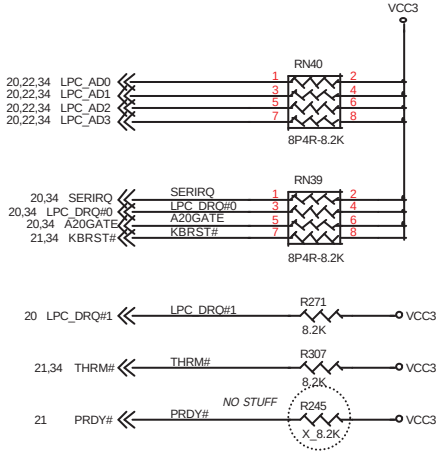
PULL-UP RESISTORS

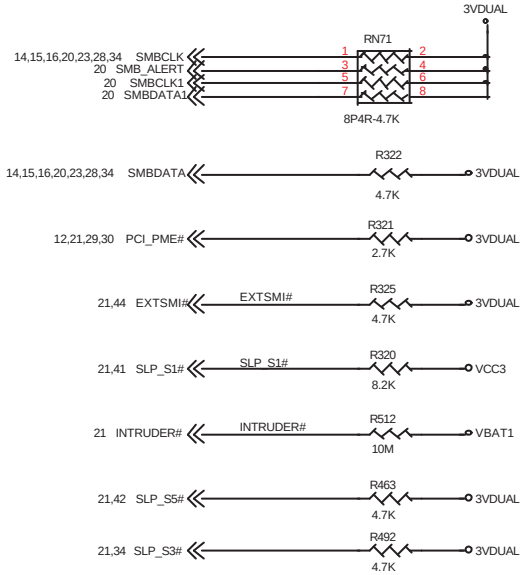
PCI BUS





MCP-1





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Title: Pull-Up Resistors		Rev: 00D
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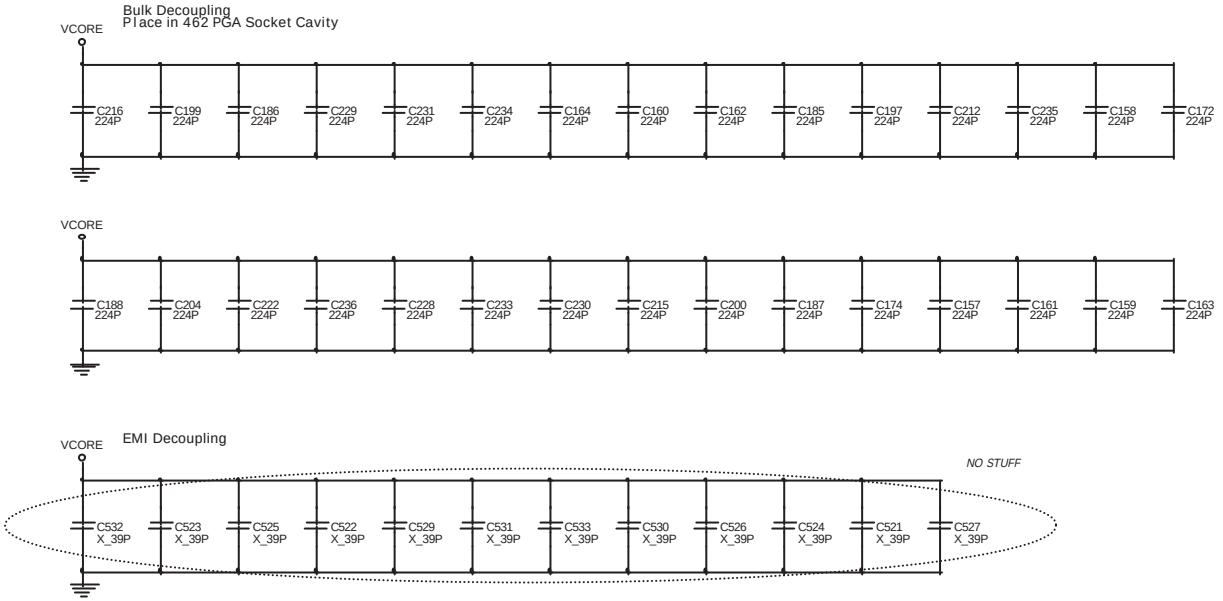
462-pin Socket Decoupling

VCORE DECOUPLING



Micro Star Restricted Secret

Title: VRM Decoupling		Rev: 00D
Document Number: MS-6367		
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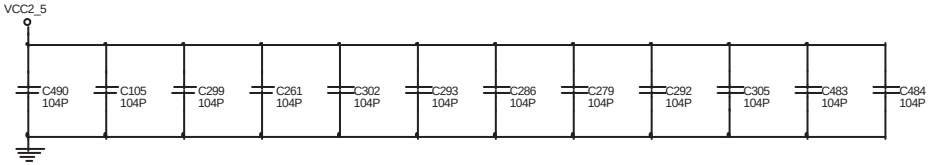
Chipset, and BULK Power Decoupling

CRUSH12 Decoupling

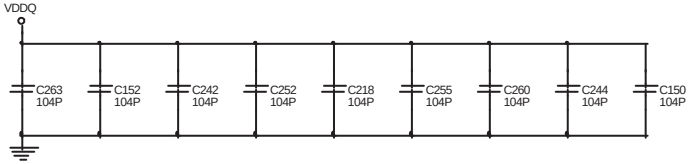
CRUSH12 Core Plane Decoupling

Distribute as close as possible to CRUSH12 System Memory Quadrant



CRUSH12 VDDQ Decoupling

Place near CRUSH12 AGP interface Quadrant

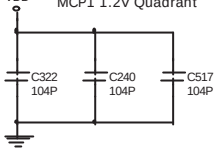


Use surface mount caps placed closed as possible to power pins with short, wide direct connections.

MCP1 Decoupling

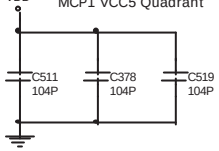
MCP1 Core Plane Decoupling

Distribute as close as possible to MCP1 1.2V Quadrant

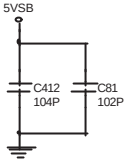


MCP1 VCC5 Decoupling

Distribute as close as possible to MCP1 VCC5 Quadrant

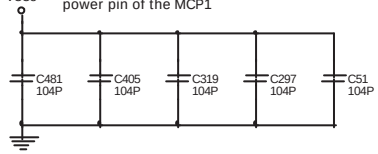


Distribute near the 5V standby Power pin of the MCP1



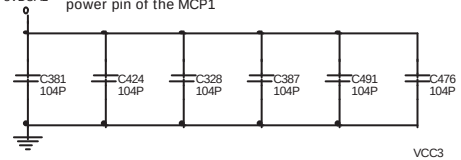
MCP1 3.3V Plane Decoupling:

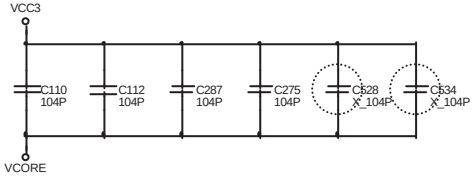
Distribute near the 3.3V power pin of the MCP1



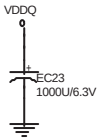
MCP1 3VDUAL Decoupling

Distribute near the 3.3V standby power pin of the MCP1

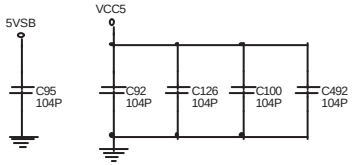




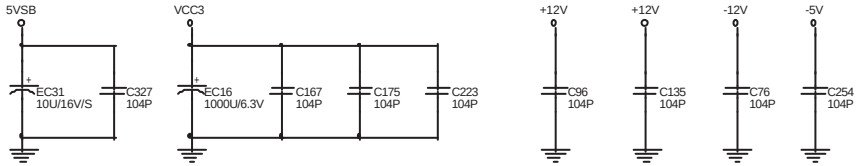
AGP Decoupling

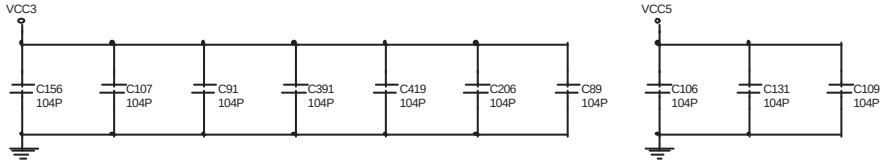


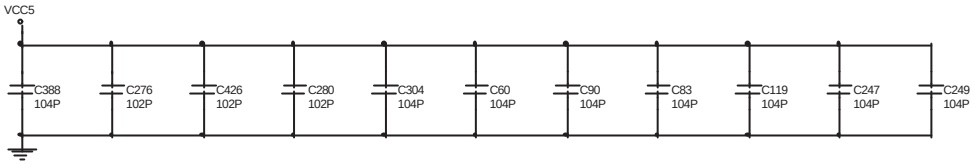
Distribute near the VCC power pin of the LPC

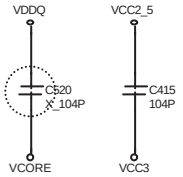


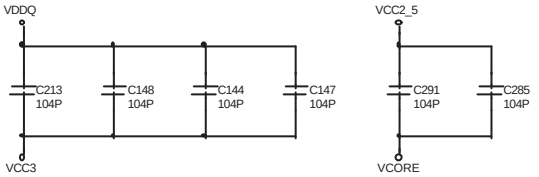
Bulk Power Decoupling











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Title	CRUSH12 and MCP1 Decoupling	Rev 00D
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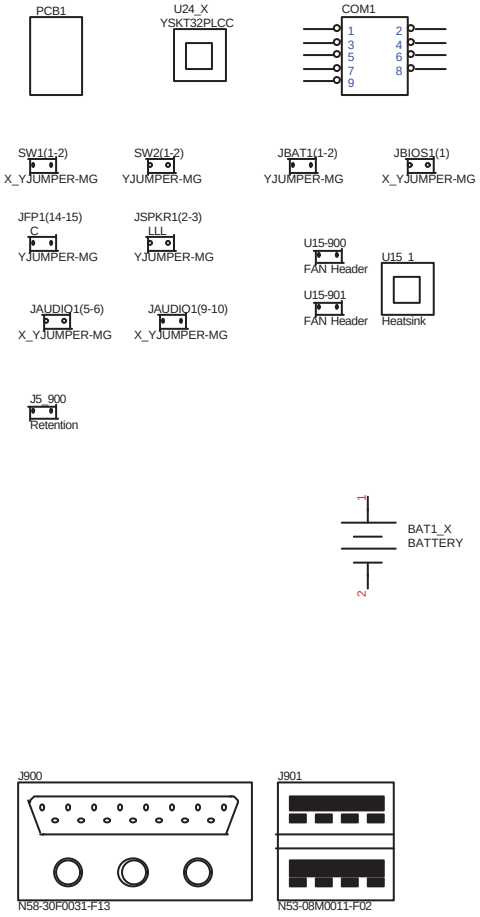
AutoBOM Manual Parts



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Title	AutoBOM Manual parts	Rev 00D
Document Number	MS-6367	
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Revision History I

Revision History (Changes from Rev 0A)

4	Changed signals FID0~FID3 pull up from VCC2_5 to Vcore.
5	Changed VR2 431L regulator load cap C129 from 0.01uF to 0.001uF for stability output.
6	Added PLL delay circuit for CRUSH and MCP1 internal PLL power.
7	Changed CRUSH ball out to version B01.
	Added LCL filter to improve SMD S2K signals INCLK noise.
8	Changed memory controller signals MCS_B#0~3 connection.
9	Changed signal LDT_RSET current reference pull down resistor from 100ohms 1% to 50ohms 1%.
	Changed signal DACRSET voltage reference pull down resistor from 121ohms 1% to 110ohms 1%.
11	Changed SW1 from 2X3 pin header to 1X3 pin header, signal SBA0 directly pull up to VDDQ.
12	Modified AGP reset input connected to PCIRST# directly, not through divide voltage resistors.
17	Changed system memory bank A MDQ, MDQS, MDQM termination resistors to 62 ohms.
19	Changed signal LDT_RSET current reference pull down resistor from 100ohms 1% to 50ohms 1%.
20	Changed the VBAT circuit.
	Changed MCP1 strap SPKR pull up to VCC5.
	Changed MCP1 signal TEST pull down resistor to 10K ohms.
21	Changed MCP1 VAUX_C circuit.
	Changed USB_VDD and USB_VREF connected to 3VDUAL.
	Changed MCP1 strap signal MII_TXD0 from pull up to pull down.
22	Connected flashrom pin 28 to GND for SST LPC flashrom.
36	Modified CPU fan circuit for MCP1 power on controled pin inital status.
43	Modified DDR_VREF regulator U28 pin 9 and 10 circuit, and remove R397 and R411.
	Changed VR4 431L regulator load cap C475 from 0.1uF to 0.001uF for stability output.
	Connected +12V to 9VDUAL for power on 9VDUAL source.
44	Changed VR3 431L regulator load cap C282 from 0.1uF to 0.001uF for stability output.
	Chnaged VDD 1.2V linear regulator to switching regulator.
45	Removed R333 for signal PWBTIN#.
	Added 7408 to powerok circuit.

Revision History II