

MS-6337

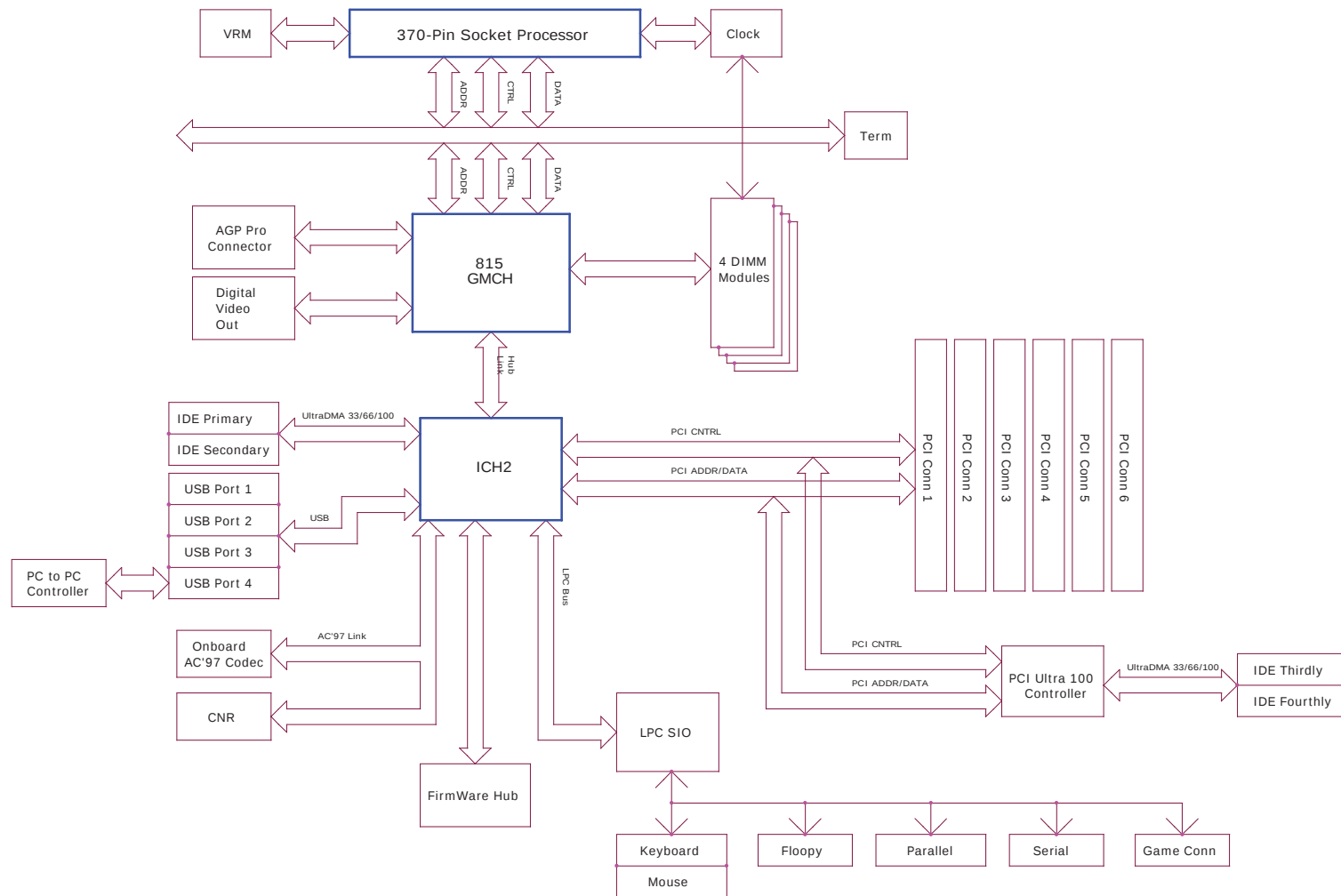
ATX
Intel® PGA 370 Processor
Intel Solano2 Chipset
Winbond 83627HF-AW LPC I/O
PROMISE PDC20265 PCI Ultra 100 Controller
Genesys USB PC to PC Networking Controller

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Block Diagram



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General Spec.

ICH2

GPIO Pin	Type	Function
GPIO 0	I	REQ#A (multifunction pin)
GPIO 1	I	PREQ#5 (multifunction pin)
GPIO 2	I	Pull up through 2.7K ohms (PIRQE#)
GPIO 3	I	Pull up through 2.7K ohms (PIRQF#)
GPIO 4	I	Pull up through 2.7K ohms (PIRQG#)
GPIO 5	I	Pull up through 2.7K ohms (PIRQH#)
GPIO 6	I	Primary IDE ATA66/100 detection (ATADET0)
GPIO 7	I	Secondary IDE ATA66/100 detection (ATADET1)
GPIO 8	I	Pull Up to 3.3VSBY through 10K ohms (LAN Wake Up)
GPIO 9	I	Not Implemented
GPIO 10	I	Not Implemented
GPIO 11	I	SMB_ALERT (multifunction pin)
GPIO 12	I	Pull Up to 3.3VSBY through 4.7K ohms (External SMI)
GPIO 13	I	Pull Up to 3.3VSBY through 4.7K ohms (LPC PME)
GPIO 14~15	I	Not Implemented
GPIO 16	O	GNT#A (multifunction pin)
GPIO 17	O	PGNT#5 (multifunction pin)
GPIO 18	O	Pull down through 8.2K ohms (unused)
GPIO 19	O	accomplished with GPIO20 for DIMM voltage
GPIO 20	O	accomplished with GPIO19 for DIMM voltage
GPIO 21	O	Pull Up to 3.3V through 4.7K ohms (Vcore Setting)
GPIO 22	OD	Not Connected
GPIO 23	O	Pull Up to 3.3V through 4.7K ohms (BIOS protect)
GPIO 24	I/O	Pull Up to 3.3VSBY through 4.7K ohms (STR Control)
GPIO 25	I/O	Pull Up to 3.3VSBY through 4.7K ohms (KBVCC Control)
GPIO 26	I/O	Not Implemented
GPIO 27	I/O	Pull Up to 3.3V through 4.7K ohms (Audio Control)
GPIO 28	I/O	CNR Detected
GPIO 29~31	O	Not Implemented

VCC3STR	GPO19	GPO20
3.3V	1	1
3.4V	0	1
3.5V	1	0
3.6V	0	0

BIOS Protect Config.	GPIO23
BIOS Un_Protected	1
BIOS Protected	0

VCORE Setting	GPIO21
CPU Default	1
Maanuel Setting	0

STR Control Config.	GPIO24
Power Off	X
Power On / Disable	1
Before Enter S3	0

KBVCC Config.	GPIO25
KB Power On Enable	1
KB Power On Disable	0

FWH

GPIO Pin	Type	Function
GPI 0	I	Pull down through 8.2K ohms (unused)
GPI 1	I	Pull down through 8.2K ohms (unused)
GPI 2	I	GPI2 = 0 GPI3 = 1 ; Flash from FDD
GPI 3	I	GPI2 = 1 GPI3 = 0 ; Boot Auto clear CMOS
GPI 4	I	Pull up through 1K ohms (unused)

LPC

GPIO Pin	Type	Function
GPIO 24	I/O	Pull Up to 5V through 22K ohms (DLED2)
GPIO 32	I/O	Pull Up to 5V through 22K ohms (DLED1)
GPIO 33	I/O	Pull Up to 5V through 22K ohms (DLED4)
GPIO 34	I/O	Pull Up to 5V through 22K ohms (DLED3)

PCI Config.

DEVICE	ICH INT Pin	IDSEL	CLOCK	CLK GEN PIN OUT
PCI Slot 1	INTA# INTB# INTC# INTD#	AD16	PCICLK1	ICS94201 13 (PCI2/SEL24_48#)
PCI Slot 2	INTB# INTC# INTD# INTA#	AD17	PCICLK2	ICS94201 15 (PCI3)
PCI Slot 3	INTC# INTD# INTA# INTB#	AD18	PCICLK3	ICS94201 16 (PCI4)
PCI Slot 4	INTD# INTA# INTB# INTC#	AD19	PCICLK4	PCI PLL 22 (PCI1)
PCI Slot 5	INTA# INTB# INTC# INTD#	AD20	PCICLK5	ICS94201 17 (PCI5)
PCI Slot 6	INTB# INTC# INTD# INTA#	AD21	PCICLK6	PCI PLL 20 (PCI6)
Ultra 100	INTB#	AD25*	ATAPCLK	PCI PLL 19 (PCI3)
PCI PLL			PCICLK1	ICS94201 19 (PCI6)

* ICH2 reserved PCI address line AD22 for the PCI-to-ISA Bridge's IDSEL input.

DIMM Config.

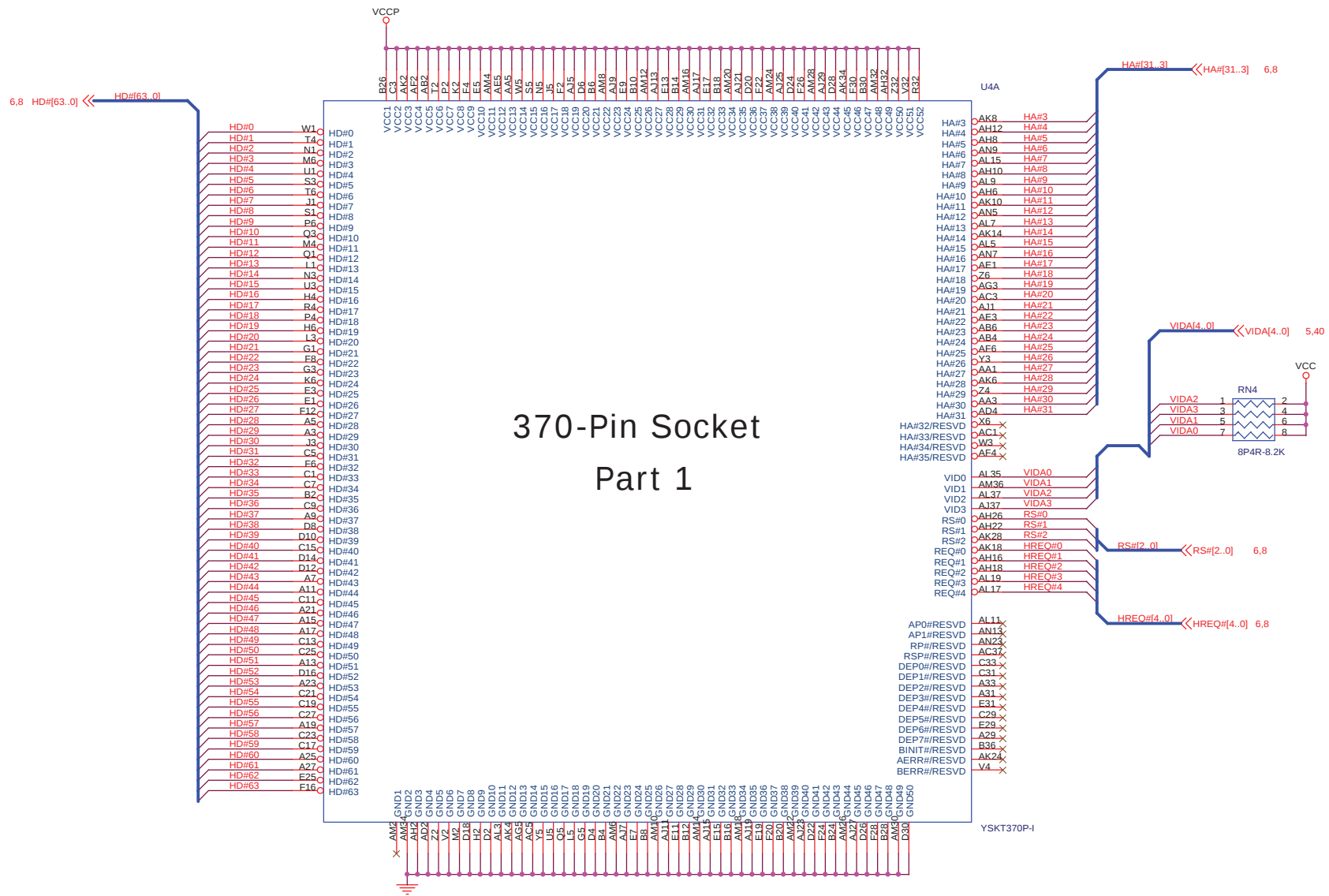
DEVICE	ADDRESS	CLOCK
DIMM 1	1010000B	DCLK4 DCLK5 DCLK0 DCLK1
DIMM 2	1010001B	DCLK11 DCLK9 DCLK2 DCLK3
DIMM 3	1010010B	DCLK8 DCLK10 DCLK7 DCLK6
DIMM 4	1010011B	DCLK10 DCLK8 DCLK6 DCLK7

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370PGA Socket Part 1

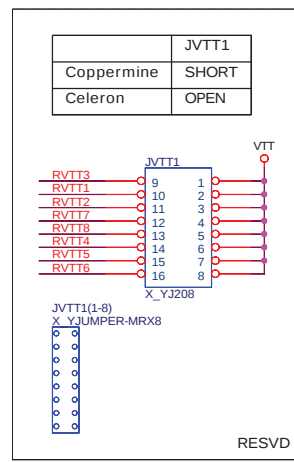
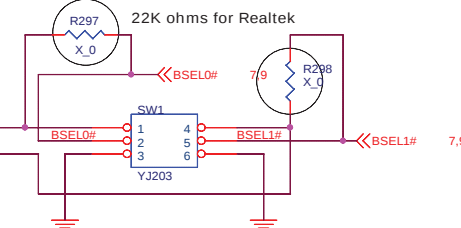
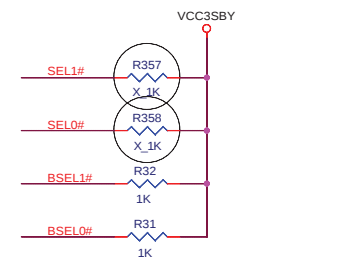
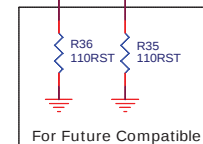
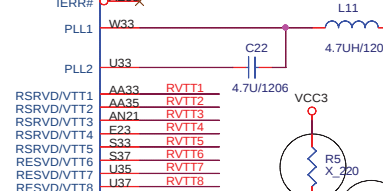
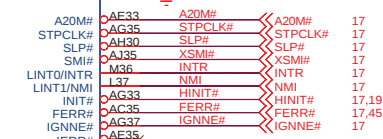
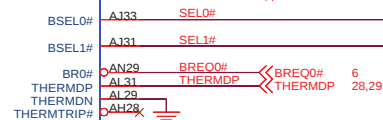
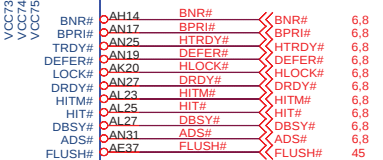
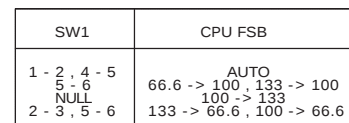
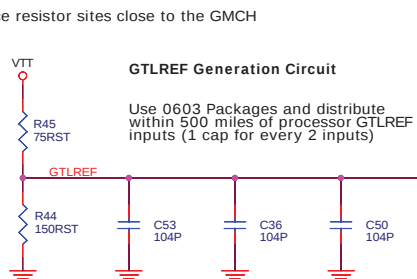
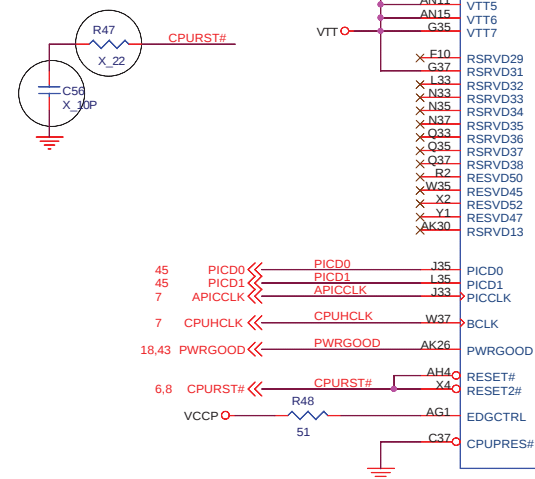
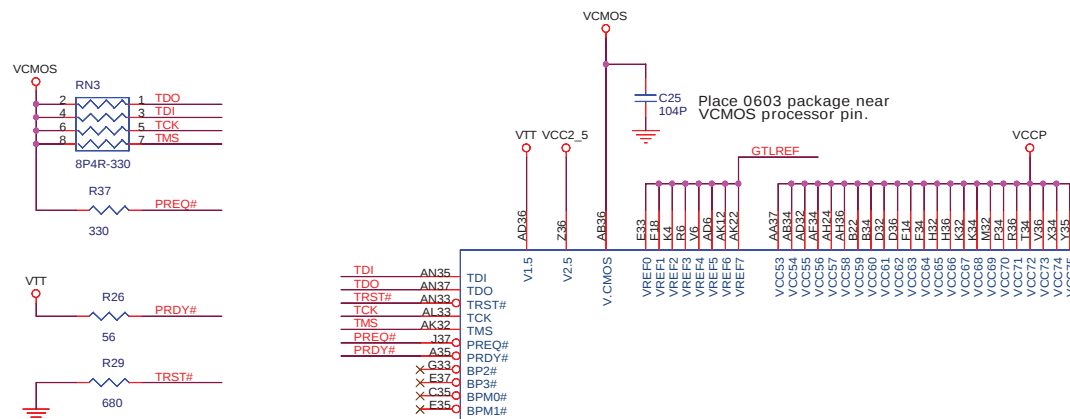
370-Pin Socket Part 1



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370PGA Socket Part 2

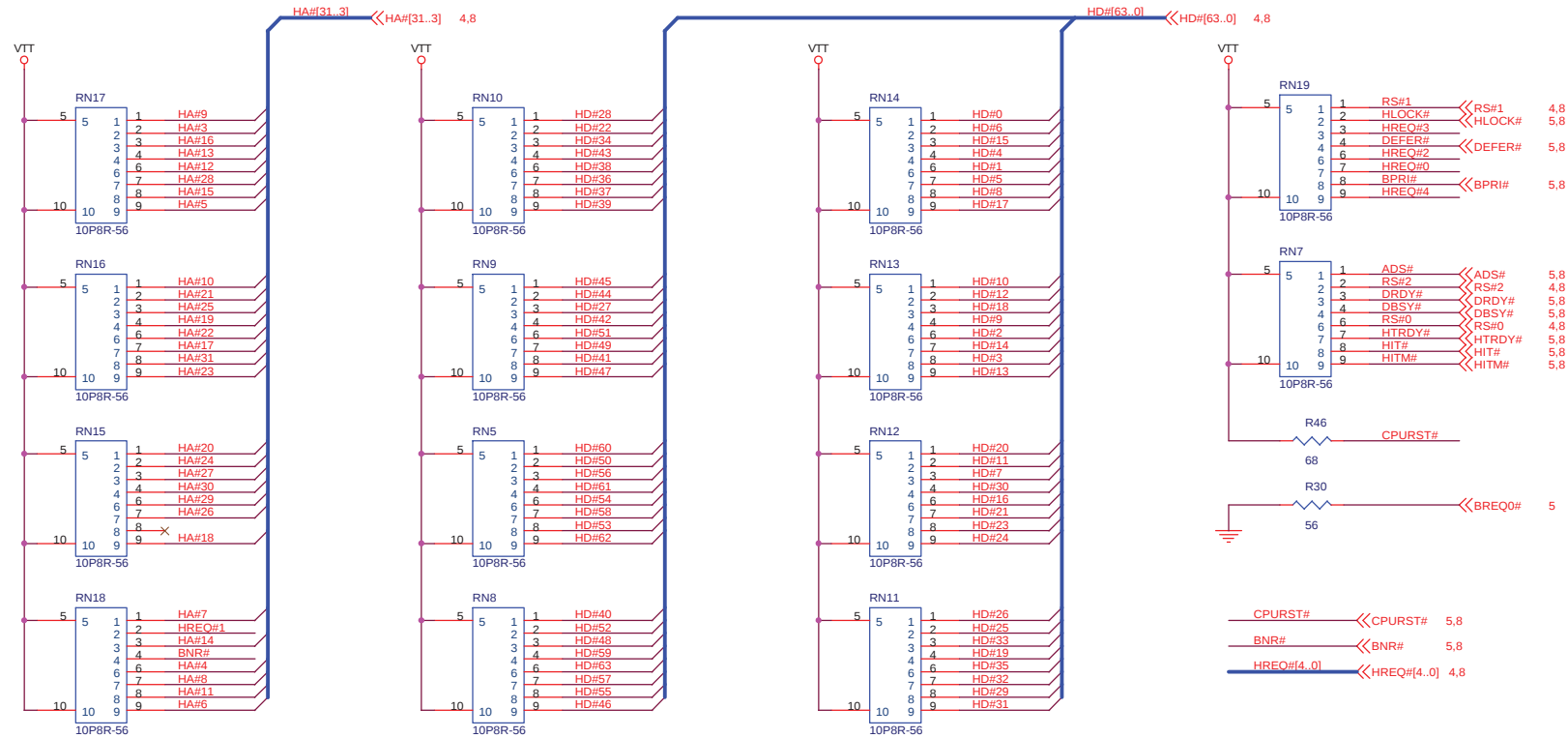


VID	VCOREDET	CPURES#	
1001	0	0	PIII FC-PGA
1011	0	0	Celeron FC-PGA
0001	1	0	Celeron PPGA
1111	X	1	No Processor

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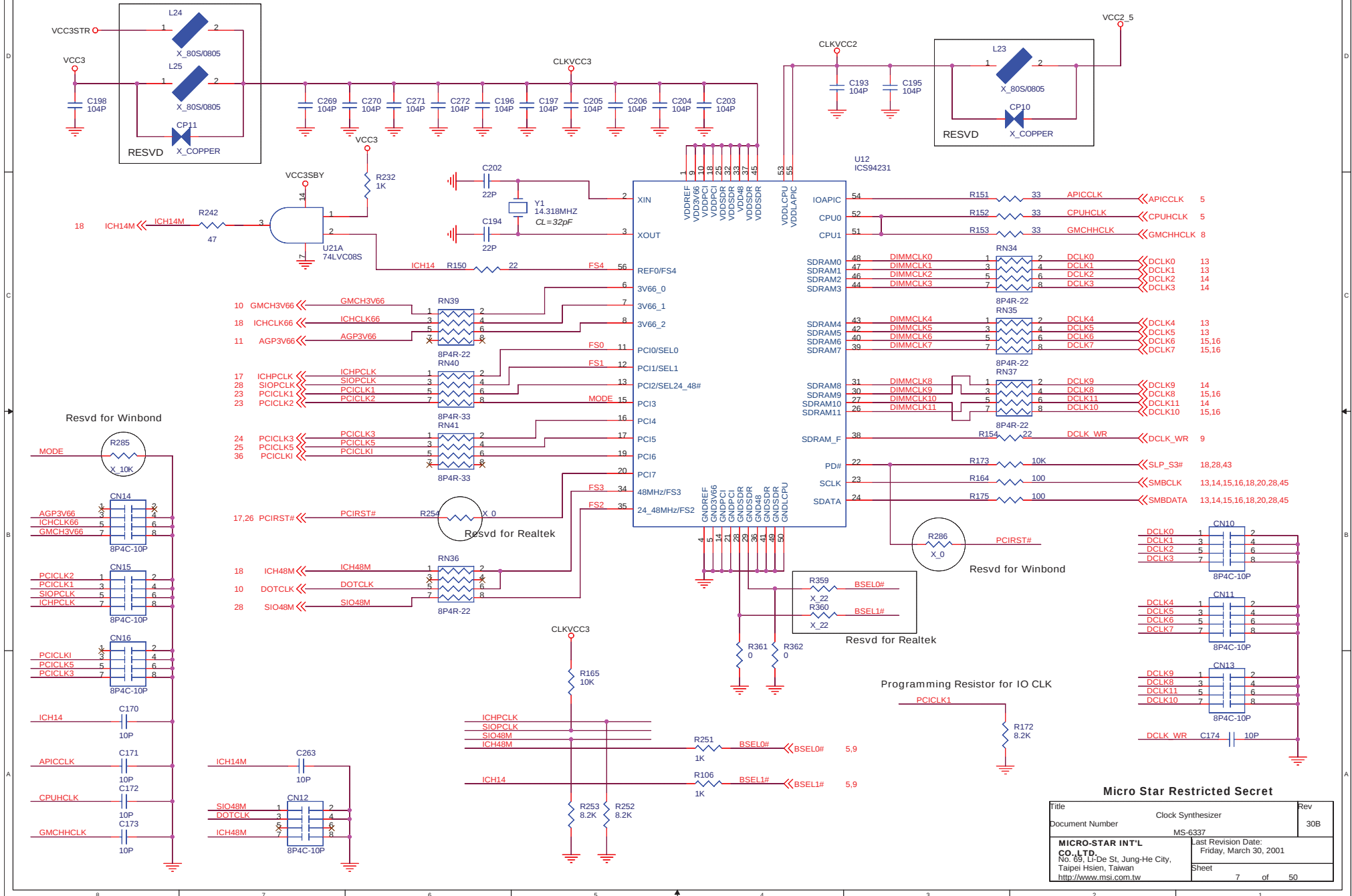
AGTL Termination



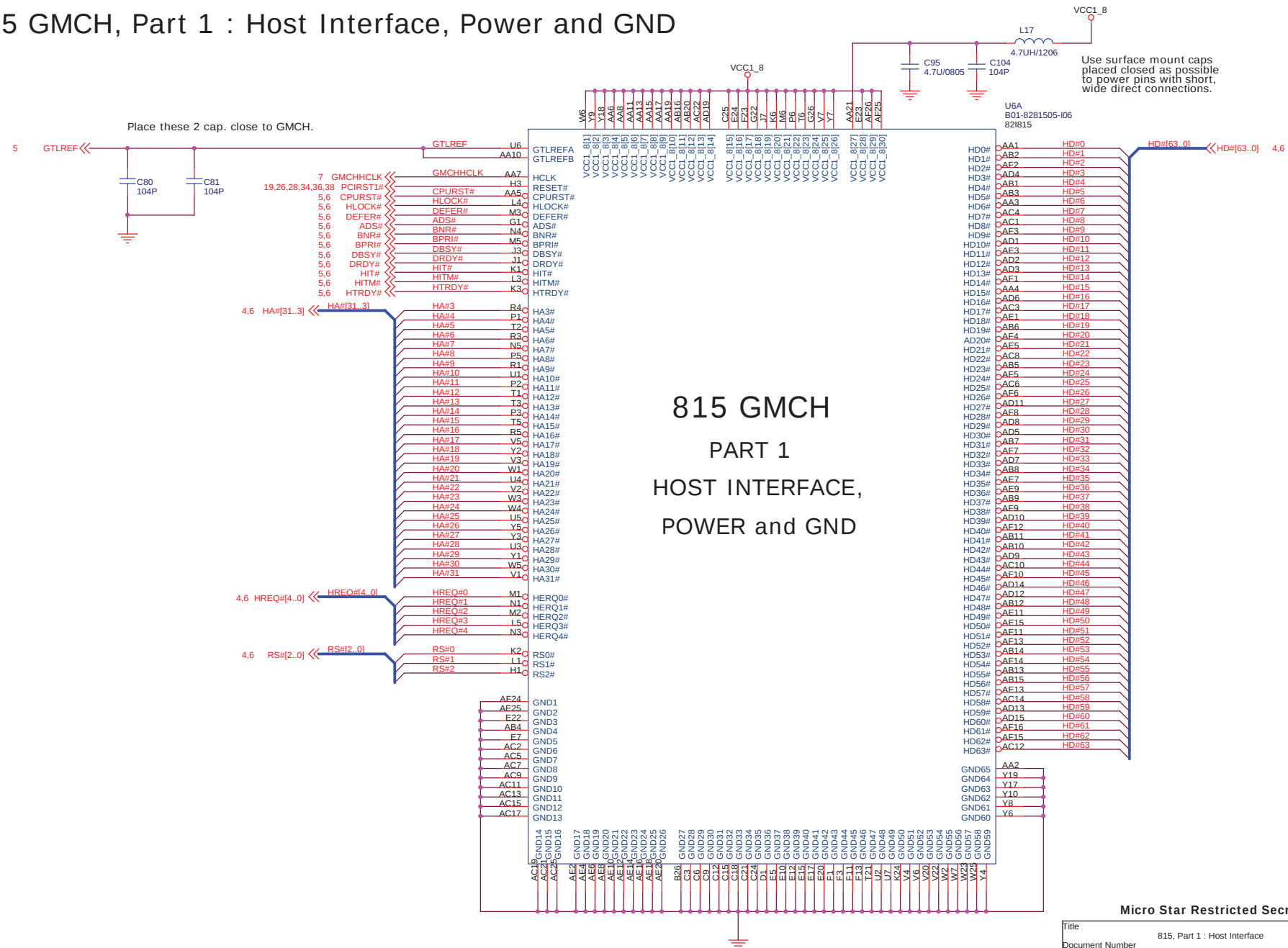
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Clock Synthesizer



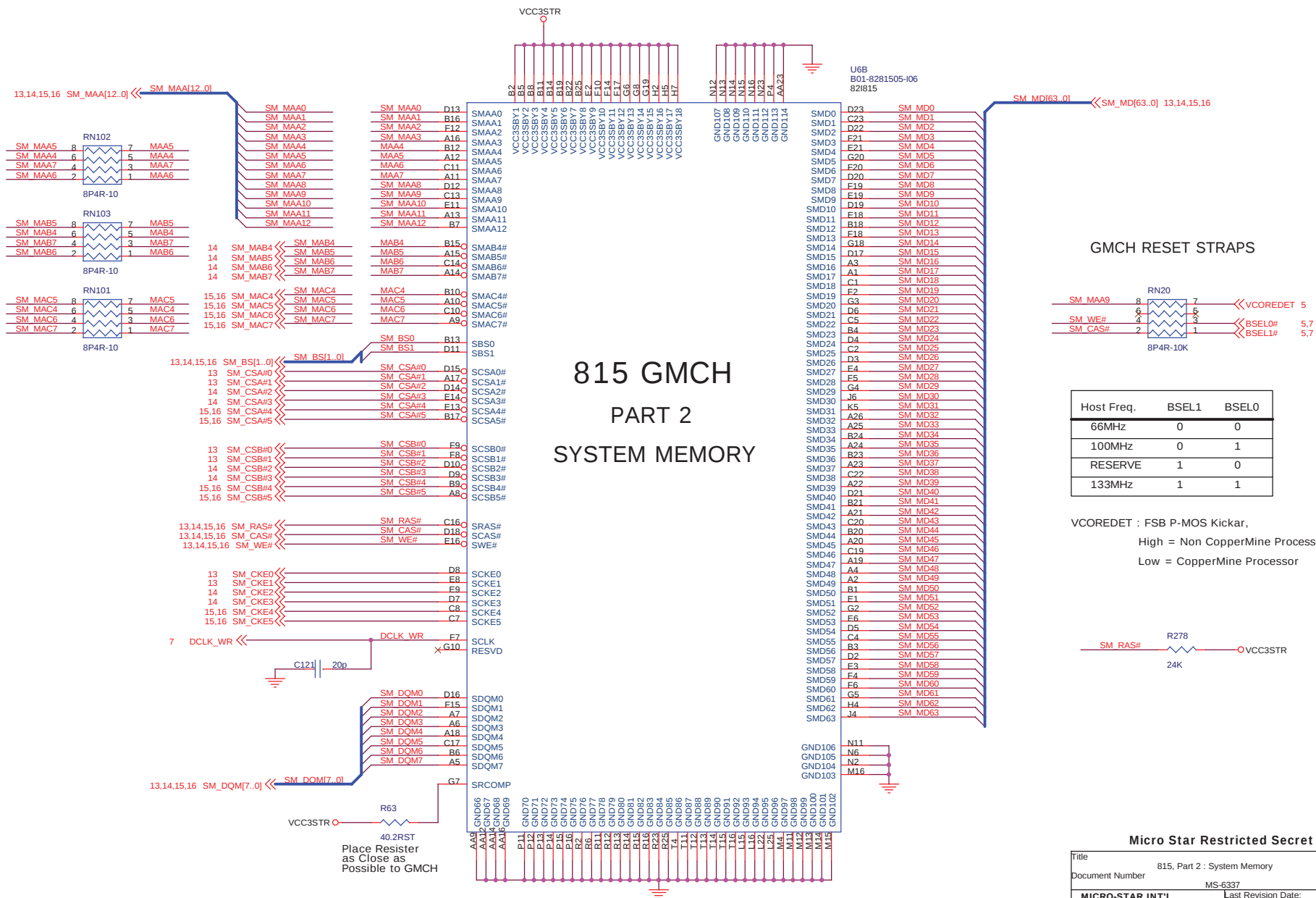
815 GMCH, Part 1 : Host Interface, Power and GND



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Title	815, Part 1 : Host Interface	Rev	
Document Number	MS-6337		30B
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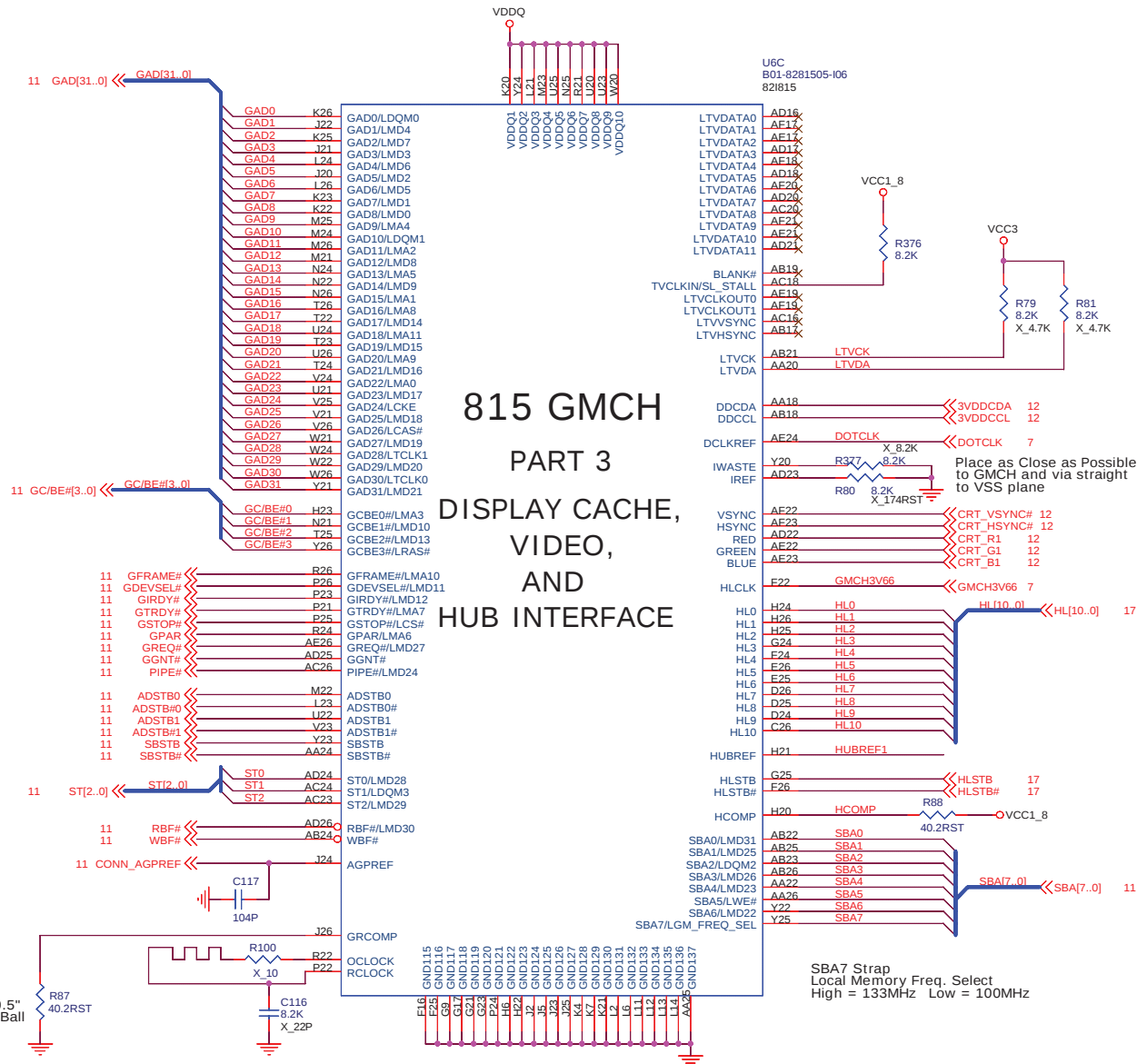
815 GMCH, Part 2 : Memory Interface



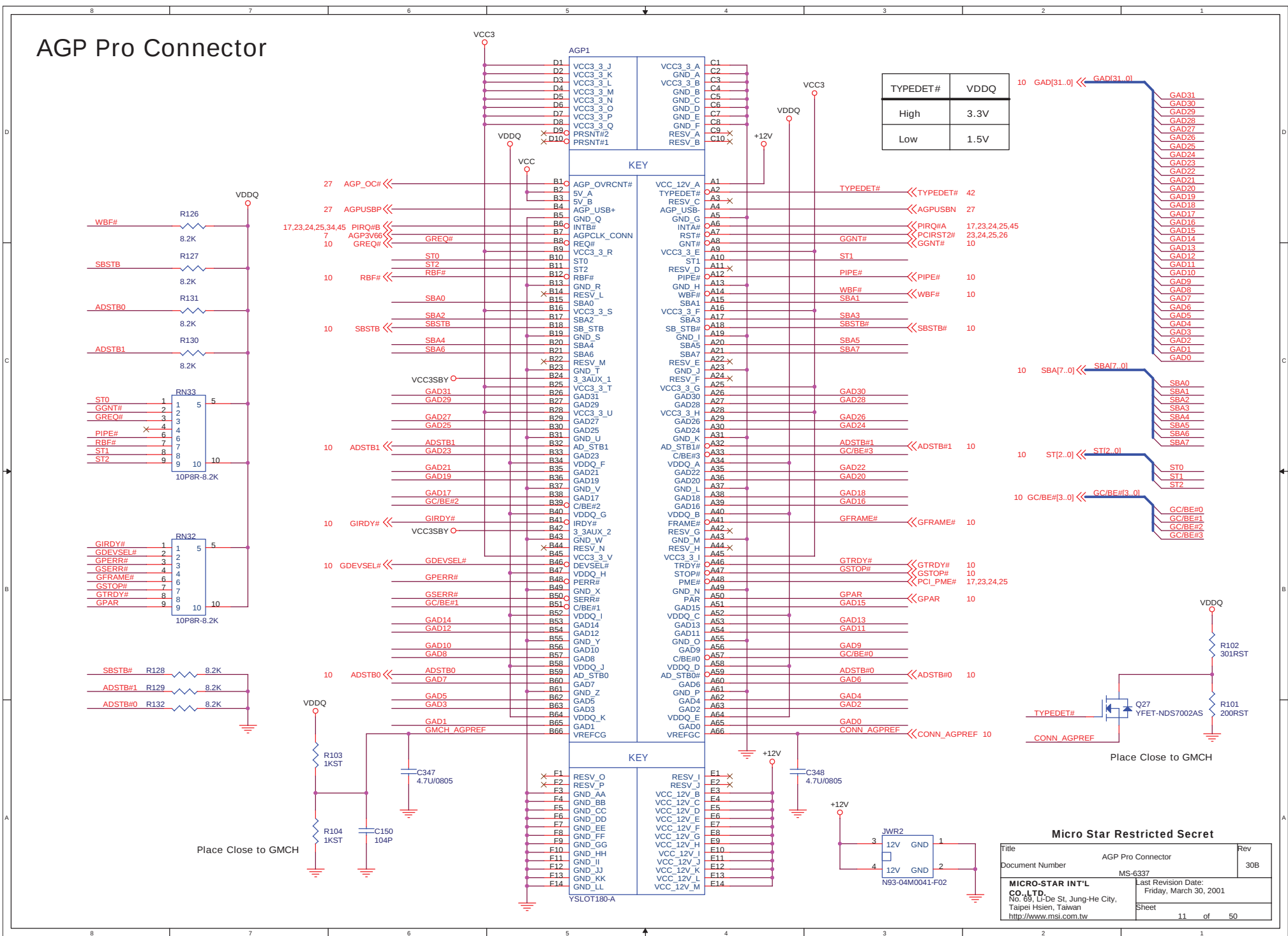
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Title	815, Part 2 : System Memory	Rev
Document Number	MS-6337	30B
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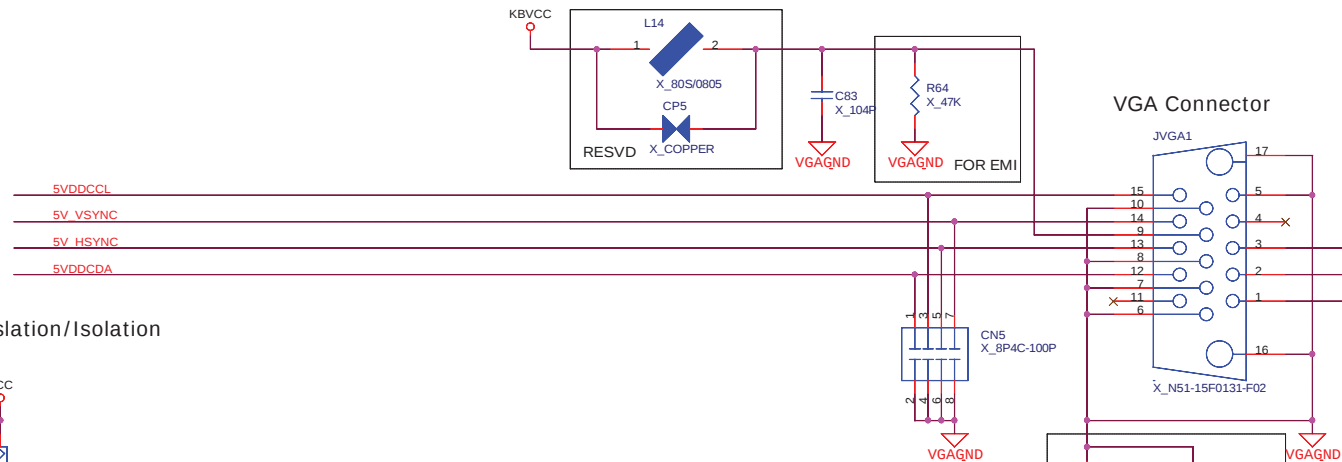
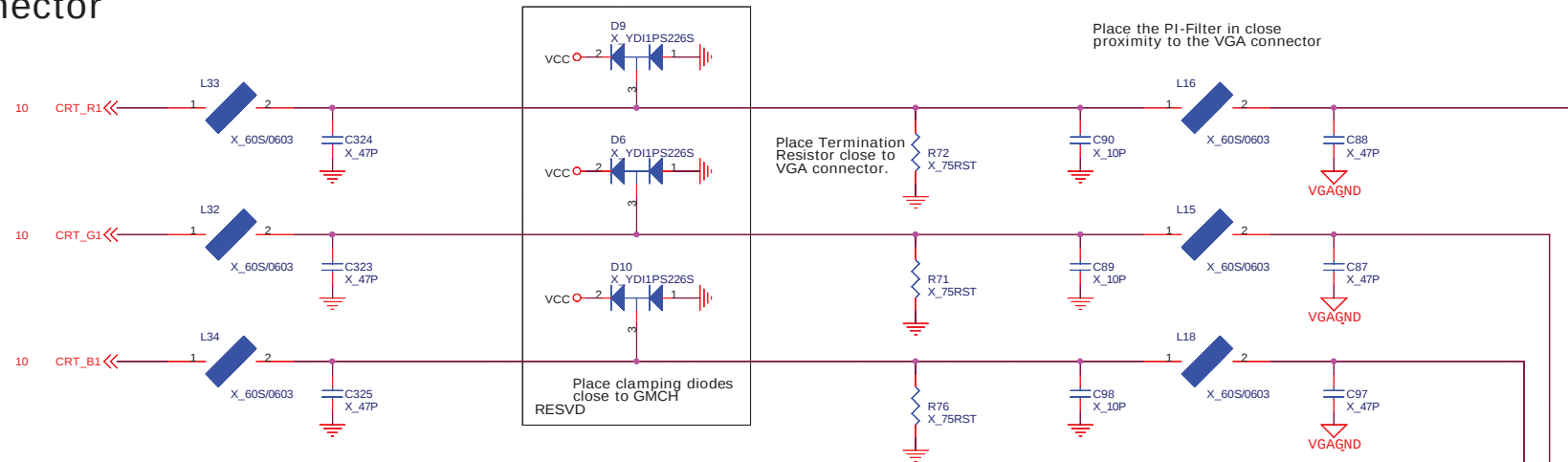
815 GMCH Part 3 : AGP/Display Cache, Video and HUB Interface



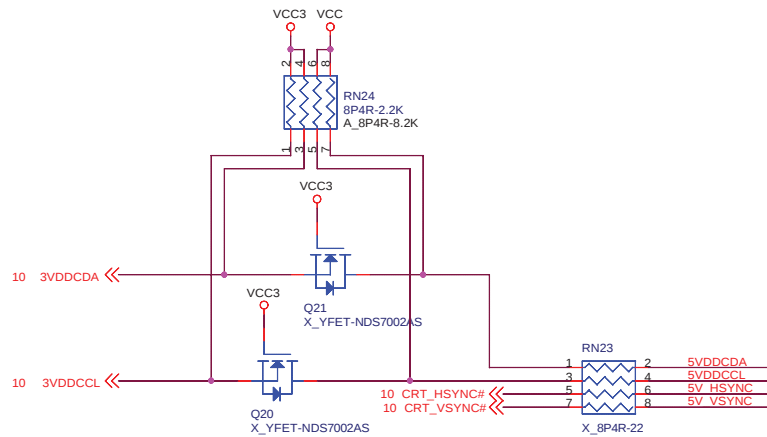
AGP Pro Connector



Video Connector



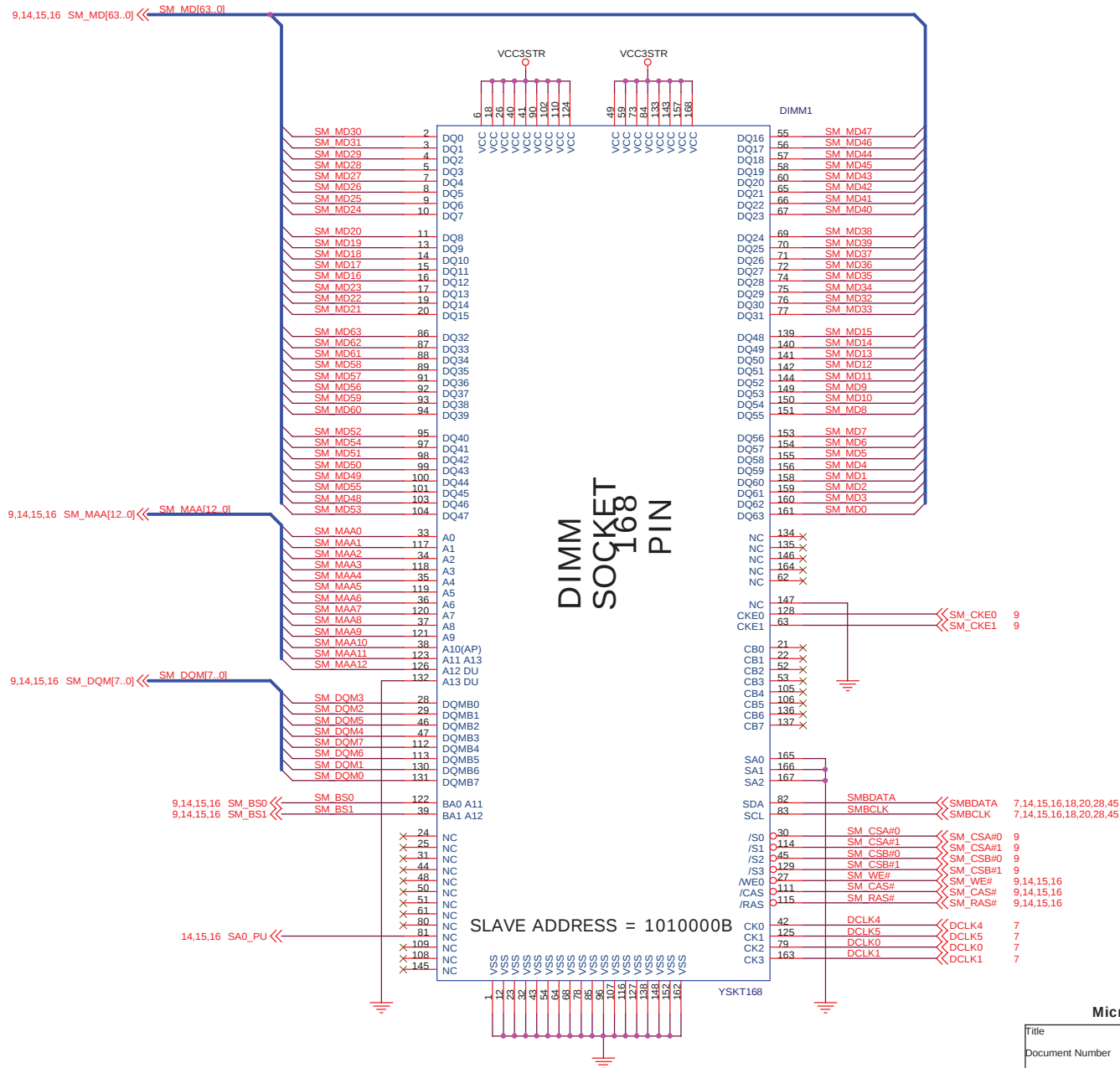
5V to 3.3V Translation/Isolation



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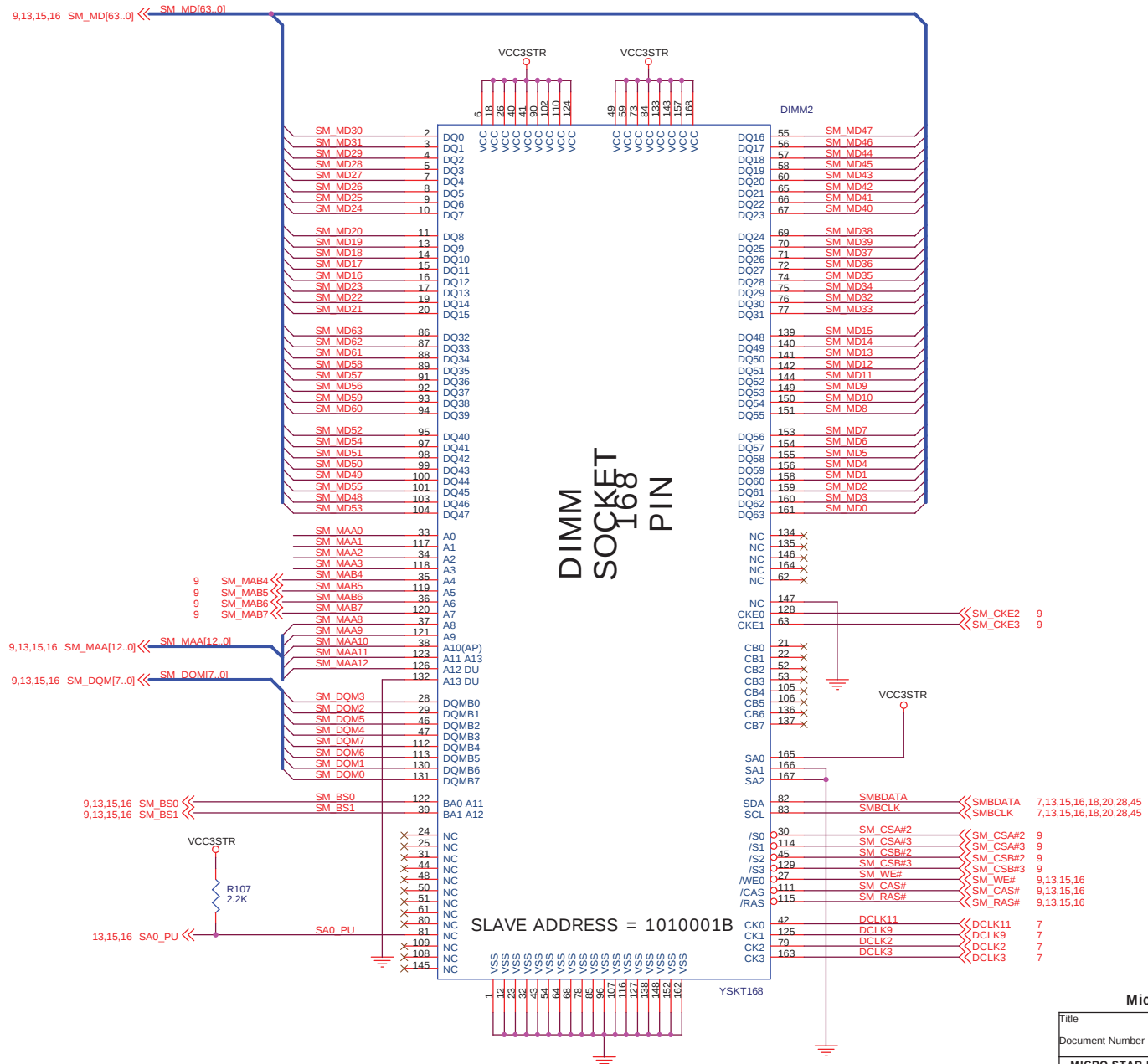
SYSTEM MEMORY



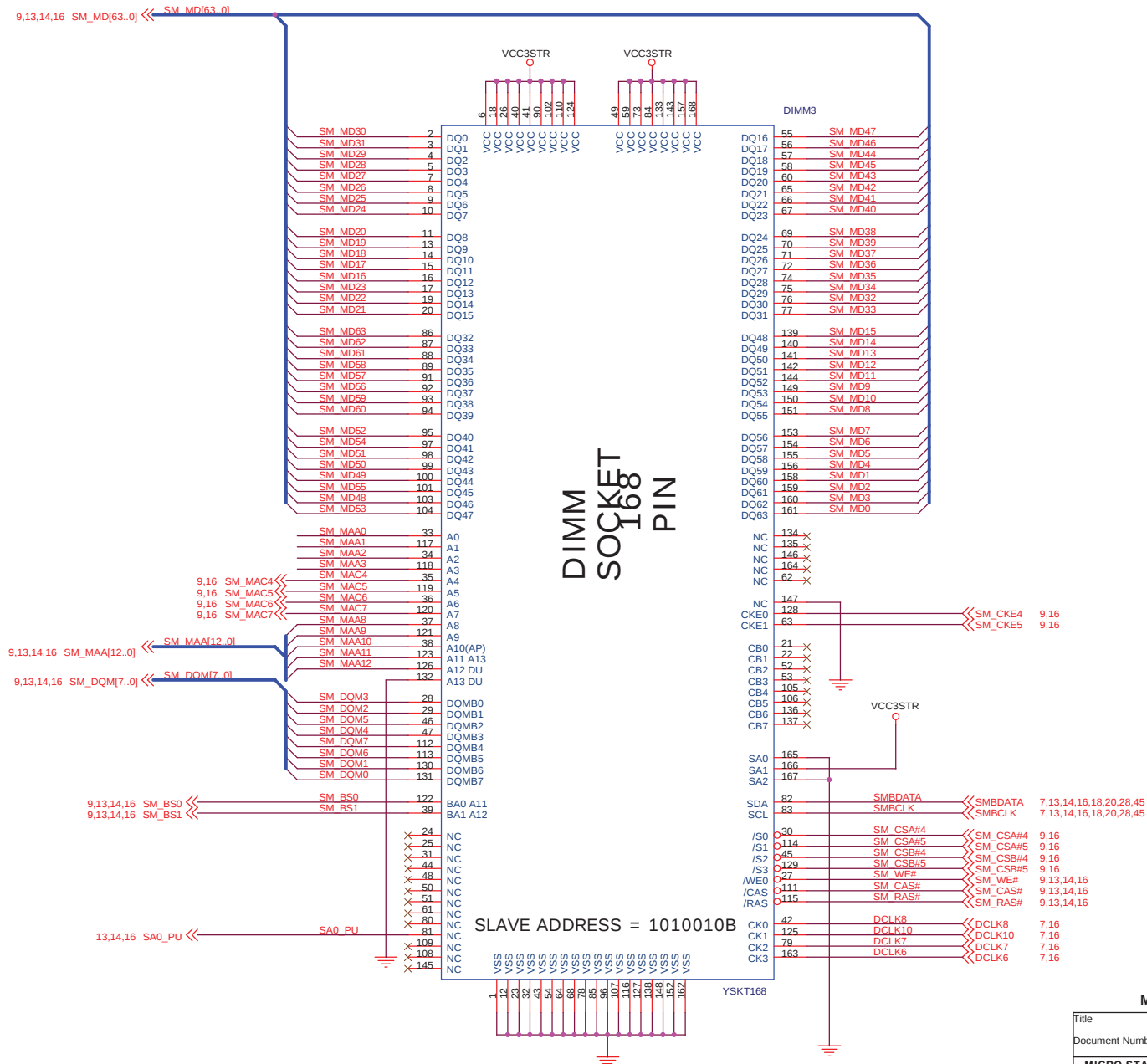
Micro Star Restricted Secret

Title	System Memory : DIMM 1	Rev
Document Number	MS-6337	30B
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SYSTEM MEMORY



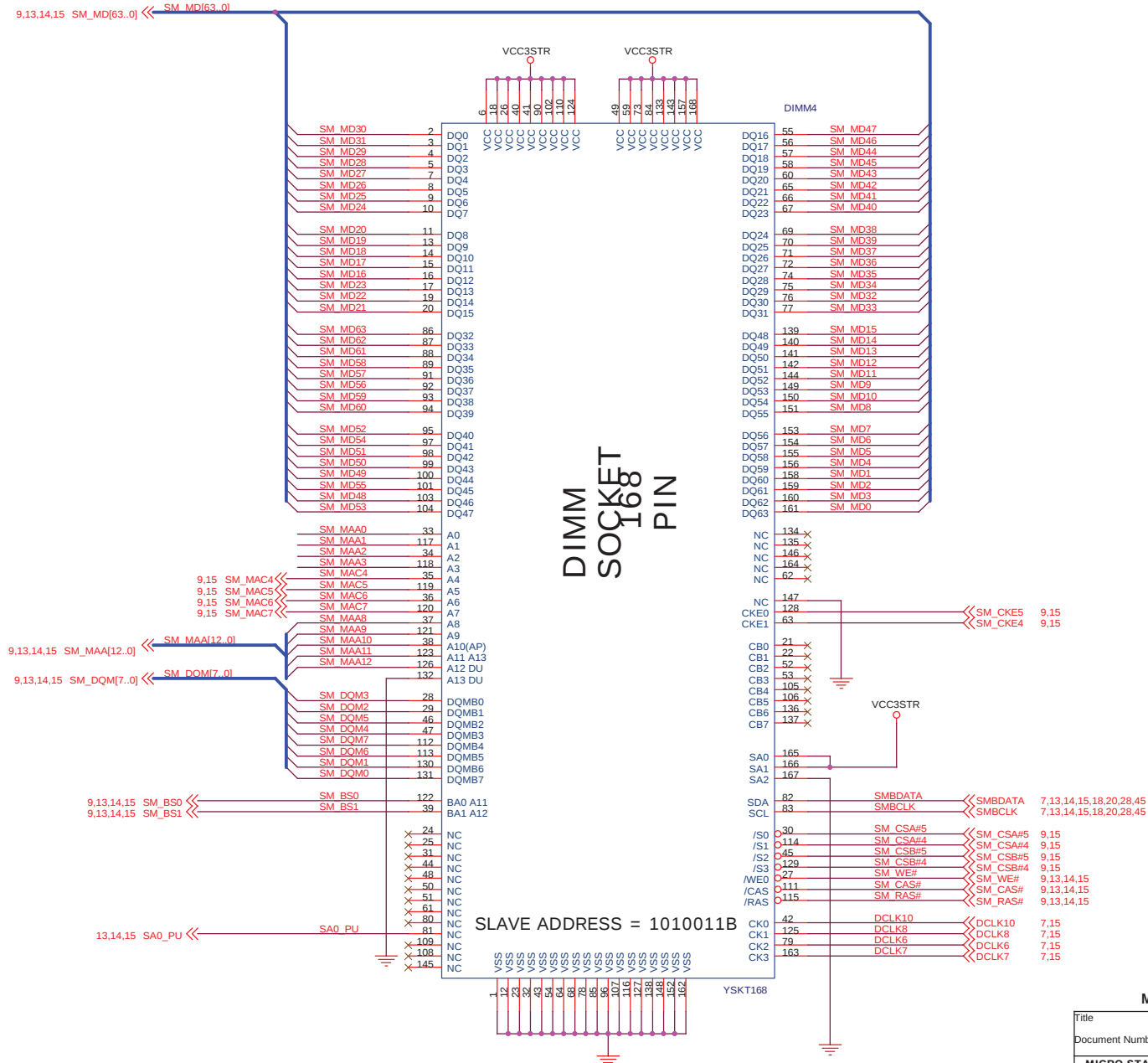
SYSTEM MEMORY



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Title	System Memory : DIMM 3	Rev
Document Number	MS-6337	30B
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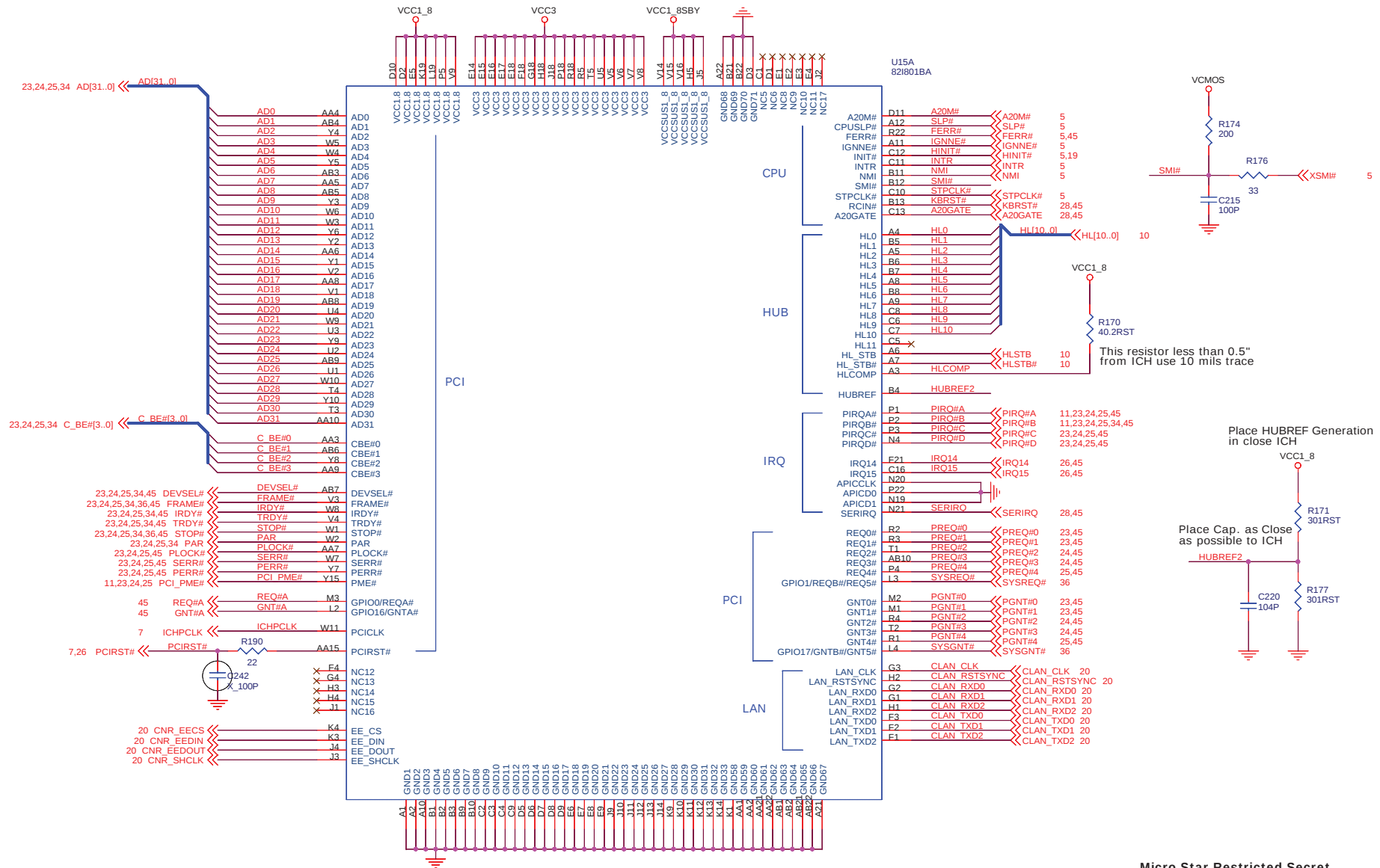
SYSTEM MEMORY



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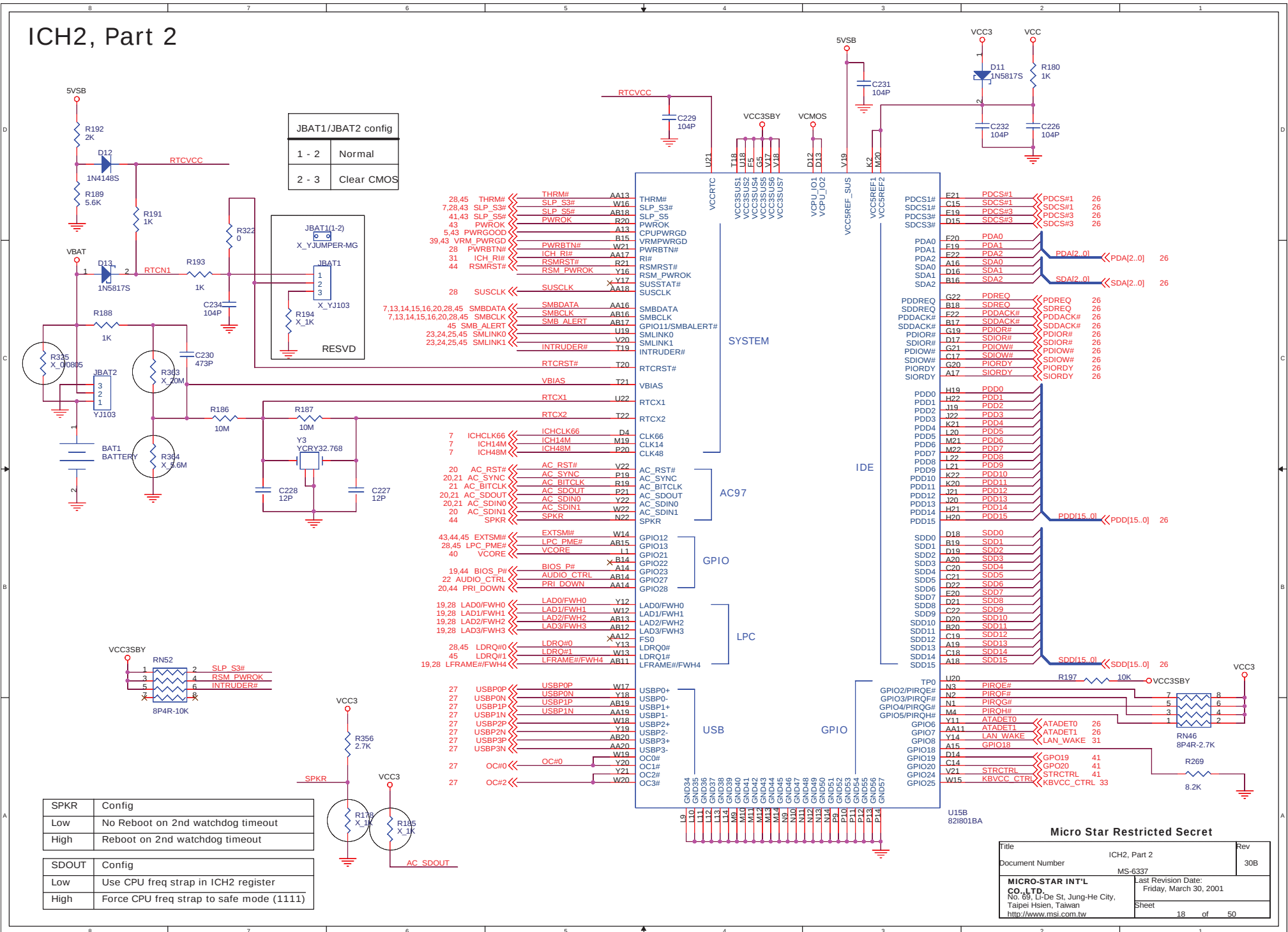
ICH2, Part 1



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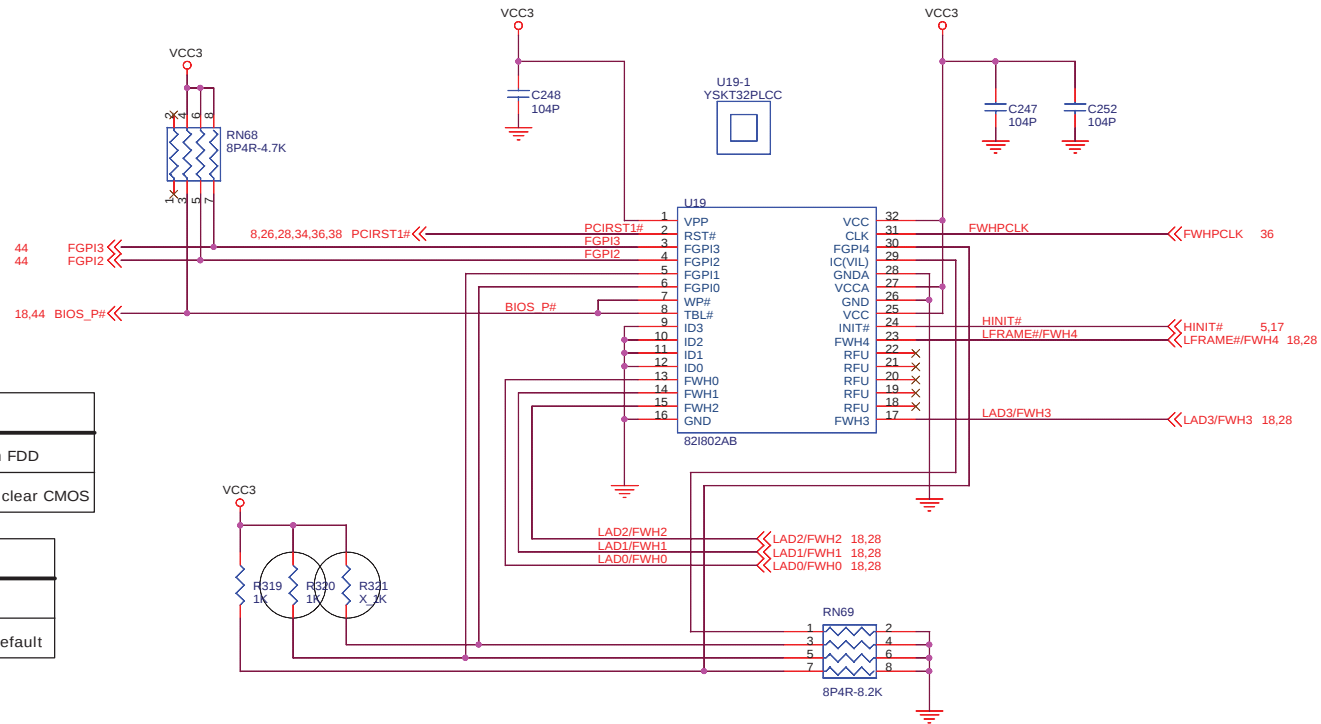
ICH2, Part 2



Firware Hub (FWH)

GPI2	GPI3	Config.
LOW	HIGH	Flash from FDD
HIGH	LOW	Boot auto clear CMOS

BIOS Update Config.		
HIGH	Un_protected	
LOW	Protected	Default



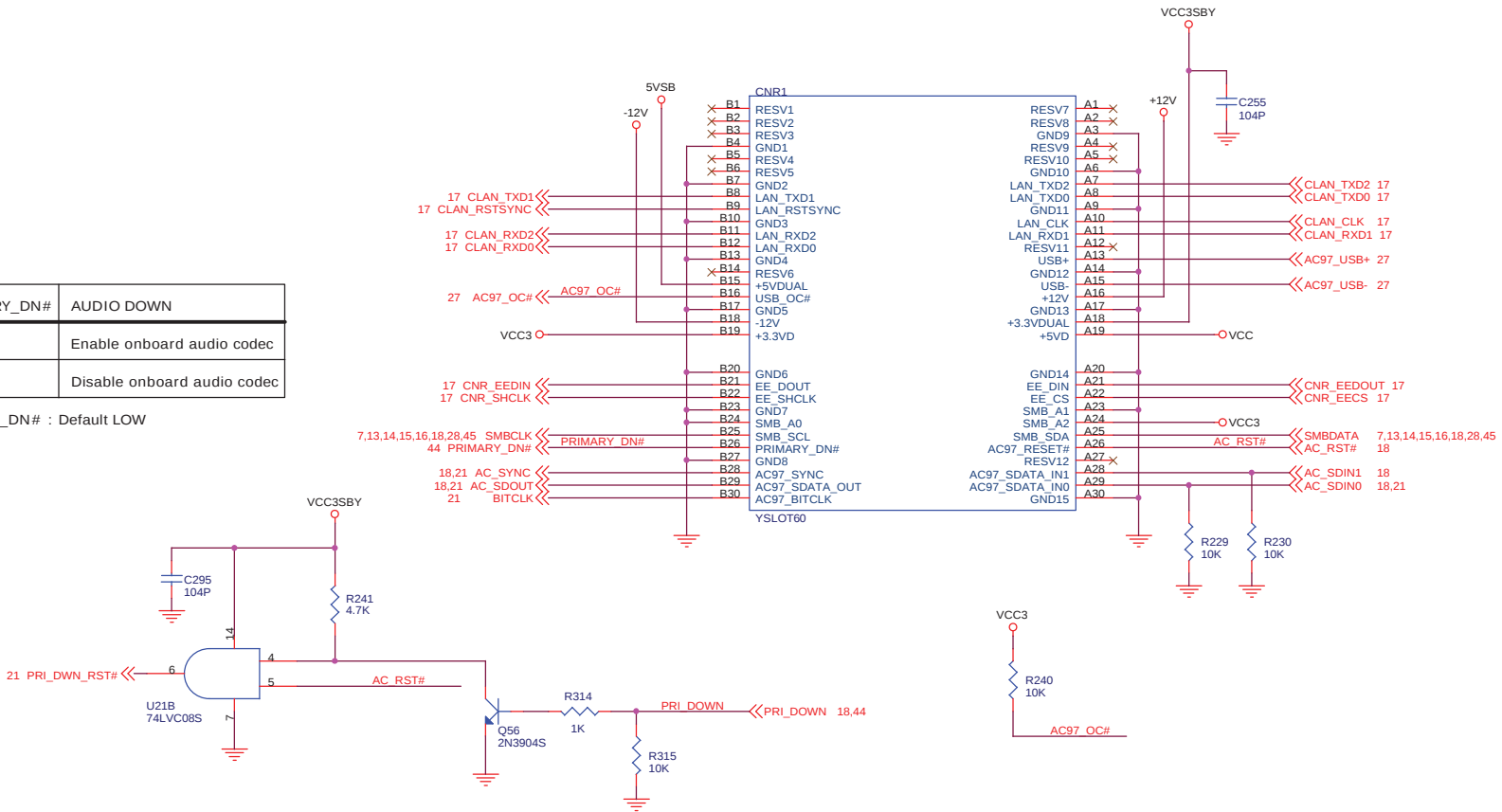
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Title	FIRWARE HUB (FWH)	Rev
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Comm. Networking Riser

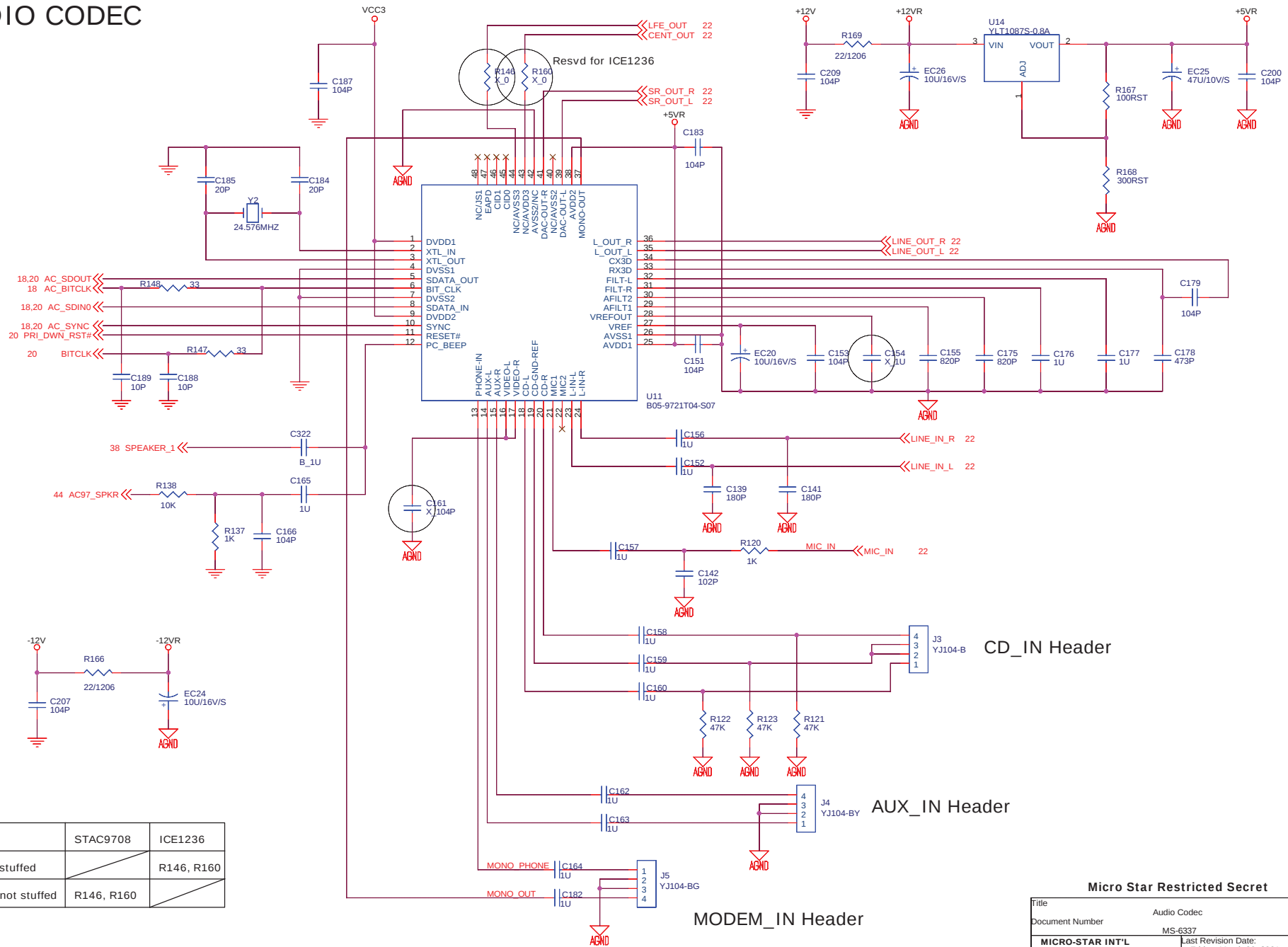
PRIMARY_DN#	AUDIO DOWN
LOW	Enable onboard audio codec
HIGH	Disable onboard audio codec

PRIMARY_DN# : Default LOW



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Title	Communication Networking Riser	Rev
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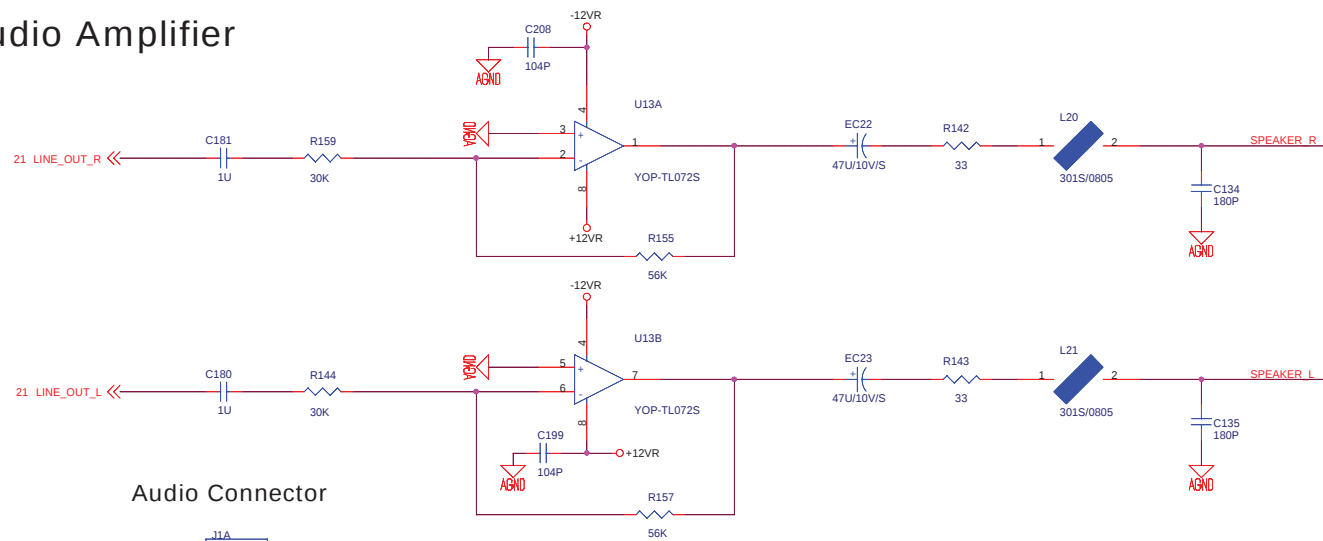
AUDIO CODEC



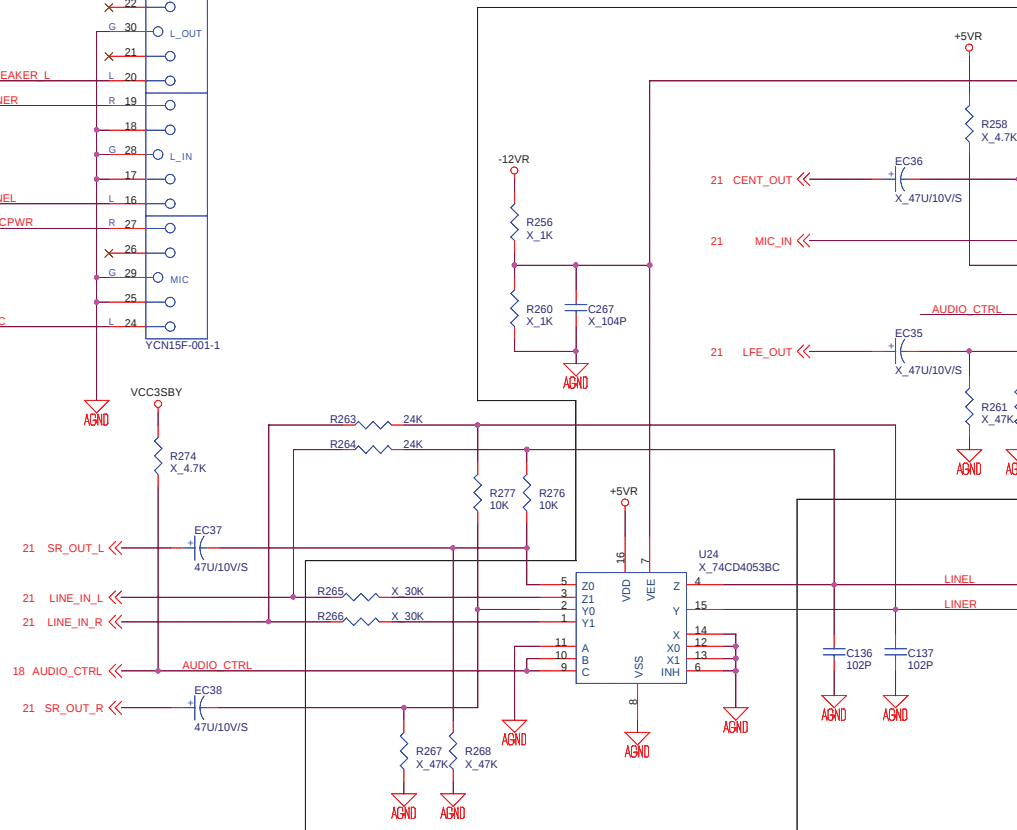
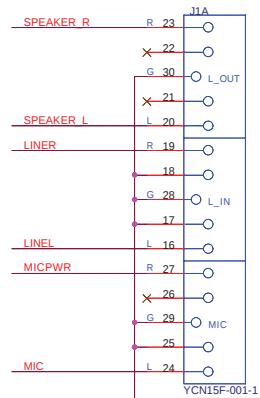
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stuffed		R146, R160
not stuffed	R146, R160	

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Title	Audio Codec	Rev
Document Number	MS-6337	30B
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Audio Amplifier



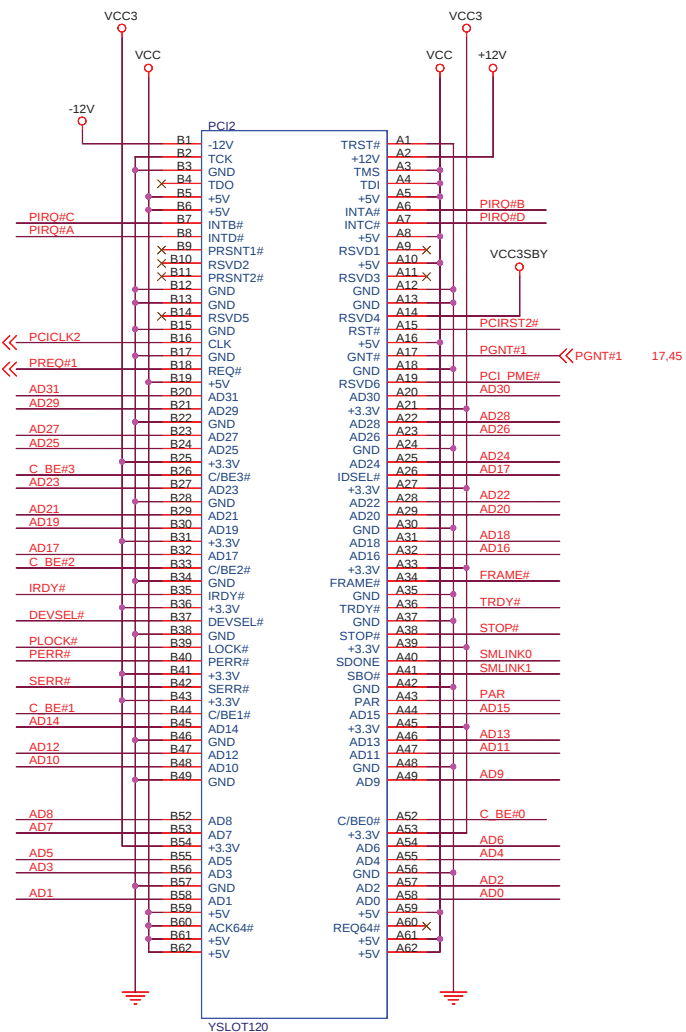
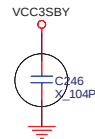
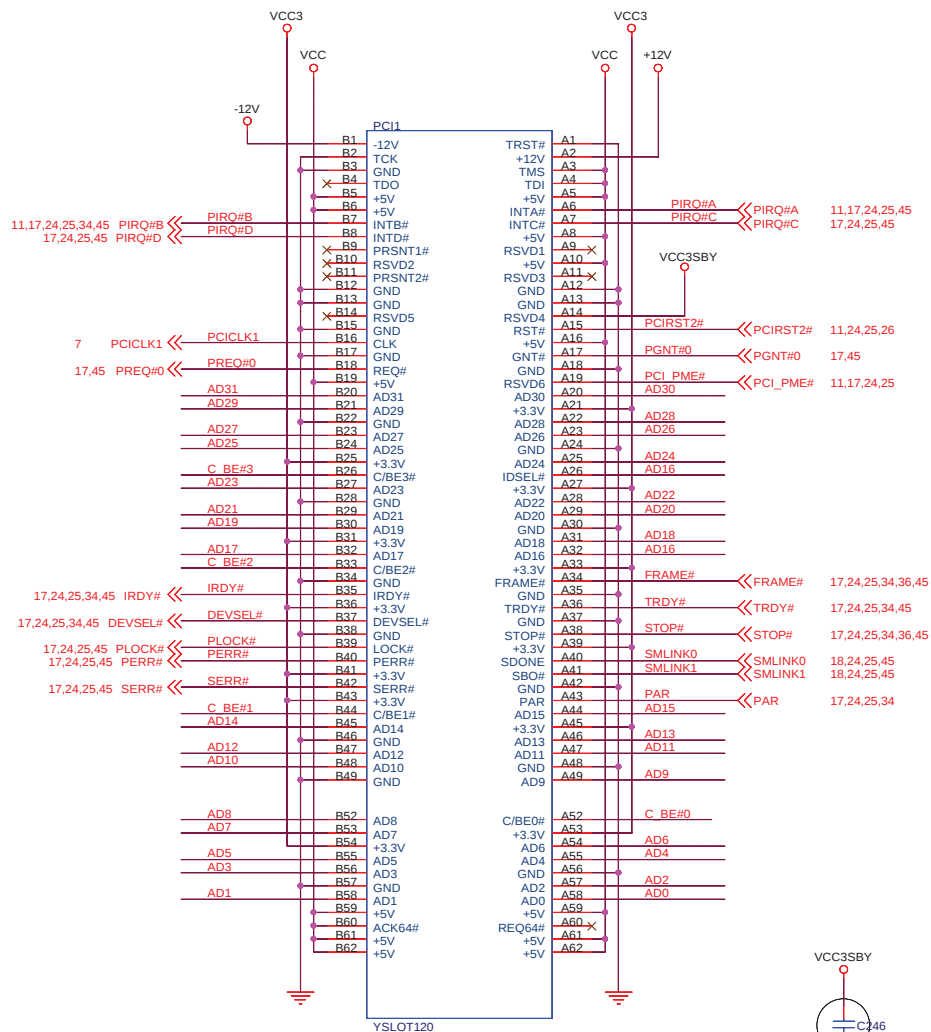
Audio Connector



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Title	Audio Amplifier	Rev
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PCI Connectors

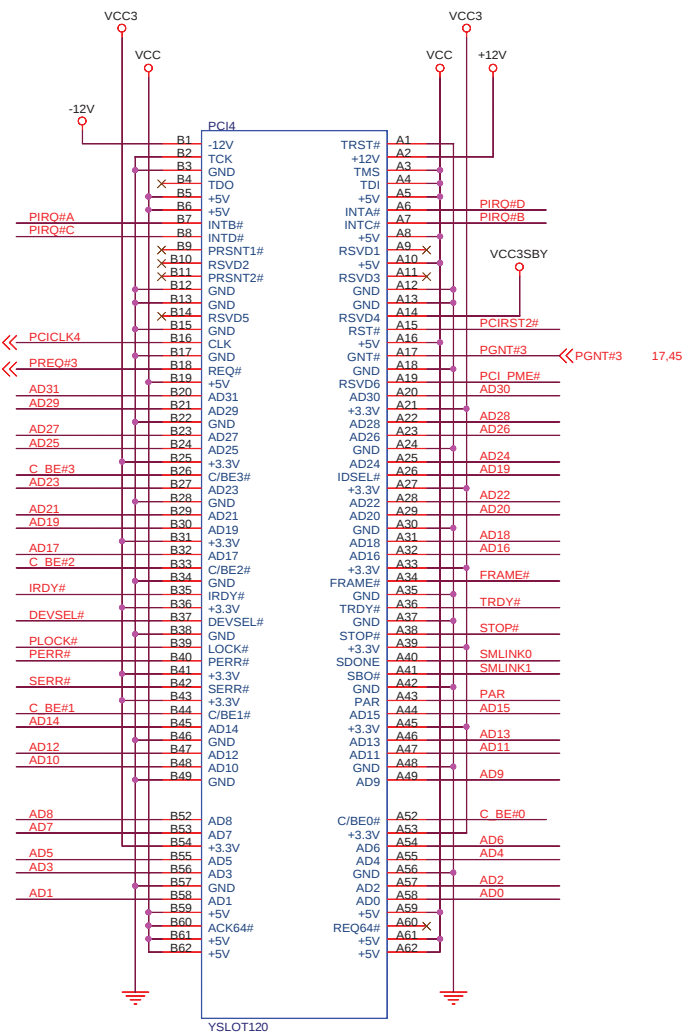
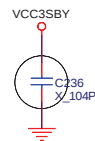
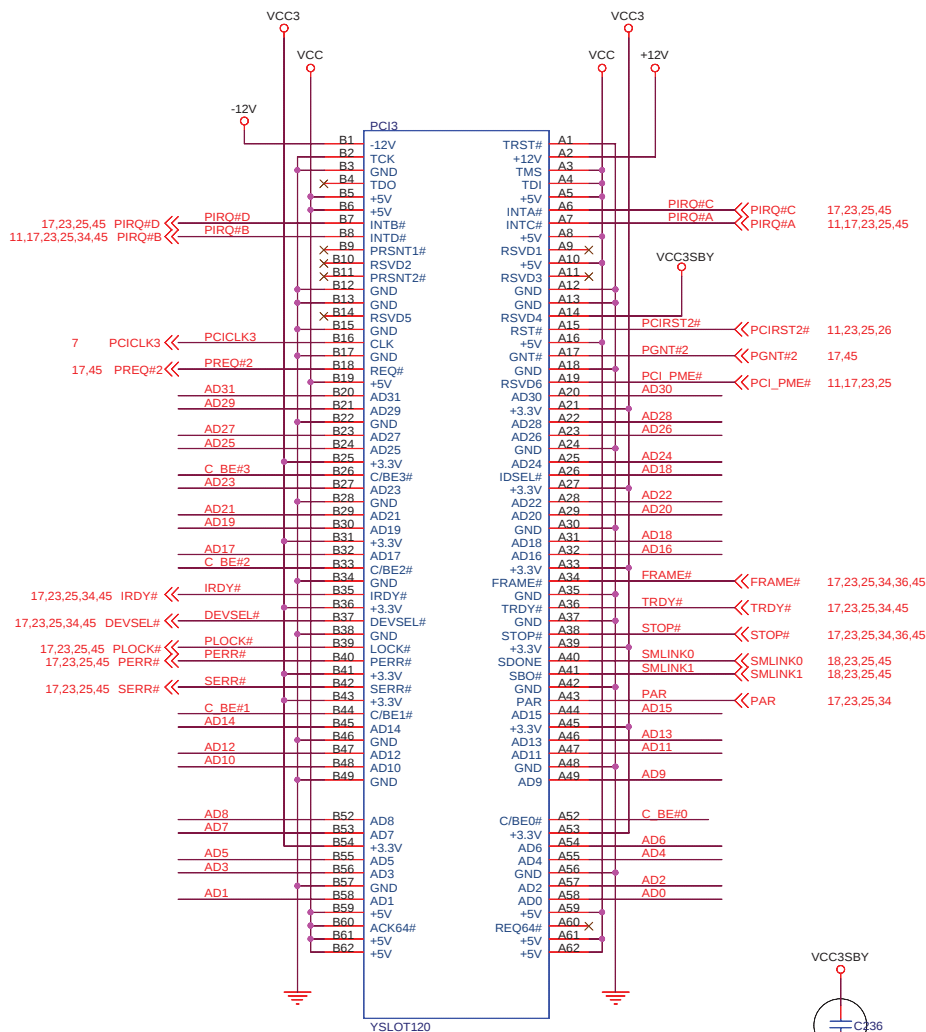


17,24,25,34 AD[31..0] << AD[31..0]
17,24,25,34 C_BE#[3..0] << C_BE#[3..0]

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PCI Connectors

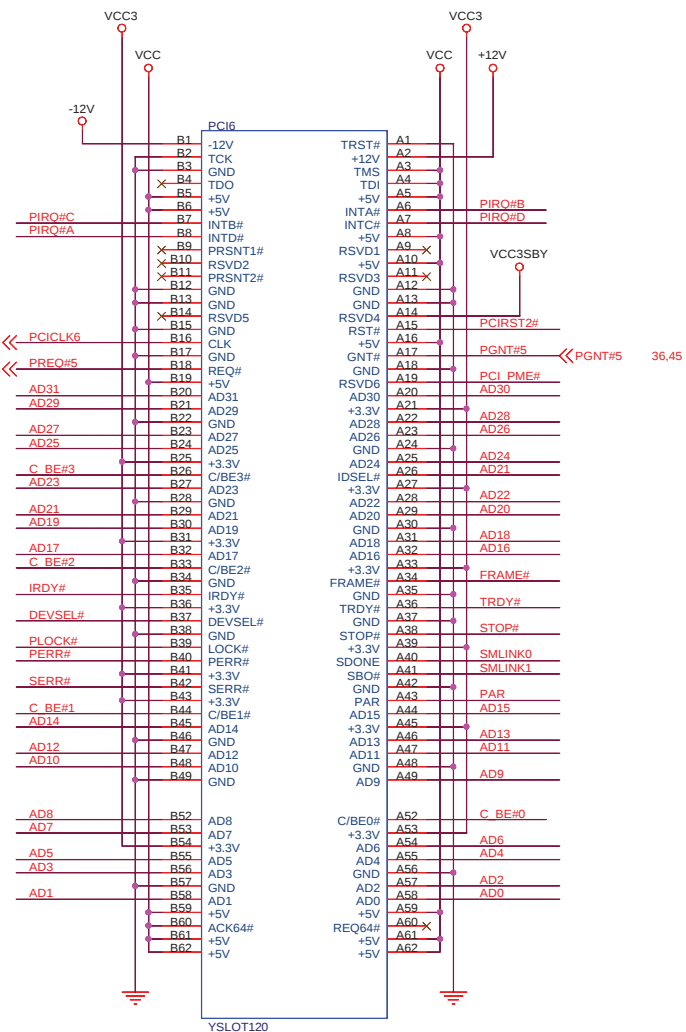
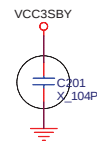
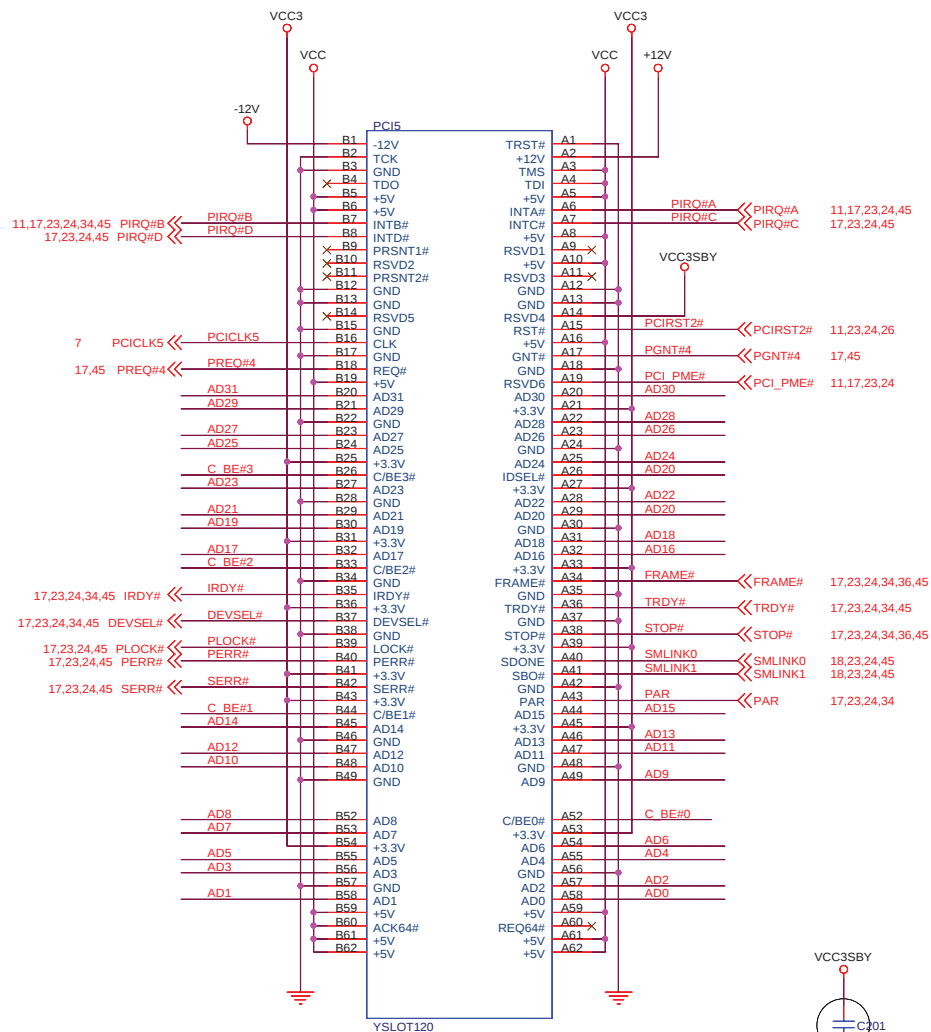


17,23,25,34 AD[31..0] << AD[31..0]
17,23,25,34 C_BE#[3..0] << C_BE#[3..0]

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PCI Connectors



17,23,24,34 AD[31..0] << AD[31..0]
17,23,24,34 C_BE#[3..0] << C_BE#[3..0]

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Title	PCI Connector 5 & 6	Rev
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[illegible][illegible]

ATA100 IDE CONNECTORS

D

C

B

A

PRIMARY IDE CONN.

SECONDARY IDE CONN.

IDEACTP#

IDEACTS#

HLED

HDDRST#

PCIRST#

PCIRST1#

PCIRST2#

SDA[2..0]

SDB[2..0]

PDA[2..0]

PDB[2..0]

IDE1

IDE2

YJ220-CB-1

YJ220-CW-1

U21D 74LVC08S

U17A 74LVC07S

U17C 74LVC07S

U17F 74LVC07S

U17B 74LVC07S

RN59 8P4R-1K

Q283 10P

Q282 10P

Micro Star Restricted Secret

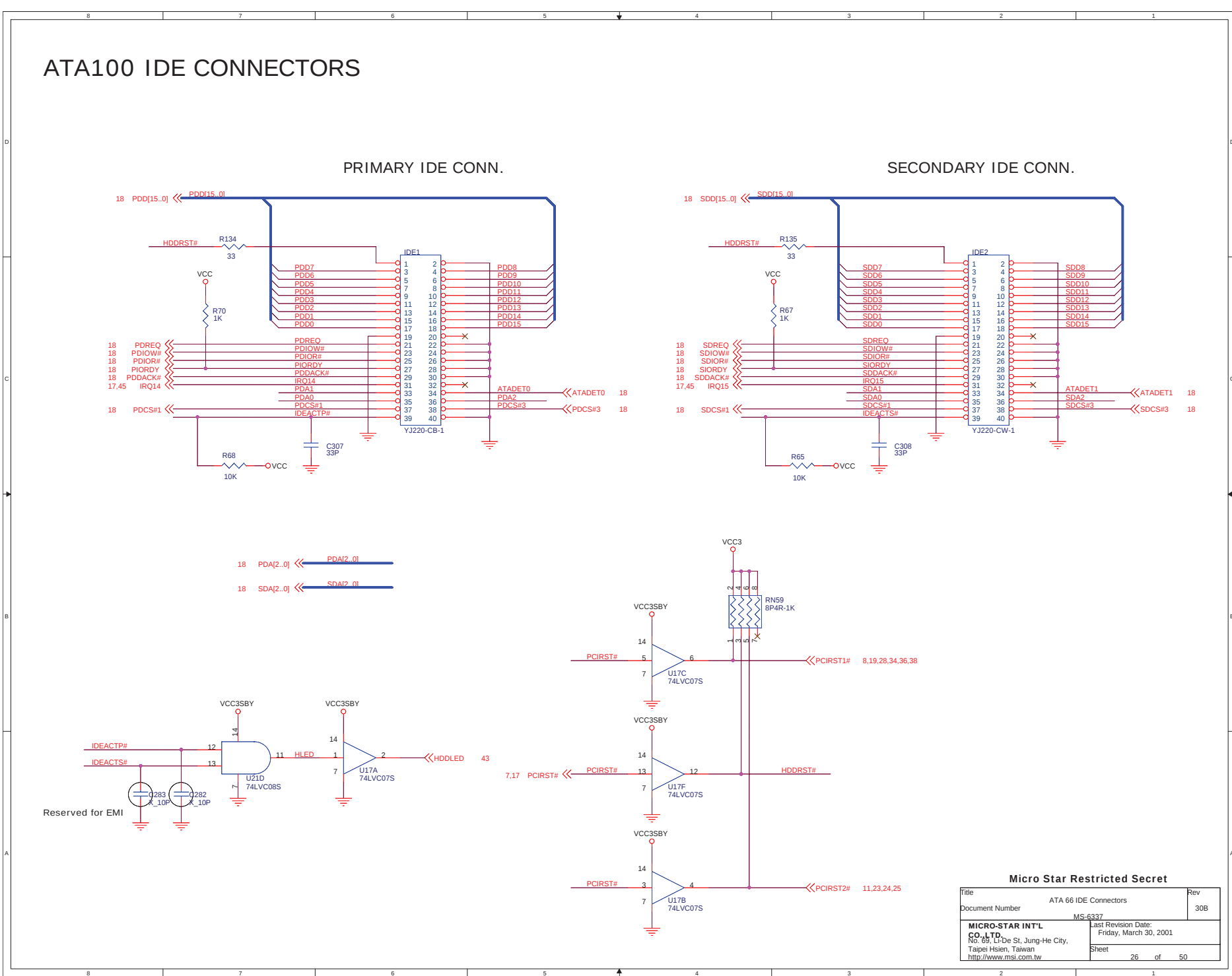
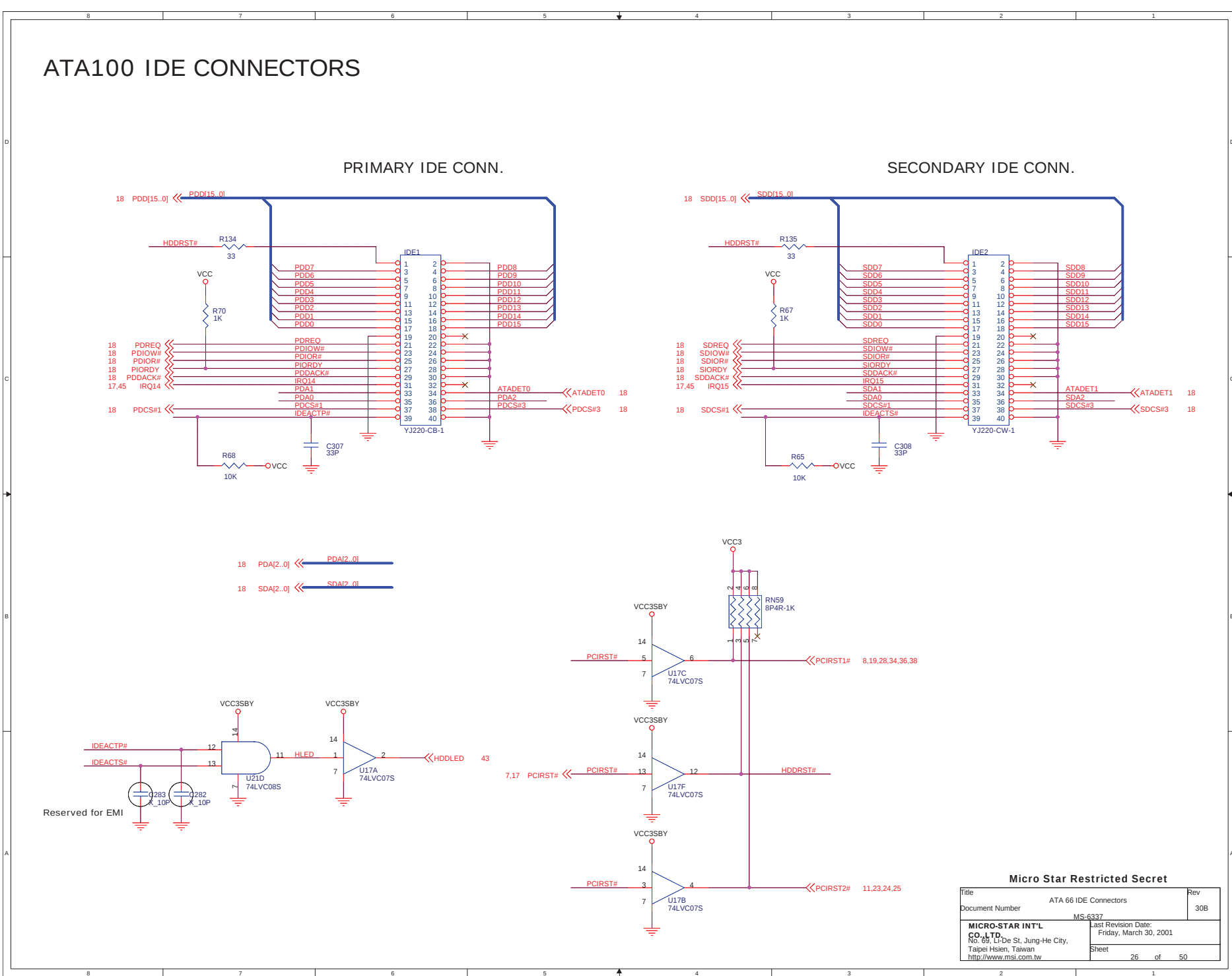
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Document Number MS-6337

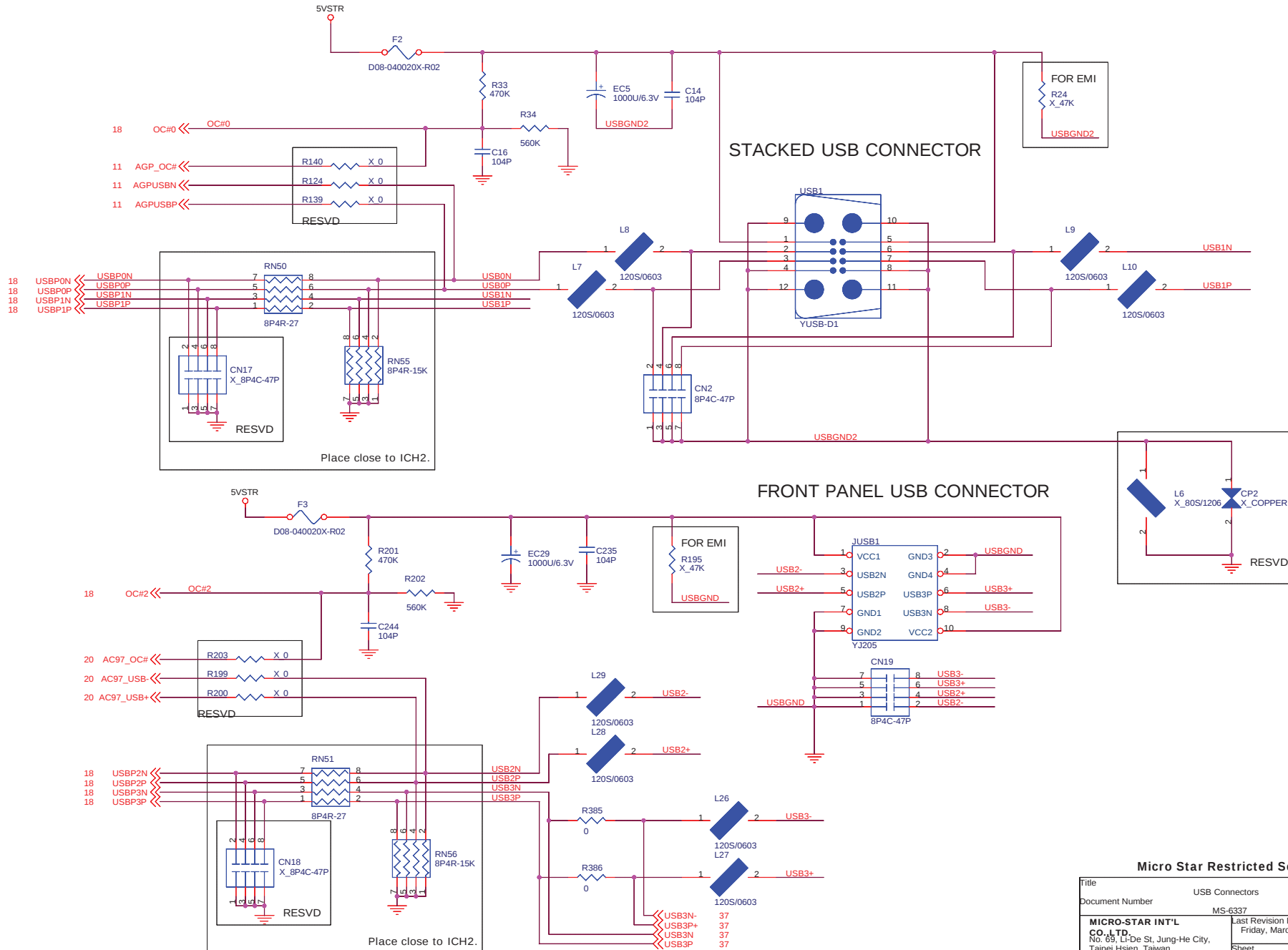
MICRO-STAR INT'L CO., LTD.
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Taipei Hsien, Taiwan
<http://www.msi.com.tw>

Last Revision Date:
Friday, March 30, 2001

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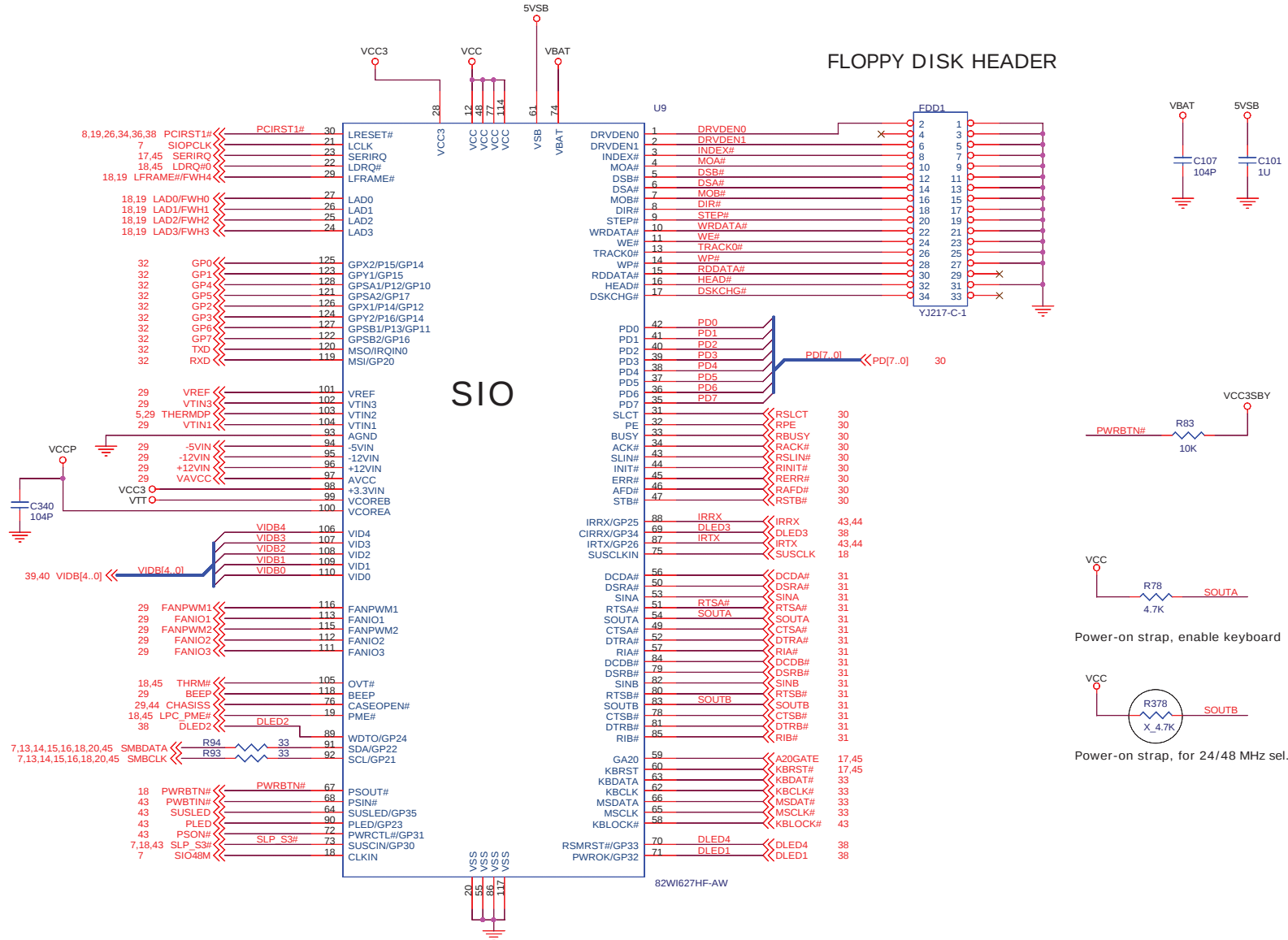
USB Connectors



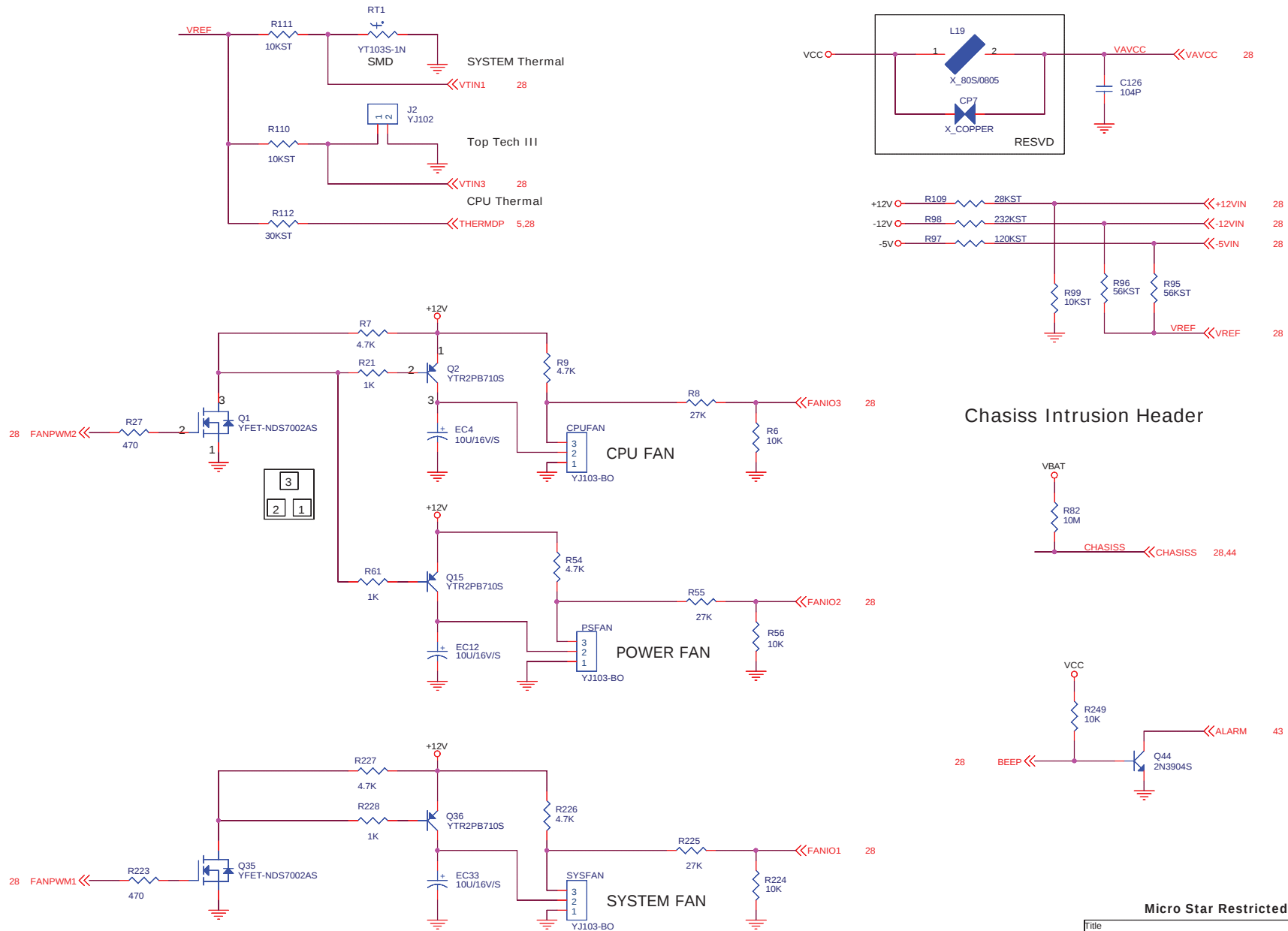
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Title	USB Connectors	Rev
Document Number	MS-6337	30B
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Super I/O

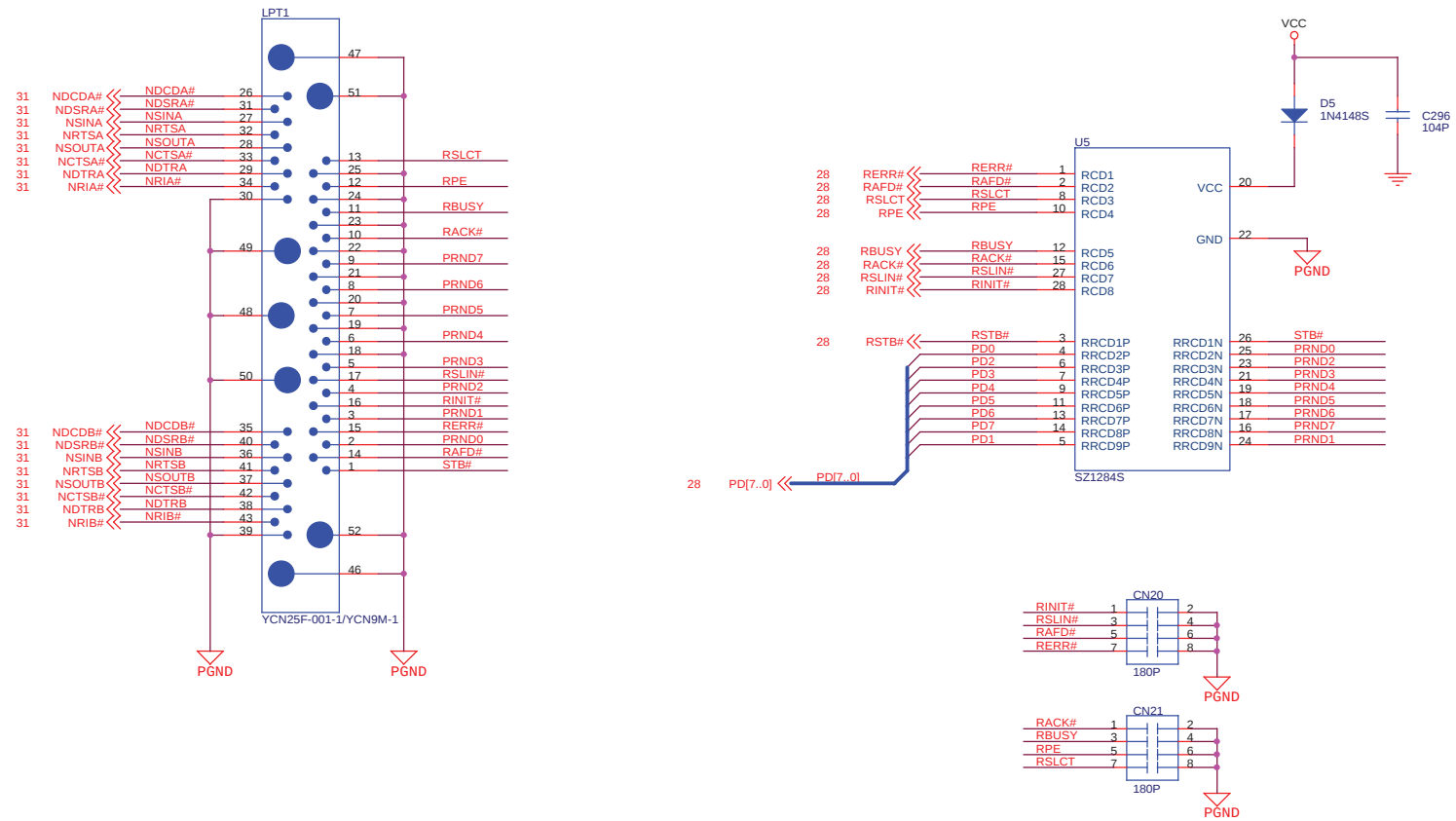


Hardware Monitor

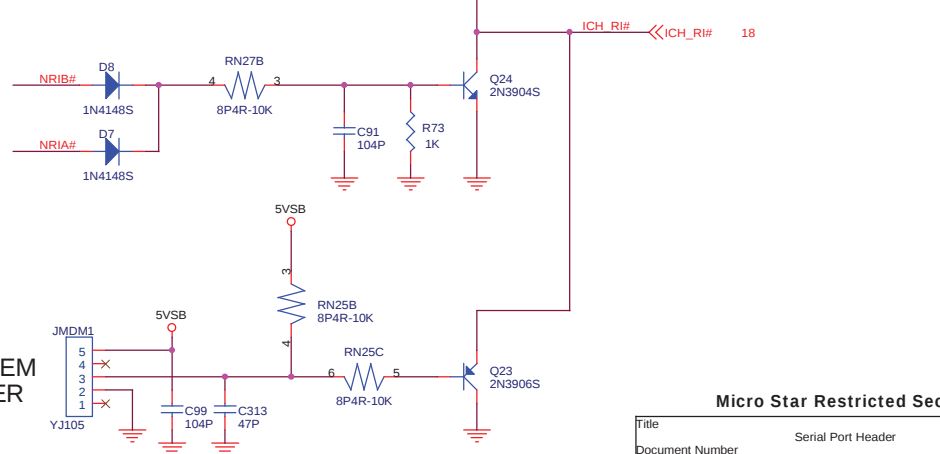
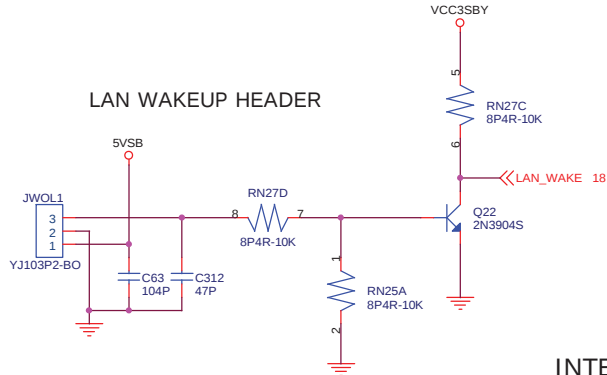
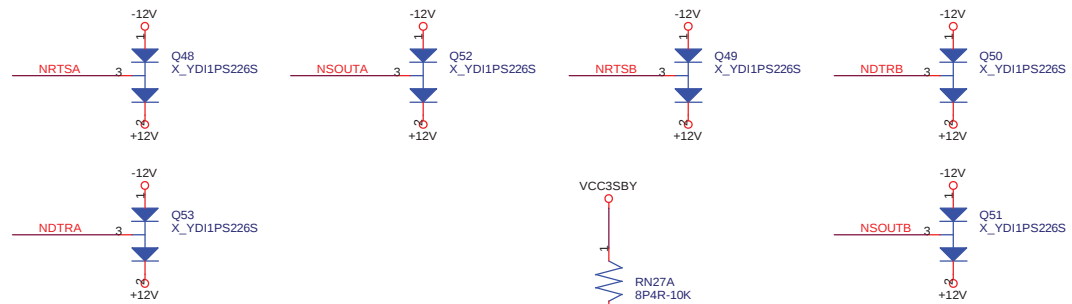
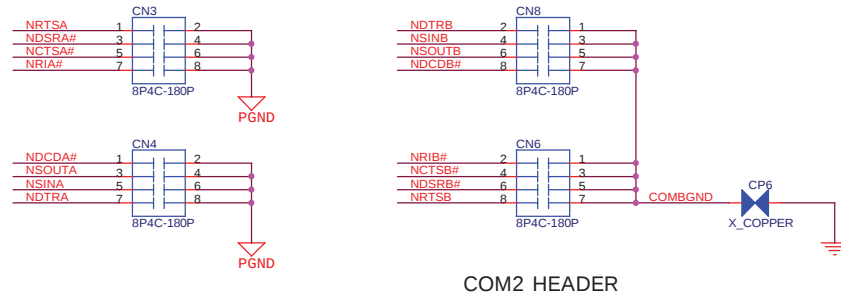
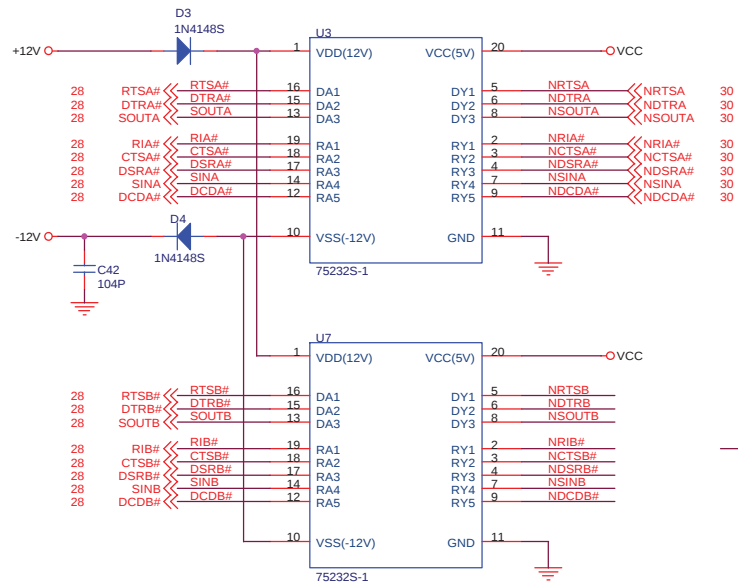


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Document Number	MS-6337	30B
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Parallel Port Header

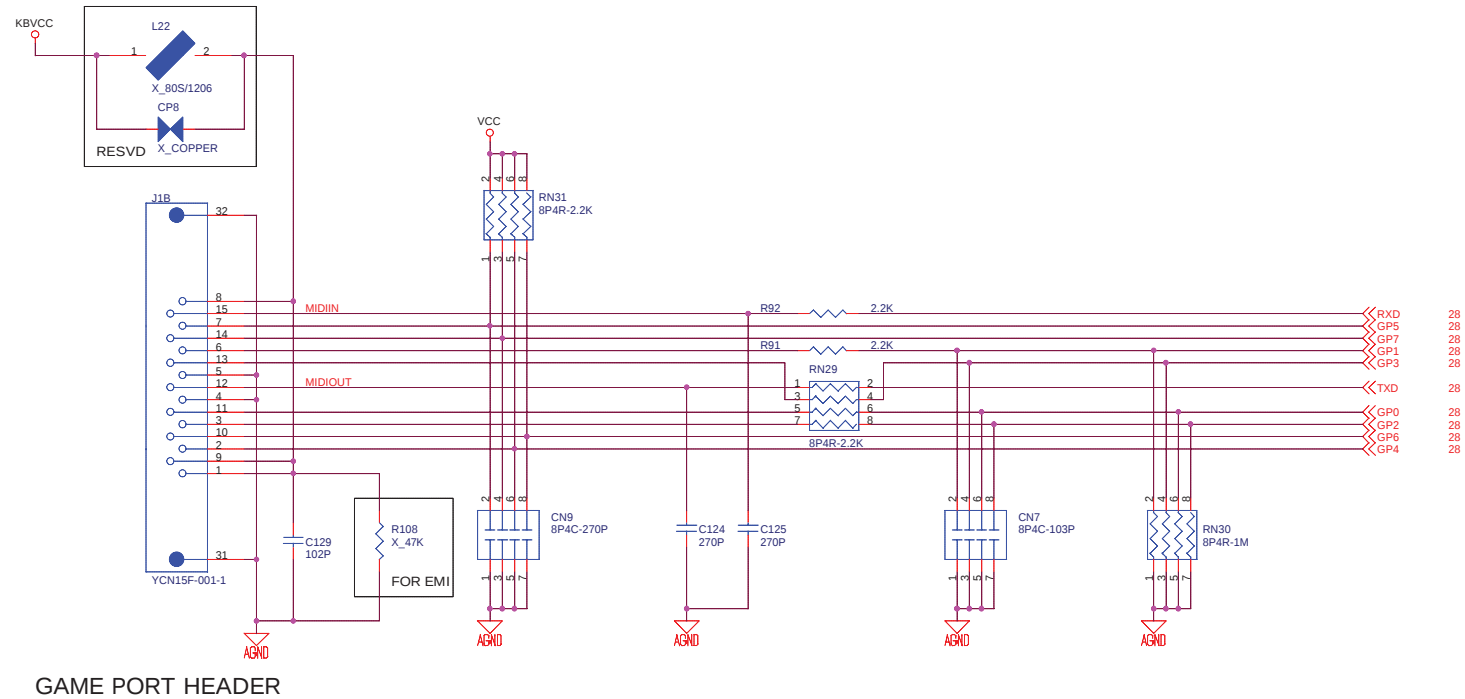


Serial Port/COM Headers



Micro Star Restricted Secret		
Title	Serial Port Header	Rev
Document Number	MS-6337	30B
MICRO-STAR INT'L CO., LTD. No. 89, Li-De St. Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Friday, March 30, 2001 Sheet 31 of 50

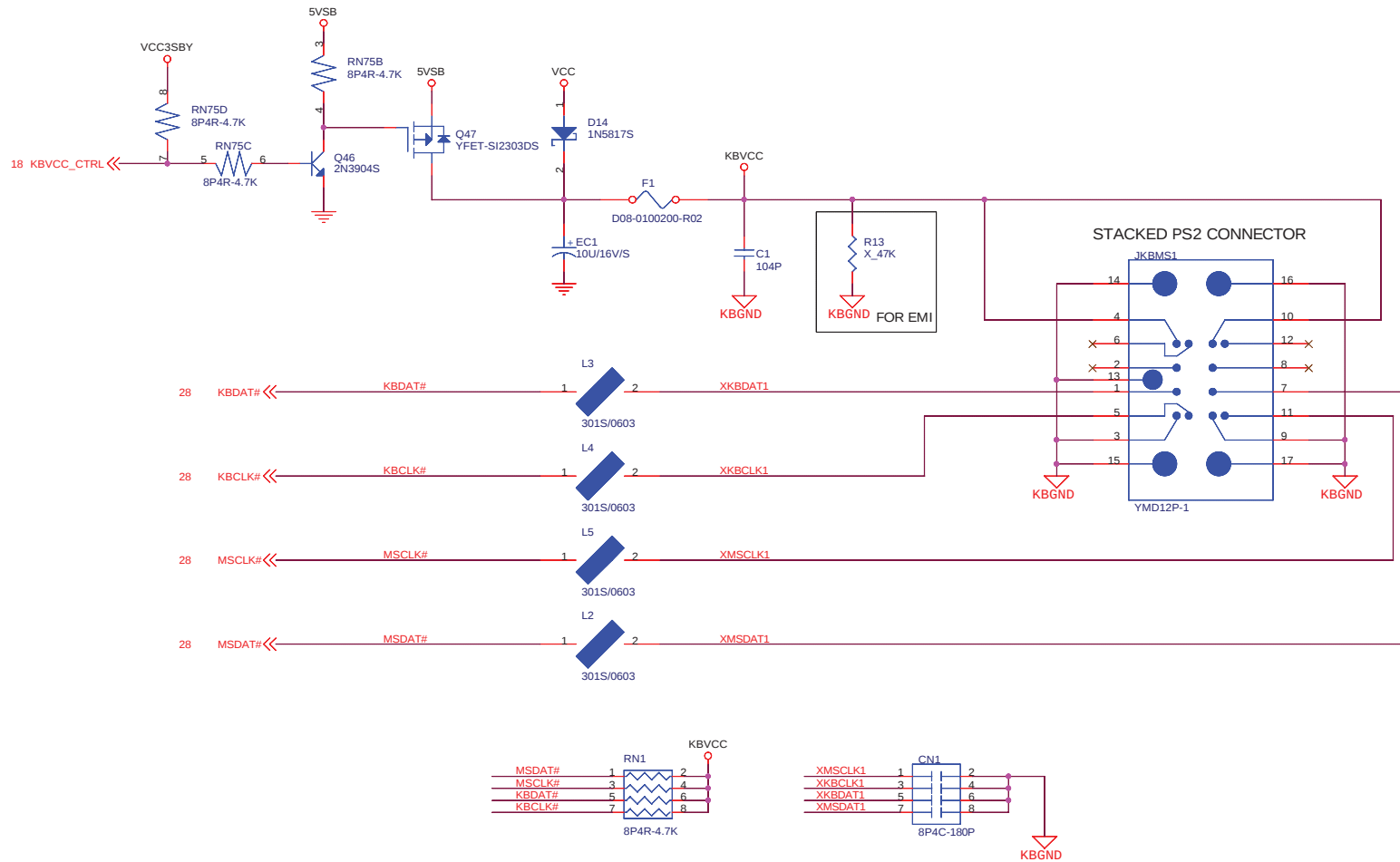
Game Port



Micro Star Restricted Secret

Title	Game Port Header	Rev
Document Number	MS-6337	30B
MICRO-STAR INT'L CO., LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Friday, March 30, 2001
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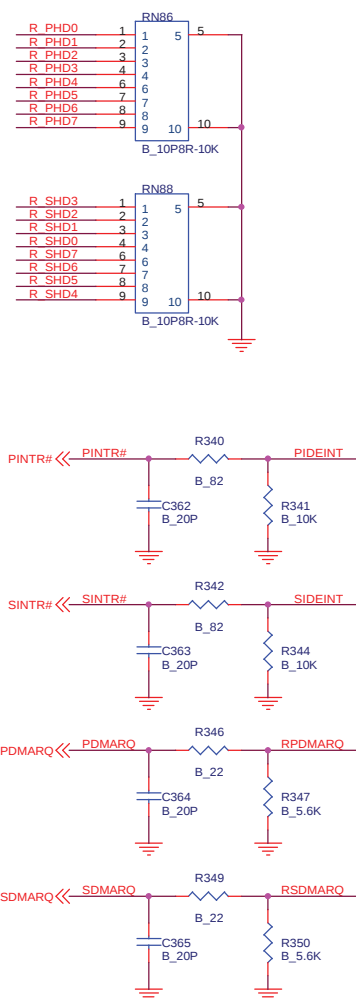
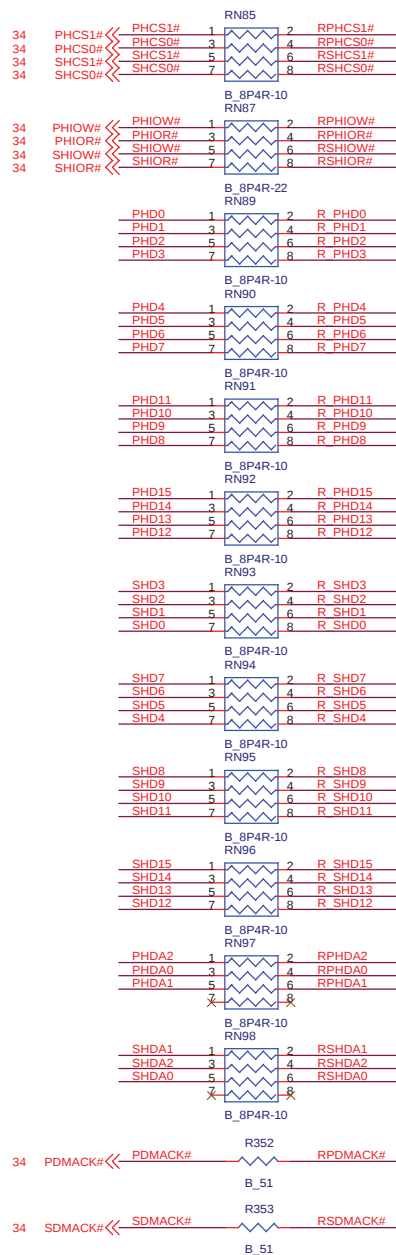
Keyboard/Mouse Ports



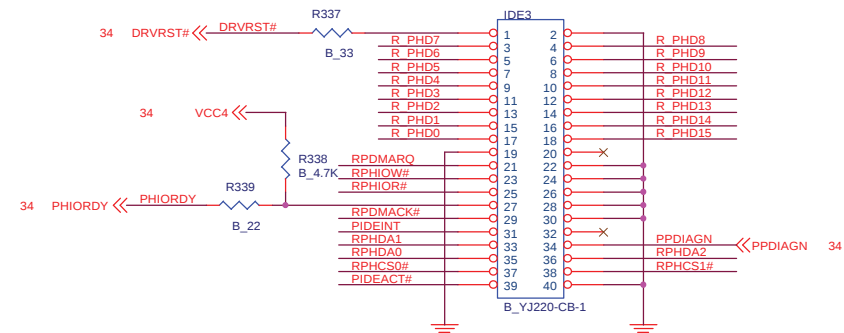
Micro Star Restricted Secret

Title	Keyboard/Mouse Ports	Rev
Document Number	MS-6337	30B
MICRO-STAR INT'L CO., LTD. No. 89, Li-De St. Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Friday, March 30, 2001 Sheet 33 of 50

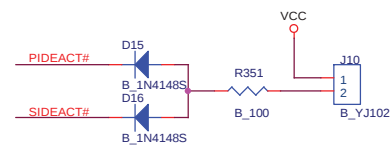
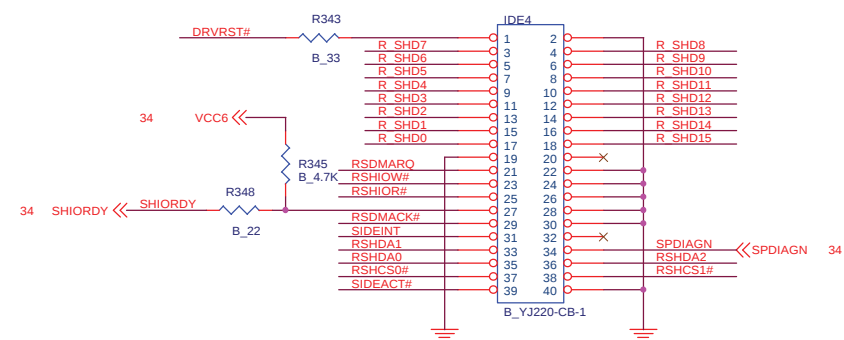
PCI Ultra 100 Connectors



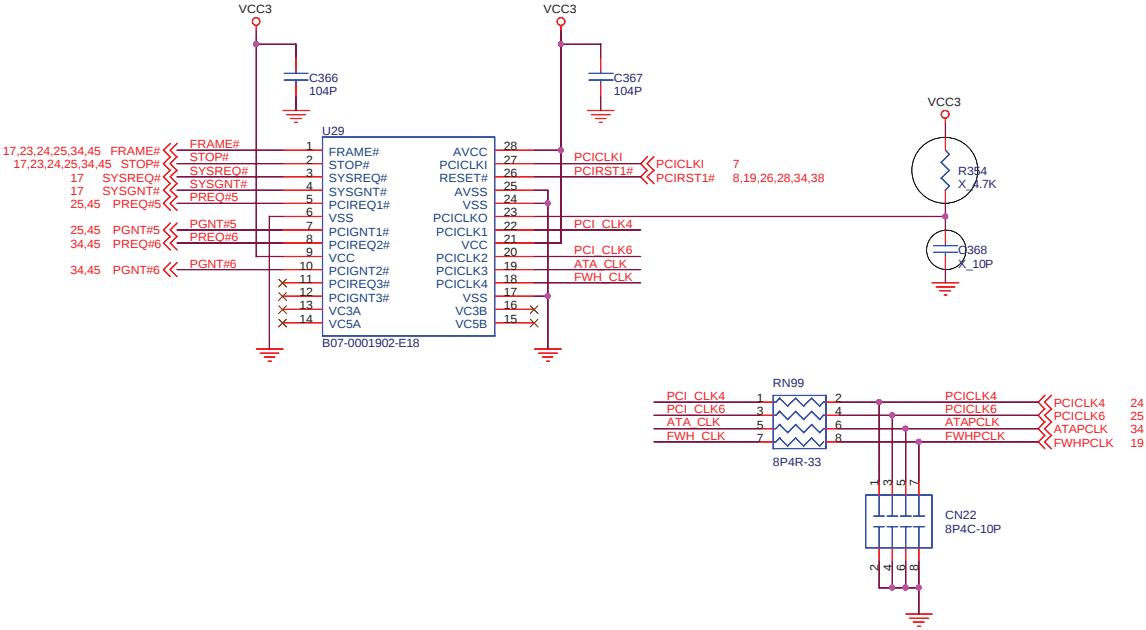
THIRDLY IDE CONN.



FOURTHLY IDE CONN.



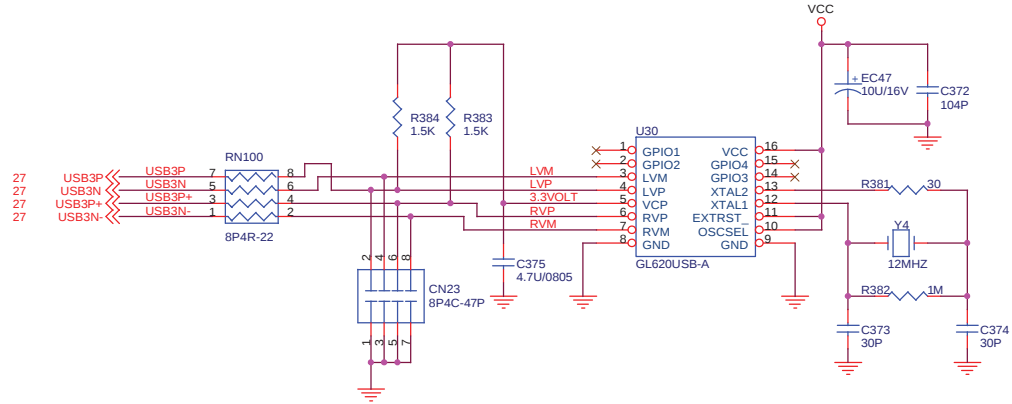
PLL and PCI Arbitor



Micro Star Restricted Secret

Title	PLL and PCI Arbitor	Rev
Document Number	MS-6337	30B
MICRO-STAR INT'L CO., LTD. No. 89, Li-De St. Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Friday, March 30, 2001 Sheet 36 of 50

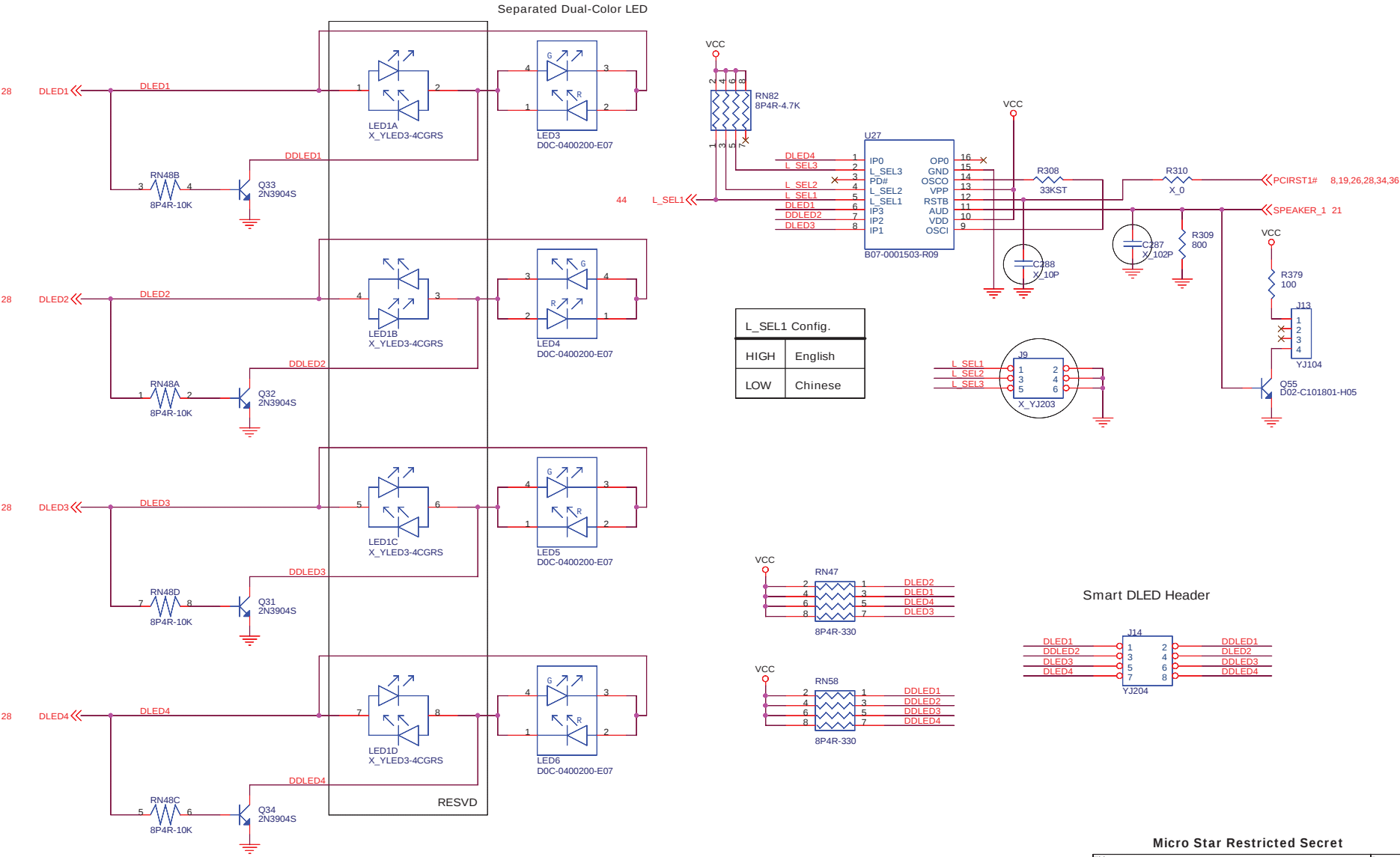
PC to PC Networking Controller



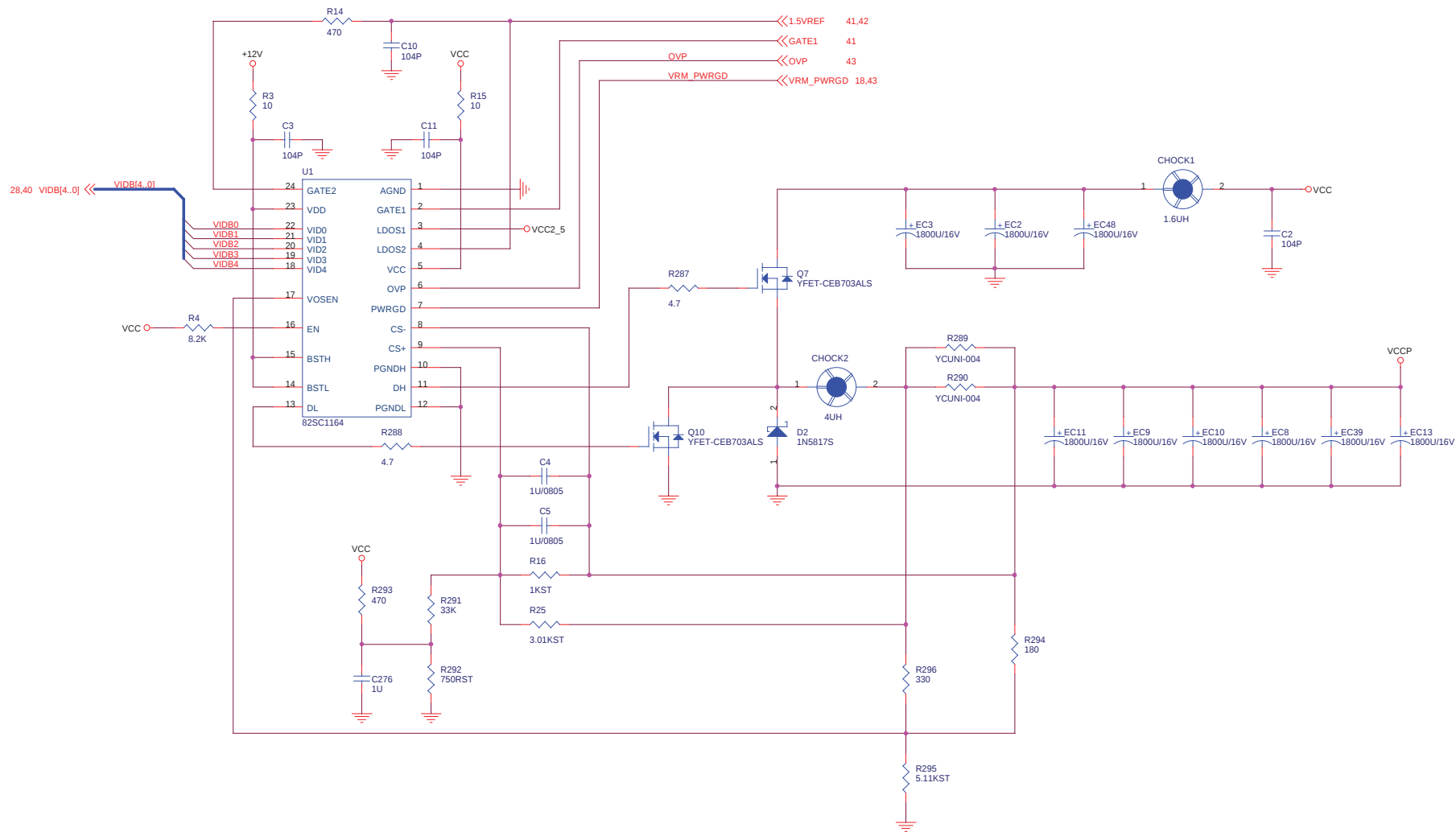
Micro Star Restricted Secret

Title	PC to PC Networking Controller	Rev
Document Number	MS-6337	30B
MICRO-STAR INT'L CO., LTD. No. 89, Li-De St. Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Friday, March 30, 2001
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Smart Diagnostic LED



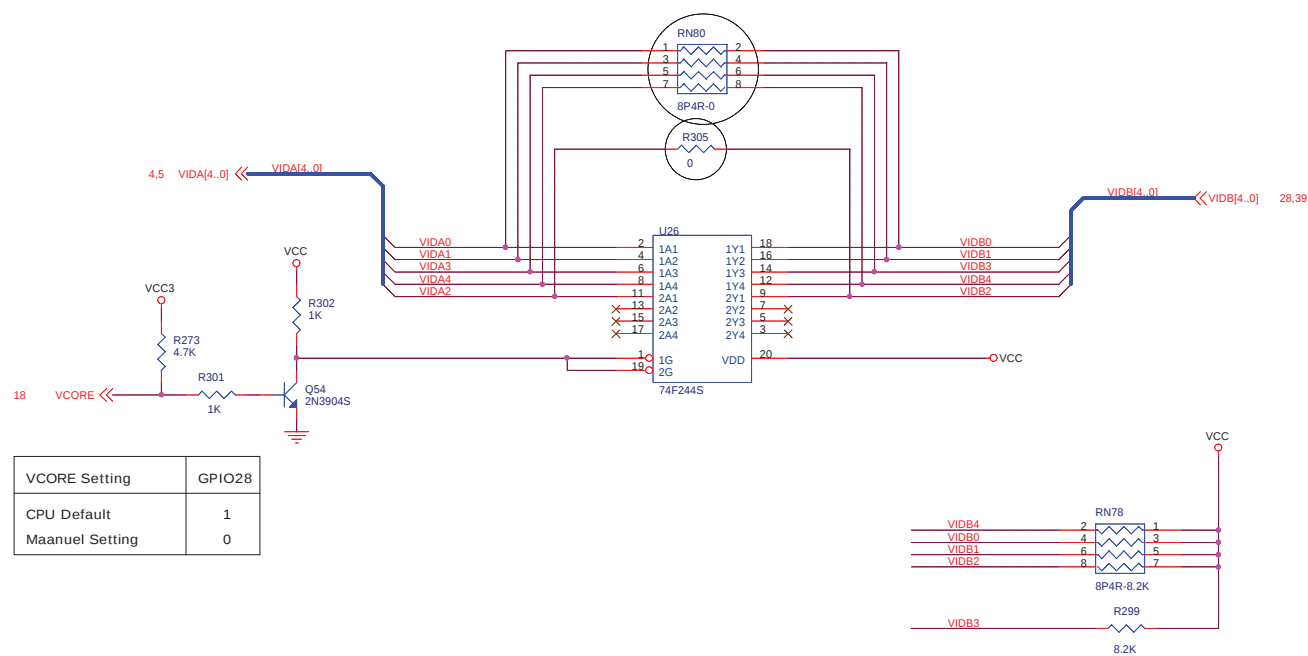
VRM 8.4



Micro Star Restricted Secret

Title	VRM 8.4	Rev
Document Number	MS-6337	30B
MICRO-STAR INT'L		Last Revision Date:
CO., LTD.		Friday, March 30, 2001
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http://www.msi.com.tw		

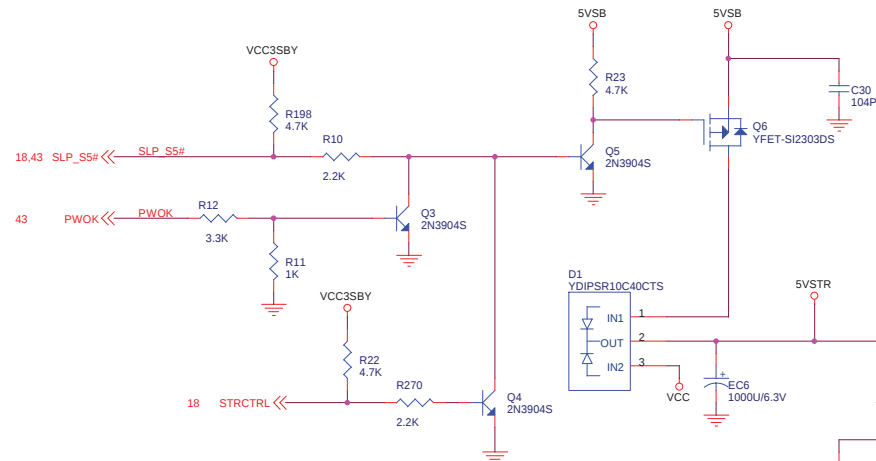
Vcore Setting



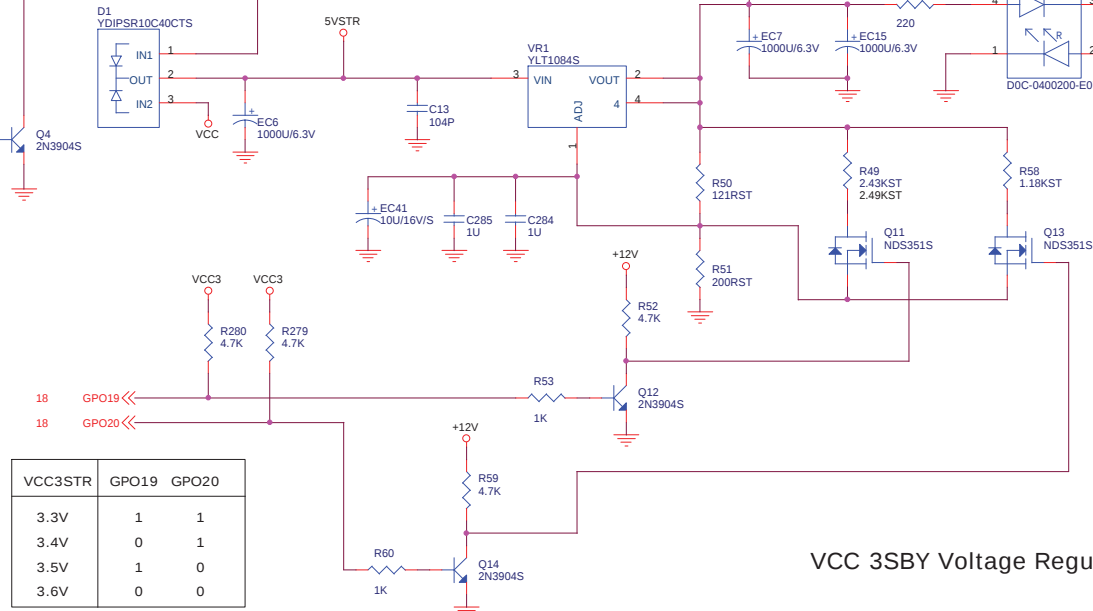
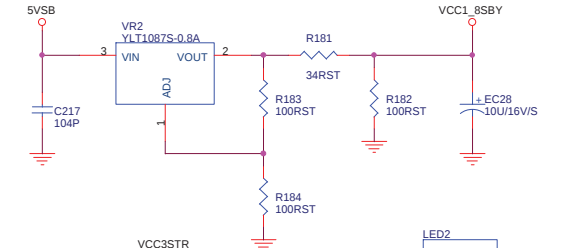
Micro Star Restricted Secret

Title	Vcore Setting	Rev
Document Number	MS-6337	30B
MICRO-STAR INT'L CO., LTD. No. 68, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Friday, March 30, 2001
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Voltage Regulators

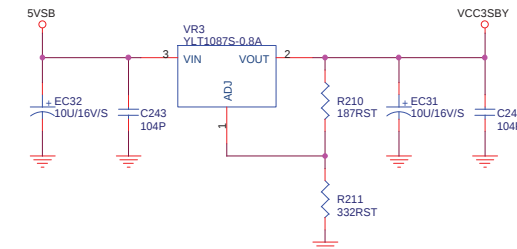


VCC 1.8SBY Voltage Regulator

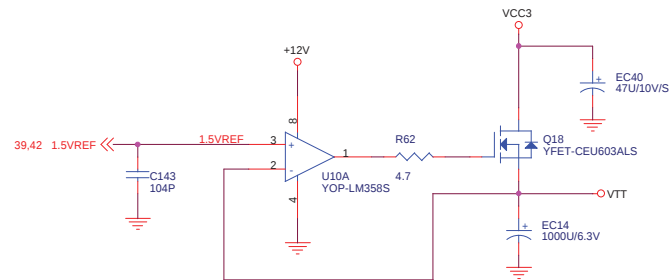


VCC3STR	GPO19	GPO20
3.3V	1	1
3.4V	0	1
3.5V	1	0
3.6V	0	0

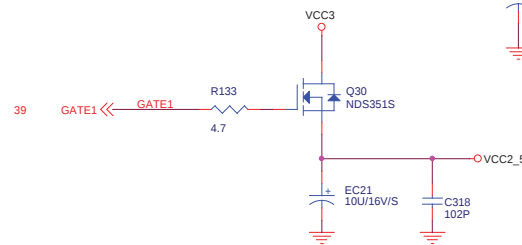
VCC 3SBY Voltage Regulator



VTT 1.5 Voltage Regulator



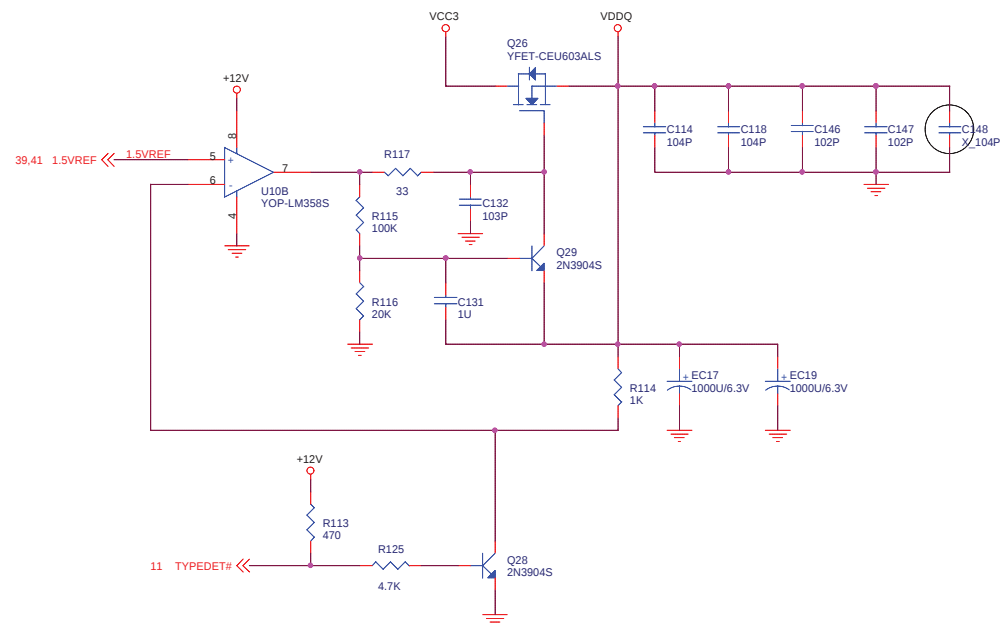
VTT 2.5 Voltage Regulator



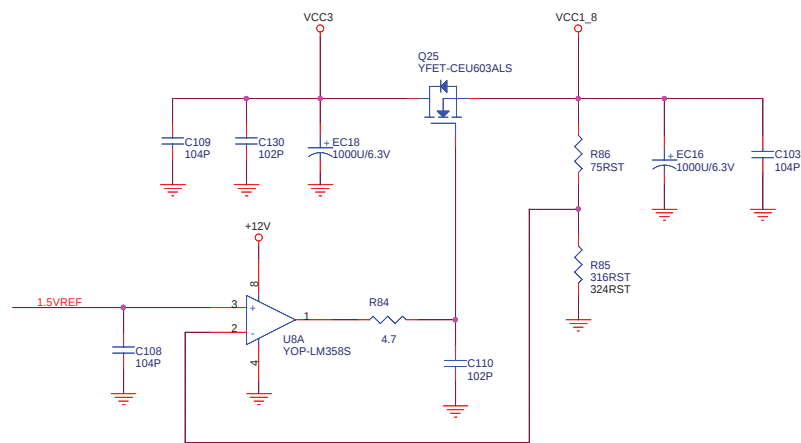
Micro Star Restricted Secret

Title	System Voltage Regulators	Rev
Document Number	MS-6337	30B
MICRO-STAR INT'L CO., LTD. No. 68, L.-De St, Jung-Ho City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Friday, March 30, 2001
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AGP Voltage Regulators



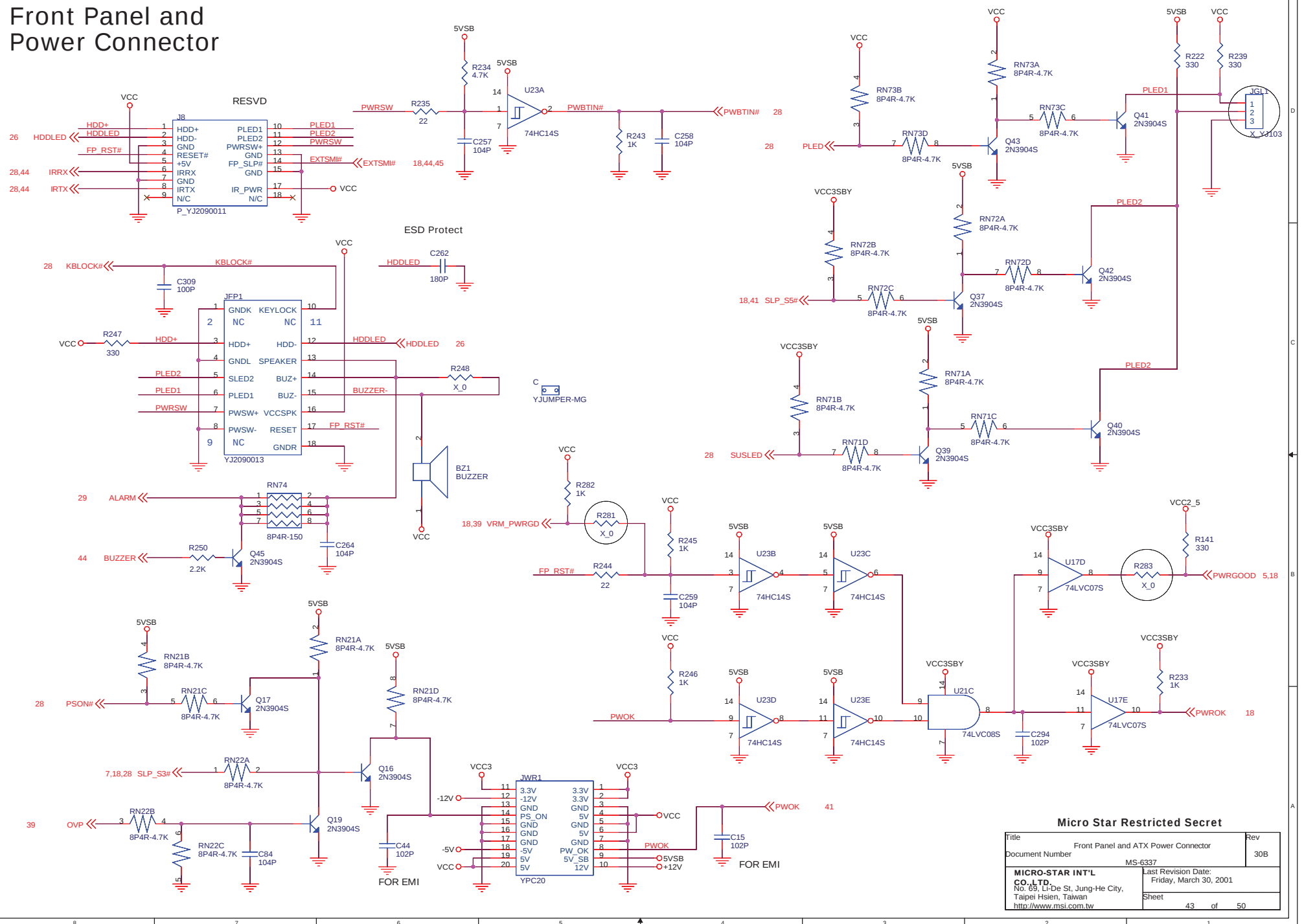
VCC 1.8 Voltage Regulator



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Title	AGP Voltage Regulators	Rev
Document Number	MS-5337	30B
MICRO-STAR INT'L CO., LTD. No. 68, Li-De St, Jung-Ho City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Friday, March 30, 2001
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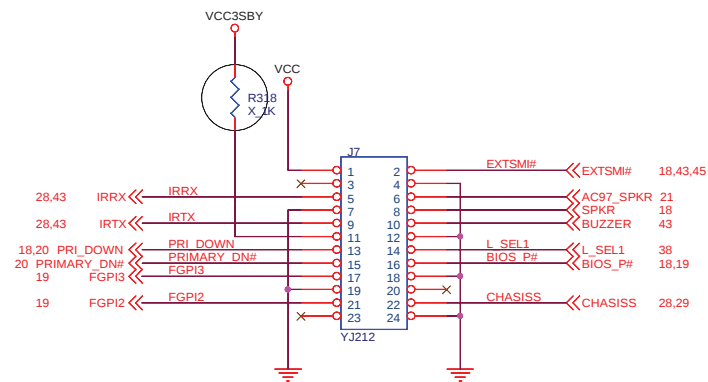
Front Panel and Power Connector



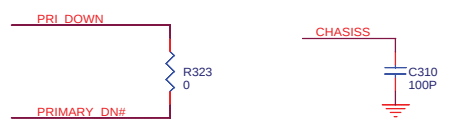
Micro Star Restricted Secret

Title	Front Panel and ATX Power Connector	Rev	
Document Number	MS-6337		30B
MICRO-STAR INT'L CO., LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Friday, March 30, 2001	
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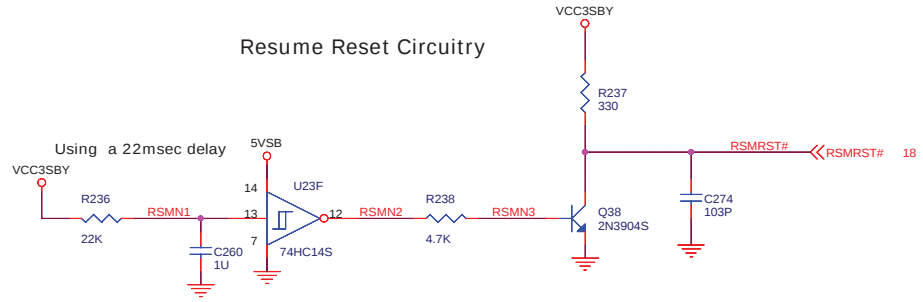
Front Panel



- J7(13-15) For Onboard Codec
- J7(21-23) For FWH GPI
- J7(14) For Smart DLED Language
- J7(16-18) For BIOS Protection



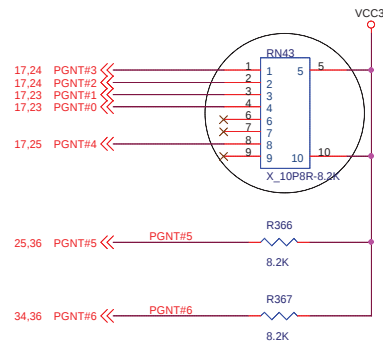
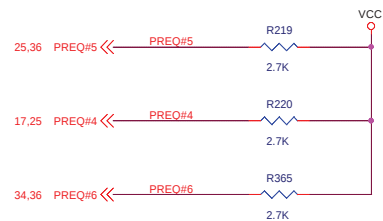
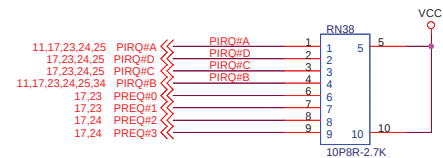
Resume Reset Circuitry



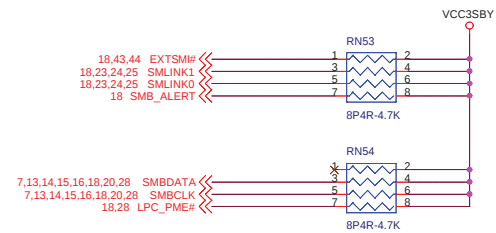
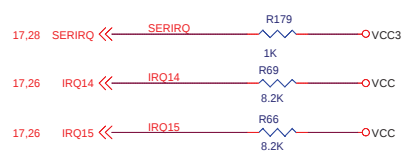
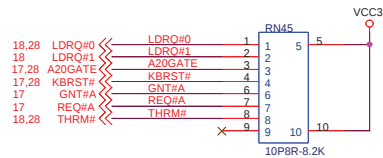
Micro Star Restricted Secret		
Title	Front Panel and ATX Power Connector	Rev
Document Number	MS-6337	30B
MICRO-STAR INT'L CO., LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Friday, March 30, 2001
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PULL-UP RESISTORS

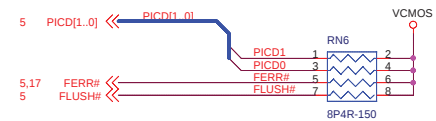
PCI BUS



ICH



CPU



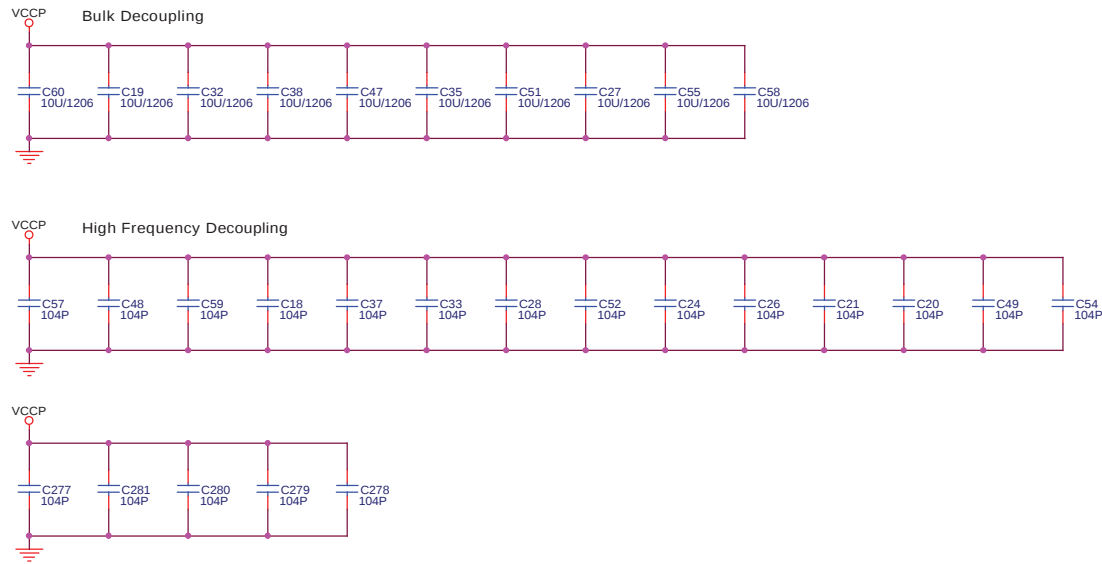
Micro Star Restricted Secret

Title	Pull-Up Resistors	Rev
Document Number	MS-6337	30B
MICRO-STAR INT'L CO., LTD. No. 68, Li-De St, Jung-Ho City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Friday, March 30, 2001 Sheet 45 of 50

370-pin Socket Decoupling

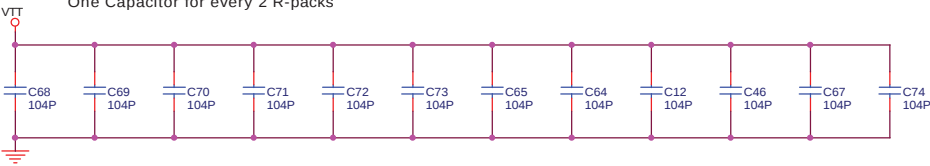
VCC_CORE DECOUPLING

Place in 370 PGA Socket Cavity



VTT DECOUPLING

0603 Package placed within 200mils of VTT Termination R-packs
One Capacitor for every 2 R-packs



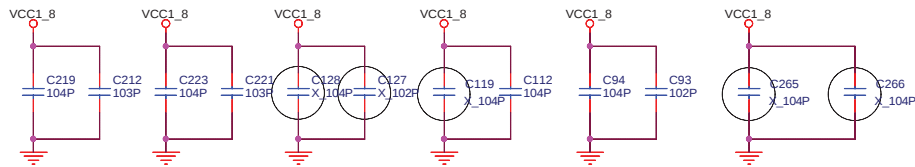
Micro Star Restricted Secret

Title	VRM Decoupling	Rev
Document Number	MS-6337	30B
MICRO-STAR INT'L CO., LTD. No. 89, Li-De St. Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Friday, March 30, 2001
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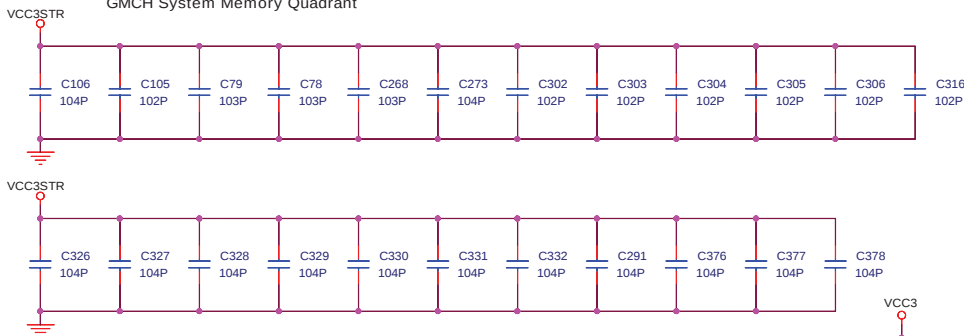
DRAM, Chipset, and BULK Power Decoupling

GMCH Decoupling

GMCH Core Plane Decoupling

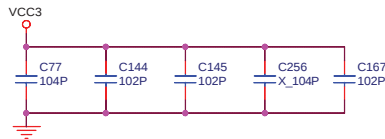


Distribute as close as possible to GMCH System Memory Quadrant

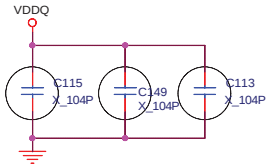


ICH2 Decoupling

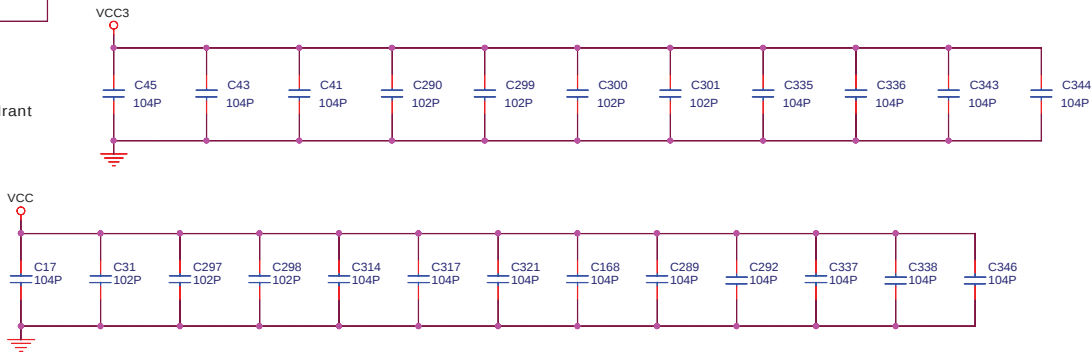
ICH2 3.3V Plane Decoupling:



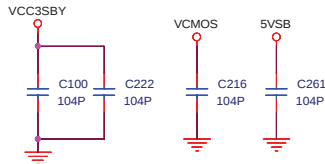
GMCH 3.3V IO Decoupling: Place near GMCH AGP interface Quadrant



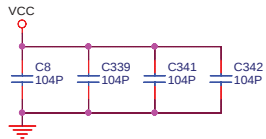
Use surface mount caps placed closed as possible to power pins with short, wide direct connections.



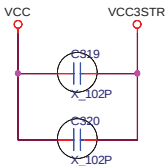
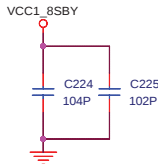
Distribute near the 3.3V standby power pin of the ICH



Distribute near the VCC power pin of the LPC

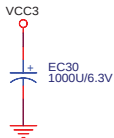


Distribute near the 1.8V standby Power pin of the ICH

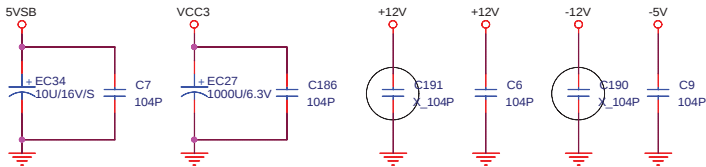


AGP Decoupling

Distribute near the power pins of both SDRAM components



Bulk Power Decoupling



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Title	DRAM, ICH, and GMCH Decoupling	Rev
Document Number	MS-6337	30B
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Revision History

Revision History (Changes from Rev 0A)

Sheet	Description
5	Stuff R37 (330 ohms) for signal PREQ#. Reversed JVT1 that is for up 1 GHz CopperMine processor.
7	Reserved R255 and R254 for REALTEK clock generator RTM560-25R. Swapped signals PCICLK4 and PCICLK5. Delete SW2 and R57, and change RN42 to R251(1K ohms) for signal BSEL0#, and add R252 and R253 (8.2K ohms) pull-down strapping resistors for clock gen FS2 and FS0. Changed SDRAM serial damping RN34, RN35, and RN37 from 22 ohms to 10 ohms R-pack for clock quality. Changed clock 48MHz serial damping RN36 from 22 ohms to 10 ohms for clock quality. Changed CPU and GMCH host clock serial damping R152 and R153 from 33 ohms to 10 ohms for clock quality. Changed clock 66MHz serial damping RN39 from 33 ohms to 22 ohms for clock quality. Changed clock 14MHz serial damping R149, R150 and R242 from 33 ohms to 22 ohms for clock quality. Reserved SDRAM clock bypass CN10, CN11 and CN13 (10pF).
8	Changed GTLREF decoupling capacitor from to 0.1uF.
9	Swapped GMCH reset strap connected RN20.
13~16	Swapped SDRAM clock. Changed SDRAM data and data mask routing.
18	Changed signal VBIAS external capacitor from 2200pF to 0.047uF for RTC accuracy. Removed RN49 (8.2K ohms), and added R269 (8.2K ohms) for GPIO18. Deleted signals MANUSET (GPIO4) and SETVID (GPIO24). Changed signal ATADET1 connect to GPIO4 instead of GPIO2, and GPIO2 connected to RN46. Changed signal NOGO connected to GPIO22 instead of GPIO18. Added signals STRCTRL (GPIO24), KBVCC_CTRL (GPIO25), AUDIO_CTRL1 (GPIO27), and AUDIO_CTRL2 (GPIO28).
21	Changed audio codec to support SigmaTel STAC9708 4-channel and ICE 1236 6-channel.
22	Changed audio codec to support SigmaTel STAC9708 4-channel and ICE 1236 6-channel.
33	Removed L1 and CP1. Added KB/MS VCC control circuit replaced JKBV1, R1 and R2.
34	Added pull-up resistor R271 (4.7K ohms) to VCC3 for ISA HS1 signal.
37	Removed ISA signal NOGO pull-up resistor R206.
38	Changed RN47 to 220 ohms for LED. Reversed LED4, LED5, LED6 and LED1 for definition.
40	Removed Vcore setting page. Removed JSTR1 jumper. Added signal STRCTRL connected to Q4 for DRAM voltage control. Changed VR2 voltage input from 5VSTR to 5VSB. Changed R42 voltage input from VCC1_8SBY to 5VSTR and R42 changed to 300 ohms and R43 changed to 100 ohms. Changed EC32 from 1000uF/6.3V to 10uF/16V SMD.
42	Reserved JGL1 header.
46	Removed C75, C76, C211, C237, C238, C253, C233, C210, C218, C192, C86, C123, C133, C29, C39, C96, C61, C66, C62, C82, C85, and C254.

Revision History (Changes from Rev 0B)

Sheet	Description
4	Changed VIDA[3:0] pull up R-pack 8.2K ohms to VCC.
5	Changed VIDA4 pull up resistor 8.2K ohms to VCC. Added C275 4.7uF/0805 for CPU CLKREF. Added SW1, R297 and R298 for signal BSEL0# and BSEL1# for overclocking.
7	Removed R231. Added four power pin bypass .1uF C269, C270, C271 and C272. Reserved R285 pull down straping for Winbond clock gen mode select. Reserved R286 to PCIRST# signal for Winbond clock gen.
8	Changed C80, C81 to .1uF/0603. Changed C104 to .1uF and C95 to 4.7uF/0805.
9	Added R278 56K ohms pulled up for GMCH power up straps. Added R284 10K ohms pulled down for GMCH power straps.
18	Changed signals ATADET0 and ATADET1 to GPIO6 and GPIO7 instead of GPIO3 (PIRQF#) and GPIO4 (PIRQG#). Changed pulled up RN46 to 2.7K ohms for ICH2 PIRQE# ~ PIRQH#.
22	Added R276 and R277 for Sigmatel 9708 4 channel function.
26	Reserved C283 and C282 10pF to signals IDEACTP# and IDEACTS# for EMI. Changed pulled up RN59 of signal PCIRST# from 8.2K ohms to 1K ohms.
37	Added R275 4.7K ohms for signals NOGO pulled up.
38	Changed DLED pulled up R-pack RN47 and RN58 from 220 ohms to 330 ohms. Added RN76, RN77 and R306 for REALTEK RTA26301.
39	Added R287 and R288 (4.7 ohms) to reduce mosfet gate noise. Added R289 and R290 (10m ohms) for current protect. Added EC39 1500uF/6.3V for Vcore. Changed R25 from 1K ohms 1% to 3.01K ohms 1% for Vcore transient.
40	Added Vcore setting circuits.
41	Changed VR1 from US1150 to 1084, and removed the control circuits for US1150. Added R279 and R280 (4.7K ohms) pulled up to VCC3 for ICH2 GPIO19 and GPIO20. Changed R52 and R59 pulled up from VCC to +12V for NMOS. Changed R49 from 2.94K ohms 1% to 2.43K ohms 1%. Changed R58 from 1.33K ohms 1% to 1.18K ohms 1%.
43	Added R281, R282 and R283 for ICH2 power good.
44	Changed R237 from 10k ohms to 330 ohms and added C274 .01uF to reduce RSMRST# noise.

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Revision History

Revision History (Changes from Rev 1)

Sheet	Description
7	Changed R242 from 22 ohms to 47 ohms for signal ICH14M for EMI. Stuffed C169, C170 (10pF), CN10, CN11, CN13 (8P4C-10pF), and C174 (4.7pF) for EMI.
9	Removed power straps R284 for signal SM_MAA11.
12	Stuffed CN5 (8P4C-100pF) for EMI.
17	Changed R174 from 150 ohms to 200 ohms.
18	Removed signal FAN_CTRL and changed VCORE to GPIO21.
20	Added C295 (104pF) close to U21 power pin 14 for EMI.
21	Stuffed C139 and C141 (470pF) for LINE_IN for EMI.
22	Stuffed C134 and C135 (180pF) for SPEAKER for EMI.
	Changed R276 and R277 from 0 ohms to 10K ohms for audio THD+N quality.
	Stuffed C136, C137 and C140 (102pF) for EMI.
26	Added C307 and C308 (33pF) for EMI.
29	Removed R28 and signal FAN_CTRL.
31	Removed L12 and CP3 for ground level layout.
32	Stuffed CN9 (8P4C-270pF), C124 and C125 (270pF) for EMI.
38	Changed post voice circuit to REALTEK.
39	Reserved R294, and changed R296 to 68 ohms and R295 to 10K ohms for VCORE transient.
41	Added EC41 (10uF/16V SMD), C284 and C285 (1uF) to regulator 1084 adj pin for improving ripple rejection.
43	Added C294, C15 and C44 (102pF) for EMI.
44	Added C310 and C311 (100pF) for EMI.
	Reserved C315 (100pF) for EMI.
	Changed J7 SPEAKER pin out for post voice DLED.
46	Changed C60, C19, C32, C38, C47, C35, C51, C27, C55 and C58 from 4.7uF/0805 to 4.7uF/1206 for VCORE transient.
47	Added C302, C303, C304, C305, C306 and C316 (102pF) to VCC3STR decoupling.
	Added C289, C290, C299, C300 and C301 (102pF) for VCC3 decoupling.
	Added C297, C298 (102pF), C314, C317 and C321 (104pF) for VCC decoupling.
	Reserved C319 and C320 (102pF) cross VCC to VCC3STR.
	Added C291, C292 and C293 (102pF) from VCC3 cross to VCC1_8, VCC and VCCSTR.

Revision History (Changes from Rev 1.0A)

Sheet	Description
12	Added LC circuit to CRT R,G,B signals for EMI.
18	Added JBAT2 1X3 header and R325 for clearing 627HF keyboard password.
	Added a resistor R322 shorting JBAT1 pin 1 and pin 2.
	Connected GPIO28 to CNR signal PRIMARY_DN# to fit to CNR spec 1.0.
19	Added three pulled up resistors to FWH GPIO, GPI1 and GPI4.
20	Changed CNR signal PRIMARY_DN# detected circuit to conform to CNR spec 1.0.
21	Added smart DLED post speech output to codec PC_BEEP pin.
28	Added a capacitor C340 104pF for 5VSB decoupling.
30	Reserved CN20 and CN21 180pF for parallel port EMI.
32	Stuffed C129 (102pF) for EMI.
38	Reserved smart DLED 8 languages supported.
	Added smart DLED post speech output to codec PC_BEEP pin.
47	Added VCC decoupling C337, C338, C345, C346, C339, C341, and C342 (104pF) for EMI.
	Added VCC3 decoupling C335, C336, C343, and C344 (104pF) for EMI.
	Added VCC3STR decoupling C326, C327, C328, C329, C330, C331 and C332 (104pF) for EMI.

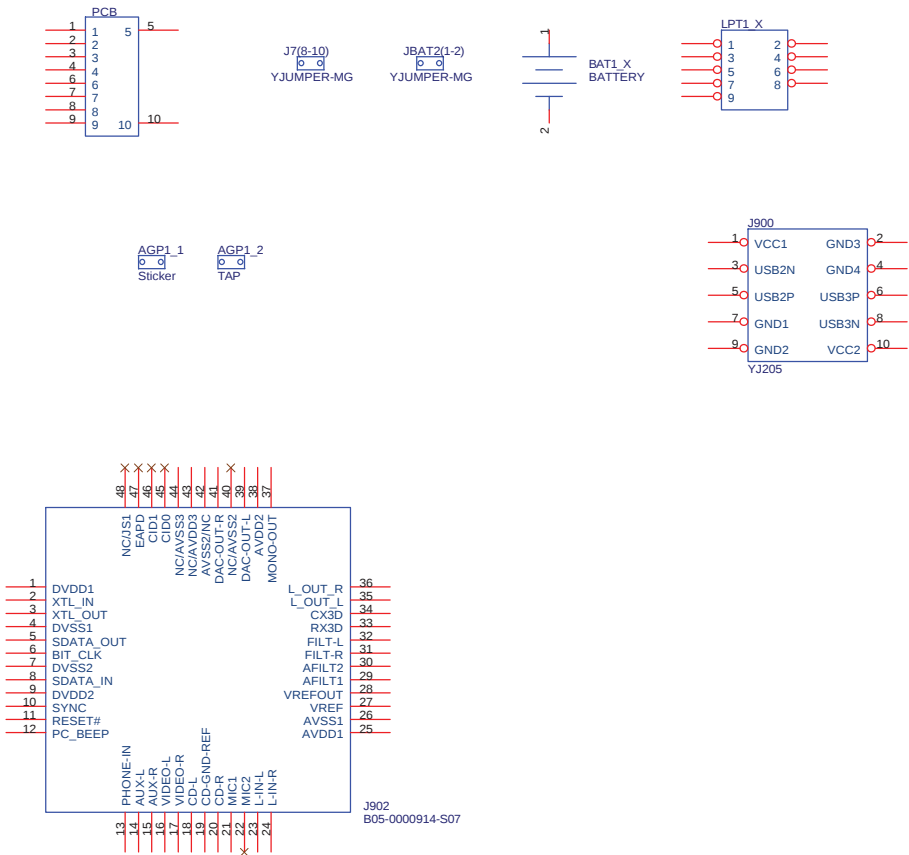
Revision History (Changes from Rev 3.0)

Sheet	Description
5	Reserved pull-up resistors R357 and R358 for processor BSEL#.
6	Changed CPU Rtt RN17, RN16, RN15, RN18, RN10, RN9, RN5, RN8, RN14, RN13, RN12, RN11, RN19, and RN7 from 10P8R-68 ohms to 10P8R-56 ohms.
	Changed signal BREQ# pull-down resistor R30 from 68 ohms to 56 ohms.
7	Changed crystal 14.31818 MHz Y1 from CL=16pF to CL=32pF, and added C194 and C202 22pF for frequency 14.31818 MHz accuracy.
	Reserved R254, R359 and R360, added R361, R362 for Realtek clock generator.
9	Added SM_MAA4~7, SM_MAB4~7 and SM_MAC4~7 serial resistors RN102, RN103 and RN101 8P4R-10 ohms.
10	Reserved signal OCLOCK serial resistor R100 and added signal RCLOCK pull-down resistor C116 8.2k ohms for 815EP MCH.
	Added signal TVCLKIN pull-up resistor R376 8.2k ohms to VCC1.8 for 815EP MCH.
	Added signal DOTCLK and IWASTE pull-down resistors C111 and R377 8.2k ohms for 815EP MCH.
	Changed signal IREF pull=down resistor R80 from 174 ohms 1% to 8.2 kohms for 815EP MCH.
13	Changed DIMM1~4 clock routing.
26	Added R65 and R68 10 kohms for harddisk active led.
27	added R385 and R386 0 ohm for PC to PC networking controller.
28	Reserved IO 627HF clock staps R378 4.7k ohms.
34	Added R380 5.1 ohms / 0805 for IDE RAID pin 117 analog VCC.
	Changed the INT# and IDSEL of IDE RAID for compaliability.
36	Removed signals SMBDATA and SMBCLK connecting to U29 pin 13 and pin 16.
37	This page is added for USB PC to PC networking circuit.
38	Changed R308 from 61.9k ohms 1% to 33k ohms 1% for post speech intrnal frequency.
	Added header J13 and R379 for post speech speaker output connecting to chassis speaker.
43	Short C369 for PC beep to buzzer.
	Disconnected signal SPEAKR to JFP1 pin 13.

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D1	VCC3_3_J	VCC3_3_A	C1
D2	VCC3_3_K	GND_A	C2
D3	VCC3_3_L	VCC3_3_B	C3
D4	VCC3_3_M	GND_B	C4
D5	VCC3_3_N	GND_C	C5
D6	VCC3_3_O	GND_D	C6
D7	VCC3_3_P	GND_E	C7
D8	VCC3_3_Q	GND_F	C8
X D9	PRSN#2	RESV_A	C9
X D10	PRSN#1	RESV_B	C10

KEY			
B1	AGP_OVRcnt#	VCC_12V_A	A1
B2	5V_A	TYPEDET#	A2
B3	5V_B	RESV_C	A3
B4	AGP_USB+	AGP_USB-	A4
B5	GND_Q	GND_G	A5
B6	INTB#	INTA#	A6
B7	AGPCLK_CONN	RST#	A7
B8	REQ#	GNT#	A8
B9	VCC3_3_R	VCC3_3_E	A9
B10	ST0	ST1	A10
B11	ST2	RESV_D	A11
B12	RBF#	PIPE#	A12
B13	GND_R	GND_H	A13
B14	RESV_L	WBF#	A14
X B15	SBA0	SBA1	A15
B16	VCC3_3_S	VCC3_3_F	A16
B17	SBA2	SBA3	A17
B18	SB_STB	SB_STB#	A18
B19	GND_S	GND_I	A19
B20	SBA4	SBA5	A20
B21	SBA6	SBA7	A21
X B22	RESV_M	RESV_E	A22
B23	GND_T	GND_J	A23
B24	3_3AUX_1	RESV_F	A24
B25	VCC3_3_T	VCC3_3_G	A25
B26	GAD31	GAD30	A26
B27	GAD29	GAD28	A27
B28	VCC3_3_U	VCC3_3_H	A28
B29	GAD27	GAD26	A29
B30	GAD25	GAD24	A30
B31	GND_U	GND_K	A31
B32	AD_STB1	AD_STB1#	A32
B33	GAD23	C/BE#3	A33
B34	VDDQ_F	VDDQ_A	A34
B35	GAD21	GAD22	A35
B36	GAD19	GAD20	A36
B37	GND_V	GND_L	A37
B38	GAD17	GAD18	A38
B39	C/BE#2	GAD16	A39
B40	VDDQ_G	VDDQ_B	A40
B41	IRDY#	FRAME#	A41
X B42	3_3AUX_2	RESV_G	A42
X B43	GND_W	GND_M	A43
X B44	RESV_N	RESV_H	A44
X B45	VCC3_3_V	VCC3_3_I	A45
X B46	DEVSEL#	TRDY#	A46
B47	VDDQ_H	STO#	A47
B48	PERR#	PME#	A48
B49	GND_X	GND_N	A49
B50	SERR#	PAR	A50
B51	C/BE#1	GAD15	A51
B52	VDDQ_I	VDDQ_C	A52
B53	GAD14	GAD13	A53
B54	GAD12	GAD11	A54
B55	GND_Y	GND_O	A55
B56	GAD10	GAD9	A56
B57	GAD8	C/BE#0	A57
B58	VDDQ_J	VDDQ_D	A58
B59	AD_STB0	AD_STB0#	A59
B60	GAD7	GAD6	A60
B61	GND_Z	GND_P	A61
B62	GAD5	GAD4	A62
B63	GAD3	GAD2	A63
B64	VDDQ_K	VDDQ_E	A64
B65	GAD1	GAD0	A65
X B66	VREFCG	VREFGC	A66

KEY			
F1	RESV_O	RESV_I	E1
X F2	RESV_P	RESV_J	E2
F3	GND_AA	VCC_12V_B	E3
F4	GND_BB	VCC_12V_C	E4
F5	GND_CC	VCC_12V_D	E5
F6	GND_DD	VCC_12V_E	E6
F7	GND_EE	VCC_12V_F	E7
F8	GND_FF	VCC_12V_G	E8
F9	GND_GG	VCC_12V_H	E9
F10	GND_HH	VCC_12V_I	E10
F11	GND_II	VCC_12V_J	E11
F12	GND_JJ	VCC_12V_K	E12
F13	GND_KK	VCC_12V_L	E13
F14	GND_LL	VCC_12V_M	E14

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