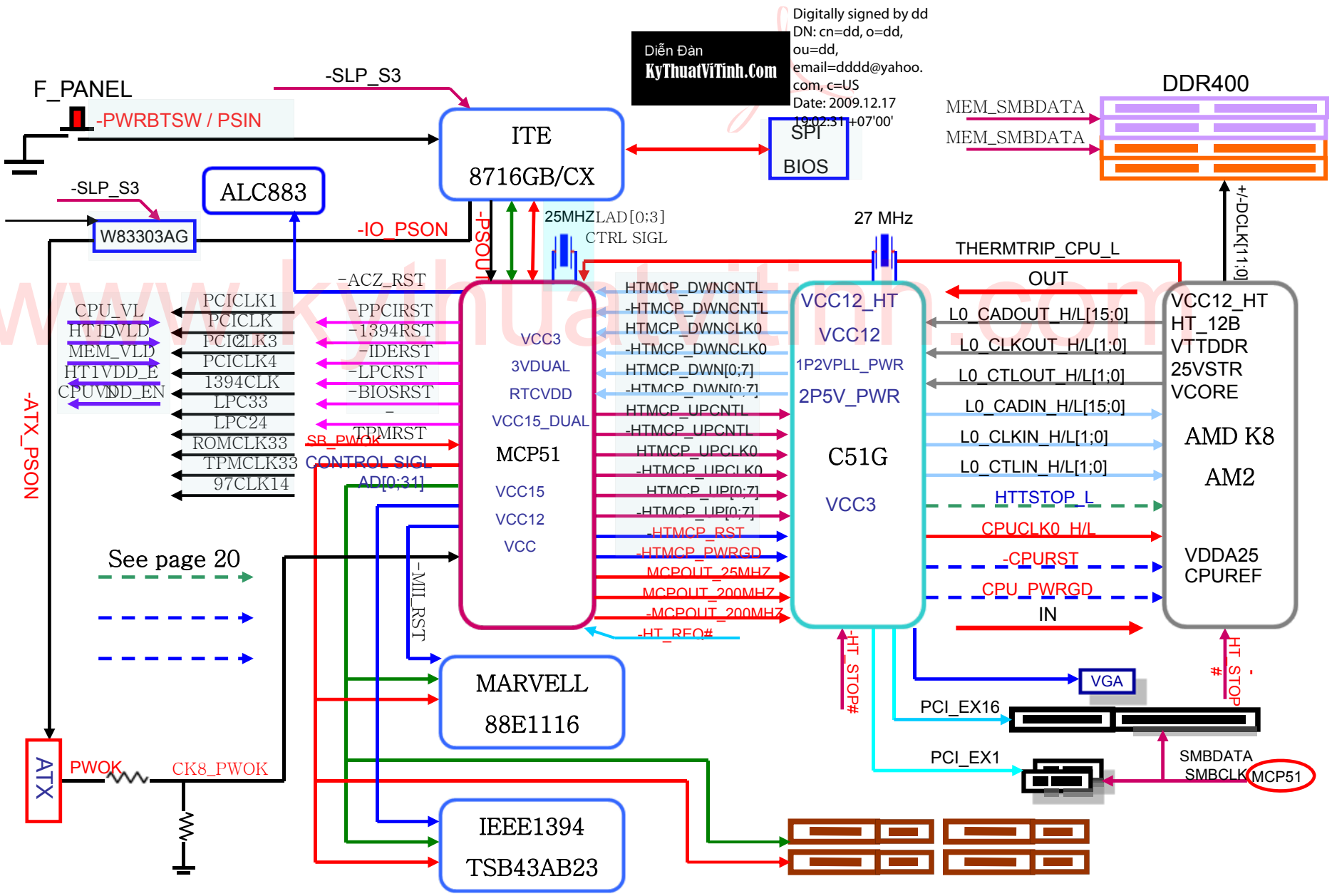
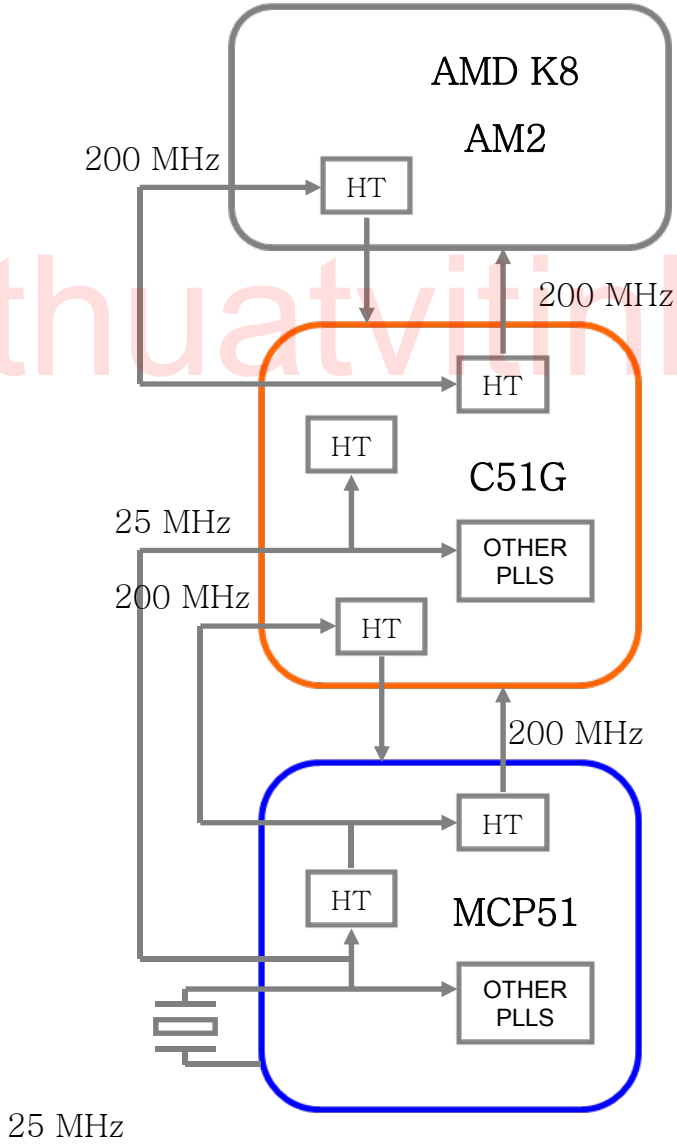
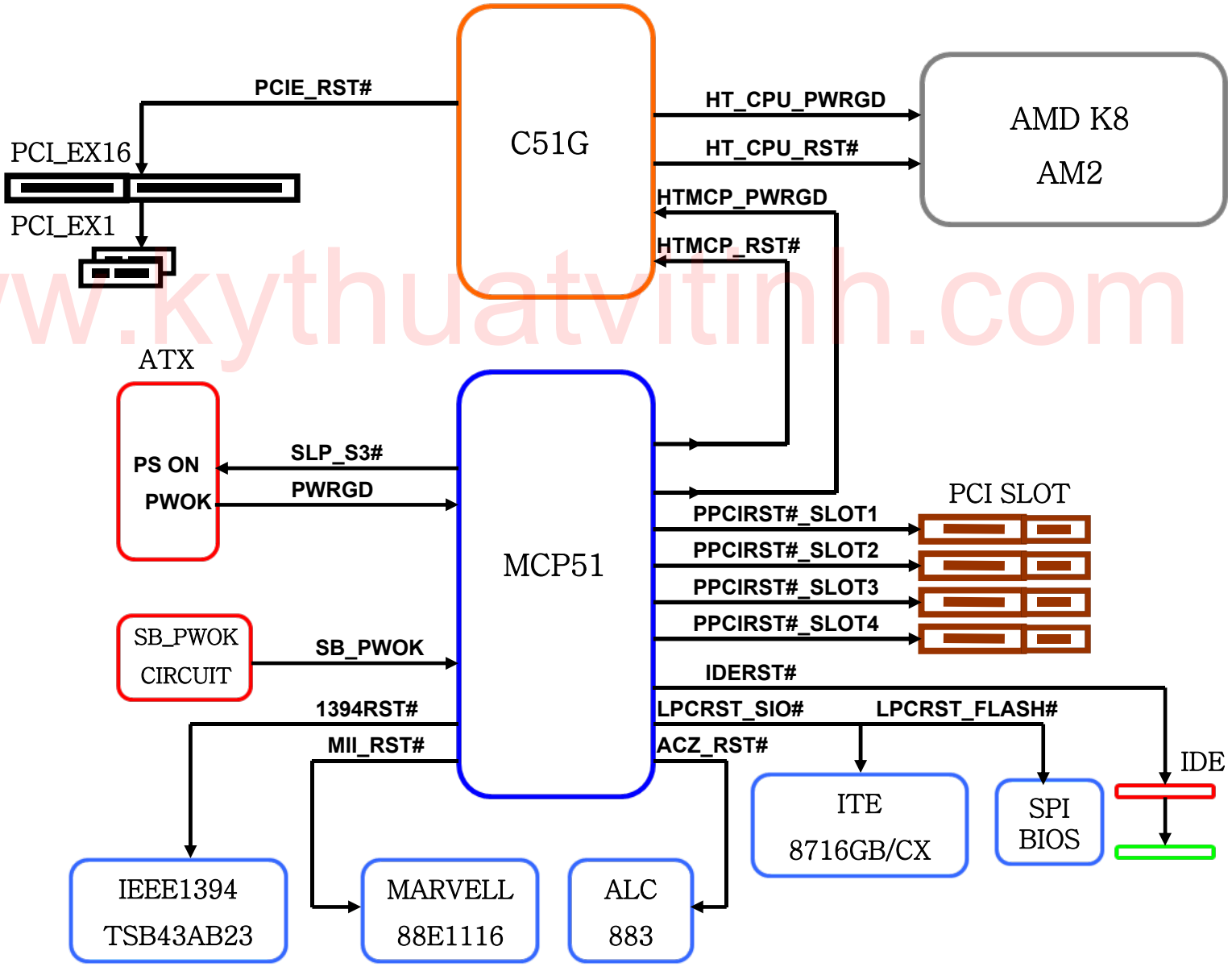
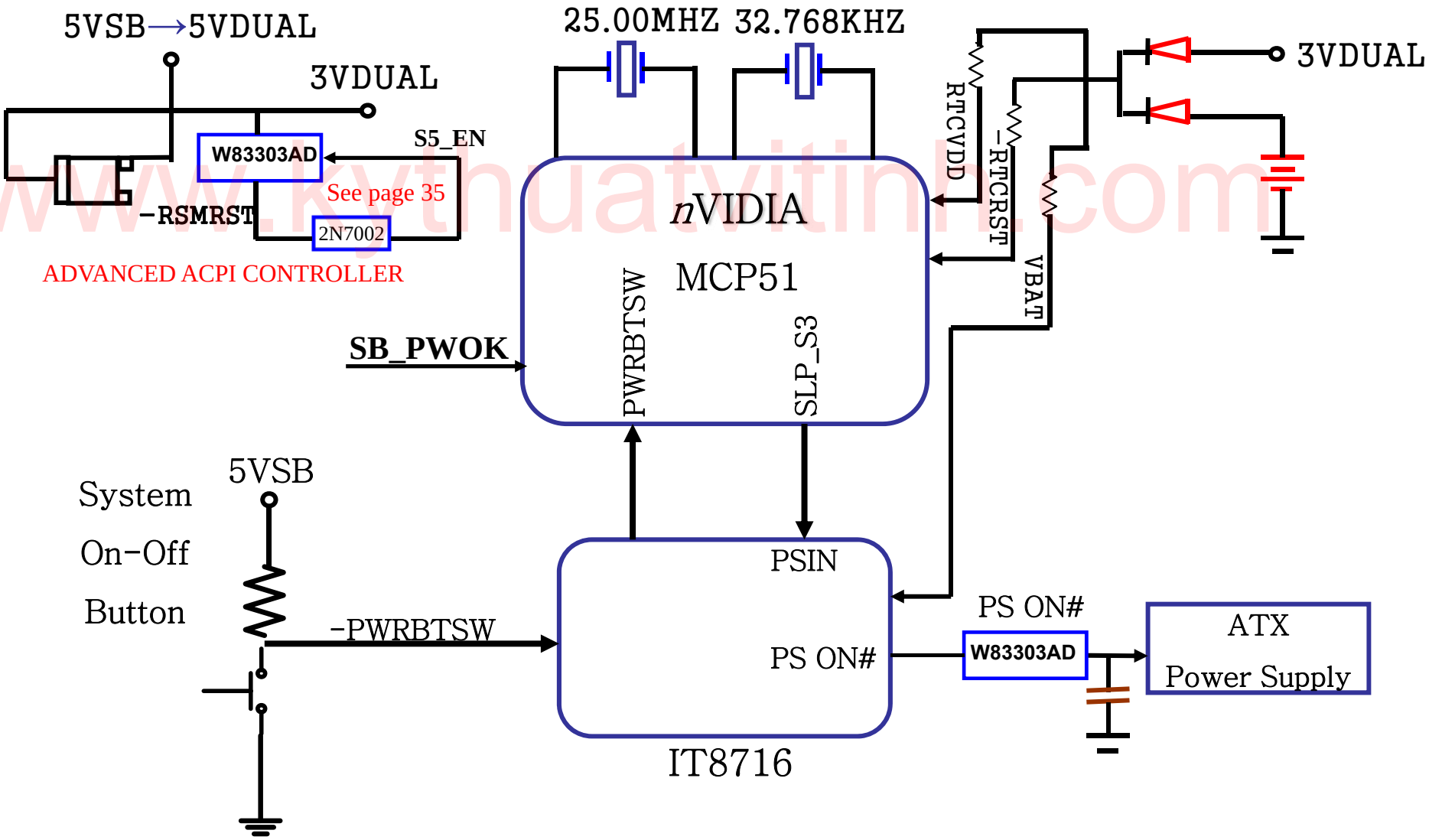
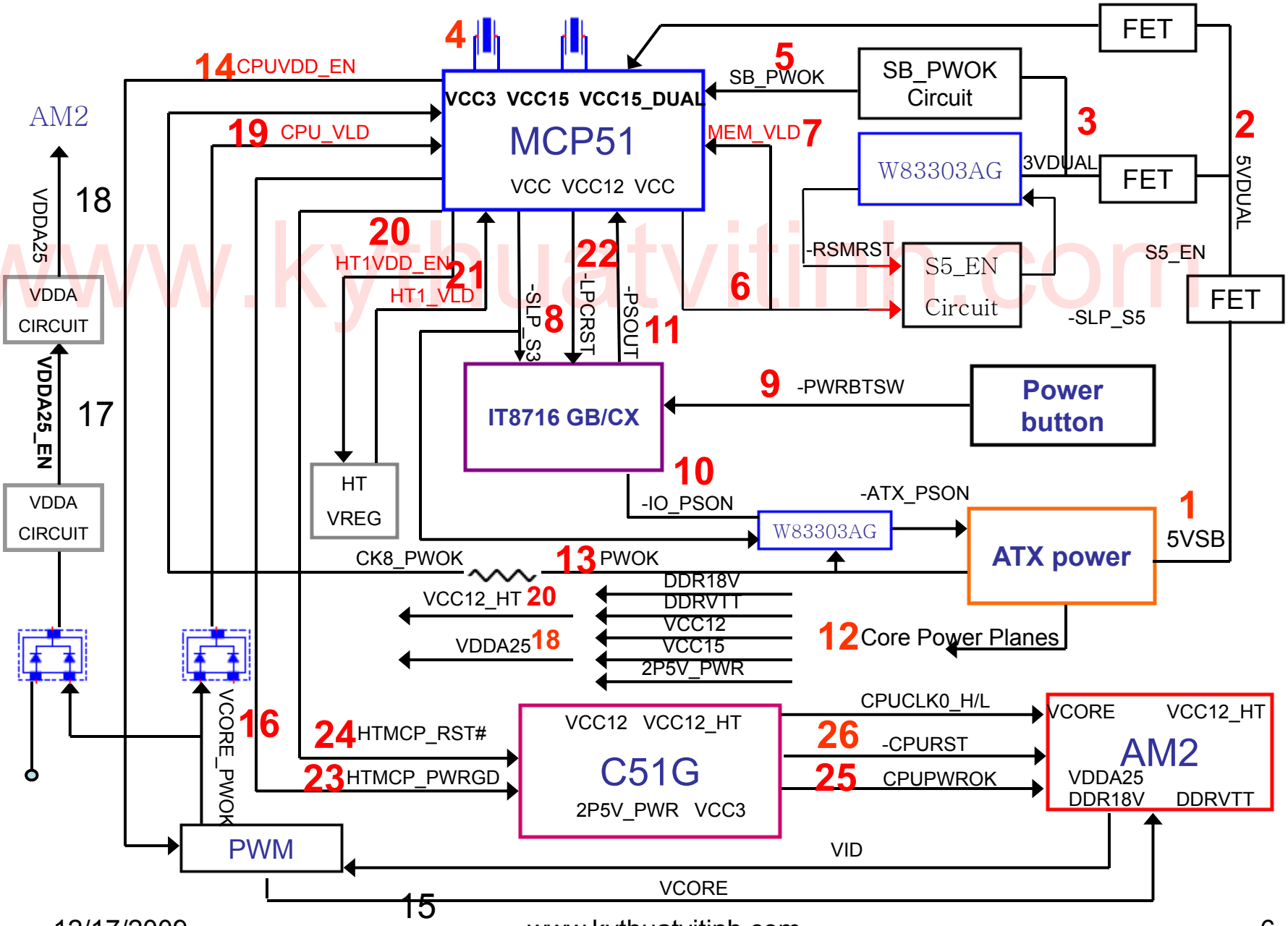


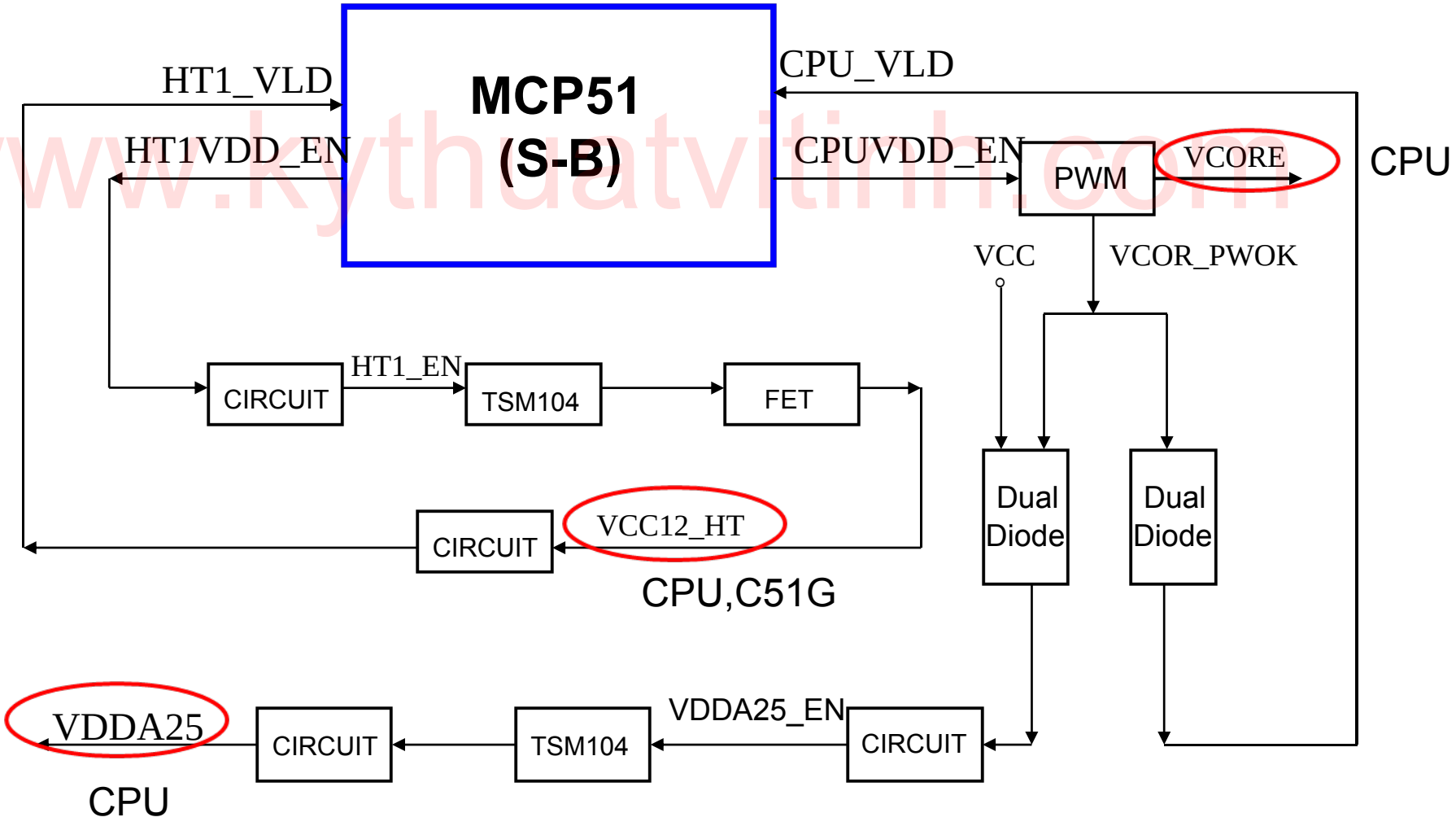


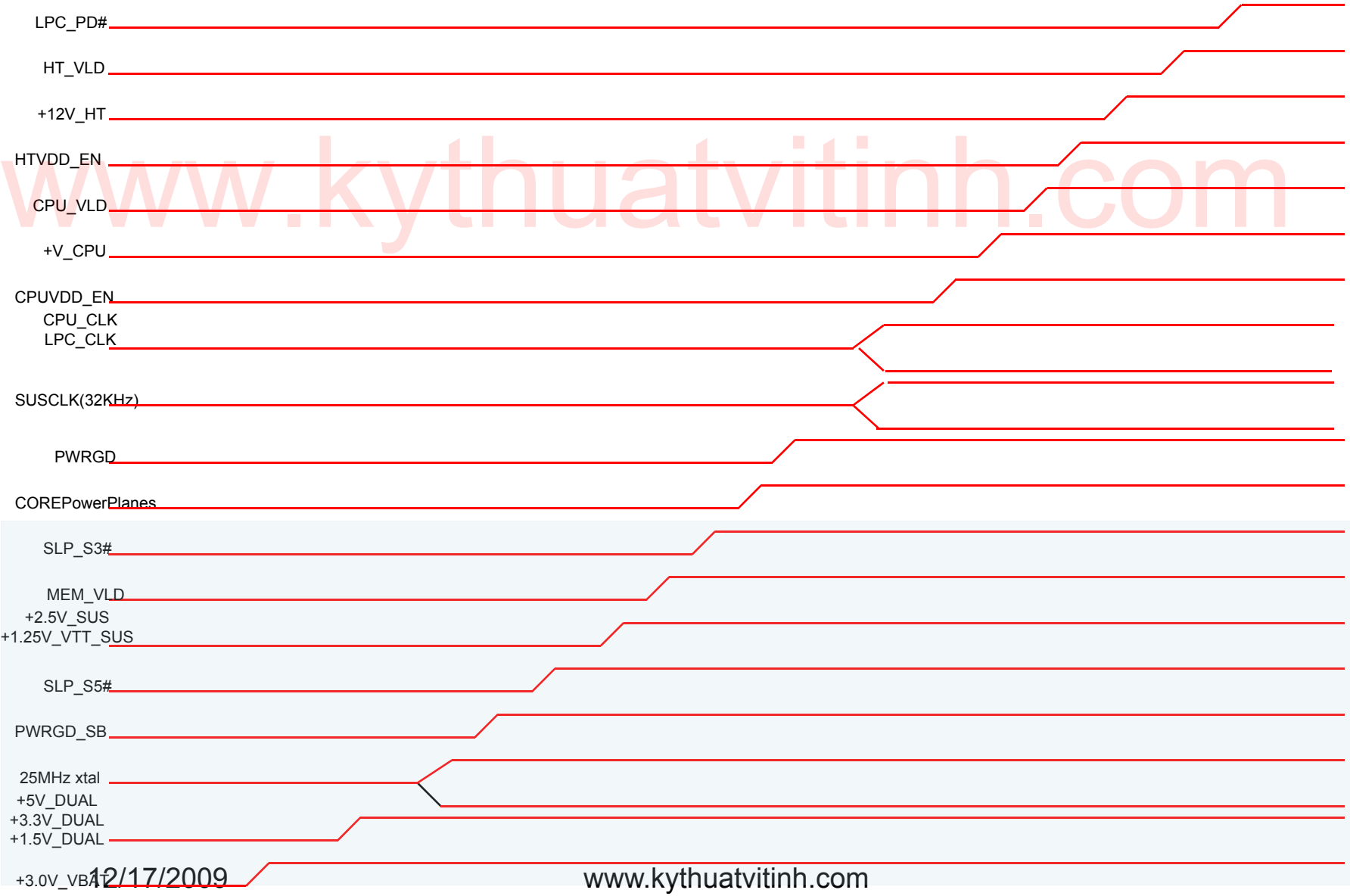




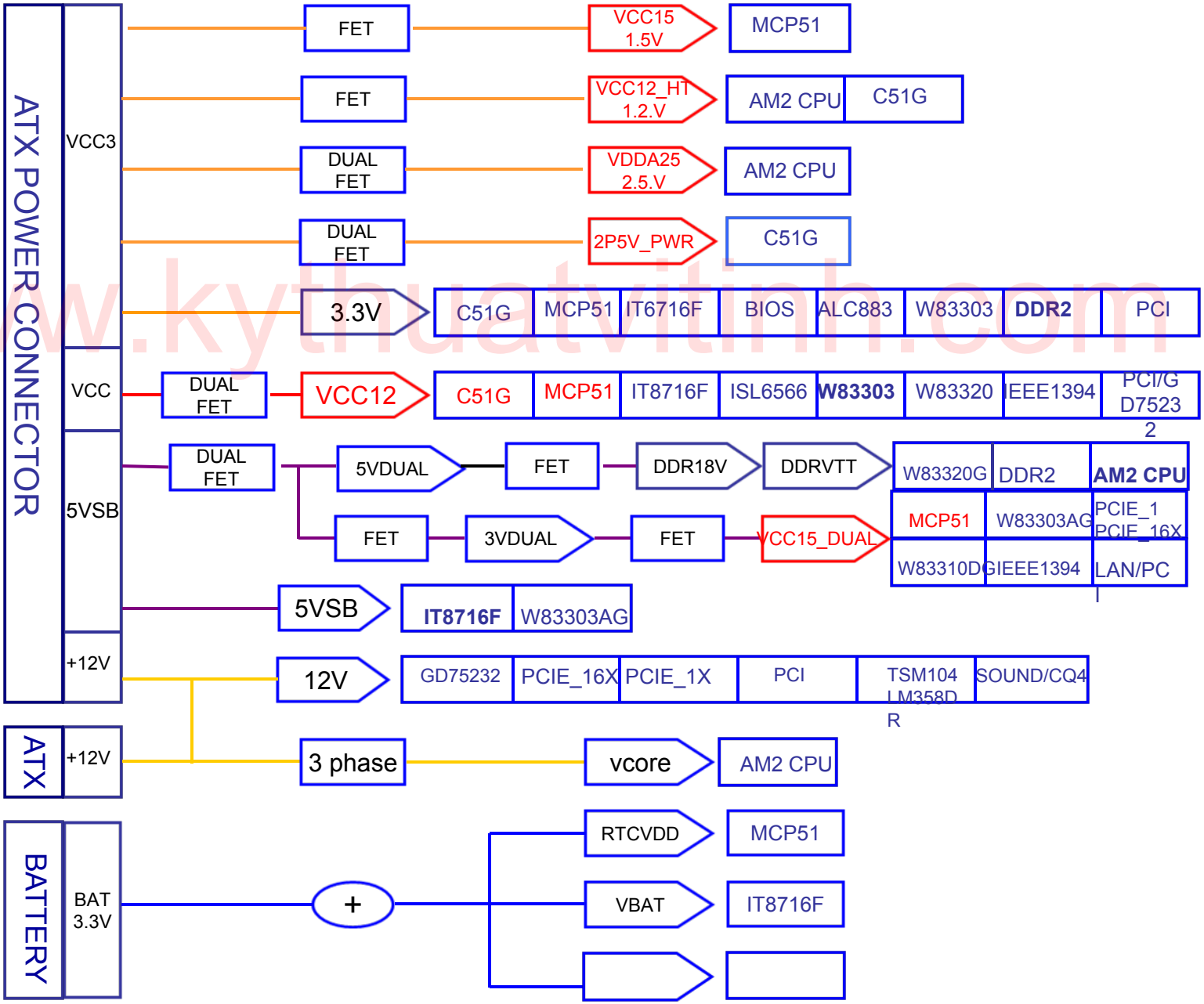


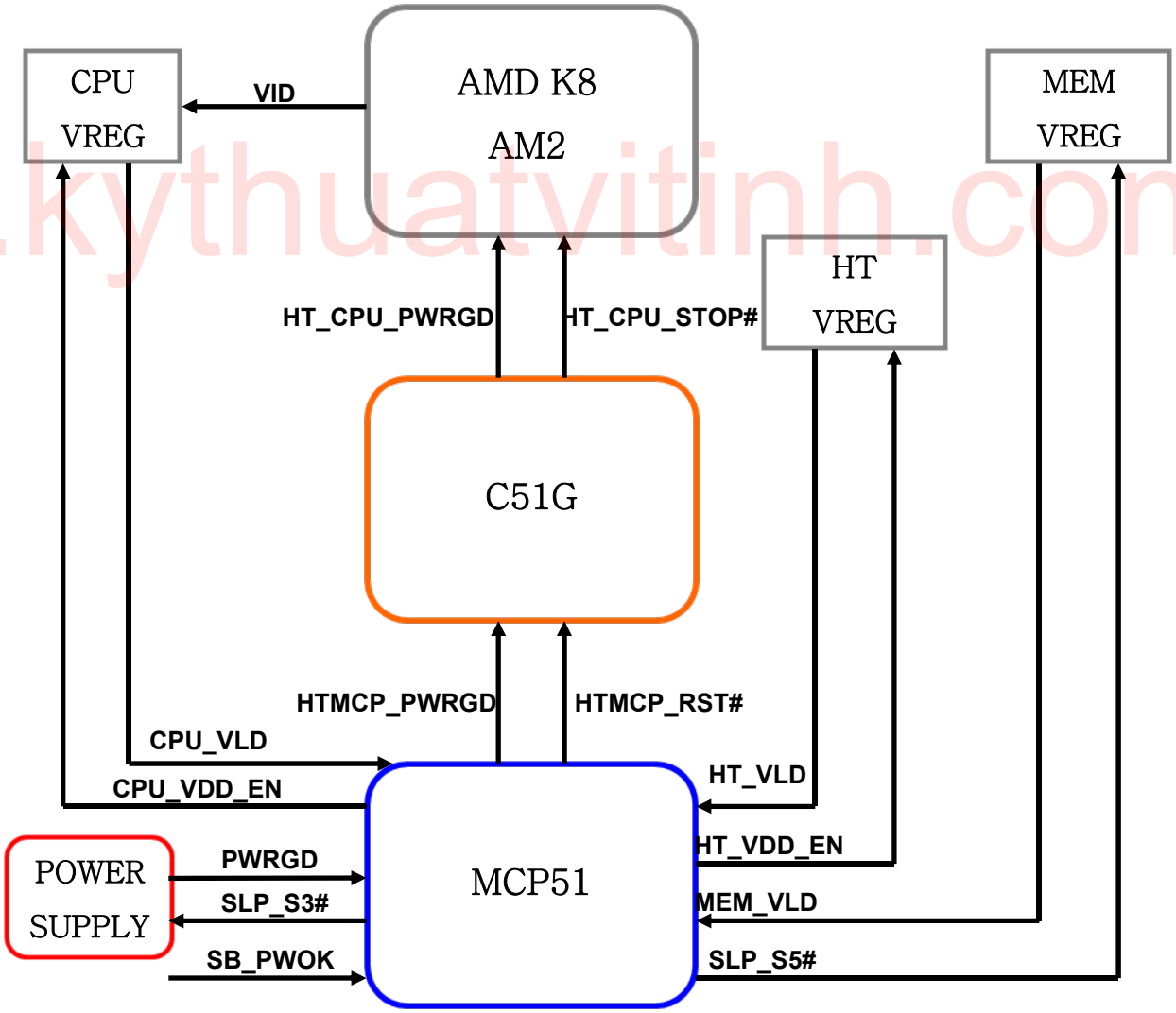
K8 Power Sequence

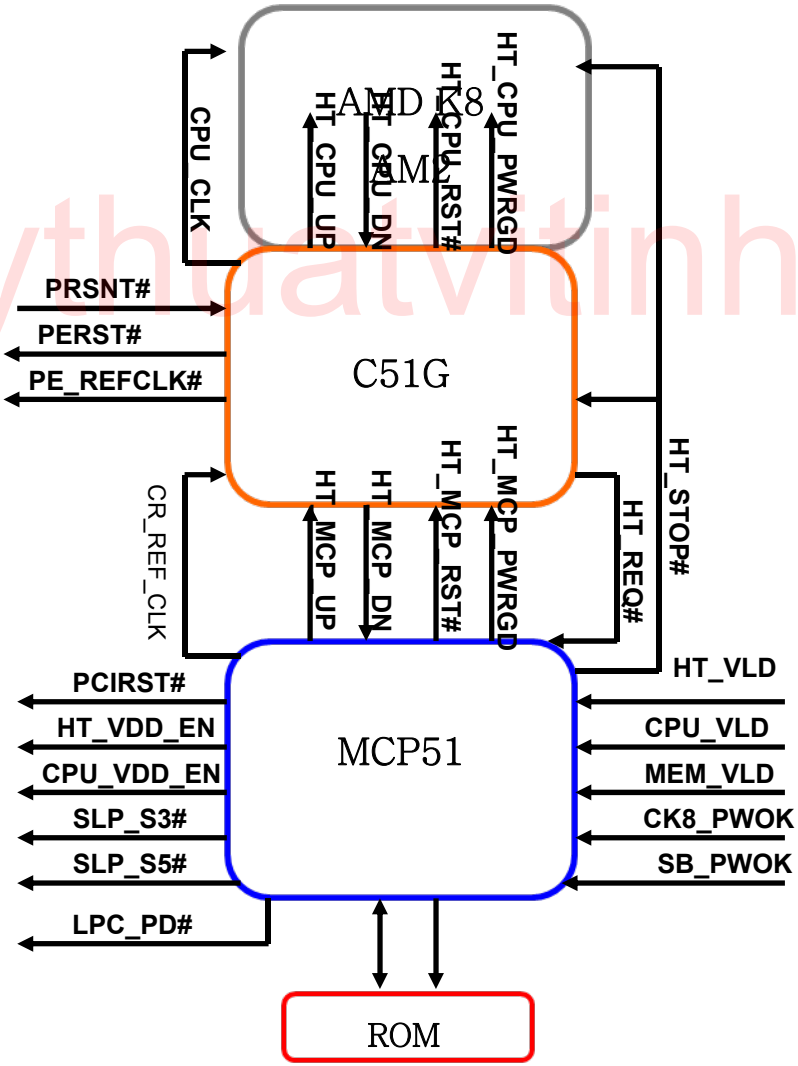


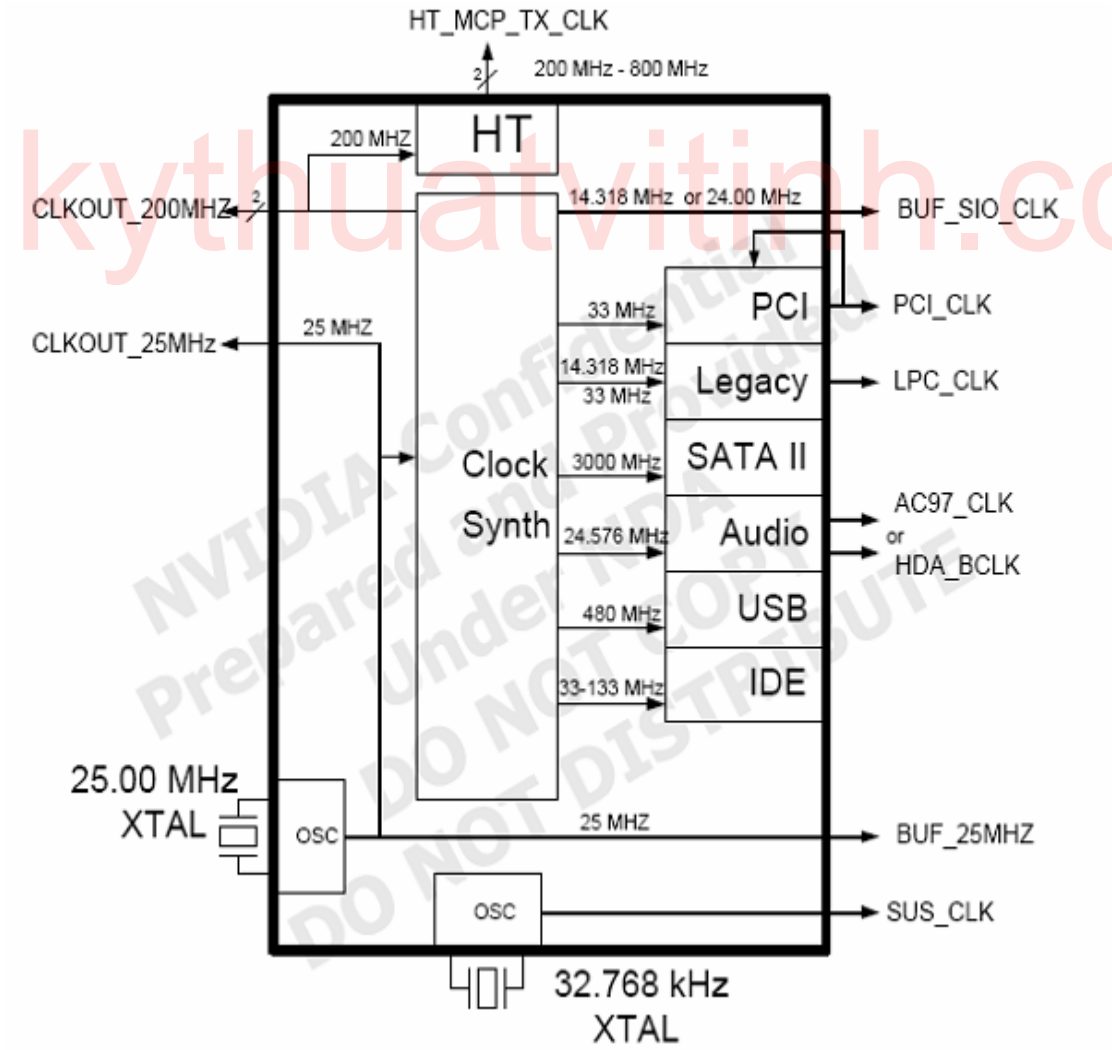


Sym	Parameter	Min	Max	Units	Notes
PS100	**+3.0VBAT** active to **+V_DUAL** active	0		ms	1, 8
PS101	**+V_DUAL** active to XTAL OSC active	0	10	ms	1, 2
PS102	**+V_DUAL** active to **PWRGD_SB** assert	10		ms	5
PS104	**PWRGD_SB** assert to **SLP_S5#** de-assert	11	12	ms	3
PS105	**SLP_S5#** de-assert to **+2.5V_SUS** valid	0		ms	4, 6
PS106	**+2.5V_SUS** valid to **MEM_VLD** assert	0		ms	5
PS107	**MEM_VLD** assert to **SLP_S3#** de-assert	10	15	ms	3
PS108	**SLP_S3#** de-assert to VCC CORE planes valid	0		ms	1, 4, 8
PS109	VCC CORE planes valid to **PWRGD** assert	0		ms	5
PS110	**PWRGD** assert to CPU and LPC clocks active	50	73	ms	7
PS111	CPU and LPC clocks active to **CPUVDD_EN** assert	10	31	ms	3
PS112	**CPUVDD_EN** assert to **+V_CPU** valid	0		ms	4
PS113	**+V_CPU** valid to **VRM_PWRGD** assert	0		ms	5
PS114	**VRM_PWRGD** assert to **HTVDD_EN** assert	10	15	ms	3
PS115	**HTVDD_EN** assert to **+1.2V_HT** valid	0		ms	4
PS116	**+1.2V_HT** valid to **HT_VLD** assert	0		ms	5
PS120	**+V_DUAL** active to power plane controls valid		10	ms	
PS121	VCC CORE planes valid to power state controls valid		1	ms	
PS122	**HT_VLD** to power state controls de-assert		12	ms	









CPU Power Supply Interface Signals

Signal	Voltage	Definition	Remark
VCORE (VDD)	1.5V	Core power supply	
VCC12_HT/HT12B (VLDT_A)	1.2V	Hyper Transport I/O ring power supplies	
VDD25 (VDDA)	2.5V	Filtered PLL Supply Voltage	
DDR18V(VDDIO)	1.8V	DDR SDRAM I/O ring power supply	
DDRVTT (VTT)	0.9V	VTT Regulator voltage	
CPU_M_VREF (M_VREF)	VREF	DRAM Interface Voltage Reference	
COREFB_H/L (VDD_FB_H/L)	A	Differential feedback for VDD Power Supply	

C51XE Power Supply Interface Signals

Signal	Voltage	Definition	Remark
VCC12 (+ 1.2V_CORE)	1.6V	Core Power Rail ,this power plane is for the C51G core	
VCC12_HT (+ 1.2V_HT)	1.2V	Isolated Hyper Transport power rail	
2P5V_PWR (+ 2.5V_CORE)	2.5V	2.5V Core Power, this voltage is used to power the core logic of the C51G	
1P2VPLL_PWR (+ 12V_PLL)	1.2V	+ 1.2V Voltage, this is a filtered version of the + 1.2V_ core voltage.	
1P2VPEA_PWR (+ 12V_PEA)	1.2V	+ 1.2V Voltage, provides power to the PCI Express integrated into the C51G	

MCP55P Power Supply Interface Signals

Signal	Voltage	Definition	Remark
RTCVDD (+ 3.3V_VBAT)	3.3V	RTC Power well ,Battery backed-up power plane on the onboard Real Time Clock.	
+ 5V_DUAL	5 V	Dual System Supply, The + 5V_SB supply powers this rail in low power status and the + 5V supply powers this rail during normal operation .	
+ 3.3V_DUAL	3.3 V	Dual Pad Supply, The + 5V_dual supply powers this rail in low power status and the + 3V supply powers this rail during normal operation .	
VCC15_DUAL (+ 1.2V_DUAL)	1.6 V	Dual Logic Supply, Power plane for the logic in the MCP51 that remains active in all system status .	
VCC12 (+ 1.2V) (+ 1.2V_HT)	1.6V	VCORE Logic Supply, Power plane for the core logic in MCP51 , also potentially used for Hyper Transport pad power.	

AMD K8 AM2 Power Sequencing Signals

Signal	I/O	Definition	Remark
MEM_VLD#	I	Memory + 2.5 V Power Valid This signal indicates that the DDR DRAM + 1.8 V power plane is valid.	
CPUVDD_EN	O	CPU VDD Enable This signal controls the voltage regulator controlling the CPU_VDD power plane.	
CPU_VLD#	I	CPU VDD Power Valid This signal indicates that the CPU VDD power plane is valid.	
HT1VDD_EN	O	Hyper Transport Link + 1.2V_HT Enable This signal controls the voltage regulator controlling the + 1.2V_HT power plane.	
HT1_VLD#	I	Hyper Transport Link + 1.2 V Power Valid This signal indicates that the + 1.2V_HT power plane is valid.