Schematics Page Index (Title / Revision / Change Date)

Page	Title of Schematics Page	Rev.	Date
01	Index Page	1.0	2008/03/20
02	Block Diagram(System)	1.0	2008/03/20
03	CLOCK GEN	1.0	2008/03/20
04	CPU HOST 1/3	1.0	2008/03/20
05	CPU THERMAL 2/3	1.0	2008/03/20
06	CPU POWER 3/3	1.0	2008/03/20
07	Eaglelake HOST/PCI-E 1/7	1.0	2008/03/20
08	Eaglelake VGA/MISC 2/7	1.0	2008/03/20
09	Eaglelake DDRII CH A 3/7	1.0	2008/03/20
10	Eaglelake DDRII CH B 4/7	1.0	2008/03/20
11	Eaglelake POWER 5/7	1.0	2008/03/20
12	Eaglelake POWER 6/7	1.0	2008/03/20
13	Eaglelake GND 7/7	1.0	2008/03/20
14	DDRII(CHA DIMM0) 1/2	1.0	2008/03/20
15	DDRII(CHB DIMM1) 2/2	1.0	2008/03/20
16	DDRII Termination	1.0	2008/03/20
17	ICH10 (PCIe/USB/PCI) 1/5	1.0	2008/03/20
18	ICH10 (HOST/SATA) 2/5	1.0	2008/03/20
19	ICH10 (PM/LAN/HDA) 3/5	1.0	2008/03/20
20	ICH10 (Power) 4/5	1.0	2008/03/20
21	ICH10 (Ground) 5/5	1.0	2008/03/20
22	Flash ROM& Debug	1.0	2008/03/20
23	Power Sequence 1/2	1.0	2008/03/20
24	Power Sequence 2/2	1.0	2008/03/20
25	INTEL GLAN Boazman	1.0	2008/03/20
26	PCIe WLAN	1.0	2008/03/20
27	TV-TUNER	1.0	2008/03/20
28	PCI BUS (Bridge) 1/2	1.0	2008/03/20
29	PCI BUS(MS/SD/iLink) 2/2	1.0	2008/03/20
30	SATA HDD /SATA ODD	1.0	2008/03/20
31	USB Port	1.0	2008/03/20
32	CIR&BT	1.0	2008/03/20
33	CAMERA	1.0	2008/03/20
34	FELICA	1.0	2008/03/20
35	Thermal & BL	1.0	2008/03/20
36	FAN	1.0	2008/03/20
37	LED	1.0	2008/03/20
38	DB CONN(PSwitch)	1.0	2008/03/20
39	NB9M (PCI-E) 1/9	1.0	2008/03/20
40	NB9M(PCIE TX) 2/9	1.0	2008/03/20
41	NB9M (PCIE RX&STRAP) 3/9	1.0	2008/03/20
42	NB9M (GDDR) 4/9	1.0	2008/03/20
43	NB9M (CRT)5/9	1.0	2008/03/20
44	NB9M (LVDS) 6/9	1.0	2008/03/20
45	NB9M (XTAL/GPIO) 7/9	1.0	2008/03/20
46	NB9M(CRYSTAL&SSIC)8/9	1.0	2008/03/20
47	NB9M (GROUND) 9/9	1.0	2008/03/20
48	VRAM(GDDR)	1.0	2008/03/20
49	VRAM(BYPASS)	1.0	2008/03/20
50	SDVO TO LVDS	1.0	2008/03/20
51	LVDS-Inverter	1.0	2008/03/20
52	CRT	1.0	2008/03/20
53	AUDIO Block Diagram(All)	1.0	2008/03/20
54	AUDIO(CODEC & POWER)	1.0	2008/03/20
55	AUDIO(HP)	1.0	2008/03/20
56	AUDIO(SPK AMP)	1.0	2008/03/20
57	AUDIO(EXT MIC & LINE IN)	1.0	2008/03/20
58	AUDIO (MUTE)	1.0	2008/03/20
59	AUDIO(EQ)	1.0	2008/03/20
60	Power Block Diagram	1.0	2008/03/20
61	DCIN	1.0	2008/03/20
62	SYSPWR(+3V/+5V)	1.0	2008/03/20
63	DDR2PWR(+1 8V/+0 9V)	1.0	2008/03/20
64	SYSPWR(+1 1V/+1 5V)	1.0	2008/03/20
65	VGAPWR	1.0	2008/03/20
66	VHCORE (1)---ISL6334A	1.0	2008/03/20
67	VHCORE (2) ---ISL6208	1.0	2008/03/20
68	HDD PWR(+12V)	1.0	2008/03/20
69	SYSPWR(+1 2V)	1.0	2008/06/14
70	OVP Protect	1.0	2008/03/20
71	Others PWR Plane	1.0	2008/03/20
72	Corwin spring(3_3/1_1V_CL)	1.0	2008/03/20
73	Hole & BOSS	1.0	2008/03/20
74	Revision History(1)	1.0	2008/03/20
75	Revision History(2)	1.0	2008/03/20
76	Revision History(3)	1.0	2008/03/20
77	Revision History(4)	1.0	2008/03/20
78	Revision History(5)	1.0	2008/04/02

Project Code & Schematics Subject:	M810 Main Board

PCB P/N	1P-0086J00-6010

P. Leader	Check by	Design by

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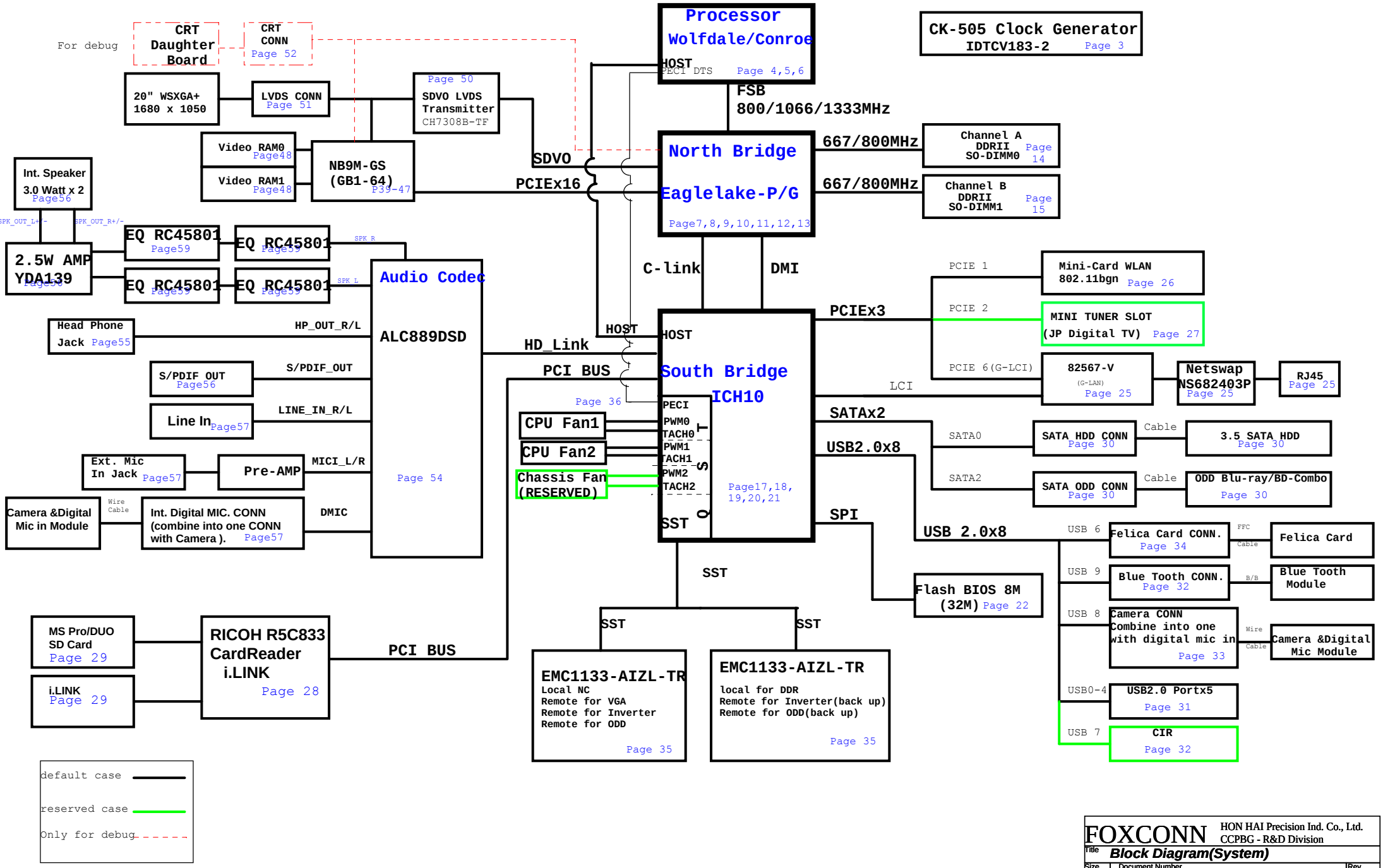
Title	Index Page	
Size A3	Document Number AIO-C Mother Board MP	Rev 1.1
Date: Tuesday, July 15, 2008	Sheet 1 of 80	

M810 Block Diagram



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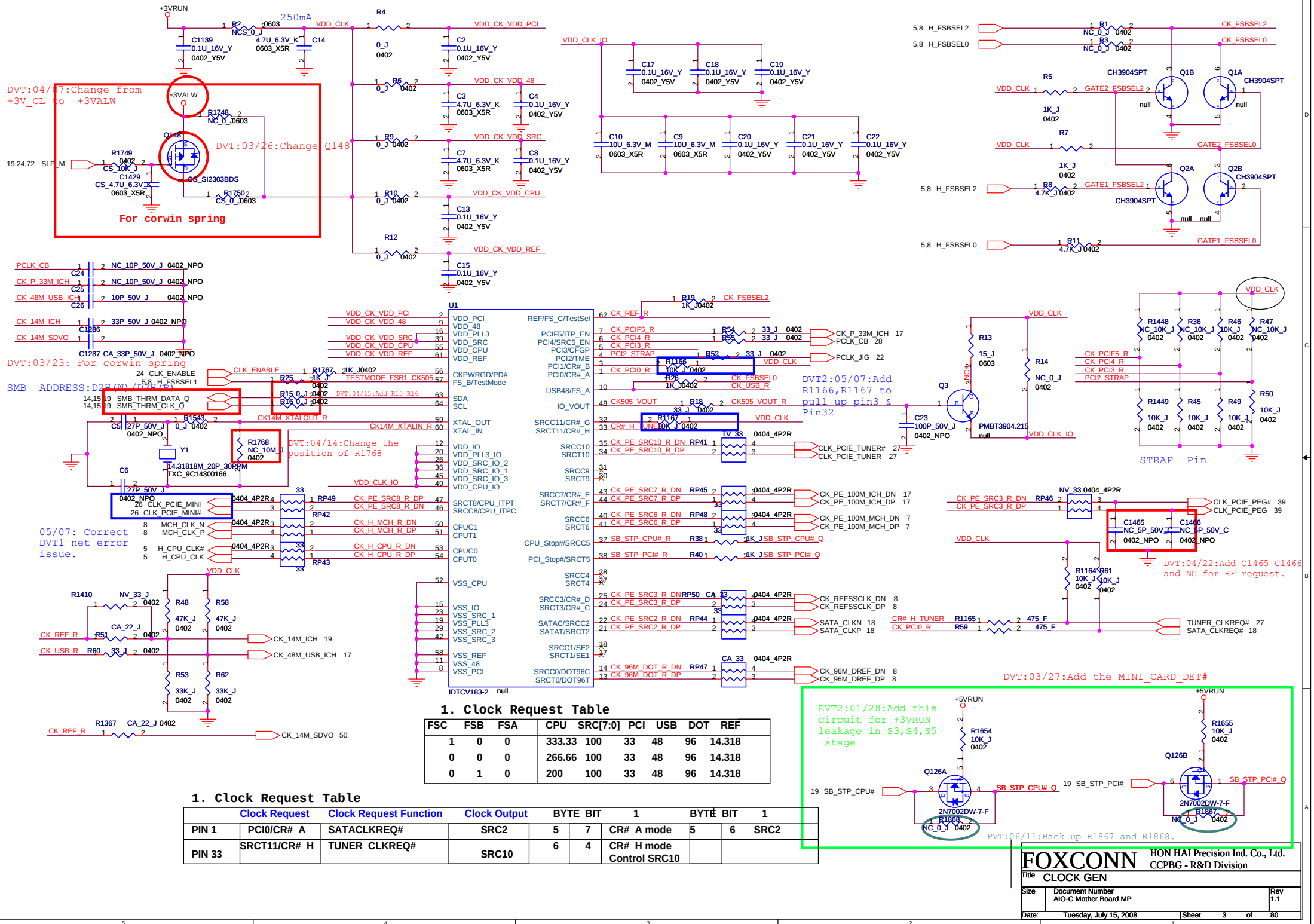
Title: Block Diagram(System)

Size	Document Number	Rev
A3	AIO-C Mother Board MP	1.1

Date: Tuesday, July 15, 2008 Sheet 2 of 80



1. Clock Request Table

FSC	FSB	FSA	CPU	SRC[7:0]	PCI	USB	DOT	REF
1	0	0	333.33	100	33	48	96	14.318
0	0	0	266.66	100	33	48	96	14.318
0	1	0	200	100	33	48	96	14.318

1. Clock Request Table

	Clock Request	Clock Request Function	Clock Output	BYTE	BIT	1	BYTE	BIT	1
PIN 1	PCI0/CR#_A	SATACLKREQ#	SRC2	5	7	CR#_A mode	5	6	SRC2
PIN 33	SRCT11/CR#_H	TUNER_CLKREQ#	SRC10	6	4	CR#_H mode Control SRC10			

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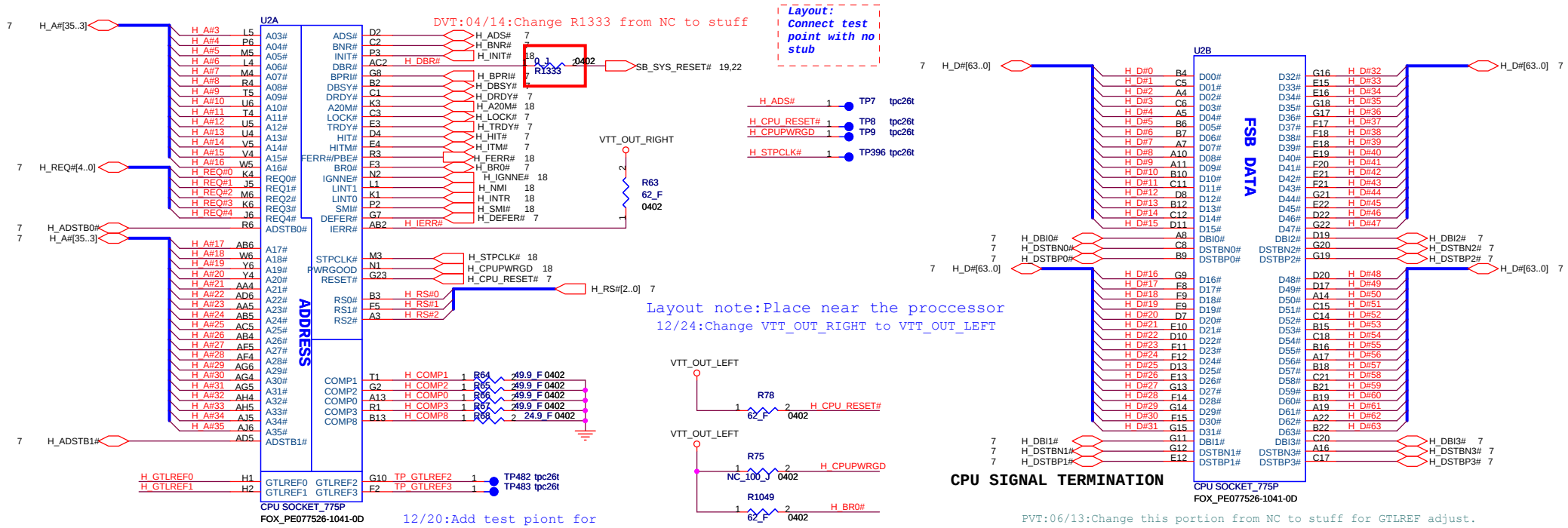
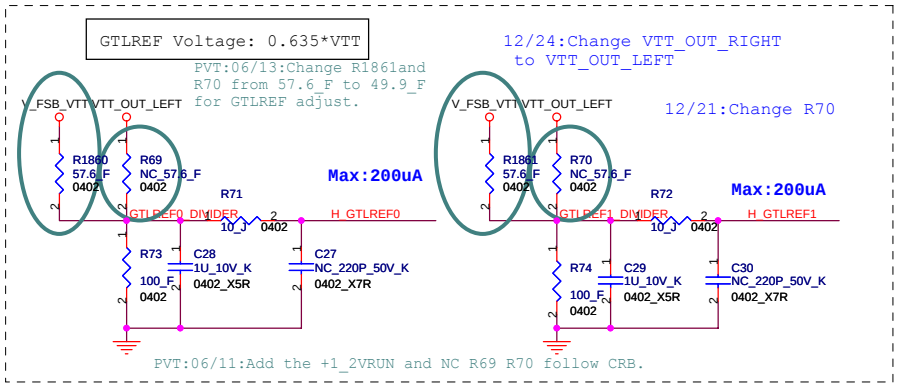
Title	CLOCK GEN	
Size	Document Number AIO-C Mother Board MP	Rev 1.1
Date: Tuesday, July 15, 2008	Sheet 3 of 80	

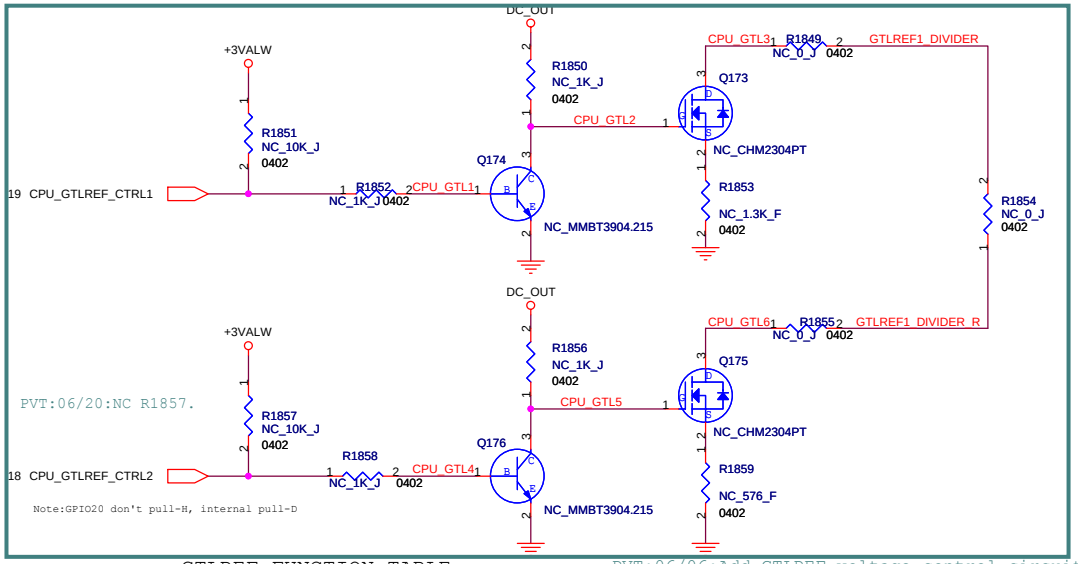




12/20:Delete H_GTLREF2 and H_GTLREF3 circuit

GTLREF Layout note:

1. voltage divider should be within 1.5 inches of the processor's GTLREF pin;
2. 220p Cap should be placed as close to the processor GTLREF pin as possible;
3. IC should be within 2.5 inches of the;
4. Trace width is 4 mils minimum at breakout and as should be as wide as possible between the breakout and the resistor divider network



GTLREF FUNCTION TABLE

CPU_GTLREF_CTRL2	CPU_GTLREF_CTRL1	Ratio Set
0	0	0.615 X VTT
0	1	0.63 X VTT
1	0	0.65 X VTT
1	1	0.67 X VTT

PVT:06/06:Add GTLREF voltage control circuit
PVT:06/20:NC GTLREF voltage control circuit

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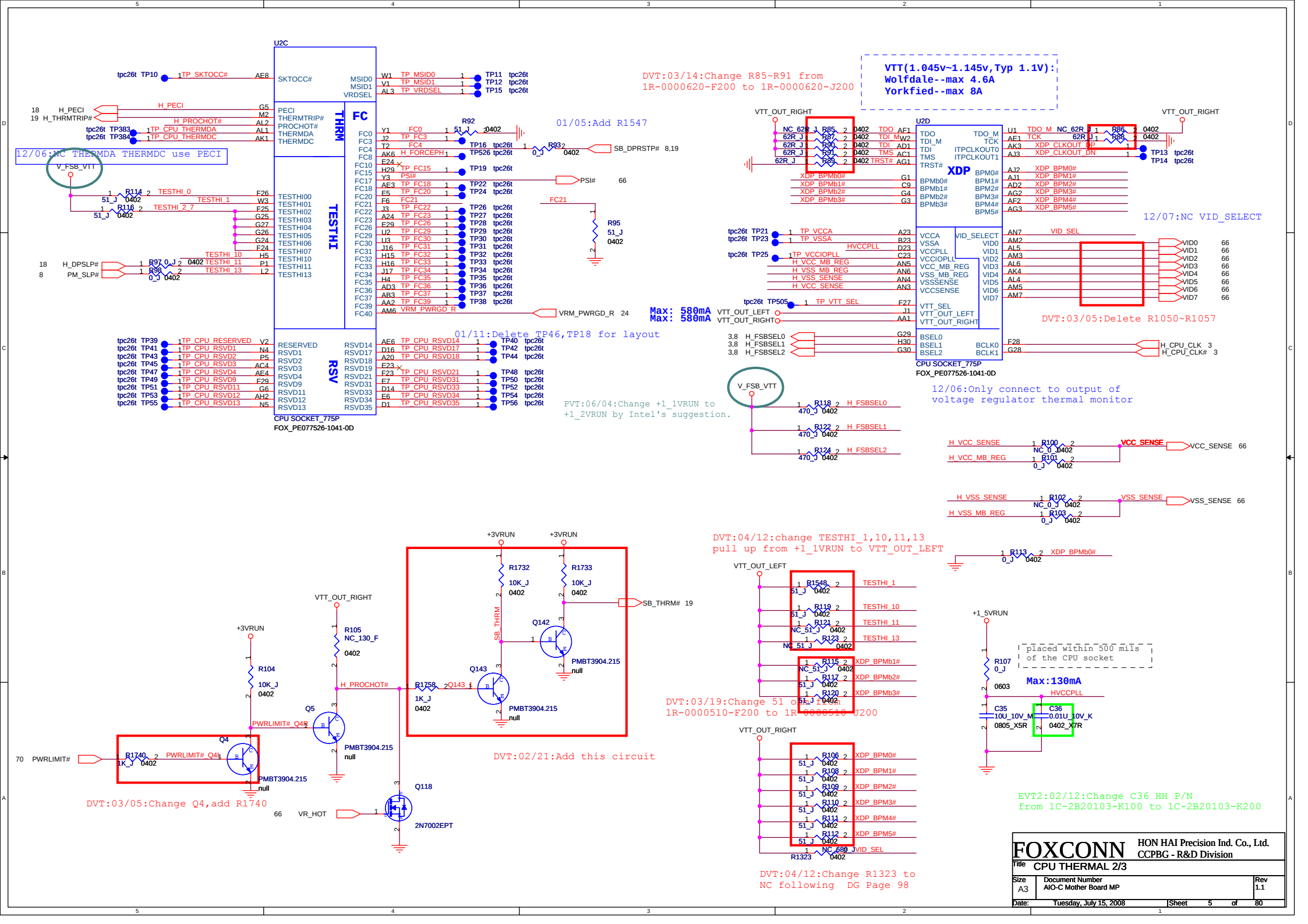
Title	CPU HOST 1/3	
Size	Document Number: AIO-C Mother Board MP	Rev: 1.1
Date: Tuesday, July 15, 2008	Sheet 4 of 80	


U2C
SKTOCC#
MSID0
MSID1
VRDSEL
PECI
THERMTRIP#
PROCHOT#
THERMDA
THERMDC
THRM
FC
TESTHI00
TESTHI01
TESTHI02
TESTHI03
TESTHI04
TESTHI05
TESTHI06
TESTHI07
TESTHI10
TESTHI11
TESTHI13
TESTHI
RESERVED
RSVD1
RSVD2
RSVD3
RSVD4
RSVD9
RSVD11
RSVD12
RSVD13
RSV
CPU SOCKET_775P
FOX_PE077526-1041-0D
12/06:NC THERMDA THERMDC use PECI
01/05:Add R1547
01/11:Delete TP46,TP18 for layout
PVT:06/04:Change +1_1VRUN to
+1_2VRUN by Intel's suggestion.
DVT:03/14:Change R85~R91 from
1R-0000620-F200 to 1R-0000620-J200
VTT(1.045v~1.145v,Typ 1.1V):
Wolfdale--max 4.6A
Yorkfied--max 8A
Max: 580mA
Max: 580mA
12/07:NC VID_SELECT
DVT:03/05:Delete R1050~R1057
12/06:Only connect to output of
voltage regulator thermal monitor
XDP
VID_SELECT
CPU SOCKET_775P
FOX_PE077526-1041-0D
DVT:04/12:change TESTHI_1,10,11,13
pull up from +1_1VRUN to VTT_OUT_LEFT
DVT:03/19:Change 51 ohm from
1R-0000510-F200 to 1R-0000510-J200
DVT:04/12:Change R1323 to
NC following DG Page 98
DVT:02/21:Add this circuit
DVT:03/05:Change Q4,add R1740
placed within 500 mils
of the CPU socket
Max:130mA
EVT2:02/12:Change C36 HH P/N
from 1C-2B20103-K100 to 1C-2B20103-K200
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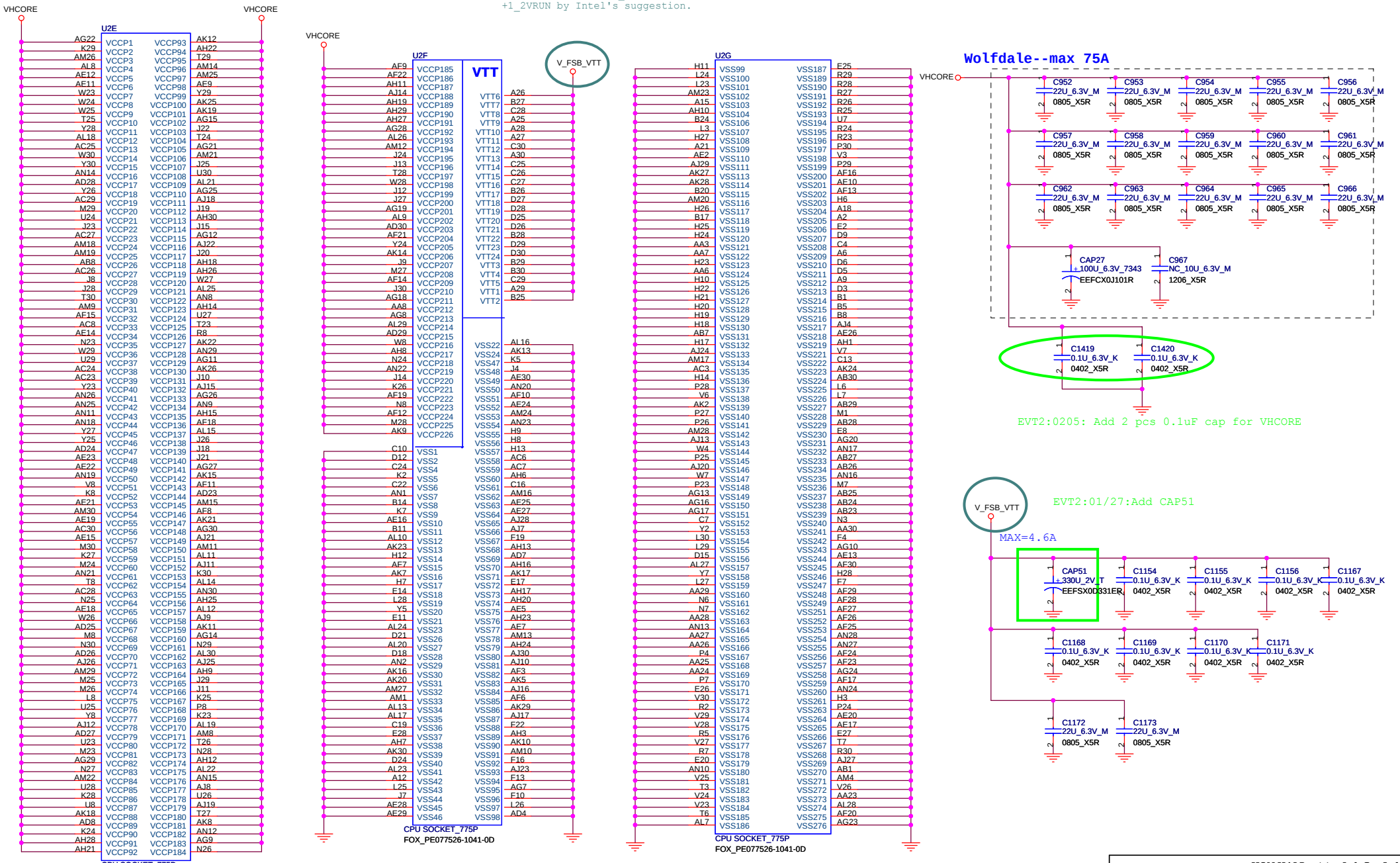
Title CPU THERMAL 2/3
Size A3
Document Number AIO-C Mother Board MP
Rev 1.1
Date: Tuesday, July 15, 2008
Sheet 5 of 80

VHCORE(0.85V-1.45V,VCC_BOOT=1.1V):
Wolfdale--max 75A
Yorkfied--max 125A

PVT:06/04:Change +1_1VRUN to
+1_2VRUN by Intel's suggestion.



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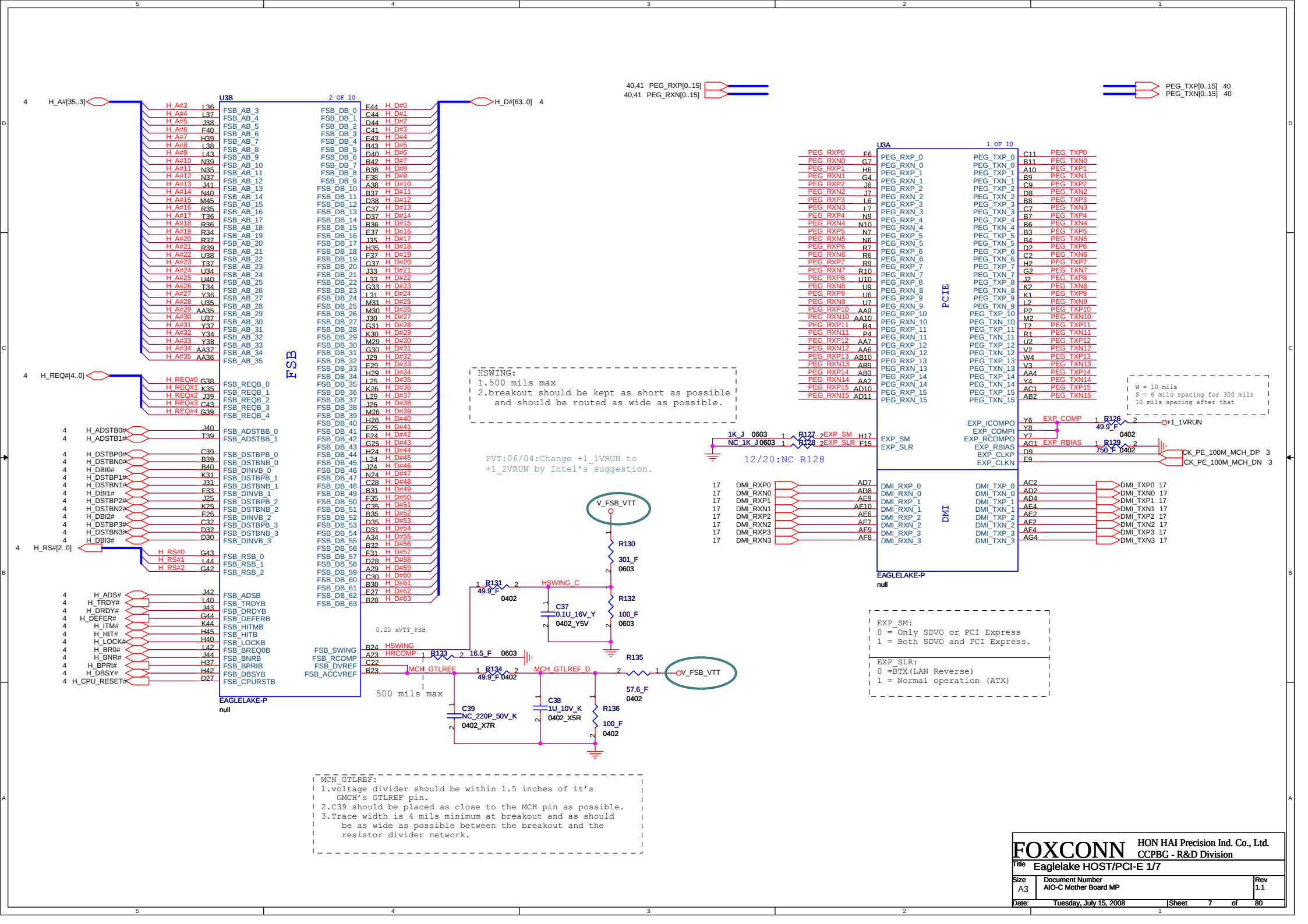
Title	CPU POWER 3/3	
Size A3	Document Number AIO-C Mother Board MP	Rev 1.1
Date: Tuesday, July 15, 2008	Sheet 6 of 80	


U3B
2 OF 10
FSB
EAGLELAKE-P
null
H_A#[35..3]
H_D#[63..0]
H_REQ#[4..0]
H_ADSTB0#
H_ADSTB1#
H_DSTBP0#
H_DSTBN0#
H_DBI0#
H_DSTBP1#
H_DSTBN1#
H_DBI1#
H_DSTBP2#
H_DSTBN2#
H_DBI2#
H_DSTBP3#
H_DSTBN3#
H_DBI3#
H_RS#[2..0]
H_ADS#
H_TRDY#
H_DRDY#
H_DEFER#
H_ITM#
H_HIT#
H_LOCK#
H_BR0#
H_BNR#
H_BPRI#
H_DBSY#
H_CPU_RESET#
FSB_SWING
FSB_RCOMP
FSB_DVREF
FSB_ACCVREF
40,41 PEG_RXP[0..15]
40,41 PEG_RXN[0..15]
PEG_TXP[0..15] 40
PEG_TXN[0..15] 40
U3A
1 OF 10
PCIE
EXP_ICOMPO
EXP_COMPI
EXP_RCOMPO
EXP_RBIAS
EXP_CLKP
EXP_CLKN
EXP_SM
EXP_SLR
EXP_COMP
EXP_RBIAS
+1_1VRUN
CK_PE_100M_MCH_DP 3
CK_PE_100M_MCH_DN 3
DMI
DMI_RXP0
DMI_RXN0
DMI_RXP1
DMI_RXN1
DMI_RXP2
DMI_RXN2
DMI_RXP3
DMI_RXN3
DMI_TXP0 17
DMI_TXN0 17
DMI_TXP1 17
DMI_TXN1 17
DMI_TXP2 17
DMI_TXN2 17
DMI_TXP3 17
DMI_TXN3 17
EAGLELAKE-P
null
HSWING:
1.500 mils max
2.breakout should be kept as short as possible
and should be routed as wide as possible.
PVT:06/04:Change +1_1VRUN to
+1_2VRUN by Intel's suggestion.
12/20:NC R128
W = 10 mils
S = 6 mils spacing for 300 mils
10 mils spacing after that
V_FSB_VTT
R130
301_F
0603
R131
49.9_F
0402
HSWING_C
C37
0.1U_16V_Y
0402_Y5V
R132
100_F
0603
0.25 xVTT_FSB
HSWING
HRCOMP
R133
16.5_F
0603
MCH_GTLREF
R134
49.9_F 0402
MCH_GTLREF_D
R135
57.6_F
0402
V_FSB_VTT
500 mils max
C39
NC_220P_50V_K
0402_X7R
C38
1U_10V_K
0402_X5R
R136
100_F
0402
EXP_SM:
0 = Only SDVO or PCI Express
1 = Both SDVO and PCI Express.
EXP_SLR:
0 =BTX(LAN Reverse)
1 = Normal operation (ATX)
MCH_GTLREF:
1.voltage divider should be within 1.5 inches of it's
GMCH's GTLREF pin.
2.C39 should be placed as close to the MCH pin as possible.
3.Trace width is 4 mils minimum at breakout and as should
be as wide as possible between the breakout and the
resistor divider network.
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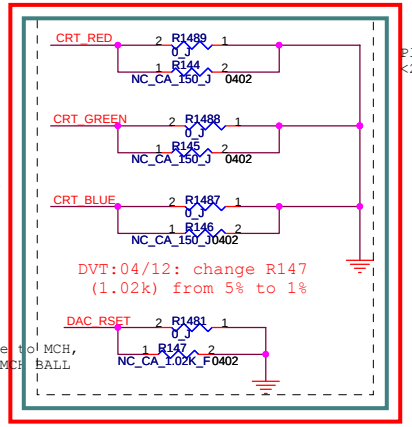
Title
Eaglelake HOST/PCI-E 1/7
Size
A3
Document Number
AIO-C Mother Board MP
Rev
1.1
Date:
Tuesday, July 15, 2008
Sheet
7
of
80

PVT:06/11:Back up CRT function:
when use CRT,stuff R144 R145
R146 R147 and NC R1489 R1488
R1487 R1481 in L sku;use the
default setting in H sku.

DVT:04/12: add option resistor
for H SKU and L SKU

PVT:06/02:Del R144 R145 R146 and R147 for
cancel CRT;Change R1489 R1488 R1487 and
R1481 from NV to normal stuff.



Place VGA RGB resistors close to MCH,
<250mils to MCH BALLs

DualX8_Enable:
2x8 PEG port Bifurcation:
0=2x8 PCIe Ports Enable
1=1x16 PCIe Port Enable

CEN:
Pulldown: Enable TCEN
Float: Disable TCEN

ITPM_ENB:
Pulldown: Enable TPM
Float: Disable TPM

Place close to MCH,
<500mil to MCH BALL

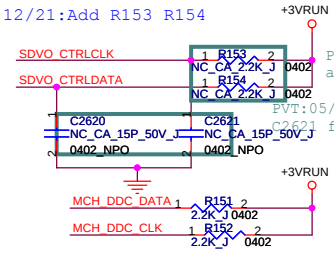
PVT:06/02:Del the R148 , R149,and the
signal ports for cancel CRT function

SDVO_CTRLDATA	L	SDVO DISABLED (DEFAULT INTERNAL PD)
SDVO_CTRLDATA	H	SDVO CARD PRESENT/PEG DISABLED

PVT:06/02:Del the
MCH_DDC_CLK&DATA port for
cancel CRT.

DVT:03/01:connect U3
pin AC30,
AD30,AE30,AF30 to GND

12/21:Add R153 R154



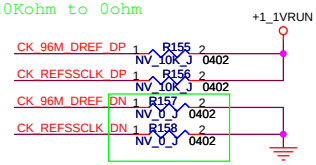
PVT:05/30:Change R153
and R154 from CA to NC.

PVT:05/28:Back up C2620 and
C2621 for black screen issue.

12/07:Change R148 R149
from 30 Ohm to 33 Ohm
Change R147 from 255 to 1K

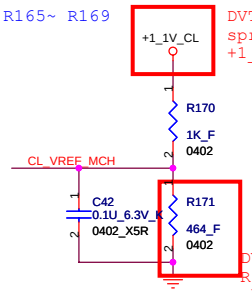
DVT:04/14: Mount R160 for
corwin spring.

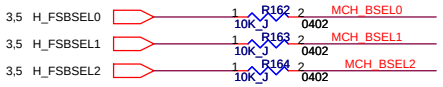
EVT2:01/22:Change R157 R158 from 10Kohm to 0ohm



12/23:Change R165~ R169

DVT:03/23: for corwin
spring:change from
+1_1VRUN to +1_1V_CL



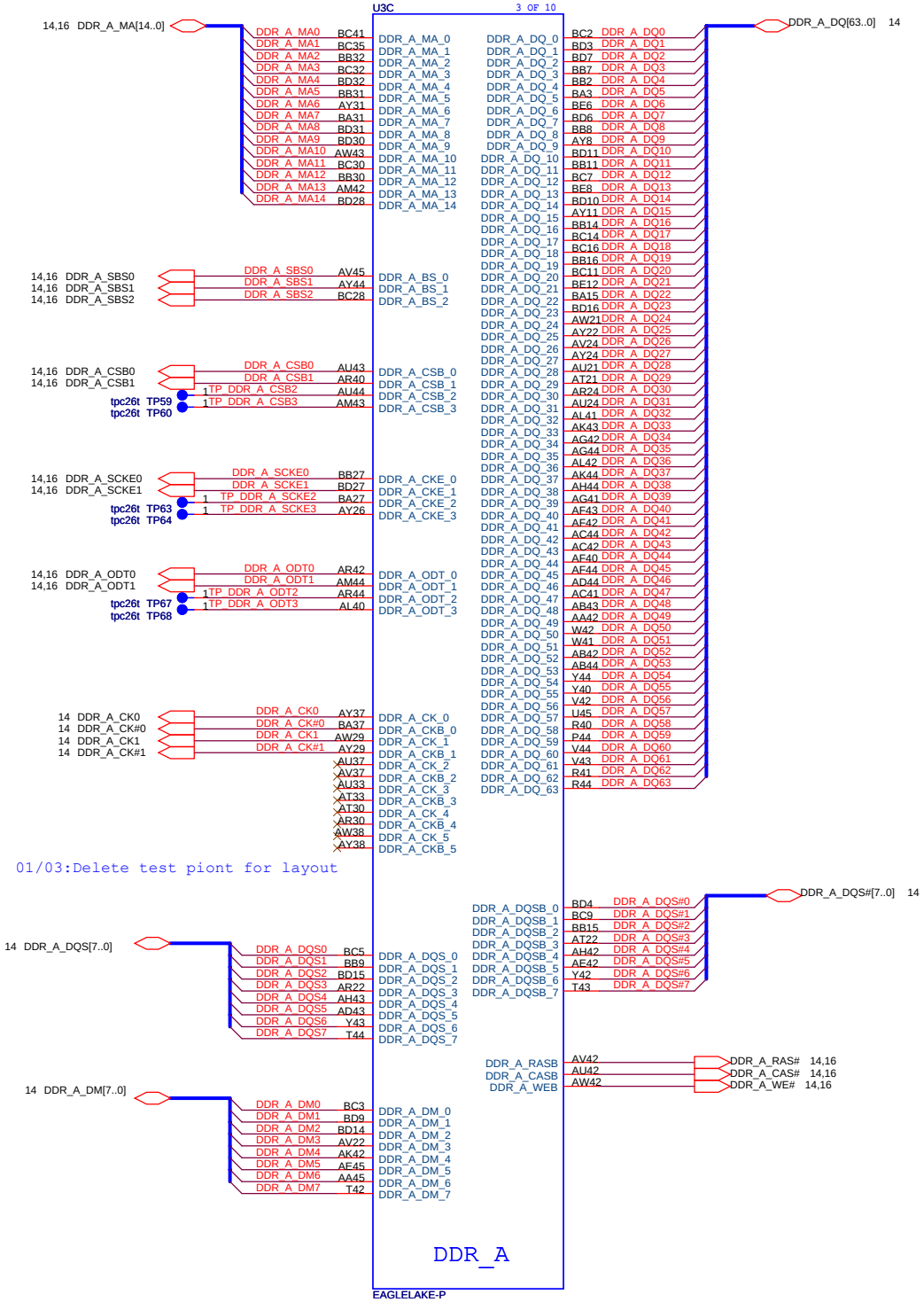


12/23:Change R162 R163 R164

DVT:02/20:change
R171 from 475
ohm to 464 ohm

MCH_CL_REF:
1.MCH_CL_REF=0.35V;
2.Trace width/Spacing: 4mil(min)/10mil(min.) for main route;
3.Breakout area: width>5mils, L<300mils;
4. 0.1 µF cap placed as close as possible to MCH_CL_REF pin.

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Eaglelake VGA/MISC 2/7	
Size	Document Number AIO-C Mother Board MP	Rev 1.1
Date: Tuesday, July 15, 2008	Sheet 8 of 80	



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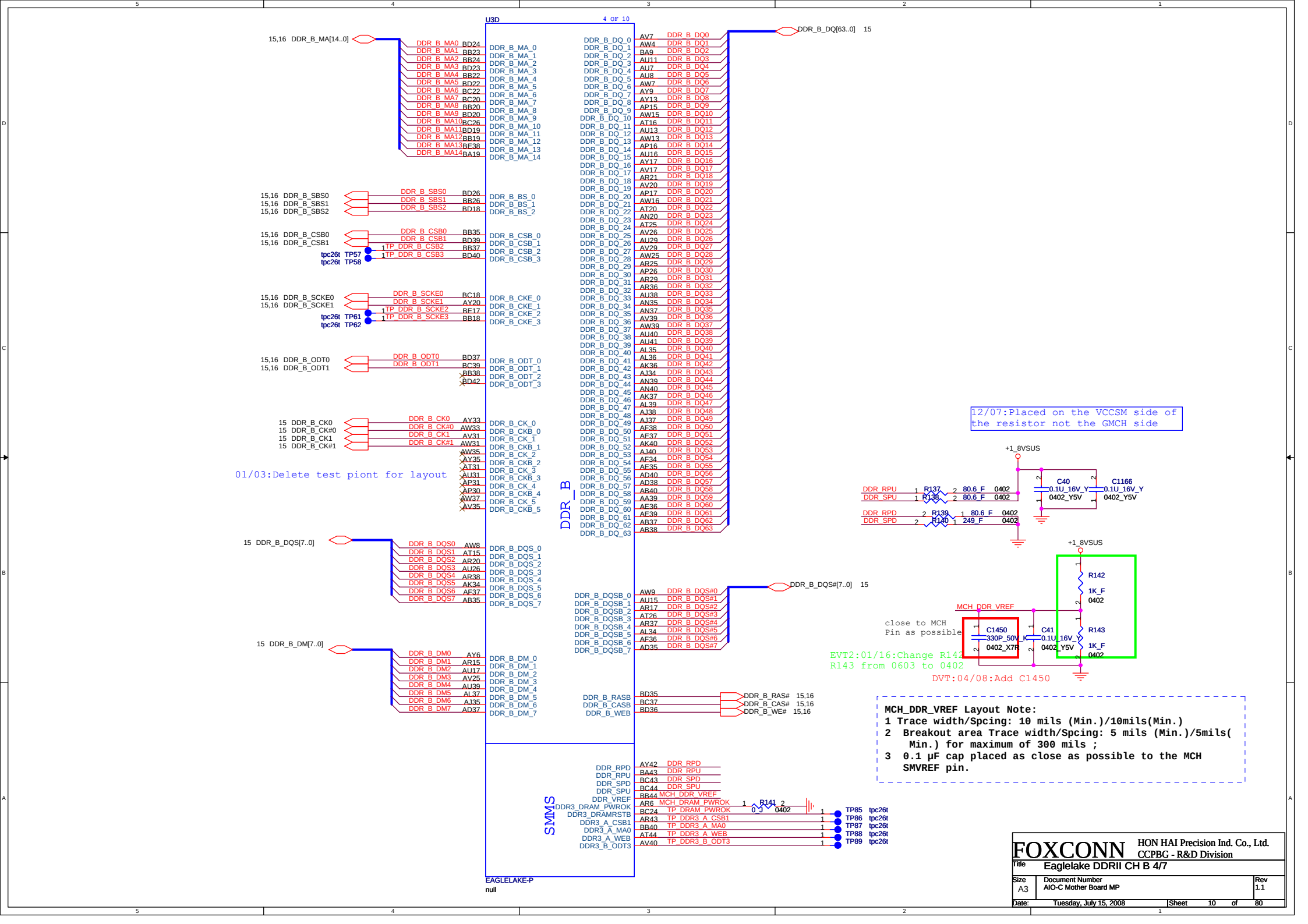
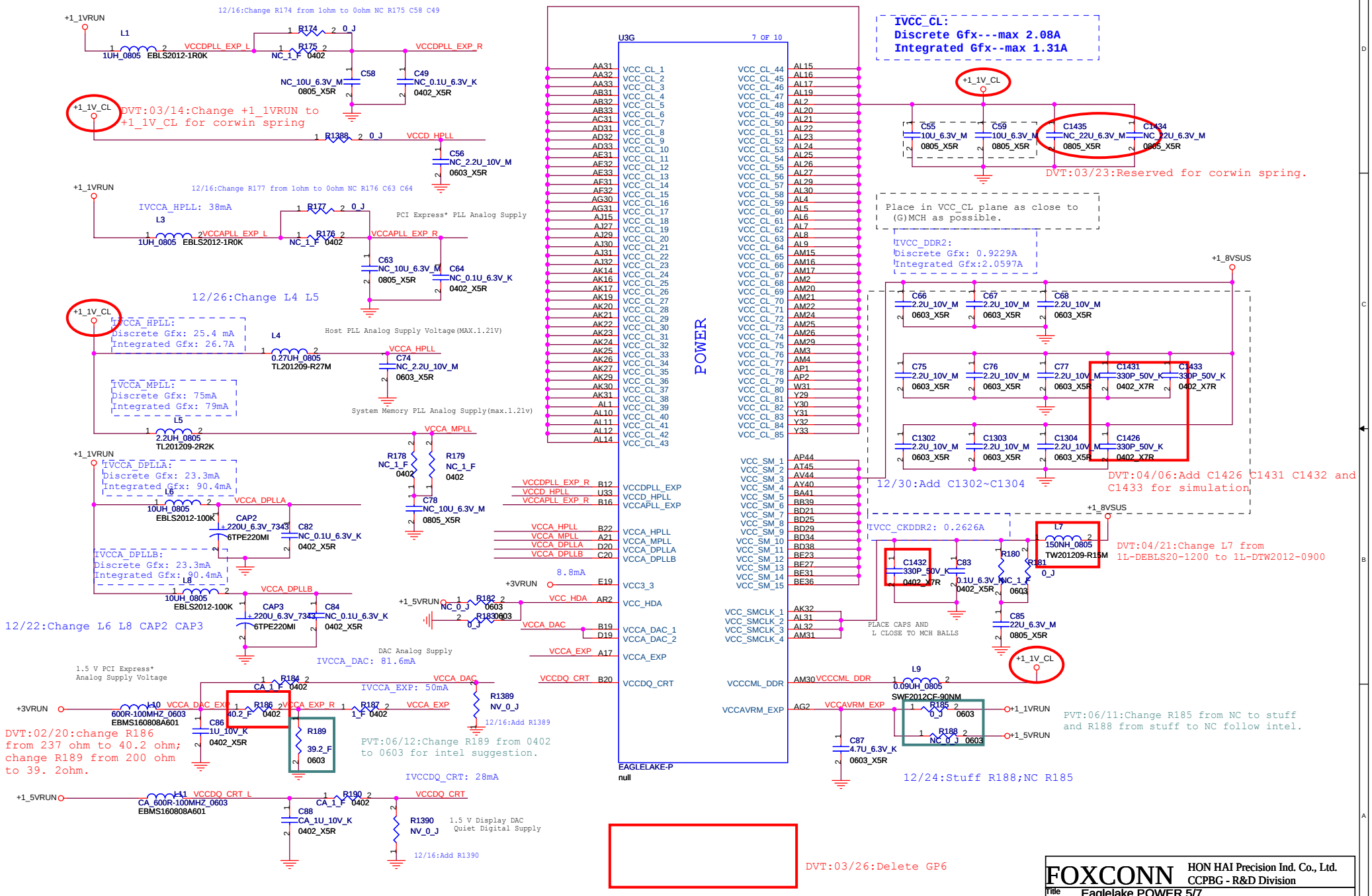
Title	Eaglelake DDRII CH A 3/7	
Size A3	Document Number AIO-C Mother Board MP	Rev 1.1
Date: Tuesday, July 15, 2008	Sheet 9 of 80	


U3D
4 OF 10
DDR_B
SMMS
EAGLELAKE-P
null
15,16 DDR_B_MA[14..0]
DDR_B_SBS0
DDR_B_SBS1
DDR_B_SBS2
DDR_B_CSB0
DDR_B_CSB1
TP_DDR_B_CSB2
TP_DDR_B_CSB3
tpc26t TP57
tpc26t TP58
DDR_B_SCKE0
DDR_B_SCKE1
TP_DDR_B_SCKE2
TP_DDR_B_SCKE3
tpc26t TP61
tpc26t TP62
DDR_B_ODT0
DDR_B_ODT1
15 DDR_B_CK0
15 DDR_B_CK#0
15 DDR_B_CK1
15 DDR_B_CK#1
01/03:Delete test piont for layout
15 DDR_B_DQS[7..0]
15 DDR_B_DM[7..0]
DDR_B_DQ[63..0] 15
DDR_B_DQS#[7..0] 15
DDR_B_RASB
DDR_B_CASB
DDR_B_WEB
DDR_B_RAS# 15,16
DDR_B_CAS# 15,16
DDR_B_WE# 15,16
DDR_RPD
DDR_RPU
DDR_SPD
DDR_SPU
DDR_VREF
DDR3_DRAM_PWROK
DDR3_DRAMRSTB
DDR3_A_CSB1
DDR3_A_MA0
DDR3_A_WEB
DDR3_B_ODT3
MCH_DDR_VREF
MCH_DRAM_PWROK
TP_DRAM_PWROK
TP_DDR3_A_CSB1
TP_DDR3_A_MA0
TP_DDR3_A_WEB
TP_DDR3_B_ODT3
R141 0 J 0402
TP85 tpc26t
TP86 tpc26t
TP87 tpc26t
TP88 tpc26t
TP89 tpc26t
12/07:Placed on the VCCSM side of the resistor not the GMCH side
+1_8VSUS
DDR_RPU R137 80.6_F 0402
DDR_SPU R138 80.6_F 0402
DDR_RPD R139 80.6_F 0402
DDR_SPD R140 249_F 0402
C40 0.1U_16V_Y 0402_Y5V
C1166 0.1U_16V_Y 0402_Y5V
R142 1K_F 0402
R143 1K_F 0402
C1450 330P_50V_K 0402_X7R
C41 0.1U_16V_Y 0402_Y5V
close to MCH
Pin as possible
EVT2:01/16:Change R142 R143 from 0603 to 0402
DVT:04/08:Add C1450
MCH_DDR_VREF Layout Note:
1 Trace width/Spcing: 10 mils (Min.)/10mils(Min.)
2 Breakout area Trace width/Spcing: 5 mils (Min.)/5mils(Min.) for maximum of 300 mils ;
3 0.1 µF cap placed as close as possible to the MCH SMVREF pin.
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title Eaglelake DDRII CH B 4/7
Size A3
Document Number AIO-C Mother Board MP
Rev 1.1
Date: Tuesday, July 15, 2008
Sheet 10 of 80



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Eaglelake POWER 5/7	
Size A3	Document Number AIO-C Mother Board MP	Rev 1.1
Date: Tuesday, July 15, 2008	Sheet 11 of 80	

For GMCH CORE POWER +1_1VRUN

12/31:Delete CAP49

VCC(MAX 1.21V):
Discrete Gfx---max 18.51A
Integrated Gfx--max 26.40A

CAP47 330U_2V_T EEFSX0D331ER
CAP48 330U_2V_T EEFSX0D331ER
C43 10U_6.3V_M 0805_X5R
C44 10U_6.3V_M 0805_X5R
C45 10U_6.3V_M 0805_X5R

12/20:Add CAP47 CAP48

C50 1U_10V_K 0603_X5R
C57 1U_10V_K 0603_X5R
C51 1U_10V_K 0603_X5R
C52 1U_10V_K 0603_X5R
C53 1U_10V_K 0603_X5R
C54 1U_10V_K 0603_X5R

Backside cap sites, placed directly underneath the VCC_Core center-array pins, with sufficient via connections

C60 22U_6.3V_M 0805_X5R
C61 22U_6.3V_M 0805_X5R
C62 22U_6.3V_M 0805_X5R

C65 10U_6.3V_M 0805_X5R
C69 10U_6.3V_M 0805_X5R
C70 10U_6.3V_M 0805_X5R
C71 1U_10V_K 0603_X5R
C72 1U_10V_K 0603_X5R
C73 1U_10V_K 0603_X5R

Top-side caps. Place along the (G)MCH edge.

C1424 0.1U_6.3V_K 0402_X5R
C1421 0.1U_6.3V_K 0402_X5R
C1422 0.1U_6.3V_K 0402_X5R
C1423 0.1U_6.3V_K 0402_X5R

EVT2:0205: Add 4 pcs 0.1uF cap for +1_1VRUN

+1_1VRUN

U3F 6 OF 10

POWER

VCC_1 VCC_2 VCC_3 VCC_4 VCC_5 VCC_6 VCC_7 VCC_8 VCC_9 VCC_10 VCC_11 VCC_12 VCC_13 VCC_14 VCC_15 VCC_16 VCC_17 VCC_18 VCC_19 VCC_20 VCC_21 VCC_22 VCC_23 VCC_24 VCC_25 VCC_26 VCC_27 VCC_28 VCC_29 VCC_30 VCC_31 VCC_32 VCC_33 VCC_34 VCC_35 VCC_36 VCC_37 VCC_38 VCC_39 VCC_40 VCC_41 VCC_42 VCC_43 VCC_44 VCC_45 VCC_46 VCC_47 VCC_48 VCC_49 VCC_50 VCC_51 VCC_52 VCC_53 VCC_54 VCC_55 VCC_56 VCC_57 VCC_58 VCC_59 VCC_60 VCC_61 VCC_62 VCC_63 VCC_64 VCC_65 VCC_66 VCC_67 VCC_68 VCC_69 VCC_70 VCC_71 VCC_72 VCC_73 VCC_74 VCC_75 VCC_76 VCC_77 VCC_78 VCC_79 VCC_80 VCC_81 VCC_82 VCC_83 VCC_84 VCC_85 VCC_86 VCC_87 VCC_88 VCC_89 VCC_90 VCC_91 VCC_92 VCC_93 VCC_94 VCC_95 VCC_96 VCC_97 VCC_98

EAGLELAKE-P
null

VCC_EXP_1 VCC_EXP_2 VCC_EXP_3 VCC_EXP_4 VCC_EXP_5 VCC_EXP_6 VCC_EXP_7 VCC_EXP_8 VCC_EXP_9 VCC_EXP_10 VCC_EXP_11 VCC_EXP_12 VCC_EXP_13 VCC_EXP_14 VCC_EXP_15 VCC_EXP_16 VCC_EXP_17 VCC_EXP_18 VCC_EXP_19 VCC_EXP_20 VCC_EXP_21 VCC_EXP_22 VCC_EXP_23 VCC_EXP_24 VCC_EXP_25 VCC_EXP_26 VCC_EXP_27 VCC_EXP_28 VCC_EXP_29 VCC_EXP_30 VCC_EXP_31 VCC_EXP_32 VCC_EXP_33 VCC_EXP_34 VCC_EXP_35 VCC_EXP_36 VCC_EXP_37 VCC_EXP_38

+1_1VRUN

PCI Express* and DMI Supply

C46 2.2U_10V_Y 0603_Y5V
C47 2.2U_10V_Y 0603_Y5V
C48 2.2U_10V_Y 0603_Y5V

Place in the VCC_EXP plane as close the (G)MCH as possible

IVCC_EXP:
Discrete Gfx---max 3.939A
Integrated Gfx--max 1.2485A

VTT_FSB(MAX 1.32V):
Discrete Gfx---max 1.009A
Integrated Gfx--max 0.9092A

System Bus Input Voltage

VTT_FSB_1 VTT_FSB_2 VTT_FSB_3 VTT_FSB_4 VTT_FSB_5 VTT_FSB_6 VTT_FSB_7 VTT_FSB_8 VTT_FSB_9 VTT_FSB_10 VTT_FSB_11 VTT_FSB_12 VTT_FSB_13 VTT_FSB_14 VTT_FSB_15 VTT_FSB_16 VTT_FSB_17 VTT_FSB_18 VTT_FSB_19 VTT_FSB_20 VTT_FSB_21 VTT_FSB_22 VTT_FSB_23 VTT_FSB_24 VTT_FSB_25 VTT_FSB_26 VTT_FSB_27 VTT_FSB_28 VTT_FSB_29 VTT_FSB_30 VTT_FSB_31 VTT_FSB_32 VTT_FSB_33 VTT_FSB_34 VTT_FSB_35

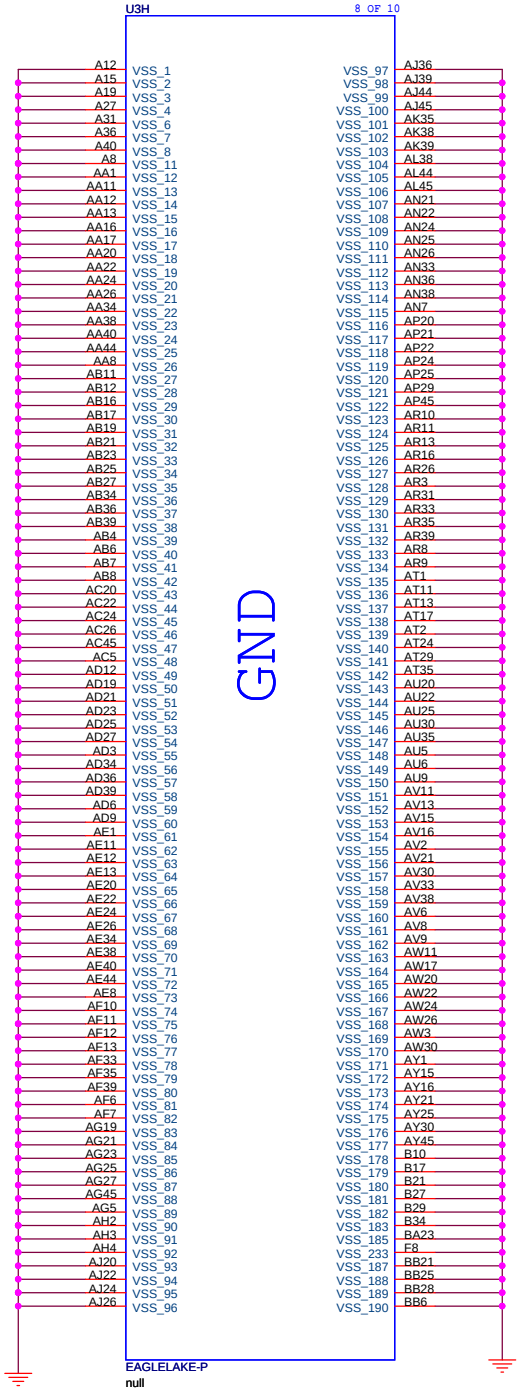
V_FSB_VTT

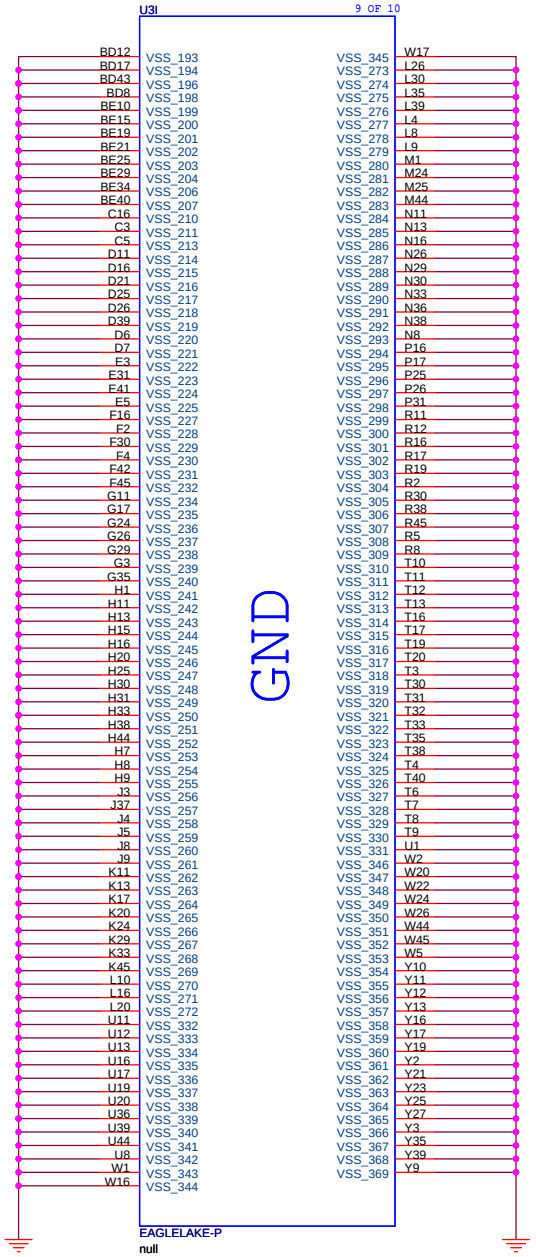
PVT:06/04:Change +1_1VRUN to +1_2VRUN by Intel's suggestion.

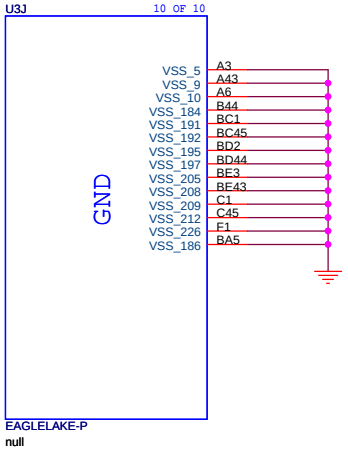
C79 2.2U_10V_Y 0603_Y5V
C80 2.2U_10V_Y 0603_Y5V
C81 2.2U_10V_Y 0603_Y5V

as close to the (G)MCH as possible(100mils from the package.)

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Eaglelake POWER 6/7	
Size A3	Document Number AIO-C Mother Board MP	Rev 1.1
Date: Tuesday, July 15, 2008	Sheet 12 of 80	







FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Eaglelake GND 7/7	
Size A3	Document Number AIO-C Mother Board MP	Rev 1.1
Date: Tuesday, July 15, 2008	Sheet 13 of 80	

1.8V per DIMM=4.06A

+1_8VSUS

+1_8VSUS

DDR2_VREF

DDR2_VREF

C89 0.1U_16V_M_B 0402

C90 2.2U_10V_M 0603_X5R

0.1 µF and 2.2 µF placed close to VREF pins

CN1

SMDFIX1 SMDFIX2

DDR_A_DM[7..0] 9
DDR_A_DQ[63..0] 9
DDR_A_DQS[7..0] 9
DDR_A_DQS#[7..0] 9
DDR_A_MA[14..0] 9,16

DDR2 SDRAM SO-DIMM (200P)

4 mm

DDR_A_CK0 9
DDR_A_CK#0 9

DDR2_EXTTS#0 1 TP455 tpc26t

DDR_A_SCKE1 9,16

DDR_A_SBS1 9,16
DDR_A_RAS# 9,16
DDR_A_CSB0 9,16

DDR_A_ODT0 9,16

DDR_A_CK1 9
DDR_A_CK#1 9

9,16 DDR_A_SCKE0

9,16 DDR_A_SBS2

9,16 DDR_A_SBS0
9,16 DDR_A_WE#

9,16 DDR_A_CAS#
9,16 DDR_A_CSB1

9,16 DDR_A_ODT1

DVT:03/26:Delete the GAP PJ26

03/11
Reserved,need to
Open to support
corwin spring

DVT:03/23: For corwin spring

3,15,19 SMB_THRM_DATA_Q
3,15,19 SMB_THRM_CLK_Q

+3VRUN

R1759 2.2K_J 0402 NCS_0_J

+3_3V_CD

R1760 2.2K_J 0402 CS_0_J

C98 2.2U_10V_M 0603_X5R

C97 0.1U_16V_Y 0402_Y5V

For corwin spring

SMBus Address: A0H(W)/A1H(R)

SA0_DIM0 R195 2 10K_J 1 0402

SA1_DIM0 R196 2 10K_J 1 0402

Place DIMM_0 near GMCH

DDR2_200P
FOX_AS0A426-N2SN-7F

DIMM_0

DVT:03/26:Delete the R197 and it's power DDRDIMM_VREF

+1_8VSUS

DDR2_VREF

(20 mil)

R1727 1K_F 0402

R1728 1K_F 0402

C109 0.1U_16V_M_B 0402

C149 NC_2.2U_10V_Y_Y 0603

DVT:04/09:Reserved C149 for sinulation.

DVT:03/07:NC R197,stuff R1727,R1728

Place these Caps near So-DIMM0

+1_8VSUS

C99 2.2U_10V_Y_Y 0603

C100 2.2U_10V_Y_Y 0603

C101 2.2U_10V_Y_Y 0603

C102 2.2U_10V_Y_Y 0603

C103 2.2U_10V_Y_Y 0603

Place these Caps near So-DIMM0

+1_8VSUS

C110 0.1U_6.3V_K 0402_X5R

C111 0.1U_6.3V_K 0402_X5R

C112 0.1U_6.3V_K 0402_X5R

C113 0.1U_6.3V_K 0402_X5R

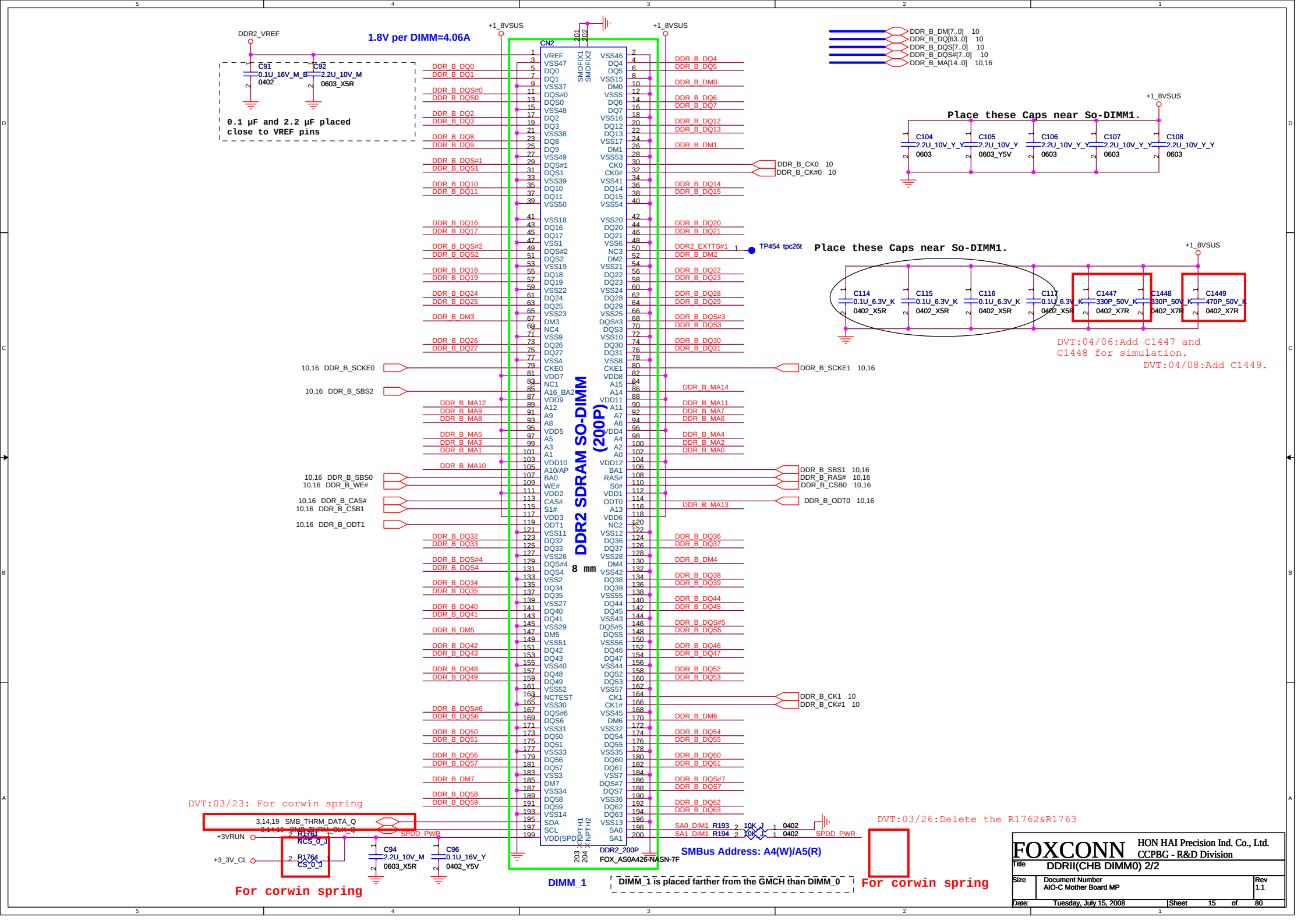
C1436 330P_50V_K 0402_X7R

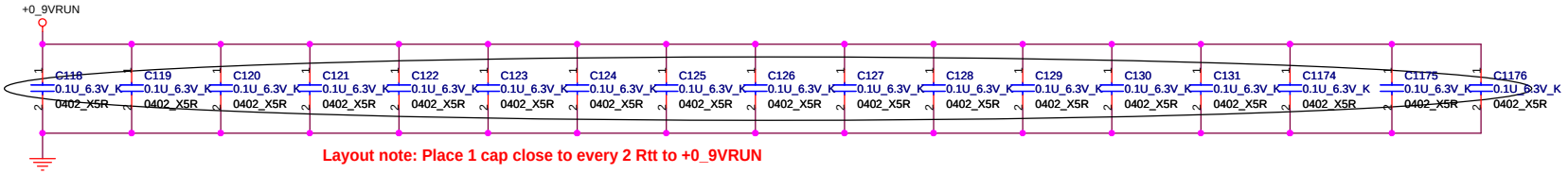
C1446 330P_50V_K 0402_X7R

DVT:04/06:Add C1436 and C1446 for simulation.

12/15:Change C110~C117

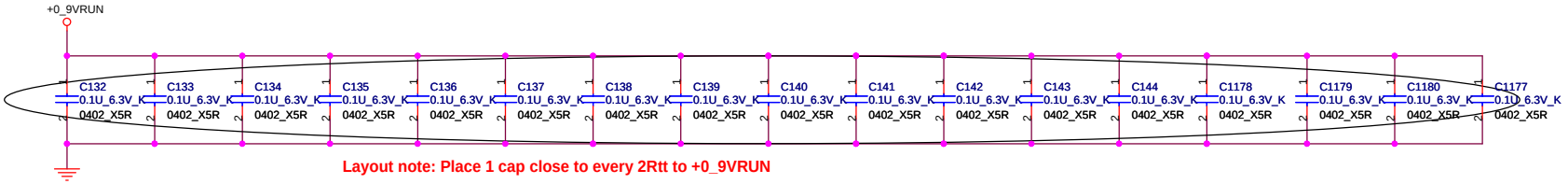
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	DDRII(CHA DIMM0) 1/2	
Size A3	Document Number AIO-C Mother Board MP	Rev 1.1
Date: Tuesday, July 15, 2008	Sheet 14 of 80	


DDR2_VREF
1.8V per DIMM=4.06A
+1_8VSUS
C91
0.1U_16V_M_B
0402
C92
2.2U_10V_M
0603_X5R
0.1 µF and 2.2 µF placed
close to VREF pins
CN2
DDR2 SDRAM SO-DIMM (200P)
8 mm
DDR2_200P
FOX_AS0A426-NASN-7F
DDR_B_DM[7..0] 10
DDR_B_DQ[63..0] 10
DDR_B_DQS[7..0] 10
DDR_B_DQS#[7..0] 10
DDR_B_MA[14..0] 10,16
Place these Caps near So-DIMM1.
C104 2.2U_10V_Y_Y 0603
C105 2.2U_10V 0603_Y5V
C106 2.2U_10V_Y_Y 0603
C107 2.2U_10V_Y_Y 0603
C108 2.2U_10V_Y_Y 0603
DDR_B_CK0 10
DDR_B_CK#0 10
TP454 tpc26t
DDR2_EXTTS#1
Place these Caps near So-DIMM1.
C114 0.1U_6.3V_K 0402_X5R
C115 0.1U_6.3V_K 0402_X5R
C116 0.1U_6.3V_K 0402_X5R
C117 0.1U_6.3V_K 0402_X5R
C1447 330P_50V_K 0402_X7R
C1448 330P_50V_K 0402_X7R
C1449 470P_50V_K 0402_X7R
DVT:04/06:Add C1447 and
C1448 for simulation.
DVT:04/08:Add C1449.
DDR_B_SCKE0 10,16
DDR_B_SCKE1 10,16
DDR_B_SBS2 10,16
DDR_B_SBS0 10,16
DDR_B_WE# 10,16
DDR_B_CAS# 10,16
DDR_B_CSB1 10,16
DDR_B_ODT1 10,16
DDR_B_SBS1 10,16
DDR_B_RAS# 10,16
DDR_B_CSB0 10,16
DDR_B_ODT0 10,16
DDR_B_CK1 10
DDR_B_CK#1 10
DVT:03/23: For corwin spring
3,14,19 SMB_THRM_DATA_Q
3,14,19 SMB_THRM_CLK_Q
+3VRUN
+3_3V_CL
R1761 NCS_0_J
R1764 CS_0_J
C94 2.2U_10V_M 0603_X5R
C96 0.1U_16V_Y 0402_Y5V
SPDD_PWR
For corwin spring
SA0_DIM1 R193 10K_J 0402
SA1_DIM1 R194 10K_J 0402
SMBus Address: A4(W)/A5(R)
DVT:03/26:Delete the R1762&R1763
For corwin spring
DIMM_1
DIMM_1 is placed farther from the GMCH than DIMM_0
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title DDRII(CHB DIMM0) 2/2
Size
Document Number AIO-C Mother Board MP
Rev 1.1
Date: Tuesday, July 15, 2008
Sheet 15 of 80



Layout note: Place 1 cap close to every 2 Rtt to +0_9VRUN

12/15:Change these caps



Layout note: Place 1 cap close to every 2Rtt to +0_9VRUN

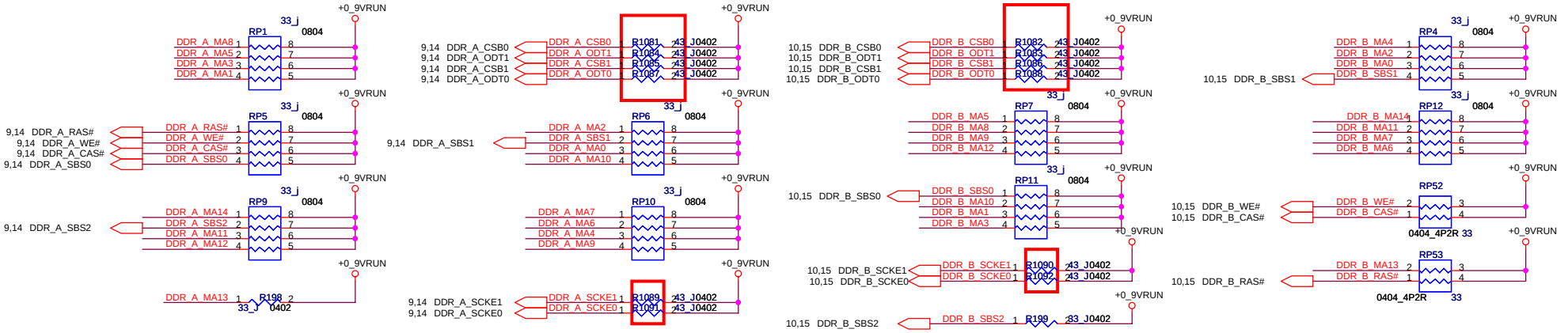
9,14 DDR_A_MA[14..0]

10,15 DDR_B_MA[14..0]

12/21:Change RP1 RP5 RP9 RP6 RP10 RP7 RP11 RP4 RP8 RP12

DVT:03/13:Change 43 ohm resistor from _F to _J

01/06:Delete RP8;Add RP52 RP53



12/05:Change PR1 PR5 PR6 PR9 PR10 from 56 Ohm to 33 Ohm
Change PR2 fom 56 Ohm to 43 Ohm *4R
Change PR13 from 56 Ohm to 43 Ohm *2R
Change R198 from 56 Ohm to 33Ohm

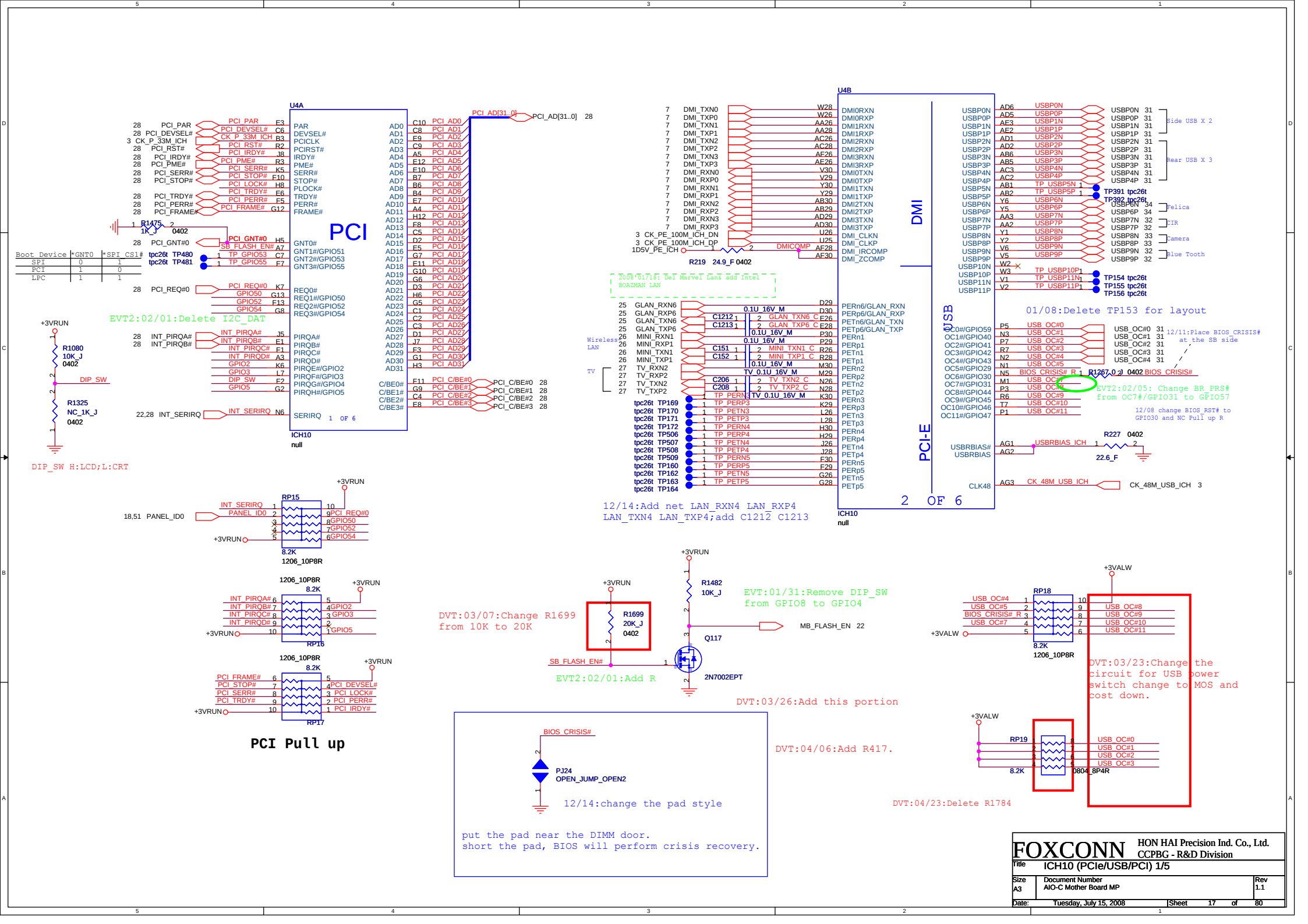
12/05:Change PR4 PR7 PR8 PR11 PR12 from 56 Ohm to 33 Ohm
Change PR3 fom 56 Ohm to 43 Ohm *4R
Change PR14 from 56 Ohm to 43 Ohm *2R
Change R199 from 56 Ohm to 33 Ohm

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: DDRII Termination

Size	Document Number	Rev
A3	AIO-C Mother Board MP	1.1

Date: Tuesday, July 15, 2008 Sheet 16 of 80


U4A
PCI
ICH10
null
1 OF 6
U4B
DMI
PCI-E
USB
2 OF 6
ICH10
null
EVT2:02/01:Delete I2C_DAT
DIP_SW H:LCD;L:CRT
2008/01/18: Del Marvel Lan& add Intel BOAZMAN LAN
01/08:Delete TP153 for layout
12/11:Place BIOS_CRISIS# at the SB side
EVT2:02/05: Change BR_PRS# from OC7#/GPIO31 to GPIO57
12/08 change BIOS_RST# to GPIO30 and NC Pull up R
12/14:Add net LAN_RXN4 LAN_RXP4 LAN_TXN4 LAN_TXP4;add C1212 C1213
DVT:03/07:Change R1699 from 10K to 20K
EVT:01/31:Remove DIP_SW from GPIO8 to GPIO4
EVT2:02/01:Add R
DVT:03/26:Add this portion
DVT:04/06:Add R417.
DVT:04/23:Delete R1784
DVT:03/23:Change the circuit for USB power switch change to MOS and cost down.
PCI Pull up
12/14:change the pad style
put the pad near the DIMM door.
short the pad, BIOS will perform crisis recovery.
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
ICH10 (PCIe/USB/PCI) 1/5
Size A3
Document Number AIO-C Mother Board MP
Rev 1.1
Date: Tuesday, July 15, 2008
Sheet 17 of 80

PVT:06/04:Change +1_1VRUN to
+1_2VRUN by Intel's suggestion.

V_FSB_VTT
R220 62_F 0402 H_FERR#
+3VALW
R1416 10K_J POWER_LED#
R1537 NC_10K_J ICH_BM_BUSY_R
R1724 NC_10K_J HW_POP_MUTE_ICH
+3VRUN
R1717 10K_J 0402 GPIO49
R223 10K_J SB_RCIN#
R224 10K_J SB_A20GATE
R226 NC_10K_J SB_SST
R225 10K_J 0402 FAN1_TACH_R
R1172 10K_J 0402 FAN2_TACH_R
R1173 0402 10K_J FAN3_TACH_R

FAN3_TACH_R
FAN2_TACH_R
FAN1_TACH_R
C145 1500P_25V_K 0402_X7R
C146 1500P_25V_K 0402_X7R
C147 1500P_25V_K 0402_X7R

Layout note: place these Cap close to ICH10 ball.

EVT2:0205: Reserve pull up for HW_POP_MUTE_ICH

EVT2:0205: add pull up for GPIO49

EVT2:02/12: Stuff R203,R206

DVT:02/20:Remove BL_OFF#

DVT:04/18:Change GPIO27 to BT_ON

DVT:04/18:Remove WLAN_EN# to GPIO11

DVT:04/20:Add R1553.

PVT:06/06:Add CPU_GTLREF_CTRL2 for adding GTLREF voltage control circuit

PVT:06/04:Add Q172 R1657 and NC R1521 for 3/5VRUN leakage.

+5VRUN
R1657 10K_J 0402
Q172
19 ICH_BM_BUSY
ICH_BM_BUSY_R
2N7002EPT
R1521 NC_0_J 0402

DVT:03/07:Connect CL_VREF_ICH from +3VRUN to +3_3V_CL for Corwin Spring

DVT：04/23 Mount R1766 and no mount R1765 to support Wake up on Intel LAN

+3VRUN +3_3V_CL
R1765 NC_0_J 0402
R1766 0_J 0402
R217 3.24K_F 0603 0.405V
CL_VREF_ICH
R218 453_F 0603
C148 0.1U_16V_Y 0402_Y5V

PVT:06/09:Change R217 from 3.24K to 3.3K for system voltage fail.

PVT:06/13:Change the R217 back to 3.24K.

12/27:Add CN46

+3VRUN
R1407 4.7K_J 0402
CN46
FLASH_STRAP_SB
HEADER_2P
FOX_HB24021

U4C
null
ICH10

HOST: H_A20M# AJ28, H_FERR# AJ27, H_IGNNE# AC22, H_INIT# AE23, H_INTR AH27, H_NMI AE24, H_SMI# AH26, H_STPCLK# AJ29, SB_RCIN# L3, SB_A20GATE P8, H_CPUPWRGD AD23, H_DPSLP# AE24, TP_INIT3_3V# M3 (tpc26t TP128)

CL: H_CL_CLK0 G22, H_CL_DATA0 H21, H_CL_RST0# G20, CL_VREF_ICH C27

IQST: FAN1_PWM AJ21, FAN2_PWM AJ22, FAN3_PWM AK22, FAN1_TACH AH21, FAN2_TACH AK21, FAN3_TACH AH22, SYS_ID5 AK23, SB_SST C19, H_PECI AC23

GPIO: POWER_LED# F16, GPIO49 AJ25, TP_GPIO34 AH5, FLASH_STRAP_SB AF6, TP_GPIO32 K2, HW_POP_MUTE_ICH G18, BT_ON A11, CPU_GTLREF_CTRL2 AE5, TP_GPIO18 K1, WLAN_BT_SW# A19, ICH_BM_BUSY_R A9

SATA: SATA0RXN AK17, SATA0RXP AJ17, SATA0TXN AK19, SATA0TXP AJ19, SATA1RXN AJ15, SATA1RXP AK15, SATA1TXN AH16, SATA1TXP AF16, SATA2RXN AJ13, SATA2RXP AK13, SATA2TXN AH14, SATA2TXP AF14, SATA3RXN AJ11, SATA3RXP AK11, SATA3TXN AF12, SATA3TXP AH12, SATA4RXN AJ9, SATA4RXP AK9, SATA4TXN AF10, SATA4TXP AH9, SATA5RXN AJ7, SATA5RXP AK7, SATA5TXN AF8, SATA5TXP AH7, SATA_CLKN AF18, SATA_CLKP AF19

EVT2:0204: Change the SATA Port to port2 for MOR request

SATA_RXN0 30, SATA_RXP0 30, SATA_TXN0 30, SATA_TXP0 30 (HDD)
TP_SATA1RXN TP129 tpc26t, TP_SATA1RXP TP130 tpc26t, TP_SATA1TXN TP127 tpc26t, TP_SATA1TXP TP131 tpc26t
SATA_RXN2 30, SATA_RXP2 30, SATA_TXN2 30, SATA_TXP2 30 (ODD)
TP_SATA3RXN TP132 tpc26t, TP_SATA3RXP TP133 tpc26t, TP_SATA3TXN TP134 tpc26t, TP_SATA3TXP TP135 tpc26t, TP_SATA4RXN TP136 tpc26t, TP_SATA4RXP TP138 tpc26t
TP_SATA4TXP TP142 tpc26t, TP_SATA5RXN TP143 tpc26t, TP_SATA5RXP TP144 tpc26t, TP_SATA5TXN TP145 tpc26t, TP_SATA5TXP TP146 tpc26t
SATA_CLKN 3, SATA_CLKP 3

0106: Delete TP140 for layout request

SATALED# 37
SATALED# AE7, SATARBIAS# AK6, SATARBIAS AJ6, SATARBIAS 24.9_F R208 0402

GPIO56, GPIO49, GPIO34, GPIO33, GPIO32, GPIO28, GPIO27, GPIO20, GPIO18, GPIO13
SATA0GP/GPIO21 AK25 PANEL_ID1 → PANEL_ID1 51
SATA1GP/GPIO19 AE20 GPIO19
SATA2GP/GPIO36 AE21 PANEL_ID0 → PANEL_ID0 17,51
SATA3GP/GPIO37 AE22 SYS_ID4
SATA4GP AF22 SATA4GP R214 10K_J +3VRUN
SATA5GP AD21 SATA5GP R215 10K_J +3VRUN
SATACLKREQ#/GPIO35 L1 → SATA_CLKREQ# 3
SCLOCK/GPIO22 AJ24 SYS_ID0
SLOAD/GPIO38 AK24 SYS_ID1
SDATAOUT0/GPIO39 AH23 SYS_ID2
SDATAOUT1/GPIO48 AD20 SYS_ID3
GPIO14/JTAGTDI/QST_BMBUSY

3 OF 6

Projet name	SYS_ID3	SYS_ID2	SYS_ID1	SYS_ID0
M810	0	0	0	0
M820	0	0	1	0
M830	0	0	0	1
M840	0	0	1	1

Model name	H	M	L
SYS_ID5	0	0	1
SYS_ID4	1	1	0

Panel Type	P1	P2	P3	P4
PANEL_ID0	0	0	1	1
PANEL_ID1	0	1	0	1

+3VRUN
R1038 NC_10K_J SYS_ID0
R1039 NC_10K_J SYS_ID1
R1040 NC_10K_J SYS_ID2
R1041 NC_10K_J SYS_ID3
R1337 NV_10K_J SYS_ID4
R1336 CA_10K_J SYS_ID5
R1534 10K_J PANEL_ID1
R1535 10K_J GPIO19

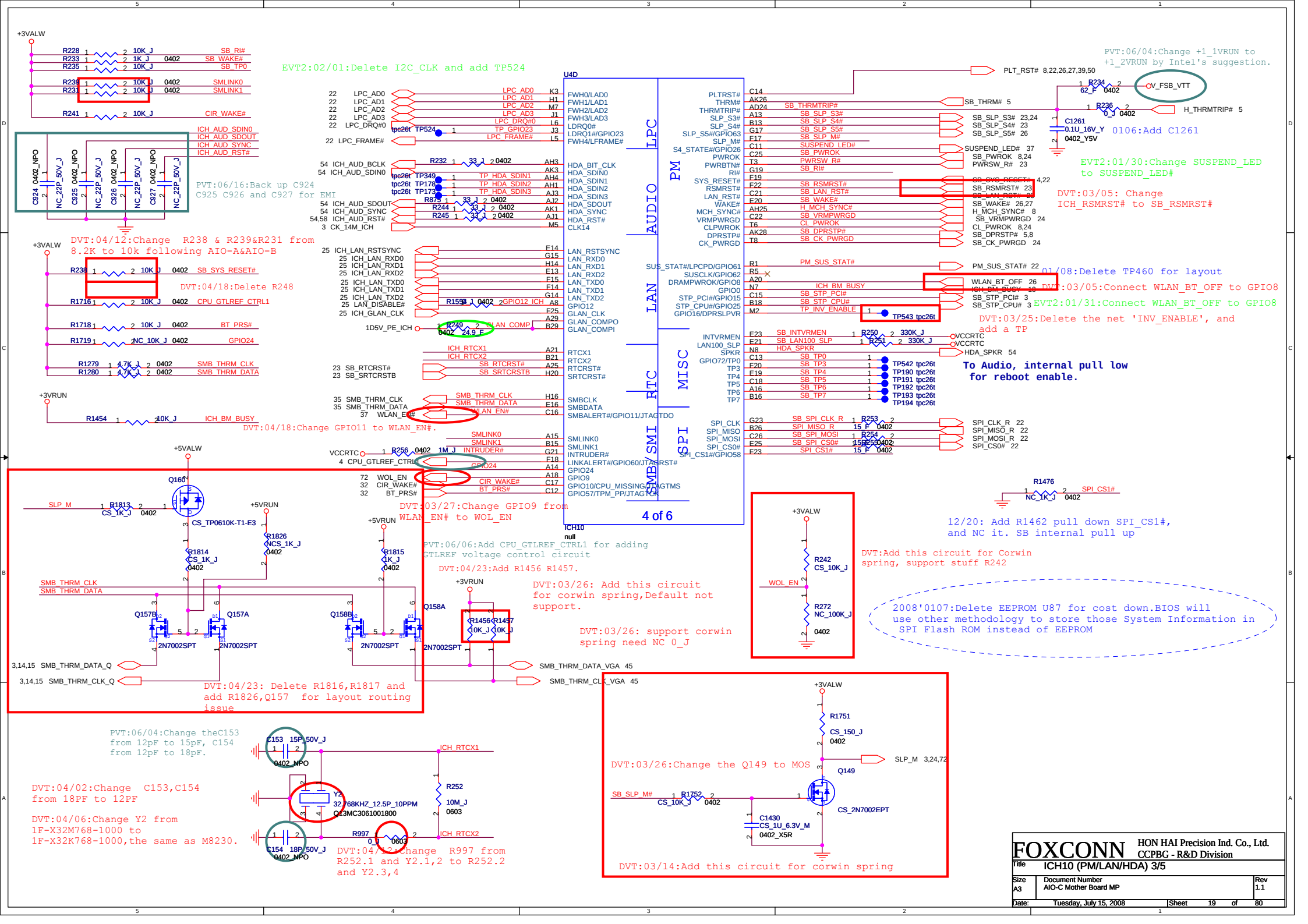
12/27:Add R1534 R1535

R1042 10K_J SYS_ID0
R1043 10K_J SYS_ID1
R1044 10K_J SYS_ID2
R1045 10K_J SYS_ID3
R1284 CA_10K_J SYS_ID4
R1281 NV_10K_J SYS_ID5

DVT:03/05:NV R1281,R1337 for M810 H;
CA R1284,R1336 for M810 L

FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	ICH10 (HOST/SATA) 2/5	
Size A3	Document Number AIO-C Mother Board MP	Rev 1.1
Date: Tuesday, July 15, 2008	Sheet 18 of 80	


EVT2:02/01:Delete I2C_CLK and add TP524
PVT:06/04:Change +1_1VRUN to +1_2VRUN by Intel's suggestion.
PVT:06/16:Back up C924 C925 C926 and C927 for EMI
DVT:04/12:Change R238 & R239&R231 from 8.2K to 10k following AIO-A&AIO-B
DVT:04/18:Delete R248
DVT:04/18:Change GPIO11 to WLAN_EN#.
DVT:03/27:Change GPIO9 from WLAN_EN# to WOL_EN
PVT:06/06:Add CPU_GTLREF_CTRL1 for adding GTLREF voltage control circuit
DVT:04/23:Add R1456 R1457.
DVT:03/26: Add this circuit for corwin spring,Default not support.
DVT:03/26: support corwin spring need NC 0_J
DVT:04/23: Delete R1816,R1817 and add R1826,Q157 for layout routing issue
PVT:06/04:Change theC153 from 12pF to 15pF, C154 from 12pF to 18pF.
DVT:04/02:Change C153,C154 from 18PF to 12PF
DVT:04/06:Change Y2 from 1F-X32M768-1000 to 1F-X32K768-1000,the same as M8230.
DVT:04/12:Change R997 from R252.1 and Y2.1,2 to R252.2 and Y2.3,4
0106:Add C1261
EVT2:01/30:Change SUSPEND_LED to SUSPEND_LED#
DVT:03/05: Change ICH_RSMRST# to SB_RSMRST#
01/08:Delete TP460 for layout
DVT:03/05:Connect WLAN_BT_OFF to GPIO8
EVT2:01/31:Connect WLAN_BT_OFF to GPIO8
DVT:03/25:Delete the net 'INV_ENABLE', and add a TP
To Audio, internal pull low for reboot enable.
12/20: Add R1462 pull down SPI_CS1#, and NC it. SB internal pull up
DVT:Add this circuit for Corwin spring, support stuff R242
2008'0107:Delete EEPROM U87 for cost down.BIOS will use other methodology to store those System Information in SPI Flash ROM instead of EEPROM
DVT:03/26:Change the Q149 to MOS
DVT:03/14:Add this circuit for corwin spring
U4D
ICH10
4 of 6
LPC
AUDIO
LAN
RTC
PM
MISC
SMB
SMI
SPI
FOXCONN
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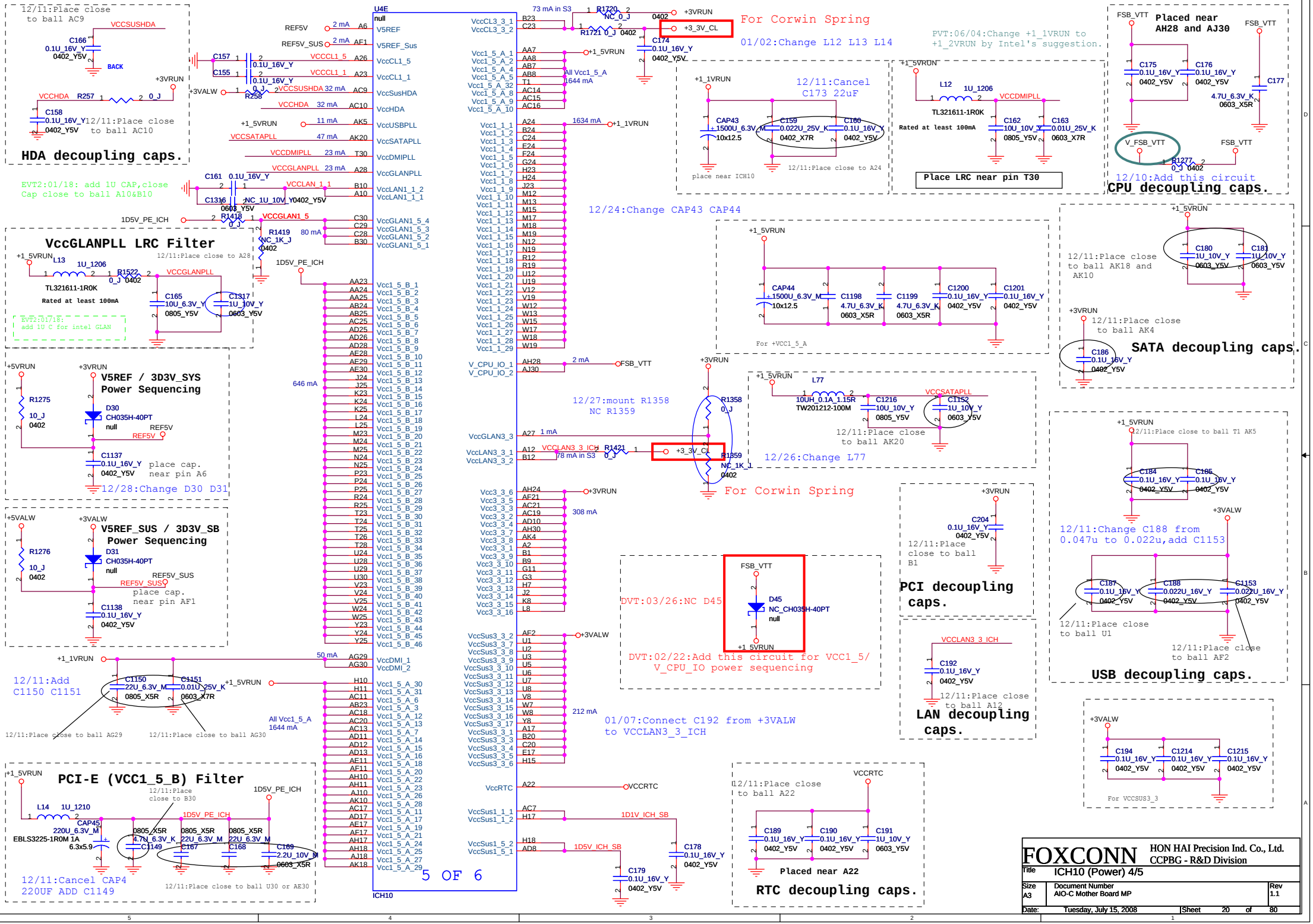
CCPBG - R&D Division
Title ICH10 (PM/LAN/HDA) 3/5
Size A3
Document Number AIO-C Mother Board MP
Rev 1.1
Date: Tuesday, July 15, 2008
Sheet 19 of 80


HDA decoupling caps.
VccGLANPLL LRC Filter
V5REF / 3D3V_SYS Power Sequencing
V5REF_SUS / 3D3V_SB Power Sequencing
PCI-E (VCC1_5_B) Filter
For Corwin Spring
01/02:Change L12 L13 L14
PVT:06/04:Change +1_1VRUN to +1_2VRUN by Intel's suggestion.
12/11:Cancel C173 22uF
Place LRC near pin T30
Placed near AH28 and AJ30
12/10:Add this circuit
CPU decoupling caps.
12/24:Change CAP43 CAP44
12/27:mount R1358 NC R1359
12/26:Change L77
SATA decoupling caps.
12/11:Change C188 from 0.047u to 0.022u,add C1153
USB decoupling caps.
DVT:03/26:NC D45
DVT:02/22:Add this circuit for VCC1_5/ V_CPU_IO power sequencing
PCI decoupling caps.
01/07:Connect C192 from +3VALW to VCCLAN3_3_ICH
LAN decoupling caps.
RTC decoupling caps.
12/11:Cancel CAP4 220UF ADD C1149
5 OF 6
ICH10
FOXCONN
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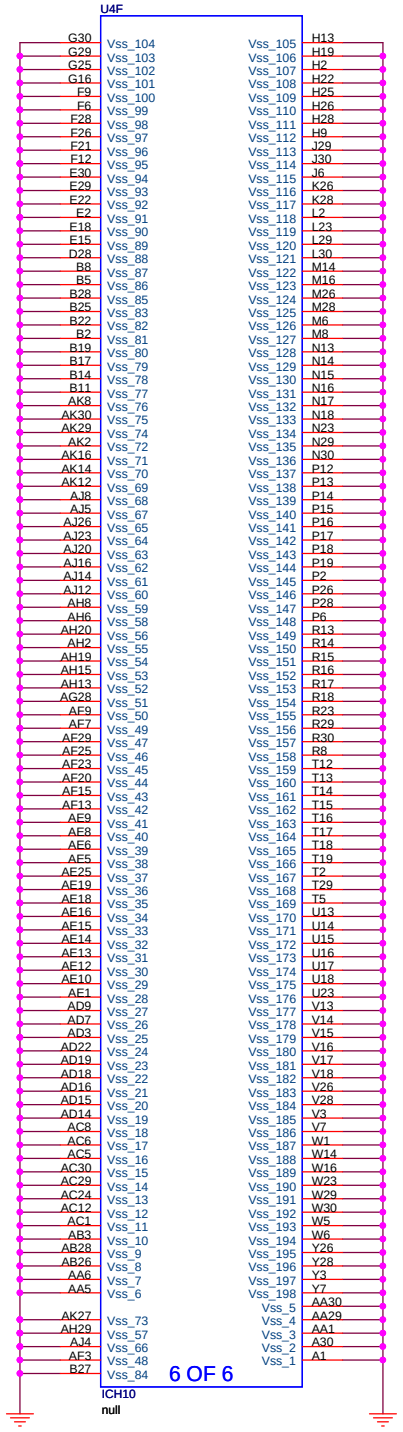
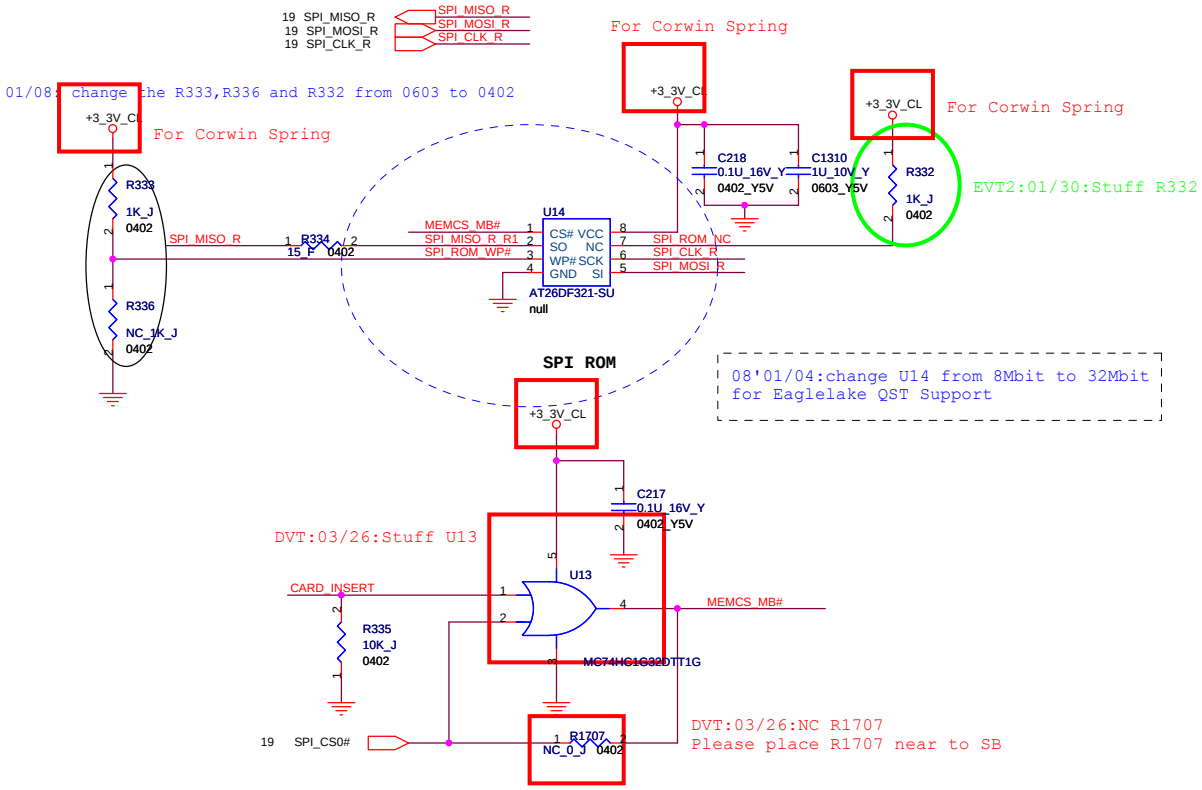
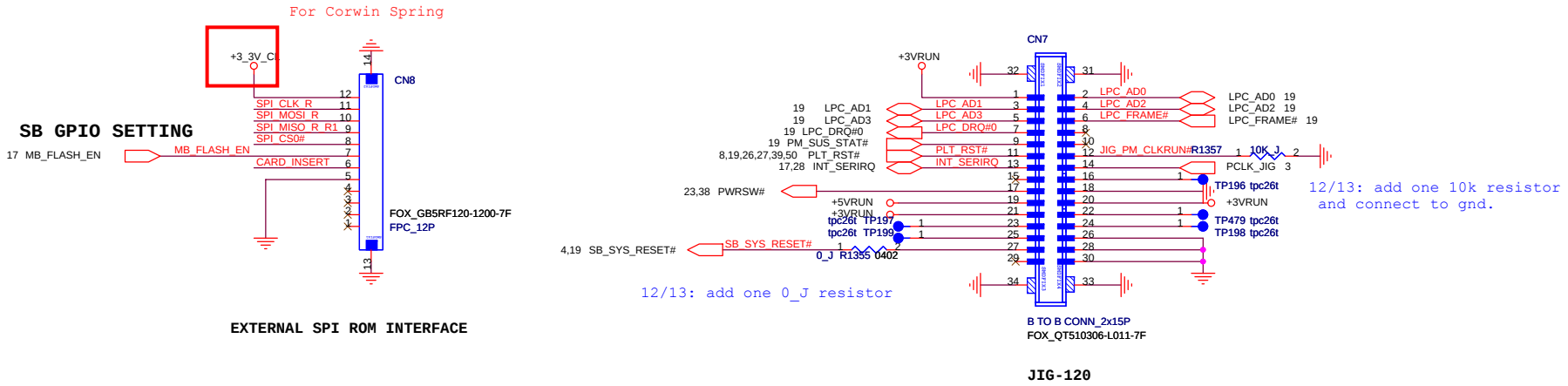
CCPBG - R&D Division
Title ICH10 (Power) 4/5
Size A3
Document Number AIO-C Mother Board MP
Rev 1.1
Date: Tuesday, July 15, 2008
Sheet 20 of 80



FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

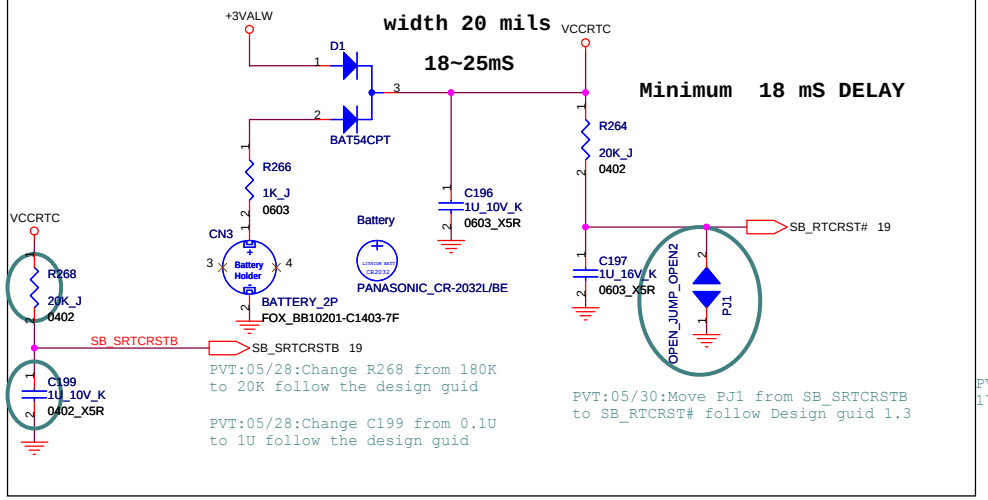
Title	ICH10 (Ground) 5/5	
Size A3	Document Number AIO-C Mother Board MP	Rev 1.1
Date: Tuesday, July 15, 2008	Sheet 21 of 80	



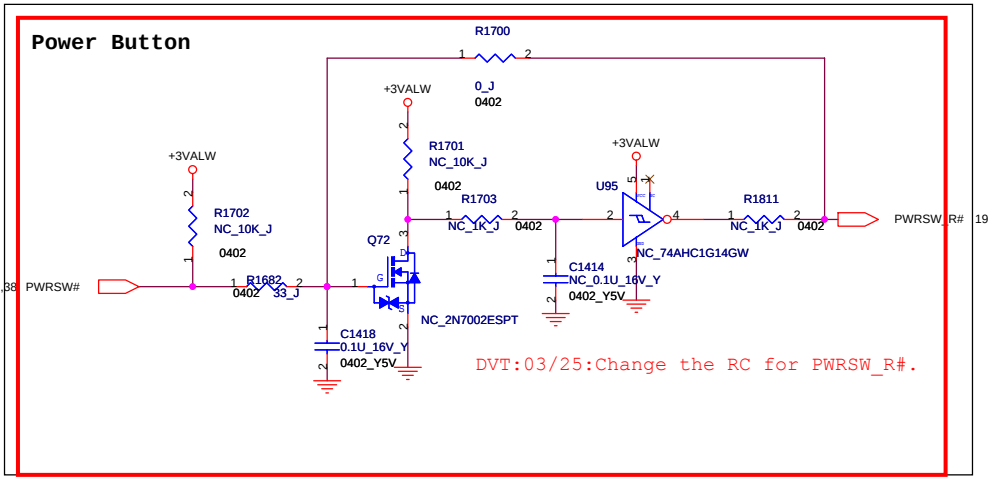


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Flash ROM& Debug	
Size A3	Document Number AIO-C Mother Board MP	Rev 1.1
Date: Tuesday, July 15, 2008	Sheet 22 of 80	

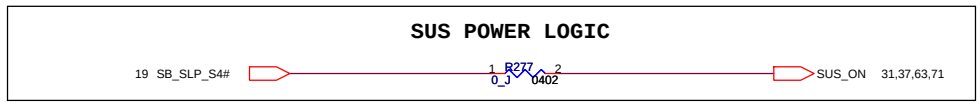
RTCRST# PORTION



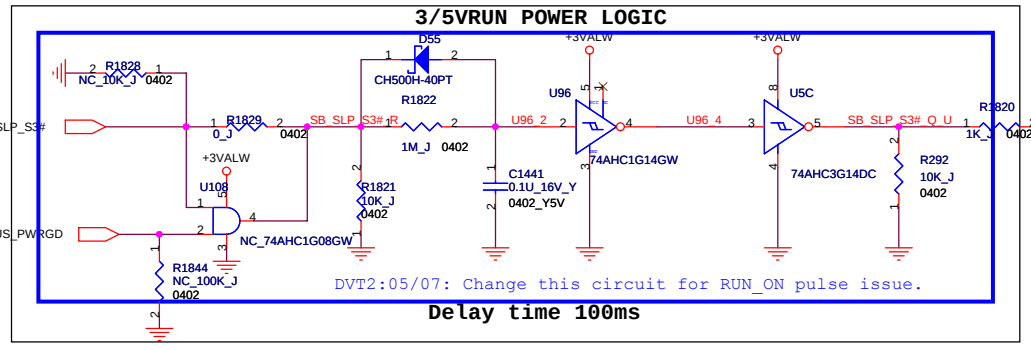
Power Button



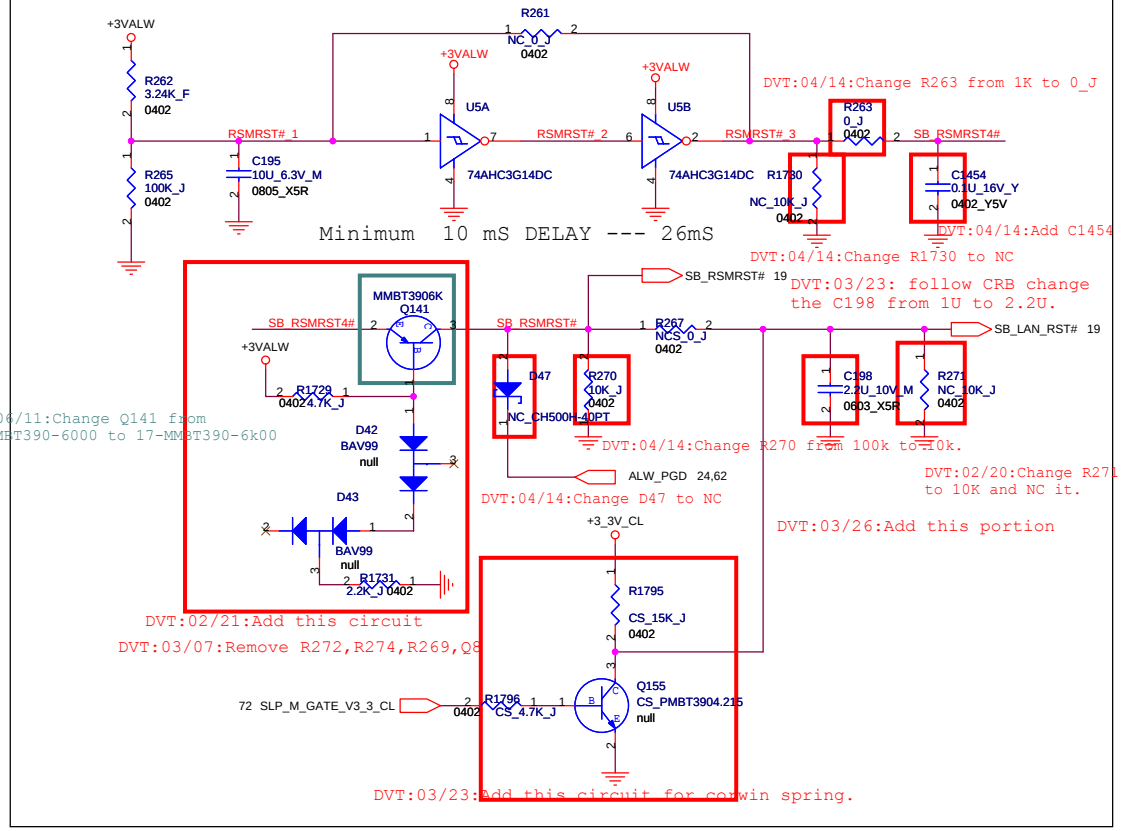
SUS POWER LOGIC



3/5VRUN POWER LOGIC

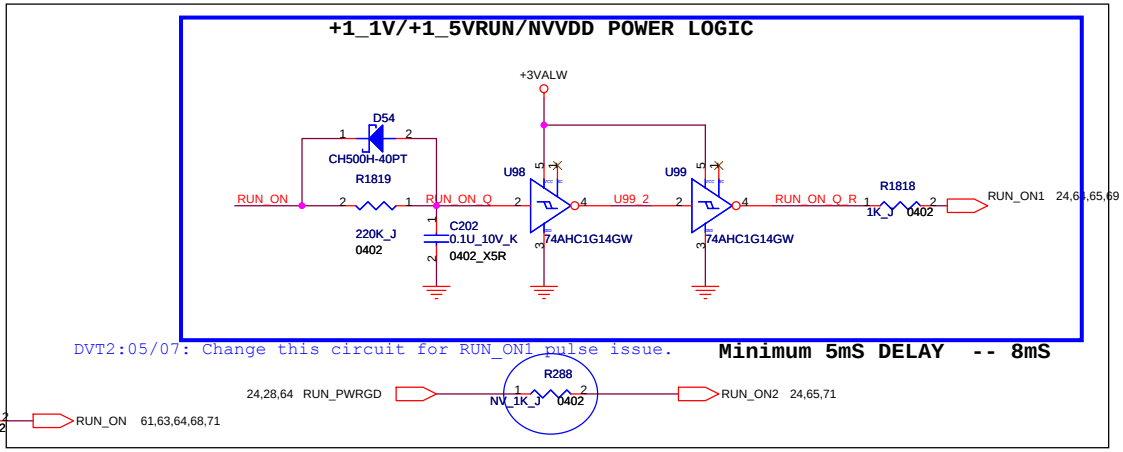


RSMRST# PORTION FOR DELAY



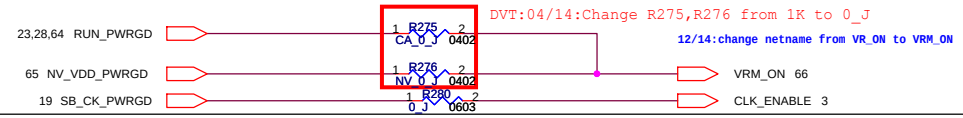
PVT:06/11:Change Q141 from
17-MMBT390-6000 to 17-MMBT390-6k00

+1_1V/+1_5VRUN/NVVDD POWER LOGIC

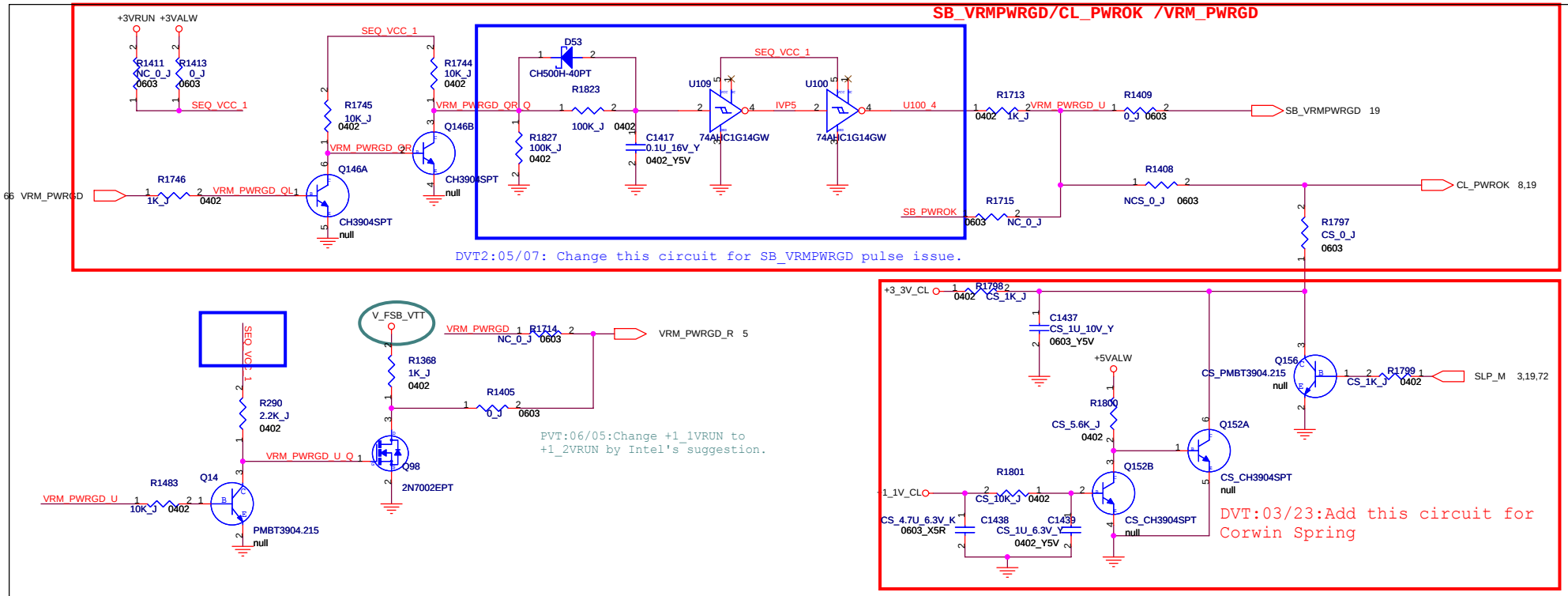


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Power Squence 1/2	
Size A3	Document Number AIO-C Mother Board MP	Rev 1.1
Date: Tuesday, July 15, 2008	Sheet 23 of 80	

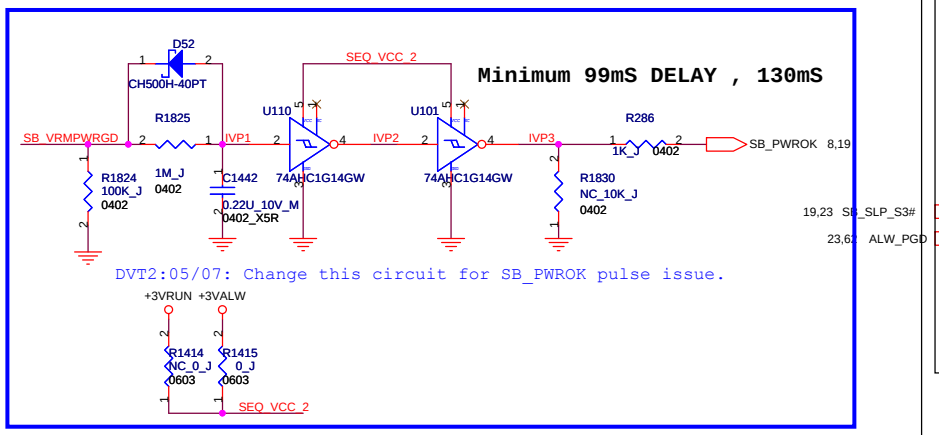
VCORE POWER LOGIC / CLOCK ENALBLE



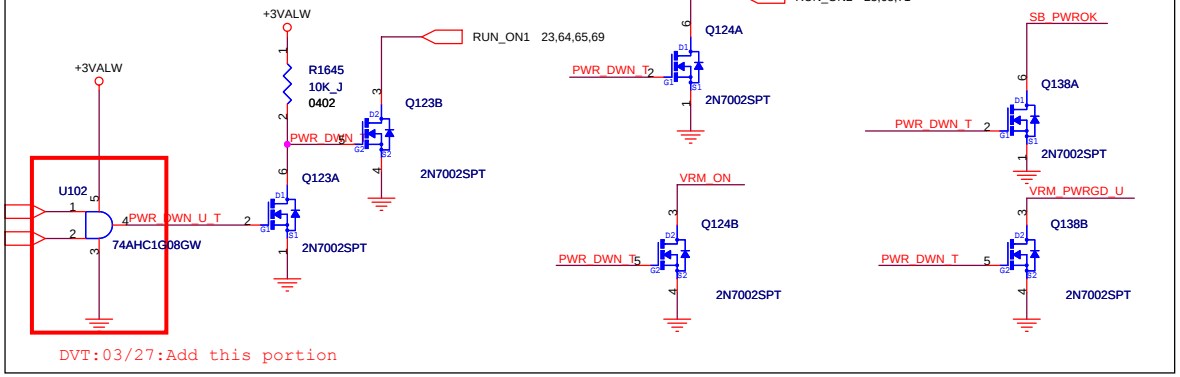
SB_VRMPWRGD/CL_PWROK /VRM_PWRGD



SB PWROK 99mS DELAY PORTION



POWER DOWN TIMING



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Power Squence 2/2	
Size A3	Document Number AIO-C Mother Board MP	Rev 1.1
Date: Tuesday, July 15, 2008	Sheet 24 of 80	

In 1000 Mb/s mode, JKCLK frequency is 62.5 MHz.
In 100 Mb/s mode, JKCLK frequency is 50 MHz.
In 10 Mb/s mode, JKCLK frequency is 5 MHz.
In power down mode, JKCLK frequency is 0 MHz.

Layout Notice: C1203 C1204 near LAN PHY

EVT2:01/30:Add C1413 and NC for EMI

Layout Notice: R1556 near LAN PHY

U56 BOAZ 82567V null

For Corwin Spring

about 730mA

DVT:03/07:Change C1319 from 4.7u to 10u,add C1427,C1428

these capitor near to the chip +1_8v_LAN

these capitor near to the chip +1v_ Vdd_LAN

DVT:03/07:NC C1330,C1329

Close to chip

DVT:03/17:Add and NC R1769

02/20:Change U56 from 82567LF to 82567V

DVT:04/14:Change the position of R1035

PVT:06/11:Change C874 from 27pf to 15pf and C866 from 27pf to 12pf follow vendor's test.

Pls split a ground plane beneath the magnetics module(L71).

EVT2:01/30:Add R1691 and NC it

PVT:06/04:Del the TP for BFT use the CN32's PIN instead of TP

DVT:03/21:Add the TP527-TP534 for L6 test

DVT:03/20:Change CN32 HH P/N

EVT2:02/12: Delete Net "GND_EMI"

DVT:04/18:Delete R1691 and R1679,and NC CN32 PIN9,10 for 2KV test

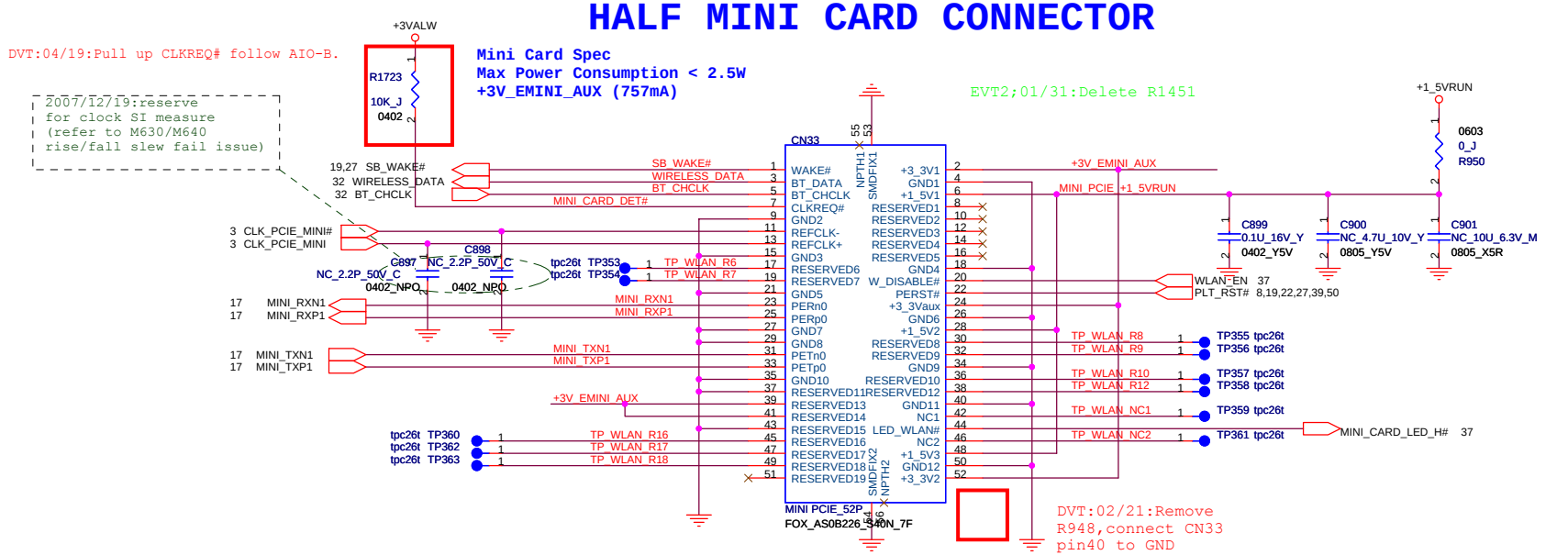
DVT:04/16:Add C347 C348 for EMI's request

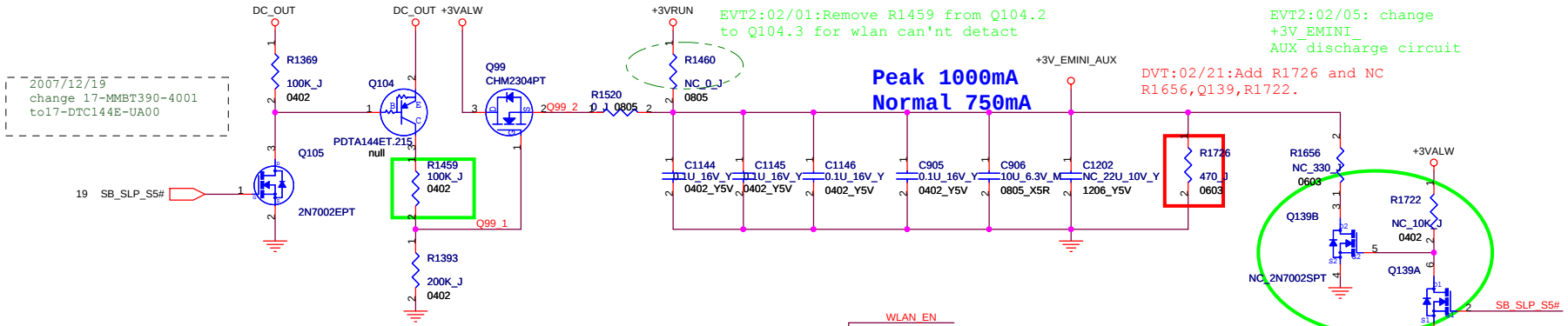
C347 C348 need close to L62

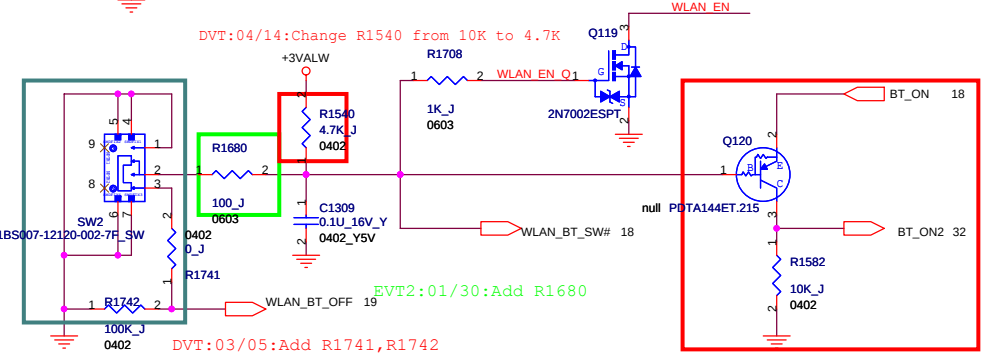
EVT2:02/10:Exchange RJ45_6, RJ45_4,RJ45_5

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	INTEL GLAN Boazman	
Size A3	Document Number AIO-C Mother Board MP	Rev 1.1
Date: Tuesday, July 15, 2008	Sheet 25 of 80	

HALF MINI CARD CONNECTOR

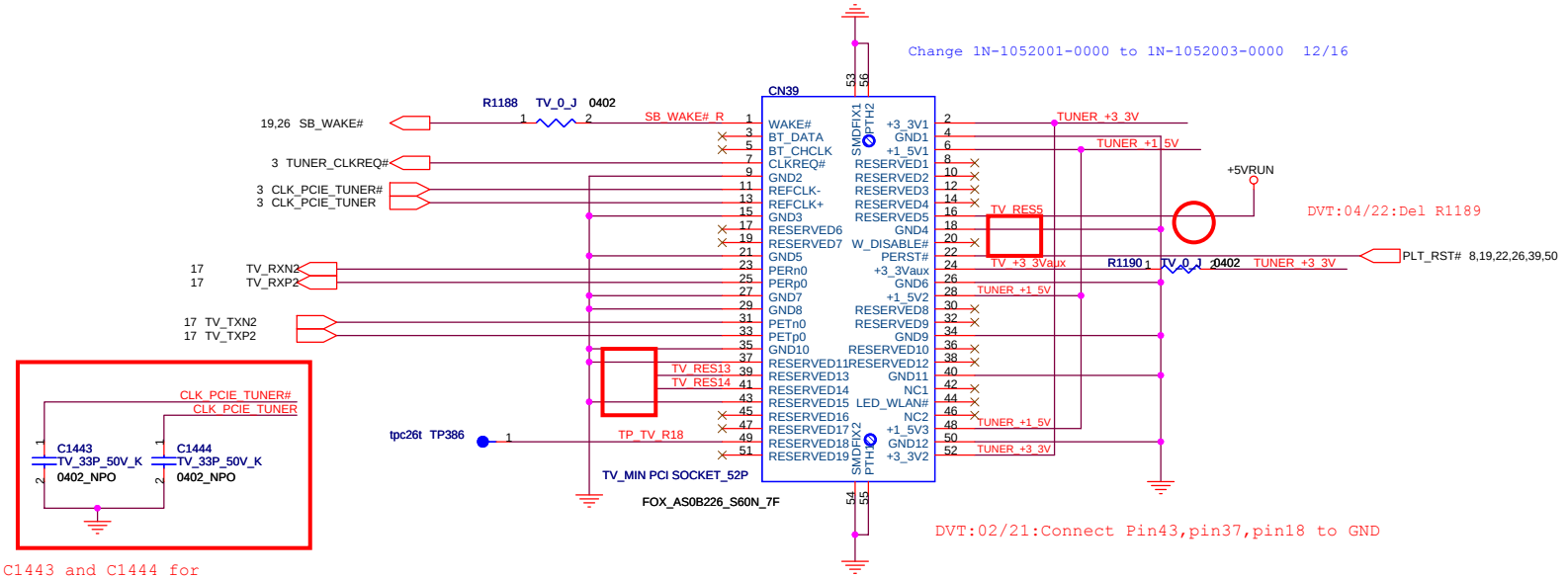


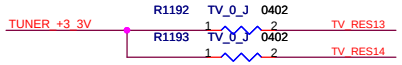


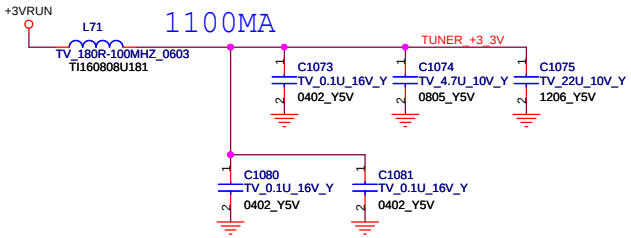


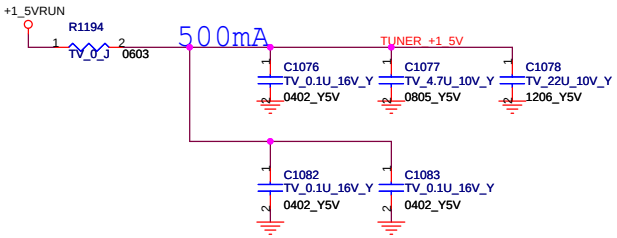
FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: PCIe WLAN		
Size: A3	Document Number: AIO-C Mother Board MP	Rev: 1.1
Date: Tuesday, July 15, 2008	Sheet 26 of 80	

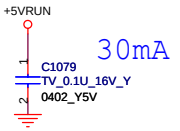
Mini-PCIE TUNER connector









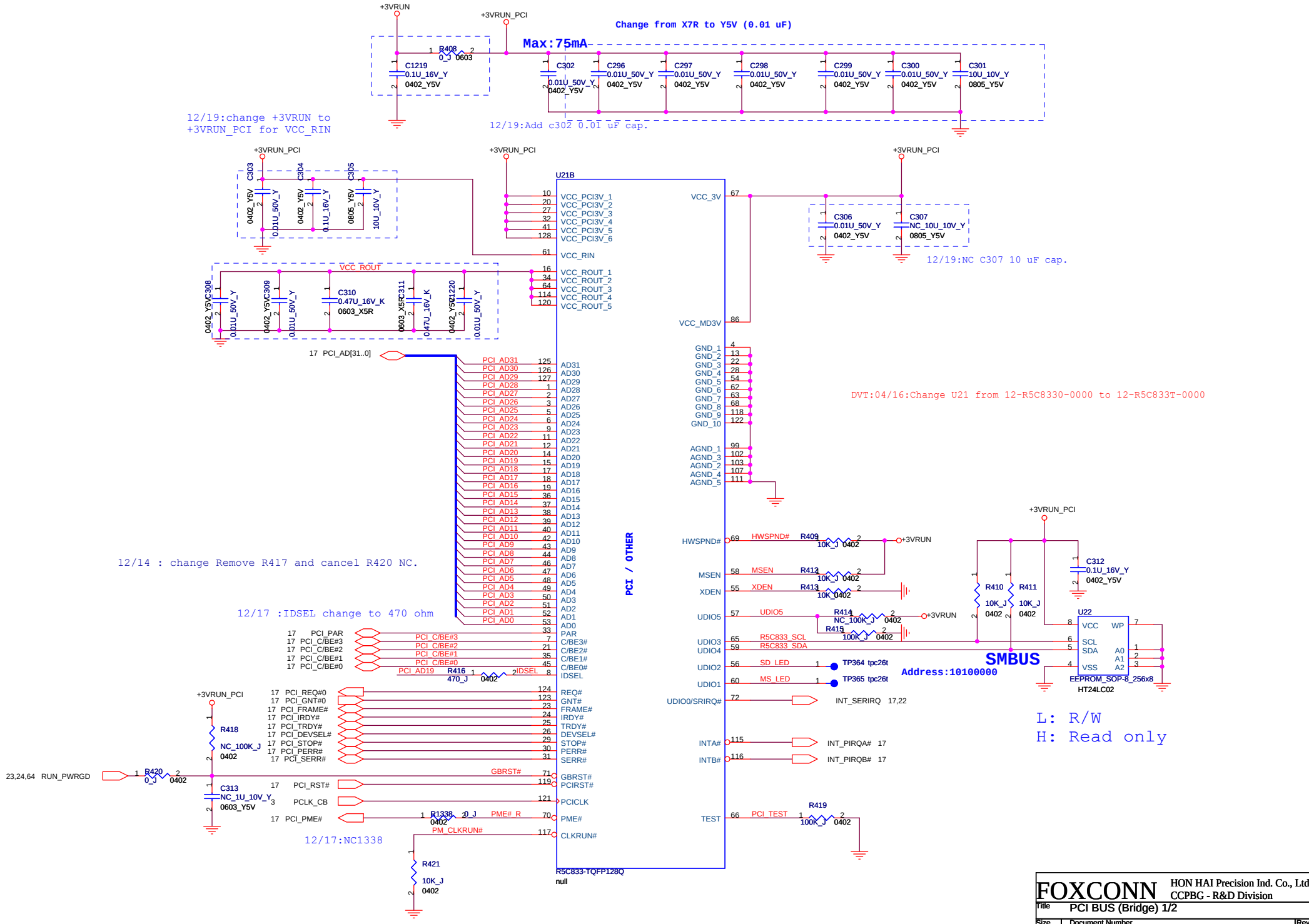


FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: *TV-TUNER*

Size	Document Number	Rev
A3	AIO-C Mother Board MP	1.1

Date: Tuesday, July 15, 2008 Sheet 27 of 80


Change from X7R to Y5V (0.01 uF)
Max:75mA
12/19:change +3VRUN to +3VRUN_PCI for VCC_RIN
12/19:Add c302 0.01 uF cap.
12/19:NC C307 10 uF cap.
DVT:04/16:Change U21 from 12-R5C8330-0000 to 12-R5C833T-0000
12/14 : change Remove R417 and cancel R420 NC.
12/17 :IDSEL change to 470 ohm
12/17:NC1338
U21B
PCI / OTHER
R5C833-TQFP128Q
null
SMBUS
Address:10100000
EEPROM_SOP-8_256x8
HT24LC02
L: R/W
H: Read only
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
PCI BUS (Bridge) 1/2
Document Number
AIO-C Mother Board MP
Rev 1.1
Tuesday, July 15, 2008
Sheet 28 of 80

DVT:04/16:Change U21 from 12-R5C8330-0000 to 12-R5C833T-0000

12/24: Change U23 from BD2056 to TI 2056.

DVT:04/02:Change C318,C324 from 10PF to 22PF.

PVT:06/11:Change C324 from 22p to 27p follow vendor's test.

01/11:Delete TP477 for layout

Add test point

PVT:06/17:Change R425 R426 R429 and R430 from 56.2ohm to 54.9 ohm.

AS CLOSE AS POSSIBLE TO R5C833

3W rule

DVT:04/14:Add R1490 and R1491same as AIO-A/B

MS/SD POWER

DVT:03/19:Change CN18 HH P/N

iLink CONN.

DVT:04/22:Change C1277 to 15PF and stuff it for EVT2 over shoot.

MS STD/DUO CONN.

Place caps close to SD socket.

SD CONN.

DVT:04/16:Add C338 for EMI's request.

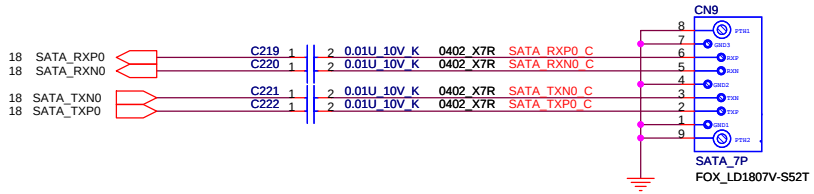
Please place C338 near CN20 pin3 and pin4

DVT:02/20:NC C337 for MOR requirement

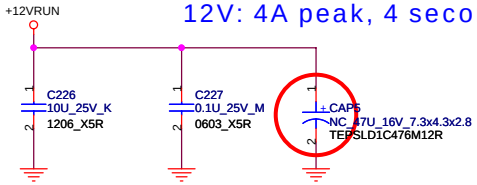
DVT:03/27:Change the MEDIA_LED to MEDIA_LED#

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
Title	PCI BUS(MS/SD/iLink) 2/2
Size A3	Document Number AIO-C Mother Board MP
Rev	1.1
Date: Tuesday, July 15, 2008	Sheet 29 of 80

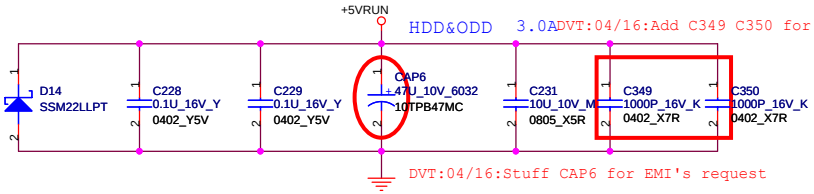
SATA HDD CONN



HDD

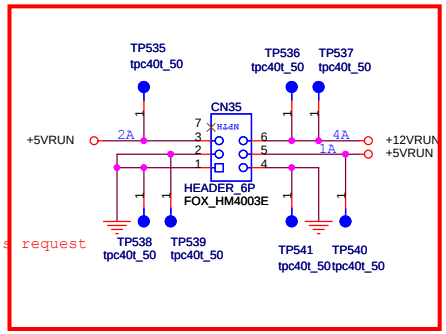


01/25:Delete the D13



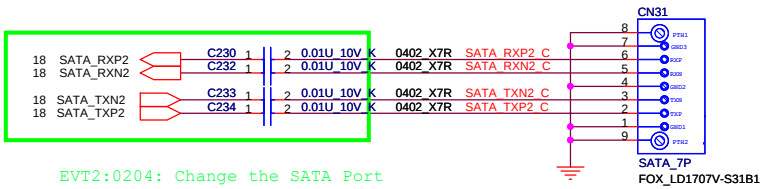
DVT:04/16:Add C349 C350 for EMI's request

DVT:04/16:Stuff CAP6 for EMI's request



DVT:03/21:Add the TP535-TP41 for L6 test

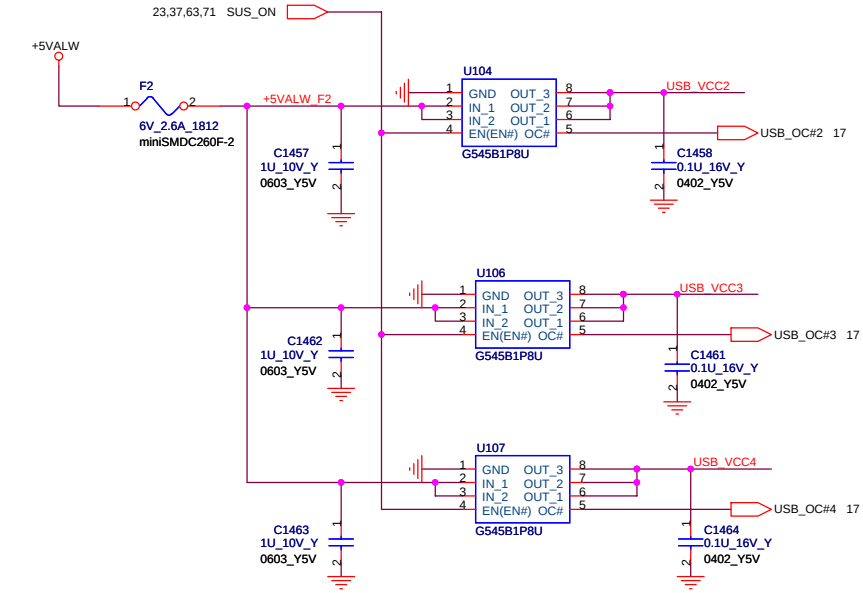
SATA ODD CONN



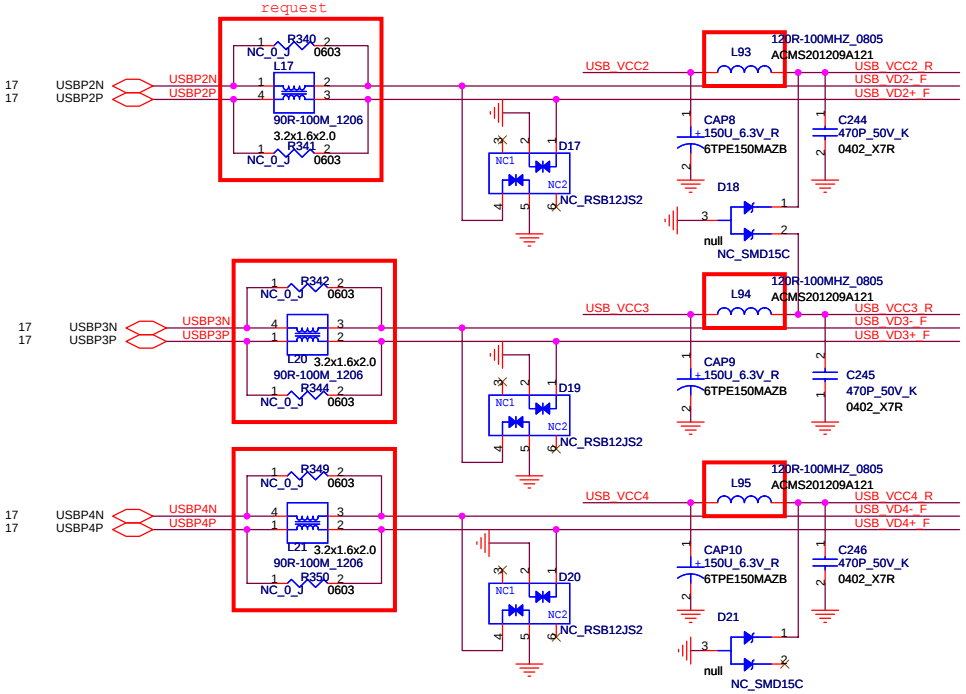
EVT2:0204: Change the SATA Port to port2 for MOR request

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	SATA HDD /SATA ODD	
Size A3	Document Number AIO-C Mother Board MP	Rev 1.1
Date: Tuesday, July 15, 2008	Sheet 30 of 80	

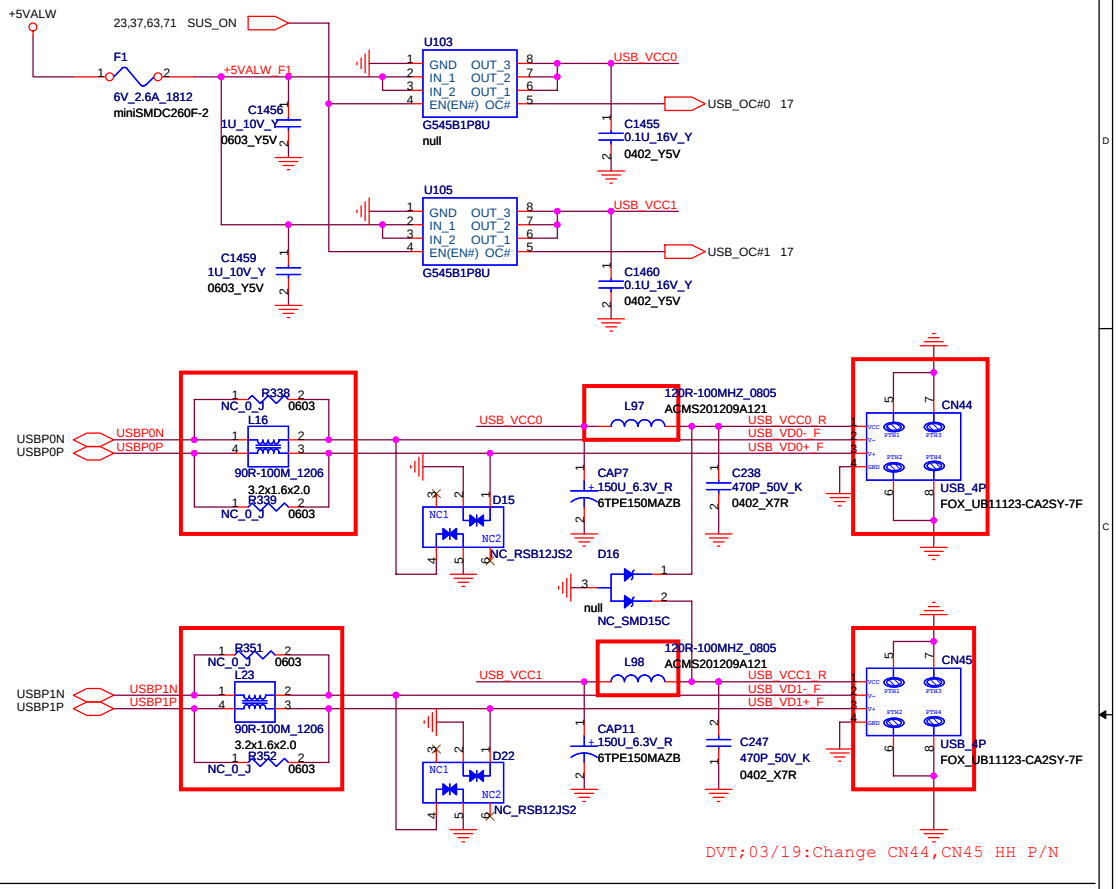
Rear side USB



DVT:04/16:Mount common choke and bead for USB signal and power rail for rear/side USB ports for EMI's request

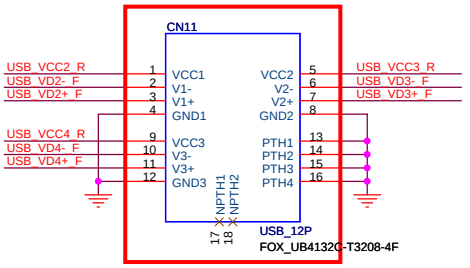


Onboard side USB



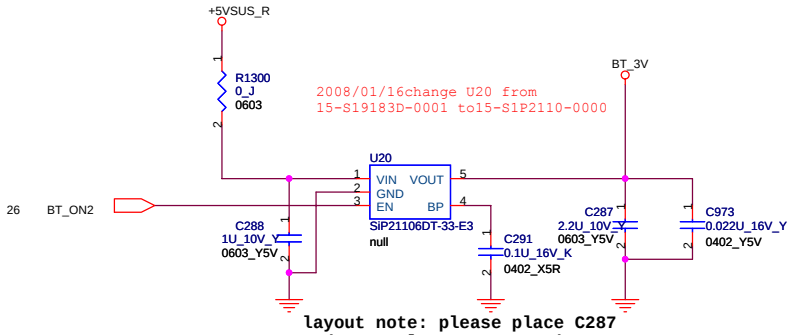
DVT;03/19:Change CN44,CN45 HH P/N

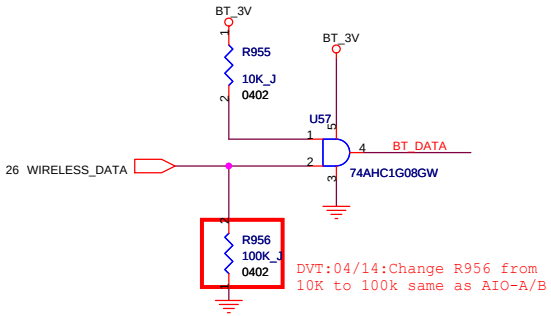
USB CONN X3



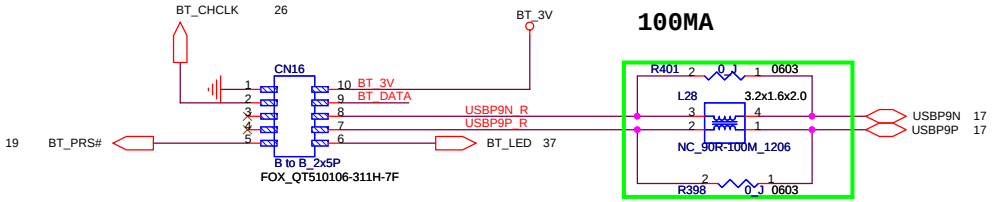
DVT;03/19:Change CN11 HH P/N

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	USB Port	
Size A3	Document Number AIO-C Mother Board MP	Rev 1.1
Date: Tuesday, July 15, 2008	Sheet 31 of 80	



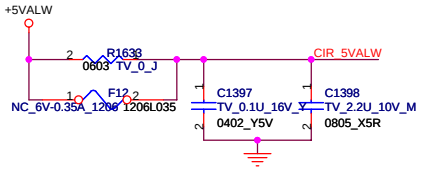


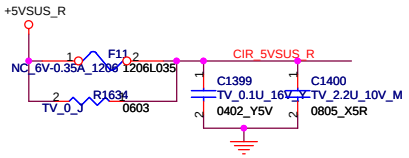
BLUE TOOTH

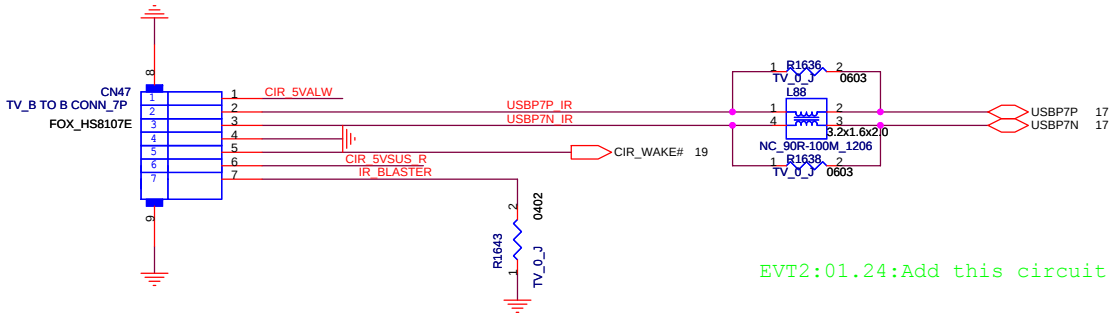


EVT2:01/31:Swap L28,R401,R398

CIR







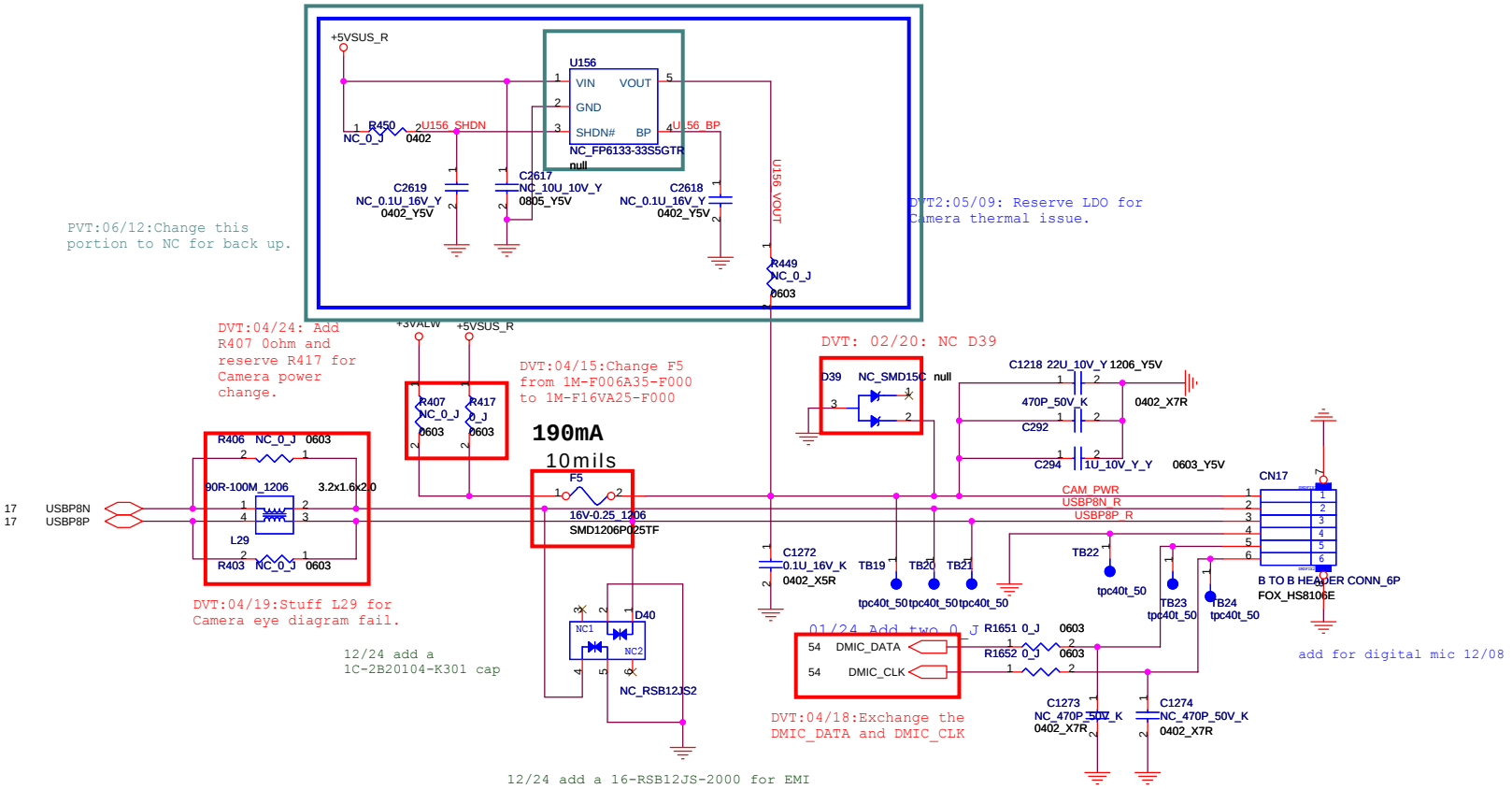
EVT2:01.24:Add this circuit

EVT2:02.01:change the CN47 and change the CIR circuit

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	CIR&BT	
Size A3	Document Number AIO-C Mother Board MP	Rev 1.1
Date: Tuesday, July 15, 2008	Sheet 32 of 80	

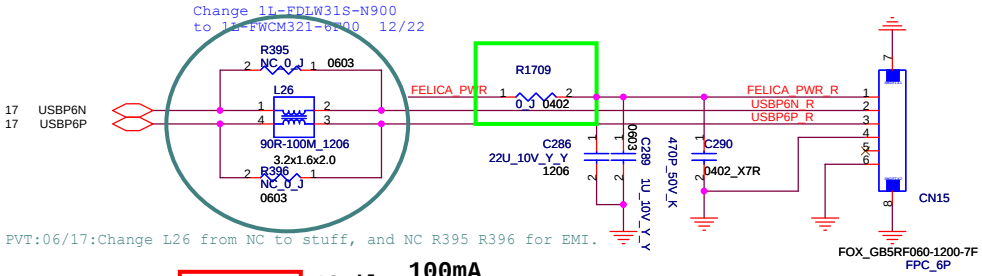
PVT:06/16:Change the U156 from 15-FP61333-0000 to 15-FP61333-0001 for vendor's change.

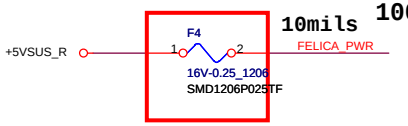
CAMERA



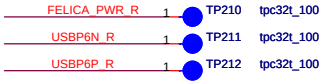
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: CAMERA		
Size: A3	Document Number: AIO-C Mother Board MP	Rev: 1.1
Date: Tuesday, July 15, 2008	Sheet 33 of 80	

Felica Connector





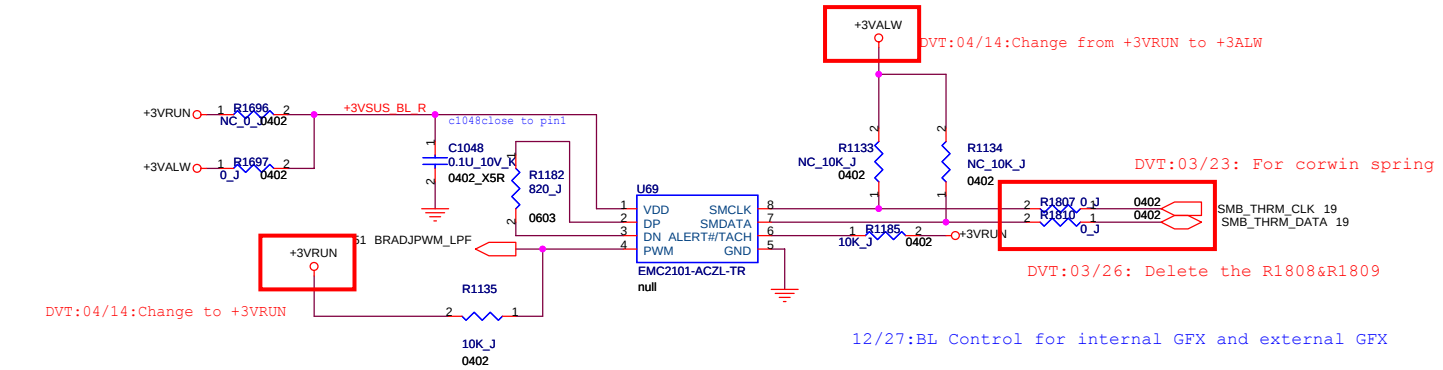
DVT:04/18:Change F4 from
1M-F006A35-F000 to 1M-F16VA25-F000



EVT2:01/28:Add this circuit
for +5VSUS_R not
discharge

DVT:03/27:Delete the +5VSUS_R discharge circuit

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	FELICA	
Size A3	Document Number AIO-C Mother Board MP	Rev 1.1
Date: Tuesday, July 15, 2008	Sheet 34 of 80	



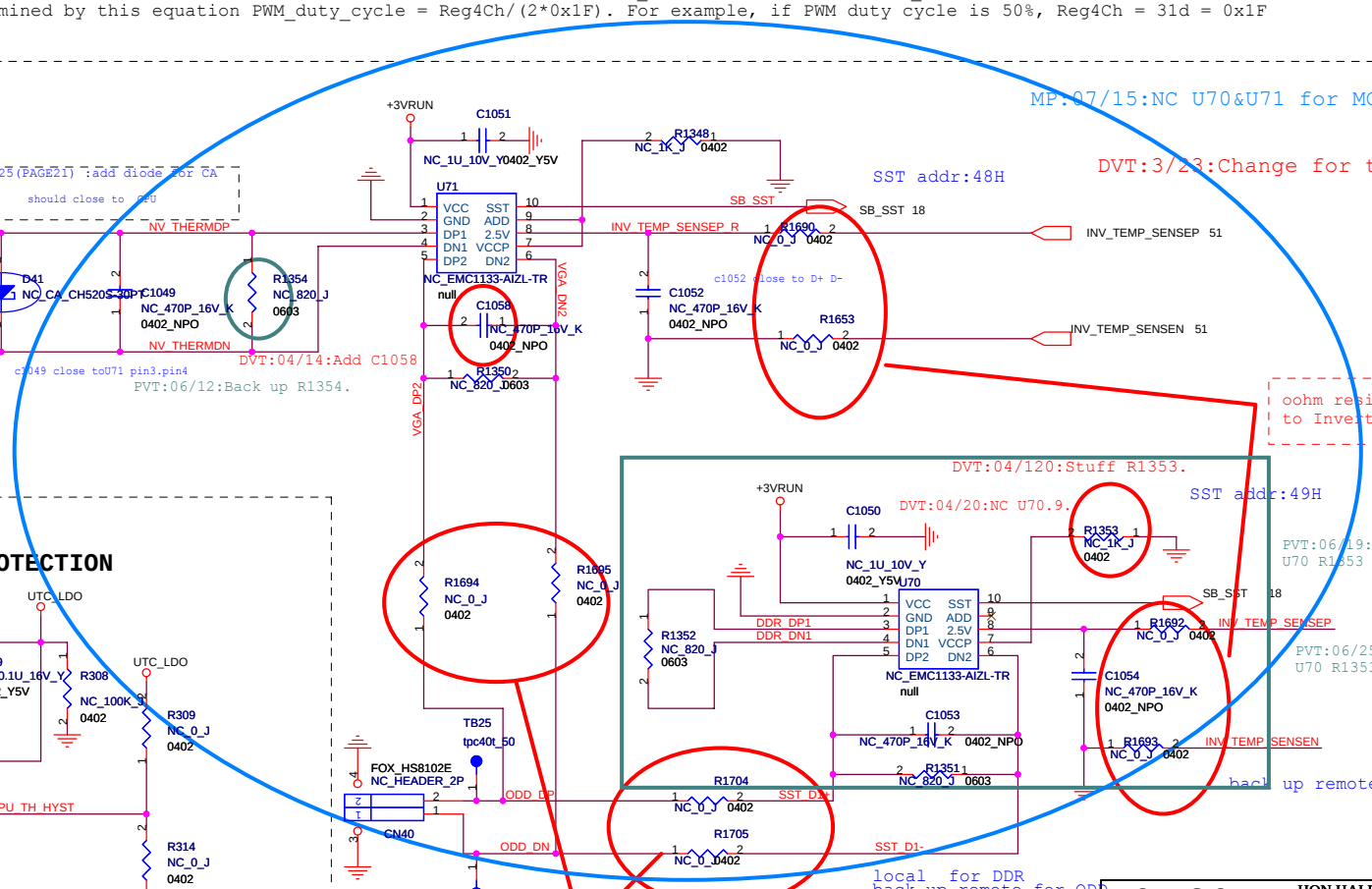
1. set 0x24 to register 4Ah.
2. set 0x1F to register 4Dh.
3. configure register 4Eh for different PWM freq using equation Value(Reg 4Eh)= 5806/PWM_freq. For example, if PWM_freq =200Hz, Reg4Eh = 29d = 0x1D
4. PWM duty cycle is determined by this equation PWM_duty_cycle = Reg4Ch/(2*0x1F). For example, if PWM duty cycle is 50%, Reg4Ch = 31d = 0x1F

U71(Close to VGA chip)

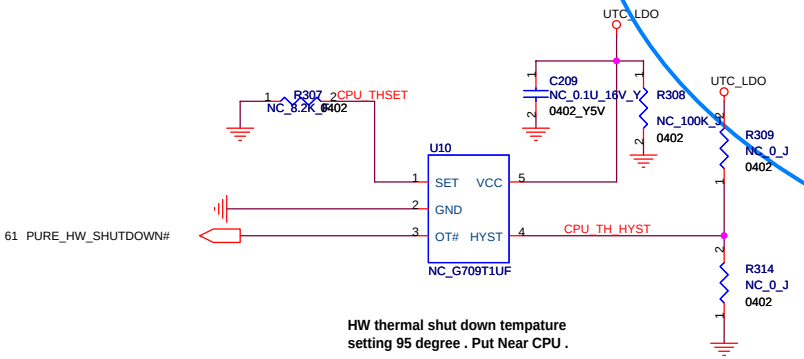
local NC
remote for VGA
remote for INVERTER
remote for ODD

U70(Close to SO-DIMM)

local for SO-DIMM)
back up remote 2 for ODD
back up remote 3 for inverter



HW THERMAL PROTECTION



HW thermal shut down tempature setting 95 degree . Put Near CPU .

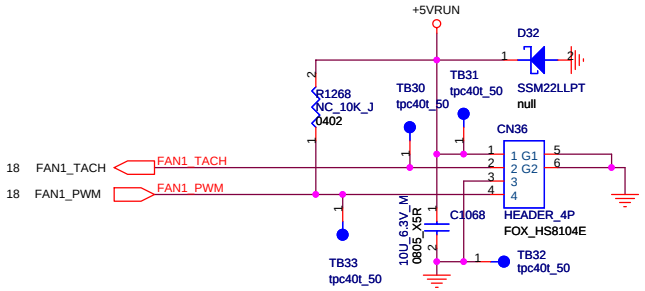
FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: **Thermal & BL**

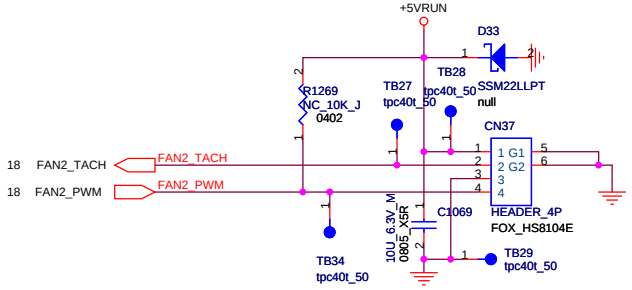
Size: A3 | Document Number: **AIO-C Mother Board MP** | Rev: 1.1

Date: Tuesday, July 15, 2008 | Sheet 35 of 80

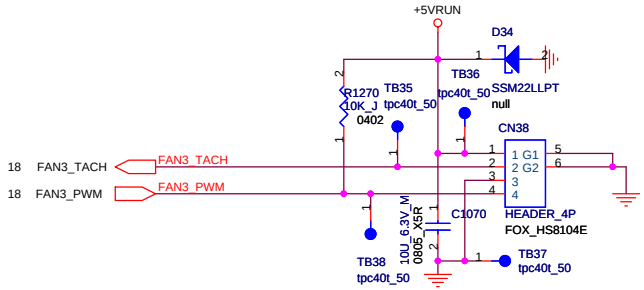
CPU FAN1



CPU FAN2



Chassis Fan(RESERVED)

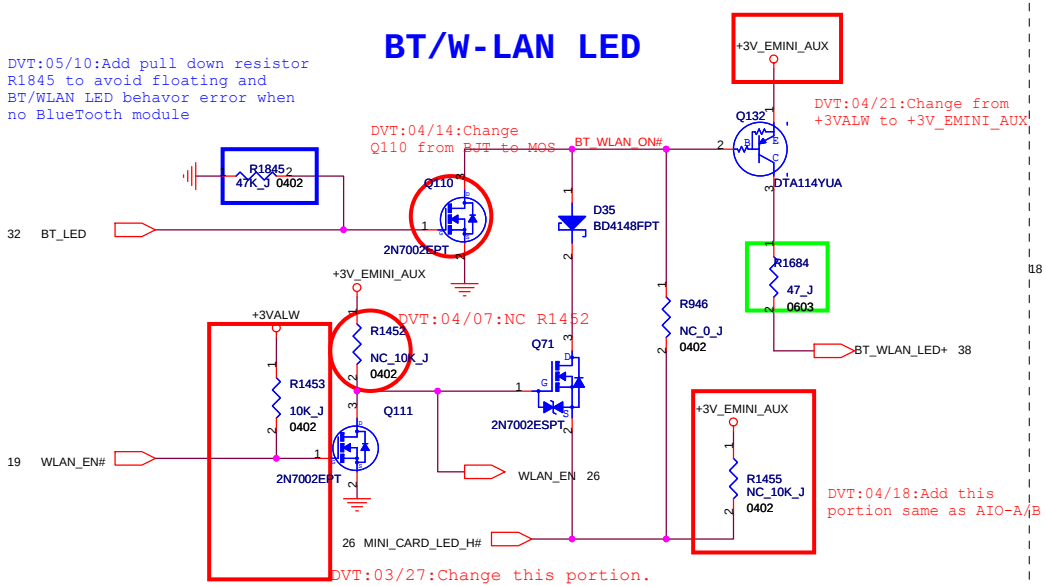


12/28(PAGE20):change D32.D33.D34

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: FAN		
Size: A3	Document Number: AIO-C Mother Board MP	Rev: 1.1
Date: Tuesday, July 15, 2008	Sheet 36 of 80	

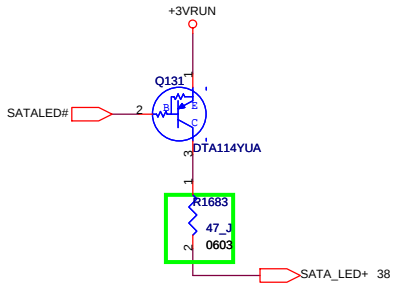
BT/W-LAN LED

DVT:05/10:Add pull down resistor R1845 to avoid floating and BT/WLAN LED behavor error when no BlueTooth module



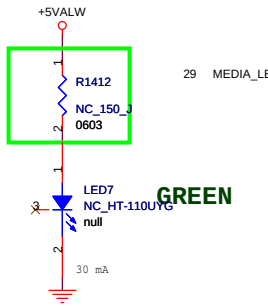
SATA LED

EVT2:02/01:Change R1683,R1684 R1698 from 150ohm to 47ohm



DDR LED

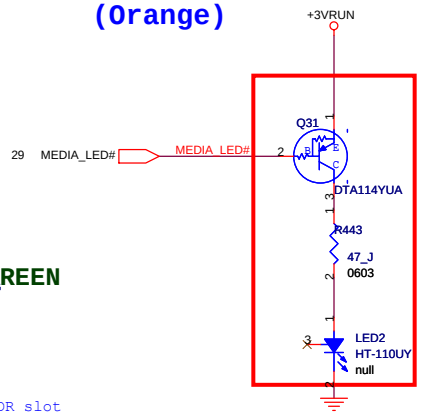
EVT2:02/01:Change R1412 from 220ohm to 150ohm



please clear DDR slot as closed as possible

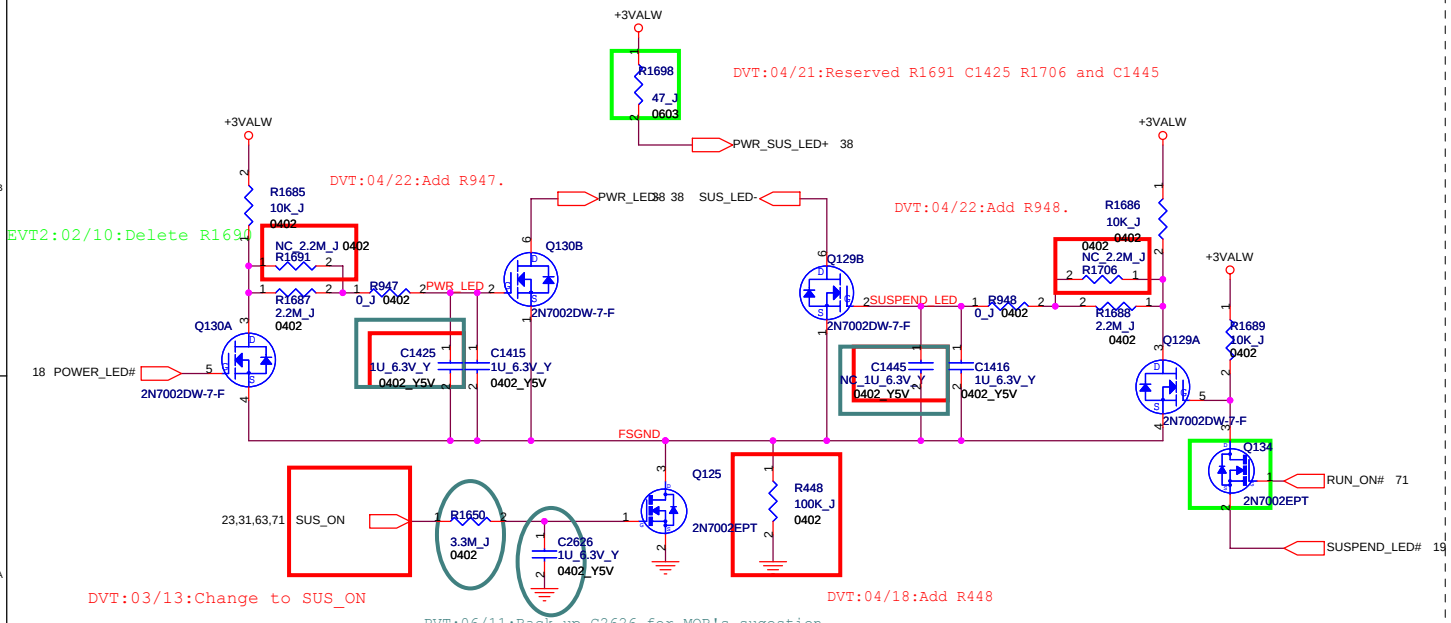
EVT2:02/17:change R443 from 220ohm to 47ohm

MS/SD LED (Orange)



DVT:03/13: Change MS/SD LED circuit from high active to low active.

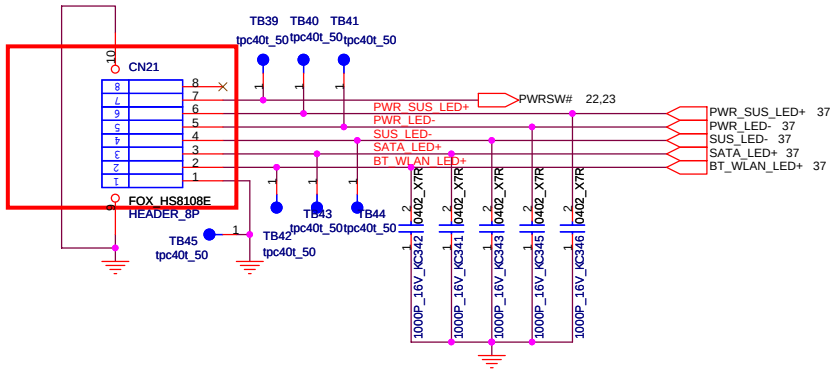
POWER/SUSPEND LED



DVT:04/21:Move DIP_SW to SB Page17

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	LED	
Size A3	Document Number AIO-C Mother Board MP	Rev 1.1
Date: Tuesday, July 15, 2008	Sheet 37 of 80	

Power BTN. Conn.



DVT:03/19:Change CN21 HH P/N

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	DB CONN(PSwitch)	
Size A3	Document Number AIO-C Mother Board MP	Rev 1.1
Date: Tuesday, July 15, 2008	Sheet 38 of 80	

DVT:02/20:change C531,C532, C669, C1055 from
1C-2B20474-M000 to 1C-2B20474-K100

DVT_0421_VGA:
for RF solution

DVT_0423_VGA:
Change 90ohm from 85ohm

PCIE : 90ohm +/- 10%

U41A — 1/13 PCI_EXPRESS — NV_NB9M-GS-S-U2 null

NVVDD and PEXVDD source need close to GPU.

NEAR BGA

Place near balls / Place near BGA / Place under GPU close to CAPs / Place under GPU close to BALL

1550mA / 210mA / 80mA / 165mA / 100MHz

width:at least 10 mil

CAP46 NV_100U_6.3V_7343 EEFCX0J101R

TP389 tpc26t TP390 tpc26t

L45 NV_10NH_0603 SWI0603CT10NJ

R675 NV_200_F0402 R676 NV_2.49K_F0402

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	NB9M (PCI-E) 1/9	
Size A3	Document Number AIO-C Mother Board MP	Rev 1.1
Date: Tuesday, July 15, 2008	Sheet 39 of 80	

DVT_0423_VGA:
Change 90ohm from 85ohm

PCIE : 90ohm +/- 10%

7 PEG_TXP[0..15]

PEG_TXP0
PEG_TXP1
PEG_TXP2
PEG_TXP3
PEG_TXP4
PEG_TXP5
PEG_TXP6
PEG_TXP7
PEG_TXP8
PEG_TXP9
PEG_TXP10
PEG_TXP11
PEG_TXP12
PEG_TXP13
PEG_TXP14
PEG_TXP15

7 PEG_TXN[0..15]

PEG_TXN0
PEG_TXN1
PEG_TXN2
PEG_TXN3
PEG_TXN4
PEG_TXN5
PEG_TXN6
PEG_TXN7
PEG_TXN8
PEG_TXN9
PEG_TXN10
PEG_TXN11
PEG_TXN12
PEG_TXN13
PEG_TXN14
PEG_TXN15

PEG_TXP0	0402_X5R	2	NV_0.1U_16V_M C770	PEG_RXP_C0
PEG_TXN0	0402_X5R	2	NV_0.1U_16V_M C771	PEG_RXN_C0
PEG_TXP1	0402_X5R	2	NV_0.1U_16V_M C772	PEG_RXP_C1
PEG_TXN1	0402_X5R	2	NV_0.1U_16V_M C773	PEG_RXN_C1
PEG_TXP2	0402_X5R	2	NV_0.1U_16V_M C774	PEG_RXP_C2
PEG_TXN2	0402_X5R	2	NV_0.1U_16V_M C776	PEG_RXN_C2
PEG_TXP3	0402_X5R	2	NV_0.1U_16V_M C778	PEG_RXP_C3
PEG_TXN3	0402_X5R	2	NV_0.1U_16V_M C779	PEG_RXN_C3
PEG_TXP4	0402_X5R	2	NV_0.1U_16V_M C781	PEG_RXP_C4
PEG_TXN4	0402_X5R	2	NV_0.1U_16V_M C783	PEG_RXN_C4
PEG_TXP5	0402_X5R	2	NV_0.1U_16V_M C784	PEG_RXP_C5
PEG_TXN5	0402_X5R	2	NV_0.1U_16V_M C786	PEG_RXN_C5
PEG_TXP6	0402_X5R	2	NV_0.1U_16V_M C788	PEG_RXP_C6
PEG_TXN6	0402_X5R	2	NV_0.1U_16V_M C790	PEG_RXN_C6
PEG_TXP7	0402_X5R	2	NV_0.1U_16V_M C792	PEG_RXP_C7
PEG_TXN7	0402_X5R	2	NV_0.1U_16V_M C793	PEG_RXN_C7
PEG_TXP8	0402_X5R	2	NV_0.1U_16V_M C794	PEG_RXP_C8
PEG_TXN8	0402_X5R	2	NV_0.1U_16V_M C795	PEG_RXN_C8
PEG_TXP9	0402_X5R	2	NV_0.1U_16V_M C796	PEG_RXP_C9
PEG_TXN9	0402_X5R	2	NV_0.1U_16V_M C797	PEG_RXN_C9
PEG_TXP10	0402_X5R	2	NV_0.1U_16V_M C798	PEG_RXP_C10
PEG_TXN10	0402_X5R	2	NV_0.1U_16V_M C799	PEG_RXN_C10
PEG_TXP11	0402_X5R	2	NV_0.1U_16V_M C800	PEG_RXP_C11
PEG_TXN11	0402_X5R	2	NV_0.1U_16V_M C801	PEG_RXN_C11
PEG_TXP12	0402_X5R	2	NV_0.1U_16V_M C802	PEG_RXP_C12
PEG_TXN12	0402_X5R	2	NV_0.1U_16V_M C803	PEG_RXN_C12
PEG_TXP13	0402_X5R	2	NV_0.1U_16V_M C804	PEG_RXP_C13
PEG_TXN13	0402_X5R	2	NV_0.1U_16V_M C805	PEG_RXN_C13
PEG_TXP14	0402_X5R	2	NV_0.1U_16V_M C810	PEG_RXP_C14
PEG_TXN14	0402_X5R	2	NV_0.1U_16V_M C811	PEG_RXN_C14
PEG_TXP15	0402_X5R	2	NV_0.1U_16V_M C812	PEG_RXP_C15
PEG_TXN15	0402_X5R	2	NV_0.1U_16V_M C813	PEG_RXN_C15

PEG_RXP_C[0..15] 39

PEG_RXP_C0
PEG_RXP_C1
PEG_RXP_C2
PEG_RXP_C3
PEG_RXP_C4
PEG_RXP_C5
PEG_RXP_C6
PEG_RXP_C7
PEG_RXP_C8
PEG_RXP_C9
PEG_RXP_C10
PEG_RXP_C11
PEG_RXP_C12
PEG_RXP_C13
PEG_RXP_C14
PEG_RXP_C15

PEG_RXN_C[0..15] 39

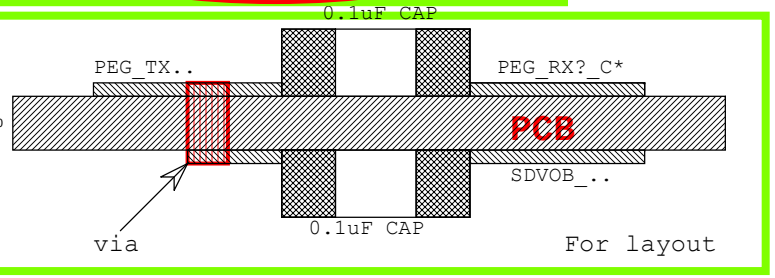
PEG_RXN_C0
PEG_RXN_C1
PEG_RXN_C2
PEG_RXN_C3
PEG_RXN_C4
PEG_RXN_C5
PEG_RXN_C6
PEG_RXN_C7
PEG_RXN_C8
PEG_RXN_C9
PEG_RXN_C10
PEG_RXN_C11
PEG_RXN_C12
PEG_RXN_C13
PEG_RXN_C14
PEG_RXN_C15

These CAP close to NB

select SDVOB
these Cap.(c775 c777 c780 c782 c785 c787 c789 c791 need to place back to back with PCIE-Tx AC cap, C827 C828 need to place back to back with PCIE-Rx AC cap)

SDVO : 90ohm +/- 10%

PEG_TXP0	0402_X5R	2	CA_0.1U_16V_M C775	SDVOB_RED+	SDVOB_RED+	50
PEG_TXN0	0402_X5R	2	CA_0.1U_16V_M C777	SDVOB_RED-	SDVOB_RED-	50
PEG_TXP1	0402_X5R	2	CA_0.1U_16V_M C780	SDVOB_GREEN+	SDVOB_GREEN+	50
PEG_TXN1	0402_X5R	2	CA_0.1U_16V_M C782	SDVOB_GREEN-	SDVOB_GREEN-	50
PEG_TXP2	0402_X5R	2	CA_0.1U_16V_M C785	SDVOB_BLUE+	SDVOB_BLUE+	50
PEG_TXN2	0402_X5R	2	CA_0.1U_16V_M C787	SDVOB_BLUE-	SDVOB_BLUE-	50
PEG_TXP3	0402_X5R	2	CA_0.1U_16V_M C789	SDVOB_CLK+	SDVOB_CLK+	50
PEG_TXN3	0402_X5R	2	CA_0.1U_16V_M C791	SDVOB_CLK-	SDVOB_CLK-	50
7,41 PEG_RXN2	0402_X5R	2	CA_0.1U_16V_M C827	STALL-	STALL-	50
7,41 PEG_RXP2	0402_X5R	2	CA_0.1U_16V_M C828	STALL+	STALL+	50



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: NB9M(PCIE TX) 2/9		
Size: A3	Document Number: AIO-C Mother Board MP	Rev: 1.1
Date: Tuesday, July 15, 2008	Sheet 40 of 80	

DVT_0423_VGA:
Change 90ohm from 85ohm

PCIE : 90ohm +/- 10%

7,40 PEG_RXP[0..15]

PEG_RXP0	C552	NV_0.1U_16V_M0402_X5R	TXP0
PEG_RXP1	C554	NV_0.1U_16V_M0402_X5R	TXP1
PEG_RXP2	C556	NV_0.1U_16V_M0402_X5R	TXP2
PEG_RXP3	C558	NV_0.1U_16V_M0402_X5R	TXP3
PEG_RXP4	C560	NV_0.1U_16V_M0402_X5R	TXP4
PEG_RXP5	C562	NV_0.1U_16V_M0402_X5R	TXP5
PEG_RXP6	C564	NV_0.1U_16V_M0402_X5R	TXP6
PEG_RXP7	C566	NV_0.1U_16V_M0402_X5R	TXP7
PEG_RXP8	C568	NV_0.1U_16V_M0402_X5R	TXP8
PEG_RXP9	C570	NV_0.1U_16V_M0402_X5R	TXP9
PEG_RXP10	C572	NV_0.1U_16V_M0402_X5R	TXP10
PEG_RXP11	C574	NV_0.1U_16V_M0402_X5R	TXP11
PEG_RXP12	C576	NV_0.1U_16V_M0402_X5R	TXP12
PEG_RXP13	C578	NV_0.1U_16V_M0402_X5R	TXP13
PEG_RXP14	C580	NV_0.1U_16V_M0402_X5R	TXP14
PEG_RXP15	C582	NV_0.1U_16V_M0402_X5R	TXP15

TXP[0..15] 39

7,40 PEG_RXN[0..15]

PEG_RXN0	C551	NV_0.1U_16V_M0402_X5R	TXN0
PEG_RXN1	C553	NV_0.1U_16V_M0402_X5R	TXN1
PEG_RXN2	C555	NV_0.1U_16V_M0402_X5R	TXN2
PEG_RXN3	C557	NV_0.1U_16V_M0402_X5R	TXN3
PEG_RXN4	C559	NV_0.1U_16V_M0402_X5R	TXN4
PEG_RXN5	C561	NV_0.1U_16V_M0402_X5R	TXN5
PEG_RXN6	C563	NV_0.1U_16V_M0402_X5R	TXN6
PEG_RXN7	C565	NV_0.1U_16V_M0402_X5R	TXN7
PEG_RXN8	C567	NV_0.1U_16V_M0402_X5R	TXN8
PEG_RXN9	C569	NV_0.1U_16V_M0402_X5R	TXN9
PEG_RXN10	C571	NV_0.1U_16V_M0402_X5R	TXN10
PEG_RXN11	C573	NV_0.1U_16V_M0402_X5R	TXN11
PEG_RXN12	C575	NV_0.1U_16V_M0402_X5R	TXN12
PEG_RXN13	C577	NV_0.1U_16V_M0402_X5R	TXN13
PEG_RXN14	C579	NV_0.1U_16V_M0402_X5R	TXN14
PEG_RXN15	C581	NV_0.1U_16V_M0402_X5R	TXN15

TXN[0..15] 39

XCLK_277
0 (Reserved)
1 (27M Hz)

NB9X TVMODE[2:0]
000

SUB_VENDOR — *ROM_SI (XXXX)*
0 (No vedio BIOS ROM)
1 (BIOS ROM is present)

SLOT_CLK_CFG — *ROM_SO (1000)*
0 (GPU and MCH not share a common reference clk)
1 (GPU and MCH share a common reference clk)

PEX_PLL_EN_TERM — *ROM_SCLK (0000)*
0 (Disable)
1 (Enable)

USER[3:0] — *STRAP0 (1000)*
1000

NB9X 3GIO_PADCFG[3:0] — *STRAP1 (0001)*
0001

NB9X PCI_DEVID[4:0] — *STRAP2 (1001)*
NB9P-GS X1001
NB9M-GS X1001

0100 64-bit Reserved
0101 32Mx32 GDDR3 - 136 ball - monolithic 64-bit Qimonda
0110 32Mx32 GDDR3 - 136 ball - monolithic 64-bit Hynix
0111 32Mx32 GDDR3 - 136 ball - monolithic 64-bit Samsung

0000 64-bit Reserved
0001 16Mx32 GDDR3 - 136 ball 64-bit Qimonda
0010 16Mx32 GDDR3 - 136 ball 64-bit Hynix
0011 16Mx32 GDDR3 - 136 ball 64-bit Samsung

MP 0708:Default is for Qimonda,
and for Samsung,it should mount 15K.

+3VRUN

NC_0.1U_10V_K C1224 0402_X7R

R1149 NV_0_J 0402

R1144 NV_30K_F 0402 — ROM_SI 45

R1147 NV_5.1K_F 0402 — ROM_SO 45

R1148 NV_15K_F 0402 — ROM_SCLK 45

R1150 NC_5.1K_F 0402

R1541 NV_10K_F 0402 — STRAP0 45

R1542 NV_34.8K_F 0402

R1152 NV_5.1K_F 0402 — STRAP1 45

R1155 NV_10K_F 0402 — STRAP2 45

0122:
delete unnecessary strap resistors.

Logical Strap bit Mapping

Resister values	Pull-up to VDD	Pull-down to GND
5KΩ	1000	0000
10KΩ	1001	0001
15KΩ	1010	0010
20KΩ	1011	0011
25KΩ	1100	0100
30KΩ	1101	0101
35KΩ	1110	0110
45KΩ	1111	0111

Strap Options

Physical Strapping pin	Power Rail	Logical Strapping pin3	Logical Strapping pin2	Logical Strapping pin1	Logical Strapping pin0
ROM_SI	+3VRUN	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
ROM_SO	+3VRUN	XCLK_277	TVMODE[2]	TVMODE[1]	TVMODE[0]
ROM_SCLK	+3VRUN	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
STRAP0	+3VRUN	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VRUN	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	+3VRUN	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]

0101
1000
0000
1xxx
0000
06E9: 1001

Use the Software Request form to add support for other panels.

24" 1920x1200
WUXGA
20" 1680x1050
WSXGA+

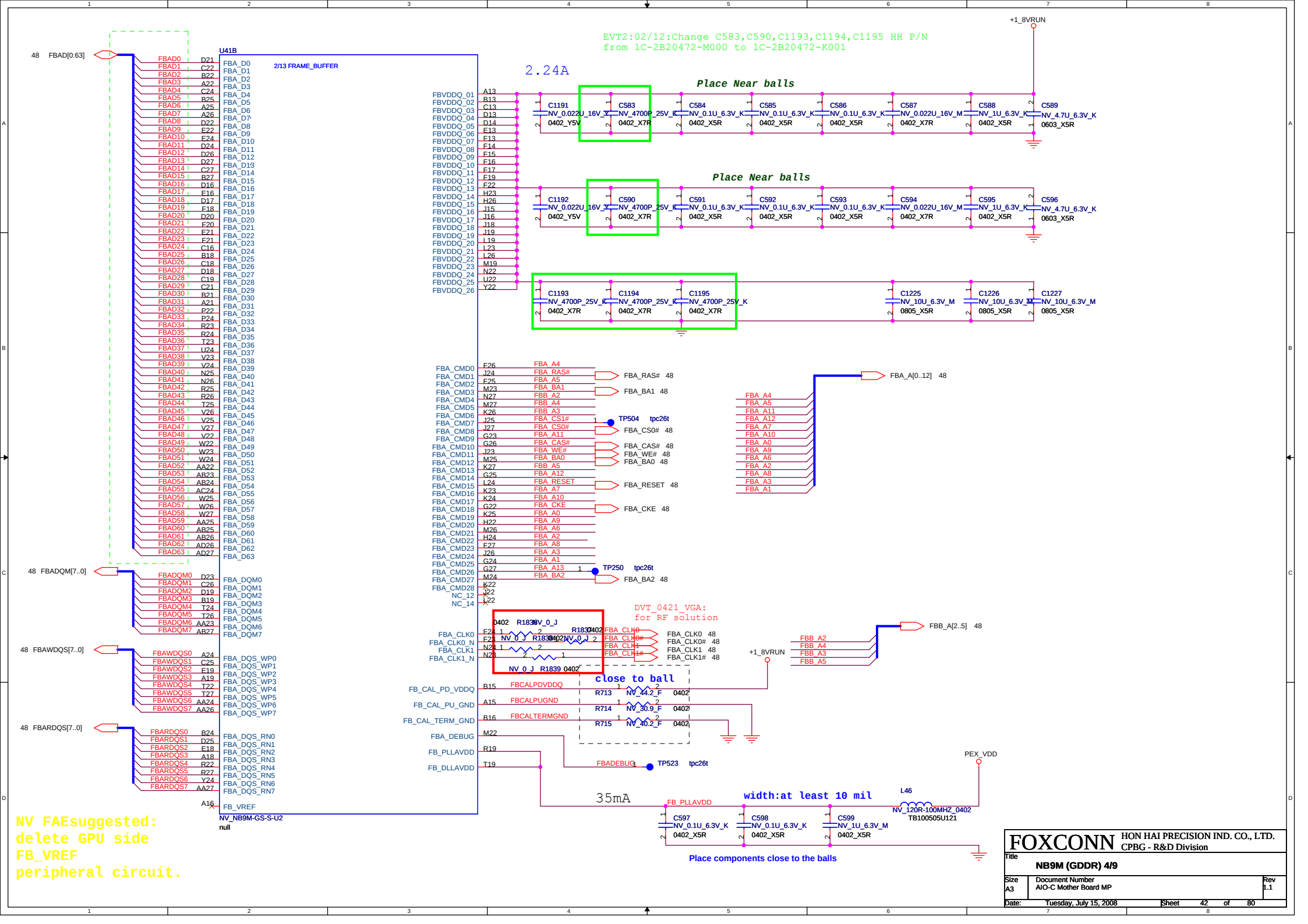
Refer to <GB1 Family Design Guide DG-03276-001_v01_secured>

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: NB9M (PCIE RX&STRAP) 3/9

Size: A3 | Document Number: AIO-C Mother Board MP | Rev: 1.1

Date: Tuesday, July 15, 2008 | Sheet 41 of 80


EVT2:02/12:Change C583,C590,C1193,C1194,C1195 HH P/N from 1C-2B20472-M000 to 1C-2B20472-K001
2.24A
Place Near balls
Place Near balls
U41B
2/13 FRAME_BUFFER
NV_NB9M-GS-S-U2
null
+1_8VRUN
DVT_0421_VGA: for RF solution
close to ball
35mA
width:at least 10 mil
Place components close to the balls
NV FAEsuggested:
delete GPU side
FB_VREF
peripheral circuit.
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
NB9M (GDDR) 4/9
Document Number
AIO-C Mother Board MP
Rev 1.1
Tuesday, July 15, 2008
Sheet 42 of 80

DVT_0422_VGA:
for RF solution

+1_8VRUN
C1477 1 2 +3VRUN NC_5P_50V_C 0402_NPO
C1480 1 2 +5VRUN NC_5P_50V_C 0402_NPO
C1482 1 2 PEX_VDD NC_5P_50V_C 0402_NPO
C1484 1 2 NV_VDD NC_5P_50V_C 0402_NPO
C1485 1 2 +1_1VRUN NC_5P_50V_C 0402_NPO
C1487 1 2 +1_8VSUS NC_5P_50V_C 0402_NPO

+3VRUN
C1478 1 2 NV_VDD NC_5P_50V_C 0402_NPO
C1481 1 2 PEX_VDD NC_5P_50V_C 0402_NPO
C1483 1 2 +1_1VRUN NC_5P_50V_C 0402_NPO

+1_1VRUN
C1486 1 2 VHCORE NC_5P_50V_C 0402_NPO

+1_8VSUS
C1479 1 2 +1_1VRUN NC_5P_50V_C 0402_NPO
C1488 1 2 +5VRUN NC_5P_50V_C 0402_NPO

+3VRUN
L99 NC_NV_220R-100MHZ_0603 FCM1608KF-221T05
width:at least 10 mil
110mA
DACA_VDD
R1862 NV_1K_J 0603
C2622 NC_NV_1U_6.3V_K 0402_X5R
C2623 NC_NV_4700P_25V_K 0402_X7R
C2624 NC_NV_470P_50V_K 0402_X7R
C2625 NC_NV_0.1U_6.3V_K 0402_X5R
DACA_VREF
DACA_RSET
R1863 NC_NV_124_F 0402
EVT2:02/12:Change C618 HH P/N
from 1C-2B20471-M000 to 1C-2B20471-K000

U41C
3/13 DACA
AG2 DACA_VDD
AF1 DACA_VREF
AE1 DACA_RSET
AD2 DACA_HSYNC
AD1 DACA_VSYNC
AE2 DACA_RED
AE3 DACA_GREEN
AD3 DACA_BLUE
NV_NB9M-GS-S-U2
null

NV_DACA_HSYNC 52
NV_DACA_VSYNC 52
50 ohm Trace
NV_DACA_RED 52
NV_DACA_GREEN 52
NV_DACA_BLUE 52
37.5 ohm Trace
R1864 NC_NV_150_F 0402
R1865 NC_NV_150_F 0402
R1866 NC_NV_150_F 0402

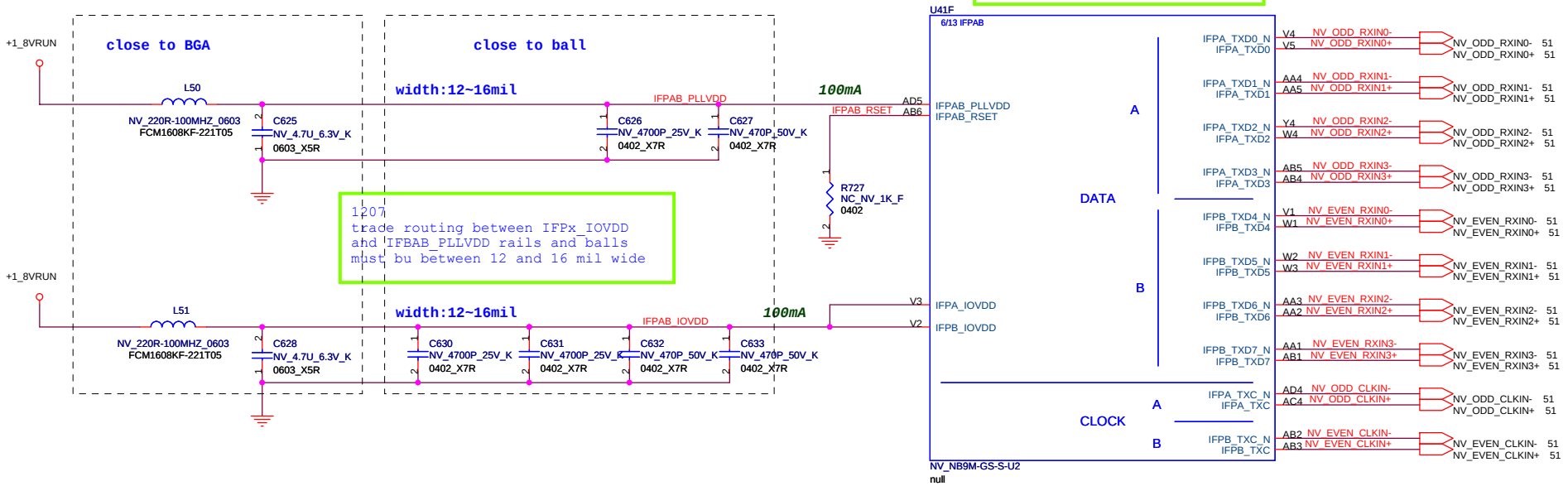
U41D
5/13 DACC
NV_DACC_VDD
R722 NV_1K_J 0603
W5 DACC_VDD
R6 DACC_VREF
V6 DACC_RSET
DACC_HSYNC U6
DACC_VSYNC U4
DACC_RED T5
DACC_GREEN T4
DACC_BLUE R4
NV_NB9M-GS-S-U2
null

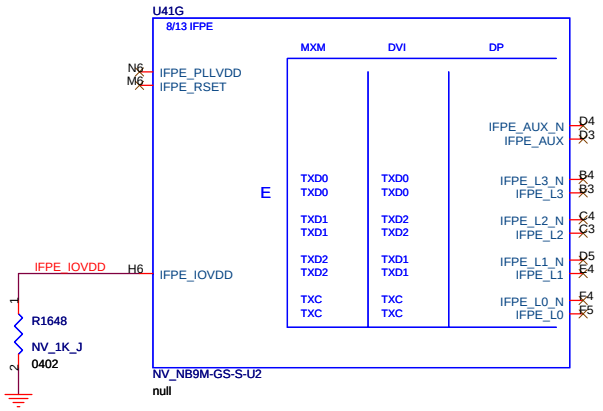
U41E
4/13 DACB
NV_DACB_VDD
R1285 NV_1K_J 0603
D7 DACB_VDD
G6 DACB_VREF
F8 DACB_RSET
DACB_CSYNC D6
DACB_RED E7
DACB_GREEN E7
DACB_BLUE E6
NV_NB9M-GS-S-U2
null

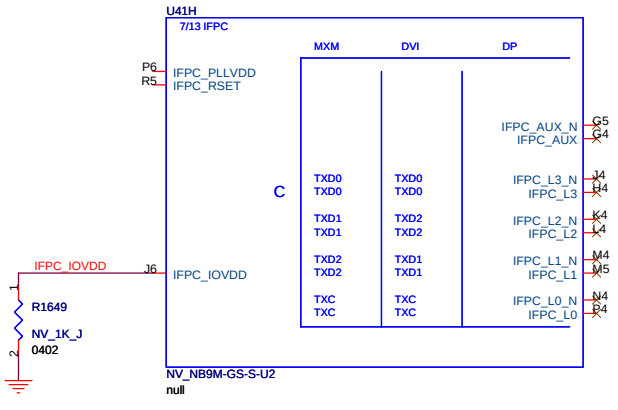
FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

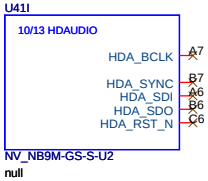
Title	NB9M (CRT)5/9	
Size A3	Document Number AIO-C Mother Board MP	Rev 1.1
Date: Tuesday, July 15, 2008	Sheet 43 of 80	

LVDS: 100ohm +/- 10%

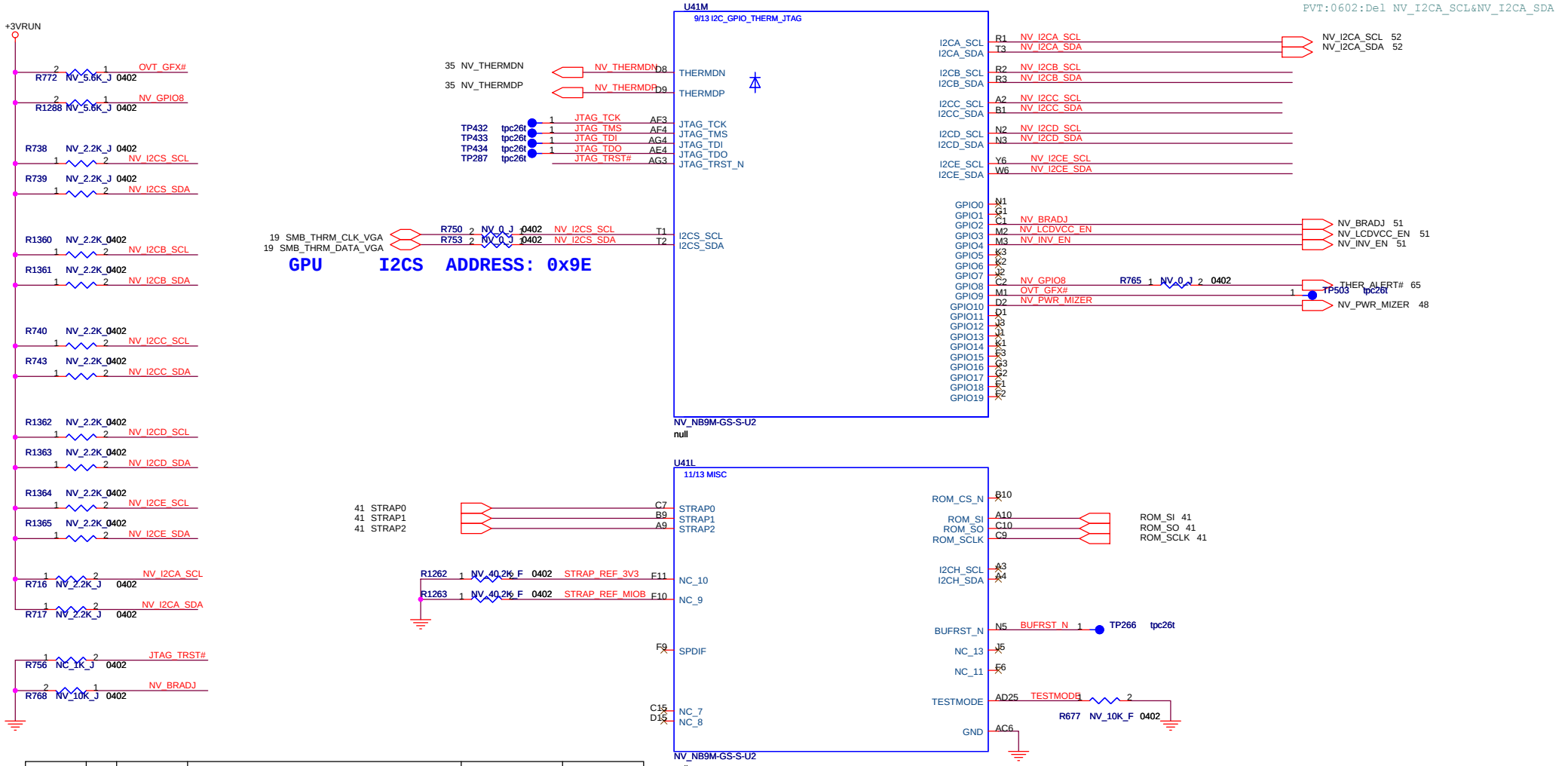








FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	NB9M (LVDS) 6/9	
Size A3	Document Number AIO-C Mother Board MP	Rev 1.1
Date: Tuesday, July 15, 2008	Sheet 44 of 80	



GPIO	I/O	Internal pull low	GPIO TABLE	Active	USE GPIO
GPIO0	n/a		gerneral purpose	n/a	NO
GPIO1	I		HPD-C	-	NO
GPIO2	O		LCD0_BL_PWM	Active High	YES
GPIO3	O		LCD0_VDD	Active high	YES
GPIO4	O		LCD0_BL_EN	Active High	YES
GPIO5	O		GPU_VID0	-	NO
GPIO6	O		GPU_VID1	-	NO
GPIO7	O		GPU_VID2/MEM_VID	-	NO
GPIO8	I/O		OVERT	Active Low	YES
GPIO9	I/O		FAN_PWM/ALERT	Active Low	no
GPIO10	O		MEM_VREF		no
	-	-	-	-	-

External pull-ups and pull-downs, when needed,must be 5-10Kohm

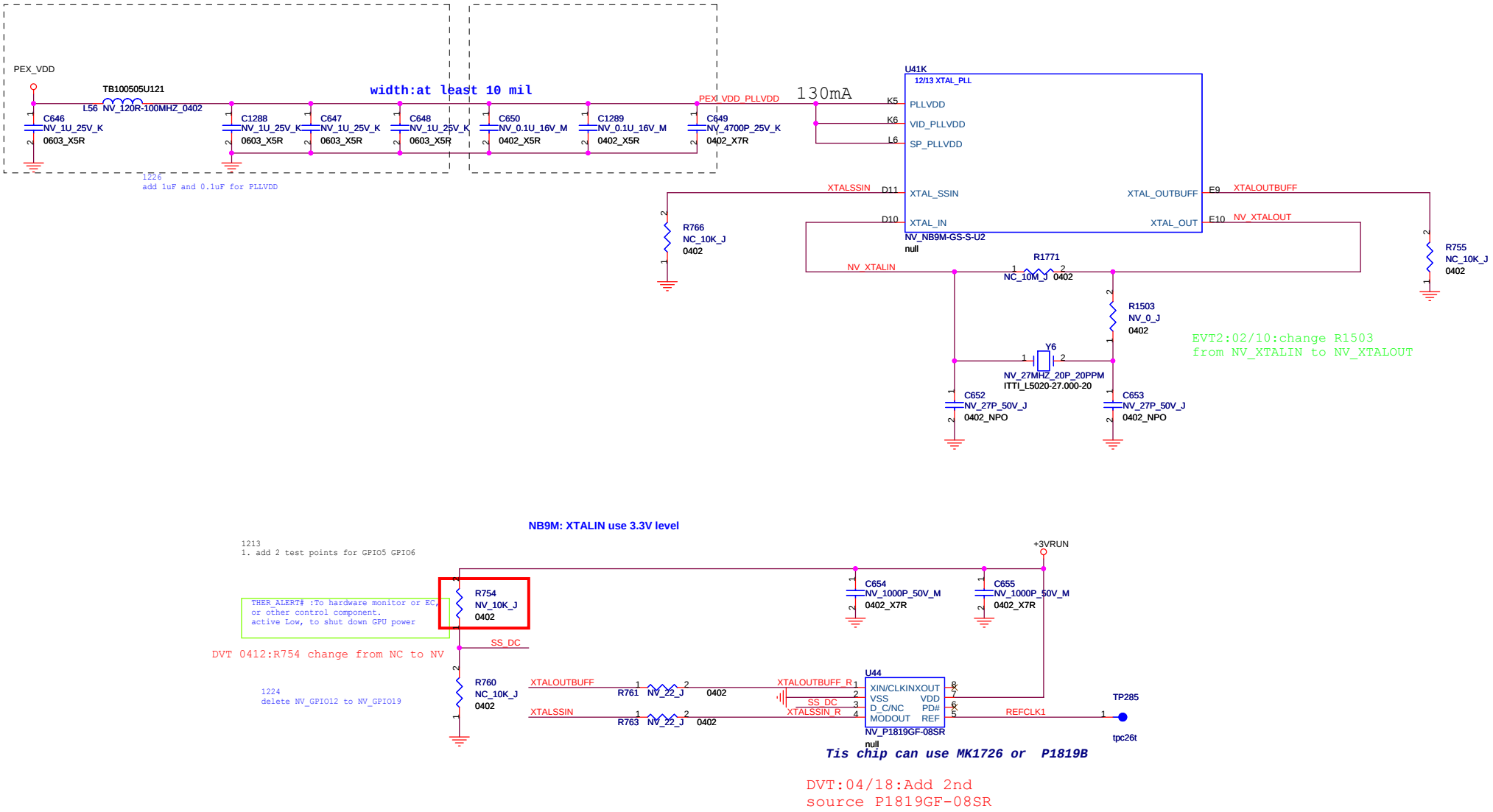
SIGNAL	I/O	Description	USE I2C	Type
I2CA_SCL I2CA_SDA	I/O	Display Interface DDC	YES	Master
I2CB_SCL I2CB_SDA	I/O	Display Interface DDC	NO	Master
I2CC_SCL I2CC_SDA	I/O	Embedded Devices Control	NO	Master
I2CD_SCL I2CD_SDA	I/O	Display Interface DDC	NO	Master
I2CE_SCL I2CE_SDA	I/O	Display Interface DDC	NO	Master
I2CS_SCL I2CS_SDA	I/O	GPU internal I2C thermal sensor. Refer to section 15.1	yes	Slave
I2CH_SCL I2CH_SDA	I/O	HDCP ROM Controler	NO	Master

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

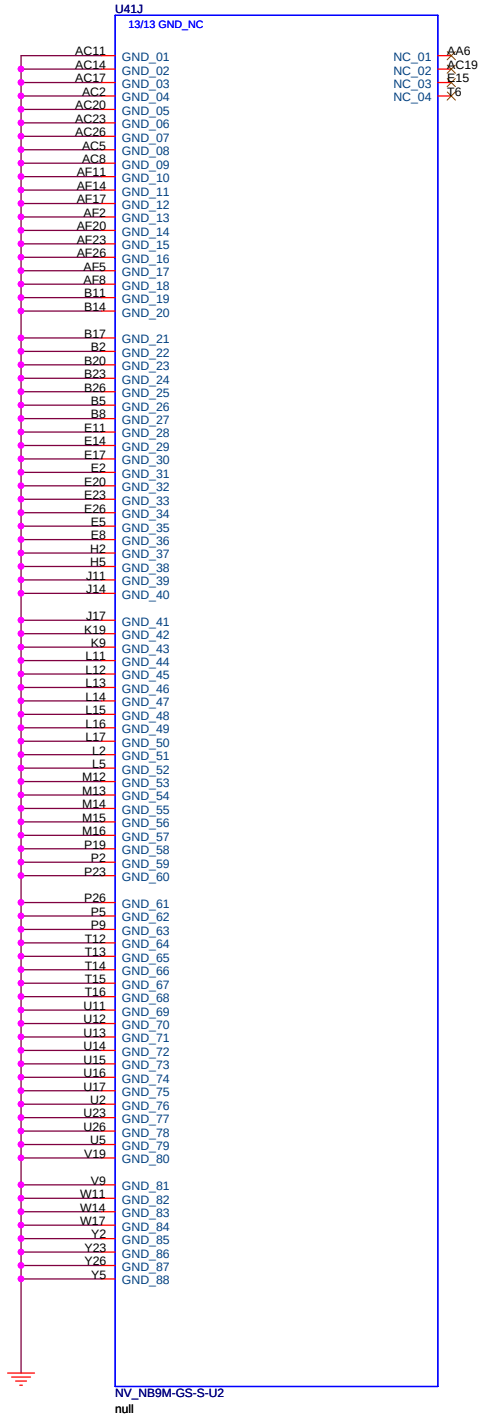
Title: NB9M (XTAL/GPIO) 7/9

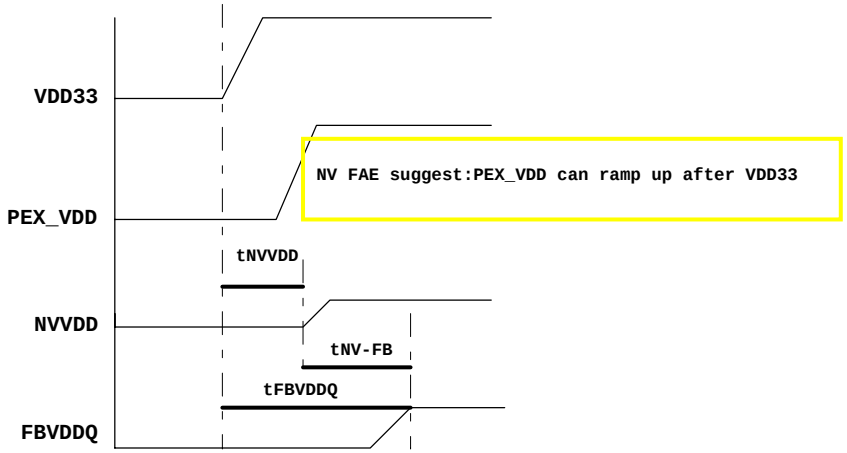
Size: A3 | Document Number: AIO-C Mother Board MP | Rev: 1.1

Date: Tuesday, July 15, 2008 | Sheet 45 of 80



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	NB9M(CRYSTAL&SSIC)8/9	
Size A3	Document Number AIO-C Mother Board MP	Rev 1.1
Date: Tuesday, July 15, 2008	Sheet 46 of 80	





Recommended Power sequencing order

The ramp time for any rail must be more than 40 us
NVVDD<=VDD(3.3V+0.5V)
FBVDDQ<=VDD(3.3V+0.5V)

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: NB9M (GROUND) 9/9		
Size: A3	Document Number: AIO-C Mother Board MP	Rev: 1.1
Date: Tuesday, July 15, 2008	Sheet 47 of 80	

DVT 04/09 :VRAM change from
13-HYB18H1-3000(700M) to
13-HYB18H1-3001(900M)

1228
connect FBA_BA2 to memory BA2.ref NB9x PDP

U59 — NV_SDRAM_PG-TFBGA-136_1G
HYB18H1G321AF-11

U60 — NV_SDRAM_PG-TFBGA-136_1G
HYB18H1G321AF-11

NV_PWR_MIZER	VREF
H	50%
L	70%

R968,R969 (120 ohm-360 ohm)
240 ohm --> Output impedence 40 ohm

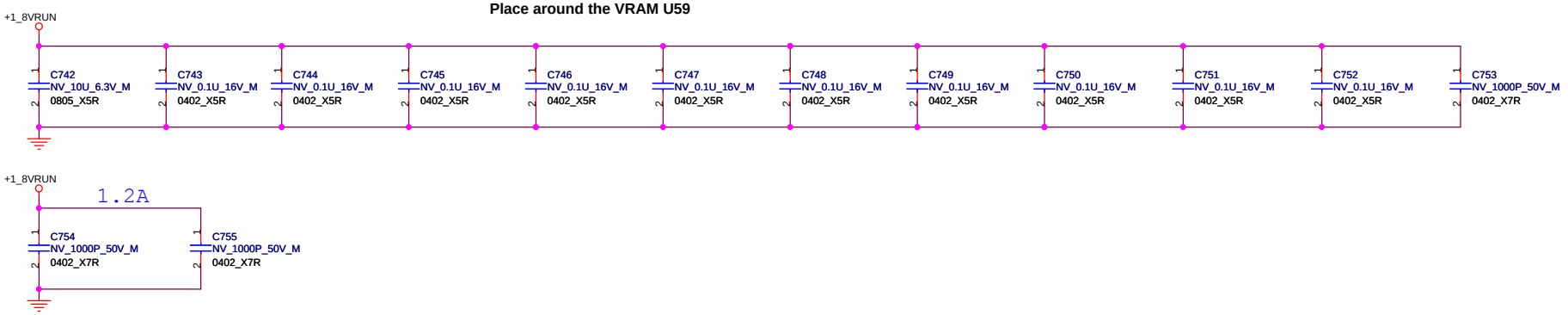
VRAM_VREF is 70%FBVDDQ for GDDR3 1.26V

FAE Suggest: Ball to termination
resistor trace length < 75ps

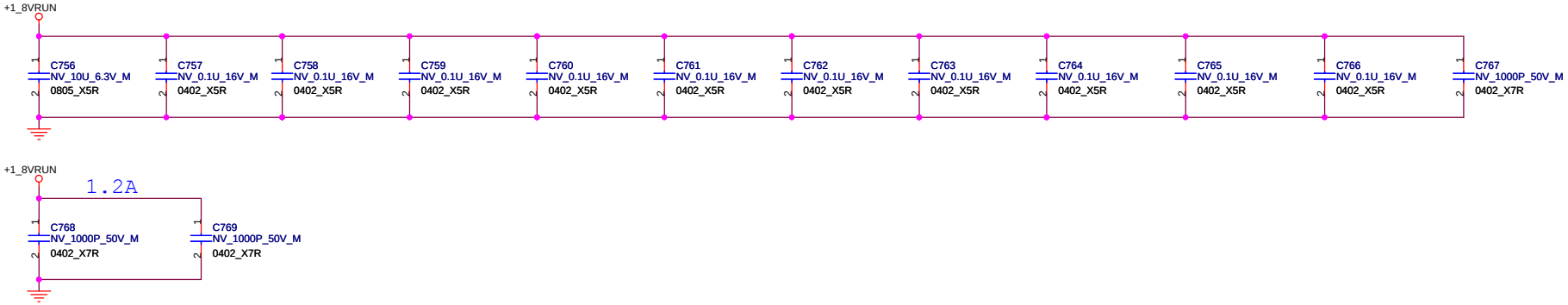
DVT_0421_VGA:
for RF solution

FOXCONN	HON HAI PRECISION IND. CO., LTD.
	CPBG - R&D Division
Title	VRAM(GDDR)
Size A3	Document Number AIO-C Mother Board MP
Rev	1.1
Date:	Tuesday, July 15, 2008
Sheet	48 of 80

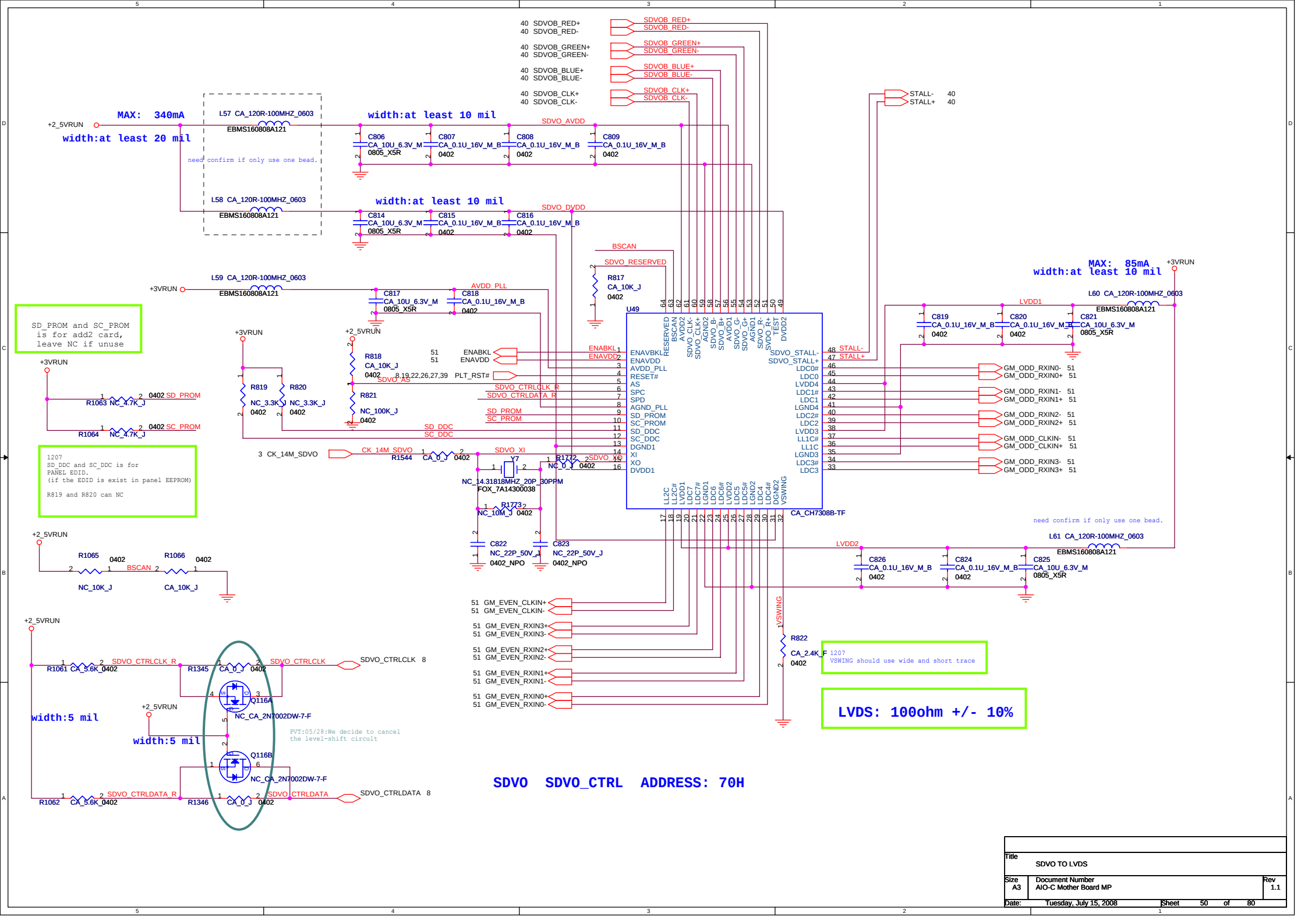
Place around the VRAM U59

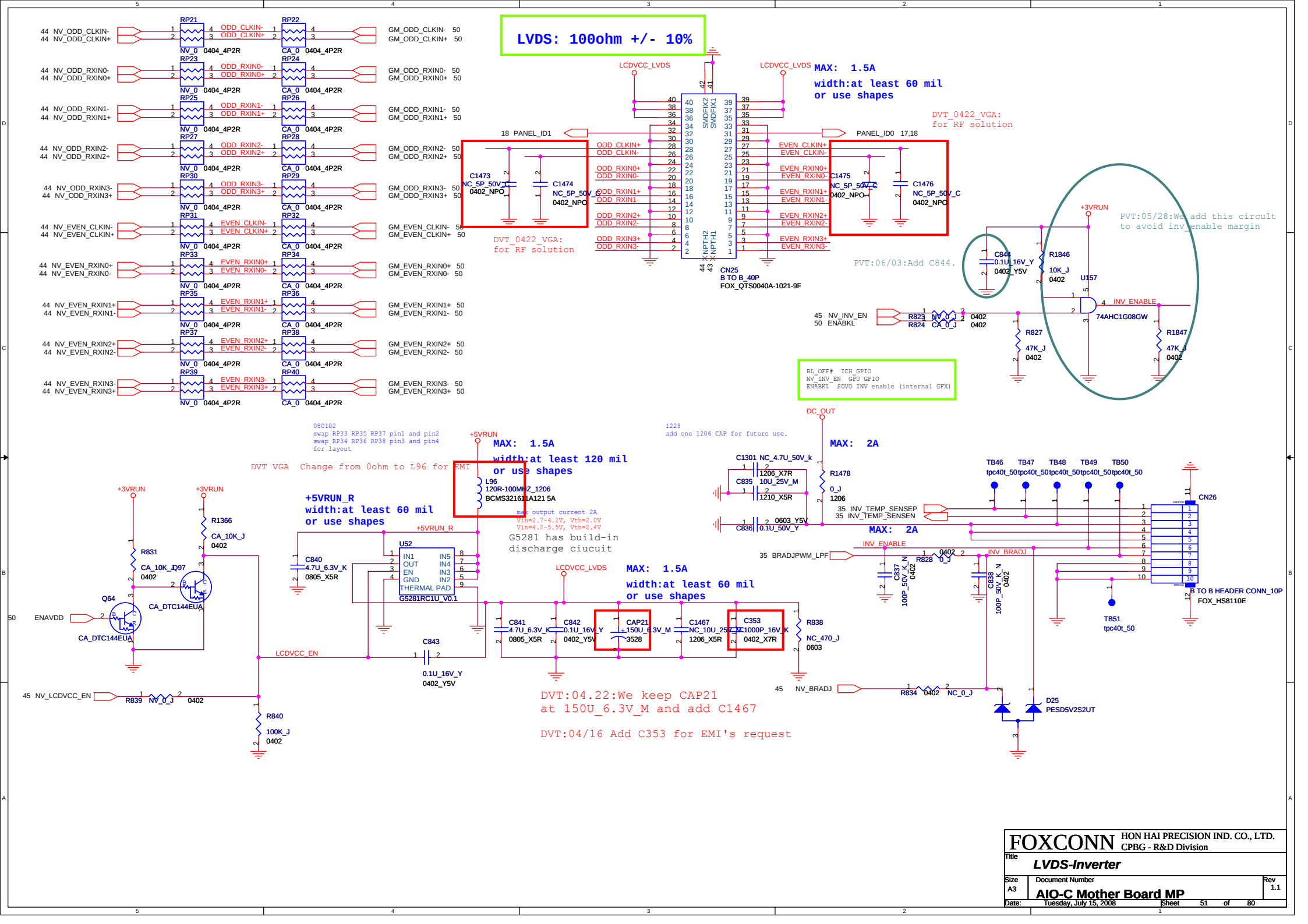


Place around the VRAM U60



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: VRAM(BYPASS)		
Size: A3	Document Number: AIO-C Mother Board MP	Rev: 1.1
Date: Tuesday, July 15, 2008	Sheet 49 of 80	


MAX: 340mA
width:at least 20 mil
+2_5VRUN
L57 CA_120R-100MHZ_0603
EBMS160808A121
need confirm if only use one bead.
L58 CA_120R-100MHZ_0603
EBMS160808A121
width:at least 10 mil
C806 CA_10U_6.3V_M 0805_X5R
C807 CA_0.1U_16V_M_B 0402
C808 CA_0.1U_16V_M_B 0402
C809 CA_0.1U_16V_M_B 0402
SDVO_AVDD
C814 CA_10U_6.3V_M 0805_X5R
C815 CA_0.1U_16V_M_B 0402
C816 CA_0.1U_16V_M_B 0402
SDVO_DVDD
40 SDVOB_RED+
40 SDVOB_RED-
40 SDVOB_GREEN+
40 SDVOB_GREEN-
40 SDVOB_BLUE+
40 SDVOB_BLUE-
40 SDVOB_CLK+
40 SDVOB_CLK-
SDVOB_RED+
SDVOB_RED-
SDVOB_GREEN+
SDVOB_GREEN-
SDVOB_BLUE+
SDVOB_BLUE-
SDVOB_CLK+
SDVOB_CLK-
STALL- 40
STALL+ 40
BSCAN
SDVO_RESERVED
R817 CA_10K_J 0402
U49
CA_CH7308B-TF
RESERVED BSCAN AVDD2 SDVO_CLK- SDVO_CLK+ AGND2 SDVO_B- SDVO_B+ AVDD1 SDVO_G- SDVO_G+ AGND1 SDVO_R- SDVO_R+ TEST DVDD2
ENAVDDKL ENAVDD AVDD_PLL RESET# AS SPC SPD AGND_PLL SD_PROM SC_PROM SD_DDC SC_DDC DGND1 XI XO DVDD1
SDVO_STALL- SDVO_STALL+ LDC0# LDC0 LVDD4 LDC1# LDC1 LGND4 LDC2# LDC2 LVDD3 LL1C# LL1C LGND3 LDC3# LDC3
LL2C LL2C# LVDD1 LDC7 LDC7# LGND1 LDC6 LDC6# LVDD2 LDC5 LDC5# LGND2 LDC4 LDC4# DGND2 VSWING
ENABKL
ENAVDD
PLT_RST#
SDVO_AS
SDVO_CTRLCLK_R
SDVO_CTRLDATA_R
SD_PROM
SC_PROM
SD_DDC
SC_DDC
MAX: 85mA
width:at least 10 mil
+3VRUN
L60 CA_120R-100MHZ_0603
EBMS160808A121
LVDD1
C819 CA_0.1U_16V_M_B 0402
C820 CA_0.1U_16V_M_B 0402
C821 CA_10U_6.3V_M 0805_X5R
GM_ODD_RXIN0- 51
GM_ODD_RXIN0+ 51
GM_ODD_RXIN1- 51
GM_ODD_RXIN1+ 51
GM_ODD_RXIN2- 51
GM_ODD_RXIN2+ 51
GM_ODD_CLKIN- 51
GM_ODD_CLKIN+ 51
GM_ODD_RXIN3- 51
GM_ODD_RXIN3+ 51
need confirm if only use one bead.
L61 CA_120R-100MHZ_0603
EBMS160808A121
LVDD2
C826 CA_0.1U_16V_M_B 0402
C824 CA_0.1U_16V_M_B 0402
C825 CA_10U_6.3V_M 0805_X5R
L59 CA_120R-100MHZ_0603
EBMS160808A121
+3VRUN
AVDD_PLL
C817 CA_10U_6.3V_M 0805_X5R
C818 CA_0.1U_16V_M_B 0402
SD_PROM and SC_PROM is for add2 card, leave NC if unuse
R1063 NC_4.7K_J 0402 SD_PROM
R1064 NC_4.7K_J 0402 SC_PROM
R819 NC_3.3K_J 0402
R820 NC_3.3K_J 0402
R818 CA_10K_J 0402
R821 NC_100K_J 0402
1207
SD_DDC and SC_DDC is for PANEL EDID.
(if the EDID is exist in panel EEPROM)
R819 and R820 can NC
3 CK_14M_SDVO
CK_14M_SDVO
R1544 CA_0_J 0402
SDVO_XI
SDVO_XO
Y7
NC_14.31818MHZ_20P_30PPM
FOX_7A14300038
R1773 NC_10M_J 0402
R1772 NC_0_J 0402
C822 NC_22P_50V_J 0402_NPO
C823 NC_22P_50V_J 0402_NPO
R1065 0402 NC_10K_J
R1066 0402 CA_10K_J
BSCAN
51 GM_EVEN_CLKIN+
51 GM_EVEN_CLKIN-
51 GM_EVEN_RXIN3+
51 GM_EVEN_RXIN3-
51 GM_EVEN_RXIN2+
51 GM_EVEN_RXIN2-
51 GM_EVEN_RXIN1+
51 GM_EVEN_RXIN1-
51 GM_EVEN_RXIN0+
51 GM_EVEN_RXIN0-
R822 CA_2.4K_F 0402
1207
VSWING should use wide and short trace
LVDS: 100ohm +/- 10%
R1061 CA_5.6K_0402
SDVO_CTRLCLK_R
R1345 CA_0_J 0402
SDVO_CTRLCLK
SDVO_CTRLCLK 8
Q116A
NC_CA_2N7002DW-7-F
width:5 mil
Q116B
NC_CA_2N7002DW-7-F
width:5 mil
PVT:05/28:We decide to cancel the level-shift circuit
R1062 CA_5.6K_0402
SDVO_CTRLDATA_R
R1346 CA_0_J 0402
SDVO_CTRLDATA
SDVO_CTRLDATA 8
SDVO CTRL ADDRESS: 70H
Title
SDVO TO LVDS
Size A3
Document Number AIO-C Mother Board MP
Rev 1.1
Date: Tuesday, July 15, 2008
Sheet 50 of 80


LVDS: 100ohm +/- 10%
RP21
RP22
RP23
RP24
RP25
RP26
RP27
RP28
RP30
RP29
RP31
RP32
RP33
RP34
RP35
RP36
RP37
RP38
RP39
RP40
NV_ODD_CLKIN-
NV_ODD_CLKIN+
NV_ODD_RXIN0-
NV_ODD_RXIN0+
NV_ODD_RXIN1-
NV_ODD_RXIN1+
NV_ODD_RXIN2-
NV_ODD_RXIN2+
NV_ODD_RXIN3-
NV_ODD_RXIN3+
NV_EVEN_CLKIN-
NV_EVEN_CLKIN+
NV_EVEN_RXIN0+
NV_EVEN_RXIN0-
NV_EVEN_RXIN1+
NV_EVEN_RXIN1-
NV_EVEN_RXIN2+
NV_EVEN_RXIN2-
NV_EVEN_RXIN3-
NV_EVEN_RXIN3+
0404_4P2R
GM_ODD_CLKIN-
GM_ODD_CLKIN+
GM_ODD_RXIN0-
GM_ODD_RXIN0+
GM_ODD_RXIN1-
GM_ODD_RXIN1+
GM_ODD_RXIN2-
GM_ODD_RXIN2+
GM_ODD_RXIN3-
GM_ODD_RXIN3+
GM_EVEN_CLKIN-
GM_EVEN_CLKIN+
GM_EVEN_RXIN0+
GM_EVEN_RXIN0-
GM_EVEN_RXIN1+
GM_EVEN_RXIN1-
GM_EVEN_RXIN2+
GM_EVEN_RXIN2-
GM_EVEN_RXIN3-
GM_EVEN_RXIN3+
LCDVCC_LVDS
MAX: 1.5A
width:at least 60 mil
or use shapes
DVT_0422_VGA:
for RF solution
18 PANEL_ID1
PANEL_ID0 17,18
C1473
NC_5P_50V_C
0402_NPO
C1474
C1475
C1476
CN25
B TO B_40P
FOX_QTS0040A-1021-9F
PVT:06/03:Add C844.
PVT:05/28:We add this circuit
to avoid inv_enable margin
+3VRUN
C844
0.1U_16V_Y
0402_Y5V
R1846
10K_J
0402
U157
74AHC1G08GW
INV_ENABLE
45 NV_INV_EN
50 ENABKL
R823
R824
NV_0_J
CA_0_J
R827
47K_J
R1847
BL_OFF# ICH_GPIO
NV_INV_EN GPU GPIO
ENABKL SDVO INV enable (internal GFX)
080102
swap RP33 RP35 RP37 pin1 and pin2
swap RP34 RP36 RP38 pin3 and pin4
for layout
DVT VGA Change from 0ohm to L96 for EMI
+5VRUN
MAX: 1.5A
width:at least 120 mil
or use shapes
L96
120R-100MHZ_1206
BCMS321611A121 5A
+5VRUN_R
width:at least 60 mil
or use shapes
max output current 2A
Vin=2.7~4.2V, Vth=2.0V
Vin=4.2~5.5V, Vth=2.4V
G5281 has build-in
discharge ciucuit
U52
IN1
OUT
EN
GND
IN5
IN4
IN3
IN2
THERMAL PAD
G5281RC1U_V0.1
C840
4.7U_6.3V_K
0805_X5R
C841
C842
0.1U_16V_Y
0402_Y5V
CAP21
150U_6.3V_M
3528
C1467
NC_10U_25V_M
1206_X5R
C353
1000P_16V_K
0402_X7R
R838
NC_470_J
0603
C843
0.1U_16V_Y
0402_Y5V
LCDVCC_EN
MAX: 1.5A
width:at least 60 mil
or use shapes
DVT:04.22:We keep CAP21
at 150U_6.3V_M and add C1467
DVT:04/16 Add C353 for EMI's request
1228
add one 1206 CAP for future use.
DC_OUT
MAX: 2A
C1301 NC_4.7U_50V_k
1206_X7R
C835 10U_25V_M
1210_X5R
C836 0.1U_50V_Y
0603_Y5V
R1478
0_J
1206
35 INV_TEMP_SENSEP
35 INV_TEMP_SENSEN
TB46
TB47
TB48
TB49
TB50
tpc40t_50
CN26
B TO B HEADER CONN_10P
FOX_HS8110E
TB51
tpc40t_50
35 BRADJPWM_LPF
INV_ENABLE
INV_BRADJ
R828
C837
C838
100P_50V_K_N
0402
+3VRUN
R1366
CA_10K_J
0402
R831
CA_10K_J
0402
Q97
Q64
CA_DTC144EUA
50 ENAVDD
45 NV_LCDVCC_EN
R839
NV_0_J
R840
100K_J
0402
45 NV_BRADJ
R834
NC_0_J
D25
PESD5V2S2UT
FOXCONN
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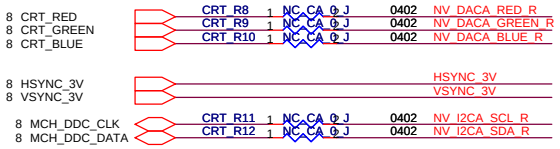
CPBG - R&D Division
Title
LVDS-Inverter
Size
A3
Document Number
AIO-C Mother Board MP
Rev
1.1
Date:
Tuesday, July 15, 2008
Sheet
51
of
80

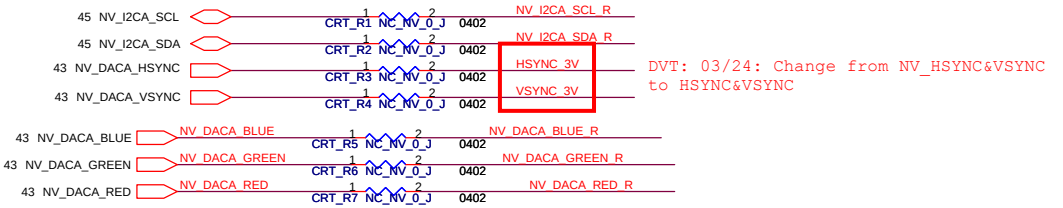
close to NB

confirm NB had use 150_F Ohm pull down to GND

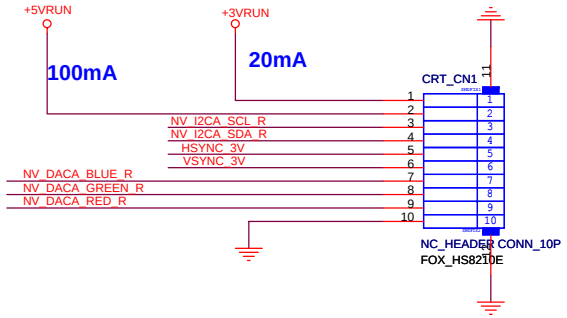


1224
change head value of CRT_R*

close to NV GPU



DVT: 03/24: Change from NV_HSYNC&VSYNC to HSYNC&VSYNC



CONN ON MB

1220
page 40:. add 22uF cap for NVVDD
page 49 :. add level shifter Q for 2.5V to 3.3V, change Y7 to a small size.
page 50:. add 0_J for LCD 5V power, add 0_J for DC_OUT, NC U53 and R830 , stuff R836.

1225
change NV_NB9M-GS(GB1-64) source package from NB9M_GS_GB1_64 to NB9M_GS_GB1_64_B
page 45 add test pad for OVT_GFX#,

1228
page 50:add one 1206 CAP for future use.
page 40:change CAP46.
page 41: 2 resistors for strap0.
page 42: add tp for FBA_CS1#, connect GPU CMD27 to memory BA2.
page 46:. add Recommended Power sequencing order

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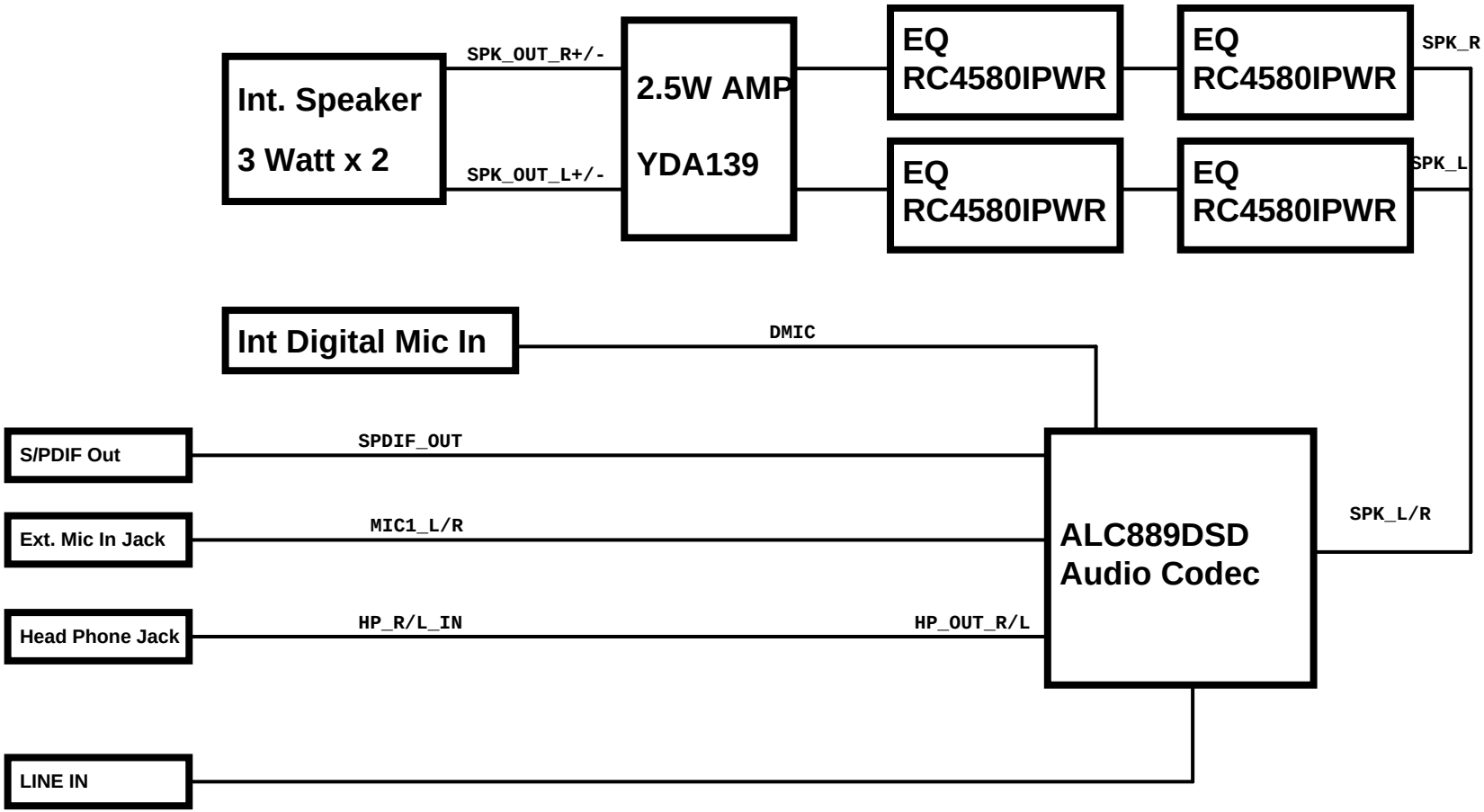
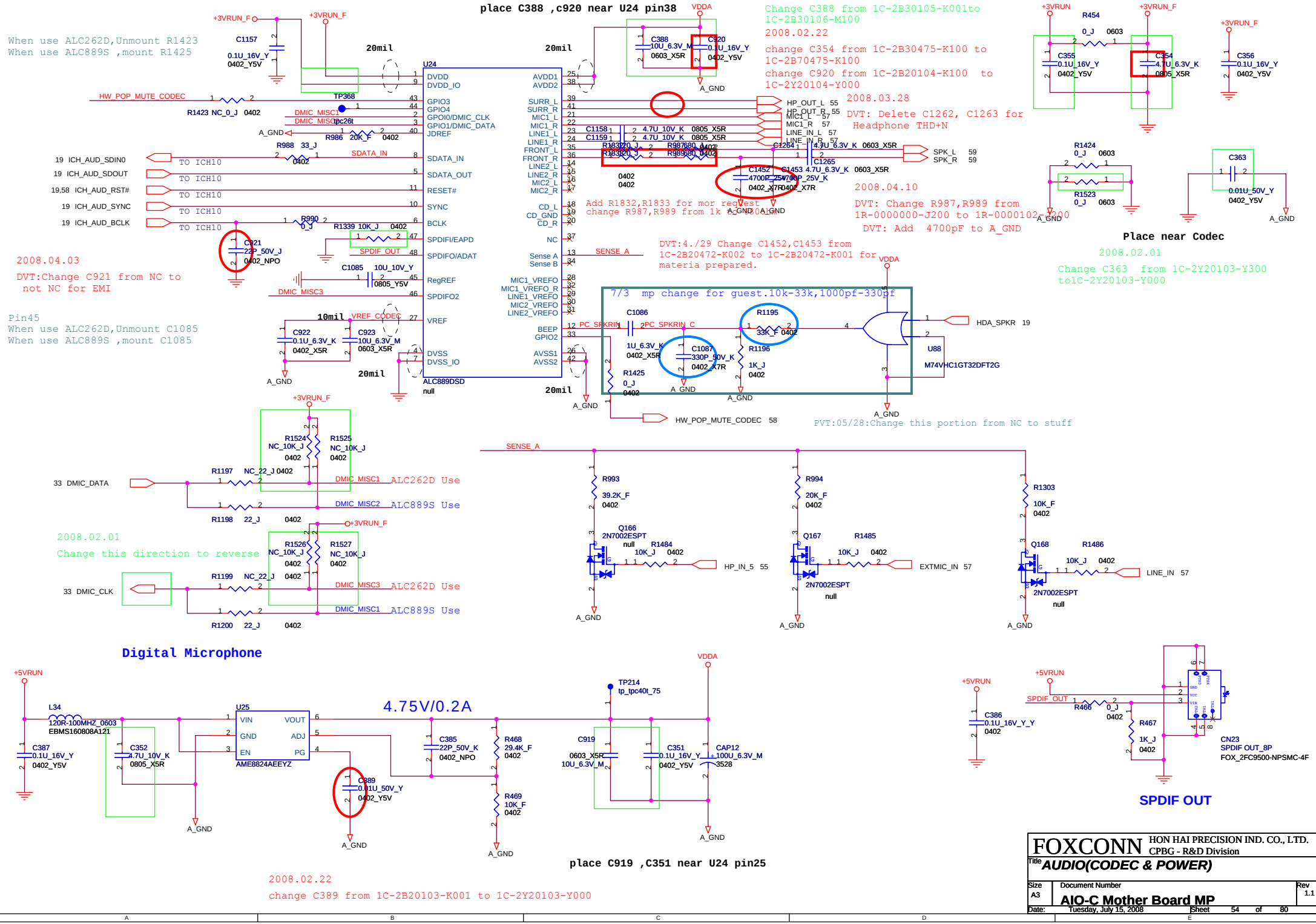
Title: CRT		
Size: A3	Document Number: AIO-C Mother Board MP	Rev: 1.1
Date: Tuesday, July 15, 2008	Sheet 52 of 80	

AIO-C Audio Block Diagram



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	***Block Diagram (All)***	
Size A3	Document Number **AIO-C Mother Board MP**	Rev 1.1
Date:	Tuesday, July 15, 2008	Sheet 53 of 80


DVT: Change U24 name from ALC889S to ALC889DSD
place C388 ,c920 near U24 pin38
2008.01.31
Change C388 from 1C-2B30105-K001to 1C-2B30106-M100
2008.02.22
change C354 from 1C-2B30475-K100 to 1C-2B70475-K100
change C920 from 1C-2B20104-K100 to 1C-2Y20104-Y000
2008.03.28
DVT: Delete C1262, C1263 for Headphone THD+N
When use ALC262D,Unmount R1423
When use ALC889S ,mount R1425
20mil
U24
ALC889DSD
null
TP368
HW_POP_MUTE_CODEC
R1423 NC_0_J 0402
DMIC_MISC1
DMIC_MISC2
R986 20K_F 0402
R988 33_J 0402
SDATA_IN
TO ICH10
19 ICH_AUD_SDIN0
19 ICH_AUD_SDOUT
19,58 ICH_AUD_RST#
19 ICH_AUD_SYNC
19 ICH_AUD_BCLK
R990 0_J
R1339 10K_J 0402
SPDIF_OUT
C921 220P_50V_J 0402_NPO
2008.04.03
DVT:Change C921 from NC to not NC for EMI
C1085 10U_10V_Y 0805_Y5V
DMIC_MISC3
Pin45
When use ALC262D,Unmount C1085
When use ALC889S ,mount C1085
10mil
VREF_CODEC
C922 0.1U_6.3V_K 0402_X5R
C923 10U_6.3V_M 0603_X5R
C1158 4.7U_10V_K 0805_X5R
C1159 4.7U_10V_K 0805_X5R
R1833 20_J 0402
R987 680_J 0402
R989 680_J 0402
C1264 4.7U_6.3V_K 0603_X5R
C1265
C1452 4700P_25V_K 0402_X7R
C1453 4700P_25V_K 0402_X7R
HP_OUT_L 55
HP_OUT_R 55
MIC1_L 57
MIC1_R 57
LINE_IN_L 57
LINE_IN_R 57
SPK_L 59
SPK_R 59
Add R1832,R1833 for mor request
change R987,R989 from 1k to 680
2008.04.10
DVT: Change R987,R989 from 1R-0000000-J200 to 1R-0000102-J200
DVT: Add 4700pF to A_GND
DVT:4./29 Change C1452,C1453 from 1C-2B20472-K002 to 1C-2B20472-K001 for materia prepared.
SENSE_A
7/3 mp change for guest.10k-33k,1000pf-330pf
C1086 1U_6.3V_K 0402_X5R
R1195 33K_F 0402
C1087 330P_50V_K 0402_X7R
R1196 1K_J 0402
R1425 0_J 0402
U88
M74VHC1GT32DFT2G
HDA_SPKR 19
PC_SPKRIN
HW_POP_MUTE_CODEC 58
PVT:05/28:Change this portion from NC to stuff
R454 0_J 0603
C355 0.1U_16V_Y 0402_Y5V
C354 4.7U_6.3V_K 0805_X5R
C356 0.1U_16V_Y 0402_Y5V
R1424 0_J 0603
R1523 0_J 0603
C363 0.01U_50V_Y 0402_Y5V
Place near Codec
2008.02.01
Change C363 from 1C-2Y20103-Y300 to1C-2Y20103-Y000
R1524 NC_10K_J 0402
R1525 NC_10K_J 0402
R1197 NC_22_J 0402
R1198 22_J 0402
33 DMIC_DATA
ALC262D Use
ALC889S Use
2008.02.01
Change this direction to reverse
R1526 NC_10K_J 0402
R1527 NC_10K_J 0402
R1199 NC_22_J 0402
R1200 22_J 0402
33 DMIC_CLK
Digital Microphone
R993 39.2K_F 0402
R994 20K_F 0402
R1303 10K_F 0402
Q166 2N7002ESPT null
Q167 2N7002ESPT null
Q168 2N7002ESPT null
R1484 10K_J 0402
R1485 10K_J 0402
R1486 10K_J 0402
HP_IN_5 55
EXTMIC_IN 57
LINE_IN 57
L34 120R-100MHZ_0603 EBMS160808A121
U25 AME8824AEEYZ
4.75V/0.2A
C387 0.1U_16V_Y 0402_Y5V
C352 4.7U_10V_K 0805_X5R
C385 22P_50V_K 0402_NPO
C389 0.01U_50V_Y 0402_Y5V
R468 29.4K_F 0402
R469 10K_F 0402
TP214 tp_tpc40t_75
C919 10U_6.3V_M 0603_X5R
C351 0.1U_16V_Y 0402_Y5V
CAP12 100U_6.3V_M 3528
place C919 ,C351 near U24 pin25
2008.02.22
change C389 from 1C-2B20103-K001 to 1C-2Y20103-Y000
C386 0.1U_16V_Y_Y 0402
R466 0_J 0402
R467 1K_J 0402
CN23 SPDIF OUT_8P FOX_2FC9500-NPSMC-4F
SPDIF OUT
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
Title AUDIO(CODEC & POWER)
Size A3
Document Number AIO-C Mother Board MP
Rev 1.1
Date: Tuesday, July 15, 2008
Sheet 54 of 80

2008.02.22

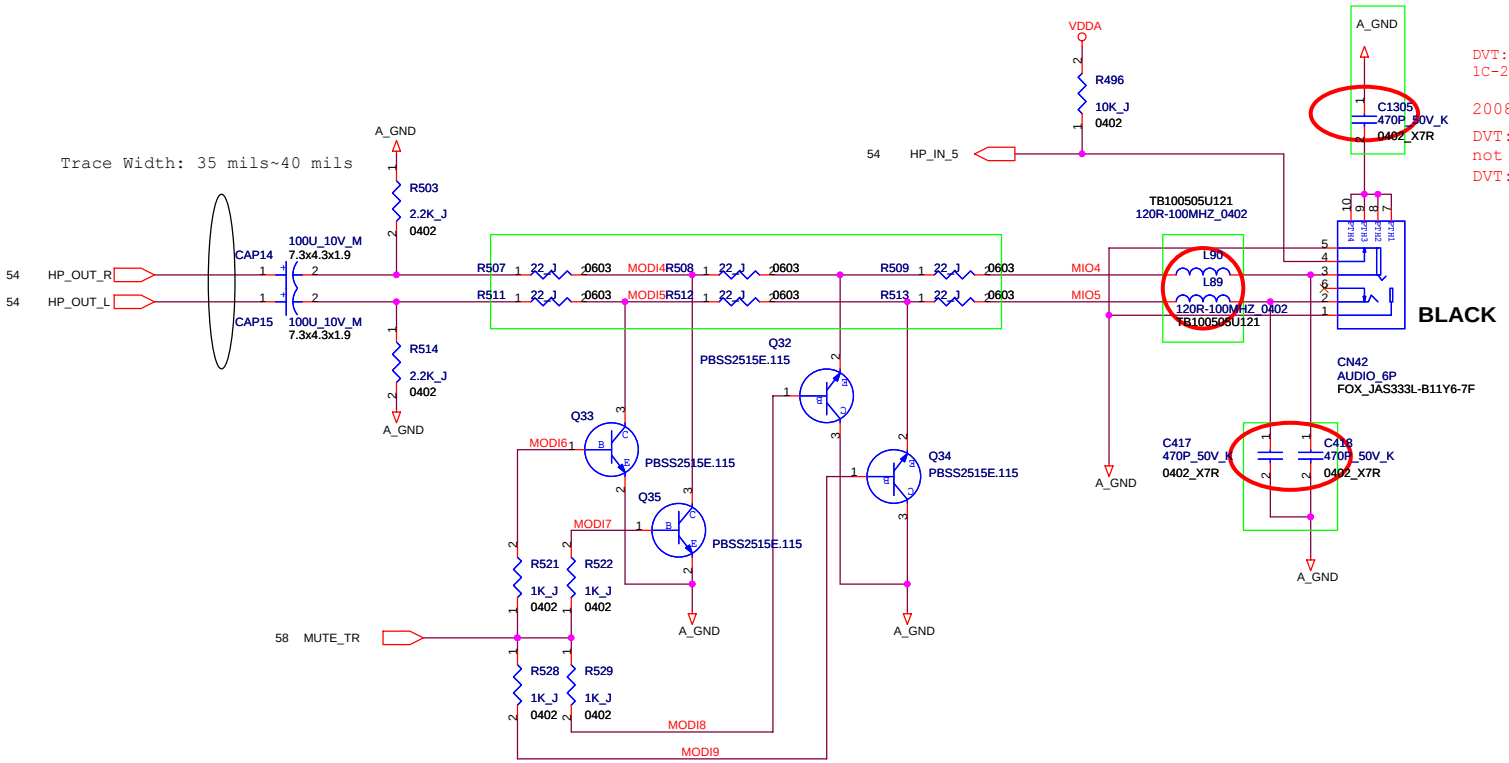
change C1305 from 1C-2B20471-K000 to 1C-2B20471-K200

DVT:04/28:Change C1305 from 1C-2B20471-K200 to 1C-2B20471-K000

2008.04.03

DVT:Change C1305 C417,C418 from NC to not NC for EMI

DVT:change R1530,R1531 to L?,L? for EMI



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	AUDIO(HP)	
Size	Document Number: AIO-C Mother Board MP	Rev 1.1
Date: Tuesday, July 15, 2008	Sheet 55 of 80	

2008.01.26
Change C1376, C1377 from 0.22U_6.3V_K to 0.1U_6.3V_K
2008.01.28
Change R1627 from 10K_J to NC_10K_J

2008.01.26
Change C1378 from 1C-2B70105-M000 to 1C-2B30225-M201
2008.02.01
Change R1624 from 1R-0000103-J200 to 1R-0000473-J200

PVT:06/10:change R1546 from 1R-0000103-J201
to 1R-0000103-J200 for pur request.

2008.01.28
Change R1629 from NC_10K_J to 10K_J

2008.04.17
DVT:Delete L80, L82, L84,L86,C1385,C1391,C1390,1394for YAMAHA's request
DVT:Change C1387 & C1393 from 0.33uF to 0.47uF for YAMAHA's request
DVT:Change C1386 & C1388 & C1392 & C1396 from 0.22uF to 0.047uF for YAMAHA's request
DVT:Add Schottky-Diode to preventing the destruction of amp.when the output line short-circuits.

Put D48 ,D49 near to U92
pin14,pin15,pin16 , put D50,D51
near to U92 pin9,pin10,pin11

PVT:0708:update the

2008.02.01
Change L80,L82,L84,L86 from 1L-BEBMS10-0500 to 1L-BACMS16-0804
2008.03.01
Change L80,L82,L84,L86 from 1L-BACMS16-0804 to 1L-BACMS16-0807

0122
Delete C1381 22U_16V_M
Delete C1384 22U_16V_M
Add CAP50 220U_6.3V_7343 for MOR's request

2008.04.10
DVT: Change this latch circuit to NC
DVT:04/14:Delete Q115,add Q170,Q171

2008.04.24
dvt: Add C1468 for mor request

DVT: Add 0_j for mor request

2008.02.18
Delete PQ75,PQ76,PR248 of protective
circuit for MOR repuest

0122
Add FUSE 24V-3.15A_0603
Add bead for MOR's require

Close to each other,do
not make ground loop

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	AUDIO (SPK & AMP)	
Size	Document Number: AIO-C Mother Board MP	Rev: 1.1
Date: Tuesday, July 15, 2008	Sheet 56 of 80	

2008.02.18

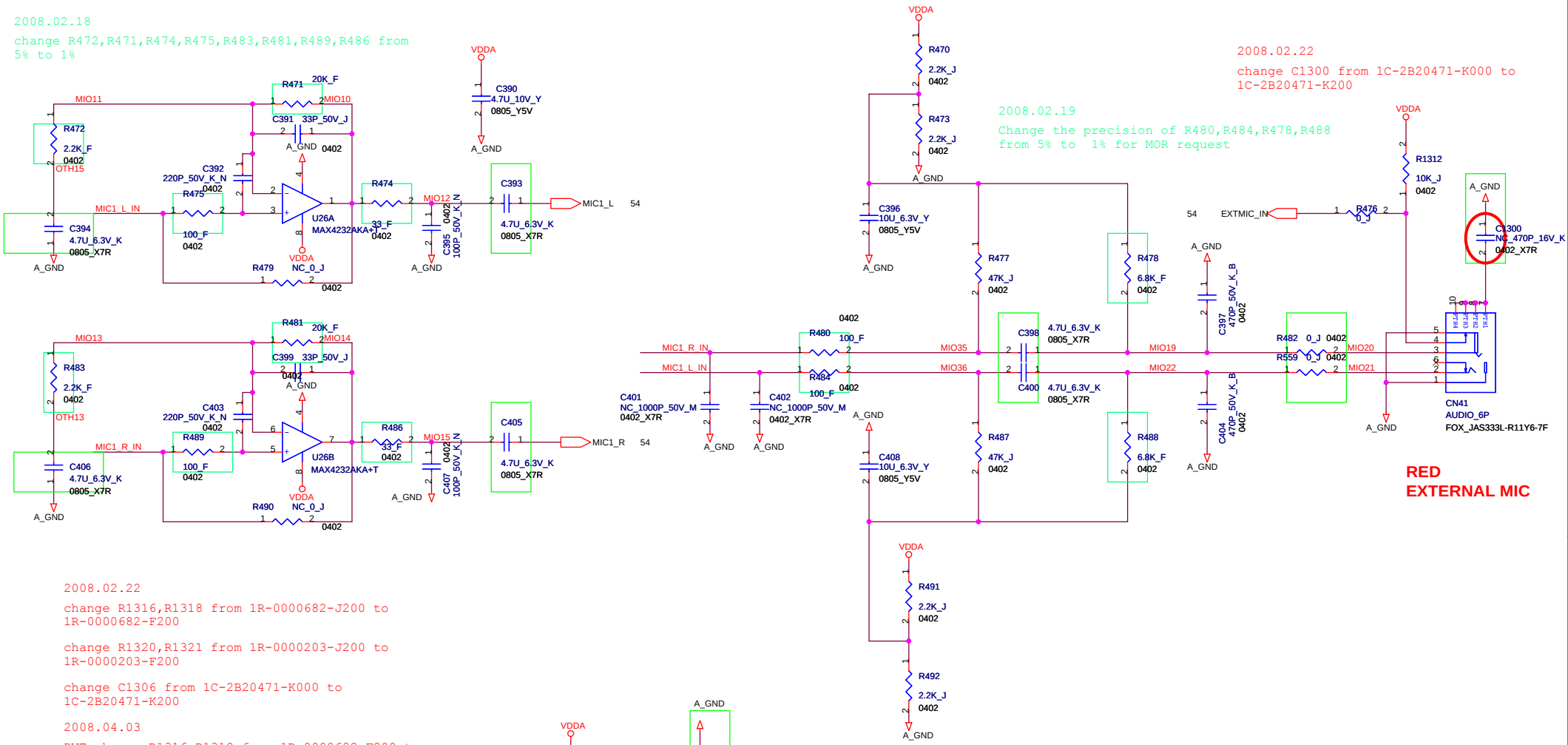
change R472,R471,R474,R475,R483,R481,R489,R486 from 5% to 1%

2008.02.19

Change the precision of R480,R484,R478,R488 from 5% to 1% for MOR request

2008.02.22

change C1300 from 1C-2B20471-K000 to 1C-2B20471-K200



2008.02.22

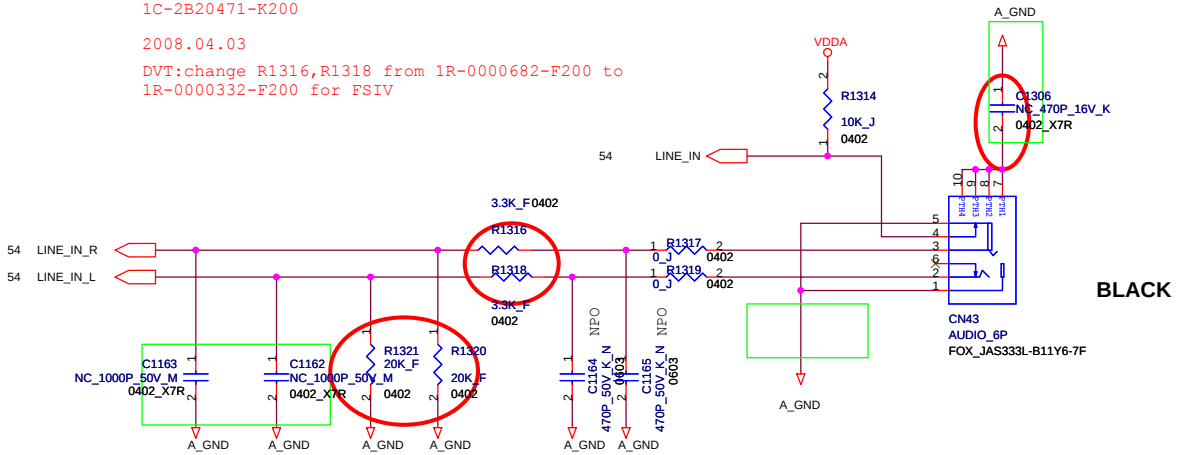
change R1316,R1318 from 1R-0000682-J200 to 1R-0000682-F200

change R1320,R1321 from 1R-0000203-J200 to 1R-0000203-F200

change C1306 from 1C-2B20471-K000 to 1C-2B20471-K200

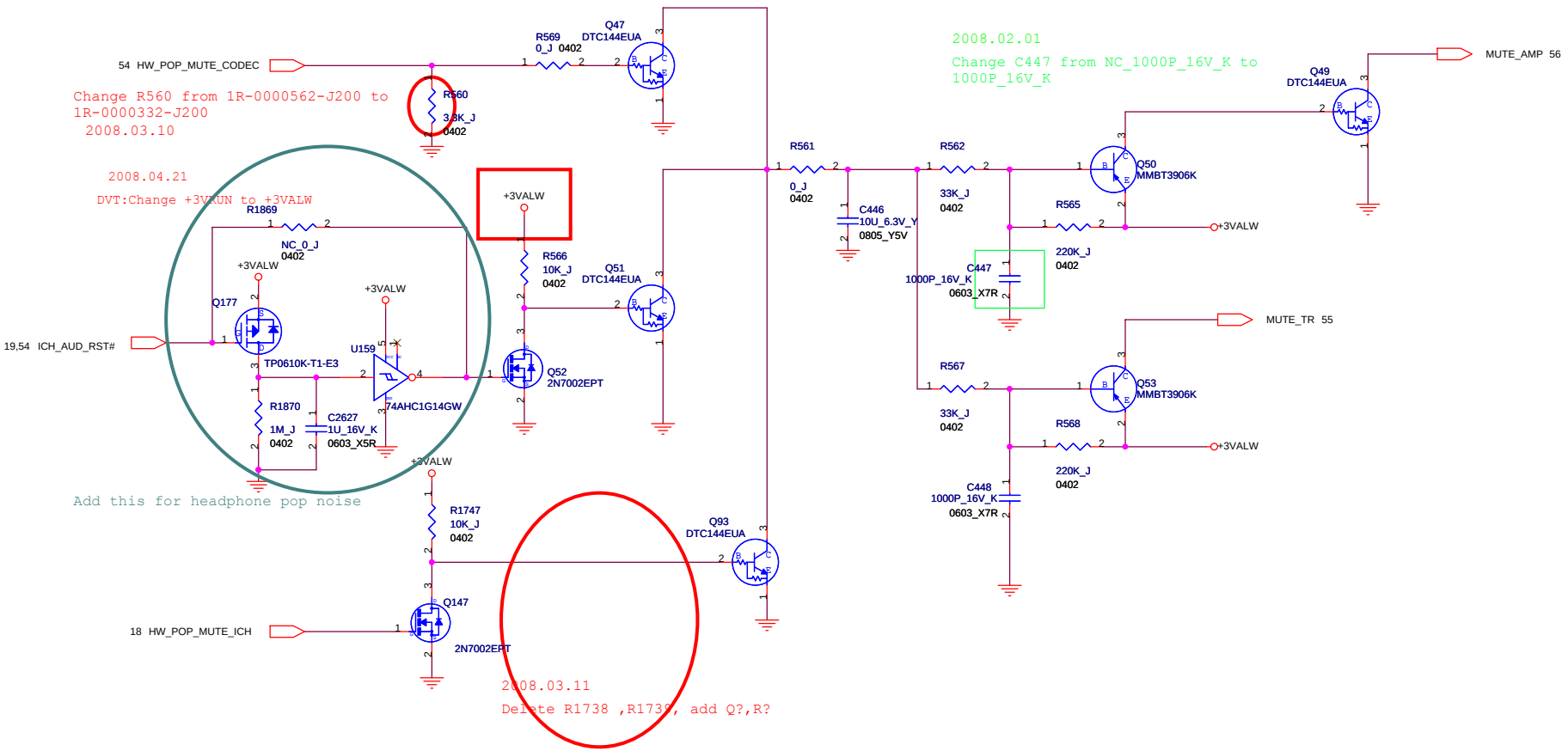
2008.04.03

DVT:change R1316,R1318 from 1R-0000682-F200 to 1R-0000332-F200 for FSIV

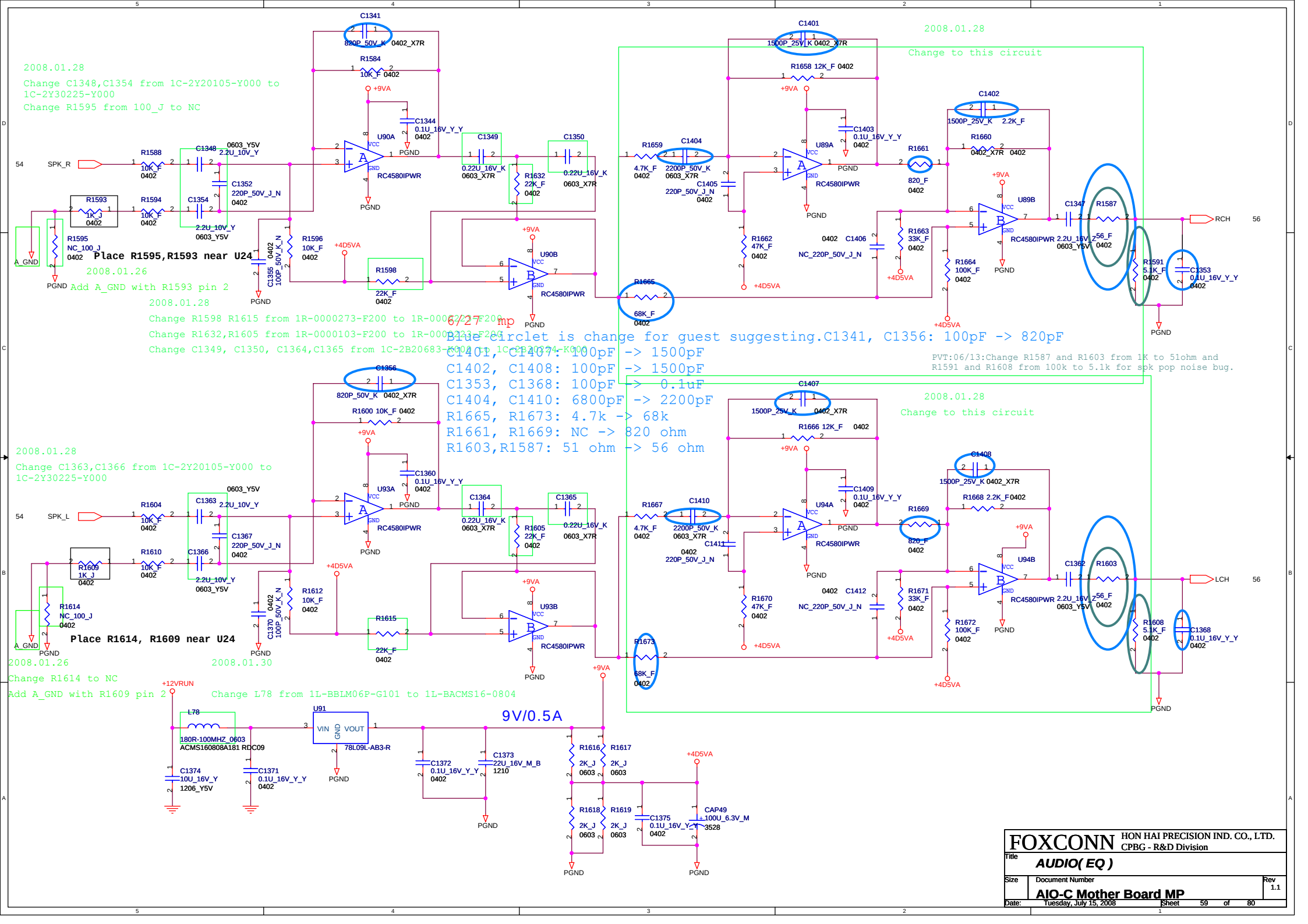


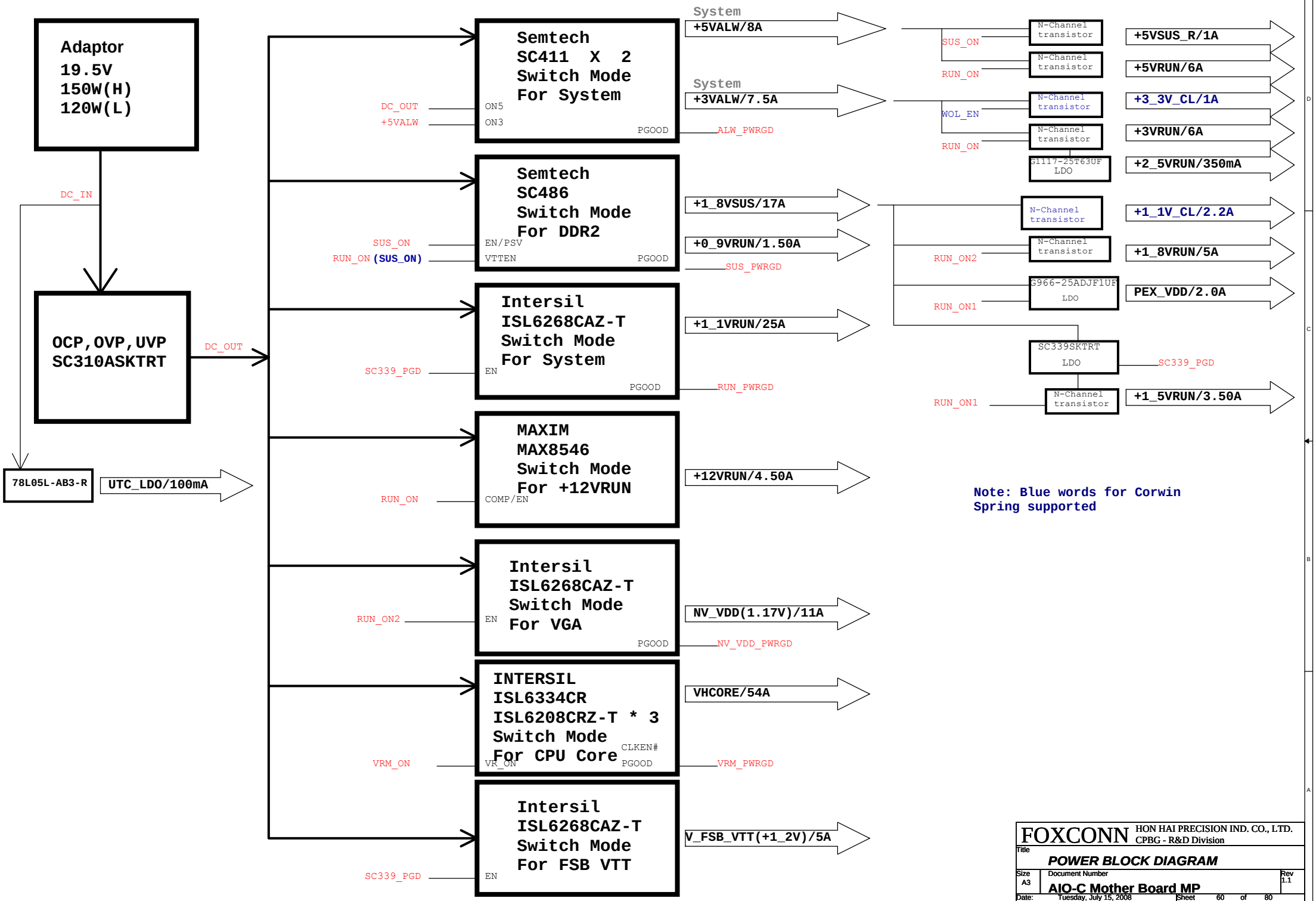
LINE IN

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title	AUDIO(EXT MIC & LINE IN)		
Size A3	Document Number AIO-C Mother Board MP		Rev 1.1
Date: Tuesday, July 15, 2008	Sheet 57 of 80		



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: AUDIO (MUTE)		
Size	Document Number: AIO-C Mother Board MP	Rev: 1.1
Date: Tuesday, July 15, 2008	Sheet 58 of 80	


2008.01.28
Change C1348,C1354 from 1C-2Y20105-Y000 to 1C-2Y30225-Y000
Change R1595 from 100_J to NC
Place R1595,R1593 near U24
2008.01.26
Add A_GND with R1593 pin 2
2008.01.28
Change R1598 R1615 from 1R-0000273-F200 to 1R-0000223-F200
Change R1632,R1605 from 1R-0000103-F200 to 1R-0000223-F200
Change C1349, C1350, C1364,C1365 from 1C-2B20683-K000 to 1C-2B20224-K000
6/27 mp
Blue circlet is change for guest suggesting.C1341, C1356: 100pF -> 820pF
C1401, C1407: 100pF -> 1500pF
C1402, C1408: 100pF -> 1500pF
C1353, C1368: 100pF -> 0.1uF
C1404, C1410: 6800pF -> 2200pF
R1665, R1673: 4.7k -> 68k
R1661, R1669: NC -> 820 ohm
R1603,R1587: 51 ohm -> 56 ohm
2008.01.28
Change to this circuit
PVT:06/13:Change R1587 and R1603 from 1K to 51ohm and R1591 and R1608 from 100k to 5.1k for sok pop noise bug.
2008.01.28
Change C1363,C1366 from 1C-2Y20105-Y000 to 1C-2Y30225-Y000
Place R1614, R1609 near U24
2008.01.26
Change R1614 to NC
2008.01.30
Add A_GND with R1609 pin 2
Change L78 from 1L-BBLM06P-G101 to 1L-BACMS16-0804
9V/0.5A
SPK_R
SPK_L
RCH
LCH
RC4580IPWR
78L09L-AB3-R
180R-100MHZ_0603
ACMS160808A181 RDC09
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
Title
AUDIO(EQ)
Size
Document Number
AIO-C Mother Board MP
Rev
1.1
Date: Tuesday, July 15, 2008
Sheet 59 of 80

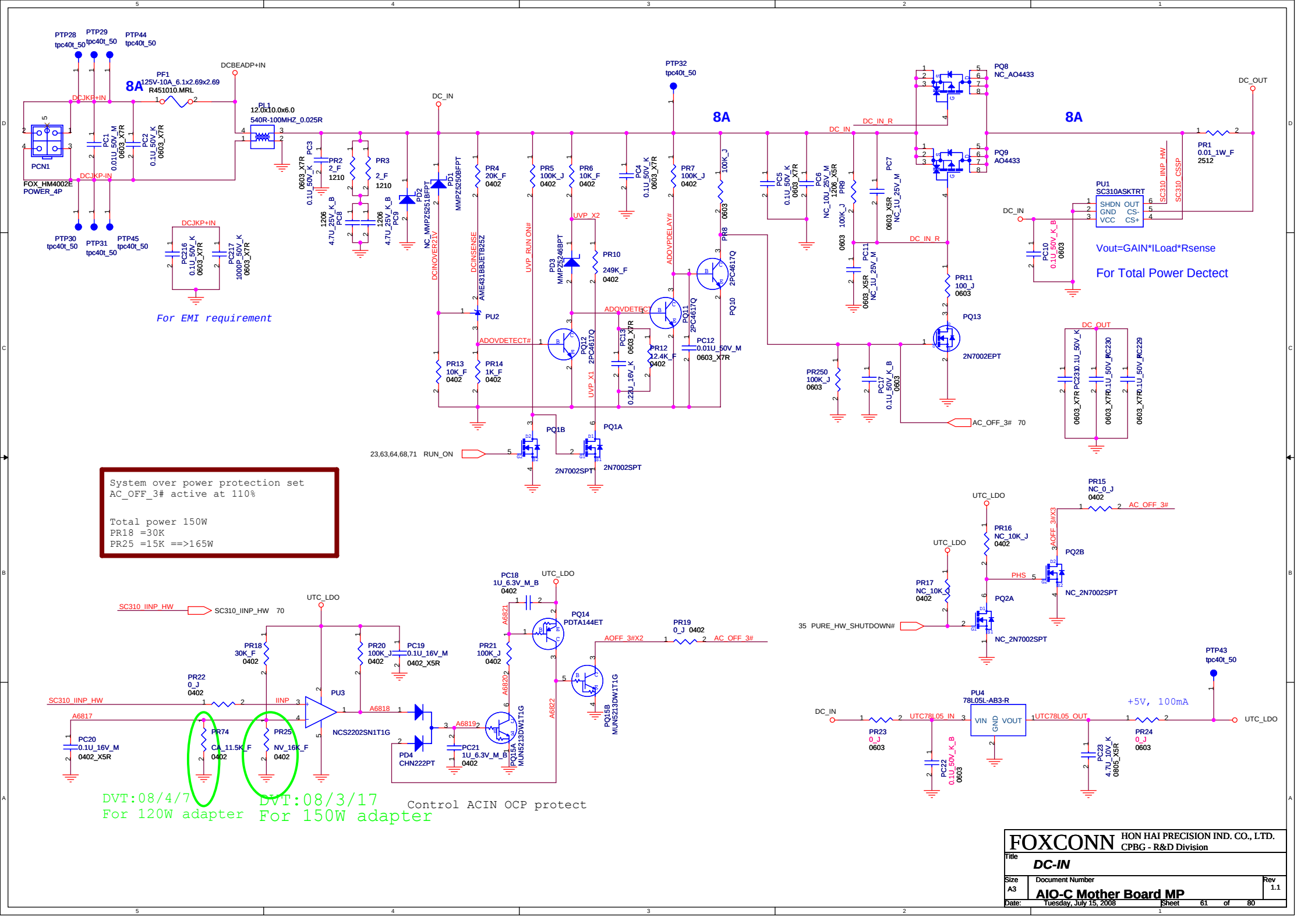


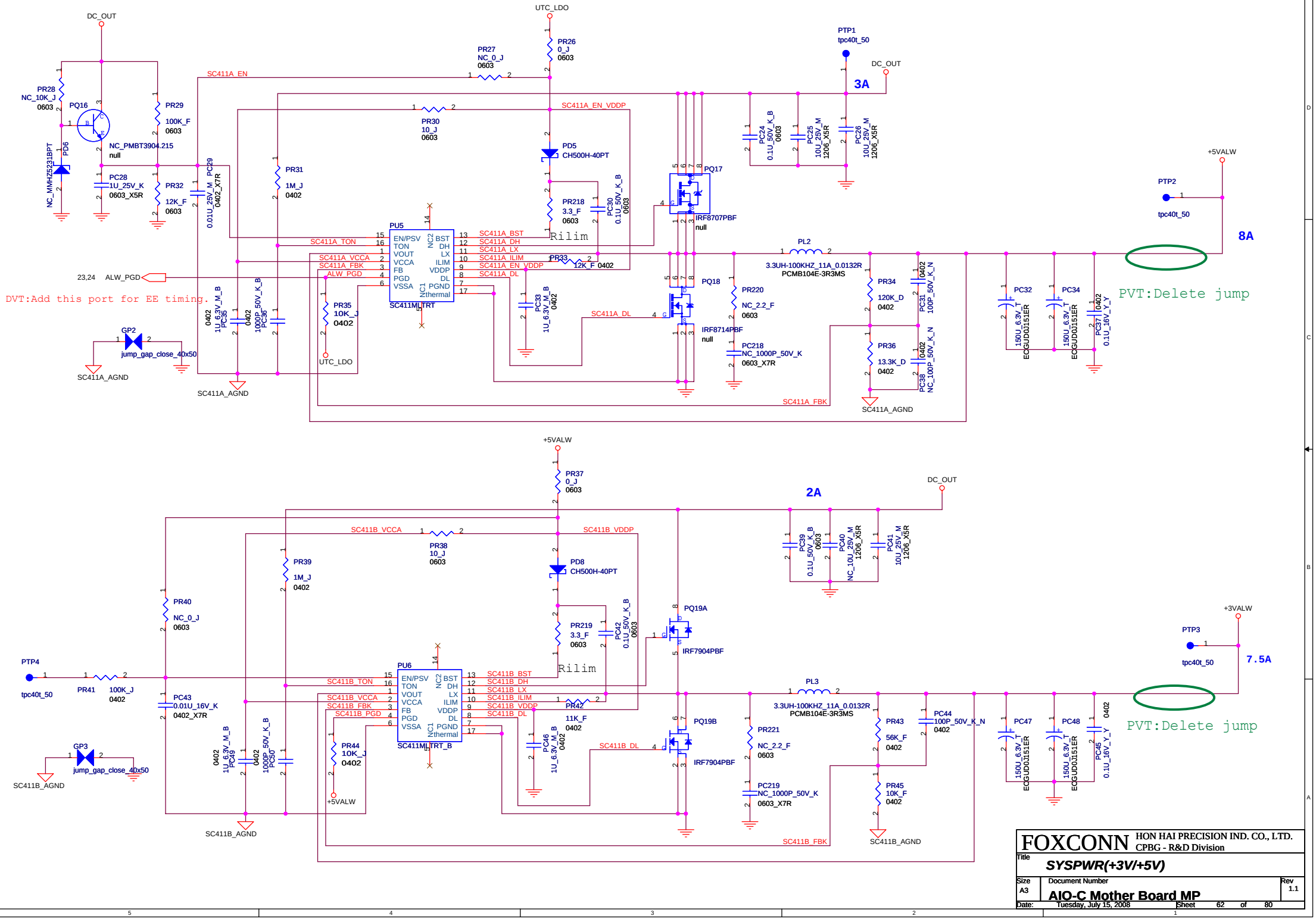
FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

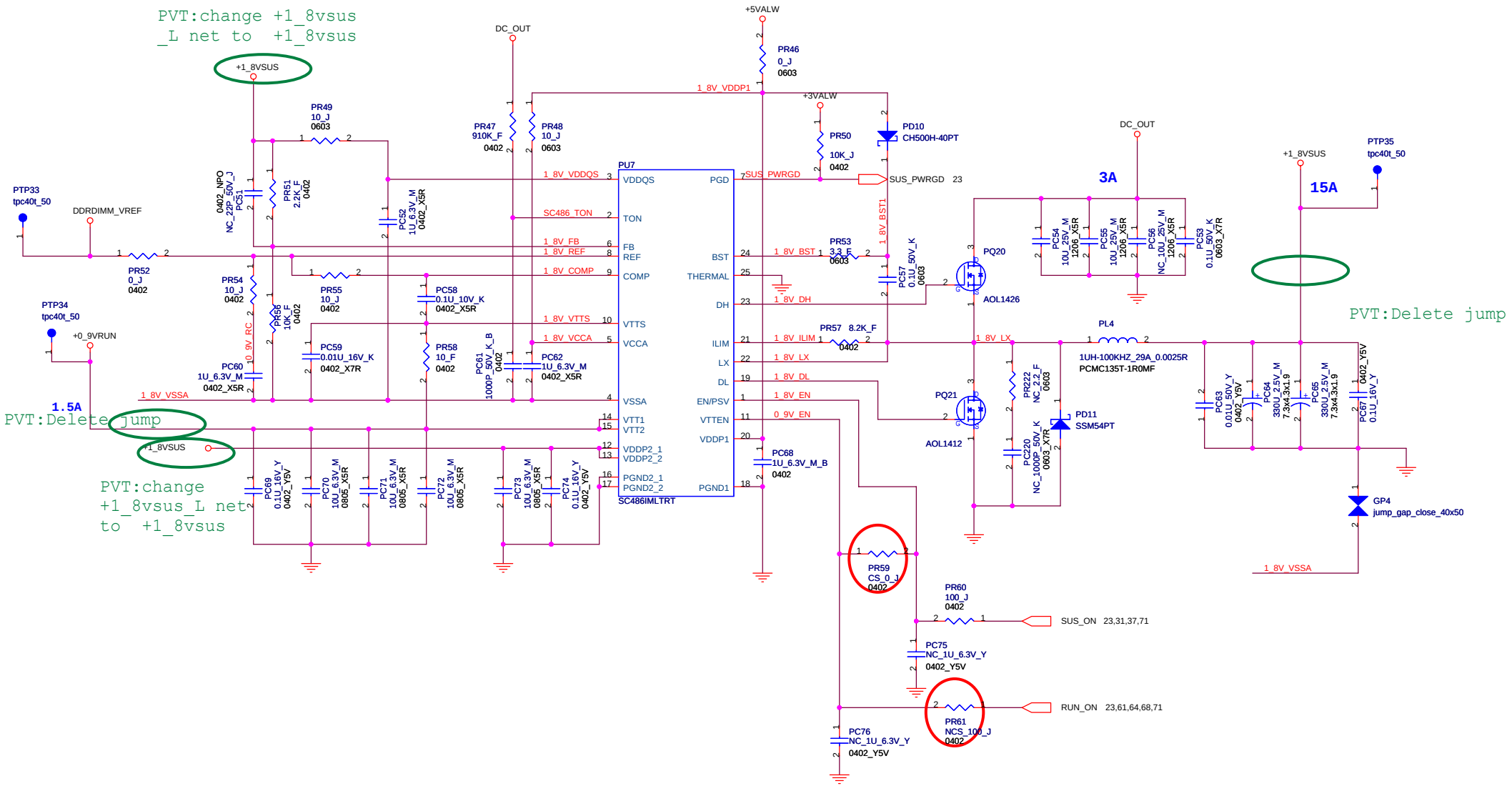
Title: POWER BLOCK DIAGRAM

Size: A3 | Document Number: AIO-C Mother Board MP | Rev: 1.1

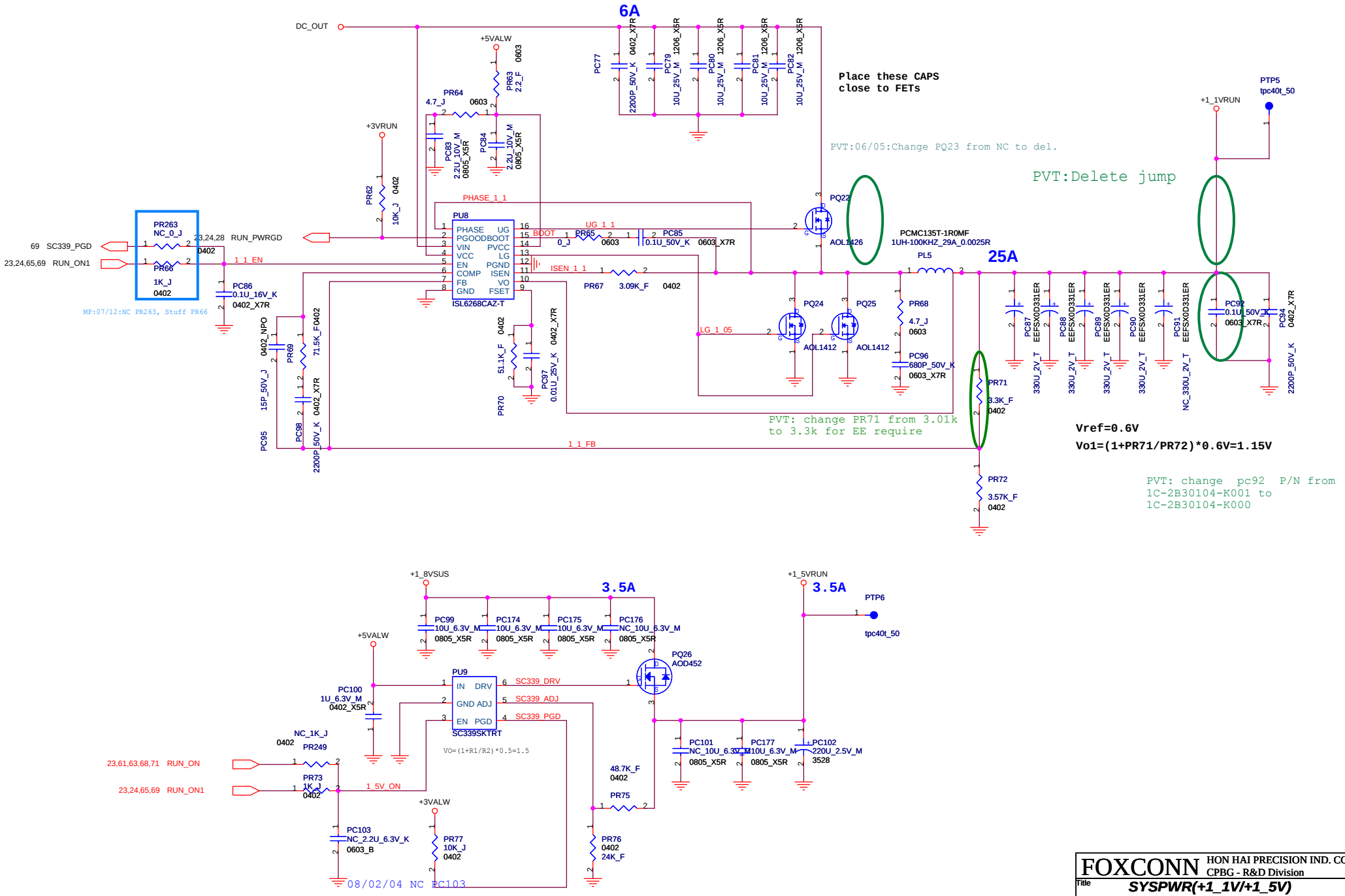
Date: Tuesday, July 15, 2008 | Sheet 60 of 80


PTP28 tpc40t_50
PTP29 tpc40t_50
PTP44 tpc40t_50
DCBEADP+IN
PF1
125V-10A_6.1x2.69x2.69
R451010.MRL
8A
DCJKP+IN
PC1 0.01U_50V_M 0603_X7R
PC2 0.1U_50V_K 0603_X7R
PCN1
FOX_HM4002E
POWER_4P
DCJKP-IN
PTP30 tpc40t_50
PTP31 tpc40t_50
PTP45 tpc40t_50
PC216 0.1U_50V_K 0603_X7R
PC217 1000P_50V_K 0603_X7R
For EMI requirement
PL1
12.0x10.0x6.0
540R-100MHZ_0.025R
DC_IN
PC3 0.1U_50V_K 0603_X7R
PR2 2_F 1210
PR3 2_F 1210
PC8 4.7U_25V_K_B 1206
PC9 4.7U_25V_K_B 1206
PD1 MMPZ5250BFPT
PD2 NC_MMPZ5251BFPT
DCINOVER21V
DCINSENSE
PU2 AME431BBJETB25Z
PR4 20K_F 0402
PR5 100K_J 0402
PR6 10K_F 0402
UVP_RUN_ON#
UVP_X2
PD3 MMPZ5246BPT
PR10 249K_F 0402
ADOVDETECT#
PR13 10K_F 0402
PR14 1K_F 0402
PQ12 2PC4617Q
UVP_X1
PC13 0.22U_16V_K 0603_X7R
PR12 12.4K_F 0402
PC12 0.01U_50V_M 0603_X7R
PQ11 2PC4617Q
PQ10 2PC4617Q
PQ1B
PQ1A
2N7002SPT
2N7002SPT
23,63,64,68,71 RUN_ON
PTP32 tpc40t_50
8A
PR7 100K_J 0402
100K_J 0603
PR8
ADOVPDELAY#
PC4 0.1U_50V_K 0603_X7R
PC5 0.1U_50V_K 0603_X7R
PC6 NC_10U_25V_M 1206_X5R
PR9 100K_J 0603
PC7 0603_X5R NC_1U_25V_M
PC11 0603_X5R NC_1U_25V_M
DC_IN_R
PR11 100_J 0603
PQ13
2N7002EPT
PR250 100K_J 0603
PC17 0.1U_50V_K_B 0603
AC_OFF_3# 70
PQ8 NC_AO4433
PQ9 AO4433
8A
DC_OUT
PR1 0.01_1W_F 2512
SC310_IINP_HW
SC310_CSSP
PU1 SC310ASKTRT
SHDN OUT
GND CS-
VCC CS+
DC_IN
PC10 0.1U_50V_K_B 0603
Vout=GAIN*ILoad*Rsense
For Total Power Dectect
DC_OUT
PC230 0.1U_50V_K 0603_X7R
PC231 0.1U_50V_K 0603_X7R
PC229 0.1U_50V_K 0603_X7R
System over power protection set
AC_OFF_3# active at 110%
Total power 150W
PR18 =30K
PR25 =15K ==>165W
SC310_IINP_HW
SC310_IINP_HW 70
UTC_LDO
PR18 30K_F 0402
PR20 100K_J 0402
PC19 0.1U_16V_M 0402_X5R
PR22 0_J 0402
PU3
NCS2202SN1T1G
IINP
A6817
A6818
A6819
PR74 CA_11.5K_F 0402
PR25 NV_16K_F 0402
PC20 0.1U_16V_M 0402_X5R
PD4 CHN222PT
PC21 1U_6.3V_M_B 0402
PQ15A MUN5213DW1T1G
PC18 1U_6.3V_M_B 0402
PQ14 PDTA144ET
PR21 100K_J 0402
A6821
A6822
A6820
PQ15B MUN5213DW1T1G
AOFF_3#X2
PR19 0_J 0402
AC_OFF_3#
DVT:08/4/7
For 120W adapter
DVT:08/3/17
For 150W adapter
Control ACIN OCP protect
PR15 NC_0_J 0402
AC_OFF_3#
PR16 NC_10K_J 0402
AOFF_3#X3
PQ2B
PHS
NC_2N7002SPT
PR17 NC_10K_J 0402
PQ2A
35 PURE_HW_SHUTDOWN#
NC_2N7002SPT
PTP43 tpc40t_50
PU4 78L05L-AB3-R
VIN GND VOUT
+5V, 100mA
DC_IN
UTC78L05_IN
UTC78L05_OUT
PR23 0_J 0603
PC22 0.1U_50V_K_B 0603
PC23 4.7U_10V_K 0805_X5R
PR24 0_J 0603
UTC_LDO
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
Title
DC-IN
Size A3
Document Number
AIO-C Mother Board MP
Rev 1.1
Date: Tuesday, July 15, 2008
Sheet 61 of 80

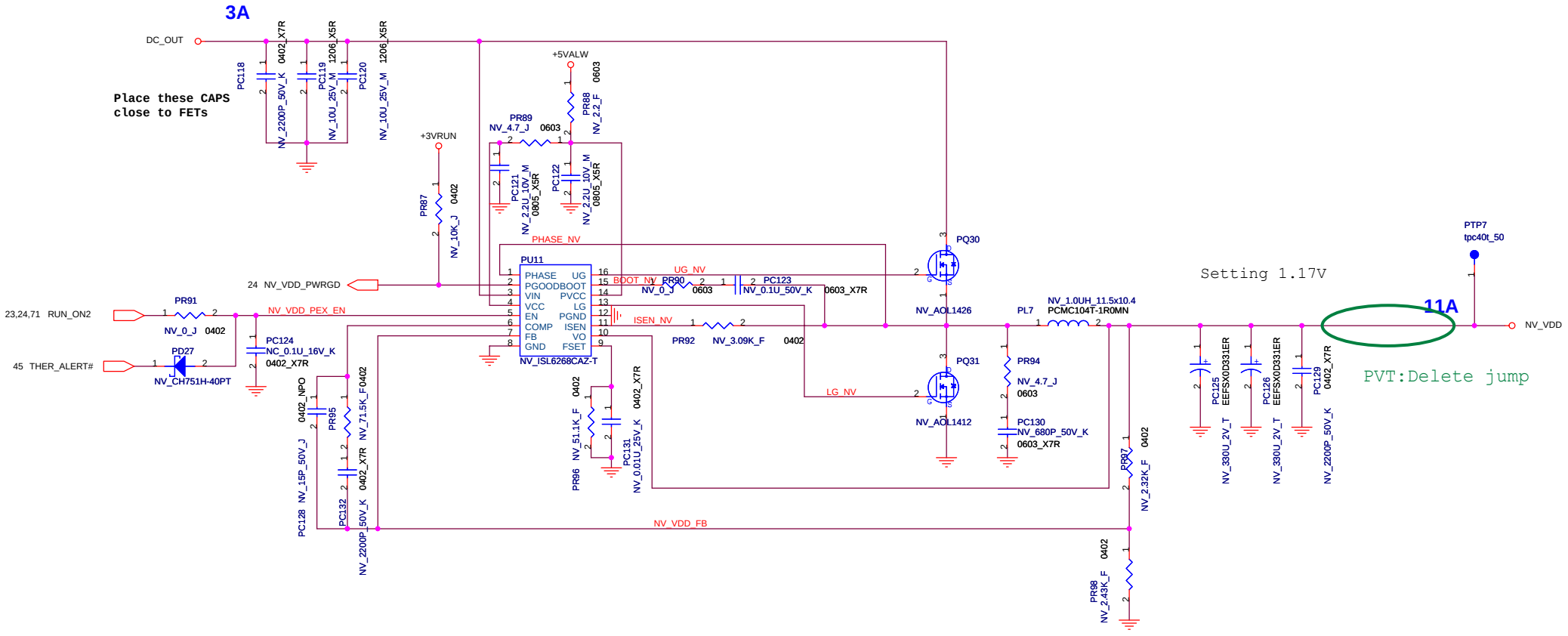

DC_OUT
UTC_LDO
PR27 NC_0_J 0603
PR26 0_J 0603
PTP1 tpc40t_50
3A
SC411A_EN
SC411A_EN_VDDP
PR28 NC_10K_J 0603
PQ16
NC_PMBT3904.215 null
PR29 100K_F 0603
PR30 10_J 0603
PD5 CH500H-40PT
PR31 1M_J 0402
PR32 12K_F 0603
PC28 1U_25V_K 0603_X5R
PC29 0.01U_25V_M 0402_X7R
PR218 3.3_F 0603
PC30 0.1U_50V_K_B 0603
PQ17
IRF8707PBF null
PC24 0.1U_50V_K_B 0603
PC25 10U_25V_M 1206_X5R
PC26 10U_25V_M 1206_X5R
+5VALW
PTP2 tpc40t_50
8A
PU5
EN/PSV TON VOUT VCCA FB PGD VSSA
BST DH LX ILIM VDDP DL PGND Thermal
SC411A_BST SC411A_DH SC411A_LX SC411A_ILIM SC411A_EN_VDDP SC411A_DL
SC411A_TON SC411A_VCCA SC411A_FBK ALW_PGD
SC411MLTRT
Rilim
PR33 12K_F 0402
PL2 3.3UH-100KHZ_11A_0.0132R PCMB104E-3R3MS
23,24 ALW_PGD
DVT:Add this port for EE timing.
PR35 10K_J 0402
PC33 1U_6.3V_M_B 0402
PC35 1U_6.3V_M_B 0402
PC36 1000P_50V_K_B 0402
PQ18
IRF8714PBF null
PR220 NC_2.2_F 0603
PC218 NC_1000P_50V_K 0603_X7R
PR34 120K_D 0402
PR36 13.3K_D 0402
PC31 100P_50V_K_N 0402
PC38 NC_100P_50V_K_N 0402
PC32 150U_6.3V_T ECGUD0J151ER
PC34 150U_6.3V_T ECGUD0J151ER
PC37 0.1U_16V_Y 0402
PVT:Delete jump
GP2 jump_gap_close_40x50
SC411A_AGND
UTC_LDO
SC411A_FBK
+5VALW
PR37 0_J 0603
2A
DC_OUT
SC411B_VCCA SC411B_VDDP
PR38 10_J 0603
PD8 CH500H-40PT
PC39 0.1U_50V_K_B 0603
PC40 NC_10U_25V_M 1206_X5R
PC41 10U_25V_M 1206_X5R
PR39 1M_J 0402
PR40 NC_0_J 0603
PR219 3.3_F 0603
PC42 0.1U_50V_K_B 0603
PQ19A
IRF7904PBF
+3VALW
PTP3 tpc40t_50
7.5A
PTP4 tpc40t_50
PR41 100K_J 0402
PU6
EN/PSV TON VOUT VCCA FB PGD VSSA
BST DH LX ILIM VDDP DL PGND Thermal
SC411B_BST SC411B_DH SC411B_LX SC411B_ILIM SC411B_VDDP SC411B_DL
SC411B_TON SC411B_VCCA SC411B_FBK SC411B_PGD
SC411MLTRT_B
Rilim
PR42 11K_F 0402
PL3 3.3UH-100KHZ_11A_0.0132R PCMB104E-3R3MS
PC43 0.01U_16V_K 0402_X7R
PC44 100P_50V_K_N 0402
PC45 0.1U_16V_Y 0402
PC46 1U_6.3V_M_B 0402
PC47 150U_6.3V_T ECGUD0J151ER
PC48 150U_6.3V_T ECGUD0J151ER
PC49 1U_6.3V_M_B 0402
PC50 1000P_50V_K_B 0402
PQ19B
IRF7904PBF
PR43 56K_F 0402
PR44 10K_J 0402
PR45 10K_F 0402
PR221 NC_2.2_F 0603
PC219 NC_1000P_50V_K 0603_X7R
PVT:Delete jump
GP3 jump_gap_close_40x50
SC411B_AGND
SC411B_FBK
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
Title
SYSPWR(+3V/+5V)
Size A3
Document Number
AIO-C Mother Board MP
Rev 1.1
Date: Tuesday, July 15, 2008
Sheet 62 of 80



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	DDR2PWR(+1_8V/+0_9V)	
Size A3	Document Number AIO-C Mother Board MP	Rev 1.1
Date: Tuesday, July 15, 2008	Sheet 63 of 80	

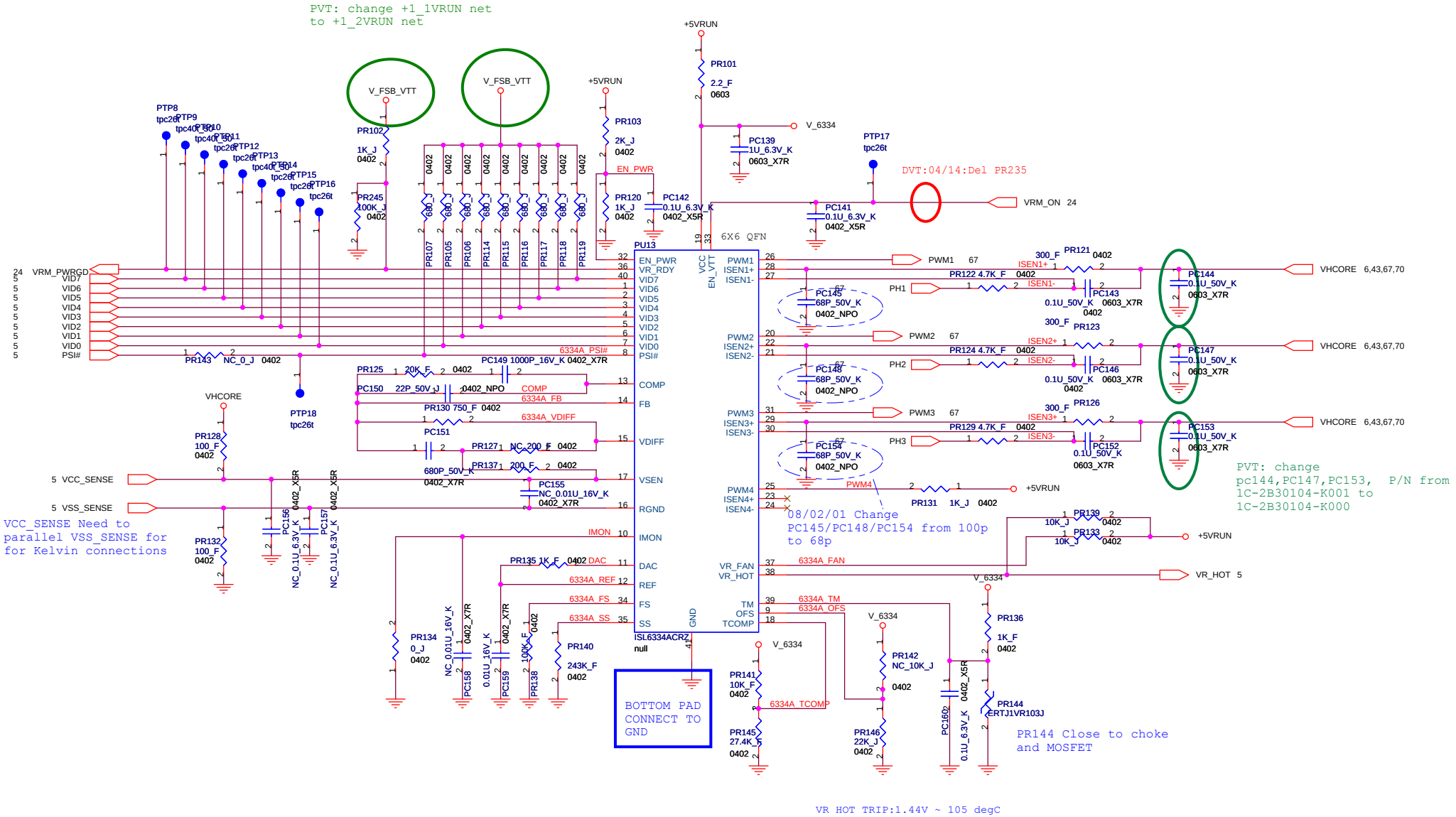


FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	SYSPWR(+1_1V/+1_5V)	
Size A3	Document Number AIO-C Mother Board MP	Rev 1.1
Date: Tuesday, July 15, 2008	Sheet 64 of 80	

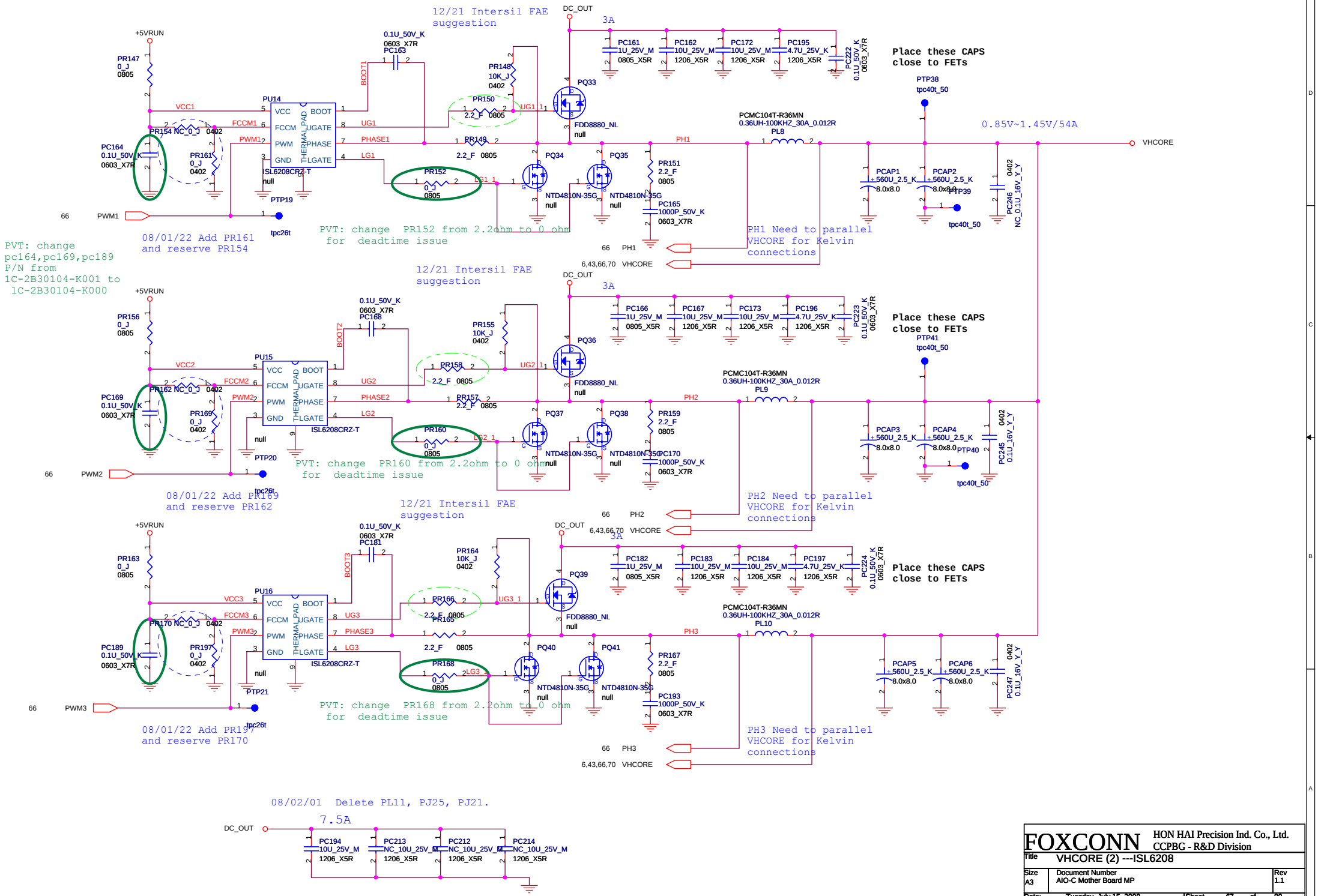


FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	VGAPWR(GMCH)	
Size A3	Document Number AIO-C Mother Board MP	Rev 1.1
Date: Tuesday, July 15, 2008	Sheet 65 of 80	

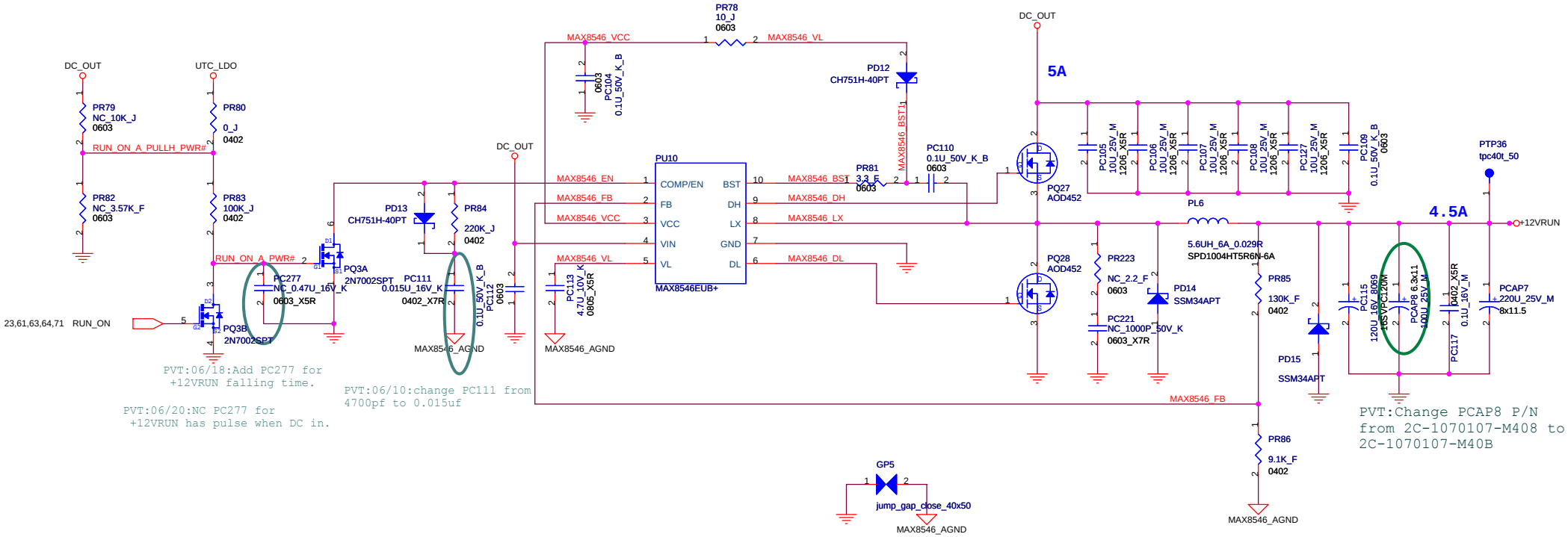
ISL6334ACRZ FOR VRD11.1 POWER CKT for 19V Vin



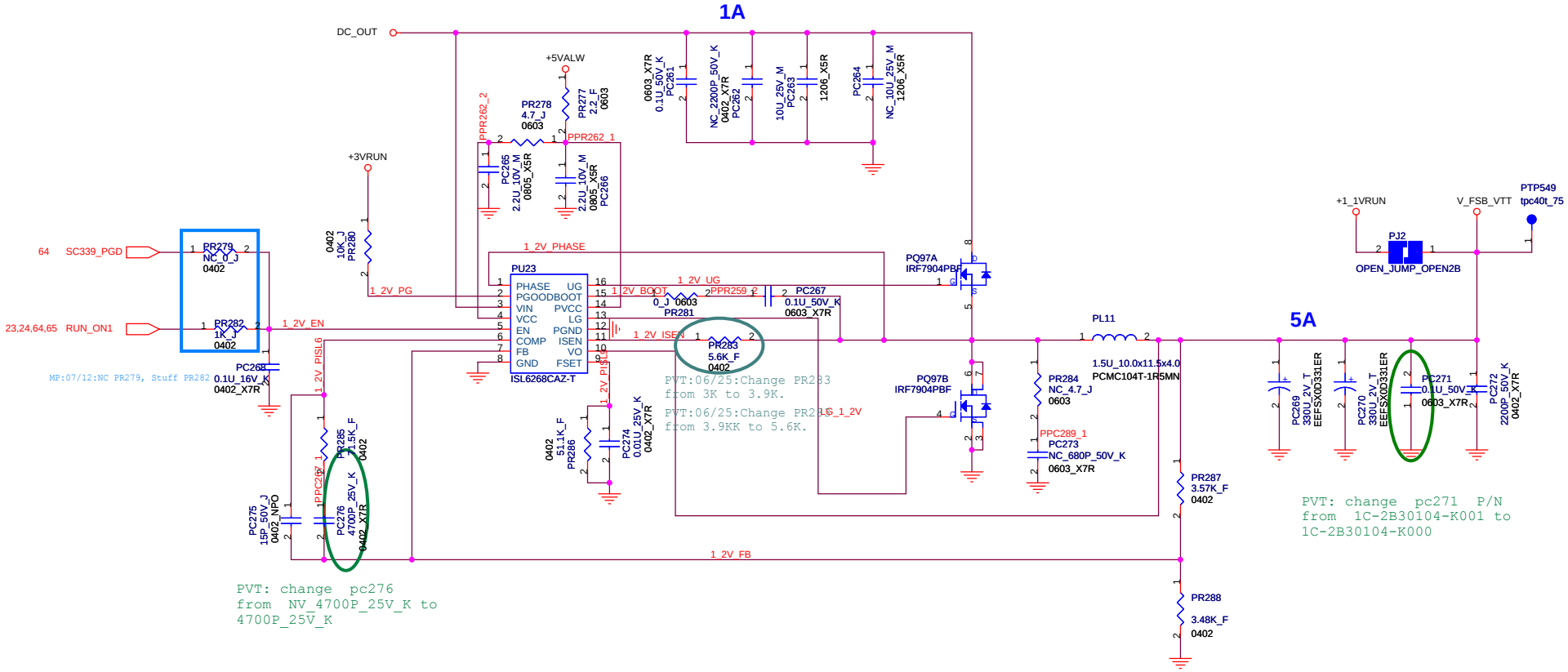
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	VHCORE (1)---ISL6334A	
Size A3	Document Number AIO-C Mother Board MP	Rev 1.1
Date: Tuesday, July 15, 2008	Sheet 66 of 80	



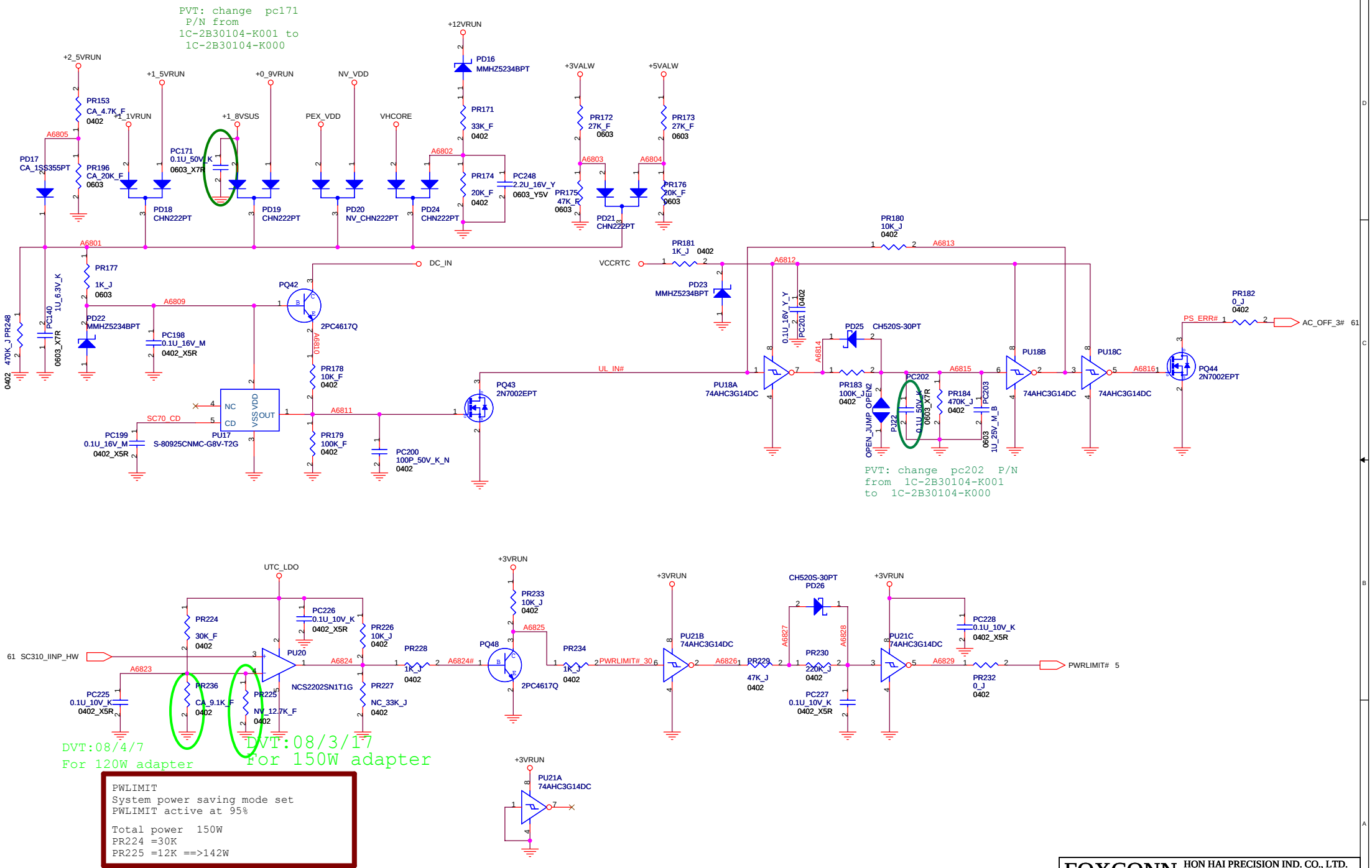
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
Title	VHCORE (2) ---ISL6208
Size A3	Document Number AIO-C Mother Board MP
Rev	1.1
Date:	Tuesday, July 15, 2008
Sheet	67 of 80



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	HDD PWR(+12V)	
Size A3	Document Number AIO-C Mother Board MP	Rev 1.1
Date: Tuesday, July 15, 2008	Sheet 68 of 80	



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	SYSPWR(+1_2V)	
Size A3	Document Number AIO-C Mother Board MP	Rev 1.1
Date: Tuesday, July 15, 2008	Sheet 69 of 80	

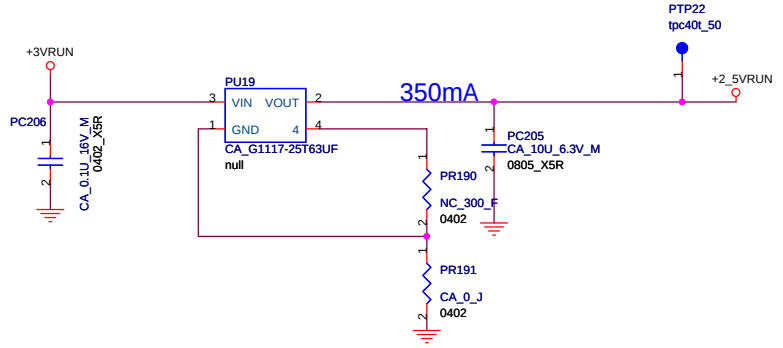


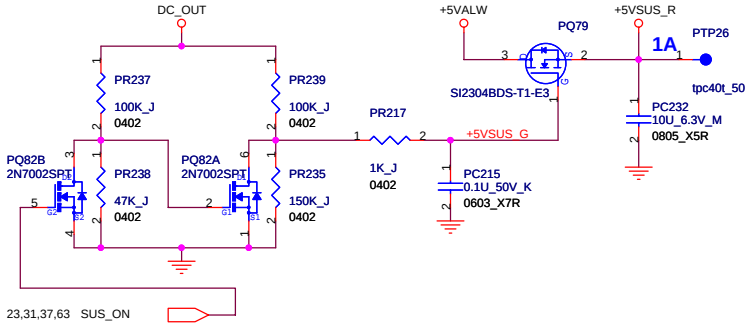
FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

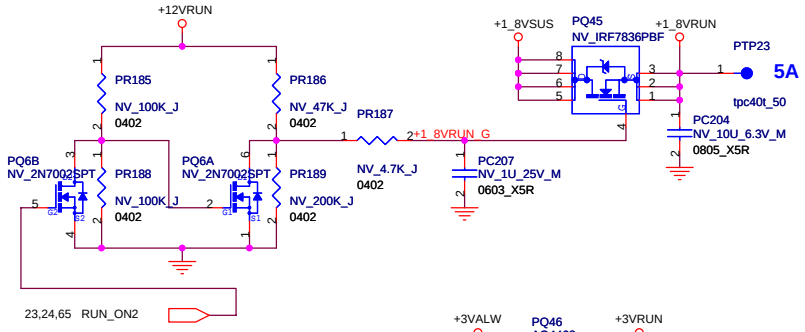
Title: **OVP Protect**

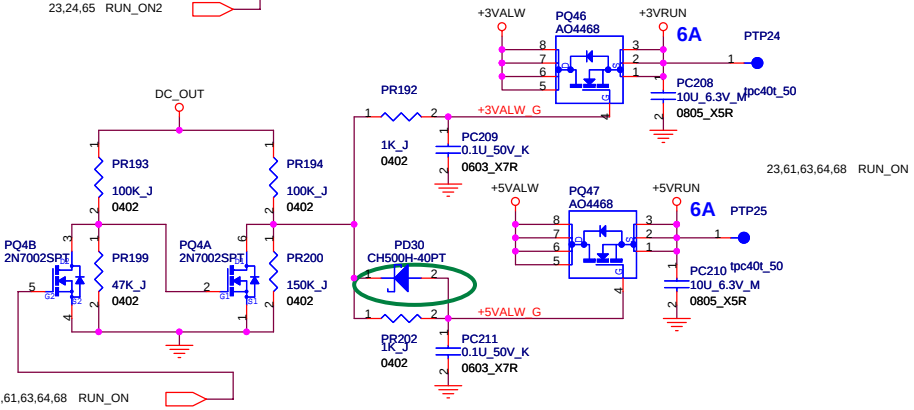
Size: A3 | Document Number: **AIO-C Mother Board MP** | Rev: 1.1

Date: Tuesday, July 15, 2008 | Sheet 70 of 80

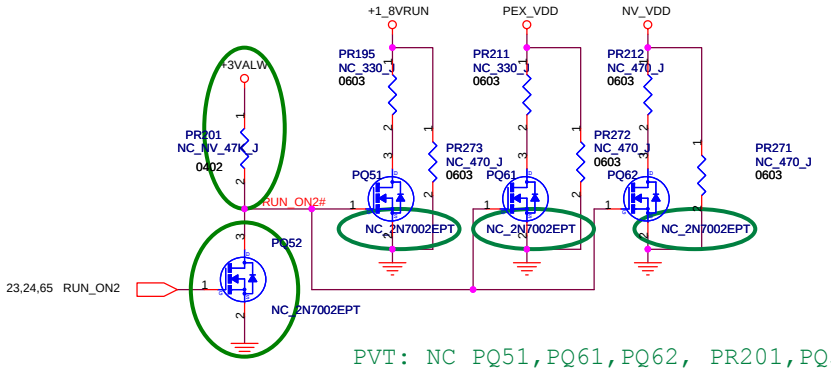




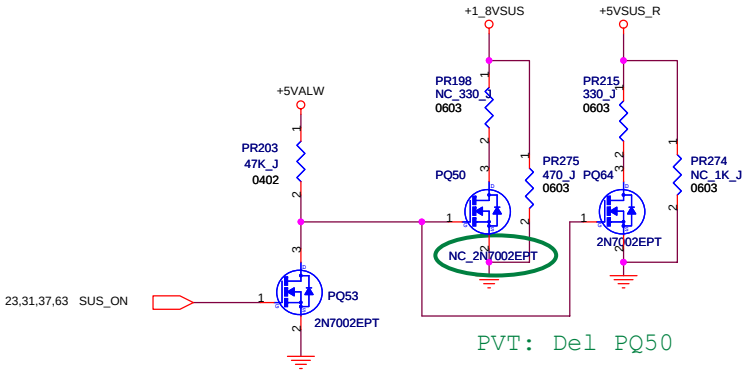




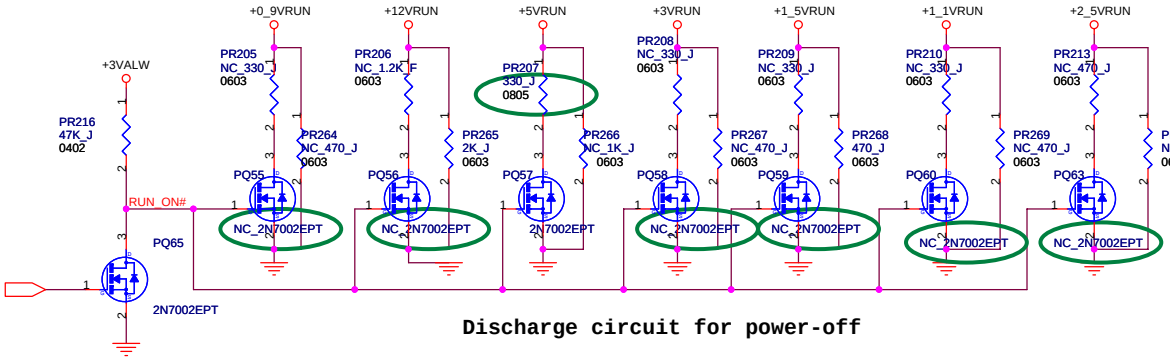
PVT: add PD30 for +5VRUN discharge timing



PVT: NC PQ51,PQ61,PQ62, PR201,PQ52



PVT: Del PQ50



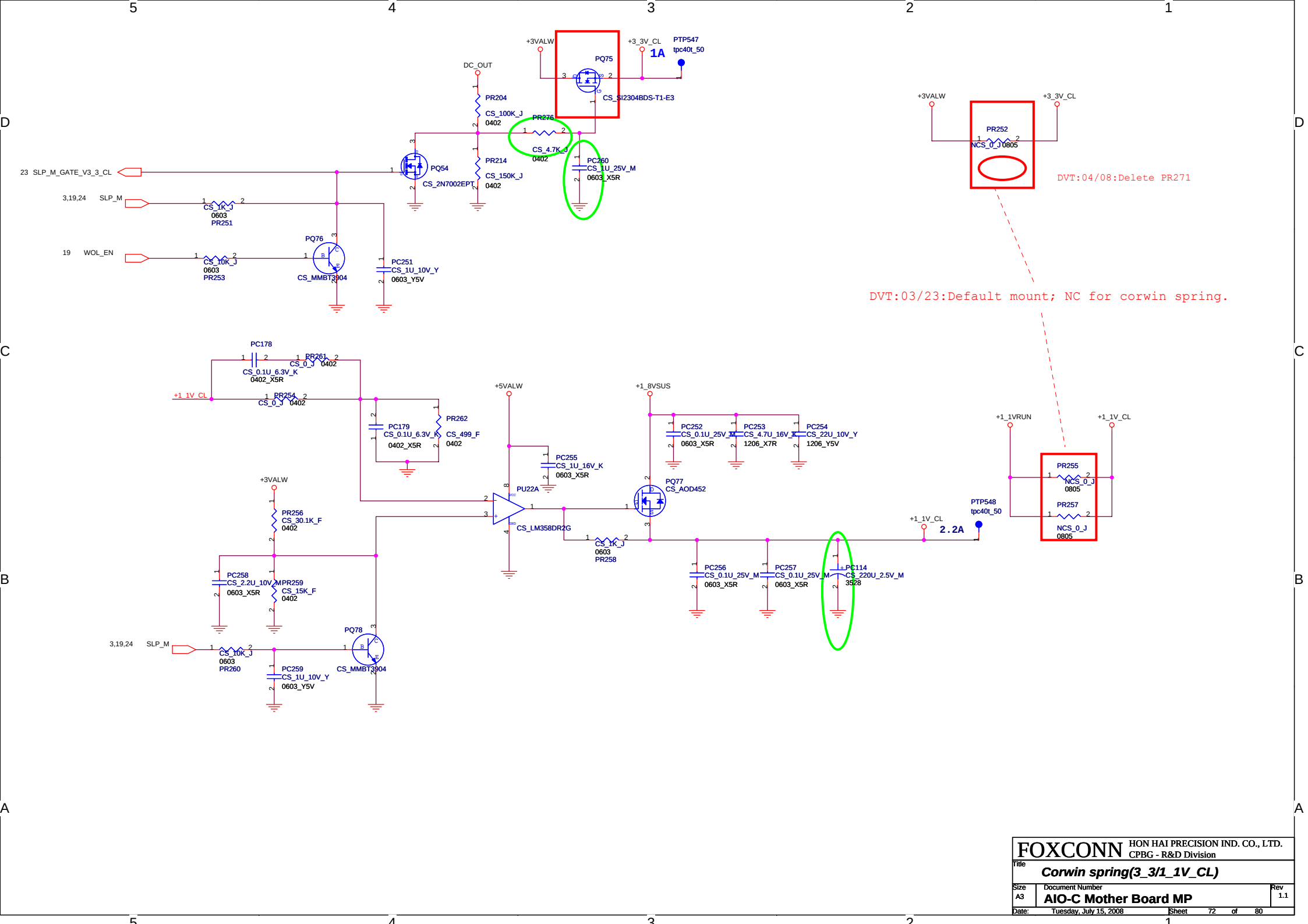
Discharge circuit for power-off

PVT: Change PR207 from 1R-0000471-J300 to 1R-0000331-J500

RUN_ON# RUN_ON# 37

PVT: NC PQ55,PQ56,PQ58,PQ59

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: *Others PWR Plane*		
Size: A3	Document Number: AIO-C Mother Board MP	Rev: 1.1
Date: Tuesday, July 15, 2008	Sheet 71 of 80	



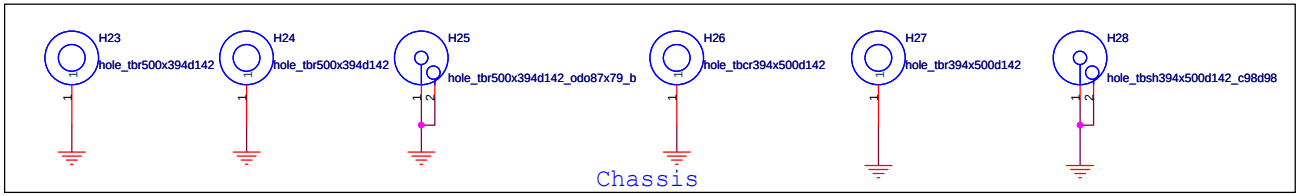
FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

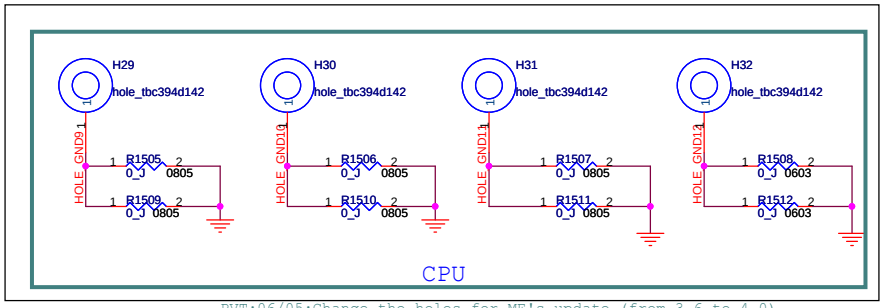
Title: *Corwin spring(3_3/1_1V_CL)*

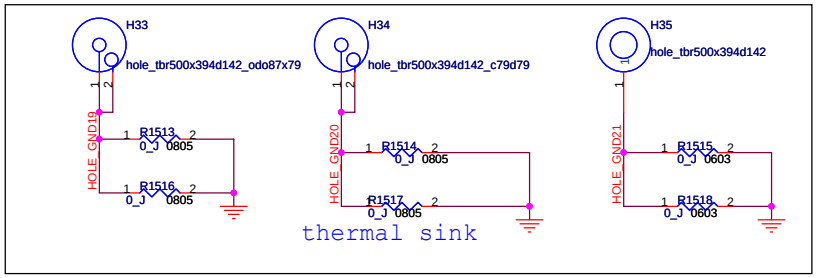
Size: A3 | Document Number: AIO-C Mother Board MP | Rev: 1.1

Date: Tuesday, July 15, 2008 | Sheet 72 of 80

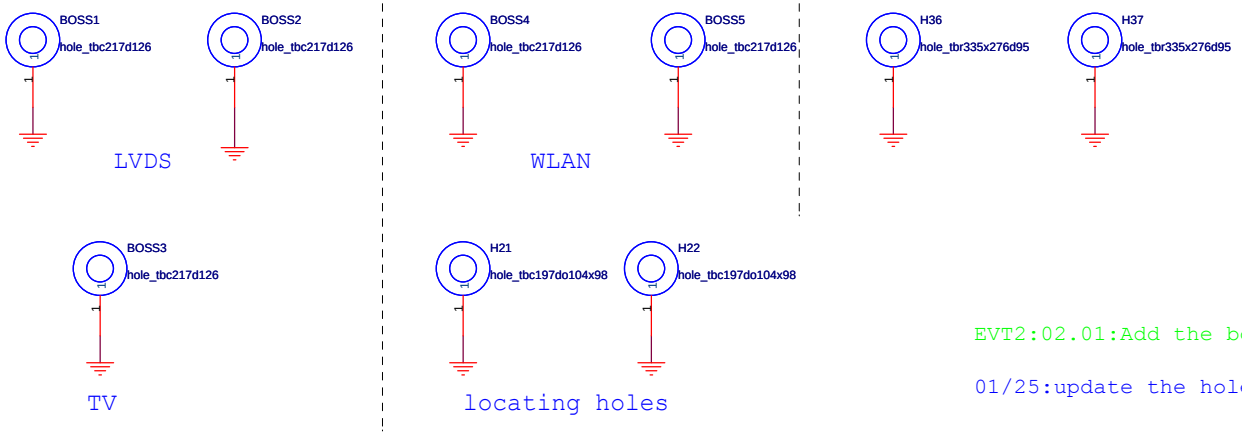
DVT:03/22:change the holes which except H21&H22







PVT:06/05:Change the holes for ME's update.(from 3.6 to 4.0).
PVT:06/06:Change the holes back to DVT for ME's update.



EVT2:02.01:Add the boss location

01/25:update the holes.

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Hole & BOSS	
Size A3	Document Number AIO-C Mother Board MP	Rev 1.1
Date: Tuesday, July 15, 2008	Sheet 73 of 80	

History (EVT2)

2008/12/09

P20: add a NC 10k resistor pull up to 5VRUN for FAN1_PWM , FAN2_PWM ,FAN3_PWM,as whether there is a internal pull up in FAN is not known.

P20: change net name from FAN_PWM1,FAN_PWM2,FAN_PWM3 to FAN1_PWM ,FAN2_PWM,FAN3_PWM,as to consistent

P16: Connect GPIO9 from BIOS_RST# to WOL_EN

P29: Change USB6N USB6P to USB8N USB8P Change USB8N USB8P to USB6N USB6P

2008/12/11

P16: Add R1279 R1280 to pull up SMB_THRM_CLK,SMB_THRM_DATA; Stuff R246,Cancel R876;Change C949 to R1278;Not connect GPIO9 to WOL_EN;Change SB_SYS_RESET# pulled up voltage to +3VALW

P04: Add C1139,change R2 size from 0402 to 0603;Cancel C11 C12

P05: Change R78 R1049 size from 0805 to 0402,connect H_CPUPWRGD from VTT_OUT_RIGHT to VTT_OUT_LEFT,connect H_CPU_RESET# from VTT_OUT_LEFT to VTT_OUT_RIGHT;Add H_STPCLK# test point TP396

P06: Cancel VRM_PWRGD level shiftterr

P08: Change R126 R131 R134 from 49.9kOhm to 49.9Ohm

P13: Change C94 from 1uF to 2.2uF,cancel C95

P15: Place BIOS_RST# at the SB side;Add PANEL_ID2,PANEL_ID3, PANEL_ID4,PANEL_ID5 to GPIO21,GPIO19,GPIO36,GPIO37;Cancel R210,R211,R212,R213;Add R1271

P17: Change VCCLAN3_3 from +3VRUN to +3VALW;Connect VCCLAN1_1 to +1_1VRUN

P25: Cancel WOL-EN circuit

P41: NC R708 R709 C600 FOR FB_VREF.
CHANGE R713 FROM 60.4 TO 40.2 CHANGE R715 FROM 40.2 TO 60.4 REF PRD.
DELETE DACB PORTION, ADD TEST PAD TO DACB SIGNAL.
STUFF R716 R717, CRT DEBUG CARD NO PULL-HIGH RESISTOR.
DELETE IFPE AND IFPC PORTION, ADD TEST PAD TO IFPE POWER AND IFPE_RSET, NC OUTPUT SIGNAL.
DELETE HDMI ROM(BEFORE NC), DELETE HDA* SIGNAL, DELETE I2CH_SCL AND I2CH_SDA(ADD TEST PAD), DELETE I2CB,I2CD, I2CE.
DELETE R770, ADD TEST PAD TO XTALSSIN AND NV_XTALIN SIGNAL.
SWAP FBAD* SIGNAL FOR LAYOUT REQUEST,ADD FBA_A[2..5] (OFF PAGE) TO CONNECT WITH GPU.
DELETE SDVO_CTRL* LEVEL SHIFTER, CONNECT THESE SIGNAL TO NB SDVO_CTRL SIGNAL.

P20: HW THERMAL PROTECT circuit recover

P20: add 0.047u cap for each FAN_TACH signal for filter, deletethe pull high 5VRUN and the diode for each FAN_TACH signal.

P21: delete the EMC2106 HW monitor circuit

P21: add CN40 for ODD transister,add Address select circuit for ADT7484/7486

P19: add level shift circuit for signal SB_VRMPWRGD and CL_PWRGD

P56: Delete PJ9&PJ10&PJ11 and net "+VGFX_CORE"

P25: Change net "VRM_PWRGD" pull high from +3VRUN to +1.1VRUN

P30: Delete PR236&PR237

P20: Change package from DPAK to IPAK for PQ34&PQ35&PQ37&PQ38&PQ40PQ41

P20: Change PR136 from 2K to 981 ohm

2008/12/13

P15: Change REQ1# REQ2# REQ3# TO GPIO 50 GPIO52 GPIO54;Connect RP18 Pin3 to USB _OC#6;PANEL_ID2~5 by pulled high to +3VRUN; Connece GPIO49 TO I2C_DAT

P15: GPIO19 GPIO33 GPIO18 GPIO56 add test piont;Del R221 R209; Connect MINI_RXN3 MINI_RXP3 MINI_TXN3 MINI_TXP3 to U4 PERN2 PERP2 PETN2 PETP2;Connect TV_RXN2 TV_RXP3 TV_TXN3 TV_TXP3 to U4 PERN5 PERP5 PETN5 PETP5

P15: SB PME# PIN connect to page30 U21 PME#

P16: Connect R248 to +3VALW;DEL R1048 R229 R237 R242 R1047; Connect R234 PIN1 TO R236 PIN1;DEL SB_RST# net and add test piont;Connect SB_SYS_RESET# TO CN27 PIN27 and add 0OHM resistor;GPIO26 add test piont;Connecet GPIO23 to I2C_CLK

P04: Change C3 C14 size from 1206 to 0603,change C7 from 0.1u to 4.7u,change C9 C10 size from 0805 to 0603

P44: delete c678 c680 c679 c677 c681.
add 2 test points for GPIO5 GPIO6.
add 5 pcs CAP.for FB_VDDQ.
add 2 0ohm for SDVO_CTRL bus.
add 1 test point for FBA_DEBUG.
add 1 Cap here, place close to L51.
delete L52.
delete c538 c540 c542 c543 c544 c545.
add 1 Cap here, place close to L50.
delete L49.

P39: CAP39 Change to 1C-33U0226-M200 for meetting MOR's requirement

P35: Delete R1310 , Add a NC_R?--0_J.
Add NC_SN74AHCT1G125DCKR,NC_SN74AHC1G04DCKNC_2N7002SPT, NC_SN74LVC1G08DCK.
Add R? R? --0_J R?--NC_10K.
U81 change to 14-SN74LVC-1G06.

P05: Add 0Ohm resistor on the SB_SYS_RESET# and NC it;NC R1058 R857 R86

P07: Add C1167~C1171

P27: change +3V_EMINI_AUX to +3V_EMINI_AUX_1

P29: Add +5VSUS and 0_J resistance.
change +5V_CAM_FELI to +5VSUS_R.

P21: change c1052 &cn40from NC,and linck to U71.
NC C1053,and linck to U70,delete R1181.R1183.R1180.R1186;
Connect U71 pin6 to NV_THERMDN,connect U71 pin6 to Connect U71 pin5 to NV_THERMDP.

P22: Add R1355 R1357

P32: change +3VALW to +5VALW and change 10K to 150ohm

P10: Add test piont for NC pin;change MCH_DDC_CLK&DAT with each other.
Delete R153 R154.

P11: Change C64 C82 C83 C84 C47 C86 C88

P13: Delete R192 R191 C93 and add test piont,change C92

P14: Add C1174~C1180

P04: Change RP42 RP43 RP44 RP49 pin1 witn pin2.
Delete R877 R878 Q67.

P22: add one 0_J resistor.
add one 10k resistor and connect to gnd.

2008/12/14

P23: Change a new conn

P24: change the 2.0A fuse to 2.6A.

add 6 resistors for I2C bus pull up, no stuff I2CB I2CC I2CD I2CE2.
change the resistor value follow PUN.
add level shifter for ENAVDD shift to 5V.

P19: Change c196 from 1u_10v_0603 to 1u_16v_0402_y5v,C197 from 10v_0603_y5v to 16v_ 0603_x5R,R268 from 180k_F to 180_J.
Change c199&C202 from 16v_Y5Vto 10v_X5R1,R270 from 10k to 100k.
add level shift ,delete R278&R279.

P20: delete 0.047u cap for each fan_tach signal,add R308

P29: Add +5VSUS and 0_J resistance

P27: add NC_22U_10V_Y resistance.
Cut off P-MOS and N-MOS and two resistance.

P30: change Remove R417 and cancel R420 NC.

P31: cancel C337 NC. Shield GND for CLK to reduce external noise for CLK.
cancel NC with R437,438,439 cancel NC with C332,333,334

P04: Add RP51

P15: Add net LAN_RXN4 LAN_RXP4 LAN_TXN4 LAN_TXP4;add C1212 C1213.

P16: Add TP466~TP474.

P25&26: Change LAN chipset from intel to MARVELL.

P17: Add CAP43 CAP44 R1358 R1359 C1198 C1199 C1200 C1201 C1214 C1215.

2008/12/15

P32: Add H3~H25

P04: Change CK_PE_SRC11_R_DP and CK_PE_SRC11_R_DN with each other

P13: Change C110~C117

P14: Change C118~C144 C1174~C1180

P17: Add CAP45

2008/12/16

P11: Change R174 from 1ohm to 0ohm NC R175 C58 C49;Change R177 from 1ohm to 0ohm NC R176 C63 C64;Add R1388 R1389 R1390

P32: Connect H9 H10 H11 H12 to GND

P13: change 5 pin conn.,bypass ME request

P27: Add 10K 0402 resistor,Cut off 0_J 0402 resistor,Change 0402 to 0603.
Change DC_OUT to +12VRUN.
Change 17-S12316D-ST00 to 17-2N7002E-PT00.
Cut off 17-2N7002S-PT00 N-mos add 17-MMBT390-4001 NPN BJT and 17-PDTA144-ET00 PNP BJT.
Delete TB48,Delete two 1C-2B20104-M000 capaticor.

P13: Change 1N-1052001-0000 to 1N-1052003-0000 conn.

2008/12/17

P04: Add R1410 SRC8 OUTPUT TUNER_ CLK ,control by CR_F# deleye the TP,and BIOS diaable TUNERCLK_REQ# PCI1 output PCLK_JIG

P16: Add U87 C1217;Add test piont for ICH10 pin M2.
Add R1411.

P20: Add D32 D33 D34 and NC D34

P27: change 17-DTC144E-UA00 to 17-MMBT390-4001.
Change 17-2N7002E-PT00 to 17-S12316D-ST00.

P28: NC_CN39,delete two hole.

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Title: Revision History(1)

Size: A3 | Document Number: AIO-C Mother Board MP | Rev: 1.1

Date: Tuesday, July 15, 2008 | Sheet 74 of 80

P29: delete R1299.
change 1C-2Y20104-Y000 to 1C-2B20104-K301.
change 1C-XX60333-J300 to 1C-2Y20223-Y000 .
change BT_3V_R to BT_3V.
change USB_PN7_L to USBP9N and change USB_PP7_L to USBP9P.

P29: change Oide Power to FELICA_PWR.
Add a 22u capacitor.
delete TP213.
delete +5VSUS and 0_J resistance.
change 1M-F6V00A5-F000 to 1M-F006A35-F000.
change CAM_5V to +5VSUS_R.

P56: Change +5VSUS to +5VALW.
Reserve PC93,PC127 for NB design guide requirement.

P62: Delete +3VSUS reserve circuit.

P32: Change the Hole size bypass ME request.

P22: change the +3VALW to +3VRUN.

P23: Change two new parts.
re-define the pin.

P40: delete r674. add 100uF CAP to NV_VDD, add PJ for 3,3VRUN to VDD33.

P41: add 1pcs for Strap.

P42: add 3pcs 10uF CAP for FBVDD/Q,add PJ for FBVDD/Q.

P44: delete C1197,C1196, C629.

P45: add 10K pull high for I2CH_SDA, pull high 10K for ROM_CS_N, 10K pull down for I2CH_SCL. delete R1408 R1409.

2008/12/18

P21: change CN 40 to HS8102E.
Add TV_TUNER clk from NC,put down PCIF5.

P27: PAGE27 add a portion circuit.

2008/12/19

P21: change CN 40 to HS8102E,change U71 to EMC1103.

P05: NC R14022007/12/19:reserve for clock SI measure (refer to M630/M640 rise/fall slew fail issue).
Change +12VRUN to DC_OUT Add 100K resistor
reserve +3VRUN.
change 17-MMBT390-4001 to17-DTC144E-UA00.
Vil = 0.0v [+/-0.3]) @intel wlanmodule spec change 17-DTC144E-UA00 to 17-2N70020-0000.
NC R1452 for intel modul spec:internal pull up.
delete reserved component for CN16 pin3.
change +5VRUN to+5VSUS_R.

P30: change +3VRUN to +3VRUN_PCI for VCC_RIN.
Add c302 0.01 uF cap.
NC C307 10 uF cap.

P31: NC this two cap.(4.7 uF) C1221 and C1222.

P24: change the usb conn for the MERD's requesst.

2008/12/20

P39: change Line in / headphone /mic connector.
mount F8 (3.5A fuse).

P25: Delete Q102 Q103 R899 R909 R907 R908 R1381 R1382 C1211;
Add R1257 R1258.

P26: Delete R1384 R1385 R1386 R1387 C941 C942.

P16: Add R1462 pull up SPI_CS1#,and NC it.

P15: Add R1461 pull low PCI_GNT#0;Connect ODD to Port1;
Connect Wirelan to Port1 TVtuner to Port2.

P29: Change CN16.

P06: Change R856 from 0Ohm to 1KOhm.

P05: Add test piont for H_GTLREF2 and H_GTLREF3;Delete H_GTLREF2 and H_GTLREF3 circuit;NC R1398 ADD R1477.

P08: NC R128.

P11: Add CAP47 CAP48.

P23: Change c226 c227 cap5.

P28: change SB_WAKE# to SB_WAKE#_R.

P29: change USBP9N to USBP9N_Rand change USBP9P USBP9P_R.

P29: Chang 1N-0010001-MWGO to 1N-0010000-M1G0.

P19: delete R1272,R1273.

P40: add 22uF cap for NVVDD.

P49: add level shifter Q for 2.5V to 3.3V, change Y7 to a small size.

P50: add 0_J for LCD 5V power, add 0_J for DC_OUT, NC U53 and R830 , stuff R836.

2008/12/21

P59: Change PR130 connected way.

P60: Change PR149,PR148,PR155,PR158,PR164,PR166 connected way.
Add PC172,PC173,PC174(10_25V) capacitor, And delete PCAP8.

P19: change c196 from 0.1u to 1u.
Connect R1458 to GND and NC it.

P05: Delete GTLREF voltage control cirfuit.
Change R70;Add R1480.

P10: Add R153 R154;Add R1481.

P14: Change RP1 RP5 RP9 RP6 RP10 RP7 RP11 RP4 RP8 RP12.

2008/12/22

P21: xchange ODD and INVERTER sensor channal for layput,and U70 from NC.

P16: Change R233 from 10K to 1K.

P11: Change L6 L8 CAP2 CAP3.

P13: Change CN1 CN2.

P29: Change 1L-FDLW31S-N900 to 1L-FWCM321-6F00.

P24: change the U_CN1 & U_CN2 location.
change new parts L17 L20 L21

2008/12/23

P16: Change R249 ;Change +1_5VRUN to 1D5V_PE_ICH;Add C1261 and NC it.

P10: Change R162~ R169.

P06: Change C36.

2008/12/24

P04: NC RP41,for disable TUNER CLK.

P19: add R1483.

P31: Change U23.

P15: Add Q117 R1482.

P17: Change CAP43 CAP44.

P25: Delete R916; Add L79 for EMC

P11: Stuff R188;NC R185.

P06: NC R115;Change R113.

P35: CAP28 CAP32 change from 33u_25v to 10u_10v *3.
R1428 R1430 R1433 change to NC.
DSPO_GND change name to O_GND.
R1435 R1436 R1437 R1438 R1439 R1440 R1441 R1442 change from 100_J to 47K_J.
C447 change to NC.
Delete R563, R1123 , and add Tp486.

P39: Add R1495 3.3_J R1496 3.3_J.
Add R1497 0_J R1498 0_J R1499 0_J R1500 0_J.

P34: Add U88.

P29: add a 16-RSB12JS-2000 diode.
add two 1C-2B20471-K000 cap.
add a 16-SMD15C0-0000 diode.

P27: default NC.

P59: Add PR137 to reserve.
Change PR245 from NC to 100K.

P27: Delete R944.

P31: Add 1000pf cap for each data of MS.and SD.

P32: add the resistors for emc.

2008/12/25

P27: add 1R-0000000-J500 resistor.

P21: add diode for CA.

P05: change R1333 from NC to STUFF and delete R1480.

2008/12/26

P19: change R272 R274.

P11: change L4 L5.

P21: change R1052 R1053.

P17: change L77.

P04: Add R1286 R1287.

P27: Change 16-BD4148F-PT00 to 16-PACDN04-2Y00 diode.

P26: add 1uF and 0.1uF for PLLVDD.

2008/12/27

P16: Change C153 C154.

P17: Change C165:Add R1522.

P15: Add CN46.

P16: Delete R998.

P04: Change Q3.

P19: Change Q14 Q98.

P15: Change Q117.
Add R1534 R1535.

P34: Add R1523 0_J.
U88 change to OR Gate for cost down.
Add R1524 NC_10K R1525 NC_10K R1526 NC_10K R1527 NC_10K.
R1339 mount 10K.

P35: Delete c1267 c1268 c1269 10U_6.3V_M,C1271NC_10U_6.3V_M.
Add C1290 0.1U_16V_Y.
Delete C1188 47u and add C1188 22u C1292 NC_22u.
Add C1297 0.1U_16V_Y.
Change C1127 from 10u to 4.7u.
Add C1291 0.1U_16V_Y.
Change C1160 from 10u to 4.7u.
Change C1184 from 47u to 22u C1185 change from 47u to NC_22u.
C1105 C1106 C1110 change to 0.1U_6.3V_K_X5R.
R1487 R1489 change to 13.3K_F Delete R1488 R1450.
R1491 change to 33K_F.
Add U89 M74VHC1GT04DFT2G.
Add R1528 NC_0_J.
Change C405 C406 C394 C393 C398 C400 to 4.7U_6.3V_K.

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Title: **Revision History(2)**

Size: A3 | Document Number: **AIO-C Mother Board MP** | Rev: 1.1

Date: Tuesday, July 15, 2008 | Sheet 75 of 80

P37: Change L37 L38 to R1520 0_J R1531 0_J.
Delete R1493 R1494 0_J.
Change C415 C416 to NC_1000P_16V_K.
Change C417 C418 to NC_470P_50V_K.
Change C1162 C1163 to NC_1000P_50V_M.
Delete GP6 .

P39: Add R1532 NC_10K_J.
Change C1020 to 2.2U_10V_M.
Change C1017 C1025 to 0.1U_16V_K.
Add C1294 22U_16V_M.
Delete C1018 0.1U_16V_K.
NC CAP41 470u.
Add C1295 22U_6.3V_M C1293 0.1U_16V_Y.
Change C1250 C1251 C1252 to 10U_16V_M.
Add R1538 20k_J change R1581 from 10K_J to 20K_J.

P11: Add CAP49.

2008/12/28

P07: Change CAP27.

P17: Change D30 D31.

P27: Add Wireless Lan SW2 &R1540 &C1299.

P31: Change LED2 from vertical to horizontail for ME request.

P36: Add C1300 NC_470P_50V_K_B.

P50: add one 1206 CAP for future use.

P40: change CAP46.

P41: 2 resistors for strap0.

P42: add tp for FBA_CS1#, connect GPU CMD27 to memory BA2.

P46: add Recommended Power sequencing order.

2008/12/29

P04: Add R1543.

P16: Delete R998.

P35: mount R1528 0_J.
Delete U35 R1256 C1128 R1257 C1254.

P20: change D32.D33.D34.

2008/12/30

P22: Change SPI ROM U14 from WINBOND (13-W25X80V-7000) to ATMEL(13-AT26DF0-7000).

P11: Add C1302~C1304.

2008/12/31

P29: Change L30 1L-BMP2160-8D00 to 1L-BT11005-0501.

P29: Change L27 1L-BMP2160-8D00 to 1L-BT11005-0501.

P11: Delete CAP49.

2008/01/01

P34: U88 change from TOSHIBA to ON.

P37: Delete R1445 and R1446,NC_0_J,Add C1305 NC_470P_50V_K_B C1306 NC_470P_50V_K_B.

2008/01/02

P17: Change L12 L13 L14.

2008/01/03

P29: Change L27 1L-BT11005-0501 to 1L-BTB1005-0502.
Change L30 1L-BT11005-0501 to 1L-BTB1005-0502.

P09: Delete test piont for layout.

P34: change C388 from 1C-2Y20105-Y000 to 1C-2B30105-K001.

P35: change C1270 from 1C-2B70106-M100 to 1C-2B70106-M200.

P39: delete R1538,r1501,change C1131 from 1C-2B30105-K300 to 1C-2B20153-M000,change R1259 from 1R-0000103-J200 to 21R-0000203-J200,Q115b 5D5VAMP 10K_J pull high.

2008/01/04

P62&28: delete +5VRUN_TV&+3VRUN_TV circuit and connect them to +5VRUN&+3VRUN directly.

P15: Change Q117 to PDTC144EU.

P60: Add PJ25 open jumper.

P06: delete R856&R1167, add Q118.

P60: change U14 from 8Mbit to 32Mbit for Eaglelake QST Support.

P54: Add PR218,PR219.

P59: Change PR139 from NC to mount.

2008/01/05

P39: Add R1546 :1R-0000103-J300 C1308:1C-2B30105-K200;Delete C1285, C1296, R1470.

P24: change the usb_gnd to usb1_gnd.

P06: Add R1547 R1548 R1549.

P11: Change C56 C66 C67 C68 C74 C75 C76 C77 C1302 C1303 C1304 from 1C-2B30225-M200 to 1C-2B30225-M201.

P17: Change C169 from 1C-2B30225-M200 to 1C-2B30225-M201.

2008/01/06

P22: Add C1310.

P14: Delete RP8;Add RP52 RP53.
SWAP PR52&PR53 for layout request.

P15: Delete TP140 for layout request.
add C145&C146&C147.
Mount R1521,NC R1454.

P16: Add C1261.

2008/01/07

P17: Connect C192 from +3VALW to VCCLAN3_3_ICH.

P15: Connect C145,C146,C147 from FAN1_TACH,FAN2_TACH,FAN3_TACH to FAN1_TACH_R,FAN2_TACH_R,FAN3_TACH_R.

P16: Delete EEPROM U87 for cost down.BIOS will use other methodology to store those System Information in SPI Flash ROM instead of EEPROM.

P24: change the position of L17 and D17,L20 and D19,L21 and D20, L16 and D15,L23 and D22.

P39: Change R1532 pin2 ,C1015 pin2 , C1019 pin2,C1126 pin1, U67 pin 37 ,16, 17, 18,3,1,R1241pin2,R1126 pin2, R1122 pin2, C1294 pin2,Q115B Pin4 from GND to PGND.

2008/01/08

P15&16: Delete TP153,TP460 for layout.

P07&40: Change CAP27&CAP46 from 1C-42T0107-M100 to 1C-42T0107-M101.

P15&16: NC R1521,mout R1454.

P22: change R338&R336&R332 from 0603 to 0402 delete IFPE_PLLVDD IFPE_RSET IFPC_PLLVDD IFPC_RSET to GND resistor.

2008/01/09

P24: change the D17&D19&D20 from GND to USB_GND.

2008/01/16

P35: Y9 change from 1F-X24M576-3003 to 1F-X24M576-3004.

P37: R507 R508 R509 R511 R512 R513 change from 0603 to 0402.
Delete R498 NC_0_J,Delete R1315 NC_0_J.

P39: Add R1550 0_J R1551 0_J.

P09: Change R142 R143 from 0603 to 0402.

P29: change U20 from15-S19183D-0001 to15-S1P2110-0000.

P27: add three N-mos for MOR feedback request.

P15: add R1553.

P39: Add C1315 NC_22U_16V.

P62: Change PR185,PR188,PR186,PR189,PR187,PR193,PR199,PR194, PR200,PR192,PR202,form 0603 to 0402 .

2008/01/16

P15&16&17&25&26: Change from MARVEL 10/100 LAN to Intel GLAN.

P62: Change PR186 from 100K_J to 47K_J.

P27: change Q120 from17-2N7002E-PT00 to 17-PDTA144-ET00.
delete R1552 and add 1K and 100K J.

P17: change L14 from 1L-DTL3216-1100 to 1L-DEBLS32-2501.

P26: change CN32.

2008/01/22

P37: R1593 & R1609 not connect to A_GND.

P39: delete L79 L81 L83 L85.
Delete C1381 22U_16V_M Delete C1384 22U_16V_M Add CAP50 220u.
Add FUSE F10 24V-3.15A_0603 Add bead L87 120R-100MHZ_1206

P60: Add PR154/ PR162/PR170 and reserve PR161/PR169/PR170..

P10: Change R157 R158 from 10Kohm to 0ohm.

2008/01/24

P57: cancel PC114,PC178,PC179;Add PCAP7 .

P32: Add the CIR circuit.

P19: ADD POWER DOWN TIMING CIRCUIT,change R288 ,R275, R276 from 0k to 1k.

P04: NC RP51.

P32: Add this circuit for power led not off when press power button for 4 second.

P13: Change CN1 CN2.

2008/01/25

P29: NC C1273 and C1274.
Add two 0_J resistor.

P16: Connect R241 pin2 to CIR_WAKE# signal.

P24: Delete the D18&D21.

P23: Delete the D13.

P32: update the holes.

2008/01/26

P32: Change the H7~H10.

P36: Change R560 from 5.6K_J to NC_5.6K_J.

P37: Change R1614 to NC;Add A_GND with R1593 pin 2;Add A_GND with R1609 pin 2.

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Title: *Revision History(3)*

Size: A3 | Document Number: AIO-C Mother Board MP | Rev: 1.1

Date: Tuesday, July 15, 2008 | Sheet 76 of 80

P39: Change C1376, C1377 from 0.22U_6.3V_K to 0.1U_6.3V_K;
Change C1378 from 1C-2B70105-M000 to 1C-2B30225-M201.

2008/01/27

P07: Add CAP51.

P21: change EMC1103 to EMC1133 for inverter sense comand.

2008/01/28

P04: Add Q126,R1654,R1655 for+3VRUN leakage in S3,S4,S5 stage.

P27: Add Q127,R1656 for +3V_EMINI_AUX not discharge.

P29: Add Q128,R1657 for +5VSUS_R not discharge.

P37: Change C1348,C1354 from 1C-2Y20105-Y000to1C-2Y30225-Y000.
Change R1595 from 100_J to NC.
Change C1363,C1366 from 1C-2Y20105-Y000to1C-2Y30225-Y000.
Change R1598 R1615 from 1R-0000273-F200to1R-0000223-F200.
Change R1632,R1605 from 1R-0000103-F200to1R-0000223-F200.
Change C1349, C1350, C1364,C1365 from 1C-2B20683-K000 to 1C-2B30224-K000.
Change the EQ circuit to this circuit.

P39: Change R1627 from 10K_J to NC_10K_J.
Change R1629 from NC_10K_J to 10K_J.

P53: PL1 P/N change 1L-FPWC121-0S00 to 1L-FPWC121-0S01.

P59: change PR121,PR126,PR123 from 270ohm to 392ohm.

2008/01/30

P37: Change L78 from 1L-BBLM06P-G101 to 1L-BACMS16-0804.

P56: Change PC102 from 220u_2.5V_M to NC.

P57: Delete Open Jumper PJ17.

P60: Delete PL11.

P62: Change PR203 PQ53 from NC to Mount.

P27: Add R1680;Change RUN_ON# to SUS_ON#;Change Q110,D35.

P29: Delete L30,add R1681.

P32: Change POWER_LED to POWER_LED#.

P22: Stuff R332.

P24: change usb1_gnd and usb_gnd to gnd;Change L15,L18,L19, L22,L24 to 0ohm resistor.

P25: Add C1413 for EMI.

P26: Delete C943;Add R1679 and NC it.

P16: Add R1682,C1414 for PWRSW# debounce.
Remove LED transistor from power D/B to M/B.

2008/01/31

P34: Change C388 from 1C-2B30105-K001to 1C-2B30106-M100.

P40: Change C547 HH.PN from 1C-2B20104-K101to 1C-2B20104-K000.

P26: Add R1691 and NC it.

P24: Add the D16,D18,D21.

P29: Swap L28,R401,R398.

P32: Change the H7~H10.

P16: Connect WLAN_BT_OFF to GPIO8.

P15: Remove DIP_SW from GPIO8 to GPIO4.
Remane WLAN_BT_SW# to WLAN_BT_ON#.

P21: Change +3VRUN to +3VSUS_BL;Add R1694 R1695 R1696 R1697.

2008/02/01

P34: Change C363 from 1C-2Y20103-Y300 to1C-2Y20103-Y000.

P32: Add the boss location.
change the CN47 and change the CIR circuit.

P59: Change PC145/PC148/PC154 from 100p to 68p.
Change PR130 from 680 ohm to 976 ohm.

P62: Change net +3VALW to +5VALW.
P34: Change this direction to reverse.
P36: Change C447 from NC_1000P_16V_K to 1000P_16V_K.

P39: Change L80,L82,L84,L86 from 1L-BEBMS10-0500 to 1L-BACMS16-0804.

2008/02/02

P32: Add Q134.

P16: NC R1700.

2008/02/03

P19: Change VRM_PWRGD delay circuit(addQ135,Q136,Q137,R1710~R1715)

2008/02/04

P19: Change VRM_PWRGD delay circuit.
Delete D3 add Q138.

P15: Change USB port pull up power from 3VALW to +3VALW.

P19: Reserve R1715 For CL_PWROK.

P16: Add pull up R.

P27: change R1582 from 100K to 10K.

P56: NC PC103.

P61: Change PJ22 from PR183.1 connection to PR183.2 connection.

2008/02/05

P15: add pull up for GPIO49.

P16: reserve pull up for GPIO24.

P56: Delete JUMP for +1_5VRUN.

P16: change R249 from 22.6ohm to 24.9ohm.
Add 4 pcs 0.1uF cap for +1_1VRUN.

P07: Add 2 pcs 0.1uF cap for VHCORE.

P16&15: Change BR_PRS# from OC7#/GPIO31 to GPIO57.

P27: change +3V_EMINI_AUX discharge circuit.

P05: Delete TP_GPIO57 dummy net.

P15: delete ICH_EEPROM_RW# dummy net.

P36: Add Q140, R1723 for GPIO.

P15: Reserve pull up for HW_POP_MUTE_ICH.

2008/02/10

P26: Exchange RJ45_6,RJ45_4,RJ45_5.
Delete R1569~R1576.

P32: Delete R1690.

P25: Delete R1566.

P45: change R1503 from NV_XTALIN to NV_XTALOUT.

2008/02/12

P06: Change C36 HH P/N from 1C-2B20103-K100 to 1C-2B20103-K200.

P22: Change U13 HH P/N from 14-NC7S32M-5X00 to 14-MC74HC1-G300.

P53: Change PU3 HH P/N from 15-LMC7225-0000 to 15-NCS2202-0000.

P61: Change PU20 HH P/N from 15-LMC7225-0000 to 15-NCS2202-0000.

P42: Change C583,C590,C1193,C1194,C1195 HH P/Nfrom 1C-2B20472-M000 to 1C-2B20472-K001.

P43: Change C618 HH P/N from 1C-2B20471-M000 to 1C-2B20471-K000.

P05: change U2 footprint.

P15: Stuff R203,R206.

P20: Stuff CN38,R1270,D34,C1070.

P26: Delete Net "GND_EMI".

2008/02/18

P33: change the codec name from ALC262 to ALC889S.

P35: change R472,R471,R474,R475,R483,R481,R489,R486 from 5% to 1%

P36: Change R560 from 5.6K_J to NC_5.6K_J for MOR request.

P39: delete PQ75,PQ76,PR248 of protective circuit for MOR repuest.

2008/02/19

P35: Change the precision of R480,R484,R478,R488 from 5% to 1% for MOR request.

2008/02/20

P29: NC D39.

P56: change PR71 from 1R-0003011-F200 to 1R-0003571-F200;change PR72 from 1R-0003571-F200 to 1R-0004021-F200.

P11: change R186 from 1R-0002370-F200 to 1R-000402X-F200;change R189 from 1R-0000201-F200 to 1R-000392X-F200.

P10: change R171 from 1R-0004750-F200 to 1R-0004640-F200.

P40: change C531,C532, C669, C1055 from 1C-2B20474-M000 to 1C-2B20474-K100.

P59: change PC151 from 1C-2B20681-M000 to 1C-2X20681-K600;change PC145,PC148,PC154 from 1C-2N20680-K000 to 1C-2N20680-J000.

P62: NC PR206, PR207, PR208, PR195.

P31: NC C337 for MOR requirement.

2008/02/21

P28: Connect CN39 Pin43,pin37,pin18 to GND.

P31: Change Q31from 17-DTC144E-UA00 to17-PMBT390-4200;Add R1725.

P27: Add R1726 and NC it;Remove R948,connect CN33 pin40 to GND.

P13: Add R1727,R1728 and NC them.

P19: NC R272,R274,R269,Q8;Add Q141,D42,D43,R1729,R1730,R1731.

P16: NC R246.

P06: Add Q142,Q143,R1732,R1733.

P56: change PR66 PN fom 1R-0000101-J200 to 1R-0000102-J200.

2008/02/22

P24: Remove USB power switch circuit U15,U16,U17,U63,U64,C979, C980,C242,C243,C981,C978,C974,C975,C976,C977;Add Q144,Q145, F13,F14,F15,R1734~R1737,C1425.

P15: Remove USB_OC#0~4 ports.
P19: Change C202 from 0.1u to 0.22u for timing.

P17: Add D44,D45 and NC them for VCC1_5,VCC1_1/V_CPU_IO power sequencing.

2008/03/01

P34: change C354 from 1C-2B30475-K100 to 1C-2B70475-K100;change C920 from 1C-2B20104-K100 to 1C-2Y20104-Y000;change C389 from 1C-2B20103-K001to 1C-2Y20103-Y000.

P35: hange C1300 from 1C-2B20471-K000 to 1C-2B20471-K200.

P38: change C1305 from 1C-2B20471-K000 to 1C-2B20471-K200.

P39: change R1316,R1318 from 1R-0000682-J200 to 1R-0000682-F200;
change R1320,R1321 from 1R-0000203-J200 to 1R-0000203-F200;
change C1306 from 1C-2B20471-K000 to 1C-2B20471-K200.

2008/03/05

P04: NC R1333.
P19: Connect WLAN_BT_SW_CL# to GPIO8.

P05: Delete R1050~R1057;Change Q4,add R1740.
P30: Add R1741,R1742.
P18: NV R1281,R1337for M810 H;CA R1284,R1336 for M810 L;AddR1743.

2008/03/07

P14: NC R197,stuff R1727,R1728.

P23: Change R292 from 100K to 220k,C202 from 0.22u to 0.1u for timing;Delete R281,R285.

P17: Change R1699 from 10K to 20K.

P06: Add C1426.

P03: NC C26,C1286,C1287.

P18: Connect CL_VREF_ICH from +3VRUN to +3VALW.

P25: Change C1319 from 4.7u to 10u,addC1427,C1428;NC C1330,C1329.

2008/03/14

P05: Change R85~R91 from 1R-0000620-F200 to 1R-0000620-J200.

(Page35) Delete R563

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Title: *Revision History(4)*

Size: A3 | Document Number: AIO-C Mother Board MP | Rev: 1.1

Date: Tuesday, July 15, 2008 | Sheet 77 of 80

2008/04/02

P54 Delete C1262, C1263 for Headphone THD+N

P61 add pc229 pc230 pc231

P62 change PR218 from 0ohm to 3.3ohm ,
change PR219 from 0 ohm to 3.3ohm

P67 change PR150,PR152,PR158,PR160,PR166,PR168
from 0 ohm to 2.2ohm.

P68 change PR81 from 0 ohm to 3.3 0ohm

P70 change PR265 from NC to 2k

P19 Change C153,C154 from 18PF to 12PF

P39 Change C318,C324 from 10PF to 22PF.

2008/04/03

P54 Change C921 from NC to not NC for EMI

P55 Change C1305 C417,C418 from NC to not NC for EMI

change R1530,R1531 to L89,L90 for EMI

P57 change R1316,R1318 from 1R-0000682-F200 to
1R-0000332-F200 for FSIV

2008/04/06

P31 Add this RC circuit for inrush current.

P11 Add C1426 C1431 C1432 and C1433 for simulation

P14 Add C1436 and C1446 for simulation.

P15 Add C1447 and C1448 for simulation.

P17 Add R417.

P24 Del R1712

P31 Change F1 F2 F13 F14 and F15 from 1M-F0061A5-F000 to

P19 Change Y2 from 1F-X32M768-1000 to 1F-X32K768-1000,
the same as M8230.

P37 NC R1452

P3 Change from +3V_CL to +3VALW

P19 Add R242 and R272 for corwin spring

2008/04/08

P15 Add C1449.

P10 Add C1450

P61 add PR74

P66 change pr136 from 931k to 910k

P69 add PR236

P71 change PCAP9 from 1C-10U0227-M100 to
pc114 1C-31R0227-MX00

P71 Delete PR271

2008/04/09

P14 Reserved C149 for sinulation.

P46 U44 change from NV_MK1726-08 to P1819EF-08SR

P48 U59,U60 change from HYB18H1G321AF-14 to
HYB18H1G321AF-11

2008/04/10

P54 Change R987,R989 from 1R-0000000-J200 to
1R-0000102-J200;Add 4700pF to A_GND

P56 Change this latch circuit to NC

P51 Change CAP21 to C1451

2008/04/14

P4 R1333 from NC to stuff

P35 R1353 Change to NC

P35 Add C1058

P23 R292 Change to NC

P23 Change R1730 to NC

P23 Change R270 from 100k to 10k.

P23 Add C1454

P23 Change R263 from 1K to 0_J

P23 Change R1819 from 100K to 1M

P32 Change R1540 from 10K to 4.7K

P24 Change R275,R276 from 1K to 0_J

P32 Change R956 from 10K to 100k same as AIO-A/B

P3 Change the position of R1768

P37 Change Q110 from BJT to MOS

P29 Add R1490 and R1491same as AIO-A/B

P66 Del PR235

P24 Change R1824 to NC

P24 Change R1830 from 47K to 10K

P25 Change the position of R1035

P3 Add R15 R16

P68 Chang PC111 from 3300p to 4700p

P70 add pr275 pr274 pr273 pr272 pr271 for discharge

P56 Delete Q115,add Q170,Q171

2008/04/15

P33 Change F5 from 0.35A to 0.25A

2008/04/16

P25 Add C347 C348 for EMI's request

P29 Add C338 for EMI's request

P28/29 Change U21 from 12-R5C8330-0000 to 12-R5C833T-0000

P30 Stuff CAP6 for EMI's request

P30 Add C349 C350 for EMI's request

P31 Mount common choke and bead for USB signal and power rail for
rear/side USB ports for EMI's request

P51 Change from 0ohm to L96 for EMI

P51 Add C353 for EMI's request

2008/04/18

P25 Delete R1691 and R1679,and NC CN32 PIN9,10

P56 Delete L80, L82, L84,L86,C1385,C1391,C1390,1394; and
change C1386 & C1388 & C1392 & C1396 from 0.22uF to
0.047uF for YAMAHA's request

P56 Change C1386 & C1388 & C1392 & C1396 from 0.22uF to
0.047uF for YAMAHA's request

P56 Add Schottky-Diode to preventing the destruction of
amp.when the output line short-circuits.

P46 Add 2nd source P1819GF-08SR

P33 Exchange the DMIC_DATA and DMIC_CLK

P19 Change GPIO11 to WLAN_EN#

P23 Change R1819 from 1M to 220K

P24 Change R1824 from 10K to 100K, and stuff

P34 Change F4 from 0.35A to 0.25A

2008/04/19

P33 Stuff L29 for Camera eye diagram fail.
P26 Pull up CLKREQ# follow AIO-B.
P35 Stuff R1353
P35 NC U70.9 for the address 49H
P23 Change R271 to 10K and NC it.
P18 Add R1553.

2008/04/21

P11 Change L7 from 1L-DEBLS20-1200 to 1L-DTW2012-0900
P54 Change U24 name from ALC889S to ALC889DSD
P56 Add 0_j for mor request
P30 Change CAP5 from 1C-44T0476-M301 to
1C-10U0476-M400 same as M840.

P30 Change CAP6 from 1C-41S0476-M000 to
1C-44T0476-M301 same as M840.

P37 Reserved R1691 C1425 R1706 and C1445

P58 Change +3VRUN to +3VALW

2008/04/22

P3 Add C1465 C1466 and NC for RF request.

P29 Stuff C1277 and change to 15pf for overshoot

P23 Add U108.

2008/04/23

P19 Add R1456 R1457.

P19 Delete R1816,R1817 and add R1826,Q157 for layout routing issue

P18 Mount R1766 and no mount R1765 to support Wake up on Intel LAN

2008/04/24

P56 dvt: Add C1468 for mor request

p54 Add R1832,R1833 for mor request

change R987,R989 from 1k to 680ohm

P33 Add R407 0ohm and reserve R417 for Camera power change

2008/04/28

p55 Change C1305 from 1C-2B20471-K200 to 1C-2B20471-K000

2008/04/29

p54 Change C1452,C1453 from 1C-2B20472-K002 to 1C-2B20472-K001 for materia
prepared.

2008/05/07

P3 Correct DVT1 net error issue.

PVT

2008/05/28

P23 Change R268 from 180K to 20K follow the design guid
P23 Change C199 from 0.1U to 1U follow the design guid
P26 Change the SW circuit for the SW function inverse
P8 Back up C2620 and C2621 for black screen issue.
P54 Change this portion from NC to stuff for PC beep

2008/05/30

P8 Change R153 and R154 from CA to NC.
P21 Move PJ1 from SB_SRTCRSTB to SB_RTCRST# follow Design guid 1.3
P62,63,64,65 Del:PJ2,PJ3,PJ4,PJ6,PJ7,PJ8,PJ12,PJ13,PJ14,PJ18,PJ19,PJ20,PJ23
P70 NC PQ50,PQ64,PQ50,PQ64,PQ55,PQ56,PQ57,PQ58,PQ59,PQ60,PQ63.
P68 Change PCAP8 P/N from 2C-I070I07-M403 To 2C-I070I07-M409.
P50 Change Q116 from stuff to NC;Change R1345,R1346 from NC to stuff.
P51 Add this circult to improve the inv_enable to avoid margin.

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Title: Revision History(5)

Size: A3 | Document Number: AIO-C Mother Board MP | Rev: 1.1

Date: Tuesday, July 15, 2008 | Sheet 78 of 80