Kirin (FX2 with NS)

VER : 3A

PWA : UW521
PWB : UW509

DDRII-SODIMM1 PG 7,8 — 533 MHz DDR II
DDRII-SODIMM2 PG 7,8 — 533 MHz DDR II

AMD S1
Turion 64 Rev.F Dual-Core/ Sempron Rev.F Single-Core
Dual-Core 35W / Single-Core 25W
(638 S1g1 socket)
PG 3,4,5,6

HT_LINK(800 MHz)

CPU VR PG 37	**CLOCKS** PG 13	**Thermal Monitor** PG 35	**SYSTEM** PG 38	**VCCP DDR II** PG 39	**BATT CHARGER** PG 36	**AC/BATT Conn.** PG 41	**RUN POWER SW** PG 40

Panel Connector PG 18 — LVDS
VGA Conn. PG 19 — VGA

RS485 A12
465 FCBGA
PG 9,10,11,12

PCI-E(1) → **Express Card** PG 25
USB2.0(P1)
PCI-E(2) → **Mini Card (WLAN)** PG 24
USB2.0(P5)
USB2.0(P0,P2) → **USB Conn. Right Side x2** PG 28
USB2.0(P4,P6) → **USB Conn. Back side x2** PG 28

A_LINK

SATA - HDD PG 23 — SATA II
Fixed PATA ODD PG 23 — IDE

SB600 A13
549 BGA
PG 14,15,16,17

AC97/Azalia
33MHz PCI

BCM4401 (rev. B0) PG 33 → **RJ45/Magnetics** PG 34
3 in 1 Card R5C832 PG 20,21 → **3 in 1 Conn.** PG 22
Mini PCI(for debug) PG 42

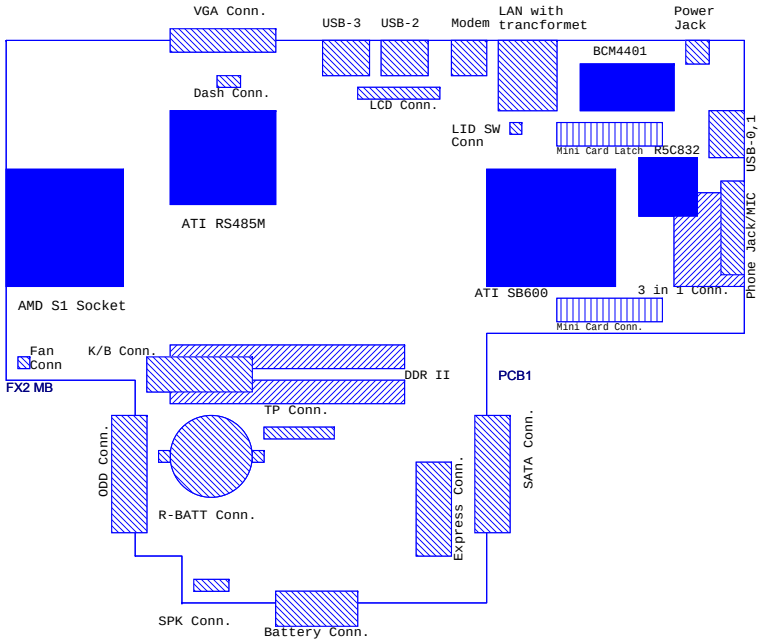
AUDIO PG 31 → **Audio Jacks** PG 32
MDC PG 26 → **Tip Ring** PG 26

LPC

KBC
NS97551/87541
PG 27

X-Bus

KB Conn. PG 35
Touch Pad PG 30
Flash ROM PG 27



QUANTA COMPUTER

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QUANTA COMPUTER

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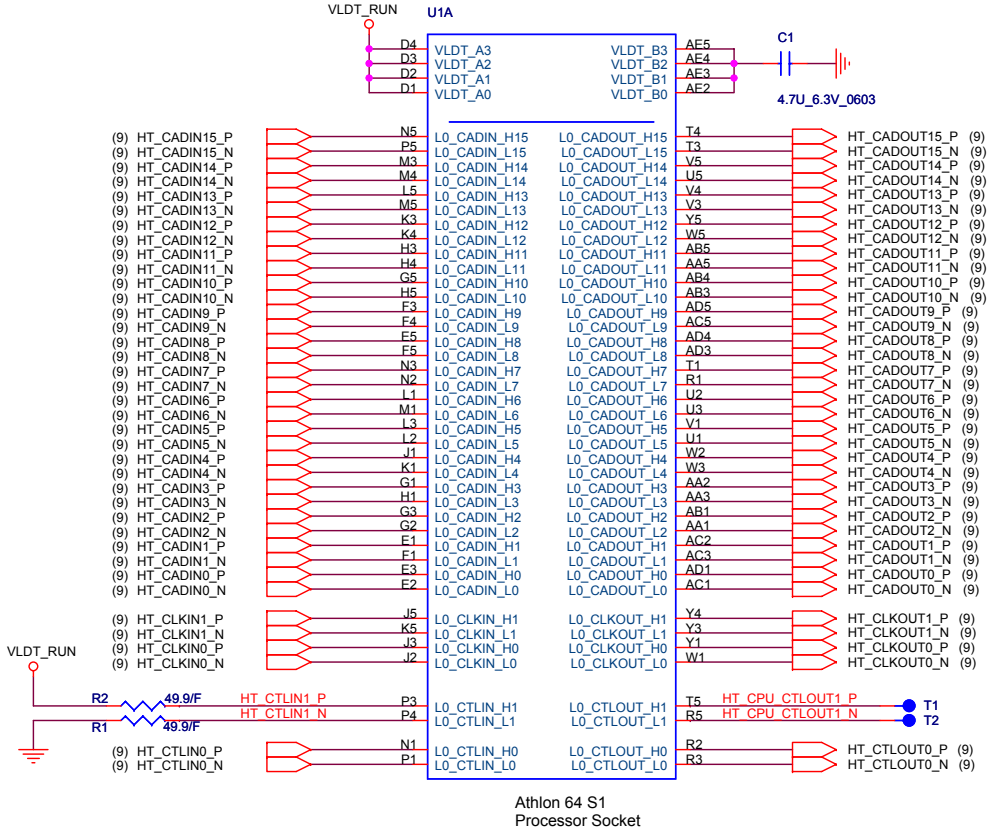
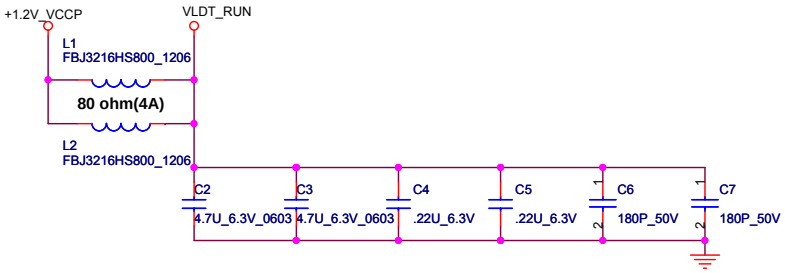
PROCESSOR HYPERTRANSPORT INTERFACE

VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



Athlon 64 S1
Processor Socket



LAYOUT: Place bypass cap on topside of board

NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
PLACE CLOSE TO VLDT0 POWER PINS

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Title	ATHLON64 HT I/F	
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Processor DDR2 Memory Interface

VDD_VTT_SUS_CPU IS CONNECTED TO THE VDD_VTT_SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

PLACE THEM CLOSE TO CPU WITHIN 1"

+1.8V_SUS
R3 2K/F
CPU_M_VREF
C8 .1U_10V
C9 1000p_50V
R4 2K/F
(39) VTT_SENSE
VTT_SENSE
C677 470P_50V
R6 39.2/F
R5 39.2/F
R566 0

U1B

MEMVREF W17
VTT_SENSE Y10
MEMZN AE10
MEMZP AE10
M_ZN
M_ZP

VTT1 D10
VTT2 C10
VTT3 B10
VTT4 AD10
VTT5 W10
VTT6 AC10
VTT7 AB10
VTT8 AA10
VTT9 A10
+0.9V_DDR_VTT

(7,8) M_A_CS#3 V19 MA0_CS_L3
(7,8) M_A_CS#2 J22 MA0_CS_L2
(7,8) M_A_CS#1 V22 MA0_CS_L1
(7,8) M_A_CS#0 T19 MA0_CS_L0

MA0_CLK_H2 Y16 M_CLKOUT1 (7)
MA0_CLK_L2 AA16 M_CLKOUT1# (7)
MA0_CLK_H1 E16 M_CLKOUT0 (7)
MA0_CLK_L1 F16 M_CLKOUT0# (7)

(7,8) M_B_CS#3 Y26 MB0_CS_L3
(7,8) M_B_CS#2 J24 MB0_CS_L2
(7,8) M_B_CS#1 W24 MB0_CS_L1
(7,8) M_B_CS#0 U23 MB0_CS_L0

MB0_CLK_H2 AF18 M_CLKOUT4 (7)
MB0_CLK_L2 AF17 M_CLKOUT4# (7)
MB0_CLK_H1 A17 M_CLKOUT3 (7)
MB0_CLK_L1 A18 M_CLKOUT3# (7)

(7,8) M_CKE3 H26 MB_CKE1
(7,8) M_CKE2 J23 MB_CKE0
(7,8) M_CKE1 J20 MA_CKE1
(7,8) M_CKE0 J21 MA_CKE0

MB0_ODT1 W23 M_ODT3 (7,8)
MB0_ODT0 W26 M_ODT2 (7,8)
MA0_ODT1 V20 M_ODT1 (7,8)
MA0_ODT0 U19 M_ODT0 (7,8)

(7,8) M_A_A[0..15]

M_A_A15 K19 MA_ADD15
M_A_A14 K20 MA_ADD14
M_A_A13 V24 MA_ADD13
M_A_A12 K24 MA_ADD12
M_A_A11 L20 MA_ADD11
M_A_A10 R19 MA_ADD10
M_A_A9 L19 MA_ADD9
M_A_A8 L22 MA_ADD8
M_A_A7 L21 MA_ADD7
M_A_A6 M19 MA_ADD6
M_A_A5 M20 MA_ADD5
M_A_A4 M24 MA_ADD4
M_A_A3 M22 MA_ADD3
M_A_A2 N22 MA_ADD2
M_A_A1 N21 MA_ADD1
M_A_A0 R21 MA_ADD0

MB_ADD15 J25 M_B_A15
MB_ADD14 J26 M_B_A14
MB_ADD13 W25 M_B_A13
MB_ADD12 L23 M_B_A12
MB_ADD11 L25 M_B_A11
MB_ADD10 U25 M_B_A10
MB_ADD9 L24 M_B_A9
MB_ADD8 M26 M_B_A8
MB_ADD7 L26 M_B_A7
MB_ADD6 N23 M_B_A6
MB_ADD5 N24 M_B_A5
MB_ADD4 N25 M_B_A4
MB_ADD3 N26 M_B_A3
MB_ADD2 P24 M_B_A2
MB_ADD1 P26 M_B_A1
MB_ADD0 T24 M_B_A0

M_B_A[0..15] (7,8)

(7,8) M_A_BS#2 K22 MA_BANK2
(7,8) M_A_BS#1 R20 MA_BANK1
(7,8) M_A_BS#0 T22 MA_BANK0

MB_BANK2 K26 M_B_BS#2 (7,8)
MB_BANK1 T26 M_B_BS#1 (7,8)
MB_BANK0 U26 M_B_BS#0 (7,8)

(7,8) M_A_RAS# T20 MA_RAS_L
(7,8) M_A_CAS# U20 MA_CAS_L
(7,8) M_A_WE# U21 MA_WE_L

MB_RAS_L U24 M_B_RAS# (7,8)
MB_CAS_L V26 M_B_CAS# (7,8)
MB_WE_L U22 M_B_WE# (7,8)

DDR II: CMD/CTRL/CLK

Athlon 64 S1
Processor Socket

U1C

(7) M_B_DQ[0..63]

M_B_DQ63 AD11 MB_DATA63
M_B_DQ62 AE11 MB_DATA62
M_B_DQ61 AE14 MB_DATA61
M_B_DQ60 AE14 MB_DATA60
M_B_DQ59 Y11 MB_DATA59
M_B_DQ58 AB11 MB_DATA58
M_B_DQ57 AC12 MB_DATA57
M_B_DQ56 AF13 MB_DATA56
M_B_DQ55 AE15 MB_DATA55
M_B_DQ54 AF16 MB_DATA54
M_B_DQ53 AC18 MB_DATA53
M_B_DQ52 AF19 MB_DATA52
M_B_DQ51 AD14 MB_DATA51
M_B_DQ50 AC14 MB_DATA50
M_B_DQ49 AE18 MB_DATA49
M_B_DQ48 AD18 MB_DATA48
M_B_DQ47 AD20 MB_DATA47
M_B_DQ46 AC20 MB_DATA46
M_B_DQ45 AF23 MB_DATA45
M_B_DQ44 AF24 MB_DATA44
M_B_DQ43 AF20 MB_DATA43
M_B_DQ42 AE20 MB_DATA42
M_B_DQ41 AD22 MB_DATA41
M_B_DQ40 AC22 MB_DATA40
M_B_DQ39 AE25 MB_DATA39
M_B_DQ38 AD26 MB_DATA38
M_B_DQ37 AA25 MB_DATA37
M_B_DQ36 AA26 MB_DATA36
M_B_DQ35 AE24 MB_DATA35
M_B_DQ34 AD24 MB_DATA34
M_B_DQ33 AA23 MB_DATA33
M_B_DQ32 AA24 MB_DATA32
M_B_DQ31 G24 MB_DATA31
M_B_DQ30 G23 MB_DATA30
M_B_DQ29 D26 MB_DATA29
M_B_DQ28 C26 MB_DATA28
M_B_DQ27 G26 MB_DATA27
M_B_DQ26 G25 MB_DATA26
M_B_DQ25 E24 MB_DATA25
M_B_DQ24 E23 MB_DATA24
M_B_DQ23 C24 MB_DATA23
M_B_DQ22 B24 MB_DATA22
M_B_DQ21 C20 MB_DATA21
M_B_DQ20 B20 MB_DATA20
M_B_DQ19 C25 MB_DATA19
M_B_DQ18 D24 MB_DATA18
M_B_DQ17 A21 MB_DATA17
M_B_DQ16 D20 MB_DATA16
M_B_DQ15 D18 MB_DATA15
M_B_DQ14 C18 MB_DATA14
M_B_DQ13 D14 MB_DATA13
M_B_DQ12 C14 MB_DATA12
M_B_DQ11 A20 MB_DATA11
M_B_DQ10 A19 MB_DATA10
M_B_DQ9 A16 MB_DATA9
M_B_DQ8 A15 MB_DATA8
M_B_DQ7 A13 MB_DATA7
M_B_DQ6 D12 MB_DATA6
M_B_DQ5 E11 MB_DATA5
M_B_DQ4 G11 MB_DATA4
M_B_DQ3 B14 MB_DATA3
M_B_DQ2 A14 MB_DATA2
M_B_DQ1 A11 MB_DATA1
M_B_DQ0 C11 MB_DATA0

MA_DATA63 AA12 M_A_DQ63
MA_DATA62 AB12 M_A_DQ62
MA_DATA61 AA14 M_A_DQ61
MA_DATA60 AB14 M_A_DQ60
MA_DATA59 W11 M_A_DQ59
MA_DATA58 Y12 M_A_DQ58
MA_DATA57 AD13 M_A_DQ57
MA_DATA56 AB13 M_A_DQ56
MA_DATA55 AD15 M_A_DQ55
MA_DATA54 AB15 M_A_DQ54
MA_DATA53 AB17 M_A_DQ53
MA_DATA52 Y17 M_A_DQ52
MA_DATA51 Y14 M_A_DQ51
MA_DATA50 W14 M_A_DQ50
MA_DATA49 W16 M_A_DQ49
MA_DATA48 AD17 M_A_DQ48
MA_DATA47 Y18 M_A_DQ47
MA_DATA46 AD19 M_A_DQ46
MA_DATA45 AD21 M_A_DQ45
MA_DATA44 AB21 M_A_DQ44
MA_DATA43 AB18 M_A_DQ43
MA_DATA42 AA18 M_A_DQ42
MA_DATA41 AA20 M_A_DQ41
MA_DATA40 Y20 M_A_DQ40
MA_DATA39 AA22 M_A_DQ39
MA_DATA38 Y22 M_A_DQ38
MA_DATA37 W21 M_A_DQ37
MA_DATA36 W22 M_A_DQ36
MA_DATA35 AA21 M_A_DQ35
MA_DATA34 AB22 M_A_DQ34
MA_DATA33 AB24 M_A_DQ33
MA_DATA32 Y24 M_A_DQ32
MA_DATA31 H22 M_A_DQ31
MA_DATA30 H20 M_A_DQ30
MA_DATA29 F22 M_A_DQ29
MA_DATA28 E21 M_A_DQ28
MA_DATA27 J19 M_A_DQ27
MA_DATA26 H24 M_A_DQ26
MA_DATA25 F22 M_A_DQ25
MA_DATA24 F20 M_A_DQ24
MA_DATA23 C23 M_A_DQ23
MA_DATA22 B22 M_A_DQ22
MA_DATA21 F18 M_A_DQ21
MA_DATA20 E18 M_A_DQ20
MA_DATA19 E20 M_A_DQ19
MA_DATA18 D22 M_A_DQ18
MA_DATA17 C19 M_A_DQ17
MA_DATA16 G18 M_A_DQ16
MA_DATA15 G17 M_A_DQ15
MA_DATA14 C17 M_A_DQ14
MA_DATA13 F14 M_A_DQ13
MA_DATA12 E14 M_A_DQ12
MA_DATA11 H17 M_A_DQ11
MA_DATA10 E17 M_A_DQ10
MA_DATA9 E15 M_A_DQ9
MA_DATA8 H15 M_A_DQ8
MA_DATA7 E13 M_A_DQ7
MA_DATA6 C13 M_A_DQ6
MA_DATA5 H12 M_A_DQ5
MA_DATA4 H11 M_A_DQ4
MA_DATA3 G14 M_A_DQ3
MA_DATA2 H14 M_A_DQ2
MA_DATA1 E12 M_A_DQ1
MA_DATA0 G12 M_A_DQ0

M_A_DQ[0..63] (7)

To SODIMM socket B (Far)

To SODIMM socket A (near)

(7) M_B_DM[0..7]

M_B_DM7 AD12 MB_DM7
M_B_DM6 AC16 MB_DM6
M_B_DM5 AF22 MB_DM5
M_B_DM4 AB26 MB_DM4
M_B_DM3 E25 MB_DM3
M_B_DM2 A22 MB_DM2
M_B_DM1 B16 MB_DM1
M_B_DM0 A12 MB_DM0

MA_DM7 Y13 M_A_DM7
MA_DM6 AB16 M_A_DM6
MA_DM5 Y19 M_A_DM5
MA_DM4 AC24 M_A_DM4
MA_DM3 F24 M_A_DM3
MA_DM2 E19 M_A_DM2
MA_DM1 C15 M_A_DM1
MA_DM0 E12 M_A_DM0

M_A_DM[0..7] (7)

M_B_DQS7 AF12 MB_DQS_H7
M_B_DQS#7 AE12 MB_DQS_L7
M_B_DQS6 AE16 MB_DQS_H6
M_B_DQS#6 AD16 MB_DQS_L6
M_B_DQS5 AF21 MB_DQS_H5
M_B_DQS#5 AF22 MB_DQS_L5
M_B_DQS4 AC25 MB_DQS_H4
M_B_DQS#4 AC26 MB_DQS_L4
M_B_DQS3 F26 MB_DQS_H3
M_B_DQS#3 E26 MB_DQS_L3
M_B_DQS2 A24 MB_DQS_H2
M_B_DQS#2 A23 MB_DQS_L2
M_B_DQS1 D16 MB_DQS_H1
M_B_DQS#1 C16 MB_DQS_L1
M_B_DQS0 C12 MB_DQS_H0
M_B_DQS#0 B12 MB_DQS_L0

MA_DQS_H7 W12 M_A_DQS7
MA_DQS_L7 W13 M_A_DQS#7
MA_DQS_H6 Y15 M_A_DQS6
MA_DQS_L6 W15 M_A_DQS#6
MA_DQS_H5 AB19 M_A_DQS5
MA_DQS_L5 AB20 M_A_DQS#5
MA_DQS_H4 AD23 M_A_DQS4
MA_DQS_L4 AC23 M_A_DQS#4
MA_DQS_H3 G22 M_A_DQS3
MA_DQS_L3 G21 M_A_DQS#3
MA_DQS_H2 C22 M_A_DQS2
MA_DQS_L2 C21 M_A_DQS#2
MA_DQS_H1 G16 M_A_DQS1
MA_DQS_L1 G15 M_A_DQS#1
MA_DQS_H0 G13 M_A_DQS0
MA_DQS_L0 H13 M_A_DQS#0

DDR: DATA

Athlon 64 S1
Processor Socket

(7) M_B_DQS[0..7]

M_B_DQS0
M_B_DQS1
M_B_DQS2
M_B_DQS3
M_B_DQS4
M_B_DQS5
M_B_DQS6
M_B_DQS7

(7) M_B_DQS#[0..7]

M_B_DQS#0
M_B_DQS#1
M_B_DQS#2
M_B_DQS#3
M_B_DQS#4
M_B_DQS#5
M_B_DQS#6
M_B_DQS#7

(7) M_A_DQS[0..7]

M_A_DQS0
M_A_DQS1
M_A_DQS2
M_A_DQS3
M_A_DQS4
M_A_DQS5
M_A_DQS6
M_A_DQS7

(7) M_A_DQS#[0..7]

M_A_DQS#0
M_A_DQS#1
M_A_DQS#2
M_A_DQS#3
M_A_DQS#4
M_A_DQS#5
M_A_DQS#6
M_A_DQS#7

+0.9V_DDR_VTT

C10 4.7U_6.3V_0603
C11 4.7U_6.3V_0603
C12 4.7U_6.3V_0603
C13 4.7U_6.3V_0603
C14 .22U_6.3V
C15 .22U_6.3V
C16 .22U_6.3V
C17 .22U_6.3V

+0.9V_DDR_VTT

C18 1000p_50V
C19 1000p_50V
C20 1000p_50V
C21 1000p_50V
C22 180P_50V
C23 180P_50V
C24 180P_50V
C25 180P_50V

QUANTA COMPUTER

Title	ATHLON64 DDRII MEMORY	
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ATHLON Control and Debug

LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

CPU_VDDA_RUN

33 ohm(3A)

CPU_VDDA_RUN — BLM18PG330SN1D_0603 (L3) — +2.5V_RUN

C26 4.7U_6.3V_0603 | C27 22U_6.3V | C28 3900p_25V | C29 100U_6.3V_3528

If AMD SI is not used, the SID pin can be left unconnected and SIC should have a 300-Ω (±5%) pulldown to VSS.

+1.8V_SUS — R7 *300_NC, R9 *300_NC, R10 300, R523 *0_NC, R524 *0_NC — (14) CPU_SIC, (14) CPU_SID — CPU_SIC_R, CPU_SID_R

for CPU rev.F , if for rev.G , populate R7,R9,R523,R524 and depopulate R10

(13) CPUCLK — C30 3900p_25V — CPU_CLKIN_SC_P / CPU_CLKIN_SC_N — R14 169/F_0603 — C31 3900p_25V — (13) CPUCLK#

R14 close U1 within 600 mil , C30 & C31 close U1 within 1250 mil

VLDT_RUN — R13 44.2/F, R12 44.2/F — place them to CPU within 1"

To Power — (37) COREFB+V, (37) COREFB-

(39) VDDIO_FB_H — R567 0 — C678 470P_50V

CPU_VDDA_RUN — U1D

VDDA2, VDDA1

CPU_HT_RESET# (T6), CPU_ALL_PWROK (T5), CPU_LDTSTOP# (T7) — RESET_L, PWROK, LDTSTOP_L

CPU_SIC_R, CPU_SID_R — SIC, SID

CPU_HTREF1, CPU_HTREF0 — HT_REF1, HT_REF0

T8 — VDD_FB_H, VDD_FB_L

T4 — VDDIO_FB_H, VDDIO_FB_L

CPU_CLKIN_SC_P, CPU_CLKIN_SC_N — CLKIN_H, CLKIN_L

CPU_DBRDY — DBRDY

CPU_TMS, CPU_TCK, CPU_TRST#, CPU_TDI — TMS, TCK, TRST_L, TDI

CPU_TEST25_H_BYPASSCLK_H, CPU_TEST25_L_BYPASSCLK_L, CPU_TEST19_PLLTEST0, CPU_TEST18_PLLTEST1 — TEST25_H, TEST25_L, TEST19, TEST18, TEST13, TEST9, TEST17, TEST16, TEST15, TEST14, TEST12

CPU_TEST17_BP3 (T13), CPU_TEST16_BPZ (T12)

(35) CPU_TEST5_THERMDC — C707 470P_50V — (35) CPU_TEST4_THERMDA — CPU_TEST5_THERMDC, CPU_TEST4_THERMDA

CPU_TEST07_ANALOG_T (T15), CPU_TEST6_DIECRACKMON (T16) — TEST7, TEST6, TEST5, TEST4, TEST3, TEST2

CPU_TEST3_GATE0 (T19), CPU_TEST2_DRAIN0 (T21)

CPU_RSVD_MA0_CLK3_P (T24), CPU_RSVD_MA0_CLK3_N (T23), CPU_RSVD_MA0_CLK0_P (T26), CPU_RSVD_MA0_CLK0_N (T28) — RSVD0, RSVD1, RSVD2, RSVD3

CPU_RSVD_MB0_CLK3_P (T34), CPU_RSVD_MB0_CLK3_N (T36), CPU_RSVD_MB0_CLK0_P (T35), CPU_RSVD_MB0_CLK0_N (T37) — RSVD4, RSVD5, RSVD6, RSVD7

MISC

RSVD8, RSVD9 — CPU_MA_RESET# (T25), CPU_MB_RESET# (T27)

RSVD10, RSVD11 — CPU_RSVD_VIDSTRB1 (T30), CPU_RSVD_VIDSTRB0 (T29)

RSVD12, RSVD13, RSVD14 — CPU_RSVD_VDDNB_FB_P (T31), CPU_RSVD_VDDNB_FB_N (T32), CPU_RSVD_CORE_TYPE (T33)

RSVD15, RSVD16, RSVD17, RSVD18, RSVD19, RSVD20

AMD NPT S1 SOCKET
Processor Socket

+1.8V_SUS — R551 300, R8 300 — H_THERMTRIP# (35)

THERMTRIP_L, PROCHOT_L — H_THERMTRIP#, H_PROCHOT#

VID5, VID4, VID3, VID2, VID1, VID0 (37)

CPU_PRESENT_L — CPU_PRESENT#

PSI_L — PSI# (37) — T11

PSI_L is a Power Status Indicator signal. This signal is asserted when the processor is in a low powerstate. PSI_L should be connected to the power supply controller, if the controller supports "skipmode, or diode emulation mode". PSI_L is asserted by the processor during the C3 and S1 states.

DBREQ_L — CPU_DBREQ#

TDO — CPU_TDO

TEST29_H, TEST29_L — CPU_TEST29_H_FBCLKOUT_P, CPU_TEST29_L_FBCLKOUT_N — R16 80.6/F

ROUTE AS 80 Ohm DIFFERENTIAL PAIR PLACE IT CLOSE TO CPU WITHIN 1"

TEST24, TEST23, TEST22, TEST21, TEST20 — CPU_TEST23_TSTUPD (T14), CPU_TEST21_SCANEN

TEST28_H, TEST28_L — CPU_TEST28_H_PLLCHRZ_P (T18), CPU_TEST28_L_PLLCHRZ_N (T17)

TEST27, TEST26, TEST10, TEST8 — CPU_TEST26_BURNIN#, CPU_TEST10_ANALOGOUT (T20), CPU_TEST08_DIG_T (T22)

(14) CPU_PWRGD — R19 0 — CPU_ALL_PWROK — R525 10K

(11,14) LDT_STOP# — R20 0 — CPU_LDTSTOP# — R526 10K

(14) LDT_RST# — R527 0 — CPU_HT_RESET# — R528 10K

R527 can be used for EMI verifing, place close to CPU

+1.8V_RUN — R24 10K — Q2 MMBT3904

+1.8V_SUS — R27 300

H_PROCHOT# — CPU_EC_PROCHOT# (27), CPU_PROCHOT# (15)

*MMBT3904_NC Q49

SB this pin is 3.3V,need it level-shift.

CPU_TEST26_BURNIN# R22 300
CPU_PRESENT# R25 1K/F
CPU_TEST25_H_BYPASSCLK_H R26 510/F

CPU_TEST21_SCANEN R32 300
CPU_TEST25_L_BYPASSCLK_L R44 510/F
CPU_TEST19_PLLTEST0 R45 300
CPU_TEST18_PLLTEST1 R46 300

+1.8V_SUS

If no use which Net need pull-up or down

HDT connector is added for debug convenience.

HDT CONNECTOR

JHDT1

GND, Resreved, Resreved, DBREQ_L, DBRDY, TCK, TMS, TDI, TRST_L, TDO, VDDIO, VDDIO, RESET_L, GND

CPU_DBREQ#, CPU_DBRDY, CPU_TCK, CPU_TMS, CPU_TDI, CPU_TRST#, CPU_TDO

+1.8V_SUS

*HDT conn_NC

+3.3V_SUS — R580 *10K_NC

+1.8V_SUS — R581 *10K_NC

Q55 *MMBT3904_NC

CPU_RESET# — CPU_HT_RESET#

QUANTA COMPUTER

Title	ATHLON64 CTRL & DEBUG	
Size	Document Number FX2	Rev 2B
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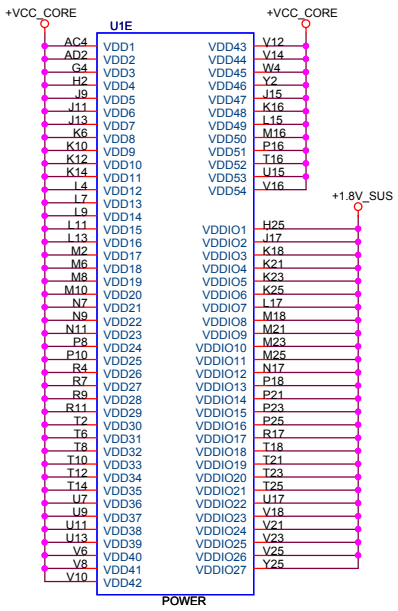
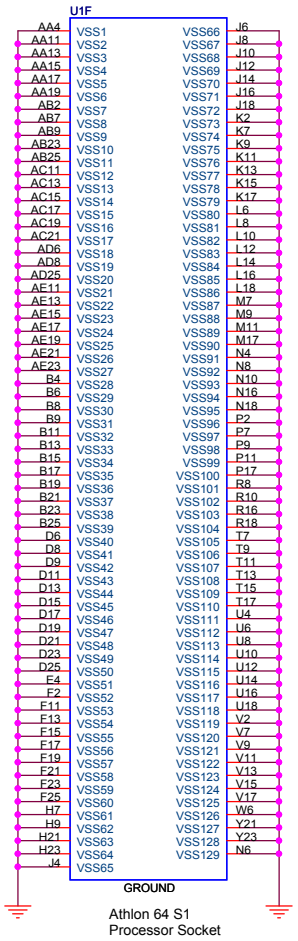
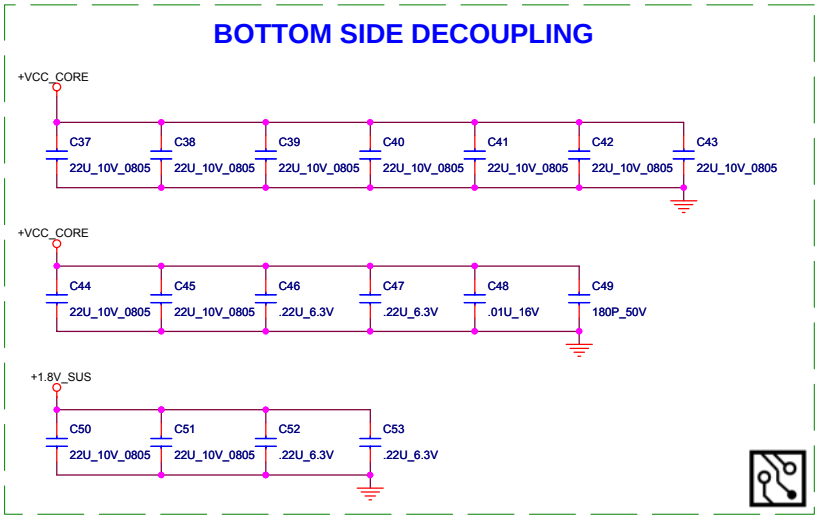
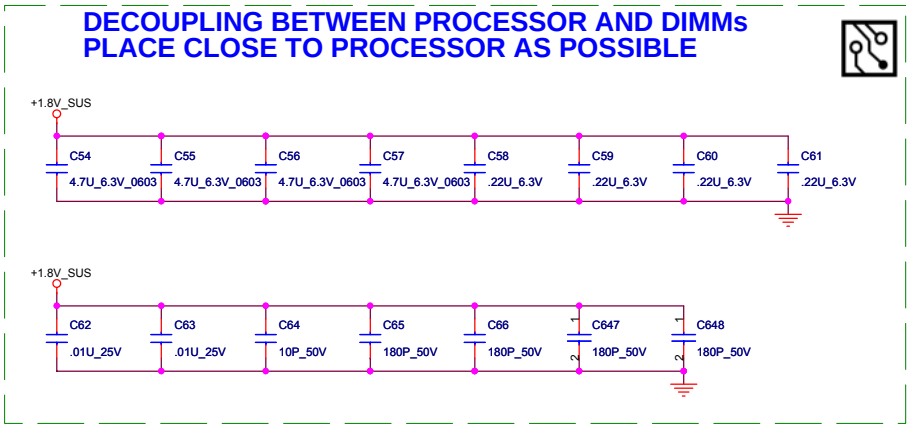
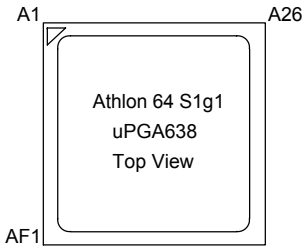






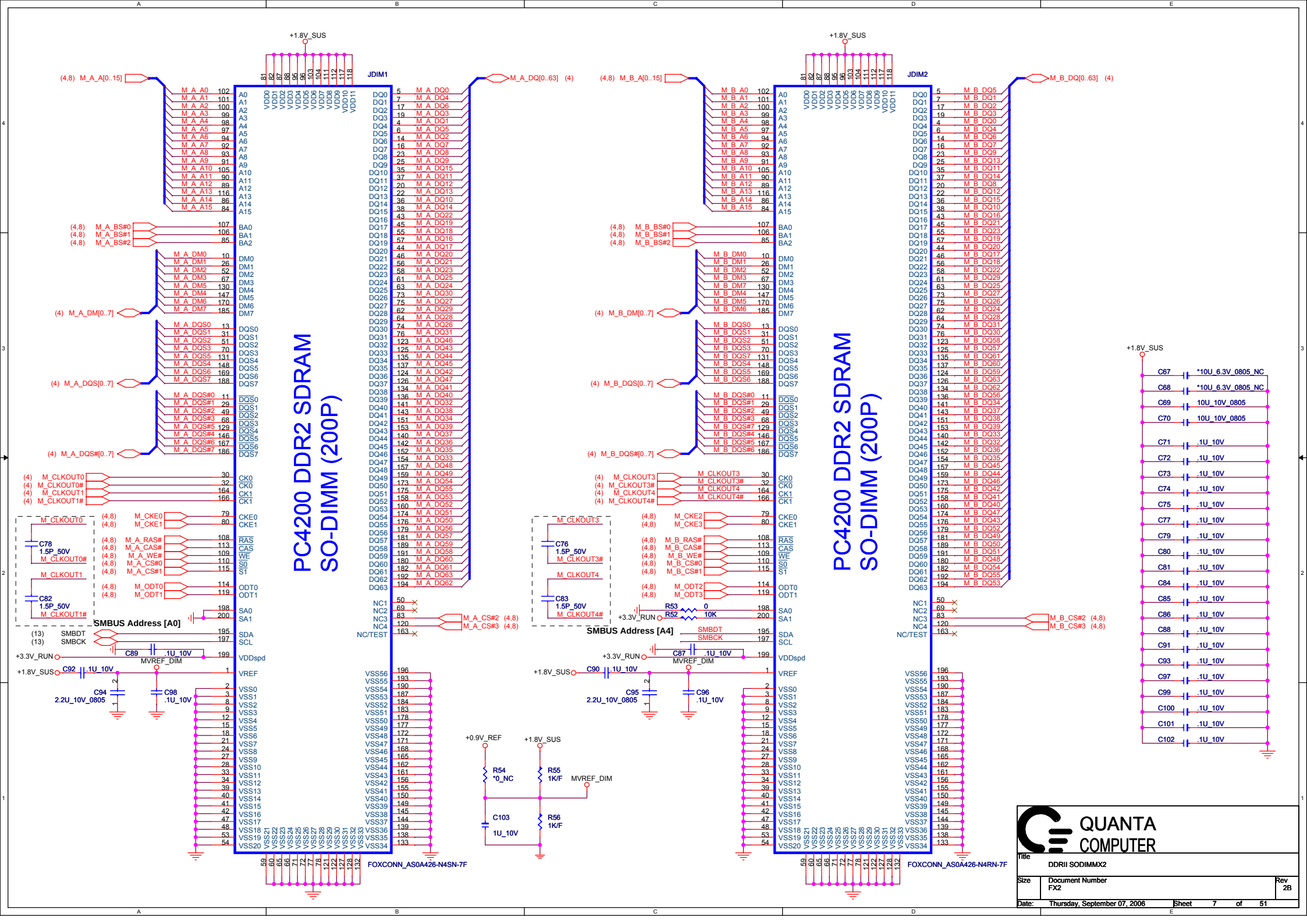




PROCESSOR POWER AND GROUND

QUANTA COMPUTER

Title	ATHLON64 PWR & GND	
Size	Document Number FX2	Rev 2B
Date: Thursday, September 07, 2006	Sheet 6 of 51	


JDIM1
JDIM2
PC4200 DDR2 SDRAM SO-DIMM (200P)
FOXCONN_AS0A426-N4SN-7F
FOXCONN_AS0A426-N4RN-7F
SMBUS Address [A0]
SMBUS Address [A4]
+1.8V_SUS
+3.3V_RUN
+0.9V_REF
MVREF_DIM
QUANTA COMPUTER
Title
DDRII SODIMMX2
Size
Document Number
FX2
Rev
2B
Date:
Thursday, September 07, 2006
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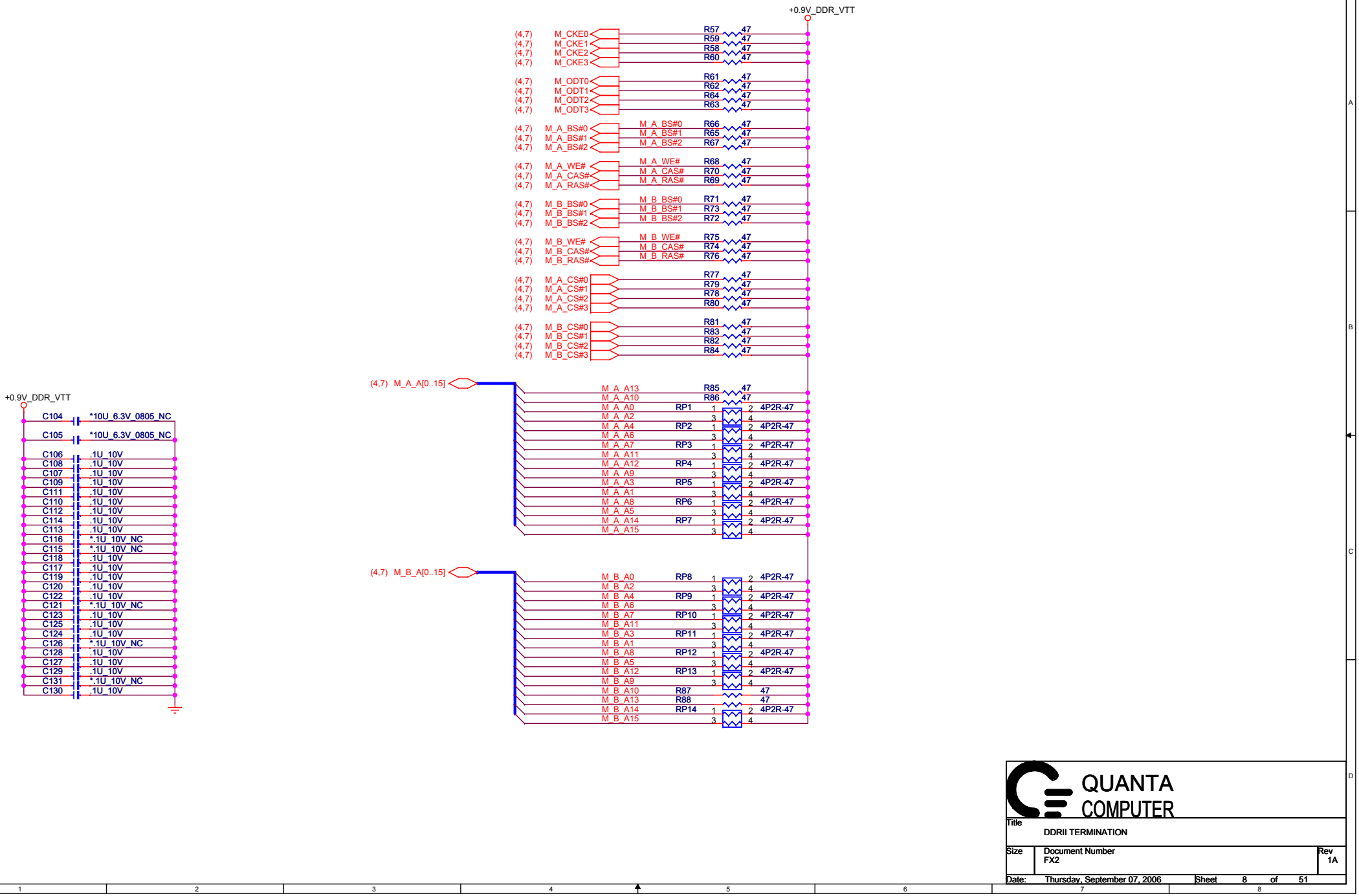
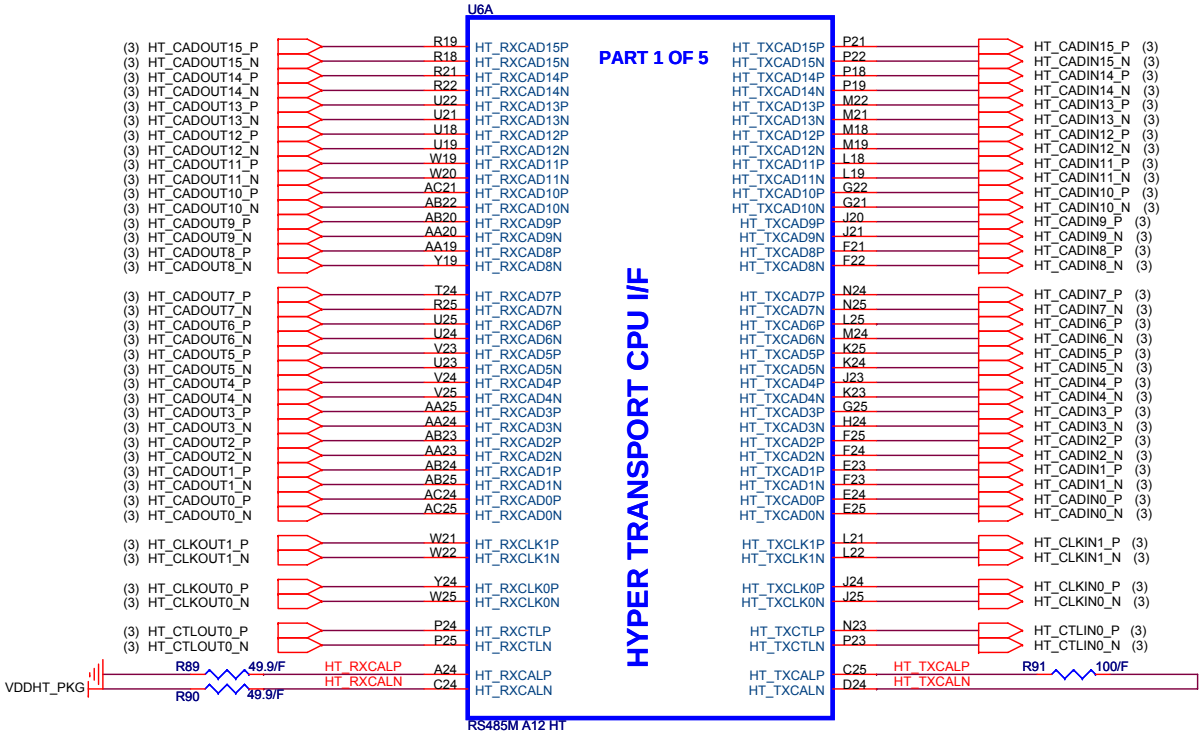
51



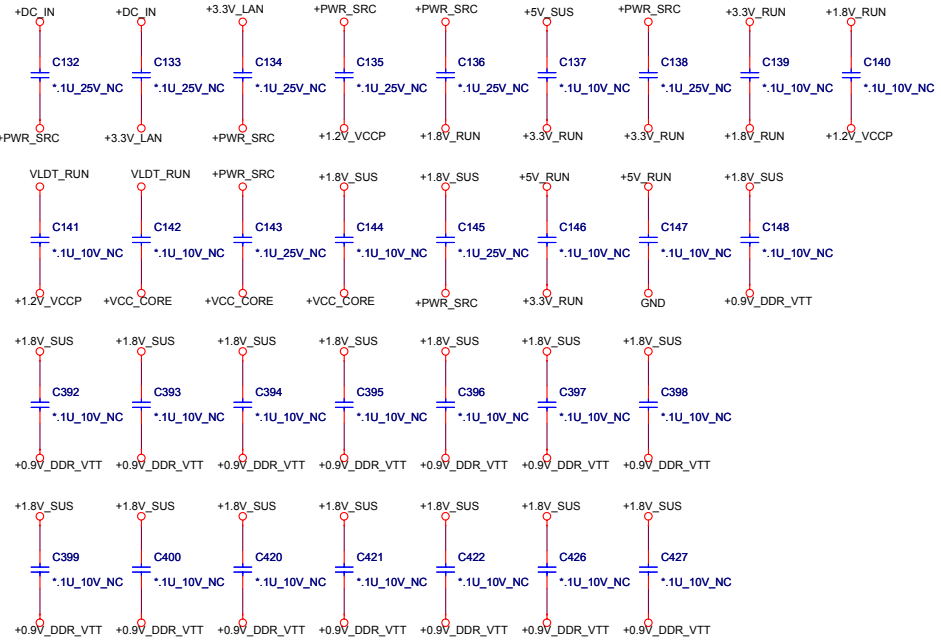
QUANTA COMPUTER

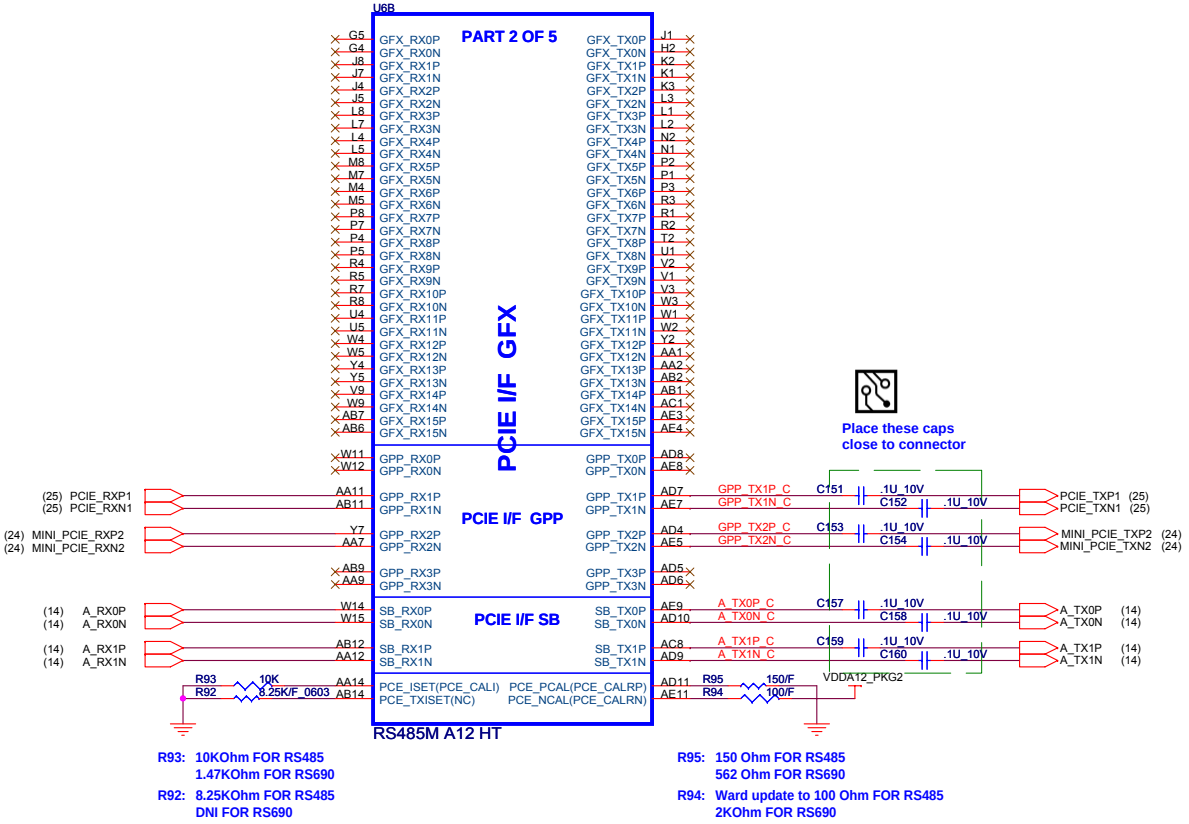
Title	DDRII TERMINATION	
Size	Document Number FX2	Rev 1A
Date: Thursday, September 07, 2006	Sheet 8 of 51	



QUANTA COMPUTER

Title	RS485-HT LINK0 I/F	
Size	Document Number FX2	Rev 1A
Date: Thursday, September 07, 2006	Sheet 9 of 51	





R93: 10KOhm FOR RS485
1.47KOhm FOR RS690

R92: 8.25KOhm FOR RS485
DNI FOR RS690

R95: 150 Ohm FOR RS485
562 Ohm FOR RS690

R94: Ward update to 100 Ohm FOR RS485
2KOhm FOR RS690

QUANTA COMPUTER

Title	RS485-PCIE LINK I/F	
Size	Document Number FX2	Rev 1A
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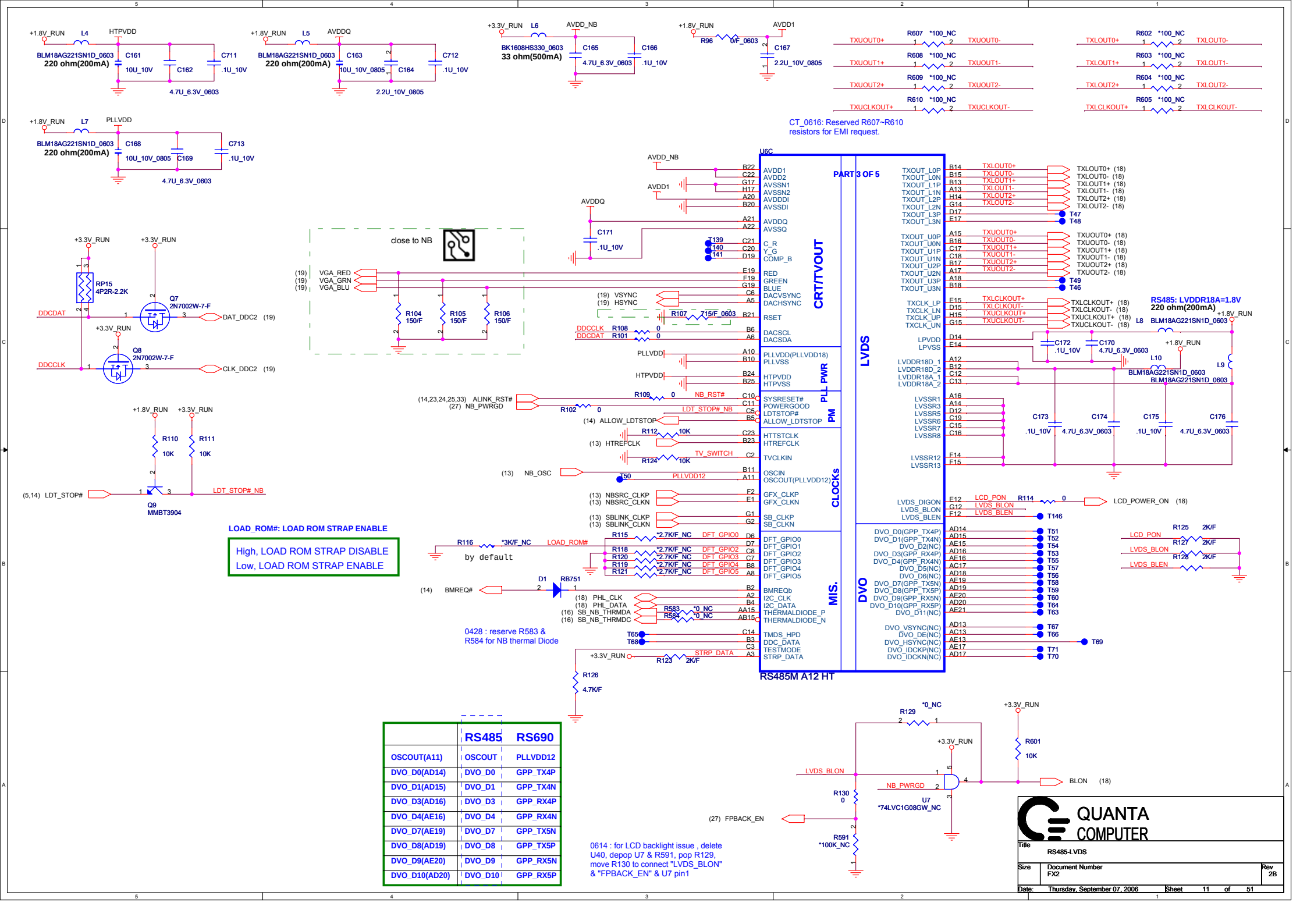
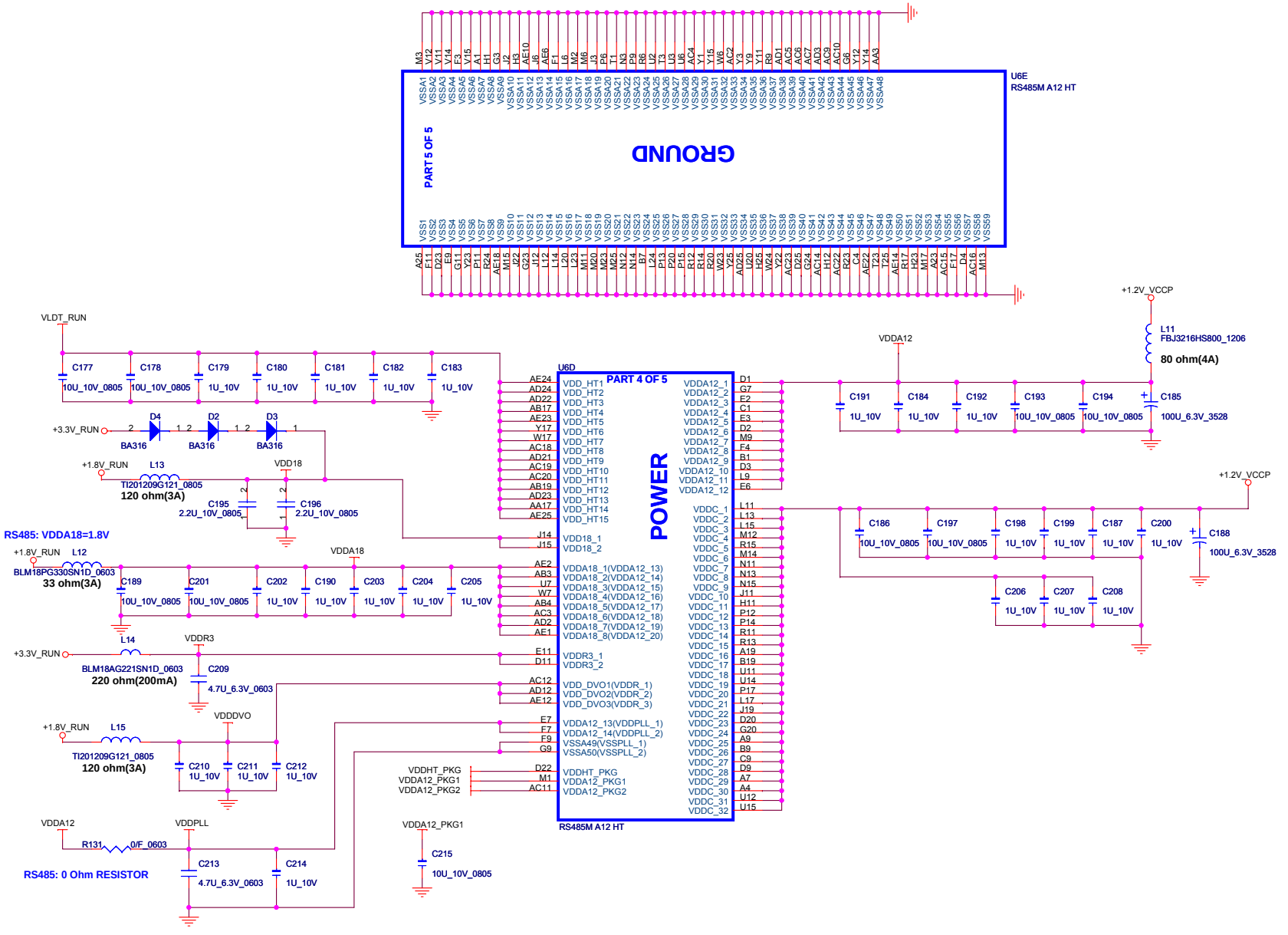


	RS485	RS690
OSCOUT(A11)	OSCOUT	PLLVDD12
DVO_D0(AD14)	DVO_D0	GPP_TX4P
DVO_D1(AD15)	DVO_D1	GPP_TX4N
DVO_D3(AD16)	DVO_D3	GPP_RX4P
DVO_D4(AE16)	DVO_D4	GPP_RX4N
DVO_D7(AE19)	DVO_D7	GPP_TX5N
DVO_D8(AD19)	DVO_D8	GPP_TX5P
DVO_D9(AE20)	DVO_D9	GPP_RX5N
DVO_D10(AD20)	DVO_D10	GPP_RX5P

QUANTA COMPUTER

Title	RS485-LVDS	
Size	Document Number FX2	Rev 2B
Date: Thursday, September 07, 2006	Sheet 11 of 51	

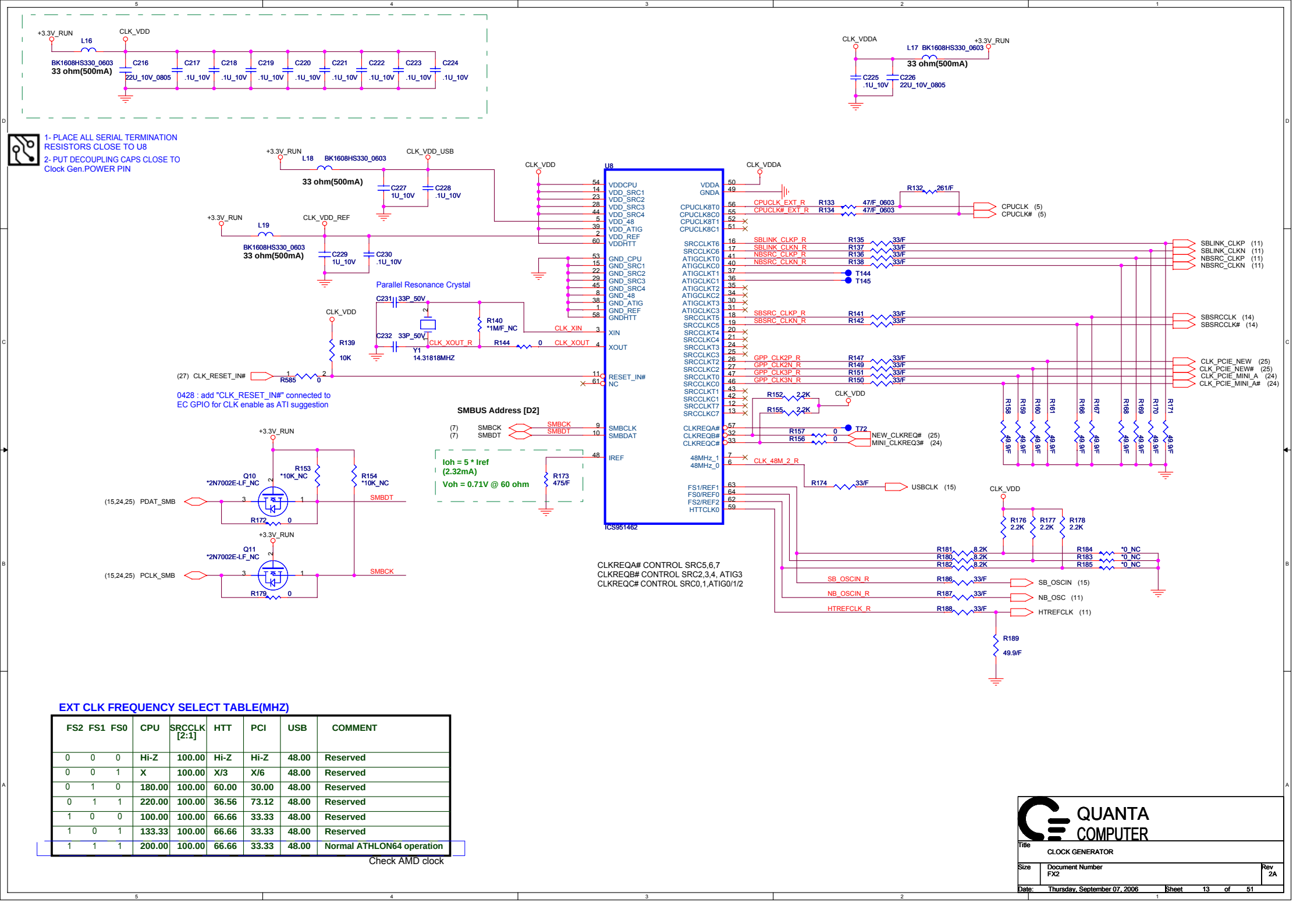


NB RS485 POWER STATES

Power Signal	S0	S1	S3	S4/S5	G3
VDDHT	ON	ON	OFF	OFF	OFF
VDDR	ON	ON	OFF	OFF	OFF
VDD18	ON	ON	OFF	OFF	OFF
VDDC	ON	ON	OFF	OFF	OFF
VDDA18	ON	ON	OFF	OFF	OFF
VDDA12	ON	ON	OFF	OFF	OFF
AVDD	ON	ON	OFF	OFF	OFF
AVDDDI	ON	ON	OFF	OFF	OFF
PLLVDD	ON	ON	OFF	OFF	OFF
HTPVDD	ON	ON	OFF	OFF	OFF
VDDR3	ON	ON	OFF	OFF	OFF
LPVDD	ON	ON	OFF	OFF	OFF
LVDDR18D	ON	ON	OFF	OFF	OFF
LVDDR18A	ON	ON	OFF	OFF	OFF

QUANTA COMPUTER

Title	RS485-POWER	
Size	Document Number FX2	Rev 2B
Date: Thursday, September 07, 2006	Sheet 12 of 51	



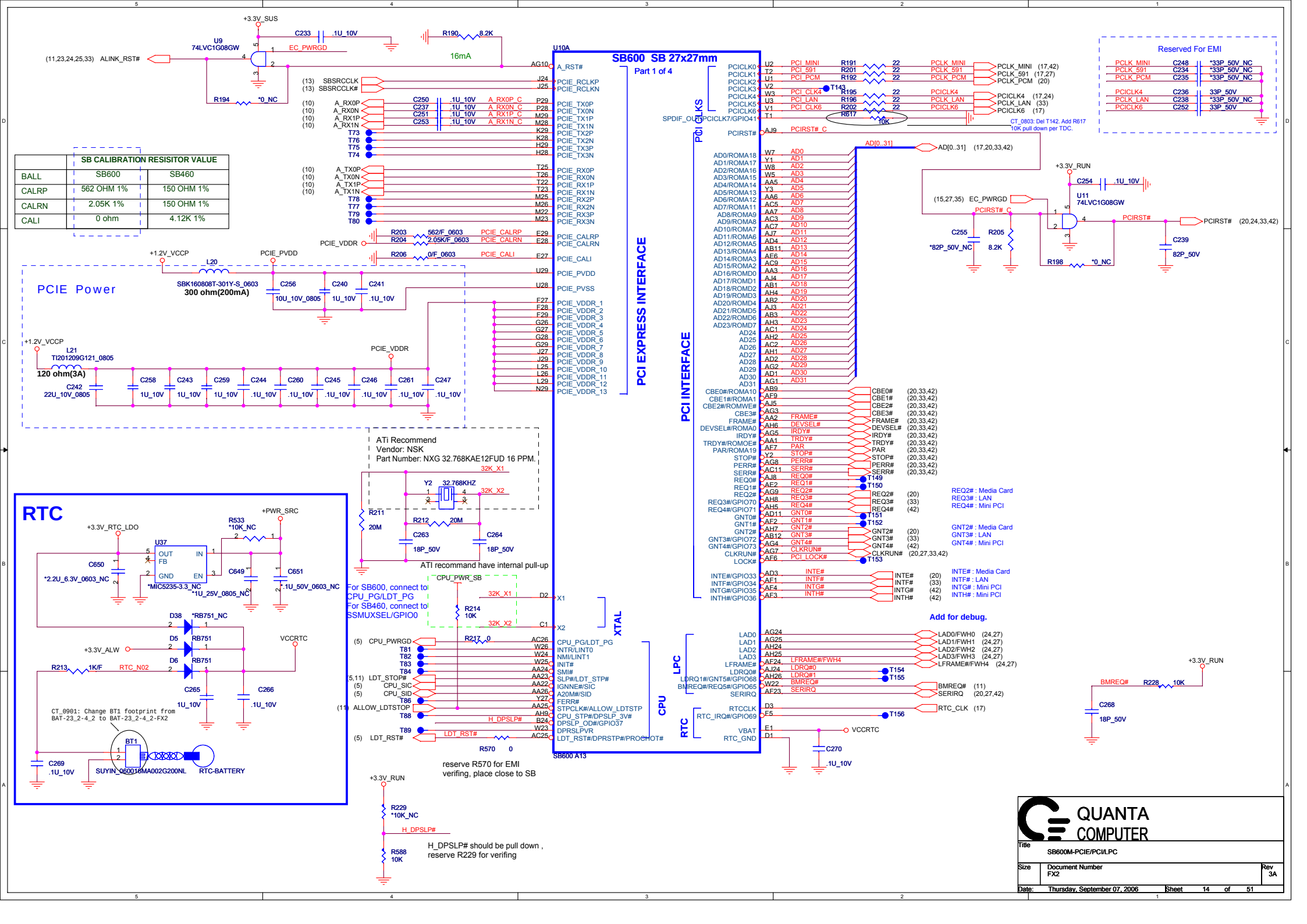
EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

Check AMD clock

QUANTA COMPUTER

Title	CLOCK GENERATOR	
Size	Document Number FX2	Rev 2A
Date: Thursday, September 07, 2006	Sheet 13 of 51	


SB600 SB 27x27mm
Part 1 of 4
PCI EXPRESS INTERFACE
PCI INTERFACE
PCI CLKS
LPC
CPU
RTC
XTAL
SB600 A13
PCIE Power
RTC
SB CALIBRATION RESISITOR VALUE
BALL | SB600 | SB460
CALRP | 562 OHM 1% | 150 OHM 1%
CALRN | 2.05K 1% | 150 OHM 1%
CALI | 0 ohm | 4.12K 1%
ATi Recommend
Vendor: NSK
Part Number: NXG 32.768KAE12FUD 16 PPM.
ATi recommand have internal pull-up
reserve R570 for EMI
verifing, place close to SB
H_DPSLP# should be pull down ,
reserve R229 for verifing
Reserved For EMI
Add for debug.
QUANTA COMPUTER
Title
SB600M-PCIE/PCI/LPC
Size
Document Number
FX2
Rev
3A
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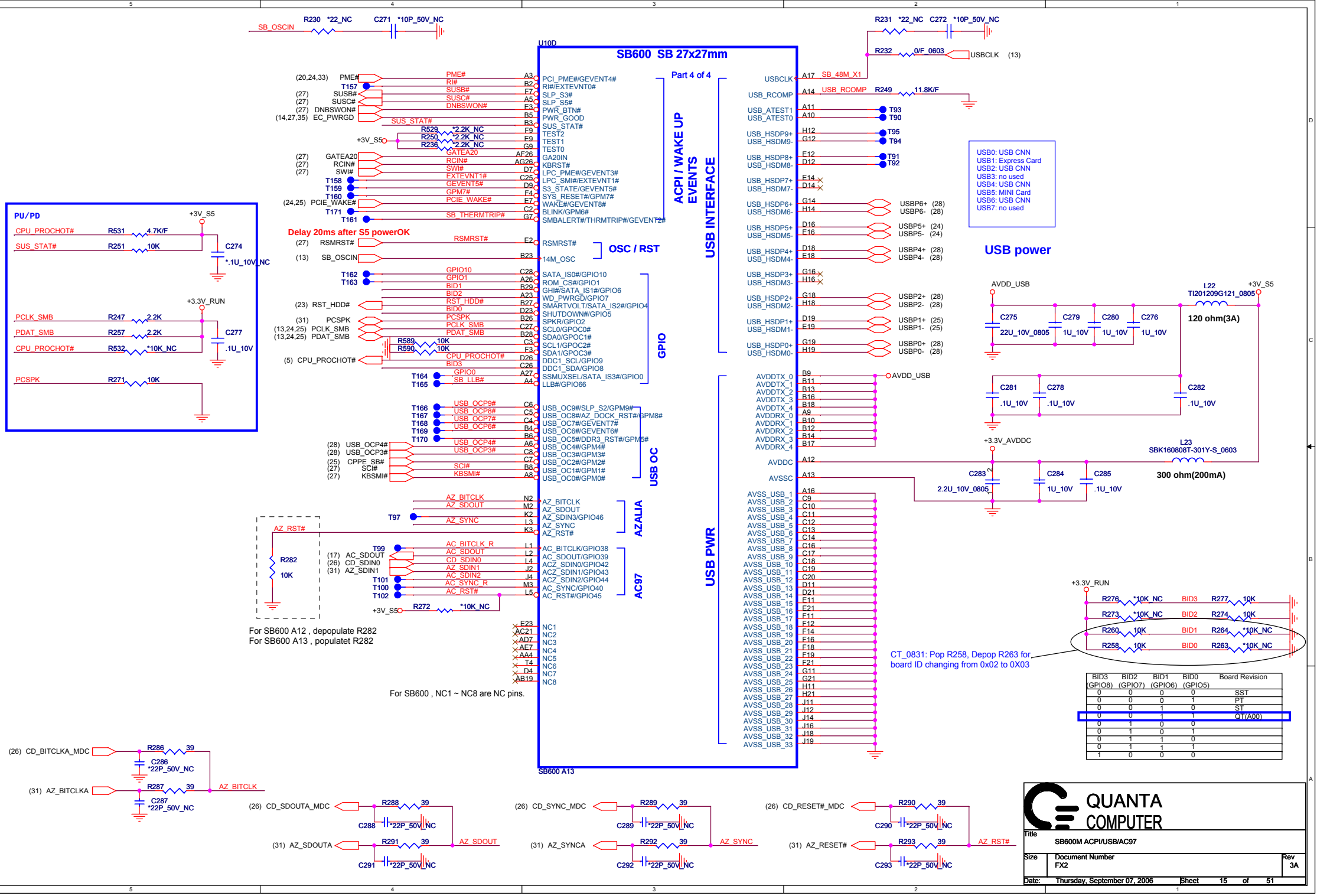
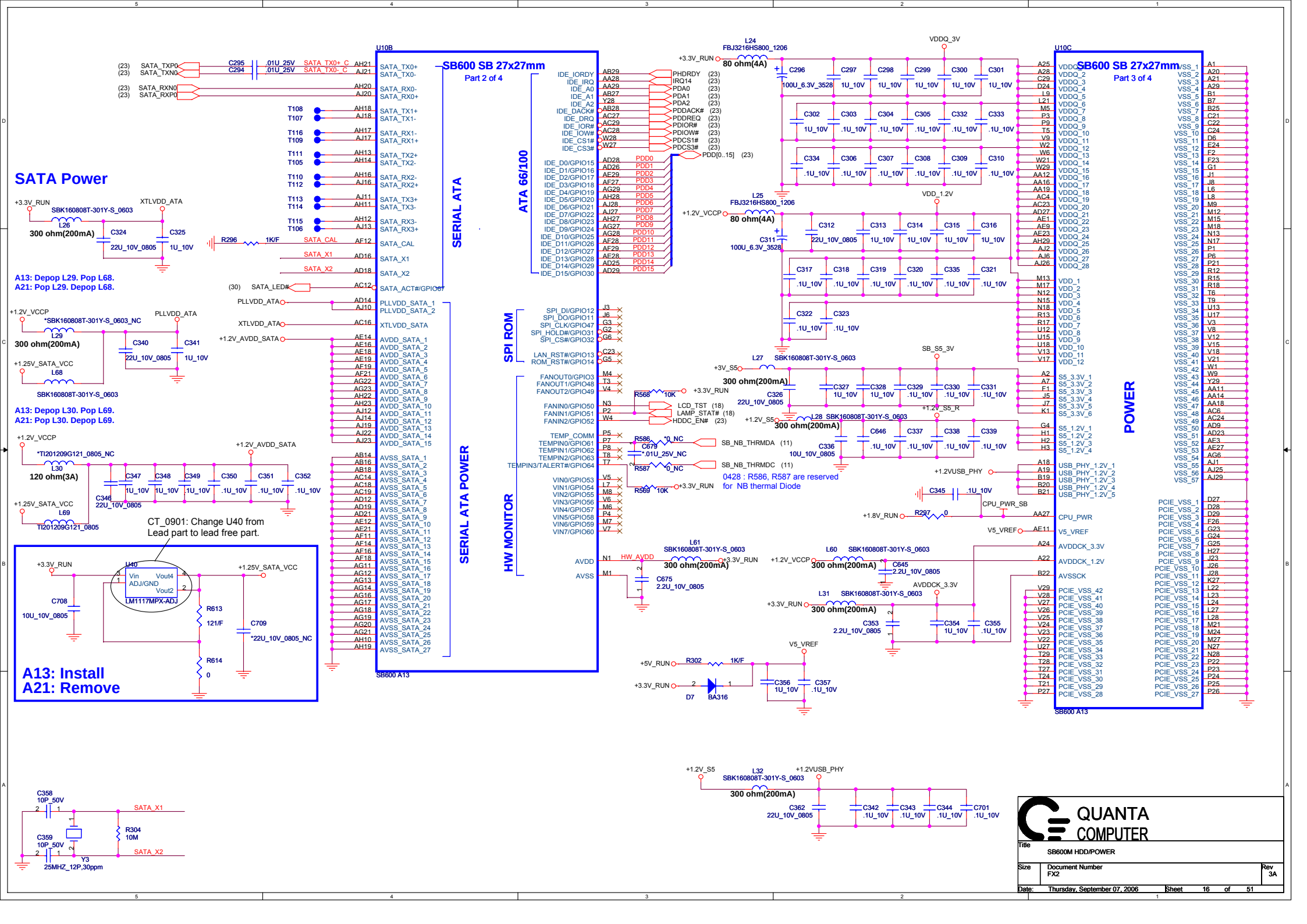

SB600 SB 27x27mm
U10D
Part 4 of 4
SB600 A13
ACPI / WAKE UP EVENTS
USB INTERFACE
GPIO
OSC / RST
AZALIA
AC97
USB OC
USB PWR
PU/PD
Delay 20ms after S5 powerOK
USB power
USB0: USB CNN
USB1: Express Card
USB2: USB CNN
USB3: no used
USB4: USB CNN
USB5: MINI Card
USB6: USB CNN
USB7: no used
For SB600 A12 , depopulate R282
For SB600 A13 , populatet R282
For SB600 , NC1 ~ NC8 are NC pins.
CT_0831: Pop R258, Depop R263 for board ID changing from 0x02 to 0X03
BID3 (GPIO8) BID2 (GPIO7) BID1 (GPIO6) BID0 (GPIO5) Board Revision
0 0 0 0 SST
0 0 0 1 PT
0 0 1 0 ST
0 0 1 1 QT(A00)
0 1 0 0
0 1 0 1
0 1 1 0
0 1 1 1
1 0 0 0
QUANTA COMPUTER
Title SB600M ACPI/USB/AC97
Size Document Number FX2 Rev 3A
Date: Thursday, September 07, 2006 Sheet 15 of 51


SATA Power
SB600 SB 27x27mm
Part 2 of 4
SB600 SB 27x27mm
Part 3 of 4
SERIAL ATA
ATA 66/100
SPI ROM
HW MONITOR
SERIAL ATA POWER
POWER
A13: Depop L29. Pop L68.
A21: Pop L29. Depop L68.
A13: Depop L30. Pop L69.
A21: Pop L30. Depop L69.
CT_0901: Change U40 from Lead part to lead free part.
A13: Install
A21: Remove
0428 : R586, R587 are reserved for NB thermal Diode
SB600 A13
QUANTA COMPUTER
SB600M HDD/POWER
Document Number FX2
Rev 3A
Thursday, September 07, 2006
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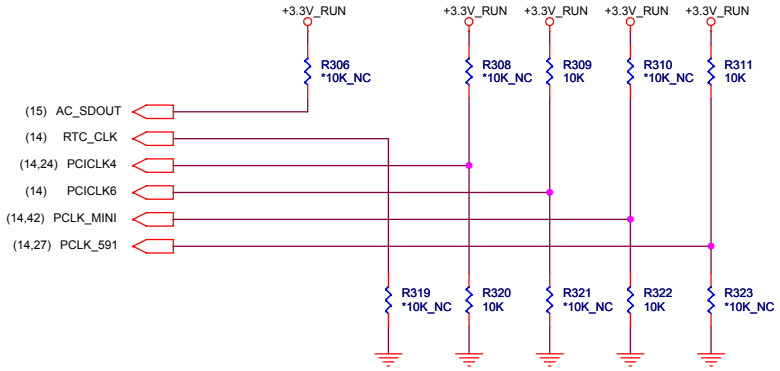
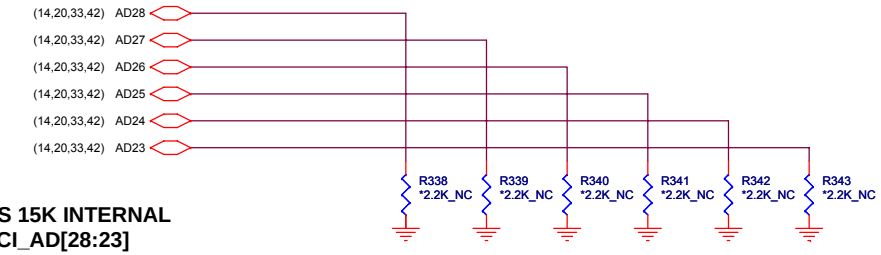


SB600 has 15K internal PD for AC_SDOUT

15K internal PU for RTC_CLK ,External PU/PD is not required.

REQUIRED STRAPS

	AC_SDOUT	RTC_CLK	PCI_CLK4	PCI_CLK6	PCLK_MINI PCLK_591 PCI_CLK0 PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48 DEFAULT	CPU IF=K8 DEFAULT	H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM DEFAULT L, L = FWH ROM
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ	CPU IF=P4	



SB600 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

DEBUG STRAPS

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	Use Long Reset DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	boot fail time disabled DEFAULT
PULL LOW	Use Short Reset	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	boot fail time enabled
	SB600 Only					SB600 Only

QUANTA COMPUTER

Title	SB600M STRAPS	
Size	Document Number FX2	Rev 2A
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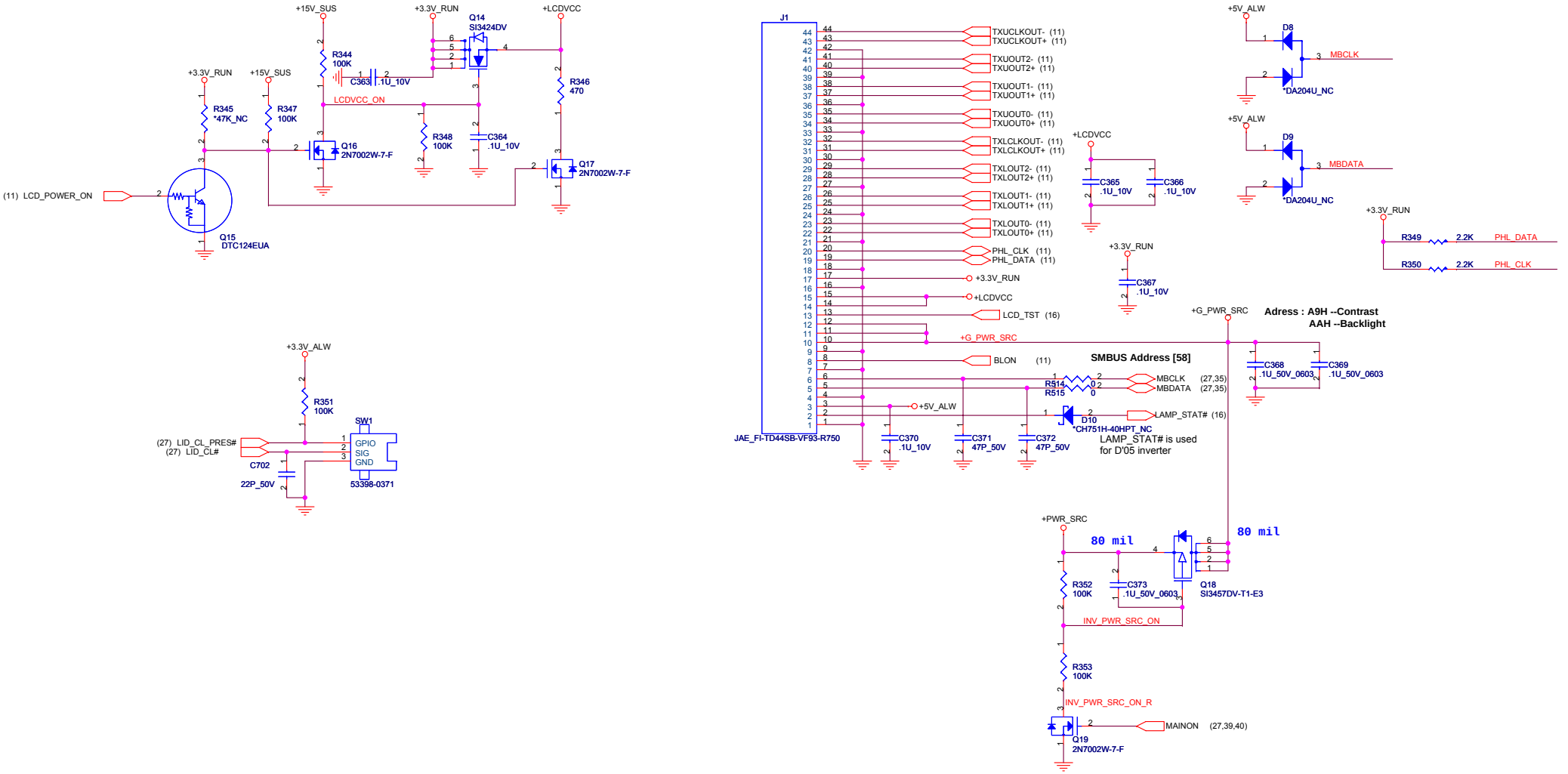

QUANTA COMPUTER

Title	LCD CONN	
Size	Document Number FX2	Rev 2A
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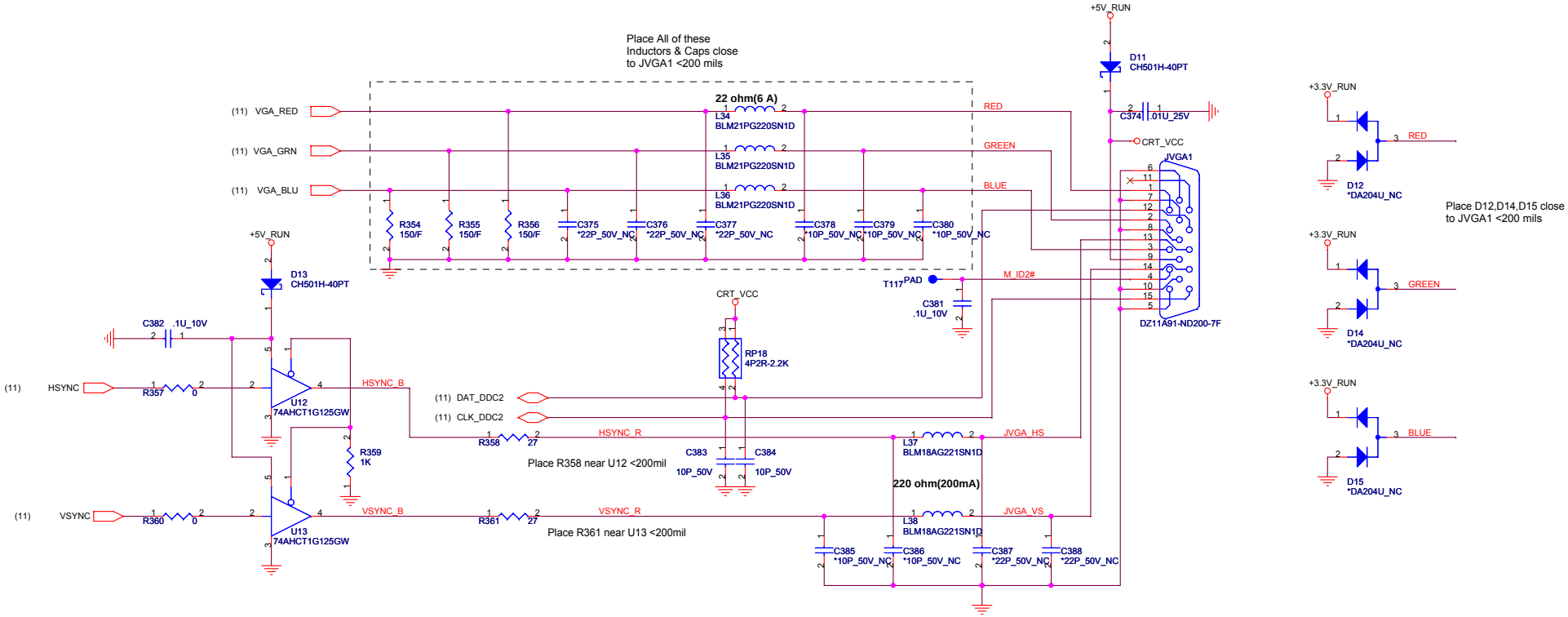
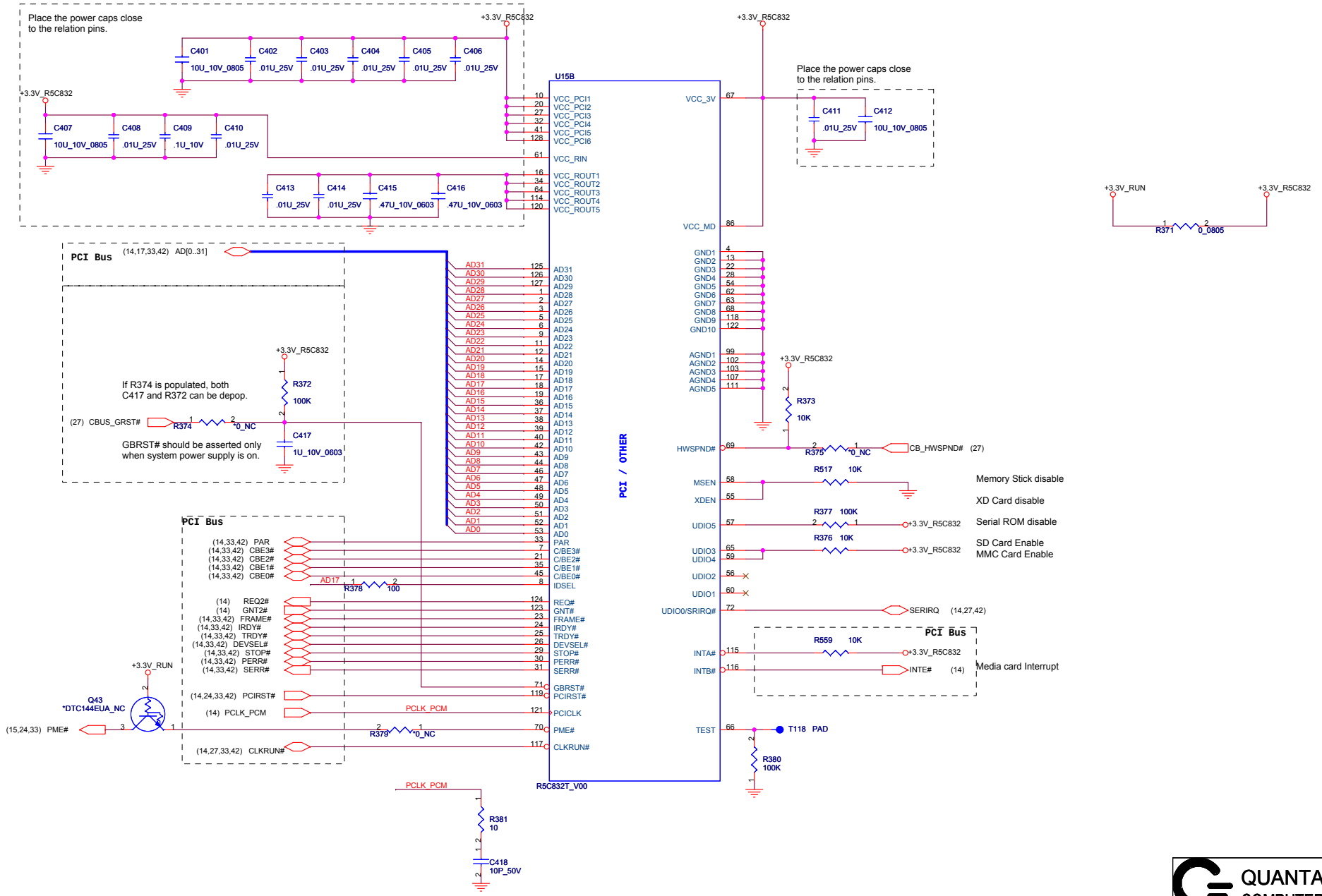


QUANTA COMPUTER

Title	CRT	
Size	Document Number FX2	Rev 2B
Date: Thursday, September 07, 2006	Sheet 19 of 51	



Title	5C832/PCI		
Size	Document Number FX2		Rev 2A
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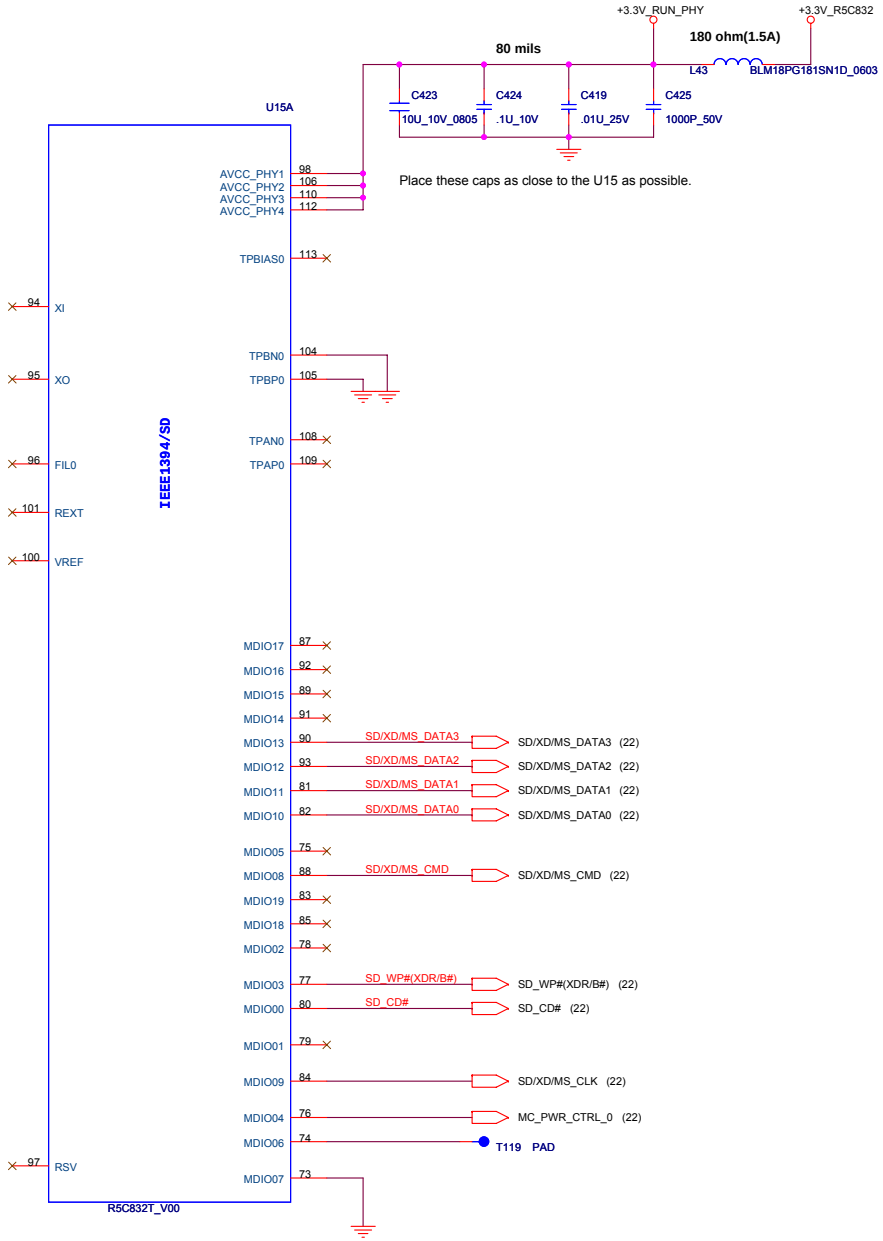

QUANTA COMPUTER

Title	CARD READER	
Size	Document Number FX2	Rev 1A
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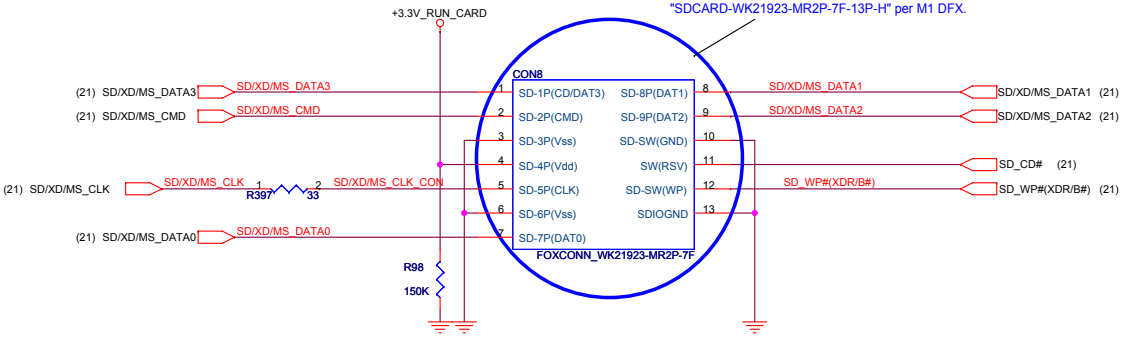
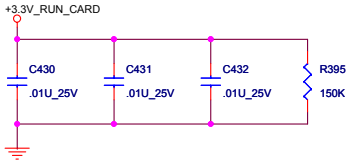
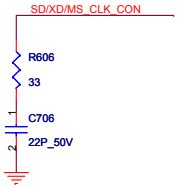
DO NOT INSERT SD/MMC SIMULTANEOUSLY.

CT_0831: Change footprint from
"SDCARD-WK21923-MR2P-7F-13P-V" to
"SDCARD-WK21923-MR2P-7F-13P-H" per M1 DFX.

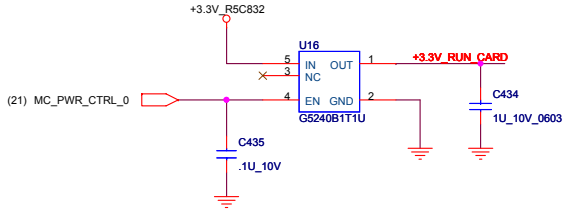






3 IN 1 CARD READER

For SD/MS power



QUANTA COMPUTER

Title	CARD READER CONN	
Size	Document Number FX2	Rev 3A
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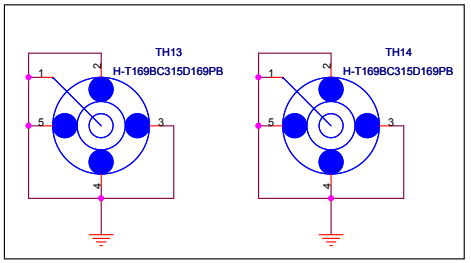
SATA HDD



Place C436, C437 close to connector side

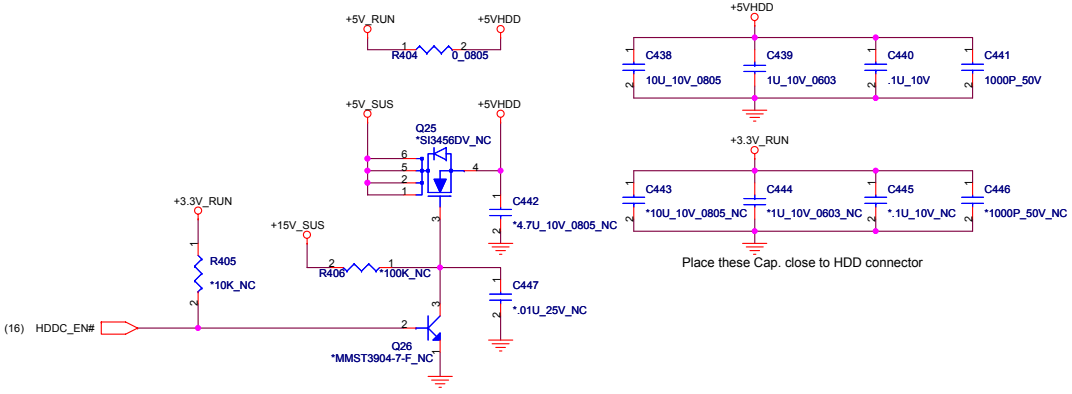
SATA_RX0-_C C436 .01U_25V SATA_RXN0 (16)

SATA_RX0+_C C437 .01U_25V SATA_RXP0 (16)

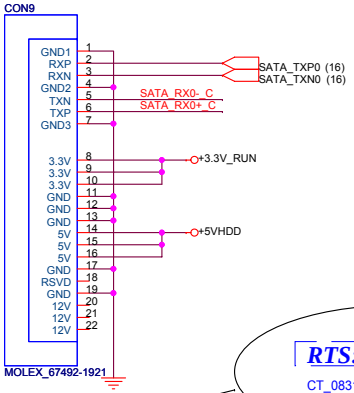
Locate caps C436, C437 near HDD Conn.
Length match SATA_C_RX0- & SATA_C_RX0+ within 20mils.

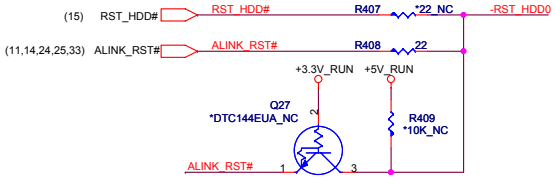
SATA drive vendors will use only 5V supply from the system and will derive 3.3V on the drive. If drive power goals are not achieved, drive vendors will use both 5V and 3.3V supplies from the system. Initial power saving using 3.3V from system is less than 5%.

Power Estimate:
SATA drive power consumption estimate at MobileMark is 1.1W. An additional 150mW can be saved using Intel's IMST driver.

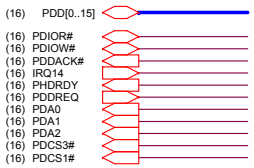


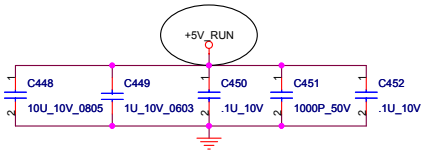
Place these Cap. close to HDD connector





PATA ODD

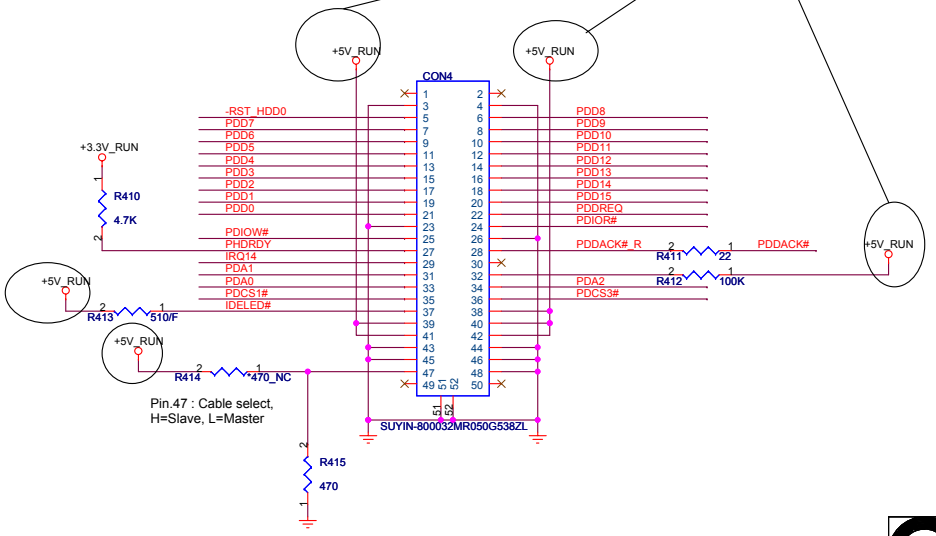




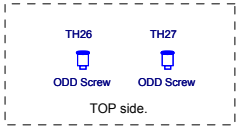
Place these Cap. close to MOD connector

RTS: Remove L66.

CT_0831: Removed L66 for RTS.



Pin.47 : Cable select,
H=Slave, L=Master



QUANTA COMPUTER

Title	SATA HDD & PATA ODD	
Size	Document Number FX2	Rev 3A
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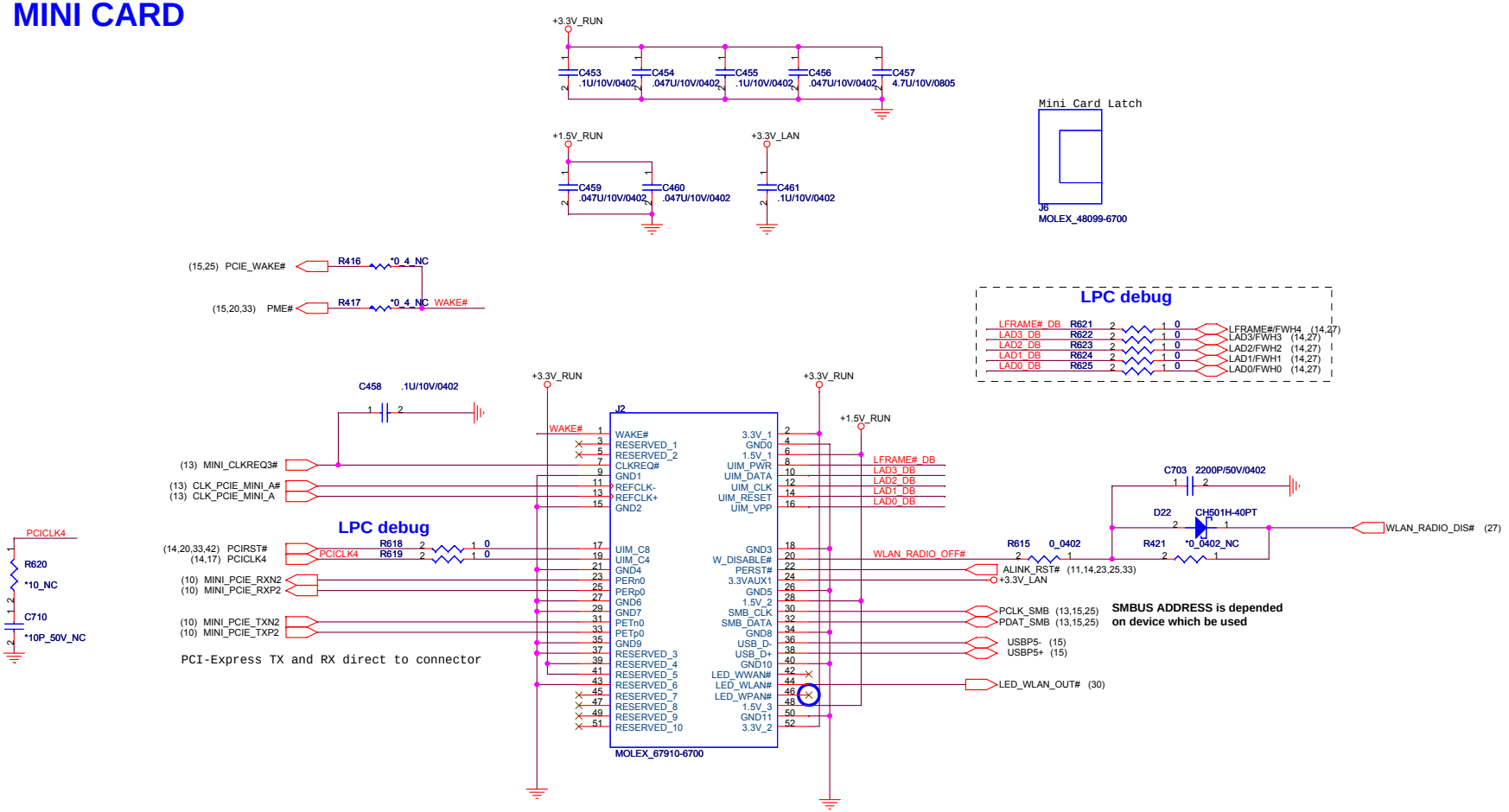
MINI CARD



Title	MINI Card		
Size	Document Number FX2		Rev 2B
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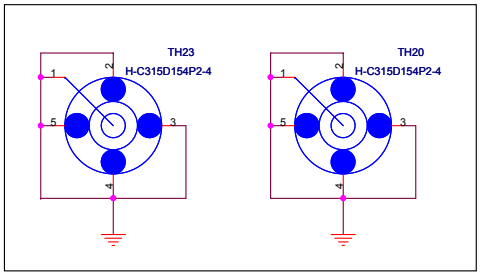
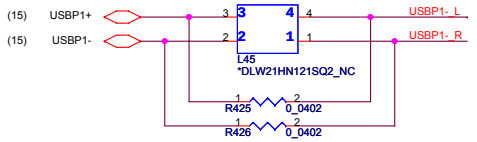
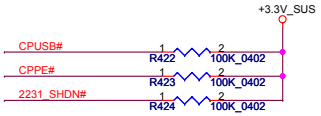
QUANTA COMPUTER

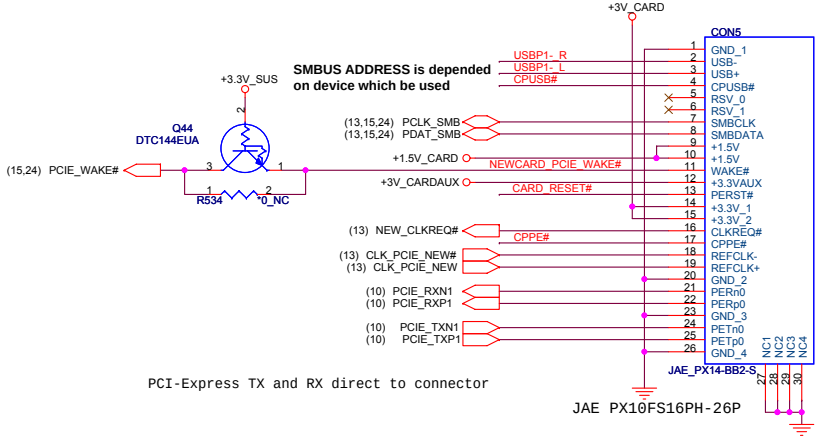
Express Card



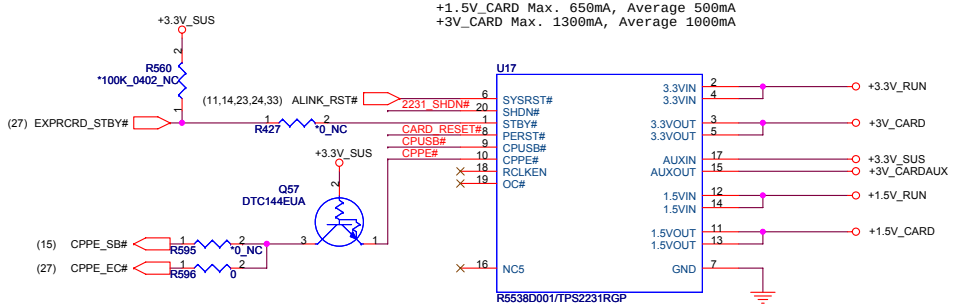
NEW CARD GUIDE POST
TOP side.





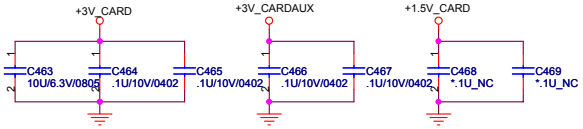


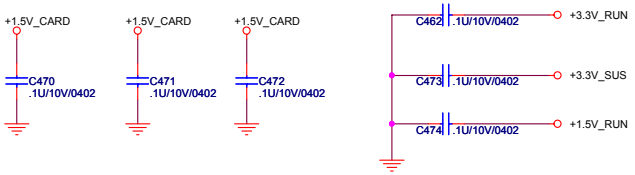
+1.5V_CARD Max. 650mA, Average 500mA
+3V_CARD Max. 1300mA, Average 1000mA



CPPE# be acknowledged by	R595	R596
South Bridge	Pop	NC
EC(KBC)	NC	Pop

+1.5V_CARD Max. 650mA, Average 500mA
+3V_CARD Max. 1300mA, Average 1000mA





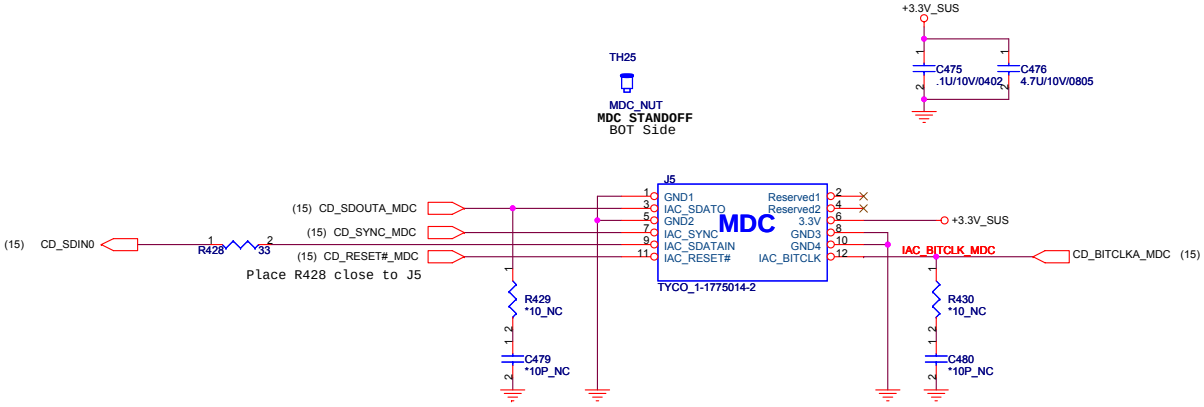
QUANTA COMPUTER

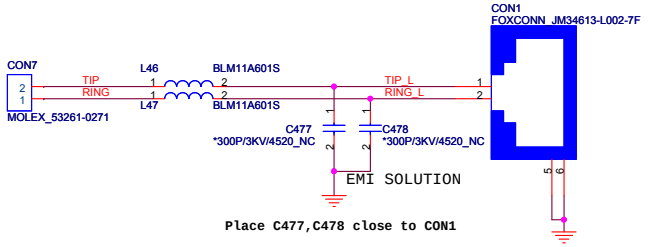
Title	Express Card	
Size	Document Number FX2	Rev 2B
Date: Thursday, September 07, 2006	Sheet 25 of 51	

MDC INTERFACE

MDC Layout Notes

1. Tip and Ring trace width = 25 mils
2. Spacing between Tip and Ring = 25 mils
3. Tip and Ring connector pitch = 25 mils
4. Keep out area from Tip and Ring to other signals = 100 mils
5. Power and Ground minimum trace width to connector = 20 mils
6. Route Tip and Ring on one layer only (top or bottom)
7. Modem internal cable wire size = 26 AWG
(stranded or twisted pair wire)





QUANTA COMPUTER

Title	MDC CONN	
Size	Document Number FX2	Rev 1A
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EC pin updated as "FX2 KBC GPIO define v14"

I/O Address		
BADDR1-0	Index	Data
0 0	2E	2F
0 1	4E	4F
1 0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
1 1	Reserved	

add R468 for +3.3_SRC & R516 connected to +3.3V_ALW as power concern about the leakage; create +3.3V_97551.

SHBM=1: Enable shared memory with host BIOS

0502 : add C680 as Loki's suggestion

CT_0727: Change C704 from 22P to 1000P.

PBAT_SMBCLK/DAT : Charger, Battery
MBCLK/DATA : LCD, Password, CPU internal thermal diode

Block 1 SMBUS Address [A0]

Block 2 SMBUS Address [A2]

DIRECTLY *50 mS*

HWPG_591 ===> NB_PWRGD ===> EC_PWRGD

NORTH BRIDGE SOUTH BRIDGE

EC & FALSH ROM

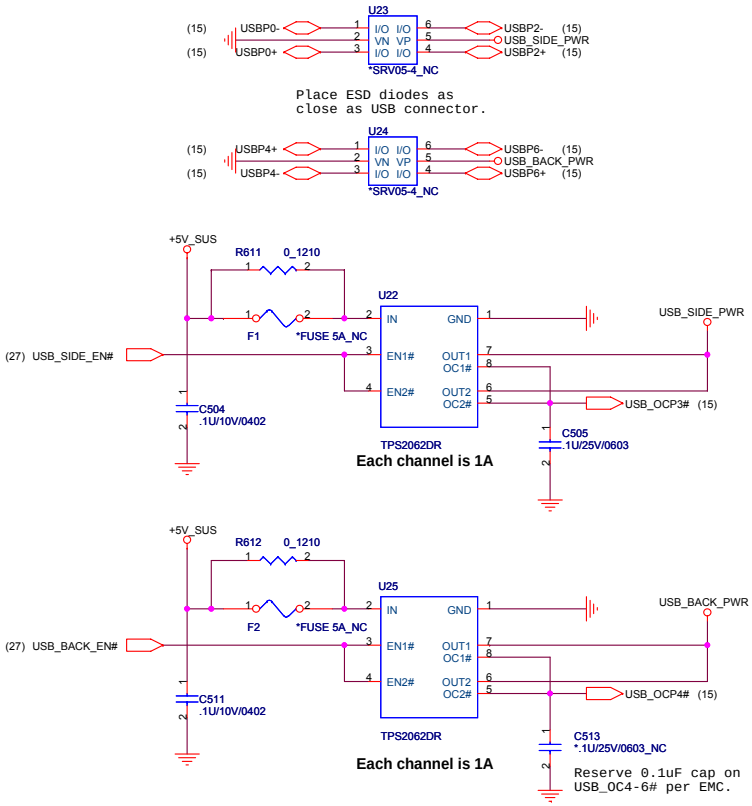
QUANTA COMPUTER

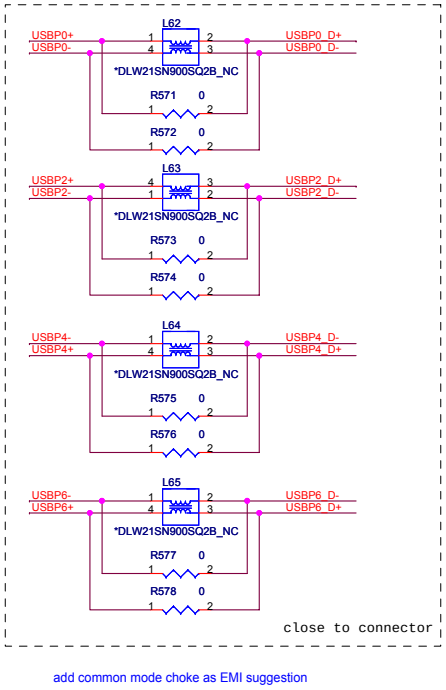
Title	PC97551 & FLASH	
Size	Document Number FX2	Rev 2B
Date: Thursday, September 07, 2006	Sheet 27 of 51	

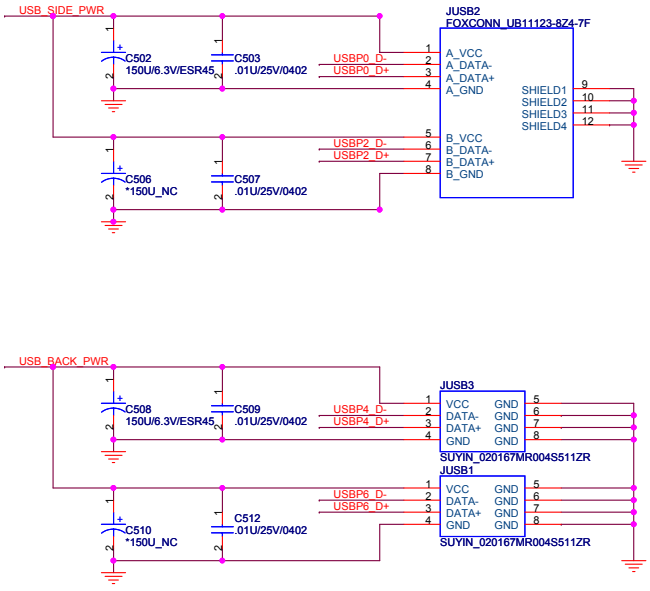
change name for ED5

copy ED5 to FX2

Waiting to check

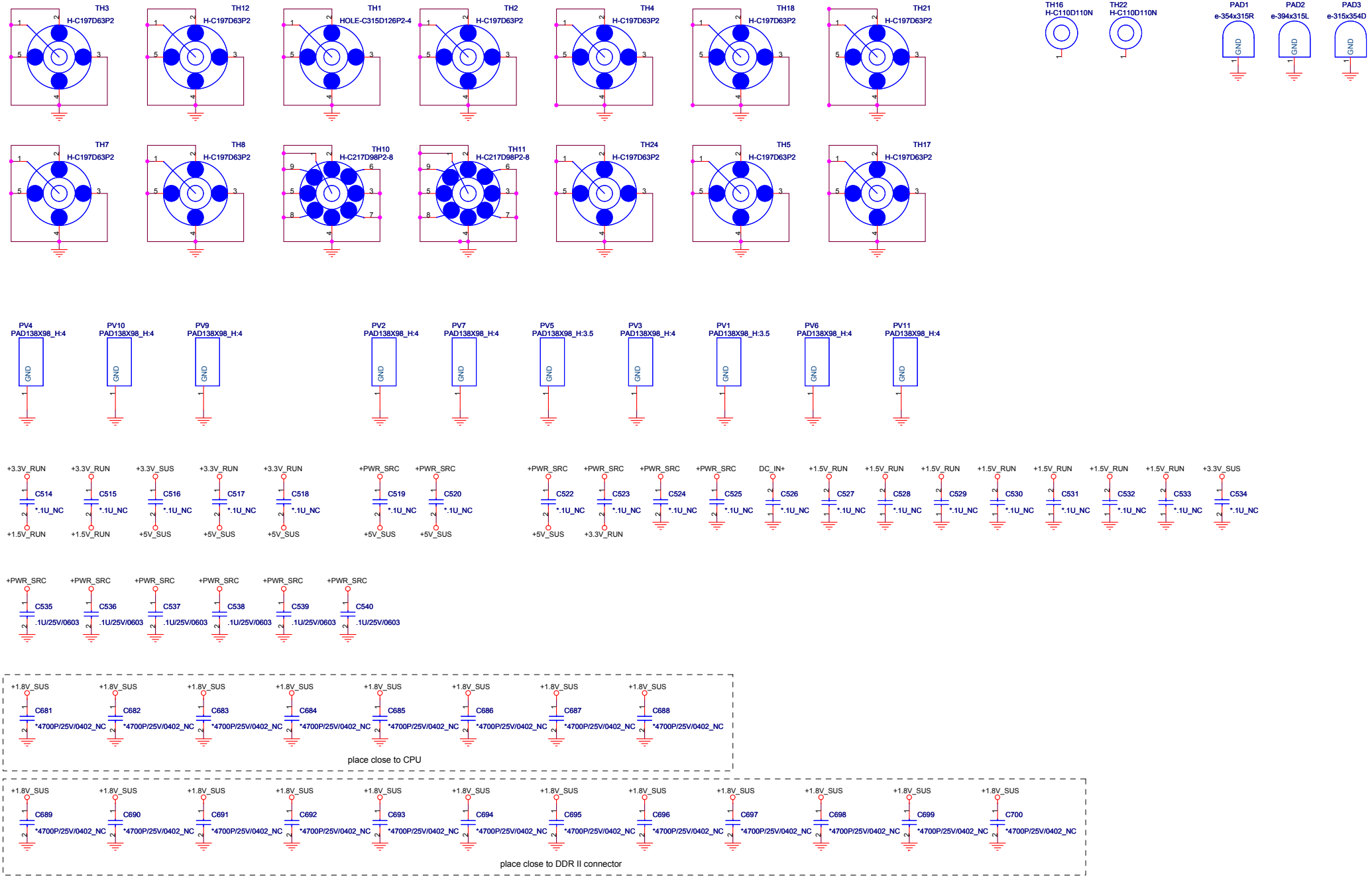






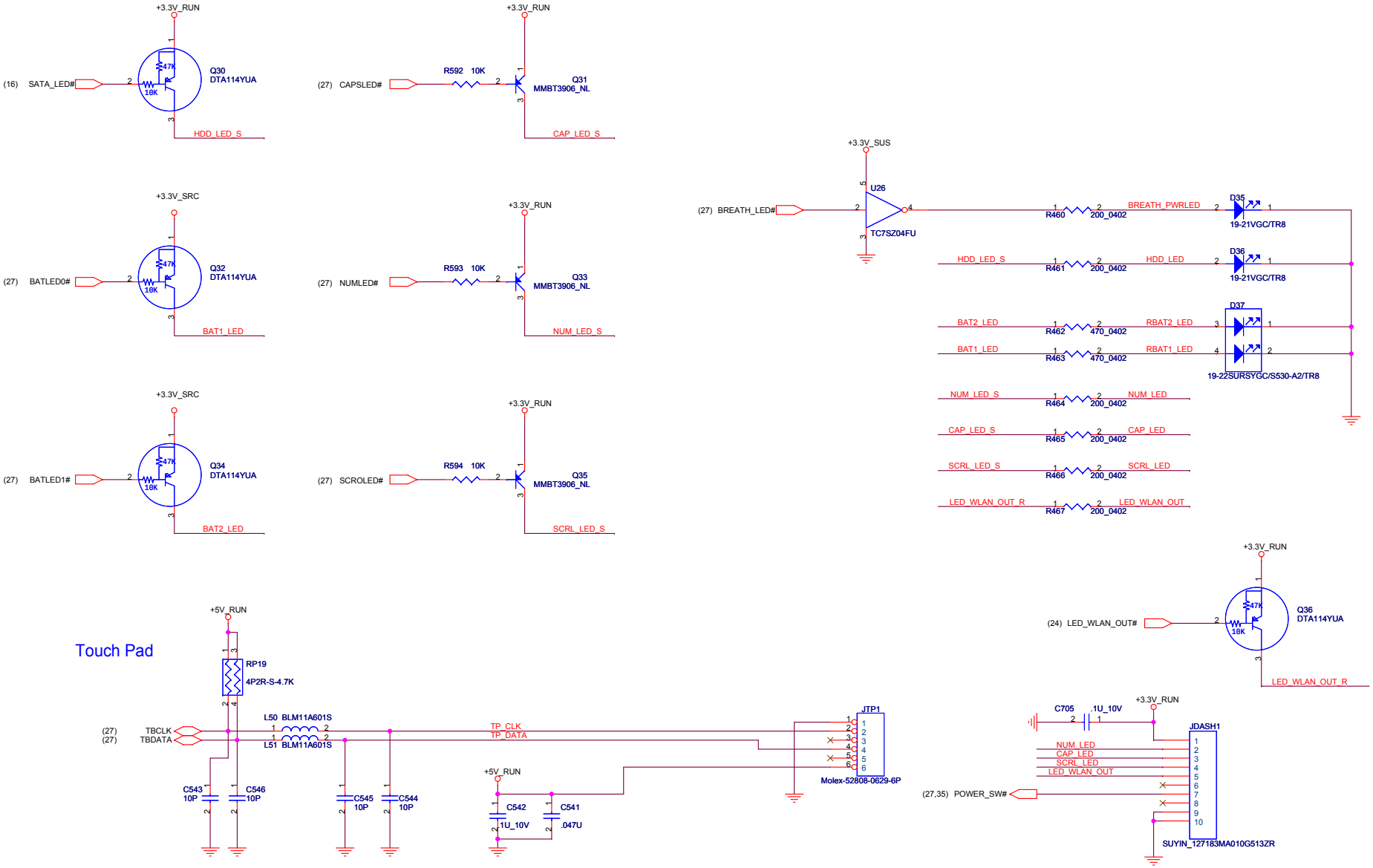
QUANTA COMPUTER

Title	USB	
Size	Document Number FX2	Rev 2B
Date: Thursday, September 07, 2006	Sheet 28 of 51	



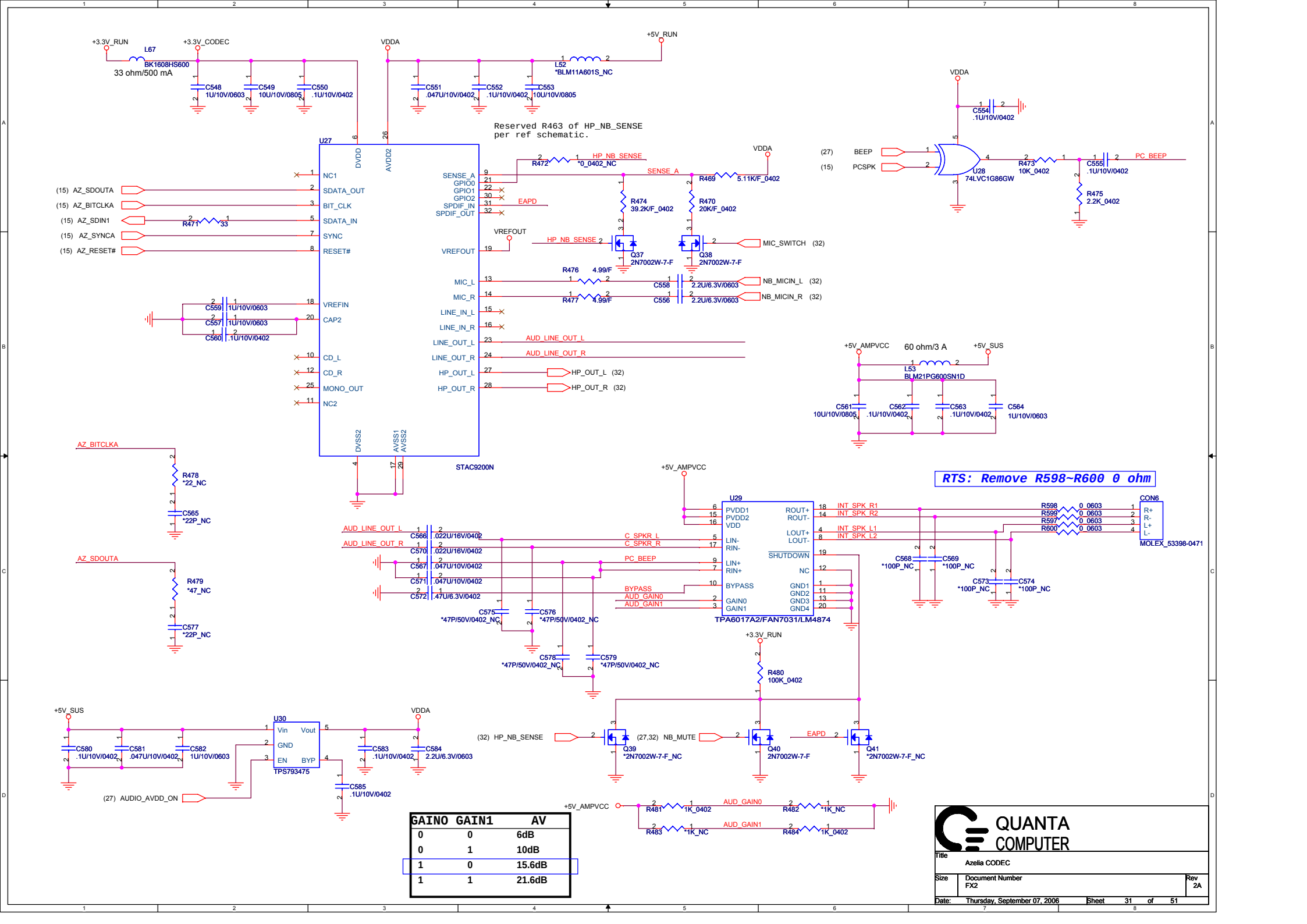
QUANTA COMPUTER

Title	EMI & Screw hole	
Size	Document Number FX2	Rev 2B
Date: Thursday, September 07, 2006	Sheet 29 of 51	



QUANTA COMPUTER

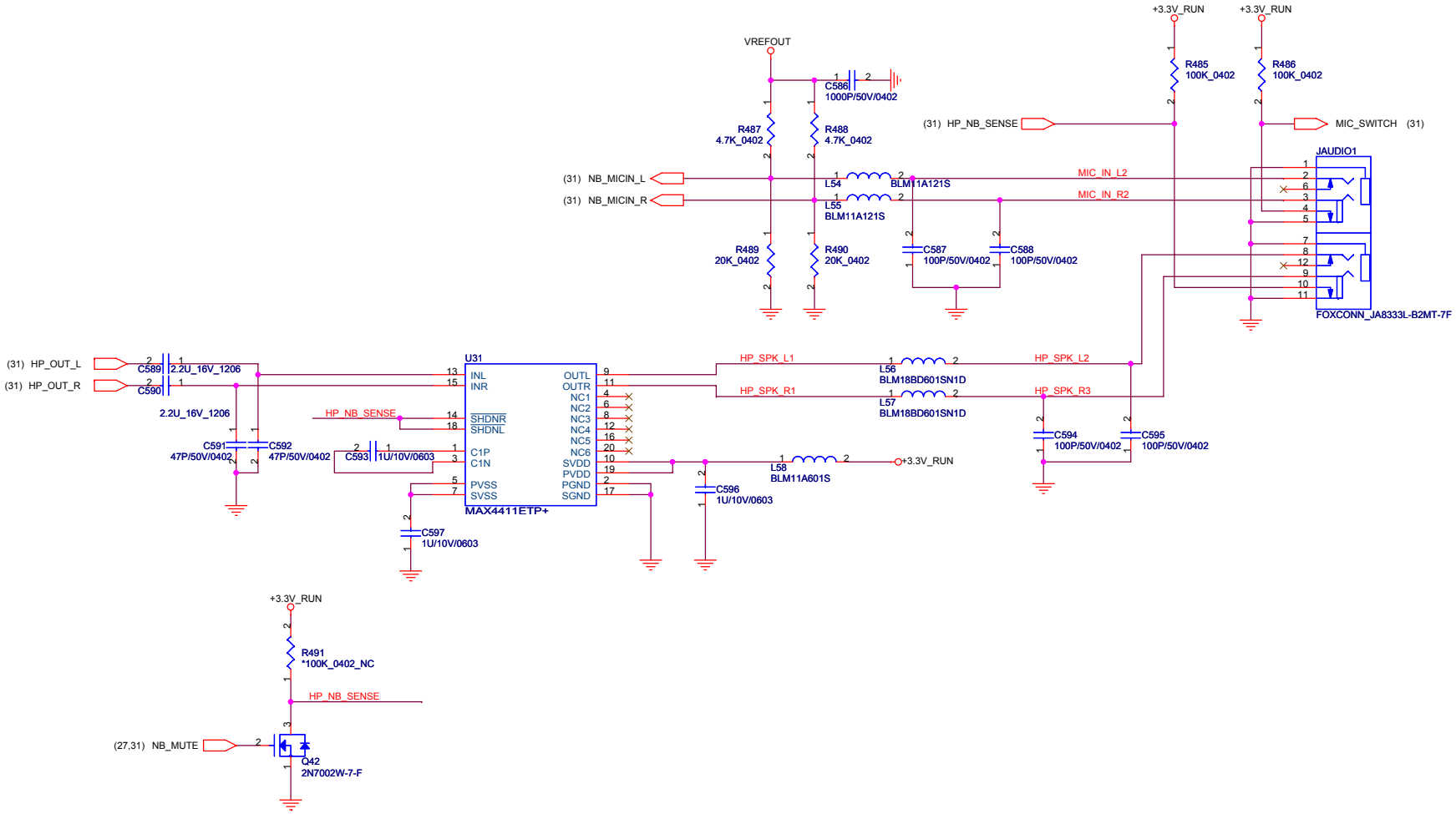
Title	SWITCH & TP & LED	
Size	Document Number FX2	Rev 2B
Date: Thursday, September 07, 2006	Sheet 30 of 51	



GAIN0	GAIN1	AV
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

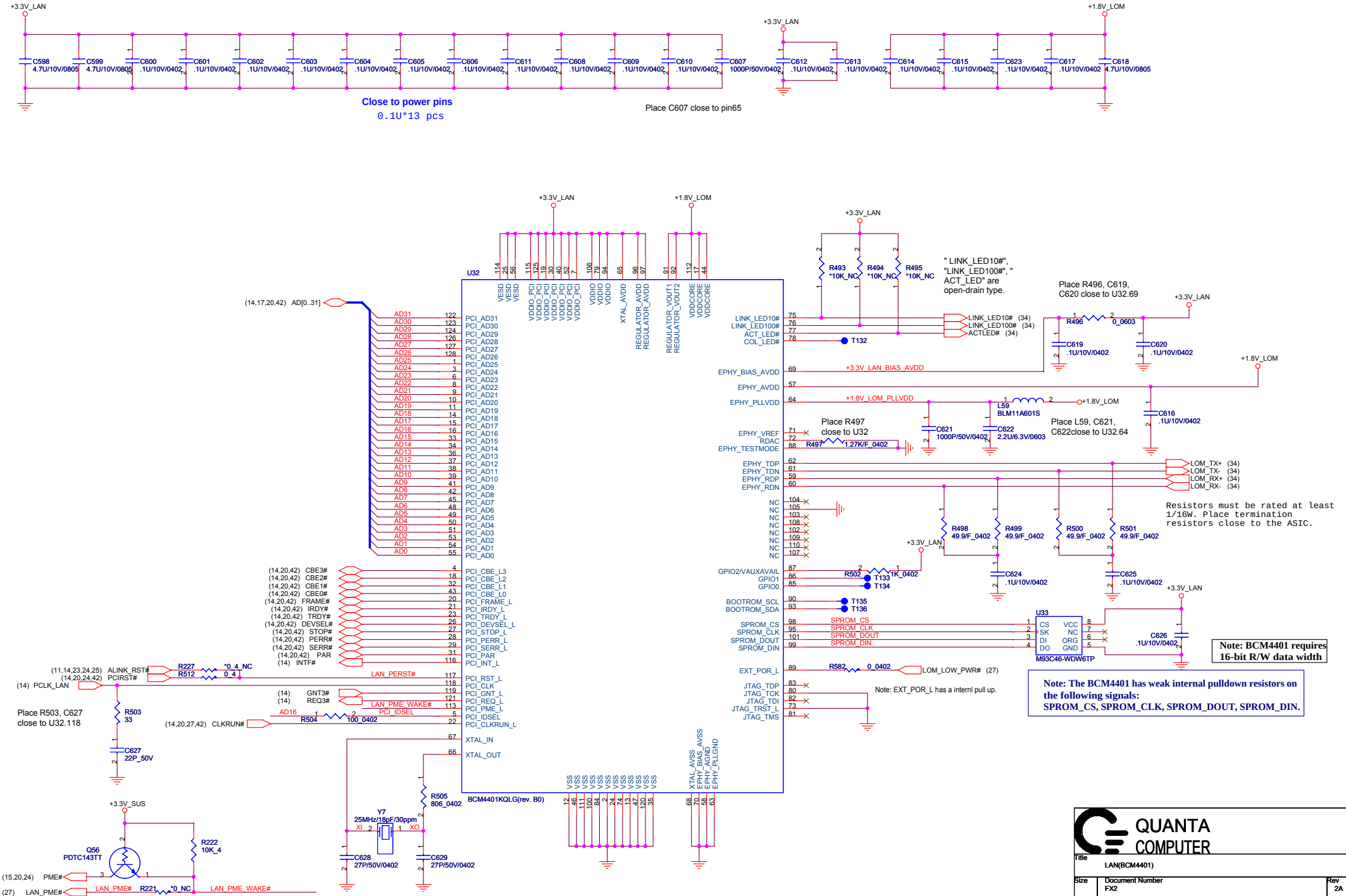
QUANTA COMPUTER

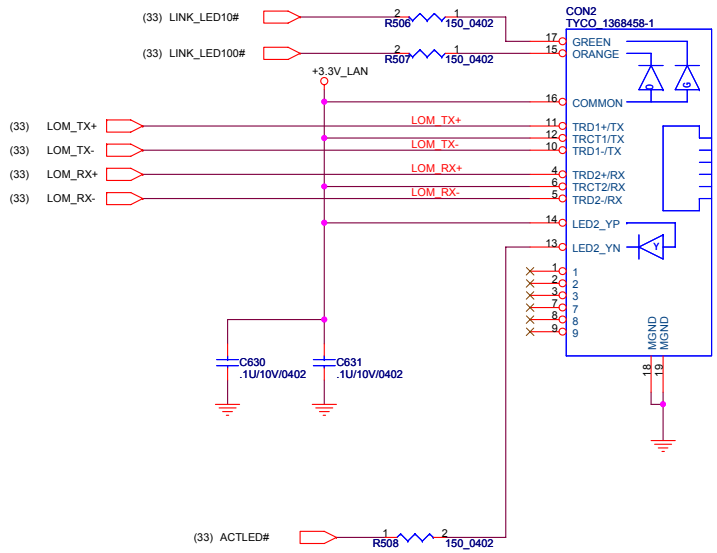
Title	Azelia CODEC	
Size	Document Number FX2	Rev 2A
Date: Thursday, September 07, 2006	Sheet 31 of 51	

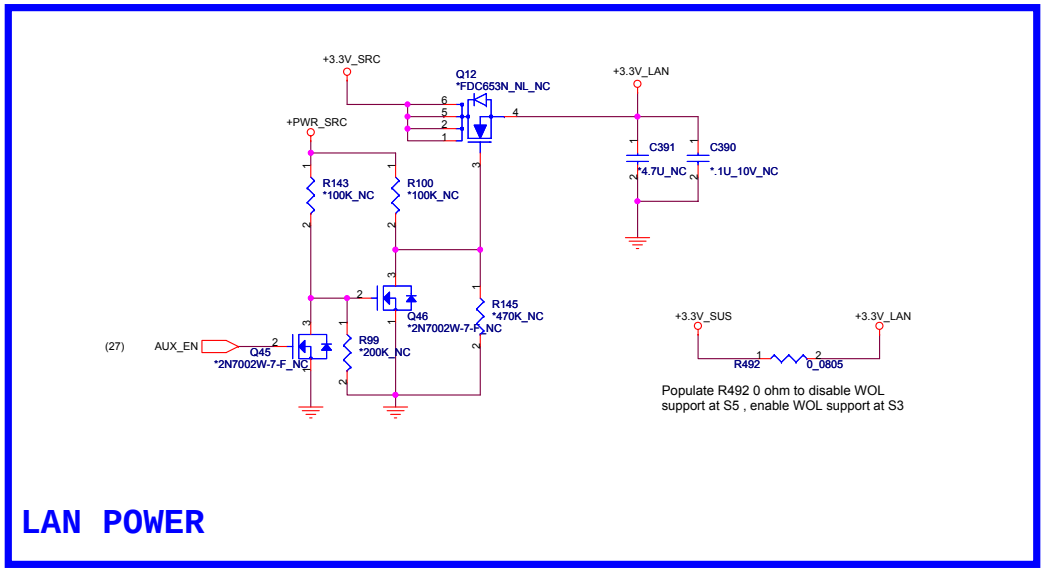


QUANTA COMPUTER

Title	AUDIO CONN	
Size	Document Number FX2	Rev 2B
Date: Thursday, September 07, 2006	Sheet 32 of 51	


+3.3V_LAN
+1.8V_LOM
C598 4.7U/10V/0805
C599 4.7U/10V/0805
C600 .1U/10V/0402
C601 .1U/10V/0402
C602 .1U/10V/0402
C603 .1U/10V/0402
C604 .1U/10V/0402
C605 .1U/10V/0402
C606 .1U/10V/0402
C611 .1U/10V/0402
C608 .1U/10V/0402
C609 .1U/10V/0402
C610 .1U/10V/0402
C607 1000P/50V/0402
C612 .1U/10V/0402
C613 .1U/10V/0402
C614 .1U/10V/0402
C615 .1U/10V/0402
C623 .1U/10V/0402
C617 .1U/10V/0402
C618 4.7U/10V/0805
Close to power pins
0.1U*13 pcs
Place C607 close to pin65
U32
BCM4401KQLG(rev. B0)
" LINK_LED10#", "LINK_LED100#", " ACT_LED" are open-drain type.
Place R496, C619, C620 close to U32.69
Place R497 close to U32
Place L59, C621, C622close to U32.64
Resistors must be rated at least 1/16W. Place termination resistors close to the ASIC.
Note: BCM4401 requires 16-bit R/W data width
Note: The BCM4401 has weak internal pulldown resistors on the following signals: SPROM_CS, SPROM_CLK, SPROM_DOUT, SPROM_DIN.
Note: EXT_POR_L has a internl pull up.
Place R503, C627 close to U32.118
M93C46-WDW6TP
Y7 25MHz/18pF/30ppm
Q56 PDTC143TT
QUANTA COMPUTER
Title LAN(BCM4401)
Size Document Number FX2 Rev 2A
Date: Thursday, September 07, 2006 Sheet 33 of 51

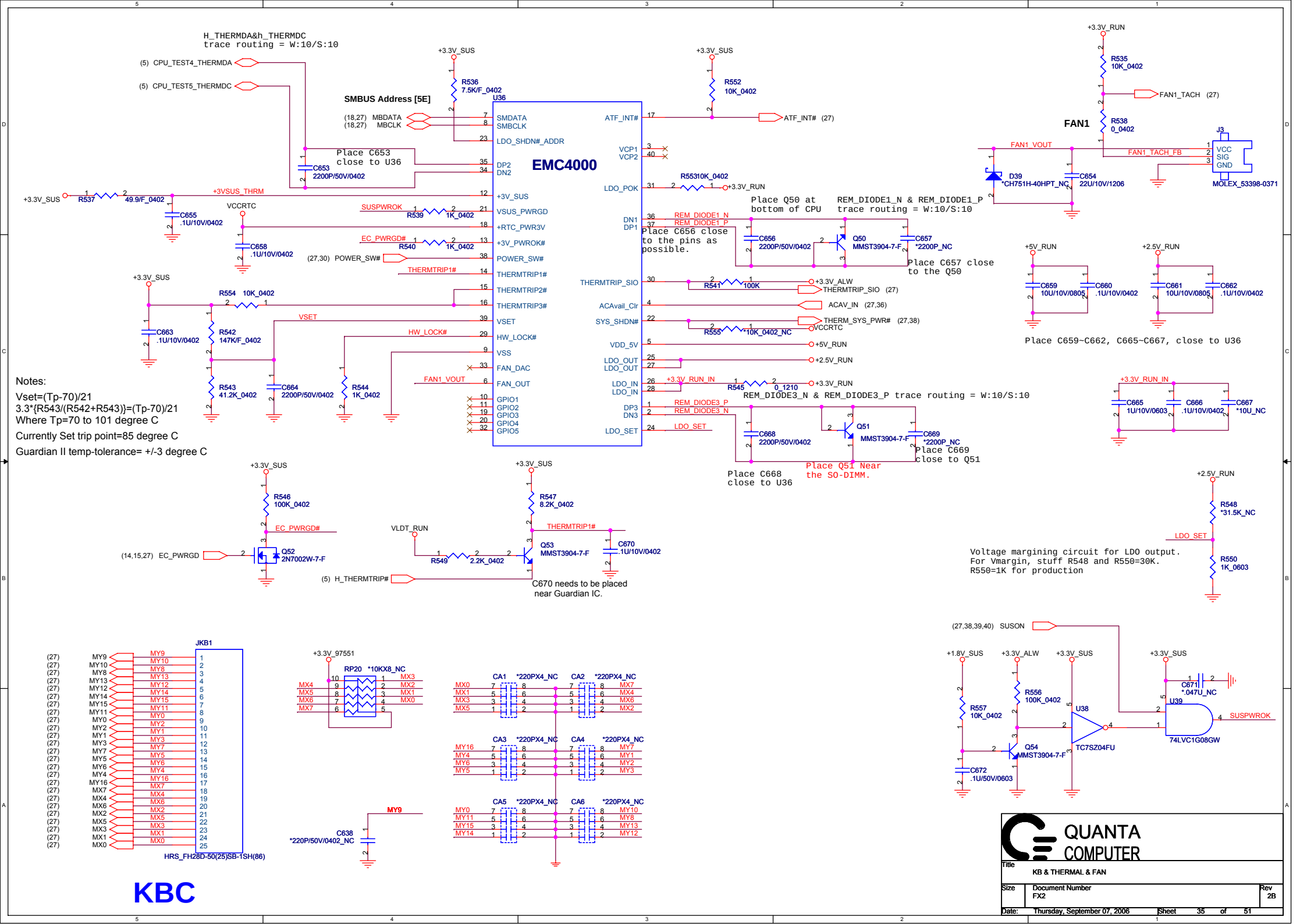




LAN POWER

QUANTA COMPUTER

Title	LAN JACK	
Size	Document Number FX2	Rev 1A
Date: Thursday, September 07, 2006	Sheet 34 of 51	


H_THERMDA&h_THERMDC
trace routing = W:10/S:10
(5) CPU_TEST4_THERMDA
(5) CPU_TEST5_THERMDC
SMBUS Address [5E]
U36
EMC4000
(18,27) MBDATA
(18,27) MBCLK
SMDATA
SMBCLK
LDO_SHDN#_ADDR
DP2
DN2
Place C653
close to U36
C653
2200P/50V/0402
+3.3V_SUS
R536
7.5K/F_0402
R537
49.9/F_0402
+3VSUS_THRM
C655
.1U/10V/0402
VCCRTC
C658
.1U/10V/0402
SUSPWROK
R539
1K_0402
EC_PWRGD#
R540
1K_0402
(27,30) POWER_SW#
THERMTRIP1#
+3V_SUS
VSUS_PWRGD
+RTC_PWR3V
+3V_PWROK#
POWER_SW#
THERMTRIP1#
THERMTRIP2#
THERMTRIP3#
VSET
HW_LOCK#
VSS
FAN_DAC
FAN_OUT
FAN1_VOUT
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
ATF_INT#
VCP1
VCP2
LDO_POK
DN1
DP1
THERMTRIP_SIO
ACAvail_Clr
SYS_SHDN#
VDD_5V
LDO_OUT
LDO_OUT
LDO_IN
LDO_IN
DP3
DN3
LDO_SET
R552
10K_0402
ATF_INT# (27)
R55310K_0402
+3.3V_RUN
Place Q50 at
bottom of CPU
REM_DIODE1_N & REM_DIODE1_P
trace routing = W:10/S:10
REM_DIODE1_N
REM_DIODE1_P
Place C656 close
to the pins as
possible.
C656
2200P/50V/0402
Q50
MMST3904-7-F
C657
*2200P_NC
Place C657 close
to the Q50
R541
100K
+3.3V_ALW
THERMTRIP_SIO (27)
ACAV_IN (27,36)
R555
*10K_0402_NC
THERM_SYS_PWR# (27,38)
VCCRTC
+5V_RUN
+2.5V_RUN
+3.3V_RUN_IN
R545
0_1210
REM_DIODE3_N & REM_DIODE3_P trace routing = W:10/S:10
REM_DIODE3_P
REM_DIODE3_N
C668
2200P/50V/0402
Q51
MMST3904-7-F
C669
*2200P_NC
Place C669
close to Q51
Place C668
close to U36
Place Q51 Near
the SO-DIMM.
+3.3V_RUN
R535
10K_0402
FAN1_TACH (27)
FAN1
R538
0_0402
J3
FAN1_VOUT
FAN1_TACH_FB
D39
*CH751H-40HPT_NC
C654
22U/10V/1206
VCC
SIG
GND
MOLEX_53398-0371
C659
10U/10V/0805
C660
.1U/10V/0402
C661
10U/10V/0805
C662
.1U/10V/0402
Place C659~C662, C665~C667, close to U36
C663
.1U/10V/0402
R554
10K_0402
R542
147K/F_0402
R543
41.2K_0402
C664
2200P/50V/0402
R544
1K_0402
C665
1U/10V/0603
C666
.1U/10V/0402
C667
*10U_NC
Notes:
Vset=(Tp-70)/21
3.3*{R543/(R542+R543)}=(Tp-70)/21
Where Tp=70 to 101 degree C
Currently Set trip point=85 degree C
Guardian II temp-tolerance= +/-3 degree C
R546
100K_0402
EC_PWRGD#
(14,15,27) EC_PWRGD
Q52
2N7002W-7-F
VLDT_RUN
R549
2.2K_0402
R547
8.2K_0402
THERMTRIP1#
Q53
MMST3904-7-F
C670
.1U/10V/0402
(5) H_THERMTRIP#
C670 needs to be placed
near Guardian IC.
R548
*31.5K_NC
LDO_SET
R550
1K_0603
Voltage margining circuit for LDO output.
For Vmargin, stuff R548 and R550=30K.
R550=1K for production
JKB1
HRS_FH28D-50(25)SB-1SH(86)
RP20 *10KX8_NC
C638
*220P/50V/0402_NC
CA1 *220PX4_NC
CA2 *220PX4_NC
CA3 *220PX4_NC
CA4 *220PX4_NC
CA5 *220PX4_NC
CA6 *220PX4_NC
(27,38,39,40) SUSON
R557
10K_0402
R556
100K_0402
Q54
MMST3904-7-F
C672
.1U/50V/0603
U38
TC7SZ04FU
U39
74LVC1G08GW
C671
*.047U_NC
SUSPWROK
KBC
QUANTA
COMPUTER
Title
KB & THERMAL & FAN
Size
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2B
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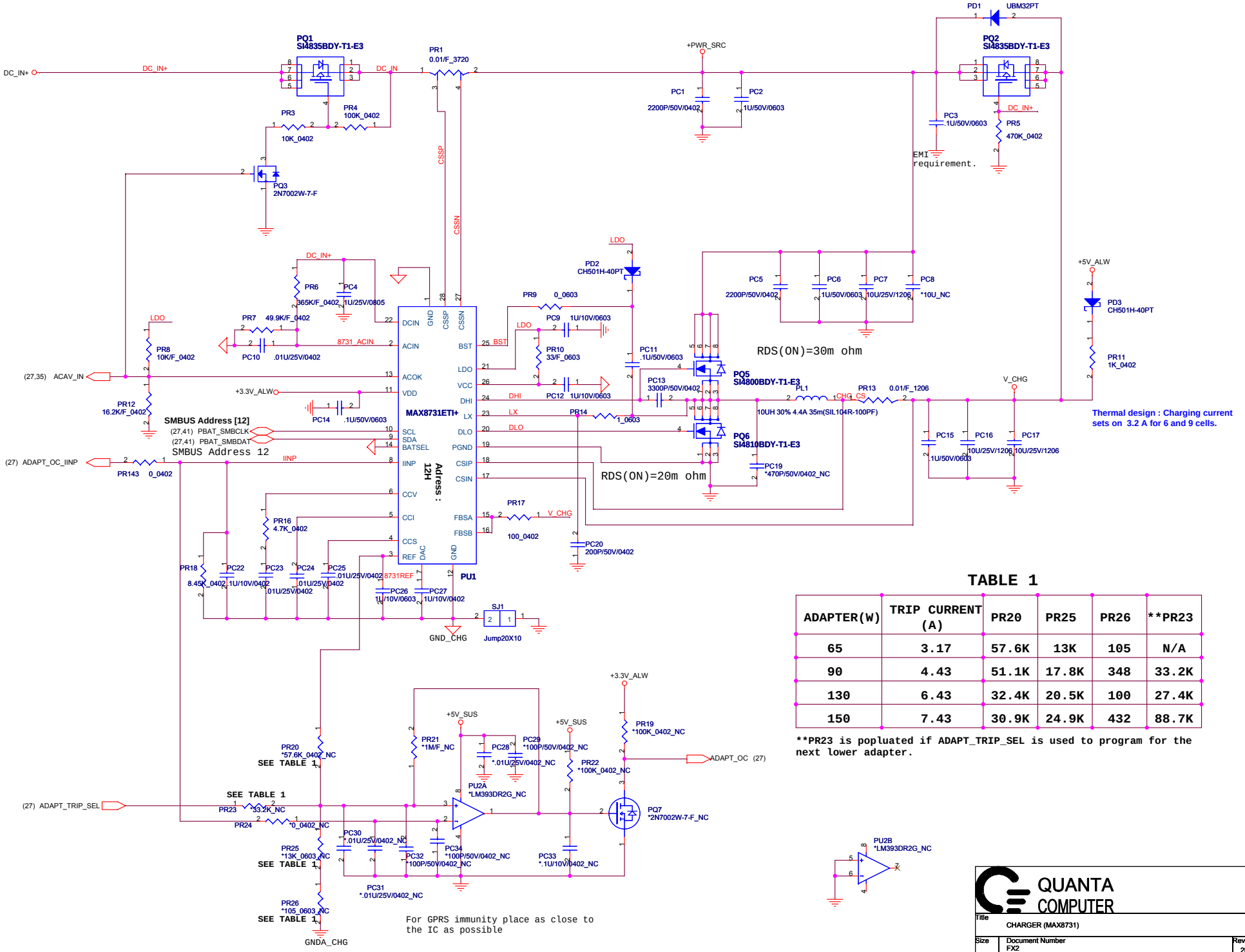


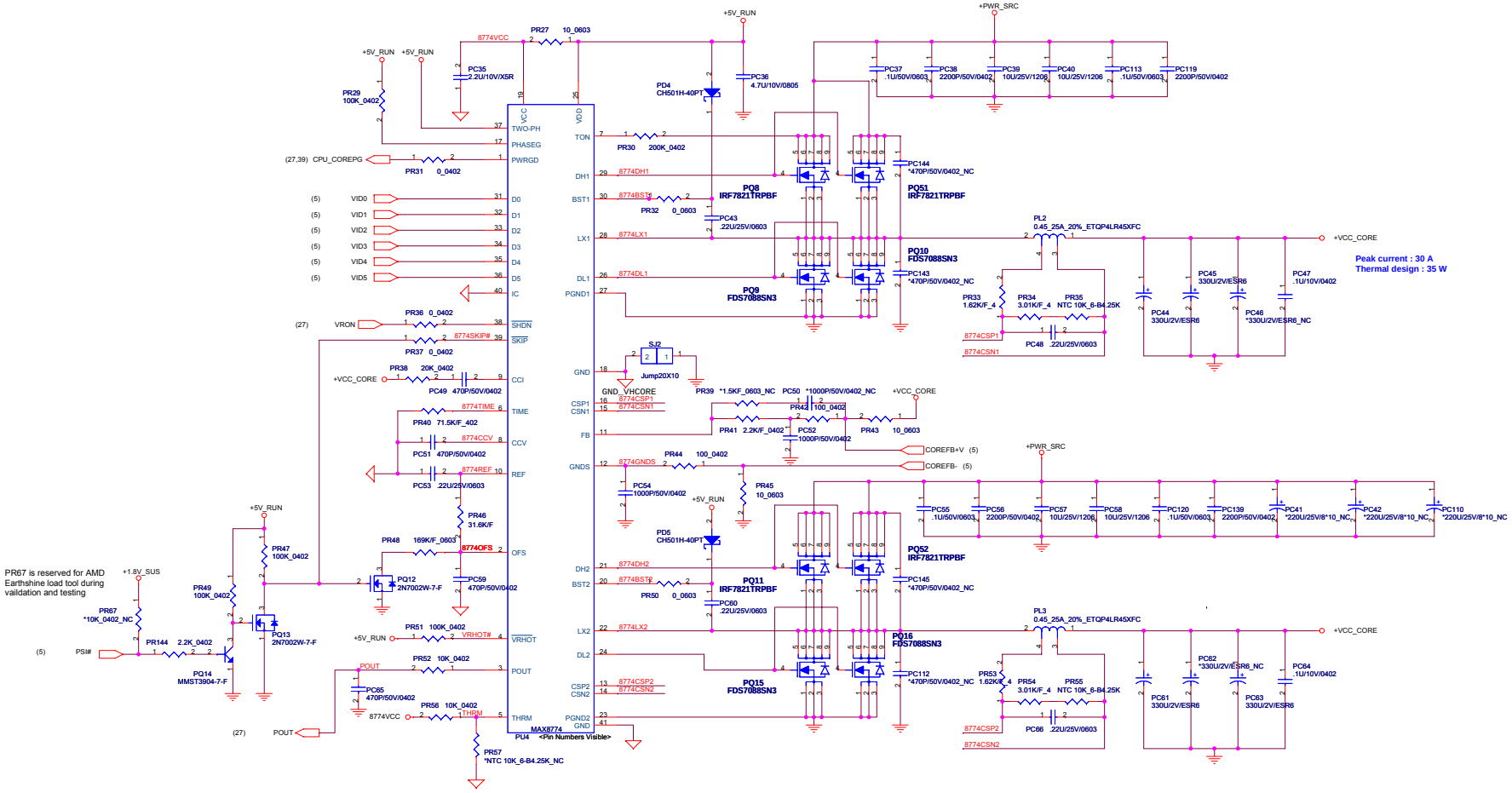
TABLE 1

ADAPTER(W)	TRIP CURRENT (A)	PR20	PR25	PR26	**PR23
65	3.17	57.6K	13K	105	N/A
90	4.43	51.1K	17.8K	348	33.2K
130	6.43	32.4K	20.5K	100	27.4K
150	7.43	30.9K	24.9K	432	88.7K

**PR23 is popluated if ADAPT_TRIP_SEL is used to program for the next lower adapter.

QUANTA COMPUTER

Title	CHARGER (MAX8731)	
Size	Document Number FX2	Rev 2B
Date: 2005/4/21	Sheet 36 of 51	



D5	D4	D3	D2	D1	D0	Output
0	0	0	0	0	0	1.5500V
0	0	0	0	0	1	1.5250V
0	0	0	0	1	0	1.5000V
0	0	0	0	1	1	1.4750V
0	0	0	1	0	0	1.4500V
0	0	0	1	0	1	1.4250V
0	0	0	1	1	0	1.4000V
0	0	0	1	1	1	1.3750V
0	0	1	0	0	0	1.3500V
0	0	1	0	0	1	1.3250V
0	0	1	0	1	0	1.3000V
0	0	1	0	1	1	1.2750V
0	0	1	1	0	0	1.2500V
0	0	1	1	0	1	1.2250V
0	0	1	1	1	0	1.2000V
0	0	1	1	1	1	1.1750V
0	1	0	0	0	0	1.1500V
0	1	0	0	0	1	1.1250V
0	1	0	0	1	0	1.1000V
0	1	0	0	1	1	1.0750V
0	1	0	1	0	0	1.0500V
0	1	0	1	0	1	1.0250V
0	1	0	1	1	0	1.0000V
0	1	0	1	1	1	0.9750V
0	1	1	0	0	0	0.9500V
0	1	1	0	0	1	0.9250V
0	1	1	0	1	0	0.9000V
0	1	1	0	1	1	0.8750V
0	1	1	1	0	0	0.8500V
0	1	1	1	0	1	0.8250V
0	1	1	1	1	0	0.8000V
0	1	1	1	1	1	0.7750V

D5	D4	D3	D2	D1	D0	Output
1	0	0	0	0	0	0.7625V
1	0	0	0	0	1	0.7500V
1	0	0	0	1	0	0.7375V
1	0	0	0	1	1	0.7250V
1	0	0	1	0	0	0.7125V
1	0	0	1	0	1	0.7000V
1	0	0	1	1	0	0.6875V
1	0	0	1	1	1	0.6750V
1	0	1	0	0	0	0.6625V
1	0	1	0	0	1	0.6500V
1	0	1	0	1	0	0.6375V
1	0	1	0	1	1	0.6250V
1	0	1	1	0	0	0.6125V
1	0	1	1	0	1	0.6000V
1	0	1	1	1	0	0.5875V
1	0	1	1	1	1	0.5750V
1	1	0	0	0	0	0.5625V
1	1	0	0	0	1	0.5500V
1	1	0	0	1	0	0.5375V
1	1	0	0	1	1	0.5250V
1	1	0	1	0	0	0.5125V
1	1	0	1	0	1	0.5000V
1	1	0	1	1	0	0.4875V
1	1	0	1	1	1	0.4750V
1	1	1	0	0	0	0.4625V
1	1	1	0	0	1	0.4500V
1	1	1	0	1	0	0.4375V
1	1	1	0	1	1	0.4250V
1	1	1	1	0	0	0.4125V
1	1	1	1	0	1	0.4000V
1	1	1	1	1	0	0.3875V
1	1	1	1	1	1	0.3750V

QUANTA COMPUTER

Title	VHCORE (MAX8774)	
Size	Document Number FX2	Rev 2B
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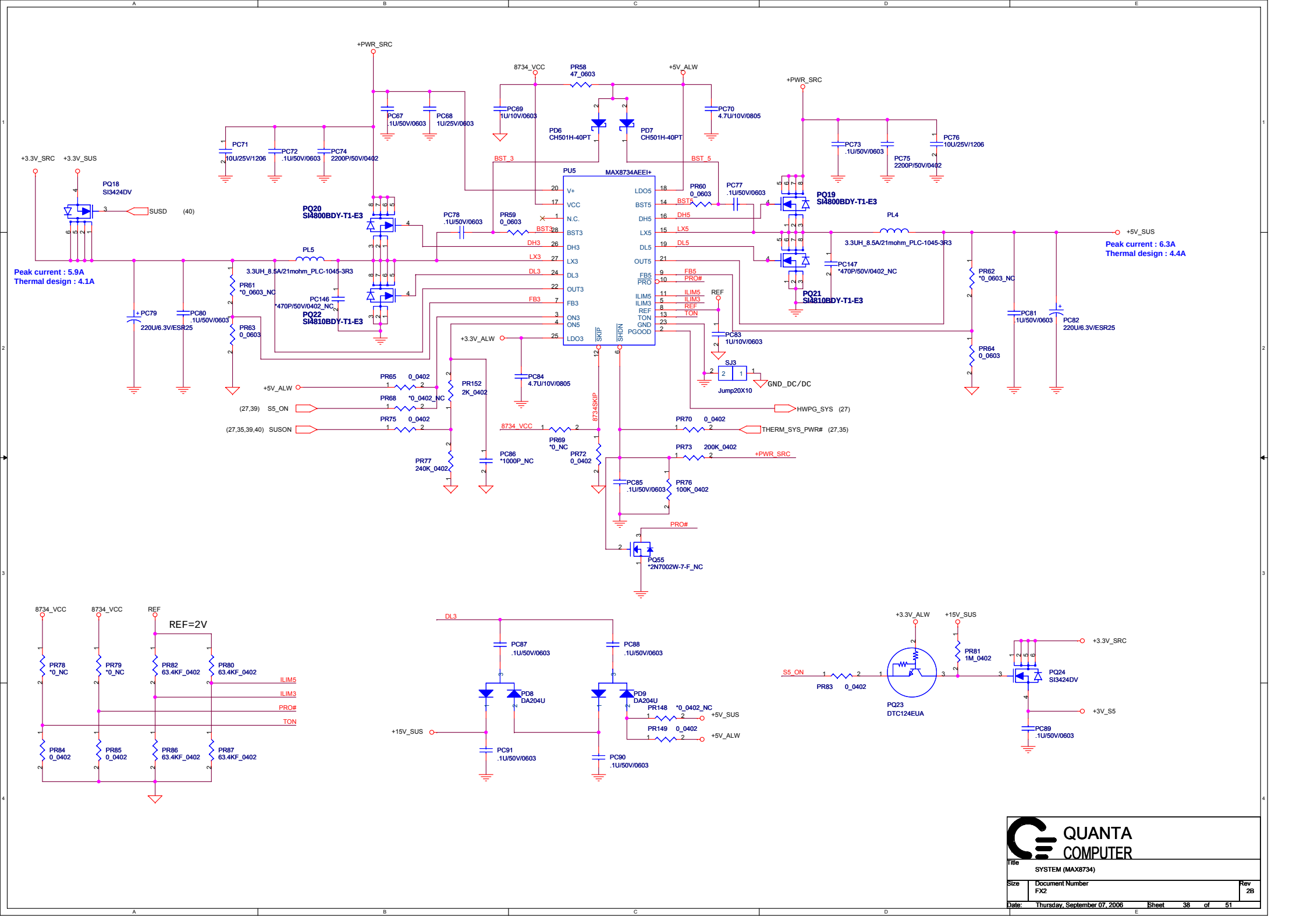
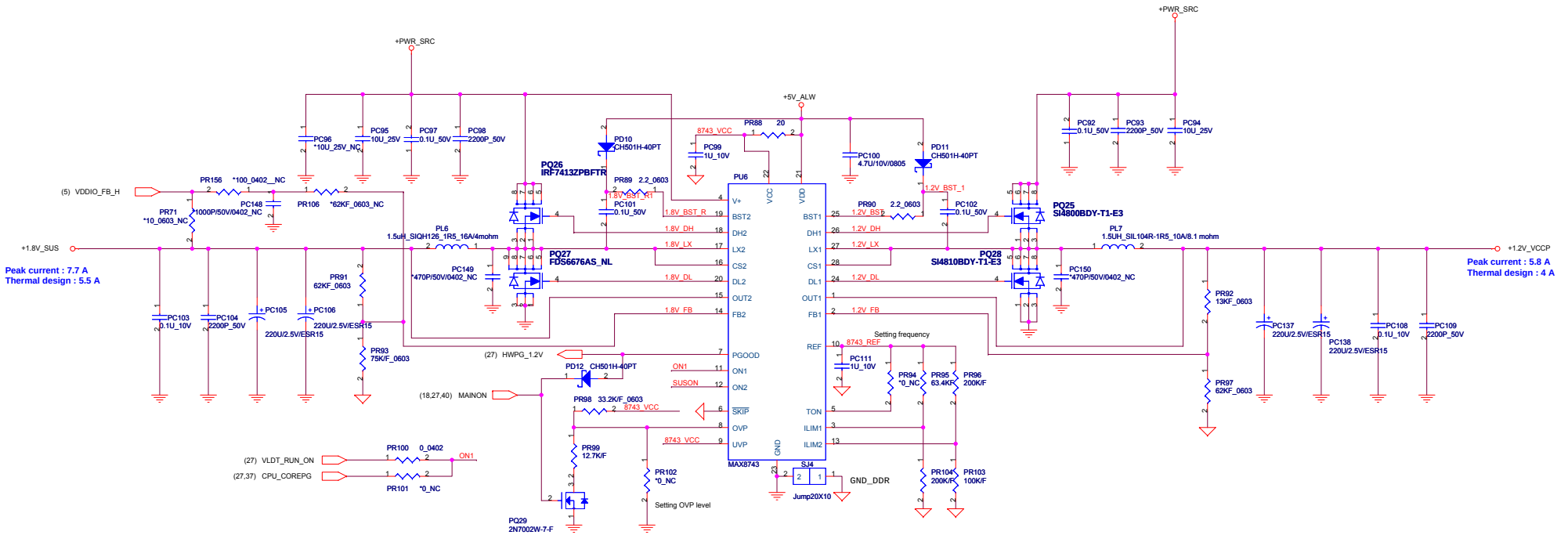
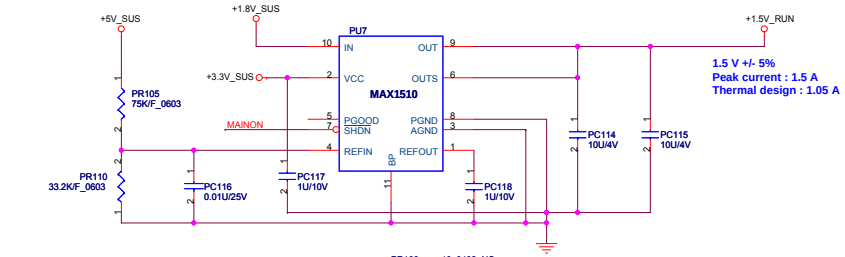
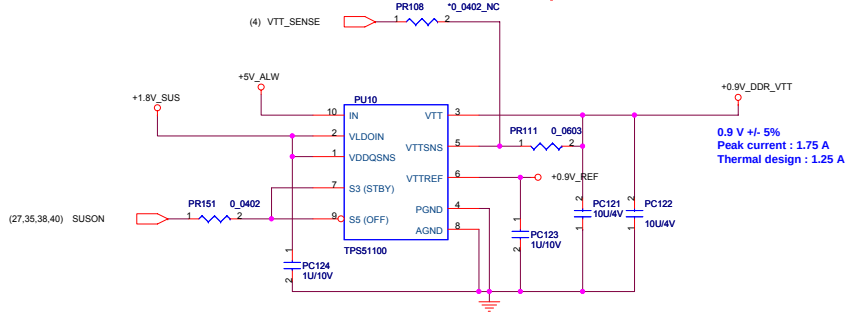


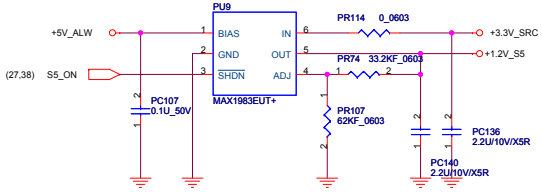
QUANTA COMPUTER

Title	SYSTEM (MAX8734)	
Size	Document Number FX2	Rev 2B
Date: Thursday, September 07, 2006	Sheet 38 of 51	

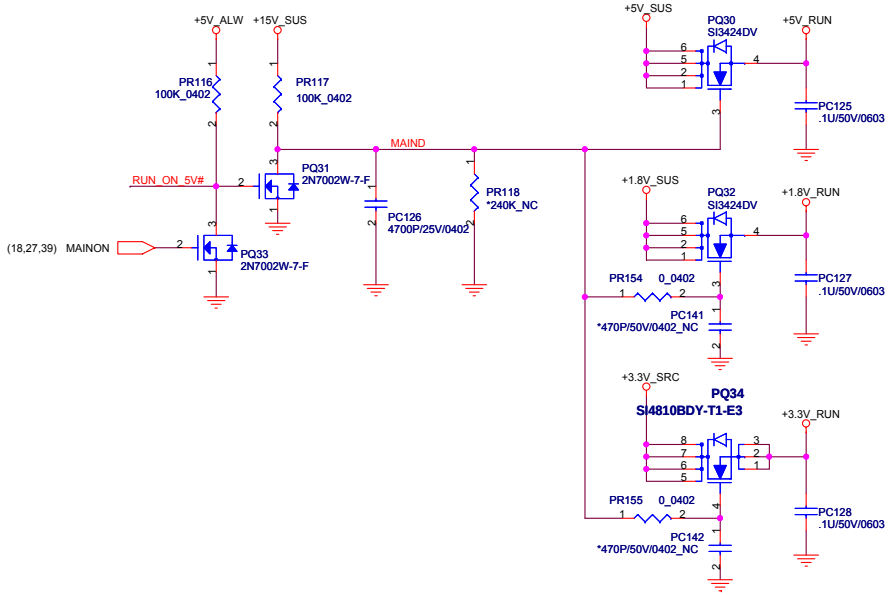


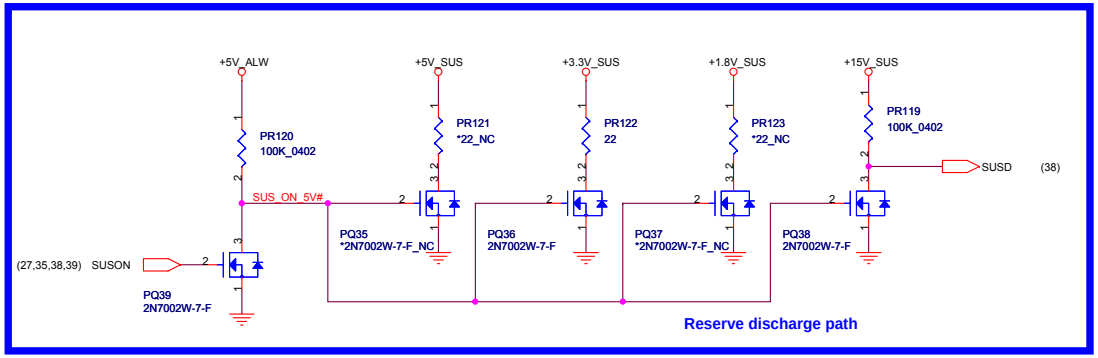


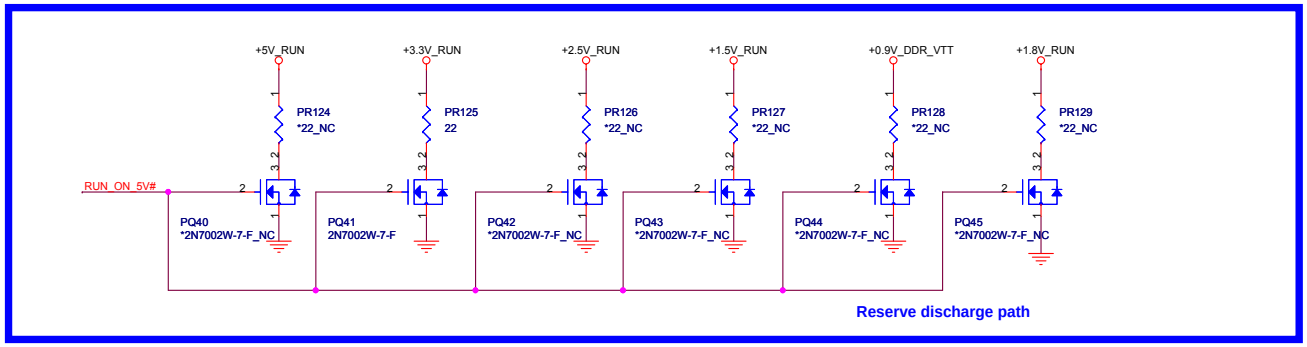




QUANTA COMPUTER		
Title: VCCP		
Size	Document Number: FX2	Rev: 2B
Date: 2005/4/21	Sheet 39 of 51	

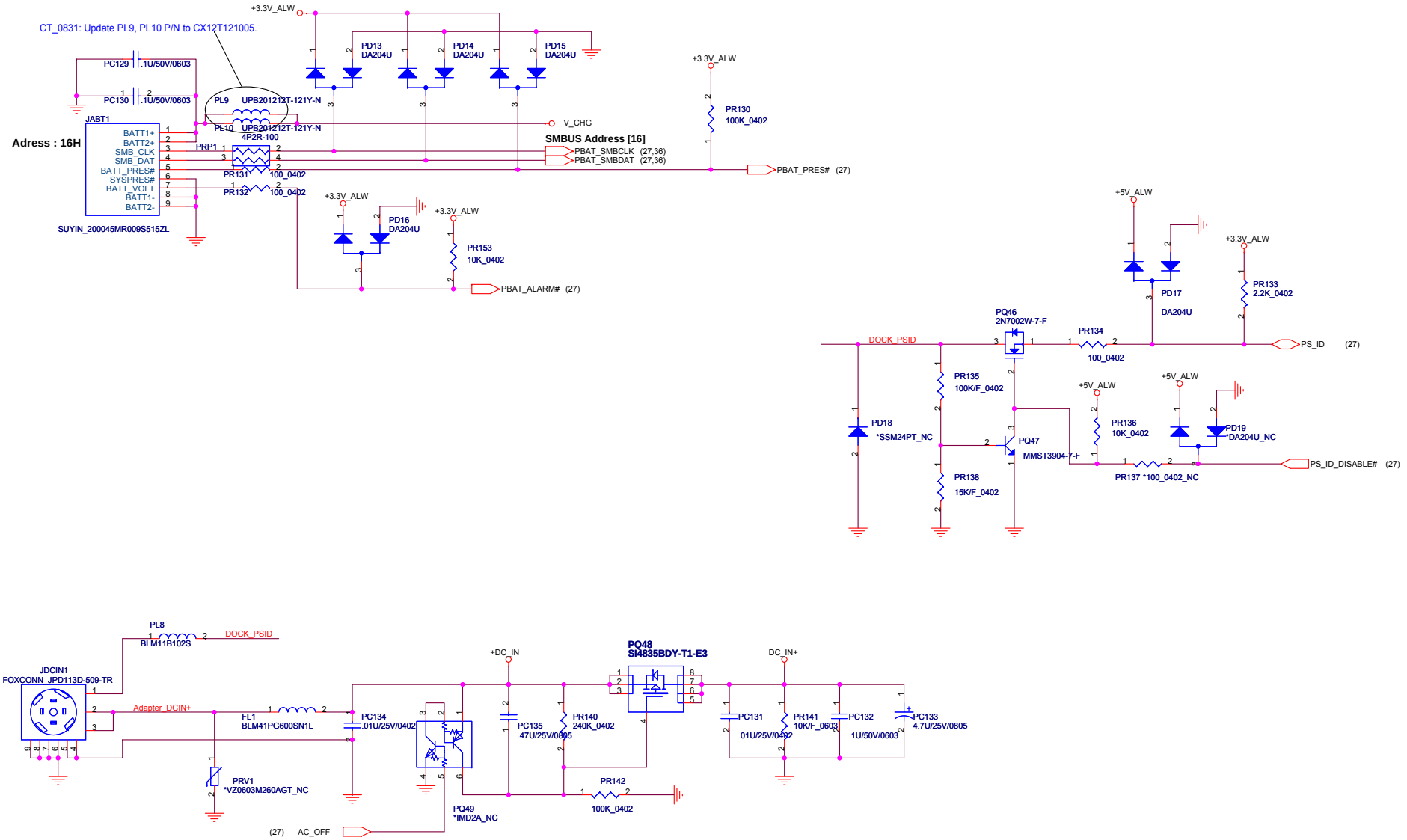






QUANTA COMPUTER

Title	RUN POWER SW	
Size	Document Number FX2	Rev 2A
Date: Thursday, September 07, 2006	Sheet 40 of 51	



Title	DCIN,Batt		
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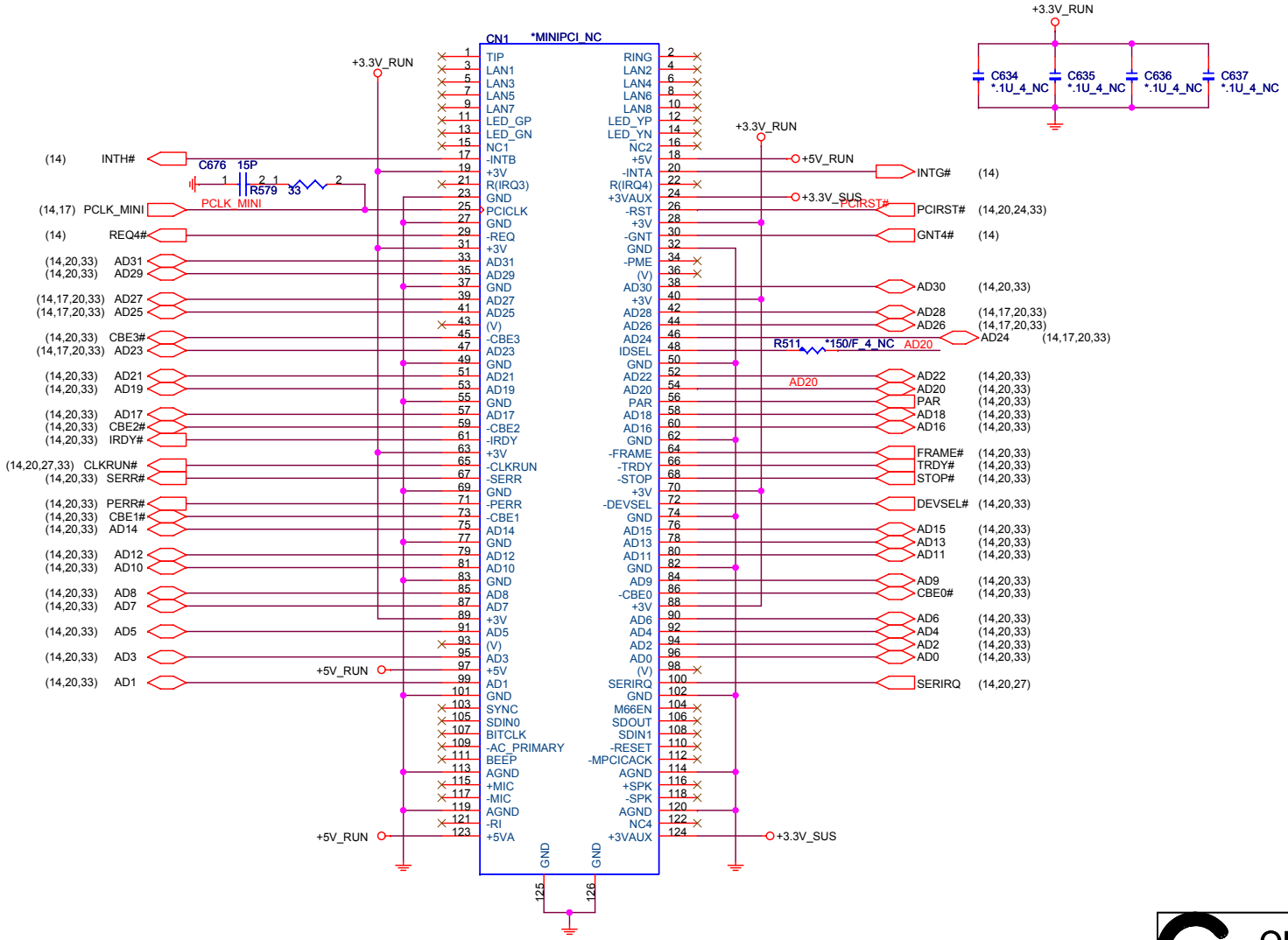
ID Select : AD20
Interrupt Pin : INTG# , INTH#
Request Indicate : REQ4#
Grant Indicate : GNT4#

DEBUG PURPOSE ONLY



MPC

QUANTA COMPUTER

Title	MINI PCI(for debug)	
Size	Document Number FX2	Rev 2A
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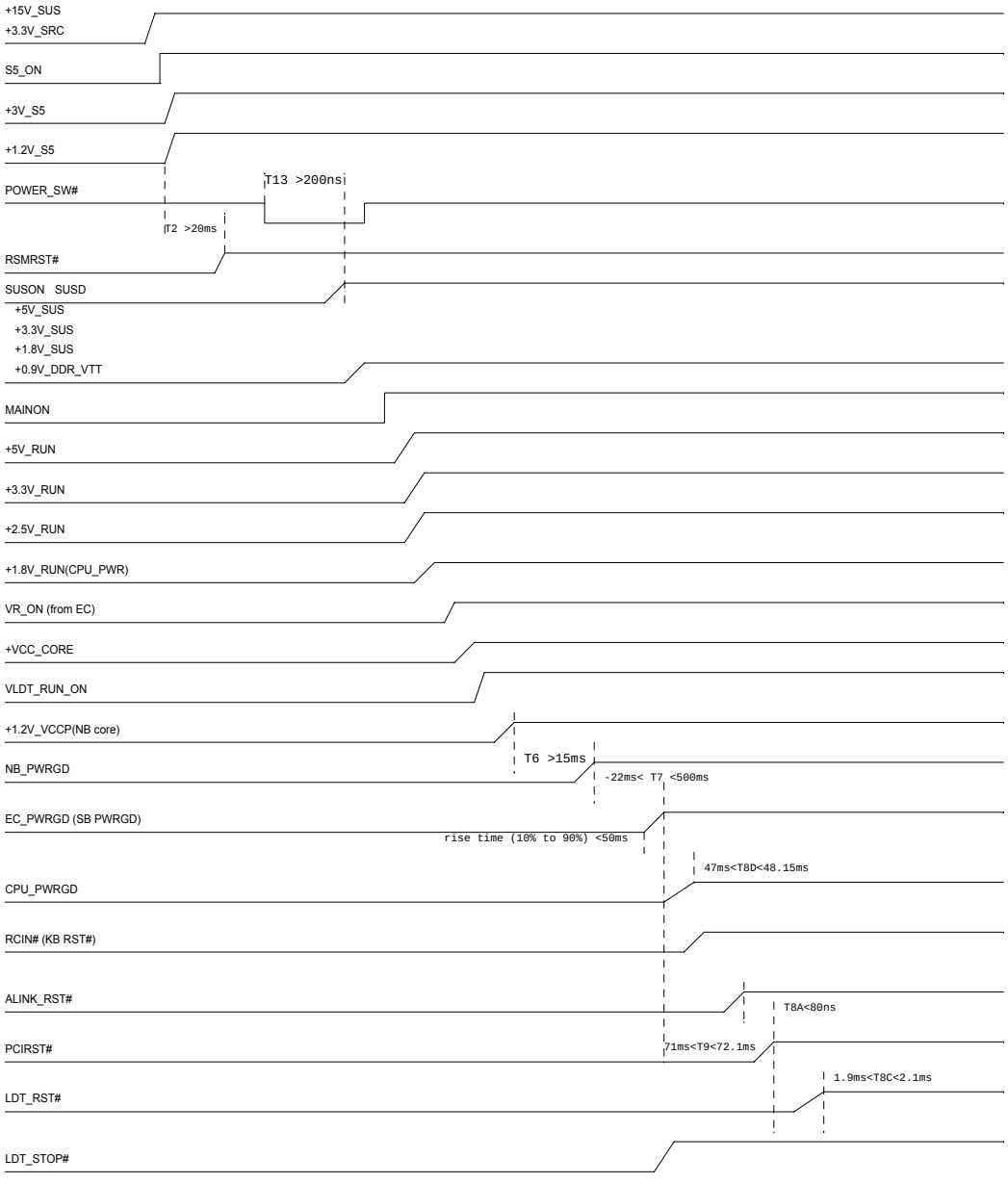
Power On Sequence



T6: NB core voltage to NB_PWRGD
T7: NB_PWRGD to SB_PWRGD
T8D: SB_PWRGD to CPU_PWRGD

T8A: ALINK_RST# to PCIRST#
T9: SB_PWRGD to PCIRST#
T8C: PCIRST# to LDT_RST#

QUANTA COMPUTER

Title	Power On Sequence	
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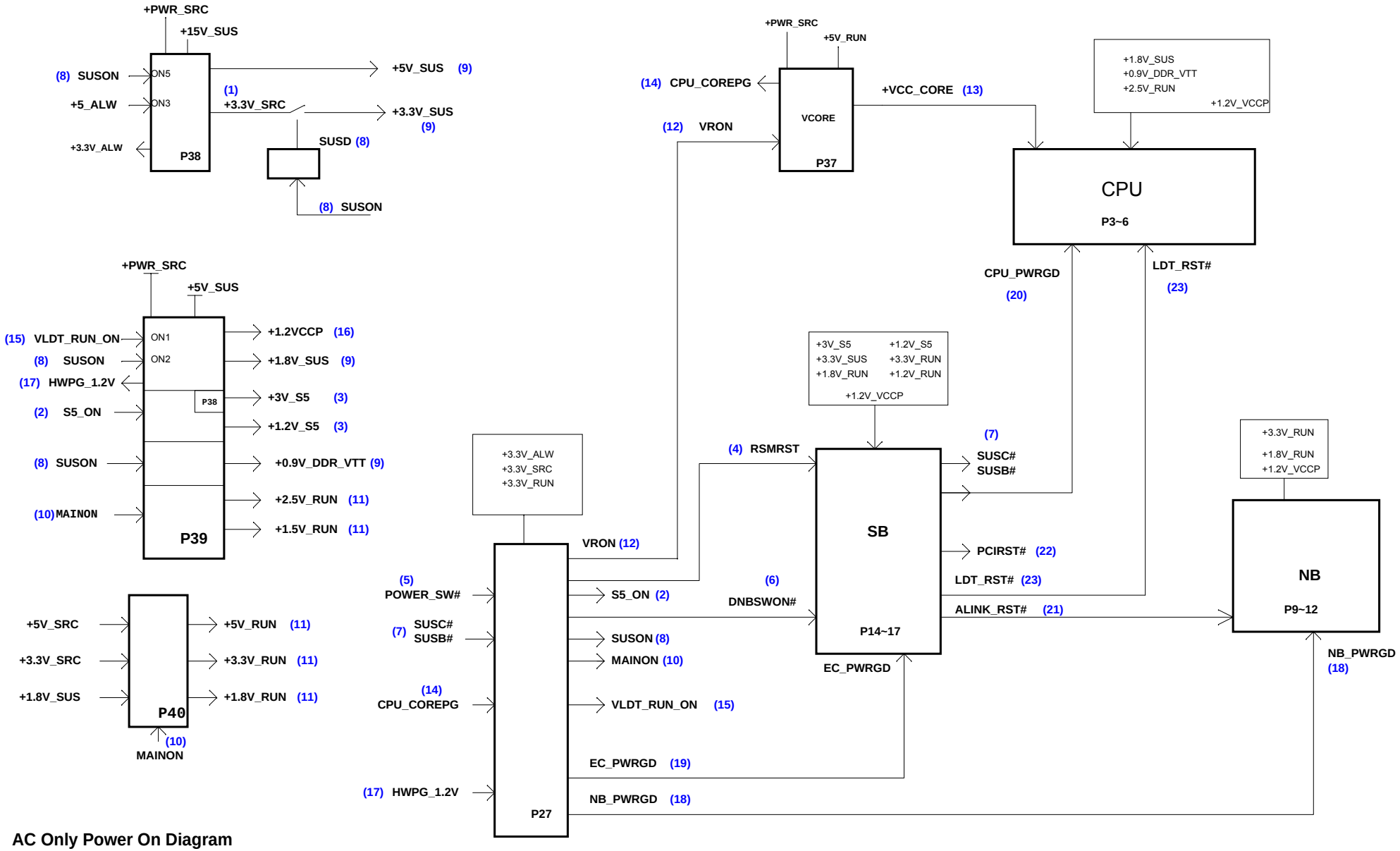

AC Only Power On Diagram

(1) +3.3V_SRC
(2) S5_ON
(3) +3V_S5, +1.2V_S5
(4) RSMRST
(5) POWER_SW#
(6) DNBSWON#
(7) SUSC#, SUSB#
(8) SUSON, SUSD
(9) +5V_SUS
+0.9V_DDR_VTT, +3.3V_SUS, +1.8V_SUS
(10) MAINON
(11) +5V_RUN, +3.3V_RUN
+2.5V_RUN, +1.8V_RUN, +1.5V_RUN
(12) VRON
(13) +VCC_CORE
(14) CPU_COREPG
(15) VLDT_RUN_ON
(16) +1.2_VCCP
(17) HWPG_1.2V
(18) NB_PWRGD
(19) EC_PWRGD
(20) CPU_PWRGD
(21) ALINK_RST#
(22) PCI_RST#
(23) LDT_RST#

QUANTA COMPUTER

Title	Power On Diagram	
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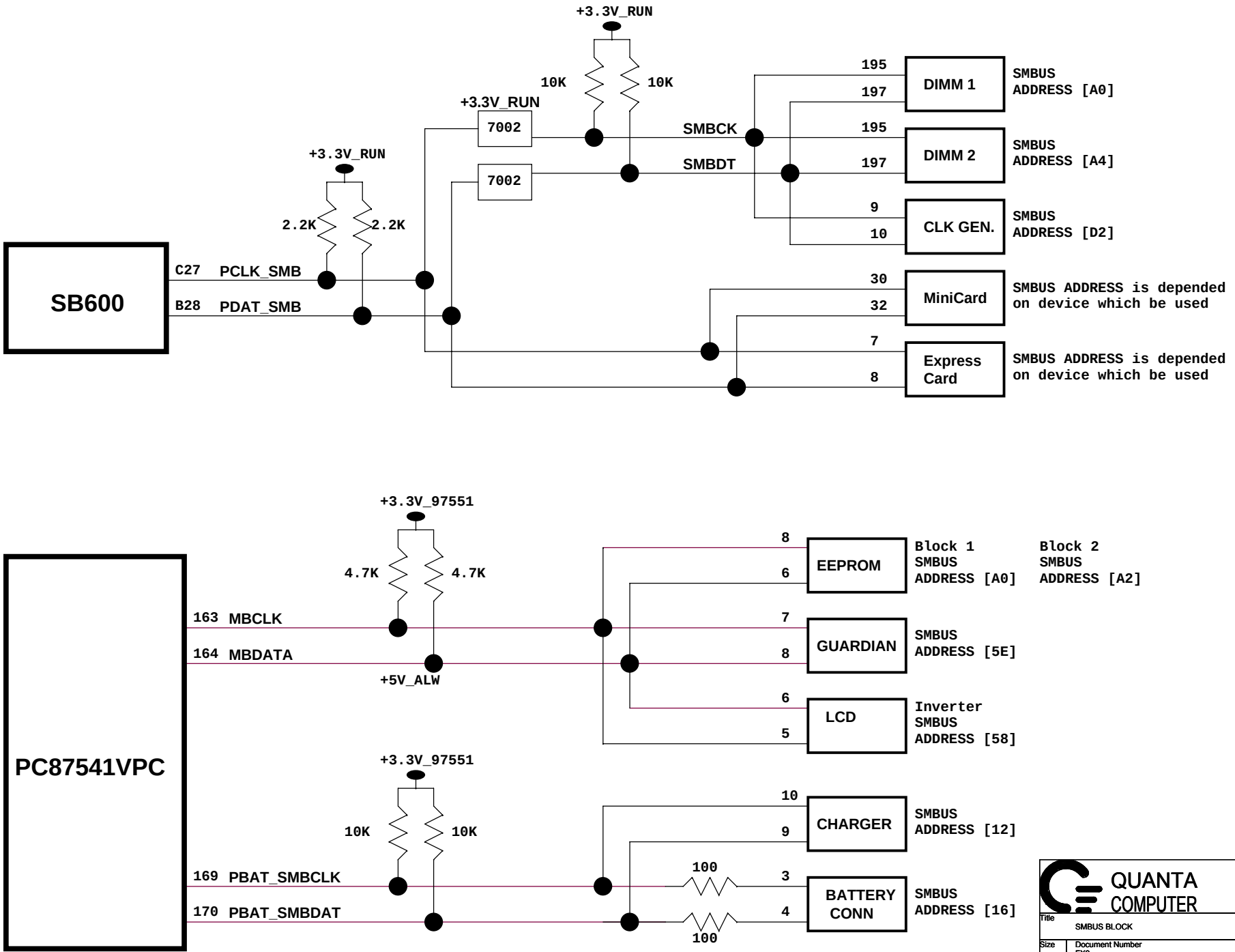
Date: Thursday, September 07, 2006	Sheet 44 of 51	



QUANTA COMPUTER

Title	SMBUS BLOCK	
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Date: Thursday, September 07, 2006	Sheet 45 of 51	