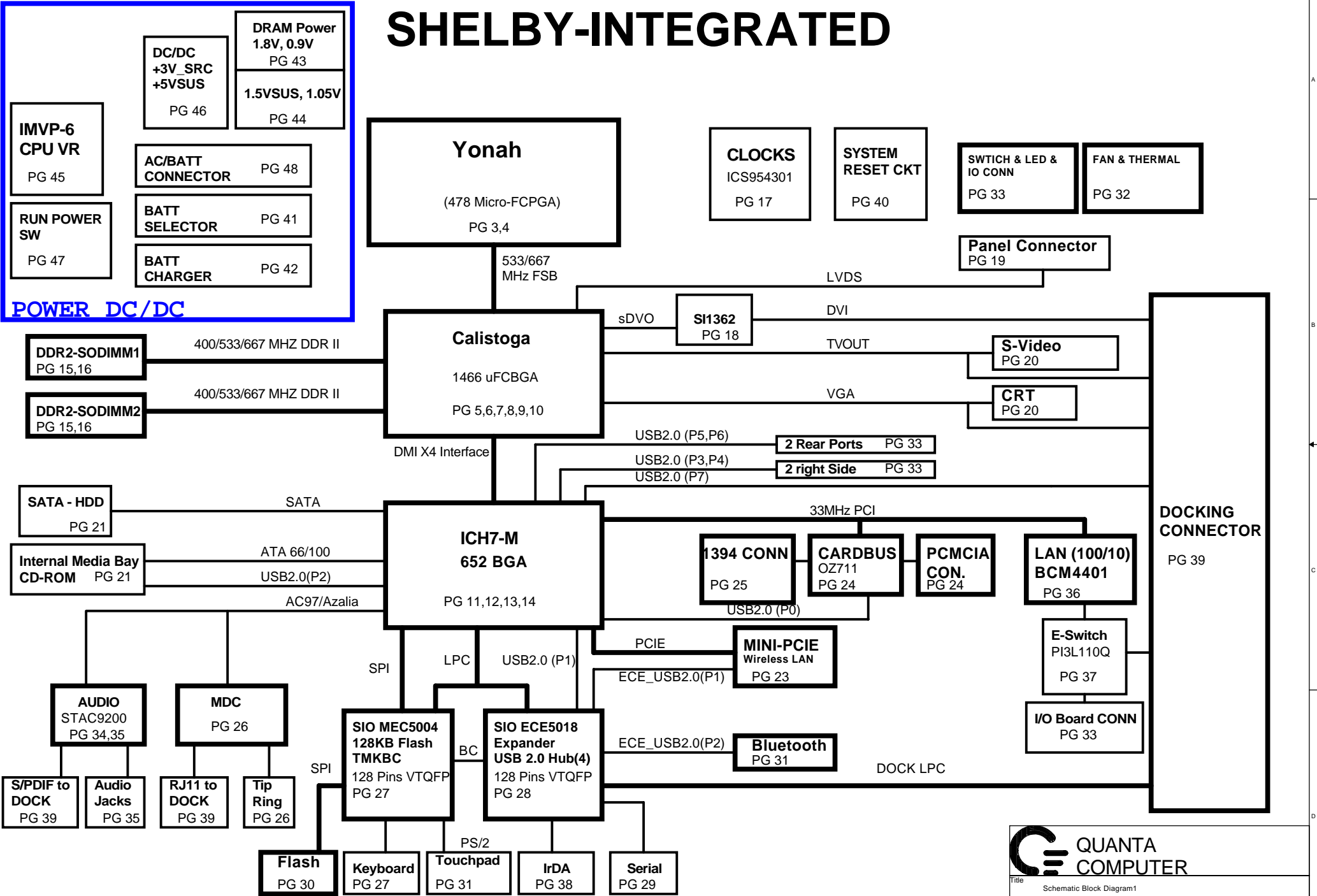
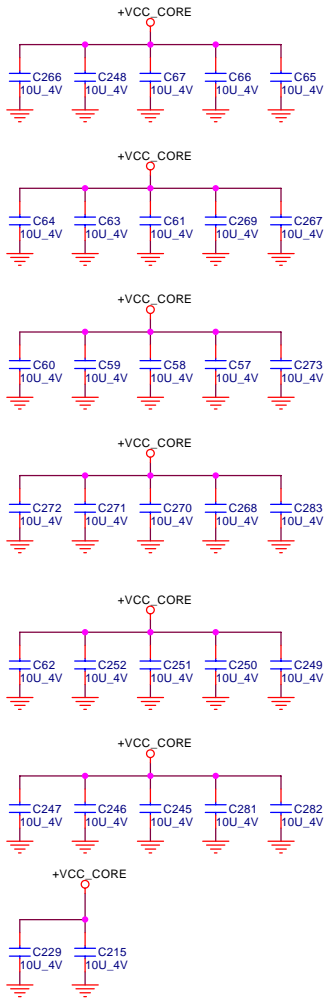


# SHELBY-INTEGRATED

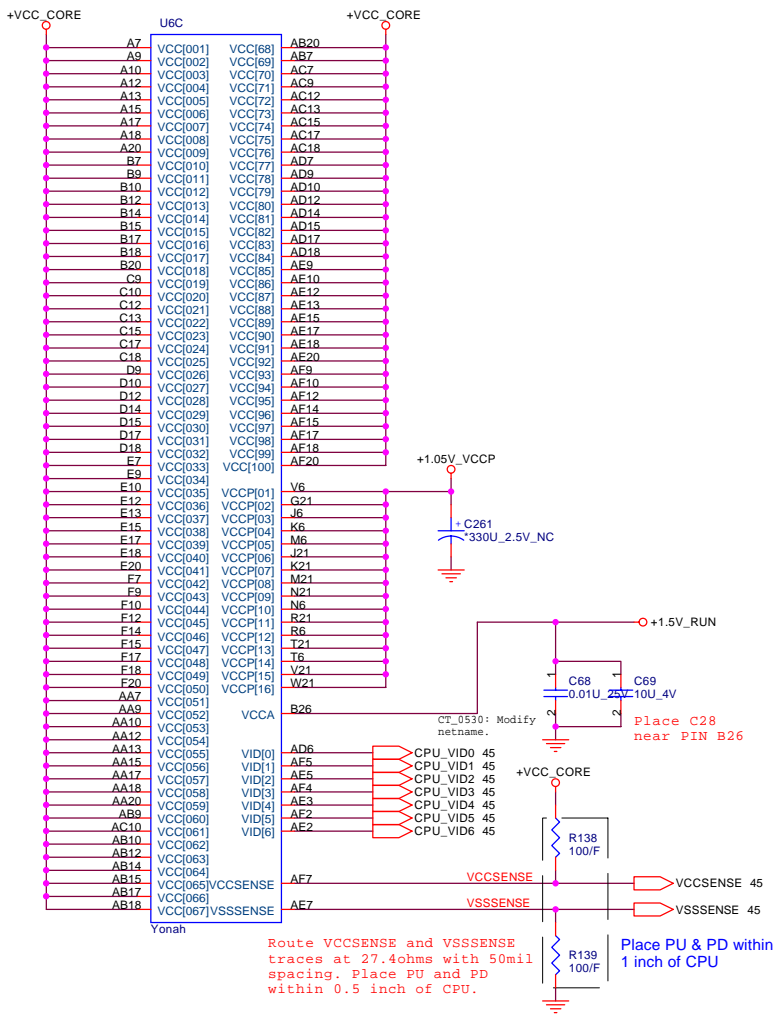
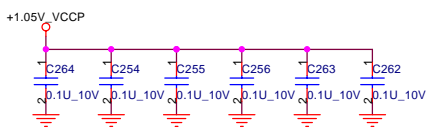




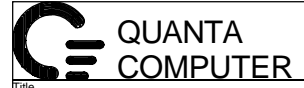
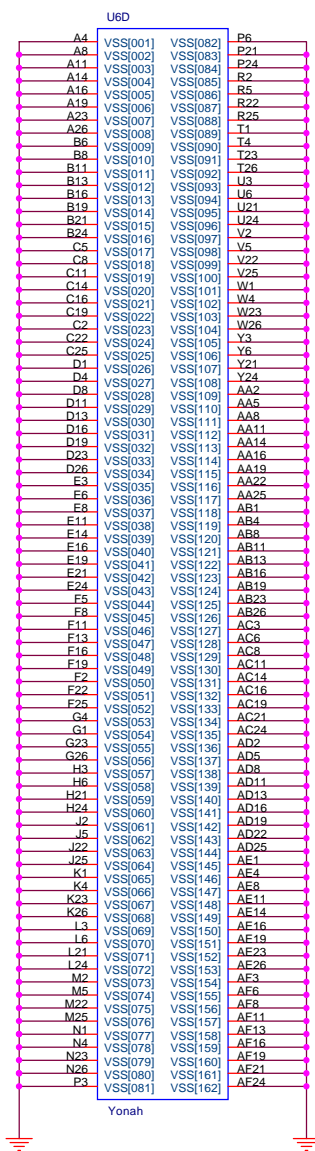




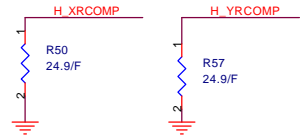
22uF 0805 X6S->105 degree C  
 8 inside cavity north side secondary layer, 8 inside cavity south side secondary layer, 6 inside cavity north side primary layer, 6 inside cavity south side primary layer.



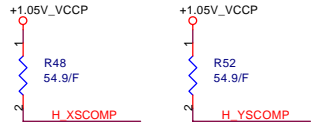
Route VCCSENSE and VSSSENSE traces at 27.4ohms with 50mil spacing. Place PU and PD within 0.5 inch of CPU.



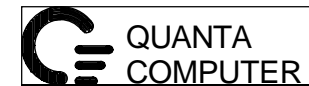
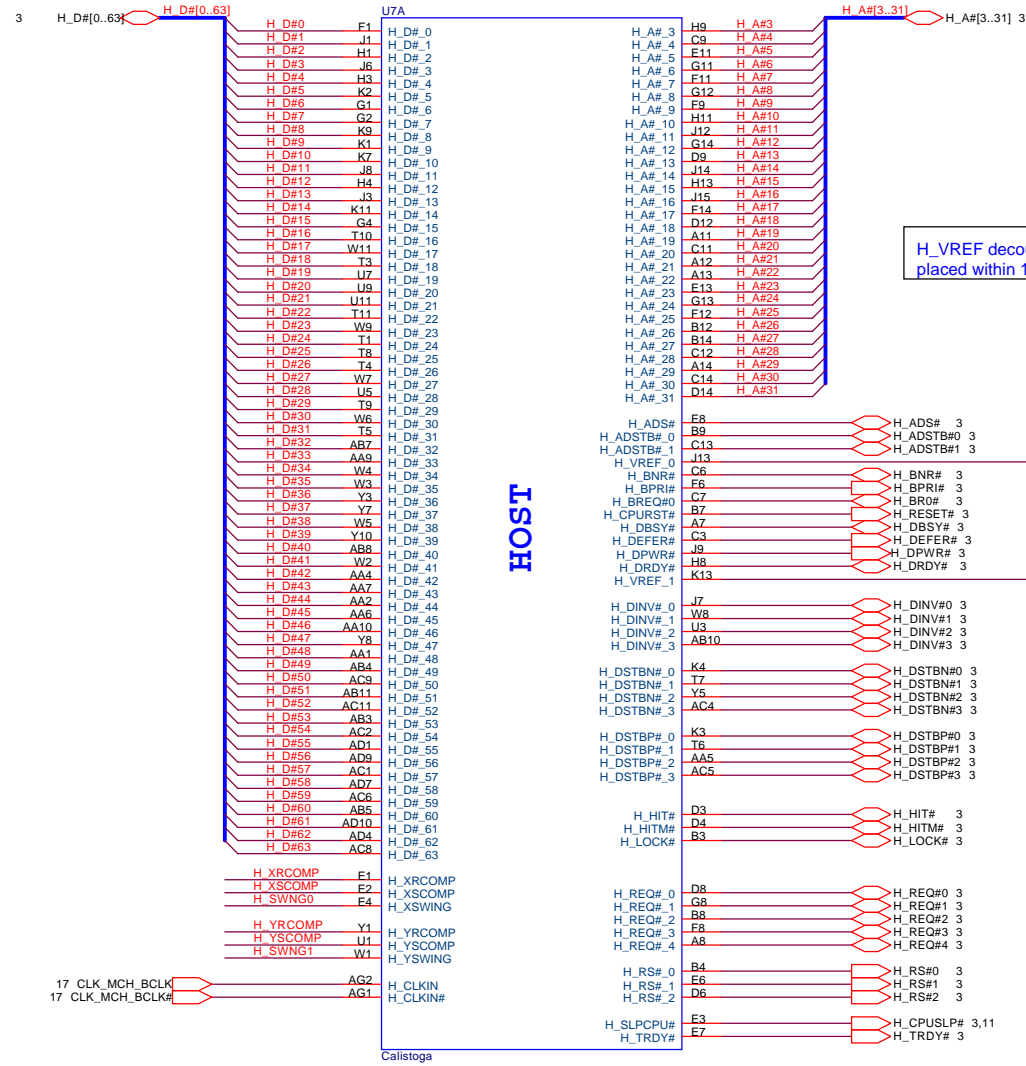
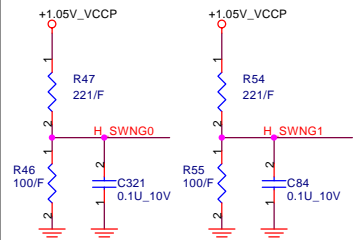
Layout note: H\_XRCOMP & H\_YRCOMP trace width and spacing is 10/20 mil



Layout note: H\_YSCOMP & H\_XSCOMP resistor should be less than 0.5" inch.

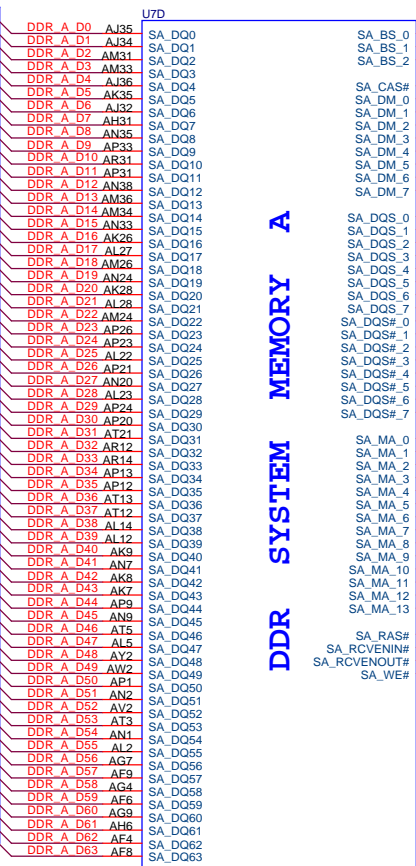


H\_SWING0, H\_SWING1 should be 10mil wide & 20mil spacing.  
H\_SWING0, H\_SWING1 Resistors & Caps should be placed within 0.5"



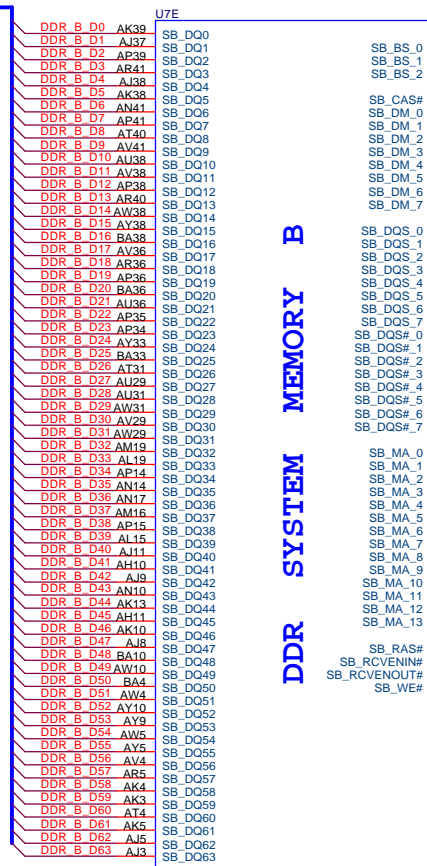


15 DDR\_A\_D[0..63]

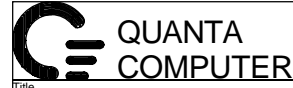


Calistoga

15 DDR\_B\_D[0..63]

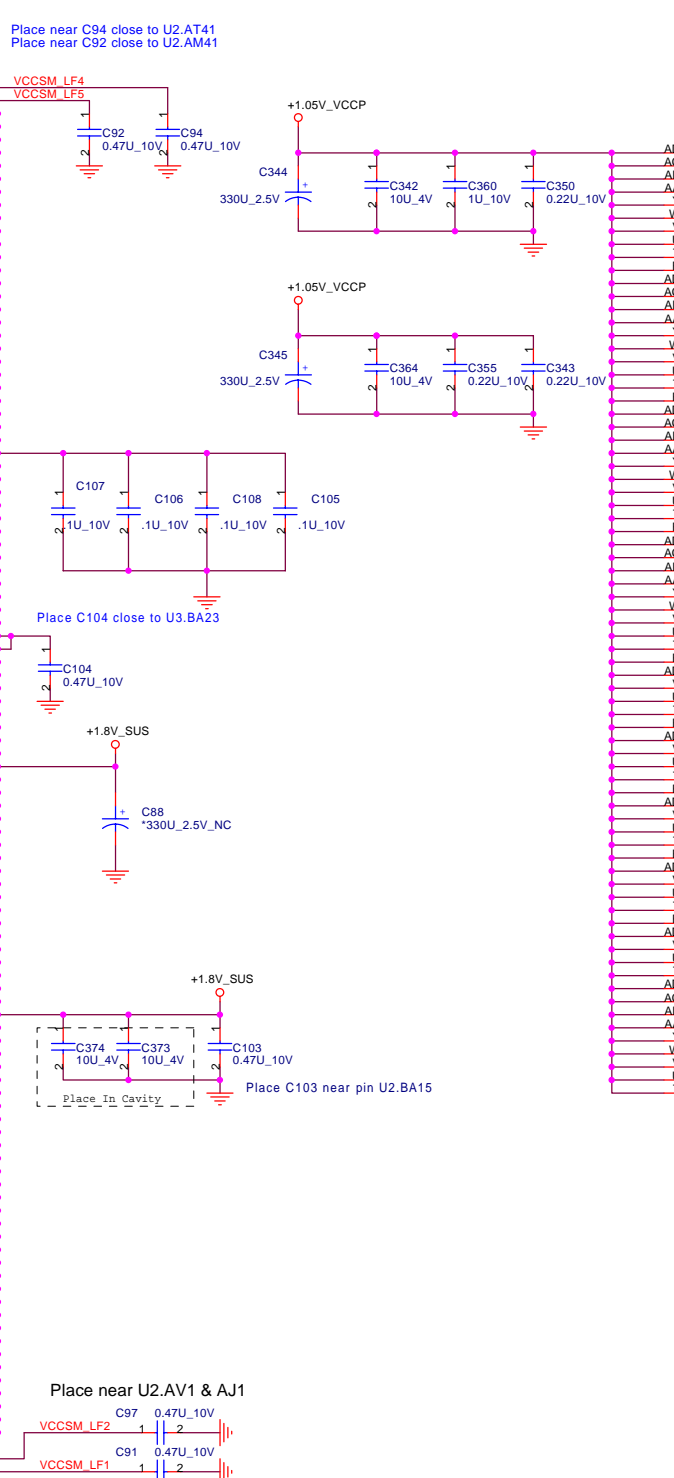


Calistoga



AA33	VCC 0
W33	VCC 1
P33	VCC 2
N33	VCC 3
L33	VCC 4
AA32	VCC 5
Y32	VCC 6
W32	VCC 7
V32	VCC 8
P32	VCC 9
N32	VCC 10
M32	VCC 11
L32	VCC 12
J32	VCC 13
AA31	VCC 14
W31	VCC 15
Y31	VCC 16
T31	VCC 17
R31	VCC 18
P31	VCC 19
N31	VCC 20
M31	VCC 21
AA30	VCC 22
Y30	VCC 23
W30	VCC 24
V30	VCC 25
P30	VCC 26
N30	VCC 27
M30	VCC 28
L30	VCC 29
AA29	VCC 30
Y29	VCC 31
W29	VCC 32
V29	VCC 33
P29	VCC 34
N29	VCC 35
M29	VCC 36
L29	VCC 37
AA28	VCC 38
Y28	VCC 39
W28	VCC 40
V28	VCC 41
P28	VCC 42
N28	VCC 43
M28	VCC 44
L28	VCC 45
AA27	VCC 46
Y27	VCC 47
W27	VCC 48
V27	VCC 49
P27	VCC 50
N27	VCC 51
M27	VCC 52
L27	VCC 53
P26	VCC 54
N26	VCC 55
L26	VCC 56
N25	VCC 57
M25	VCC 58
L25	VCC 59
P24	VCC 60
N24	VCC 61
M24	VCC 62
AB23	VCC 63
AA23	VCC 64
Y23	VCC 65
N23	VCC 66
M23	VCC 67
L23	VCC 68
AC22	VCC 69
AB22	VCC 70
Y22	VCC 71
W22	VCC 72
P22	VCC 73
N22	VCC 74
M22	VCC 75
L22	VCC 76
AC21	VCC 77
AA21	VCC 78
W21	VCC 79
N21	VCC 80
M21	VCC 81
L21	VCC 82
AC20	VCC 83
AB20	VCC 84
Y20	VCC 85
W20	VCC 86
P20	VCC 87
N20	VCC 88
M20	VCC 89
L20	VCC 90
AB19	VCC 91
AA19	VCC 92
Y19	VCC 93
N19	VCC 94
M19	VCC 95
L19	VCC 96
N18	VCC 97
M18	VCC 98
L18	VCC 99
P17	VCC 100
N17	VCC 101
M17	VCC 102
L16	VCC 103
M16	VCC 104
VCC 105	VCC 105
VCC 106	VCC 106
VCC 107	VCC 107
VCC 108	VCC 108
VCC 109	VCC 109
VCC 110	VCC 110

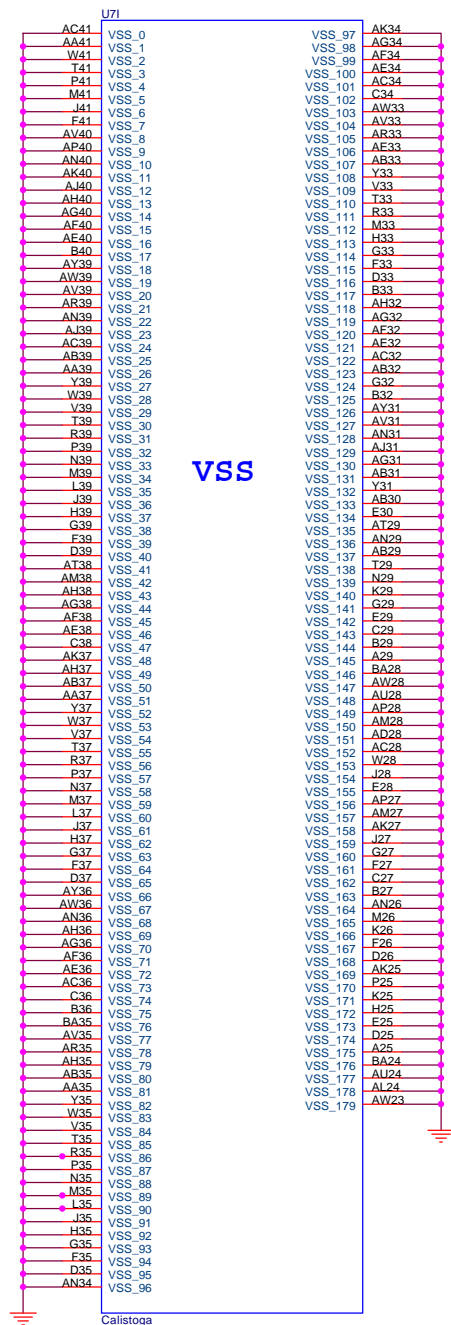
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VCC_SM_1	AM41
VCC_SM_2	AL40
VCC_SM_3	BA34
VCC_SM_4	AY34
VCC_SM_5	AW34
VCC_SM_6	AV34
VCC_SM_7	AU34
VCC_SM_8	AT34
VCC_SM_9	AR34
VCC_SM_10	BA30
VCC_SM_11	AY30
VCC_SM_12	AW30
VCC_SM_13	AV30
VCC_SM_14	AU30
VCC_SM_15	AT30
VCC_SM_16	AR30
VCC_SM_17	AN30
VCC_SM_18	AM29
VCC_SM_19	AL29
VCC_SM_20	AK29
VCC_SM_21	AJ29
VCC_SM_22	AH29
VCC_SM_23	AJ28
VCC_SM_24	AH28
VCC_SM_25	AJ27
VCC_SM_26	AH27
VCC_SM_27	AY26
VCC_SM_28	AW26
VCC_SM_29	AV26
VCC_SM_30	AU26
VCC_SM_31	AT26
VCC_SM_32	AJ26
VCC_SM_33	AH26
VCC_SM_34	AJ25
VCC_SM_35	AH25
VCC_SM_36	AJ24
VCC_SM_37	AH24
VCC_SM_38	BA23
VCC_SM_39	AJ23
VCC_SM_40	BA22
VCC_SM_41	AY22
VCC_SM_42	AW22
VCC_SM_43	AV22
VCC_SM_44	AU22
VCC_SM_45	AT22
VCC_SM_46	AR22
VCC_SM_47	AN22
VCC_SM_48	AM22
VCC_SM_49	AL22
VCC_SM_50	AK22
VCC_SM_51	AJ22
VCC_SM_52	AH22
VCC_SM_53	AK20
VCC_SM_54	BA19
VCC_SM_55	AY19
VCC_SM_56	AW19
VCC_SM_57	AV19
VCC_SM_58	AU19
VCC_SM_59	AT19
VCC_SM_60	AR19
VCC_SM_61	AN19
VCC_SM_62	AM19
VCC_SM_63	AL19
VCC_SM_64	AK19
VCC_SM_65	AJ19
VCC_SM_66	AH19
VCC_SM_67	AJ18
VCC_SM_68	AH18
VCC_SM_69	AJ17
VCC_SM_70	AH17
VCC_SM_71	AJ16
VCC_SM_72	AH16
VCC_SM_73	BA15
VCC_SM_74	AY15
VCC_SM_75	AW15
VCC_SM_76	AV15
VCC_SM_77	AU15
VCC_SM_78	AT15
VCC_SM_79	AR15
VCC_SM_80	AN15
VCC_SM_81	AM15
VCC_SM_82	AL15
VCC_SM_83	AK15
VCC_SM_84	AJ15
VCC_SM_85	AH15
VCC_SM_86	AK12
VCC_SM_87	AJ12
VCC_SM_88	AH12
VCC_SM_89	AG12
VCC_SM_90	AK11
VCC_SM_91	BA8
VCC_SM_92	AY8
VCC_SM_93	AW8
VCC_SM_94	AV8
VCC_SM_95	AU8
VCC_SM_96	AT8
VCC_SM_97	AR8
VCC_SM_98	AN8
VCC_SM_99	AM8
VCC_SM_100	AL8
VCC_SM_101	AK8
VCC_SM_102	AJ8
VCC_SM_103	AH8
VCC_SM_104	AV6
VCC_SM_105	AW6
VCC_SM_106	AT6
VCC_SM_107	AR6
VCC_SM_108	AN6
VCC_SM_109	AM6
VCC_SM_110	AL6
VCC_SM_111	AK6
VCC_SM_112	AJ6
VCC_SM_113	AH6
VCC_SM_114	AV1
VCC_SM_115	AW1
VCC_SM_116	AT1
VCC_SM_117	AR1
VCC_SM_118	AN1
VCC_SM_119	AM1
VCC_SM_120	AL1
VCC_SM_121	AK1
VCC_SM_122	AJ1
VCC_SM_123	AH1



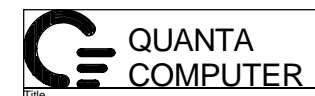
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AB27	VCC_NCTF1
AA27	VCC_NCTF2
Y27	VCC_NCTF3
W27	VCC_NCTF4
V27	VCC_NCTF5
U27	VCC_NCTF6
T27	VCC_NCTF7
R27	VCC_NCTF8
AD26	VCC_NCTF9
AC26	VCC_NCTF10
AB26	VCC_NCTF11
AA26	VCC_NCTF12
Y26	VCC_NCTF13
W26	VCC_NCTF14
V26	VCC_NCTF15
U26	VCC_NCTF16
T26	VCC_NCTF17
R26	VCC_NCTF18
AD25	VCC_NCTF19
AC25	VCC_NCTF20
AB25	VCC_NCTF21
AA25	VCC_NCTF22
Y25	VCC_NCTF23
W25	VCC_NCTF24
V25	VCC_NCTF25
U25	VCC_NCTF26
T25	VCC_NCTF27
R25	VCC_NCTF28
AD24	VCC_NCTF29
AC24	VCC_NCTF30
AB24	VCC_NCTF31
AA24	VCC_NCTF32
Y24	VCC_NCTF33
W24	VCC_NCTF34
V24	VCC_NCTF35
U24	VCC_NCTF36
T24	VCC_NCTF37
R24	VCC_NCTF38
AD23	VCC_NCTF39
AC23	VCC_NCTF40
AB23	VCC_NCTF41
AA23	VCC_NCTF42
Y23	VCC_NCTF43
W23	VCC_NCTF44
V23	VCC_NCTF45
U23	VCC_NCTF46
T23	VCC_NCTF47
R23	VCC_NCTF48
AD22	VCC_NCTF49
AC22	VCC_NCTF50
AB22	VCC_NCTF51
AA22	VCC_NCTF52
Y22	VCC_NCTF53
W22	VCC_NCTF54
V22	VCC_NCTF55
U22	VCC_NCTF56
T22	VCC_NCTF57
R22	VCC_NCTF58
AD21	VCC_NCTF59
AC21	VCC_NCTF60
AB21	VCC_NCTF61
AA21	VCC_NCTF62
Y21	VCC_NCTF63
W21	VCC_NCTF64
V21	VCC_NCTF65
U21	VCC_NCTF66
T21	VCC_NCTF67
R21	VCC_NCTF68
AD20	VCC_NCTF69
AC20	VCC_NCTF70
AB20	VCC_NCTF71
AA20	VCC_NCTF72
Y20	VCC_NCTF73
W20	VCC_NCTF74
V20	VCC_NCTF75
U20	VCC_NCTF76
T20	VCC_NCTF77
R20	VCC_NCTF78
AD19	VCC_NCTF79
AC19	VCC_NCTF80
AB19	VCC_NCTF81
AA19	VCC_NCTF82
Y19	VCC_NCTF83
W19	VCC_NCTF84
V19	VCC_NCTF85
U19	VCC_NCTF86
T19	VCC_NCTF87
R19	VCC_NCTF88
AD18	VCC_NCTF89
AC18	VCC_NCTF90
AB18	VCC_NCTF91
AA18	VCC_NCTF92
Y18	VCC_NCTF93
W18	VCC_NCTF94
V18	VCC_NCTF95
U18	VCC_NCTF96
T18	VCC_NCTF97
R18	VCC_NCTF98
AD17	VCC_NCTF99
AC17	VCC_NCTF100
AB17	VCC_NCTF101
AA17	VCC_NCTF102
Y17	VCC_NCTF103
W17	VCC_NCTF104
V17	VCC_NCTF105
U17	VCC_NCTF106
T17	VCC_NCTF107
R17	VCC_NCTF108
AD16	VCC_NCTF109
AC16	VCC_NCTF110
AB16	VCC_NCTF111
AA16	VCC_NCTF112
Y16	VCC_NCTF113
W16	VCC_NCTF114
V16	VCC_NCTF115
U16	VCC_NCTF116
T16	VCC_NCTF117
R16	VCC_NCTF118
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AC15	VCC_NCTF120
AB15	VCC_NCTF121
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AA13	VCC_NCTF142
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R12	VCC_NCTF158
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AB11	VCC_NCTF161
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T11	VCC_NCTF167
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AB1	VCC_NCTF261
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Y1	VCC_NCTF263
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T0	VCC_NCTF277
R0	VCC_NCTF278
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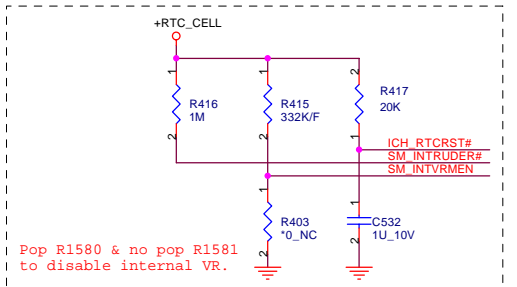
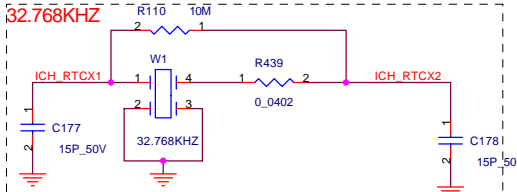




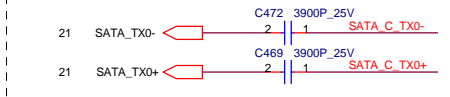
VSS



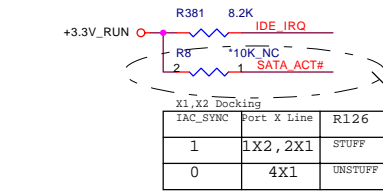
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Calistoga (VSS,NCTF)		
Size	Document Number	Rev
Custom	DM5	1A
Date:	星期二, 十二月 27, 2005	Sheet 10 of 59



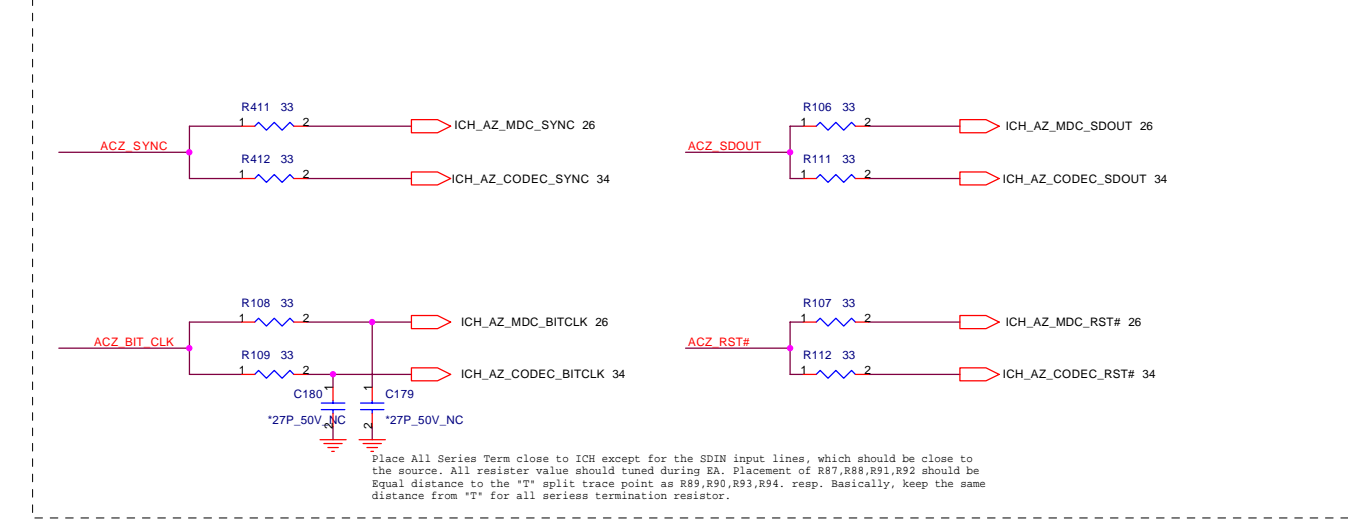
Pop R1580 & no pop R1581 to disable internal VR.



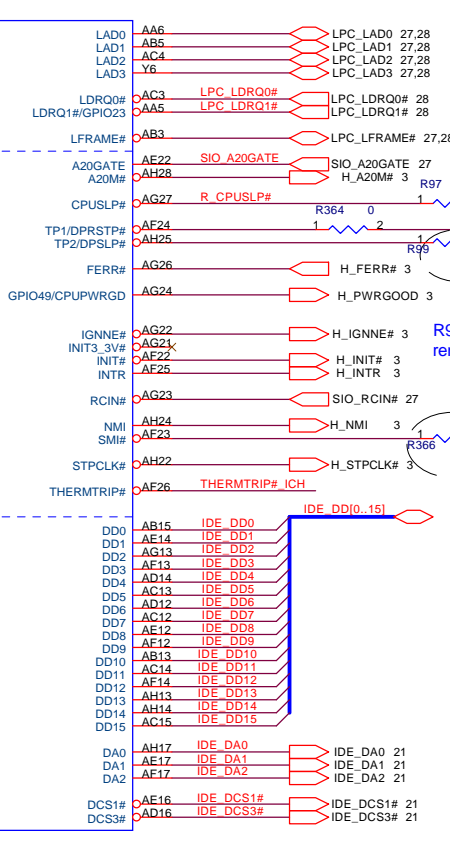
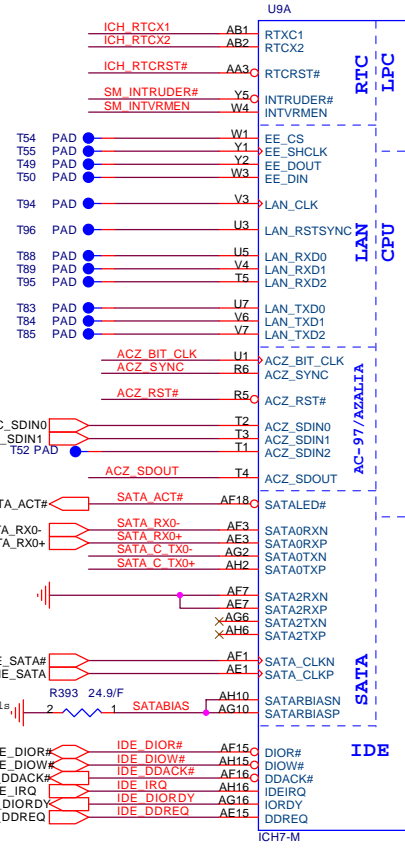
Distance between the ICH-7 M and cap on the 'P' signal should be identical distance between the ICH-6 M and cap on the 'N' signal for same pair.



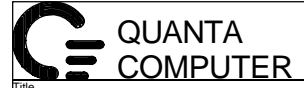
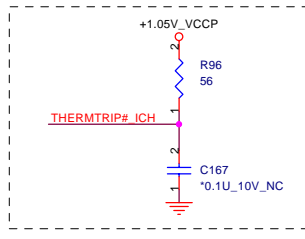
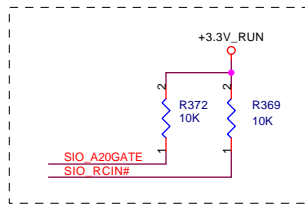
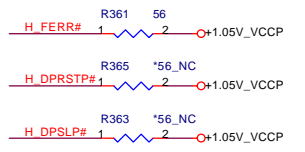
R8 can be removed on RTS

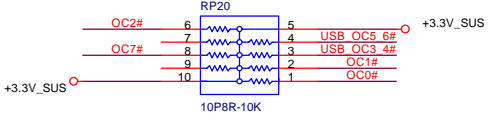
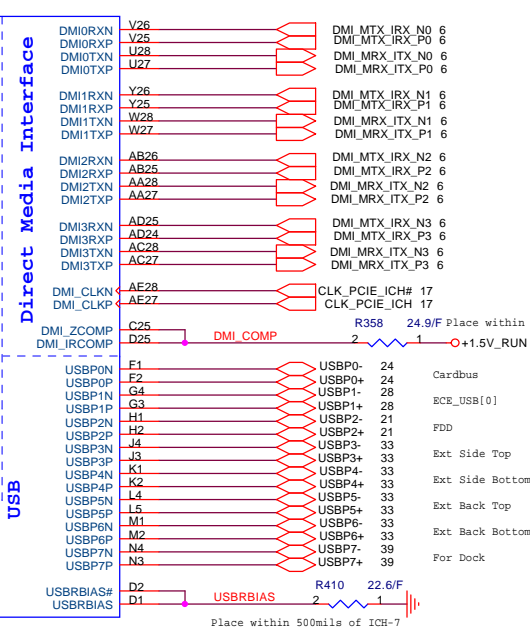
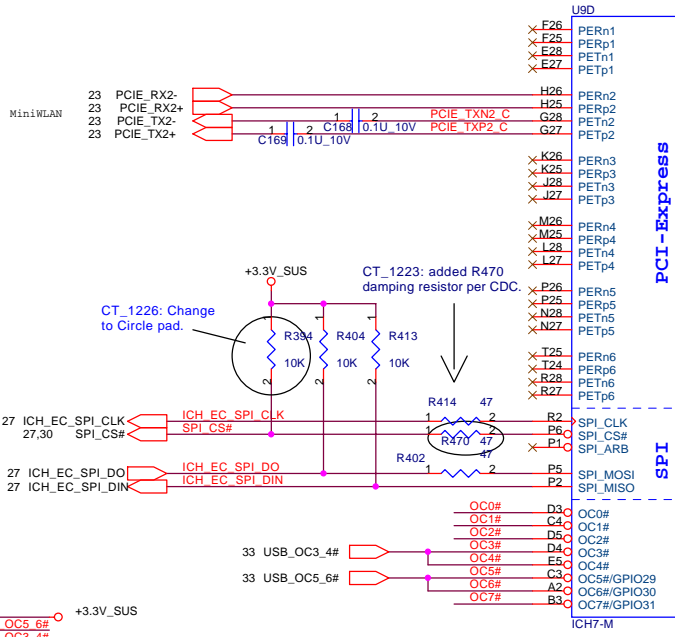


Place All Series Term close to ICH except for the SDIN input lines, which should be close to the source. All resistor value should tuned during EA. Placement of R87,R88,R91,R92 should be Equal distance to the "T" split trace point as R89,R90,R93,R94. resp. Basically, keep the same distance from "T" for all series termination resistor.



R99 & R366 can be removed on RTS

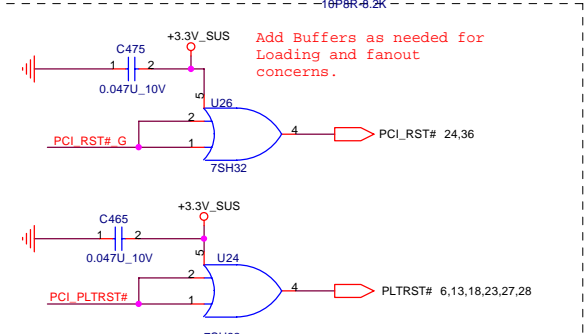
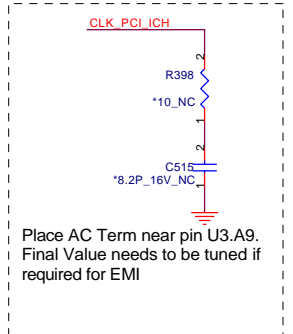
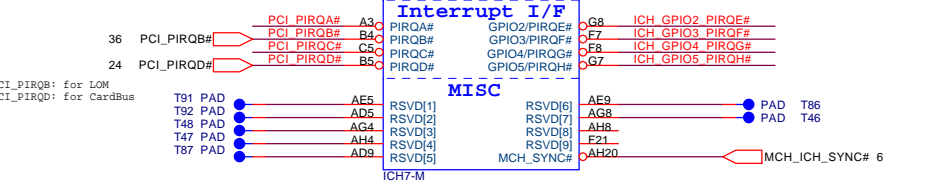
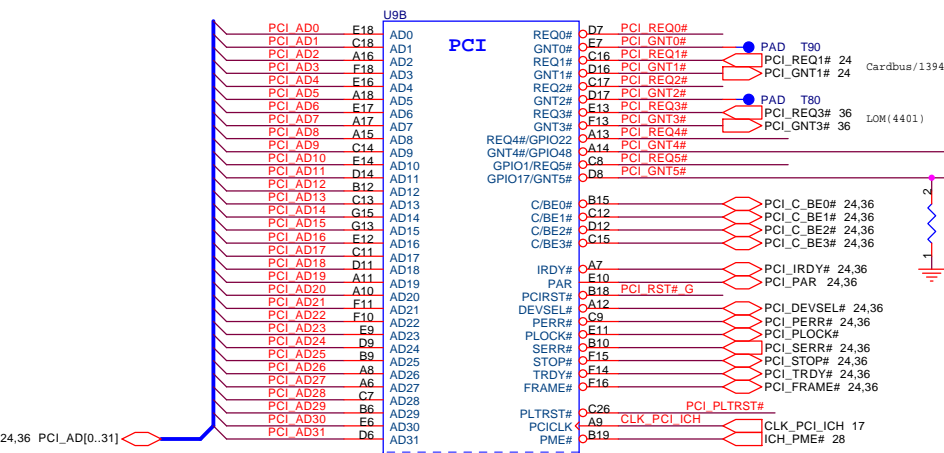




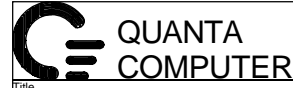
R331 NP boot from FW, populate boot from MiniPCI.

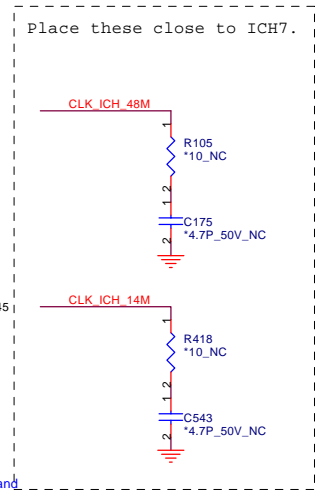
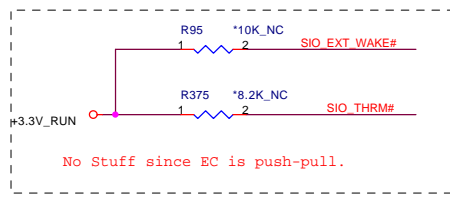
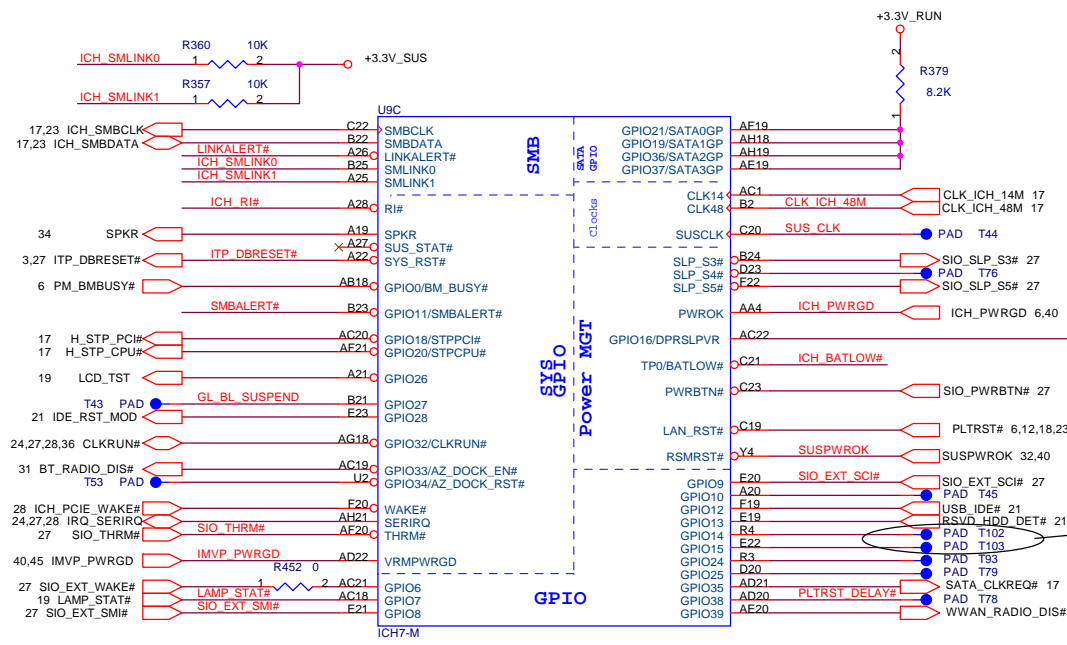
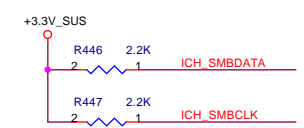
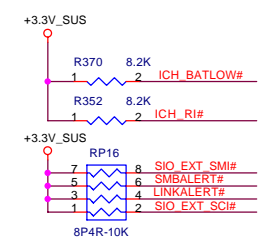
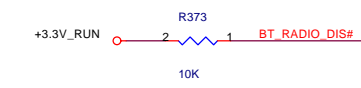
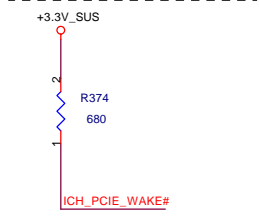
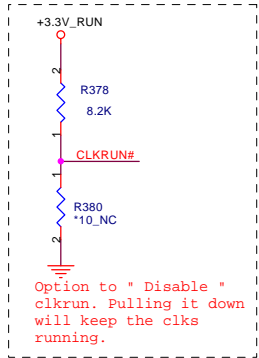
REQ0 : DOCKING  
REQ1 : Card Bus  
REQ4 : BroadCOM LAN

	GNT5#	GNT4#
LPC 11	No stuff	No stuff
PCI 10	No stuff	Stuff
SPI 01	Stuff	No stuff

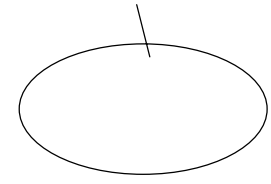


DOCK	REQ0	GNT0	PIRQA
Cardbus or Cardbus/1394	REQ1	GNT1	PIRQD
1394/MediaCard	REQ2	GNT2	PIRQC
LOM(4401)	REQ3	GNT3	PIRQB



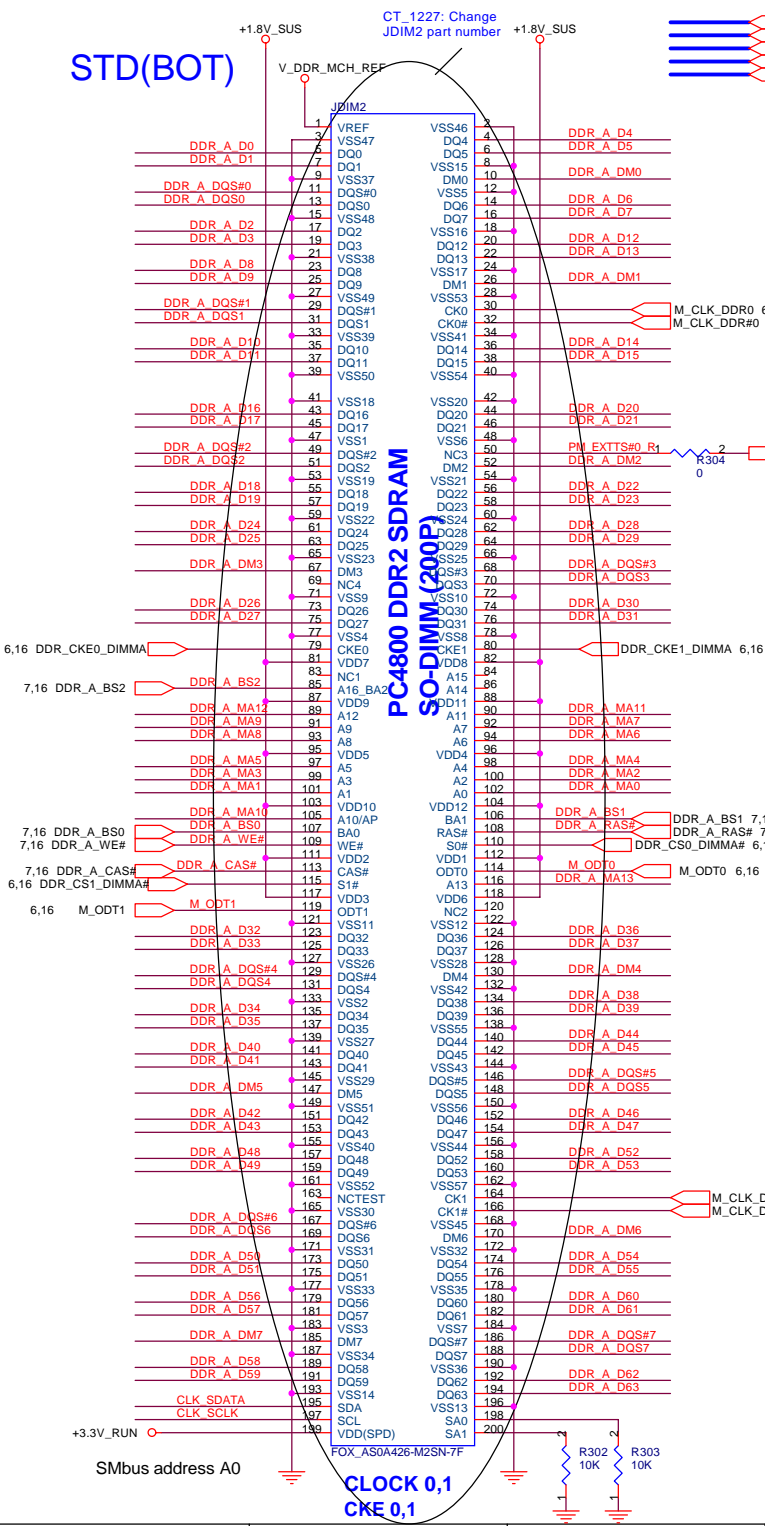


CT\_1212: Removed HDDC\_EN# and MODC\_EN# from ICH7 GPIO14 & 15. Removed R463, R464 100Kohm.

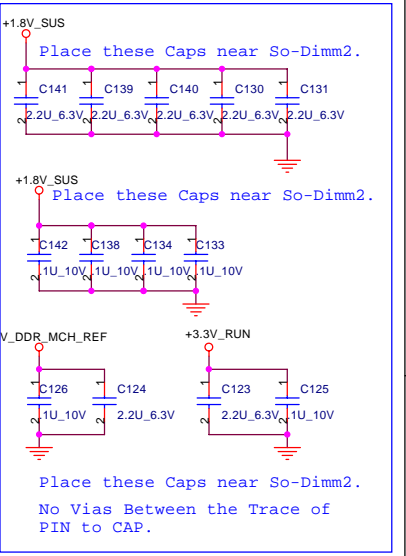
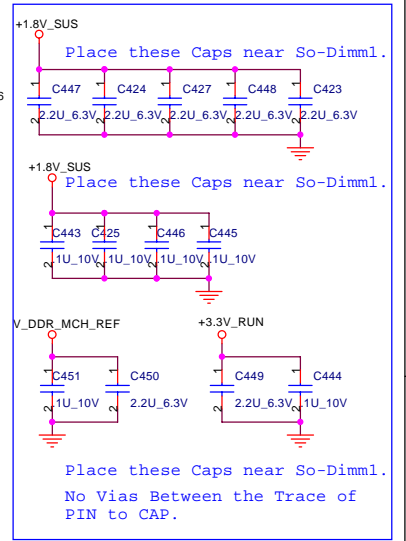
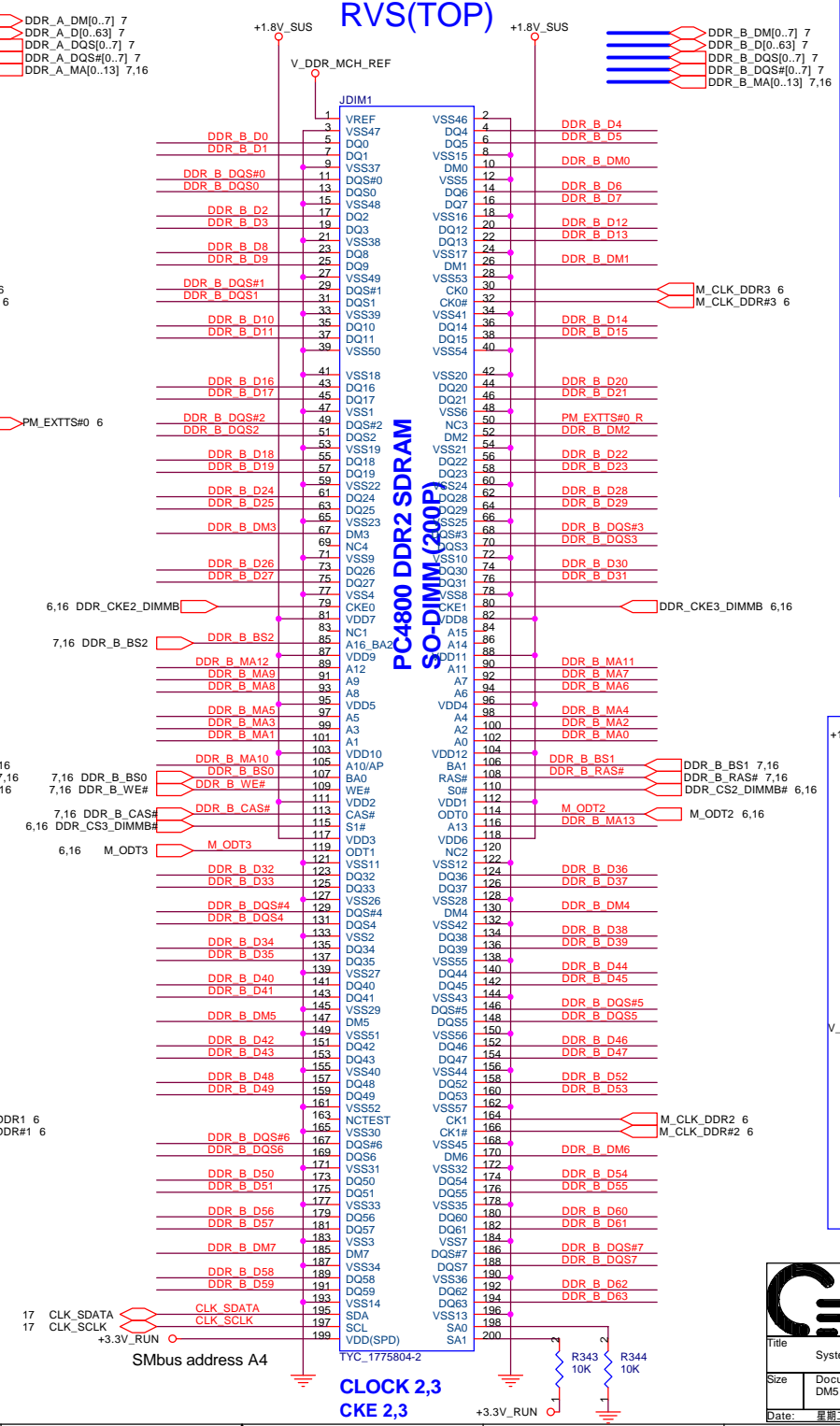




# STD(BOT)



# RVS(TOP)



**QUANTA COMPUTER**

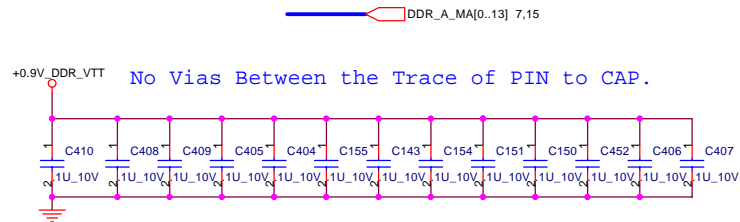
Title: System DRAM Expansion (200P-DDR\_SODIMM X 2)

Size	Document Number	Rev
	DM5	3A

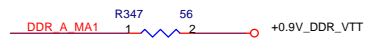
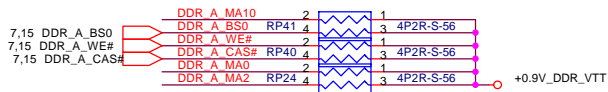
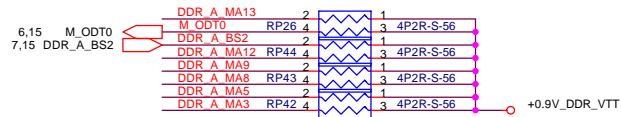
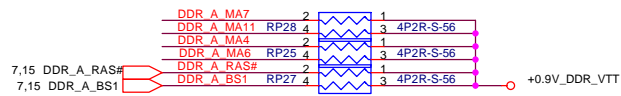
Date: 星期二, 十二月 27, 2005 Sheet 15 of 59

# DDRII DUAL CHANNEL A,B.

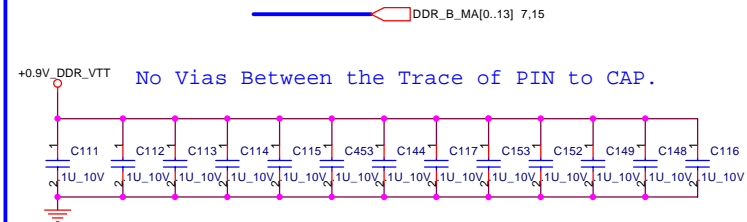
## DDRII A CHANNEL



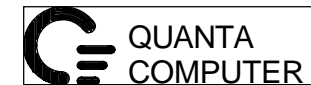
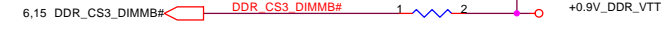
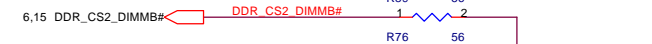
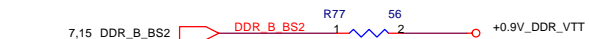
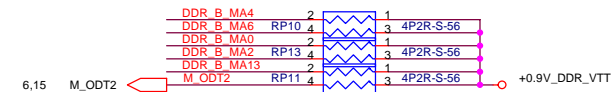
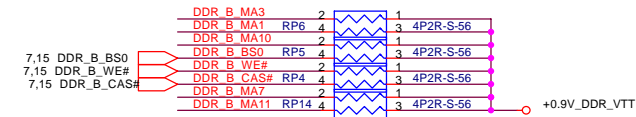
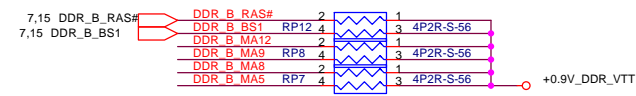
Layout note: Place 1 cap close to every 1 R-pack terminated to +0.9V\_DDR\_VTT.



## DDRII B CHANNEL



Layout note: Place 1 cap close to every 1 R-pack terminated to +0.9V\_DDR\_VTT.



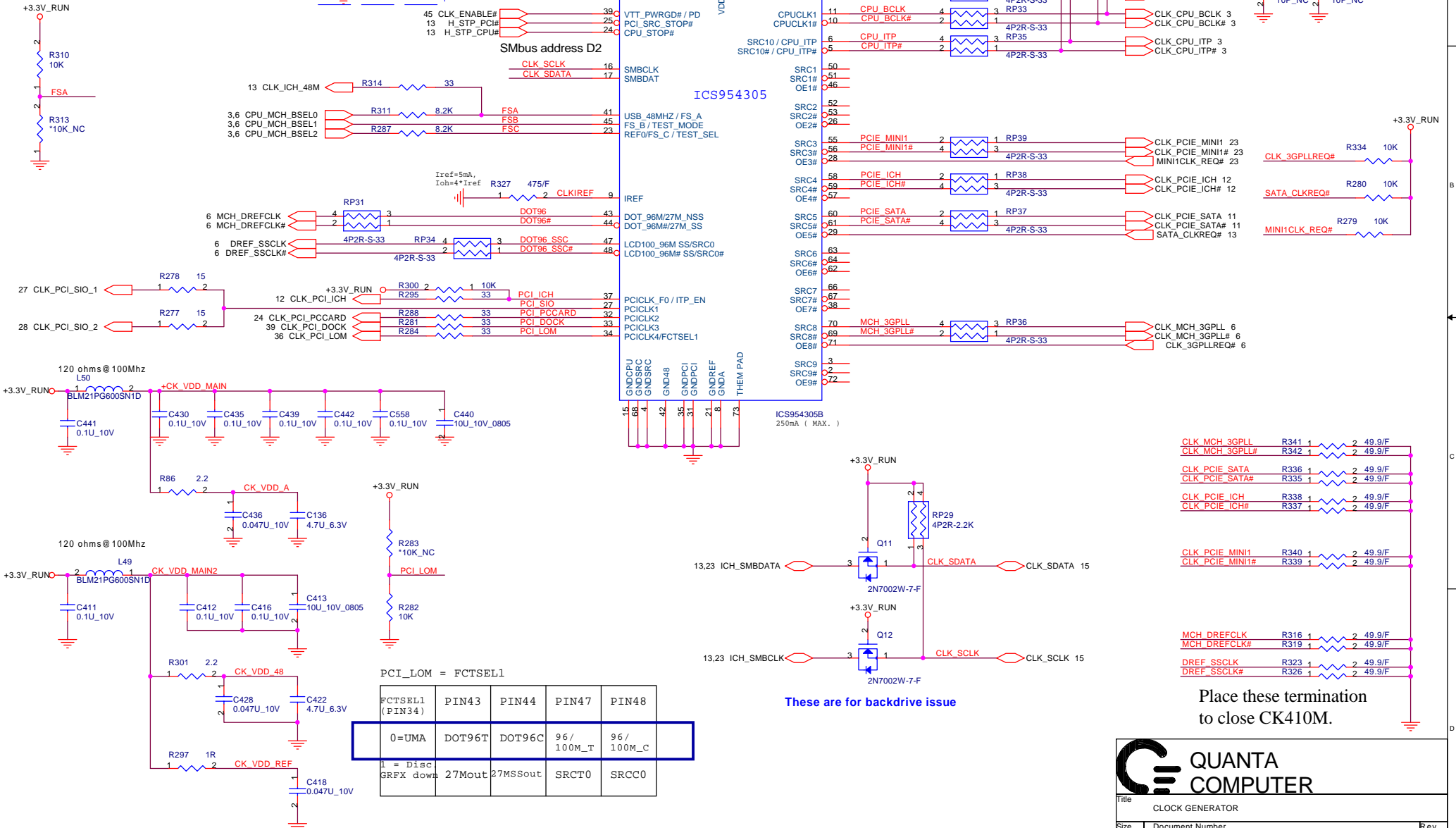
Title DDR.RES.ARRAY		
Size DM5	Document Number DM5	Rev 1A
Date: 星期二, 十二月 27, 2005	Sheet 16	of 59



FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

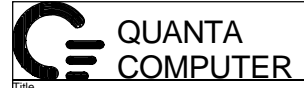
Close to Clock GEN.

Place these termination to close CK410M.

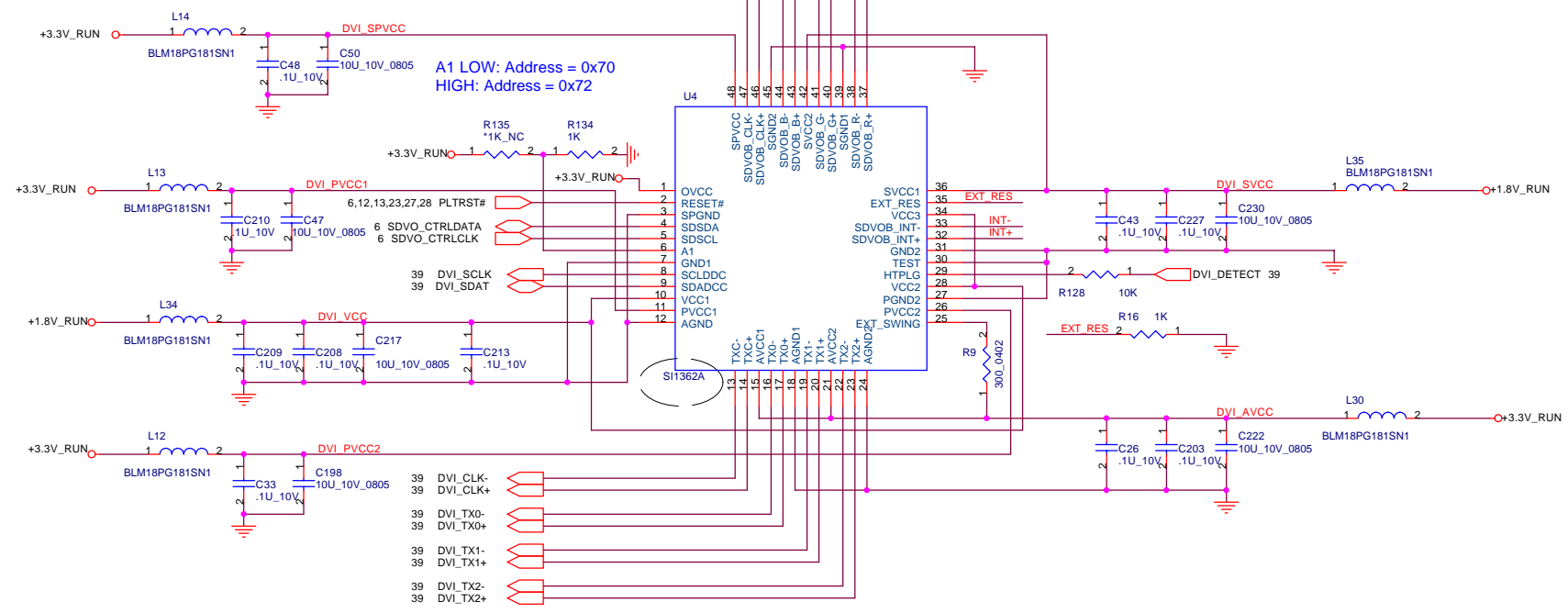
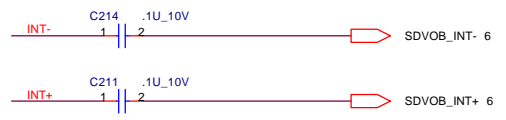
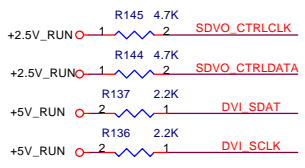


These are for backdrive issue

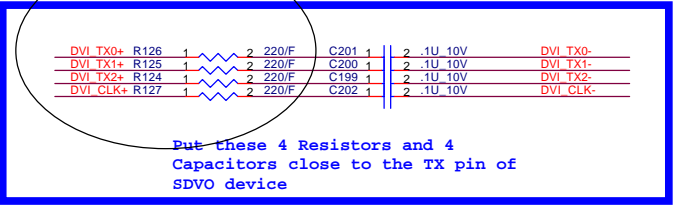
Place these termination to close CK410M.



Placed this Bypass capacitor close to OVCC.



CT\_1227: Change U4 from 1362 to 1362A. Change R124-R127 from 110/F to 220/F ohm.



QUANTA COMPUTER

Title: SIL 1362 DVI

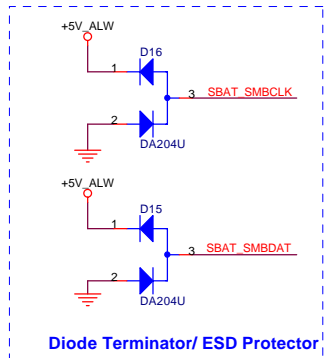
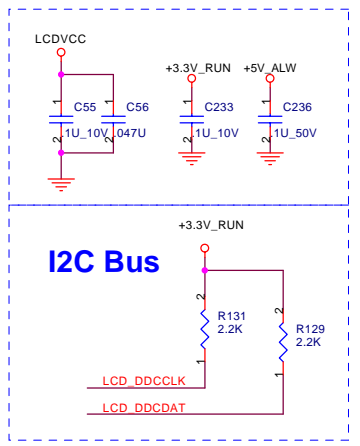
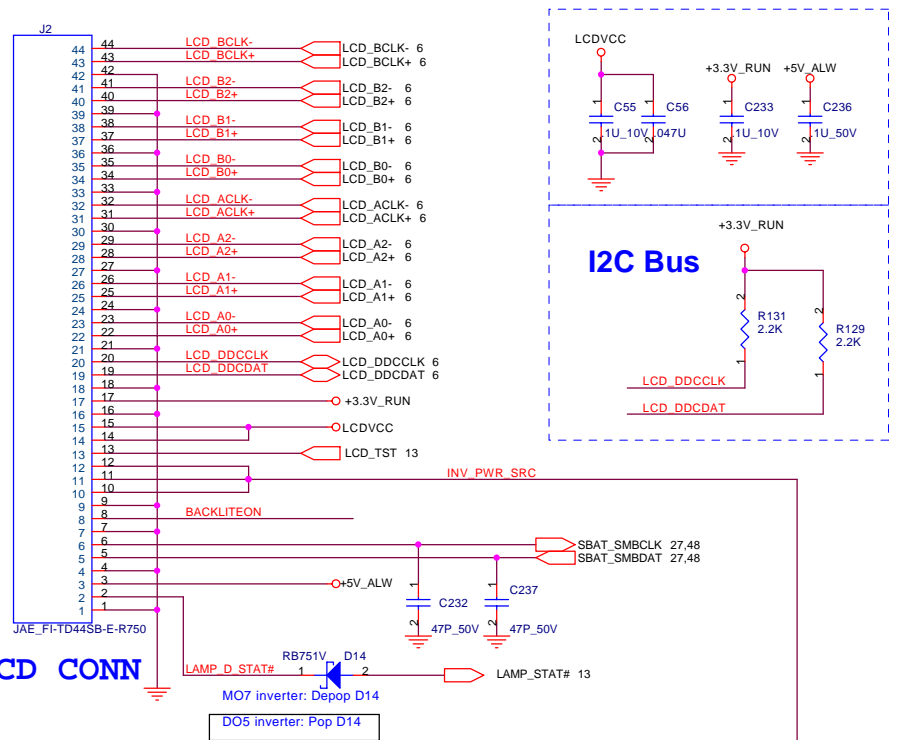
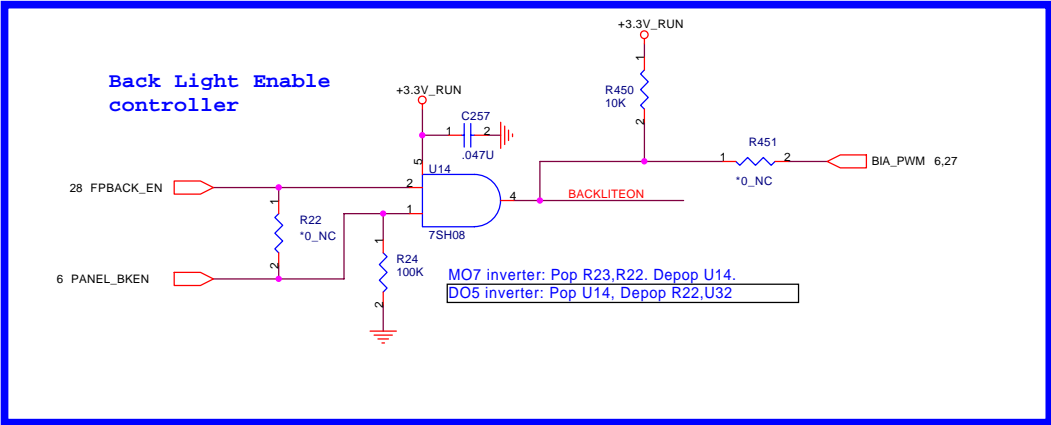
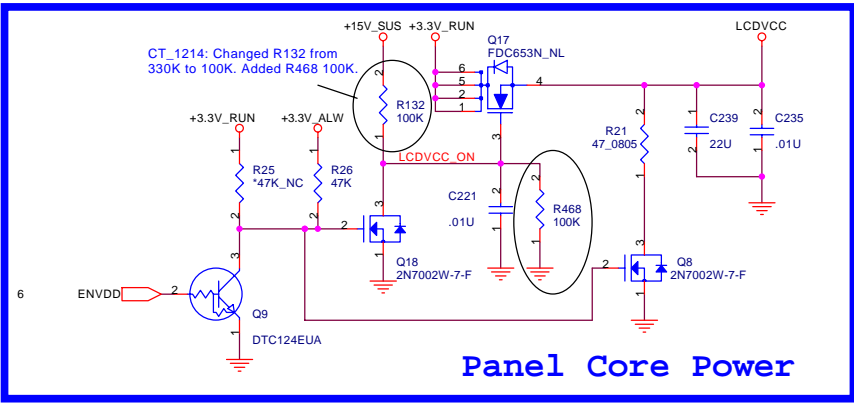
Size: Document Number  
CusomDM5

Date: 星期三, 十二月 27, 2005

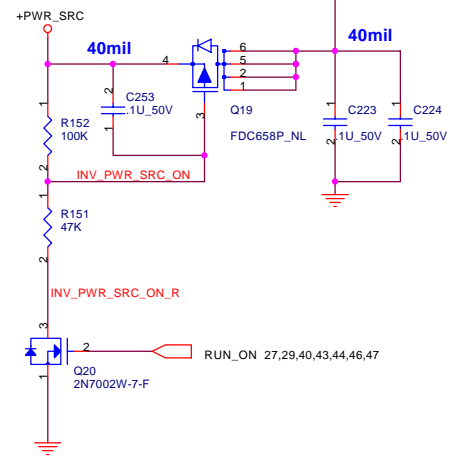
Sheet: 18 of 59

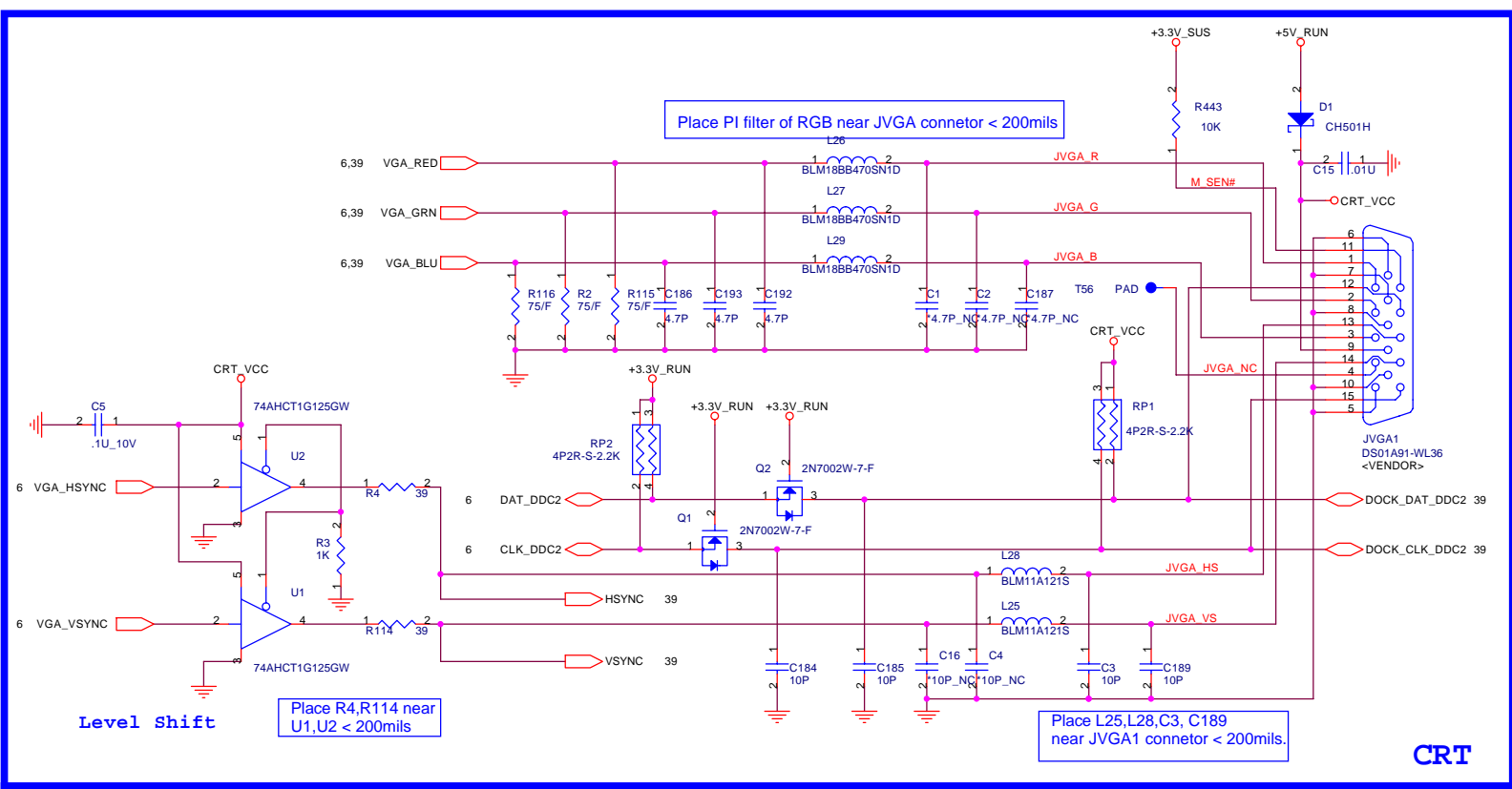
Rev: 3A

Need to apply P/N for new J2 CONN.

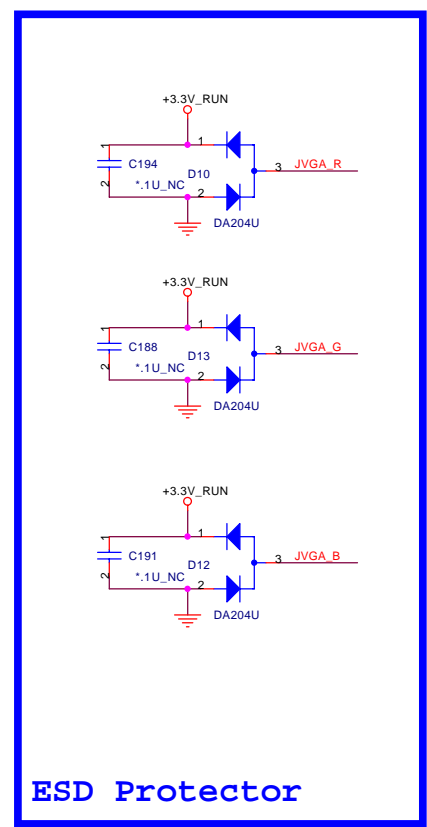


Address : A9H --Contrast  
AAH --Backlight

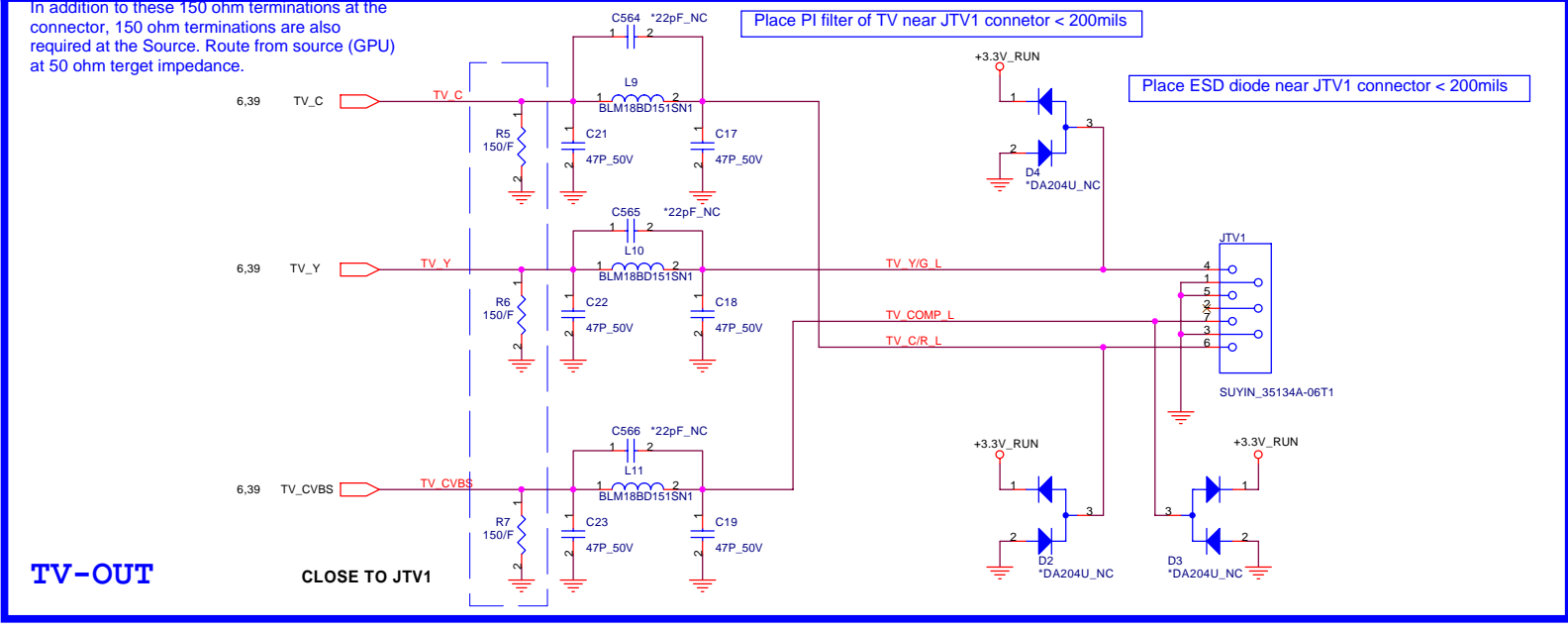




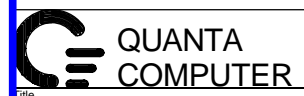
**CRT**



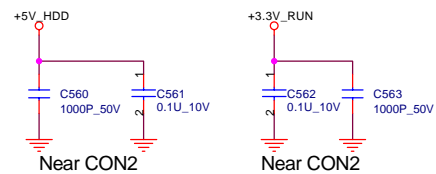
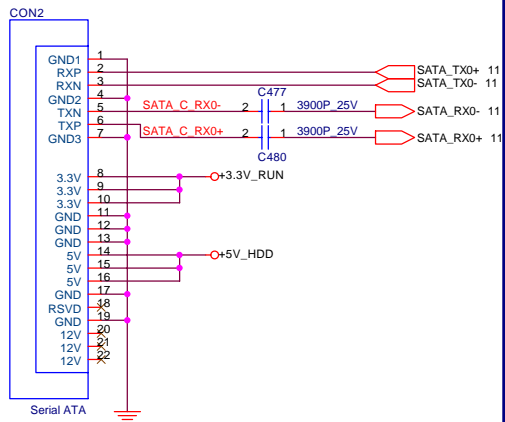
**ESD Protector**



**TV-OUT**



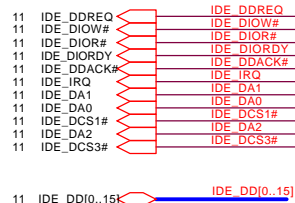
# Check SATA Footprint



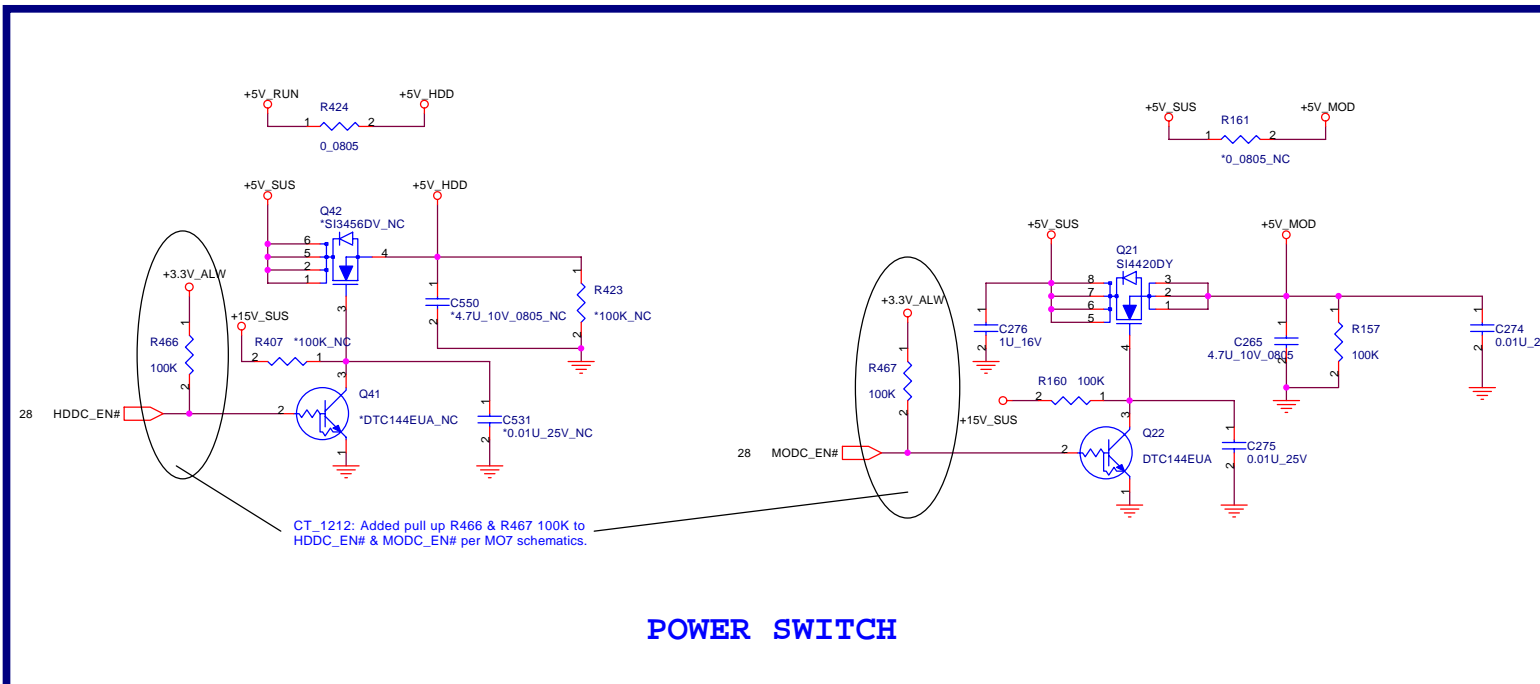
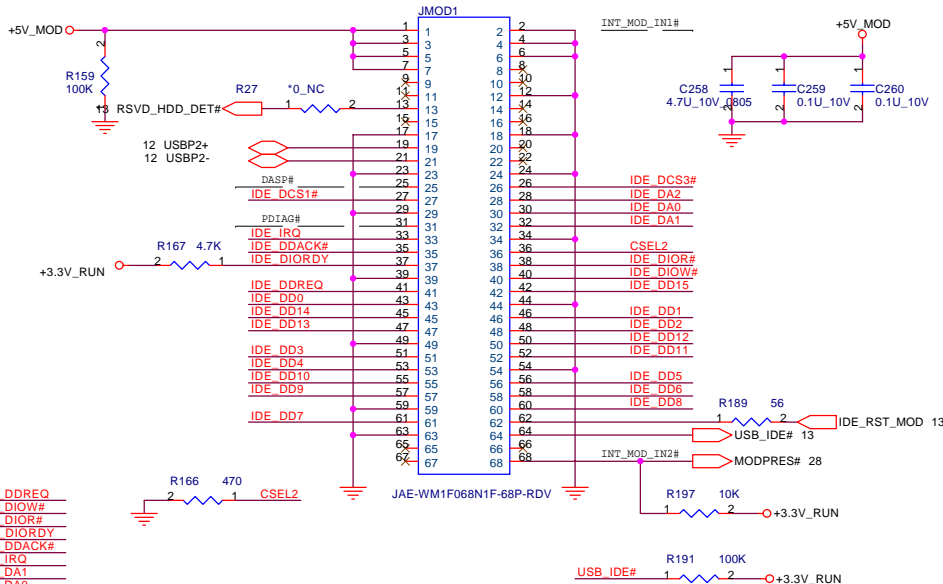
SATA HDD CONN

Near CON2

Near CON2

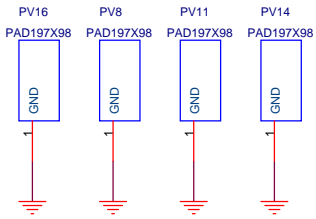


MEDIA BAY

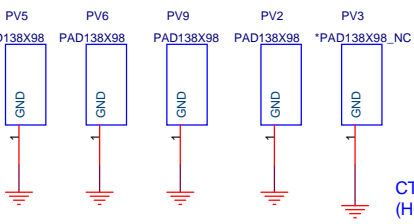
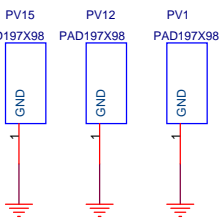
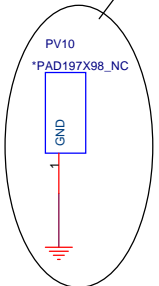
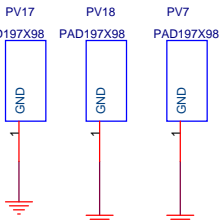
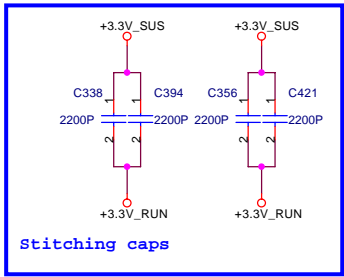


POWER SWITCH



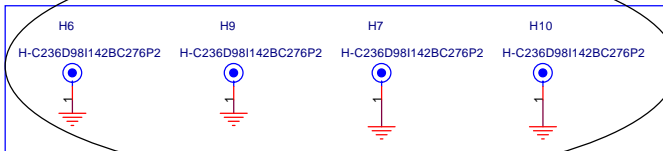


CT\_1226: Depop PV10 per mechanical request/EMI confirmed

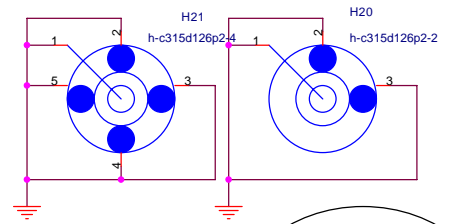
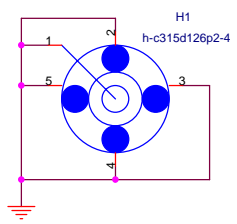
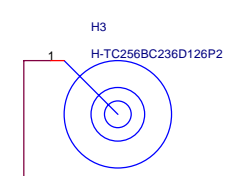
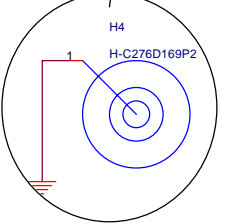
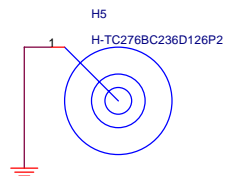
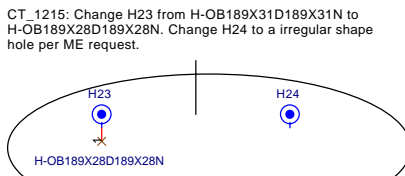


CT\_1215: Change CPU screw holes (H6,H7,H9,H10) from 2.6mm to 2.5mm.

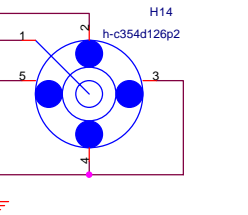
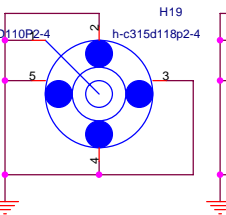
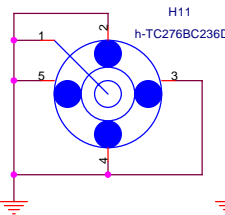
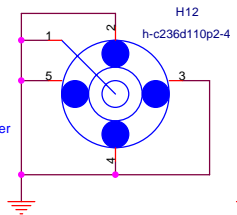
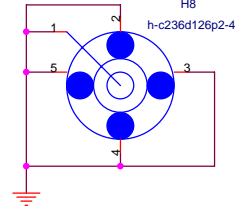
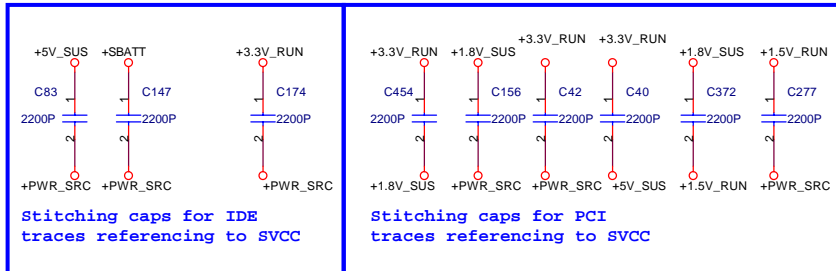
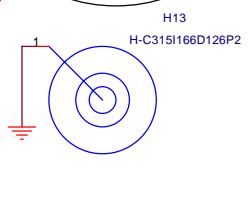
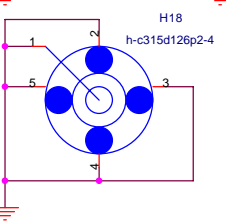
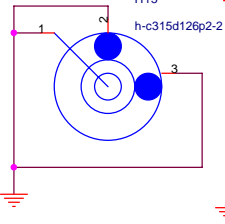
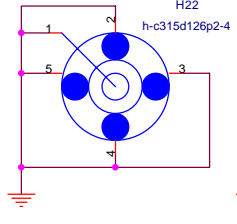
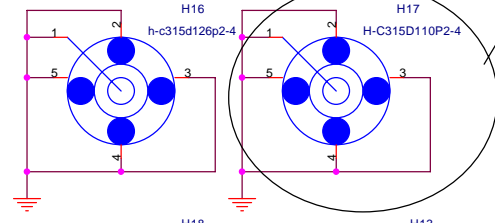
**CPU SCREW HOLES**



CT\_1215: Change H4 hole diameter from 3.9mm to 4.3 per ME.



CT\_1215: Change H17 from 3.2mm to 2.8mm.

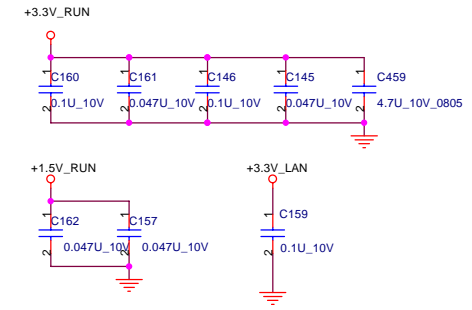
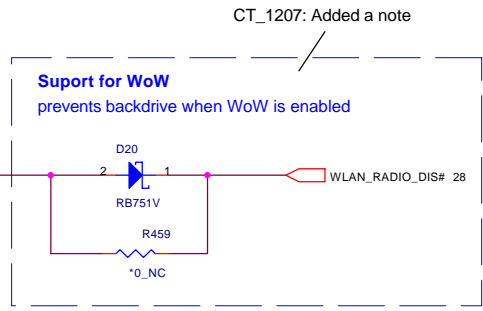
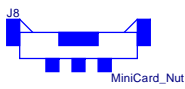
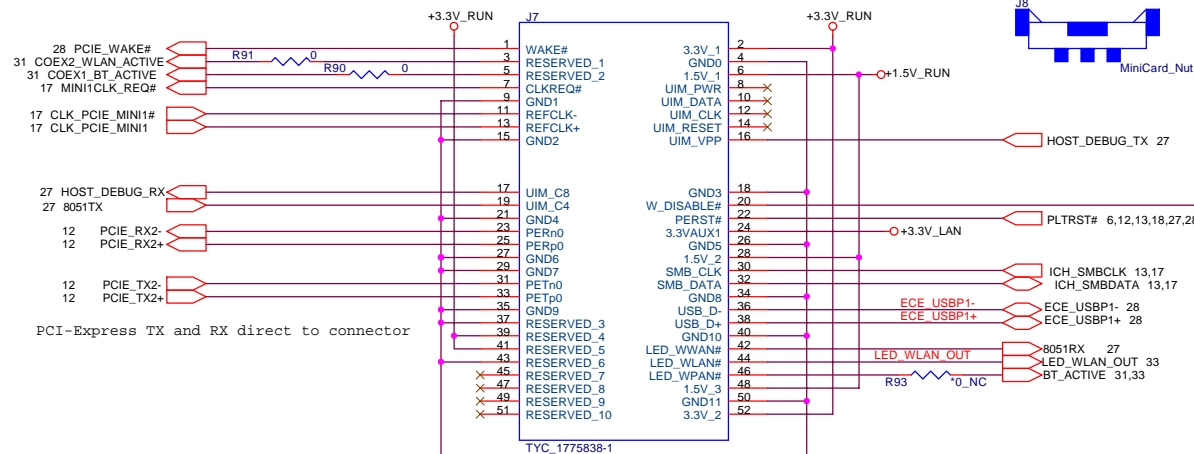


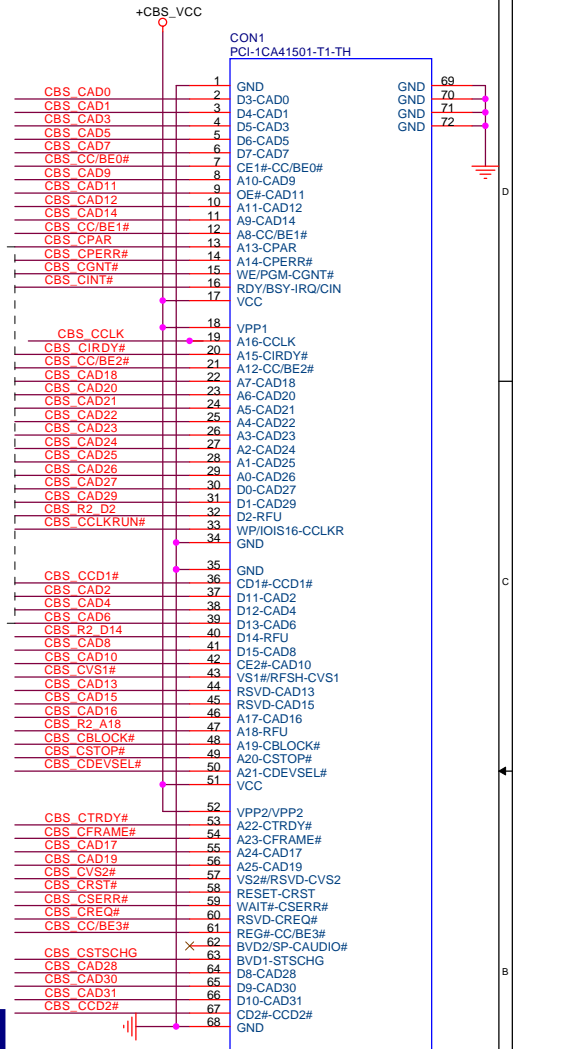
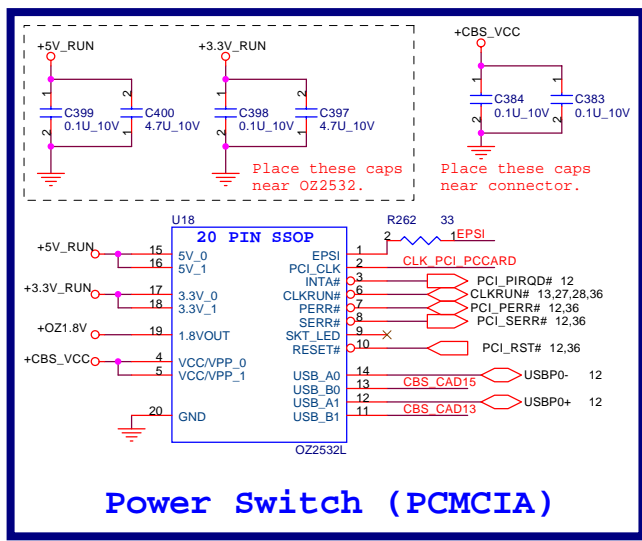
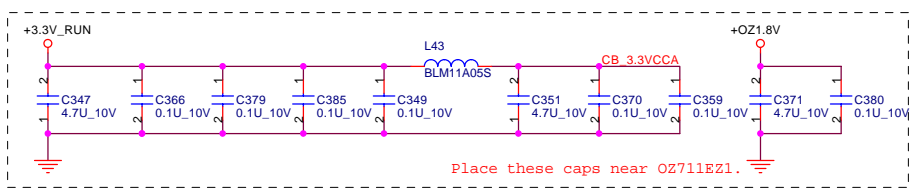
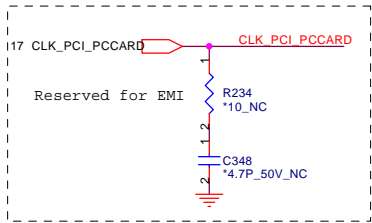
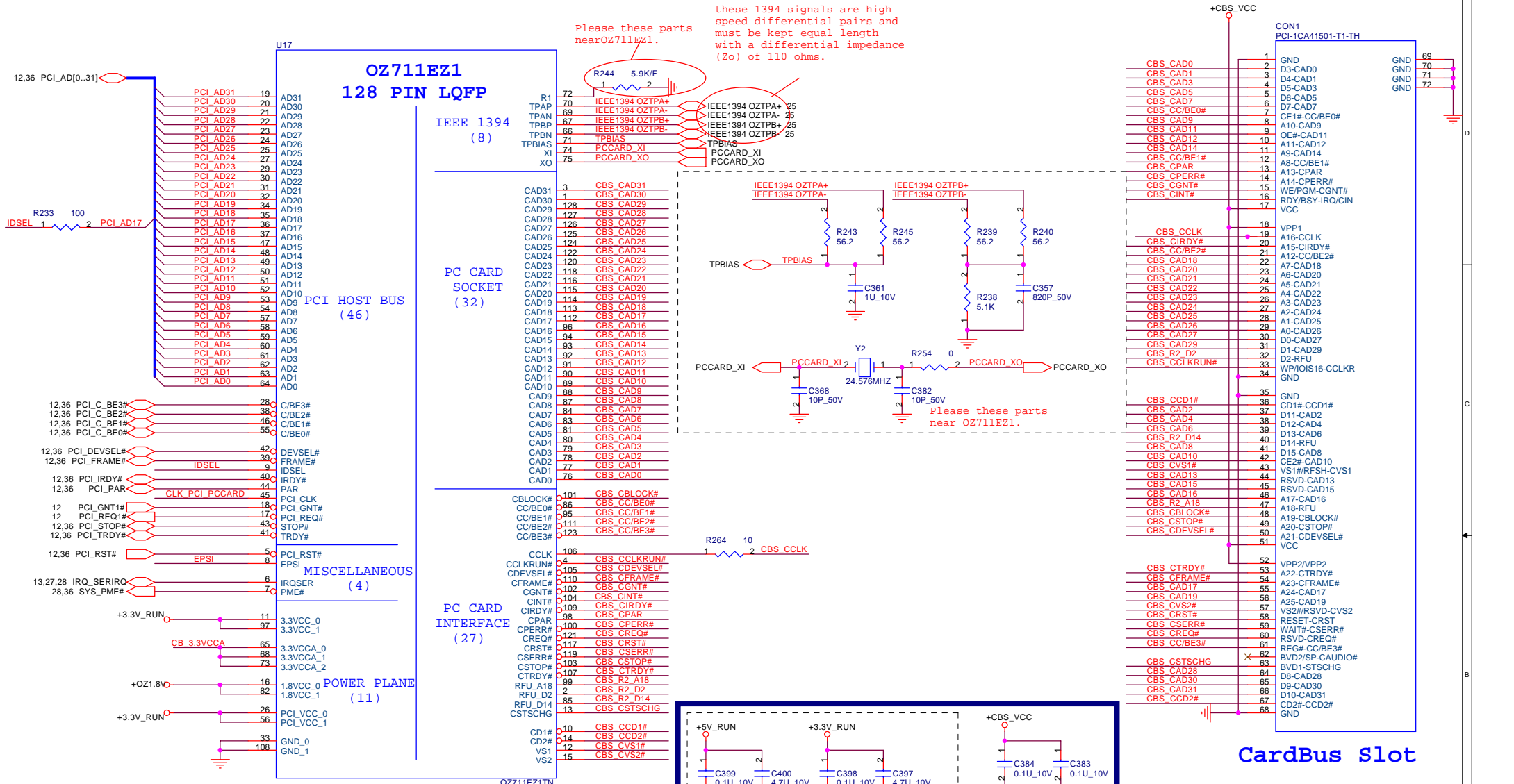
**QUANTA COMPUTER**

Title: SCREW PAD

Size: Document Number DM5 Rev 3A

Date: 星期二, 十二月 27, 2005 Sheet 22 of 59





**QUANTA COMPUTER**

Title: PCCARD

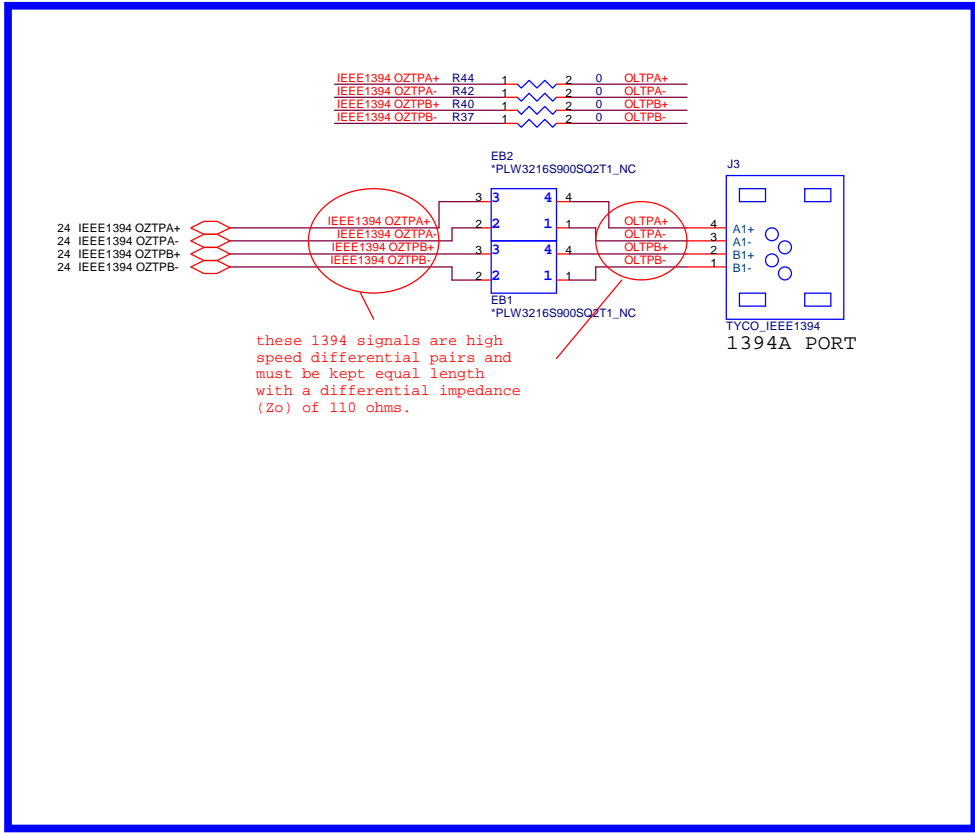
Size: Document Number DM5

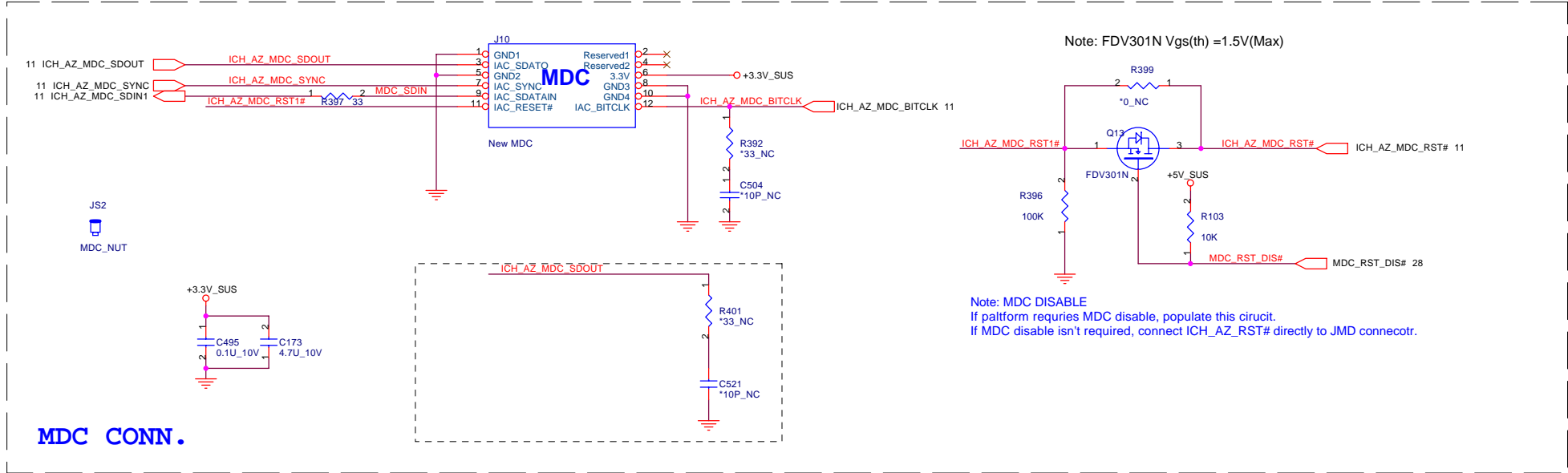
Date: 星期二, 十二月 27, 2005

Sheet: 24 of 59

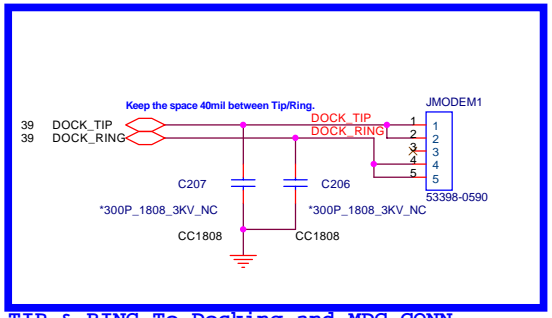
Rev: 1A



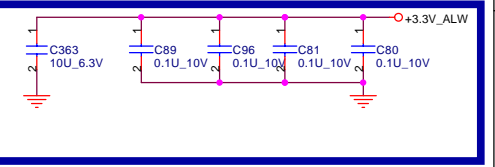
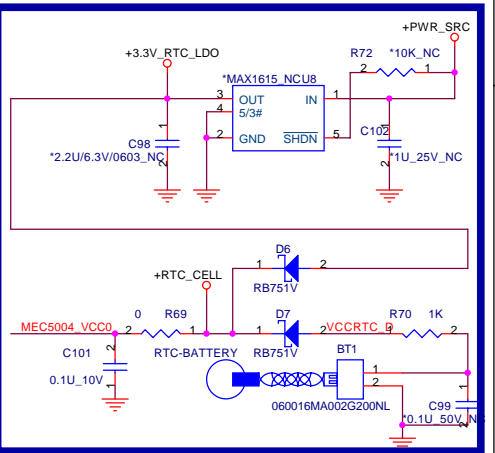
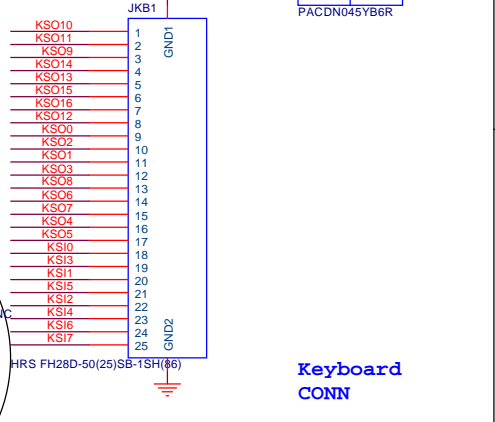
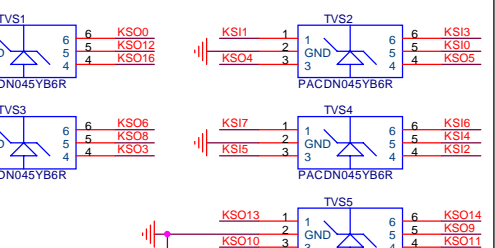
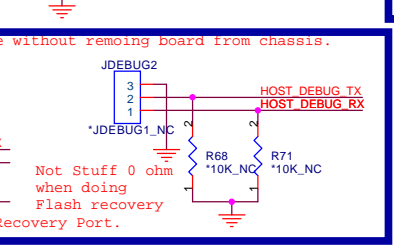
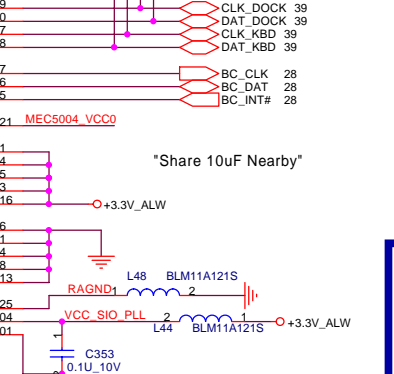
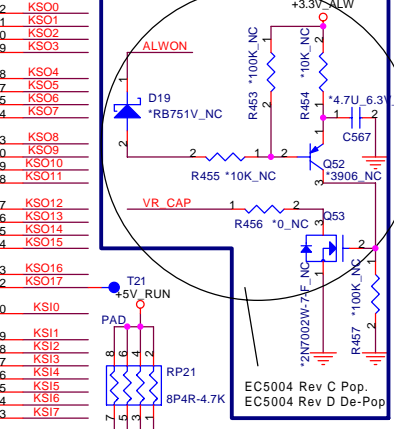
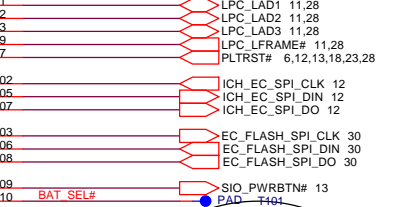
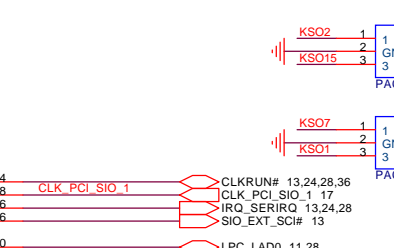
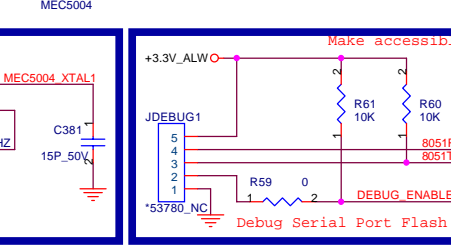
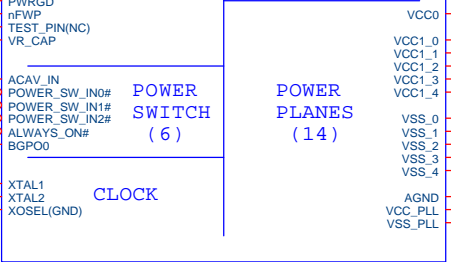
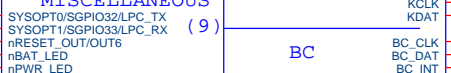
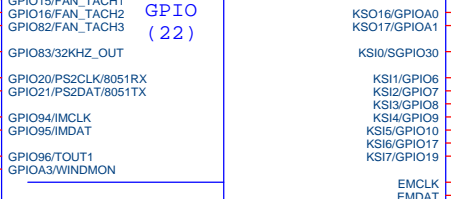
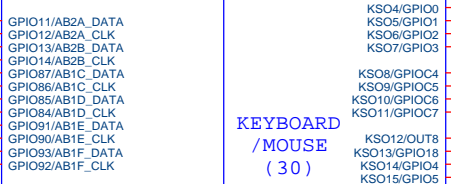
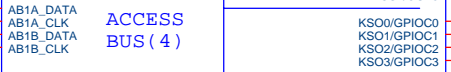
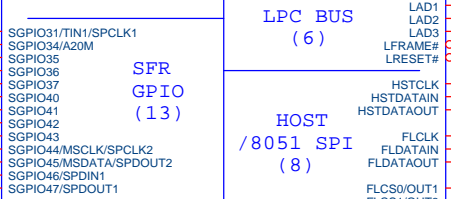
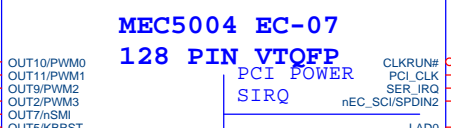
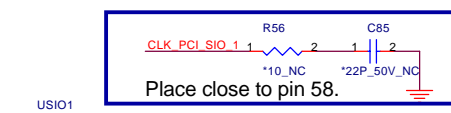
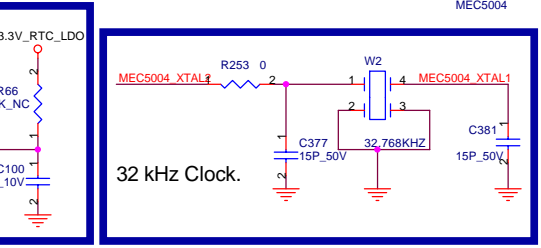
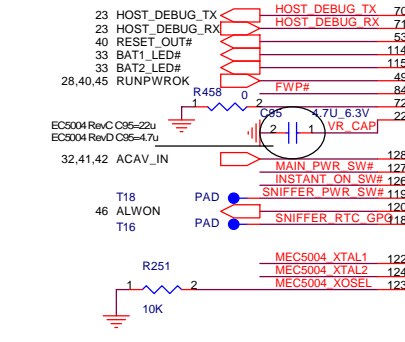
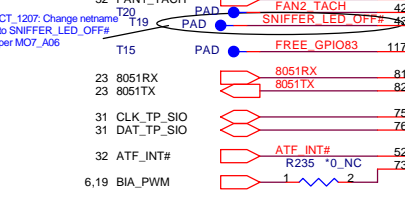
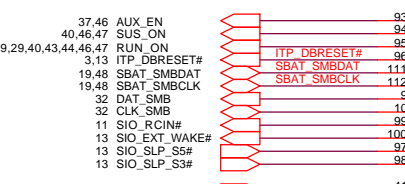
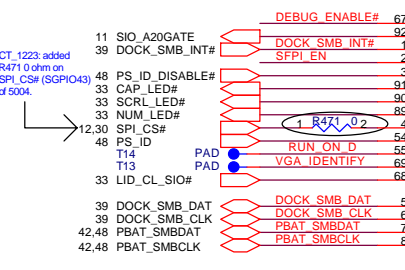
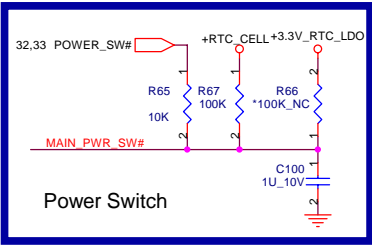
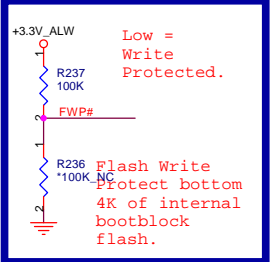
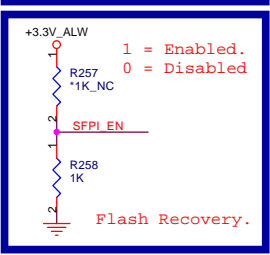
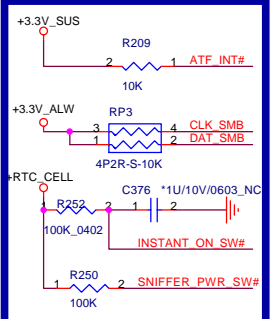
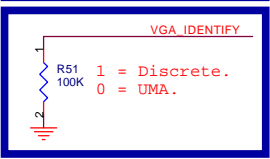
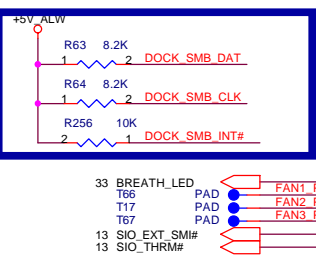
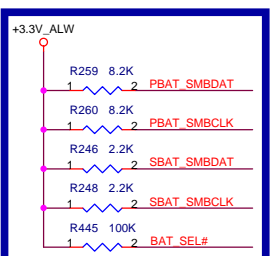




**MDC CONN.**



**TIP & RING To Docking and MDC CONN.**



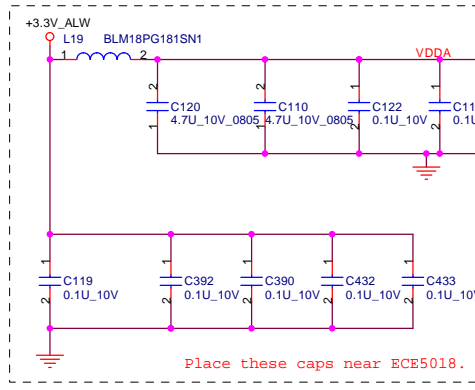
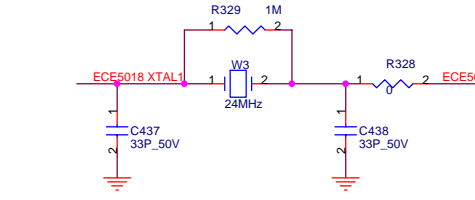
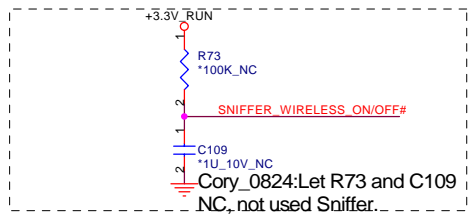
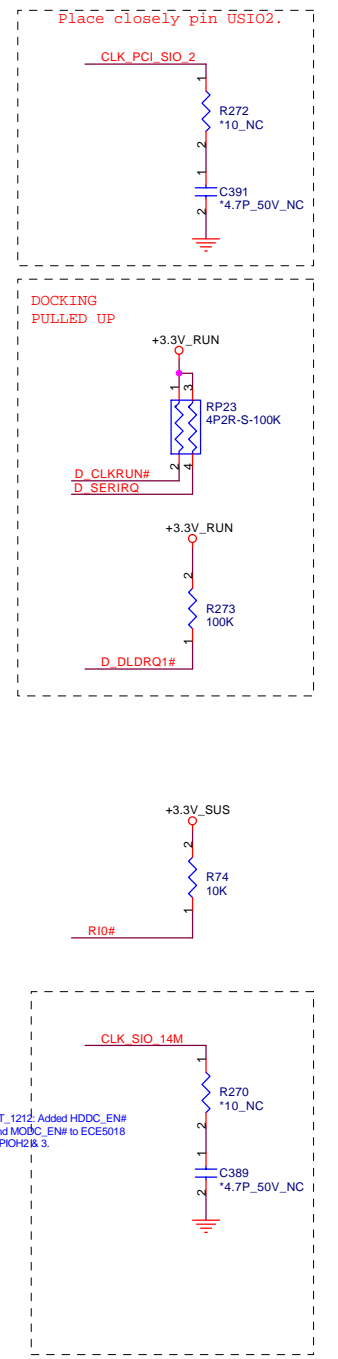
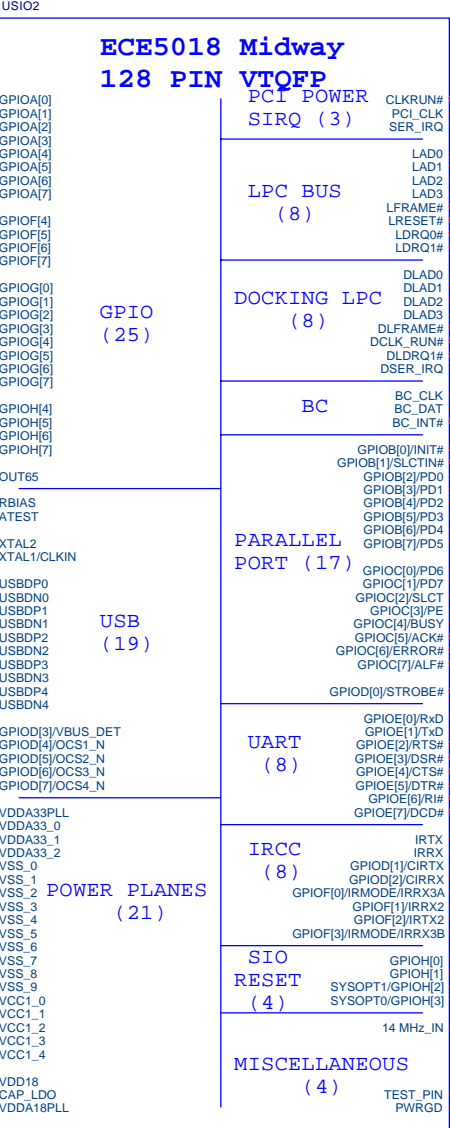
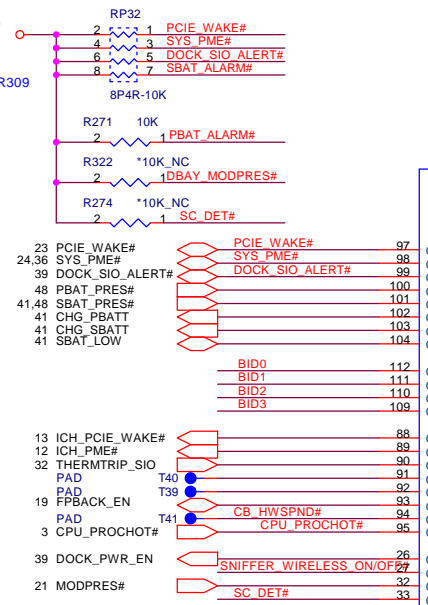
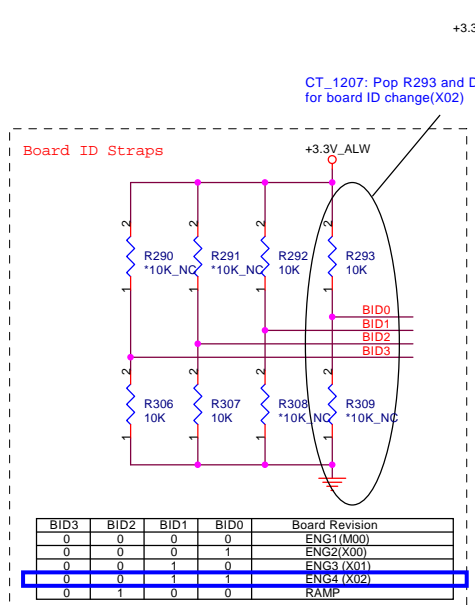
Cory\_0824: Changed C96 and C80 from 0.047u to 0.1u when M07 A04.

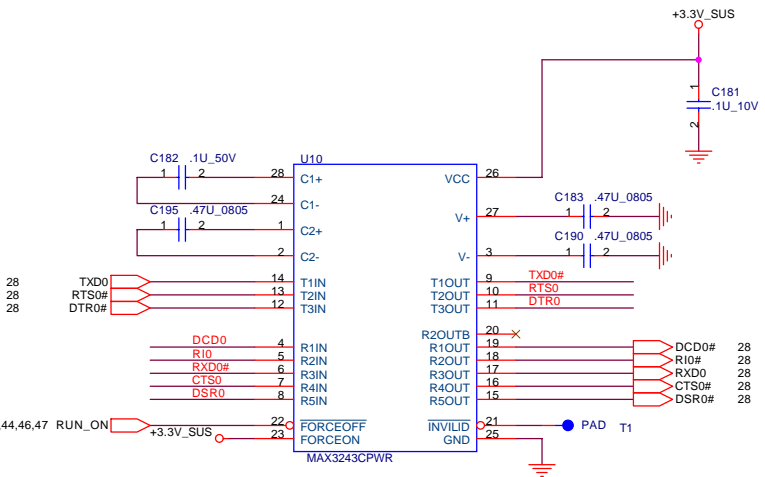
QUANTA COMPUTER

Title: Ultra I/O Controller MEC5004

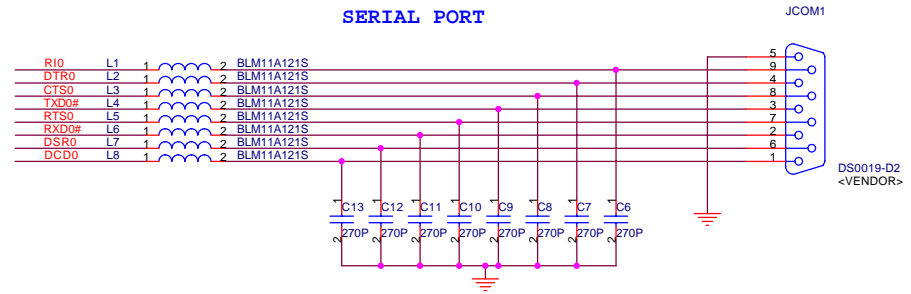
Size	Document Number	Rev
	DM5	1A

Date: 星期二, 十二月 27, 2005 Sheet 27 of 59



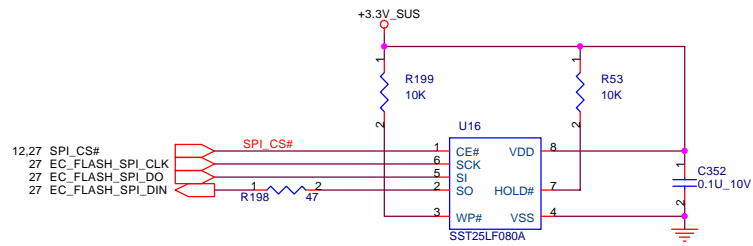


If MAX3243 pin 22 tied to RUN\_ON, then it can not support Ring Out

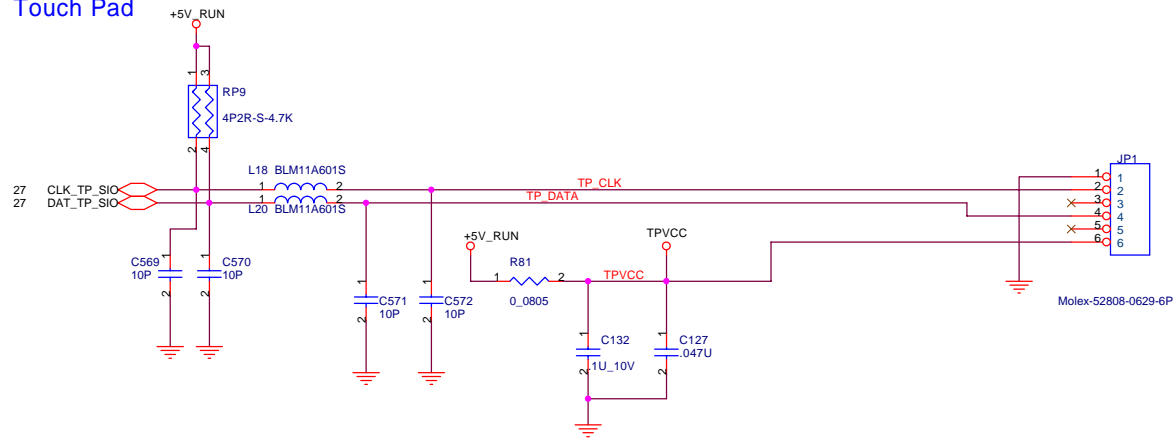


Place them close to serial port

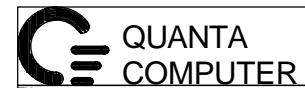
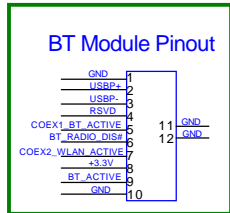
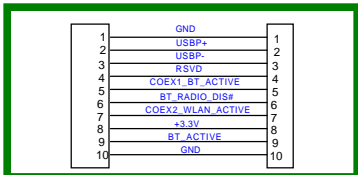
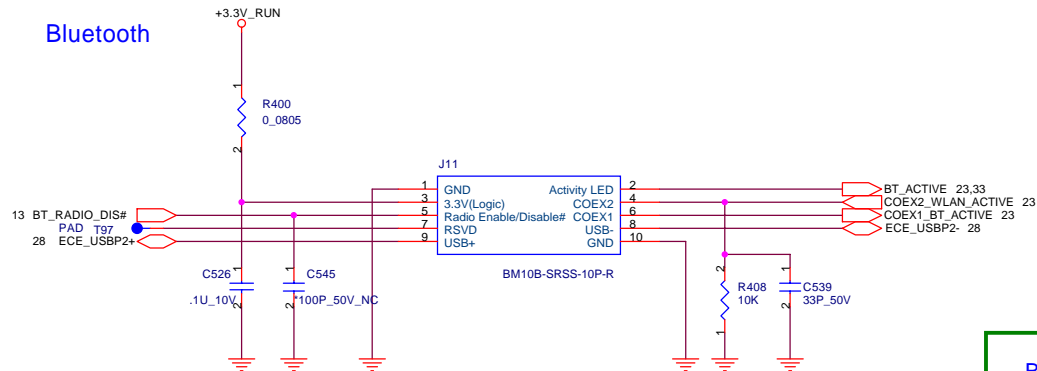
8Mbit (1M Byte), SPI

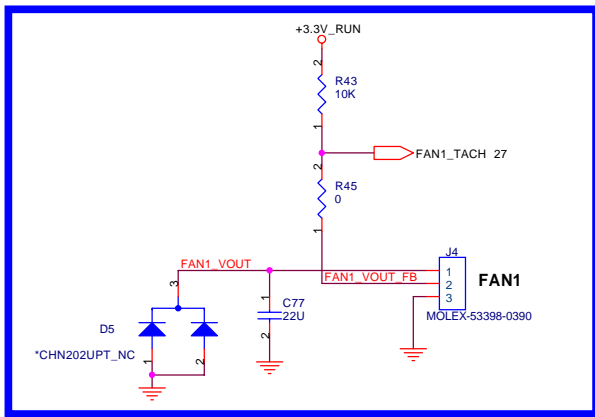


### Touch Pad

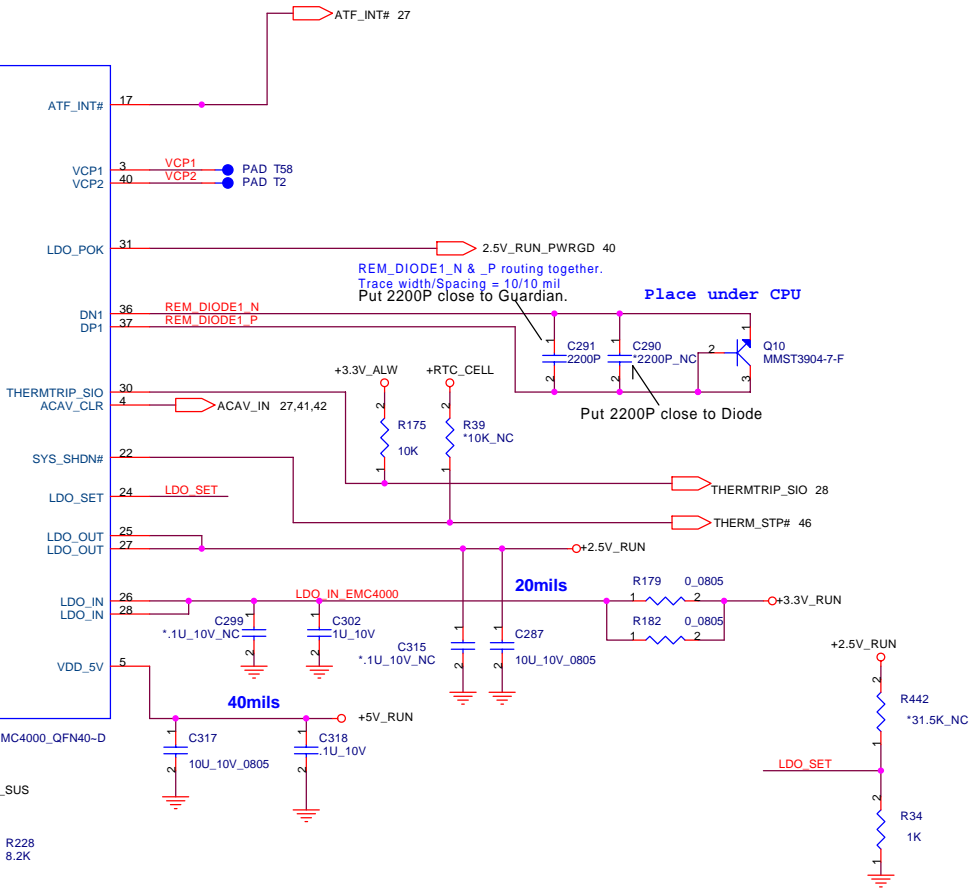
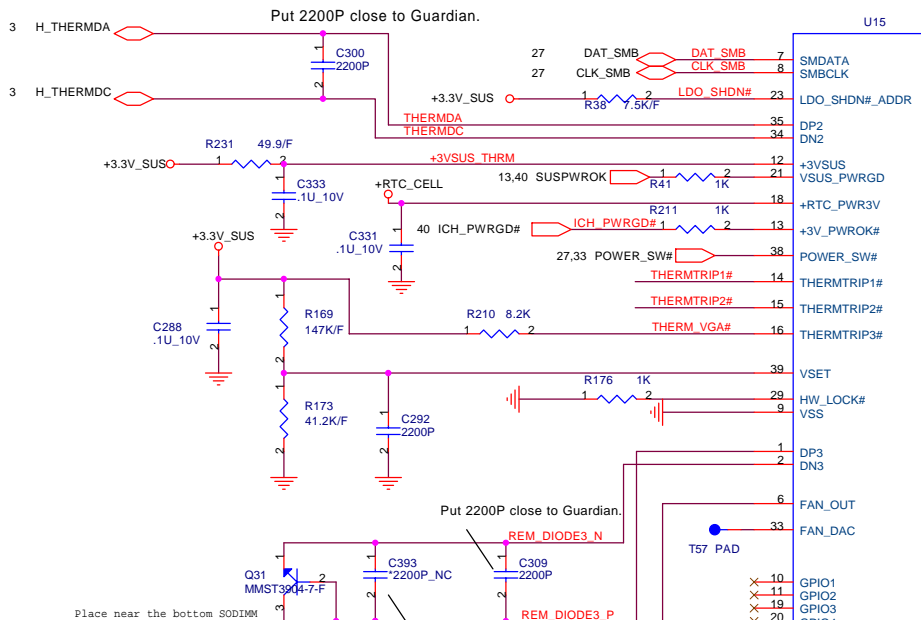


### Bluetooth

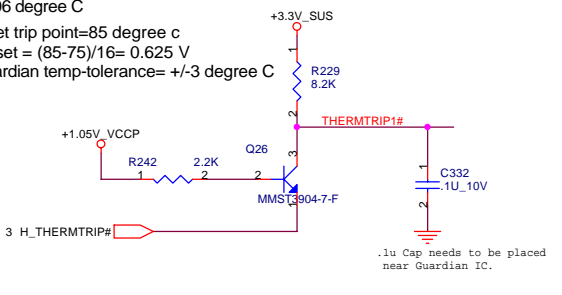




H\_THERMDA & H\_THERMDC routing together. Trace width/Spacing = 10/10 mil



Notes:  
 $V_{set} = (T_p - 75) / 21$   
 Where  $T_p = 75$  to 106 degree C  
 Set trip point = 85 degree C  
 $V_{set} = (85 - 75) / 16 = 0.625$  V  
 Guardian temp-tolerance = +/- 3 degree C



**QUANTA COMPUTER**

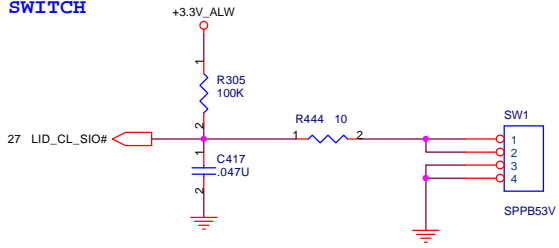
Title: FAN & THERMAL

Size: DMS	Document Number: DMS	Rev: 1A
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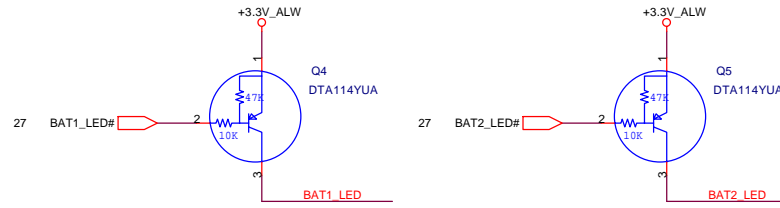
Date: 星期二, 十二月 27, 2005 Sheet 32 of 59



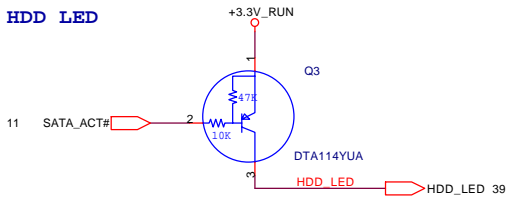
### LID SWITCH



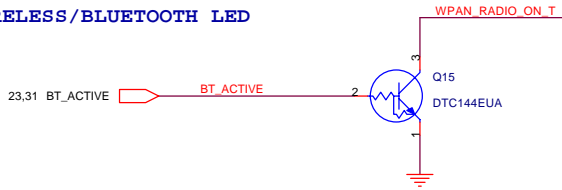
### BATTERY 1,2 LED



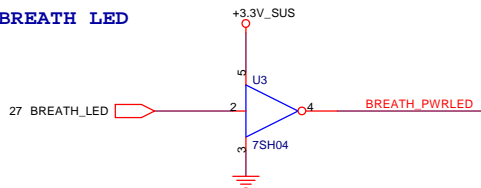
### HDD LED



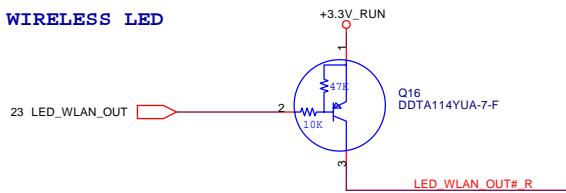
### WIRELESS/BLUETOOTH LED



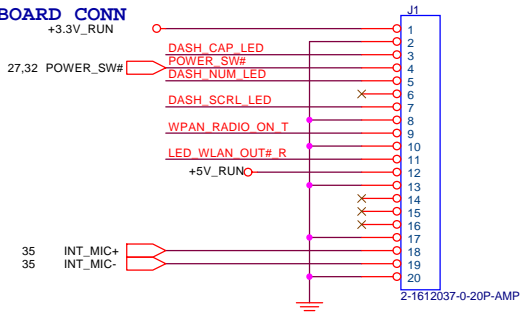
### BREATH LED



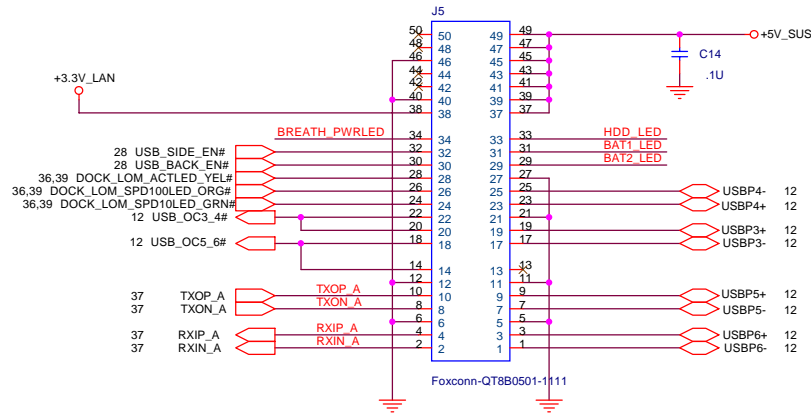
### WIRELESS LED



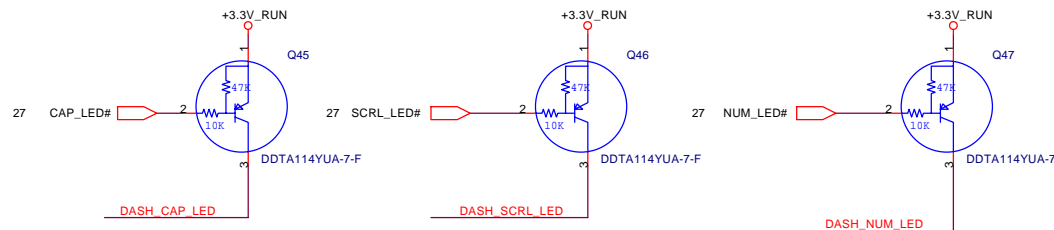
### DASH BOARD CONN

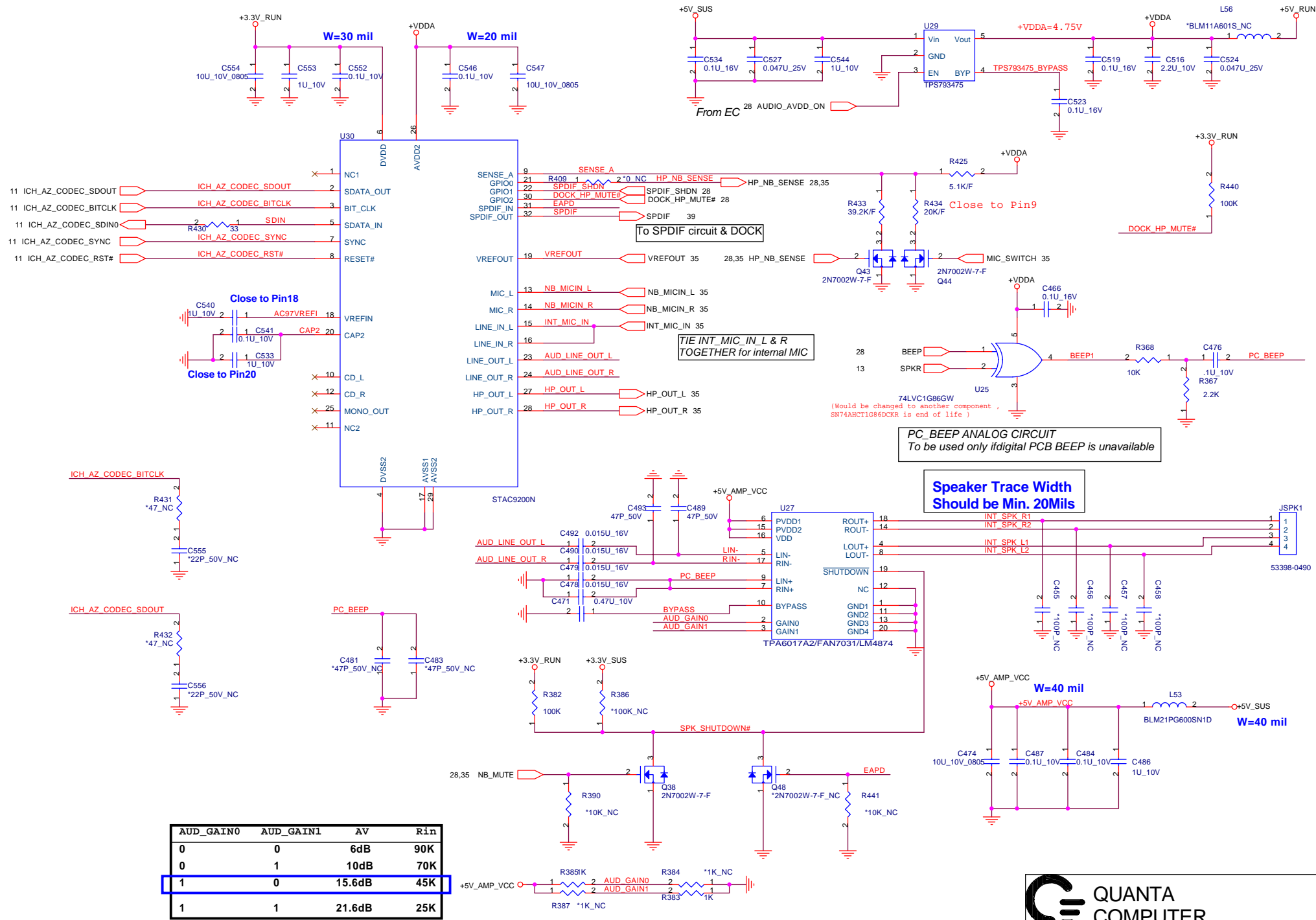


### MB TO I/O-BOARD CONN



### CAP, SCRL, NUM LEDS

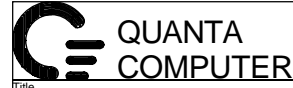


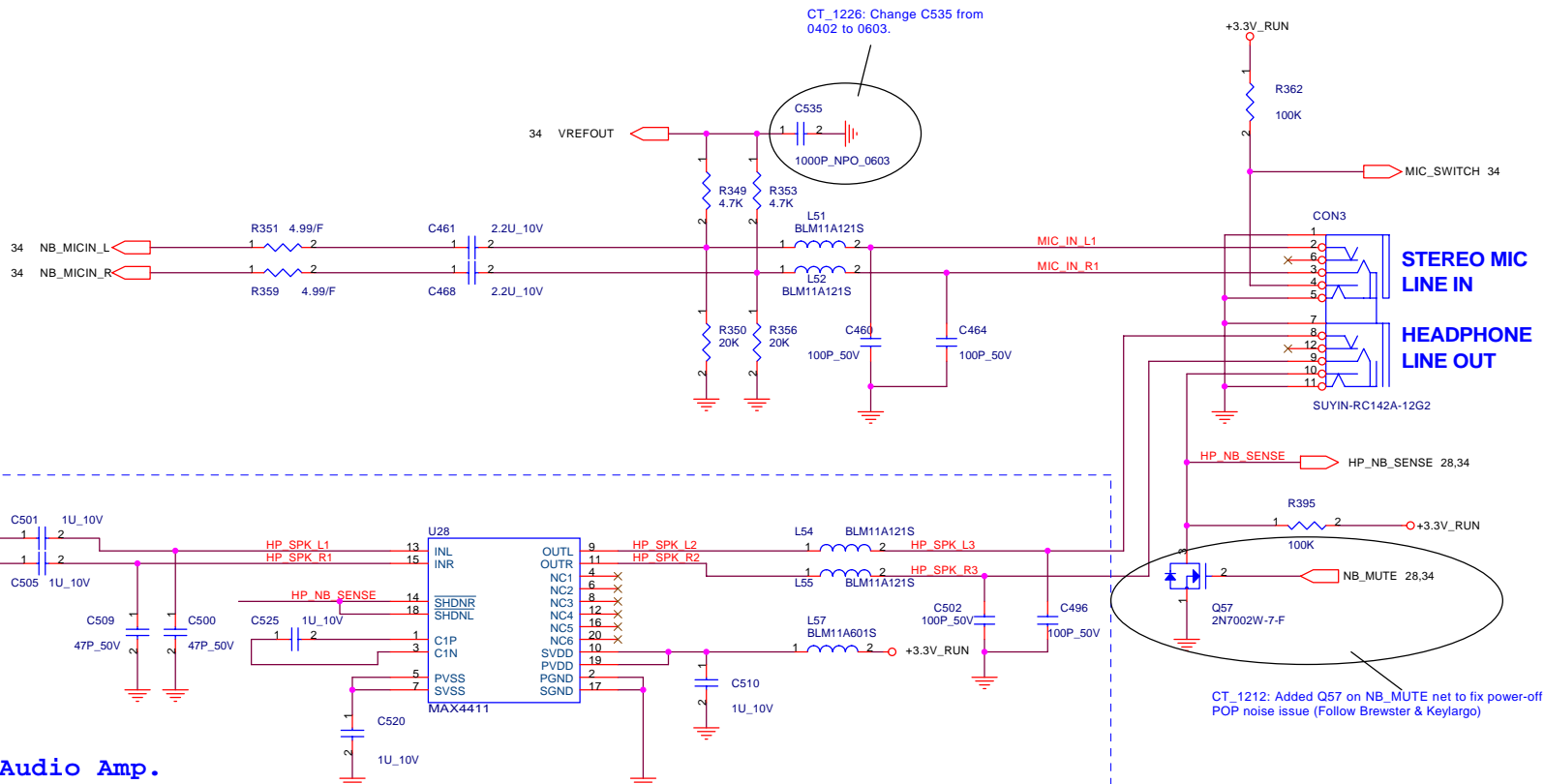


AUD_GAIN0	AUD_GAIN1	AV	Rin
0	0	6dB	90K
0	1	10dB	70K
1	0	15.6dB	45K
1	1	21.6dB	25K

**PC\_BEEP ANALOG CIRCUIT**  
To be used only if digital PCB BEEP is unavailable

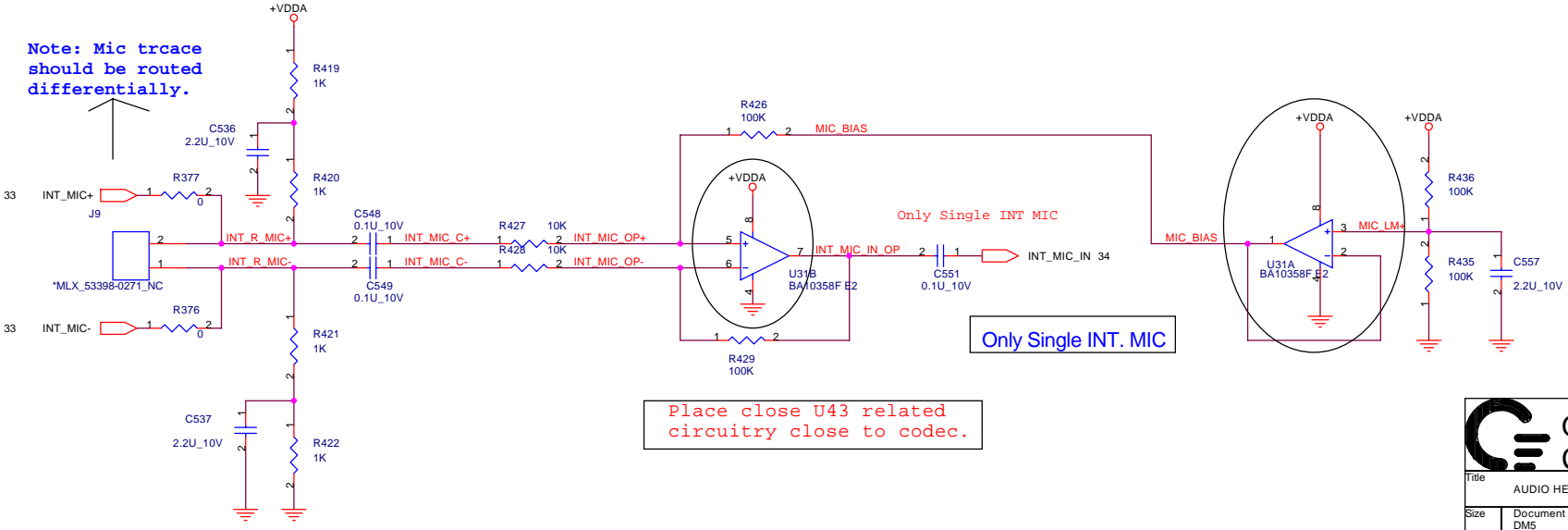
**Speaker Trace Width**  
Should be Min. 20Mils





**Headphone Audio Amp.**

Note: Mic trace should be routed differentially.



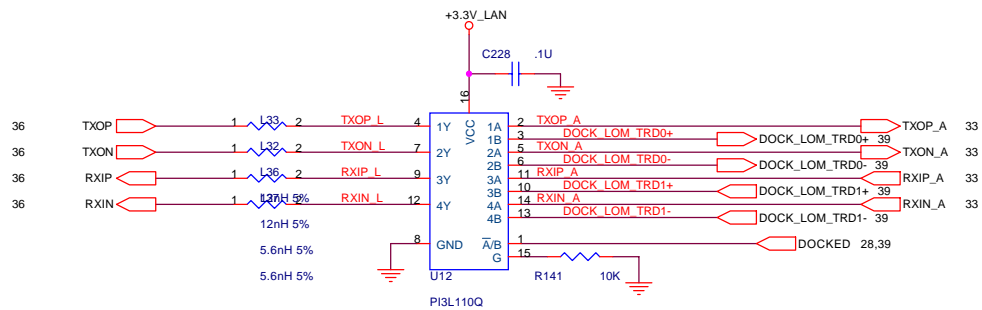
**QUANTA COMPUTER**

Title: AUDIO HEADPHONE CONN

Size	Document Number	Rev
	DM5	1A

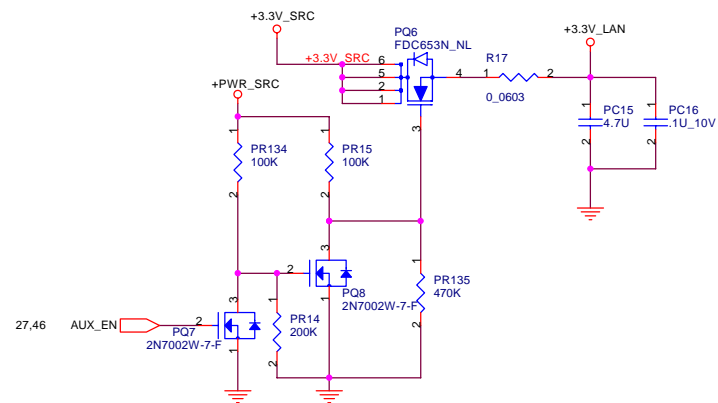
Date: 星期二, 十二月 27, 2005 Sheet 35 of 59



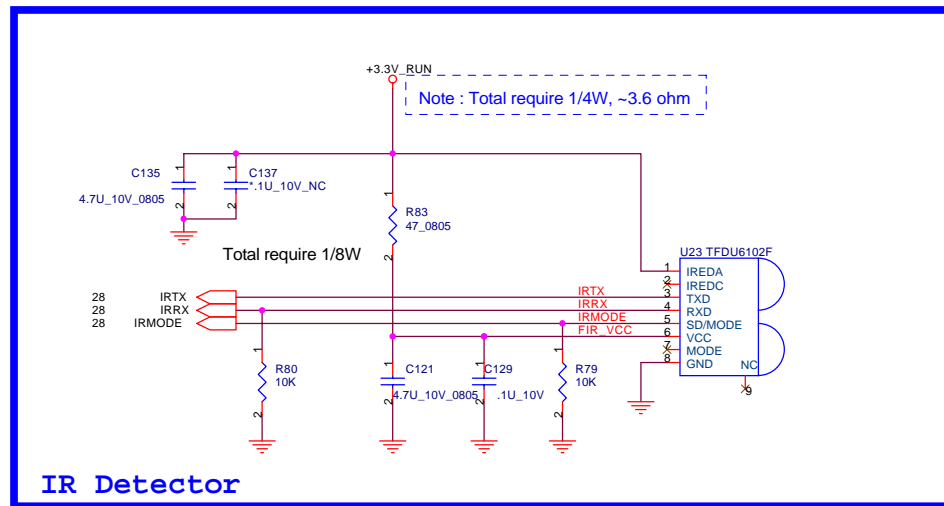


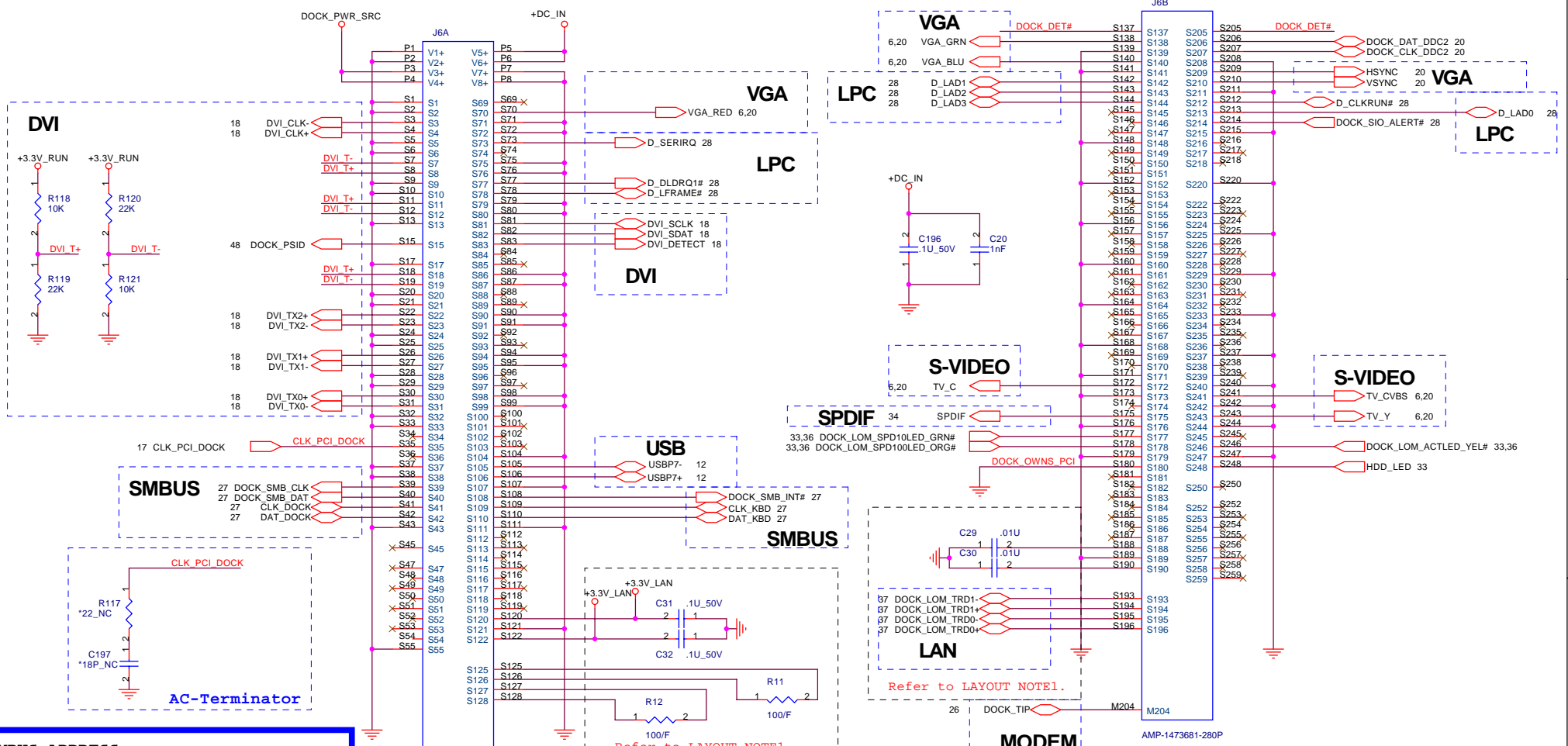
10/100LAN\_E-SWITCH

CT\_1207: Removed ESD1 & ESD2 & C573, C574 per ADC Comm team B. Boes.



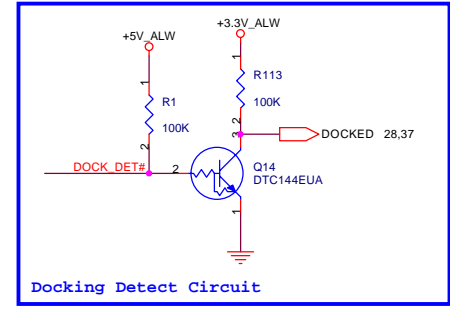
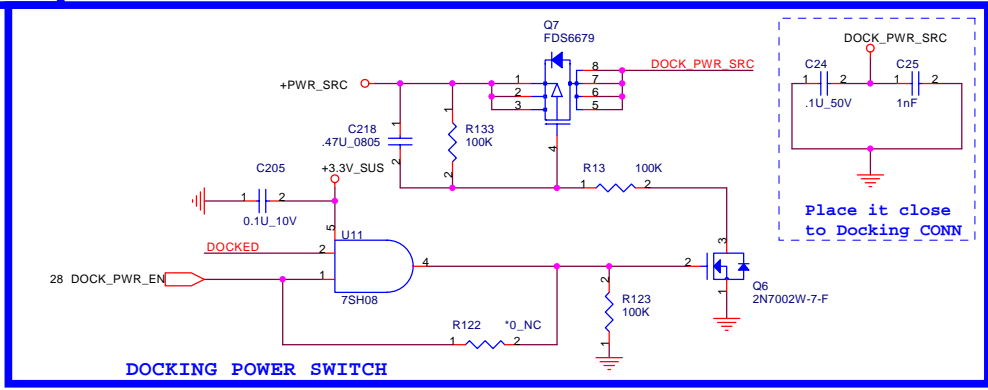
LAN POWER





**SMBUS ADDRESS :**  
**DOCK/APR Microprocessor -- 74H**  
**DOCK USB/IDE Interface(FX2) -- 72H**  
**DOCK SMBus Battery 16h Charger 12h IDE I/F 70h D-BAY**  
**72h SIO 48h**

**LAYOUT NOTES1:**  
 Terminators should be as close as possible to dock connector pins.  
 Keep traces as short as possible.



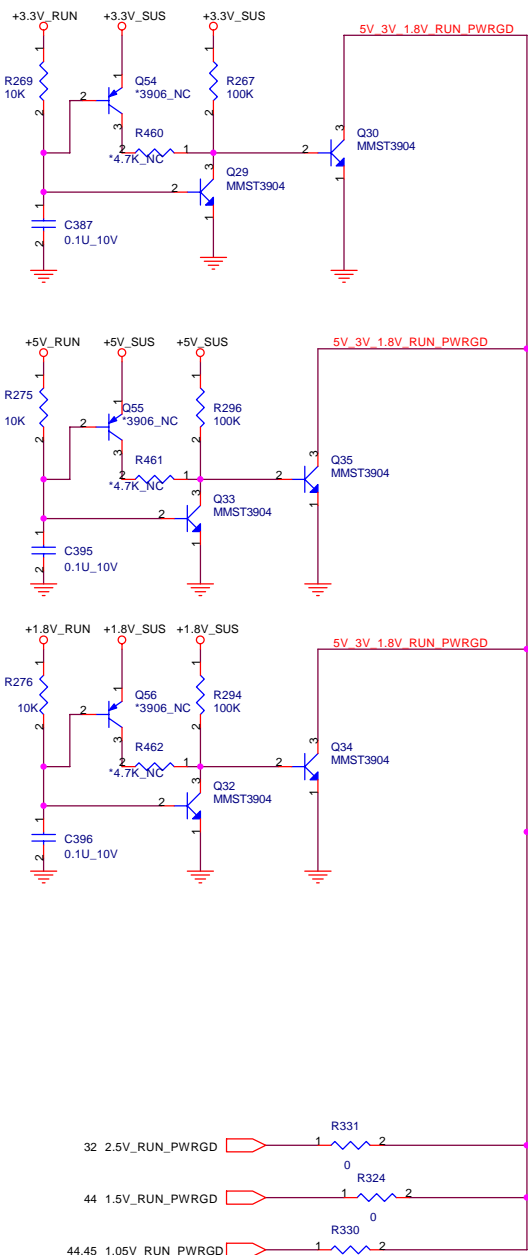
### RUN POWER OPTIONS:

**OPTION 1**

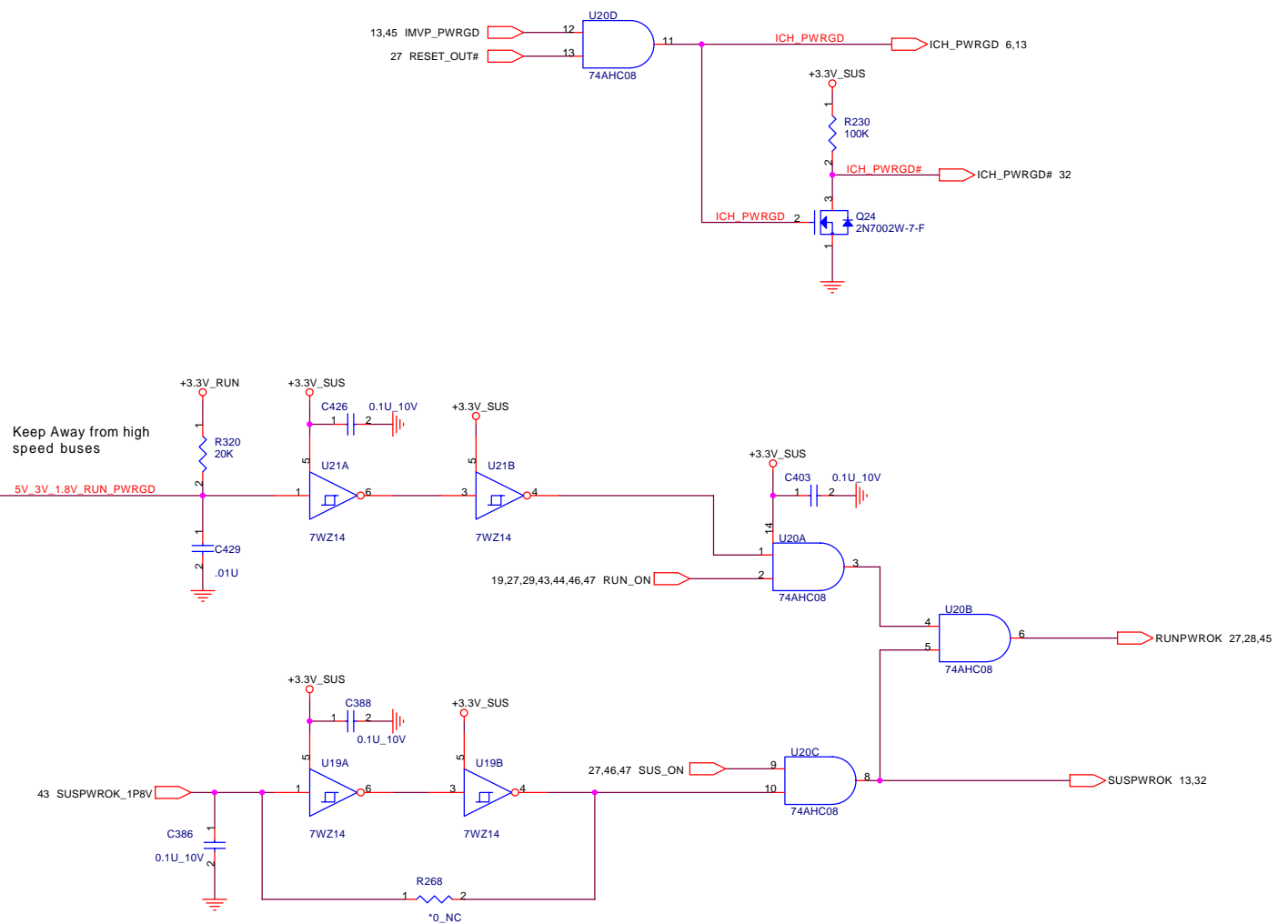
R269, R275, R276 = 10K ohm  
 Population: C387, C395, C396, Q29, Q32, Q33, R267, R296, R294.  
 Depopulation: Q54, Q55, Q56, R460, R461, R462.

**OPTION 2**

R269, R275 = 200K ohm, R276 = 100K ohm.  
 Population: Q54, Q55, Q56, R460, R461, R462.  
 Depopulation: C387, C395, C396, Q29, Q32, Q33, R267, R296, R294.

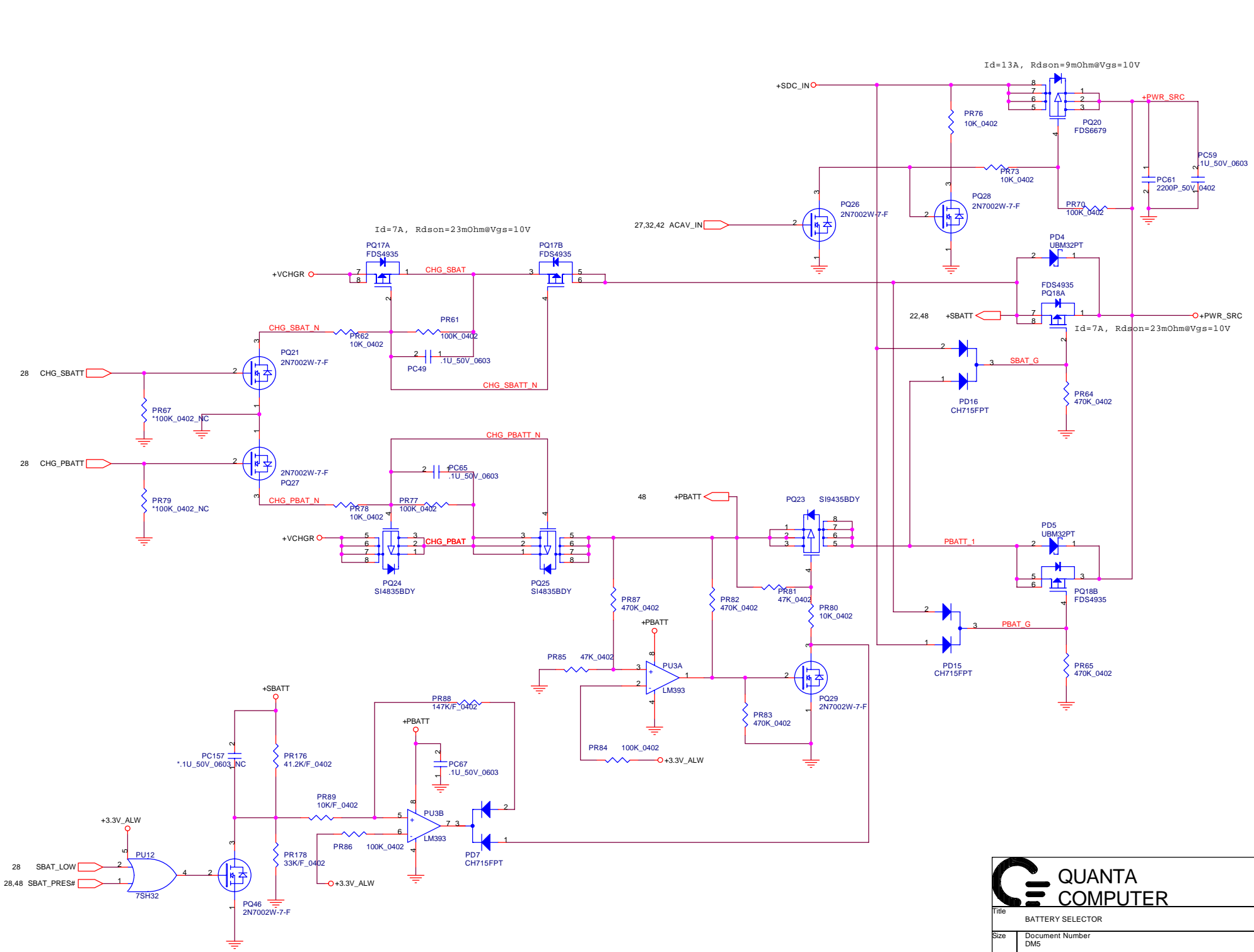


Keep Away from high speed buses



Title SYSTEM RESET/POWER GOOD		
Size	Document Number DM5	Rev 1A
Date:	星期三, 十二月 27, 2005	Sheet 40 of 59





**QUANTA COMPUTER**

Title: BATTERY SELECTOR

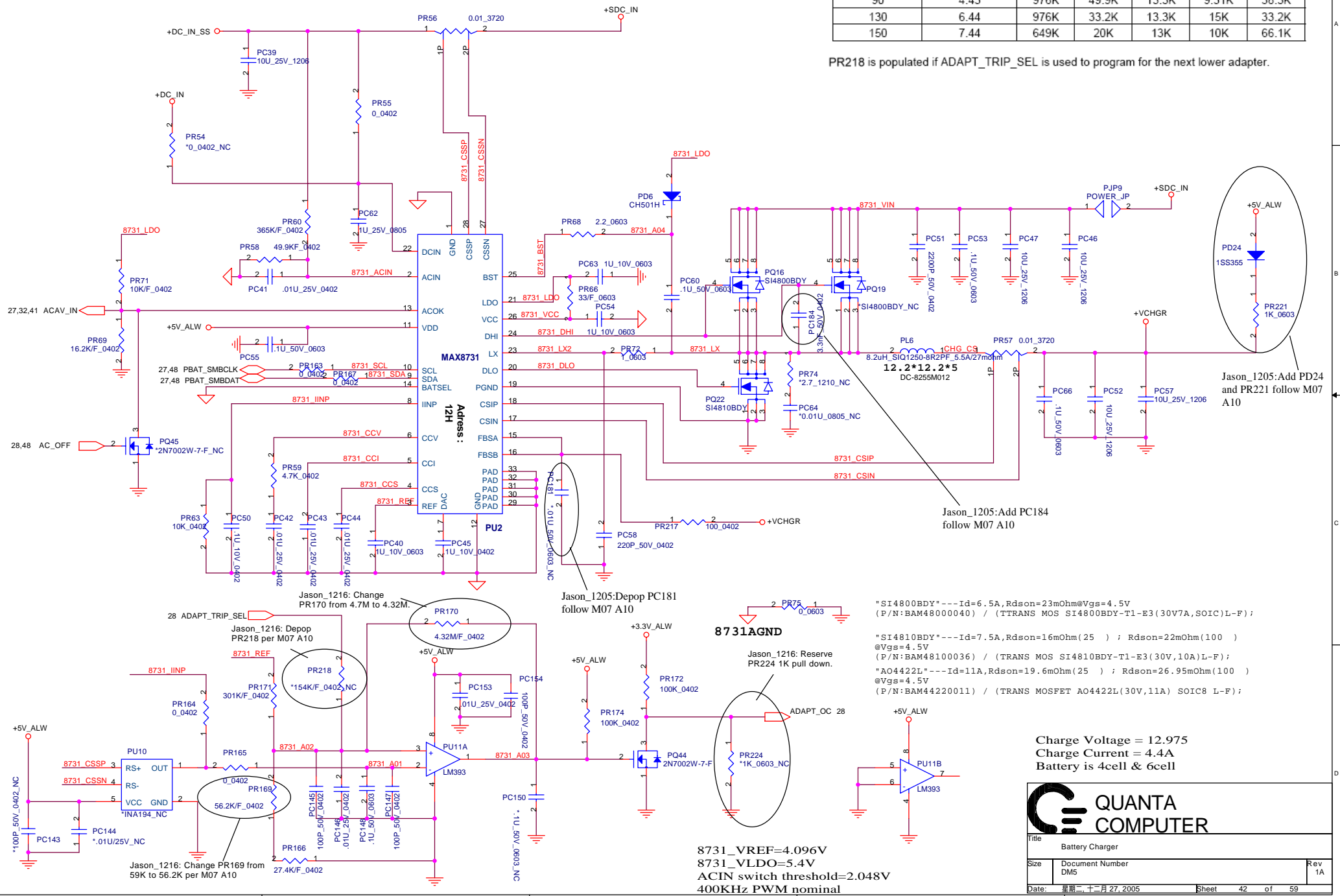
Size	Document Number	Rev
DM5		1A

Date: 星期二, 十二月 27, 2005 Sheet 41 of 59

TABLE 1

ADAPTER (W)	TRIP CURRENT (A)	PR170	PR171	PR169	PR166	PR218
65	3.17	4.32M	301K	56.2K	27.4K	N/A
90	4.43	976K	49.9K	13.3K	9.31K	38.3K
130	6.44	976K	33.2K	13.3K	15K	33.2K
150	7.44	649K	20K	13K	10K	66.1K

PR218 is populated if ADAPT\_TRIP\_SEL is used to program for the next lower adapter.



Jason\_1205: Add PD24 and PR221 follow M07 A10

Jason\_1205: Add PC184 follow M07 A10

Jason\_1216: Change PR170 from 4.7M to 4.32M.  
Jason\_1216: Depop PR218 per M07 A10

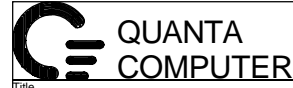
Jason\_1205: Depop PC181 follow M07 A10

Jason\_1216: Reserve PR224 1K pull down.

"SI4800BDY"---Id=6.5A,Rdson=23mOhm@Vgs=4.5V  
(P/N:BAM48000040) / (TTRANS MOS SI4800BDY-T1-E3(30V7A,SOIC)L-F);

"SI4810BDY"---Id=7.5A,Rdson=16mOhm(25); Rdson=22mOhm(100)  
@Vgs=4.5V  
(P/N:BAM48100036) / (TRANS MOS SI4810BDY-T1-E3(30V,10A)L-F);  
"AO4422L"---Id=11A,Rdson=19.6mOhm(25); Rdson=26.95mOhm(100)  
@Vgs=4.5V  
(P/N:BAM44220011) / (TRANS MOSFET AO4422L(30V,11A) SOIC8 L-F);

Charge Voltage = 12.975  
Charge Current = 4.4A  
Battery is 4cell & 6cell

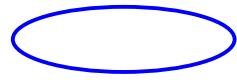


Title Battery Charger		
Size	Document Number DM5	Rev 1A
Date: 星期三, 十二月 27, 2005	Sheet 42	of 59

8731\_VREF=4.096V  
8731\_VLDO=5.4V  
ACIN switch threshold=2.048V  
400KHz PWM nominal



POP for TI51116



DePOP for TI51116

1.8 Volt +/-5%  
Design Current:7.28A  
Maximum Current: 10.5A  
OCP: min A; max A


NEC-TPS51116G47MM(5)12R-  
7.3\*4.3\*2.8-15mohm

0.9 Volt +/-5%  
Design Current:1.05A  
Maximum Current: 1.5A  
Current limit =3.8A

"IRF7413ZTRPBF"---Id=13A,Rdson=10.5mOhm@Vgs=4.5V  
(P/N:BAM74130036) / (TRANS MOSFET IRF7413ZTRPBF(30V,13A)L-F);

"FDS6676AS"---Id=14.5A,Rdson=5.9mOhm(25 )@Vgs=4.5V ; ,Rdson=8.11mOhm(100 )@Vgs=4.5V  
(P/N:BAM66760026) / (TRANS MOSFET FDS6676AS\_NL(30V,14.5A)ROHS);  
Use the worst-case value for RDS(ON) from the MOSFET data sheet, and add a margin of 0.5%/C for the rise in RDS(ON) with temperature.

OCP=14A; Rdson=5.9mOhm(25 )  
OCP=10.6A; Rdson=8.11mOhm(100 )

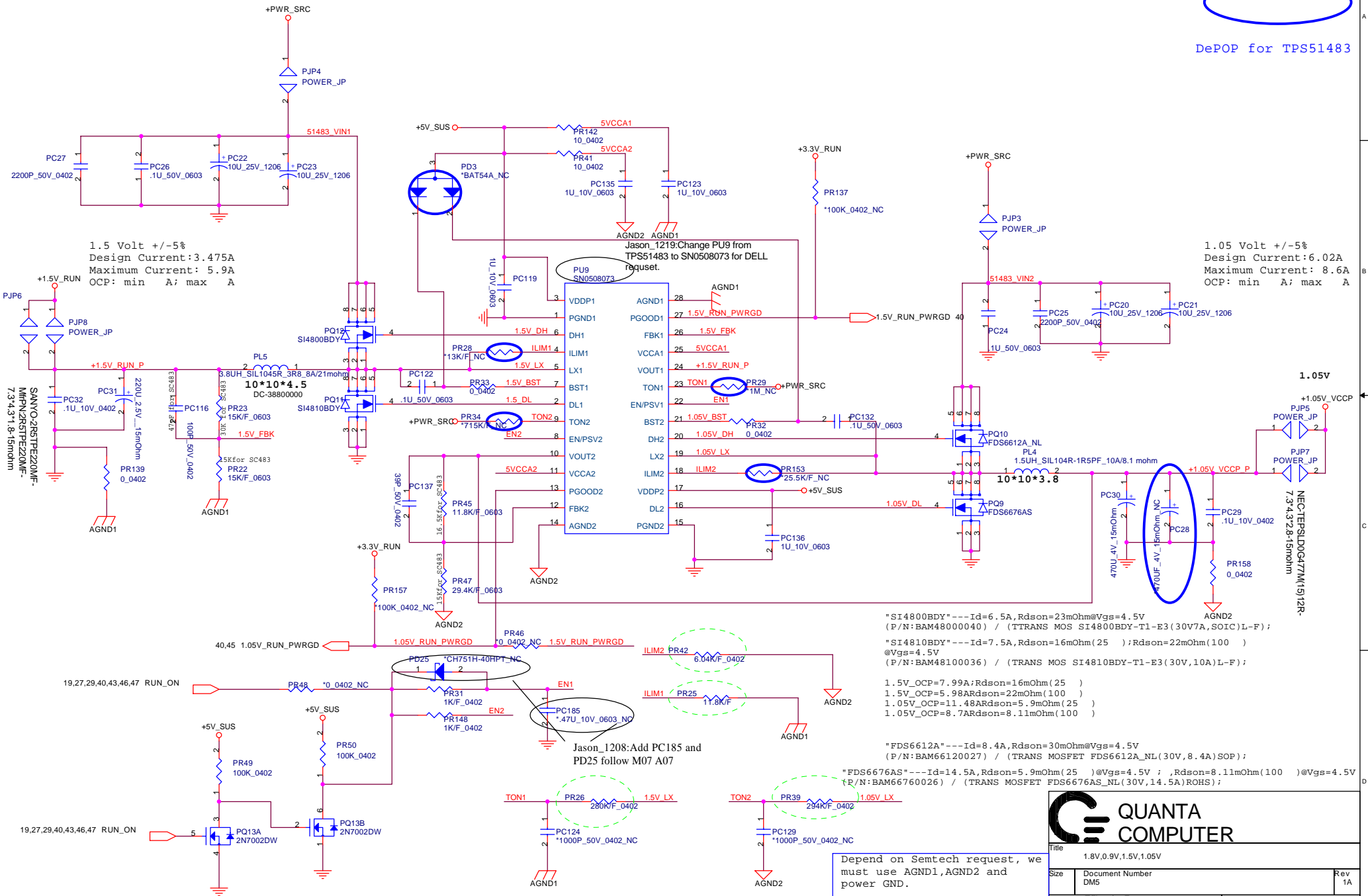


QUANTA  
COMPUTER

Title		1.8V,0.9V
Size	Document Number	Rev
	DM5	1A
Date:	星期二, 十二月 27, 2005	Sheet 43 of 59

POP for TPS51483

DePOP for TPS51483



**QUANTA COMPUTER**

Title: 1.8V,0.9V,1.5V,1.05V

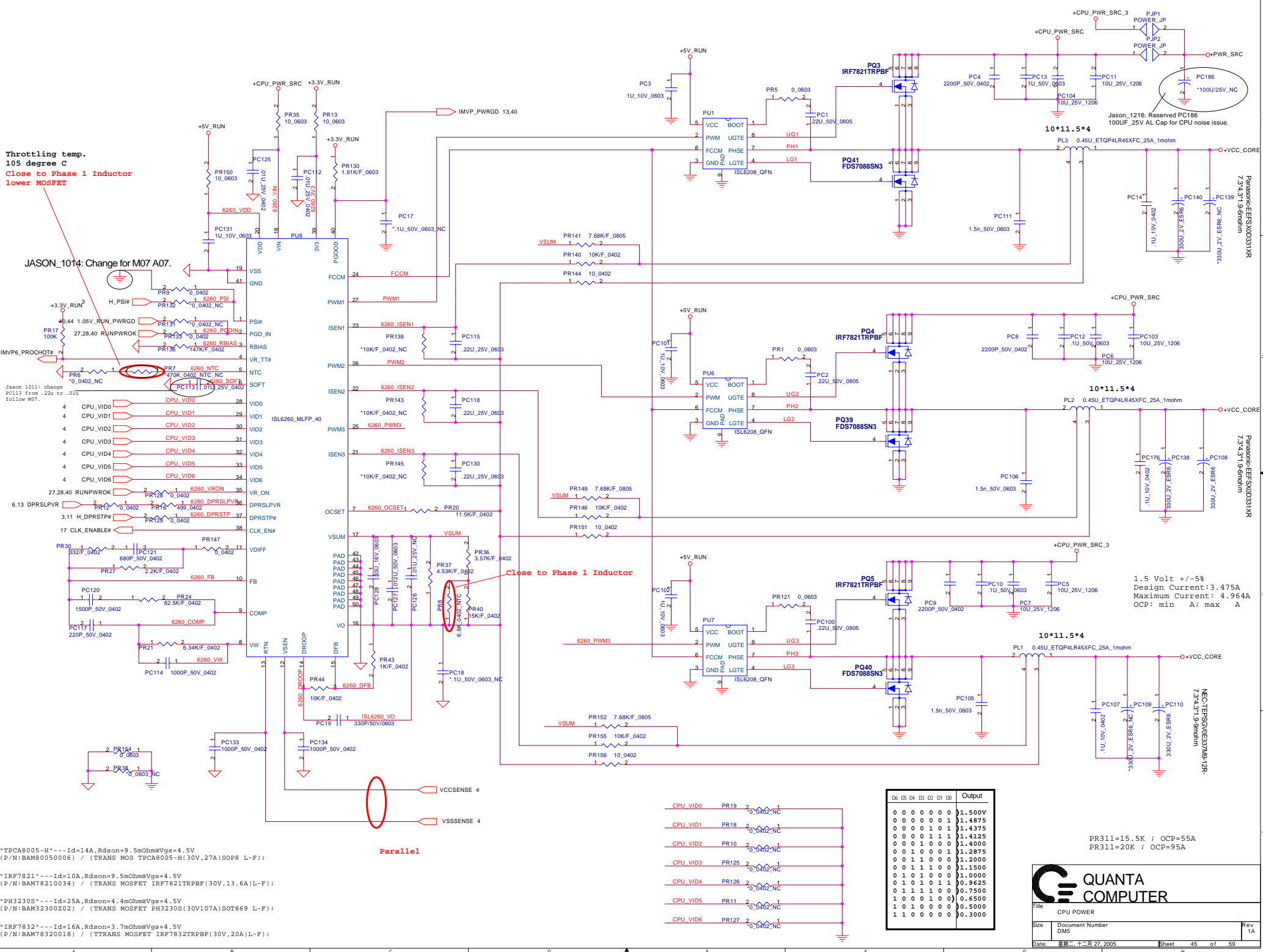
Size	Document Number	Rev
	DMS	1A

Date: 星期二, 十二月 27, 2005 Sheet 44 of 59

Depend on Semtech request, we must use AGND1, AGND2 and power GND.

Throttling temp.  
105 degree C  
Close to Phase 1 Inductor  
lower MOSFET

JASON\_1014: Change for M07 A07.



"TPCA8005-H"---Id=14A,Rdson=9.5mOhm@Vgs=4.5V  
(P/N:BAM80050006) / (TRANS MOS TPCA8005-H(30V,27A)SOP8 L-F);

"IRF7821"---Id=10A,Rdson=9.5mOhm@Vgs=4.5V  
(P/N:BAM78210034) / (TRANS MOSFET IRF7821TRPBF(30V,13.6A)L-F);

"PH3230S"---Id=25A,Rdson=4.4mOhm@Vgs=4.5V  
(P/N:BAM32300202) / (TRANS MOSFET PH3230S(30V107A)SOT669 L-F);

"IRF7832"---Id=16A,Rdson=3.7mOhm@Vgs=4.5V  
(P/N:BAM78320018) / (TRANS MOSFET IRF7832TRPBF(30V,20A)L-F);

Parallel

- CPU\_VID0 PR19 2 0\_0402 1
- CPU\_VID1 PR18 2 0\_0402 1
- CPU\_VID2 PR10 2 0\_0402 1
- CPU\_VID3 PR125 2 0\_0402 1
- CPU\_VID4 PR126 2 0\_0402 1
- CPU\_VID5 PR11 2 0\_0402 1
- CPU\_VID6 PR127 2 0\_0402 1

D6	D5	D4	D3	D2	D1	D0	Output
0	0	0	0	0	0	0	1.500V
0	0	0	0	0	0	1	1.4875
0	0	0	0	1	0	1	1.4375
0	0	0	1	0	1	1	1.4125
0	0	1	0	0	1	1	1.4000
0	0	1	0	1	1	1	1.2875
0	0	1	1	0	0	1	1.2000
0	0	1	1	1	0	1	1.1500
0	1	0	0	0	1	0	1.0000
0	1	0	1	0	1	0	0.9625
0	1	1	1	0	0	0	0.7500
1	0	0	0	0	0	0	0.6500
1	0	0	0	0	0	1	0.5000
1	1	0	0	0	0	0	0.3000

PR311=15.5K ; OCP=55A  
PR311=20K ; OCP=95A

**QUANTA COMPUTER**

Title: CPU POWER  
Size: Document Number DM5  
Date: 星期二, 十二月 27, 2005 Sheet 45 of 59 Rev 1A

3.3 Volt +/-5%  
 Design Current: 4.24A  
 Maximum Current: 6.06A  
 OCP: min A; max A

+3.3V\_SRC  
 PJP18 POWER\_JP

+3.3V\_SRC P  
 PJP16 POWER\_JP

+3.3V\_RTC\_LDO  
 PJP17 POWER\_JP

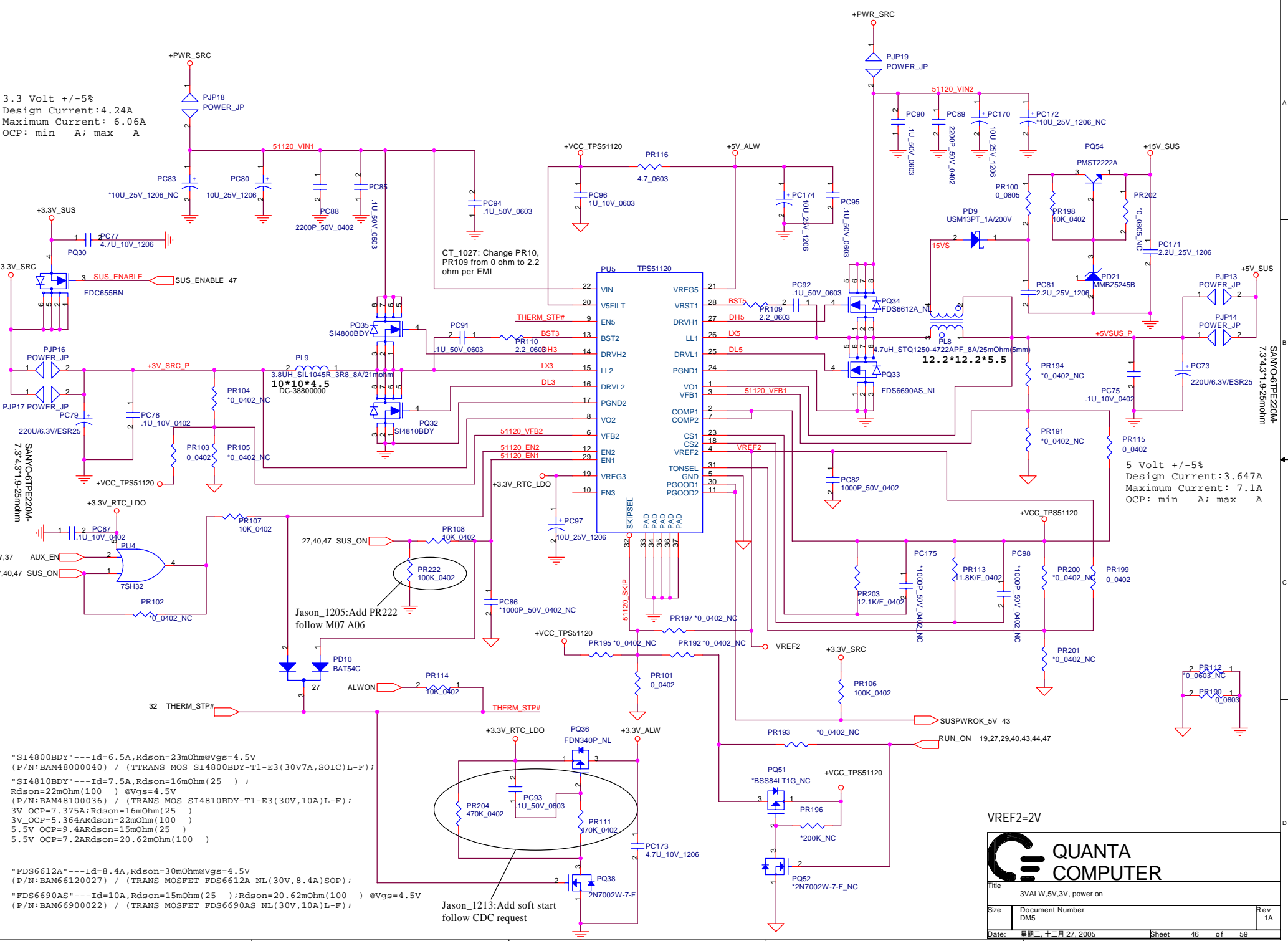
"SI4800BDY"---Id=6.5A,Rdson=23mOhm@Vgs=4.5V  
 (P/N:BAM48000040) / (TRANS MOS SI4800BDY-T1-E3(30V7A,SOIC)L-F);  
 "SI4810BDY"---Id=7.5A,Rdson=16mOhm(25);  
 Rdson=22mOhm(100) @Vgs=4.5V  
 (P/N:BAM48100036) / (TRANS MOS SI4810BDY-T1-E3(30V,10A)L-F);  
 3V\_OCP=7.375A;Rdson=16mOhm(25)  
 3V\_OCP=5.364A;Rdson=22mOhm(100)  
 5.5V\_OCP=9.4A;Rdson=15mOhm(25)  
 5.5V\_OCP=7.2A;Rdson=20.62mOhm(100)

"FDS6612A"---Id=8.4A,Rdson=30mOhm@Vgs=4.5V  
 (P/N:BAM66120027) / (TRANS MOSFET FDS6612A\_NL(30V,8.4A)SOP);  
 "FDS6690AS"---Id=10A,Rdson=15mOhm(25);Rdson=20.62mOhm(100) @Vgs=4.5V  
 (P/N:BAM66900022) / (TRANS MOSFET FDS6690AS\_NL(30V,10A)L-F);

Jason\_1213: Add soft start  
 follow CDC request

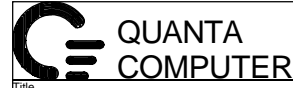
Jason\_1205: Add PR222  
 follow M07 A06

CT\_1027: Change PR10,  
 PR109 from 0 ohm to 2.2  
 ohm per EMI

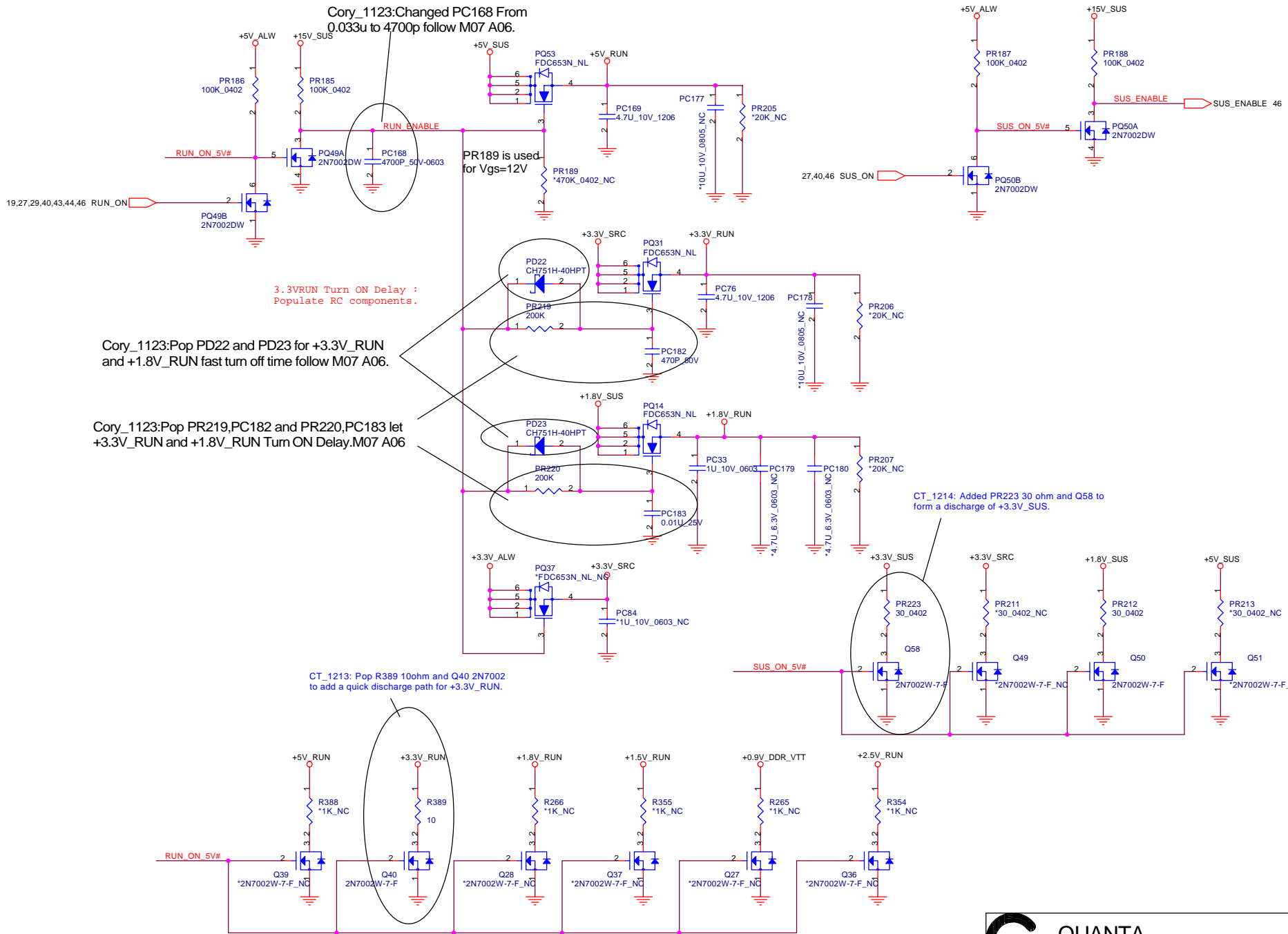


5 Volt +/-5%  
 Design Current: 3.647A  
 Maximum Current: 7.1A  
 OCP: min A; max A

VREF2=2V



Title 3VALW.5V.3V. power on		
Size	Document Number DM5	Rev 1A
Date:	星期三, 十二月 27, 2005	Sheet 46 of 59



Cory\_1123:Changed PC168 From 0.033u to 4700p follow M07 A06.

3.3VRUN Turn ON Delay :  
Populate RC components.

Cory\_1123:Pop PD22 and PD23 for +3.3V\_RUN  
and +1.8V\_RUN fast turn off time follow M07 A06.

Cory\_1123:Pop PR219,PC182 and PR220,PC183 let  
+3.3V\_RUN and +1.8V\_RUN Turn ON Delay.M07 A06

CT\_1214: Added PR223 30 ohm and Q58 to  
form a discharge of +3.3V\_SUS.

CT\_1213: Pop R389 10ohm and Q40 2N7002  
to add a quick discharge path for +3.3V\_RUN.

Reserve discharge path

**QUANTA COMPUTER**

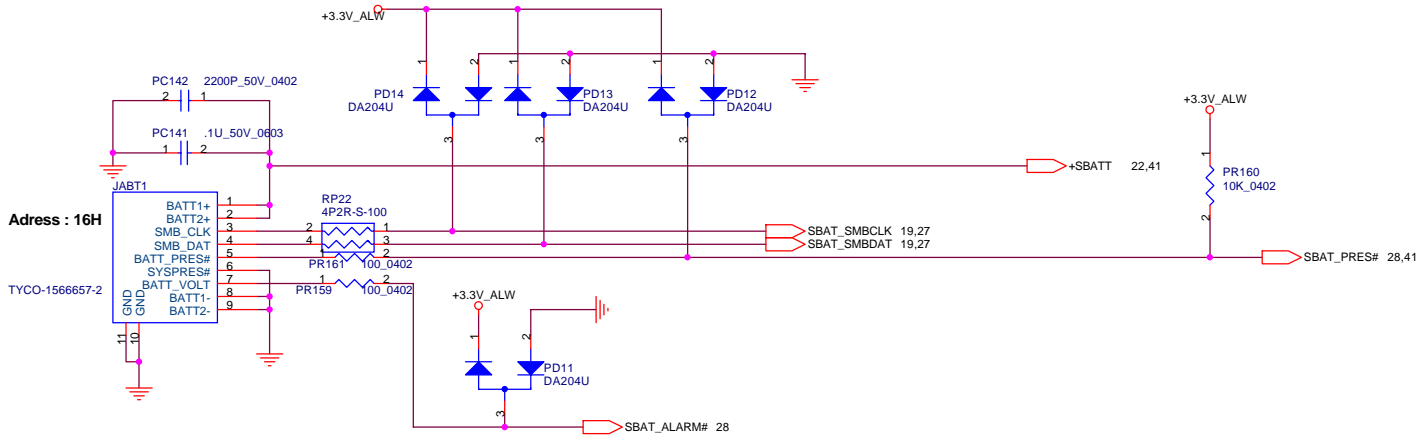
Title: RUN POWER SW

Size: DM5	Document Number: 1A	Rev: 1A
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Date: 星期二, 十二月 27, 2005      Sheet 47 of 59

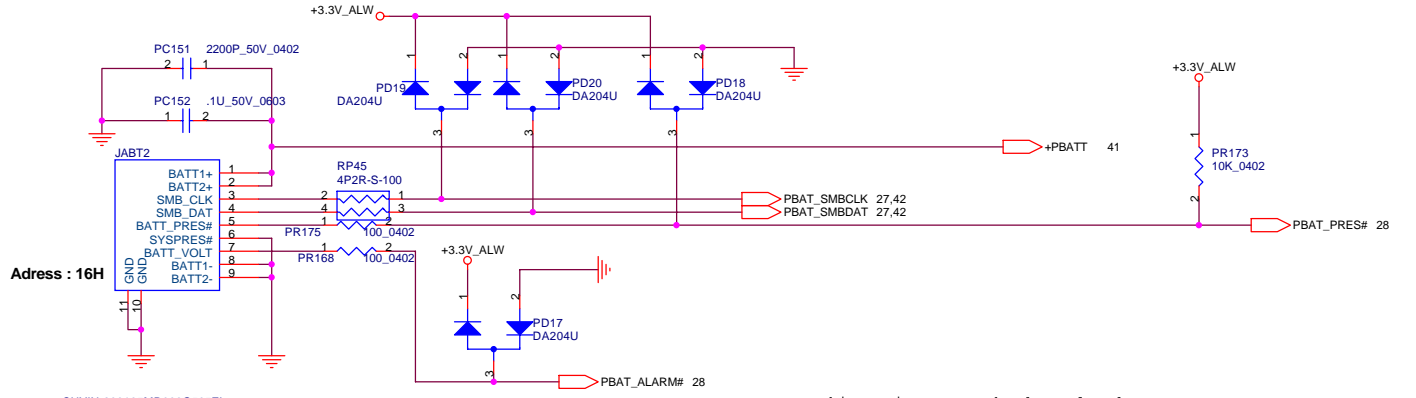
Address : 16H

TYCO-1566657-2



Address : 16H

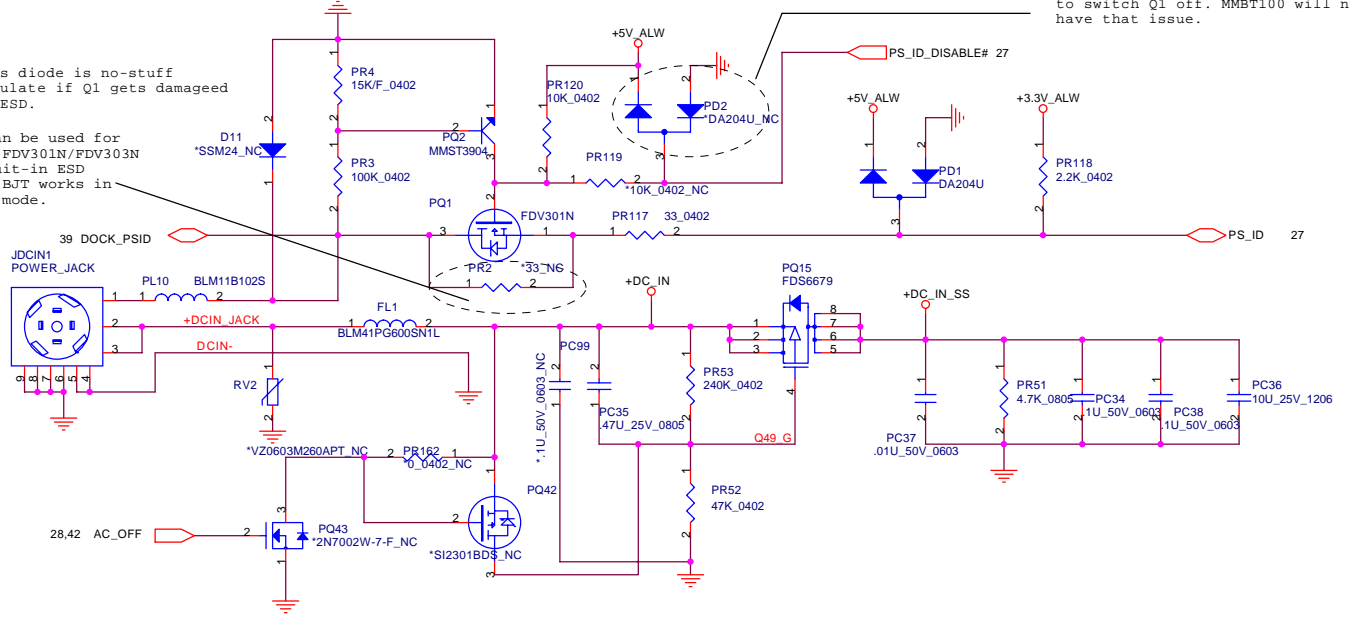
SUYIN-200185MR009G505ZL



This resistor must be depopulated if FDV301N/FDV303 are used to avoid a 1.36mA constant current drain from +3VALW. Thus, Bios will not be to switch Q1 off. MMBT100 will not have that issue.

This diode is no-stuff populate if Q1 gets damaged by ESD.

Three transistor can be used for Q1 (pin compatible): FDV301N/FDV303N has low Vgs\_on w/built-in ESD protection. MMBT100 BJT works in reverse conduction mode.



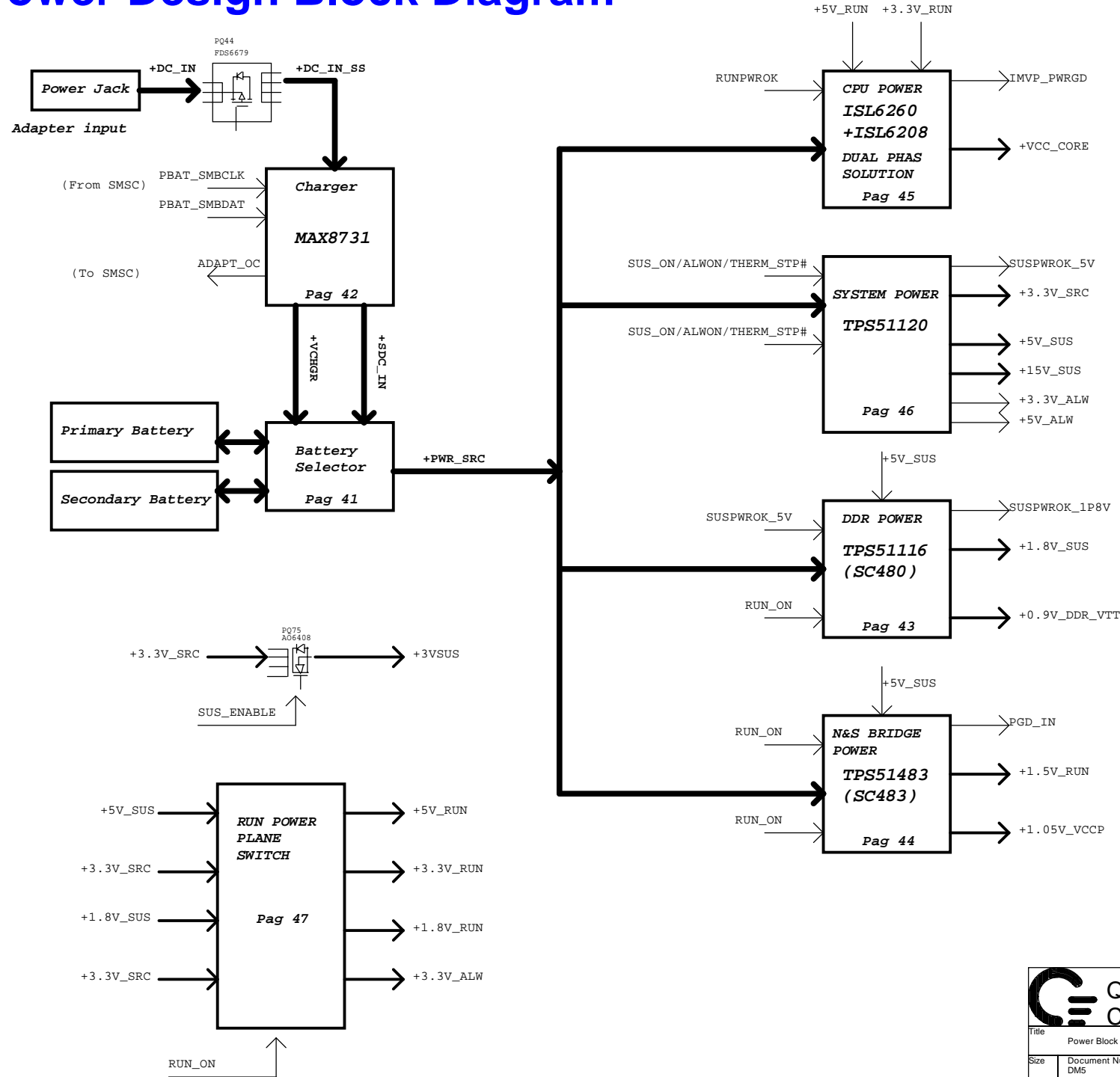
**QUANTA COMPUTER**

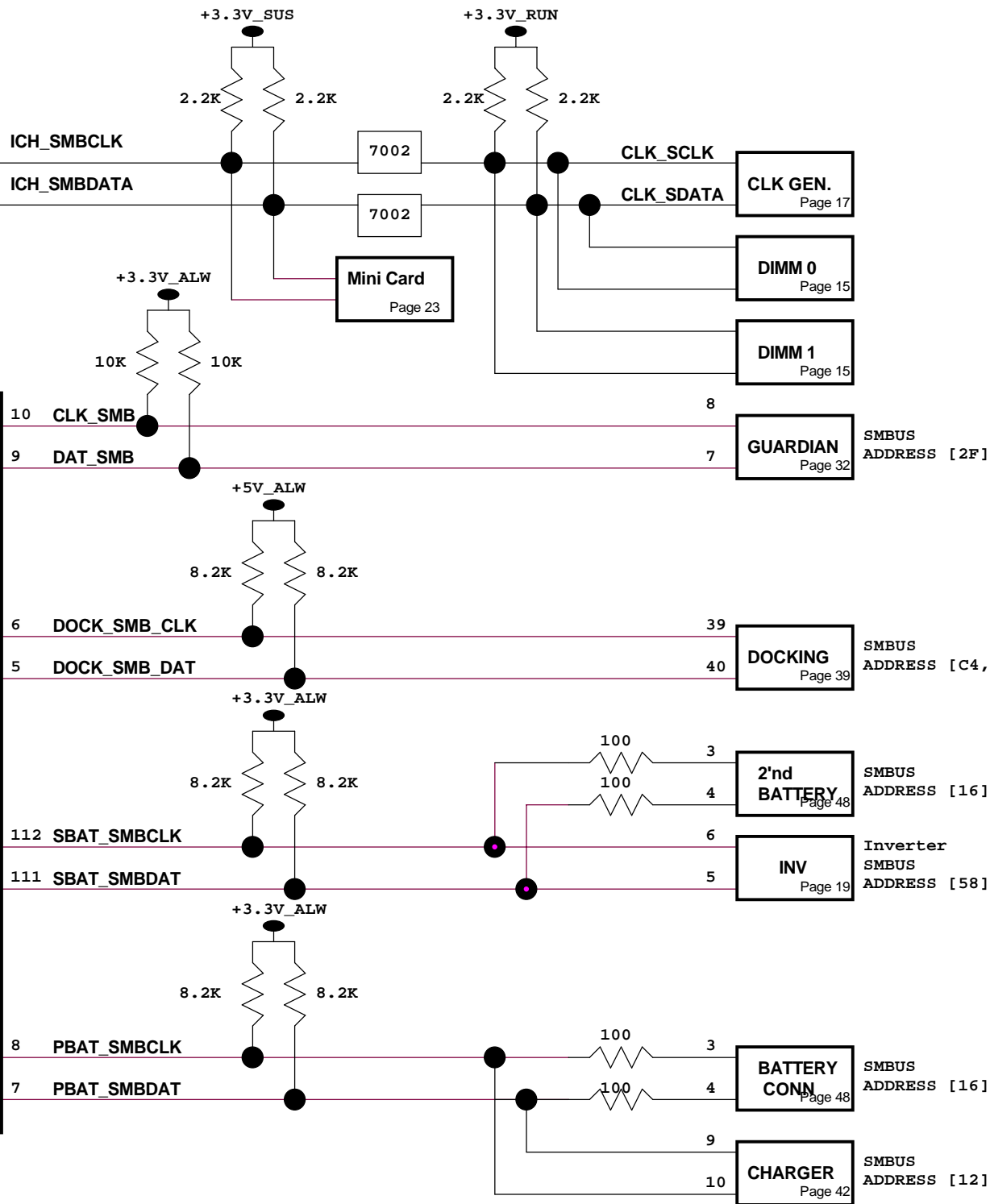
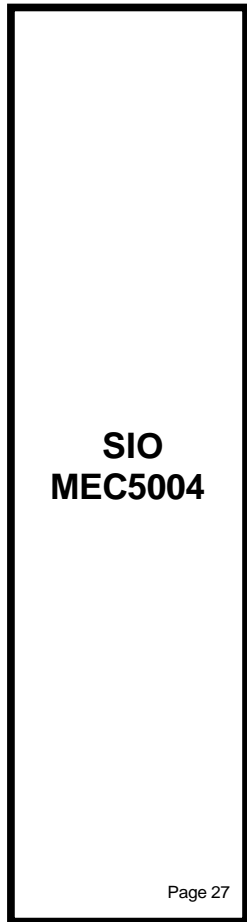
Title: DCIN,BATT CONNECTOR

Size: DM5	Document Number: DM5	Rev: 1A
Date: 星期三, 十二月 27, 2005	Sheet: 48	of 59



# DM5 Power Design Block Diagram





**QUANTA COMPUTER**

Title		
SMBUS Block Diagram		
Size	Document Number	Rev
	DMS	1A
Date: 星期二, 十二月 27, 2005		
Sheet		of
50		59