

MODEL NAME : *KML50*

PCB NO : *LA-4596P (DA60000B710)*

BOM P/N : *11*

Half Penny Bridge 15.4

# Compal Confidential

Schematic Document

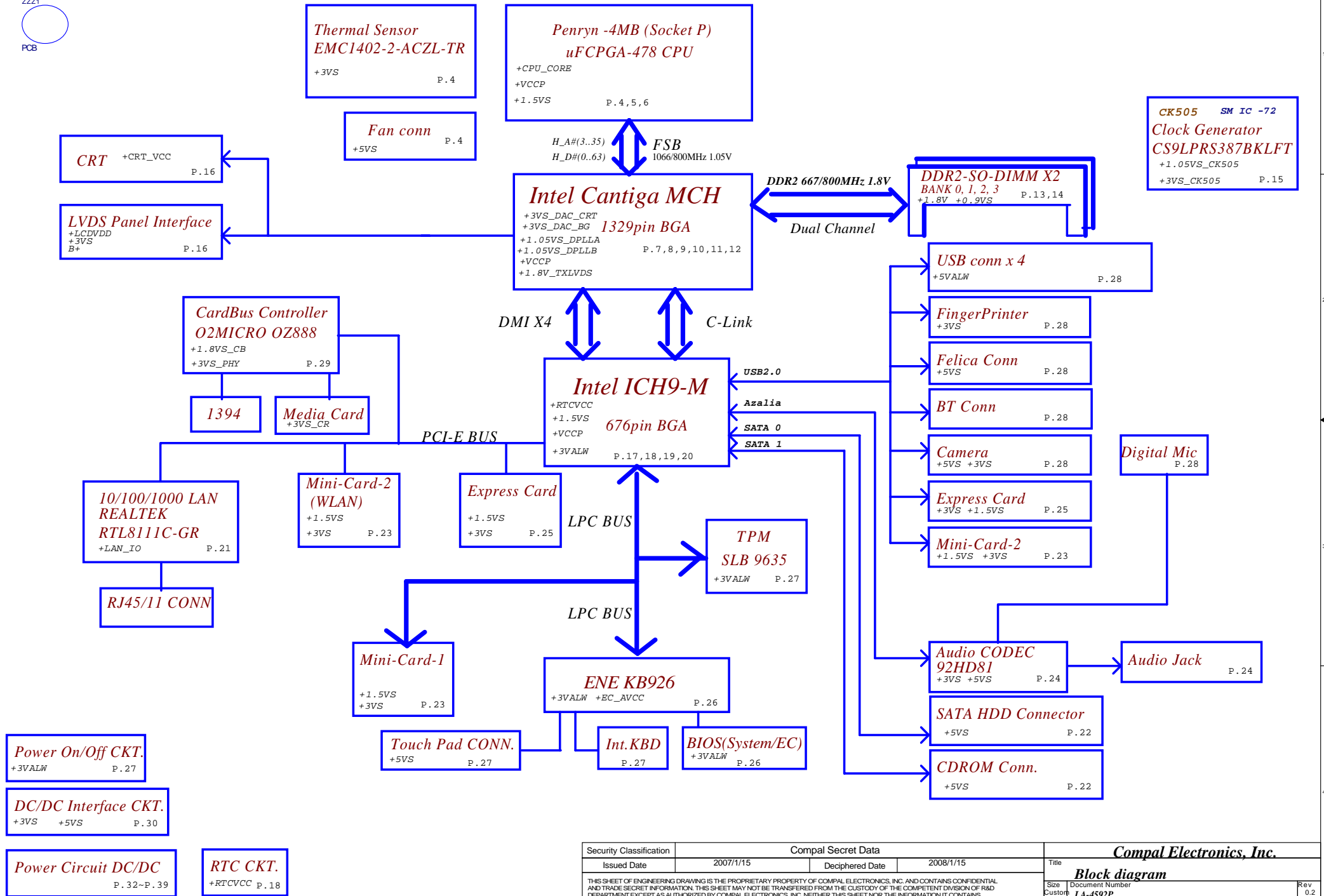
## Cantiga + ICH9

2009 / 01 / 14 Rev:1.0(A00)

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# Half Penny Bridge 15.4

File Name : LA-4596P



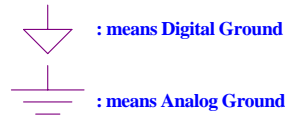
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**Voltage Rails**    **O MEANS ON**    **X MEANS OFF**

power plane / State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE +1.8VS
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

**Symbol Note :**



@ : means just reserve , no build  
CONN@ : means ME CONN compont.  
TPM@:TPM compont

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	GLAN RTL8111DL
Lane 3	MINI CARD-2 WLAN
Lane 4	EXPRESS CARD
Lane 5	CARD READER OZ888
Lane 6	NA

SATA	DESTINATION
Lane 0	HDD
Lane 1	ODD
Lane 4	NA
Lane 5	NA

ICH9-M	USB PORT#	DESTINATION
	0	JUSBP1
1	CAMERA	
2	JUSBP3                      Top	
3	Felica	
4	Blue Tooth	
5	Finger Printer	
6	JMINI2-WLAN	
7	Express card	
8	JUSBP3                      Bottom	
9	JMINI1-WWAN	
10	JUSBP4	
11	NA	

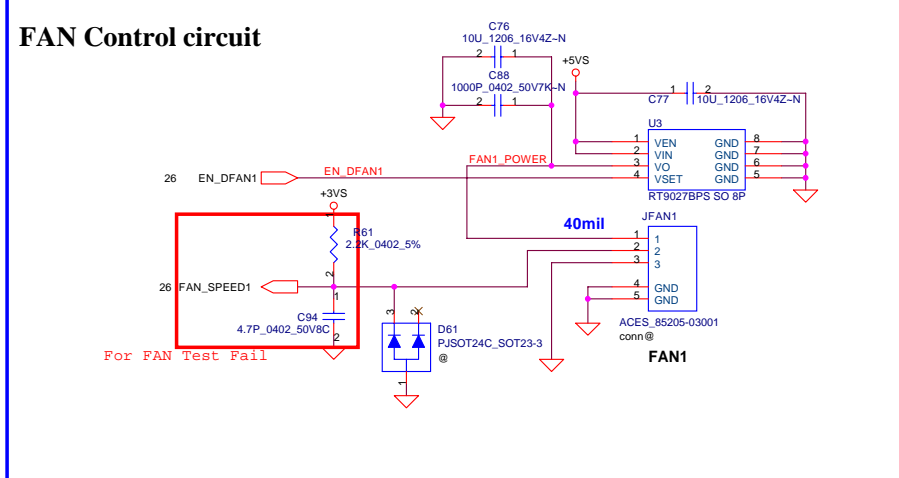
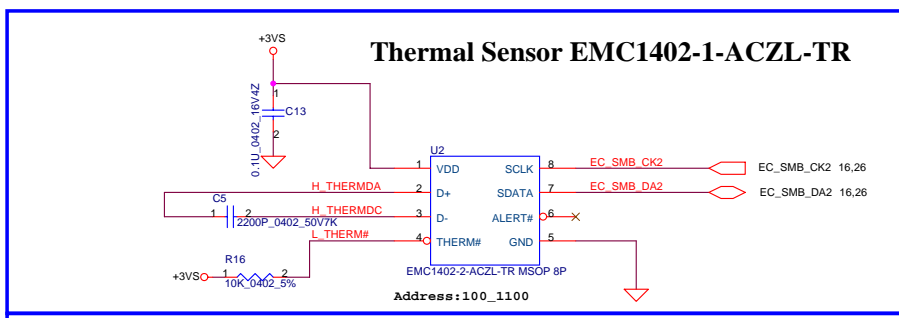
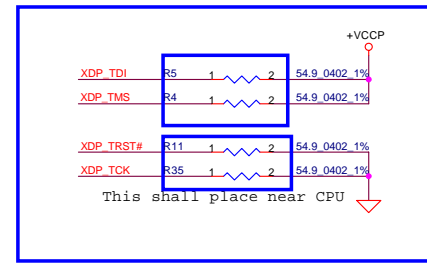
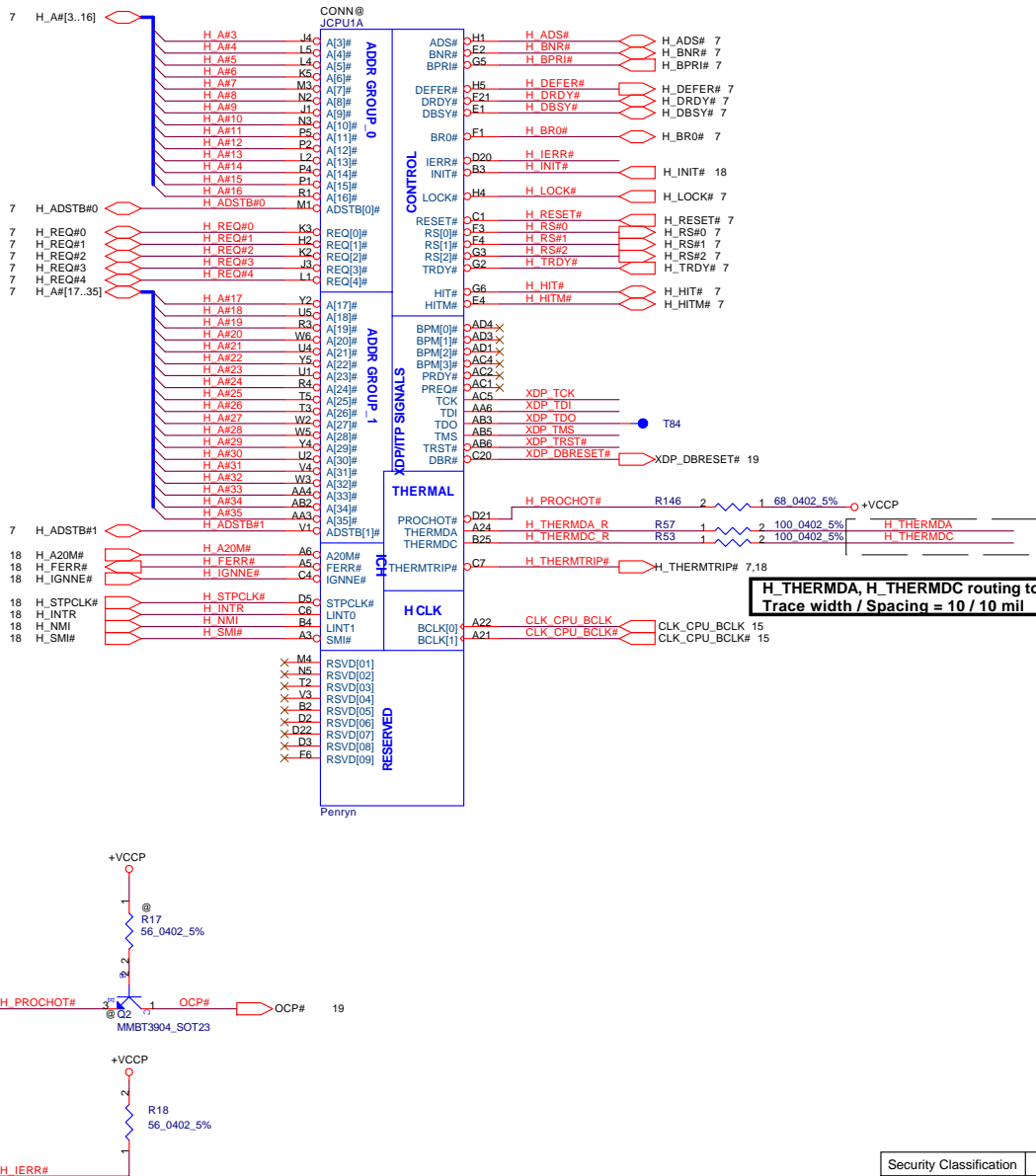
SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

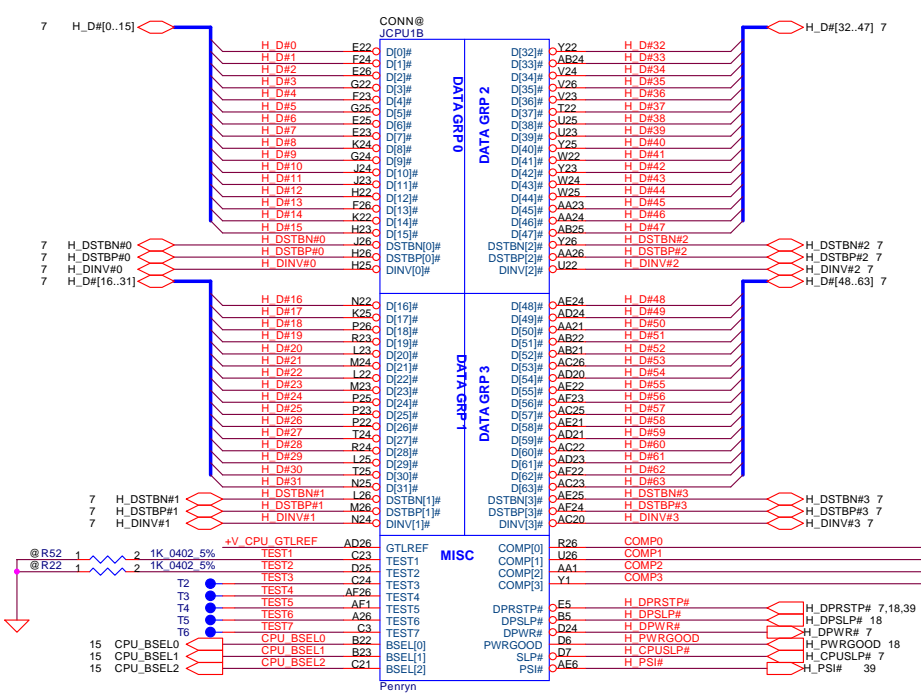
**I2C / SMBUS ADDRESSING**

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

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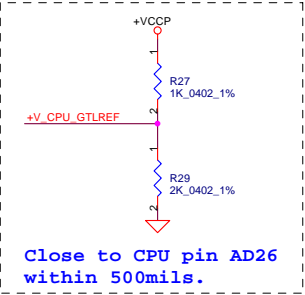
Security Classification	Compal Secret Data		Title	<b>Compal Electronics, Inc.</b>	
Issued Date	2006/02/13	Deciphered Date	2006/03/10	Penryn(1/3)-AGTL+/ITP-XDP	
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layout note: Rout H\_DPRSTP# from ICH9 to IMPV6 then to GMCH & CPU  
 layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

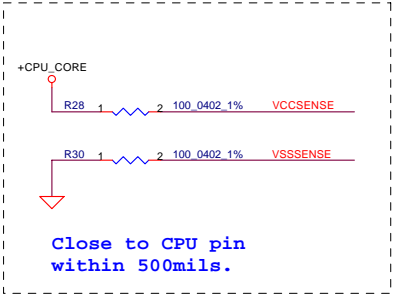
Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4



Close to CPU pin AD26 within 500mils.

For 6 layer  
 $Z=27.4 \text{ ohm}$   
 VCCSENSE, VSSSENSE/ 14mils (MS),  
 16mils (SL) width, 7mils space, 25mils  
 space to other signals Mismatch =25mils.

Length match within 25 mils.  
 The trace width/space/other is 20/7/25.

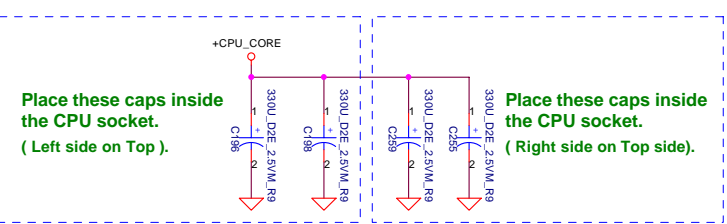
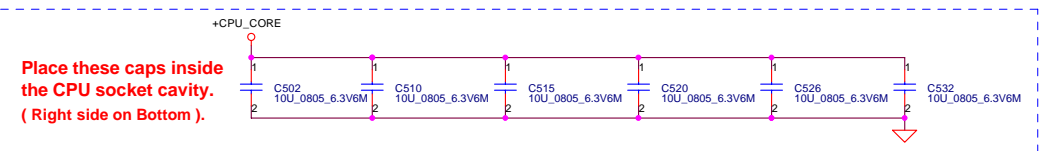
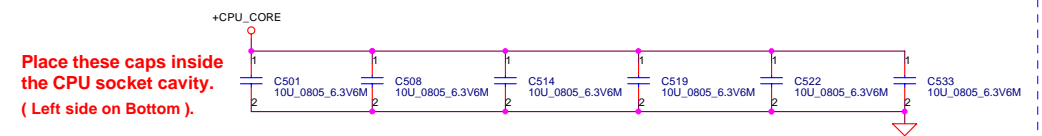
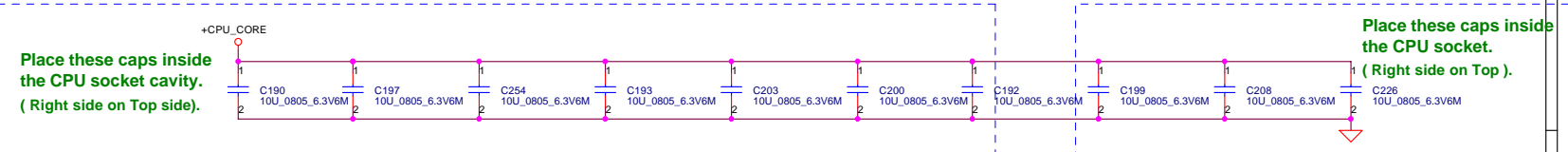
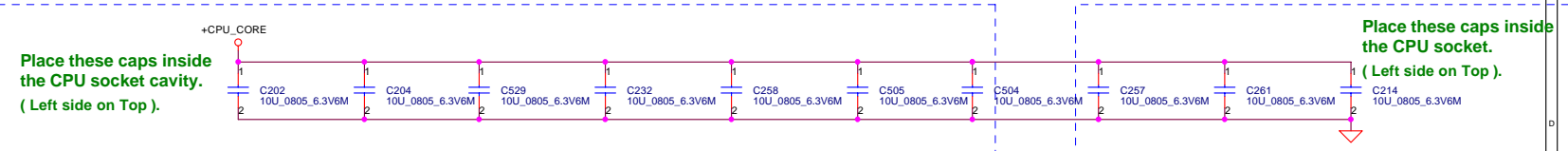


Close to CPU pin within 500mils.

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**High Frequency Decoupling**  
**10uF 0805 X5R -> 85 degree.**

CONN@	JCPU1D				
A4	VSS001	VSS082	P6		
A8	VSS002	VSS083	P24		
A11	VSS003	VSS084	R2		
A14	VSS004	VSS085	R5		
A16	VSS005	VSS086	R22		
A19	VSS006	VSS087	R25		
A23	VSS007	VSS088	T1		
AE2	VSS008	VSS089	T4		
B6	VSS009	VSS090	T7		
B8	VSS010	VSS091	T23		
B11	VSS011	VSS092	T26		
B13	VSS012	VSS093	U3		
B16	VSS013	VSS094	U6		
B19	VSS014	VSS095	U21		
B21	VSS015	VSS096	U24		
B24	VSS016	VSS097	V5		
C5	VSS017	VSS098	V22		
C8	VSS018	VSS099	V25		
C11	VSS019	VSS100	W1		
C14	VSS020	VSS101	W4		
C16	VSS021	VSS102	W23		
C19	VSS022	VSS103	W26		
C2	VSS023	VSS104	Y3		
C22	VSS024	VSS105	Y6		
C25	VSS025	VSS106	Y21		
D4	VSS026	VSS107	Y24		
D8	VSS027	VSS108	AA2		
D11	VSS028	VSS109	AA5		
D13	VSS029	VSS110	AA8		
D16	VSS030	VSS111	AA11		
D19	VSS031	VSS112	AA14		
D23	VSS032	VSS113	AA16		
D26	VSS033	VSS114	AA19		
E3	VSS034	VSS115	AA22		
E6	VSS035	VSS116	AA25		
ER	VSS036	VSS117	AB1		
ER	VSS037	VSS118	AB4		
E11	VSS038	VSS119	AB8		
E14	VSS039	VSS120	AB11		
E16	VSS040	VSS121	AB13		
E19	VSS041	VSS122	AB16		
E21	VSS042	VSS123	AB19		
E24	VSS043	VSS124	AB23		
F6	VSS044	VSS125	AB26		
FR	VSS045	VSS126	AC3		
F11	VSS046	VSS127	AC6		
F13	VSS047	VSS128	AC8		
F16	VSS048	VSS129	AC11		
F19	VSS049	VSS130	AC14		
F2	VSS050	VSS131	AC16		
F25	VSS051	VSS132	AC19		
F22	VSS052	VSS133	AC21		
G4	VSS053	VSS134	AC24		
G1	VSS054	VSS135	AD2		
G23	VSS055	VSS136	AD5		
G26	VSS056	VSS137	AD8		
H3	VSS057	VSS138	AD11		
H6	VSS058	VSS139	AD13		
H21	VSS059	VSS140	AD16		
J2	VSS060	VSS141	AD19		
J5	VSS061	VSS142	AD22		
J22	VSS062	VSS143	AD25		
J25	VSS063	VSS144	AE1		
K1	VSS064	VSS145	AE4		
K4	VSS065	VSS146	AE8		
K23	VSS066	VSS147	AE11		
K26	VSS067	VSS148	AE14		
L3	VSS068	VSS149	AE16		
L6	VSS069	VSS150	AE19		
L21	VSS070	VSS151	AE23		
L24	VSS071	VSS152	AE26		
M2	VSS072	VSS153	A2		
M22	VSS073	VSS154	AF6		
M5	VSS074	VSS155	AF8		
M25	VSS075	VSS156	AF11		
N1	VSS076	VSS157	AF13		
N4	VSS077	VSS158	AF16		
N23	VSS078	VSS159	AF19		
N26	VSS079	VSS160	AF21		
P3	VSS080	VSS161	A25		
	VSS081	VSS162	AF25		
		VSS163			



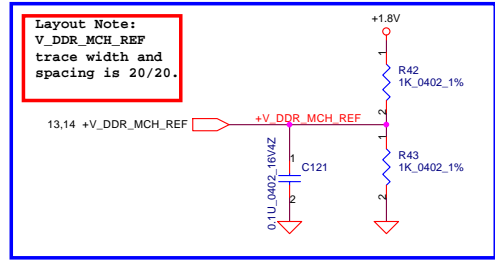
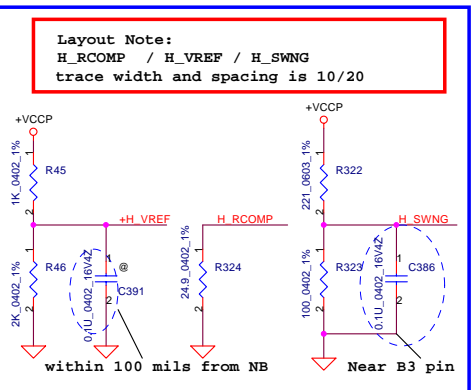
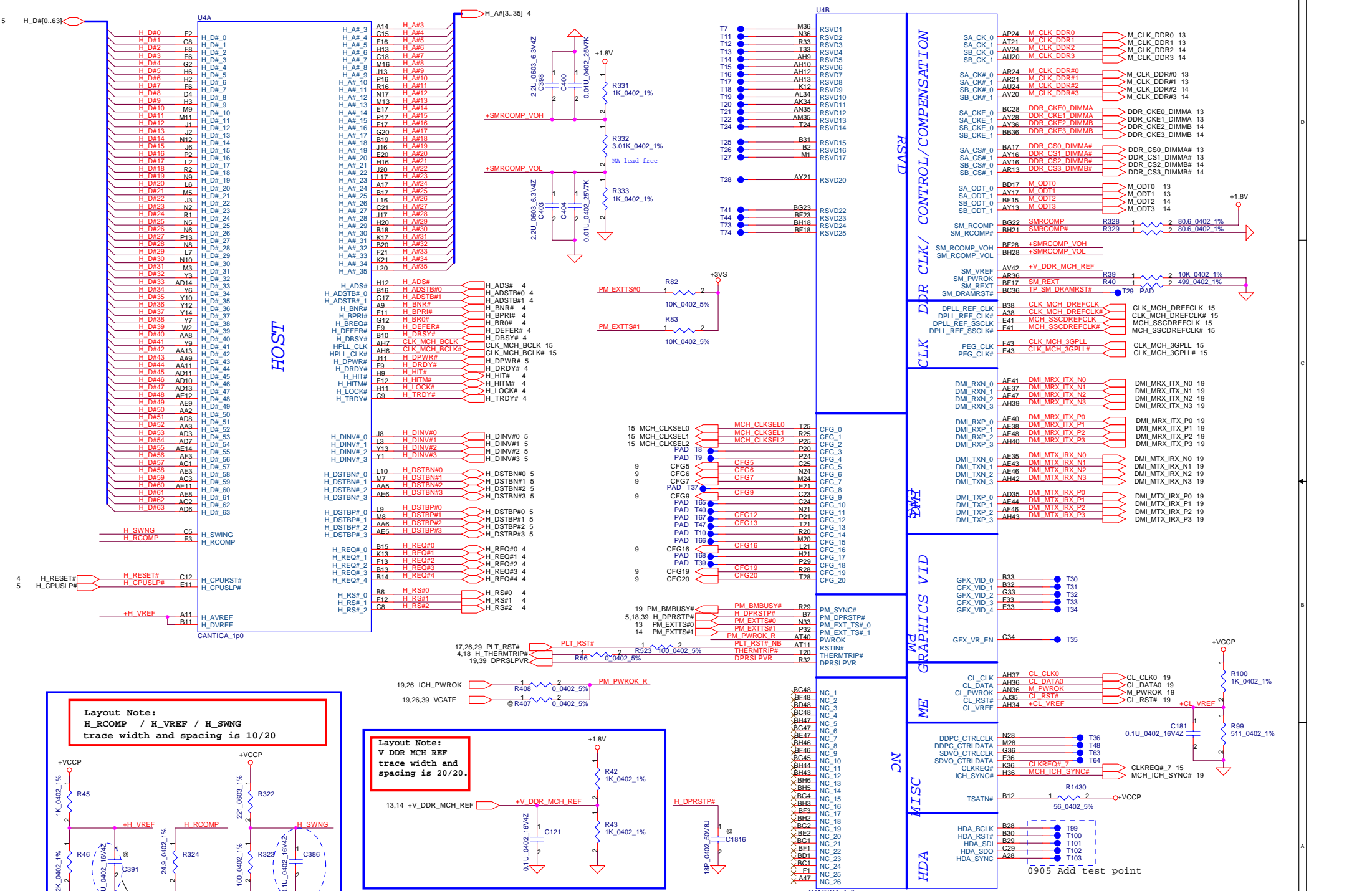
**ESR <= 1.5m ohm**  
**Capacitor > 880 uF**



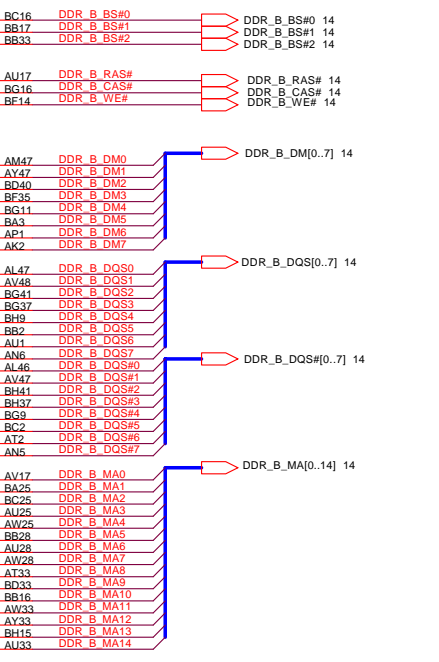
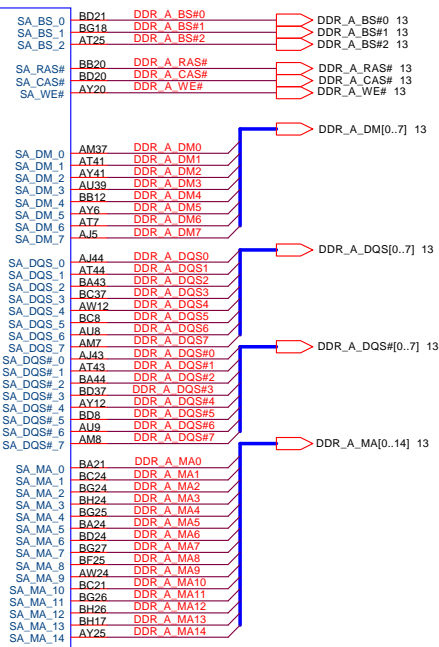
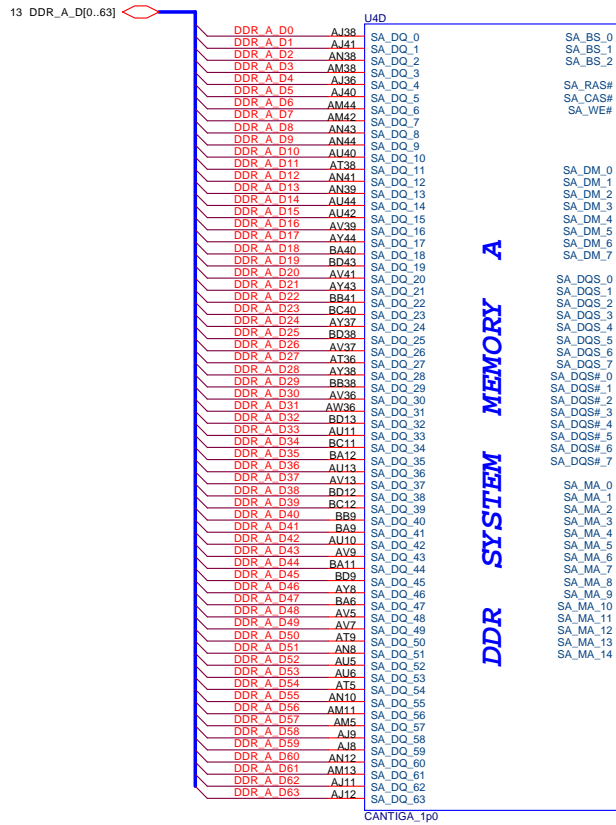
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<b>Penryn(3/3)-AGTL+/ITP-XDP</b>		
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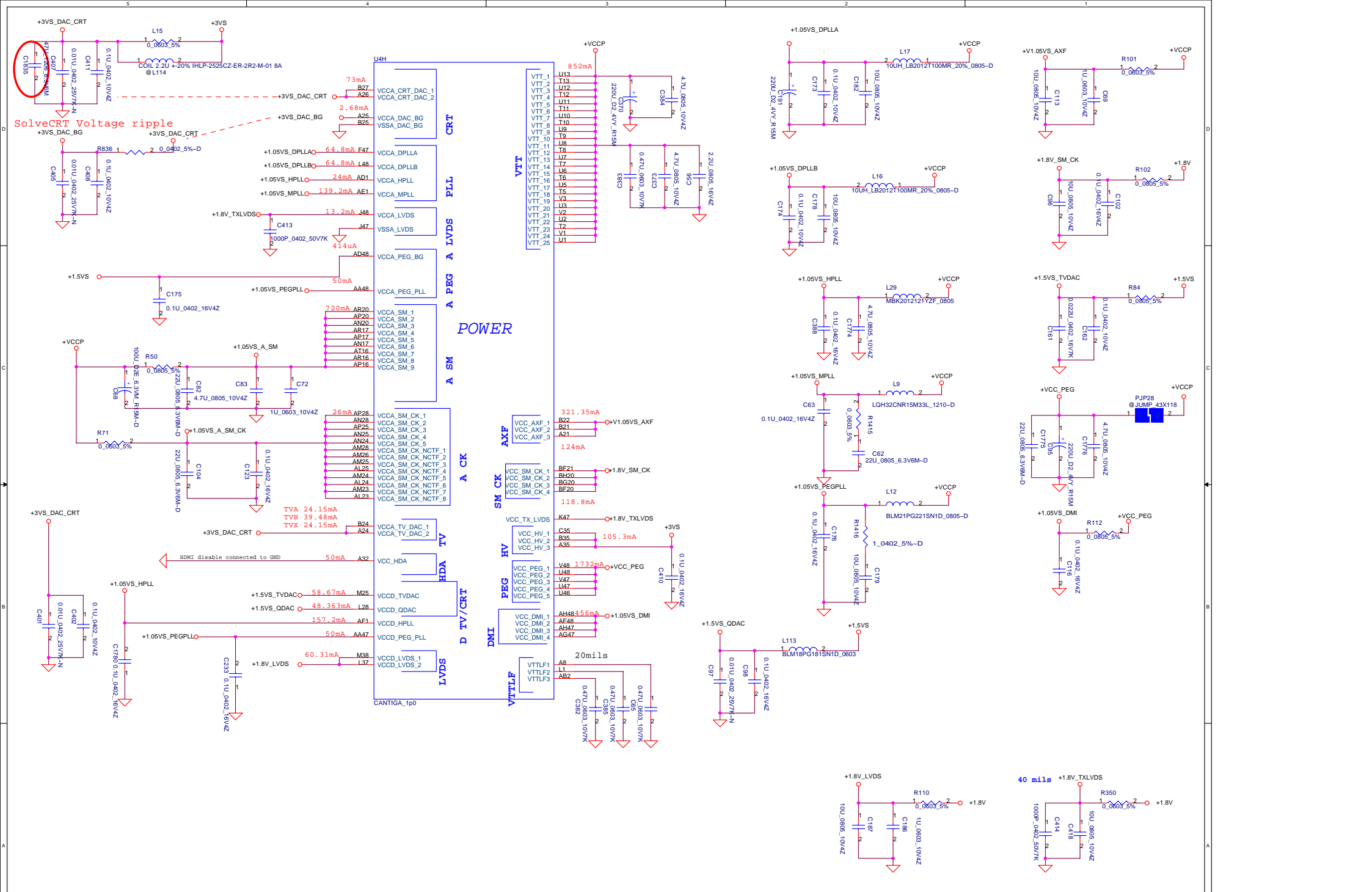
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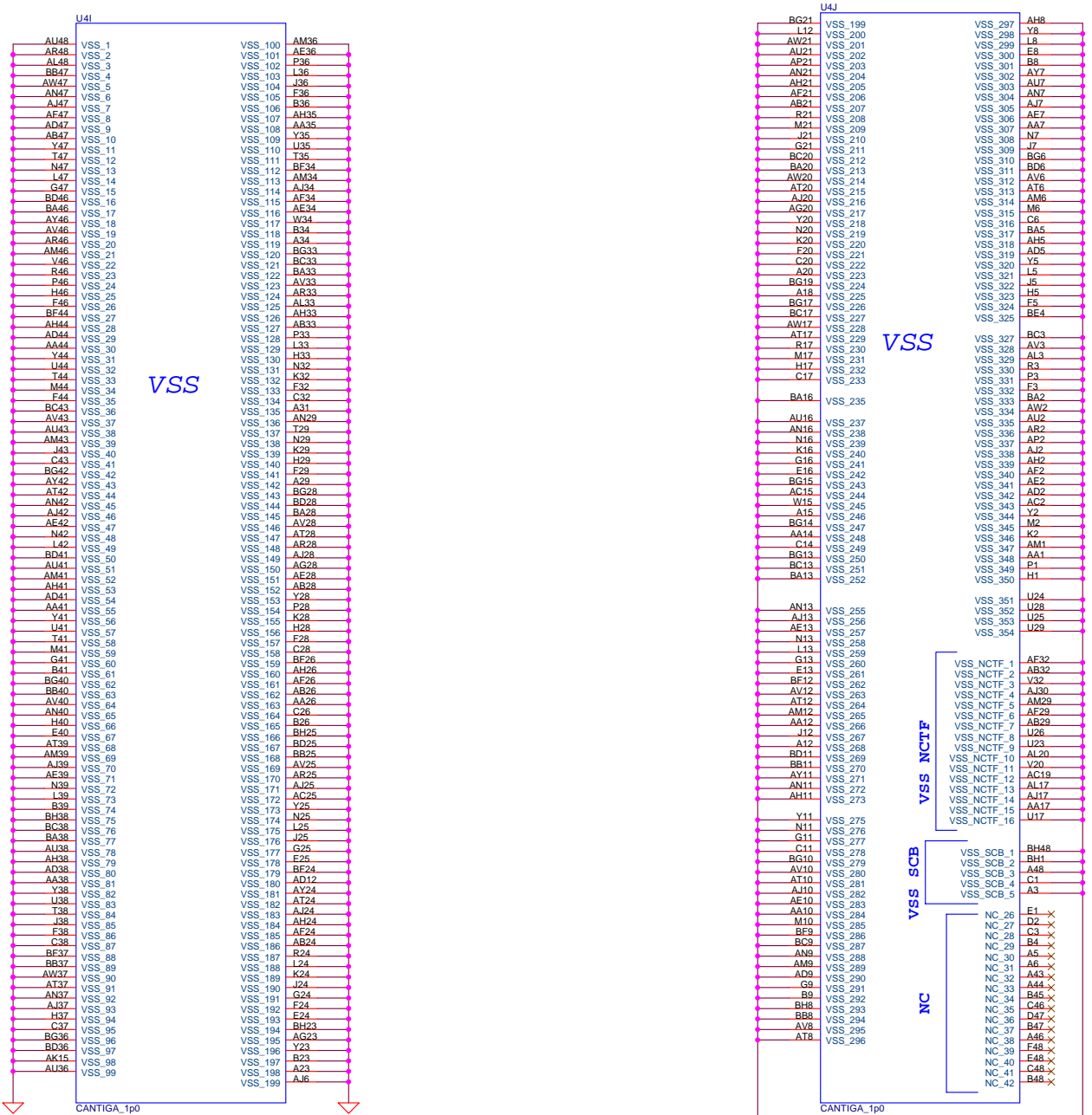




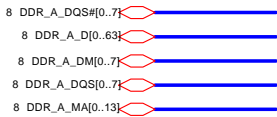
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<b>Cantiga(4/6)-PWR</b>	
Size	Document Number
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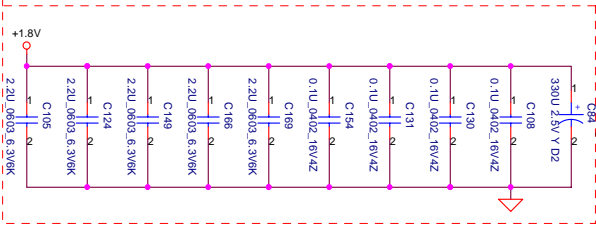




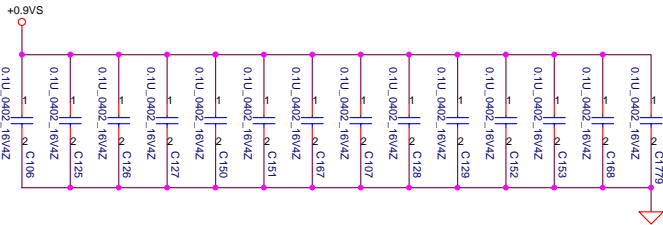
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Size	Document Number	Rev		
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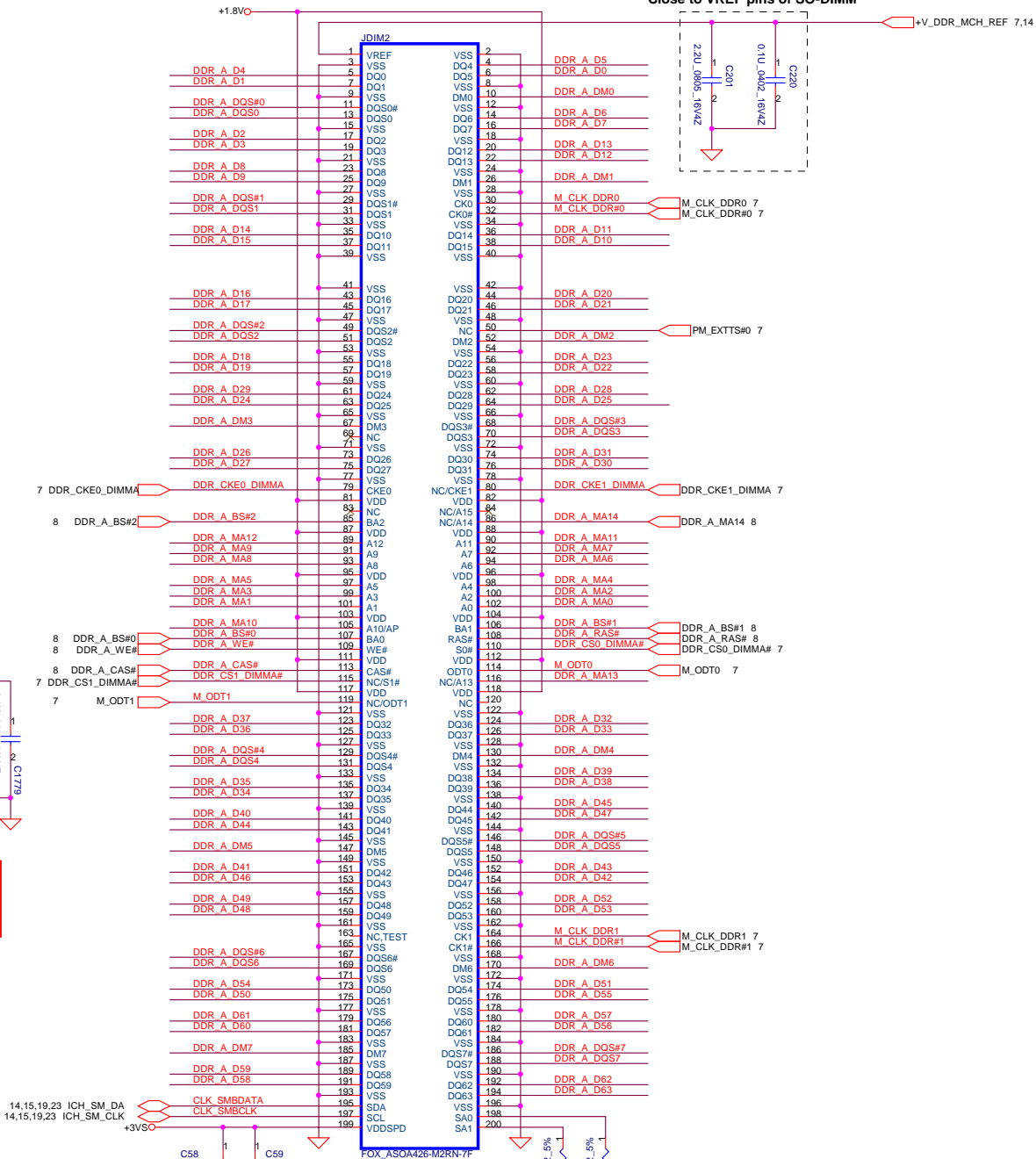
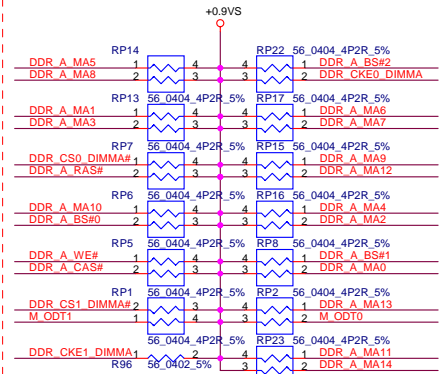
**Layout Note:**  
Place near JDIM1



**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9V

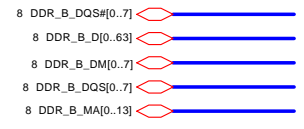


**Layout Note:**  
Place these resistor closely JP41, all trace length Max=1.5"

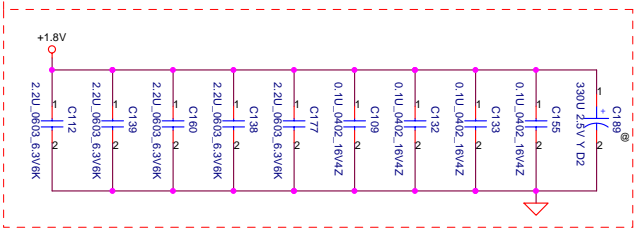


**SO-DIMM A  
REVERSE  
Bottom side**

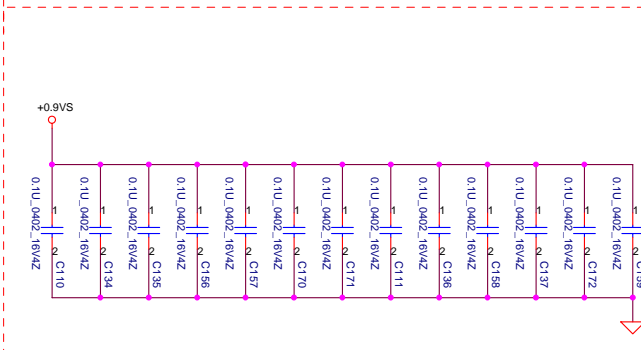
Security Classification		Compal Secret Data		Title		
Issued Date	2007/1/15	Deciphered Date	2008/1/15	DDR2 SO-DIMM I		
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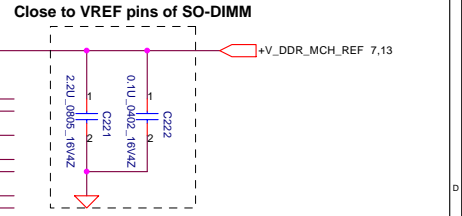
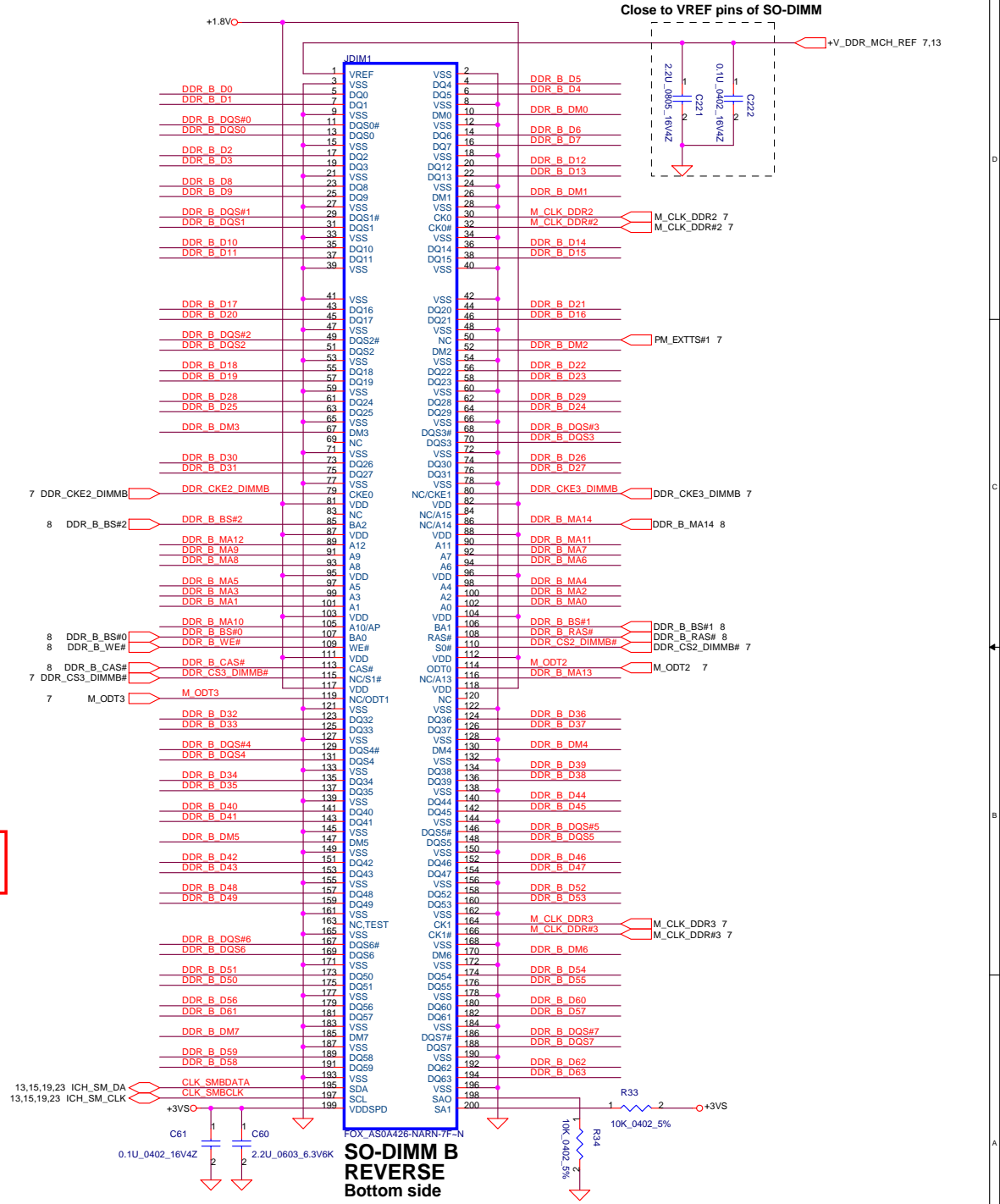
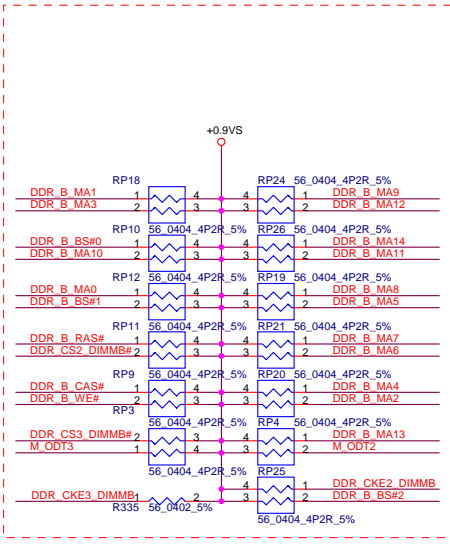
**Layout Note:**  
Place near JDIM2



**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9VS



**Layout Note:**  
Place these resistor closely JP42, all trace length Max=1.5"



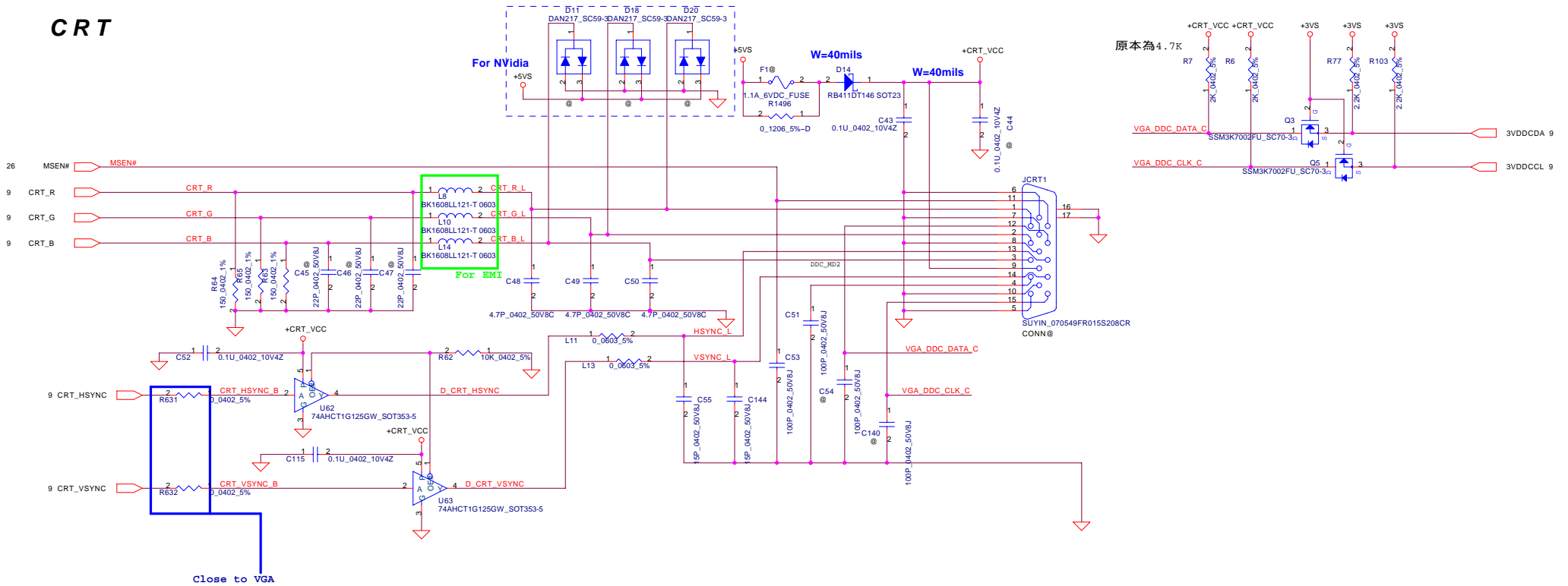
**SO-DIMM B  
REVERSE  
Bottom side**

Security Classification	Compal Secret Data		Title	
Issued Date	2007/1/15	Deciphered Date	2008/1/15	Document Number
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				Rev 0.2
Date: Thursday, February 19, 2009				Sheet 14 of 43

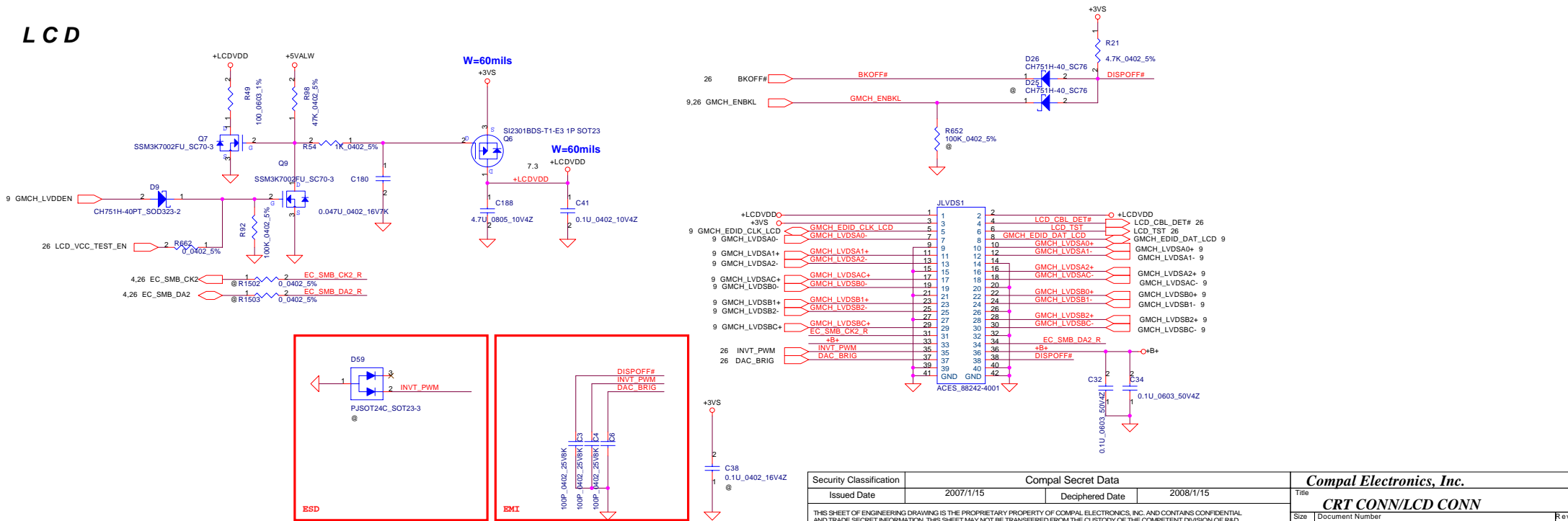
**Compal Electronics, Inc.**  
**DDR2 SO-DIMM II**  
LA-4592P



# CRT

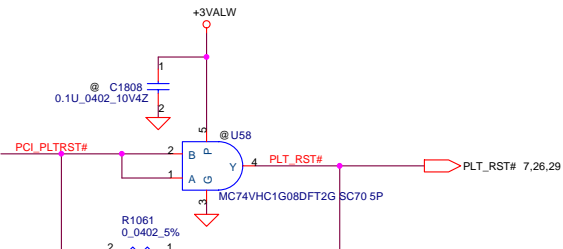
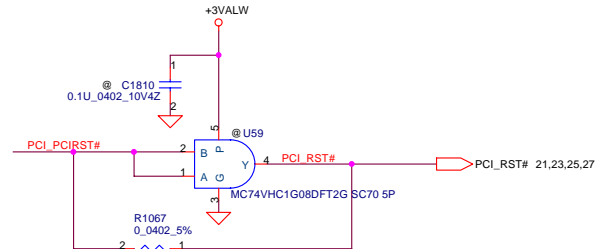
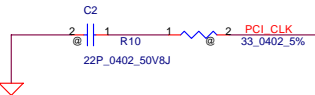
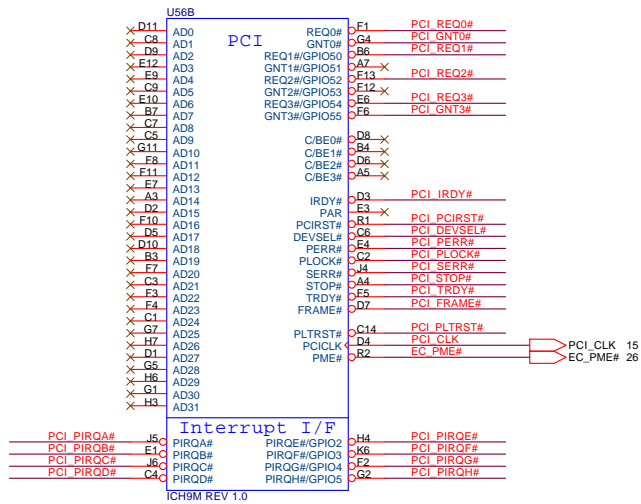
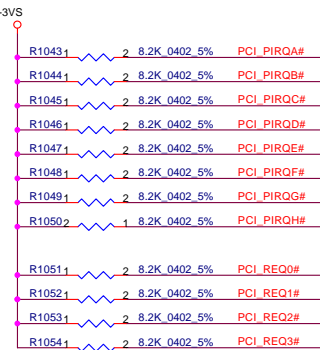
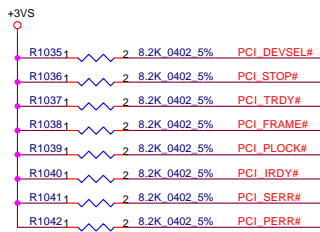


# LCD



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Issued Date	2007/1/15	Deciphered Date	2008/1/15	Title <b>CRT CONN/LCD CONN</b>	
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Size	Document Number	Date		Sheet	Rev
	LA-4592P	Thursday, February 19, 2009		16	0.2

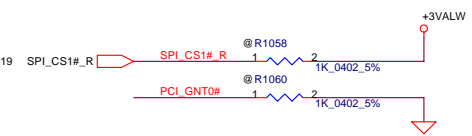




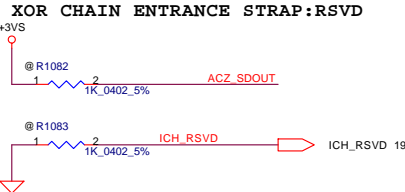
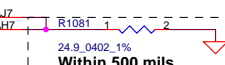
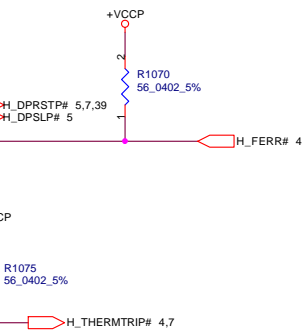
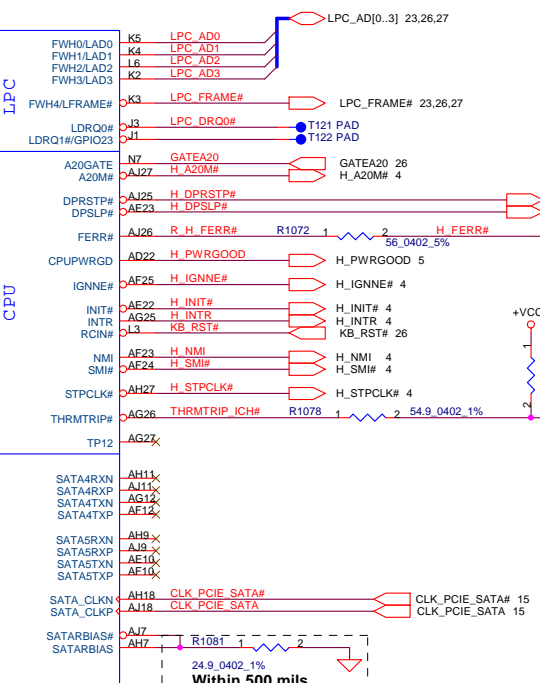
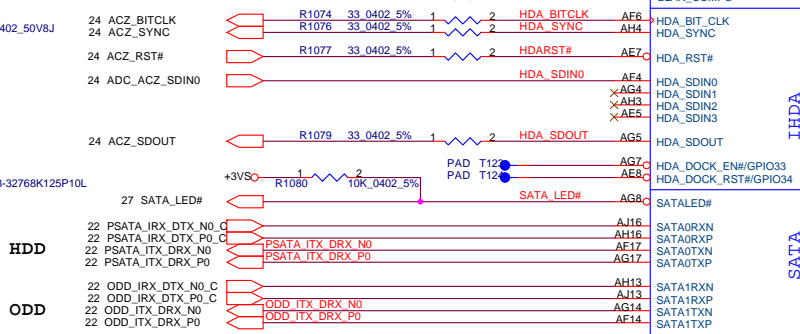
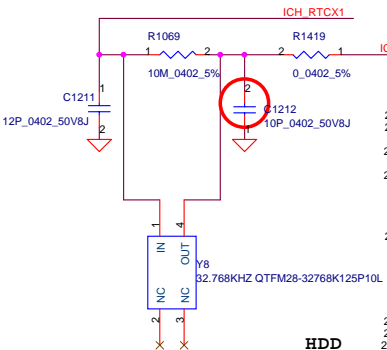
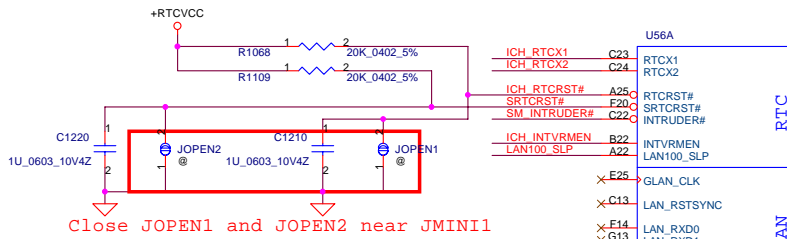
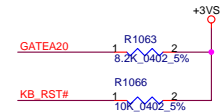
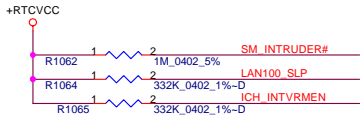
A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default *



Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



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Issued Date	2006/02/13	Deciphered Date	2006/03/10	LA-4592P	
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				LA-4592P	Rev 0.2
Date: Thursday, February 19, 2009				Sheet 17	of 43



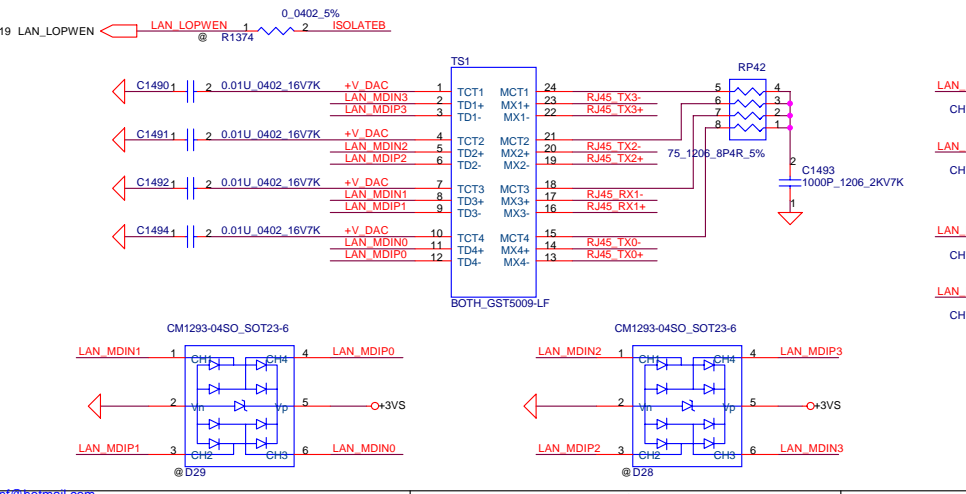
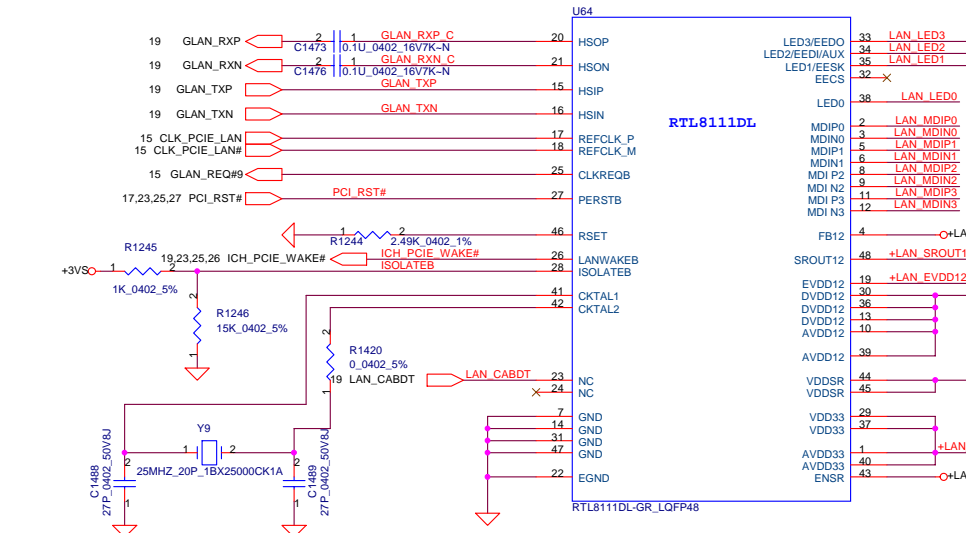
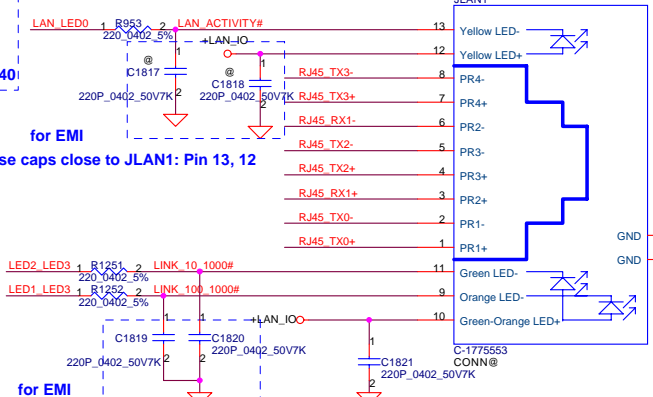
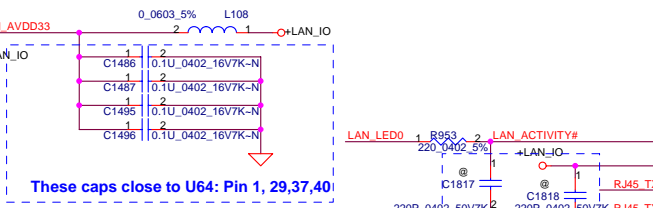
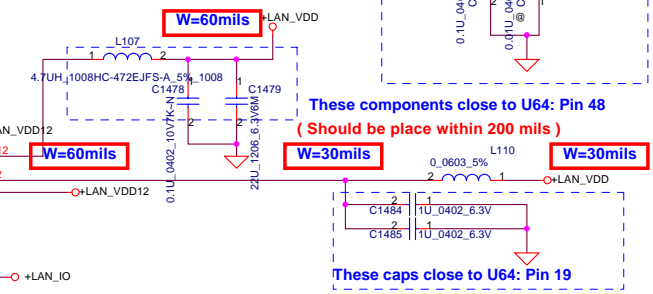
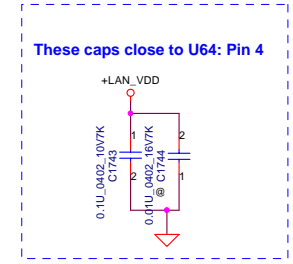
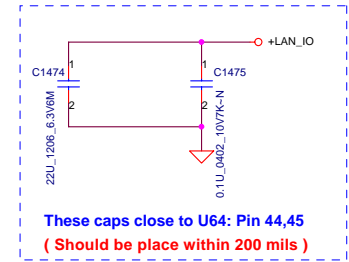
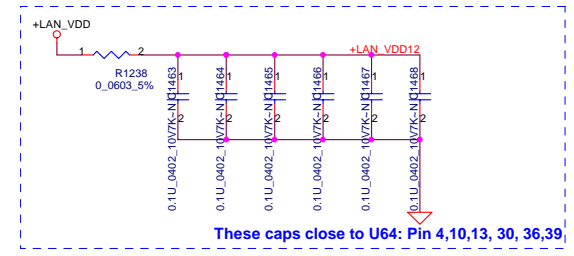
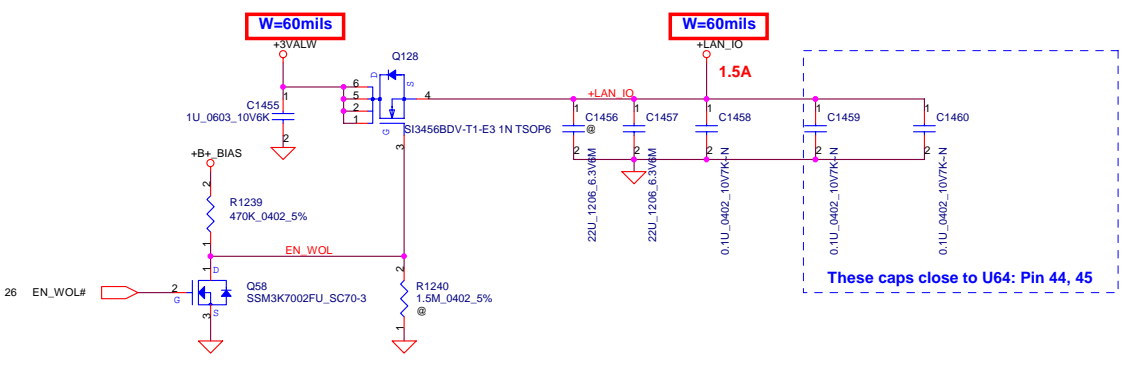
Security Classification	Compal Secret Data	
Issued Date	2006/02/13	Deciphered Date
		2006/03/10

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Title			<b>Compal Electronics, Inc.</b>	
Date			<b>ICH9(2/4) LAN,HD,IDE,LPC</b>	
Size	Document Number	Rev		
Custom	<b>LA-4592P</b>	0.2		
Date:	Thursday, February 19, 2009	Sheet	18	of 43

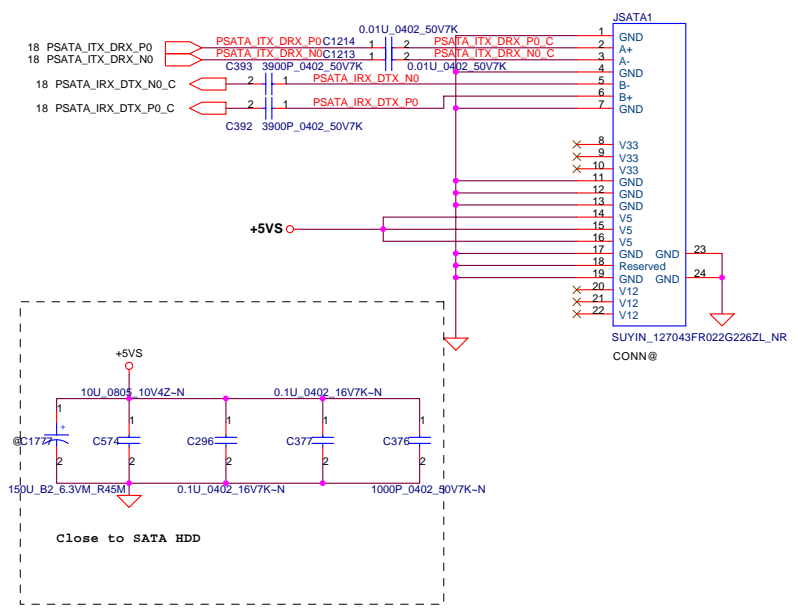




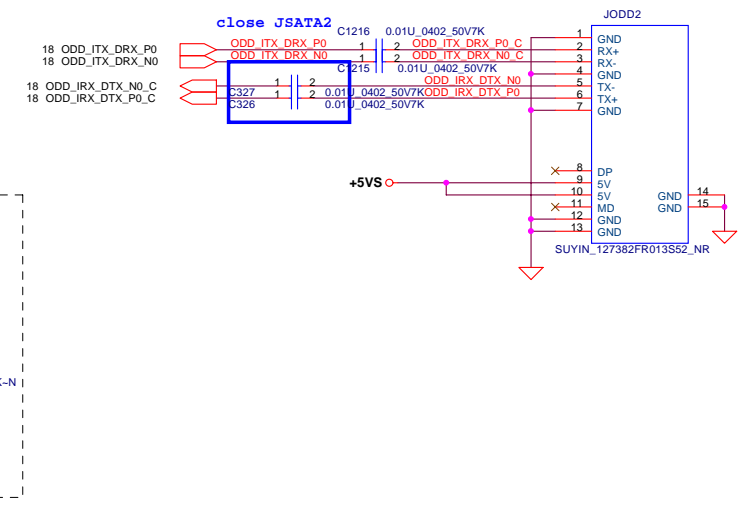


Security Classification		Compal Secret Data		Title	
Issued Date	2008/03/21	Deciphered Date	2009/03/21	Gigabit LAN RTL8111C	
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				LA-4592P	Rev 0.2
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# SATA HDD CONN

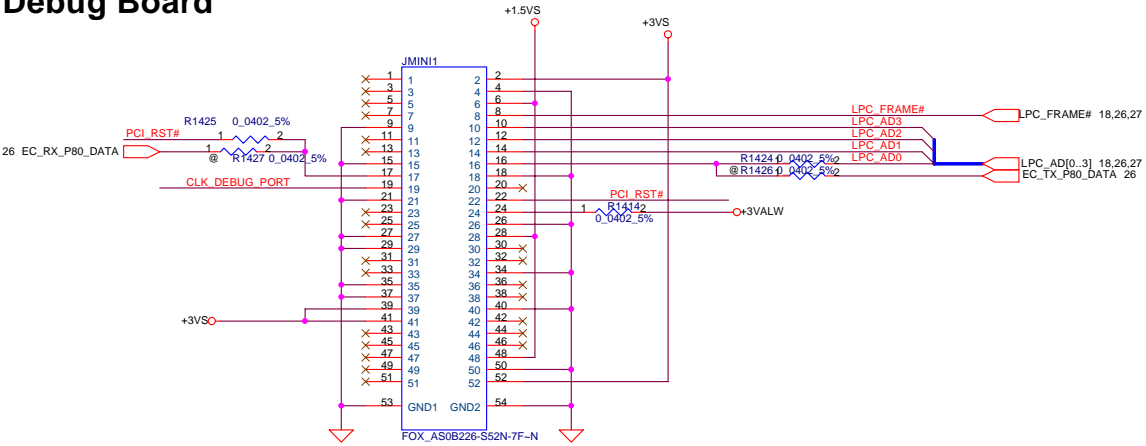


# SATA ODD CONN

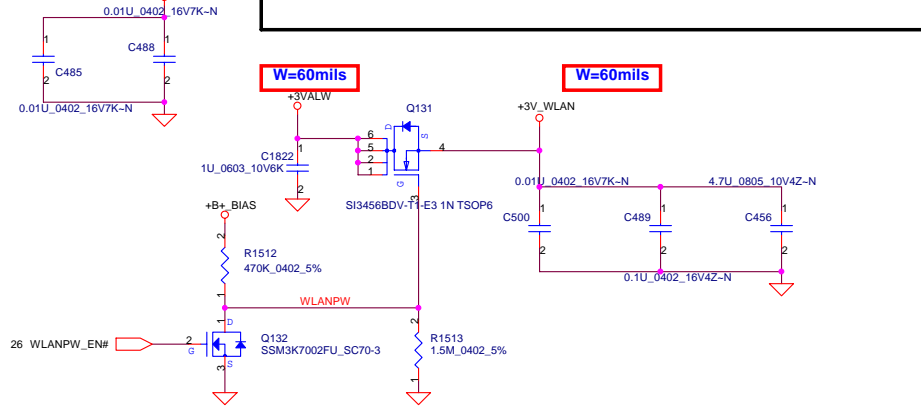
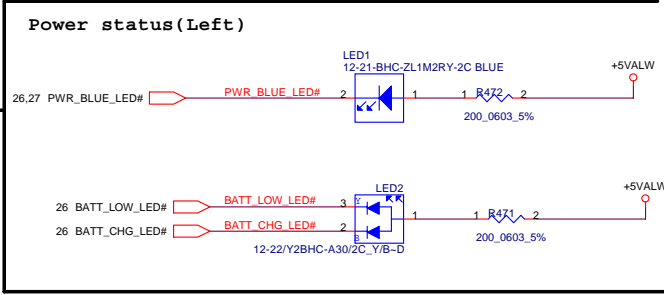
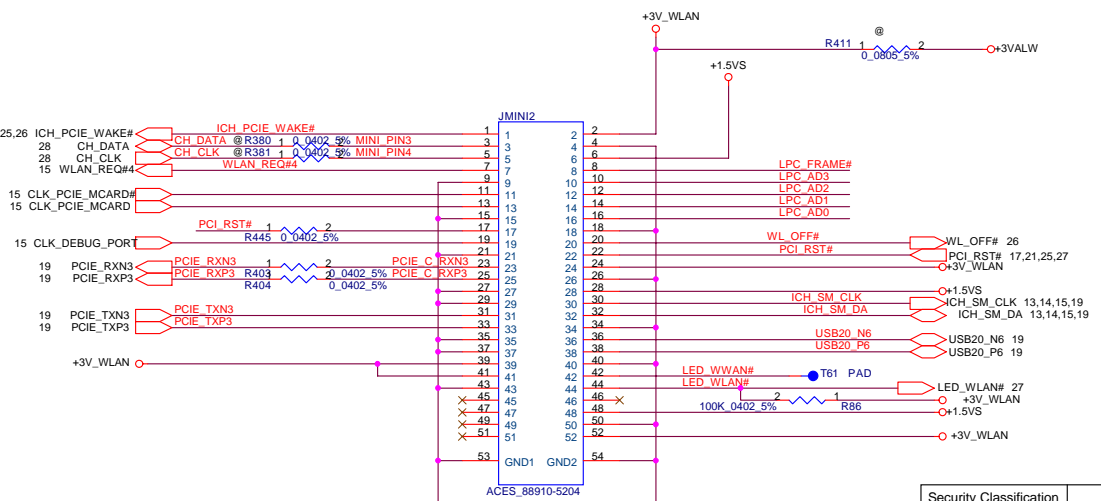


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Issued Date	2007/1/15	Deciphered Date	2008/1/15	HDD/CDROM
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Date: Thursday, February 19, 2009				Sheet 22 of 43
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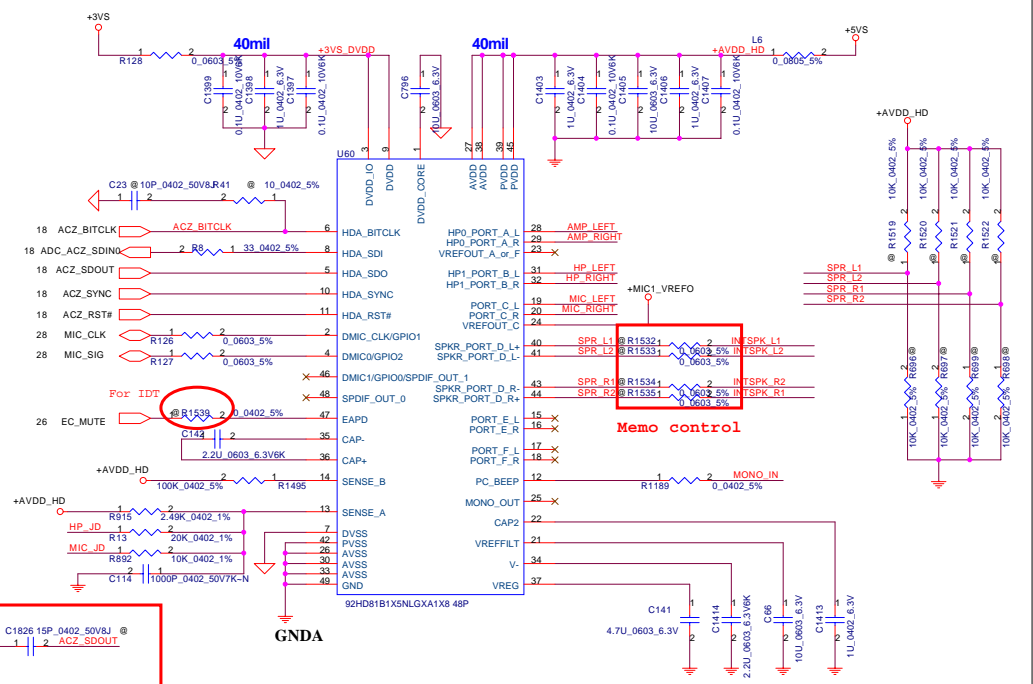
# Debug Board



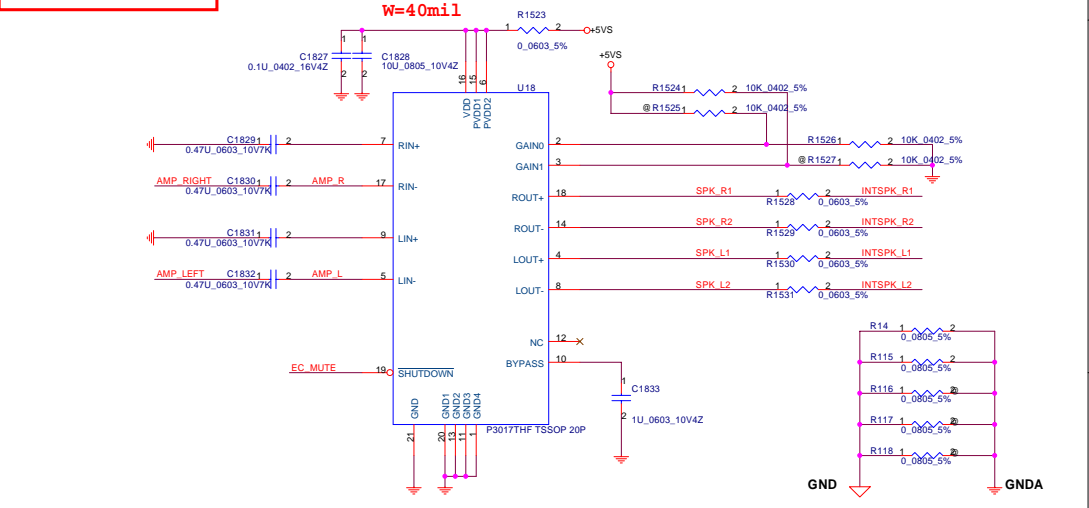
# Mini-Express Card---WLAN



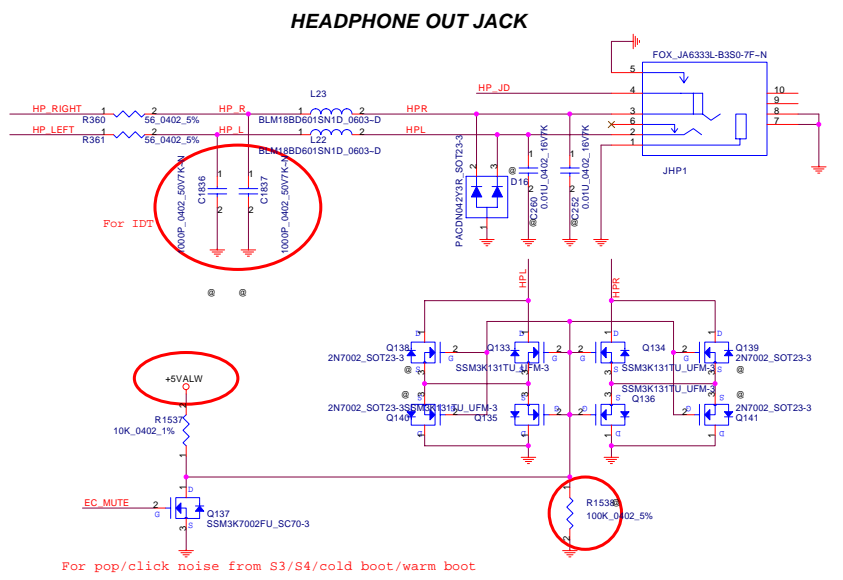
Security Classification		Compal Secret Data		Title	
Issued Date	2007/1/15	Deciphered Date	2008/1/15	Mini-Card/LED	
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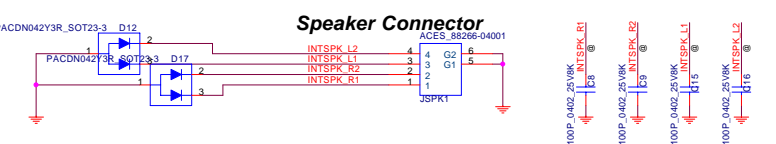
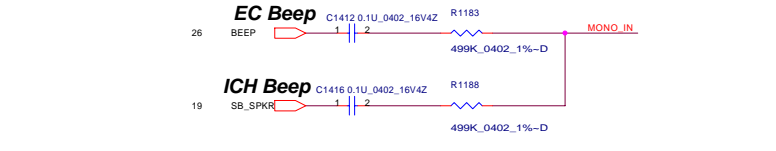
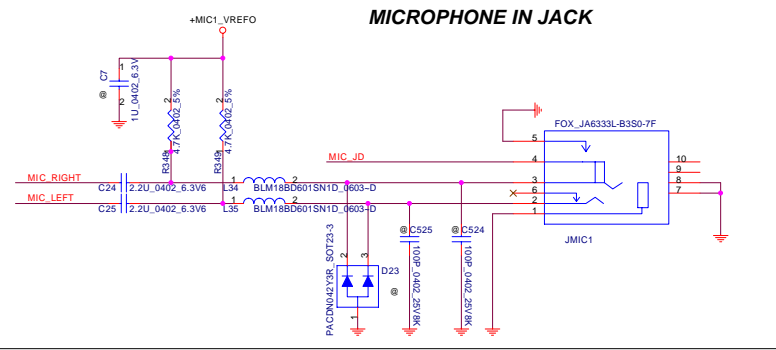
C1826 18P 0402 50V8J @  
1 2 ACZ\_SDOUT  
For SED TEST



	GAIN0	GAIN1	GAIN
	0	0	6dB
*	0	1	10dB
	1	0	15.6dB
	1	1	21.6dB



For pop/click noise from S3/S4/cold boot/warm boot



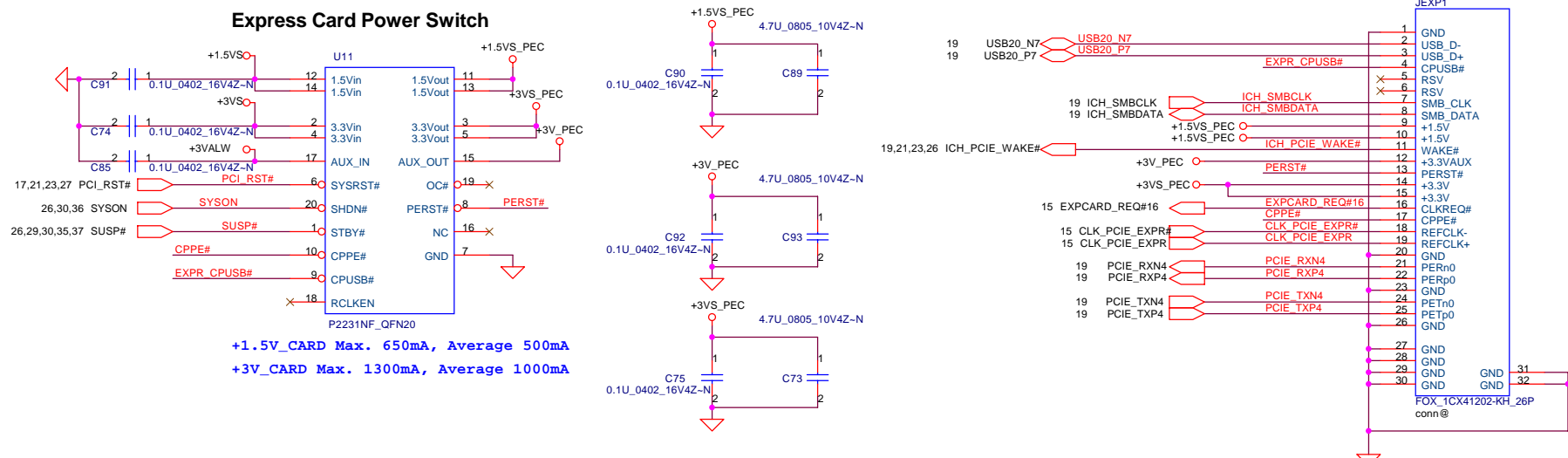
Compal Electronics, Inc.

Change to 100p from 0.01u for EMI  
-1012

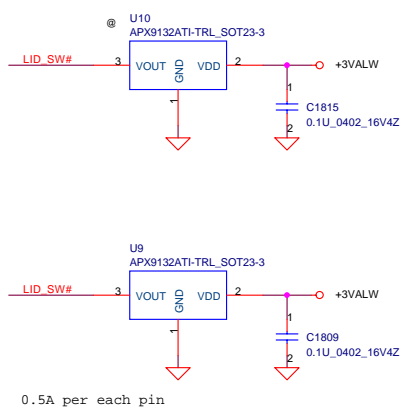
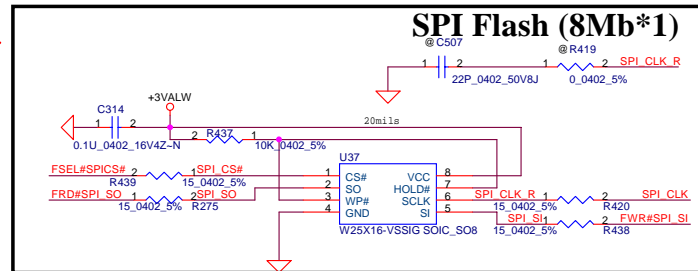
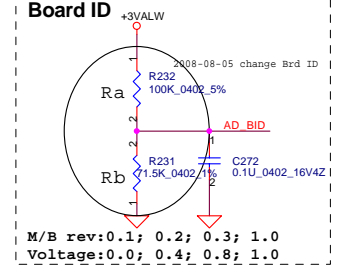
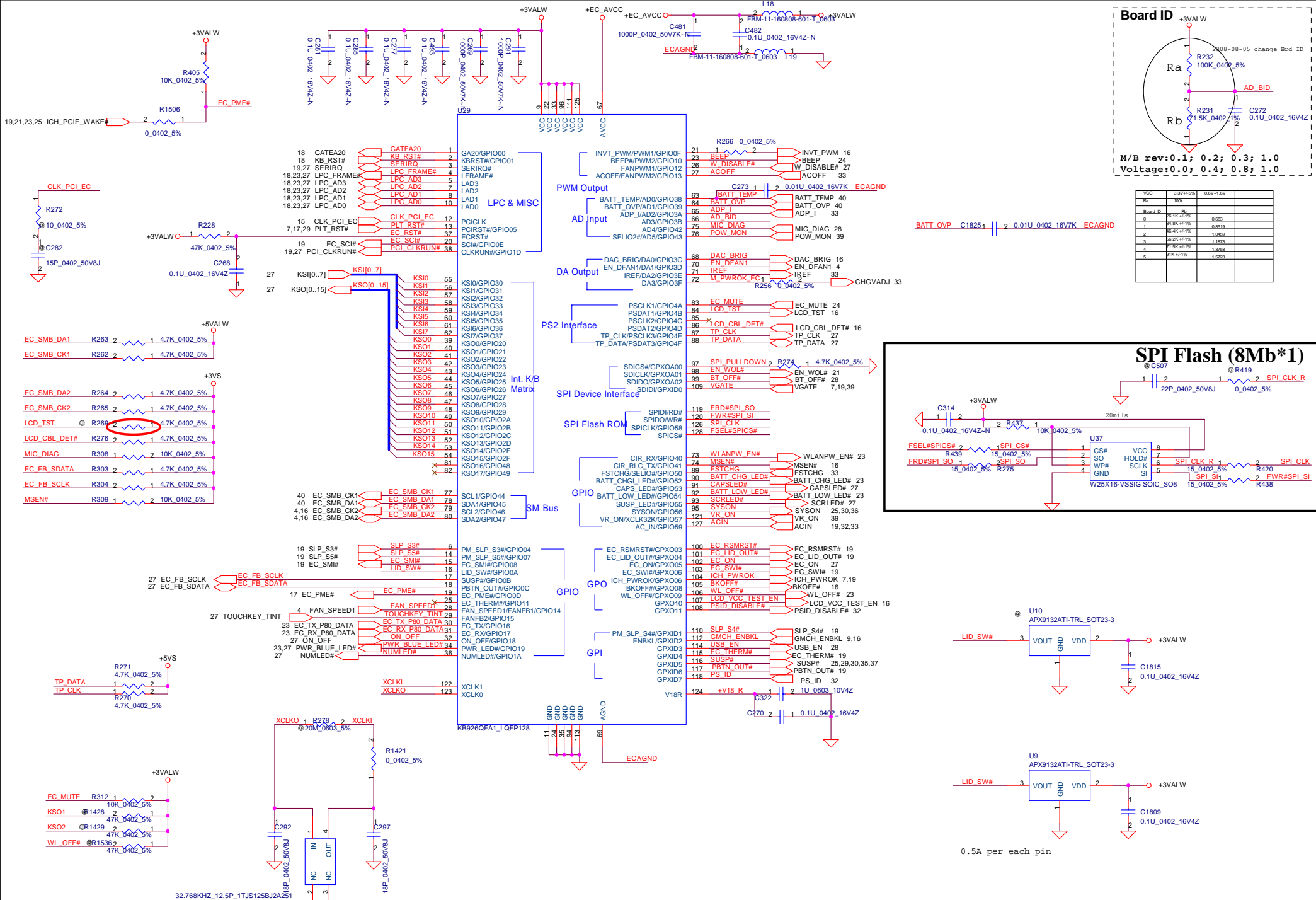
Buzzer need to support ICH/PCM\_SPK/Battery\_low and WL\_on/off



# Express card

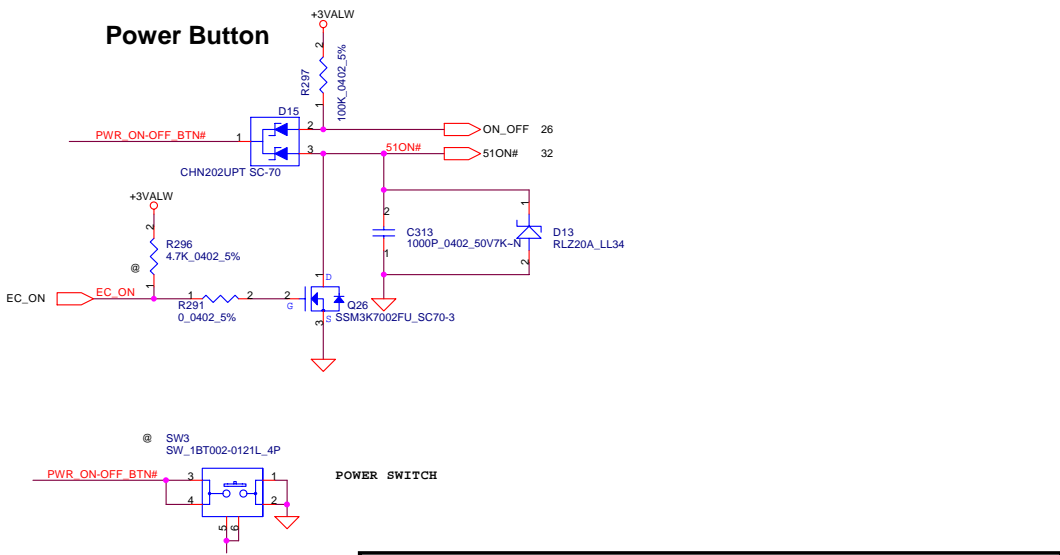


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Issued Date	2007/1/15	Deciphered Date	2008/1/15	Title	
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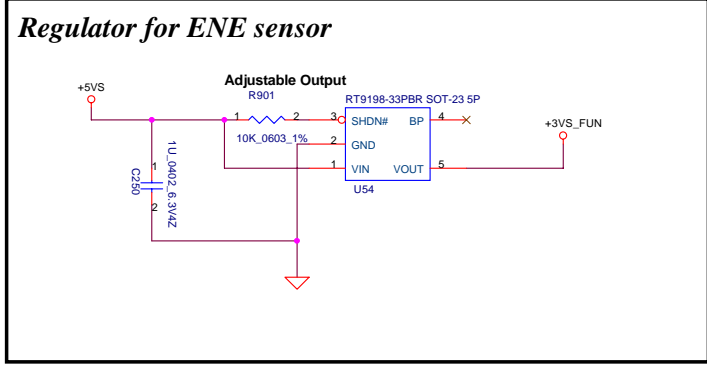
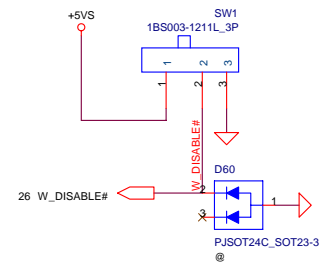


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Issued Date	2007/1/15	Deciphered Date	2008/1/15	Title	BIOS & EC I/O Port
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Size	Document Number	Rev			
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Date:	Thursday, February 19, 2009	Sheet	26	of	43

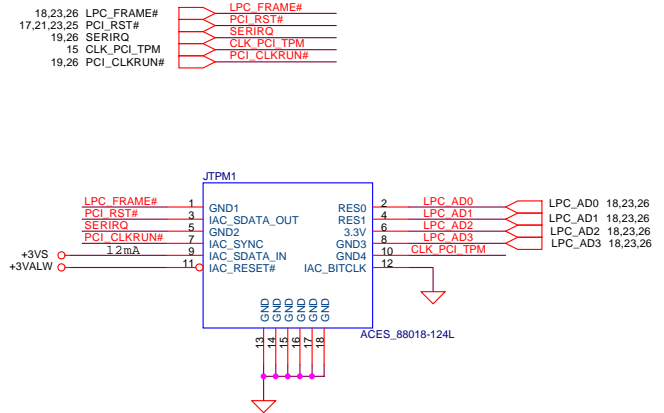
### Power Button



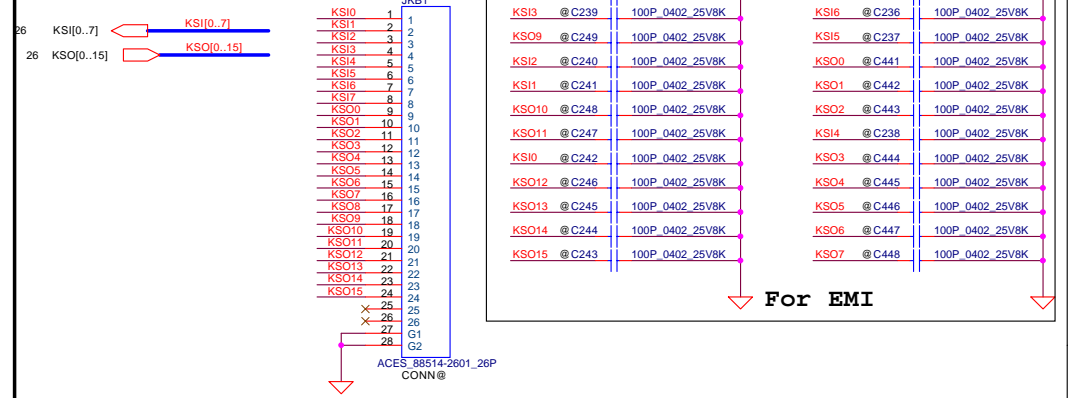
### Wireless\_BTN



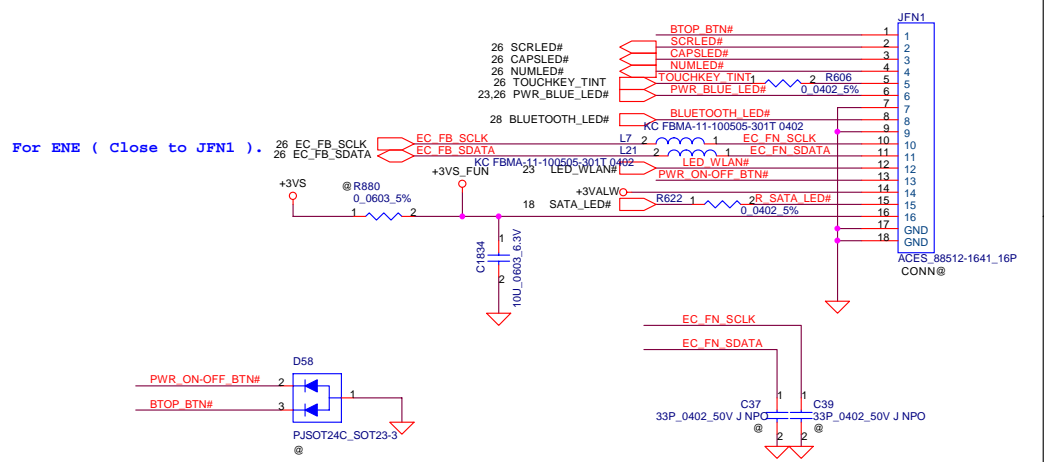
### TPM 1.2



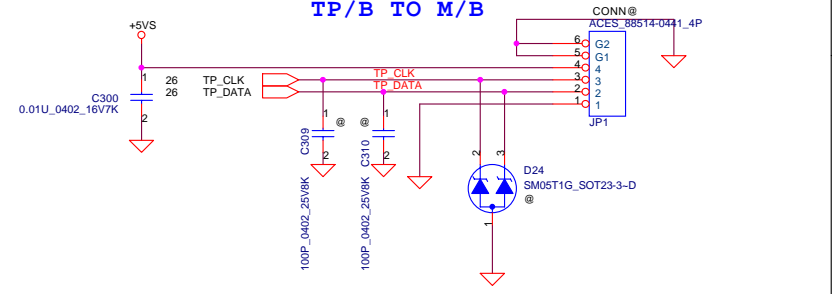
### INT\_KBD CONN.



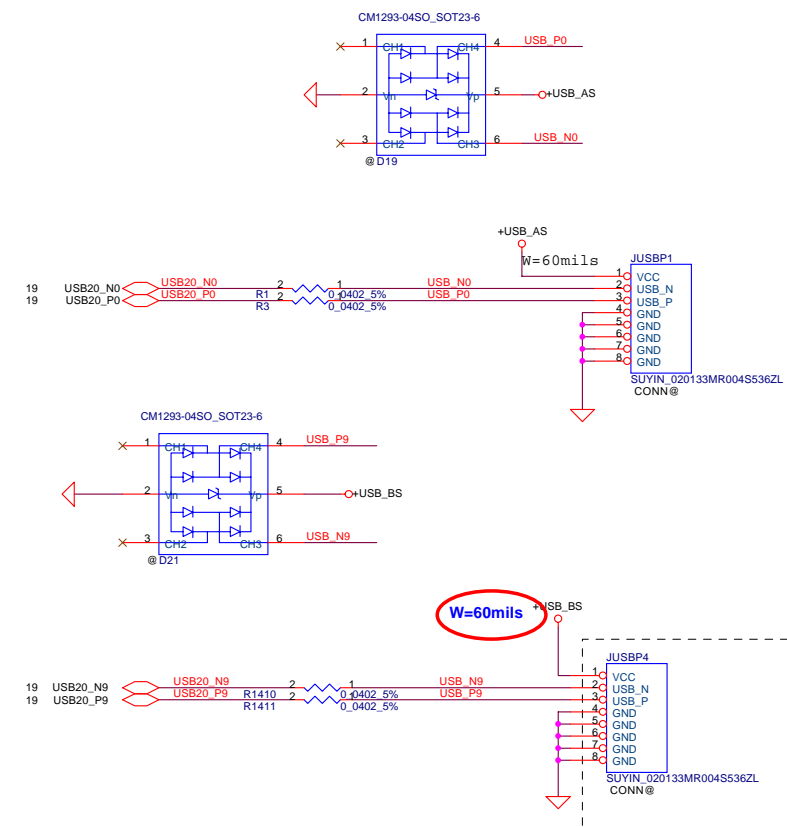
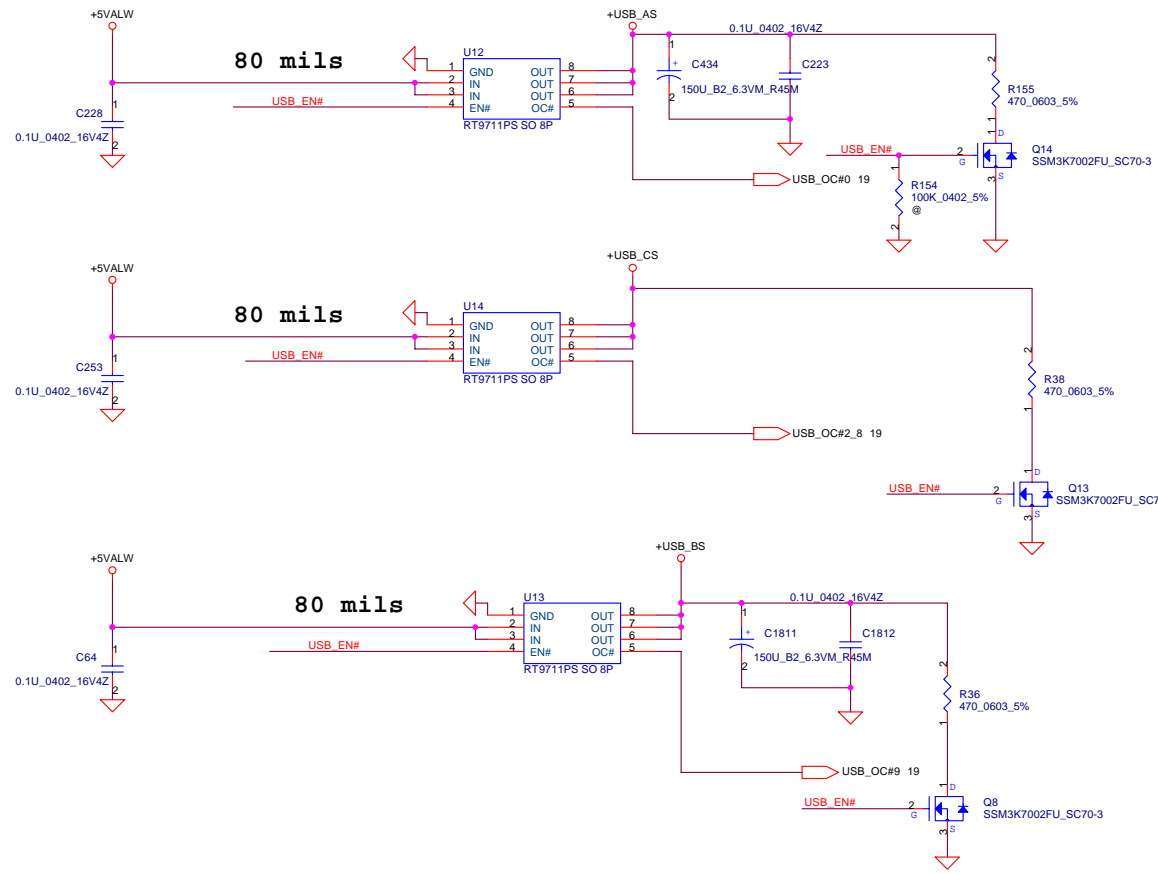
### Function/B CONN.



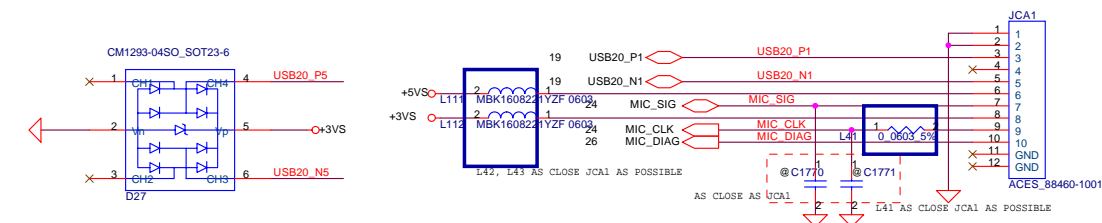
### Touch PAD/B CONN.



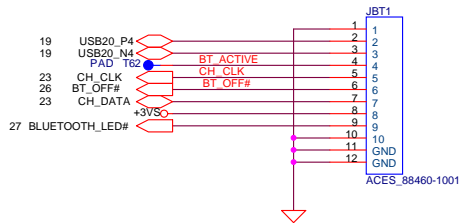
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2007/1/15	Deciphered Date	2008/1/15	Title <b>PWR_OK/BTN/TP</b>	
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Date:	Thursday, February 19, 2009	Sheet	27	of	43



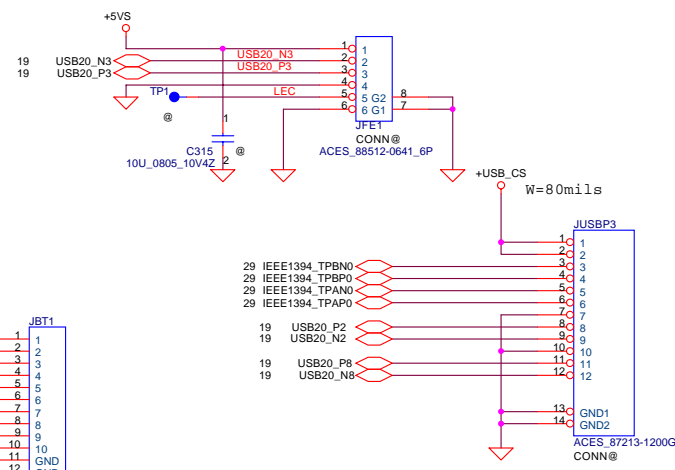
**Check Module pin define Camera Conn**



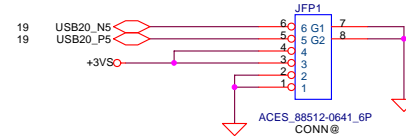
**Bluetooth**



**Felica Conn**



**Fingerprint**



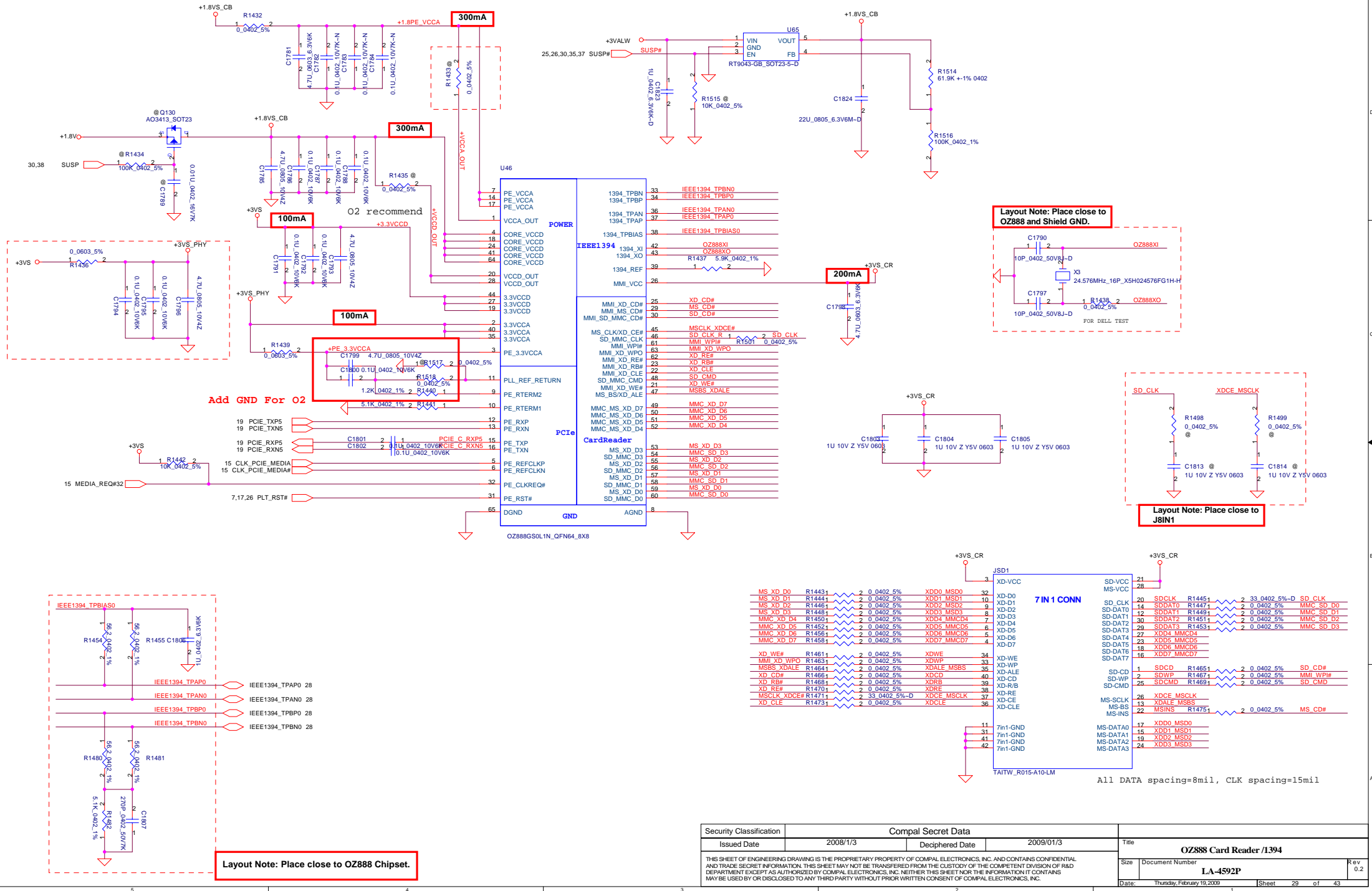
Security Classification	Compal Secret Data		Title	
Issued Date	2007/1/15	Deciphered Date	2008/1/15	<b>USB/BlueTooth/FP/Felica</b>
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**Compal Electronics, Inc.**

**USB/BlueTooth/FP/Felica**

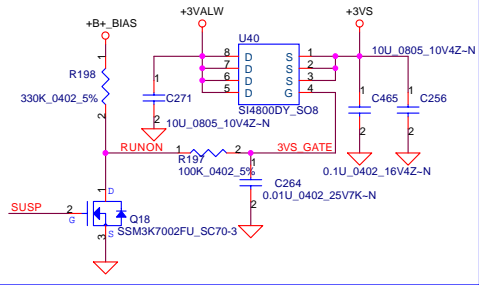
Size | Document Number  
Custom | **LA-4592P**

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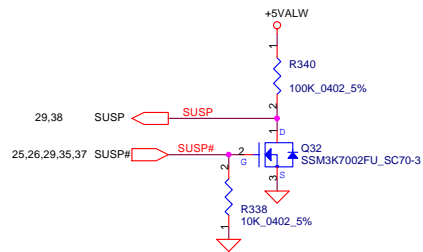
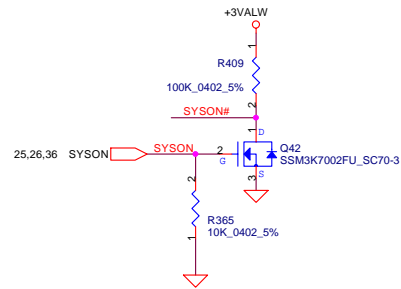
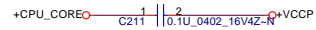
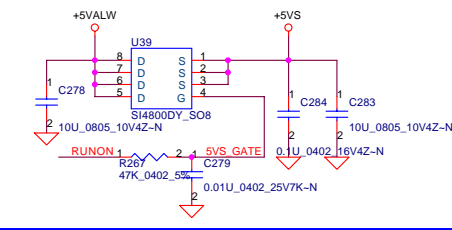


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Issued Date	2008/1/3	Deciphered Date	2009/01/3	Rev
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Size	Document Number	LA-4592P	Date:	Thursday, February 19, 2009
			Sheet	29 of 43

### +3VALW to +3VS Transfer

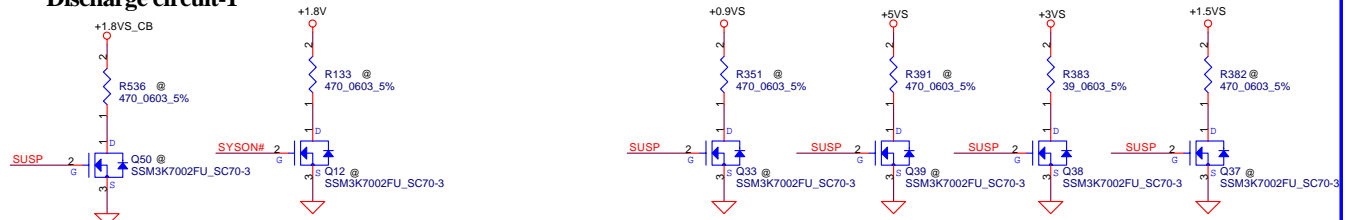


### +5VALW to +5VS Transfer



### VGA Discharge circuit

#### Discharge circuit-1

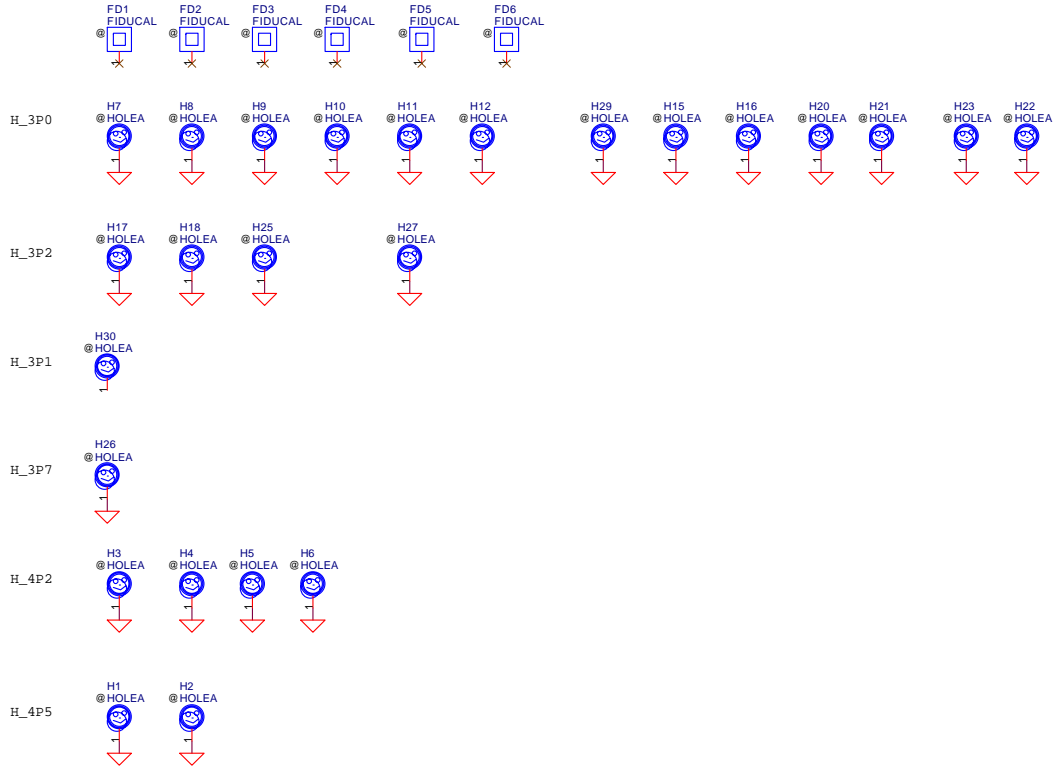


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				Custom	LA-4592P
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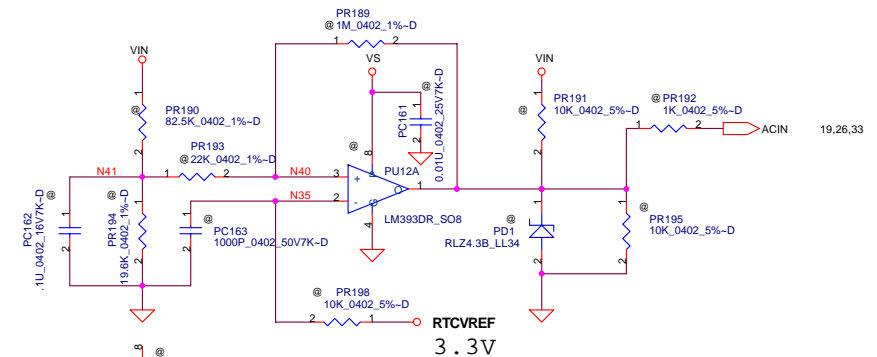
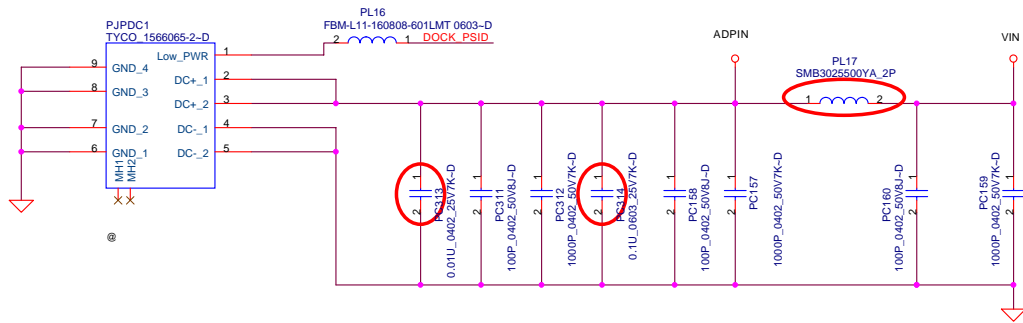
Compal Electronics, Inc.

DC/DC Circuits

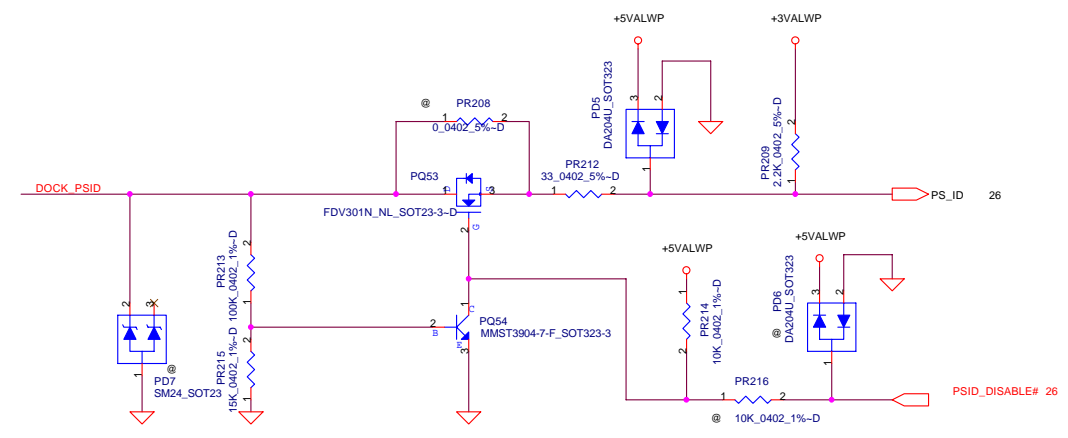
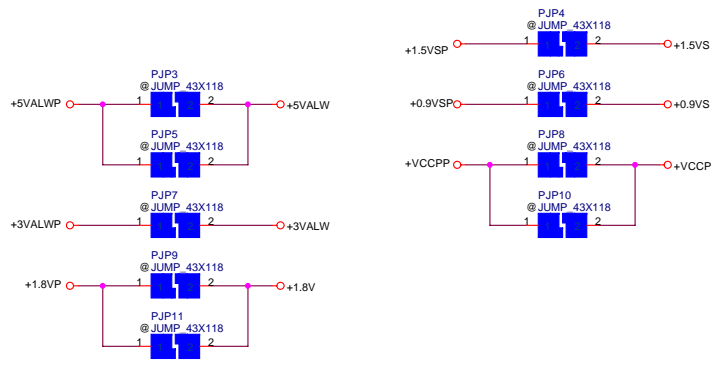
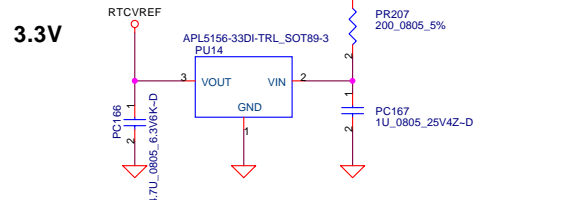
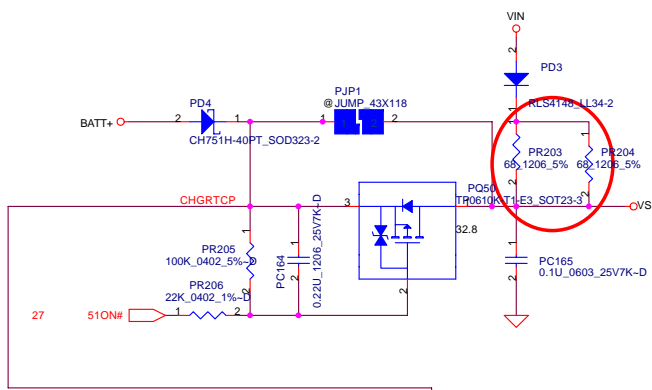
Size: Document Number  
 Custom: LA-4592P  
 Date: Thursday, February 19, 2009  
 Sheet: 30 of 43  
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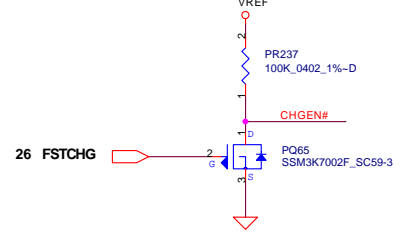
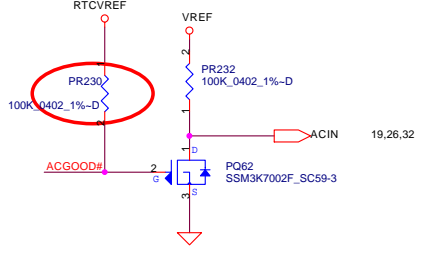
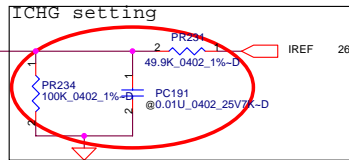
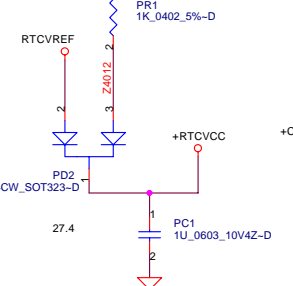
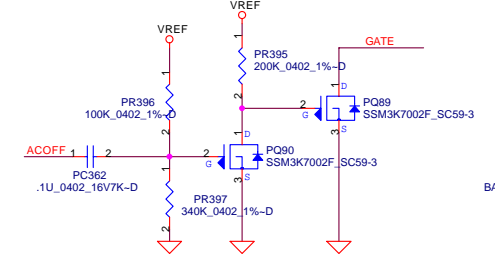
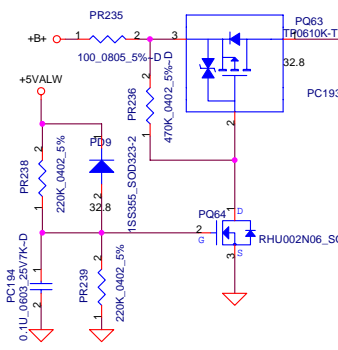
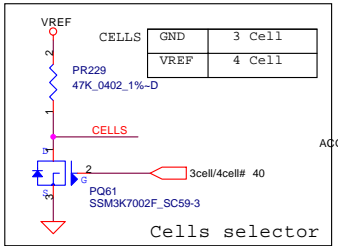
Vin Detector			
	Max.	typ.	Min.
L-->H	18.234	17.841	17.449
H-->L	17.597	17.210	16.813



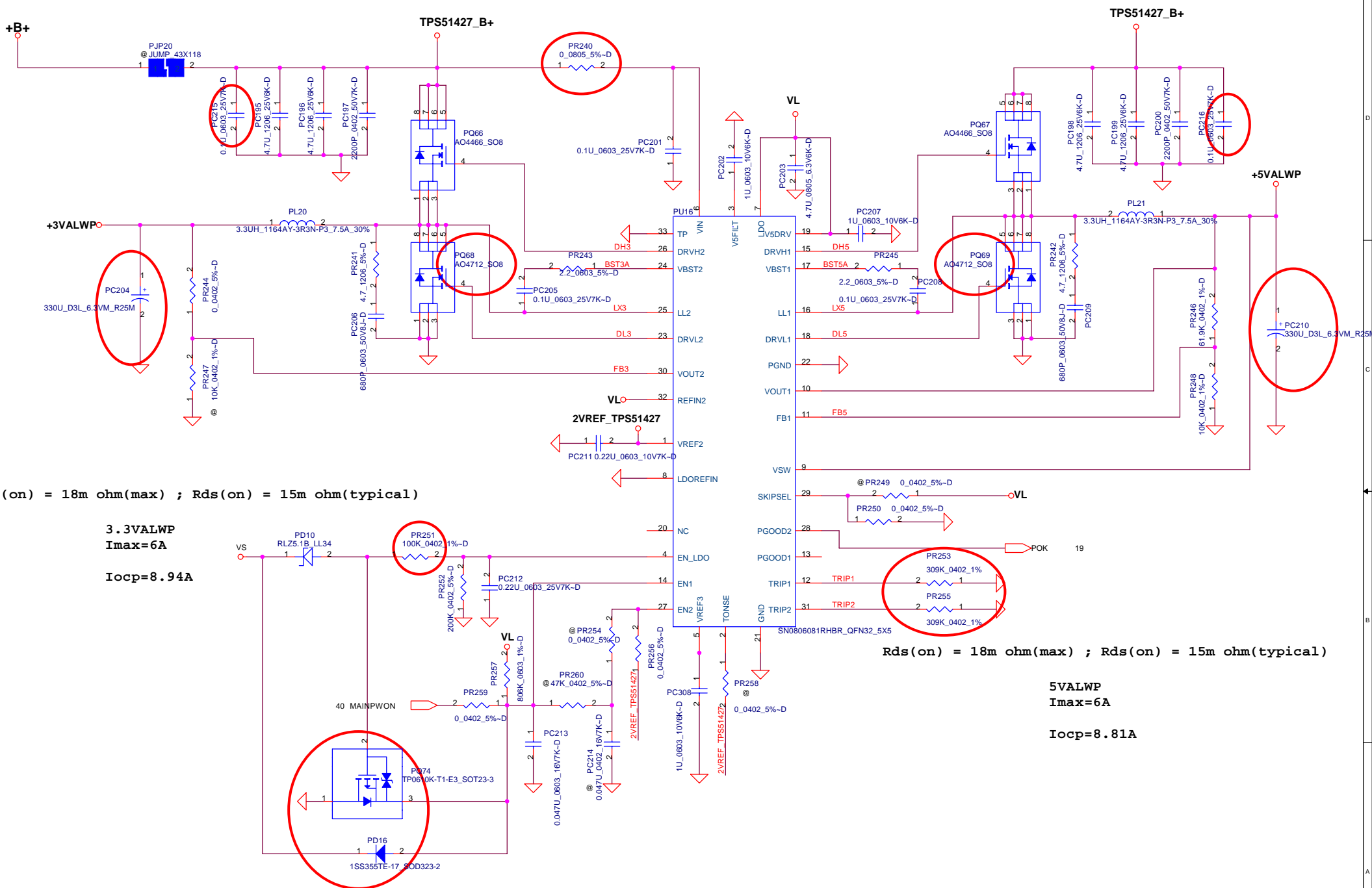
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Title		DCIN / Vin Detector	
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90W adapter  
 $I_{charge} = (V_{rsset}/V_{vdac}) * (0.1/PR34) = 3.34A$   
 $I_{adapter} = (V_{acset}/V_{vdac}) * (0.1/PR17) = 3.1A$   
 Input OVP : 22.3V  
 Input UVP : 16.98V  
 Fsw : 300KHz



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Issued Date	2006/10/1	Deciphered Date	2007/5/01	
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Size B			Document Number	Rev 0.2
			KML50	
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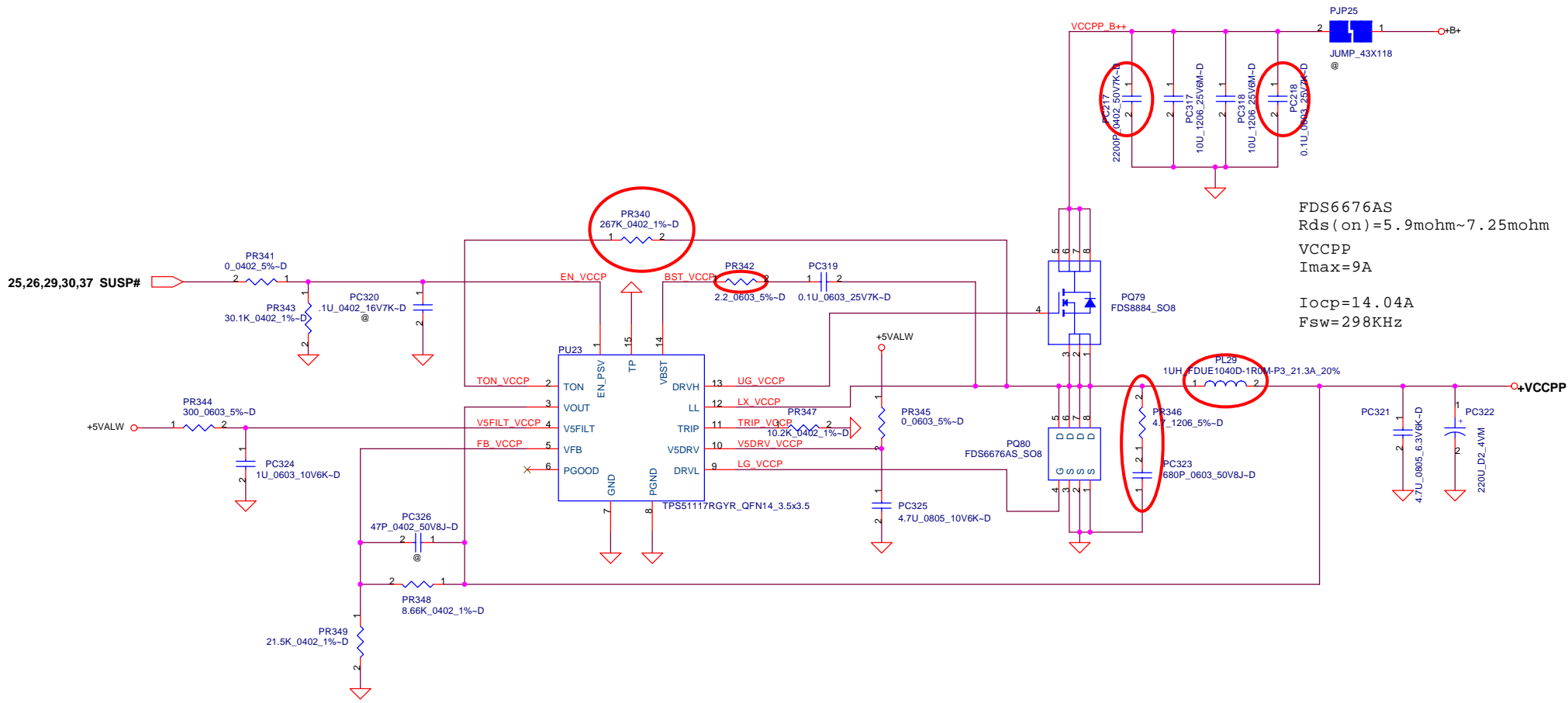
$R_{ds(on)} = 18m\ ohm(max) ; R_{ds(on)} = 15m\ ohm(typical)$

**3.3VALWP**  
 **$I_{max}=6A$**   
 **$I_{ocp}=8.94A$**

$R_{ds(on)} = 18m\ ohm(max) ; R_{ds(on)} = 15m\ ohm(typical)$

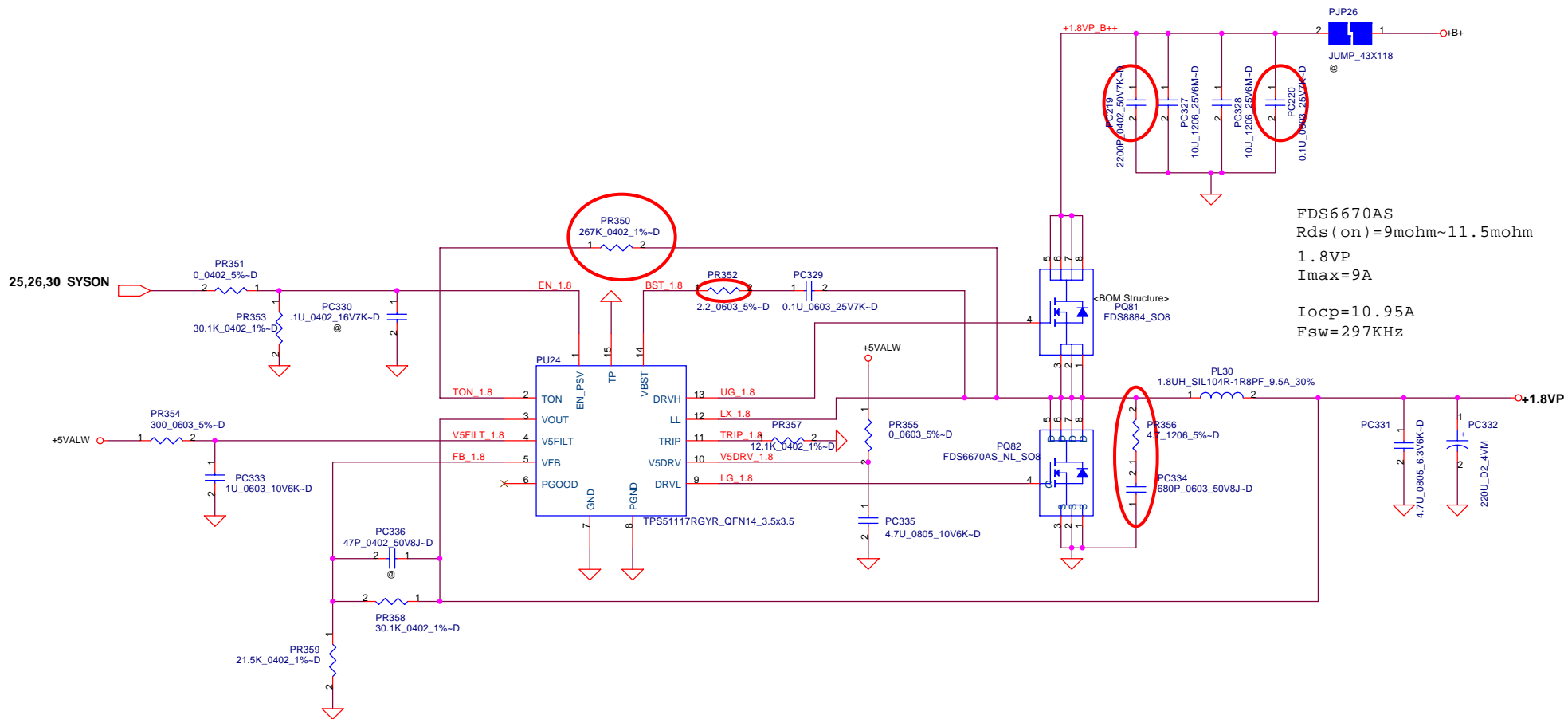
**5VALWP**  
 **$I_{max}=6A$**   
 **$I_{ocp}=8.81A$**

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Size	Document Number	Rev		Date:	
Custom	<b>LA-4596P</b>	0.2		Thursday, February 19, 2009	
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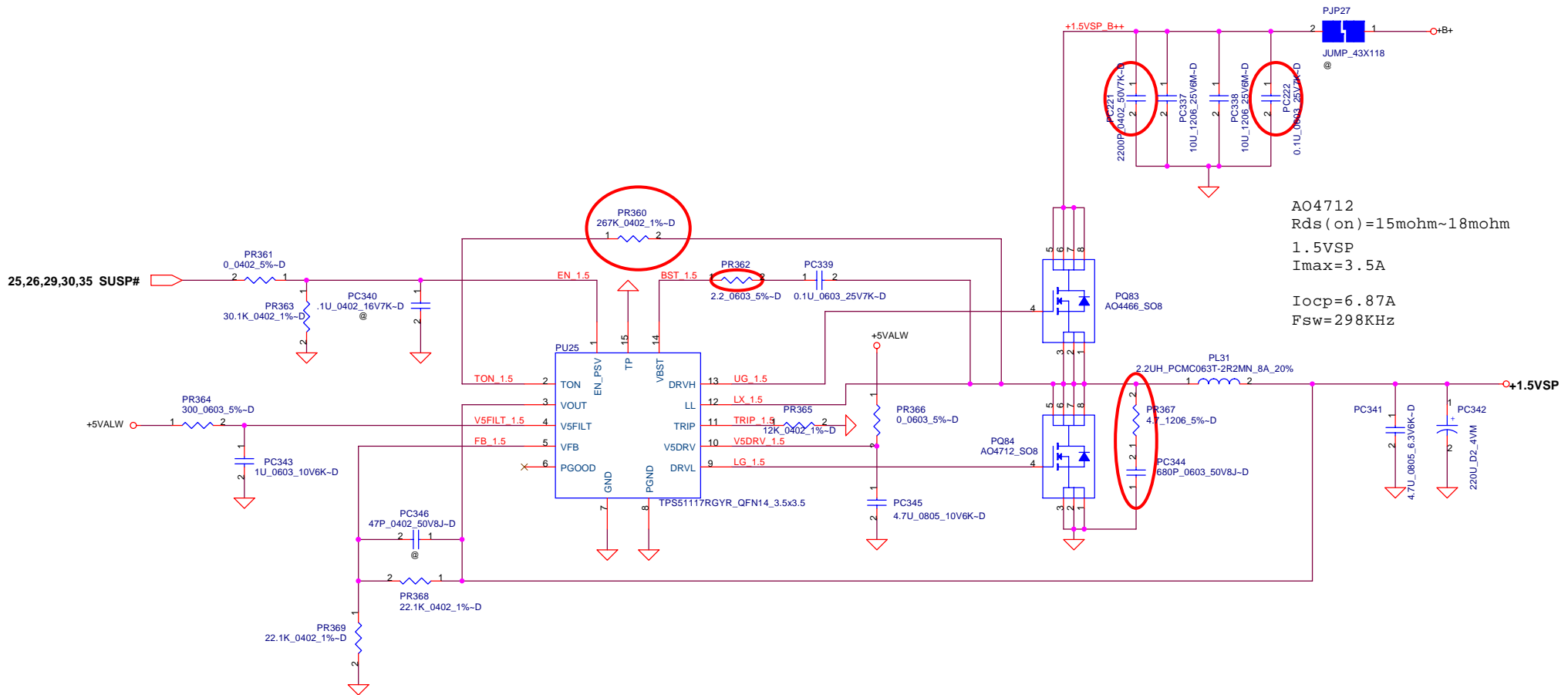


FDS6676AS  
 $R_{ds(on)} = 5.9\text{mohm} \sim 7.25\text{mohm}$   
 VCCPP  
 $I_{max} = 9\text{A}$   
 $I_{ocp} = 14.04\text{A}$   
 $f_{sw} = 29.8\text{KHz}$

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Size	Document Number			Rev	
	LA-4596P			0.1	
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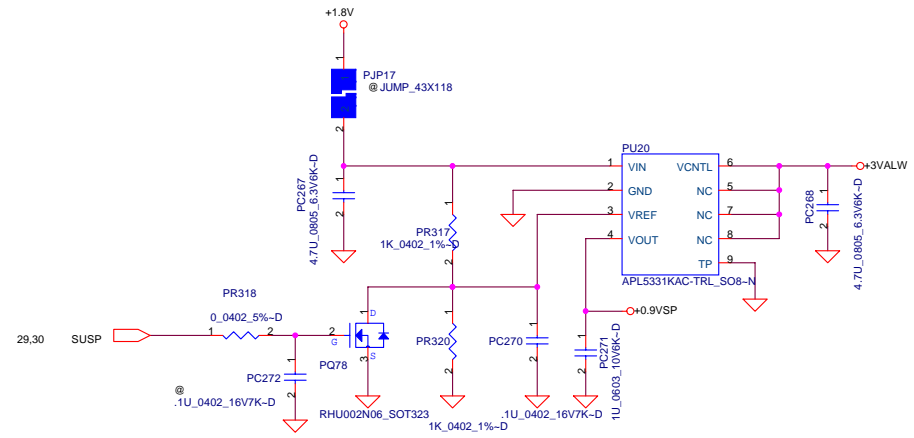
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Issued Date	2006/10/1	Deciphered Date	2007/05/30	Title	
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	LA-4596P			0.2	
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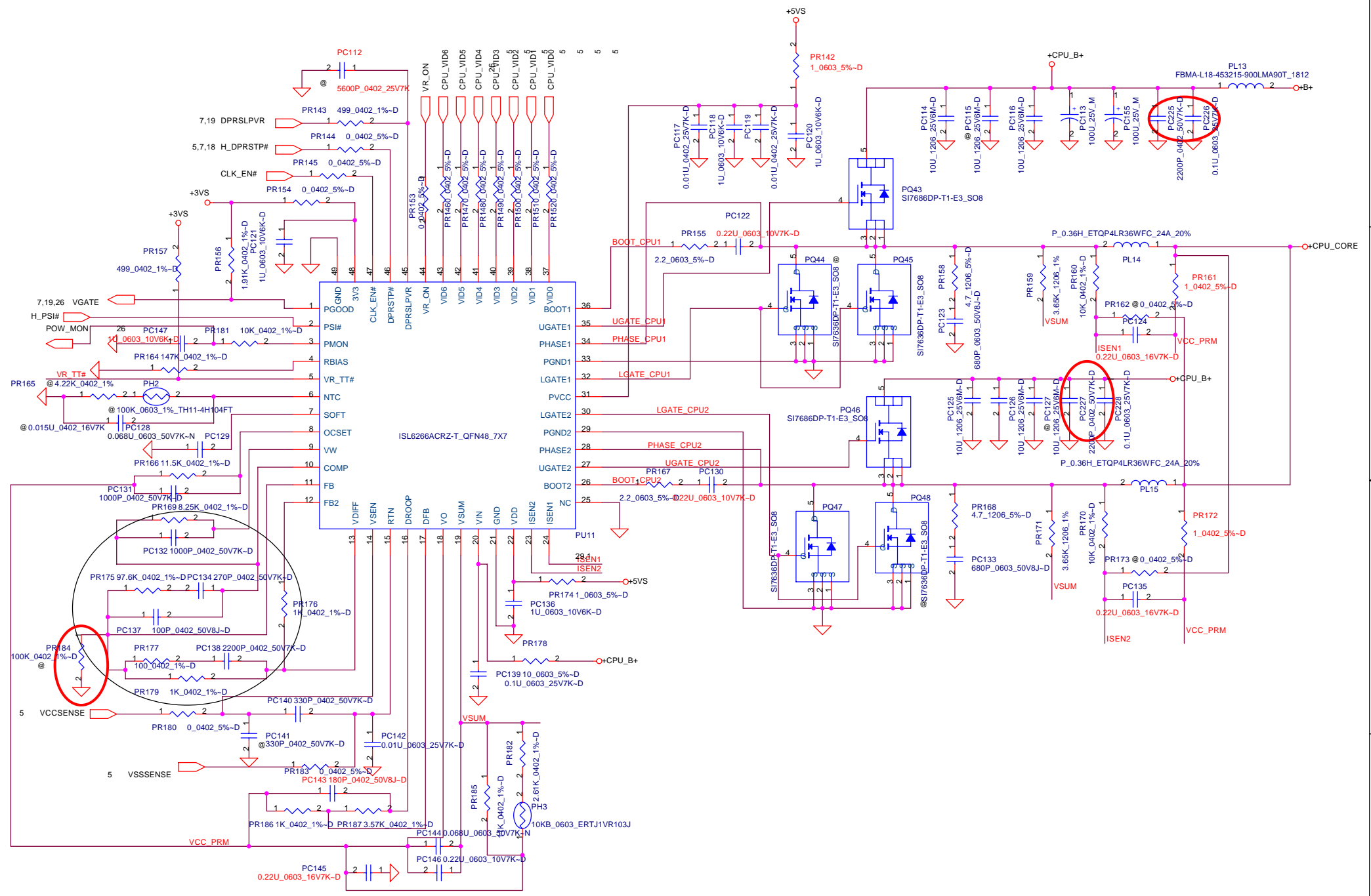
AO4712  
 $R_{ds(on)} = 15\text{mohm} \sim 18\text{mohm}$   
 1.5VSP  
 $I_{max} = 3.5\text{A}$   
 $I_{ocp} = 6.87\text{A}$   
 $F_{sw} = 298\text{KHz}$

25,26,29,30,35 SUSP#

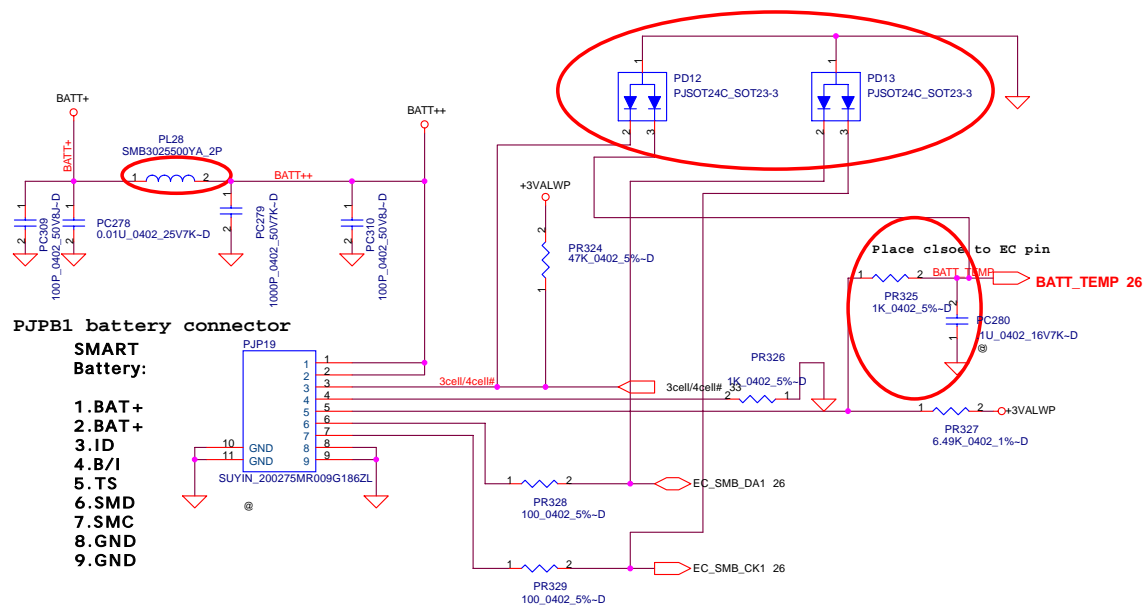
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				Date: Thursday, February 19, 2009		Sheet 38 of 43

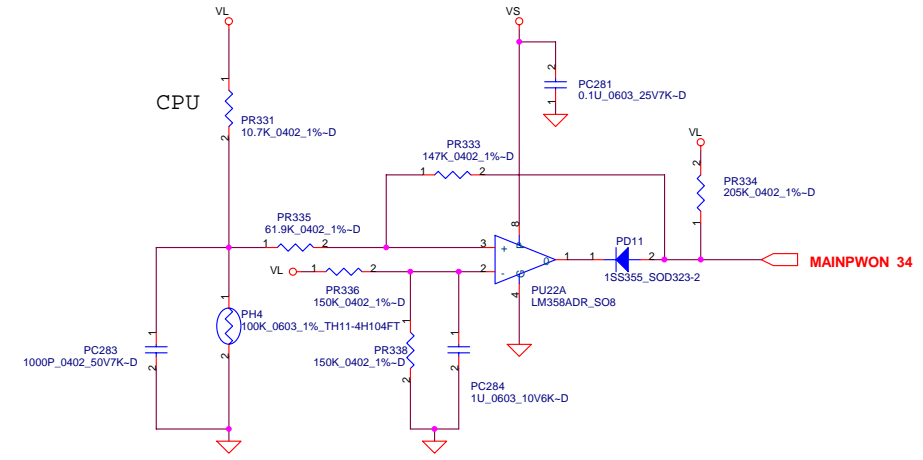
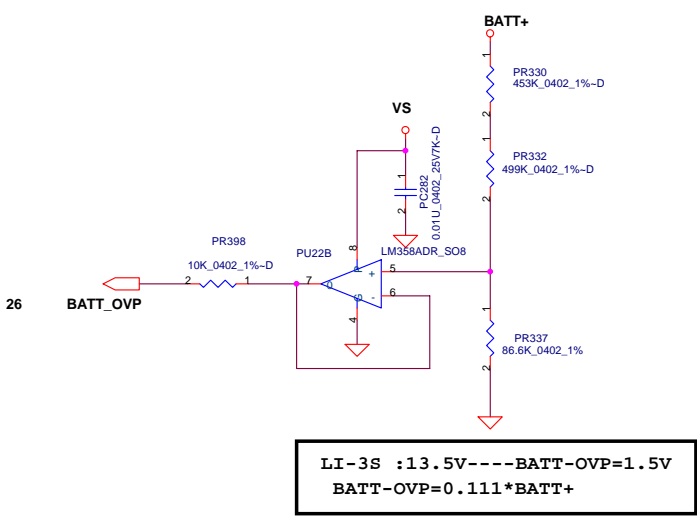


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**Battery Connect/OTP**

CPU  
**PH1 under CPU bottom side :**  
 CPU thermal protection at 90 +/-3 degree C  
 Recovery at 50 +/-3 degree C



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<b>Compal Electronics, Inc.</b>				
<b>BATTERY CONN</b>				
Size	Document Number	Rev		
Custom	<b>LA-4596P</b>	0.2		
Date:	Thursday, February 19, 2009	Sheet	40	of 43

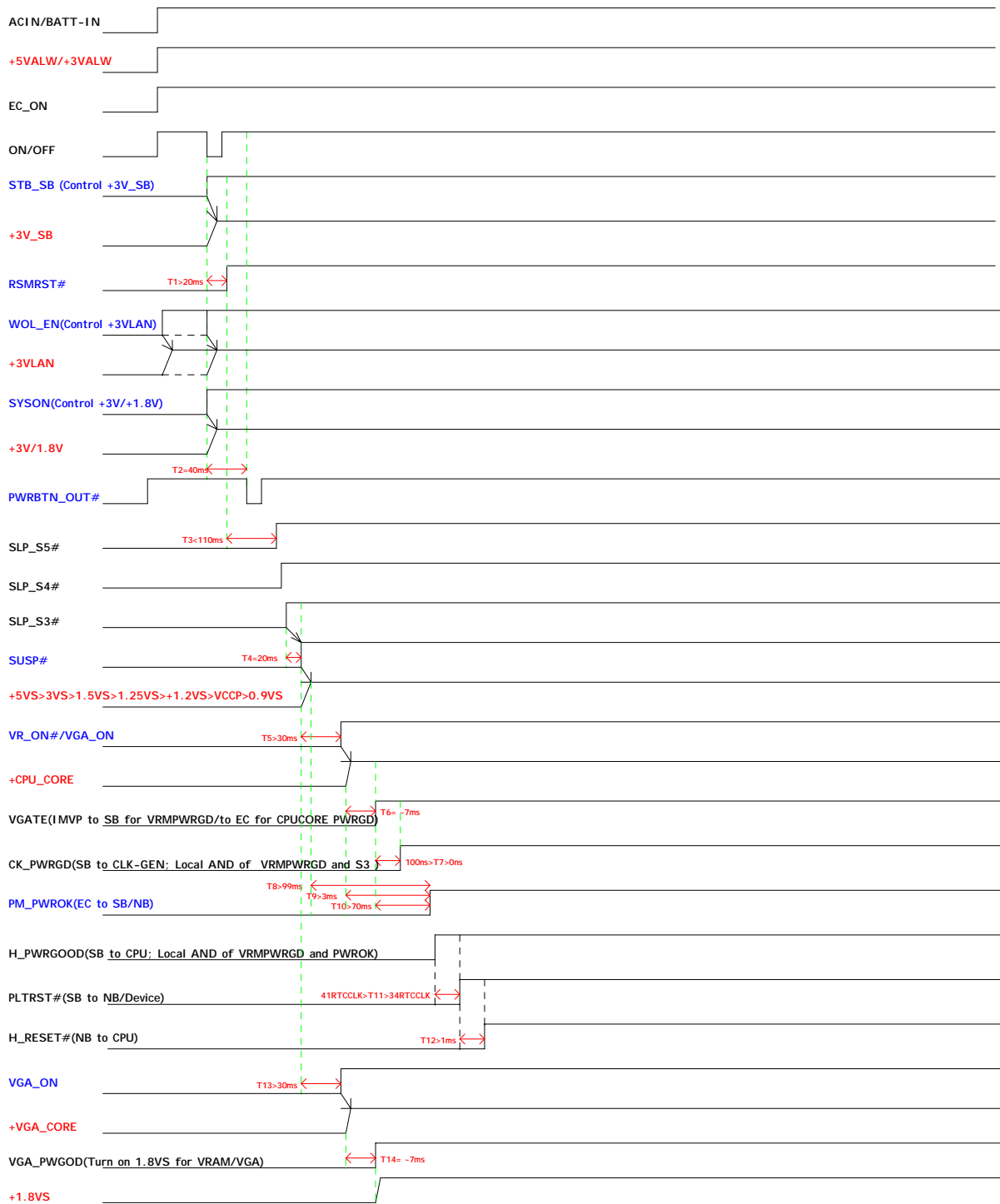


Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	32	DCIN /Vin Detector	08/12/08	COMPAL	common circuit design modify	change PR203 from 33 to 68 and add PR204 to 68	0.3
2			08/12/08	COMPAL	design modify	change PL17 from SM010018880 to SM010008E10	0.3
3	33	Charger	08/12/08	COMPAL	vendor FAE suggest	change PR272 PR339 from 1 to 3.3	0.3
4	40	BATTERY CONN	08/12/08	COMPAL	design modify	change PL28 from SM010018210 to SM010008E10	0.3
5	32	DCIN /Vin Detector	08/12/12	COMPAL	increase capacitor for EMI request	add PC313 at 0.01uf and PC314 at 0.1uf	0.3
6	35	VCCPP	08/12/12	COMPAL	change resister for EMI request	change PR342 from 0 to 2.2	0.3
7	36	1.8VP	08/12/12	COMPAL	change resister for EMI request	change PR352 from 0 to 2.2	0.3
8	37	1.5VSP	08/12/12	COMPAL	change resister for EMI request	change PR362 from 0 to 2.2	0.3
9	35	VCCPP	08/12/18	COMPAL	add resister and capacitor for EMI request	add PR346 at 4.7and pc323 at 680p	0.3
10	36	1.8VP	08/12/18	COMPAL	add resister and capacitor for EMI request	add PR356 at 4.7and pc334 at 680p	0.3
11	37	1.5VSP	08/12/18	COMPAL	add resister and capacitor for EMI request	add PR367 at 4.7and pc344 at 680p	0.3
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	28	USB/BT/ FP/ Felica/Camera	2008/12/02	Compal_HW	Small USB board no function	Modify Pin definition of JUSBP3	0.2
2	24	HDA-IDT_92HD81	2008/12/02	Compal_HW	R voice and L voice fail	Modify Pin definition of JSPK1	0.2
3	27	PWR_OK/ BTN/ KB / TP/TPM1.2	2008/12/02	Compal_HW	Switch function fail	Modify Pin definition of SW1	0.2
4	21	LAN-8111D	2008/12/16	Compal_HW	EMI LAN test fail	Add C1817-C1820 for LAN connector	0.2
5	23	Mini-Card/WWAN/Roboson	2008/12/16	Compal_HW	S5 wake on Wirlesslan fail	Add U89 to control wirless lan voltage	0.2
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