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Project Code & Schematics Subject: H902 Main Board 8L

PCB P/N:	1P-009CJ00-8000 (IRIS)
	1P-009C500-8000 (HANNSTAR)
	1P-009C200-8000 (NANYA)
BT DB P/N:	1P-1098J01-8000 (IRIS)
	1P-1098501-8000 (HANNSTAR)
	1P-1098201-8000 (NANYA)
LED DB P/N:	1P-1098J00-8000 (IRIS)
	1P-1098500-8000 (HANNSTAR)
	1P-1098200-8000 (NANYA)
P/B DB P/N:	1P-1098J02-8000 (IRIS)
	1P-1098502-8000 (HANNSTAR)
	1P-1098202-8000 (NANYA)

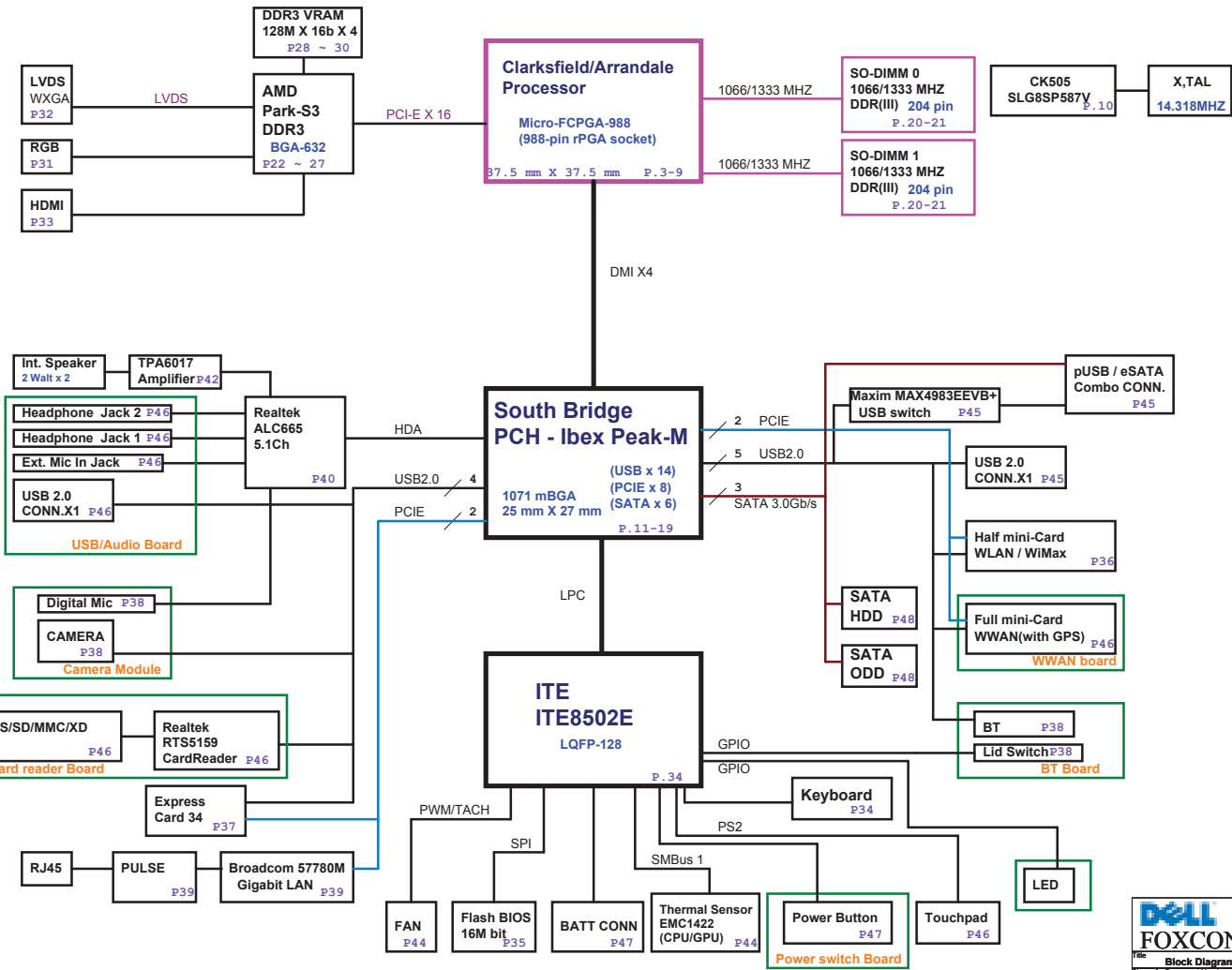
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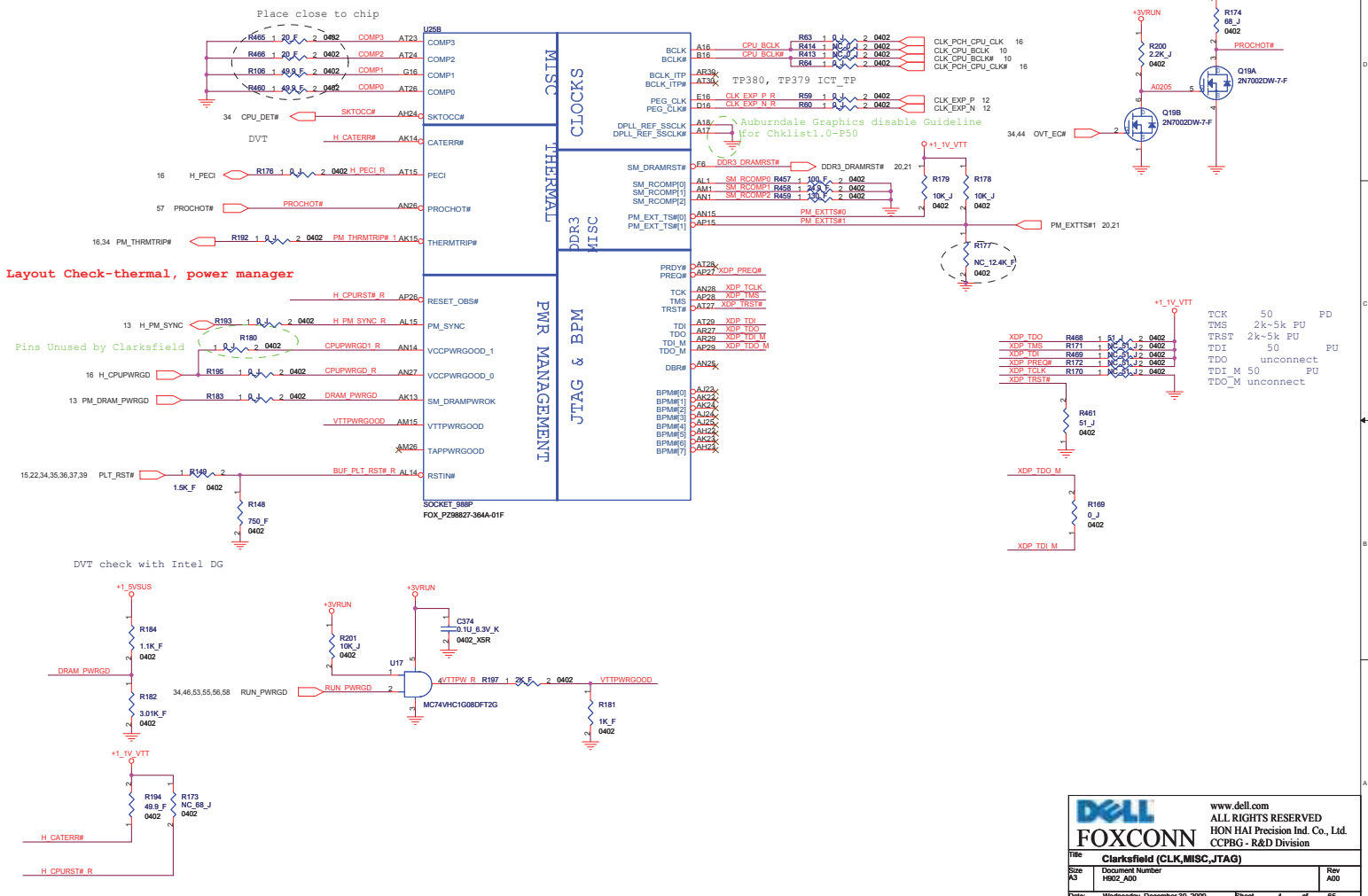
H902 Calpella + Discrete VGA



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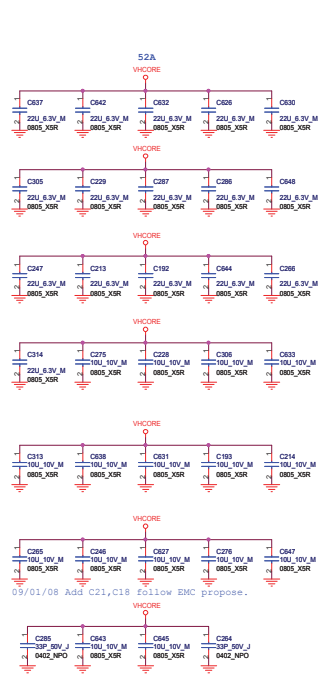
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Layout Note:
 Comp0,2 connect with Zo=27.4 ohm, make trace length shorter than 0.5". Width=20mil (MS)
 Comp1,3 connect with Zo=5 ohm, make trace length shorter than 0.5". Width=5mil (MS)



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		Clarksfield (CLK,MISC,JTAG)	
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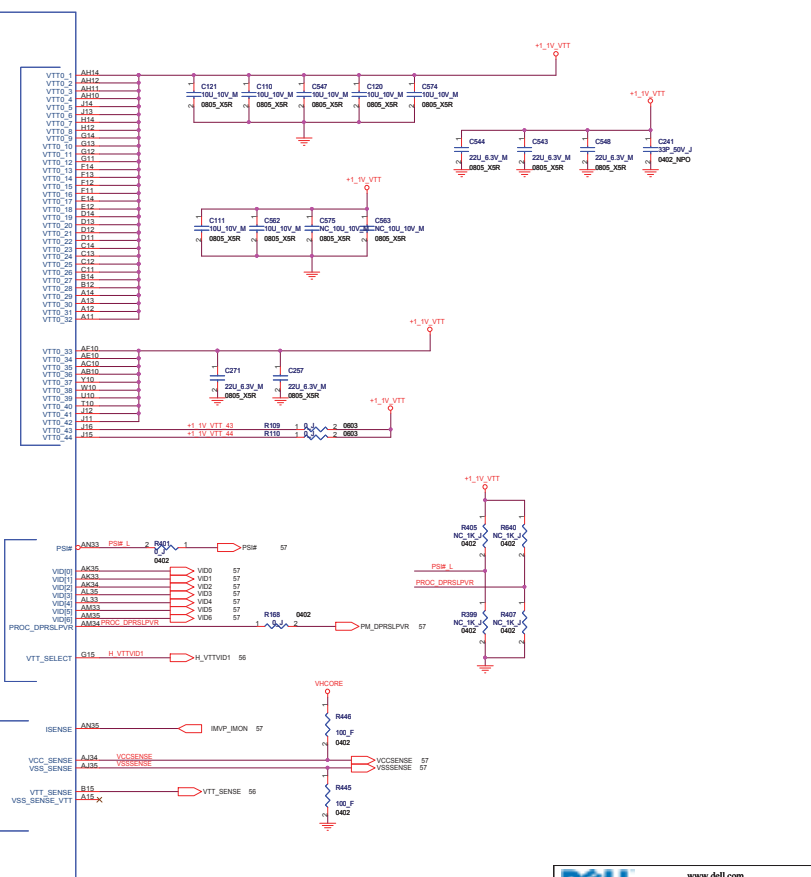


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1.1V RAIL POWER

CPV TTDS

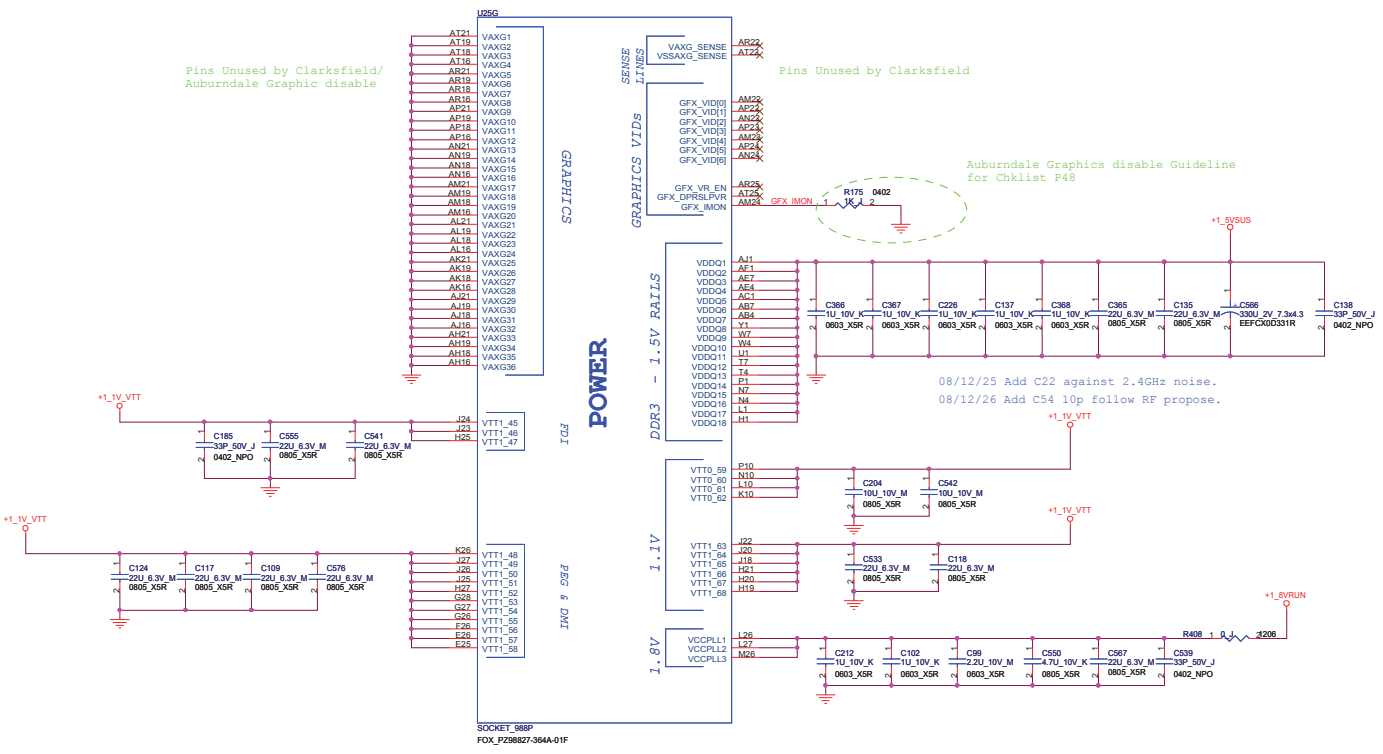
SENSE LINE



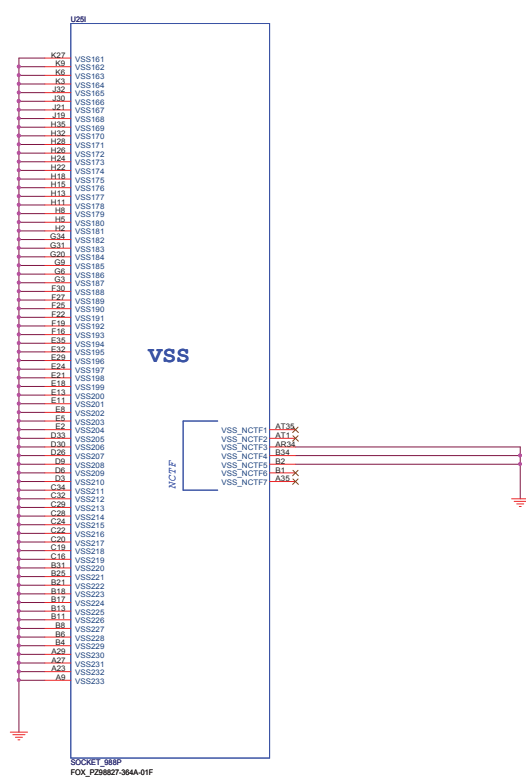
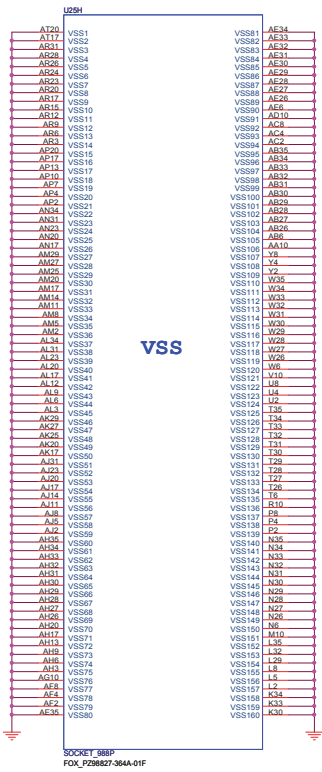
SOCKET_8BP
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Clarksfield (GRAPHIC POWER)		
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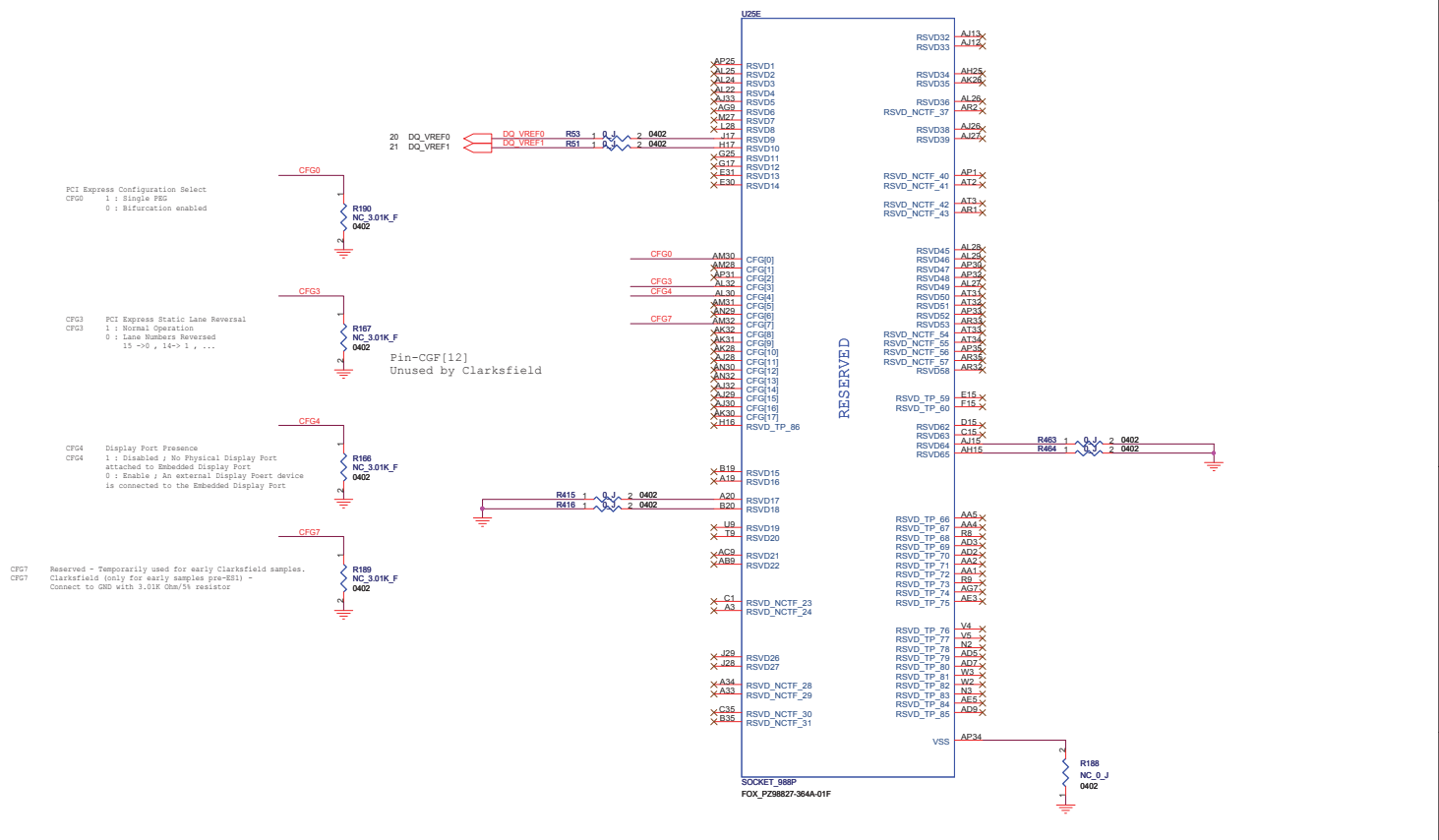


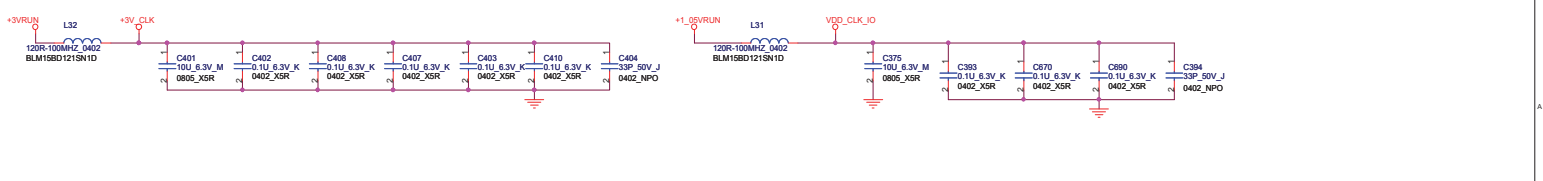
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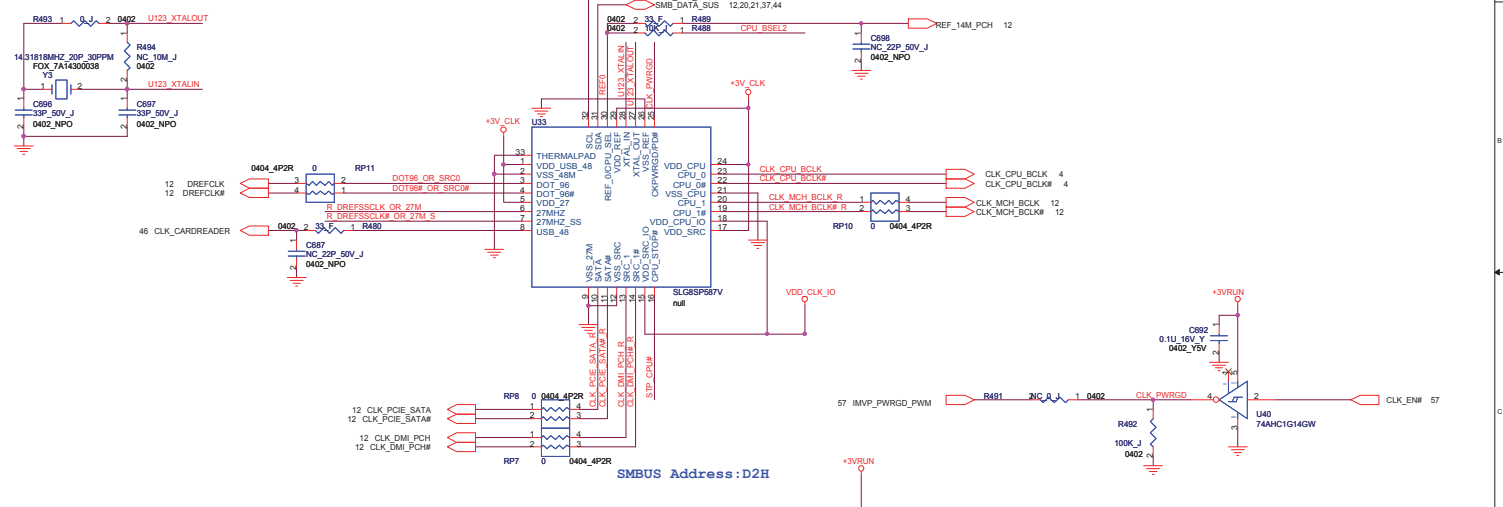
File: Clarkfield (GND)
 Location: Name:
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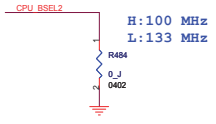
DVT Check if we have to change to HAMONY



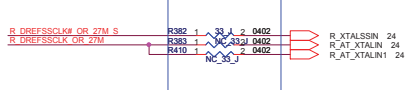
FSP Table

FS	CPU	Power On	SRC	SATA	DOT96	27MHz	REF
0	133MHz	Default	100MHz	100MHz	96MHz	27MHz	14.318MHz
1	100MHz						

08/12/31 Delete R5497.



H:100 MHz
L:133 MHz

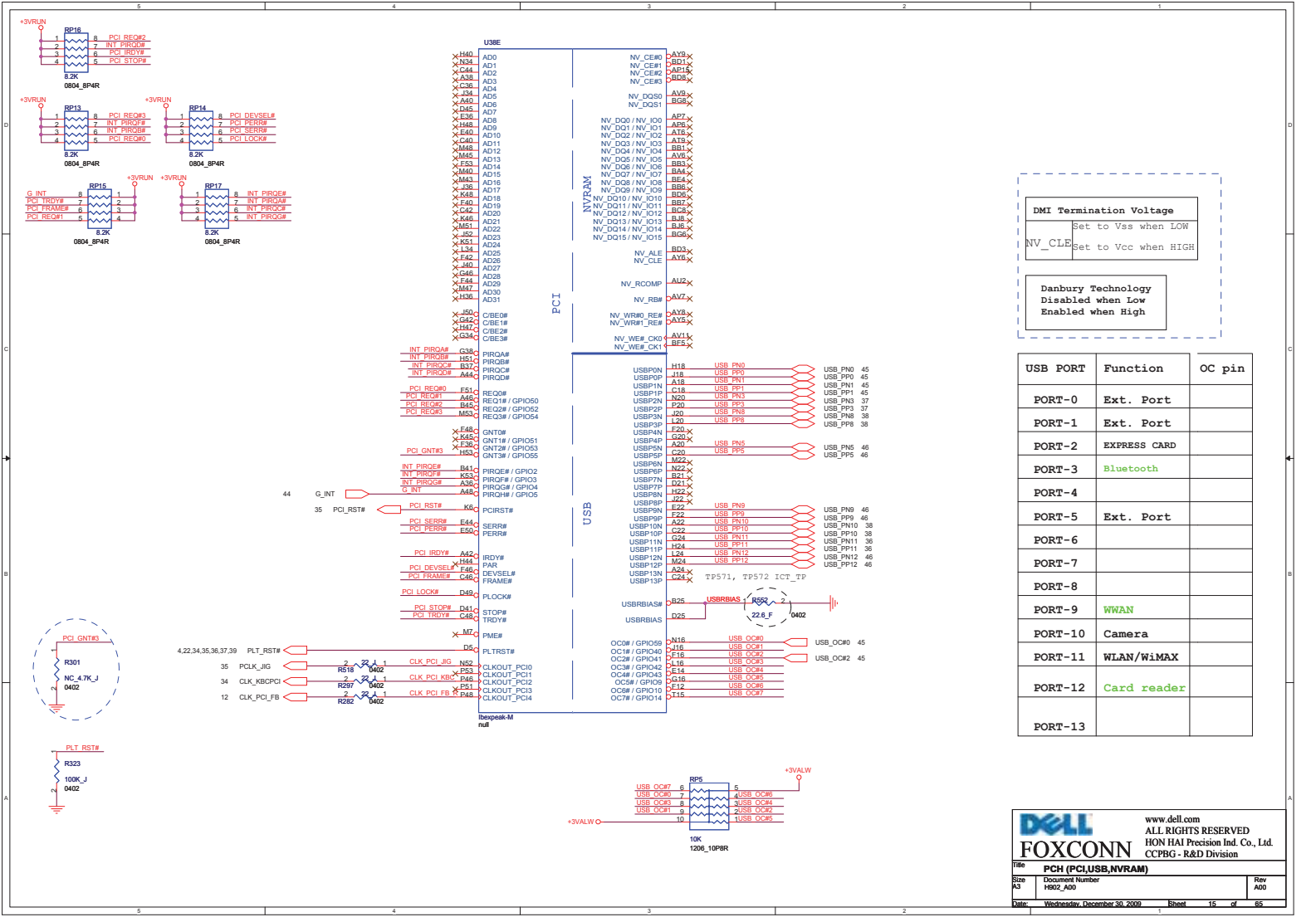


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CLOCK GEN

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DMI Termination Voltage
 NV_CLE Set to Vss when LOW
 Set to Vcc when HIGH

Danbury Technology
 Disabled when Low
 Enabled when High

USB PORT	Function	OC pin
PORT-0	Ext. Port	
PORT-1	Ext. Port	
PORT-2	EXPRESS CARD	
PORT-3	Bluetooth	
PORT-4		
PORT-5	Ext. Port	
PORT-6		
PORT-7		
PORT-8		
PORT-9	WWAN	
PORT-10	Camera	
PORT-11	WLAN/WiMAX	
PORT-12	Card reader	
PORT-13		

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USB

AV7	VSS1699	VSS2999	H49
B11	VSS1699	VSS2999	H5
B15	VSS1611	VSS2811	J24
B19	VSS1612	VSS2812	K43
B23	VSS1613	VSS2813	K47
B35	VSS1644	VSS2844	R7
B39	VSS1666	VSS2866	L14
B43	VSS1677	VSS2877	L18
B47	VSS1688	VSS2888	L2
B7	VSS1699	VSS2899	L22
BG12	VSS1770	VSS2970	L32
BG16	VSS1771	VSS2971	L40
BG20	VSS1772	VSS2972	L44
BG24	VSS1773	VSS2973	L52
BG28	VSS1774	VSS2974	M12
BG32	VSS1775	VSS2975	M16
BG36	VSS1776	VSS2976	N38
BG40	VSS1777	VSS2977	N38
BG44	VSS1778	VSS2978	M34
BG48	VSS1779	VSS2979	M38
BG52	VSS1800	VSS2980	M42
BG56	VSS1801	VSS2981	M46
BG60	VSS1802	VSS2982	M49
BG64	VSS1803	VSS2983	M8
BG68	VSS1804	VSS2984	M8
BG72	VSS1805	VSS2985	N24
BG76	VSS1806	VSS2986	P11
BG80	VSS1807	VSS2987	AD15
BG84	VSS1808	VSS2988	P22
BG88	VSS1809	VSS2989	F50
BG92	VSS1810	VSS2990	P32
BG96	VSS1811	VSS2991	P34
BG100	VSS1812	VSS2992	P42
BG104	VSS1813	VSS2993	P46
BG108	VSS1814	VSS2994	P47
BG112	VSS1815	VSS2995	R2
BG116	VSS1816	VSS2996	R2
BG120	VSS1817	VSS2997	T41
BG124	VSS1818	VSS2998	T46
BG128	VSS1819	VSS2999	T49
BG132	VSS1820	VSS3000	T8
BG136	VSS1821	VSS3001	T8
BG140	VSS1822	VSS3002	U30
BG144	VSS1823	VSS3003	U31
BG148	VSS1824	VSS3004	U32
BG152	VSS1825	VSS3005	U34
BG156	VSS1826	VSS3006	P38
BG160	VSS1827	VSS3007	P11
BG164	VSS1828	VSS3008	P16
BG168	VSS1829	VSS3009	P16
BG172	VSS1830	VSS3010	V20
BG176	VSS1831	VSS3011	V22
BG180	VSS1832	VSS3012	V20
BG184	VSS1833	VSS3013	V31
BG188	VSS1834	VSS3014	V31
BG192	VSS1835	VSS3015	V34
BG196	VSS1836	VSS3016	V36
BG200	VSS1837	VSS3017	V38
BG204	VSS1838	VSS3018	V45
BG208	VSS1839	VSS3019	V43
BG212	VSS1840	VSS3020	V47
BG216	VSS1841	VSS3021	V46
BG220	VSS1842	VSS3022	V49
BG224	VSS1843	VSS3023	V5
BG228	VSS1844	VSS3024	V7
BG232	VSS1845	VSS3025	V8
BG236	VSS1846	VSS3026	V2
BG240	VSS1847	VSS3027	W52
BG244	VSS1848	VSS3028	Y11
BG248	VSS1849	VSS3029	Y12
BG252	VSS1850	VSS3030	Y15
BG256	VSS1851	VSS3031	Y15
BG260	VSS1852	VSS3032	Y23
BG264	VSS1853	VSS3033	Y28
BG268	VSS1854	VSS3034	Y30
BG272	VSS1855	VSS3035	Y32
BG276	VSS1856	VSS3036	Y31
BG280	VSS1857	VSS3037	Y38
BG284	VSS1858	VSS3038	Y43
BG288	VSS1859	VSS3039	Y46
BG292	VSS1860	VSS3040	Y48
BG296	VSS1861	VSS3041	Y8
BG300	VSS1862	VSS3042	Y8
BG304	VSS1863	VSS3043	Y8
BG308	VSS1864	VSS3044	P24
BG312	VSS1865	VSS3045	T43
BG316	VSS1866	VSS3046	T43
BG320	VSS1867	VSS3047	AT8
BG324	VSS1868	VSS3048	AT8
BG328	VSS1869	VSS3049	AD47
BG332	VSS1870	VSS3050	Y47
BG336	VSS1871	VSS3051	AT12
BG340	VSS1872	VSS3052	AT15
BG344	VSS1873	VSS3053	AM5
BG348	VSS1874	VSS3054	AM5
BG352	VSS1875	VSS3055	AK45
BG356	VSS1876	VSS3056	AK39
BG360	VSS1877	VSS3057	AV14
BG364	VSS1878	VSS3058	AV14
BG368	VSS1879	VSS3059	AV14
BG372	VSS1880	VSS3060	AV14

USBH

AB16	VSS01	VSS809	AK30
AA18	VSS02	VSS810	AK31
AA20	VSS03	VSS811	AK32
AA22	VSS04	VSS812	AK32
AA19	VSS05	VSS813	AK34
AA24	VSS06	VSS814	AK35
AA26	VSS07	VSS815	AK35
AA28	VSS08	VSS816	AK43
AA30	VSS09	VSS817	AK46
AA31	VSS10	VSS818	AK48
AA32	VSS11	VSS819	AK5
AA33	VSS12	VSS820	AK3
AB15	VSS13	VSS821	AL2
AB16	VSS14	VSS822	AL24
AB17	VSS15	VSS823	AK11
AB18	VSS16	VSS824	AK11
AB19	VSS17	VSS825	AK11
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AB21	VSS19	VSS827	AK11
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AB23	VSS21	VSS829	AK11
AB24	VSS22	VSS830	AK11
AB25	VSS23	VSS831	AK11
AB26	VSS24	VSS832	AK11
AB27	VSS25	VSS833	AK11
AB28	VSS26	VSS834	AK11
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AB37	VSS35	VSS843	AK11
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AB82	VSS80	VSS888	AK11

DELL
FOXCONN

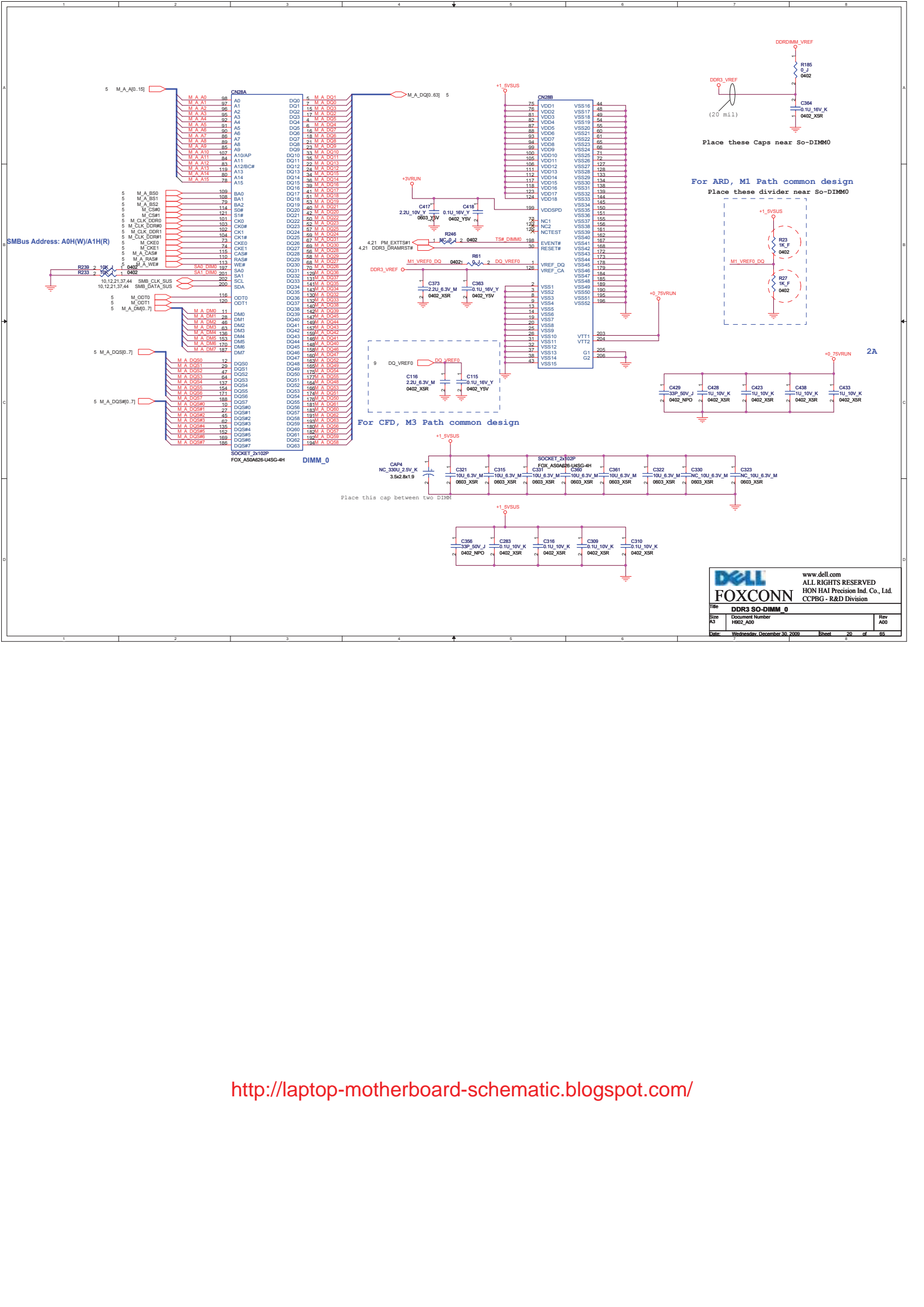
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PCH (VSS)

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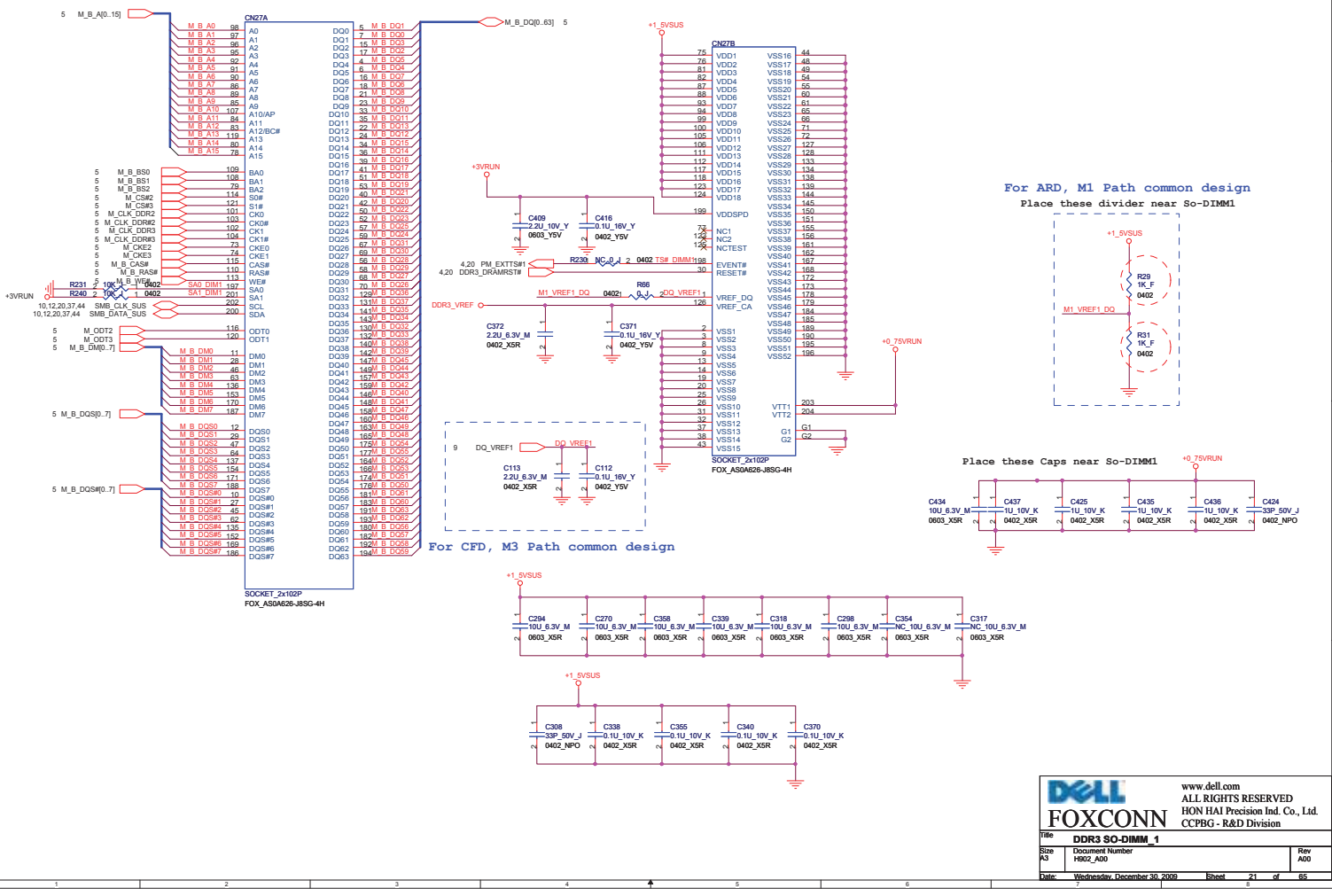
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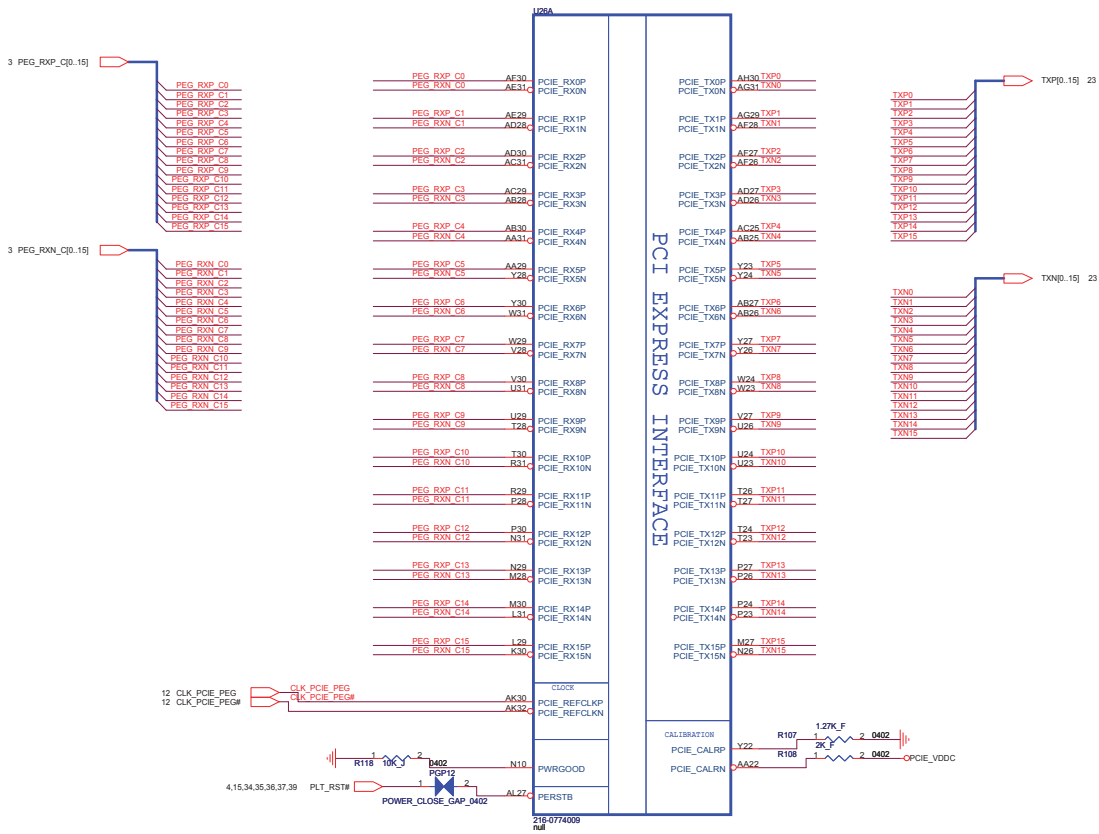
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DDR3 SO-DIMM 0

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Title: VGA (PCI-E) 1/6		
Size: A3	Document Number: H802_A00	Rev: A00
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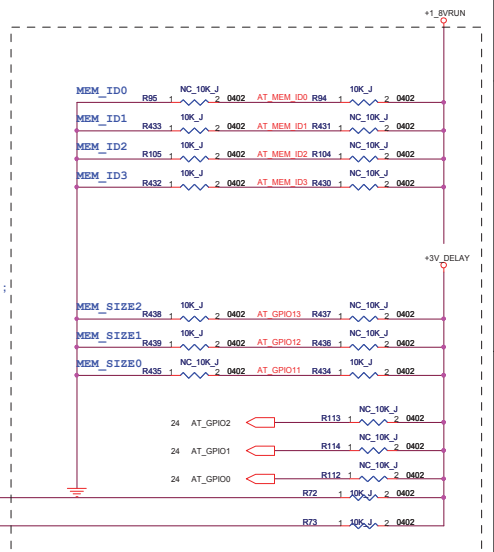
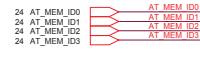
	Mount	NC
Samsung 1GB K4W2G1646B-HC12 P/N: 13-K4W2G16-3000	R432 (0), R105 (0) R433 (0), R94 (1)	R430 (1), R104 (1) R431 (1), R95 (0)
Hynix 1GB H5TQ2G63BFR-12C P/N: 13-H5T02G6-3000	R432 (0), R105 (0) R433 (0), R95 (0)	R430 (1), R104 (1) R431 (1), R94 (1)



Strap for DDR3
ATI_DVDPDATA[1:0 :21:20]
0000 128Mx16 Hynix 1GB
0001 128Mx16 Samsung 1GB

If no ROM attached, GPIO[13:12:11] ;
CONFIG(2:0)
controls the memory aperture size.
64MB 010
128MB 000
256MB 001
512MB 001

HSYNC , VSYNC
AUD[1] , AUD[0]
0,0 No audio function
0,1 Audio for DisplayPort and HDMI if dongle is detected
1,0 Audio for DisplayPort only
1,1 Audio for both DisplayPort and HDMI

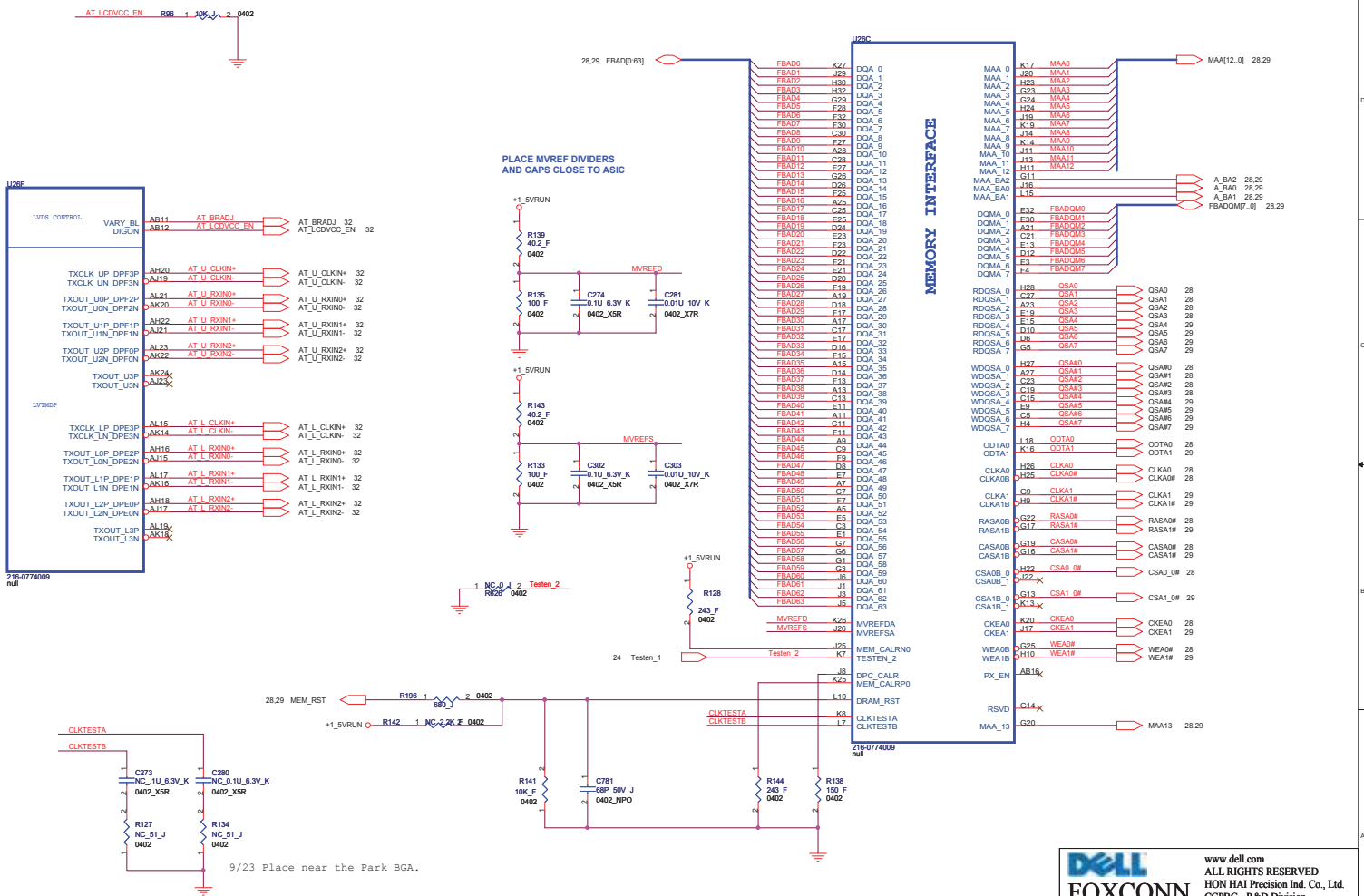


GPIO 0 : PCIE FULL TX OUTPUT SWING
GPIO 1 : PCIE TRANSMITTER DE-EMPHASIS ENABLED
GPIO 2 : PCIE GEN2 ENABLED

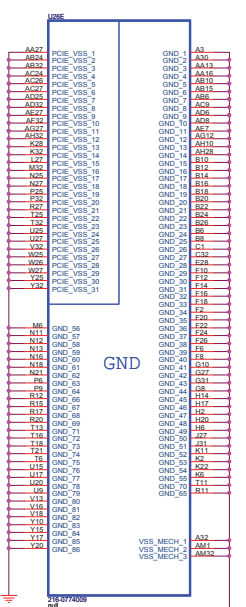
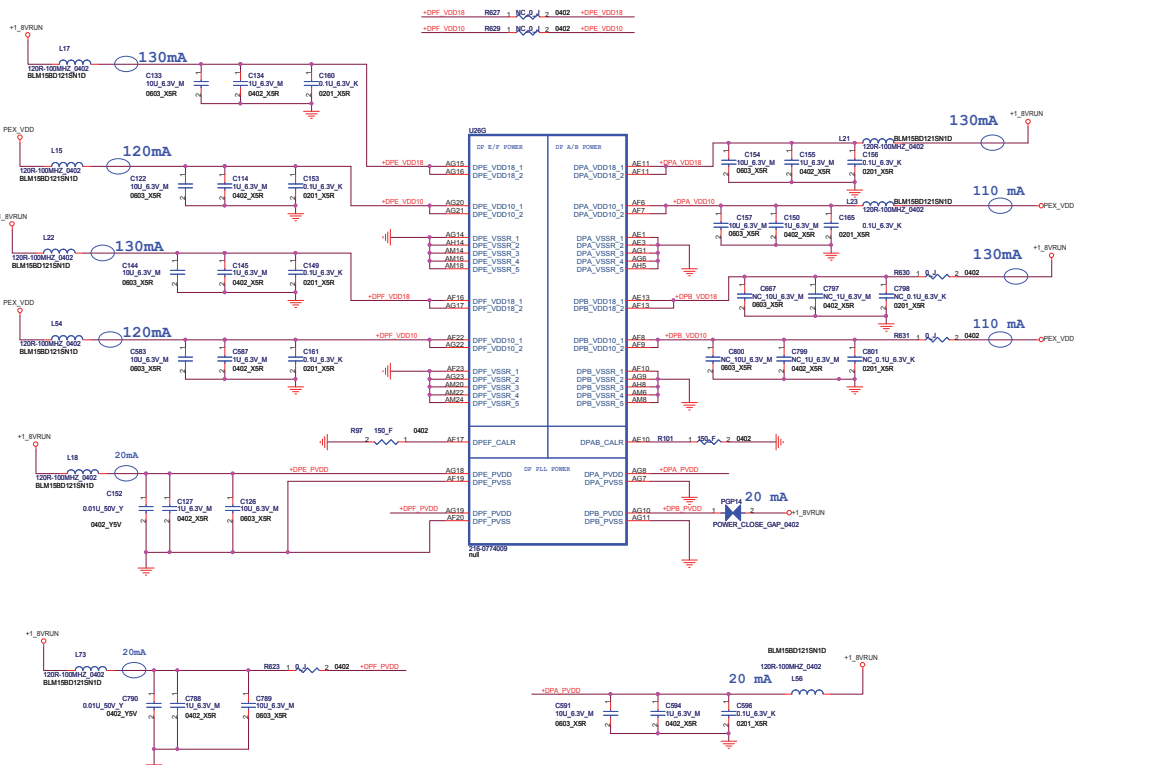
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Title: VGA (STRAP) 2/6		
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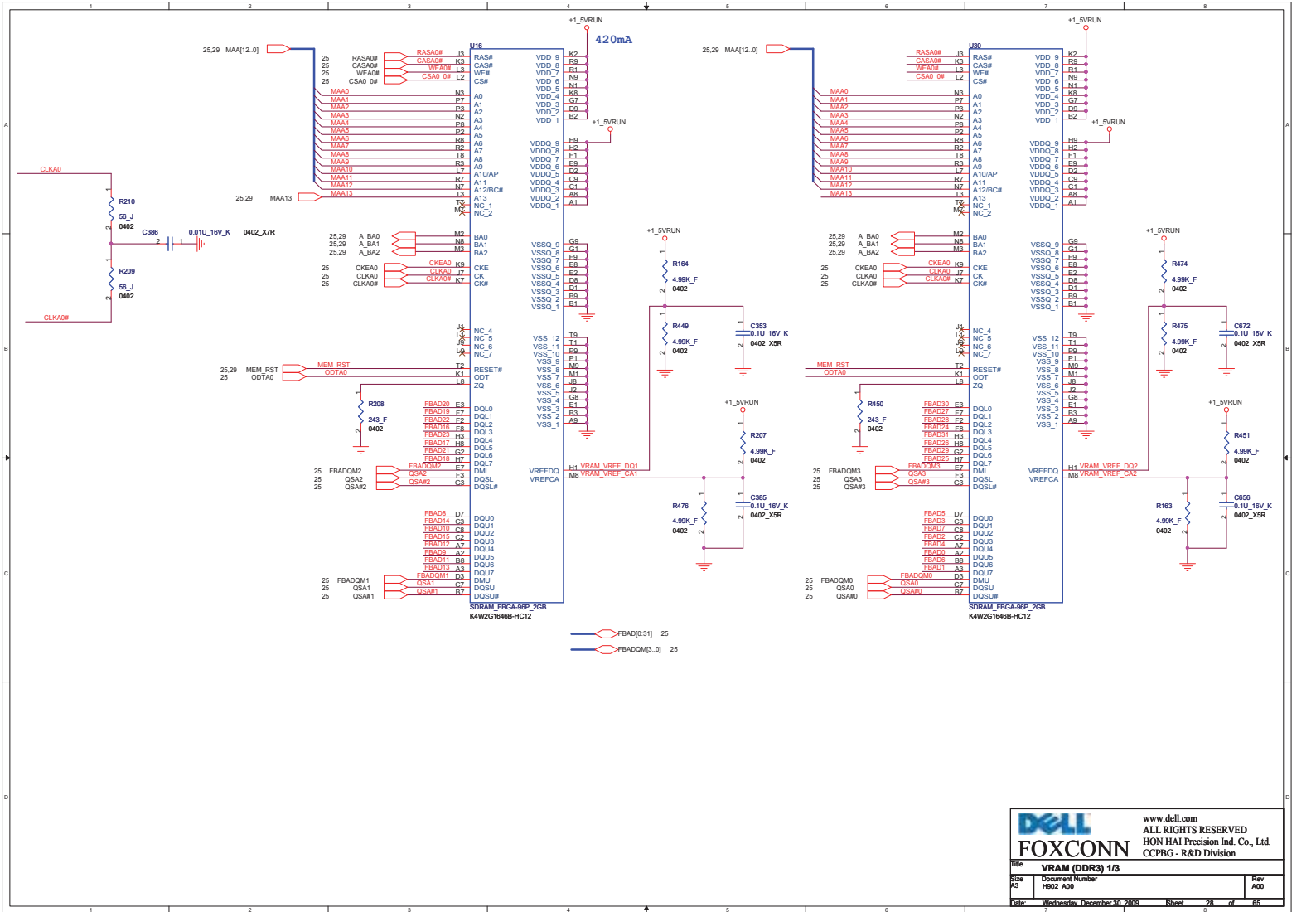
 HON HAI Precision Ind. Co., Ltd.

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File	VGA (POWER) 516	Rev	ADD
Doc	Document Number		
Control	1902_ADD		

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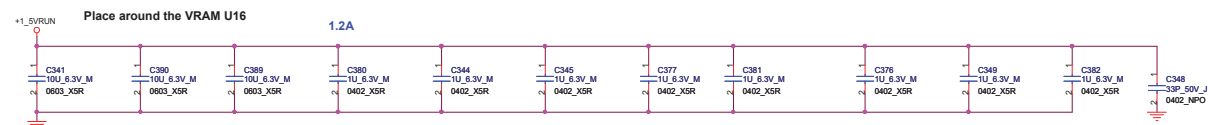
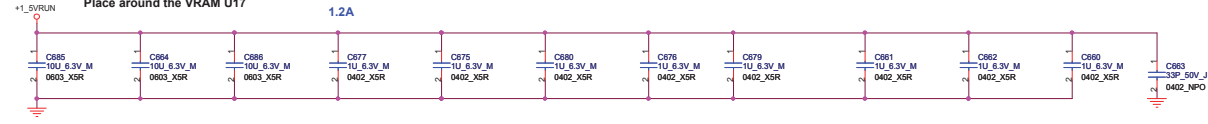
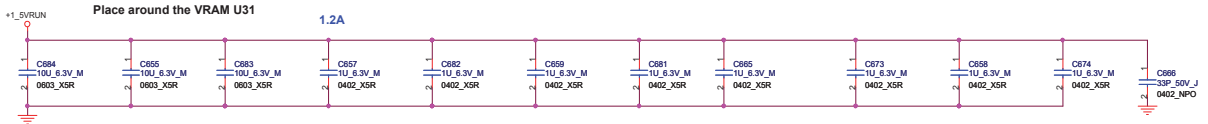
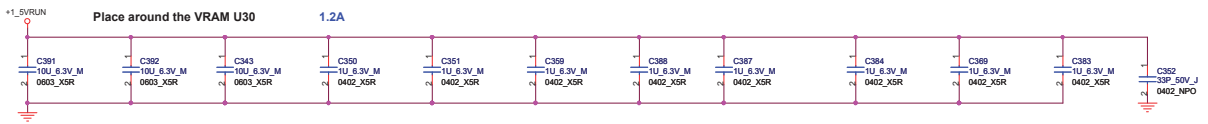
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VRAM (DDR3) 1/3

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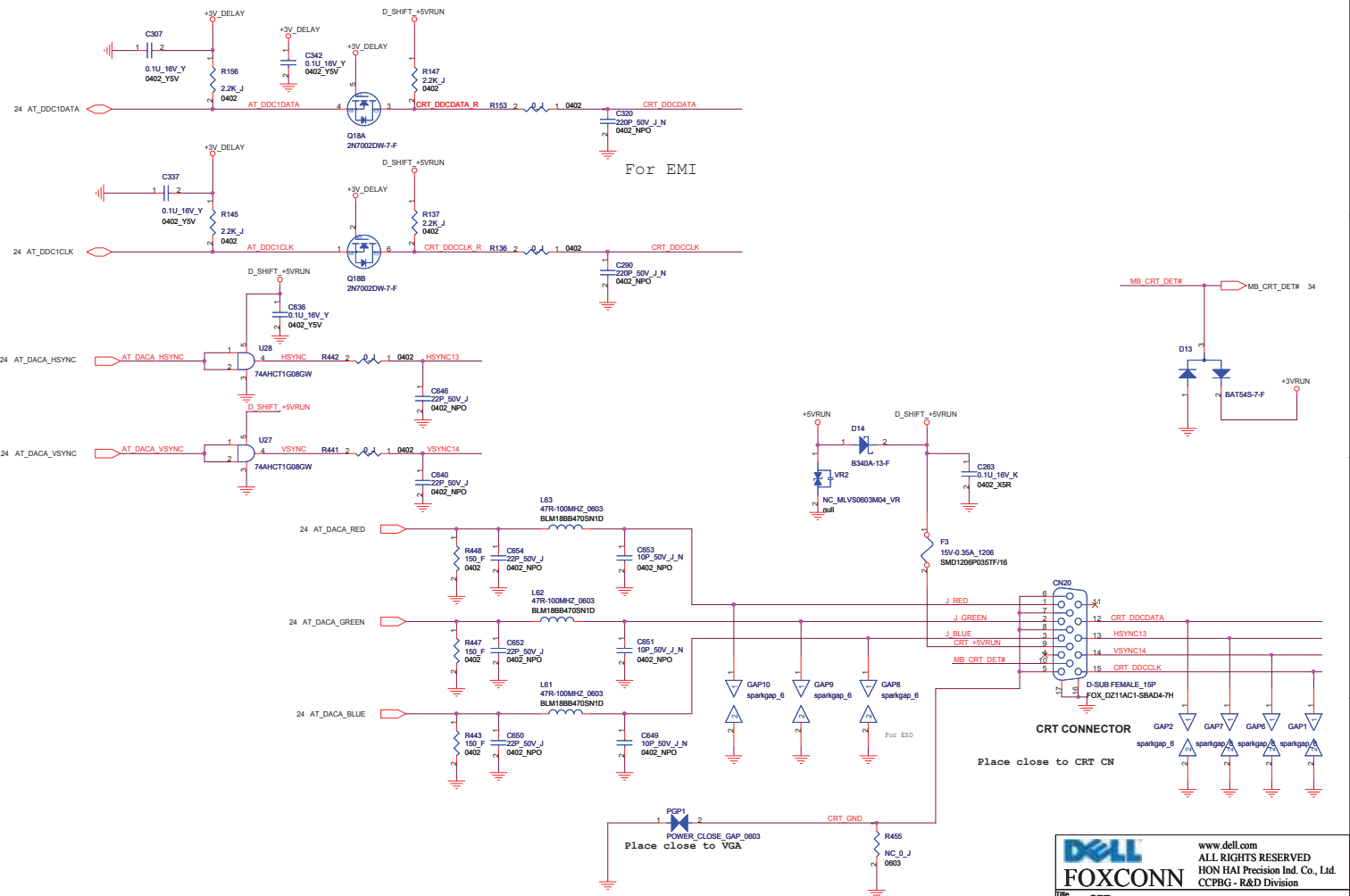
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VRAM (BYPASS) 3/3

Title:	Document Number	Rev
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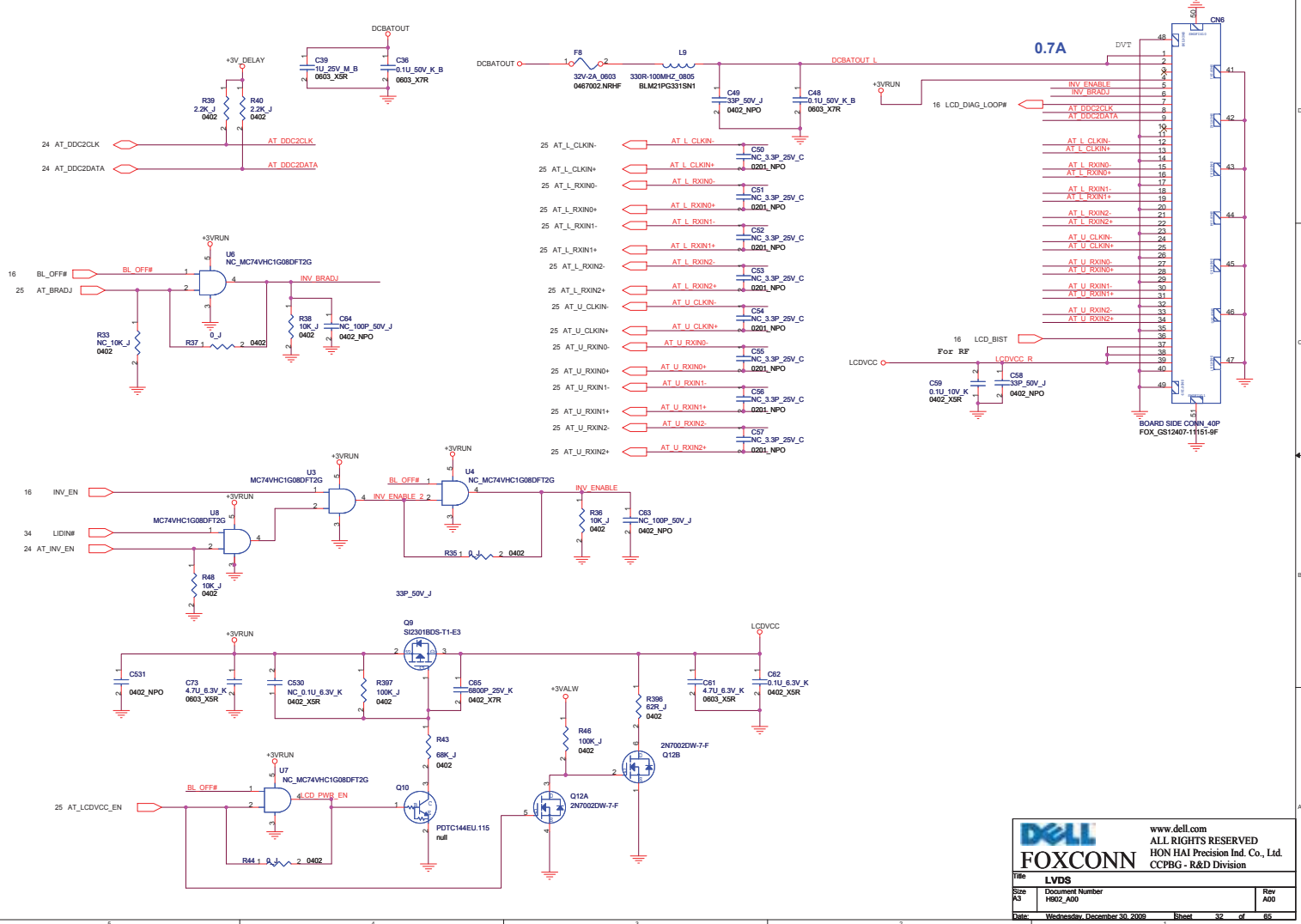


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Title: CRT		
Size: A3	Document Number: H802_A00	Rev: A00
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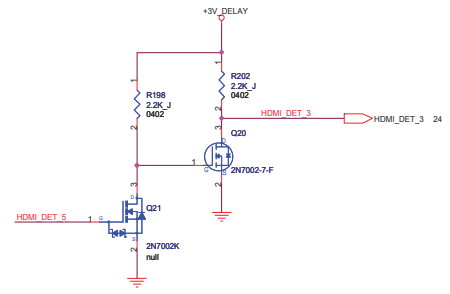
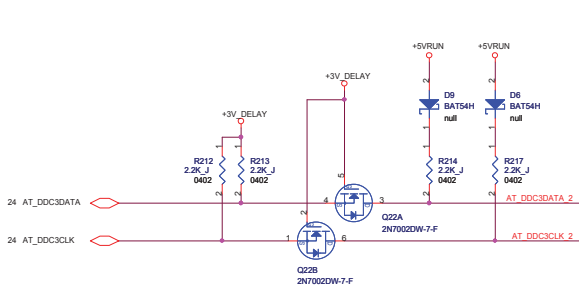




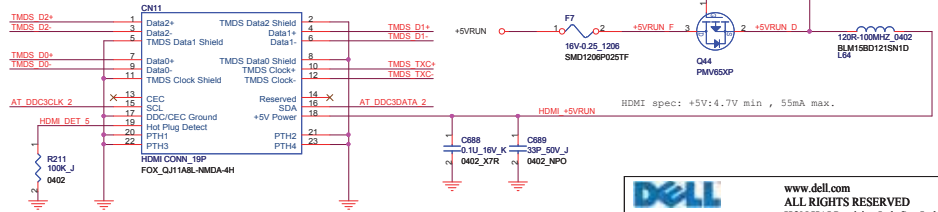
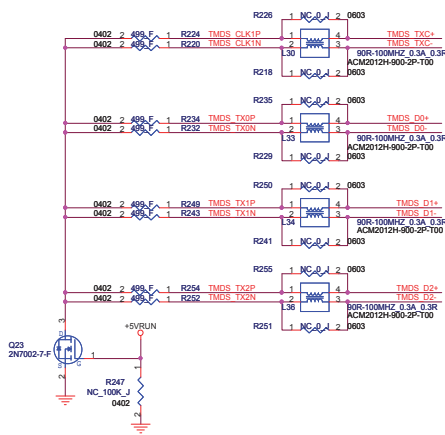
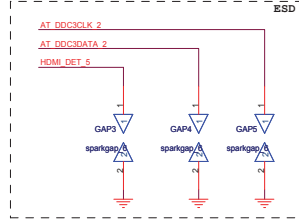

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Title: LVDS		
Size: A3	Document Number: H802_A00	Rev: A00
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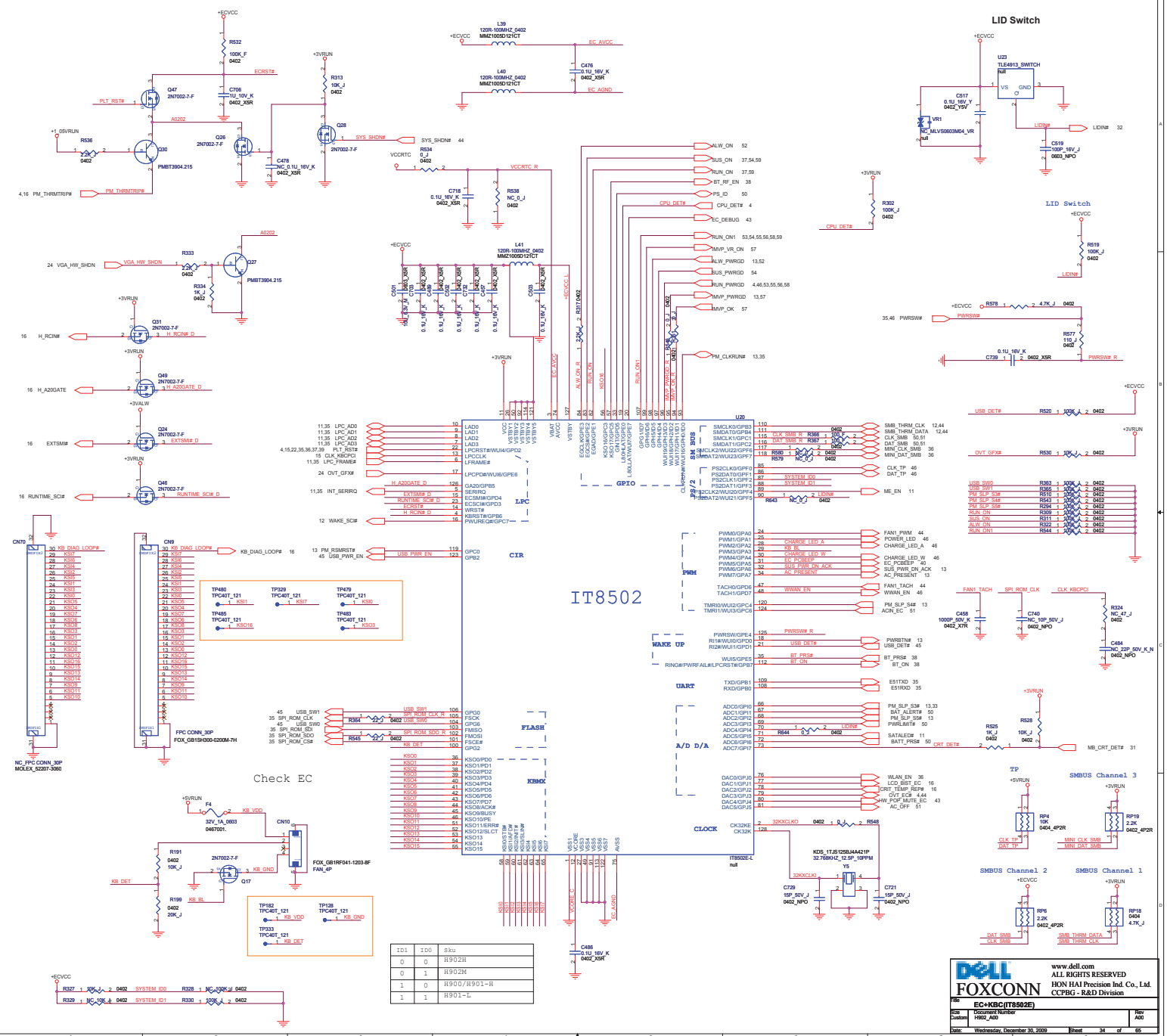


- 24 TMSD_CLKIN → TMSD_CLKIN
- 24 TMSD_CLK1P → TMSD_CLK1P
- 24 TMSD_TX0N → TMSD_TX0N
- 24 TMSD_TX0P → TMSD_TX0P
- 24 TMSD_TX1N → TMSD_TX1N
- 24 TMSD_TX1P → TMSD_TX1P
- 24 TMSD_TX2N → TMSD_TX2N
- 24 TMSD_TX2P → TMSD_TX2P



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Title: HDMI		
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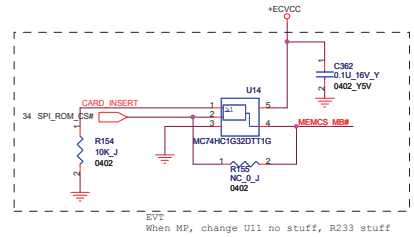
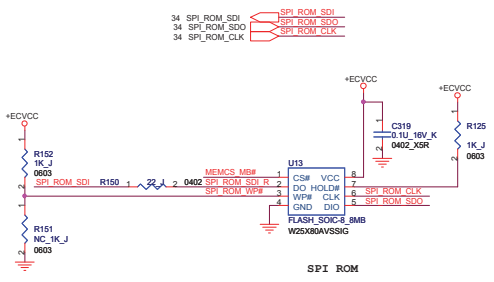


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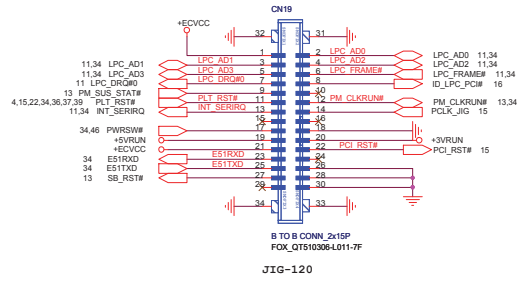
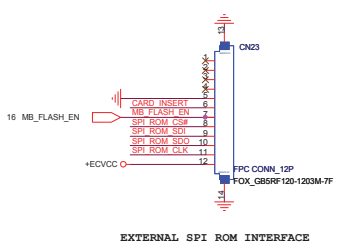
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Part: EC-KBC(IT8502E)
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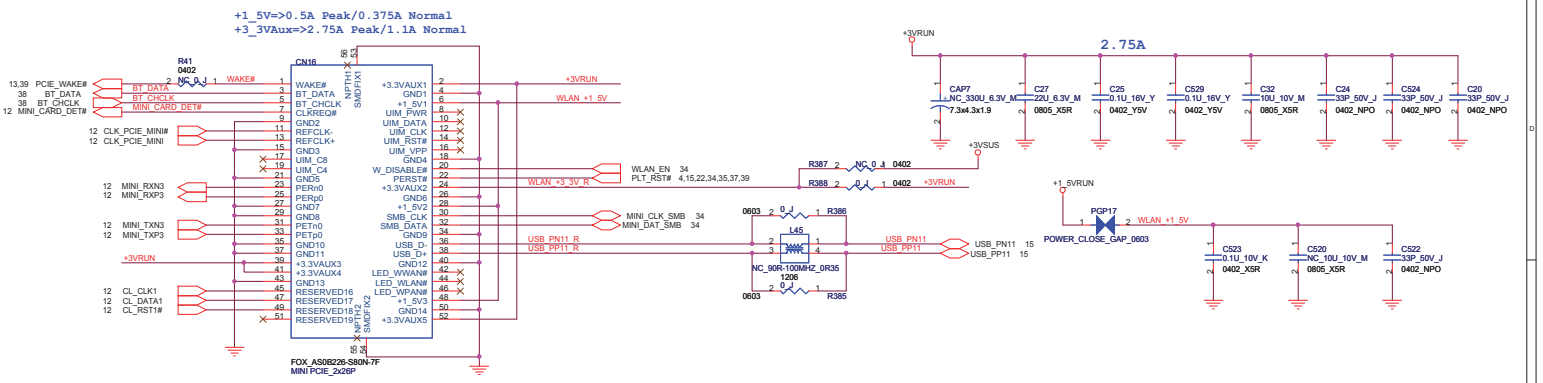


Discuss with SW about BIOS Capacity

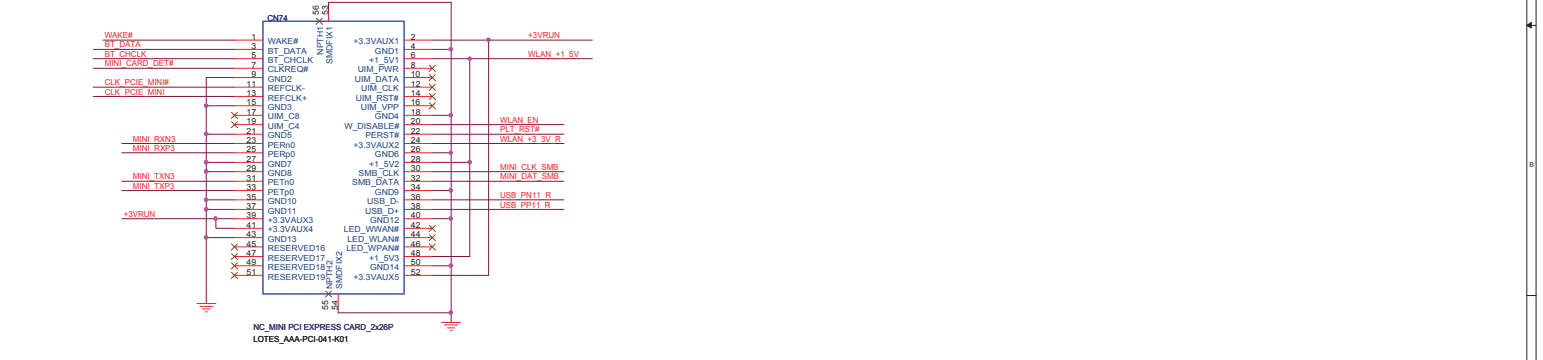


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		Flash ROM/SPI	
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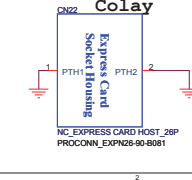
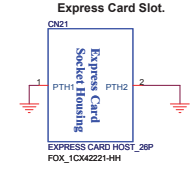
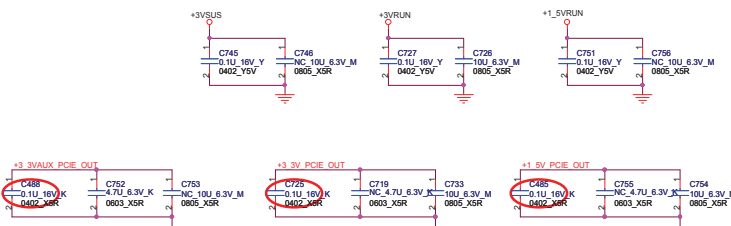
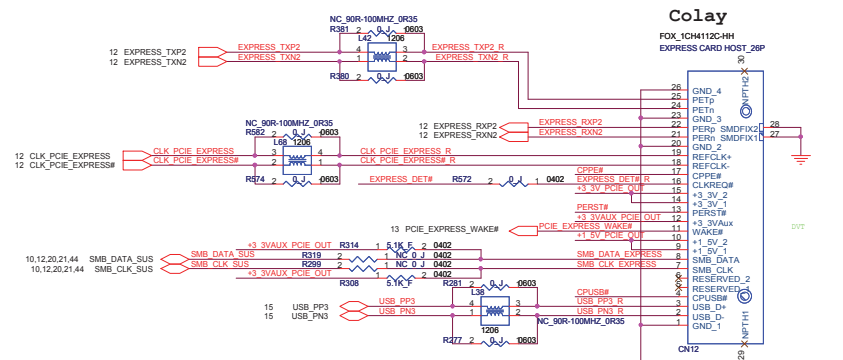
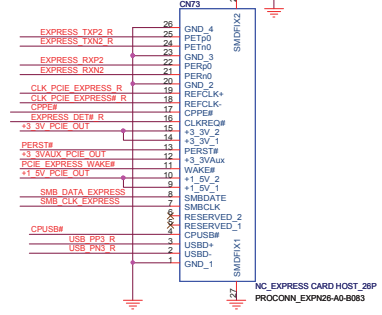
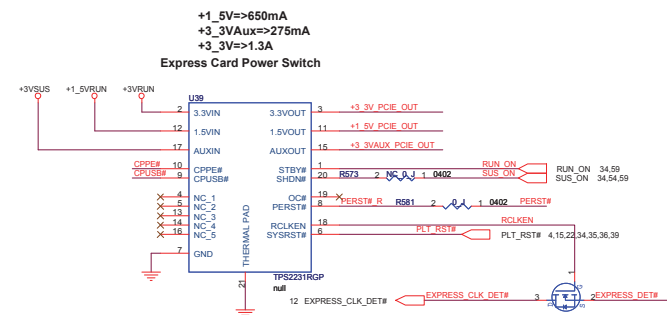
Half Mini Card for WLAN or WiMAX



NC Mini PCI Express Card 2x28P
LOTES_AA-PCI-041-K01

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		WLAN/Wimax Mini-PCIe Card	
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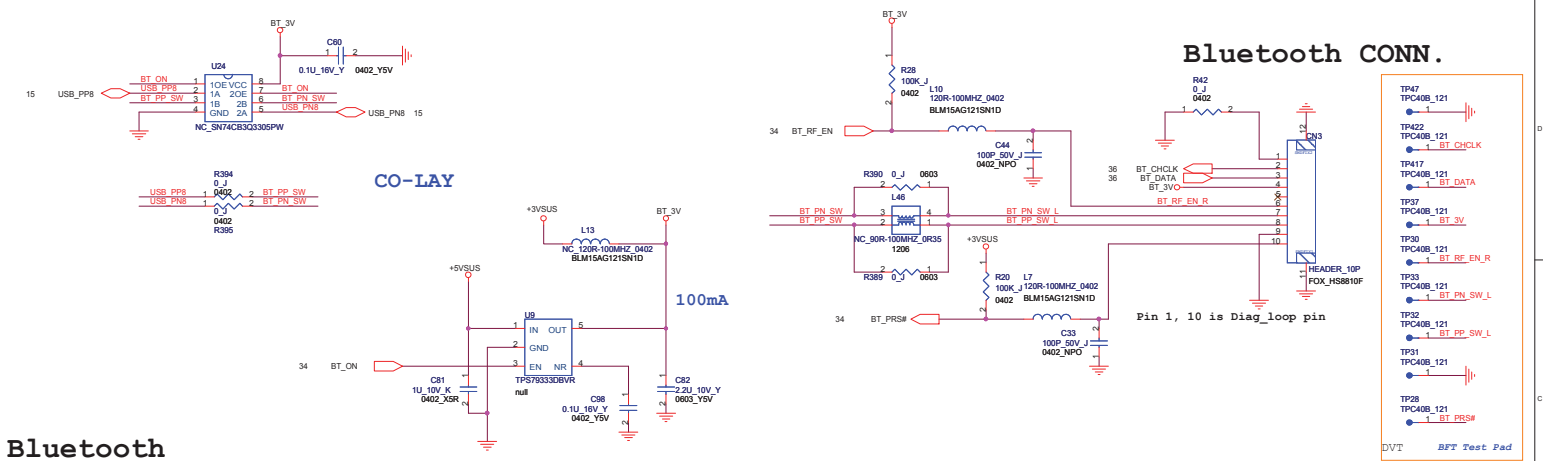
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Express card

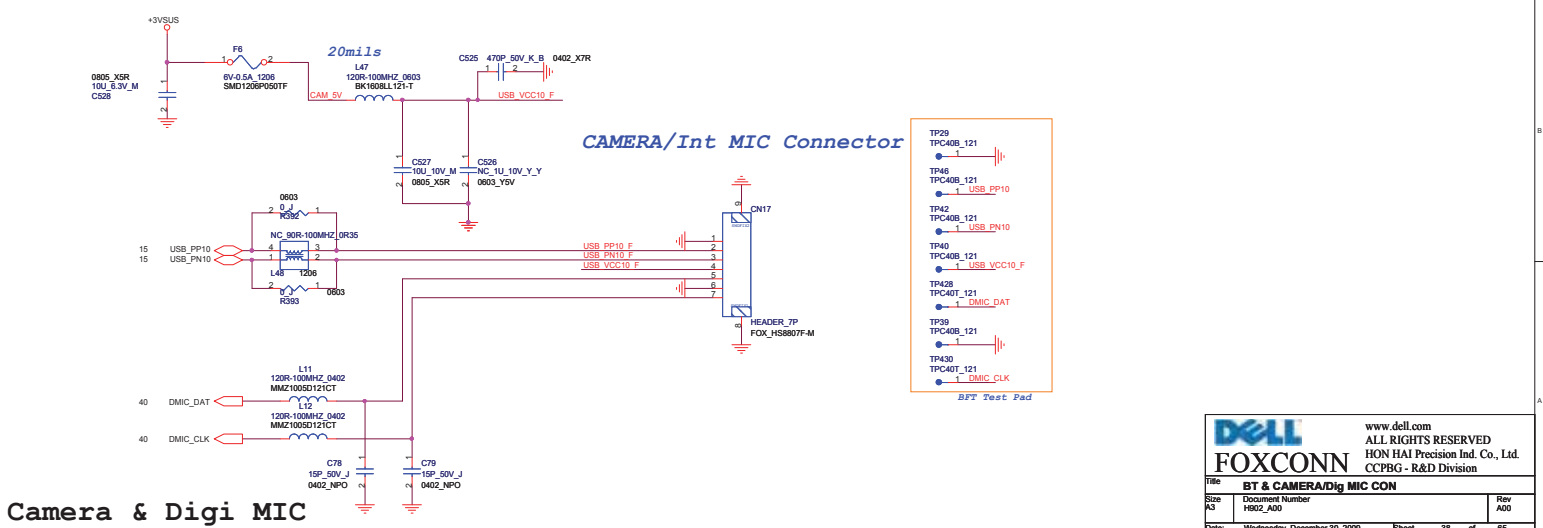
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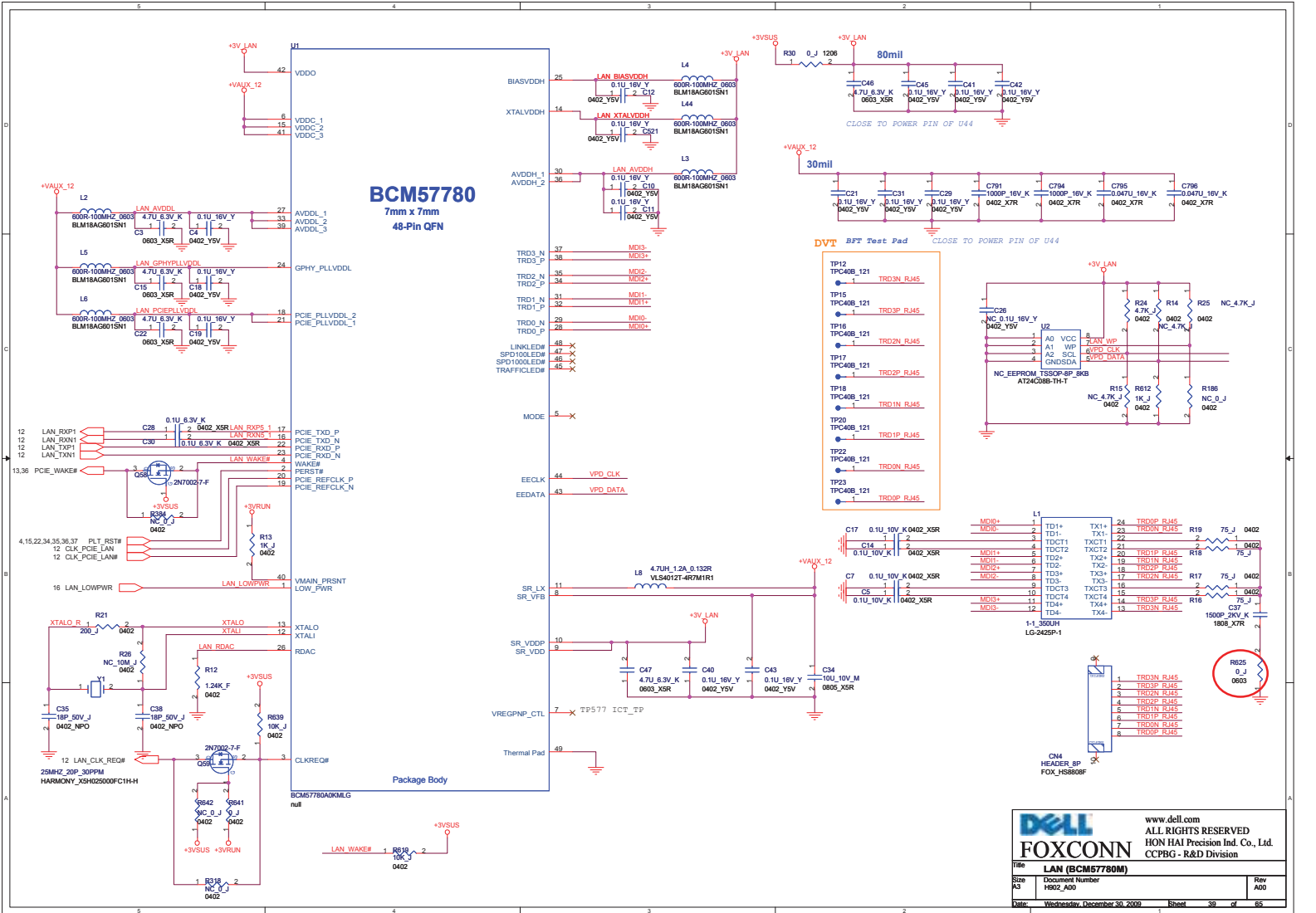
Bluetooth



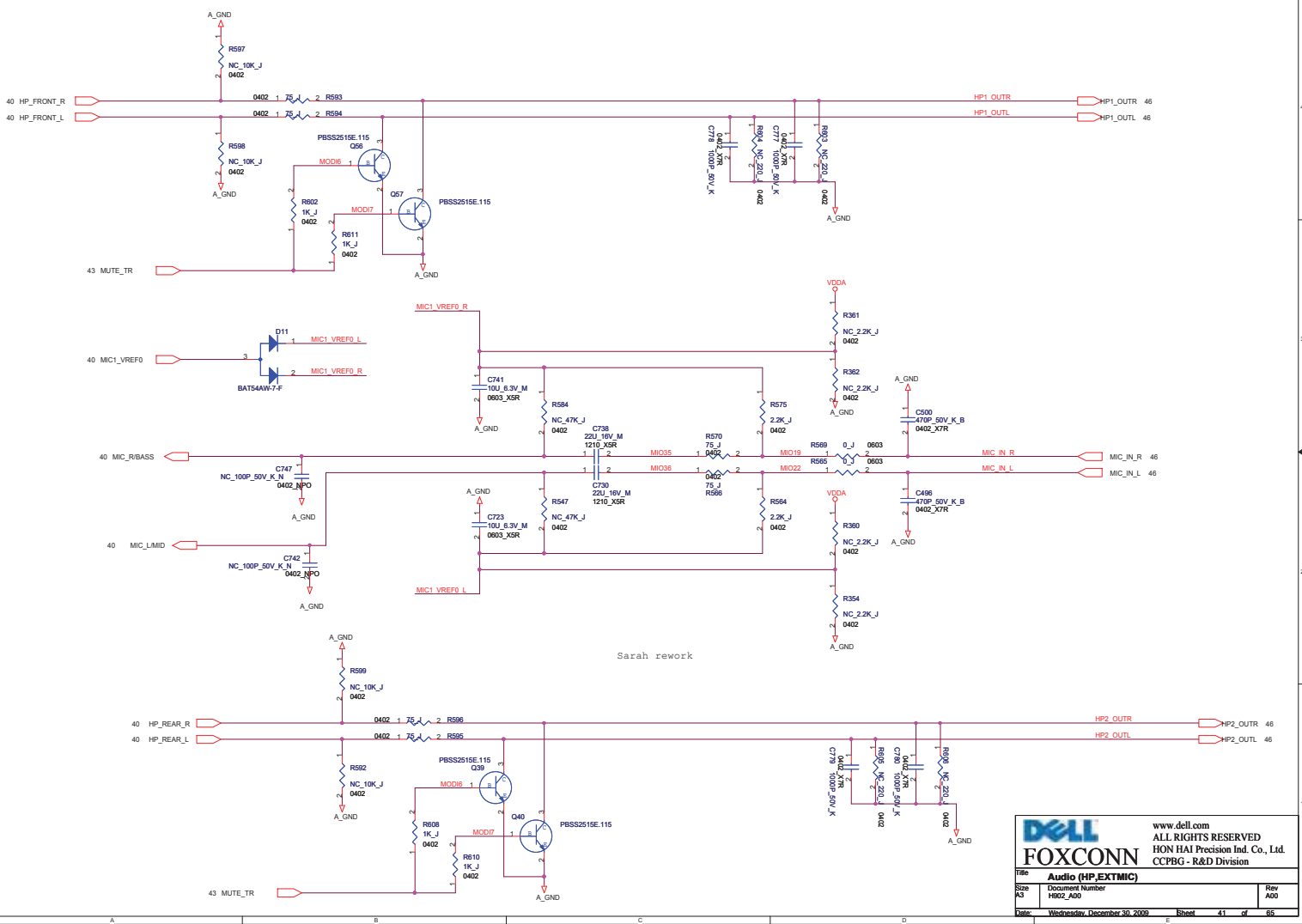
Camera & Digi MIC

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BT & CAMERA/Dig MIC CON		
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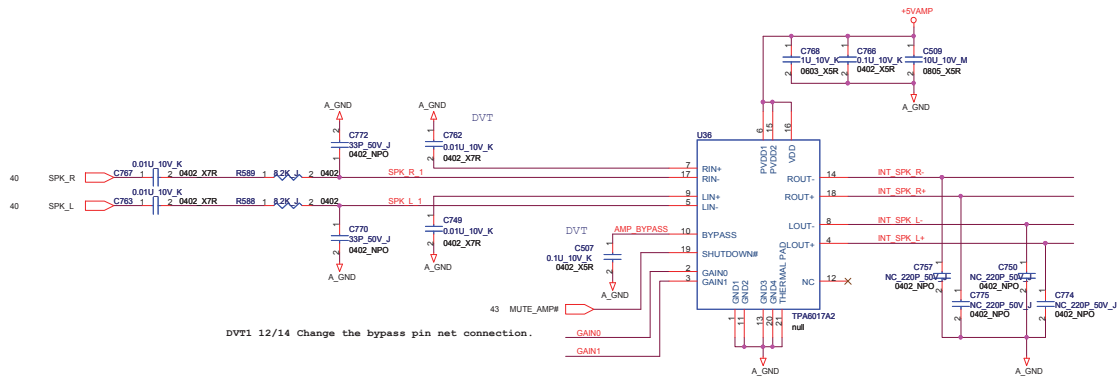
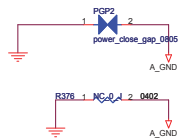
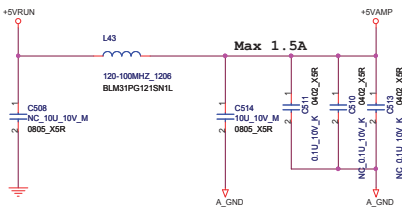
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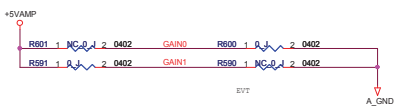
Sarah rework

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Audio (HP,EXTMIC)		HON HAI Precision Ind. Co., Ltd.	
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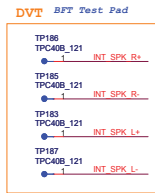
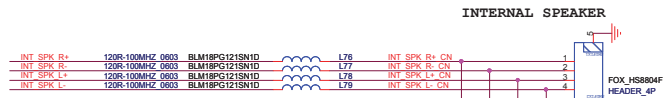
DVT1 12/14 Change the bypass pin net connection.



SPEAKER AMP

	GAIN0	GAIN1
6 dB	0	0
10 dB	0	1
15.6 dB	1	0
21.6 dB	1	1

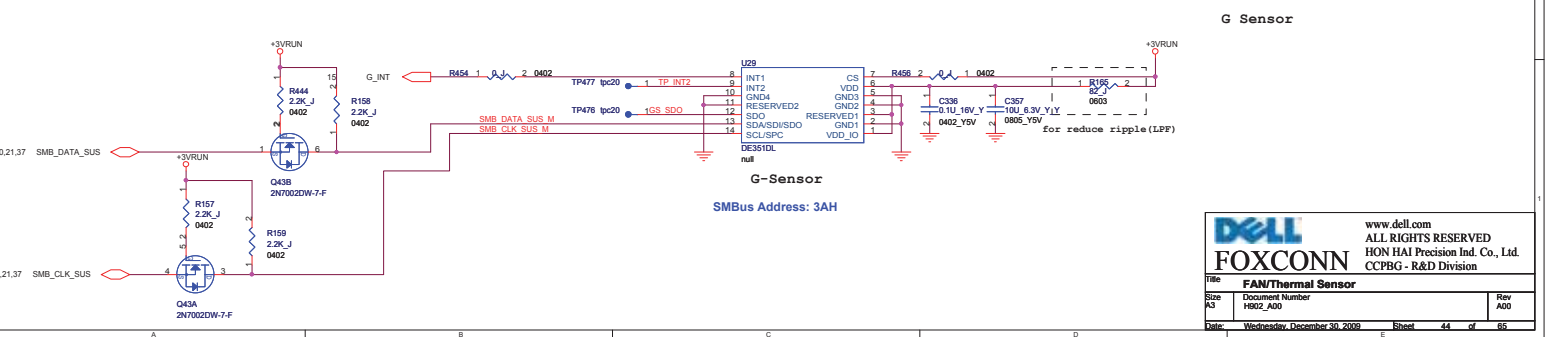
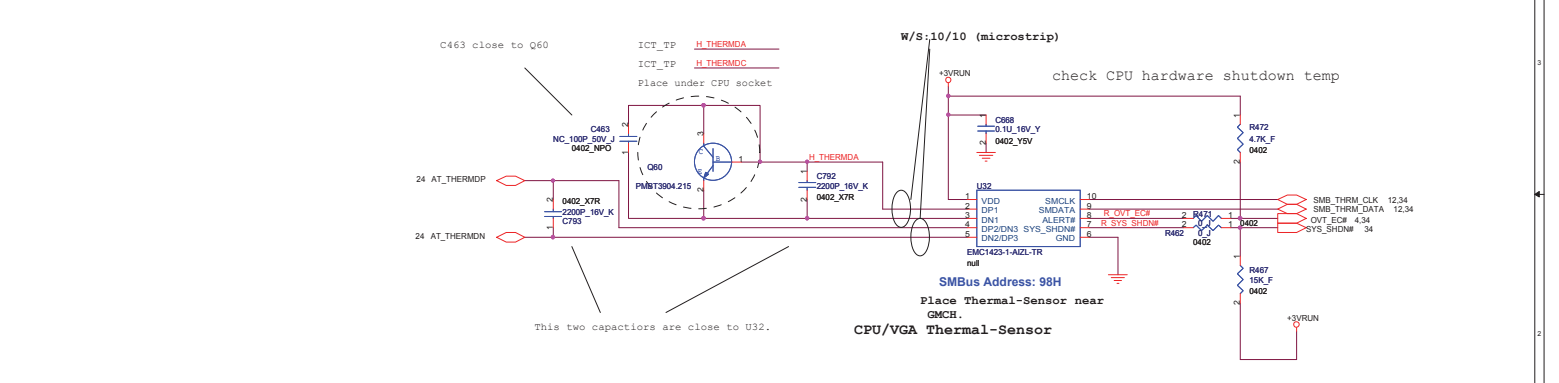
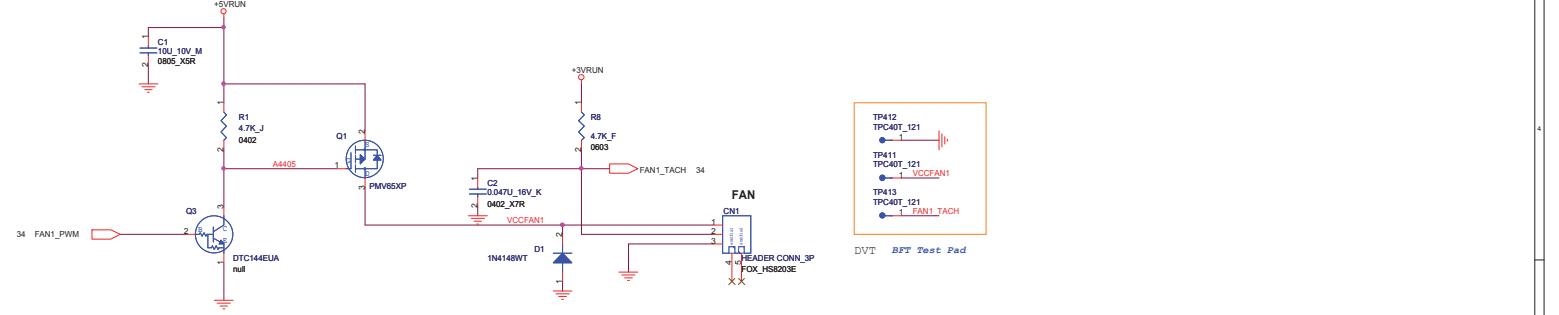
$dB = 20 \log Gain$
 If set 10dB, gain is 3.162.
 $P_o = \{(1.2V_{rms} * 3.162)^2\} / 4 = 3.599 W$



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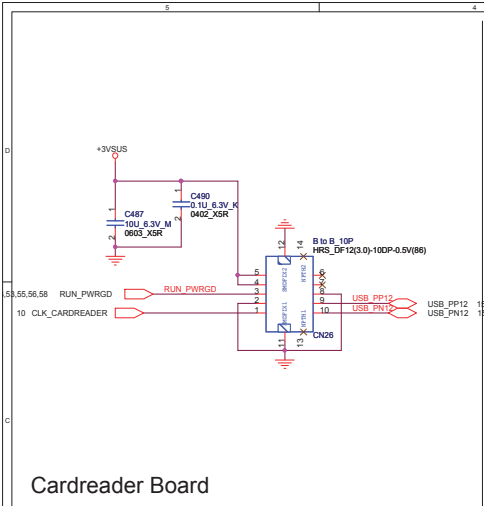


G Sensor

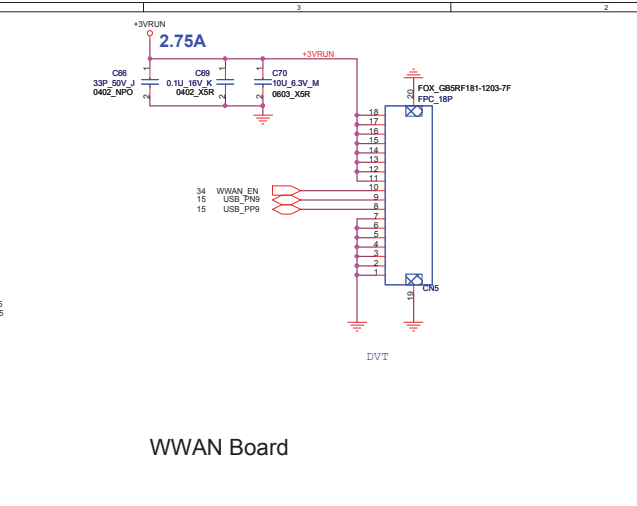
SMBus Address: 3AH

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FAN/Thermal Sensor					
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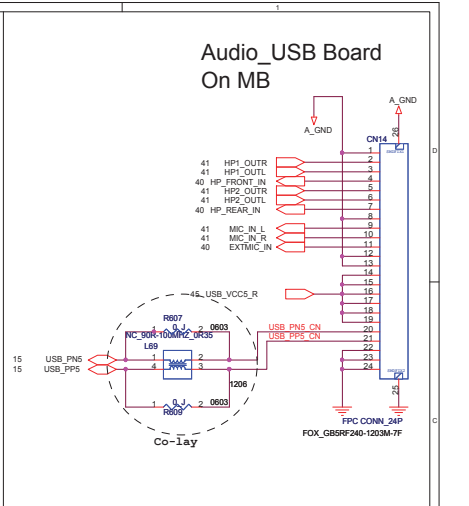
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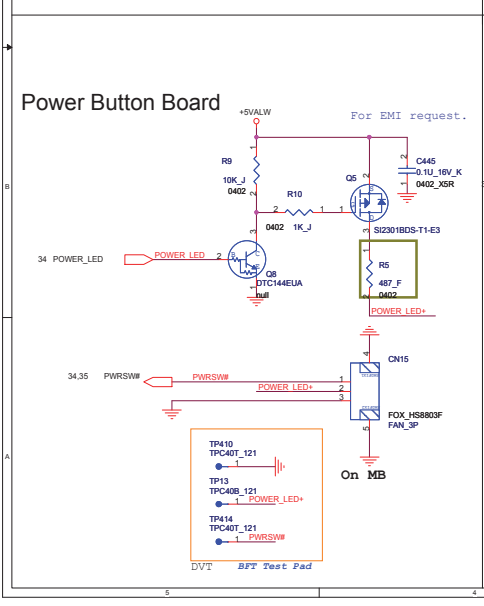
Cardreader Board



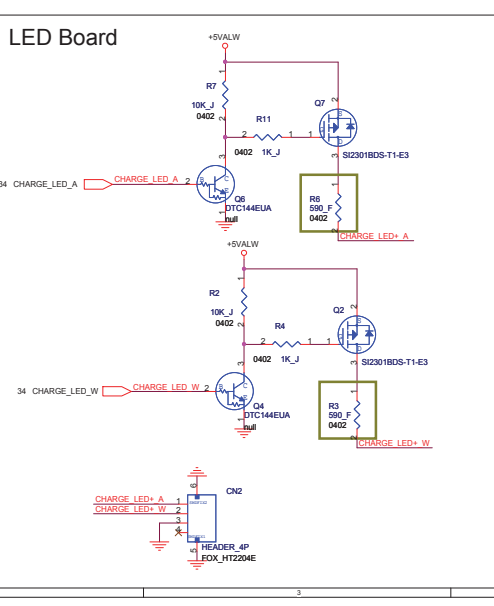
WWAN Board



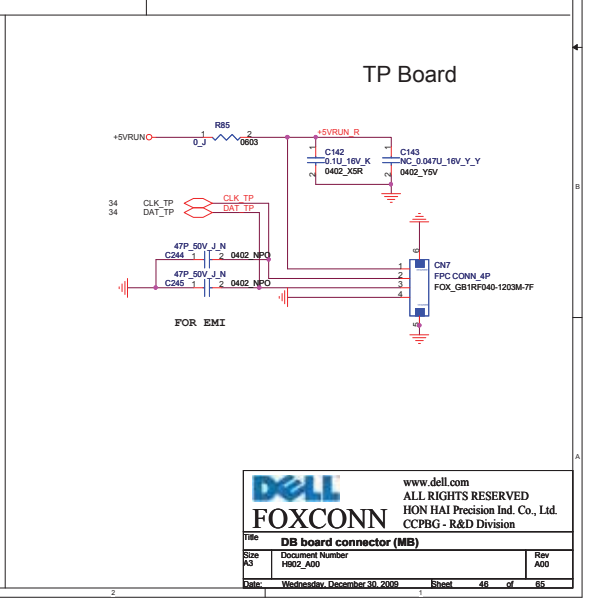
Audio_USB Board On MB



Power Button Board



LED Board



TP Board

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FOXCONN

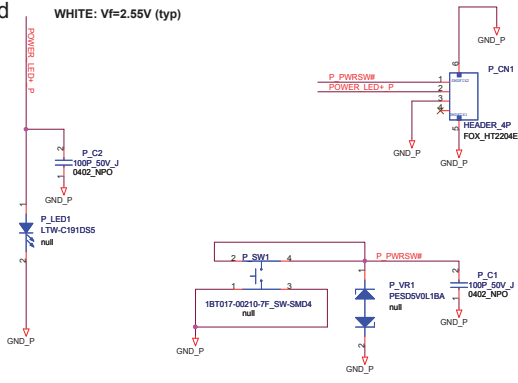
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DB board connector (MB)

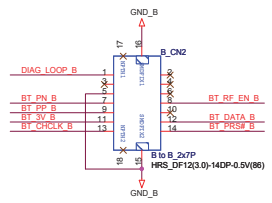
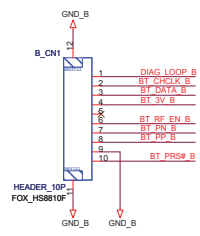
Title:	Document Number:	Rev:
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Power Button Board

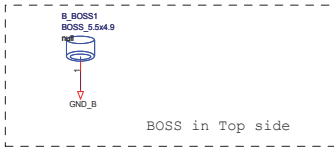
WHITE: Vf=2.55V (typ)



POWER BUTTON



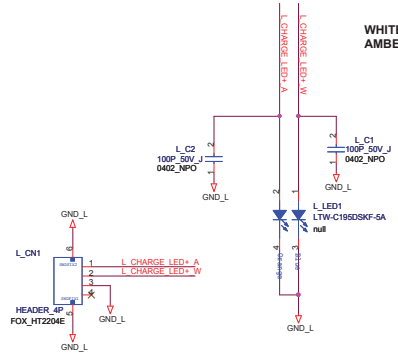
Bluetooth CONN.



Bluetooth Board

LED Board

WHITE: Vf=2.55V (typ)
AMBER: Vf=2.0V (typ)

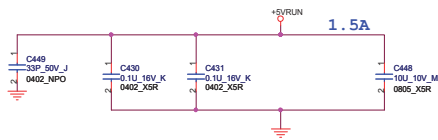


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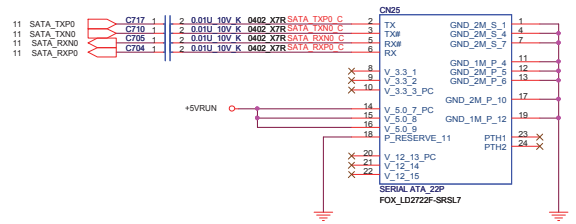
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Title: PWR_BTN&LED&BT DB

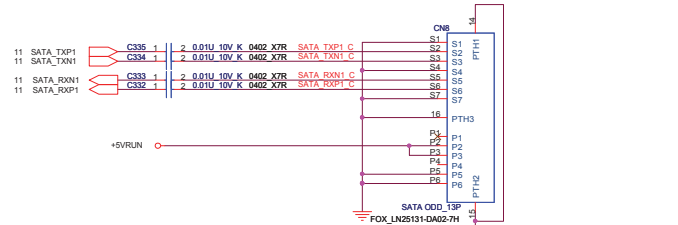
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SATA HDD CONN

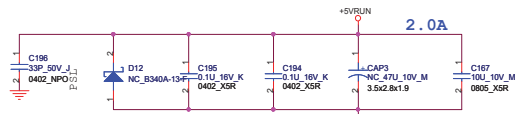


SATA ODD CONN



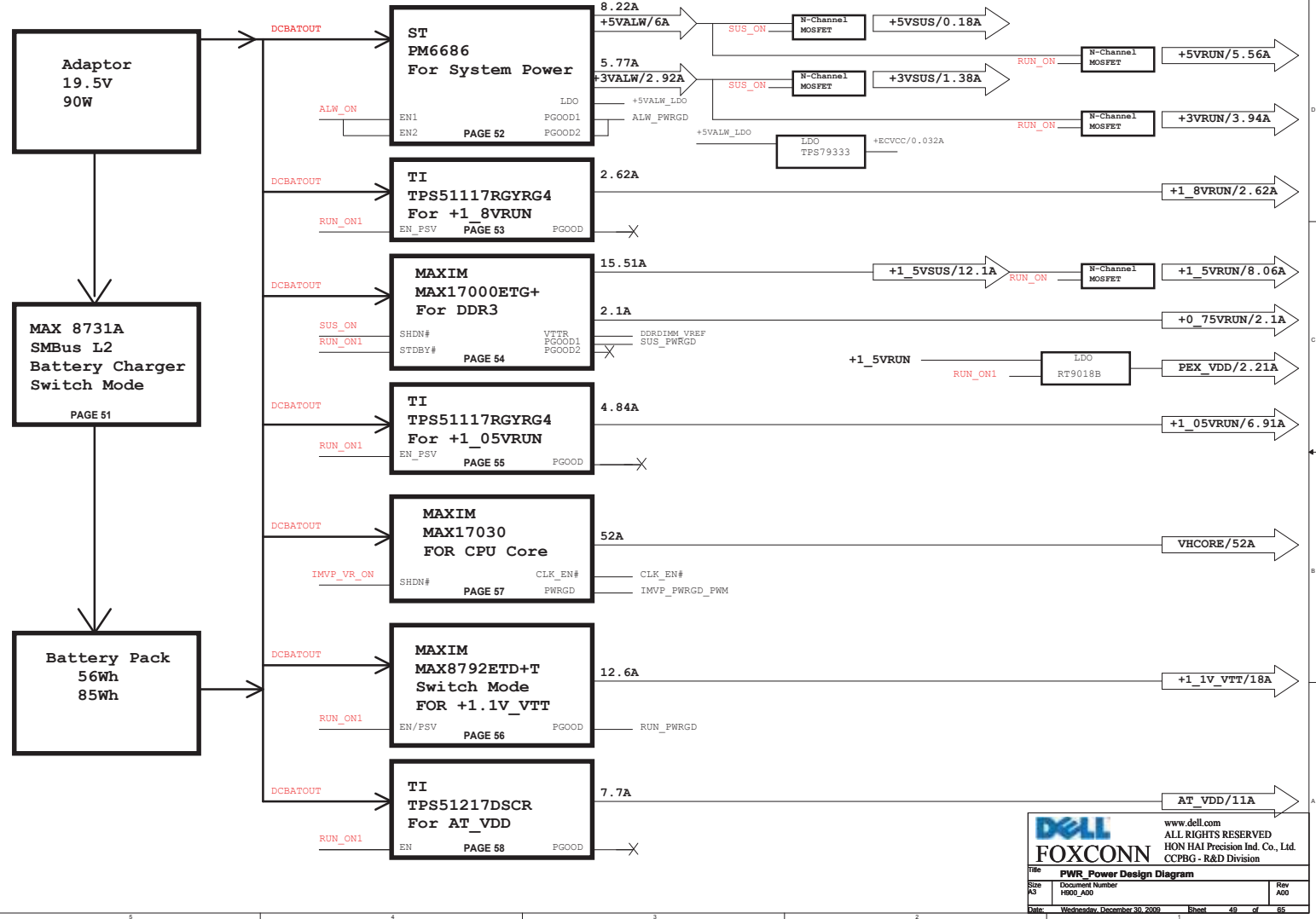
ODD CON ADAPTER

Add CN68 need 2N-0013009-FRG0 in BOM



Consider to change to Flash board connector.

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Title: SATA HDD/ODD			
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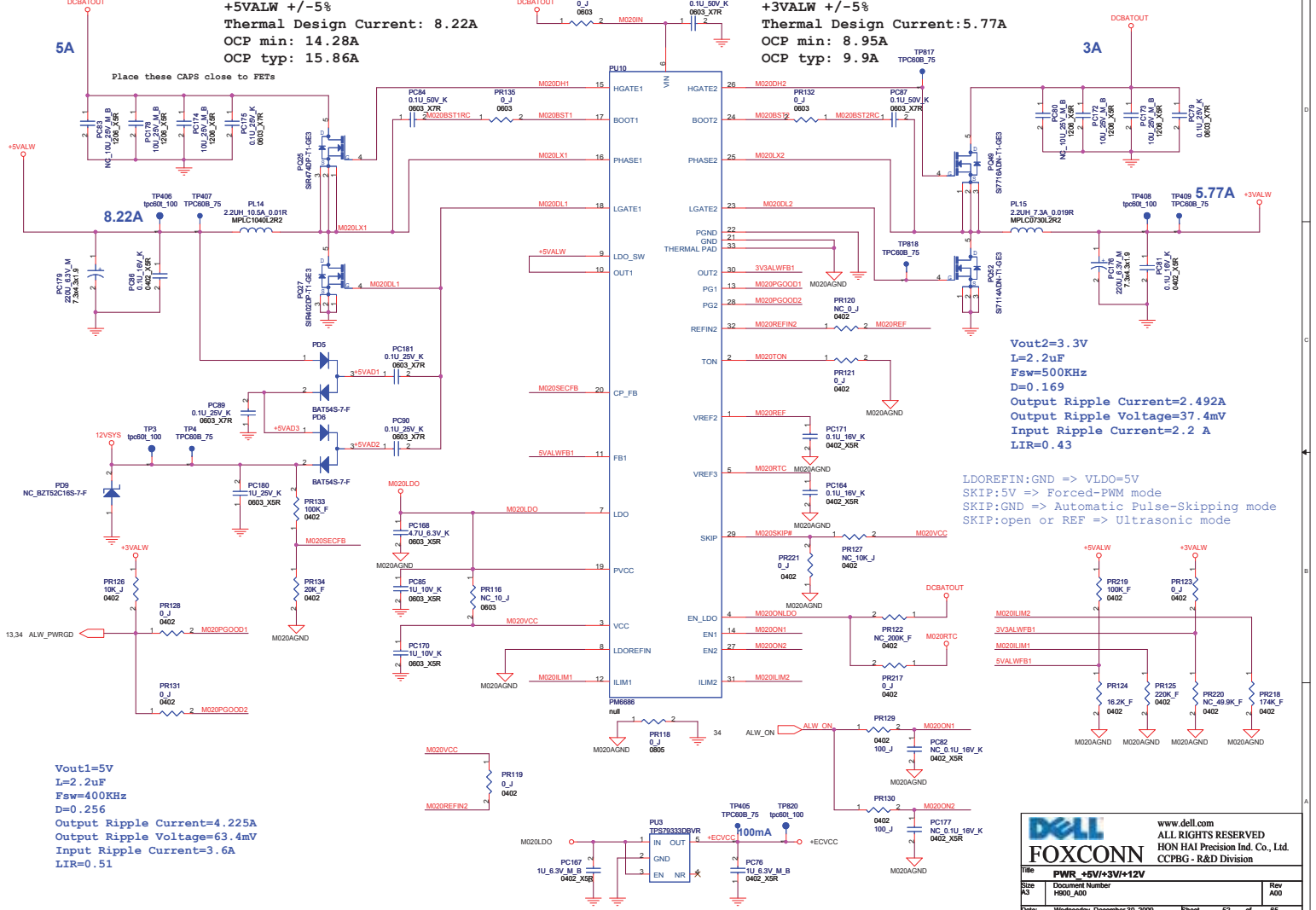
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Title: PWR Power Design Diagram		
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+5VALW +/-5%
Thermal Design Current: 8.22A
OCp min: 14.28A
OCp typ: 15.86A

+3VALW +/-5%
Thermal Design Current: 5.77A
OCp min: 8.95A
OCp typ: 9.9A

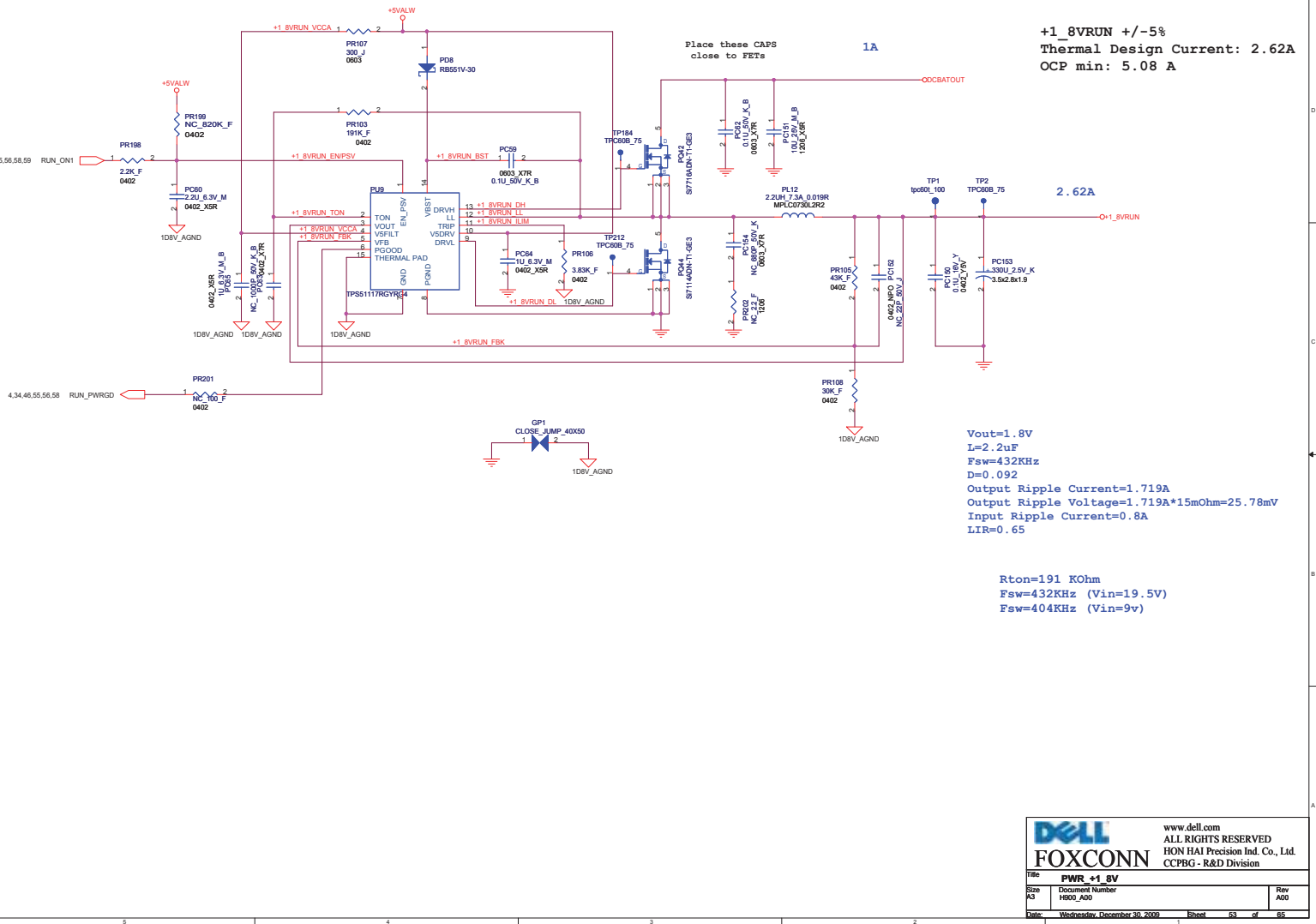


Vout2=3.3V
I=2.2uF
Fsw=500KHz
D=0.169
Output Ripple Current=2.492A
Output Ripple Voltage=37.4mV
Input Ripple Current=2.2 A
LIR=0.43

LDOREFIN:GND => VLDO=5V
 SKIP:5V => Forced-PWM mode
 SKIP:GND => Automatic Pulse-Skipping mode
 SKIP:open or REF => Ultrasonic mode

Vout1=5V
L=2.2uF
Fsw=400KHz
D=0.256
Output Ripple Current=4.225A
Output Ripple Voltage=63.4mV
Input Ripple Current=3.6A
LIR=0.51

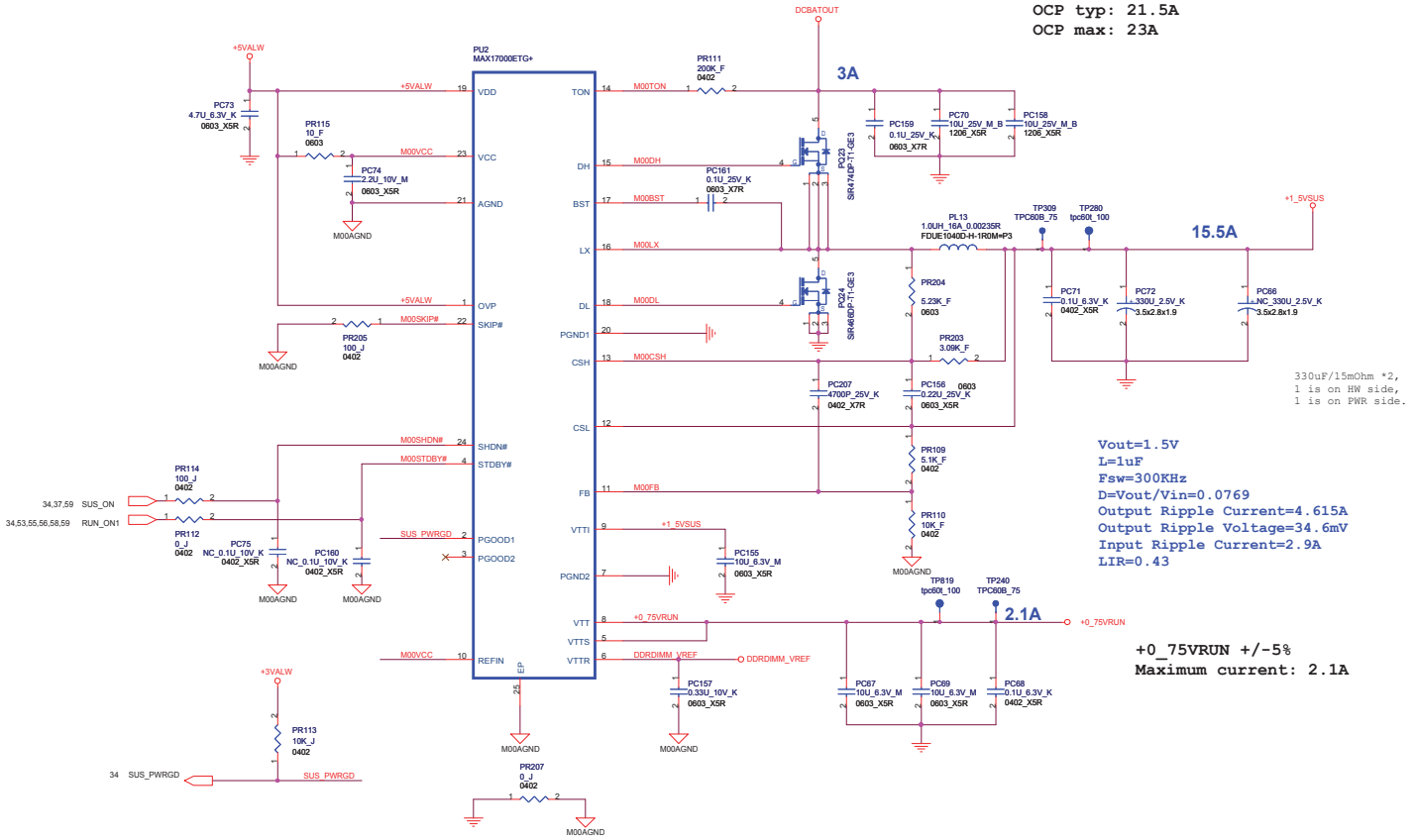
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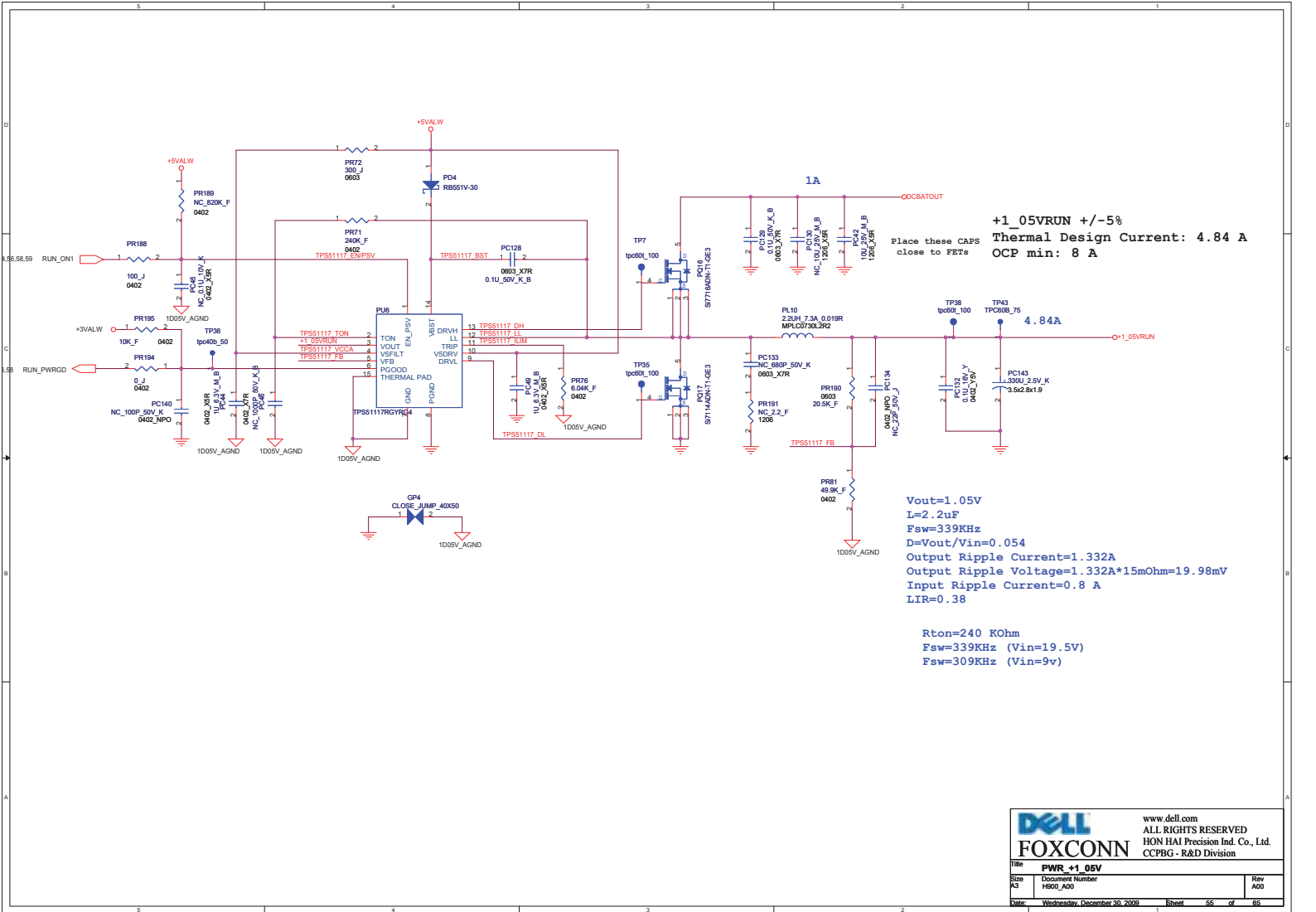
+1_5VSUS +/-5%
 Thermal Design Current: 15.5A
 OCP min: 20.3A
 OCP typ: 21.5A
 OCP max: 23A





Vout=1.5V
 L=1µF
 Fsw=300KHz
 D=Vout/Vin=0.0769
 Output Ripple Current=4.615A
 Output Ripple Voltage=34.6mV
 Input Ripple Current=2.9A
 LIR=0.43

+0_75VRLN +/-5%
 Maximum current: 2.1A

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Title: PWR +1_5V/+0_75V		
Size: A3	Document Number: H800_A00	Rev: A00
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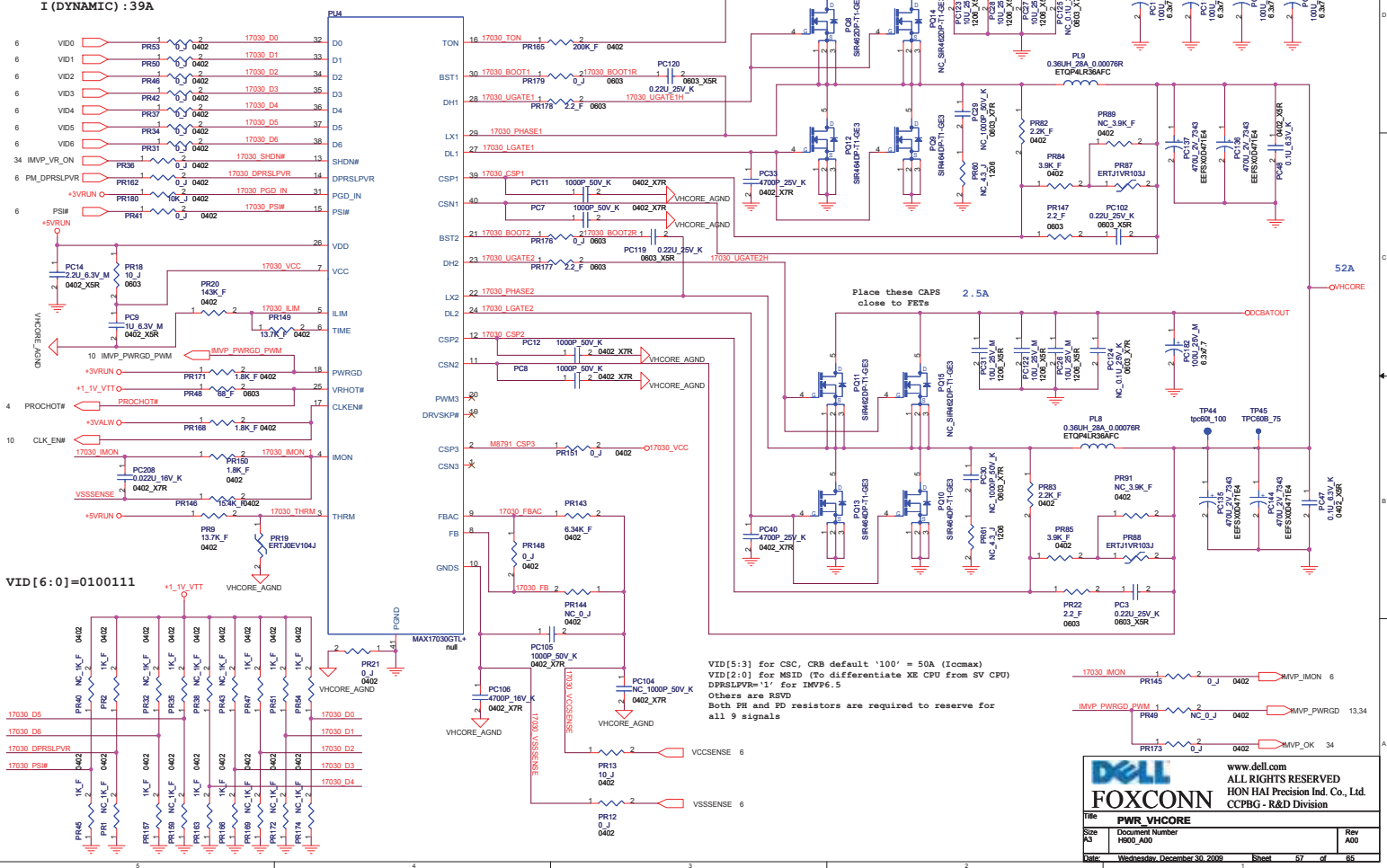
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Clardsfield SV 45W CPU
 V(HFM): 0.95V
 V(LFM): 0.875V
 LL: -1.9mOhm
 I(HFM): 51A
 I(TDC): 38A
 I(DYNAMIC): 39A

OCP setting: 61.7A (30.83A per phase).
 PR649=13.7K Ohm
 OCPmax: 65.6A
 OCPmin: 58.2A

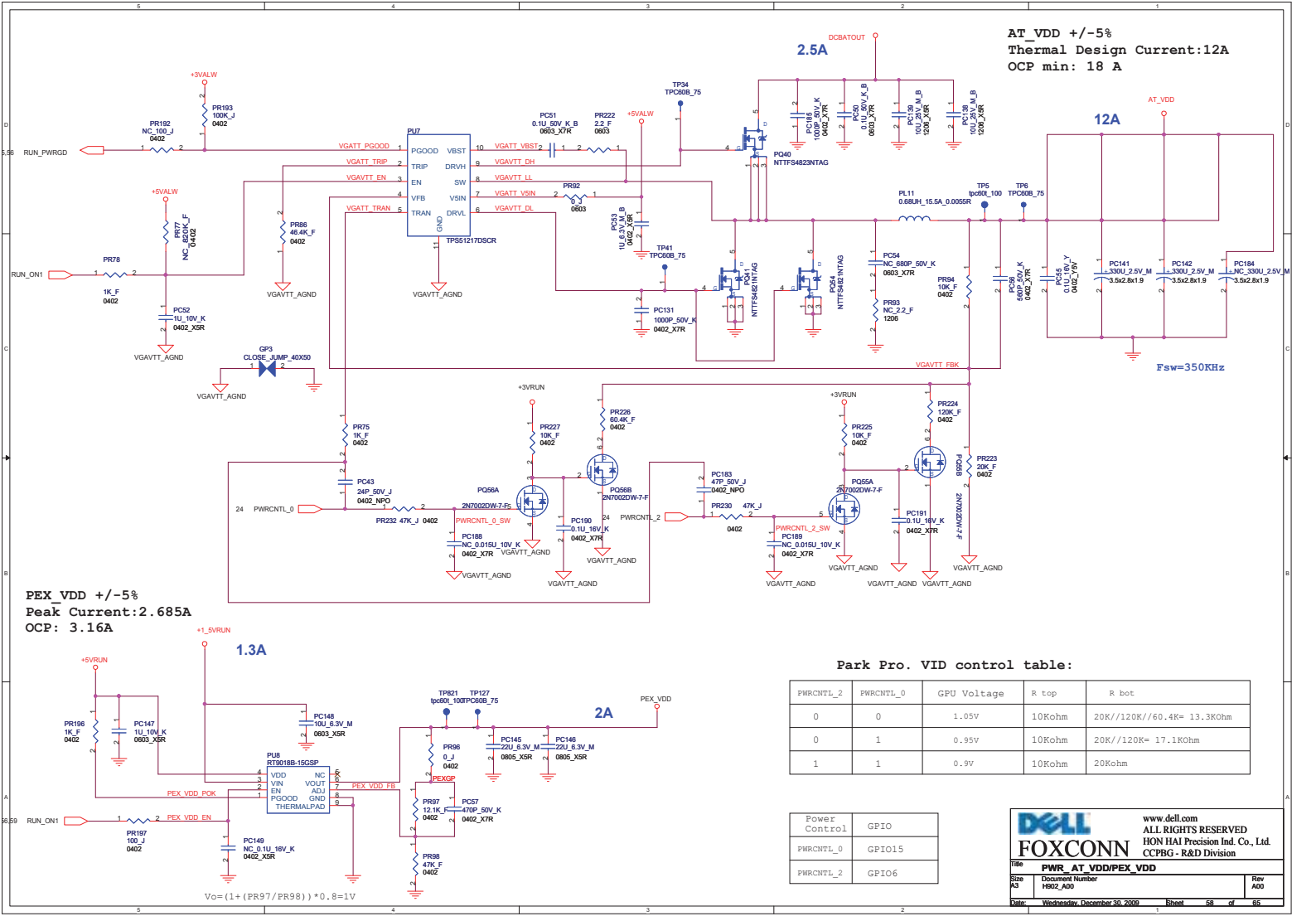


VID[5:3] for CSC, CRB default '100' = 50A (Iccmax)
 VID[2:0] for MSD (To differentiate XE CPU from SV CPU)
 DPRSLPWR='1' for IMVP6.5
 Others are RSVD
 Both PH and PD resistors are required to reserve for all 9 signals

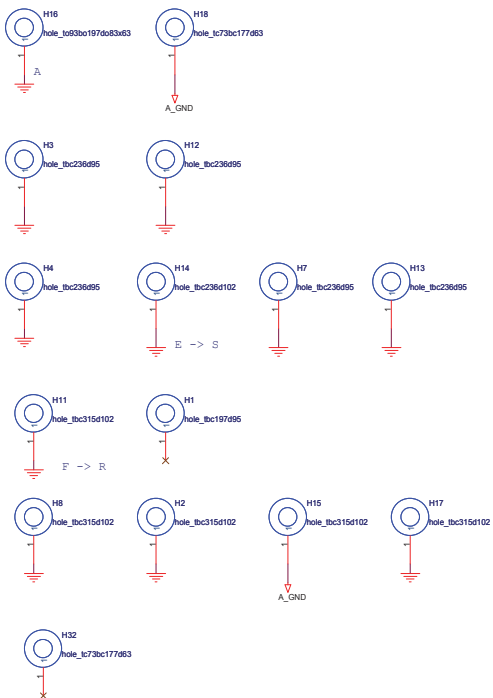
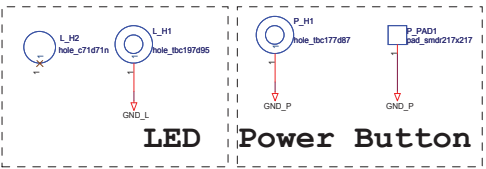
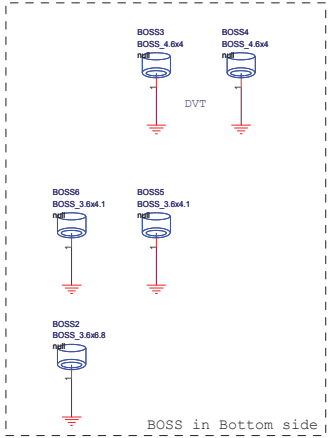
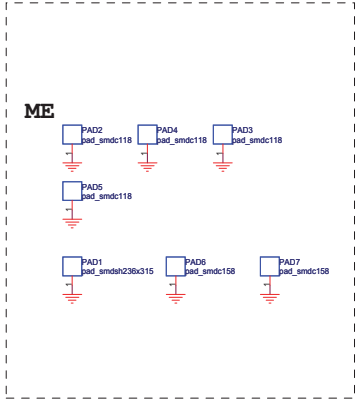
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H902 DVT

(2009/09/25)

- P.25 Change R139 & R143 from 100 ohm to 40.2 ohm for AMD recommend.
- P.24 Change AT_MEM ID0-3 connect to DVDDATA_0-3.
- P.26 Reserve R627 & R629 for reduce DPE/F_PLL.
- P.26 Add R630 & R631 to replace Bead L74, L75 and NC C667, C797, C798, C800, C799, C801 for AMD recommend.
- P.25 NC C273, C280, R127, R134 for AMD recommend.


H902 PVT

(2009/11/03)

- P.22-27 Change U26 HHPN to 12-2160774-0002.
- P.17 Change L35, L37, L66, L67 to 1L-DML2201-2M00 for PUR recommend.
- P.20 Change C364 to 1C-2B20104-K301 for PUR recommend.
- P.31 Change C263 to 1C-2B20104-K301 for PUR recommend.
- P.34 Change C457, C732, C502, C489, C703, C476, C486, C503, C718 & C739 to 1C-2B20104-K301 for PUR recommend.
- P.35 Change C319 to 1C-2B20104-K301 for PUR recommend.
- P.37 Change C485 & C488 & C725 to 1C-2B20104-K301 for PUR recommend.
- P.45 Change C68 & C532 to 1C-2B20104-K301 for PUR recommend.
- P.46 Change C69 & C142 to 1C-2B20104-K301 for PUR recommend.
- P.46 Change C194, C195, C430 & C431 to 1C-2B20104-K301 for PUR recommend.

(2009/11/18)

- P.46 Add C445 0.1uF for EMI recommend.
- P.33 Change CN11 for ME recommend.

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H900 EVT -> DVT

(2009/03/26)

- P.47 Add BT2(CSR) BC_BOSS1 NC for reserve.
- P.32 Change LVDS connector pin define switch Pin4 and Pin10. (Pin4 NC, Pin10 +3VRUN)
- P.47 Add BT2(CSR) BC_BOSS1 NC for reserve.

(2009/03/27)

- P.46 Modify WWAN CN5 pin define.
- P.32 LVDS CN, change +3VRUN to pin 4, pin3 to NC prevent DCBATOUT short to +3VRUN.

(2009/03/31)

- P.42 Change R588,R589 to 8.2K ohm for 1.5W speaker.

(2009/04/01)

- P.40 Change R332 to 13.3K for Realtek recommend.
- P.24 Reserve R382, R383, R617 and R293 0 ohm for Park.
- P.24 Reserve L71, C785 1uF, C786 10uF, C787 0.1uF, L70, C782 1uF, C783 10uF, C784 0.1uF for Park.
- P.24 Reserve R619, R620 0 ohm for Park.
- P.27 Add R622 0 ohm for saperate Park schematics.
- P.27 Reserve R618 and R621 0ohm, C512 1uF, C515 10uF, and L72 for Park.

(2009/04/02)

- P.26 Reserve L73, C788 1uF, C789 10uF, C790 0.1uF and R623 0ohm for Park.

(2009/04/03)

- P.27 Reserve R624 150 ohm, R627 0 ohm for Park.
- P.27 Add R625,R626 0 ohm for Park.

(2009/04/06)

- P.11 Stuff R495 for Flash SPI.

(2009/04/10)

- P.11 Change PCH SPI_CS# to SPI_ROM_CS#.
- P.34 Change H_PWRGD to H_CPUPWRGD.

(2009/04/13)

- P.40 Reserve R628 0 ohm for PC beep.
- P.42 Change R45,R47,R49,R50 to bead L76,L77,L78,L79 for EMI request.
- P.24 Change L19 to BLM18BB121SN1D to solve AT_DPLL_PVDD Vpp over spec issue.
- P.32 Change F8 to 467002 (32V-2A_0603) for LVDS VCC protection.
- P.47 Del BC_CN4,BC_CN3,BC_BOSS1,BC_TP1,BC_TP2 for BT2 board is not necessary.
- P.42 Change C767,C763,C762,C749 to 0.01uF; C507 to 0.1uF for speaker pop noise.
- P.32 Del R29 0ohm for no necessary.
- P.36 Del R27 0ohm for no necessary.
- P.45 Change R384, R34, R52 to close gap PGP4,PGP5,PGP6.
- P.45 Change F5,F1 to close gap PGP7,PGP8 for un-necessary.
- P.22 Change R410 0ohm to close gap PGP12.
- P.26 Change R92,R93 0ohm to close gap PGP13,PGP14.
- P.36 Change R391 0ohm to close gap PGP17.

(2009/04/15)

- P.39 Add D15, D16 for solving leakage issue.

(2009/04/23)

- P.4 Del R196 0ohm for no necessary.

(2009/04/24)

- P.4 Add CPU DET# for Dell PC Beep.

(2009/04/27)

- P.4 Change R184 to 1.1K ohm R182 to 3.01K ohm for Intel recommend.

(2009/04/28)

- P.36 Del R27 0 ohm for DVT.
- P.41 Change R602, R611, R608, R610 to 1k ohm for Audio headphone noise.
- P.45 Add F1 and F5 for protection and del PGP7 and PGP8.

(2009/04/30)

- P.6 Del R401, R115 for Vcore power plane.
- P.38 Change TP29, TP46, TP42, TP40, TP39, TP428, TP430 to TPC40B_121.
- P.50 Change TP8, TP11, TP14, TP10, TP9 to TPC60B_121.
- P.44 Change TP412, TP411, TP413 to TPC40T_121.
- P.39 Change TP12, TP15, TP16, TP17, TP18, TP20, TP22, TP23 to TPC40B_121.
- P.42 Change TP186, TP185, TP183, TP187 to TPC40B_121.
- P.34 Change TP480, TP485, TP329, TP479, TP483, TP182, TP333, TP128 to TPC40T_121.
- P.46 Change TP414, TP410 to TPC40T_121 and TP13 to TPC40B_121.
- P.38 Change TP47, TP422, TP417, TP37, TP30, TP33, TP32, TP31, TP28 to TPC40B_121.
- P.11 Change C736 to 15pF for crystal vendor recommend.
- P.39 Change C35 and C38 to 18pF for crystal vendor recommend.
- P.34 Del Q28 and R318 2.2k ohm for CPU PC Beep solution .

(2009/05/5)

- P.32 Change C65 to 6800pF for LVDS sequence.
- P.39 Reserve R318 and R384 0 ohm for leakage solution.
- P.45 Change F1 and F5 to 1M-F08V05A-0000.

(2009/05/8)



- P.16 Reserve R391 1K ohm for following the CRB.
- P.7 Del R55 0 ohm for leakage.
- P.35 Change U13 to W25X80A.
- P.31 Change L61, L62, L63 to 33R100MHz for CRT SI issue.

(2009/05/11)

- P.17 Change C479 to 1uF for Intel recommend.
- P.24 Reserve R410 and R629 0 ohm for Park.
- P.24 Reserve R634, R631, R632, and R633 0 ohm for Park.
- P.24 Del R619 and R620 0 ohm for Park NC.
- P.25 Change C781 to 1nF for AMD recommend.
- P.25 Reserve R630 680 ohm and R115 10K PD for Park.
- P.27 Reserve R635 0 ohm for Park.
- P.25 Add TP172, TP173, TP174, TP175, TP176 and TP177 for Layout request.
- P.60 Change BOSS3 and BOSS4 for ME request.
- P.17 Del C445 and C463 33pF for unused.
- P.36 Del R27 0 hom for unused.
- P.45 Del F1, F5, and R31 0 ohm for unused.
- P.46 Del F2 for unused.

(2009/05/12)

- P.46 Reserve R637 and R638 0 ohm for WWAN change.
- P.46 Add R636 0 ohm for WWAN change.
- P.13 Add R92 and R93 1k ohm for Intel recommend.

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H900 EVT -> DVT

(2009/05/13)

P.25 Add R196 0 ohm and change R630 68 ohm to DRAM_RST pin for AMD recommend.

(2009/05/14)

P.12 Add R620 0 ohm to GND in Xtal_in for Intel recommend.
P.7 Del R407, R399, and R405 0 ohm for 1.1VTT power plane.

(2009/05/20)

P.4 Change R173 to NC for un-used.
P.27 Change C208 from 0.22u 10V to 0.22u 16V for derating issue.
P.17 Stuff R268 0 ohm to GND for disable Intel internal LAN.

(2009/05/22)

P.17 Change R237 and R265 from 0603 to 0805 for derating.
P.27 Change R146 from 0805 to 1206 for derating.

(2009/05/25)

P.17 Change CAP5 and CAP6 from 35m ohm ESR to 45m ohm ESR.

(2009/06/06)

P.39 Add Q58, Q59, R619, and R639 10K ohm and del D15 & D16 for leakage issue.
P.6 Add R401 0 ohm and Add R399, R405, R407, R640 1K ohm NC for C-state debugging.

(2009/06/16)

P.6 Add R641 & R642 0 ohm for controlling LAN_CLK_REQ# turn on voltage.
P.34 Add R643 & R644 0 ohm for debugging white screen issue.

(2009/06/25)

P.11 Change RTC battery P/N from 1M-BCR2032-LB00 to 1M-BCR2032-LB01.

(2009/07/01)

P.60 Add H32 for ME request.

(2009/07/14)

P.12 Add R645 & R646 2.2K ohm for SMBUS PH.

(2009/07/20)

P.38 Change C33 and C44 from NPO 10% to 5% for PUR recommend.
P.47 Change P_C1, P_C2, L_C1, L_C2 from 10pF NPO 10% to 5% for PUR recommend.
P.40 Change C499 and C505 from 12pF NPO 10% to 5% for PUR recommend.
P.11 Change C735 from 12pF NPO 10% to 5% for PUR recommend.
P.38 Change C78 and C79 from 15pF NPO 10% to 5% for PUR recommend.
P.11 Change C736 from 15pF NPO 10% to 5% for PUR recommend.
P.46 Change C244 and C245 from 47pF NPO 10% to 5% for PUR recommend.
P.39 Add C445 0.1uF for Hipot test.
P.27 Delete R146 0ohm for derating.
P.18 Delete R257 0ohm for derating.
P.17 Delete R237 0ohm for derating.

(2009/07/22)

P.17 Change C208 0.22uF from 16V to 25V for derating.
P.39 Add C791, C794 1000pF and C795, C796 0.047uF for EMI request.
P.12 Change R303 & R331 from 4.7K to 2.2K ohm NC.

H900 DVT -> PVT

(2009/07/24)

P.34 Add Q28 and NC C478 0.1uF for Sys_shdn#.
P.44 Change R467 from 33K to 10K ohm & R472 from 15K to 6.8Kohm for thermal setting.
P.39 NC C26 0.1uF, R14 1K ohm and U2 24C08.
Add R612 1K ohm for disable external EEPROM.
P.44 Add C463 100p NC for Thermal sensor vendor recommend.

(2009/07/28)

P.9 Change R51 & R53 from NC to introduce.
P.33 Change HDMI connector from 2N-0019003-FKGO to 2N-0019002-MKGO

H900 PVT -> X-Build

(2009/08/03)

P.31 Change L61, L62, and L63 from 33R to 47R for CRT debug.
P.33 Change D5 location to D9 for Safety recommend.
P.11 Change D9 location to D5 for Safety recommend.
P.11 Change R340 & R341 location to R427 & R426 for Safety recommend.
P.24 Change R426 location to R341 for Safety recommend.
P.45 Change R427 location to R340 for Safety recommend.
P.32 Change U5 location to U4 for Safety recommend.
P.10 Change U37 location to U40 for Safety recommend.
P.45 Change U4 & U40 location to U5 & U37 for Safety recommend.
P.4 Change U17 from 14-MC74VHC-1G04 to 14-74AHC1G-1400 for L6 recommend.

(2009/08/07)

P.31 Change C646 & C640 from 47p to 22p.

(2009/08/20)

P.30 Change L1 to LanKom 1T-1LG2425-P100.
P.20 Change R61 to NC for DDR Intel recommend.
P.21 Change R66 to NC for DDR Intel recommend.

(2009/08/22)



P.20 & 21 Del R146 & R237 for customer recommend.
P.20 Reserve R23 & R27 1K ohm for intel DDR3 M1 solution.
P.21 Reserve R29 & R31 1K ohm for intel DDR3 M1 solution.

(2009/08/24)

P.24 Add R636 0 ohm for EMI recommend.
P.24 Add Cap7 330 uF for debugging WLAN issue.


(2009/08/25)

P.44 Add R637, R638, R645 & R646 0 ohm for Intel recommend.

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1	2009/04/10	P.55	+1_05VRUN	1.05V Vripple over spec.	Change PC143 from 220uF 2.5V 35m Ohm(1C-31R0227-MX00) to 330uF 2.5V 15m Ohm(1C-33U0337-KX00).	X01
2	2009/04/13	P.51	Charger	Change PR152 for ADAPT OC function.	Change PR152 from 8.45K 0402 1%(1R-0008451-F200) to 10K 0402 1%(1R-0000103-F200)	X01
3	2009/05/06	P.57	VCORE	Fine tune VCORE setting for loadline, transition and mosfet ring issue.	Add PC7 :470pF 50V X7R 0402(1C-2B20471-K000) Add PC106 :4700pF 16V X7R 0402(1C-2B20472-K002) Add PC29 and PC30 :1000pF 50V X7R(1C-2B3012-MX00) Add PR60 and PR61 :4.3 Ohm 1206 5%(1R-000043X-J600) Del PQ14 and PQ15 SiR462DP-T1-GE3 (17-S1R462D-PT00) Change PR12 from 10 Ohm 0402 5%(1R-0000100-J200) to 0 Ohm 0402 5%(1R-0000000-J200) Change PR143 from 7.15K Ohm 0402 1%(1R-0007151-F200) to 6.34K Ohm 0402 1%(1R-0006341-F200) Change PR82 and PR83 from 2.7K Ohm 0402 1%(1R-0000272-F200) to 2.2K Ohm 0402 1%(1R-0000222-F200) Change PR84 and PR85 from 4.02K Ohm 0402 1%(1R-0004021-F200) to 1.69K Ohm 0402 1%(1R-0001691-F200)	X01
4	2009/05/06	P.58	AT_VDD	Changing H-S,L-S Mosfets and boost resistor for solving ring issue.	Change PQ40 from Si7716ADN(17-S17716A-DN00) to AON7402L(17-AON7402-L000) Change PQ41 from Si7114ADN(17-S17114A-DN00) to AON7700(17-AON7700-0000) Change PR222 from 0 Ohm 0603 1%(1R-0000000-J300) to 1 Ohm 0603 1%(1R-000010X-F300)	X01
5	2009/05/07	P.54	+1_5VSUS	Modifying OCP setting for +1_5VSUS.	Change PR204 from 4.87K 0603 1%(1R-0004871-F300) to 5.23K 0603 1%(1R-0005231-F300) Change PR203 from 3.24K 0603 1%(1R-0003241-F300) to 3.09K 0603 1%(1R-0003091-F300)	X01
6	2009/05/11	P.56	+1_1V_VTT	Change remote sense detection from CPU to output Cap.	Add PR184 10 Ohm 0402 1%(1R-0000100-F200) Delete PR183 0 Ohm 0402 5%(1R-0000000-J200)	X01
7	2009/05/12	P.50	PSID	Change PQ4 to high ESD protection (6000KV).	Change PQ4 from 2N7002K(17-2N7002K-0001) to FDV301N(17-FDV301N-0000).	X01
8	2009/05/12	P.55 P.56	+1_05VRUN +1_1V_VTT	Change RUN_PWRGD singal from +1_1V_VTT rail to +1_05VRUN rail.	Delete PR70 100 Ohm 0402 1%(1R-0000101-F200) Add PR195 10 Kohm 0402 1%(1R-0000103-F200) Add PR194 0 Ohm 0402 5%(1R-0000000-J200)	X01
9	2009/05/13	P.57	VCORE	PROCHOT# signal pull-up resistor is 56 ohm in IMVP side.	Change PR48 from 56 Ohm 0603 1%(1R-0000560-J300) to 68 Ohm 0603 1%(1R-0000680-F300)	X01
10	2009/05/20	P.58	PEX_VDD	Modify feedback capacitor for improving loop response.	Change PC57 from 0.01uF 0402 25V X7R(1C-2B20103-M000) to 470pF 0402 50V X7R(1C-2B20471-K000)	X01
11	2009/05/20	P.51	DC_IN	Modify resistor and capacitor for reducing adapeter's inrush current.	Change PR28 from 47KOhm 0402 5%(1R-0000473-J200) to 100KOhm 0402 5%(1R-0000104-J200) Change PC6 from 0.1uF 0603 50V(1C-2B30104-K000) to 0.22uF 0603 25V X5R(1C-2B30224-K400)	X01
12	2009/05/26	P.54	+1_5VSUS	Add a capacitor between CSH and FB for improving jitter issue.	Add PC207 4700pF 25V 0402 X7R 10%(1C-2B20472-K001)	X01

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13	2009/06/18	P.57	V_CORE	Change GND design for C-state issue	Change PR21.1 to PGND. Change PR21.2 to AGND. Change PC14.2 to PGND.	X02
14	2009/07/02	P.57	V_CORE	Change boost resistor to reduce ring of Mosfet. Add feedback capacitor to reduce ground noise.	Change PR178 from 0 Ohm 0603 5% (1R-0000000-J300) to 2.2 Ohm 0603 1% (1R-000022X-F300) Change PR177 from 0 Ohm 0603 5% (1R-0000000-J300) to 2.2 Ohm 0603 1% (1R-000022X-F300) Add PC7: 1000pF 16V X7R (1C-2B20102-K001) . Add PC8: 1000pF 16V X7R (1C-2B20102-K001) . Add PC11: 1000pF 16V X7R (1C-2B20102-K001) . Add PC12: 1000pF 16V X7R (1C-2B20102-K001) .	X02
15	2009/07/06	P.51	Charger	Change rating voltage from 25V to 50V and size from 0603 to 0805 for Capacitor(PC6).	Change PC6 from 0.22uF 25V X5R 0603 10% (1C-2B30224-K400) to 0.22uF 50V X5R 0805 10% (1C-2B70224-K600)	
16	2009/07/10	P.57	V_CORE	Modify DCR feedback and IMON setting.	Change PR84 and PR85 from 1.69K 0402 1% (1R-000169I-F200) to 3.9K 0402 1% (1R-000390I-F200) Change PR150 from 10K 0402 1% (1R-0000103-F200) to 1.8K 0402 1% (1R-0000182-F200) Change PC208 from 0.1uF 6.3V 0402 (1C-2B20104-K101) to 0.022uF 16V 0402 X7R (1C-2B20223-K000) Change PR146 from 12K 0402 1% (1R-0000123-F200) to 15.4K 0402 1% (1R-0001542-F200)	X02
17	2009/07/20	P.59	Other power plane	Add discharge path for 1_5VRUN and 1_05VRUN	Add PR104:330 Ohm 0603 5% (1R-0000331-J300) Add PR95:330 Ohm 0603 5% (1R-0000331-J300) Add FQ21:2N7002-7-F SOT-23 (17-2N70027-F000) Add FQ18:2N7002-7-F SOT-23 (17-2N70027-F000)	X02
18	2009/07/24	P.57	V_CORE	Add AL capacitor to reduce acoustic noise.	Add PC113:EEEFK1E101XP,100uF,25V,20%, 6.3*7.7,0.34ohm (1C-1XX0107-M400) Add PC182:EEEFK1E101XP,100uF,25V,20%, 6.3*7.7,0.34ohm (1C-1XX0107-M400)	X02
19	2009/09/25	P.58	VGA_CORE	Add more GPIO pin for VAG 4 level controller	Add NC_PC187,NC_PC188,NC_PC189 PR230,PR231,PR232, 0ohm Remove PR79, PR80	X02
20	2009/09/25	P.58	VGA_CORE	Change AOS MOS to ON MOS for reducing risk of induce voltage	Change PQ40 PQ41 and PQ54 to ON MOS 4823 and 4821.	
21	2009/11/19	P.58	VGA_CORE	EMI request add one cap	Add PC185 1000pF	
22	2009/11/19	P.58	VGA_CORE	Reduce inductor current when VID change	change PR230, PR232, from 0 to 47K. change PC188, PC189, from 0.047uF to 0.015uF. PC56 from 22pF to 560pF NC_PC131, PC141, PC142, from 330uF 15mohm to 330uF 9mohm. Add NC_PC190,NC_PC191 change PR86, to 46.4K for OCP 15A	
23	2009/11/19	P.58	VGA_CORE	TI suggest reducing short through risk	change PR222, from 1 ohm to 2.2 ohm	
24	2009/11/19	P.58	VGA_CORE	Remove unused GPIO pin	Remove PQ57,PD10,PR228,PR229	
24	2009/11/27	P.58	VGA_CORE	R C delay as Dell request	NC_PC188, PC_PC189 and add PC190, PC191 0.1uF	

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