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Project Code & Schematics Subject: H902 Main Board 8L

PCB P/N:	1P-009CJ00-8000 (IRIS)
	1P-009C500-8000 (HANNSTAR)
	1P-009C200-8000 (NANYA)
BT DB P/N:	1P-1098J01-8000 (IRIS)
	1P-1098501-8000 (HANNSTAR)
	1P-1098201-8000 (NANYA)
LED DB P/N:	1P-1098J00-8000 (IRIS)
	1P-1098500-8000 (HANNSTAR)
	1P-1098200-8000 (NANYA)
P/B DB P/N:	1P-1098J02-8000 (IRIS)
	1P-1098502-8000 (HANNSTAR)
	1P-1098202-8000 (NANYA)

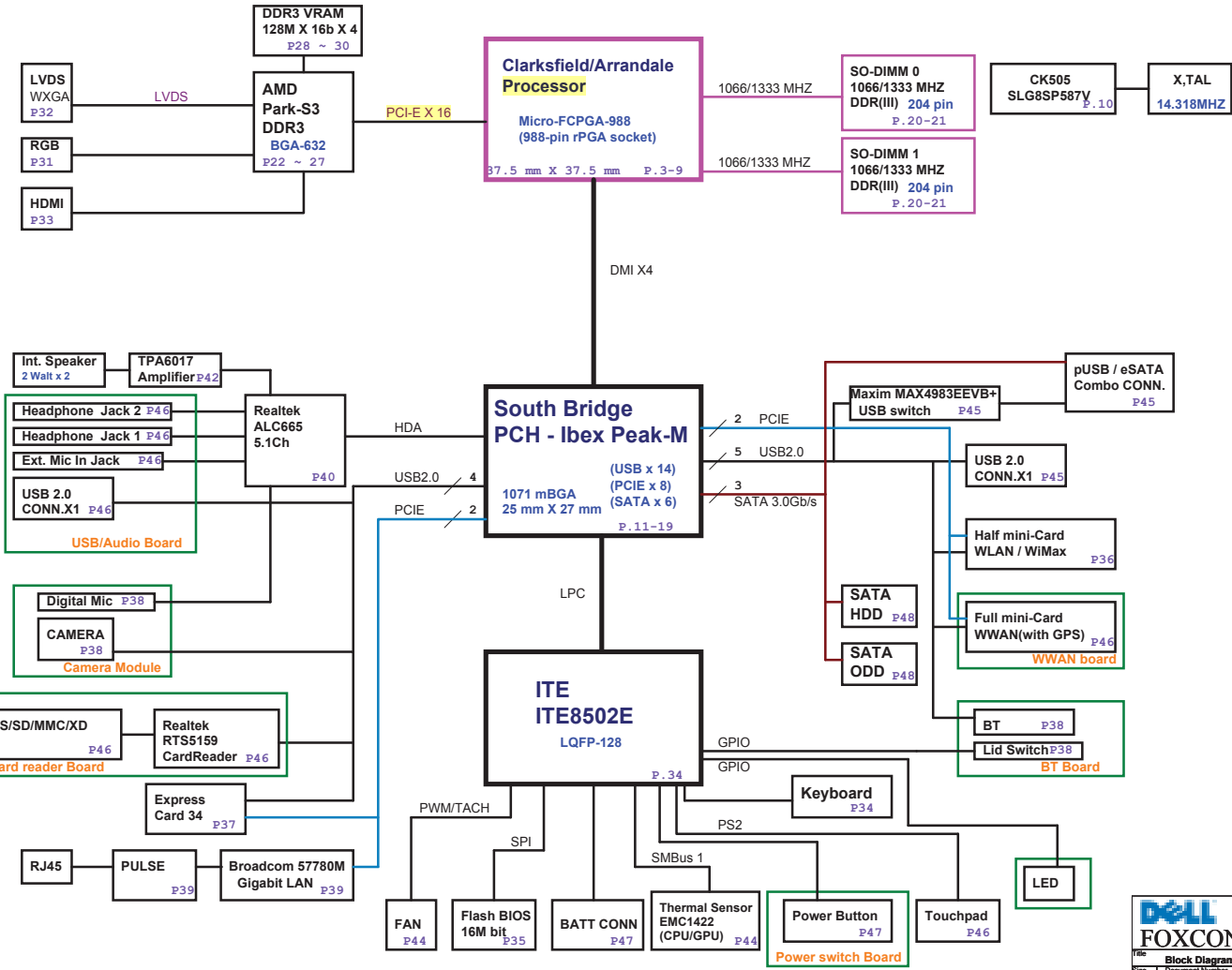
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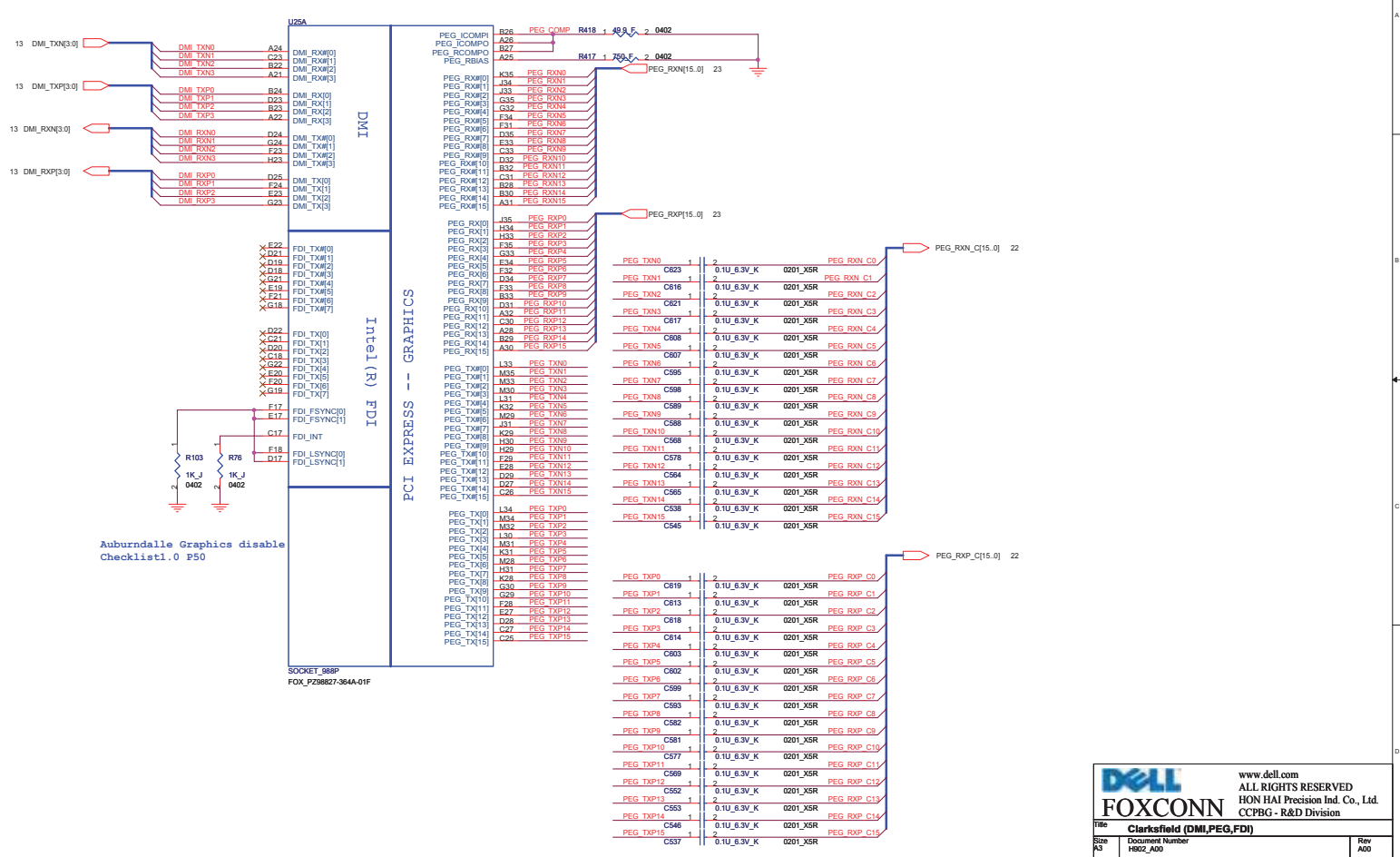
H902 Calpella + Discrete VGA



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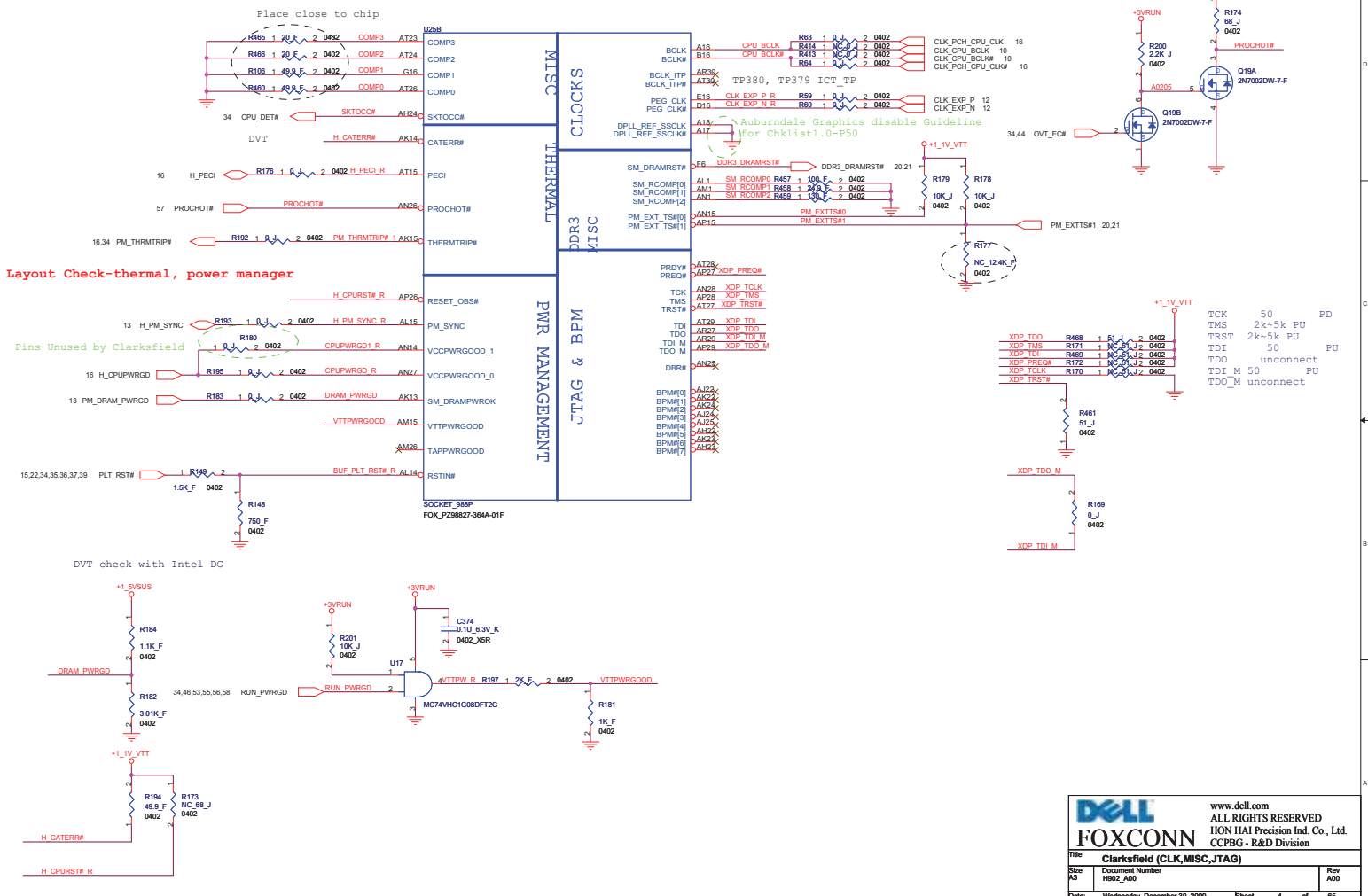
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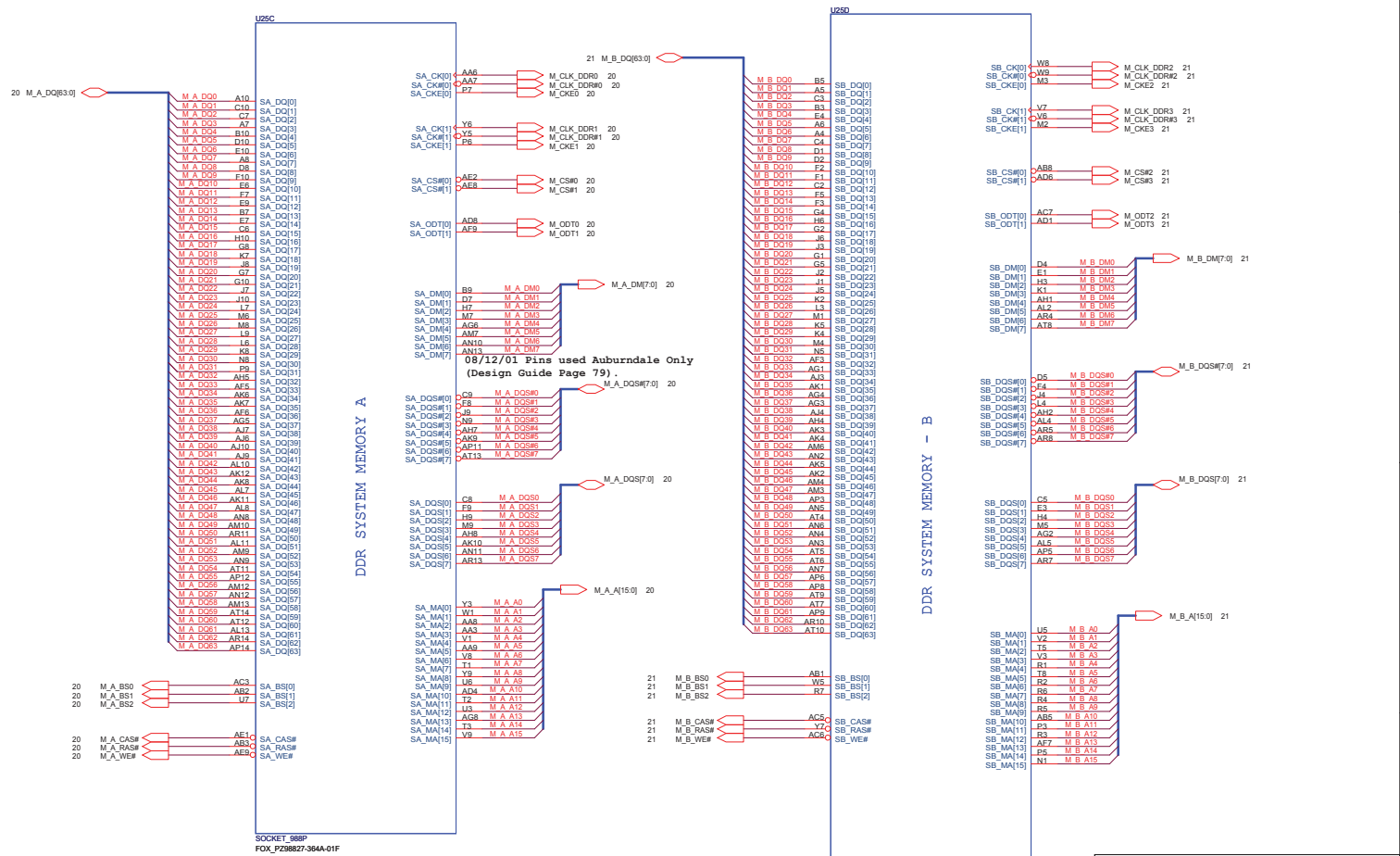
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Clarksfield (DMI,PEG,FDI)			
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Layout Note:
 Comp0,2 connect with Zo=27.4 ohm, make trace length shorter than 0.5". Width=20mil (MS)
 Comp1,3 connect with Zo=5 ohm, make trace length shorter than 0.5". Width=5mil (MS)



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		Clarkfield (CLK,MISC,JTAG)	
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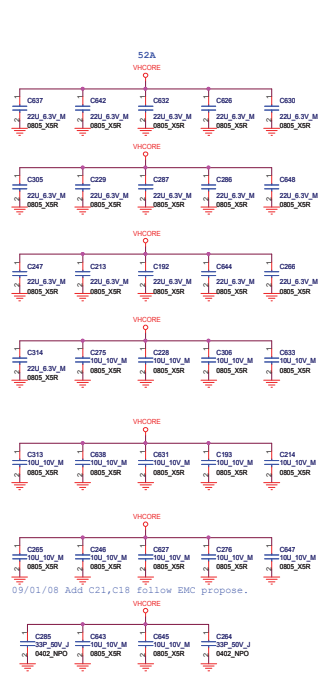
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Clarksfield (DDR3)

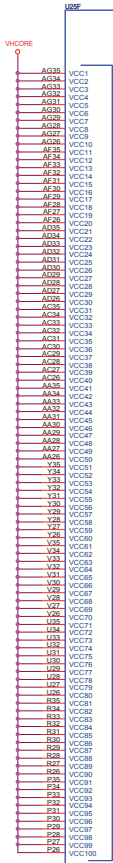
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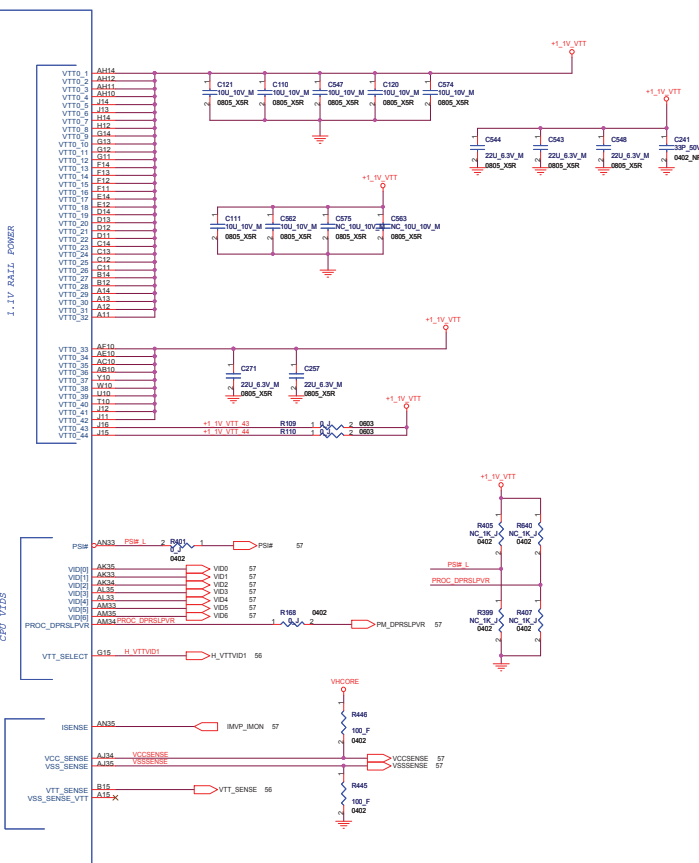


09/01/08 Add C21,C18 follow EMC propose.



POWER

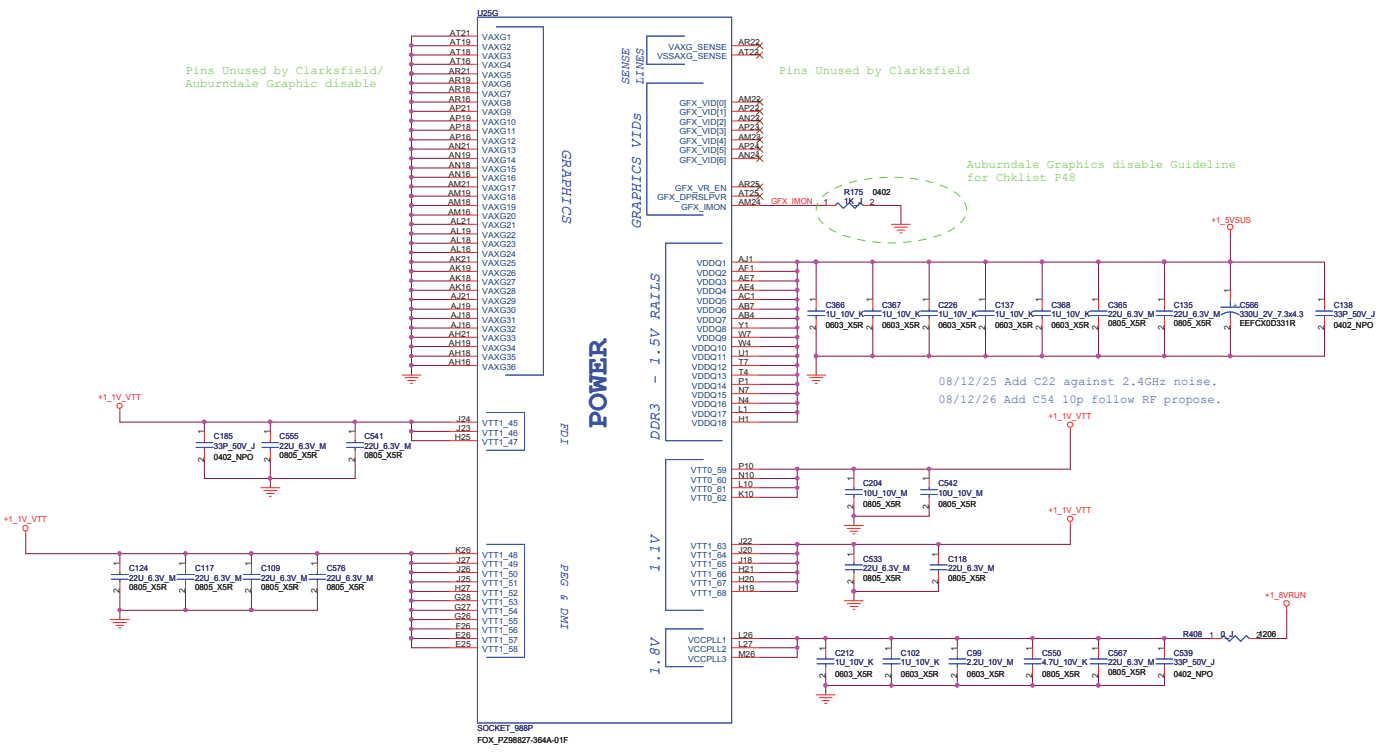
SENSE LINE



SOCKET_99P
FOX_P22827-364A-01P

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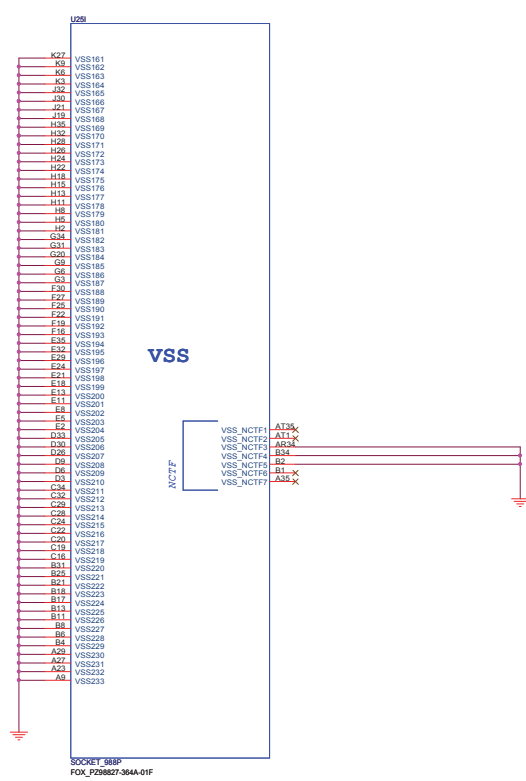
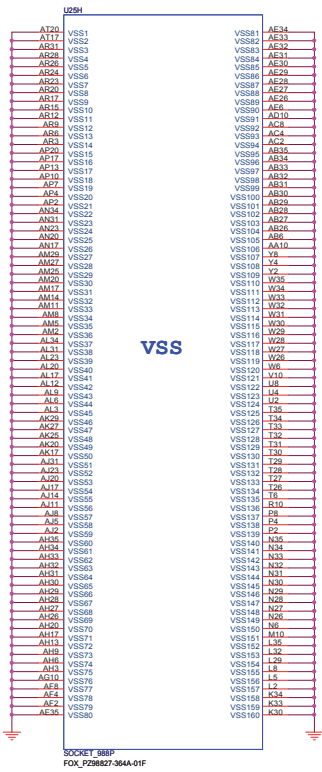
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Clarksfield (GRAPHIC POWER)

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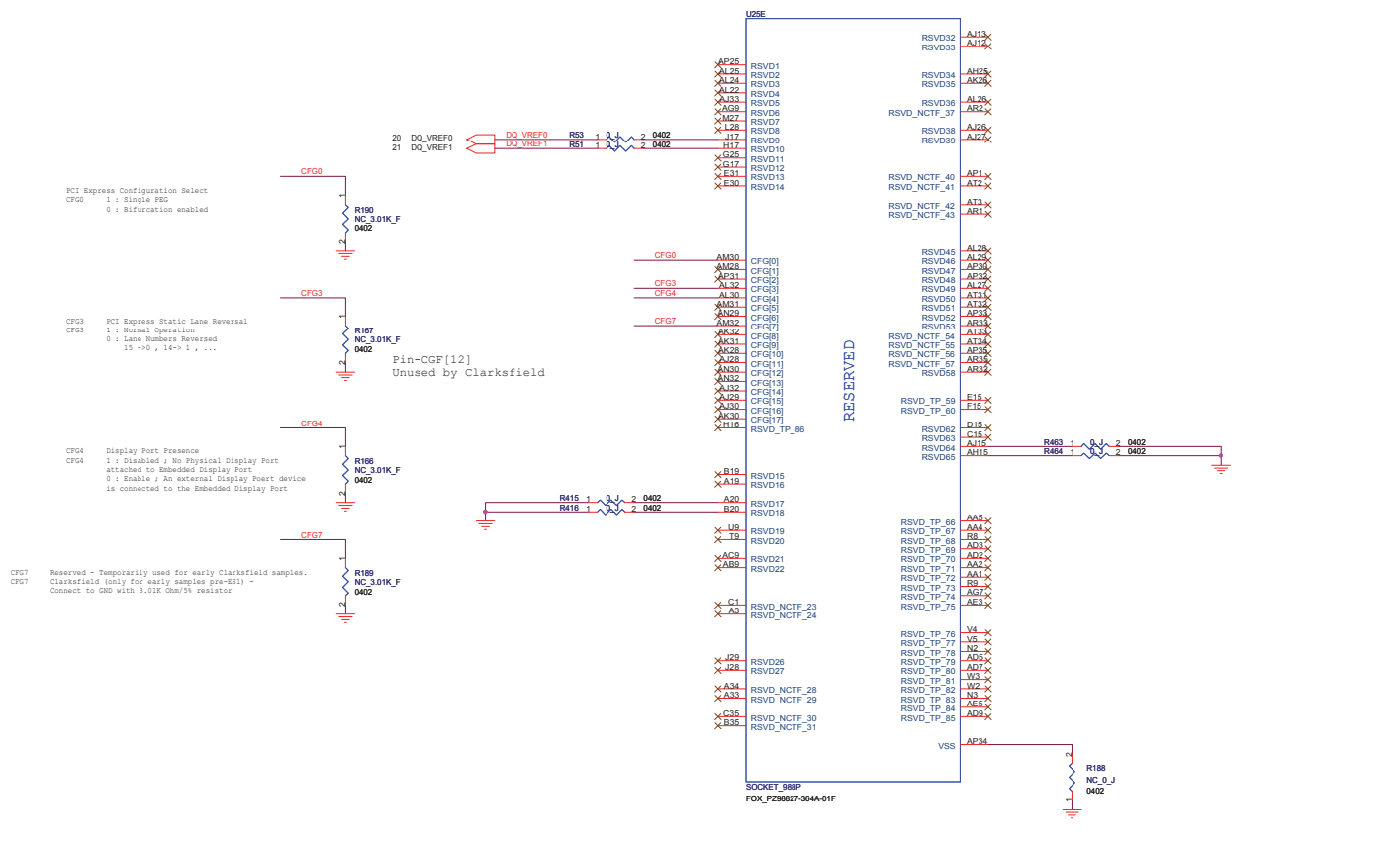


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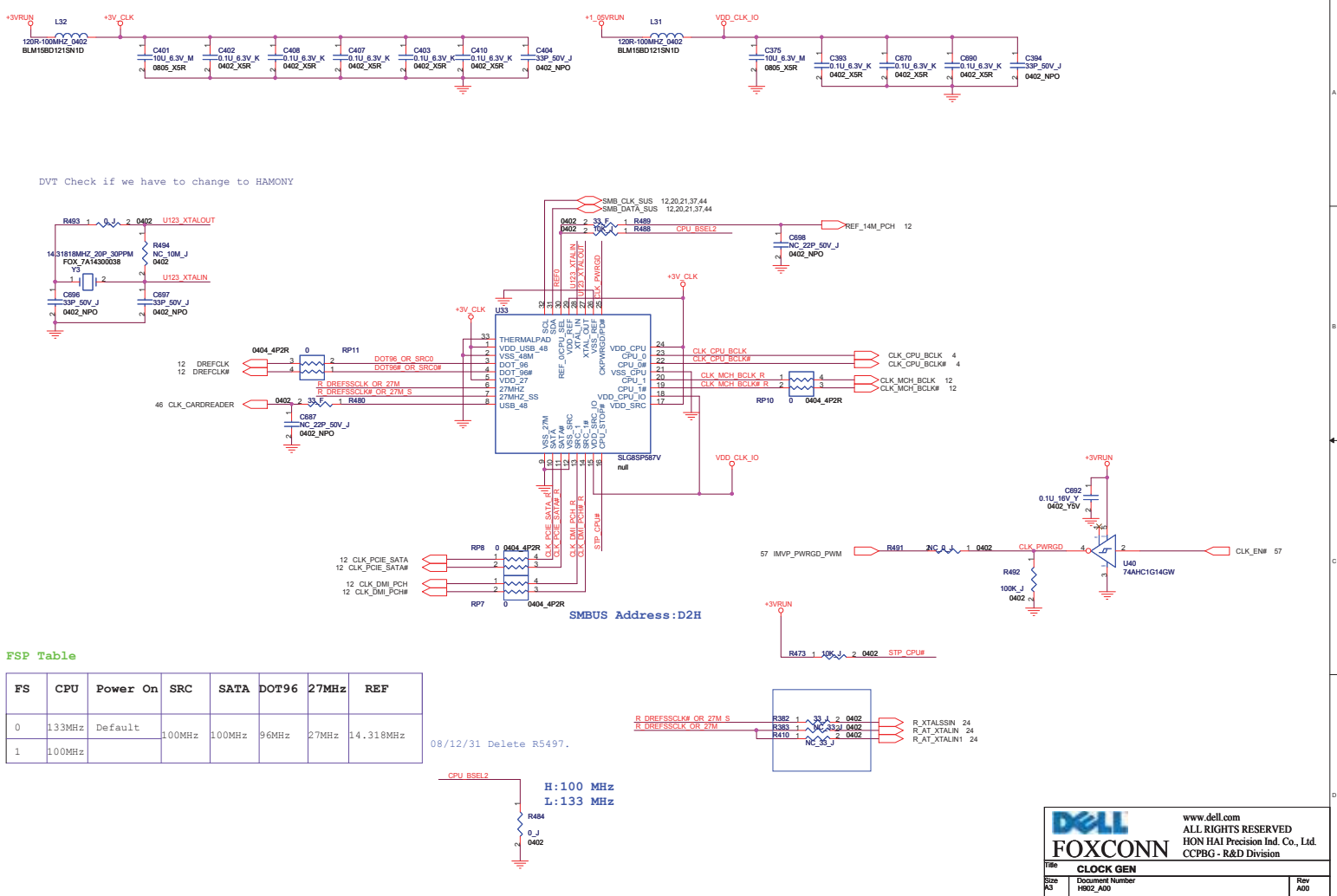
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Clarksfield (RESERVED)

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DVT Check if we have to change to HAMONY

SMBUS Address:D2H

FSP Table

FS	CPU	Power On	SRC	SATA	DOT96	27MHz	REF
0	133MHz	Default	100MHz	100MHz	96MHz	27MHz	14.318MHz
1	100MHz						

08/12/31 Delete R5497.



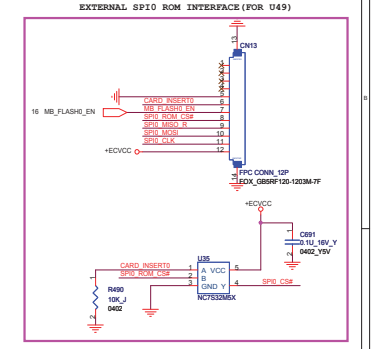
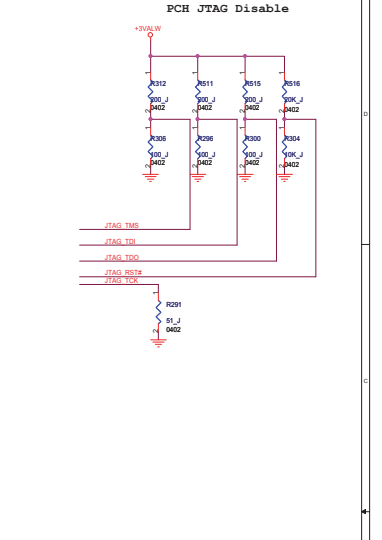
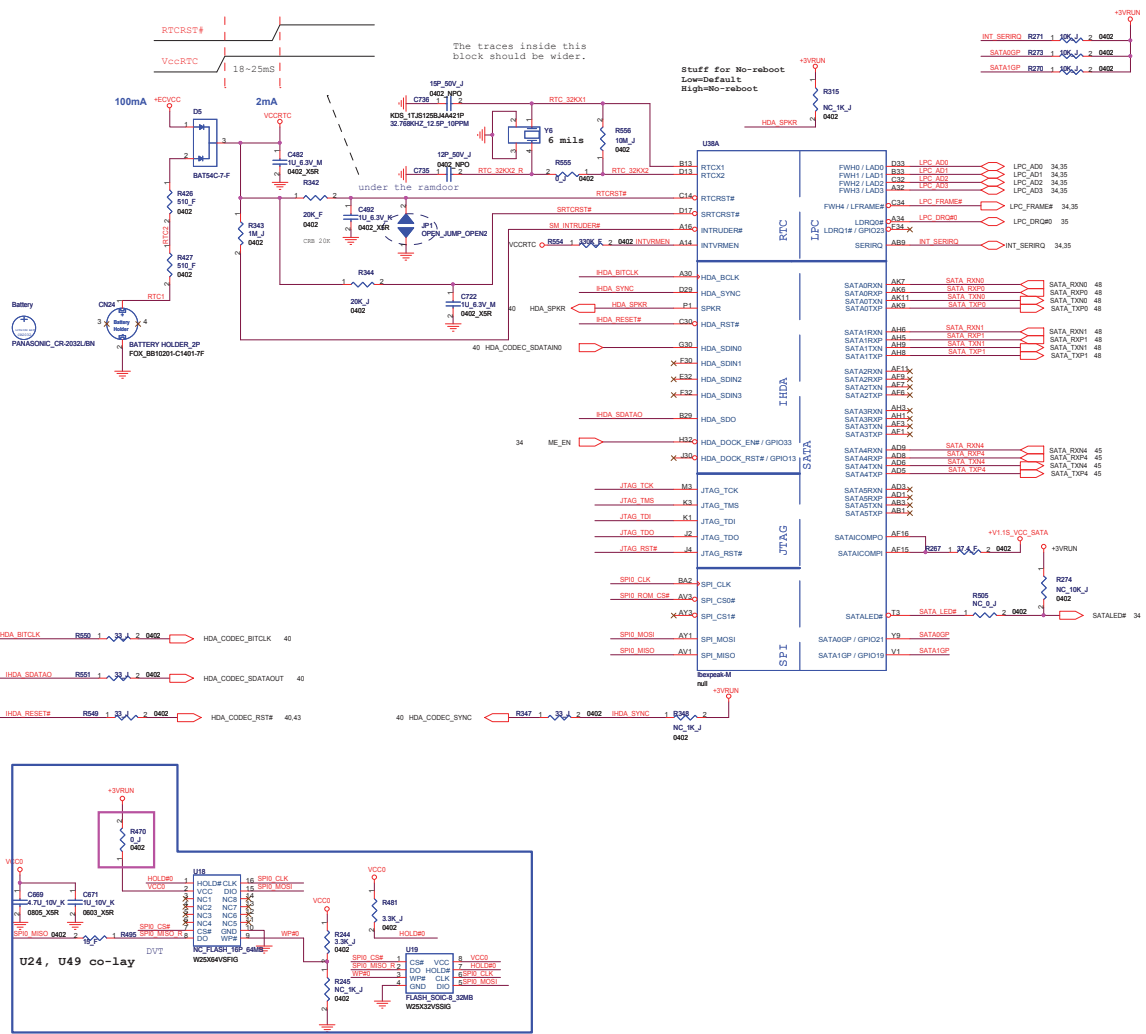
H:100 MHz
L:133 MHz

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CLOCK GEN

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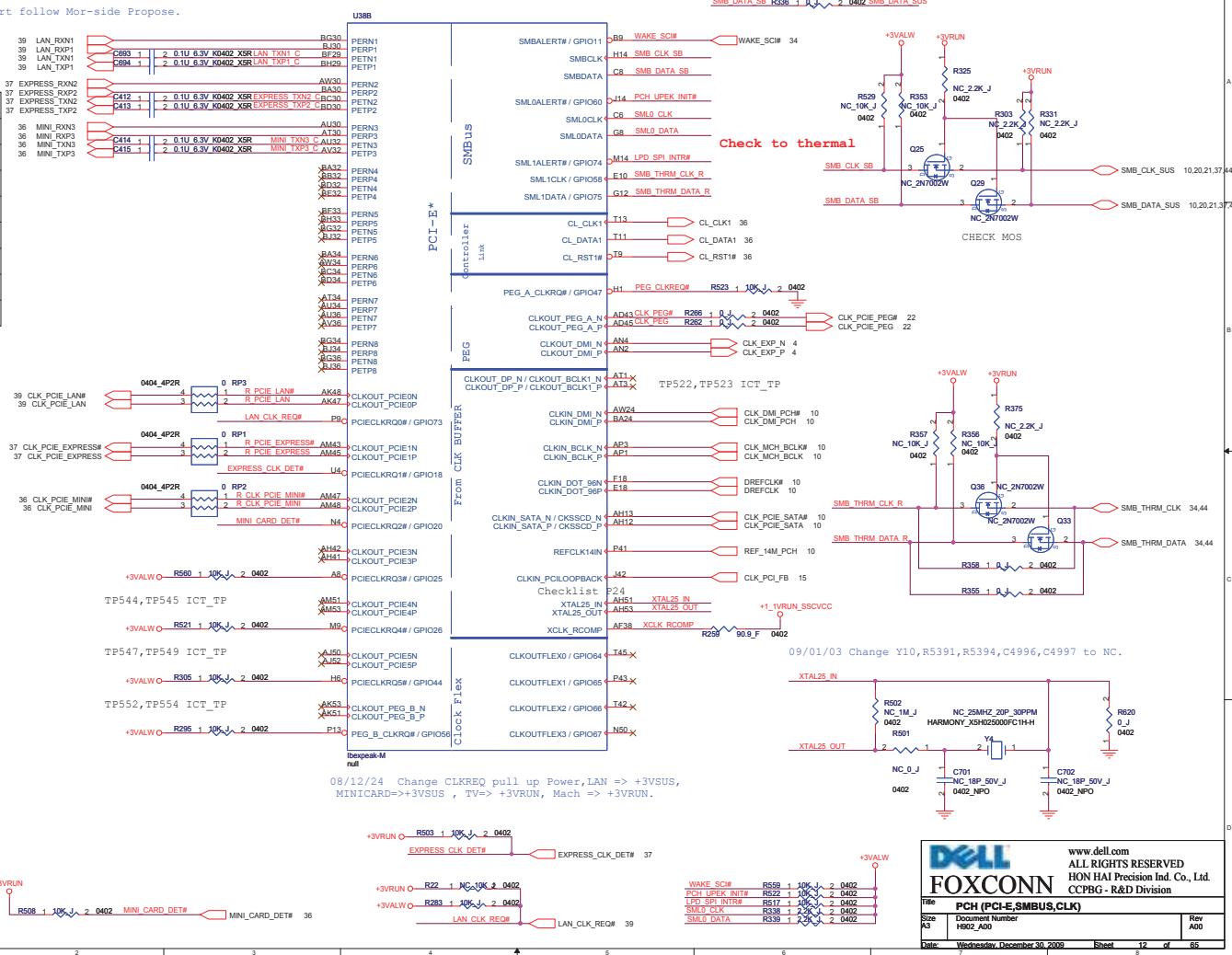


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PCH (HDA, JTAG, SATA)			
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PCI-E Port Table

Port	Function
Port1	LAN
Port2	Express Card
Port3	WLAN
Port4	Un-used
Port5	Un-used
Port6	Un-used
Port7	Un-used
Port8	Un-used

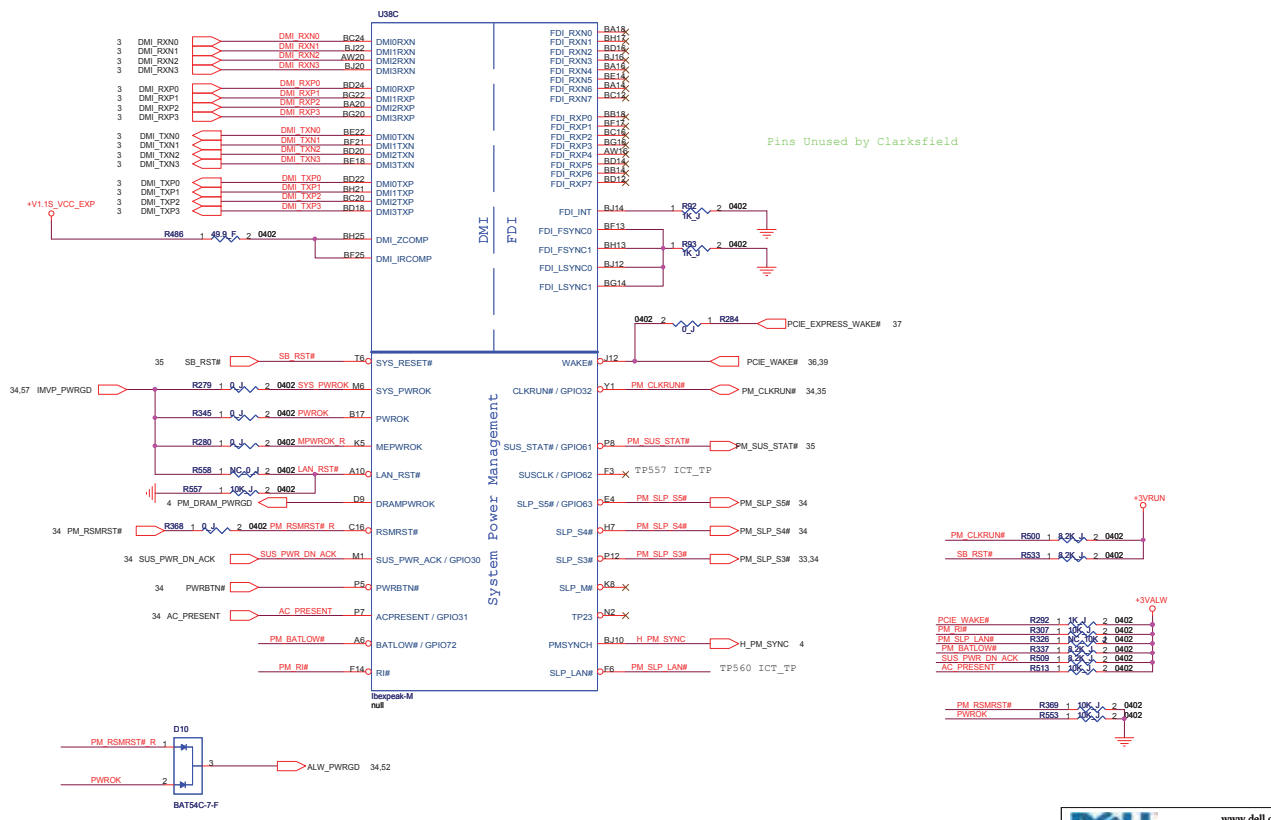


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PCH (PCI-E,SMBUS,CLK)

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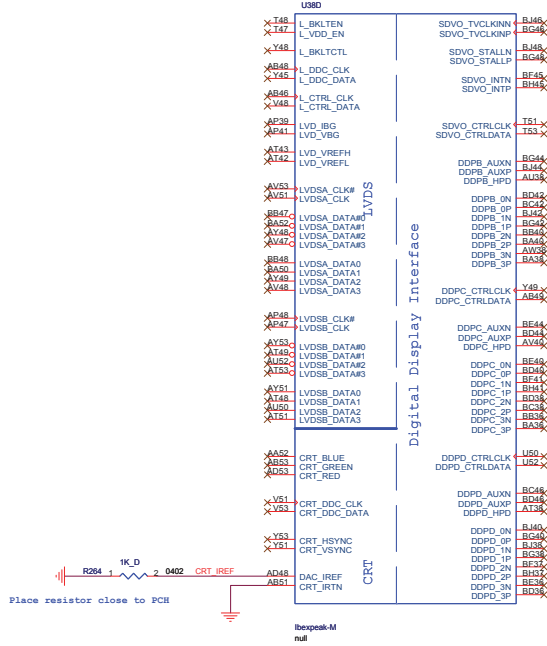


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PCH Intergrated Graphics Disable



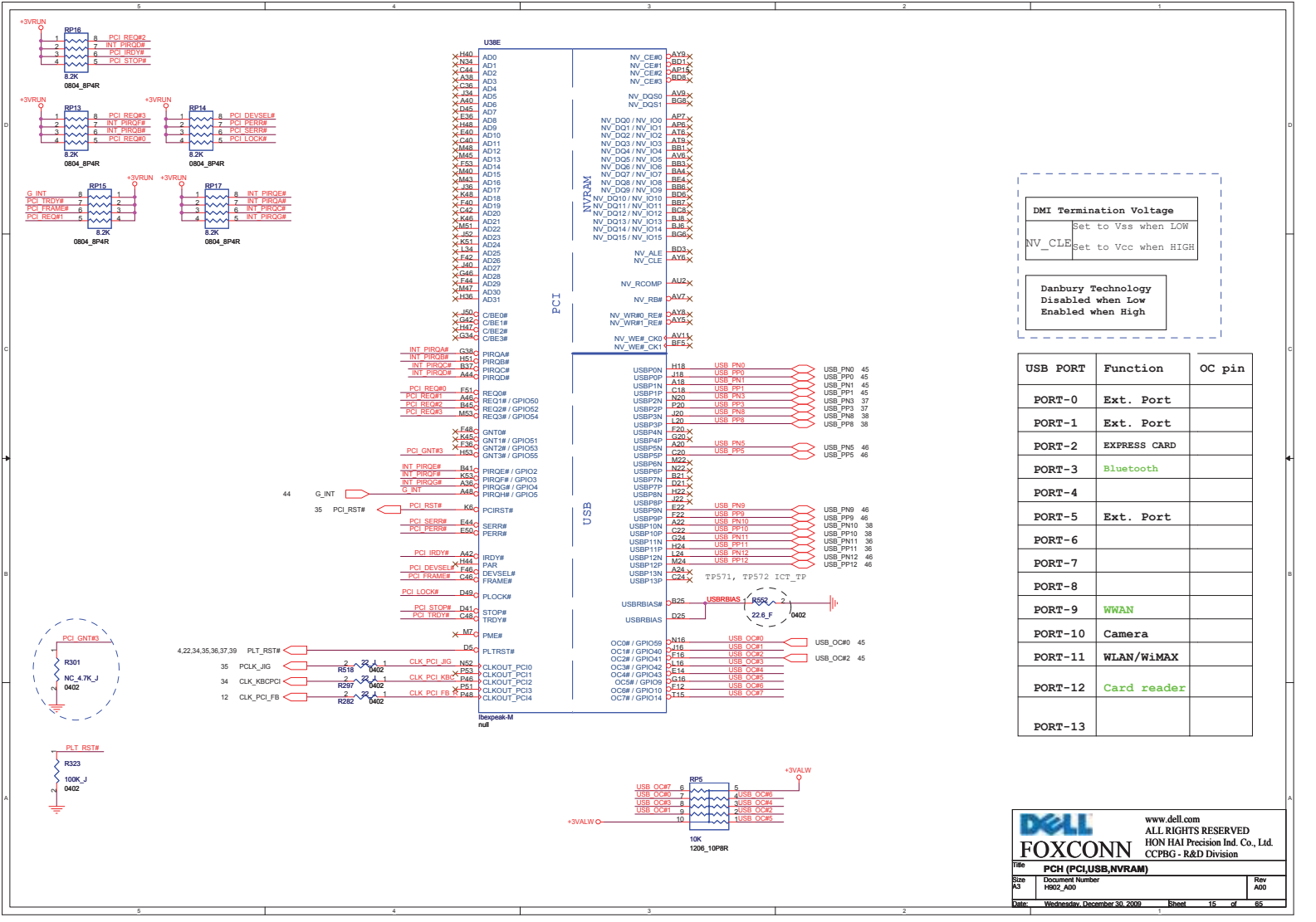
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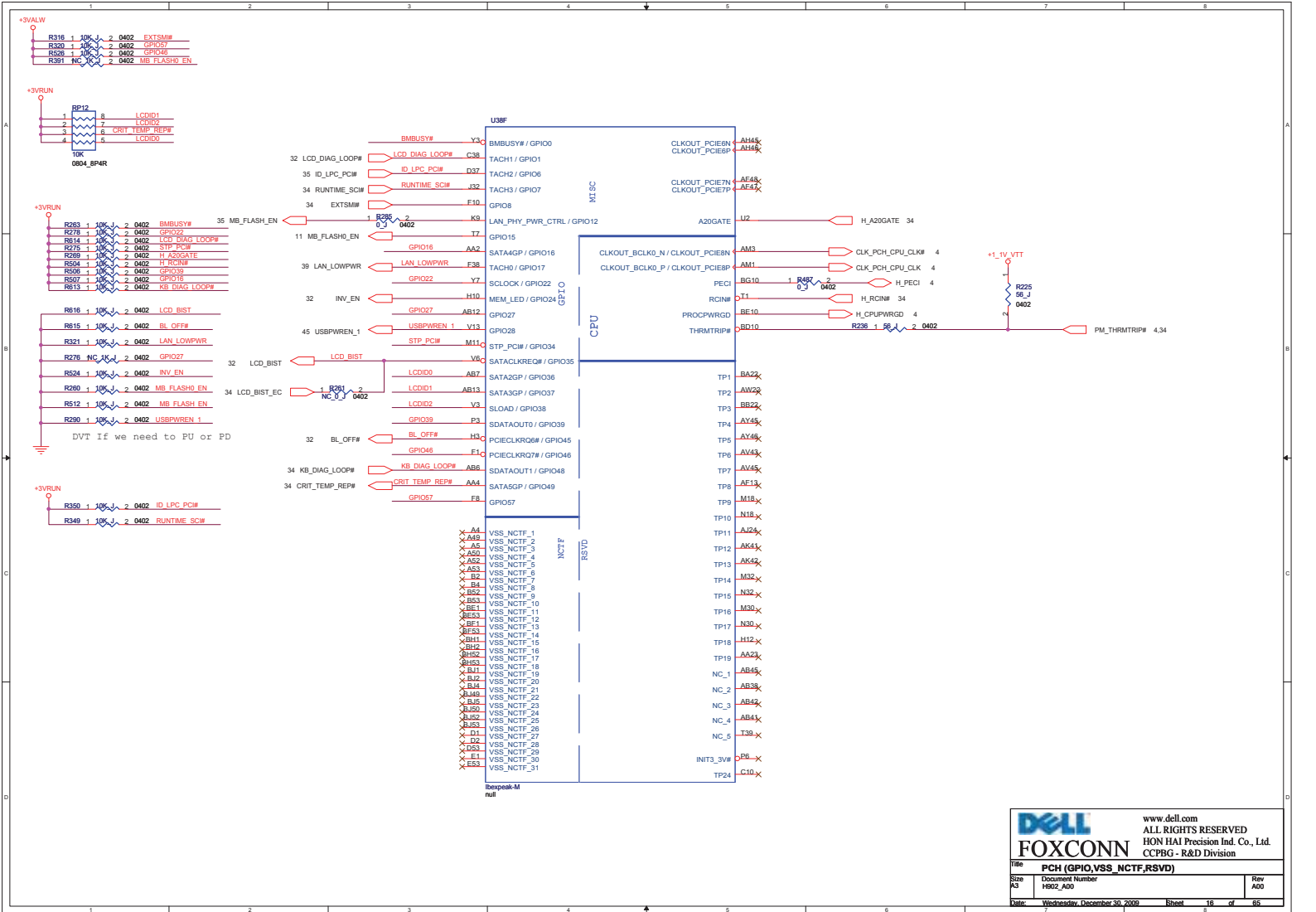
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Title: PCH (PCI,USB,NVDRAM)
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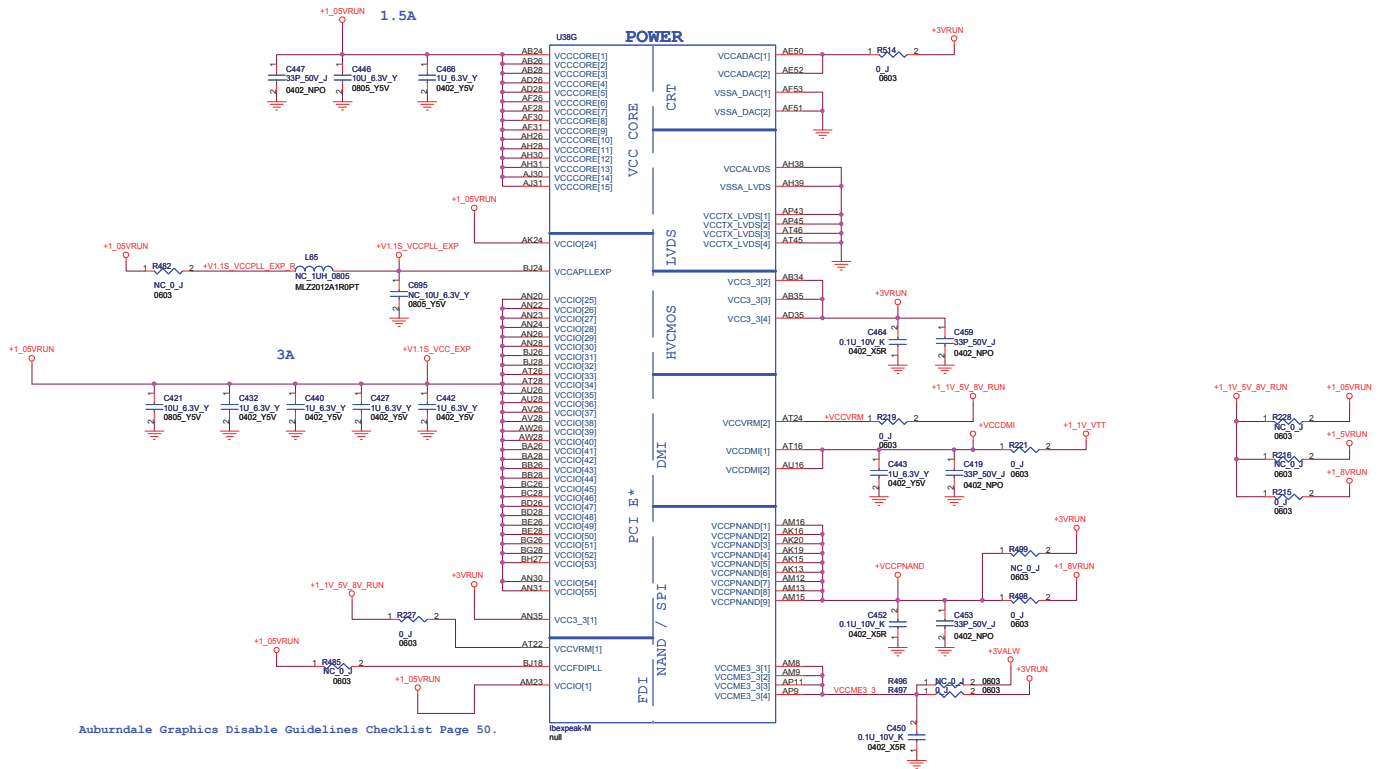


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PCH (POWER) 2/2

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USB		
AV7	VSS169	H49
B11	VSS169	H5
B15	VSS161	J24
B16	VSS161	K11
B23	VSS162	K43
B31	VSS163	K47
B35	VSS164	R7
B38	VSS166	L14
B43	VSS167	L18
B47	VSS166	L2
B7	VSS166	L22
BG12	VSS169	L32
BH12	VSS170	L60
BH16	VSS172	L62
BB20	VSS173	L52
BB4	VSS174	M12
BB30	VSS175	M16
BB34	VSS176	M20
BB38	VSS177	N38
BB42	VSS178	M34
BB46	VSS179	M38
BB5	VSS180	M42
BC10	VSS181	M46
BC14	VSS182	M49
BC18	VSS183	M8
BC2	VSS184	M8
BC22	VSS185	N24
BC26	VSS186	N24
BC46	VSS187	P22
BC44	VSS188	P30
BC52	VSS190	P32
BD9	VSS191	P34
BD48	VSS192	P42
BD5	VSS193	P47
BE12	VSS195	R2
BE16	VSS196	R2
BE20	VSS197	T12
BE30	VSS198	T46
BE34	VSS199	T46
BE38	VSS200	T49
BE42	VSS201	T8
BE46	VSS202	T8
BE48	VSS203	U31
BE50	VSS204	U32
BE5	VSS205	U34
BE8	VSS206	P38
BE3	VSS207	P11
BF49	VSS209	P16
BF51	VSS210	P16
BG18	VSS210	V20
BG24	VSS212	V22
BG4	VSS213	V20
BG50	VSS214	V31
BH11	VSS215	V31
BH15	VSS216	V36
BH12	VSS217	V38
BH36	VSS218	V45
BH31	VSS219	V43
BH35	VSS220	V47
BH38	VSS221	V46
BH43	VSS222	V49
BH47	VSS223	V49
BH7	VSS224	V5
CI2	VSS225	V7
C50	VSS226	V8
D51	VSS227	W2
E12	VSS227	W52
E16	VSS229	X11
E20	VSS230	Y12
E24	VSS231	Y15
E34	VSS232	Y23
E38	VSS233	Y28
E42	VSS234	Y30
E46	VSS235	Y31
E48	VSS236	Y32
E8	VSS237	Y38
E8	VSS238	Y43
F49	VSS239	Y46
F5	VSS241	Y49
G10	VSS242	Y5
G14	VSS243	Y8
G2	VSS244	Y8
G22	VSS245	P24
G22	VSS248	T43
G32	VSS247	AT51
G36	VSS248	AT8
G40	VSS249	AD47
G44	VSS250	Y47
G52	VSS251	AT12
AF38	VSS252	AM5
H16	VSS253	AT13
H20	VSS254	AM5
H30	VSS255	AK45
H34	VSS256	AK38
H38	VSS257	AV14
H42	VSS258	VSS366

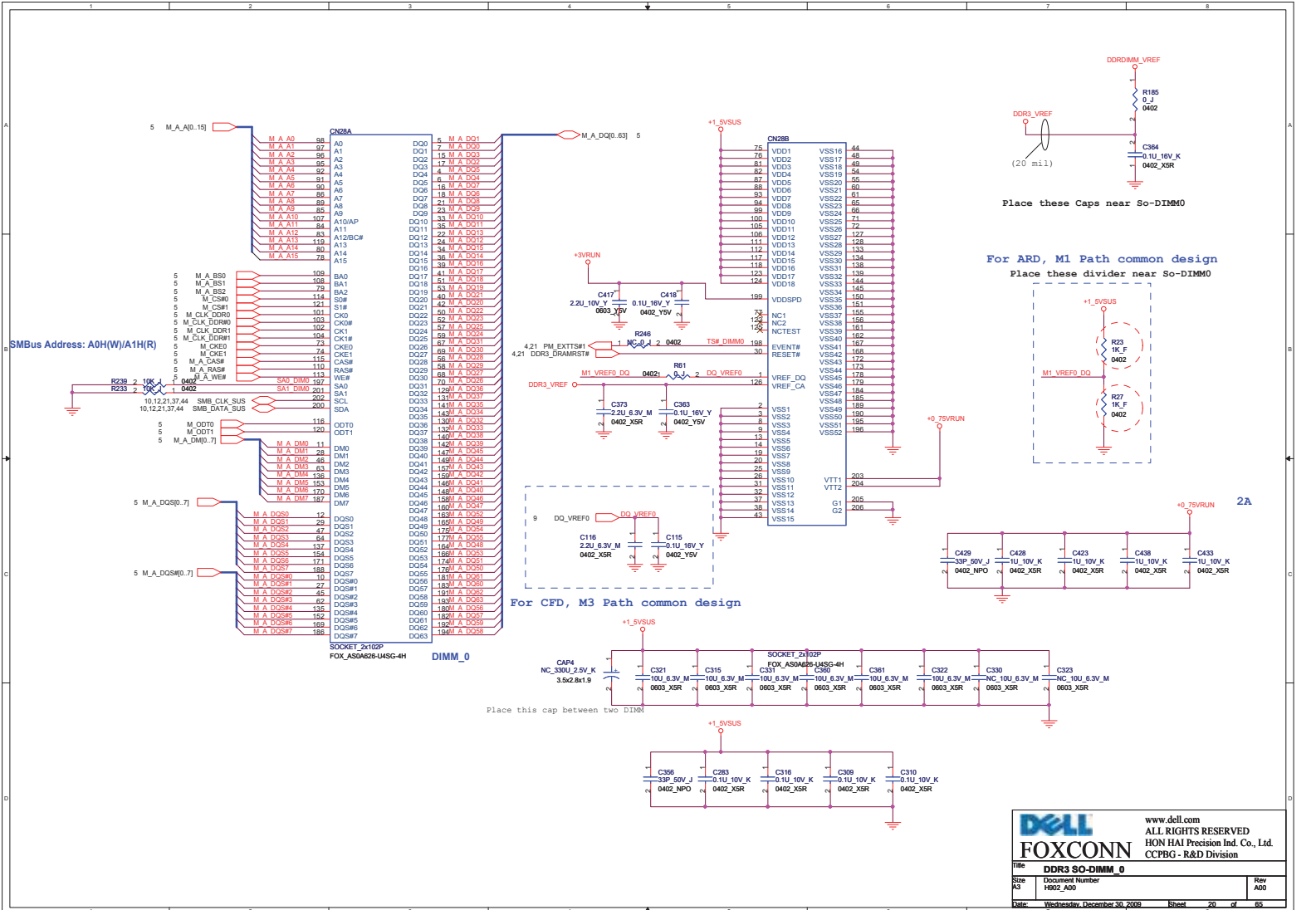
USBH		
AB16	VSS01	
AA18	VSS01	VSS80
AA20	VSS02	VSS81
AA22	VSS03	VSS82
AA19	VSS04	VSS83
AA24	VSS05	VSS84
AA28	VSS06	VSS85
AA30	VSS08	VSS87
AA31	VSS09	VSS88
AA32	VSS10	VSS89
AA33	VSS11	VSS90
AB15	VSS12	VSS91
AB30	VSS13	VSS92
AB30	VSS14	VSS93
AB30	VSS15	VSS94
AB30	VSS16	VSS95
AB30	VSS17	VSS96
AB47	VSS18	VSS97
AB5	VSS19	VSS98
AB5	VSS20	VSS99
AB8	VSS21	VSS100
AC2	VSS22	VSS101
AC2	VSS23	VSS102
AD11	VSS24	VSS103
AD12	VSS25	VSS104
AD18	VSS26	VSS105
AD23	VSS27	VSS106
AD30	VSS28	VSS107
AD31	VSS29	VSS108
AD32	VSS30	VSS109
AD34	VSS31	VSS110
AU22	VSS32	VSS111
AD32	VSS33	VSS112
AD46	VSS34	VSS113
AD7	VSS35	VSS114
AE2	VSS36	VSS115
AE4	VSS37	VSS116
AF4	VSS38	VSS117
AF12	VSS39	VSS118
AF12	VSS40	VSS119
AH49	VSS41	VSS120
AU4	VSS42	VSS121
AF6	VSS43	VSS122
AP13	VSS44	VSS123
AK4	VSS45	VSS124
AE5	VSS46	VSS125
AE6	VSS47	VSS126
AE9	VSS48	VSS127
AF5	VSS49	VSS128
AF8	VSS50	VSS129
AG2	VSS51	VSS130
AH11	VSS52	VSS131
AH15	VSS53	VSS132
AH15	VSS54	VSS133
AH18	VSS55	VSS134
AH24	VSS56	VSS135
AV18	VSS57	VSS136
AH4	VSS58	VSS137
AH7	VSS59	VSS138
AH7	VSS60	VSS139
AJ3	VSS61	VSS140
AJ2	VSS62	VSS141
AJ20	VSS63	VSS142
AJ22	VSS64	VSS143
AJ23	VSS65	VSS144
AJ28	VSS66	VSS145
AJ28	VSS67	VSS146
AJ32	VSS68	VSS147
AJ34	VSS69	VSS148
AT5	VSS70	VSS149
AK4	VSS71	VSS150
AK12	VSS72	VSS151
AK12	VSS73	VSS152
AK19	VSS74	VSS153
AK28	VSS75	VSS154
AK22	VSS76	VSS155
AK27	VSS77	VSS156
AK23	VSS78	VSS157
AK28	VSS79	VSS158

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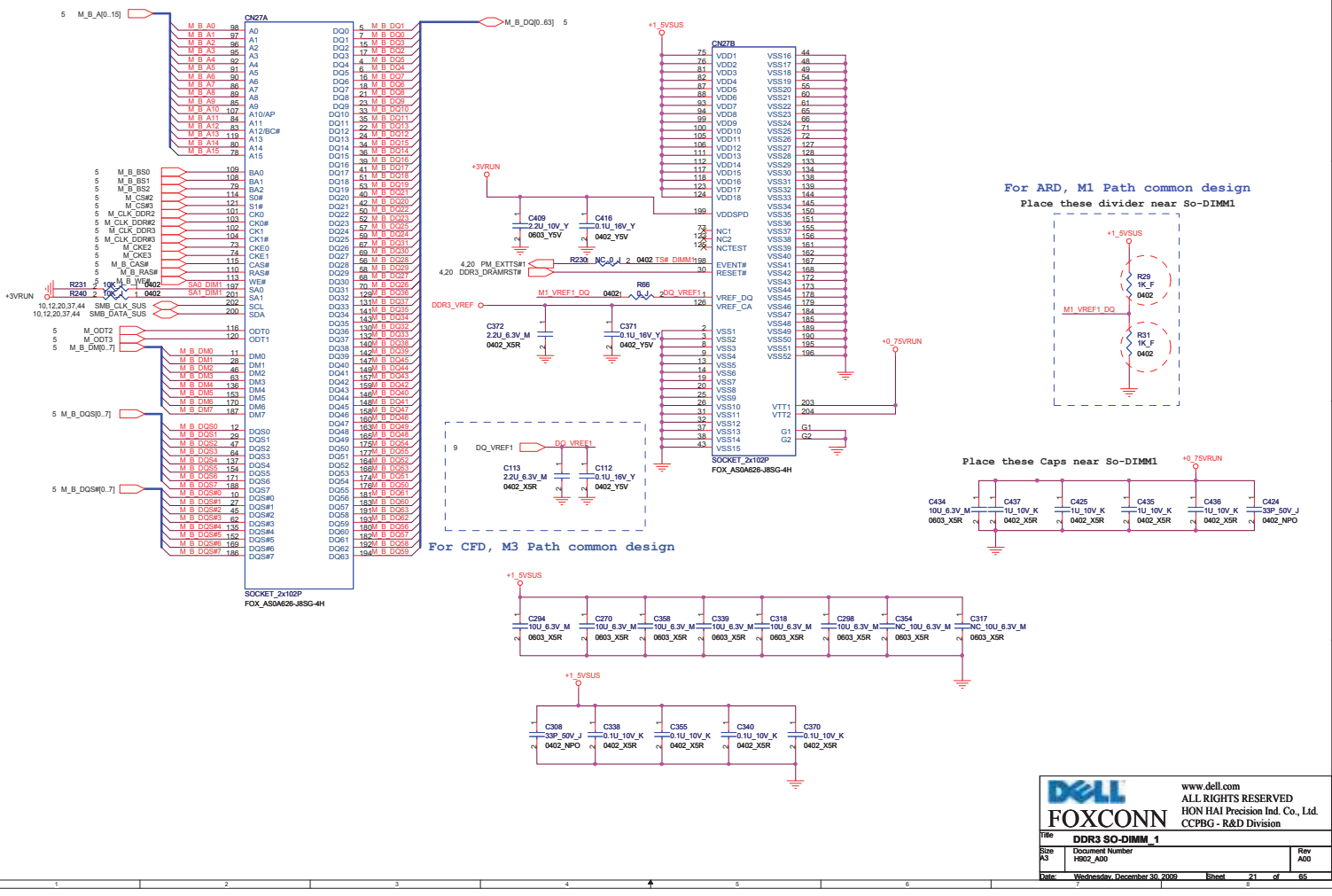
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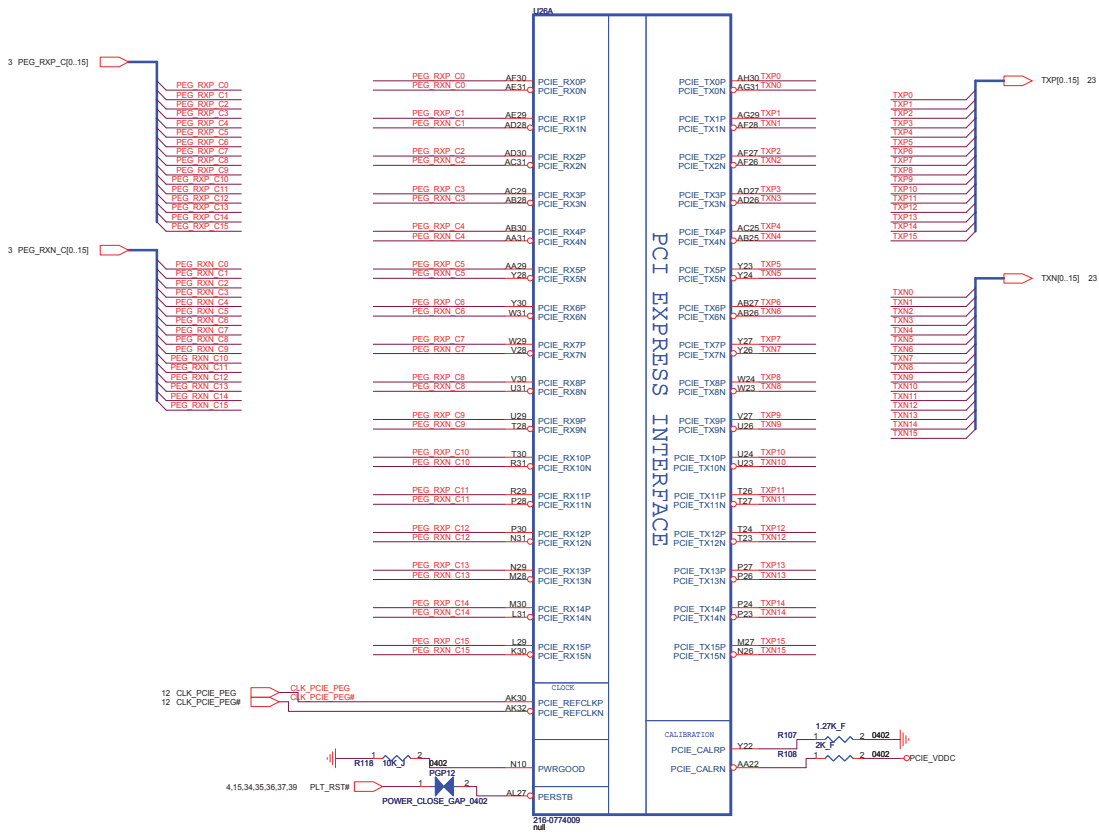
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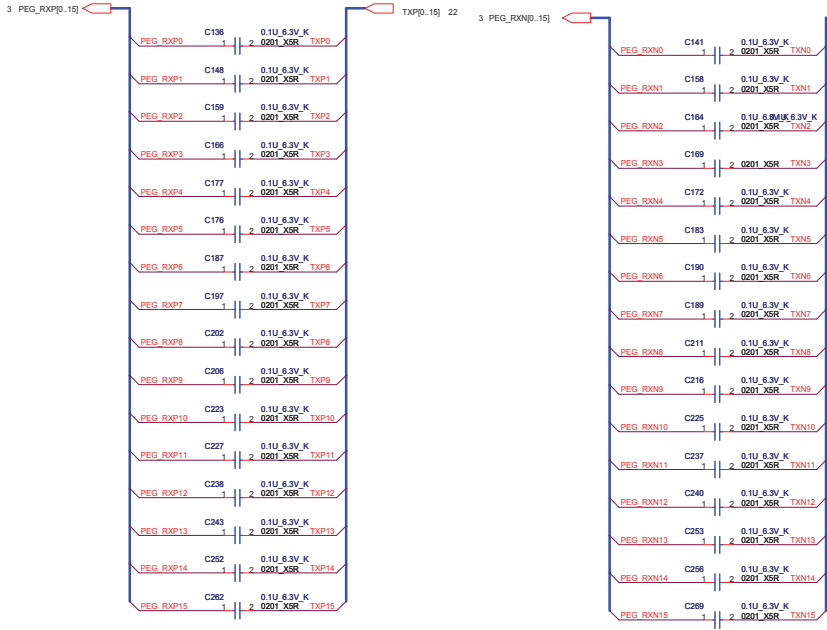
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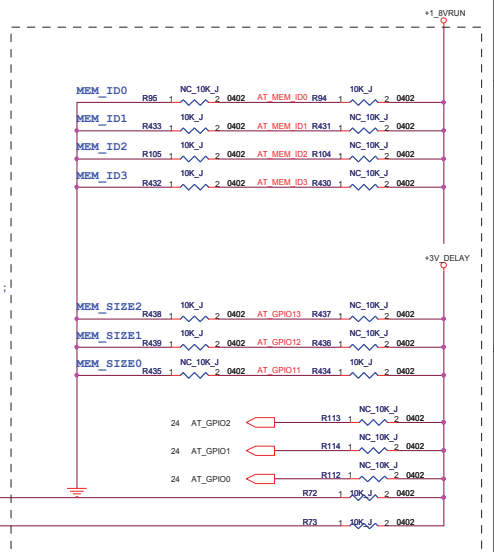
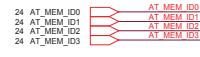
	Mount	NC
Samsung 1GB K4W2G1646B-HC12 P/N: 13-K4W2G16-3000	R432 (0), R105 (0) R433 (0), R94 (1)	R430 (1), R104 (1) R431 (1), R95 (0)
Hynix 1GB H5TQ2G63BFR-12C P/N: 13-H5T02G6-3000	R432 (0), R105 (0) R433 (0), R95 (0)	R430 (1), R104 (1) R431 (1), R94 (1)



Strap for DDR3
ATI_DVDPDATA[1:0 :21:20]
0000 128Mx16 Hynix 1GB
0001 128Mx16 Samsung 1GB

If no ROM attached, GPIO[13:12:11] ;
CONFIG(2:0)
controls the memory aperture size.
64MB 010
128MB 000
256MB 001
512MB 001

HSYNC , VSYNC
AUD[1] , AUD[0]
0,0 No audio function
0,1 Audio for DisplayPort and HDMI if dongle is detected
1,0 Audio for DisplayPort only
1,1 Audio for both DisplayPort and HDMI

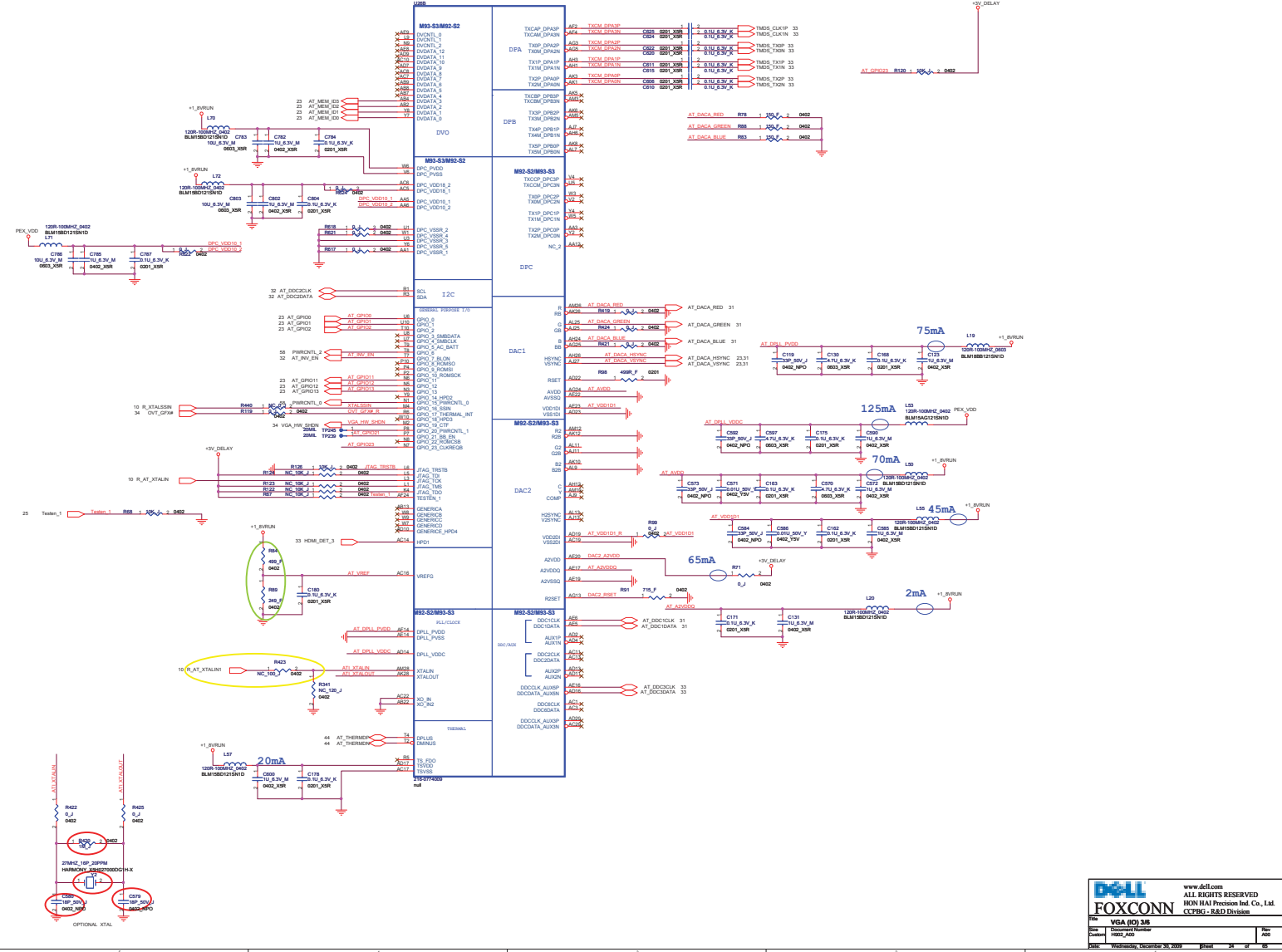


GPIO 0 : PCIE FULL TX OUTPUT SWING
GPIO 1 : PCIE TRANSMITTER DE-EMPHASIS ENABLED
GPIO 2 : PCIE GEN2 ENABLED

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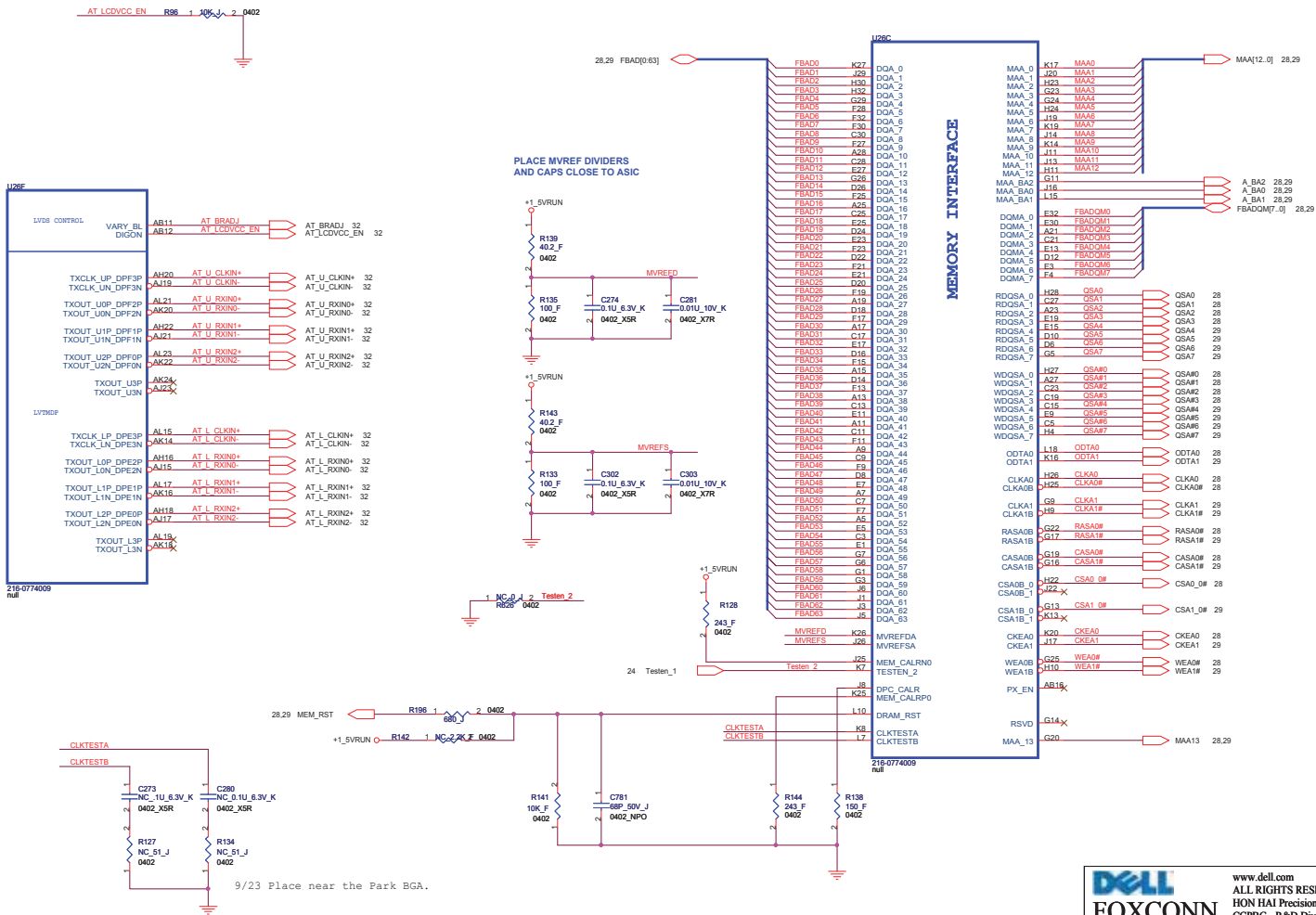
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Size: A3	Document Number: H802_A00	Rev: A00	
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Place to connect two ground for EMI recommend.



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 VISA (H) SR
 Date: Wednesday, December 24, 2008 10:02 AM Page 24 of 38

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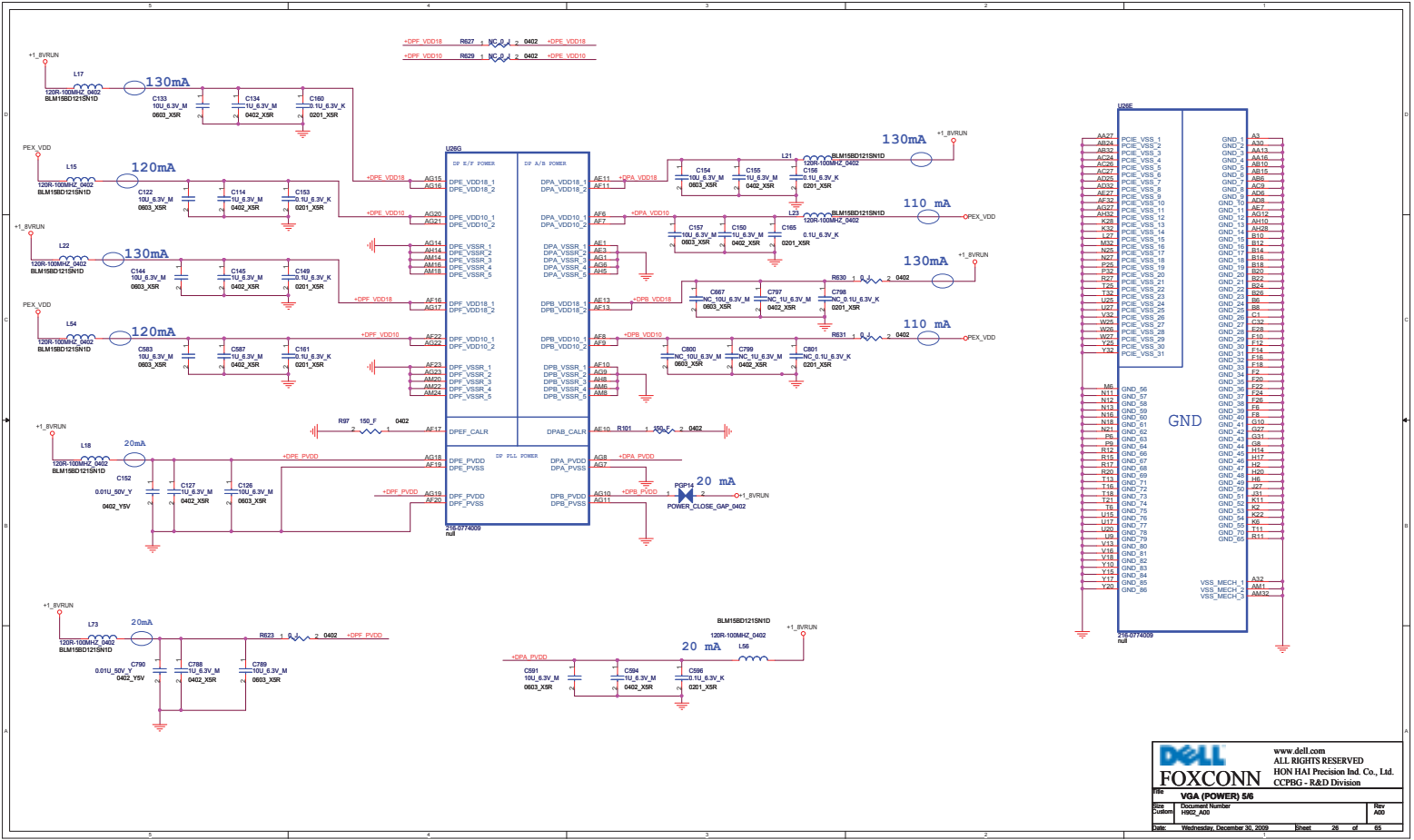


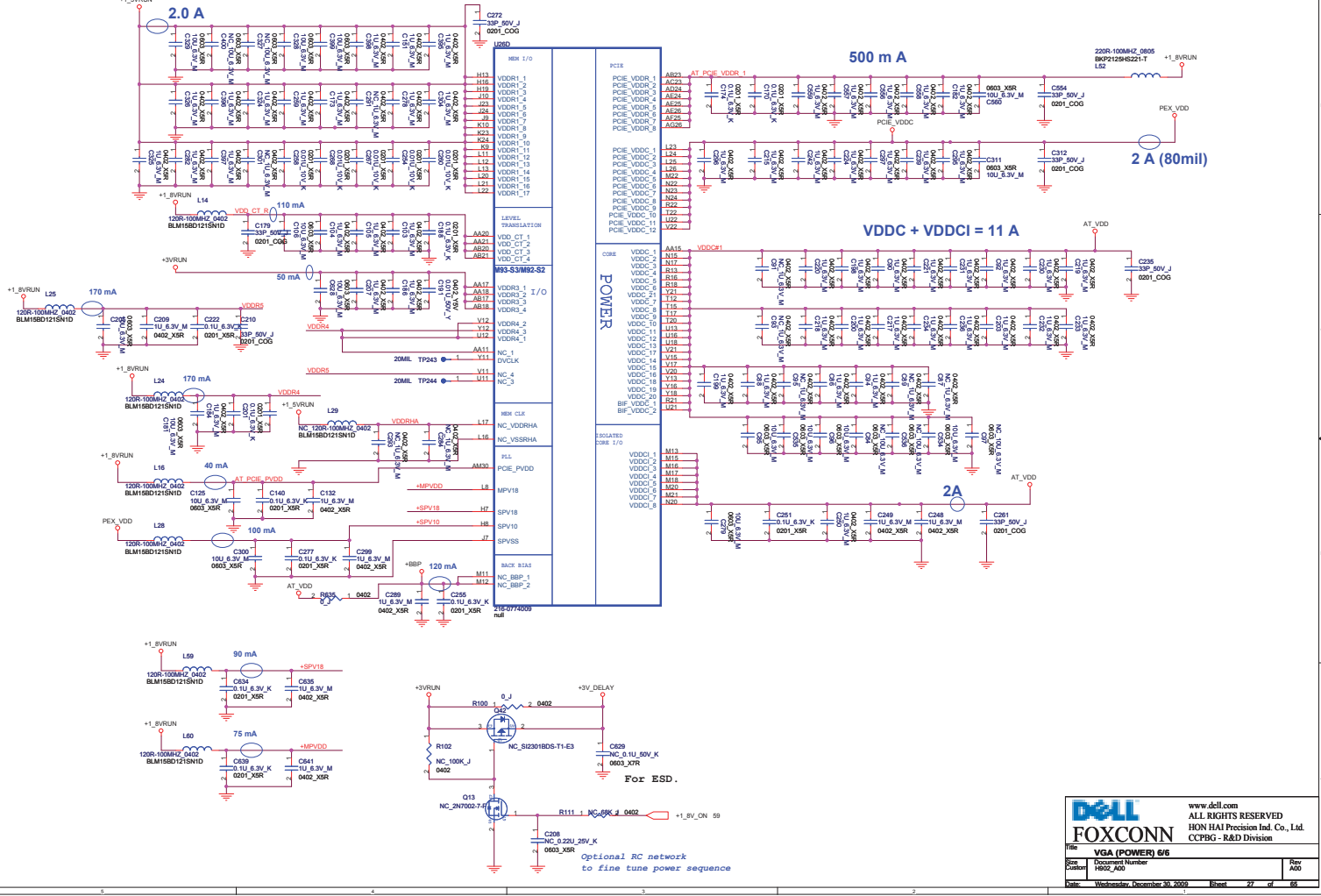
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Date: Wednesday, December 30, 2009	Sheet: 26	of: 85

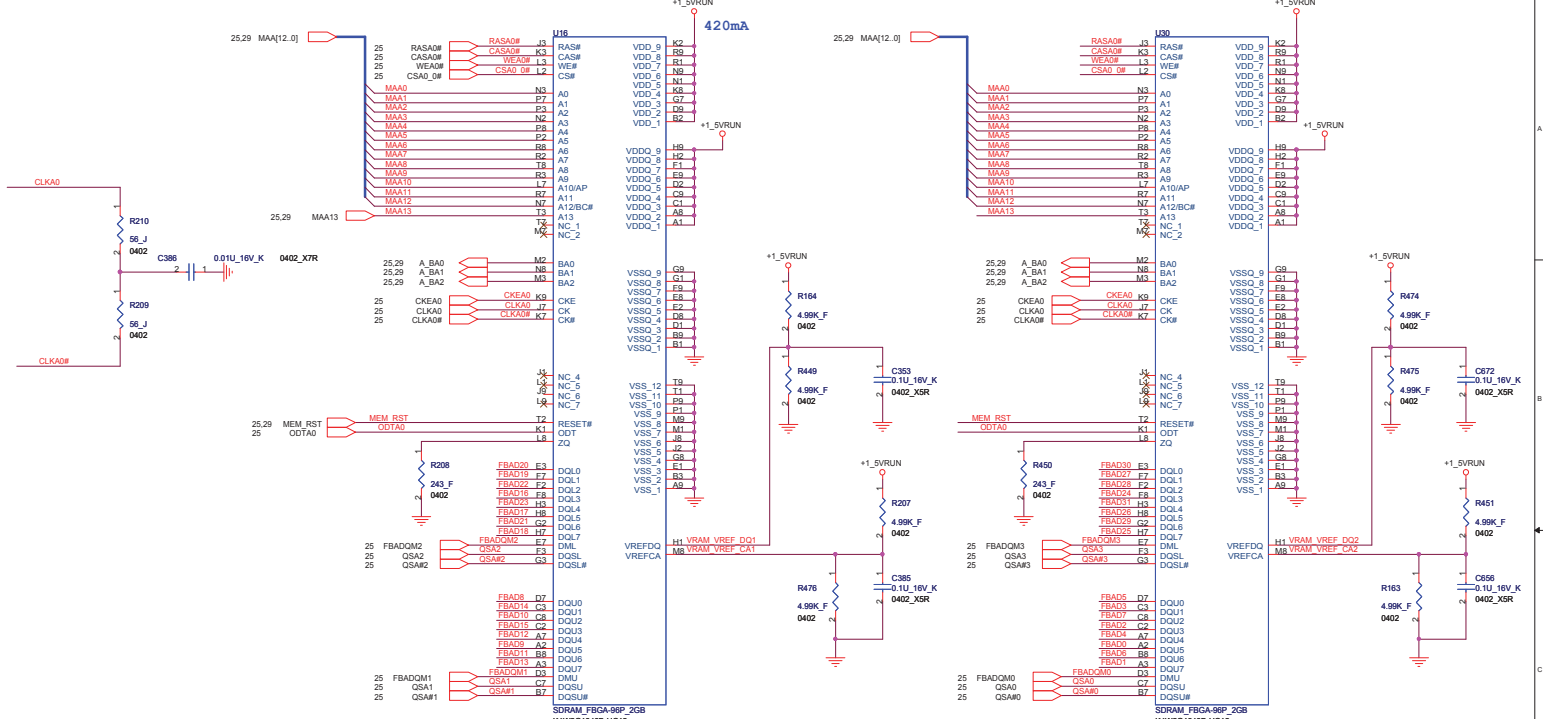
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File VGA (POWER) 016
Size 100KB
Document Number R602_000
Rev Add
Date Wednesday, December 30, 2009 **Sheet** 27 of 66

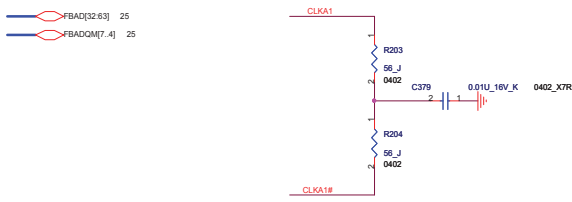
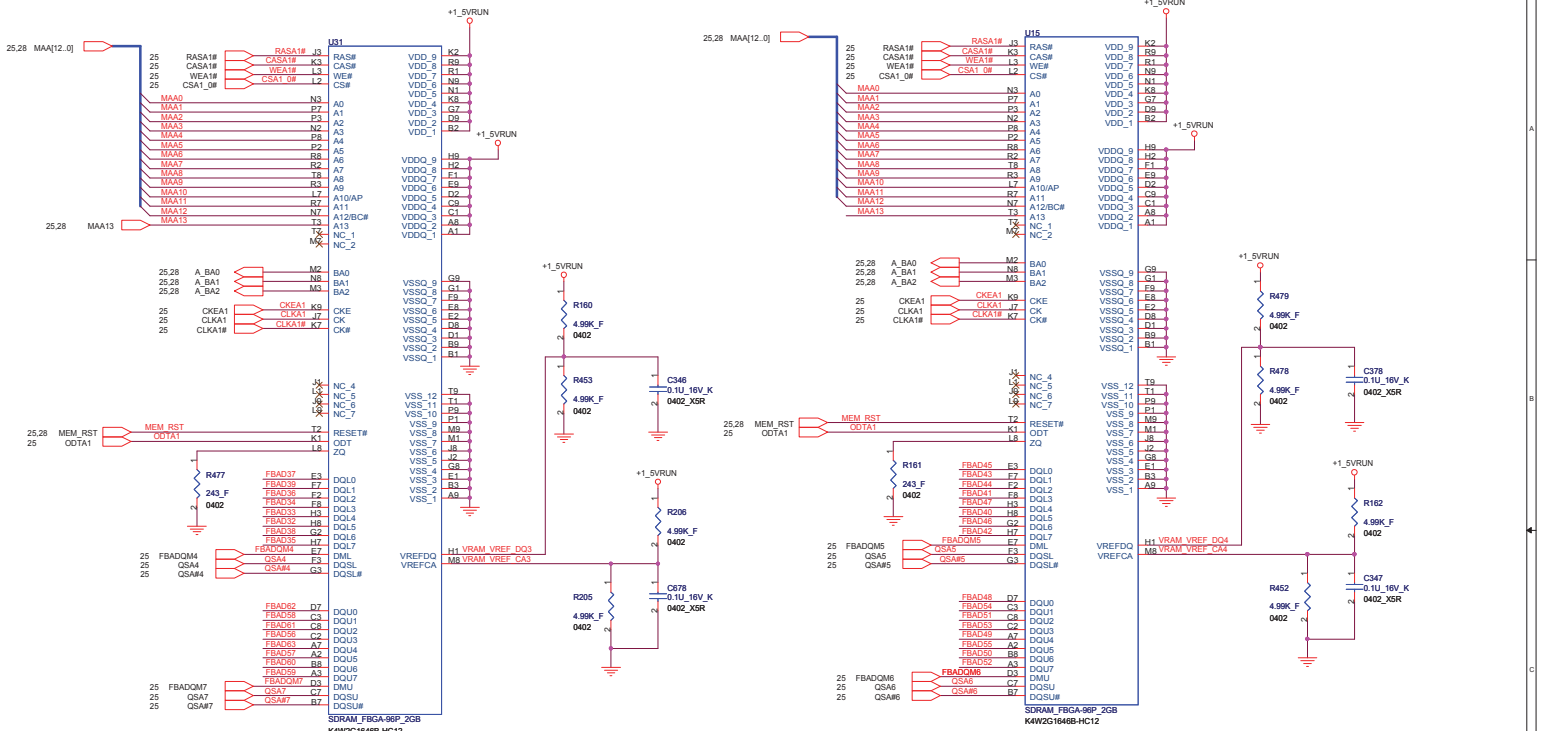


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VRAM (DDR3) 1/3
 Title: _____
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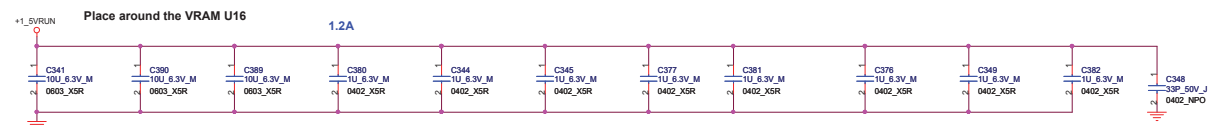
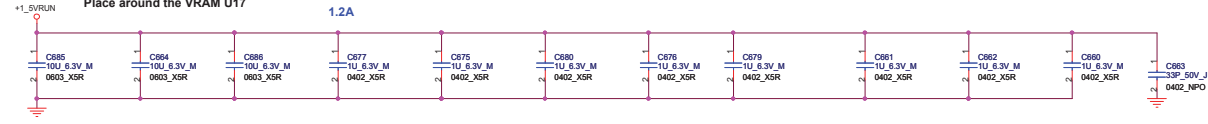
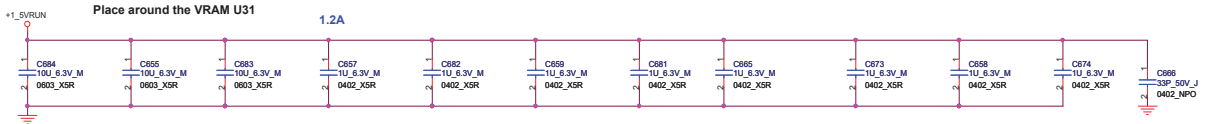
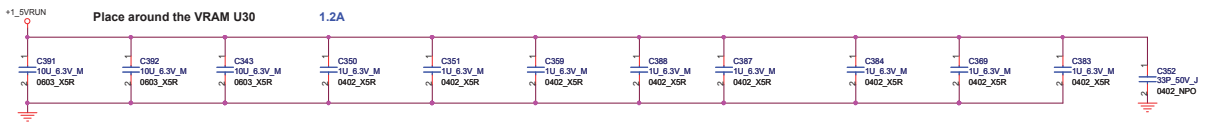
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VRAM (DDR3) 2/3

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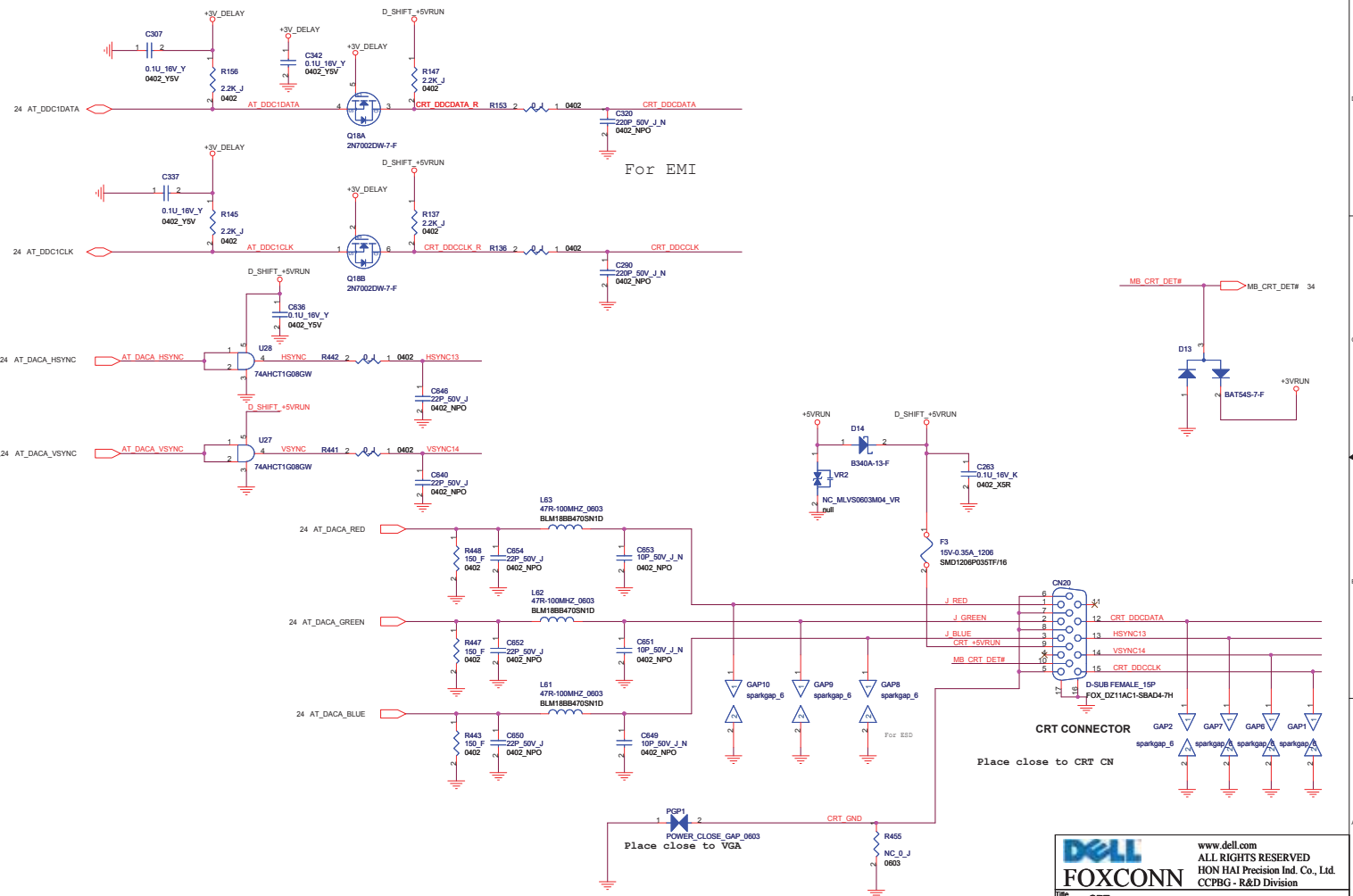
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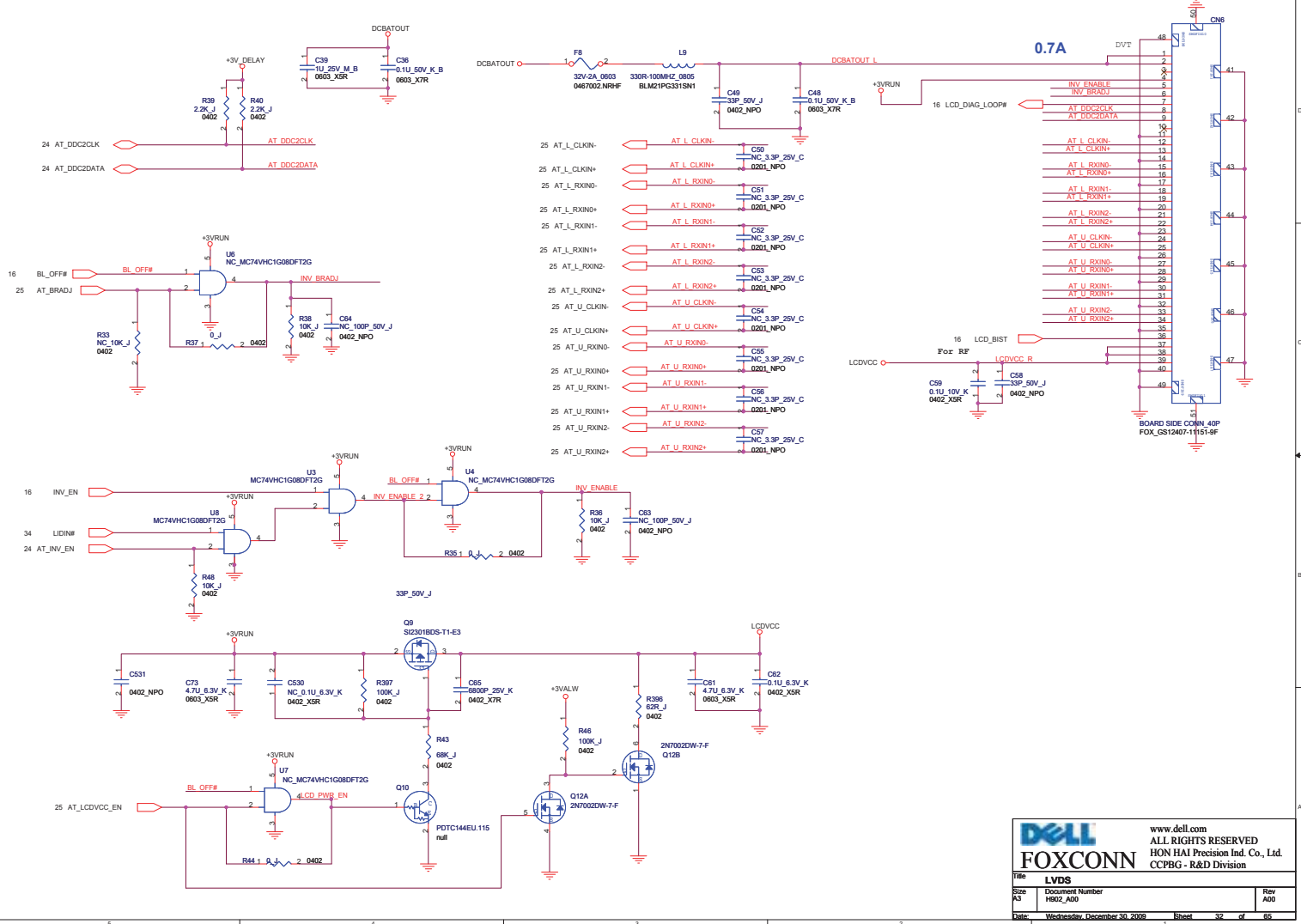
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Title:	Document Number	Rev
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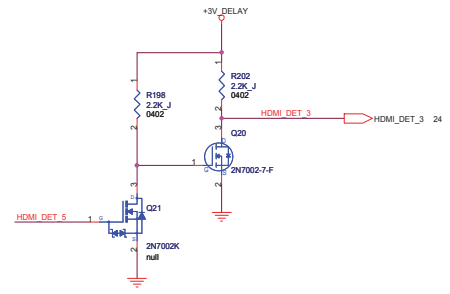
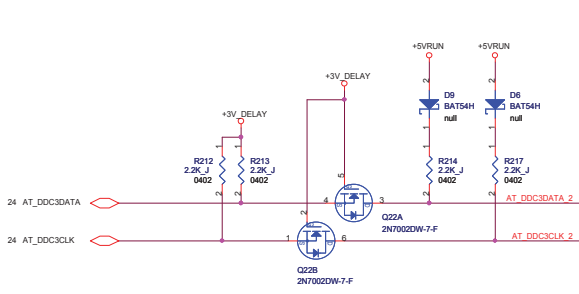
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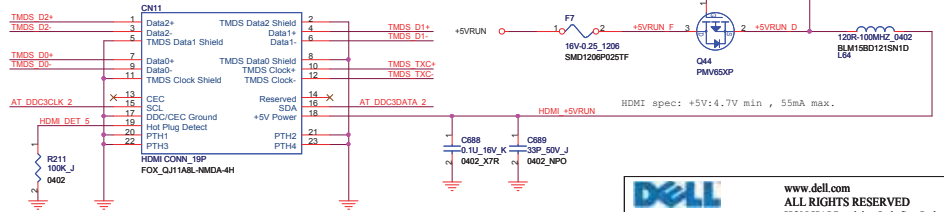
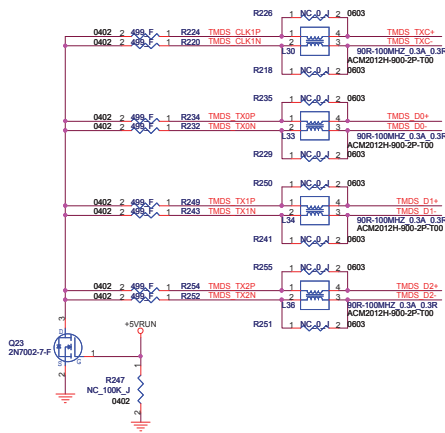
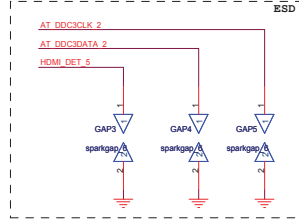
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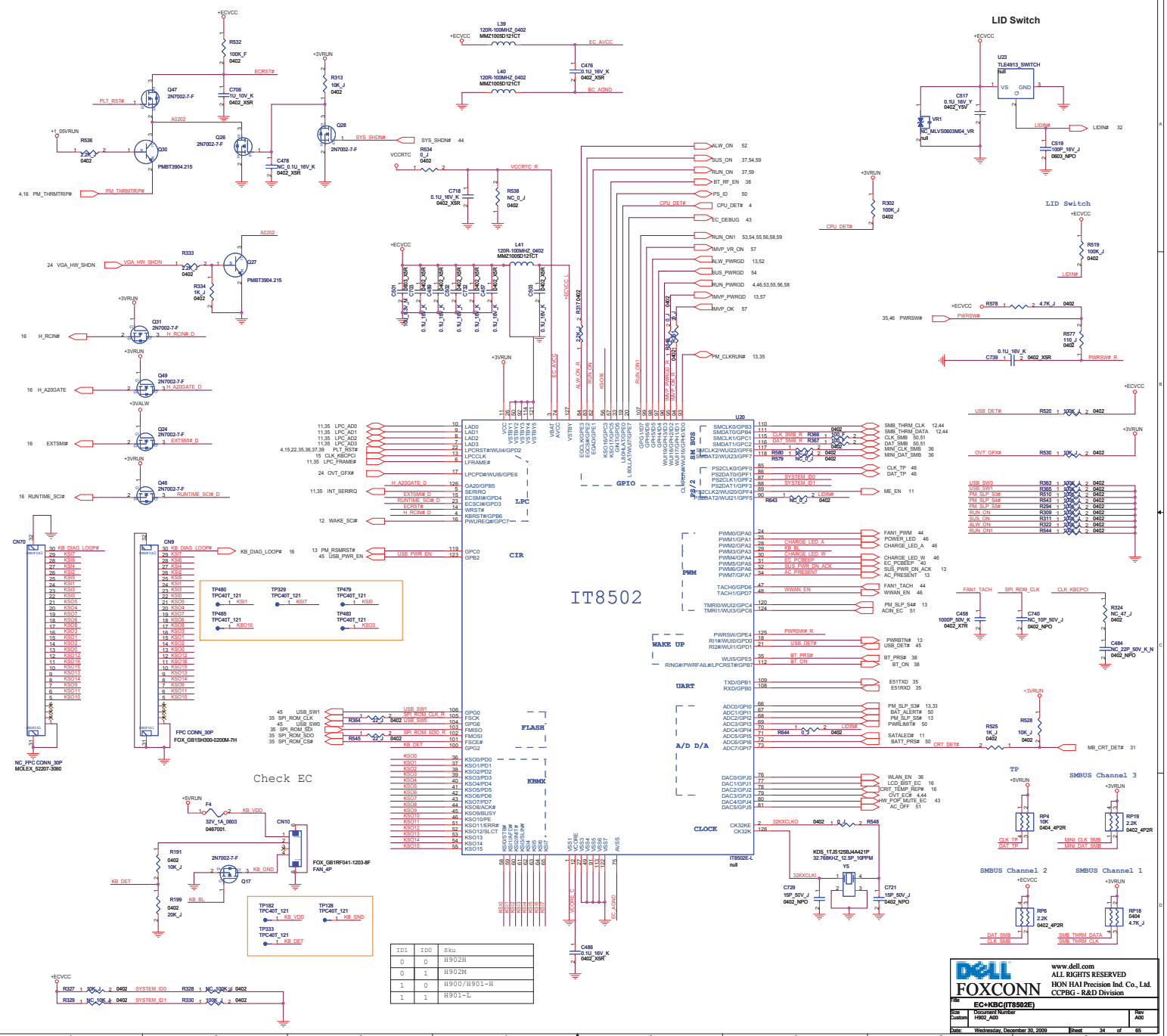


- 24 TMSD_CLKIN → TMSD_CLKIN
- 24 TMSD_CLK1P → TMSD_CLK1P
- 24 TMSD_TX0N → TMSD_TX0N
- 24 TMSD_TX0P → TMSD_TX0P
- 24 TMSD_TX1N → TMSD_TX1N
- 24 TMSD_TX1P → TMSD_TX1P
- 24 TMSD_TX2N → TMSD_TX2N
- 24 TMSD_TX2P → TMSD_TX2P



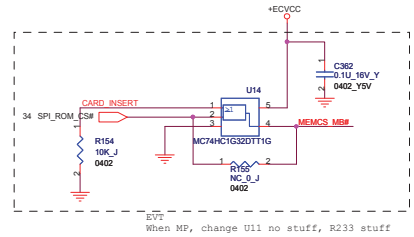
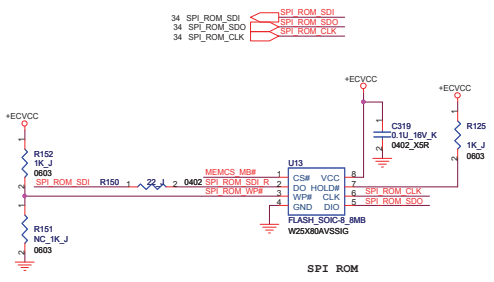
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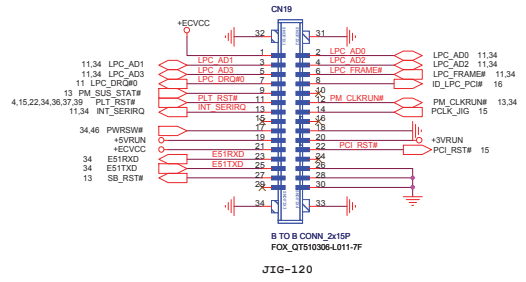
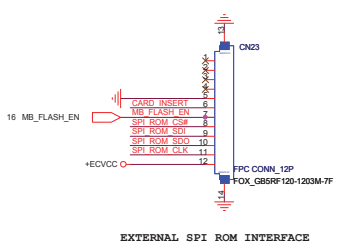


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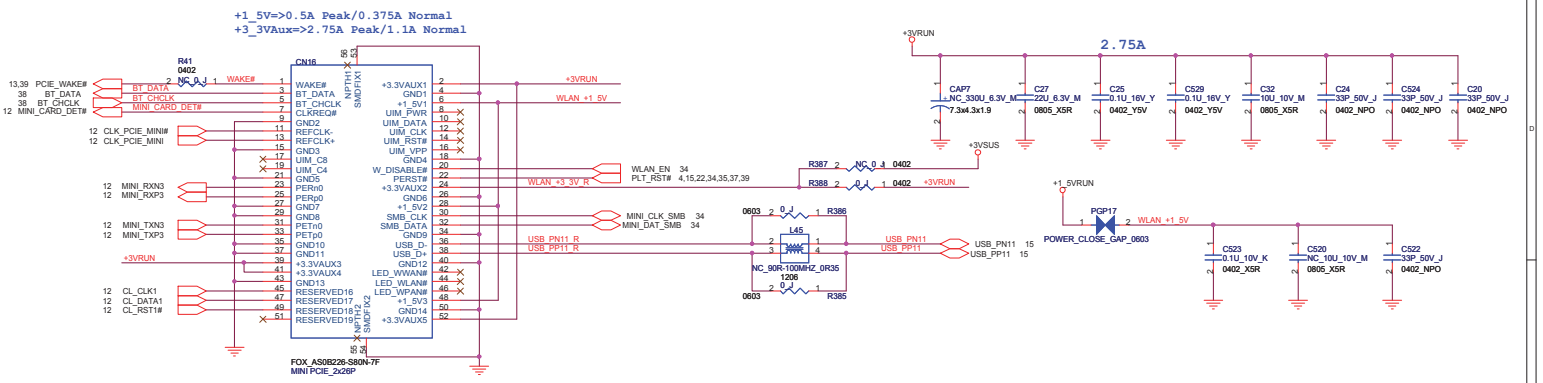


Discuss with SW about BIOS Capacity

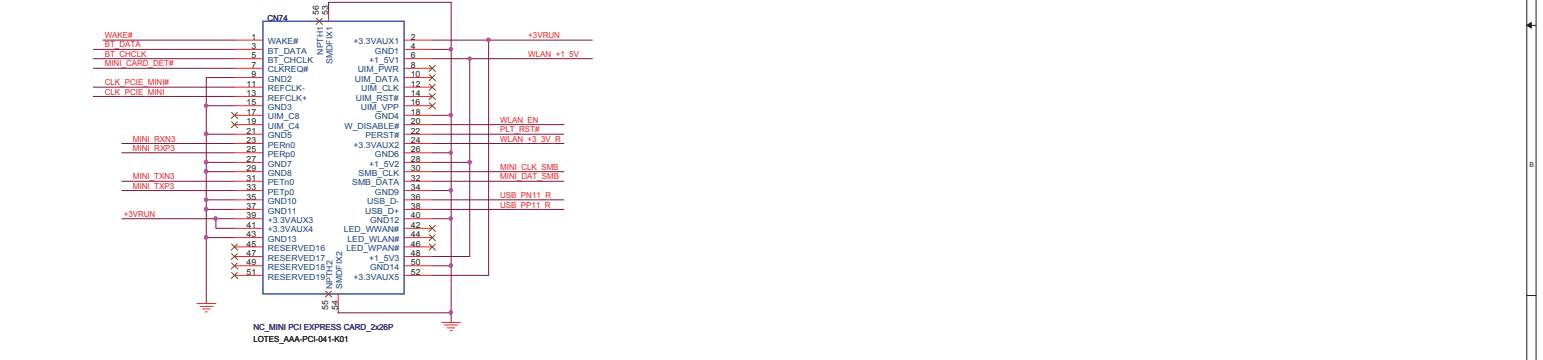


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		Flash ROM/SPI	
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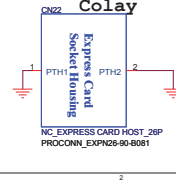
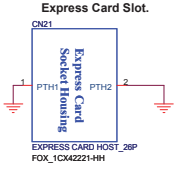
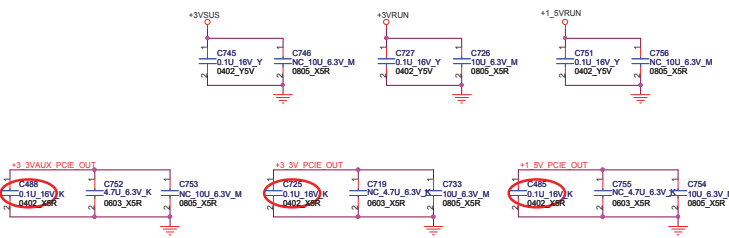
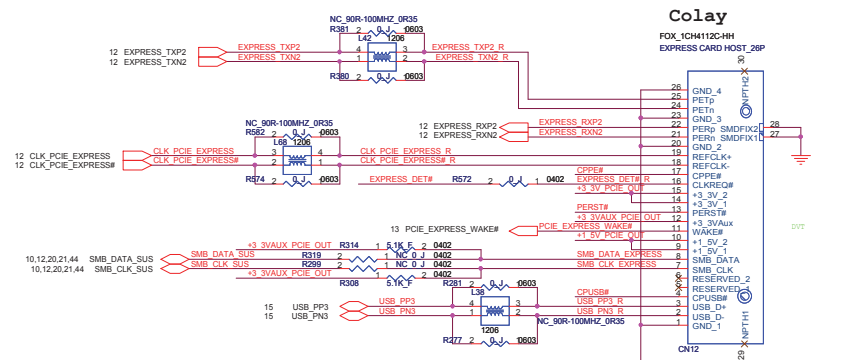
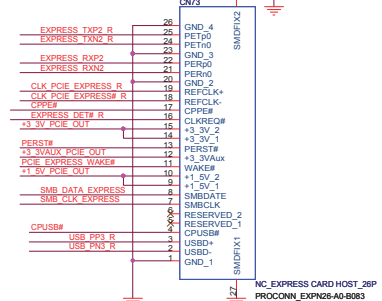
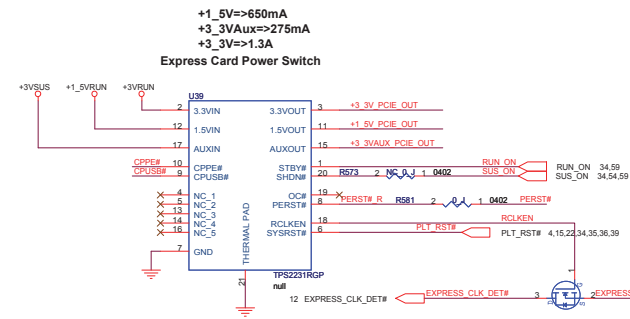
Half Mini Card for WLAN or WiMAX



NC Mini PCI EXPRESS CARD 2x28P
 LOTES_MAA-PCI-041-K01

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WLAN/Wimax Mini-PCIE Card		
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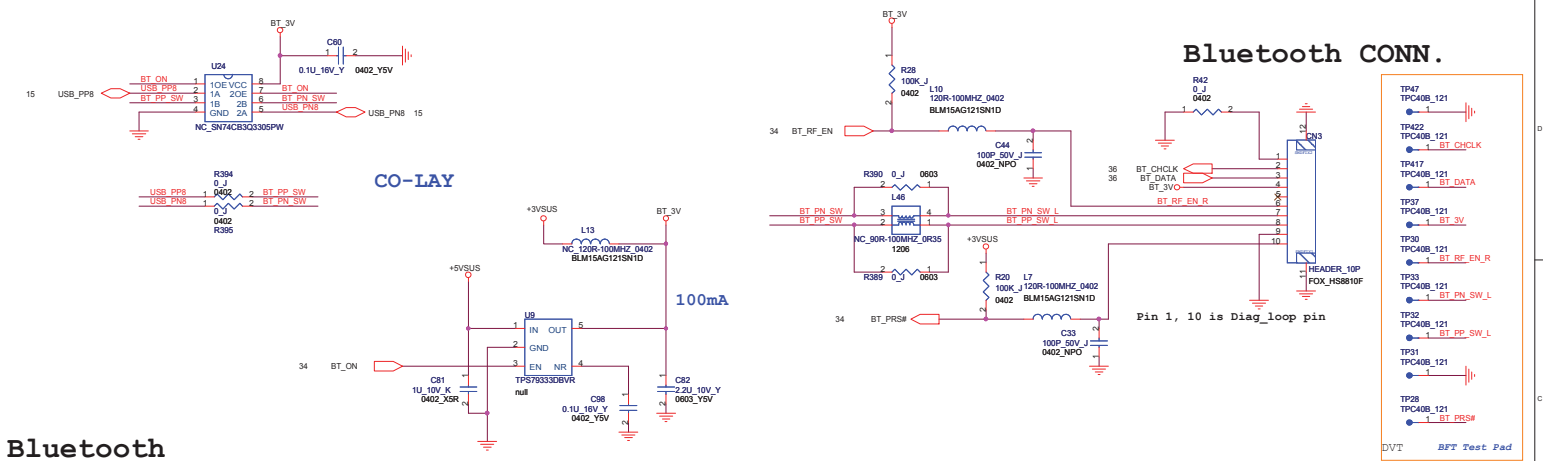


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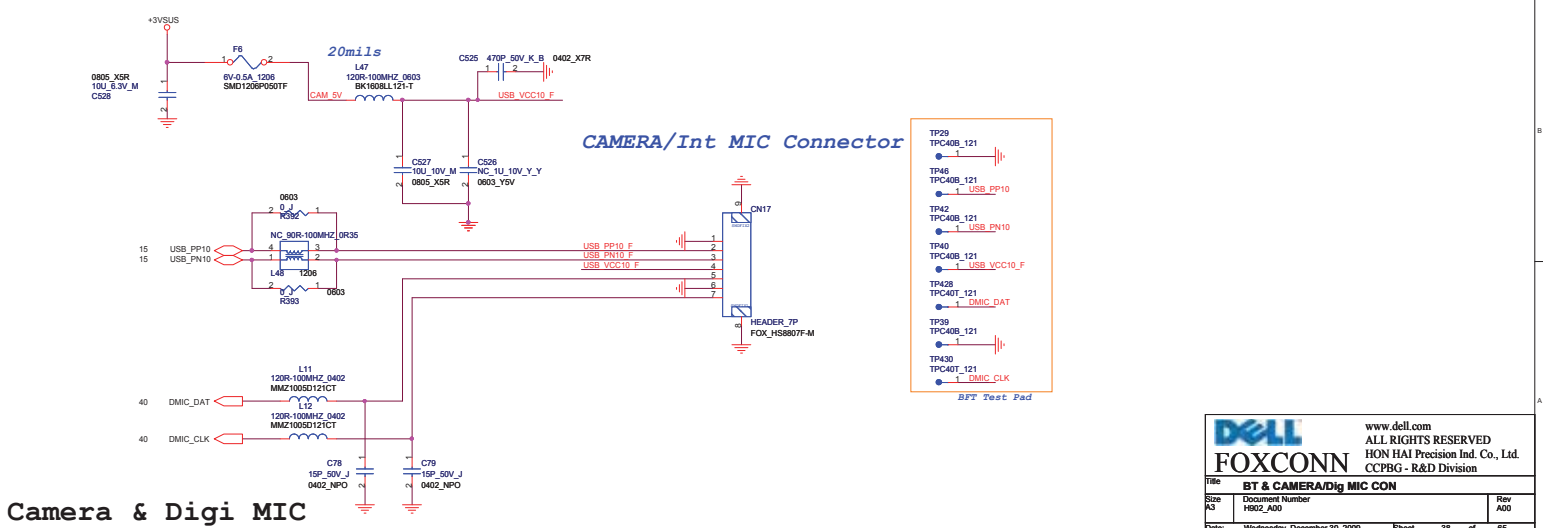
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Bluetooth

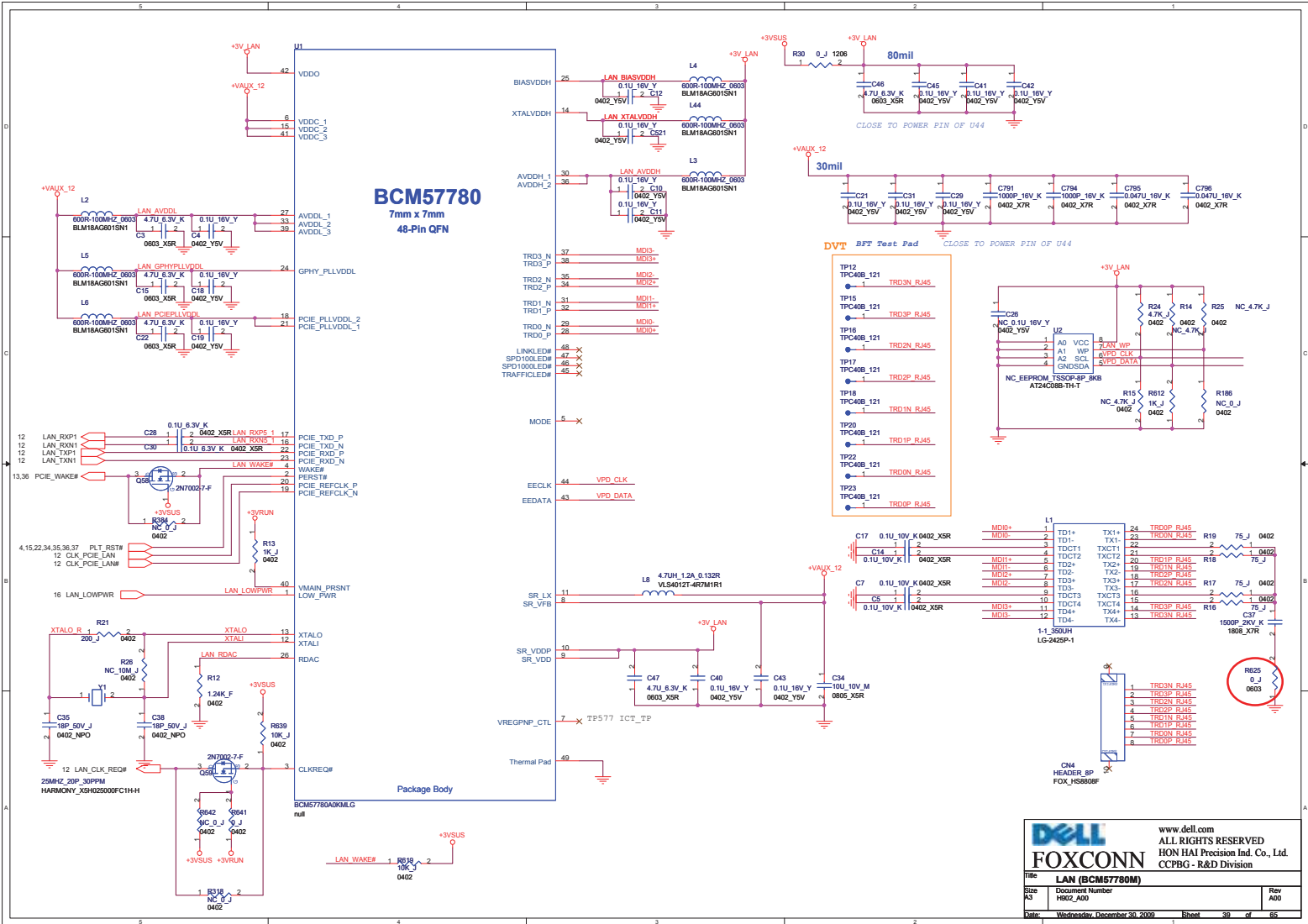


Camera & Digi MIC

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BT & CAMERA/Dig MIC CON

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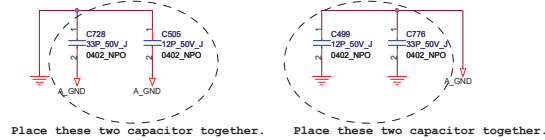
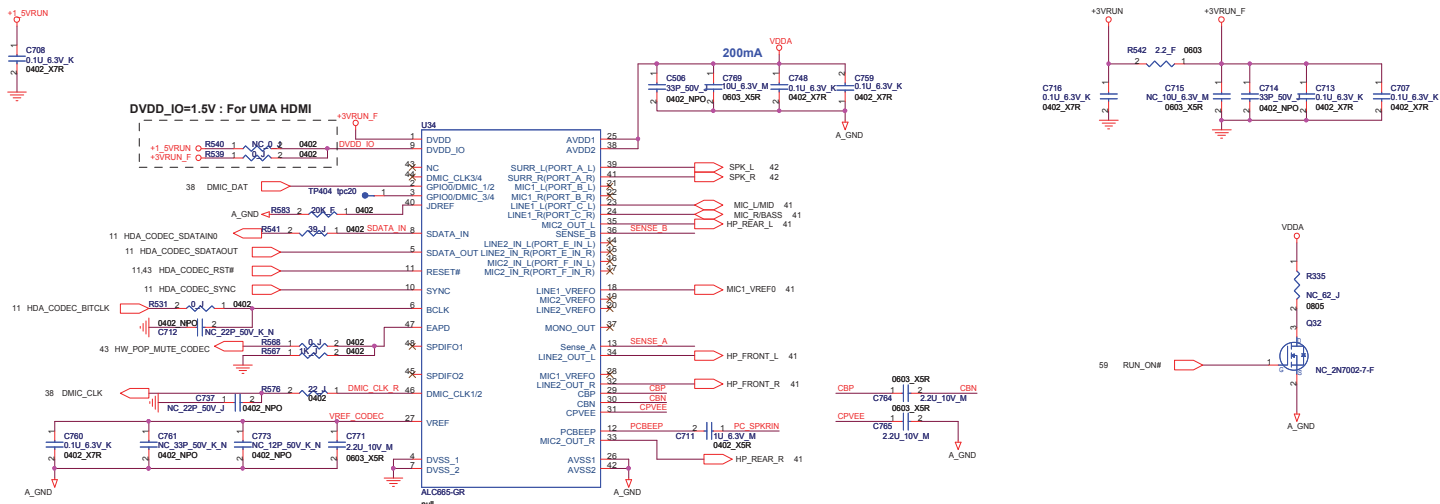
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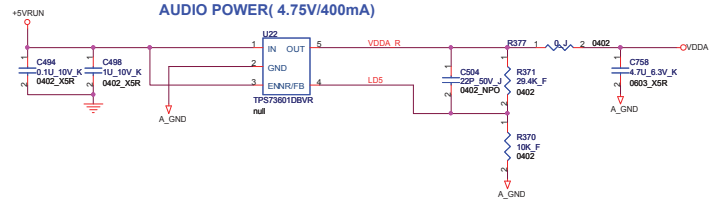
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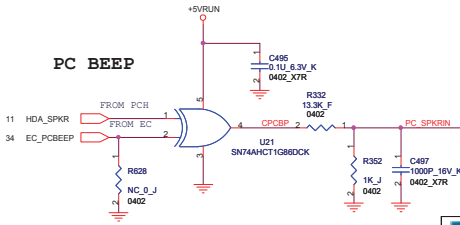
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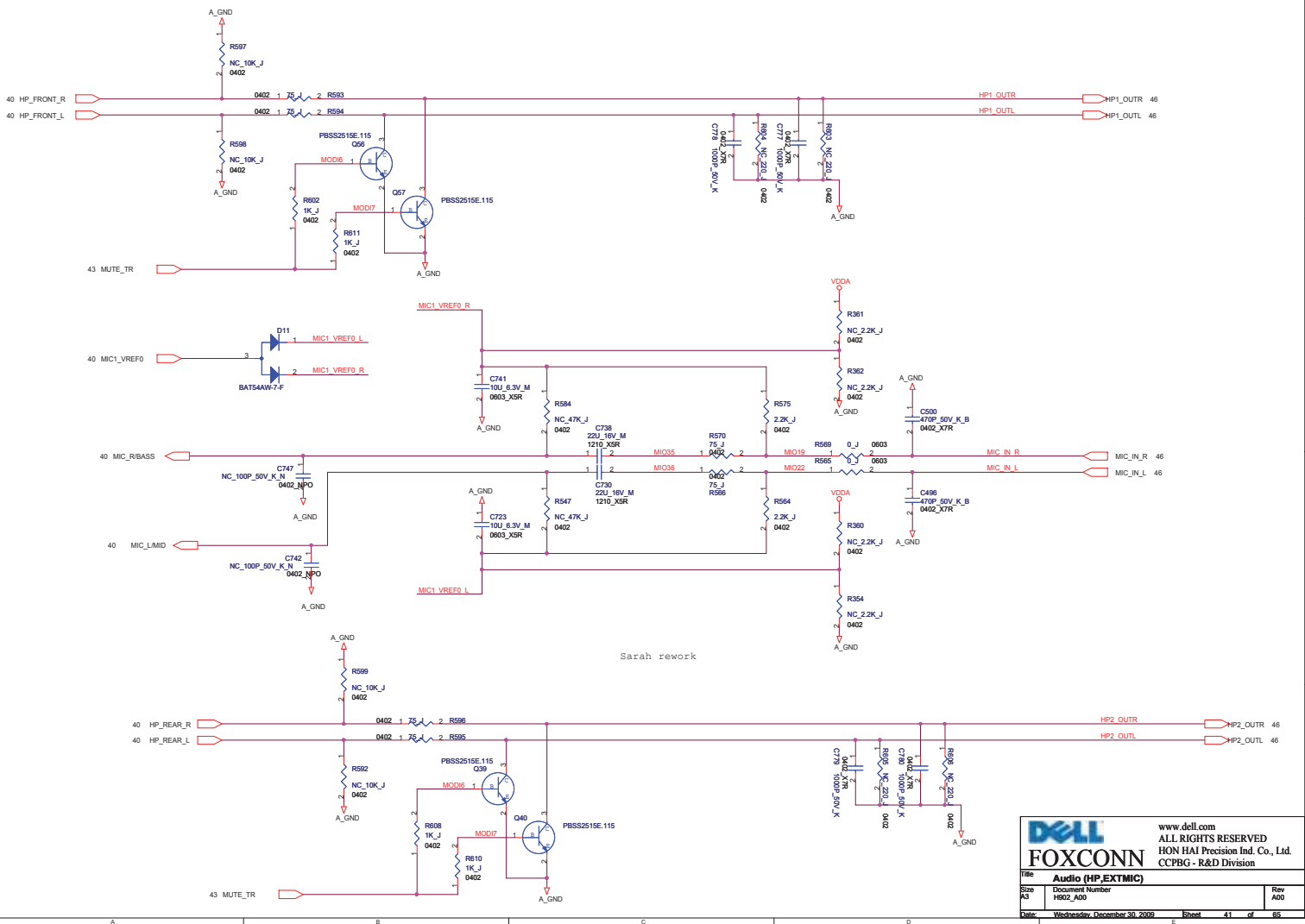
AUDIO POWER (4.75V/400mA)



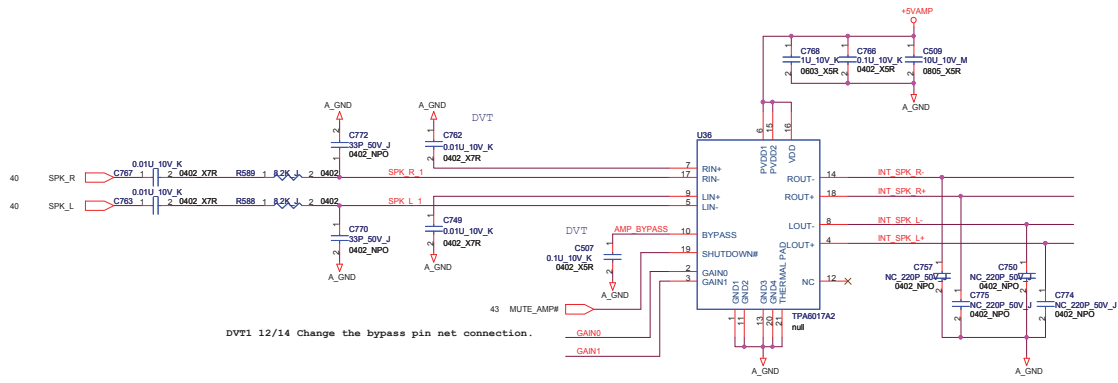
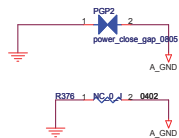
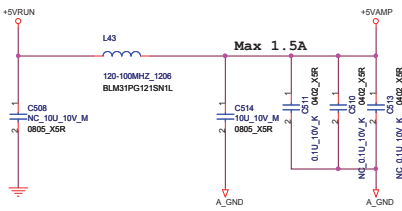
PC BEEP



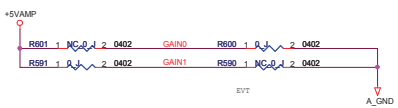
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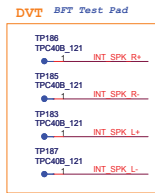
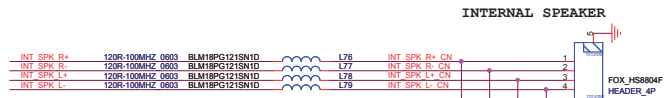
DVT1 12/14 Change the bypass pin net connection.



SPEAKER AMP

	GAIN0	GAIN1
6 dB	0	0
10 dB	0	1
15.6 dB	1	0
21.6 dB	1	1

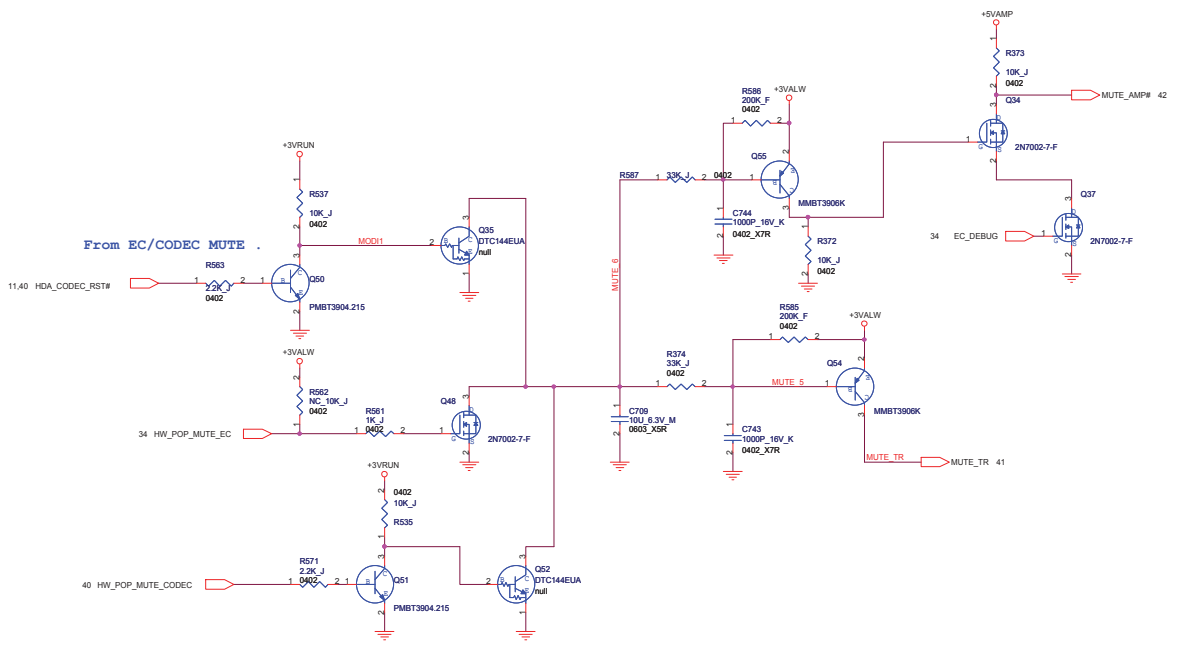
$dB = 20 \log Gain$
 If set 10dB, gain is 3.162.
 $P_o = \{(1.2V_{rms} * 3.162)^2\} / 4 = 3.599 W$



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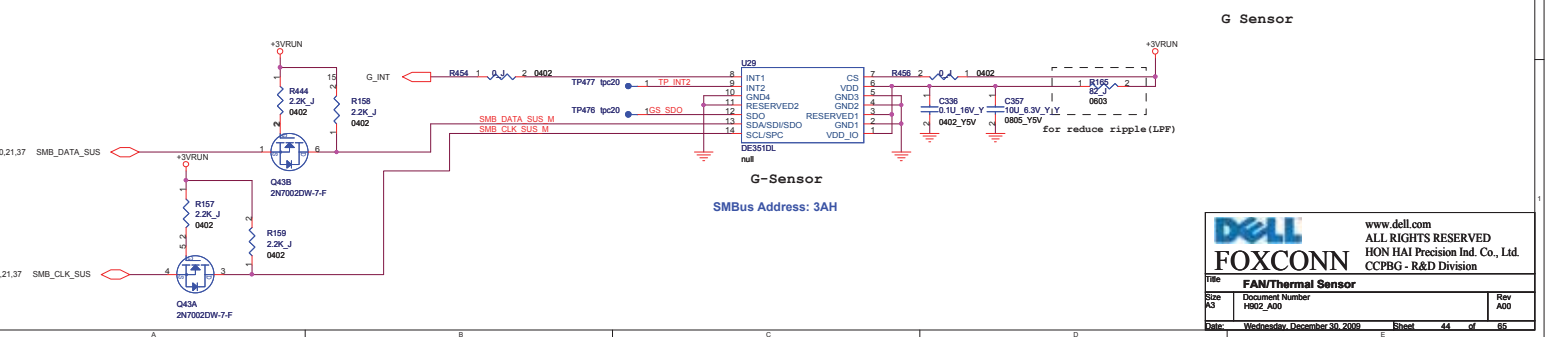
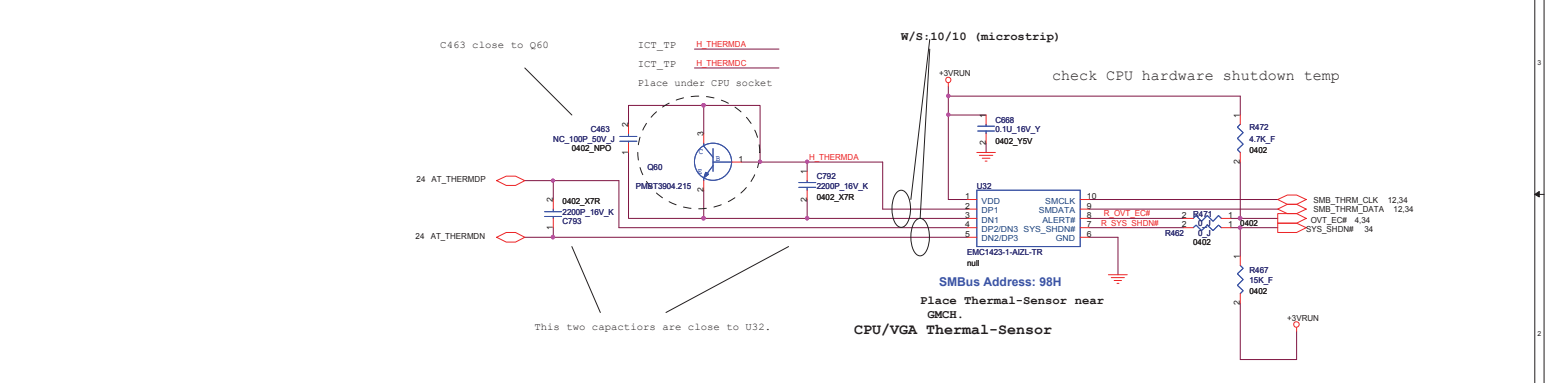
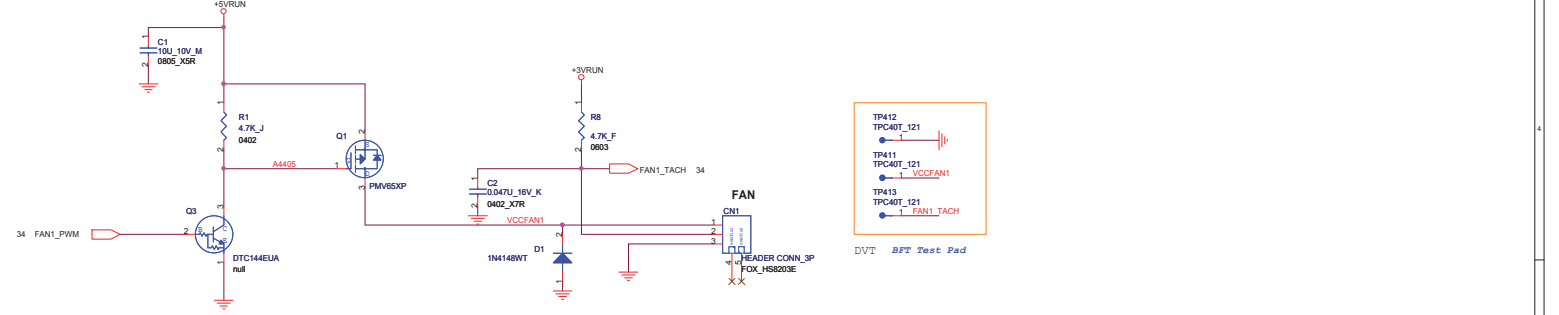
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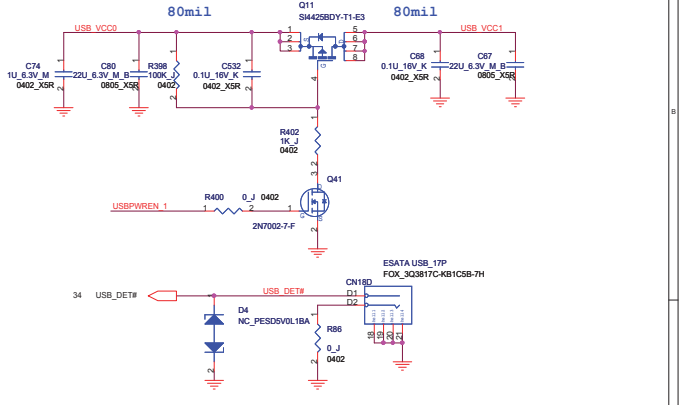
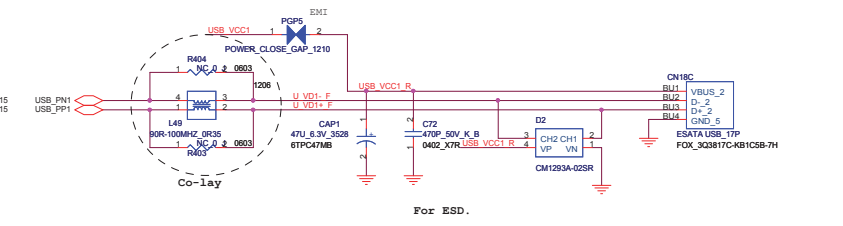
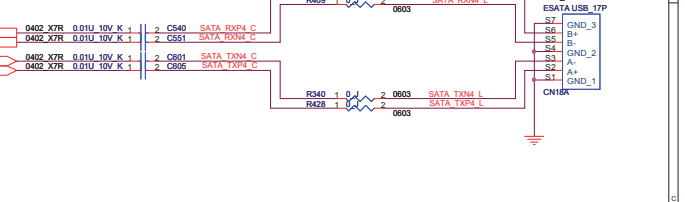
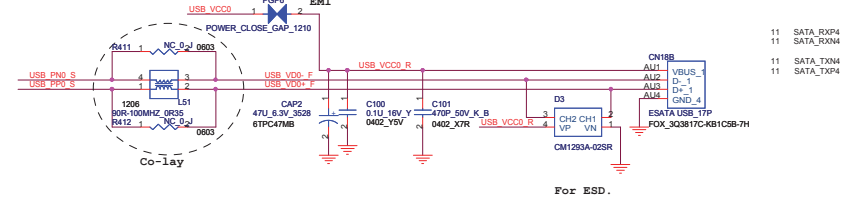
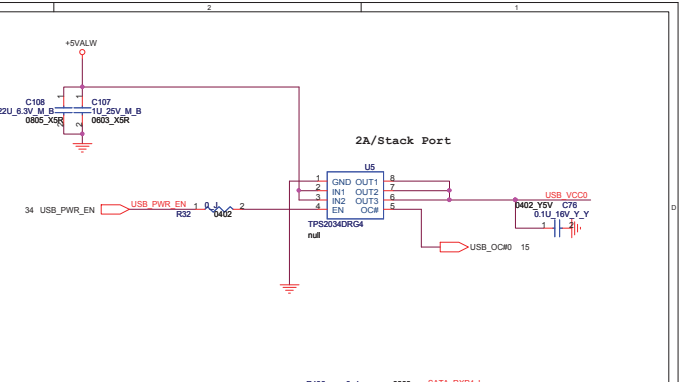
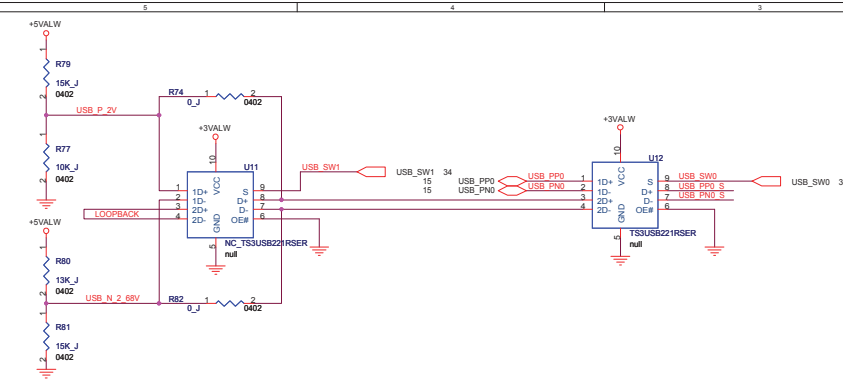


DELL
FOXCONN

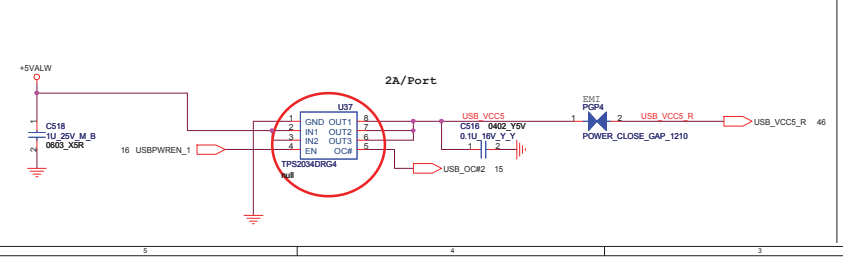
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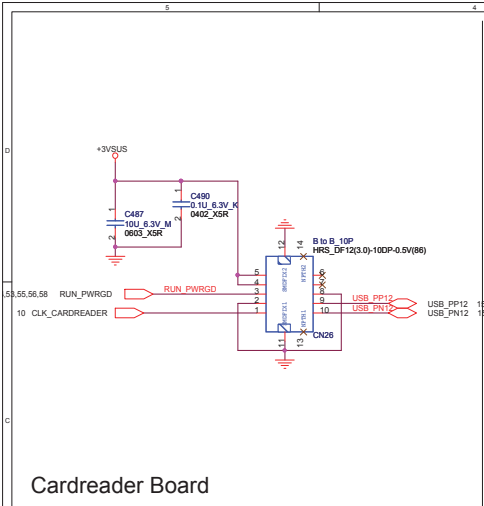
USB + e-SATA on MB



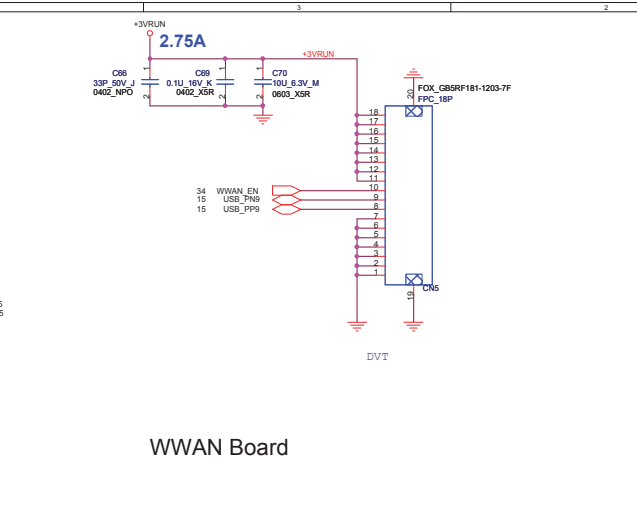
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Title: USB2.0 & e-SATA		
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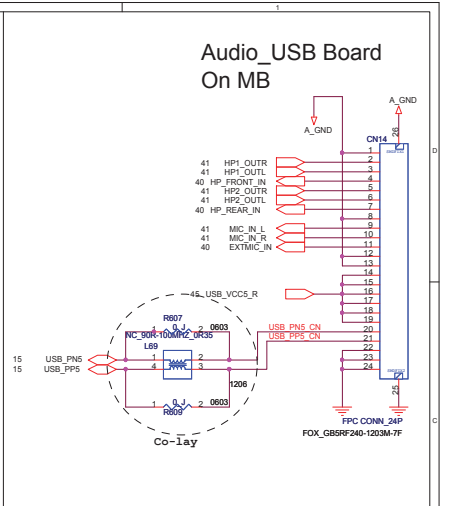
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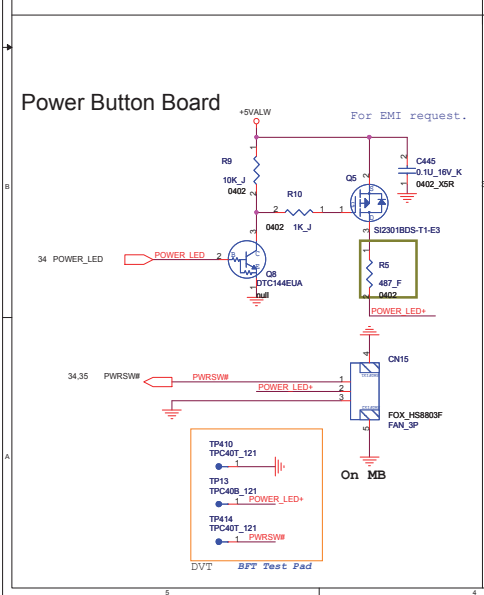
Cardreader Board



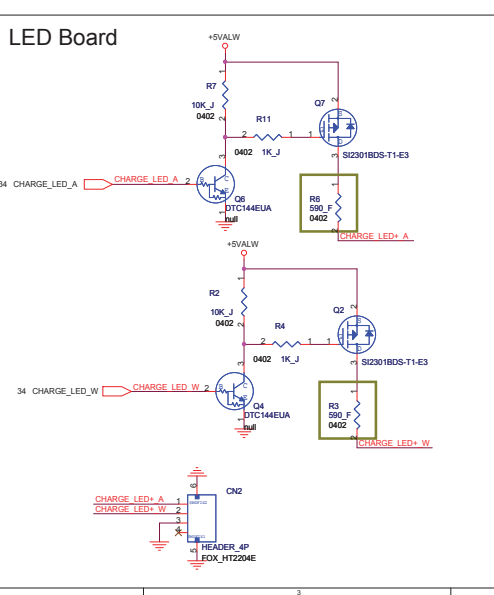
WWAN Board



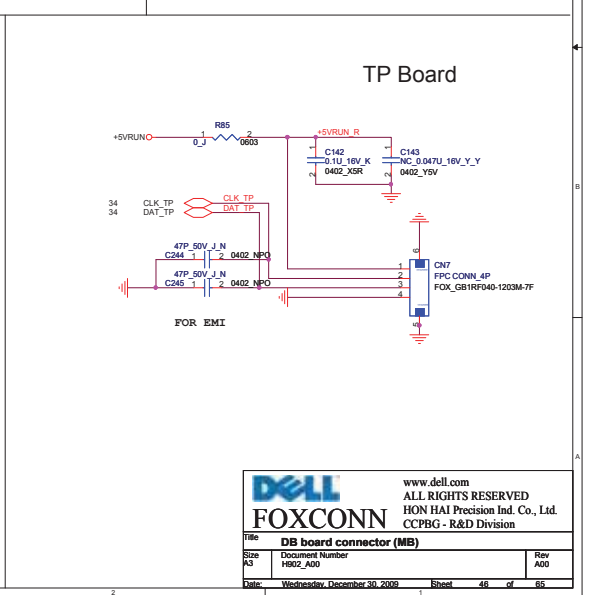
Audio_USB Board On MB



Power Button Board



LED Board



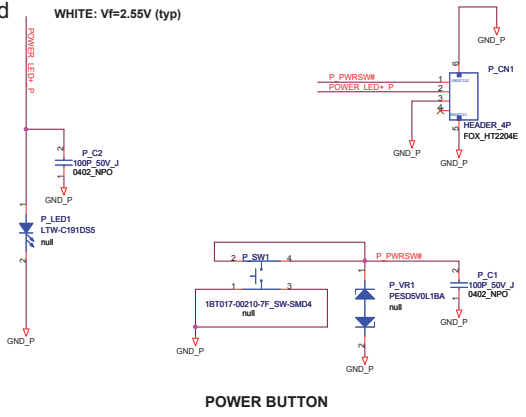
TP Board

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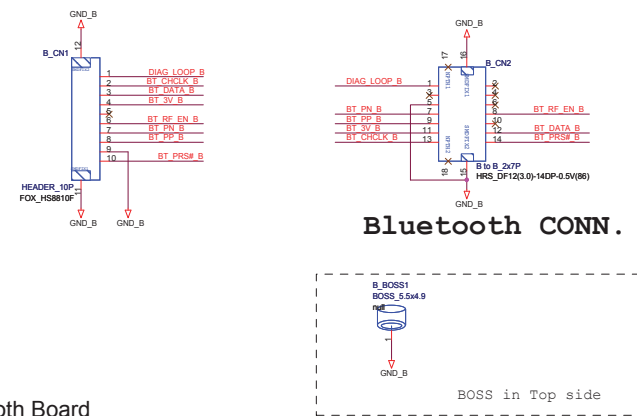
DB board connector (MB)

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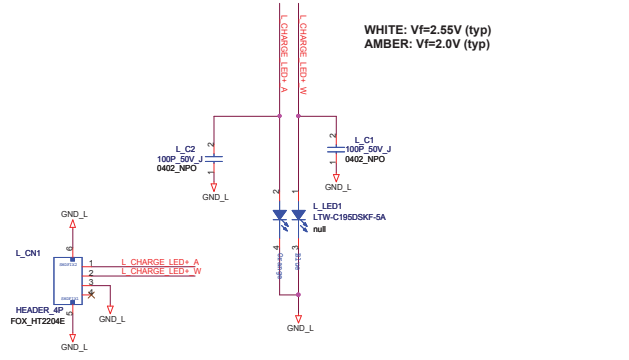
Power Button Board



Bluetooth Board



LED Board



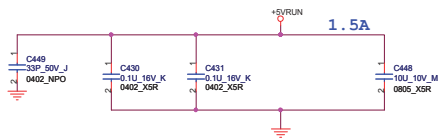
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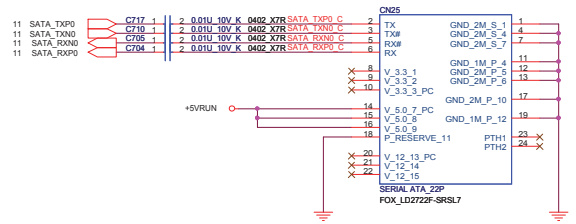
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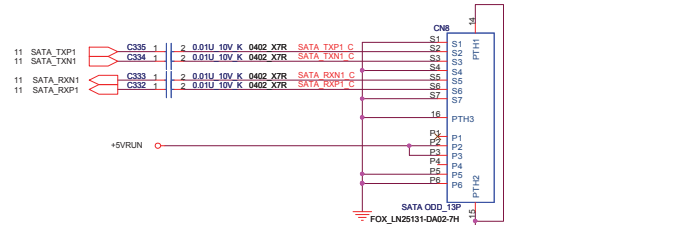
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SATA HDD CONN

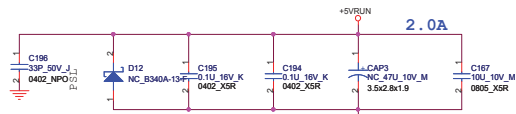


SATA ODD CONN



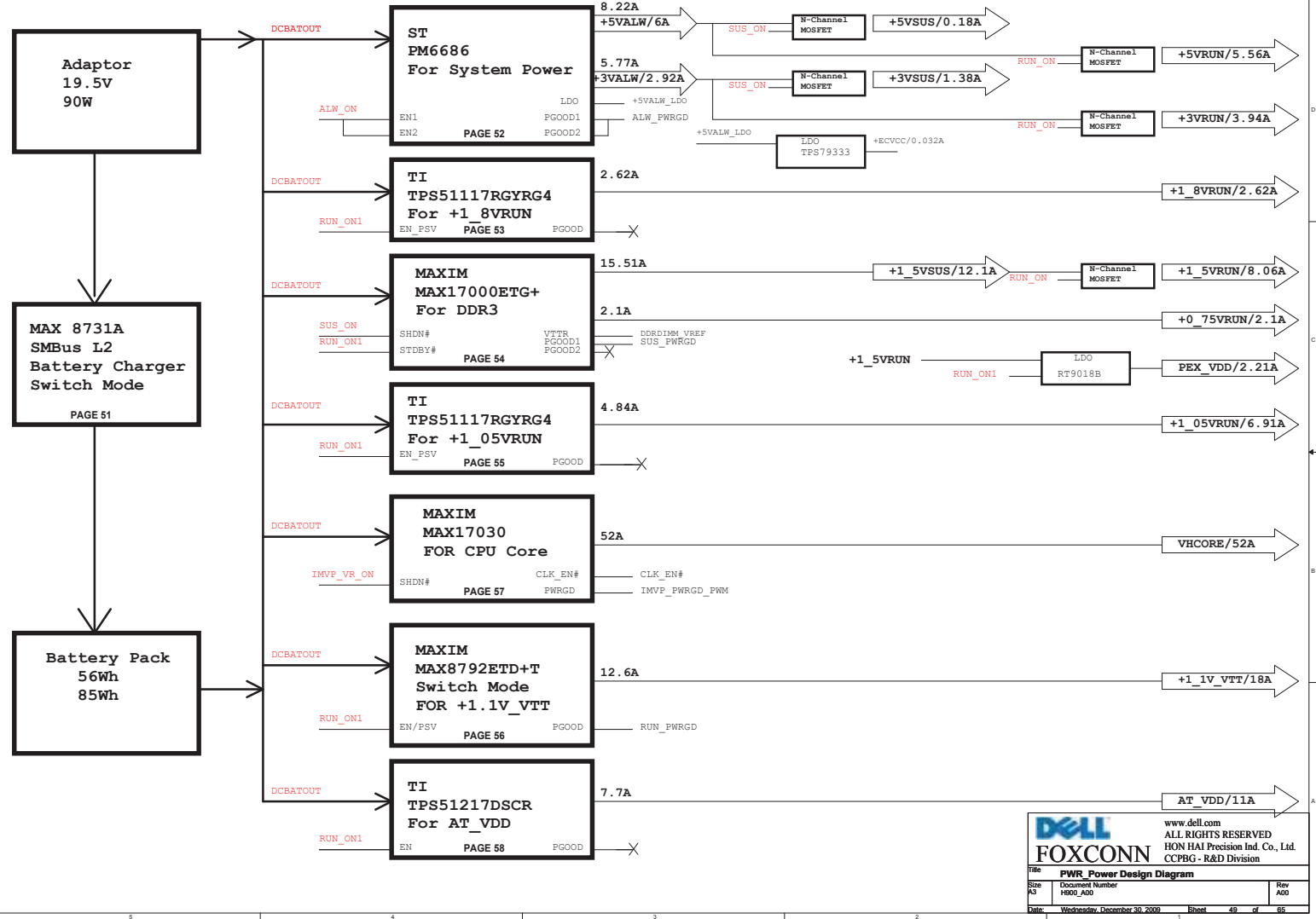
ODD CON ADAPTER

Add CN68 need 2N-0013009-FRG0 in BOM



Consider to change to Flash board connector.

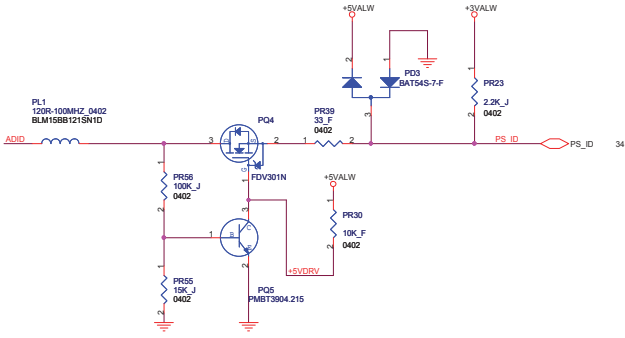
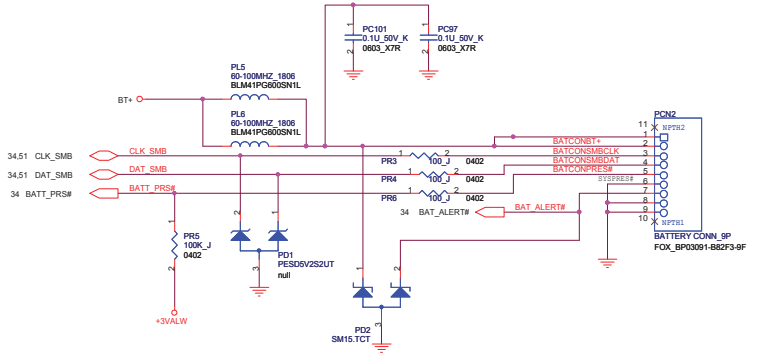
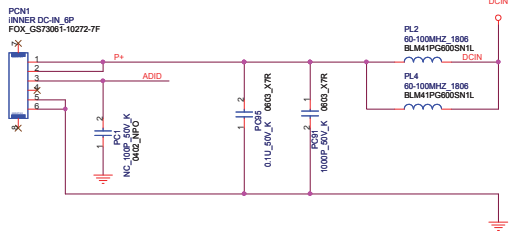
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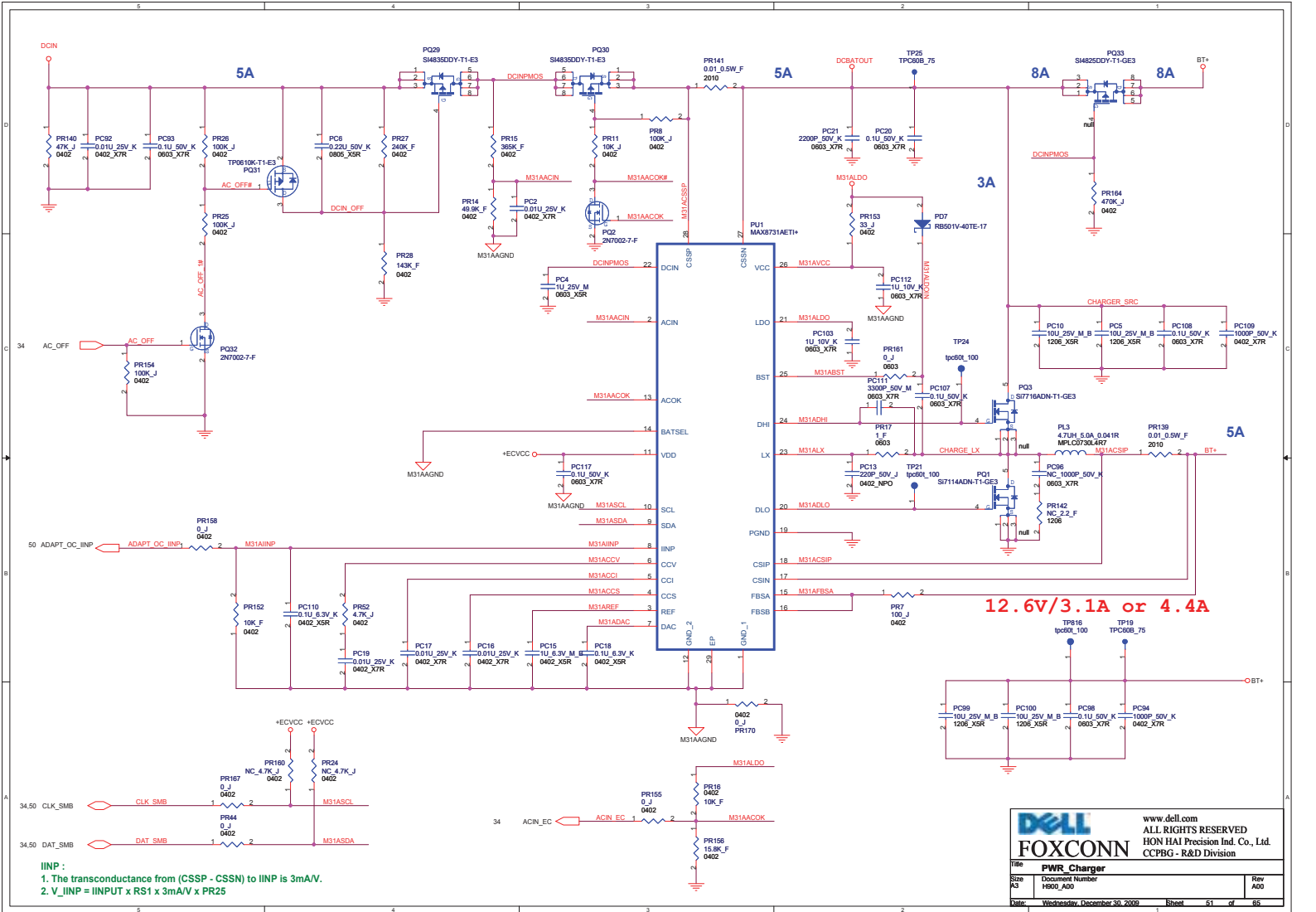
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Title: PWR DCIN & Battery			
Size: A3	Document Number: H800_A00	Rev: A00	
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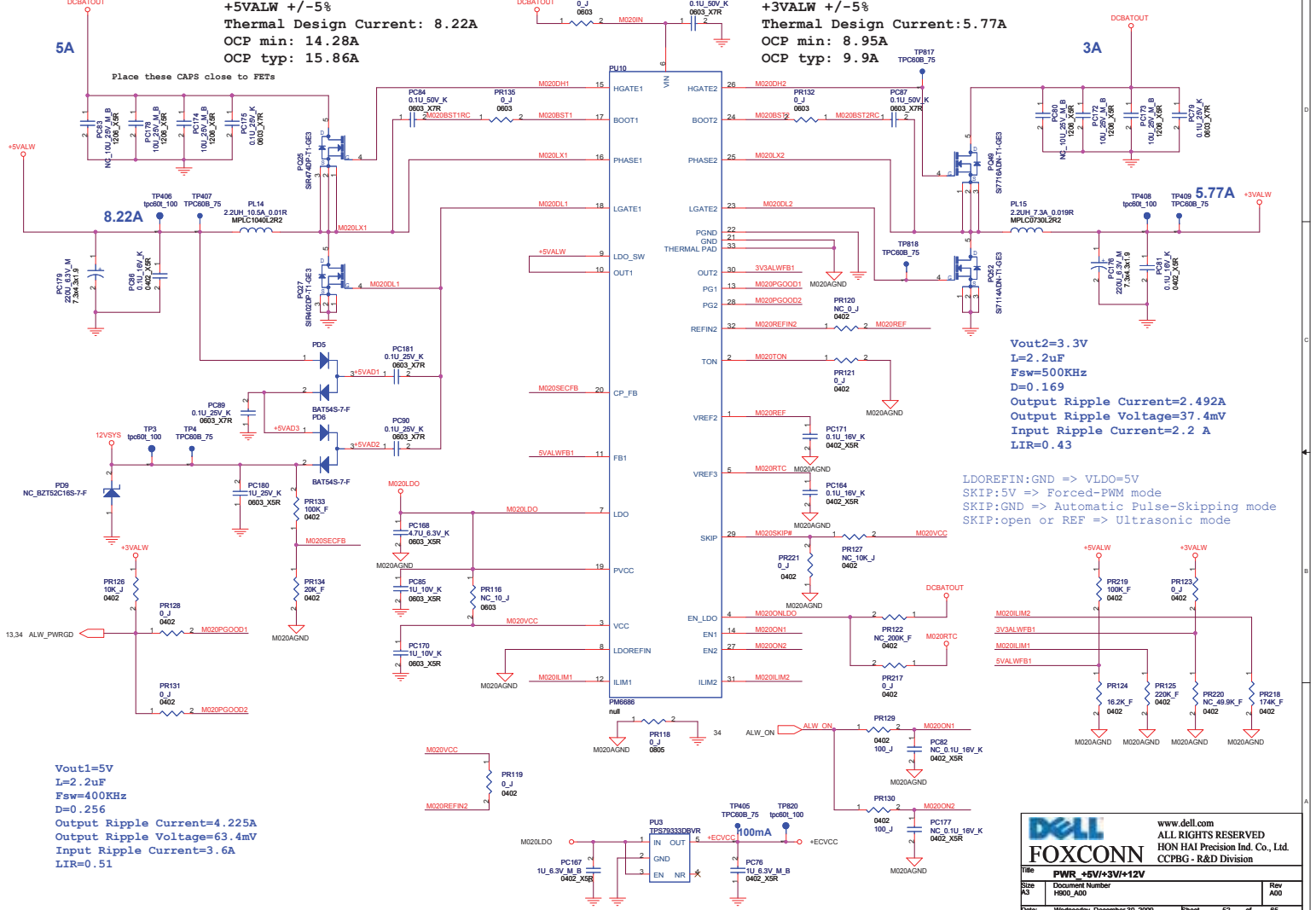
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<http://laptop-motherboard-schematic.blogspot.com/>

+5VALW +/-5%
Thermal Design Current: 8.22A
OCp min: 14.28A
OCp typ: 15.86A

+3VALW +/-5%
Thermal Design Current: 5.77A
OCp min: 8.95A
OCp typ: 9.9A

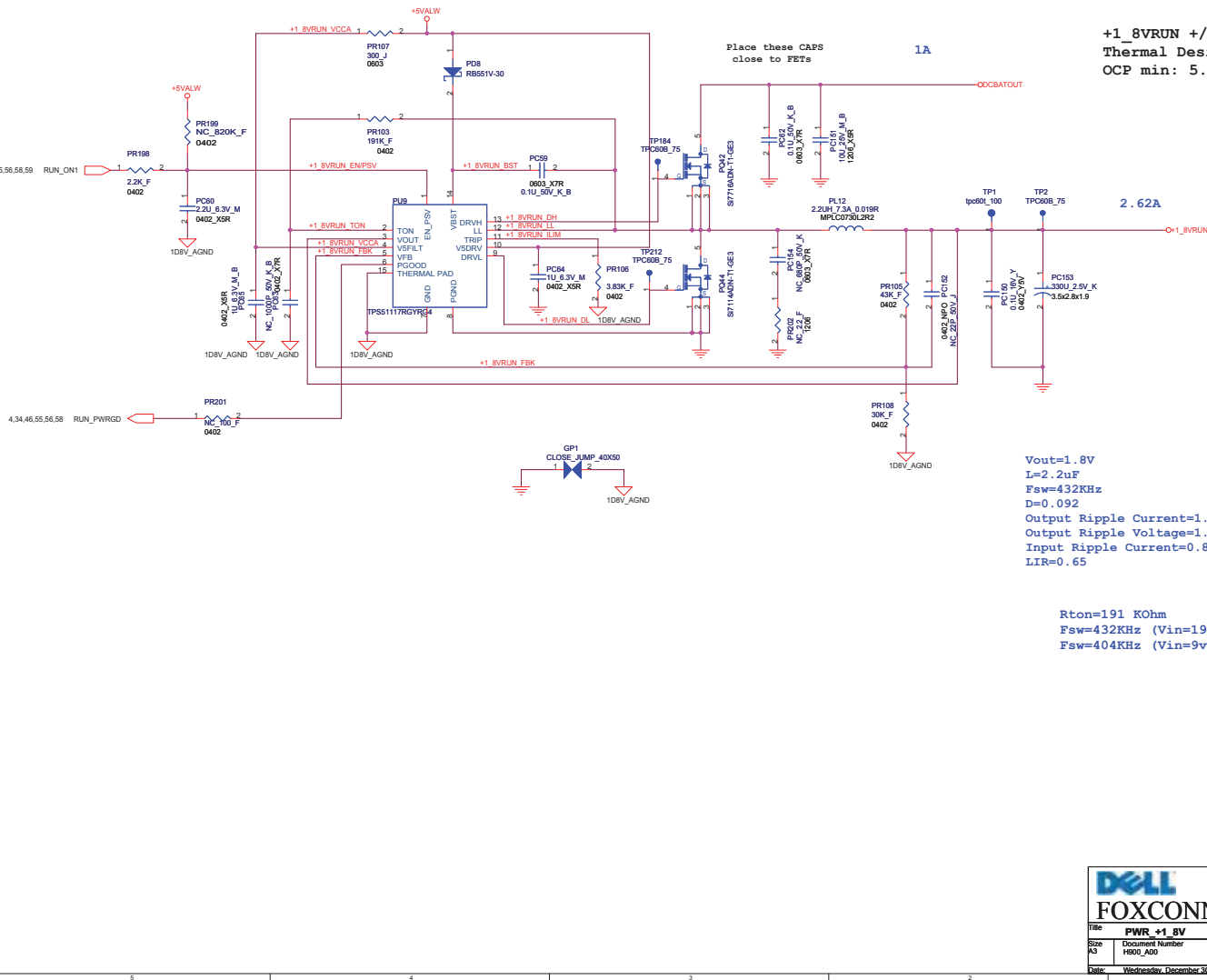


Vout2=3.3V
I=2.2uF
Fsw=500KHz
D=0.169
Output Ripple Current=2.492A
Output Ripple Voltage=37.4mV
Input Ripple Current=2.2 A
LIR=0.43

LDOREFIN:GND => VLDO=5V
 SKIP:5V => Forced-PWM mode
 SKIP:GND => Automatic Pulse-Skipping mode
 SKIP:open or REF => Ultrasonic mode

Vout1=5V
L=2.2uF
Fsw=400KHz
D=0.256
Output Ripple Current=4.225A
Output Ripple Voltage=63.4mV
Input Ripple Current=3.6A
LIR=0.51

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		Title: PWR -+5V/+3V/+12V	Document Number: H800_A00
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+1.8VRUN +/-5%
Thermal Design Current: 2.62A
OCp min: 5.08 A

Place these CAPS
close to FETs

1A

2.62A

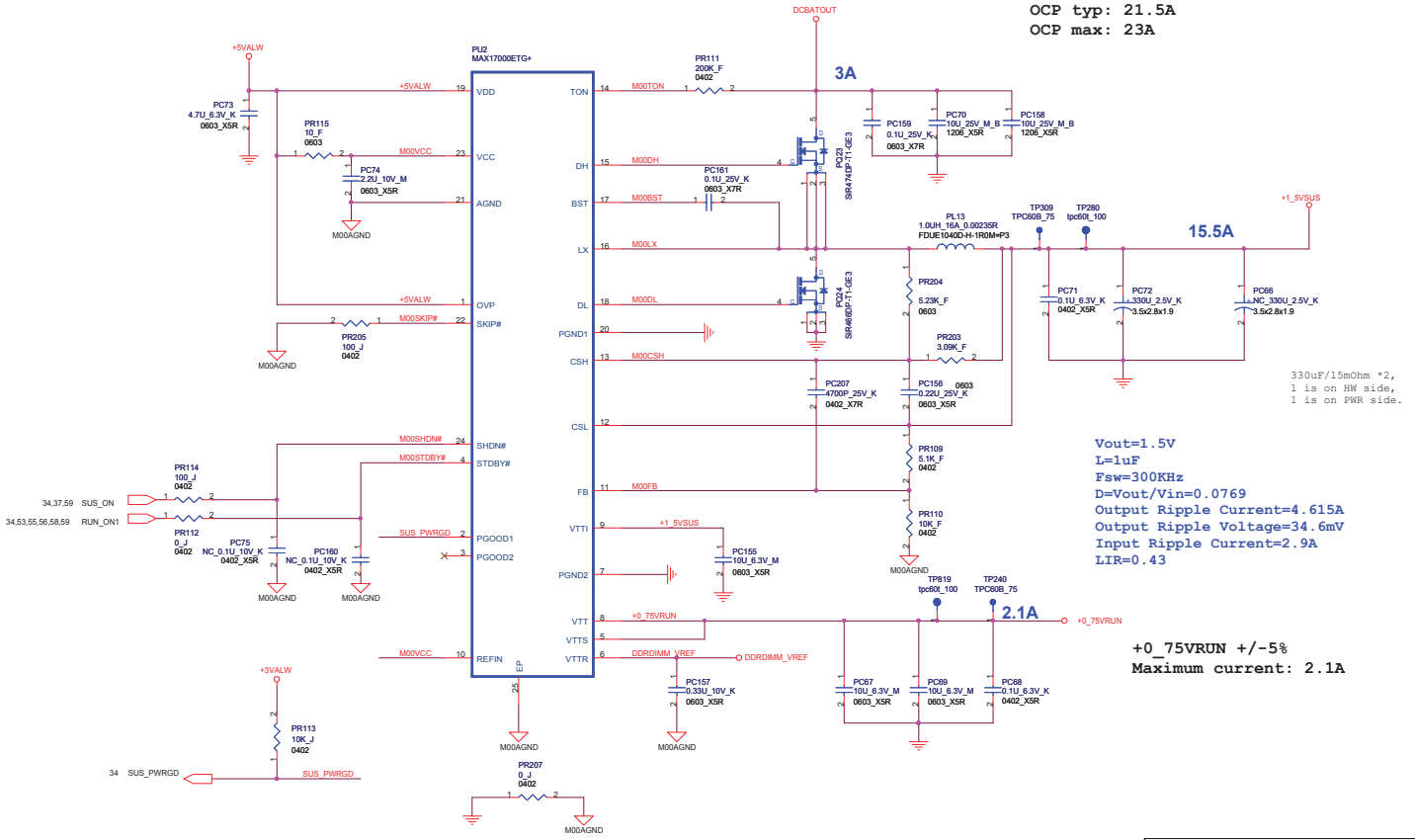
$V_{out}=1.8V$
 $L=2.2\mu F$
 $F_{sw}=432KHz$
 $D=0.092$
Output Ripple Current=1.719A
Output Ripple Voltage=1.719A*15mOhm=25.78mV
Input Ripple Current=0.8A
LIR=0.65

$R_{ton}=191\text{ KOhm}$
 $F_{sw}=432KHz$ ($V_{in}=19.5V$)
 $F_{sw}=404KHz$ ($V_{in}=9V$)

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Title: PWR +1.8V			
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+1_5VSUS +/-5%
 Thermal Design Current: 15.5A
 OCP min: 20.3A
 OCP typ: 21.5A
 OCP max: 23A

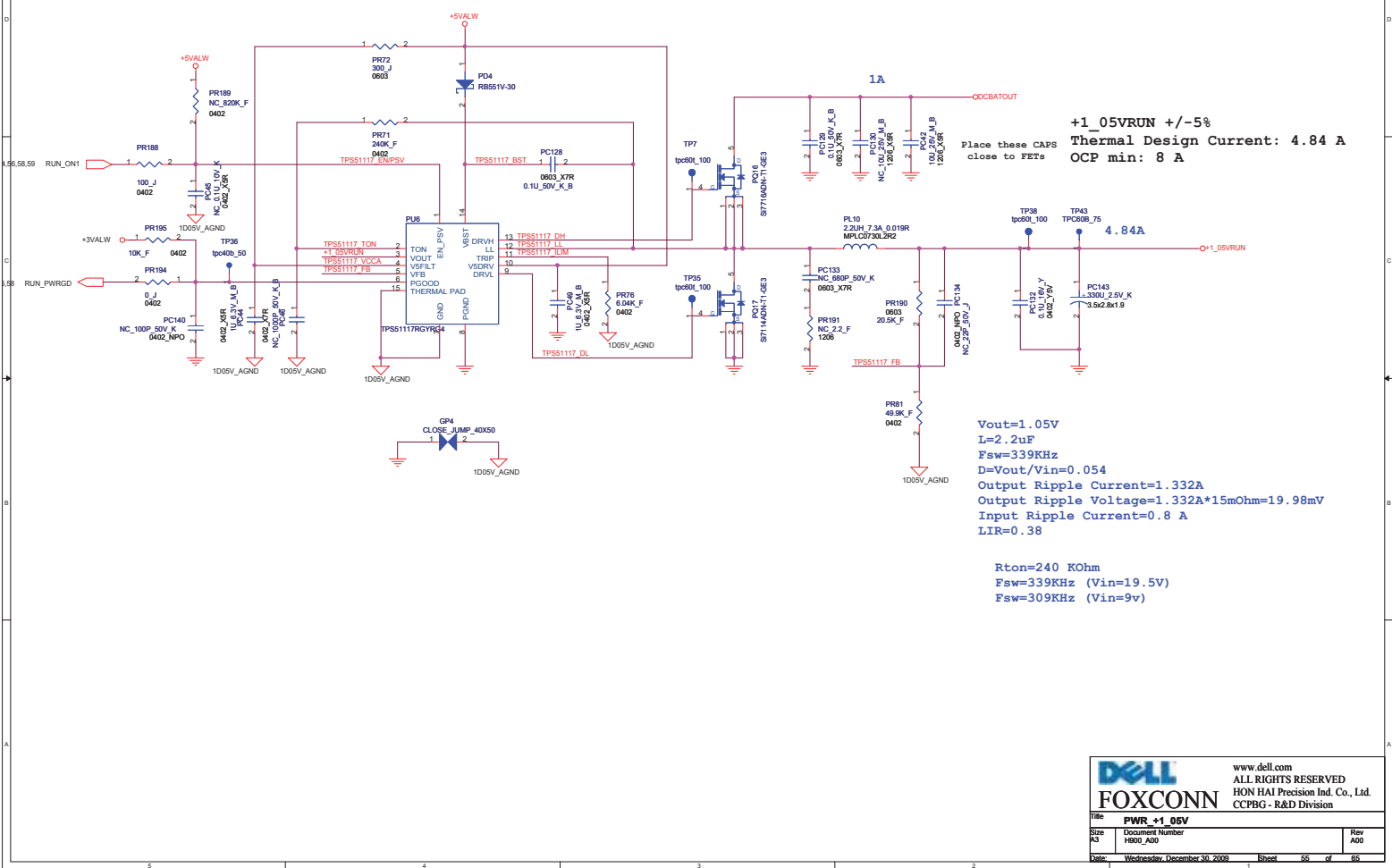


Vout=1.5V
 L=1uF
 Fsw=300KHz
 D=Vout/Vin=0.0769
 Output Ripple Current=4.615A
 Output Ripple Voltage=34.6mV
 Input Ripple Current=2.9A
 LIR=0.43

+0_75VRLN +/-5%
 Maximum current: 2.1A

330uF/15mOhm *2,
 1 is on HW side,
 1 is on PWR side.

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PWR +1_5V/+0_75V		
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+1_05VRUN +/-5%
Thermal Design Current: 4.84 A
OCp min: 8 A

Place these CAPS
close to FBZS

Vout=1.05V
I=2.2uF
Fsw=339KHz
D=Vout/Vin=0.054
Output Ripple Current=1.332A
Output Ripple Voltage=1.332A*15mOhm=19.98mV
Input Ripple Current=0.8 A
LIR=0.38

Rton=240 Kohm
Fsw=339KHz (Vin=19.5V)
Fsw=309KHz (Vin=9v)

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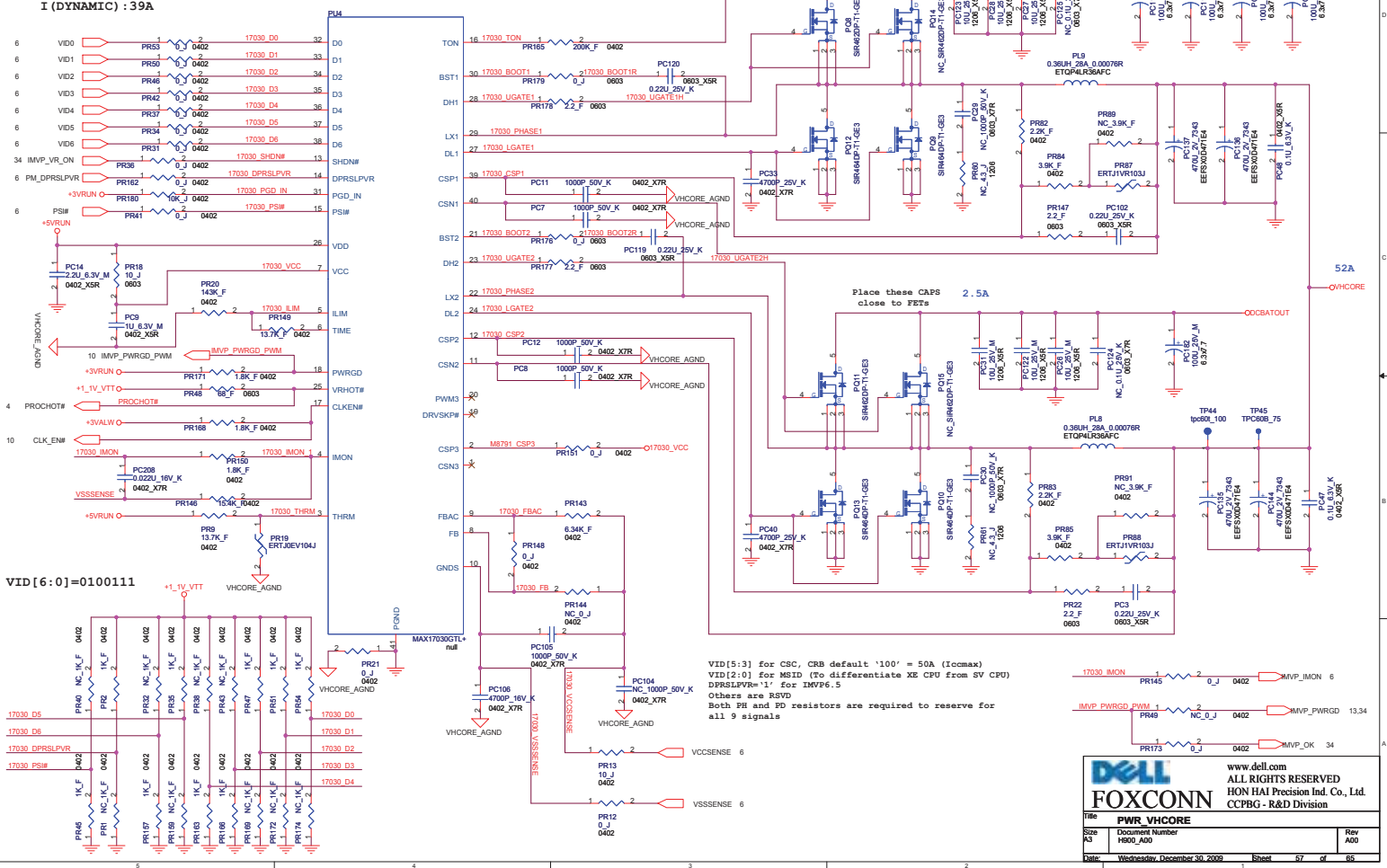
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PWR +1_05V		
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Clardsfield SV 45W CPU
 V(HFM): 0.95V
 V(LFM): 0.875V
 LL: -1.9mOhm
 I(HFM): 51A
 I(TDC): 38A
 I(DYNAMIC): 39A

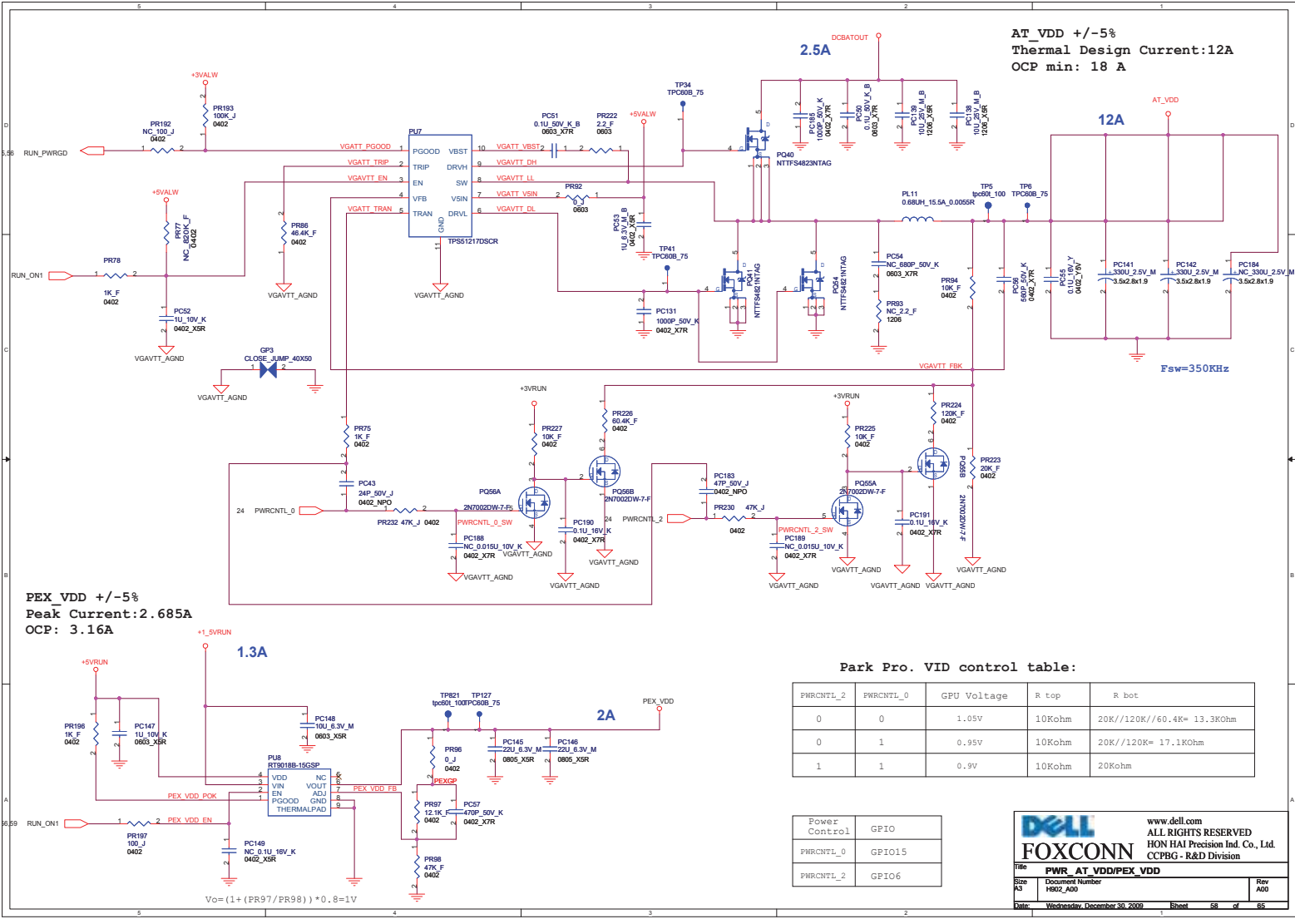
OCP setting: 61.7A (30.83A per phase).
 PR649=13.7K Ohm
 OCPmax: 65.6A
 OCPmin: 58.2A



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AT VDD +/-5%
Thermal Design Current:12A
OCP min: 18 A

PEX VDD +/-5%
Peak Current:2.685A
OCP: 3.16A

Park Pro. VID control table:

PWRCNTL_2	PWRCNTL_0	GPU Voltage	R top	R bot
0	0	1.05V	10Kohm	20K//120K//60.4K= 13.3Kohm
0	1	0.95V	10Kohm	20K//120K= 17.1Kohm
1	1	0.9V	10Kohm	20Kohm

Power Control	GPIO
PWRCNTL_0	GPIO15
PWRCNTL_2	GPIO6

DELL
FOXCONN

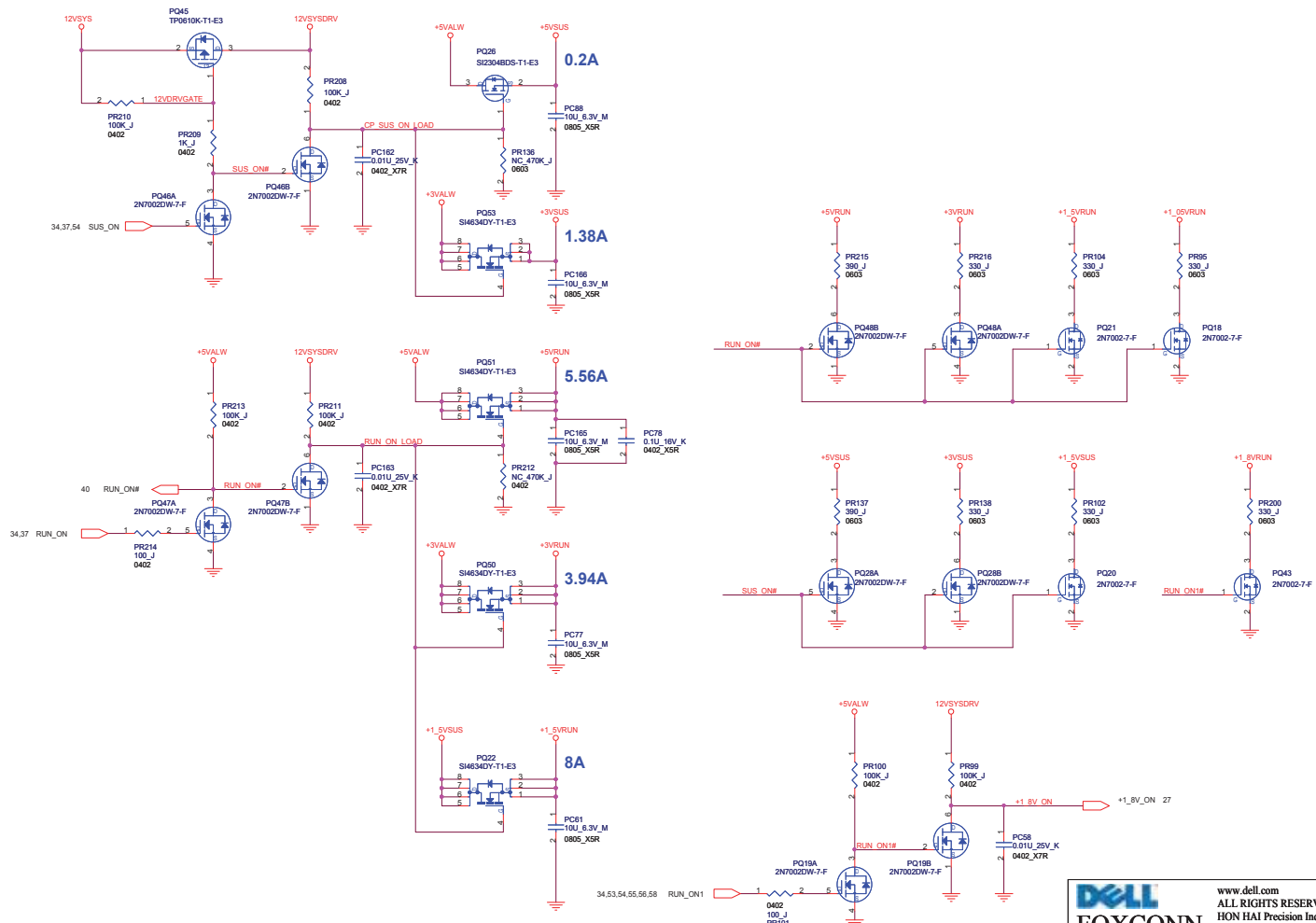
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Title: **PWR AT VDD/PEX VDD**

Size: A3 Document Number: H802_A00 Rev: A00

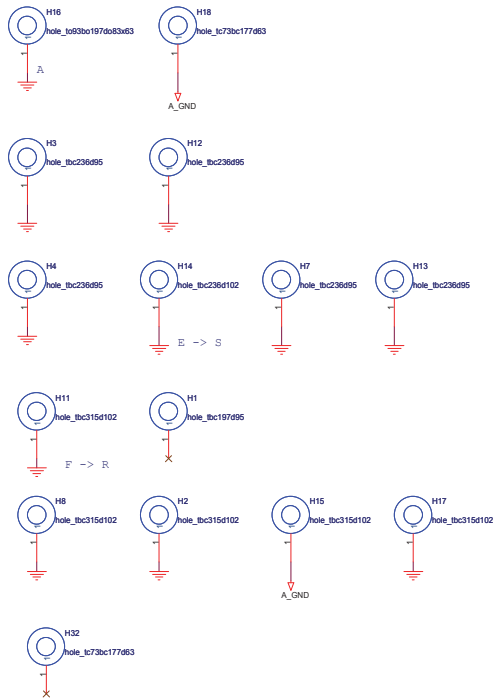
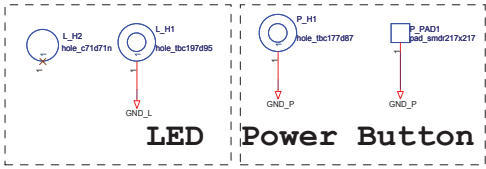
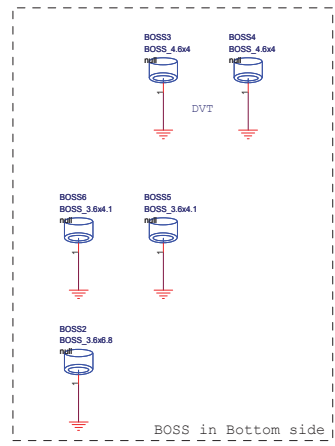
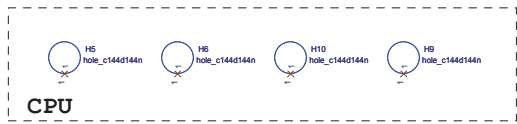
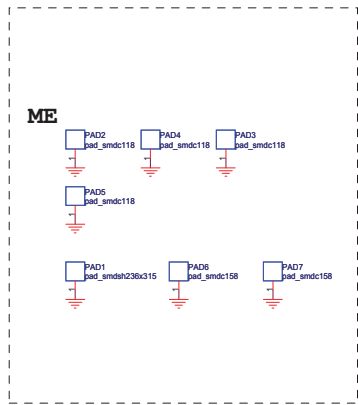
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$$V_o = (1 + (PR97/PR98)) * 0.8 = 1V$$



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		PWR Others power plane	
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H902 DVT

(2009/09/25)

- P.25 Change R139 & R143 from 100 ohm to 40.2 ohm for AMD recommend.
- P.24 Change AT_MEM ID0-3 connect to DVDDATA_0-3.
- P.26 Reserve R627 & R629 for reduce DPE/F_PLL.
- P.26 Add R630 & R631 to replace Bead L74, L75 and NC C667, C797, C798, C800, C799, C801 for AMD recommend.
- P.25 NC C273, C280, R127, R134 for AMD recommend.


H902 PVT

(2009/11/03)

- P.22-27 Change U26 HHPN to 12-2160774-0002.
- P.17 Change L35, L37, L66, L67 to 1L-DML2201-2M00 for PUR recommend.
- P.20 Change C364 to 1C-2B20104-K301 for PUR recommend.
- P.31 Change C263 to 1C-2B20104-K301 for PUR recommend.
- P.34 Change C457, C732, C502, C489, C703, C476, C486, C503, C718 & C739 to 1C-2B20104-K301 for PUR recommend.
- P.35 Change C319 to 1C-2B20104-K301 for PUR recommend.
- P.37 Change C485 & C488 & C725 to 1C-2B20104-K301 for PUR recommend.
- P.45 Change C68 & C532 to 1C-2B20104-K301 for PUR recommend.
- P.46 Change C69 & C142 to 1C-2B20104-K301 for PUR recommend.
- P.46 Change C194, C195, C430 & C431 to 1C-2B20104-K301 for PUR recommend.

(2009/11/18)

- P.46 Add C445 0.1uF for EMI recommend.
- P.33 Change CN11 for ME recommend.

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H900 EVT -> DVT

(2009/03/26)

- P.47 Add BT2(CSR) BC_BOSS1 NC for reserve.
- P.32 Change LVDS connector pin define switch Pin4 and Pin10. (Pin4 NC, Pin10 +3VRUN)
- P.47 Add BT2(CSR) BC_BOSS1 NC for reserve.

(2009/03/27)

- P.46 Modify WWAN CN5 pin define.
- P.32 LVDS CN, change +3VRUN to pin 4, pin3 to NC prevent DCBATOUT short to +3VRUN.

(2009/03/31)

- P.42 Change R588,R589 to 8.2K ohm for 1.5W speaker.

(2009/04/01)

- P.40 Change R332 to 13.3K for Realtek recommend.
- P.24 Reserve R382, R383, R617 and R293 0 ohm for Park.
- P.24 Reserve L71, C785 1uF, C786 10uF, C787 0.1uF, L70, C782 1uF, C783 10uF, C784 0.1uF for Park.
- P.24 Reserve R619, R620 0 ohm for Park.
- P.27 Add R622 0 ohm for saperate Park schematics.
- P.27 Reserve R618 and R621 0ohm, C512 1uF, C515 10uF, and L72 for Park.

(2009/04/02)

- P.26 Reserve L73, C788 1uF, C789 10uF, C790 0.1uF and R623 0ohm for Park.

(2009/04/03)

- P.27 Reserve R624 150 ohm, R627 0 ohm for Park.
- P.27 Add R625,R626 0 ohm for Park.

(2009/04/06)

- P.11 Stuff R495 for Flash SPI.

(2009/04/10)

- P.11 Change PCH SPI_CS# to SPI_ROM_CS#.
- P.34 Change H_PWRGD to H_CPUPWRGD.

(2009/04/13)

- P.40 Reserve R628 0 ohm for PC beep.
- P.42 Change R45,R47,R49,R50 to bead L76,L77,L78,L79 for EMI request.
- P.24 Change L19 to BLM18BB121SN1D to solve AT_DPLL_PVDD Vpp over spec issue.
- P.32 Change F8 to 467002 (32V-2A_0603) for LVDS VCC protection.
- P.47 Del BC_CN4,BC_CN3,BC_BOSS1,BC_TP1,BC_TP2 for BT2 board is not necessary.
- P.42 Change C767,C763,C762,C749 to 0.01uF; C507 to 0.1uF for speaker pop noise.
- P.32 Del R29 0ohm for no necessary.
- P.36 Del R27 0ohm for no necessary.
- P.45 Change R384, R34, R52 to close gap PGP4,PGP5,PGP6.
- P.45 Change F5,F1 to close gap PGP7,PGP8 for un-necessary.
- P.22 Change R410 0ohm to close gap PGP12.
- P.26 Change R92,R93 0ohm to close gap PGP13,PGP14.
- P.36 Change R391 0ohm to close gap PGP17.

(2009/04/15)

- P.39 Add D15, D16 for solving leakage issue.

(2009/04/23)

- P.4 Del R196 0ohm for no necessary.

(2009/04/24)

- P.4 Add CPU DET# for Dell PC Beep.

(2009/04/27)

- P.4 Change R184 to 1.1K ohm R182 to 3.01K ohm for Intel recommend.

(2009/04/28)

- P.36 Del R27 0 ohm for DVT.
- P.41 Change R602, R611, R608, R610 to 1k ohm for Audio headphone noise.
- P.45 Add F1 and F5 for protection and del PGP7 and PGP8.

(2009/04/30)

- P.6 Del R401, R115 for Vcore power plane.
- P.38 Change TP29, TP46, TP42, TP40, TP39, TP428, TP430 to TPC40B_121.
- P.50 Change TP8, TP11, TP14, TP10, TP9 to TPC60B_121.
- P.44 Change TP412, TP411, TP413 to TPC40T_121.
- P.39 Change TP12, TP15, TP16, TP17, TP18, TP20, TP22, TP23 to TPC40B_121.
- P.42 Change TP186, TP185, TP183, TP187 to TPC40B_121.
- P.34 Change TP480, TP485, TP329, TP479, TP483, TP182, TP333, TP128 to TPC40T_121.
- P.46 Change TP414, TP410 to TPC40T_121 and TP13 to TPC40B_121.
- P.38 Change TP47, TP422, TP417, TP37, TP30, TP33, TP32, TP31, TP28 to TPC40B_121.
- P.11 Change C736 to 15pF for crystal vendor recommend.
- P.39 Change C35 and C38 to 18pF for crystal vendor recommend.
- P.34 Del Q28 and R318 2.2k ohm for CPU PC Beep solution .

(2009/05/5)

- P.32 Change C65 to 6800pF for LVDS sequence.
- P.39 Reserve R318 and R384 0 ohm for leakage solution.
- P.45 Change F1 and F5 to 1M-F08V05A-0000.

(2009/05/8)



- P.16 Reserve R391 1K ohm for following the CRB.
- P.7 Del R55 0 ohm for leakage.
- P.35 Change U13 to W25X80A.
- P.31 Change L61, L62, L63 to 33R100MHz for CRT SI issue.

(2009/05/11)

- P.17 Change C479 to 1uF for Intel recommend.
- P.24 Reserve R410 and R629 0 ohm for Park.
- P.24 Reserve R634, R631, R632, and R633 0 ohm for Park.
- P.24 Del R619 and R620 0 ohm for Park NC.
- P.25 Change C781 to 1nF for AMD recommend.
- P.25 Reserve R630 680 ohm and R115 10K PD for Park.
- P.27 Reserve R635 0 ohm for Park.
- P.25 Add TP172, TP173, TP174, TP175, TP176 and TP177 for Layout request.
- P.60 Change BOSS3 and BOSS4 for ME request.
- P.17 Del C445 and C463 33pF for unused.
- P.36 Del R27 0 hom for unused.
- P.45 Del F1, F5, and R31 0 ohm for unused.
- P.46 Del F2 for unused.

(2009/05/12)

- P.46 Reserve R637 and R638 0 ohm for WWAN change.
- P.46 Add R636 0 ohm for WWAN change.
- P.13 Add R92 and R93 1k ohm for Intel recommend.

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H900 EVT -> DVT

(2009/05/13)

P.25 Add R196 0 ohm and change R630 68 ohm to DRAM_RST pin for AMD recommend.

(2009/05/14)

P.12 Add R620 0 ohm to GND in Xtal_in for Intel recommend.
P.7 Del R407, R399, and R405 0 ohm for 1.1VTT power plane.

(2009/05/20)

P.4 Change R173 to NC for un-used.
P.27 Change C208 from 0.22u 10V to 0.22u 16V for derating issue.
P.17 Stuff R268 0 ohm to GND for disable Intel internal LAN.

(2009/05/22)

P.17 Change R237 and R265 from 0603 to 0805 for derating.
P.27 Change R146 from 0805 to 1206 for derating.

(2009/05/25)

P.17 Change CAP5 and CAP6 from 35m ohm ESR to 45m ohm ESR.

(2009/06/06)

P.39 Add Q58, Q59, R619, and R639 10K ohm and del D15 & D16 for leakage issue.
P.6 Add R401 0 ohm and Add R399, R405, R407, R640 1K ohm NC for C-state debugging.

(2009/06/16)

P.6 Add R641 & R642 0 ohm for controlling LAN_CLK_REQ# turn on voltage.
P.34 Add R643 & R644 0 ohm for debugging white screen issue.

(2009/06/25)

P.11 Change RTC battery P/N from 1M-BCR2032-LB00 to 1M-BCR2032-LB01.

(2009/07/01)

P.60 Add H32 for ME request.

(2009/07/14)

P.12 Add R645 & R646 2.2K ohm for SMBUS PH.

(2009/07/20)

P.38 Change C33 and C44 from NPO 10% to 5% for PUR recommend.
P.47 Change P_C1, P_C2, L_C1, L_C2 from 10pF NPO 10% to 5% for PUR recommend.
P.40 Change C499 and C505 from 12pF NPO 10% to 5% for PUR recommend.
P.11 Change C735 from 12pF NPO 10% to 5% for PUR recommend.
P.38 Change C78 and C79 from 15pF NPO 10% to 5% for PUR recommend.
P.11 Change C736 from 15pF NPO 10% to 5% for PUR recommend.
P.46 Change C244 and C245 from 47pF NPO 10% to 5% for PUR recommend.
P.39 Add C445 0.1uF for Hipot test.
P.27 Delete R146 0ohm for derating.
P.18 Delete R257 0ohm for derating.
P.17 Delete R237 0ohm for derating.

(2009/07/22)

P.17 Change C208 0.22uF from 16V to 25V for derating.
P.39 Add C791, C794 1000pF and C795, C796 0.047uF for EMI request.
P.12 Change R303 & R331 from 4.7K to 2.2K ohm NC.

H900 DVT -> PVT

(2009/07/24)

P.34 Add Q28 and NC C478 0.1uF for Sys_shdn#.
P.44 Change R467 from 33K to 10K ohm & R472 from 15K to 6.8Kohm for thermal setting.
P.39 NC C26 0.1uF, R14 1K ohm and U2 24C08.
Add R612 1K ohm for disable external EEPROM.
P.44 Add C463 100p NC for Thermal sensor vendor recommend.

(2009/07/28)

P.9 Change R51 & R53 from NC to introduce.
P.33 Change HDMI connector from 2N-0019003-FKGO to 2N-0019002-MKGO

H900 PVT -> X-Build

(2009/08/03)

P.31 Change L61, L62, and L63 from 33R to 47R for CRT debug.
P.33 Change D5 location to D9 for Safety recommend.
P.11 Change D9 location to D5 for Safety recommend.
P.11 Change R340 & R341 location to R427 & R426 for Safety recommend.
P.24 Change R426 location to R341 for Safety recommend.
P.45 Change R427 location to R340 for Safety recommend.
P.32 Change U5 location to U4 for Safety recommend.
P.10 Change U37 location to U40 for Safety recommend.
P.45 Change U4 & U40 location to U5 & U37 for Safety recommend.
P.4 Change U17 from 14-MC74VHC-1G04 to 14-74AHC1G-1400 for L6 recommend.

(2009/08/07)

P.31 Change C646 & C640 from 47p to 22p.

(2009/08/20)

P.30 Change L1 to LanKom 1T-1LG2425-P100.
P.20 Change R61 to NC for DDR Intel recommend.
P.21 Change R66 to NC for DDR Intel recommend.

(2009/08/22)



P.20 & 21 Del R146 & R237 for customer recommend.
P.20 Reserve R23 & R27 1K ohm for intel DDR3 M1 solution.
P.21 Reserve R29 & R31 1K ohm for intel DDR3 M1 solution.

(2009/08/24)

P.24 Add R636 0 ohm for EMI recommend.
P.24 Add Cap7 330 uF for debugging WLAN issue.


(2009/08/25)

P.44 Add R637, R638, R645 & R646 0 ohm for Intel recommend.

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1	2009/04/10	P.55	+1_05VRUN	1.05V Vripple over spec.	Change PC143 from 220uF 2.5V 35m Ohm(1C-31R0227-MX00) to 330uF 2.5V 15m Ohm(1C-33U0337-KX00).	X01
2	2009/04/13	P.51	Charger	Change PR152 for ADAPT OC function.	Change PR152 from 8.45K 0402 1%(1R-0008451-F200) to 10K 0402 1%(1R-0000103-F200)	X01
3	2009/05/06	P.57	VCORE	Fine tune VCORE setting for loadline, transition and mosfet ring issue.	Add PC7 :470pF 50V X7R 0402(1C-2B20471-K000) Add PC106 :4700pF 16V X7R 0402(1C-2B20472-K002) Add PC29 and PC30 :1000pF 50V X7R(1C-2B3012-MX00) Add PR60 and PR61 :4.3 Ohm 1206 5%(1R-000043X-J600) Del PQ14 and PQ15 SiR462DP-T1-GE3 (17-S1R462D-PT00) Change PR12 from 10 Ohm 0402 5%(1R-0000100-J200) to 0 Ohm 0402 5%(1R-0000000-J200) Change PR143 from 7.15K Ohm 0402 1%(1R-0007151-F200) to 6.34K Ohm 0402 1%(1R-0006341-F200) Change PR82 and PR83 from 2.7K Ohm 0402 1%(1R-0000272-F200) to 2.2K Ohm 0402 1%(1R-0000222-F200) Change PR84 and PR85 from 4.02K Ohm 0402 1%(1R-0004021-F200) to 1.69K Ohm 0402 1%(1R-0001691-F200)	X01
4	2009/05/06	P.58	AT_VDD	Changing H-S,L-S Mosfets and boost resistor for solving ring issue.	Change PQ40 from Si7716ADN(17-S17716A-DN00) to AON7402L(17-AON7402-L000) Change PQ41 from Si7114ADN(17-S17114A-DN00) to AON7700(17-AON7700-0000) Change PR222 from 0 Ohm 0603 1%(1R-0000000-J300) to 1 Ohm 0603 1%(1R-000010X-F300)	X01
5	2009/05/07	P.54	+1_5VSUS	Modifying OCP setting for +1_5VSUS.	Change PR204 from 4.87K 0603 1%(1R-0004871-F300) to 5.23K 0603 1%(1R-0005231-F300) Change PR203 from 3.24K 0603 1%(1R-0003241-F300) to 3.09K 0603 1%(1R-0003091-F300)	X01
6	2009/05/11	P.56	+1_1V_VTT	Change remote sense detection from CPU to output Cap.	Add PR184 10 Ohm 0402 1%(1R-0000100-F200) Delete PR183 0 Ohm 0402 5%(1R-0000000-J200)	X01
7	2009/05/12	P.50	PSID	Change PQ4 to high ESD protection (6000KV).	Change PQ4 from 2N7002K(17-2N7002K-0001) to FDV301N(17-FDV301N-0000).	X01
8	2009/05/12	P.55 P.56	+1_05VRUN +1_1V_VTT	Change RUN_PWRGD singal from +1_1V_VTT rail to +1_05VRUN rail.	Delete PR70 100 Ohm 0402 1%(1R-0000101-F200) Add PR195 10 Kohm 0402 1%(1R-0000103-F200) Add PR194 0 Ohm 0402 5%(1R-0000000-J200)	X01
9	2009/05/13	P.57	VCORE	PROCHOT# signal pull-up resistor is 56 ohm in IMVP side.	Change PR48 from 56 Ohm 0603 1%(1R-0000560-J300) to 68 Ohm 0603 1%(1R-0000680-F300)	X01
10	2009/05/20	P.58	PEX_VDD	Modify feedback capacitor for improving loop response.	Change PC57 from 0.01uF 0402 25V X7R(1C-2B20103-M000) to 470pF 0402 50V X7R(1C-2B20471-K000)	X01
11	2009/05/20	P.51	DC_IN	Modify resistor and capacitor for reducing adapeter's inrush current.	Change PR28 from 47KOhm 0402 5%(1R-0000473-J200) to 100KOhm 0402 5%(1R-0000104-J200) Change PC6 from 0.1uF 0603 50V(1C-2B30104-K000) to 0.22uF 0603 25V X5R(1C-2B30224-K400)	X01
12	2009/05/26	P.54	+1_5VSUS	Add a capacitor between CSH and FB for improving jitter issue.	Add PC207 4700pF 25V 0402 X7R 10%(1C-2B20472-K001)	X01

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13	2009/06/18	P.57	V_CORE	Change GND design for C-state issue	Change PR21.1 to PGND. Change PR21.2 to AGND. Change PC14.2 to PGND.	X02
14	2009/07/02	P.57	V_CORE	Change boost resistor to reduce ring of Mosfet. Add feedback capacitor to reduce ground noise.	Change PR178 from 0 Ohm 0603 5% (1R-0000000-J300) to 2.2 Ohm 0603 1% (1R-000022X-F300) Change PR177 from 0 Ohm 0603 5% (1R-0000000-J300) to 2.2 Ohm 0603 1% (1R-000022X-F300) Add PC7: 1000pF 16V X7R (1C-2B20102-K001) . Add PC8: 1000pF 16V X7R (1C-2B20102-K001) . Add PC11: 1000pF 16V X7R (1C-2B20102-K001) . Add PC12: 1000pF 16V X7R (1C-2B20102-K001) .	X02
15	2009/07/06	P.51	Charger	Change rating voltage from 25V to 50V and size from 0603 to 0805 for Capacitor(PC6).	Change PC6 from 0.22uF 25V X5R 0603 10% (1C-2B30224-K400) to 0.22uF 50V X5R 0805 10% (1C-2B70224-K600)	
16	2009/07/10	P.57	V_CORE	Modify DCR feedback and IMON setting.	Change PR84 and PR85 from 1.69K 0402 1% (1R-000169I-F200) to 3.9K 0402 1% (1R-000390I-F200) Change PR150 from 10K 0402 1% (1R-0000103-F200) to 1.8K 0402 1% (1R-0000182-F200) Change PC208 from 0.1uF 6.3V 0402 (1C-2B20104-K101) to 0.022uF 16V 0402 X7R (1C-2B20223-K000) Change PR146 from 12K 0402 1% (1R-0000123-F200) to 15.4K 0402 1% (1R-0001542-F200)	X02
17	2009/07/20	P.59	Other power plane	Add discharge path for 1_5VRUN and 1_05VRUN	Add PR104:330 Ohm 0603 5% (1R-0000331-J300) Add PR95:330 Ohm 0603 5% (1R-0000331-J300) Add FQ21:2N7002-7-F SOT-23 (17-2N70027-F000) Add FQ18:2N7002-7-F SOT-23 (17-2N70027-F000)	X02
18	2009/07/24	P.57	V_CORE	Add AL capacitor to reduce acoustic noise.	Add PC113:EEEFK1E101XP,100uF,25V,20%, 6.3*7.7,0.34ohm (1C-1XX0107-M400) Add PC182:EEEFK1E101XP,100uF,25V,20%, 6.3*7.7,0.34ohm (1C-1XX0107-M400)	X02
19	2009/09/25	P.58	VGA_CORE	Add more GPIO pin for VAG 4 level controller	Add NC_PC187,NC_PC188,NC_PC189 PR230,PR231,PR232, 0ohm Remove PR79, PR80	X02
20	2009/09/25	P.58	VGA_CORE	Change AOS MOS to ON MOS for reducing risk of induce voltage	Change PQ40 PQ41 and PQ54 to ON MOS 4823 and 4821.	
21	2009/11/19	P.58	VGA_CORE	EMI request add one cap	Add PC185 1000pF	
22	2009/11/19	P.58	VGA_CORE	Reduce inductor current when VID change	change PR230, PR232, from 0 to 47K. change PC188, PC189, from 0.047uF to 0.015uF. PC56 from 22pF to 560pF NC_PC131, PC141, PC142, from 330uF 15mohm to 330uF 9mohm. Add NC_PC190,NC_PC191 change PR86, to 46.4K for OCP 15A	
23	2009/11/19	P.58	VGA_CORE	TI suggest reducing short through risk	change PR222, from 1 ohm to 2.2 ohm	
24	2009/11/19	P.58	VGA_CORE	Remove unused GPIO pin	Remove PQ57,PD10,PR228,PR229	
24	2009/11/27	P.58	VGA_CORE	R C delay as Dell request	NC_PC188, PC_PC189 and add PC190, PC191 0.1uF	



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