Key West Block Diagram

Project code: 91.4D901.001
PCB P/N : 48.4D901.0SC
REVISION : 05209-SC

CLK GEN 3
ICS954226AG
SB

4,5 Mobile CPU
Celeron/Dothan

Host BUS 400MHz

DDRII*2 400MHz 11,12

6,7,8,9,10 Alviso
GML

LVDS
LCD 13

RGB CRT
CRT 14

DMI I/F 100MHz

15,16,17,18 ICH6-M

Mini-PCI 25
802.11a/b/g

RJ45 CONN 22
10/100 BCM4401 21
PCI BUS

RJ11 CONN 22
MODEM 26
MDC 1.5 Card

SB
AZALIA

LINE OUT 24
OP AMP 24
MAX4411

MIC IN 24
AC'97 CODEC 23
STAC9220

OP AMP 24
TPA6017

SB
2CH SPEAKER

USB 2.0
USB x 3 26

P IDE
MASTER
HDD 20

SLAVE
DVD/ CD-RW 20

PCI EXPRESS / USB 2.0
PCI EXPRESS CARD 20

LPC Bus
Power Switch 20
TPS2231

KBC 27
H8S/2111B

FlashRom 29
4Mb
(512kB)

Touch Pad 28

Int. KB 28

SMBus
Thermal Sensor & Fan 19
ENC 6N300
SB

SYSTEM DC/DC 33 MAX8734A SB	
INPUTS	OUTPUTS
DCBATOUT	5V_S3 3V_S3

SYSTEM DC/DC 34,35 TPS5130	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D2V_S0 1D8V_S3

MAXIM CHARGER 31 MAX1909	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 4.0A 5V 100mA

CPU DC/DC 32 MAX1907	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 27A

PCB LAYER

L1: Signal 1
L2: GND
L3: Signal 2
L4: Signal 3
L5: VCC
L6: Signal 4

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram
Size: A3 | Document Number: KeyWest | Rev: SC
Date: Thursday, June 30, 2005 | Sheet 1 of 37

ICH6-M Integrated Pull-up and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, EE_CS, GNT[5]#/GPO[17], GNT[6]#/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]#/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVR, SPKR	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

ICH6-M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

Power name description

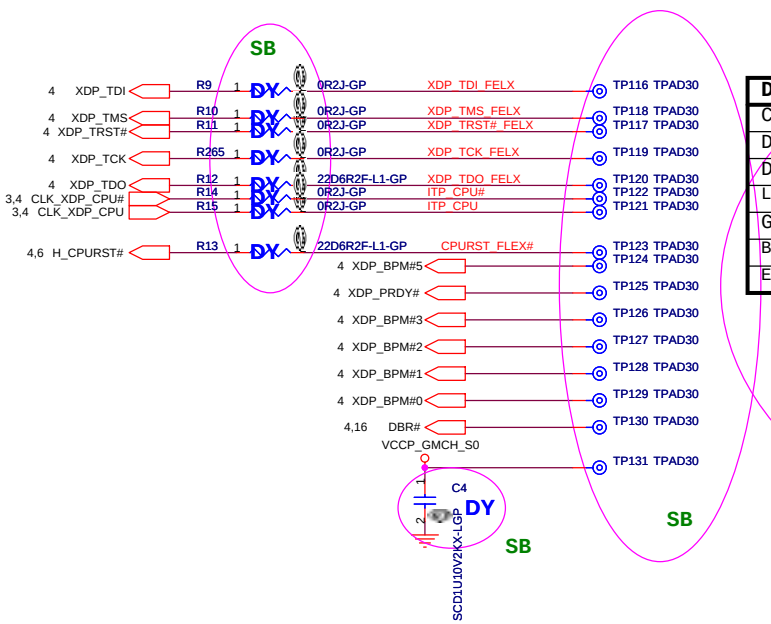
5V_S0= 5 Voltage power up on system work(S0 state)
5V_S3= 5 Voltage suspend to RAM(S3 state)
5V_S5= 5 Voltage soft off(S5 state)
3D3V_S0= 3.3 Voltage power up on system work(S0 state)
3D3V_S3= 3.3 Voltage suspend to RAM(S3 state)
3D3V_S5= 3.3 Voltage soft off(S5 state)
LVDDR_2D5V= 2.5 Voltage power up on system work(S0 state)
1D8V_S3= 1.8 Voltage suspend to RAM(S3 state)
2D5V_S0= 2.5 Voltage power up on system work(S0 state)

VCC_CORE_S0= CPU VID Voltage power up on system work(S0 state)
1D5V_VCCA_S0= 1.5 Voltage power up on system work(S0 state)
1D5V_S0= 1.5 Voltage power up on system work(S0 state)
1D5V_S5= 1.5 Voltage soft off(S5 state)
DDR_VREF_S3= 1.25 Voltage suspend to RAM(S3 state)
0D9V_S0= 0.9 Voltage power up on system work(S0 state)
1D2_VGA_S0= 1.2 Voltage power up on system work(S0 state) for VGA
1D05V_S0= 1.05 Voltage power up on system work(S0 state)
CORE_GMCH_S0= 1.05 Voltage power up on system work(S0 state) for ALVISO core power
VCCP_GMCH_S0= 1.05 Voltage power up on system work(S0 state)for ALVISO BUSIO power

10,34,35,36,37 1D05V_S0 — 1D05V_S0
4,5,6,7,9,10,15,17,19,32,37 VCCP_GMCH_S0 — VCCP_GMCH_S0
6,9,10,37 CORE_GMCH_S0 — CORE_GMCH_S0
12,35,36 0D9V_S0 — 0D9V_S0
7,11,35 DDR_VREF_S3 — DDR_VREF_S3
5,7,9,16,17,20,36,37 1D5V_S0 — 1D5V_S0
17,34,35,36 1D5V_S3 — 1D5V_S3
5 1D5V_VCCA_S0 — 1D5V_VCCA_S0
5,32,36 VCC_CORE_S0 — VCC_CORE_S0
7,9,14,17,34,36 2D5V_S0 — 2D5V_S0
7,9,10,11,12,16,34,35,36,37 1D8V_S3 — 1D8V_S3
3,4,5,7,9,11,13,15,16,17,18,19,20,23,24,25,27,29,32,34,36,37 3D3V_S0 — 3D3V_S0
16,17,18,19,20,25,26,33,37 3D3V_S3 — 3D3V_S3
4,13,16,19,27,28,29,30,31,32,33,34,35,36 3D3V_S5 — 3D3V_S5
21,22,36,37 3D3V_LAN_S5 — 3D3V_LAN_S5
15,19,28,33,36 +3D3VRTC — +3D3VRTC
33,36 +3V_SRC — +3V_SRC

13,14,17,18,19,20,24,25,27,28,32,35,36,37 5V_S0 — 5V_S0
13,17,19,23,24,26,33,34,35,36,37 5V_S3 — 5V_S3
13,32,33,34,36 5V_S5 — 5V_S5

13,31,33,34,35,36,37 DCBATOUT — DCBATOUT
30,31,37 AD+ — AD+
30,31,37 BT+ — BT+



Device	SMBus addr.
Clock Gen.	D2
DDR Module 1	A0
DDR Module 2	A4
LCD	58
Guardian	5E
Battery	16
EEPROM	A2

USB Port	Key West Define
USBP[0]	USB1 Up connector
USBP[1]	New card used
USBP[2]	USB1 Down connector
USBP[3]	NC
USBP[4]	USB2 connector
USBP[5]	NC
USBP[6]	NC
USBP[7]	NC

PCIE Port	Key West Define
PE[1]	NC
PE[2]	NC
PE[3]	NC
PE[4]	New card used

SB

PCI RESOURCE TABLE

DEVICE	IDSEL	PCI IRQ	REQ# / GNT#
Mini-PCI	AD19	P_INTB# / P_INTD#	REQ3#/GNT3#
LAN	AD16	P_INTC#	REQ4#/GNT4#

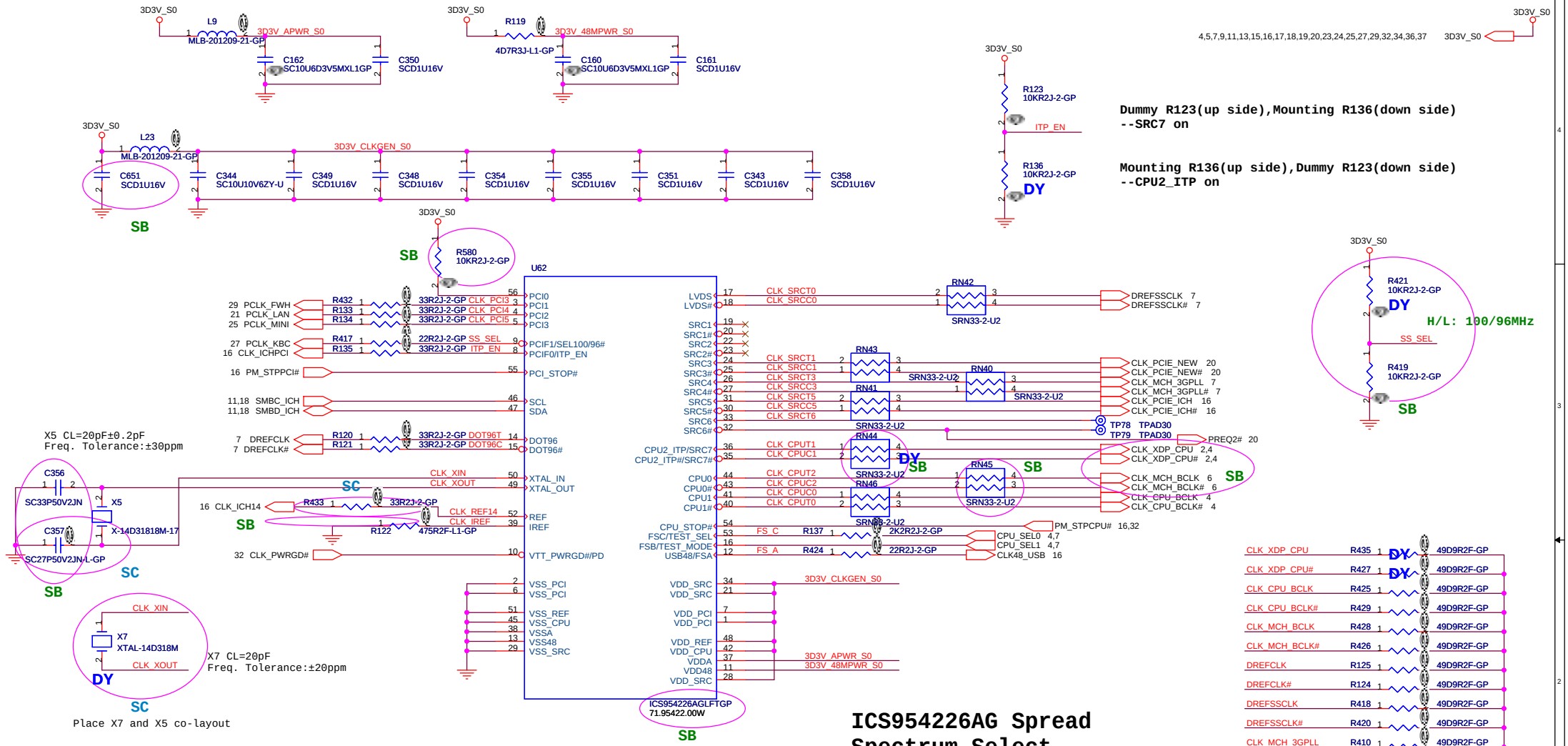
SB

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *ITP*

Size: A3 | Document Number: KeyWest | Rev: SC

Date: Thursday, June 30, 2005 | Sheet 2 of 37



1st source: 71.75422.00W (ICS954226AGLFTGP)
2nd source: 71.00140.00W (IDTCV140PAG-GP)

NEAR CLKGEN

ICS954226AG Spread Spectrum Select

S3	S2	S1	S0	Spread Amount%
0	0	0	0	-0.8
0	0	0	1	-1.0
0	0	1	0	-1.25
0	0	1	1	-1.5
0	1	0	0	-1.75
0	1	0	1	-2.0
0	1	1	0	-2.5
0	1	1	1	-3.0
1	0	0	0	+/-0.3
1	0	0	1	+/-0.4
1	0	1	0	+/-0.5
1	0	1	1	+/-0.6
1	1	0	0	+/-0.8
1	1	0	1	+/-1.0
1	1	1	0	+/-1.25
1	1	1	1	+/-1.5

FS_C	FS_B	FS_A	CPU
0	0	0	266M
0	0	1	133M
0	1	0	200M
0	1	1	166M
1	0	0	333M
1	0	1	100M
1	1	0	400M
1	1	1	Reserved

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Clock Generator (ICS954226AG)

Size: A3 | Document Number: KeyWest | Rev: SC

Date: Thursday, June 30, 2005 | Sheet 3 of 37

1st source:62.10055.011
2nd source:62.10053.061
3rd source:62.10053.111

U46A 62.10055.011

U46B 62.10055.011

PZ47903

Only support 400MHz (GML)

CPU

ITP Conn.

TCK(PIN A13)

TCK(PIN 5)

FBO(PIN 11)

All place within 2" to CPU

Place testpoint on H_IERR# with a GND 0.1" away

PM_THRMTRIP# should connect to ICH6 and Alviso without T-ing (No stub)

Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" . Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .

Layout Note: 0.5" max length.

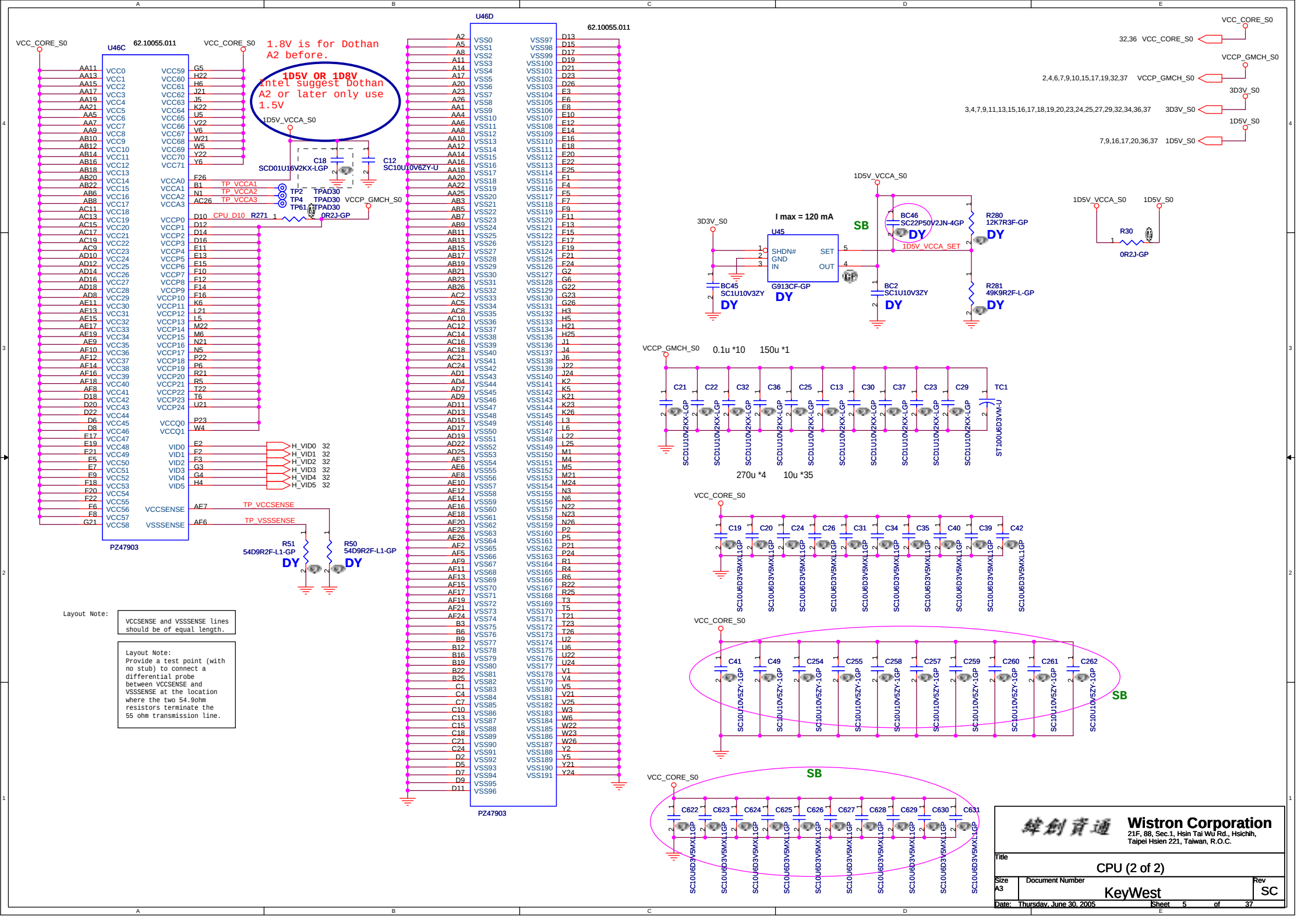
BSEL[1:0]	Freq.(MHz)
L H	100
L L	133

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (1 of 2)

Size: A3 | Document Number: KeyWest | Rev: SC

Date: Thursday, June 30, 2005 | Sheet 4 of 37


U46C
62.10055.011
PZ47903
U46D
62.10055.011
PZ47903
VCC_CORE_S0
1.8V is for Dothan A2 before.
1D5V OR 1D8V
Intel suggest Dothan A2 or later only use 1.5V
1D5V_VCCA_S0
SCD01U16V2KX-LGP
SC10U10V6ZY-U
TP_VCCA1
TP_VCCA2
TP_VCCA3
TP2
TP4
TP61
TPAD30
VCCP_GMCH_S0
CPU_D10
R271
0R2J-GP
TP_VCCSENSE
TP_VSSSENSE
R51
R50
54D9R2F-L1-GP
DY
H_VID0
H_VID1
H_VID2
H_VID3
H_VID4
H_VID5
Layout Note:
VCCSENSE and VSSSENSE lines should be of equal length.
Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.
VCC_CORE_S0
32,36 VCC_CORE_S0
VCCP_GMCH_S0
2,4,6,7,9,10,15,17,19,32,37 VCCP_GMCH_S0
3D3V_S0
3,4,7,9,11,13,15,16,17,18,19,20,23,24,25,27,29,32,34,36,37 3D3V_S0
1D5V_S0
7,9,16,17,20,36,37 1D5V_S0
1D5V_VCCA_S0
I max = 120 mA
SB
U45
SHDN#
GND
IN
SET
OUT
G913CF-GP
BC46
SC22P50V2JN-4GP
BC45
SC1U10V3ZY
BC2
R280
12K7R3F-GP
R281
49K9R2F-L-GP
1D5V_VCCA_SET
R30
0R2J-GP
VCCP_GMCH_S0
0.1u *10
150u *1
270u *4
10u *35
SCD1U10V2KX-LGP
ST100U6D3VM-U
VCC_CORE_S0
SC10U6D3V5MXL1GP
SC10U10V5ZY-1GP
SB
SC10U6D3V5MXL11GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU (2 of 2)
Size
A3
Document Number
KeyWest
Rev
SC
Date: Thursday, June 30, 2005
Sheet 5 of 37

Trace 10 mil wide with 20 mil spacing

H_XRCOMP — R78 24D9R2F-L-GP — 2

H_YRCOMP — R91 24D9R2F-L-GP — 2

VCCP_GMCH_S0 — R77 54D9R2F-L1-GP — H_XSCOMP

VCCP_GMCH_S0 — R92 54D9R2F-L1-GP — H_YSCOMP

VCCP_GMCH_S0 — R75 221R3F-1-GP — H_XSWING — R76 100R2F-L1-GP-U — C85 SCD1U16V

VCCP_GMCH_S0 — R89 221R3F-1-GP — H_YSWING — R90 100R2F-L1-GP-U — C98 SCD1U16V

Trace 10 mil wide with 20 mil spacing

Alviso Strapping Signals and Configuration

REV.NO. 1.0
REF. NO. 15577 page 183

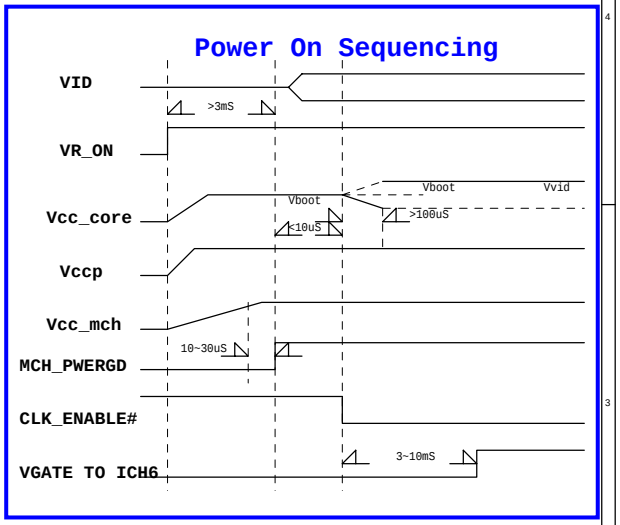
Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 **101 = FSB400** others = Reversed
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4 (Default)**
CFG6	Reserved	**0 = DDR2 (Default)** 1 = DDR1
CFG7	CPU Strap	0 = Reserved **1 = Dothan (Default)**
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reserve Lanes **1 = Normal (Default)**
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled **11 = Normal Operation (Default)**
CFG[15:14]	Reversed	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG17	Reversed	
CFG18	GMCH core VCC Select	**0 = 1.05V (Default)** 1 = 1.5V
CFG19	CPU VTT Select	**0 = 1.05V (Default)** 1 = 1.2V
CFG20	Reversed	
SDVOCRTL_DATA	SDVO Present	**0 = No SDVO device present(Default)** 1= SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORK In signal.

CORE_GMCH_S0
9,10,37 CORE_GMCH_S0

VCCP_GMCH_S0
2,4,5,7,9,10,15,17,19,32,37 VCCP_GMCH_S0

Power On Sequencing



4 H_D#[63..0]

U18A — HOST

H_D#0 E4 HD0# … H_D#63 W2 HD63#

H_XRCOMP C1 HXRCOMP
H_XSCOMP C2 HXSCOMP
H_XSWING D1 HXSWING
H_YRCOMP T1 HYRCOMP
H_YSCOMP L1 HYSCOMP
H_YSWING P1 HYSWING

HA3# G9 H_A#3 … HA31# F13 H_A#31

H_A#[31..3] 4

HADS# F8 H_ADS# 4
HADSTB#0 B9 H_ADSTB#0 4
HADSTB#1 E13 H_ADSTB#1 4
HVREF J11 H_VREF
HBNR# A5 H_BNR# 4
HBPRI# D5 H_BPRI# 4
HBREQ0# E7 H_BREQ#0 4
HCPURST# H10 H_CPURST# 2,4

VCCP_GMCH_S0
R310 100R2F-L1-GP-U
H_VREF
C281 SCD1U10V2KX-LGP
R311 200R2F-L-GP

HCLKINN AB1 CLK_MCH_BCLK# 3
HCLKINP AB2 CLK_MCH_BCLK 3

HDBSY# C6 H_DBSY# 4
HDEFER# E6 H_DEFER# 4
HDINV#0 H8 H_DINV#0 … HDINV#3 U5 H_DINV#3
H_DINV#[3..0] 4
HDPWR# G6 H_DPWR# 4
HDRDY# E7 H_DRDY# 4

CORE_GMCH_S0
R358 0R2J-GP DY
H_DPWR#

HDSTBN#0 G4 H_DSTBN#0 … HDSTBN#3 V3 H_DSTBN#3
H_DSTBN#[3..0] 4
HDSTBP#0 G5 H_DSTBP#0 … HDSTBP#3 W4 H_DSTBP#3
H_DSTBP#[3..0] 4

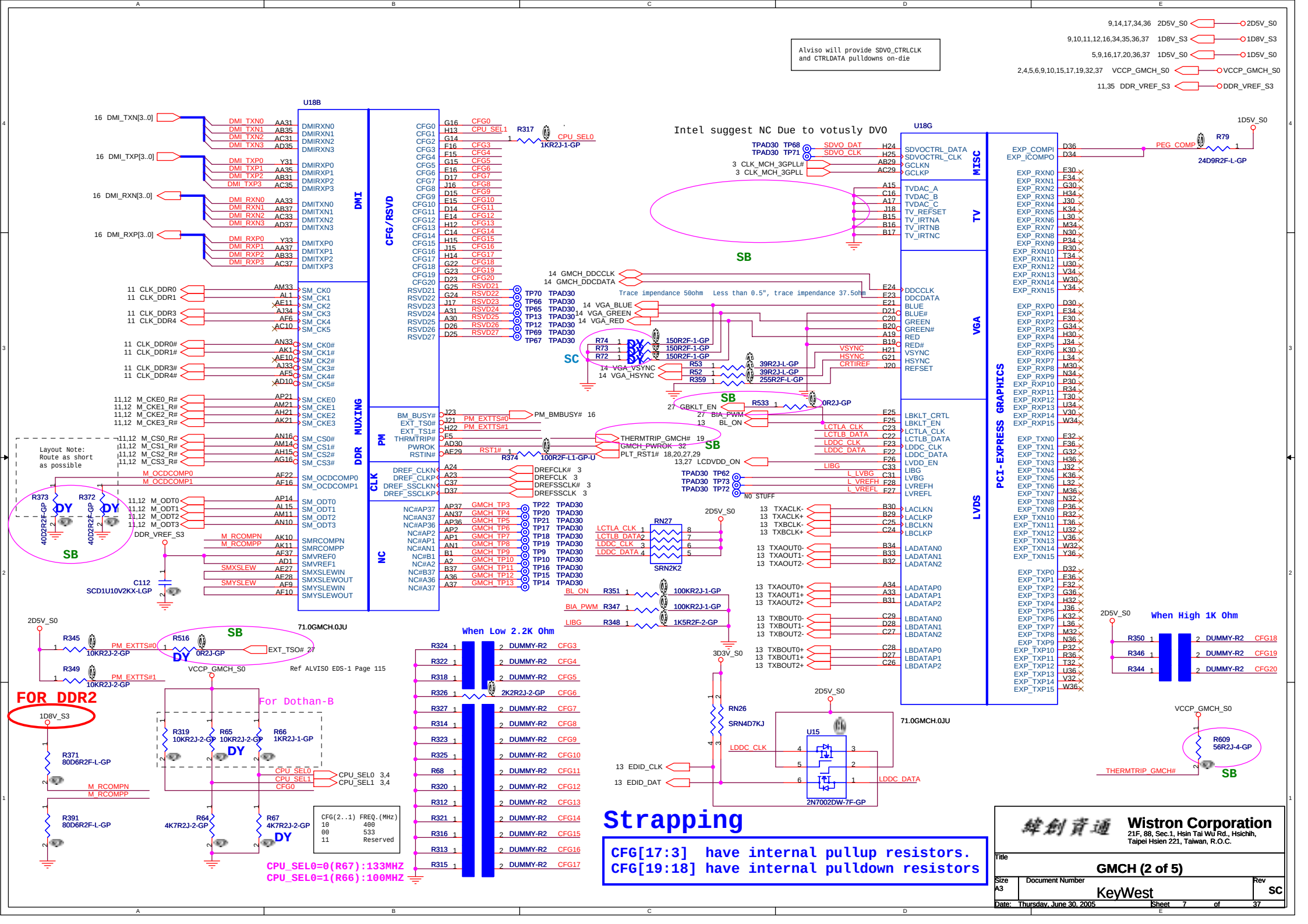
HEDRDY# F6 TP_H_EDRDY# — TP64 TPAD30
HHIT# D4 H_HIT# 4
HHITM# D6 H_HITM# 4
HLOCK# B3 H_LOCK# 4
HPCREQ# A11 TP_H_PCREQ# — TP11 TPAD30
HREQ#0 A7 H_REQ#0 … HREQ#4 C8 H_REQ#4
H_REQ#[4..0] 4
HRS#0 A4 H_RS#0 … HRS#2 C5 H_RS#2
H_RS#[2..0] 4
HCPUSLP# G8 H_CPUSLP#_GMCH
R291 0R2J-GP
H_CPUSLP# 4,15
HTRDY# B5 H_TRDY# 4

71.0GMCH.0JU

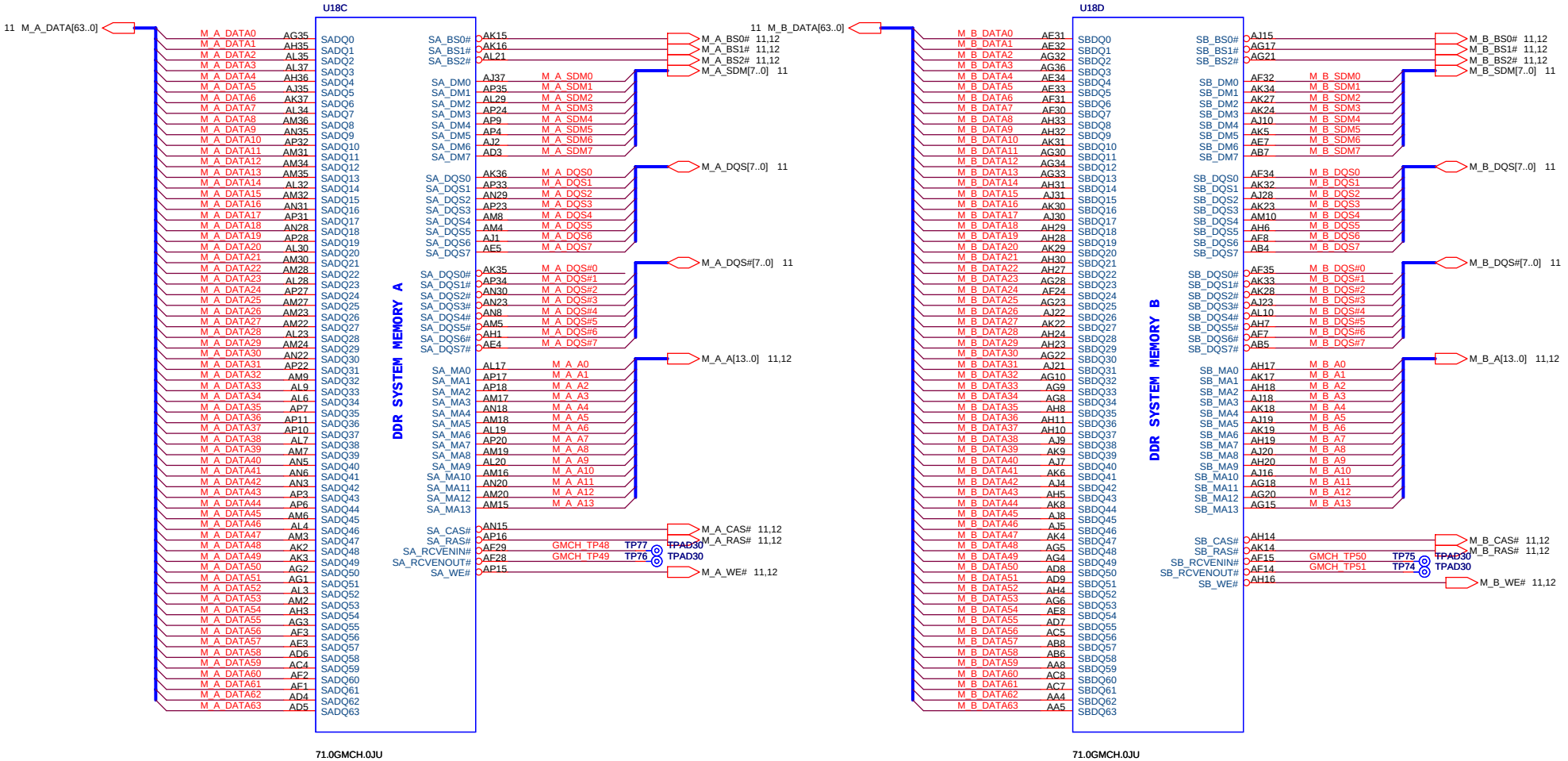
For Banias/Celeron-M:R1079=DUMMY
For Dothan A:R1079=DUMMY
For Dothan B:R1079=0R

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GMCH (1 of 5)
Size: A3 | Document Number: KeyWest | Rev: SC
Date: Thursday, June 30, 2005 | Sheet 6 of 37


U18B
DMI
CFG/RSVD
DDR MUXING
PM
CLK
NC
U18G
MISC
TV
VGA
LVDS
PCI-EXPRESS GRAPHICS
Intel suggest NC Due to votusly DVO
Alviso will provide SDVO_CTRLCLK and CTRLDATA pulldowns on-die
9,14,17,34,36 2D5V_S0
9,10,11,12,16,34,35,36,37 1D8V_S3
5,9,16,17,20,36,37 1D5V_S0
2,4,5,6,9,10,15,17,19,32,37 VCCP_GMCH_S0
11,35 DDR_VREF_S3
SB
SC
DY
FOR DDR2
For Dothan-B
When Low 2.2K Ohm
When High 1K Ohm
Layout Note: Route as short as possible
Trace impendance 50ohm Less than 0.5", trace impendance 37.5ohm
71.0GMCH.0JU
Ref ALVISO EDS-1 Page 115
CPU_SEL0=0(R67):133MHZ
CPU_SEL0=1(R66):100MHZ
CFG[2..1) FREQ.(MHz)
10 400
00 533
11 Reserved
Strapping
CFG[17:3] have internal pullup resistors.
CFG[19:18] have internal pulldown resistors
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
GMCH (2 of 5)
Size A3
Document Number KeyWest
Rev SC
Date: Thursday, June 30, 2005
Sheet 7 of 37

SUPPORT DDRII 400

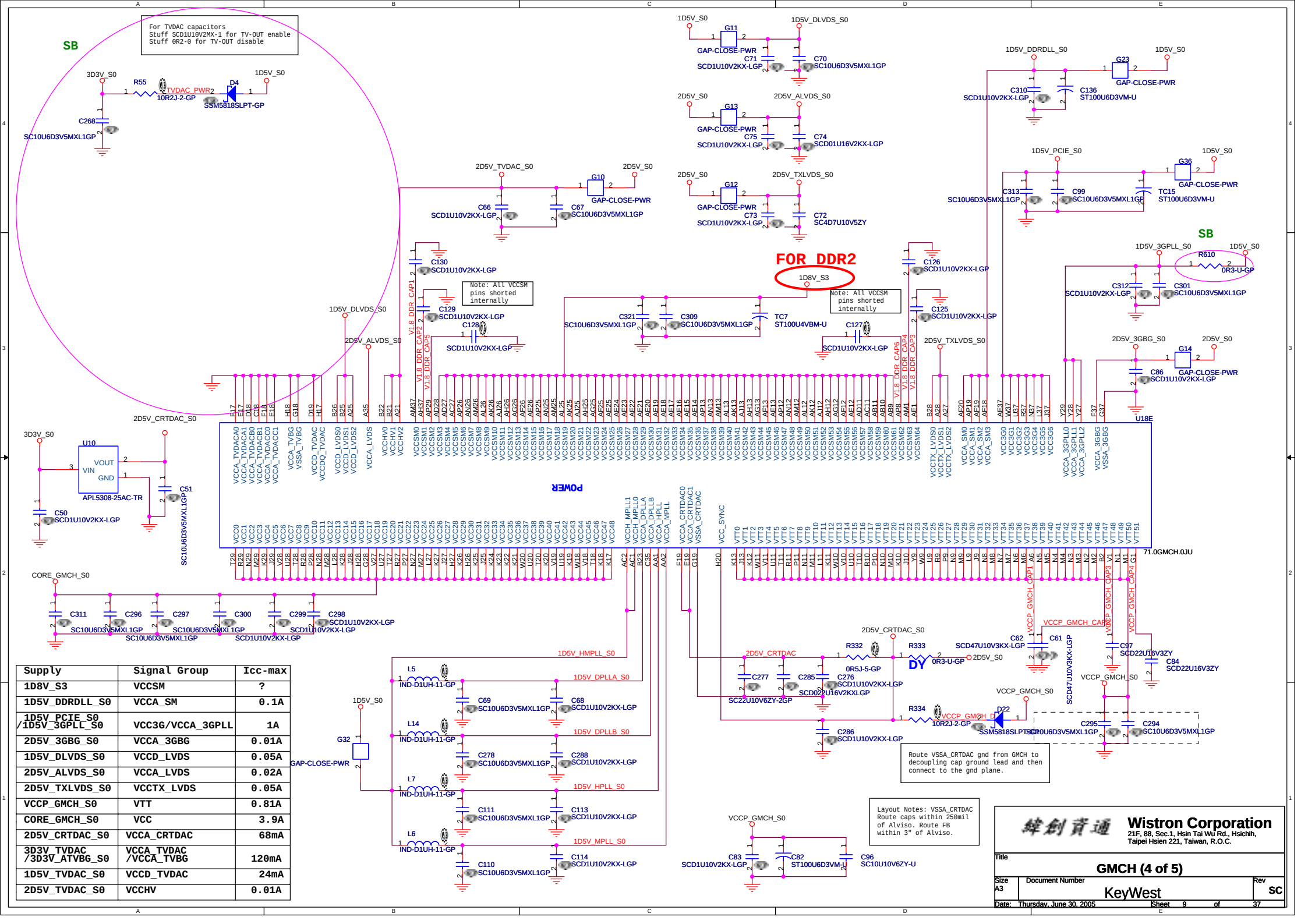


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GMCH (3 of 5)

Size: A3 | Document Number: KeyWest | Rev: SC

Date: Thursday, June 30, 2005 | Sheet 8 of 37



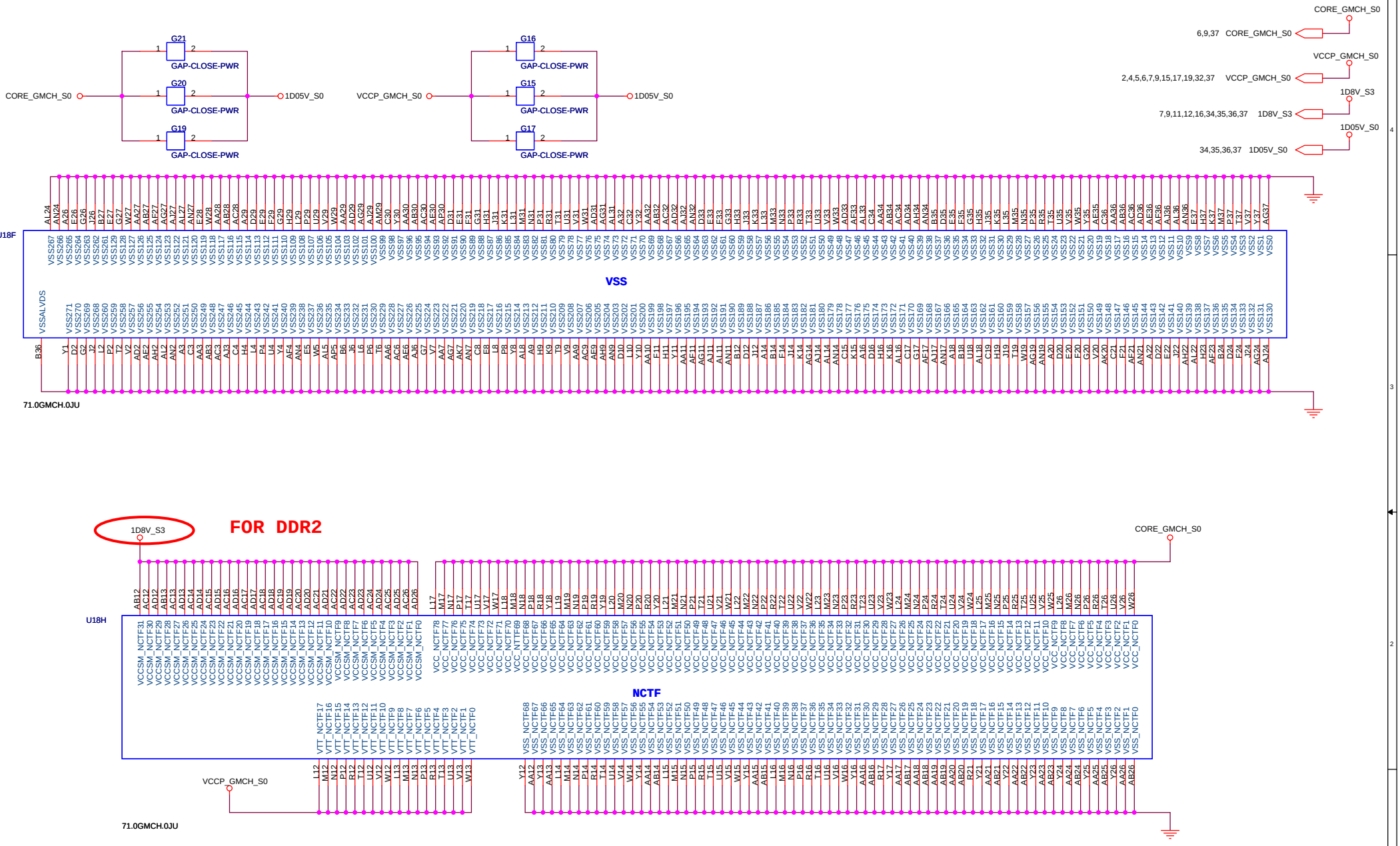
Supply	Signal Group	Icc-max
1D8V_S3	VCCSM	?
1D5V_DDRDLL_S0	VCCA_SM	0.1A
1D5V_PCIE_S0 /1D5V_3GPLL_S0	VCC3G/VCCA_3GPLL	1A
2D5V_3GBG_S0	VCCA_3GBG	0.01A
1D5V_DLVDS_S0	VCCD_LVDS	0.05A
2D5V_ALVDS_S0	VCCA_LVDS	0.02A
2D5V_TXLVDS_S0	VCCTX_LVDS	0.05A
VCCP_GMCH_S0	VTT	0.81A
CORE_GMCH_S0	VCC	3.9A
2D5V_CRTDAC_S0	VCCA_CRTDAC	68mA
3D3V_TVDAC /3D3V_ATVBG_S0	VCCA_TVDAC /VCCA_TVBG	120mA
1D5V_TVDAC_S0	VCCD_TVDAC	24mA
2D5V_TVDAC_S0	VCCHV	0.01A

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GMCH (4 of 5)

Size: A3 | Document Number: KeyWest | Rev: SC

Date: Thursday, June 30, 2005 | Sheet 9 of 37

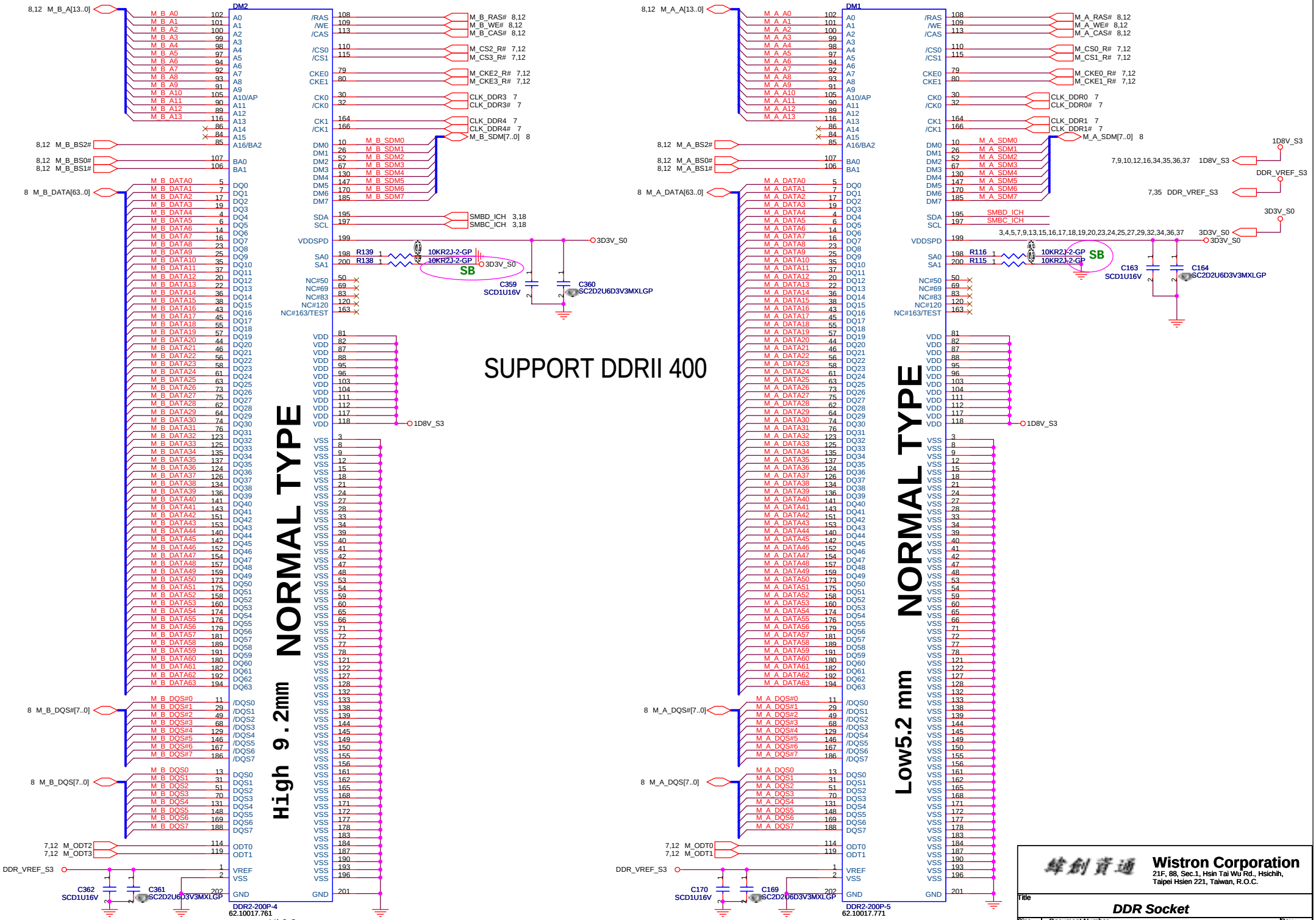


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **GMCH (5 of 5)**

Size	Document Number	Rev
A3	KeyWest	SC

Date: Thursday, June 30, 2005 Sheet 10 of 37


DM2
DDR2-200P-4
62.10017.761
High 9.2mm NORMAL TYPE
Hi 9.2 mm
SUPPORT DDRII 400
SB
10KR2J-2-GP
C359 SCD1U16V
C360 SC2D2U6D3V3MXLGP
C362 SCD1U16V
C361 SC2D2U6D3V3MXLGP
DM1
DDR2-200P-5
62.10017.771
Low5.2 mm NORMAL TYPE
C163 SCD1U16V
C164 SC2D2U6D3V3MXLGP
C170 SCD1U16V
C169 SC2D2U6D3V3MXLGP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDR Socket
Size Custom
Document Number
KeyWest
Rev SC
Date: Thursday, June 30, 2005
Sheet 11 of 37

PLACE CAPS BETWEEN AND NEAR DDR SKTS
PLACE EACH 0.1UF CAP CLOSE TO POWER PIN

1D8V_S3

C152 SCD1U16V
C150 SCD1U16V
C151 SCD1U16V
C149 SCD1U16V
C183 SCD1U16V
C178 SCD1U16V
C168 SCD1U16V
C166 SCD1U16V

C167 SCD1U16V
C179 SCD1U16V
C180 SCD1U16V
C165 SCD1U16V
C184 SCD1U16V
C182 SCD1U16V
C181 SCD1U16V
C177 SCD1U16V

C176 SCD1U16V
C153 SC10U6D3V5MX-1LGP
C185 SC10U6D3V5MX-1LGP
EC30 SCD1U16V
EC38 SCD1U16V
EC23 SCD1U16V
EC24 SCD1U16V

Address / CommandControl

0D9V_S0

8,11 M_A_A1
8,11 M_A_A0
RN32 SRN56-2-U2
C198 SCD1U16V

8,11 M_A_A3
8,11 M_A_A10
RN34 SRN56-2-U2
C197 SCD1U16V

8,11 M_B_CAS#
8,11 M_B_RAS#
RN5 SRN56-2-U2
C196 SCD1U16V

8,11 M_B_WE#
7,11 M_CS3_R#
RN7 SRN56-2-U2
C195 SCD1U16V

8,11 M_A_A7
8,11 M_A_A6
RN35 SRN56-2-U2
C191 SCD1U16V

8,11 M_A_A4
8,11 M_A_A2
RN33 SRN56-2-U2
C194 SCD1U16V

8,11 M_B_BS0#
8,11 M_B_A2
RN8 SRN56-2-U2
C193 SCD1U16V

8,11 M_B_A10
8,11 M_B_A4
RN9 SRN56-2-U2
C192 SCD1U16V

7,11 M_CKE2_R#
8,11 M_B_A5
RN13 SRN56-2-U2
C199 SCD1U16V

8,11 M_B_A11
8,11 M_B_A6
RN14 SRN56-2-U2
C200 SCD1U16V

0D9V_S0

8,11 M_A_BS1#
8,11 M_A_RAS#
RN30 SRN56-2-U2
C333 SCD1U16V

7,11 M_CS0_R#
8,11 M_A_A13
RN28 SRN56-2-U2
C334 SCD1U16V

8,11 M_B_BS2#
8,11 M_B_A12
RN12 SRN56-2-U2
C335 SCD1U16V

7,11 M_CKE3_R#
8,11 M_B_A7
RN15 SRN56-2-U2
C336 SCD1U16V

7,11 M_CS2_R#
8,11 M_B_A13
RN4 SRN56-2-U2
C337 SCD1U16V

8,11 M_B_A0
8,11 M_B_BS1#
RN6 SRN56-2-U2
C338 SCD1U16V

8,11 M_A_WE#
8,11 M_A_BS0#
RN31 SRN56-2-U2
C339 SCD1U16V

8,11 M_A_CAS#
7,11 M_CS1_R#
RN29 SRN56-2-U2
C340 SCD1U16V

8,11 M_B_A3
8,11 M_B_A1
RN10 SRN56-2-U2
C201 SCD1U16V

8,11 M_B_A9
8,11 M_B_A8
RN11 SRN56-2-U2
C202 SCD1U16V

7,11 M_CKE0_R#
8,11 M_A_BS2#
RN39 SRN56-2-U2
C330 SCD1U16V

8,11 M_A_A12
8,11 M_A_A9
RN38 SRN56-2-U2
C331 SCD1U16V

7,11 M_CKE1_R#
8,11 M_A_A11
RN36 SRN56-2-U2
C332 SCD1U16V

8,11 M_A_A8
8,11 M_A_A5
RN37 SRN56-2-U2
C329 SCD1U16V

0D9V_S0

7,11 M_ODT0 R402 56R2J-4-GP
7,11 M_ODT1 R401 56R2J-4-GP
7,11 M_ODT2 R140 56R2J-4-GP
7,11 M_ODT3 R141 56R2J-4-GP

0D9V_S0
35,36 0D9V_S0

1D8V_S3
7,9,10,11,16,34,35,36,37 1D8V_S3

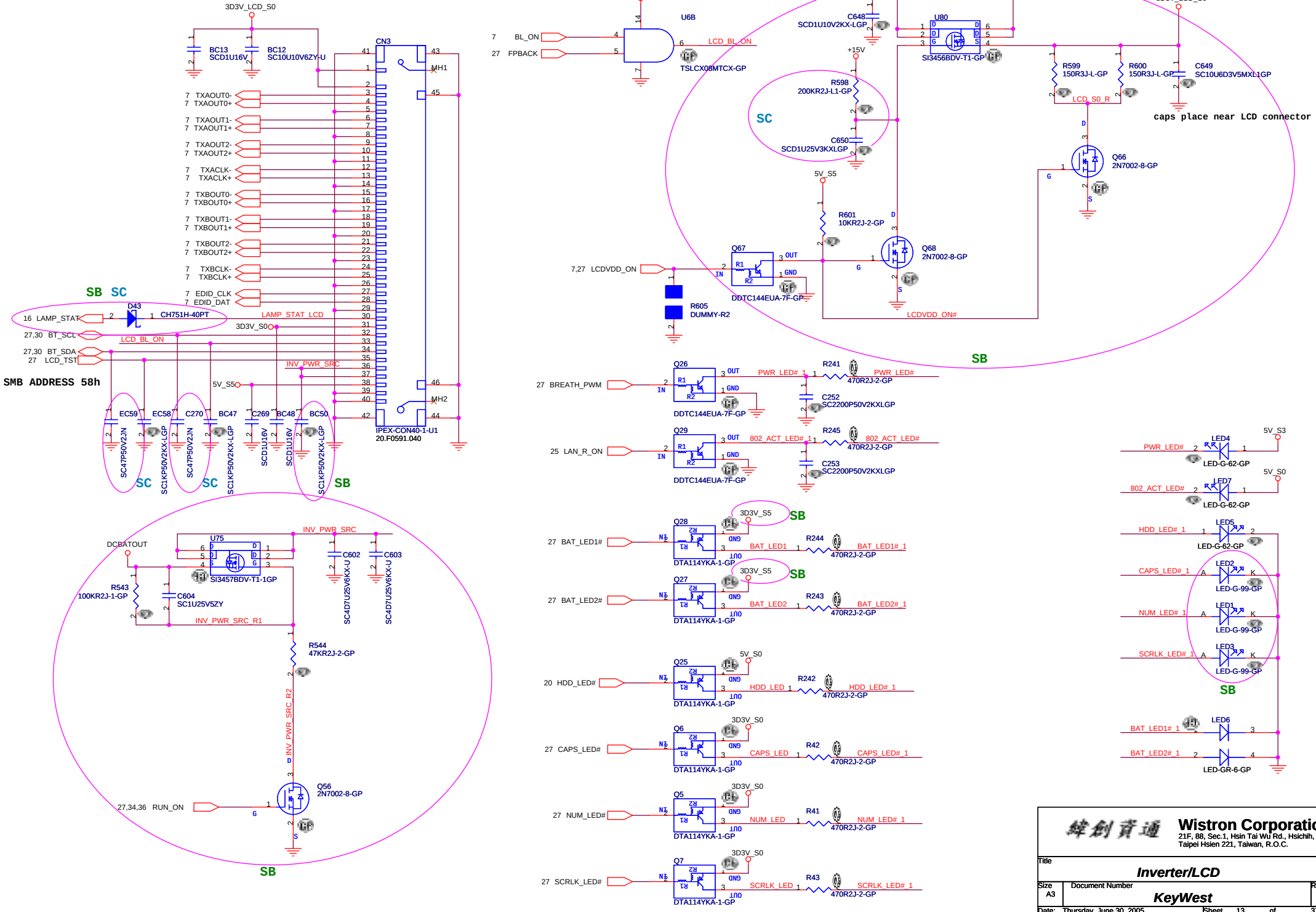
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR Serial/Terminator Resistor

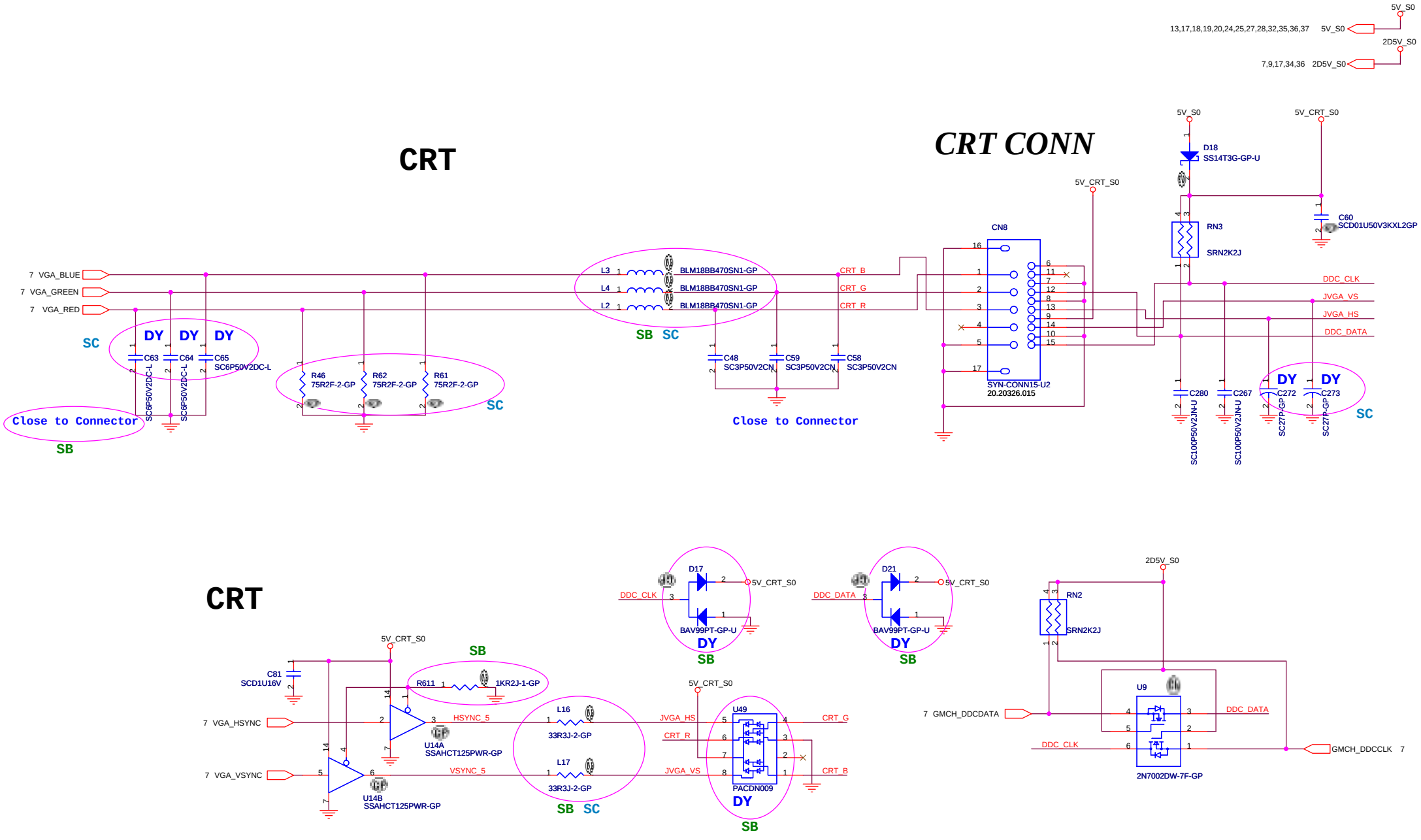
Size	Document Number	Rev
A3	KeyWest	SC

Date: Thursday, June 30, 2005 Sheet 12 of 37

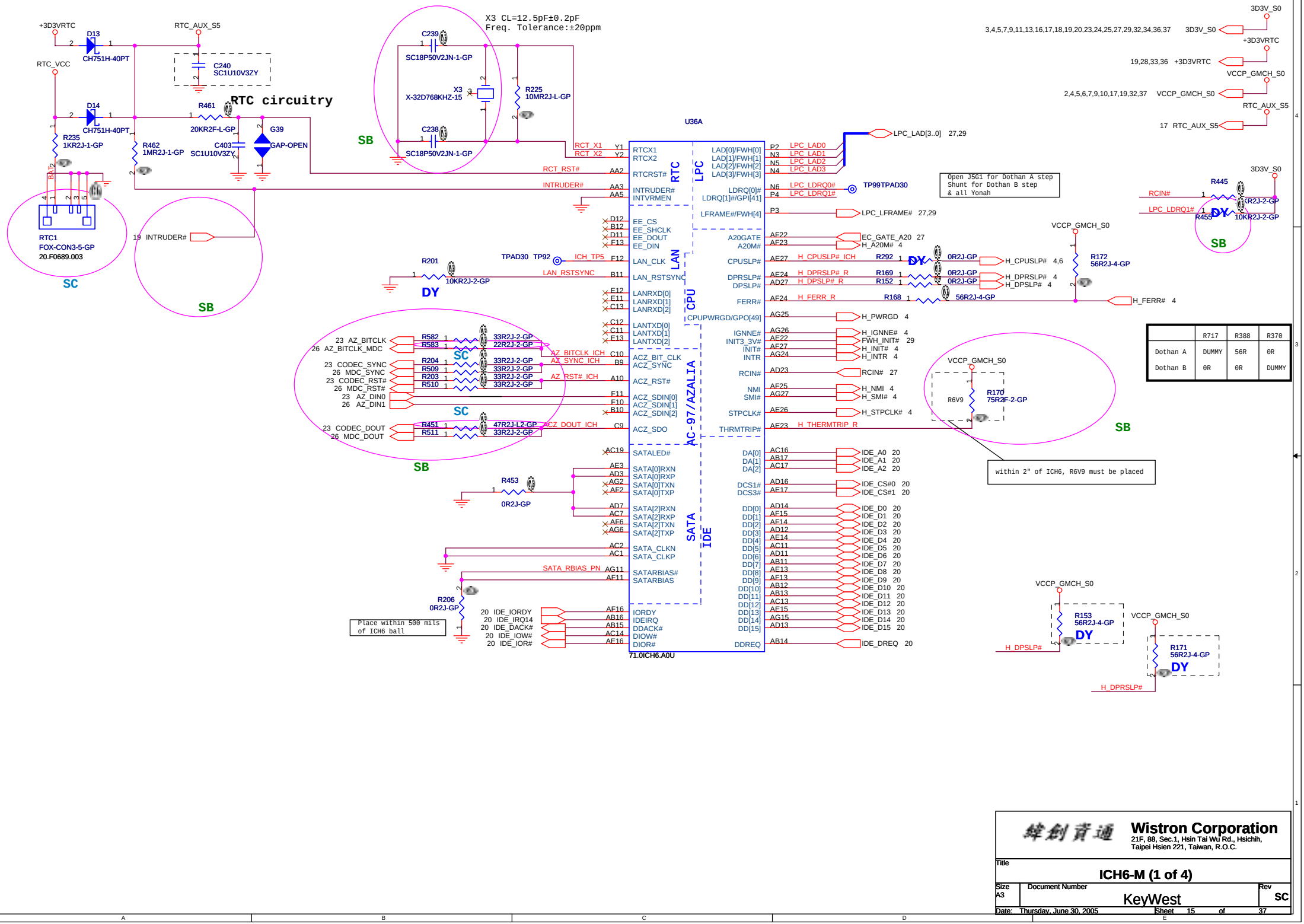
INVERTER/LCD



華創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	***Inverter/LCD***		
Size A3	Document Number ***KeyWest***		Rev ***SC***
Date: Thursday, June 30, 2005	Sheet 13 of 37		



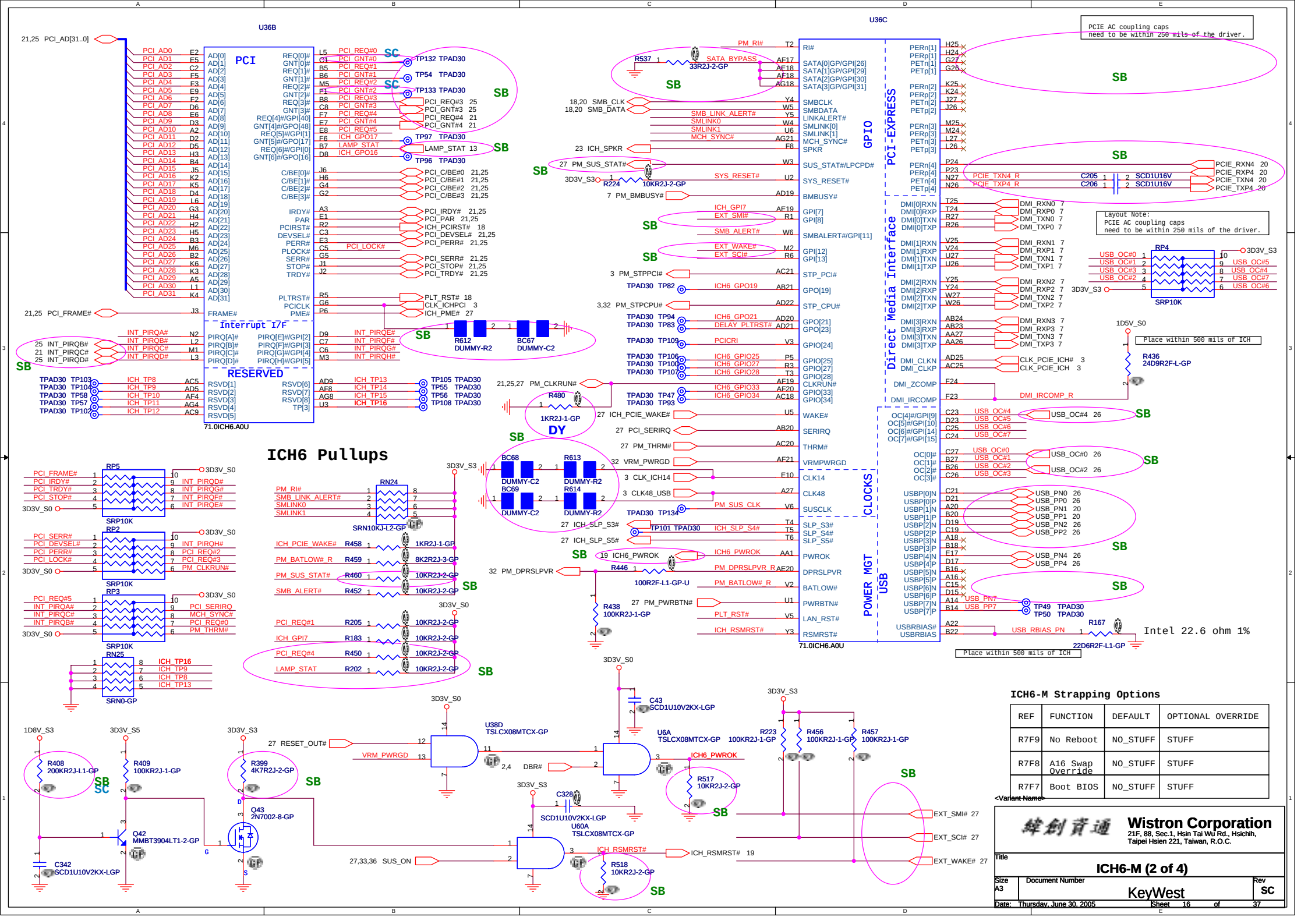
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**CRT**	
Size: A3	Document Number: **KeyWest**	Rev: SC
Date: Thursday, June 30, 2005	Sheet 14 of 37	



	R717	R388	R370
Dothan A	DUMMY	56R	0R
Dothan B	0R	0R	DUMMY

Size	Document Number	Rev
A3		SC

Date: Thursday, June 30, 2005 Sheet 15 of 37



ICH6-M Strapping Options

REF	FUNCTION	DEFAULT	OPTIONAL OVERRIDE
R7F9	No Reboot	NO_STUFF	STUFF
R7F8	A16 Swap Override	NO_STUFF	STUFF
R7F7	Boot BIOS	NO_STUFF	STUFF

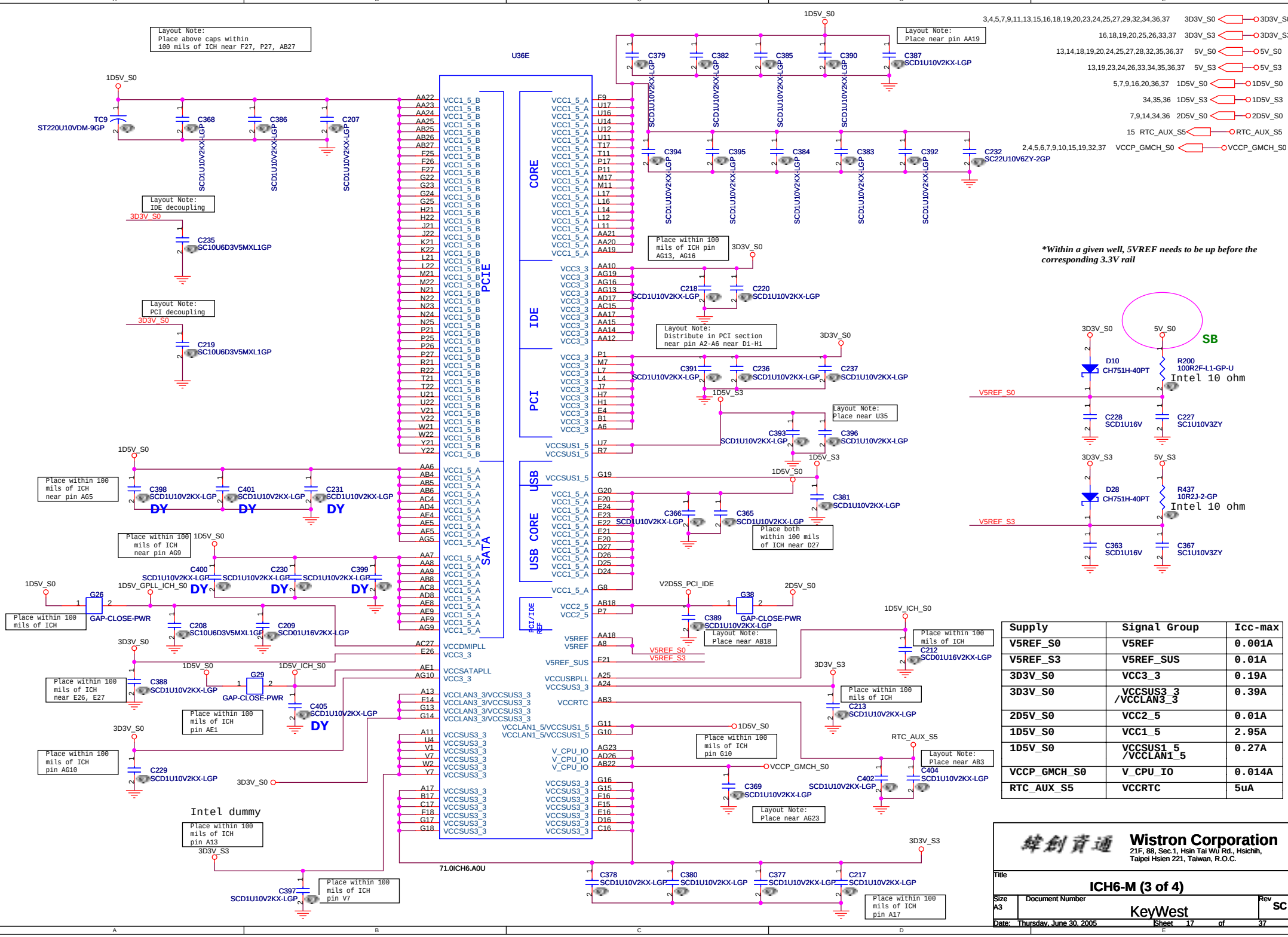
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

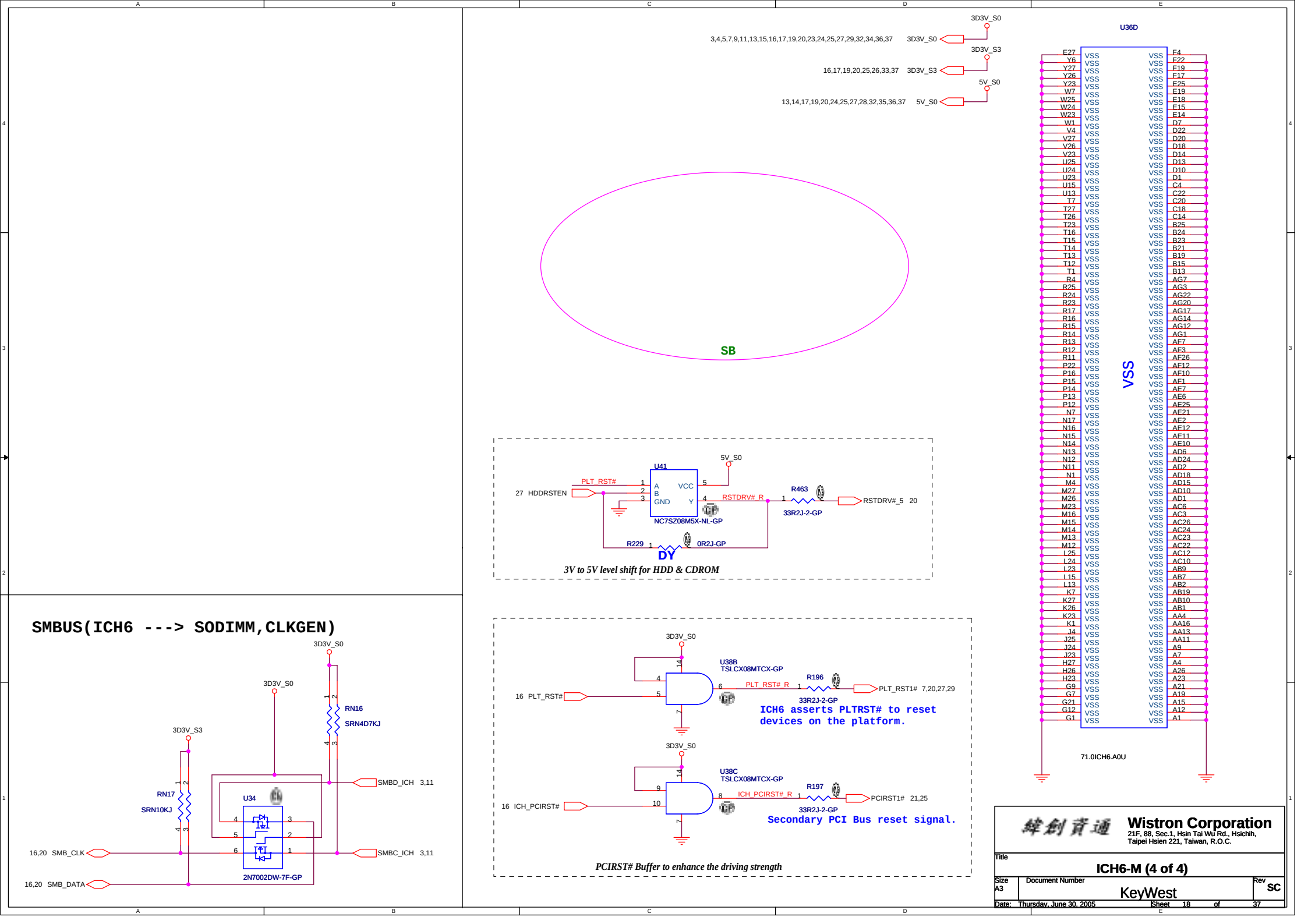
Title: ICH6-M (2 of 4)

Size: A3 | Document Number: KeyWest | Rev: SC

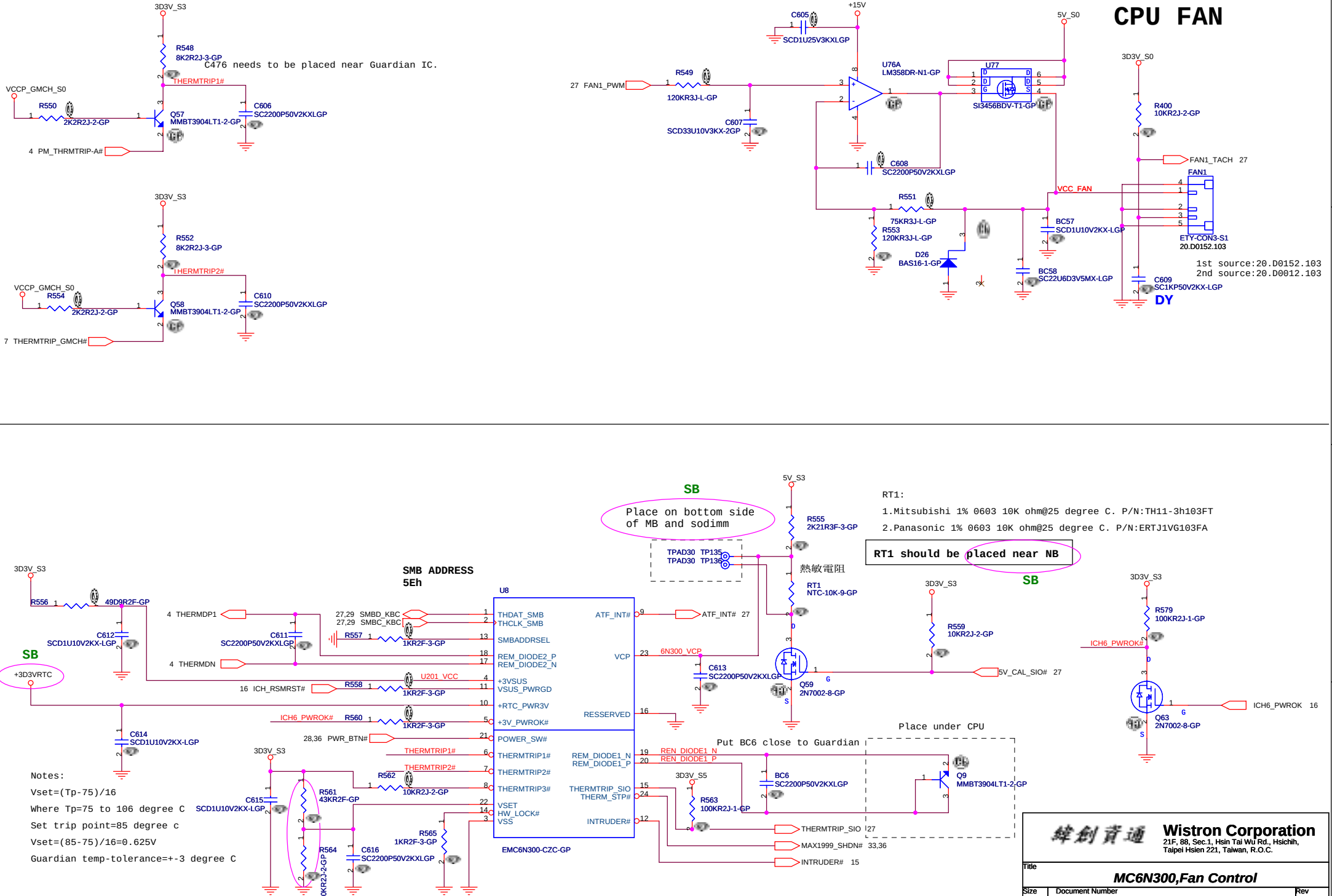
Date: Thursday, June 30, 2005 | Sheet 16 of 37



Supply	Signal Group	Icc-max
V5REF_S0	V5REF	0.001A
V5REF_S3	V5REF_SUS	0.01A
3D3V_S0	VCC3_3	0.19A
3D3V_S0	VCCSUS3_3 /VCCLAN3_3	0.39A
2D5V_S0	VCC2_5	0.01A
1D5V_S0	VCC1_5	2.95A
1D5V_S0	VCCSUS1_5 /VCCLAN1_5	0.27A
VCCP_GMCH_S0	V_CPU_IO	0.014A
RTC_AUX_S5	VCCRTC	5uA


3D3V_S0
3,4,5,7,9,11,13,15,16,17,19,20,23,24,25,27,29,32,34,36,37
3D3V_S0
3D3V_S3
16,17,19,20,25,26,33,37
3D3V_S3
5V_S0
13,14,17,19,20,24,25,27,28,32,35,36,37
5V_S0
SB
U36D
VSS
71.0ICH6.A0U
5V_S0
U41
27 HDDRSTEN
PLT_RST#
A
B
GND
VCC
Y
RSTDRV#_R
R463
33R2J-2-GP
RSTDRV#_5 20
NC7SZ08M5X-NL-GP
R229
0R2J-GP
DY
3V to 5V level shift for HDD & CDROM
SMBUS(ICH6 ---> SODIMM,CLKGEN)
3D3V_S0
3D3V_S0
3D3V_S3
RN16
SRN4D7KJ
RN17
SRN10KJ
U34
SMBD_ICH 3,11
SMBC_ICH 3,11
16,20 SMB_CLK
16,20 SMB_DATA
2N7002DW-7F-GP
3D3V_S0
U38B
TSLCX08MTCX-GP
16 PLT_RST#
PLT_RST#_R
R196
33R2J-2-GP
PLT_RST1# 7,20,27,29
ICH6 asserts PLTRST# to reset devices on the platform.
3D3V_S0
U38C
TSLCX08MTCX-GP
16 ICH_PCIRST#
ICH_PCIRST#_R
R197
33R2J-2-GP
PCIRST1# 21,25
Secondary PCI Bus reset signal.
PCIRST# Buffer to enhance the driving strength
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH6-M (4 of 4)
Size
A3
Document Number
KeyWest
Rev
SC
Date: Thursday, June 30, 2005
Sheet 18 of 37

CPU FAN



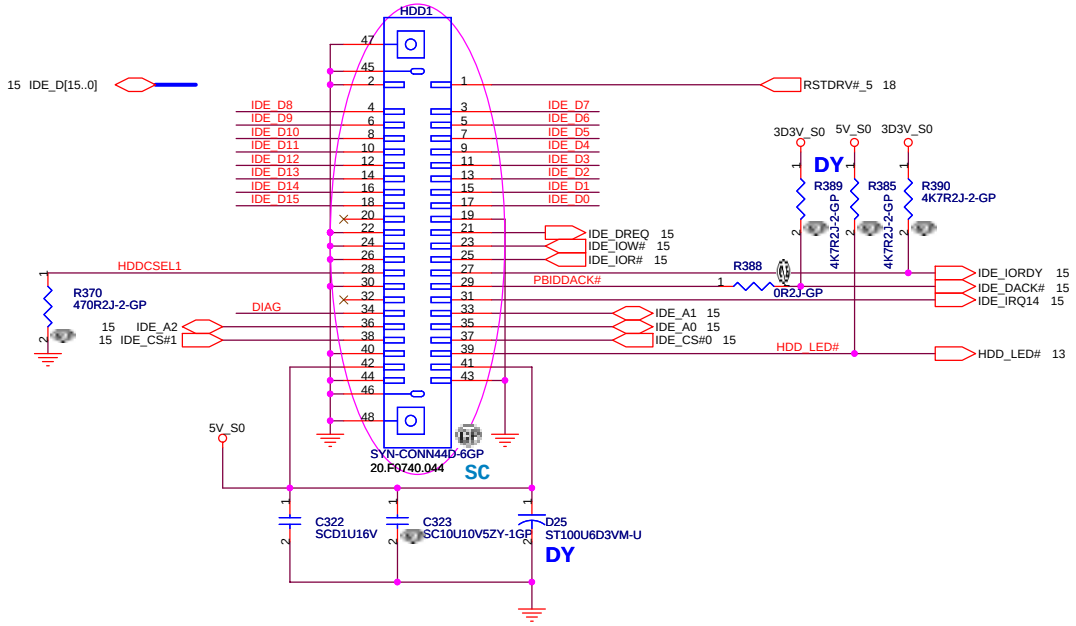
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **MC6N300,Fan Control**

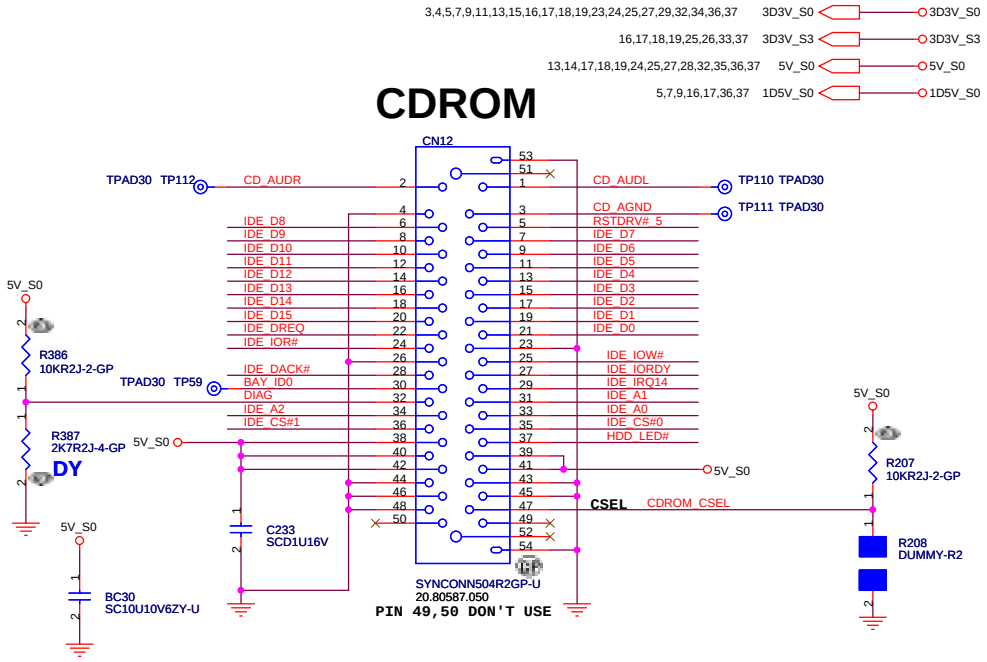
Size	Document Number	Rev
A3	KeyWest	SC

Date: Thursday, June 30, 2005 Sheet 19 of 37

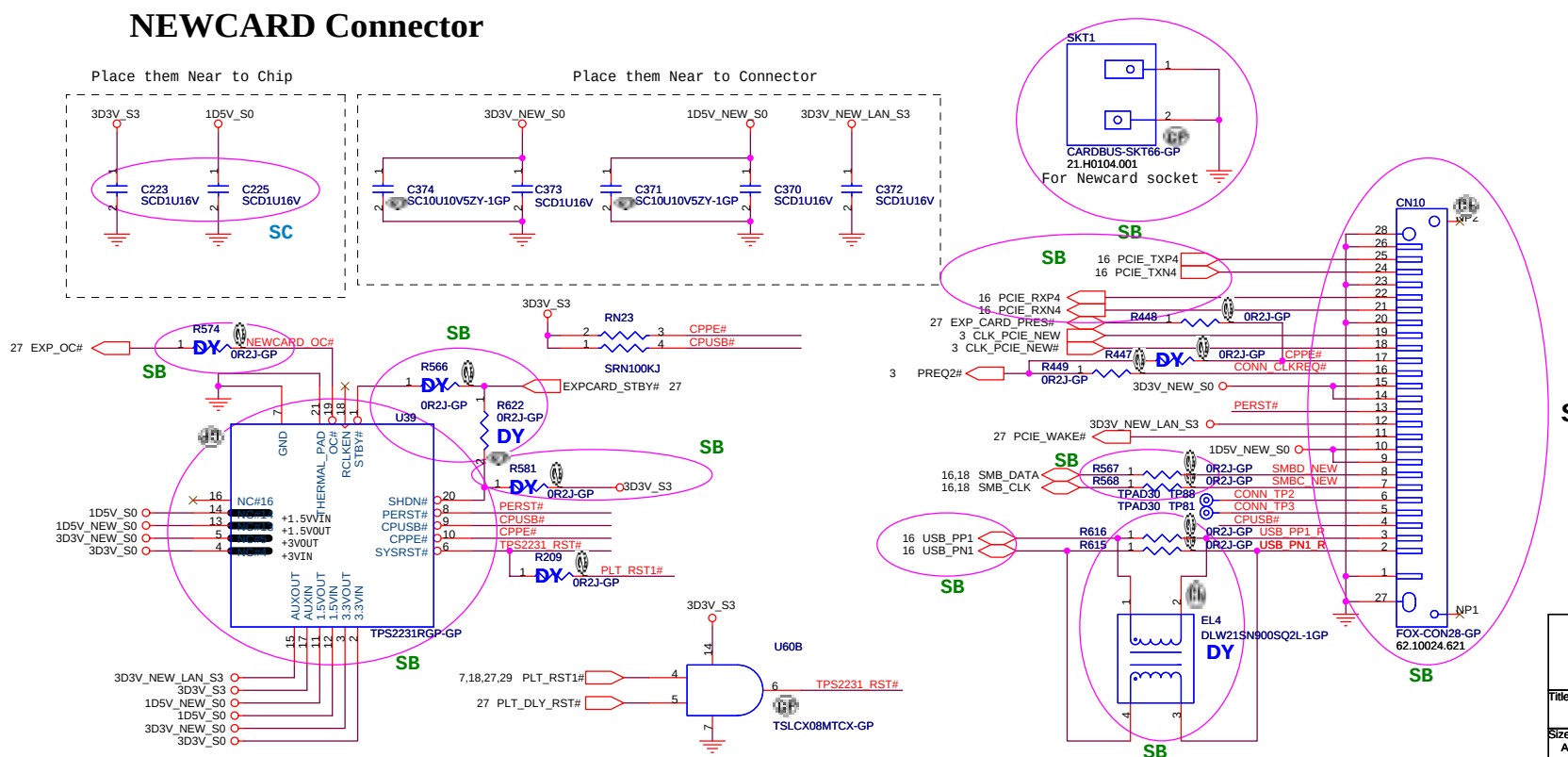
HDD Connector



CDROM



NEWCARD Connector



SMBUS(ICH6--NEWCARD,LAN)

華創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***HDD / CDROM / NEW CARD***	
Size A3	Document Number KeyWest	Rev SC
Date: Thursday, June 30, 2005	Sheet 20 of 37	

Broadcom LAN

BCM4401

LAN EEPROM

Close to power pin

Place near Chip

Place RDAC CKT as close to chip as possible

Place PLLVDD2_LAN/BIASVDD_LAN CKT as close to chip as possible

BCM4401 requires 16-Bit R/W data width

Atmal: AT93C46-10SI "72.93C46.R01" (Main source)
ST : M93C46-W "72.93C46.N01", (2nd source)
if use 2nd source R297 need to install

Note: The BCM4401L has weak internal pulldown resistors on the follow signals:

SPROM_CS,SPROM_CLK,SPROM_DOUT,SPROM_DIN

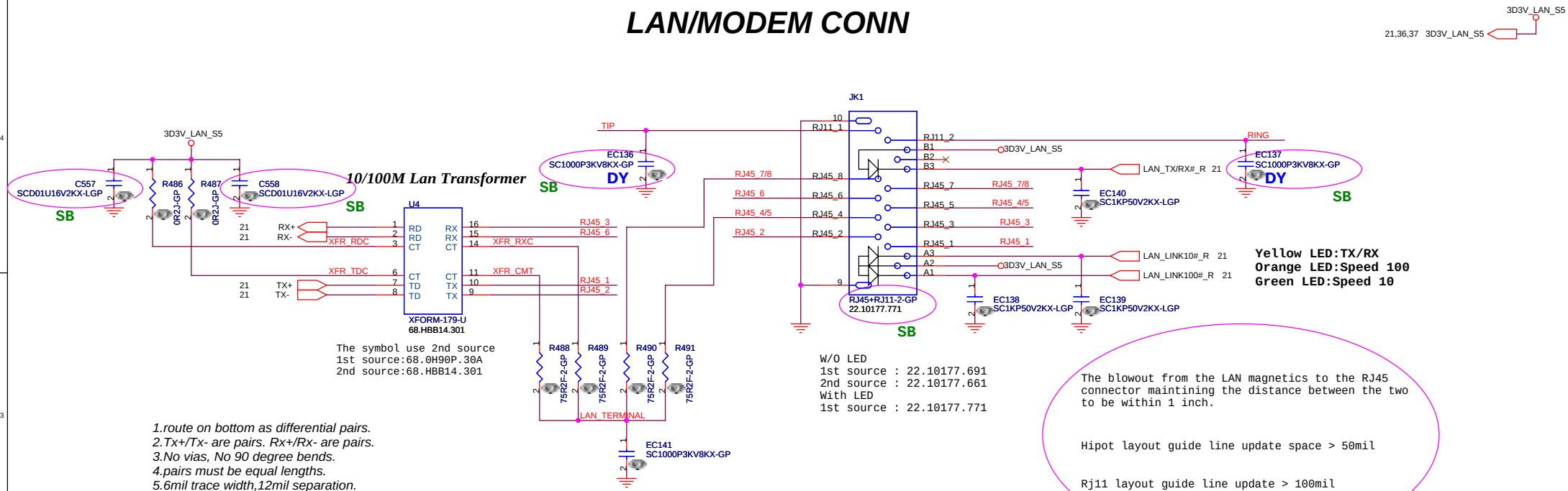
X6 CL=20pF±0.2pF
Freq. Tolerance:±30ppm

EXT_POR_L is an active low signal used to place the BCM4401 into IDDQ mode, <5 mA current consumption

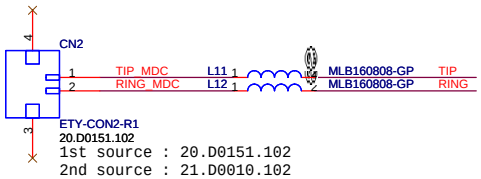
Change LAN solution

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	LAN BCM4401
Size: Custom	Document Number: KeyWest
Rev	SC
Date: Thursday, June 30, 2005	Sheet 21 of 37

LAN/MODEM CONN



10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

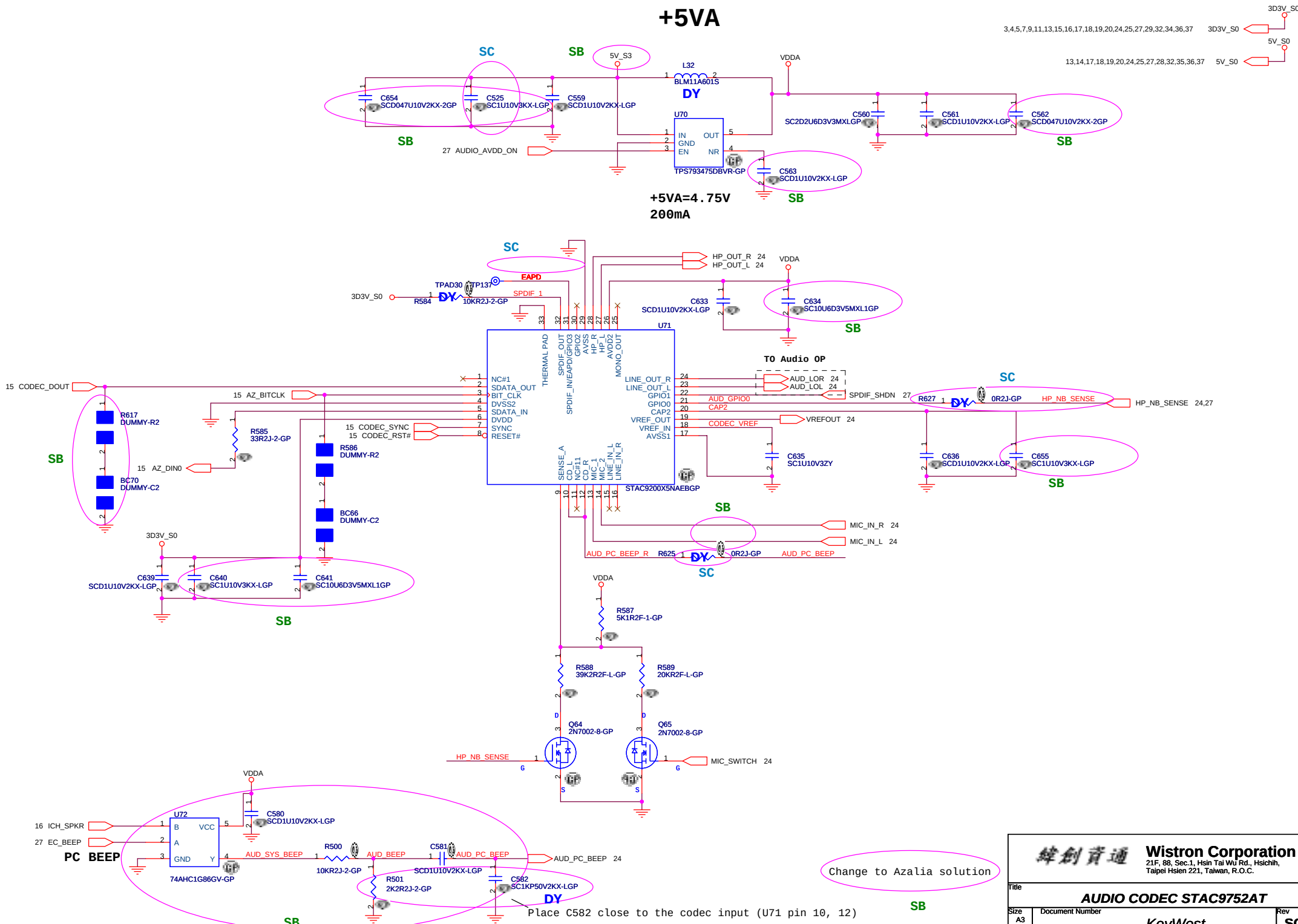


Change LAN solution

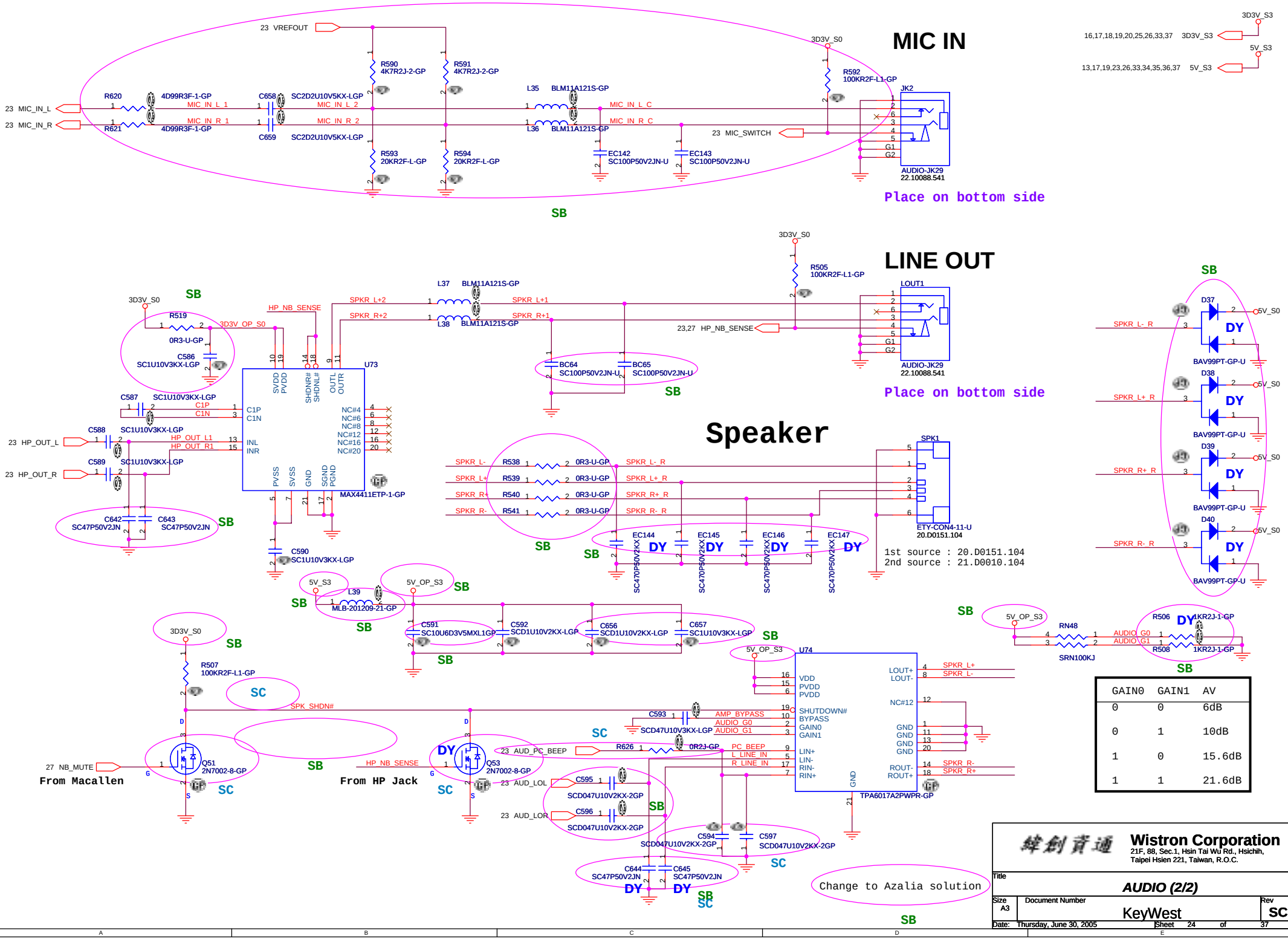
SB

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LAN Connector		
Size: A3	Document Number: KeyWest	Rev: SC
Date: Thursday, June 30, 2005	Sheet 22 of 37	

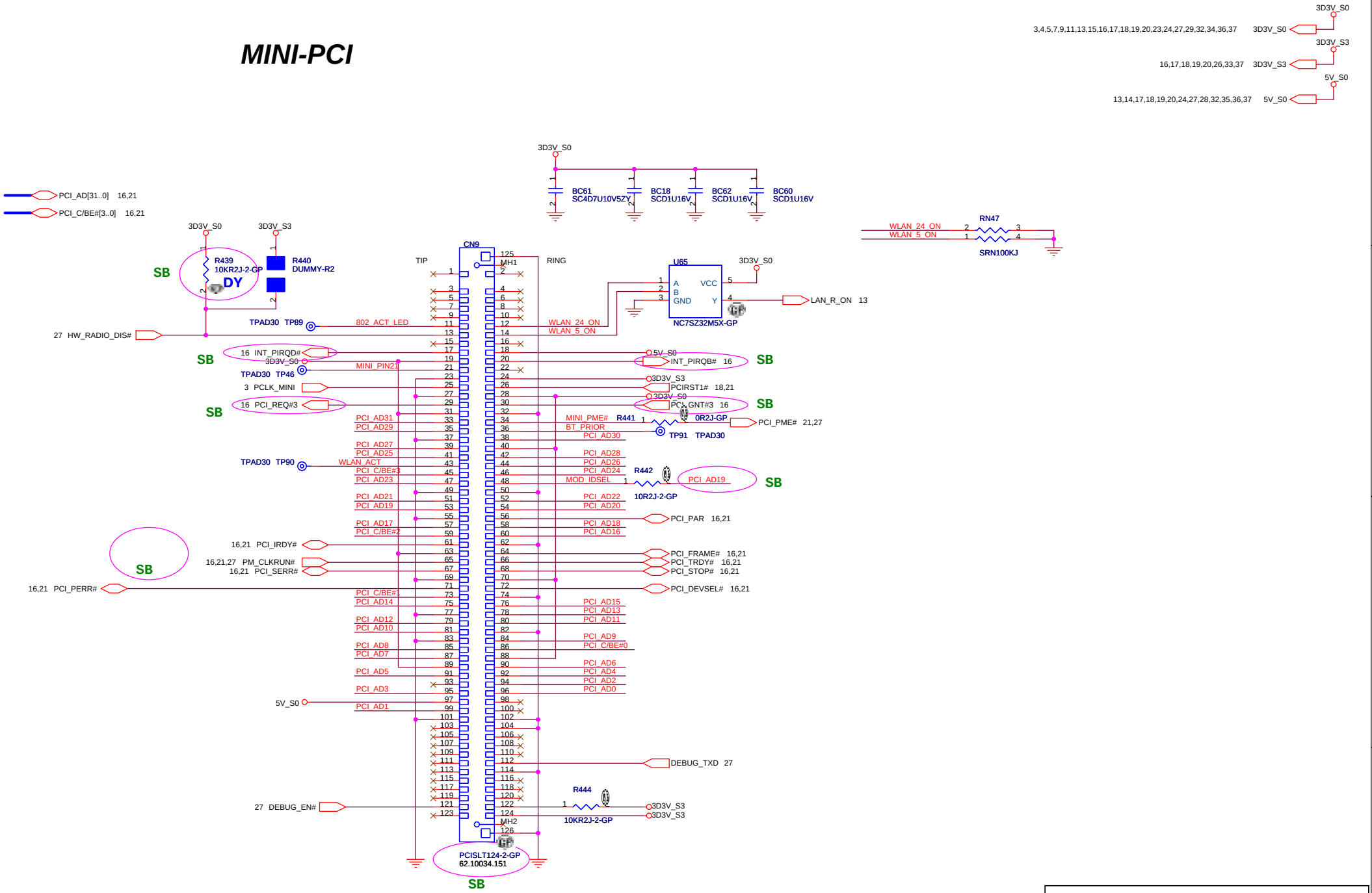
+5VA



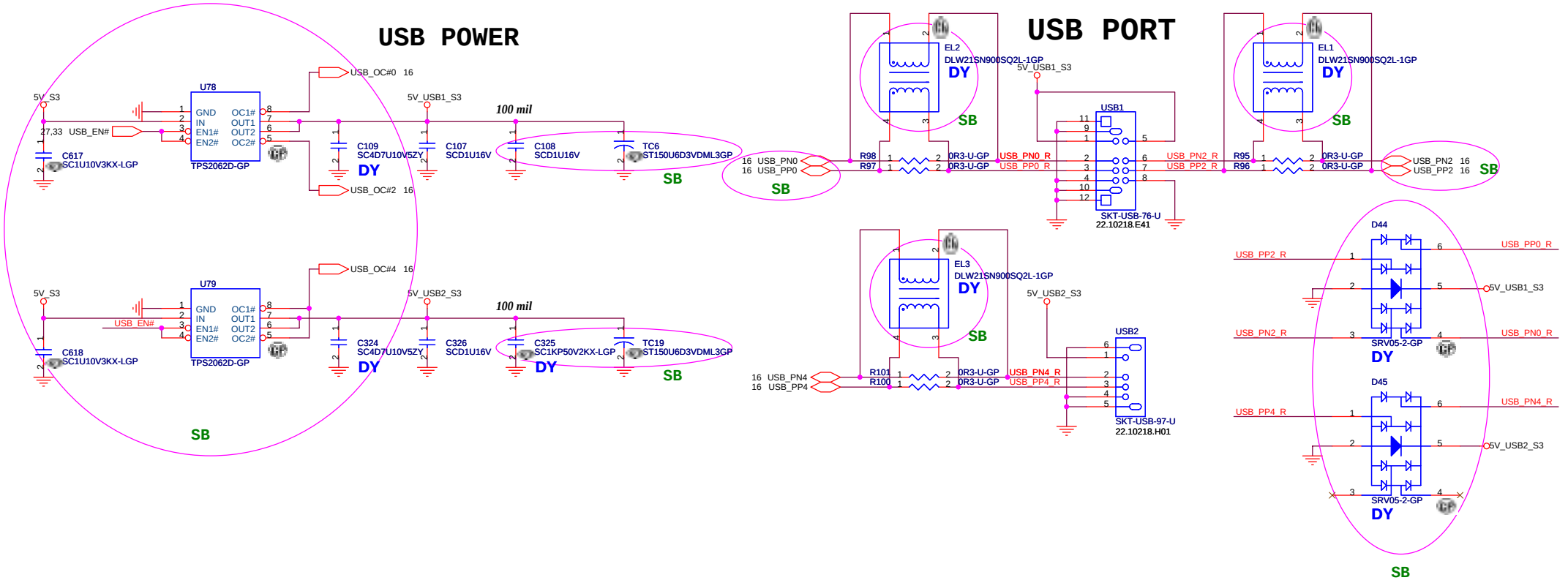
Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: AUDIO CODEC STAC9752AT		
Size: A3	Document Number: KeyWest	Rev: SC
Date: Thursday, June 30, 2005	Sheet 23 of 37	

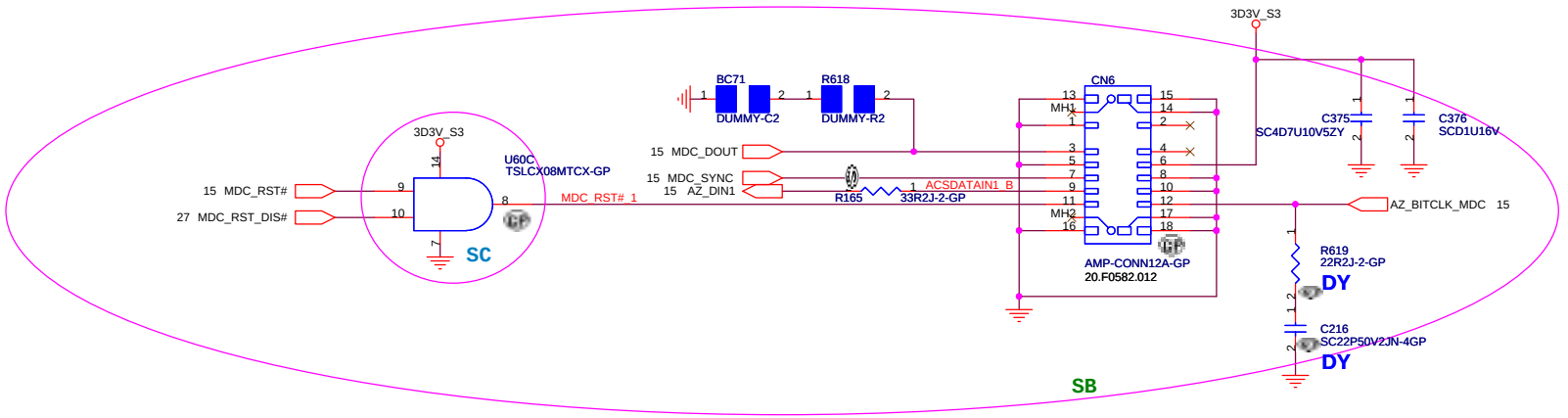

MIC IN
LINE OUT
Speaker
Place on bottom side
Place on bottom side
From Macallen
From HP Jack
Change to Azalia solution
1st source : 20.D0151.104
2nd source : 21.D0010.104
GAIN0 GAIN1 AV
0 0 6dB
0 1 10dB
1 0 15.6dB
1 1 21.6dB
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
AUDIO (2/2)
KeyWest
Date: Thursday, June 30, 2005
Sheet 24 of 37

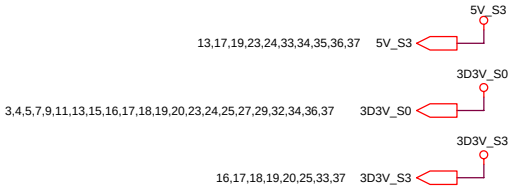
MINI-PCI



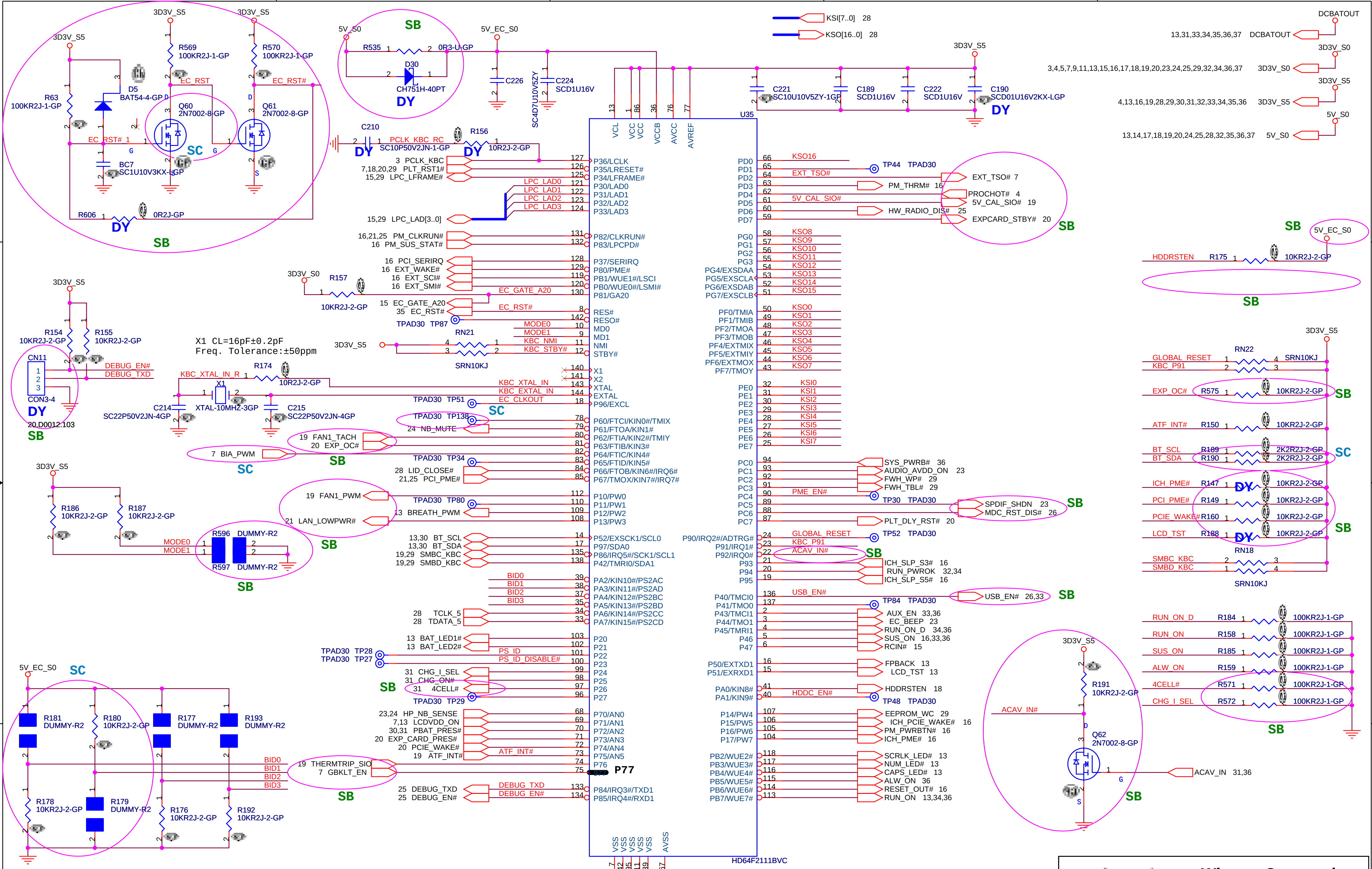
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***MINI-PCI***	
Size A3	Document Number KeyWest	Rev SC
Date: Thursday, June 30, 2005	Sheet 25 of 37	







華創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***USB / MDC CONN.***	
Size A3	Document Number KeyWest	Rev SC
Date: Thursday, June 30, 2005	Sheet 26 of 37	



BID3	BID2	BID1	BID0	Board Rev.
0	0	0	0	NFF
0	0	0	1	X00
0	0	1	0	X01
0	0	1	1	X02
0	1	0	0	X03
0	1	0	1	???

緯創資通

Wistron Corporation

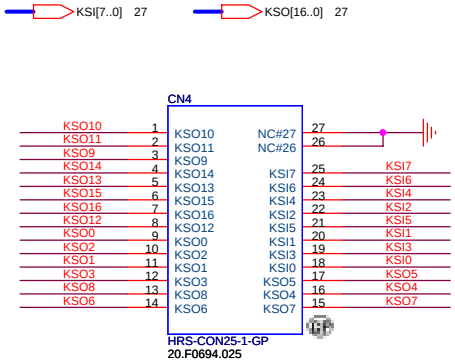
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **KBC_H8S/2160B**

Size: A3 | Document Number: **KeyWest** | Rev: **SC**

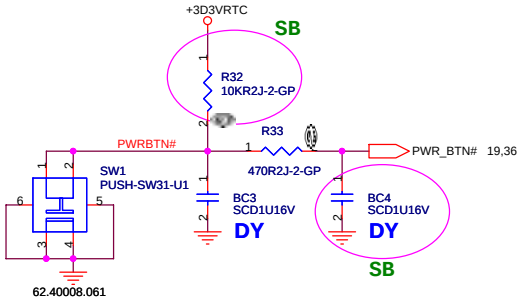
Date: Thursday, June 30, 2005 | Sheet 27 of 37

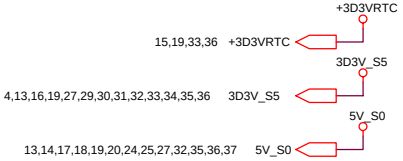
INTERNAL KEYBOARD CONNECTOR



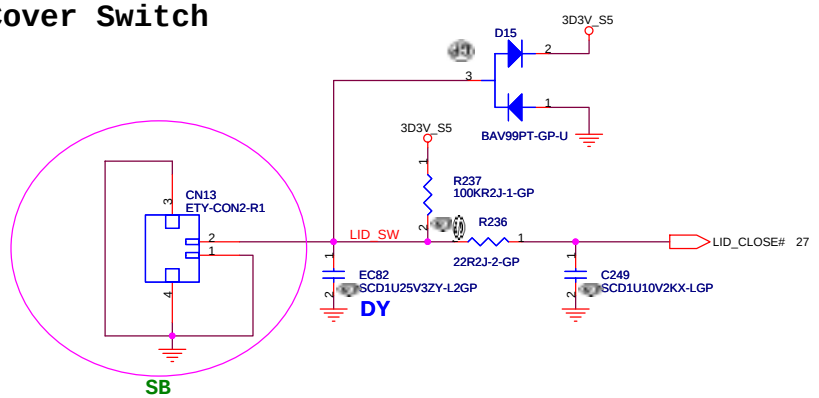
1st source : 20.F0694.025
2nd source : 20.F0642.025

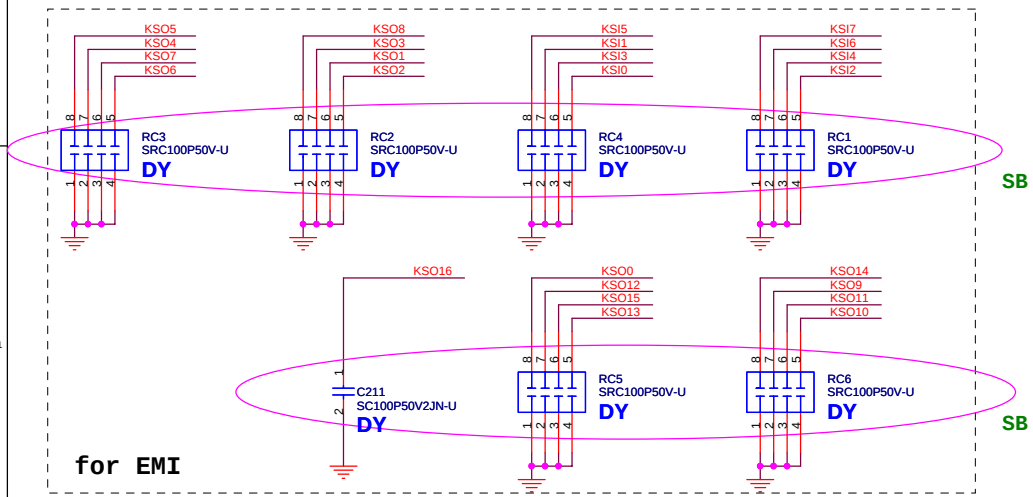
POWER BUTTON



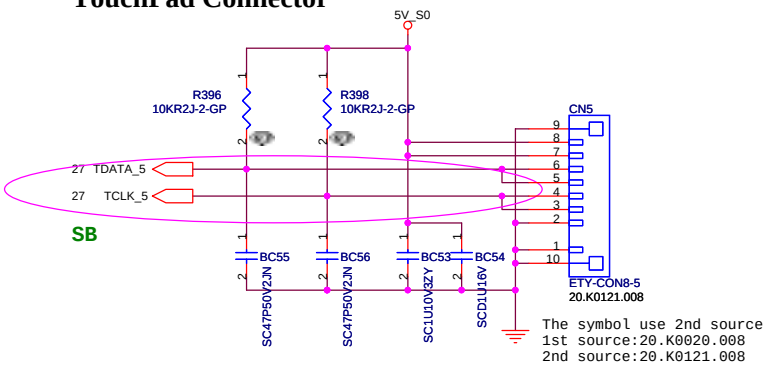


Cover Switch





TouchPad Connector



The symbol use 2nd source
1st source:20.K0020.008
2nd source:20.K0121.008

<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***KB / TPAD / LID SW / PWR BTN***	
Size A3	Document Number ***KeyWest***	Rev **SC**
Date: Thursday, June 30, 2005	Sheet 28 of 37	

3D3V_S5

4,13,16,19,27,28,30,31,32,33,34,35,36 3D3V_S5

512KB Flash

Unused FGPI pins must not be float

LPC_LAD[3..0] 15,27

RP1
SELECT_FWH 1
FWH_FGPI4 2
FWH_FGPI3 3
FWH_FGPI2 4
5
10
9
8
7 FWH_FGPI1
6 FWH_FGPI0
SRP10K

SB

3D3V_S0

C242 SCD1U16V

C241 SC1U10V3ZY

LPC_LFRAME# 15,27
FWH_INIT# 15
PLT_RST1# 7,18,20,27
SELECT_FWH

PCLK_FWH 3

R227 DUMMY-R3

PCLK_FWH_RC

C243 DUMMY-C3

U40

RN20

SRN10KJ

27 FWH_TBL#
27 FWH_WP#

A0/ID0
A1/ID1
A2/ID2
A3/ID3
A4/TBL#
A5/WP#
A6/FGPI0
A7/FGPI1
A8/FGPI2
A9/FGPI3
A10/FGPI4

FWH_FGPI0
FWH_FGPI1
FWH_FGPI2
FWH_FGPI3
FWH_FGPI4

VDD VDD
VSS VSS
WE#/FWH4
OE#/INIT#
R/C#/CLK
RST#
IC
NC#27 NC#26 NC#22 NC#1

DQ0/FWH0
DQ1/FWH1
DQ2/FWH2
DQ3/FWH3
DQ4/RES
DQ5/RES
DQ6/RES
DQ7/RES

LPC_LAD0
LPC_LAD1
LPC_LAD2
LPC_LAD3

49LF004B334C-GP
72.49004.F03

SCOKET:
62.10002.032
62.10005.032

SMBus address A2

User Password

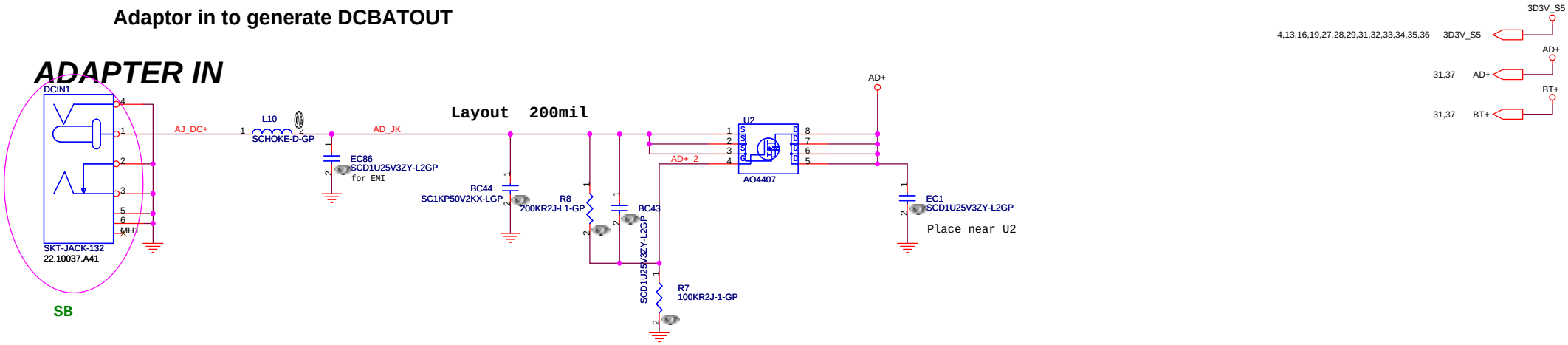
U32
A0 A1 A2 GND
VCC WP SCL SDA
AT24C04N-10SU-GP

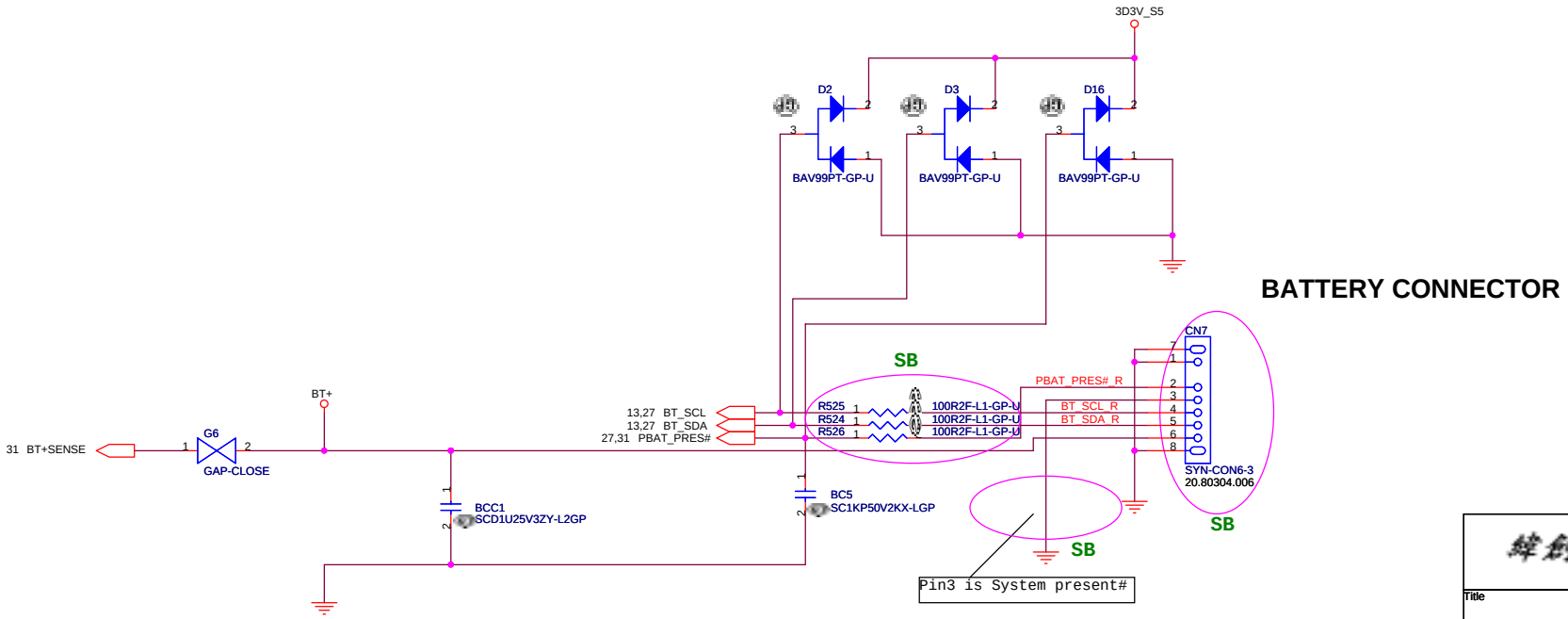
C188
SCD1U10V2KX-LGP

EEPROM_WC 27
SMBC_KBC 19,27
SMBD_KBC 19,27

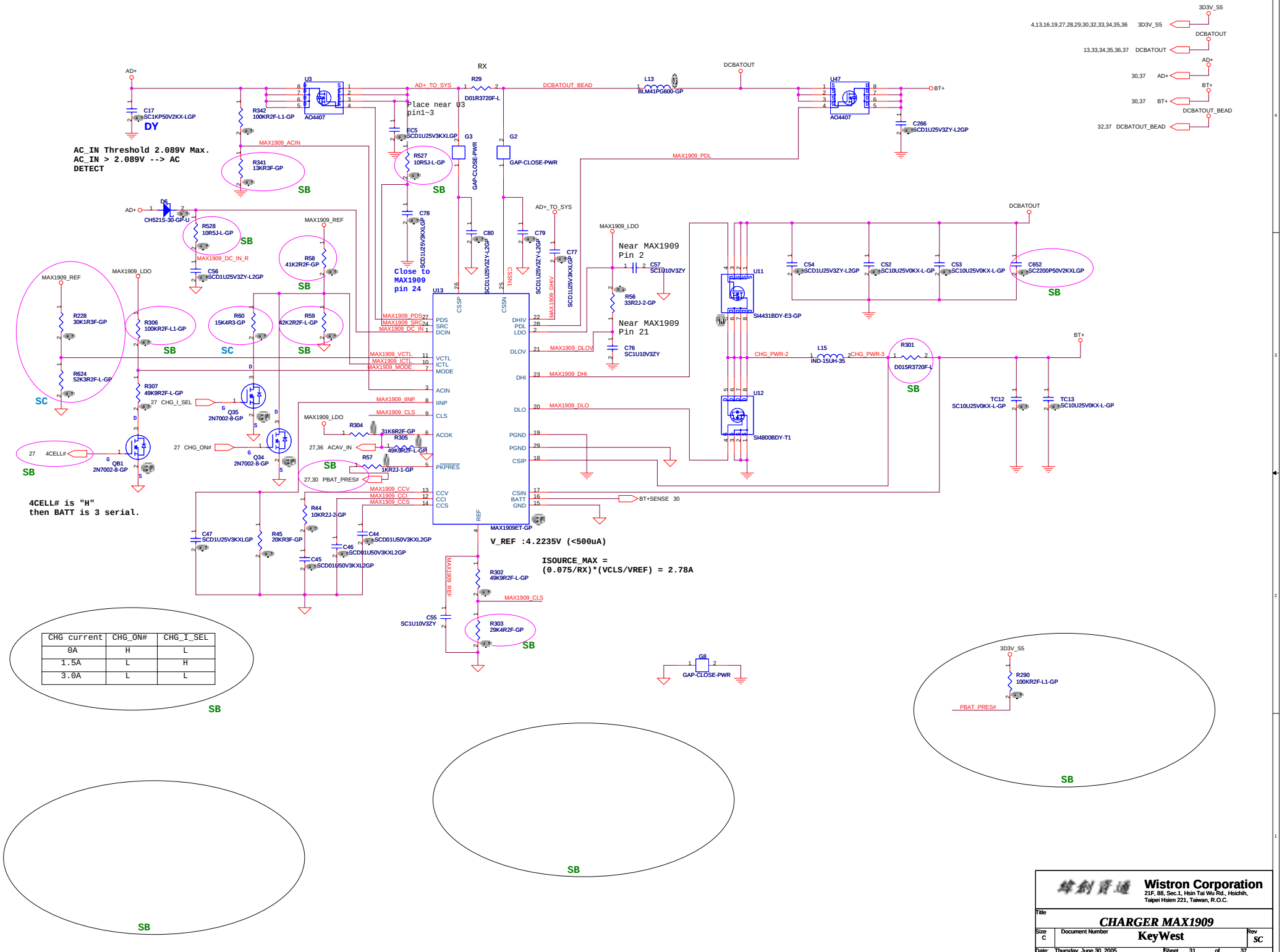
華創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***BIOS***	
Size A3	Document Number ***KeyWest***	Rev **SC**
Date: Thursday, June 30, 2005	Sheet 29 of 37	

Adaptor in to generate DCBATOUT





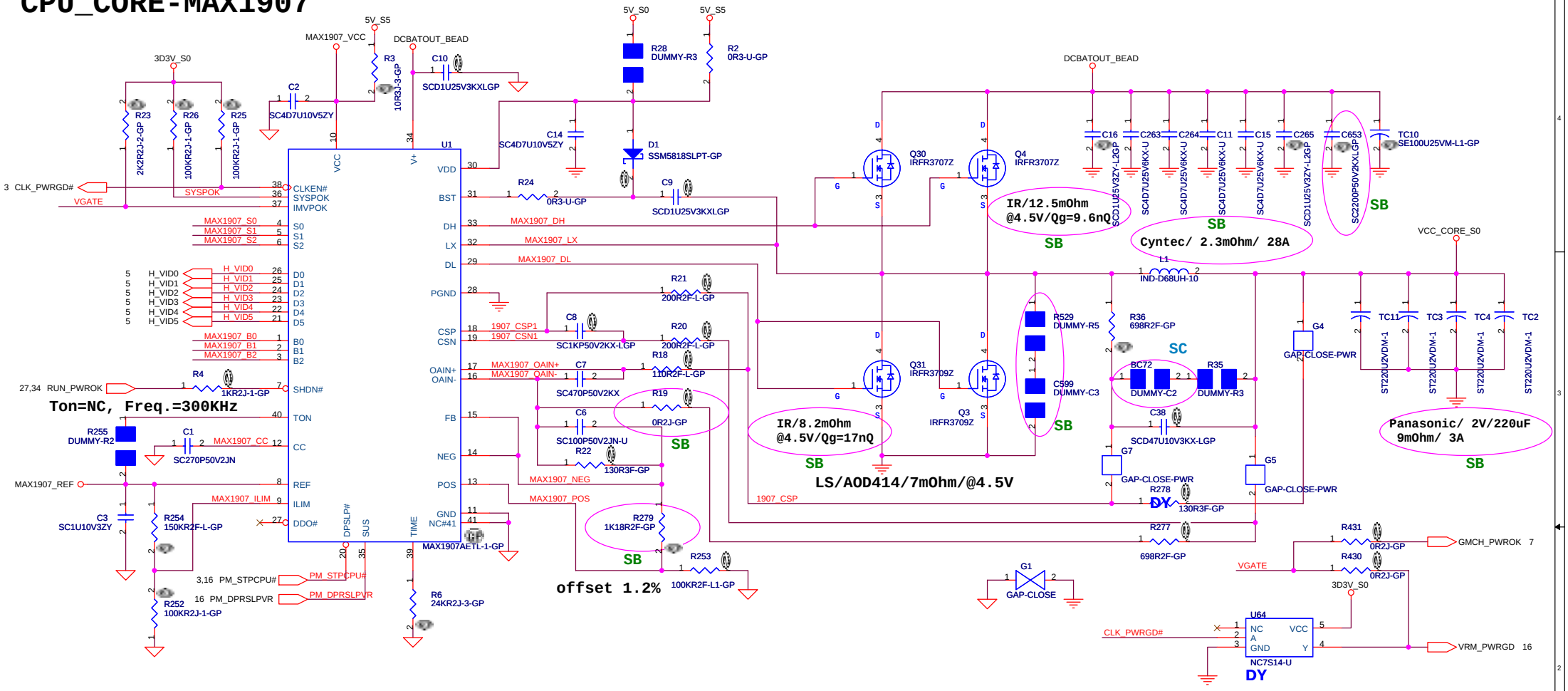
Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Adaptor/ Bettery conn.*		
Size: A3	Document Number: KeyWest	Rev: SC
Date: Thursday, June 30, 2005	Sheet 30 of 37	



CHG current	CHG_ON#	CHG_I_SEL
0A	H	L
1.5A	L	H
3.0A	L	L

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	CHARGER MAX1909
Size C	Document Number KeyWest
Rev SC	
Date: Thursday, June 30, 2005	Sheet 31 of 37

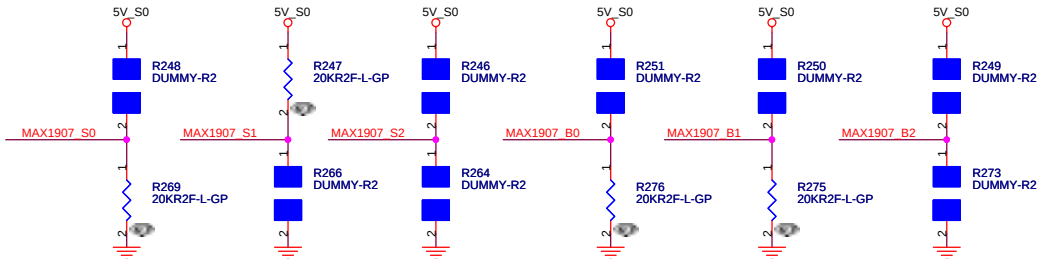
CPU_CORE-MAX1907



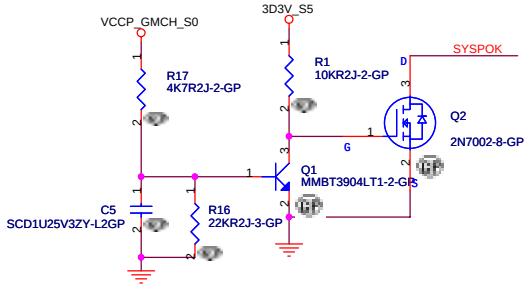
OCP=30A, Vally current = 27.5A,
Vilim=550mV(55mVp-p*10)

Deeper Sleep Voltage : 0.748V
, S0=L, S1=H, S2=Open,

Boot-up Voltage : 1.2V
, B0=L, B1=L, B2=Open



VID						Vcore
VID5	VID4	VID3	VID2	VID1	VID0	V
0	1	0	1	1	1	1.340
0	1	1	0	0	0	1.324
0	1	1	0	1	0	1.292
0	1	1	1	0	0	1.260
0	1	1	1	0	1	1.244
0	1	1	1	1	1	1.212
1	0	0	0	0	1	1.180
1	0	0	0	1	1	1.148
1	0	0	1	1	0	1.100
1	0	1	0	0	1	1.052
1	0	1	0	1	1	1.020
1	0	1	1	1	0	0.972
1	1	0	0	0	0	0.940



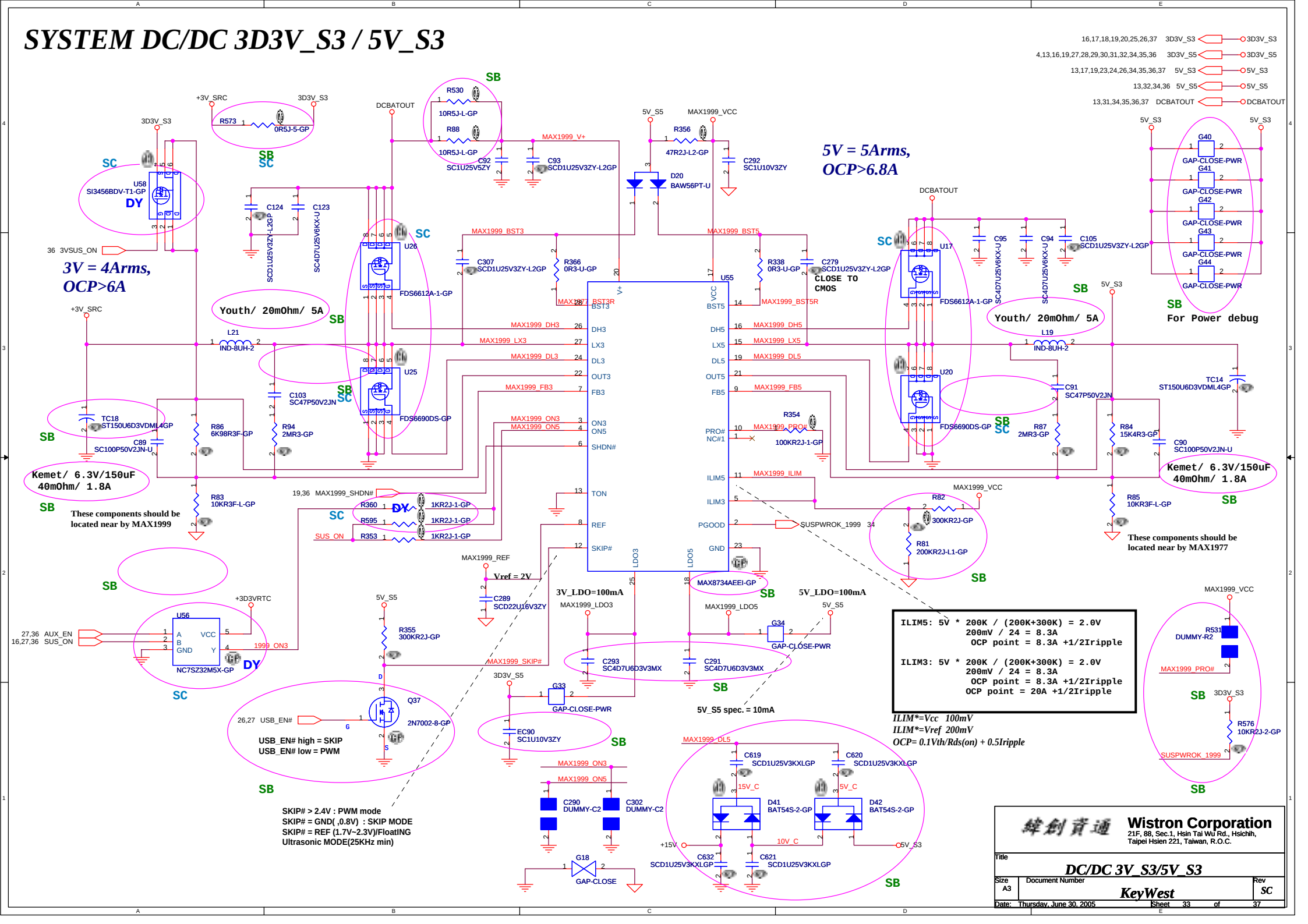
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IMVP IV-CPU POWER-MAX1907

Size: A3 | Document Number: KeyWest | Rev: SC

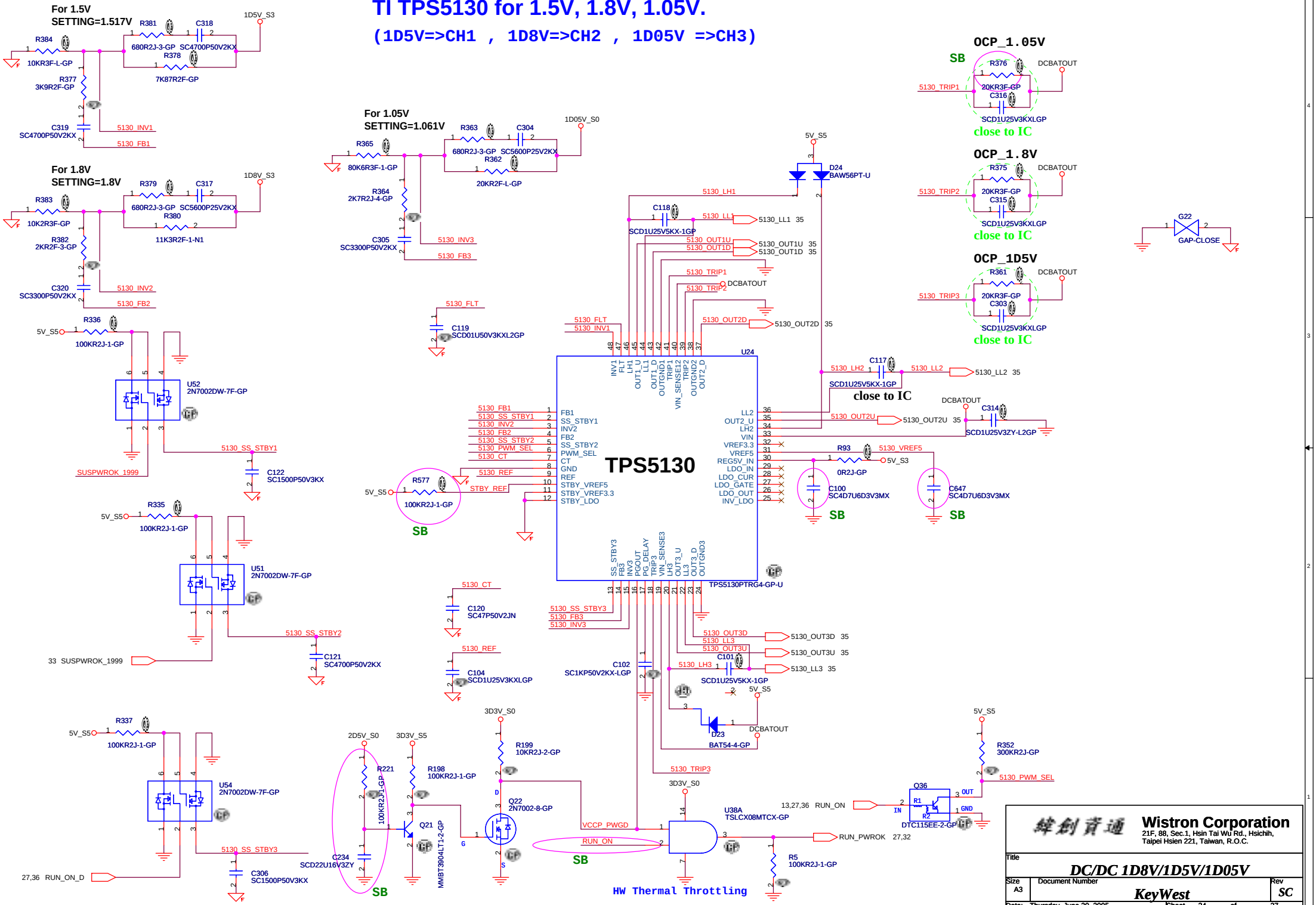
Date: Thursday, June 30, 2005 | Sheet 32 of 37

SYSTEM DC/DC 3D3V_S3 / 5V_S3



TI TPS5130 for 1.5V, 1.8V, 1.05V.

(1D5V=>CH1 , 1D8V=>CH2 , 1D05V =>CH3)



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	DC/DC 1D8V/1D5V/1D05V	
Size: A3	Document Number: KeyWest	Rev: SC
Date: Thursday, June 30, 2005	Sheet 34 of 37	

TI TPS5130 for 1.5V, 1.8V, 1.05V

(1D5V=>CH1 , 1D8V=>CH2 , 1D05V =>CH3)

13,31,33,34,36,37 DCBATOUT
13,32,33,34,36 5V_S5
10,34,36,37 1D05V_S0
7,9,10,11,12,16,34,36,37 1D8V_S3
13,14,17,18,19,20,24,25,27,28,32,36,37 5V_S0
12,36 0D9V_S0
17,34,36 1D5V_S3

DCBATOUT
U29 SI4800BDY-T1
C133 SCD1U25V3ZY-L2GP
C134 SC4D7U25V6KX-U
VISHAY/30mOhm
@4.5V/Qg=8.7nQ
SB
1D5V/5A
OCP=10A
L22 IND-4D7UH-56
1D5V_S3
34 5130_OUT1U
34 5130_LL1
5130_OUT1U
5130_LL1
U28 IRF7807ZPBF-GP
Rds(on)=20mOhm
YOUTH/16mOhm/ 7A
SB
Panasonic/2V/220uF
9mOhm/3A
SB
TC17 ST220U2VDM-1
IR/18.2mOhm
@4.5V/Qg=7.2nQ
SB
34 5130_OUT1D
5130_OUT1D

1D5V_S3 G45 GAP-CLOSE-PWR SB
For Power debug

1D8V_S3 G46 G47 G48 G49 G50 G51 GAP-CLOSE-PWR SB
For Power debug

DCBATOUT
U22 SI4800BDY-T1
C115 SCD1U25V3ZY-L2GP
C116 SC4D7U25V6KX-U
1D8V/5A
OCP=10A
L20 IND-4D7UH-56
1D8V_S3
34 5130_OUT2U
34 5130_LL2
5130_OUT2U
5130_LL2
U23 IRF7807ZPBF-GP
Rds(on)=20mOhm
YOUTH/16mOhm/ 7A
SB
TC16 ST220U4VDM-L7-GP
KEMENT/4V/220uF
40mOhm/ 1.8A
SB
34 5130_OUT2D
5130_OUT2D

DCBATOUT
U19 SI4800BDY-T1
C87 SCD1U25V3ZY-L2GP
C88 SC4D7U25V6KX-U
1D05V/5A
OCP=10A
L18 IND-4D7UH-56
1D05V_S0
34 5130_OUT3U
34 5130_LL3
5130_OUT3U
5130_LL3
U16 IRF7807ZPBF-GP
Rds(on)=20mOhm
YOUTH/16mOhm/ 7A
SB
R80 1KR2J-1-GP DY
TC5 ST220U4VDM-L6-GP
KEMENT/4V/220uF
25mOhm/ 2.2A
SB
34 5130_OUT3D
5130_OUT3D

For DDR REF S3 Power

1D8V_S3
C186 SCD1U25V3KXLGP
C187 SCD1U25V3KXLGP
R142 220R3F-1-GP
R144 220R3F-1-GP
DDR_VREF_1
U33 G1214 DY
5V_S3
C204 SCD1U16V
C203 SCD1U16V
R143 0R3-U-GP
DDR_VREF_S3
VREFOUT = 0.9V

DDR_VREF_S3 need
10 mil and must
neat NB and DIMM

Power budget:0.9V/2.2Apeak (For DDR2_VTT)

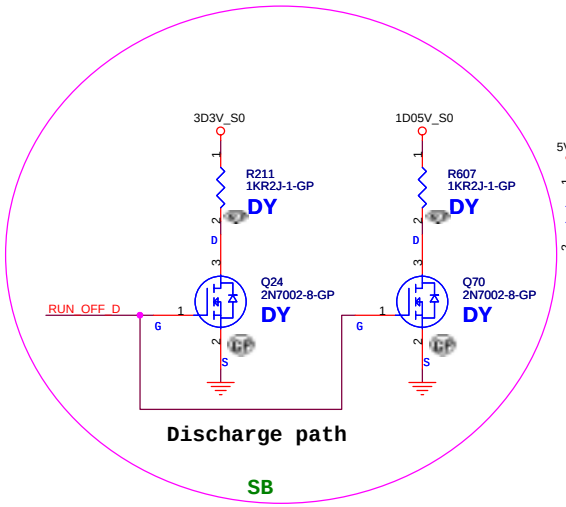
0D9V / 1A
0D9V_S0
1D8V_S3
5V_S0
U63 APL5331KAC-TRLGP
C345 SC10U10V5ZY-1GP
TC8 SE220U16VM-L-GP DY
C353 SC10U10V5ZY-1GP
TC21 ST150U4VBM-L2-GP
C352 SCD1U10V2KX-LGP
C346 SCD1U10V2KX-LGP
R414 1KR2F-3-GP DY
R145 0R2J-GP
R415 1KR2F-3-GP DY
APL5331_VREF1
DDR_VREF_1
3D3V_S5 SB
C271 SCD1U10V2KX-LGP

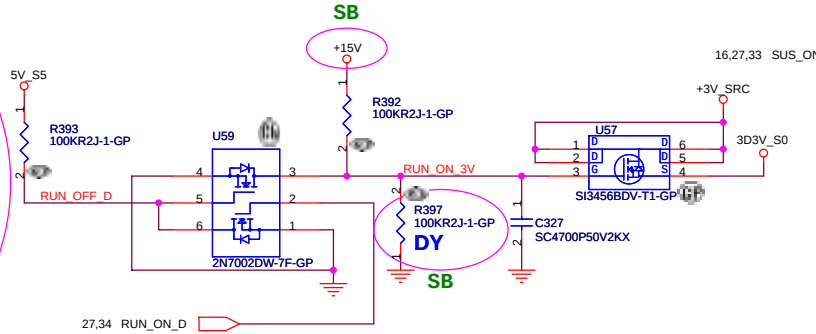
L3# circuit

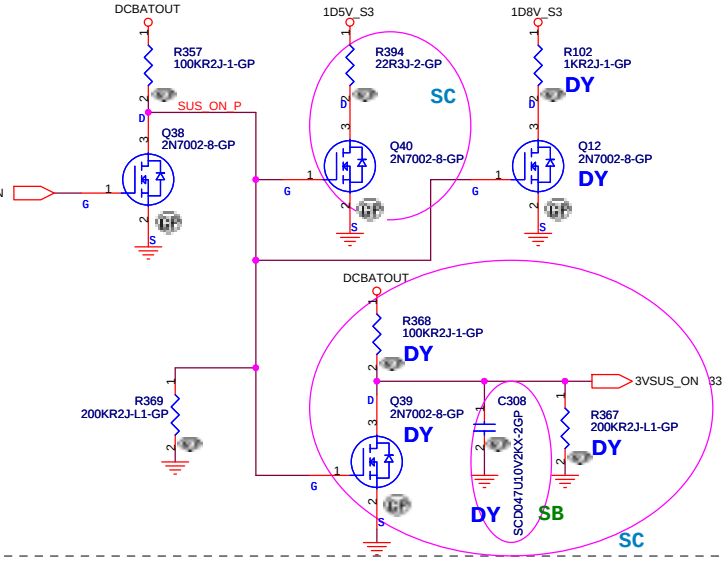
3D3V_S5
R340 100KR2J-1-GP
R339 33KR2J-3-GP
R300 100KR2J-1-GP
HTH
U53 G680LT1F-GP
BL3#
D19 BAT54-4-GP DY
EC_RST# 27

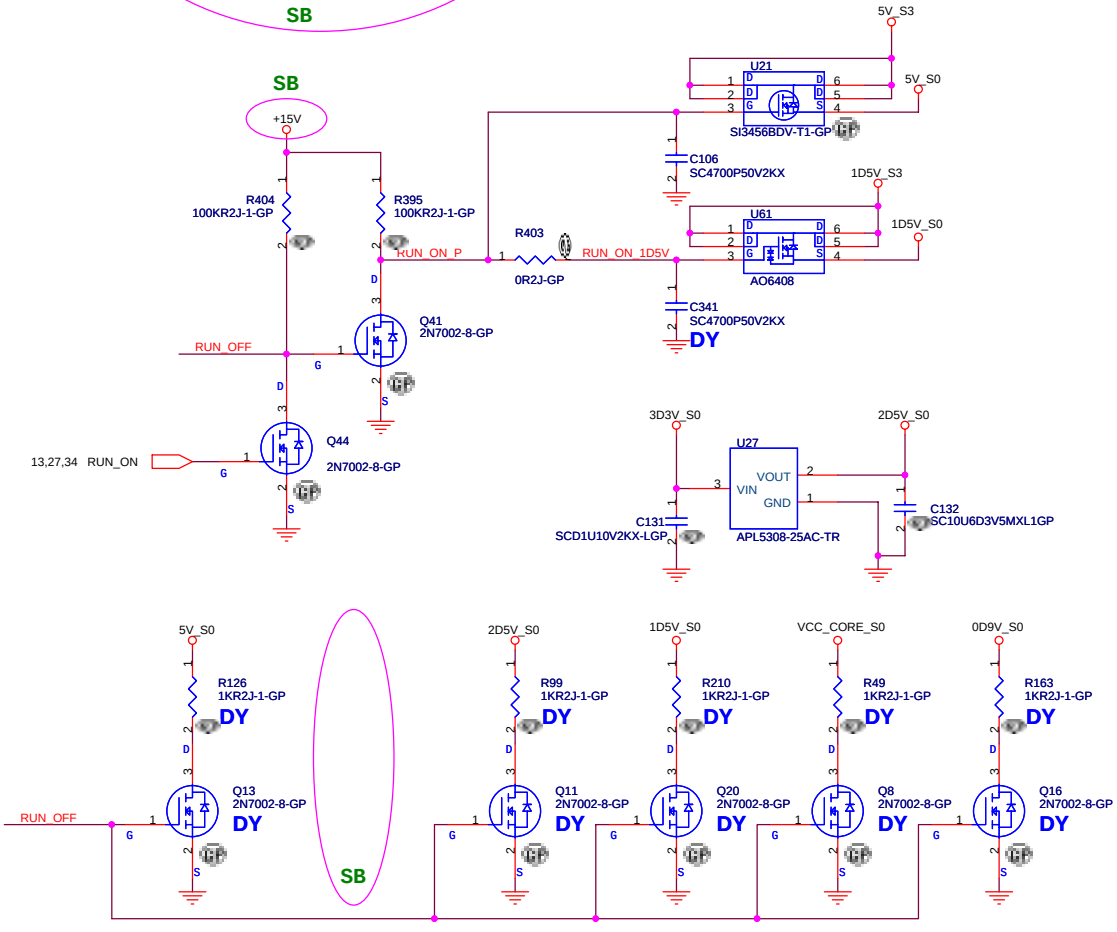
Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	39.DC/DC 1D8V/1D5V/1D05V-2
Size A3	Document Number KeyWest
Rev	SC
Date: Thursday, June 30, 2005	Sheet 35 of 37

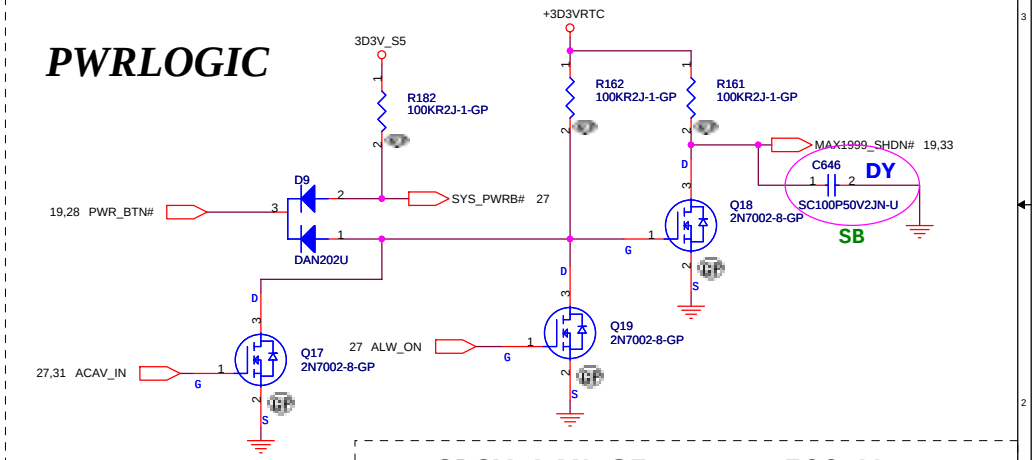
Run Power

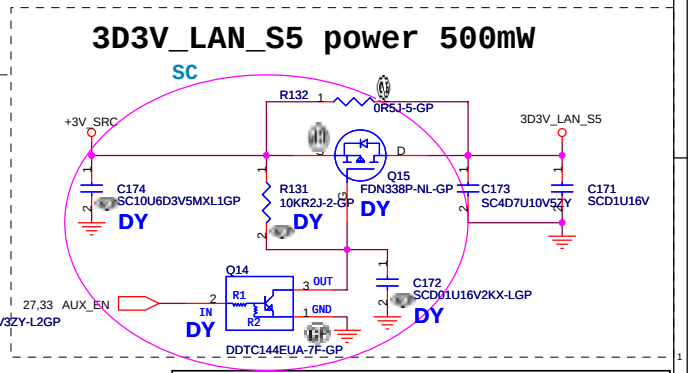


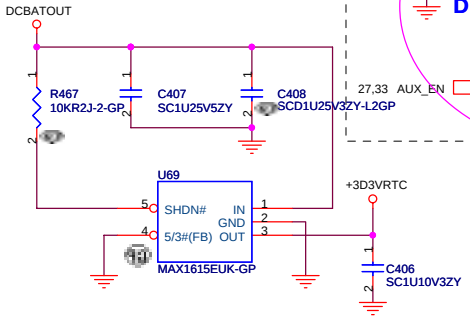




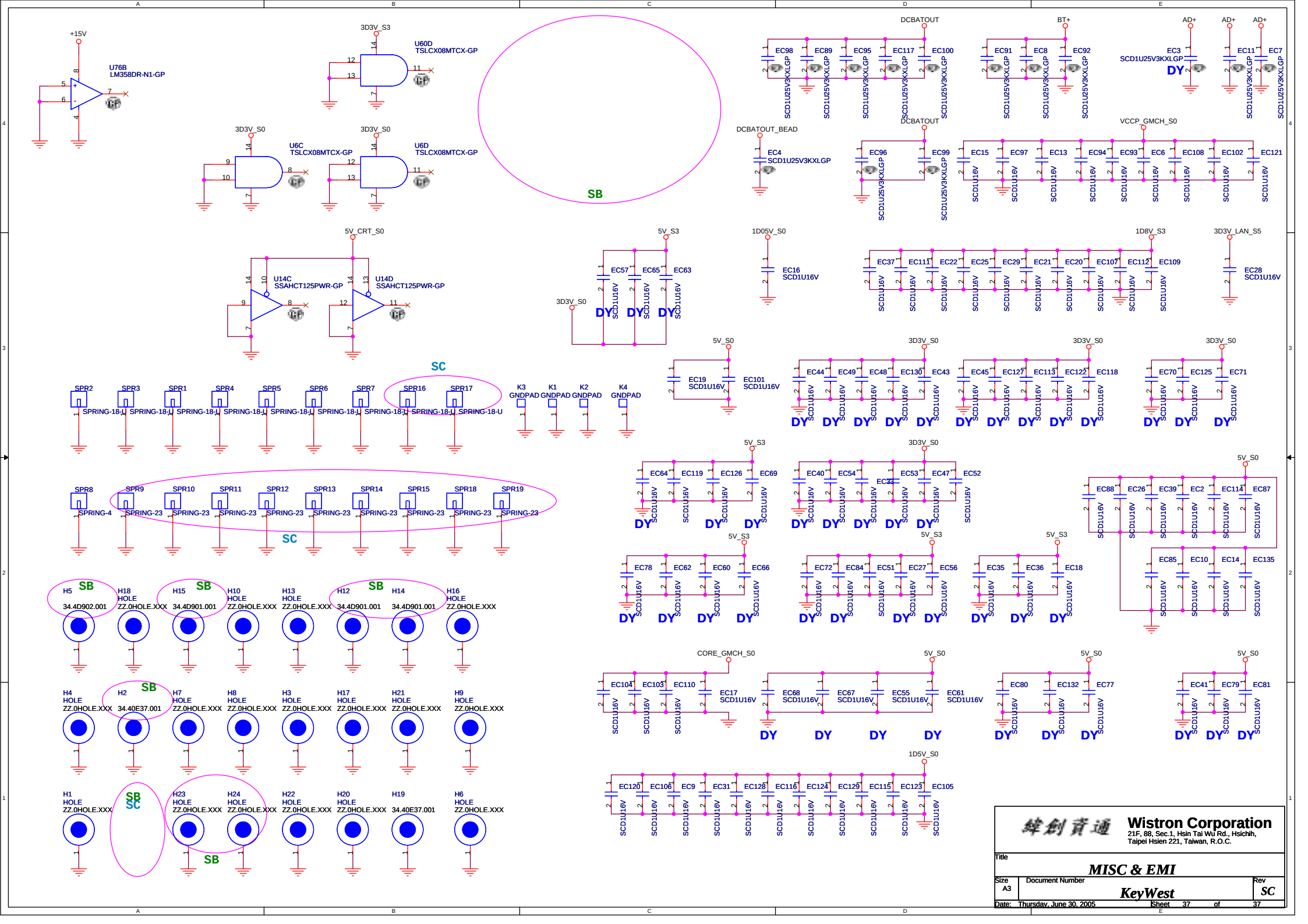








Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: PWRPLANE&PWRLOGIC		
Size: A3	Document Number: KeyWest	Rev: SC
Date: Thursday, June 30, 2005	Sheet 36 of 37	


+15V
U76B
LM358DR-N1-GP
3D3V_S3
U60D
TSLCX08MTCX-GP
3D3V_S0
U6C
TSLCX08MTCX-GP
U6D
TSLCX08MTCX-GP
SB
DCBATOUT
EC98 EC89 EC95 EC117 EC100
SCD1U25V3KXLGP
BT+
EC91 EC8 EC92
AD+
EC3 EC11 EC7
DY
DCBATOUT_BEAD
EC4
VCCP_GMCH_S0
EC96 EC99
EC15 EC97 EC13 EC94 EC93 EC6 EC108 EC102 EC121
SCD1U16V
5V_CRT_S0
U14C
SSAHCT125PWR-GP
U14D
SSAHCT125PWR-GP
5V_S3
EC57 EC65 EC63
1D05V_S0
EC16
1D8V_S3
EC37 EC111 EC22 EC25 EC29 EC21 EC20 EC107 EC112 EC109
3D3V_LAN_S5
EC28
SC
SPR2 SPR3 SPR1 SPR4 SPR5 SPR6 SPR7 SPR16 SPR17
SPRING-18-U
K3 K1 K2 K4
GNDPAD
5V_S0
EC19 EC101
3D3V_S0
EC44 EC49 EC48 EC130 EC43
EC45 EC127 EC113 EC122 EC118
EC70 EC125 EC71
SPR8 SPR9 SPR10 SPR11 SPR12 SPR13 SPR14 SPR15 SPR18 SPR19
SPRING-4
SPRING-23
EC64 EC119 EC126 EC69
EC40 EC54 EC53 EC47 EC52
EC88 EC26 EC39 EC2 EC114 EC87
EC85 EC10 EC14 EC135
EC78 EC62 EC60 EC66
EC72 EC84 EC51 EC27 EC56
EC35 EC36 EC18
H5 H18 H15 H10 H13 H12 H14 H16
HOLE
ZZ.0HOLE.XXX
34.4D902.001
34.4D901.001
H4 H2 H7 H8 H3 H17 H21 H9
34.40E37.001
H1 H23 H24 H22 H20 H19 H6
CORE_GMCH_S0
EC104 EC103 EC110 EC17
EC68 EC67 EC55 EC61
SCD1U16V
EC80 EC132 EC77
EC41 EC79 EC81
1D5V_S0
EC120 EC106 EC9 EC31 EC128 EC116 EC124 EC129 EC115 EC123 EC105
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
MISC & EMI
Size
A3
Document Number
KeyWest
Rev
SC
Date: Thursday, June 30, 2005
Sheet 37 of 37