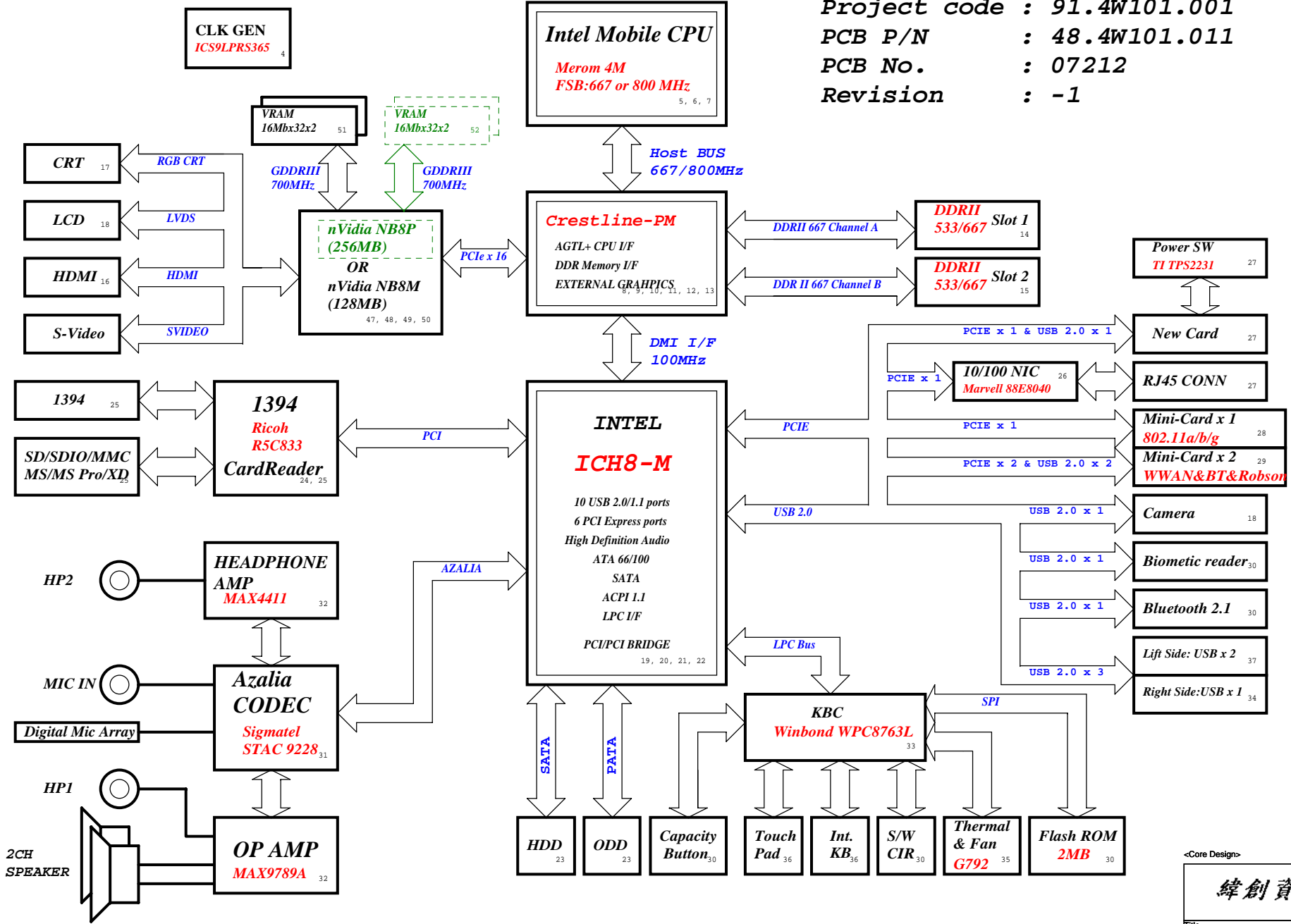


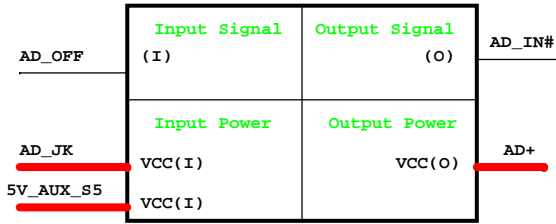
Hawke Intel Discrete Block Diagram

Project code : 91.4W101.001
 PCB P/N : 48.4W101.011
 PCB No. : 07212
 Revision : -1

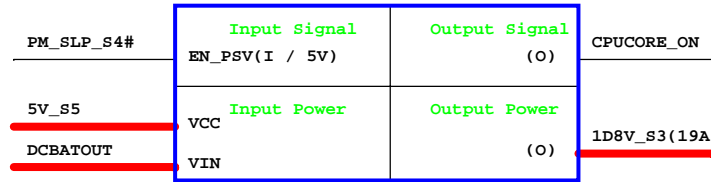


BATTERY CHARGER MAX8731A ₃₈	
INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT
SYSTEM DC/DC TPS51120 ₃₉	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5
SYSTEM DC/DC TPS5117 _{42, 43}	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3
SYSTEM DC/DC TPS51100 ₄₄	
INPUTS	OUTPUTS
1D8V_S3	0D9V_S3
SYSTEM DC/DC RT9018 ₄₄	
INPUTS	OUTPUTS
1D8V_S3 1D8V_S3	1D5V_S0 1D25V_S0
VGA DC/DC TPS5117 ₅₃	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFX_CORE_S0
CPU DC/DC ISL6262A ₄₀	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
PCB LAYER	
L1: TOP	
L2: GND	
L3: Signal	
L4: Signal	
L5: VCC	
L6: Singal	
L7: GND	
L8: BOT	

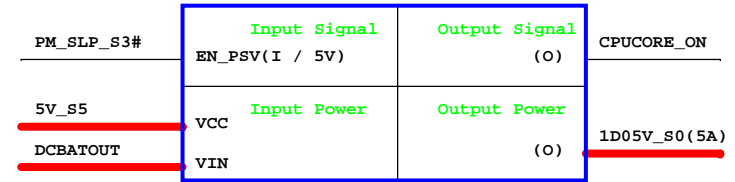
Adapter



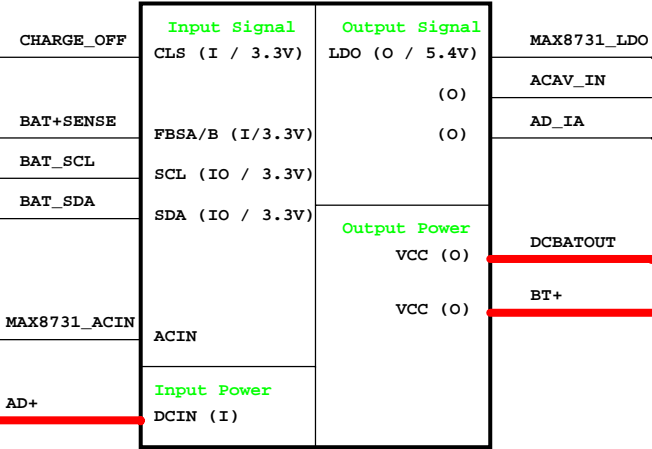
TPS51117 1D8V



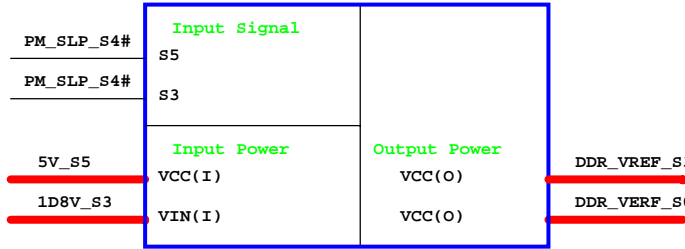
TPS51117 1D05V



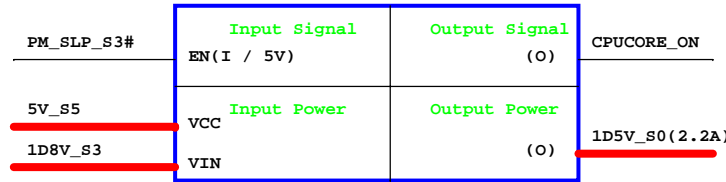
Charger MAX8731A



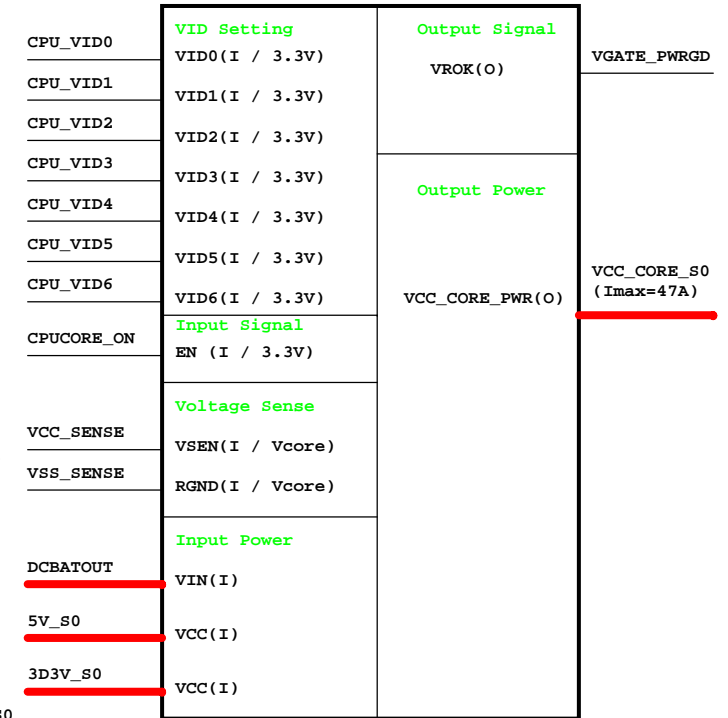
TI TPS51100 0.9V/DDR_VREF_S3



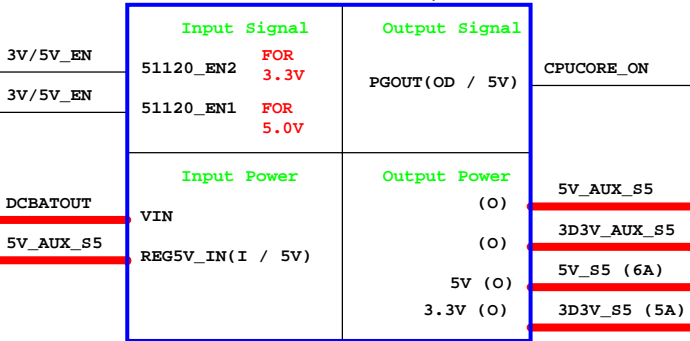
RT9018A 1D5V



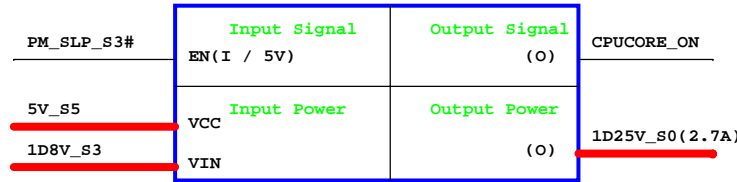
ISL6262A CPU_CORE



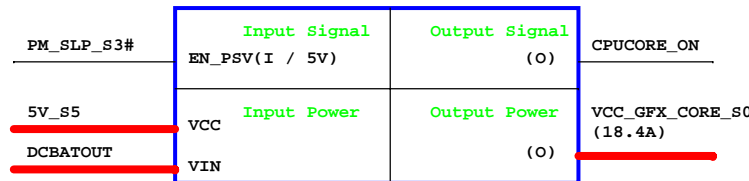
TI TPS51120 3D3V/5V



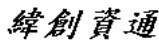
RT9018A 1D25V



TPS51117 VGA_CORE



<Core Design>

 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
Power Block Diagram		
Size A3	Document Number	Rev
	Hawke-Intel	-1
Date: Sunday, September 09, 2007		
Sheet		57

INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIe Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIe Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIe Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWB BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCL1_5 VRM Enable/Disable.Always sampled.	Enables integrated VccSus1_05,VccSus1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIe LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overridden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

ICH_RSVP_Tp3	AZ_DOUT_ICH	Description
0	1	RVSD
1	1	Enter XOR Chain
0	0	Normal Operation(default)
1	1	set PCIe port cofig bit1

PCI_GNT#3	low = A16 swap override enable	high = default
0	1	high = default

PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPT
1	0	PCI
1	1	LPC(Default)

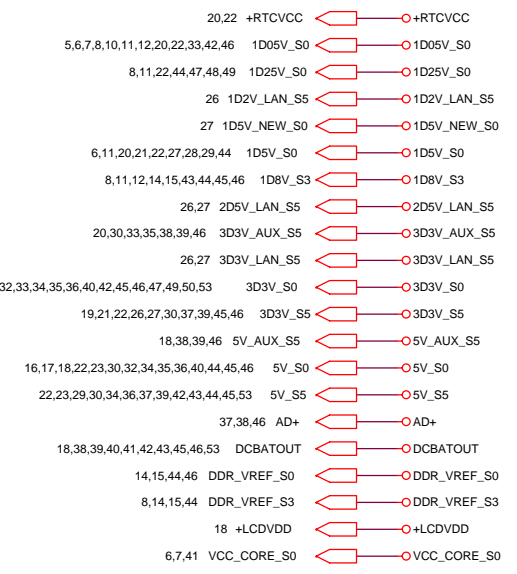
SM_INTVRMEN	High=Enable	Low=Disable
0	1	Low=Disable

LAN100_SLP	High=Enable	Low=Disable
0	1	Low=Disable

DEFAULE HIGH

SPKR	LOW = Defaule	High=No Reboot
0	1	High=No Reboot

8.2K PULL HIGH



PCI ROUTING

	IDSEL	INT	REQ	GNT
1394/ MediaCard	AD25	A D	0	0

INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	TBD

USB TABLE

USB0	Ext Lift Side (Bottom)
USB1	Ext Lift Side (Top)
USB2	Ext Right Side
USB3	N/A
USB4	WWAN
USB5	Bluetooth
USB6	Camera
USB7	Biometric
USB8	Express Card
USB9	3rd mini card

PCIe Routing

LANE1	10/100M Bit LOM
LANE2	MiniCard WLAN
LANE3	MiniCard WWAN
LANE4	BT/UWB/Robson
LANE5	Express Card
LANE6	N/A

INTEL CRESTLINE STRAP PIN

CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	DMI X 4 ★
CFG 8	Low Power PCI Express	Normal★ Low Power mode
CFG 9	PCI Express Graphics Lane Reversal	Lane Reversal Normal Mode(Lanes★ number in order)
CFG 16	FSB Dynamic ODT	Disabled Enabled★
CFG 19	DMI Lane Reserved	Normal Operation★ Reserved Lane
CFG 20	Concurrent SDVO/PCIe	Only PCIe or SDVO is operation★ PCIe and SDVO are operation simultaneous
SDVO_CTRL_DATA	NO SDVO Card Present★	SDVO Card Present
CFG 12	XOR/ALL-Z	
CFG 13	Reserved	
LL(00)	Reserved	
LH(01)	XOR Mode Enabled	
HL(10)	All Z Mode Enabled	
HR(11)	Normal Operation	

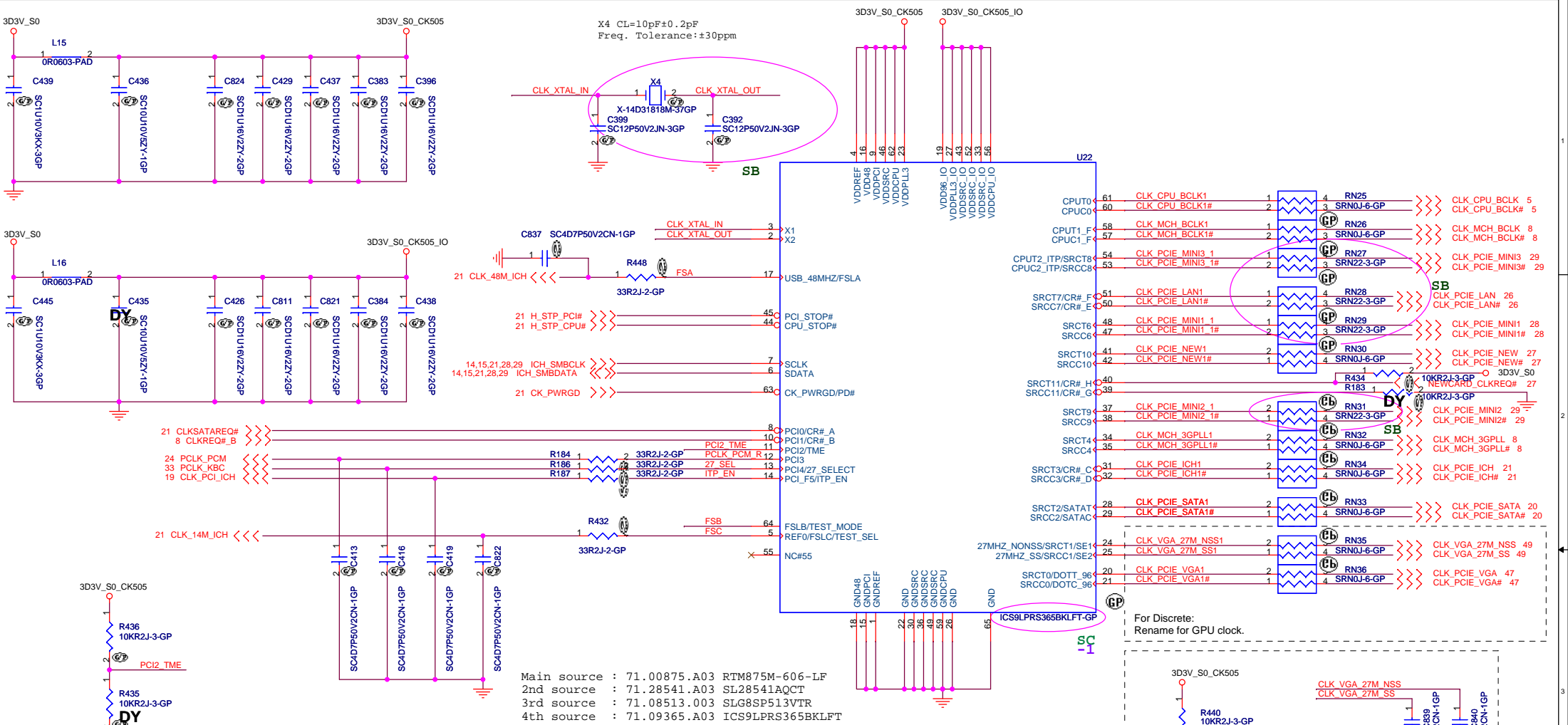
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Table of Content

Size A3 Document Number Hawke-Intel Rev -1

Date: Sunday, September 09, 2007 Sheet 3 of 57



Main source : 71.00875.A03 RTM875M-606-LF
 2nd source : 71.28541.A03 SL28541AQT
 3rd source : 71.08513.003 SLG8SP513VTR
 4th source : 71.09365.A03 ICS9LPRS365BKLFT

PCI2_TME	Output
0	Overclocking of CPU and SRC allowed
1	Overclocking of CPU and SRC not allowed

FS_C	FS_B	FS_A	CPU
1	0	1	100M
0	0	1	133M
0	1	0	200M
0	1	1	166M

ITP_EN	Output
0	SRC8
1	CPU_ITP



Design Note:

- All of Input pin didn't have internal pull up resistor.
- Clock Request (CR) function are enable by registers.
- ICS9LPRS365 integrated serial resistor of differential clock, so put 0 ohm serial resistor in the schematic.

27_SEL strap 0:For 965GM, 1:For 965PM

27_SEL	PIN 20	PIN 21	PIN 24	PIN 25	
0	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100	965GM
1	SRCT0	SRCC0	27M_NSS	27M_SS	965PM

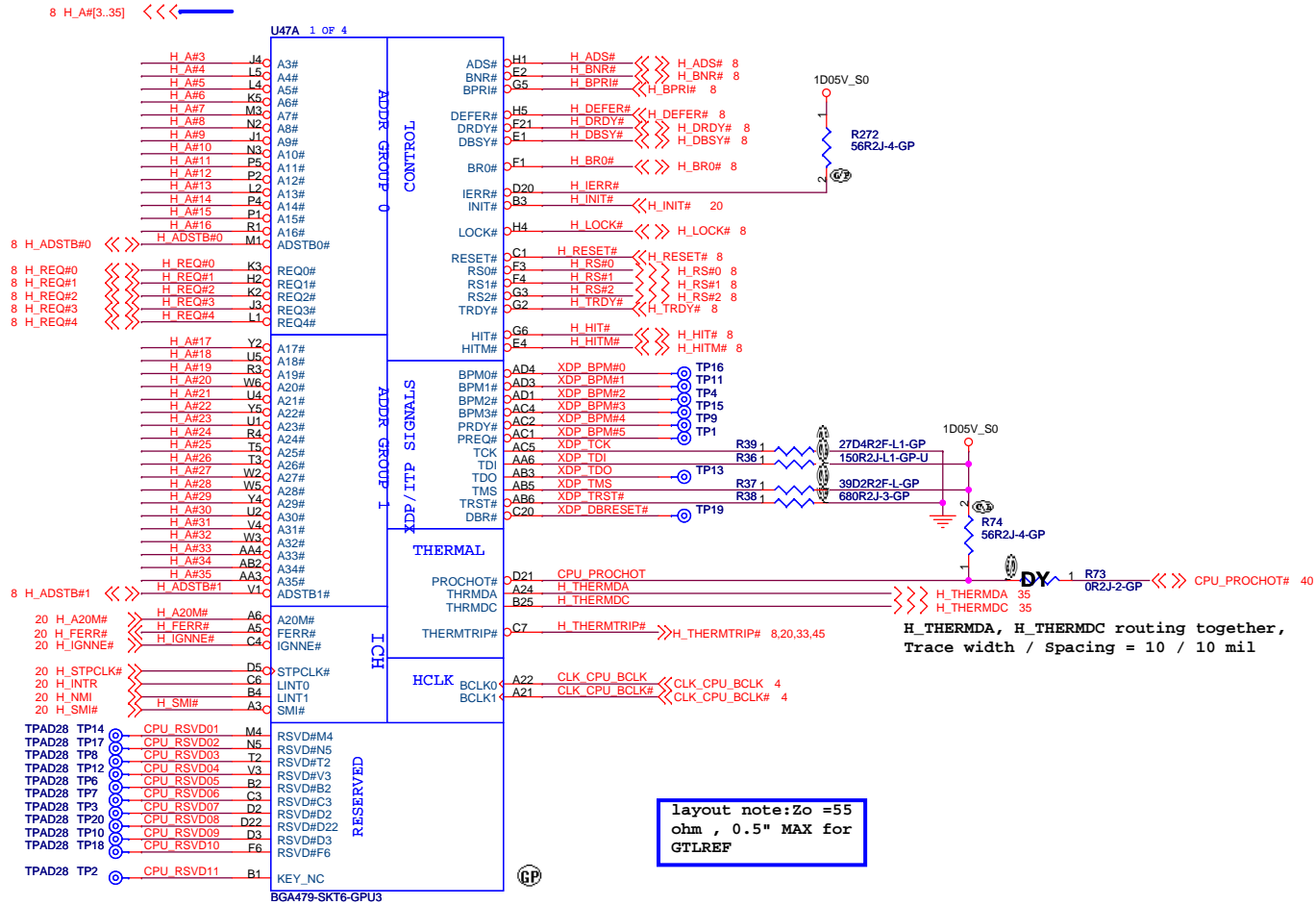
<Core Design>

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Clock generator ICS9LPRS365**

Size A3 Document Number **Hawke-Intel** Rev **-1**

Date: Sunday, September 09, 2007 Sheet 4 of 57

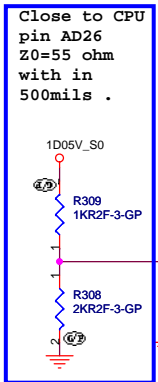
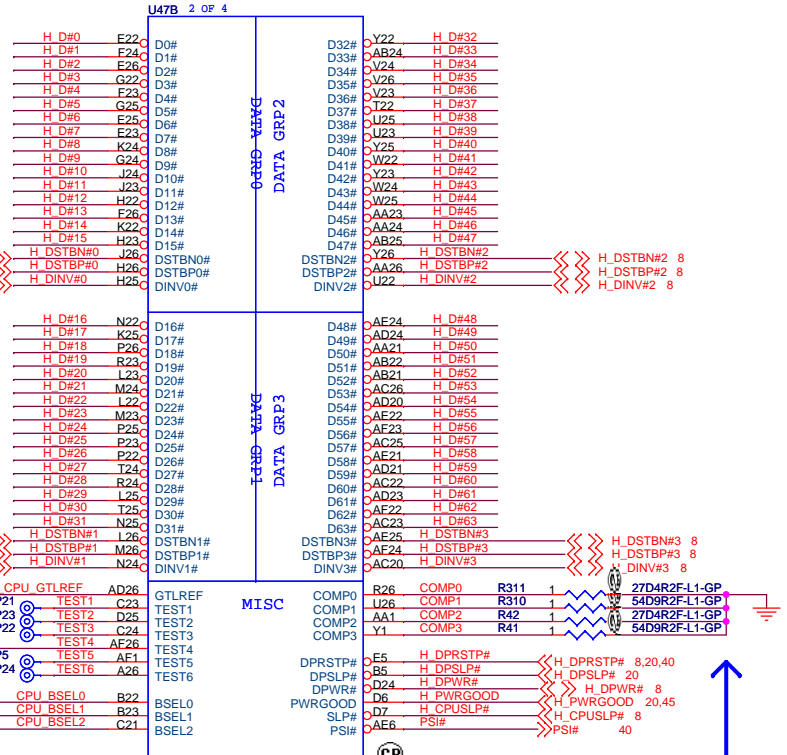


layout note:Zo =55
ohm , 0.5" MAX for
GTLREF

Main source : 62.10079.021 Tyco 2-1871873-4
2nd source : 62.10040.221 Foxconn PZ47827-274M-41

<Core Design>

8 H_D#[0..63] <<<



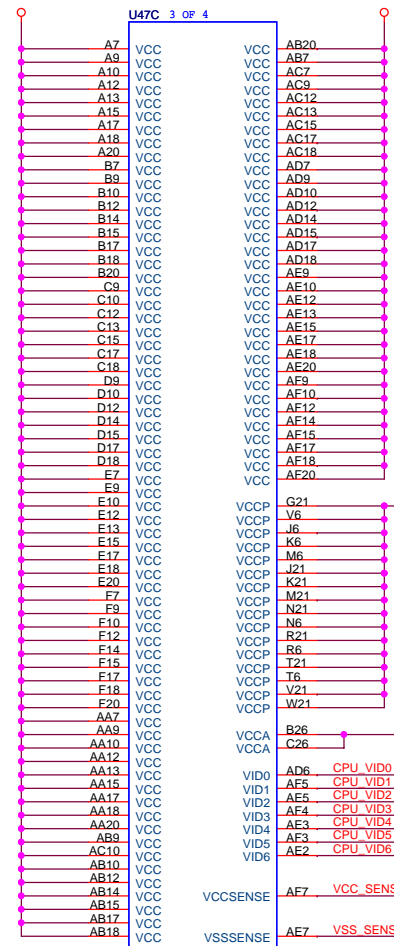
Close to CPU pin AD26 Z0=55 ohm with in 500mils .

PLACE C617 close to the TEST4 PIN, make sure TEST3,TEST4,TEST5 trace routing is reference to GND and away other noisy signals

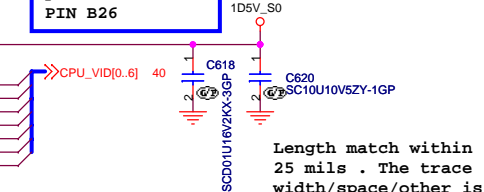
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

Resistor Placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal . COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils .

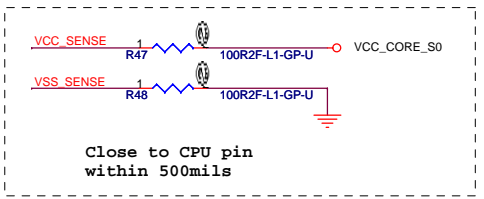
VCC_CORE_S0 VCC_CORE_S0



layout note: place C618 near PIN B26



Length match within 25 mils . The trace width/space/other is 20/7/25 .

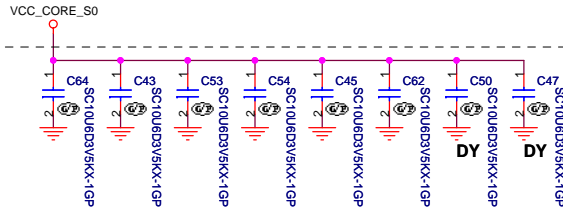


U47D 4 OF 4		
A4	VSS	P6
A8	VSS	P24
A11	VSS	R2
A14	VSS	R5
A16	VSS	R22
A19	VSS	R25
A23	VSS	T1
B6	VSS	T4
B8	VSS	T23
B11	VSS	T26
B13	VSS	U3
B16	VSS	U6
B19	VSS	U21
B21	VSS	U24
B24	VSS	V2
C5	VSS	V5
C8	VSS	V22
C11	VSS	V25
C14	VSS	W1
C16	VSS	W4
C19	VSS	W23
C2	VSS	W26
C22	VSS	Y3
C25	VSS	Y6
D1	VSS	Y21
D4	VSS	Y24
D8	VSS	AA2
D11	VSS	AA5
D13	VSS	AA8
D16	VSS	AA11
D19	VSS	AA14
D23	VSS	AA16
D26	VSS	AA19
E3	VSS	AA22
E6	VSS	AA25
E8	VSS	AB1
E11	VSS	AB4
E14	VSS	AB8
E16	VSS	AB11
E19	VSS	AB13
E21	VSS	AB16
E24	VSS	AB19
F5	VSS	AB23
F8	VSS	AB26
F11	VSS	AC3
F13	VSS	AC6
F16	VSS	AC8
F19	VSS	AC11
F2	VSS	AC14
F22	VSS	AC16
F25	VSS	AC19
G4	VSS	AC21
G1	VSS	AC24
G23	VSS	AD2
G26	VSS	AD5
H3	VSS	AD8
H6	VSS	AD11
H21	VSS	AD13
H24	VSS	AD16
J2	VSS	AD19
J5	VSS	AD22
J22	VSS	AD25
J25	VSS	AE1
K1	VSS	AE4
K4	VSS	AE8
K23	VSS	AE11
K26	VSS	AE14
L3	VSS	AE16
L6	VSS	AE19
L21	VSS	AE23
L24	VSS	AE26
M2	VSS	A2
M5	VSS	AF6
M22	VSS	AF8
M25	VSS	AF11
N1	VSS	AF13
N4	VSS	AF16
N23	VSS	AF19
N26	VSS	AF21
P3	VSS	A25
	VSS	AF25

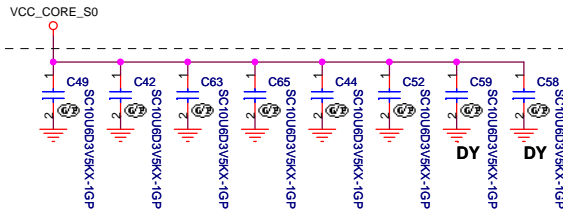
BGA479-SKT6-GPU3



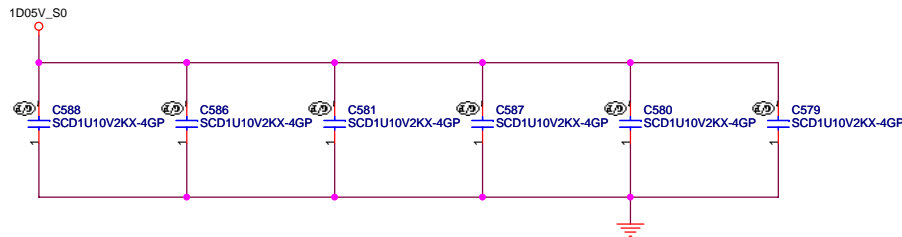
Place these capacitors on L1
(North side ,Secondary Layer)



Place these capacitors on L1
(North side ,Secondary Layer)



Mid Frequncd Decoupling



Place these
inside socket
cavity on L1
(North side
Secondary)

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Meron(3/3)-GND&Bypass		
Size	Document Number	Rev
A3	Hawke-Intel	-1
Date:	Sunday, September 09, 2007	Sheet 7 of 57

<<>> DDR_A_D[0..63] 14
 >>> DDR_A_BS[0..2] 14
 >>> DDR_A_DM[0..7] 14
 <<>> DDR_A_DQS[0..7] 14
 <<>> DDR_A_DQS#[0..7] 14
 >>> DDR_A_MA[0..14] 14

<<>> DDR_B_D[0..63] 15
 >>> DDR_B_BS[0..2] 15
 >>> DDR_B_DM[0..7] 15
 <<>> DDR_B_DQS[0..7] 15
 <<>> DDR_B_DQS#[0..7] 15
 >>> DDR_B_MA[0..14] 15

U57D 4 OF 10

DDR A D0	AR43	SA_DQ0	SA_BS0	BB19	DDR A BS0	
DDR A D1	AW44	SA_DQ1	SA_BS1	BK19	DDR A BS1	
DDR A D2	BA45	SA_DQ2	SA_BS2	BF29	DDR A BS2	
DDR A D3	AV46	SA_DQ3				
DDR A D4	AR41	SA_DQ4	SA_CAS#	BL17	DDR A CAS#	>>> DDR_A_CAS# 14
DDR A D5	AR45	SA_DQ5				
DDR A D6	AT42	SA_DQ6	SA_DM0	AT45	DDR A DM0	
DDR A D7	AW47	SA_DQ7	SA_DM1	BD44	DDR A DM1	
DDR A D8	BB45	SA_DQ8	SA_DM2	BD42	DDR A DM2	
DDR A D9	BF48	SA_DQ9	SA_DM3	AW38	DDR A DM3	
DDR A D10	BG47	SA_DQ10	SA_DM4	AW13	DDR A DM4	
DDR A D11	BJ45	SA_DQ11	SA_DM5	BG8	DDR A DM5	
DDR A D12	BB47	SA_DQ12	SA_DM6	AY5	DDR A DM6	
DDR A D13	BG50	SA_DQ13	SA_DM7	AN6	DDR A DM7	
DDR A D14	BH49	SA_DQ14				
DDR A D15	BE45	SA_DQ15	SA_DQS0	AT46	DDR A DQS0	
DDR A D16	AW43	SA_DQ16	SA_DQS1	BE48	DDR A DQS1	
DDR A D17	BE44	SA_DQ17	SA_DQS2	BB43	DDR A DQS2	
DDR A D18	BG42	SA_DQ18	SA_DQS3	BC37	DDR A DQS3	
DDR A D19	BE40	SA_DQ19	SA_DQS4	BB16	DDR A DQS4	
DDR A D20	BF44	SA_DQ20	SA_DQS5	BH6	DDR A DQS5	
DDR A D21	BH45	SA_DQ21	SA_DQS6	BB2	DDR A DQS6	
DDR A D22	BG40	SA_DQ22	SA_DQS7	AP3	DDR A DQS7	
DDR A D23	BE40	SA_DQ23	SA_DQS#0	AT47	DDR A DQS#0	
DDR A D24	AR40	SA_DQ24	SA_DQS#1	BD47	DDR A DQS#1	
DDR A D25	AW40	SA_DQ25	SA_DQS#2	BC41	DDR A DQS#2	
DDR A D26	AT39	SA_DQ26	SA_DQS#3	BA37	DDR A DQS#3	
DDR A D27	AW36	SA_DQ27	SA_DQS#4	BA16	DDR A DQS#4	
DDR A D28	AW41	SA_DQ28	SA_DQS#5	BH7	DDR A DQS#5	
DDR A D29	AY41	SA_DQ29	SA_DQS#6	BC1	DDR A DQS#6	
DDR A D30	AV38	SA_DQ30	SA_DQS#7	AP2	DDR A DQS#7	
DDR A D31	AT38	SA_DQ31				
DDR A D32	AV13	SA_DQ32	SA_MA0	BJ19	DDR A MA0	
DDR A D33	AT13	SA_DQ33	SA_MA1	BD20	DDR A MA1	
DDR A D34	AW11	SA_DQ34	SA_MA2	BK27	DDR A MA2	
DDR A D35	AV11	SA_DQ35	SA_MA3	BH28	DDR A MA3	
DDR A D36	AU15	SA_DQ36	SA_MA4	BL24	DDR A MA4	
DDR A D37	AT11	SA_DQ37	SA_MA5	BK28	DDR A MA5	
DDR A D38	BA13	SA_DQ38	SA_MA6	BJ27	DDR A MA6	
DDR A D39	BA11	SA_DQ39	SA_MA7	BJ25	DDR A MA7	
DDR A D40	BE10	SA_DQ40	SA_MA8	BL28	DDR A MA8	
DDR A D41	BD10	SA_DQ41	SA_MA9	BA28	DDR A MA9	
DDR A D42	BD8	SA_DQ42	SA_MA10	BC19	DDR A MA10	
DDR A D43	AY9	SA_DQ43	SA_MA11	BE28	DDR A MA11	
DDR A D44	BG10	SA_DQ44	SA_MA12	BG30	DDR A MA12	
DDR A D45	AW9	SA_DQ45	SA_MA13	BJ16	DDR A MA13	
DDR A D46	BD7	SA_DQ46	SA_MA14	BJ29	DDR A MA14	
DDR A D47	BB9	SA_DQ47				
DDR A D48	BB5	SA_DQ48	SA_RAS#	BE18	DDR A RAS#	>>> DDR_A_RAS# 14
DDR A D49	AY7	SA_DQ49	SA_RCVEN#	AY20	SA_RCVEN#	TP56
DDR A D50	AT5	SA_DQ50				
DDR A D51	AT7	SA_DQ51	SA_WE#	BA19	DDR A WE#	>>> DDR_A_WE# 14
DDR A D52	AY6	SA_DQ52				
DDR A D53	BB7	SA_DQ53				
DDR A D54	AR5	SA_DQ54				
DDR A D55	AR5	SA_DQ55				
DDR A D56	AR9	SA_DQ56				
DDR A D57	AN3	SA_DQ57				
DDR A D58	AM8	SA_DQ58				
DDR A D59	AN10	SA_DQ59				
DDR A D60	AT9	SA_DQ60				
DDR A D61	AN9	SA_DQ61				
DDR A D62	AM9	SA_DQ62				
DDR A D63	AN11	SA_DQ63				

DDR SYSTEM MEMORY A

U57E 5 OF 10

DDR B D0	AP49	SB_DQ0	SB_BS0	AY17	DDR B BS0	
DDR B D1	AR51	SB_DQ1	SB_BS1	BG18	DDR B BS1	
DDR B D2	AW50	SB_DQ2	SB_BS2	BG36	DDR B BS2	
DDR B D3	AW51	SB_DQ3				
DDR B D4	AN51	SB_DQ4	SB_CAS#	BE17	DDR B CAS#	>>> DDR_B_CAS# 15
DDR B D5	AN50	SB_DQ5				
DDR B D6	AV50	SB_DQ6	SB_DM0	AR50	DDR B DM0	
DDR B D7	AV49	SB_DQ7	SB_DM1	BD49	DDR B DM1	
DDR B D8	BA50	SB_DQ8	SB_DM2	BK45	DDR B DM2	
DDR B D9	BA49	SB_DQ9	SB_DM3	BL39	DDR B DM3	
DDR B D10	BA49	SB_DQ10	SB_DM4	BH12	DDR B DM4	
DDR B D11	BE50	SB_DQ11	SB_DM5	BJ7	DDR B DM5	
DDR B D12	BA51	SB_DQ12	SB_DM6	BF3	DDR B DM6	
DDR B D13	AY49	SB_DQ13	SB_DM7	AW2	DDR B DM7	
DDR B D14	BE50	SB_DQ14				
DDR B D15	BF49	SB_DQ15	SB_DQS0	AT50	DDR B DQS0	
DDR B D16	BJ44	SB_DQ16	SB_DQS1	BD50	DDR B DQS1	
DDR B D17	BJ44	SB_DQ17	SB_DQS2	BK46	DDR B DQS2	
DDR B D18	BJ43	SB_DQ18	SB_DQS3	BK39	DDR B DQS3	
DDR B D19	BL43	SB_DQ19	SB_DQS4	BJ12	DDR B DQS4	
DDR B D20	BK47	SB_DQ20	SB_DQS5	BL7	DDR B DQS5	
DDR B D21	BK49	SB_DQ21	SB_DQS6	BE2	DDR B DQS6	
DDR B D22	BK43	SB_DQ22	SB_DQS7	AV2	DDR B DQS7	
DDR B D23	BK42	SB_DQ23	SB_DQS#0	AU150	DDR B DQS#0	
DDR B D24	BJ41	SB_DQ24	SB_DQS#1	BC50	DDR B DQS#1	
DDR B D25	BL41	SB_DQ25	SB_DQS#2	BL45	DDR B DQS#2	
DDR B D26	BJ37	SB_DQ26	SB_DQS#3	BK38	DDR B DQS#3	
DDR B D27	BJ36	SB_DQ27	SB_DQS#4	BK12	DDR B DQS#4	
DDR B D28	BJ40	SB_DQ28	SB_DQS#5	BK7	DDR B DQS#5	
DDR B D29	BK41	SB_DQ29	SB_DQS#6	BE2	DDR B DQS#6	
DDR B D30	BK35	SB_DQ30	SB_DQS#7	AV3	DDR B DQS#7	
DDR B D31	BK37	SB_DQ31				
DDR B D32	BK13	SB_DQ32	SB_MA0	BC18	DDR B MA0	
DDR B D33	BE11	SB_DQ33	SB_MA1	BG28	DDR B MA1	
DDR B D34	BK11	SB_DQ34	SB_MA2	BG25	DDR B MA2	
DDR B D35	BC11	SB_DQ35	SB_MA3	AW17	DDR B MA3	
DDR B D36	BC13	SB_DQ36	SB_MA4	BE25	DDR B MA4	
DDR B D37	BE12	SB_DQ37	SB_MA5	BE25	DDR B MA5	
DDR B D38	BC12	SB_DQ38	SB_MA6	BA29	DDR B MA6	
DDR B D39	BG12	SB_DQ39	SB_MA7	BC28	DDR B MA7	
DDR B D40	BJ10	SB_DQ40	SB_MA8	AY28	DDR B MA8	
DDR B D41	BL9	SB_DQ41	SB_MA9	BD37	DDR B MA9	
DDR B D42	BL5	SB_DQ42	SB_MA10	BG17	DDR B MA10	
DDR B D43	BK5	SB_DQ43	SB_MA11	BE37	DDR B MA11	
DDR B D44	BK9	SB_DQ44	SB_MA12	BA39	DDR B MA12	
DDR B D45	BK10	SB_DQ45	SB_MA13	BG13	DDR B MA13	
DDR B D46	BJ8	SB_DQ46	SB_MA14	BE24	DDR B MA14	
DDR B D47	BJ6	SB_DQ47				
DDR B D48	BE4	SB_DQ48	SB_RAS#	AV16	DDR B RAS#	>>> DDR_B_RAS# 15
DDR B D49	BH5	SB_DQ49	SB_RCVEN#	AY18	SB_RCVEN#	TP51
DDR B D50	BG1	SB_DQ50				
DDR B D51	BC2	SB_DQ51	SB_WE#	BC17	DDR B WE#	>>> DDR_B_WE# 15
DDR B D52	BK3	SB_DQ52				
DDR B D53	BE4	SB_DQ53				
DDR B D54	BD3	SB_DQ54				
DDR B D55	BJ2	SB_DQ55				
DDR B D56	BA3	SB_DQ56				
DDR B D57	BB3	SB_DQ57				
DDR B D58	AR1	SB_DQ58				
DDR B D59	AT3	SB_DQ59				
DDR B D60	AY2	SB_DQ60				
DDR B D61	AY3	SB_DQ61				
DDR B D62	AL2	SB_DQ62				
DDR B D63	AT2	SB_DQ63				

DDR SYSTEM MEMORY B

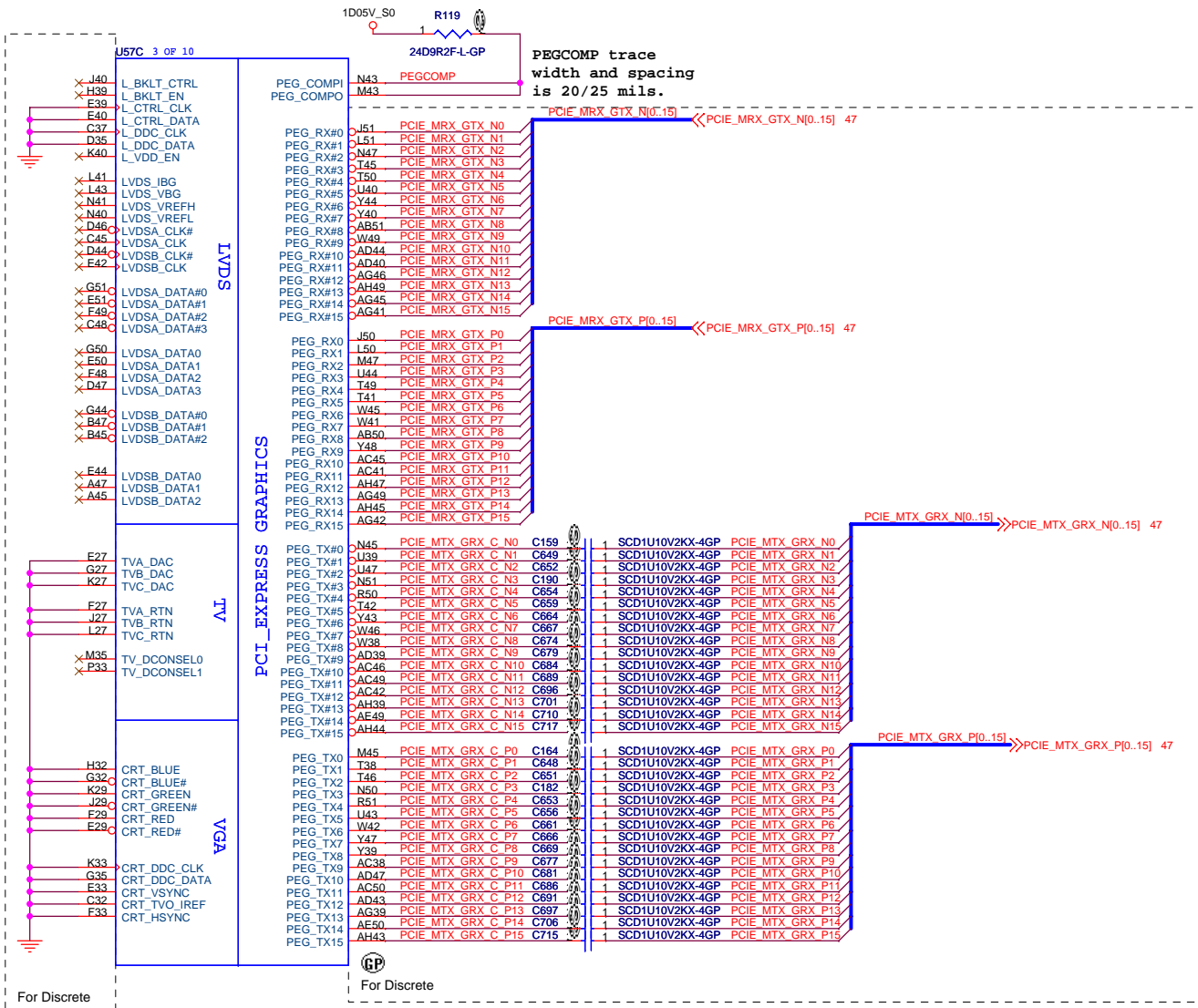
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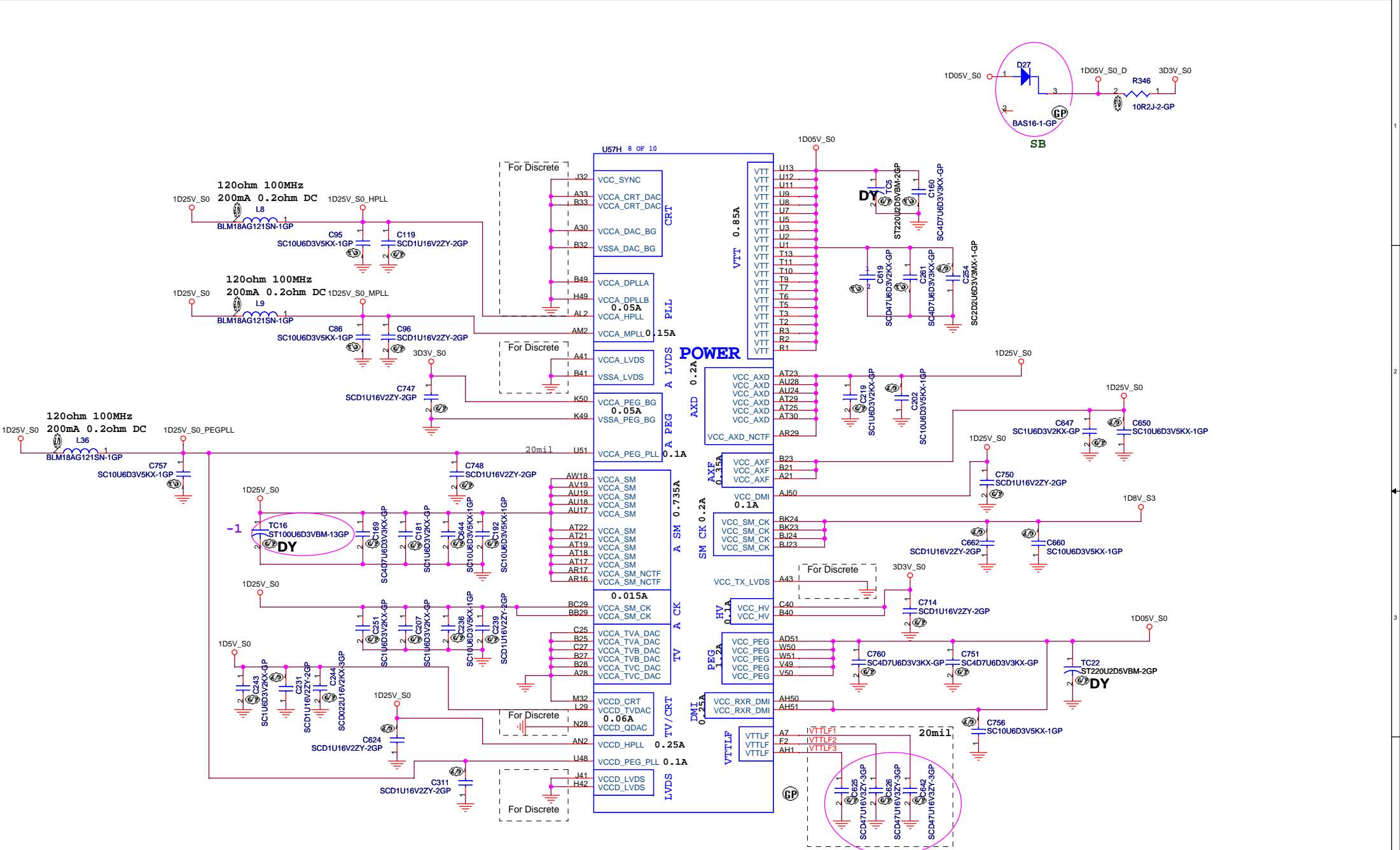


Title		
CRESTLINE(2/6)-DDR2 A/B CH		
Size	Document Number	Rev
A3	Hawke-Intel	-1
Date:	Sunday, September 09, 2007	Sheet 9 of 57

Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disable 1 = Enable *
CFG[18:17]	Reversed
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19(DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) 1 = Reverse lane *
CFG20(PCIE/SDVO consurrent)	0 = Only PCIE or SDVO is operational * 1 = PCIE/SDVO are operating simu.





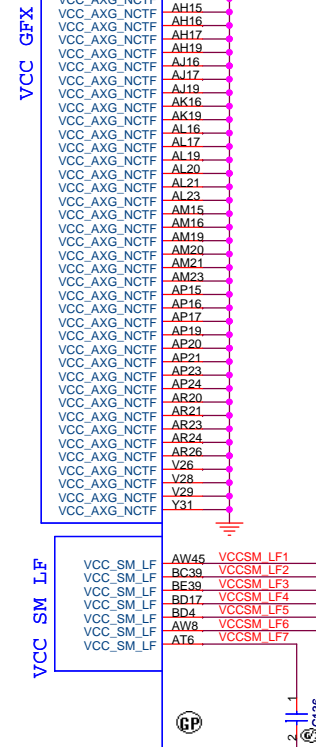
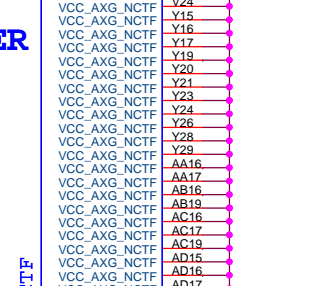
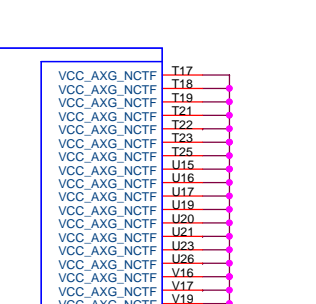
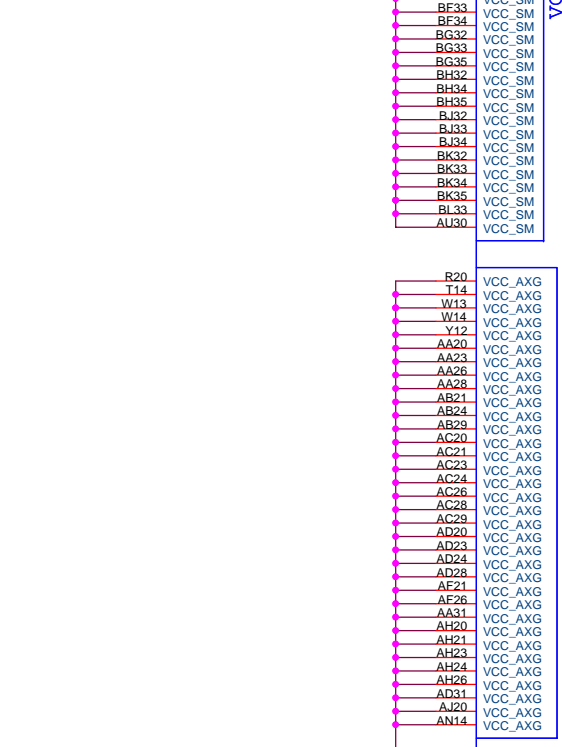
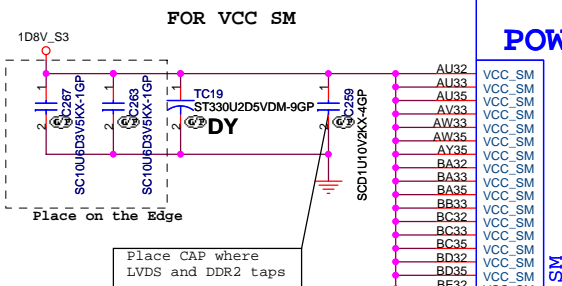
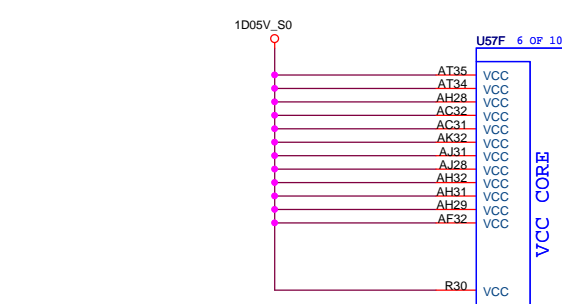
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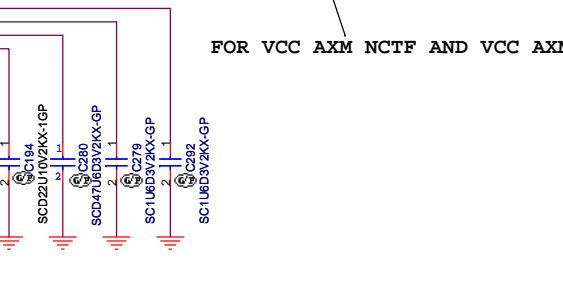
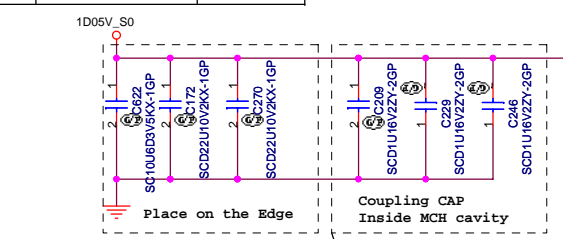
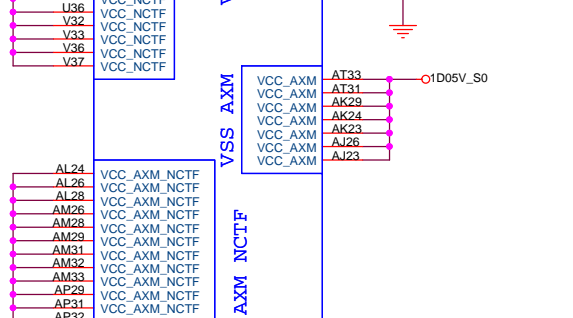
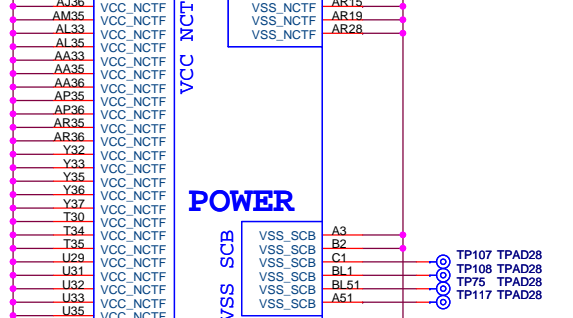
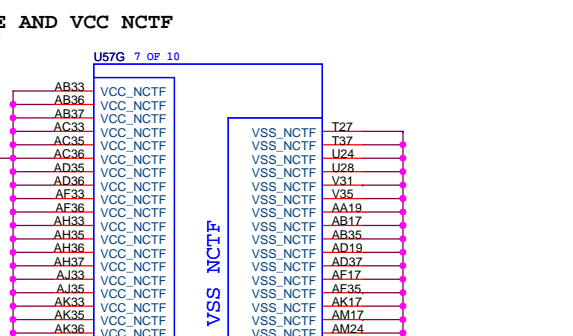
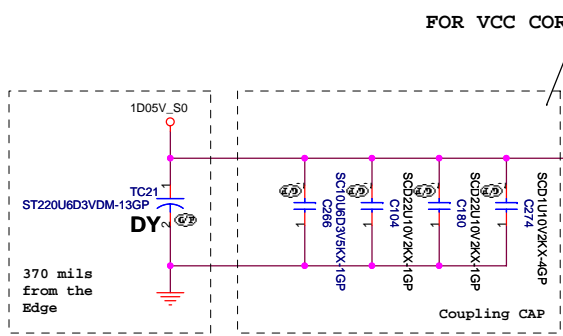
Title: **CRESTLINE(4/6)-PWR**

Size: A3 Document Number: Hawke-Intel Rev: -1

Date: Sunday, September 09, 2007 Sheet 11 of 57



Supply	Signal Group	Icc-max
+1.05V_VCCP	VCC	1.31A
+1.05V_VCCP	VCC_NCTF	A
+1.05V_VCCP	VTT	0.85A
+1.05V_VCCP	VCC_PEG	1.2A
+1.05V_VCCP	VCC_RXR_DMI	0.25A
+1.05V_VCCP	VCC_ATX	84.15mA (Non-AMT)
+1.8V_SUS	VCC_SM	2.4A
+1.8V_SUS	VCC_SM_CK	0.2A
+1.25V_RUN	VCCA_HPLL	0.05A
+1.25V_RUN	VCCA_MPLL	0.15A
+1.25V_RUN	VCCA_SM	0.735A (667MHz)
+1.25V_RUN	VCCA_SM_NCTF	A
+1.25V_RUN	VCCA_SM_CK	0.015A (667MHz)
+1.25V_RUN	VCCD_HPLL	0.25A
+1.25V_RUN	VCCA_AXD	0.2A
+1.25V_RUN	VCCA_AXD_NCTF	A
+1.25V_RUN	VCCA_PEG_PLL /VCCD_PEG_PLL	0.1A
+1.25V_RUN	VCCA_AXF	0.35A
+1.25V_RUN	VCCA_DMI	0.1A
+1.5V_RUN	VCCD_TVDAC	0.06A
+3.3V_RUN	VCCA_PEG_BG	0.005A
+3.3V_RUN	VCC_HV	0.1A



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Title: **CRESTLINE(5/6)-PWR/GND**

Size: A3 Document Number: **Hawke-Intel** Rev: **-1**

Date: Sunday, September 09, 2007 Sheet 12 of 57

U57I 9 OF 10

A13	VSS	VSS	AW24
A15	VSS	VSS	AW29
A17	VSS	VSS	AW32
A24	VSS	VSS	AW5
AA21	VSS	VSS	AW7
AA24	VSS	VSS	AY10
AA29	VSS	VSS	AY24
AB20	VSS	VSS	AY37
AB23	VSS	VSS	AY42
AB26	VSS	VSS	AY43
AB28	VSS	VSS	AY45
AB31	VSS	VSS	AY47
AC10	VSS	VSS	AY50
AC13	VSS	VSS	B10
AC3	VSS	VSS	B20
AC39	VSS	VSS	B24
AC43	VSS	VSS	B29
AC47	VSS	VSS	B30
AD1	VSS	VSS	B35
AD21	VSS	VSS	B38
AD26	VSS	VSS	B43
AD29	VSS	VSS	B46
AD3	VSS	VSS	B5
AD41	VSS	VSS	B8
AD45	VSS	VSS	BA1
AD49	VSS	VSS	BA17
AD5	VSS	VSS	BA18
AD50	VSS	VSS	BA2
AD8	VSS	VSS	BA24
AE10	VSS	VSS	BB12
AE14	VSS	VSS	BB25
AE6	VSS	VSS	BB40
AF20	VSS	VSS	BB44
AF23	VSS	VSS	BB49
AF24	VSS	VSS	BB8
AF31	VSS	VSS	BC16
AG2	VSS	VSS	BC24
AG38	VSS	VSS	BC25
AG43	VSS	VSS	BC36
AG47	VSS	VSS	BC40
AG50	VSS	VSS	BC51
AH3	VSS	VSS	BD13
AH40	VSS	VSS	BD2
AH41	VSS	VSS	BD28
AH7	VSS	VSS	BD45
AH9	VSS	VSS	BD48
AJ11	VSS	VSS	BD5
AJ13	VSS	VSS	BE1
AJ21	VSS	VSS	BE19
AJ24	VSS	VSS	BE23
AJ29	VSS	VSS	BE30
AJ32	VSS	VSS	BE42
AJ43	VSS	VSS	BE51
AJ45	VSS	VSS	BE8
AJ49	VSS	VSS	BF12
AK20	VSS	VSS	BF16
AK21	VSS	VSS	BF36
AK26	VSS	VSS	BG19
AK28	VSS	VSS	BG2
AK31	VSS	VSS	BG24
AK51	VSS	VSS	BG29
AL1	VSS	VSS	BG39
AM11	VSS	VSS	BG48
AM13	VSS	VSS	BG5
AM3	VSS	VSS	BG51
AM4	VSS	VSS	BH17
AM41	VSS	VSS	BH30
AM45	VSS	VSS	BH44
AN1	VSS	VSS	BH46
AN38	VSS	VSS	BH8
AN39	VSS	VSS	BJ11
AN43	VSS	VSS	BJ13
AN5	VSS	VSS	BJ38
AN7	VSS	VSS	BJ4
AP4	VSS	VSS	BJ42
AP48	VSS	VSS	BJ46
AP50	VSS	VSS	BK15
AR11	VSS	VSS	BK17
AR2	VSS	VSS	BK25
AR39	VSS	VSS	BK29
AR44	VSS	VSS	BK36
AR47	VSS	VSS	BK40
AR7	VSS	VSS	BK44
AT10	VSS	VSS	BK6
AT14	VSS	VSS	BK8
AT41	VSS	VSS	BL11
AT49	VSS	VSS	BL13
AU1	VSS	VSS	BL19
AU23	VSS	VSS	BL22
AU29	VSS	VSS	BL37
AU3	VSS	VSS	BL47
AU36	VSS	VSS	C12
AU49	VSS	VSS	C16
AU51	VSS	VSS	C19
AV39	VSS	VSS	C28
AV48	VSS	VSS	C29
AW1	VSS	VSS	C33
AW12	VSS	VSS	C36
AW16	VSS	VSS	C41

VSS

U57J10 OF 10

C46	VSS	VSS	W11
C50	VSS	VSS	W39
C7	VSS	VSS	W43
D13	VSS	VSS	W47
D24	VSS	VSS	W5
D3	VSS	VSS	W7
D32	VSS	VSS	Y13
D39	VSS	VSS	Y2
D45	VSS	VSS	Y41
D49	VSS	VSS	Y45
E10	VSS	VSS	Y49
E16	VSS	VSS	Y5
E24	VSS	VSS	Y50
E28	VSS	VSS	Y11
E32	VSS	VSS	P29
E47	VSS	VSS	T29
F19	VSS	VSS	T31
F36	VSS	VSS	T33
F4	VSS	VSS	R28
F40	VSS		
F50	VSS		
G1	VSS		
G13	VSS		
G16	VSS	VSS	AA32
G19	VSS	VSS	AB32
G24	VSS	VSS	AD32
G28	VSS	VSS	AF28
G29	VSS	VSS	AF29
G33	VSS	VSS	AT27
G42	VSS	VSS	AV25
G45	VSS	VSS	HS0
G48	VSS		
G8	VSS		
H24	VSS		
H28	VSS		
H4	VSS		
H45	VSS		
J11	VSS		
J16	VSS		
J2	VSS		
J24	VSS		
J28	VSS		
J33	VSS		
J35	VSS		
J39	VSS		
K12	VSS		
K47	VSS		
K8	VSS		
L1	VSS		
L17	VSS		
L20	VSS		
L24	VSS		
L28	VSS		
L3	VSS		
L33	VSS		
L49	VSS		
M28	VSS		
M42	VSS		
M46	VSS		
M49	VSS		
M5	VSS		
M50	VSS		
M9	VSS		
N11	VSS		
N14	VSS		
N17	VSS		
N29	VSS		
N32	VSS		
N36	VSS		
N39	VSS		
N44	VSS		
N49	VSS		
N7	VSS		
P19	VSS		
P2	VSS		
P23	VSS		
P3	VSS		
P50	VSS		
R49	VSS		
T39	VSS		
T43	VSS		
T47	VSS		
U41	VSS		
U45	VSS		
U50	VSS		
V2	VSS		
V3	VSS		

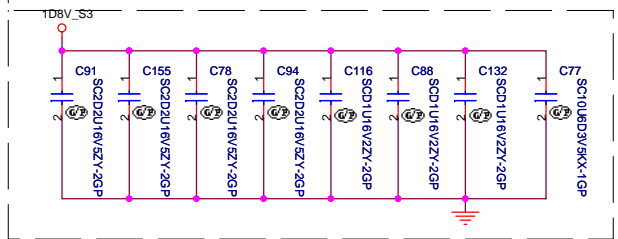
VSS

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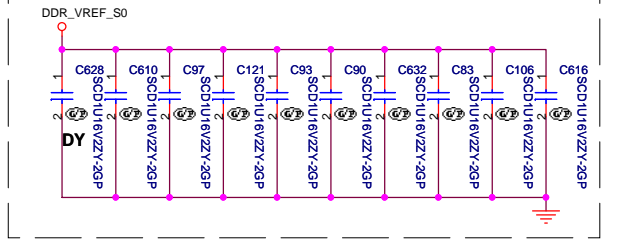
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Title		
CRESTLINE(6/6)-PWR/GND		
Size	Document Number	Rev
A3	Hawke-Intel	-1
Date:	Sunday, September 09, 2007	Sheet 13 of 57

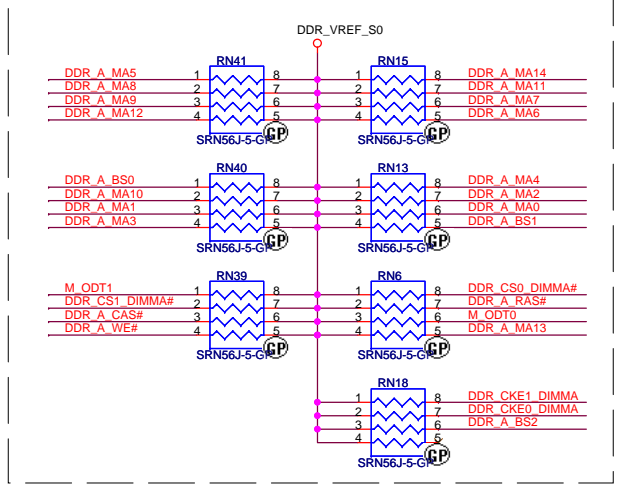
Layout Note:
Place near DM1



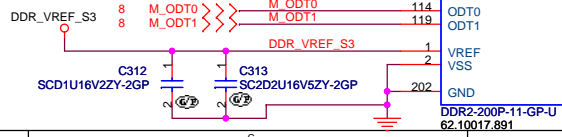
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



change to 8P4R

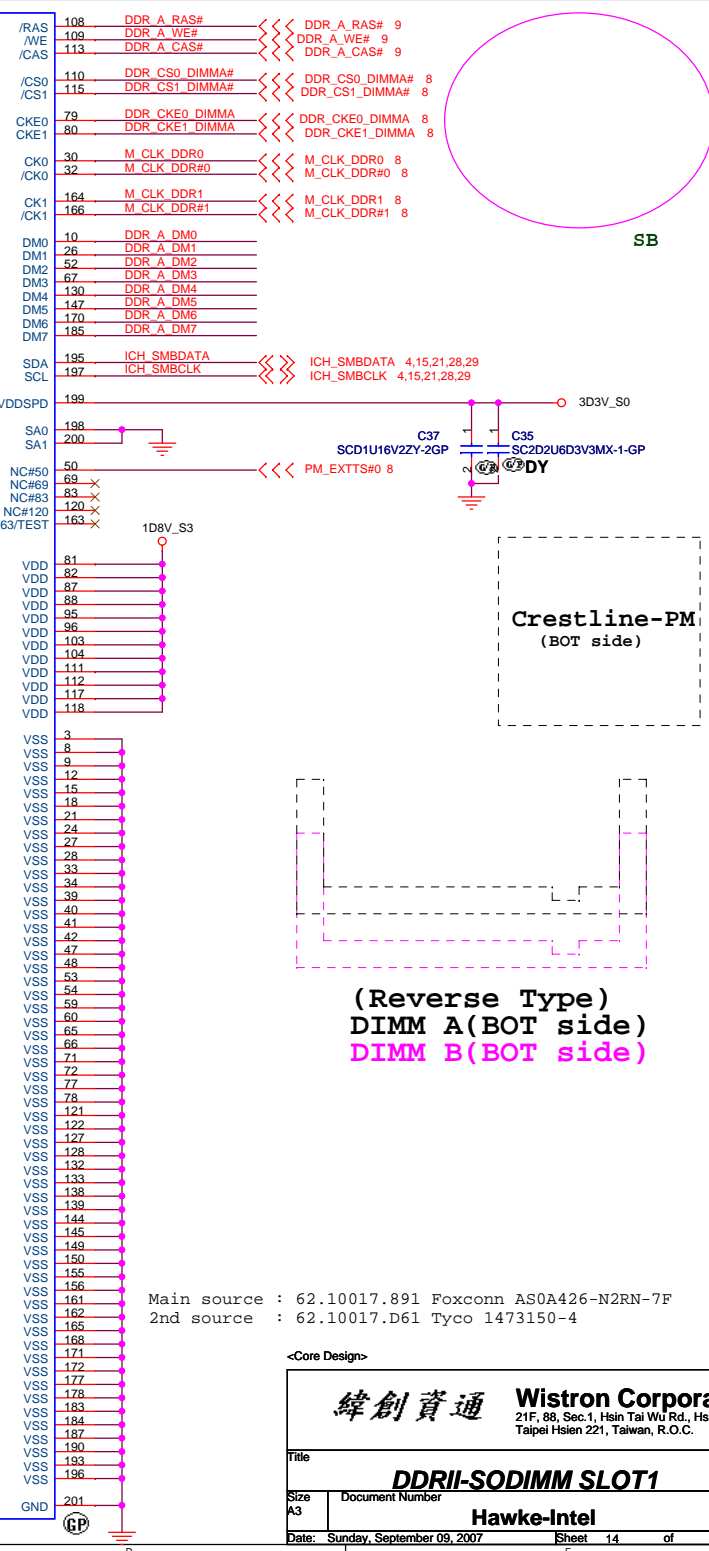


Layout Note:
Place these resistors closely DM1, all trace length Max=1.5"



Pin	Signal	Pin	Signal
102	DDR A MA9	108	DDR A RAS#
101	DDR A MA1	109	DDR A WE#
100	DDR A MA2	113	DDR A CAS#
99	DDR A MA3	110	DDR CS0 DIMMA#
98	DDR A MA4	115	DDR CS1 DIMMA#
97	DDR A MA5	79	DDR CKE0 DIMMA
96	DDR A MA6	80	DDR CKE1 DIMMA
95	DDR A MA7	30	M_CLK_DDR0
94	DDR A MA8	32	M_CLK_DDR#0
93	DDR A MA9	164	M_CLK_DDR1
92	DDR A MA10	166	M_CLK_DDR#1
91	DDR A MA11	10	DDR A DM0
90	DDR A MA12	26	DDR A DM1
89	DDR A MA13	52	DDR A DM2
88	DDR A MA14	67	DDR A DM3
87	DDR A BS2	130	DDR A DM4
85	DDR A BS1	147	DDR A DM5
107	DDR A D0	170	DDR A DM6
106	DDR A D1	185	DDR A DM7
5	DDR A D2	195	ICH_SMBDATA
7	DDR A D3	197	ICH_SMBCLK
17	DDR A D4	199	VDDSPD
19	DDR A D5	198	SA0
4	DDR A D6	200	SA1
6	DDR A D7	50	NC#50
14	DDR A D8	69	NC#69
16	DDR A D9	83	NC#83
23	DDR A D10	120	NC#120
25	DDR A D11	163	NC#163/TEST
35	DDR A D12	81	VDD
37	DDR A D13	82	VDD
20	DDR A D14	87	VDD
22	DDR A D15	88	VDD
36	DDR A D16	95	VDD
38	DDR A D17	96	VDD
43	DDR A D18	103	VDD
45	DDR A D19	104	VDD
55	DDR A D20	111	VDD
57	DDR A D21	112	VDD
44	DDR A D22	117	VDD
46	DDR A D23	118	VDD
56	DDR A D24	3	VSS
63	DDR A D25	8	VSS
73	DDR A D26	9	VSS
75	DDR A D27	12	VSS
62	DDR A D28	15	VSS
64	DDR A D29	18	VSS
74	DDR A D30	21	VSS
76	DDR A D31	24	VSS
123	DDR A D32	27	VSS
135	DDR A D33	28	VSS
137	DDR A D34	33	VSS
124	DDR A D35	34	VSS
126	DDR A D36	39	VSS
134	DDR A D37	40	VSS
136	DDR A D38	41	VSS
141	DDR A D39	42	VSS
143	DDR A D40	47	VSS
151	DDR A D41	48	VSS
153	DDR A D42	53	VSS
140	DDR A D43	54	VSS
142	DDR A D44	55	VSS
152	DDR A D45	59	VSS
154	DDR A D46	60	VSS
157	DDR A D47	65	VSS
159	DDR A D48	66	VSS
173	DDR A D49	71	VSS
175	DDR A D50	72	VSS
168	DDR A D51	77	VSS
160	DDR A D52	78	VSS
162	DDR A D53	121	VSS
179	DDR A D54	122	VSS
181	DDR A D55	127	VSS
189	DDR A D56	128	VSS
191	DDR A D57	132	VSS
180	DDR A D58	133	VSS
182	DDR A D59	138	VSS
192	DDR A D60	139	VSS
194	DDR A D61	144	VSS
11	DDR A D62	145	VSS
23	DDR A D63	149	VSS
49	DDR A D64	150	VSS
68	DDR A D65	155	VSS
129	DDR A D66	156	VSS
146	DDR A D67	161	VSS
167	DDR A D68	162	VSS
186	DDR A D69	165	VSS
13	DDR A D70	168	VSS
31	DDR A D71	171	VSS
51	DDR A D72	172	VSS
70	DDR A D73	177	VSS
131	DDR A D74	183	VSS
148	DDR A D75	184	VSS
169	DDR A D76	187	VSS
188	DDR A D77	190	VSS
13	DDR A DQS0	193	VSS
13	DDR A DQS1	196	VSS
29	DDR A DQS2	201	GND
49	DDR A DQS3	202	GND
68	DDR A DQS4	201	GND
129	DDR A DQS5	201	GND
146	DDR A DQS6	201	GND
167	DDR A DQS7	201	GND
186	DDR A DQS8	201	GND
114	M_ODT0	114	M_ODT0
114	M_ODT1	114	M_ODT1
119	M_ODT1	119	M_ODT1
114	M_ODT0	114	M_ODT0
119	M_ODT1	119	M_ODT1

REVERSE TYPE High 5.2 mm



(Reverse Type)
DIMM A (BOT side)
DIMM B (BOT side)

Main source : 62.10017.891 Foxconn AS0A426-N2RN-7F
2nd source : 62.10017.D61 Tyco 1473150-4

<Core Design>

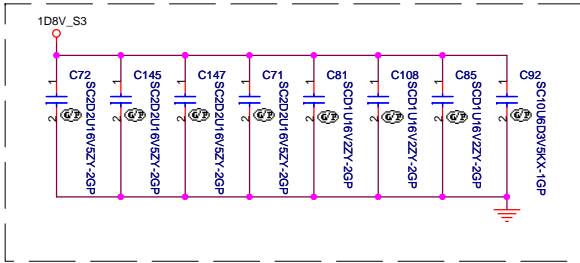
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDRII-SODIMM SLOT1**

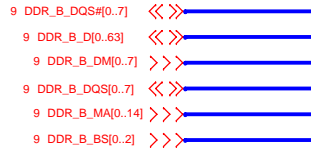
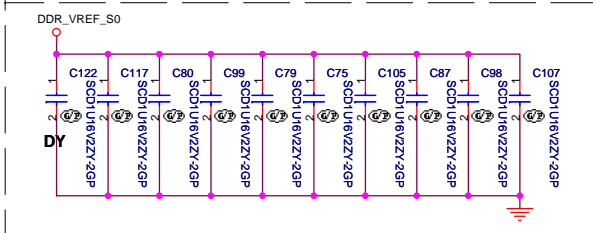
Size A3 Document Number **Hawke-Intel** Rev **-1**

Date: Sunday, September 09, 2007 Sheet 14 of 57

Layout Note:
Place near DM2



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



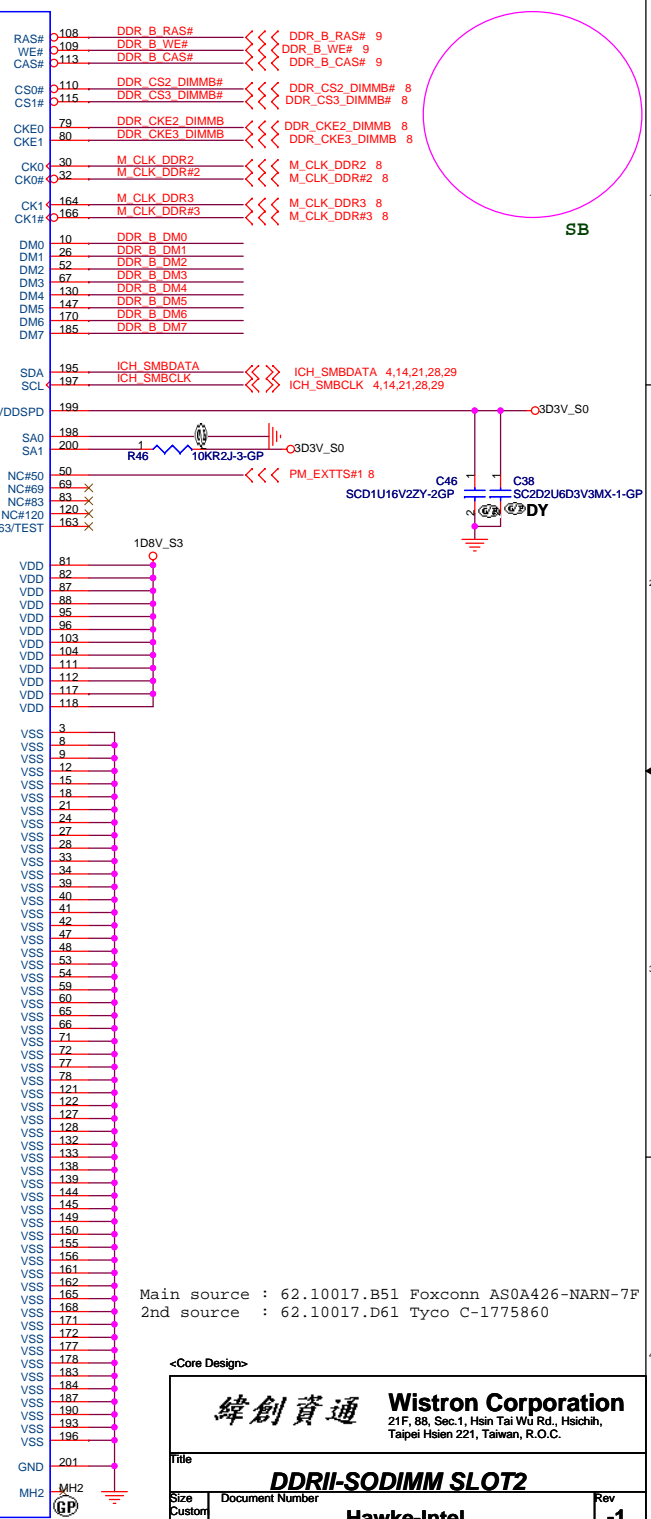
DDR_B MA0	102	A0
DDR_B MA1	101	A1
DDR_B MA2	100	A2
DDR_B MA3	99	A3
DDR_B MA4	98	A4
DDR_B MA5	97	A5
DDR_B MA6	94	A6
DDR_B MA7	92	A7
DDR_B MA8	93	A8
DDR_B MA9	91	A9
DDR_B MA10	90	A10/AP
DDR_B MA11	89	A11
DDR_B MA12	116	A12
DDR_B MA13	86	A13
DDR_B MA14	84	A14
DDR_B BS2	85	A15
DDR_B BS0	107	BA0
DDR_B BS1	106	BA1

DDR_B D0	5	DQ0
DDR_B D1	7	DQ1
DDR_B D2	17	DQ2
DDR_B D3	19	DQ3
DDR_B D4	4	DQ4
DDR_B D5	6	DQ5
DDR_B D6	14	DQ6
DDR_B D7	16	DQ7
DDR_B D8	23	DQ8
DDR_B D9	25	DQ9
DDR_B D10	35	DQ10
DDR_B D11	37	DQ11
DDR_B D12	20	DQ12
DDR_B D13	22	DQ13
DDR_B D14	38	DQ14
DDR_B D15	38	DQ15
DDR_B D16	43	DQ16
DDR_B D17	45	DQ17
DDR_B D18	55	DQ18
DDR_B D19	57	DQ19
DDR_B D20	44	DQ20
DDR_B D21	46	DQ21
DDR_B D22	56	DQ22
DDR_B D23	58	DQ23
DDR_B D24	61	DQ24
DDR_B D25	63	DQ25
DDR_B D26	73	DQ26
DDR_B D27	75	DQ27
DDR_B D28	62	DQ28
DDR_B D29	64	DQ29
DDR_B D30	74	DQ30
DDR_B D31	76	DQ31
DDR_B D32	123	DQ32
DDR_B D33	125	DQ33
DDR_B D34	135	DQ34
DDR_B D35	137	DQ35
DDR_B D36	124	DQ36
DDR_B D37	126	DQ37
DDR_B D38	134	DQ38
DDR_B D39	136	DQ39
DDR_B D40	141	DQ40
DDR_B D41	143	DQ41
DDR_B D42	151	DQ42
DDR_B D43	153	DQ43
DDR_B D44	140	DQ44
DDR_B D45	142	DQ45
DDR_B D46	154	DQ46
DDR_B D47	154	DQ47
DDR_B D48	157	DQ48
DDR_B D49	159	DQ49
DDR_B D50	173	DQ50
DDR_B D51	175	DQ51
DDR_B D52	158	DQ52
DDR_B D53	160	DQ53
DDR_B D54	174	DQ54
DDR_B D55	176	DQ55
DDR_B D56	179	DQ56
DDR_B D57	181	DQ57
DDR_B D58	189	DQ58
DDR_B D59	191	DQ59
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DDR_B D62	192	DQ62
DDR_B D63	194	DQ63

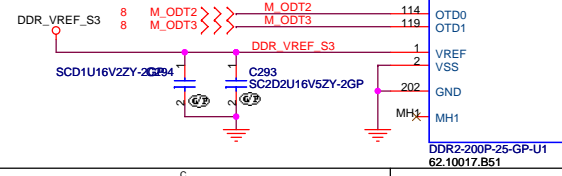
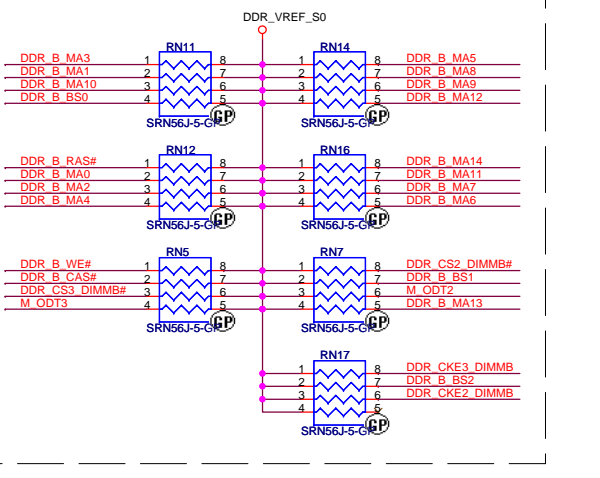
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DDR_B DQS#1	29	DQS1#
DDR_B DQS#2	49	DQS2#
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DDR_B DQS#4	129	DQS4#
DDR_B DQS#5	148	DQS5#
DDR_B DQS#6	167	DQS6#
DDR_B DQS#7	186	DQS7#
DDR_B DQS0	13	DQS0
DDR_B DQS1	31	DQS1
DDR_B DQS2	51	DQS2
DDR_B DQS3	70	DQS3
DDR_B DQS4	131	DQS4
DDR_B DQS5	148	DQS5
DDR_B DQS6	169	DQS6
DDR_B DQS7	188	DQS7

DDR_B DQS#0	11	DQS0#
DDR_B DQS#1	29	DQS1#
DDR_B DQS#2	49	DQS2#
DDR_B DQS#3	69	DQS3#
DDR_B DQS#4	129	DQS4#
DDR_B DQS#5	148	DQS5#
DDR_B DQS#6	167	DQS6#
DDR_B DQS#7	186	DQS7#
DDR_B DQS0	13	DQS0
DDR_B DQS1	31	DQS1
DDR_B DQS2	51	DQS2
DDR_B DQS3	70	DQS3
DDR_B DQS4	131	DQS4
DDR_B DQS5	148	DQS5
DDR_B DQS6	169	DQS6
DDR_B DQS7	188	DQS7

REVERSE TYPE High 9.2 mm



Layout Note:
Place these resistors closely DM2, all trace length Max=1.5"



Main source : 62.10017.B51 Foxconn AS0A426-NARN-7F
2nd source : 62.10017.D61 Tyco C-1775860

<Core Design>

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DDRII-SODIMM SLOT2

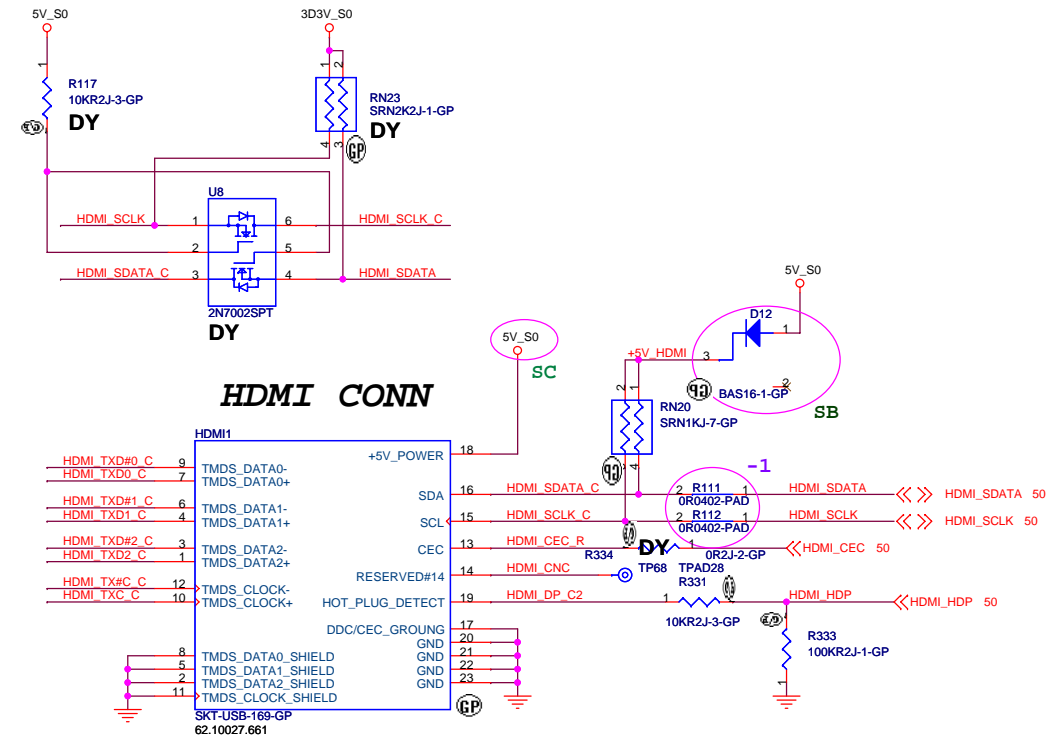
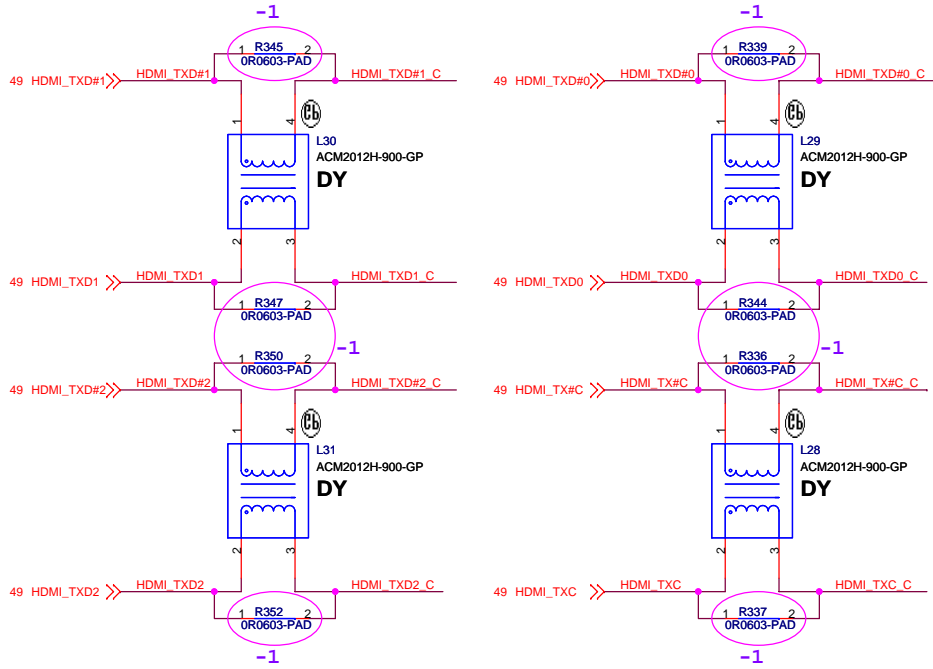
File: **Hawke-Intel**

Size Custom Document Number: **Hawke-Intel**

Date: Sunday, September 09, 2007 Sheet 15 of 57

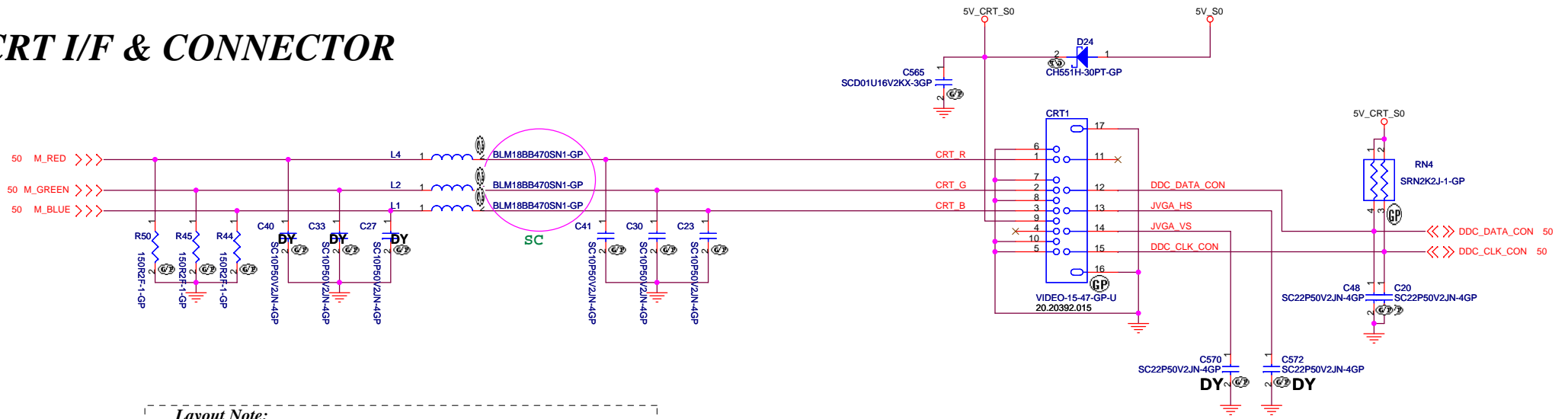
Rev: **-1**

HDMI I/F & CONNECTOR

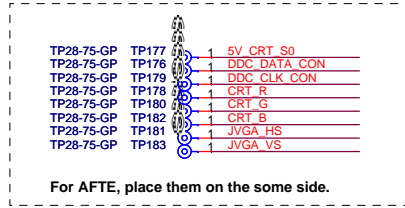
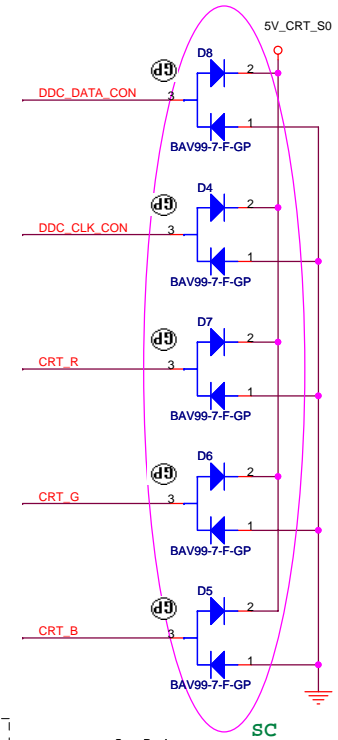
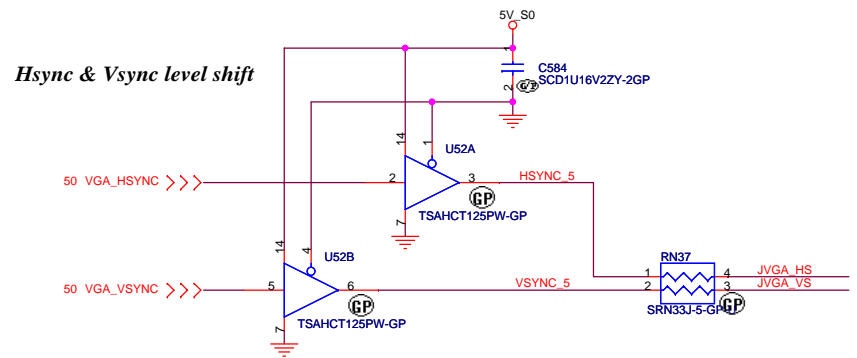


Main source : 62.10027.661 Molex 47408-0201
 2nd source : 62.10078.121 Tyco C1759548-1

CRT I/F & CONNECTOR



Layout Note:
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



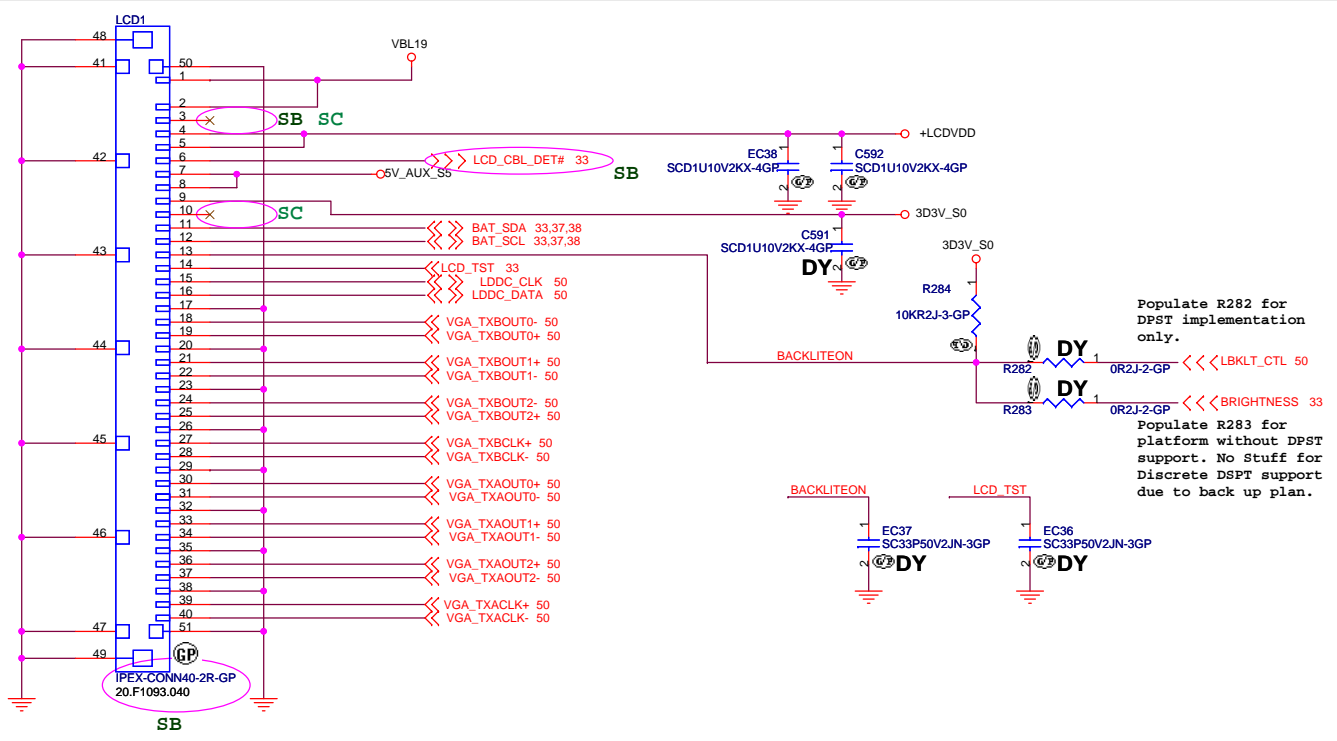
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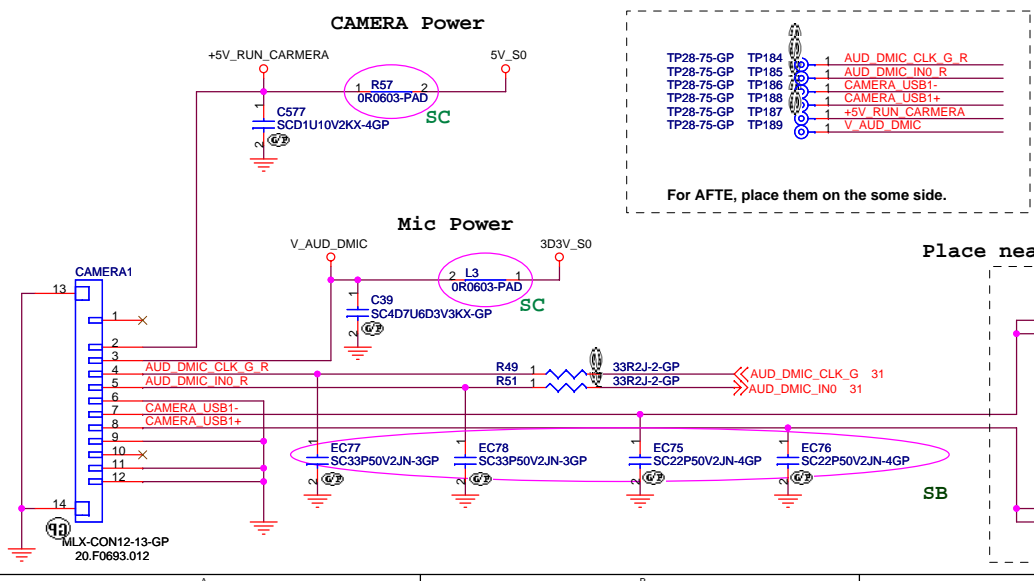
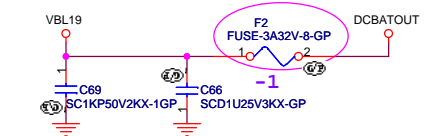
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Size A3	Document Number	Rev
	Hawke-Intel	-1

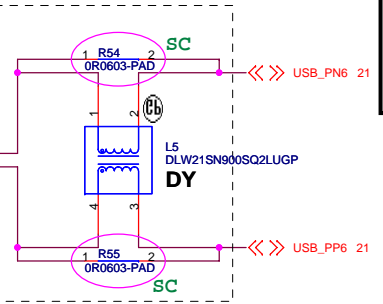
Date: Sunday, September 09, 2007 Sheet 17 of 57



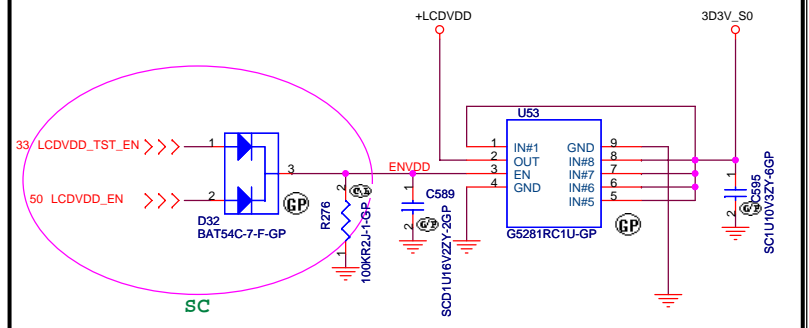
INVERTER POWER



Place near connector CAMERA1.



LCD POWER



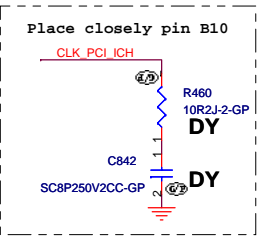
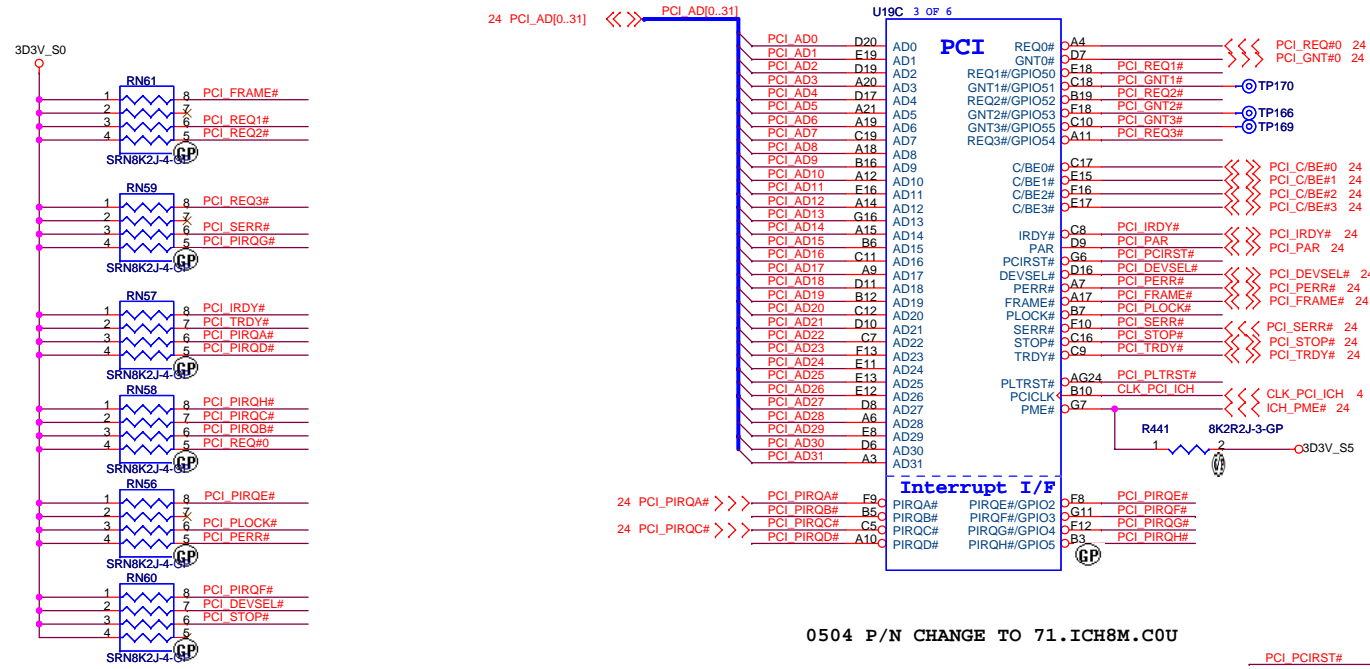
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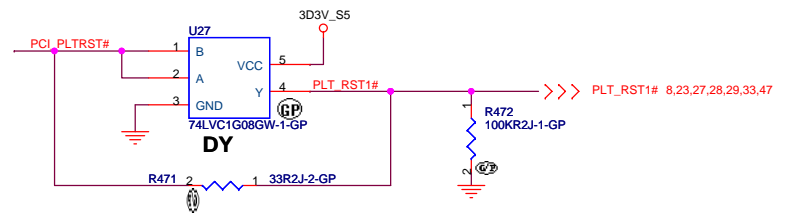
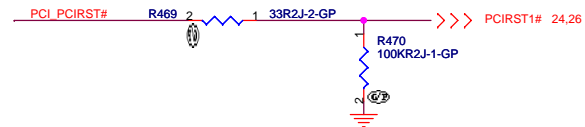
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Size A3	Document Number Hawke-Intel	Rev -1
Date: Sunday, September 09, 2007	Sheet 18	of 57

PCI Interface Routing

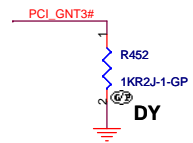
	IDSEL	INT	REQ	GNT
1394/ MediaCard	AD25	A D	0	0



0504 P/N CHANGE TO 71.ICH8M.COU



A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default *



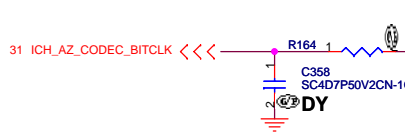
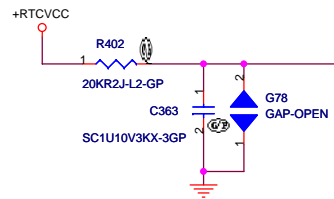
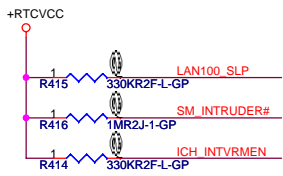
ICH8-Strap PIN

BOOT BIOS Strap		
PCI_GNT#0 (R166)	SPI_CS#1 (R167)	BOOT BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC
A16 swap override strap		
PCI_GNT#3 (R168)	low = A16 swap override enable high = default	

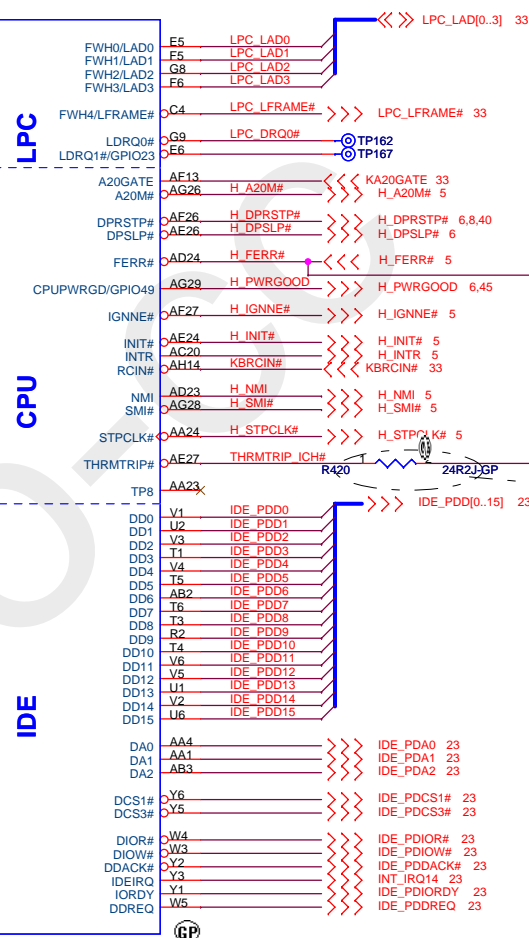
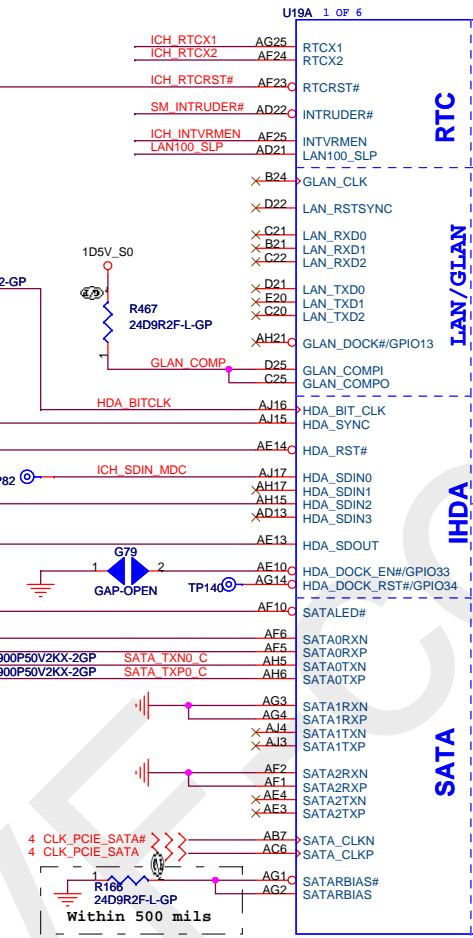
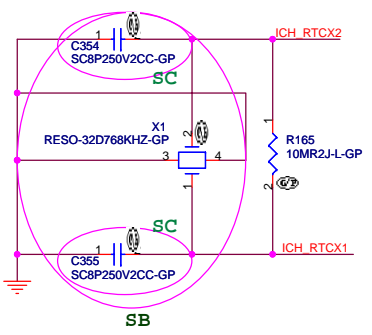
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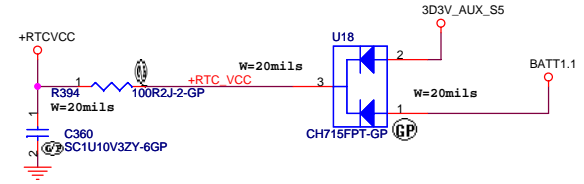
Title		
ICH8(1/4)-PCI/INT		
Size A3	Document Number	Rev
	Hawke-Intel	-1
Date: Sunday, September 09, 2007	Sheet 19 of	57



X1 CL=12.5pF±0.2pF
Freq. Tolerance:±20ppm



RTC POWER



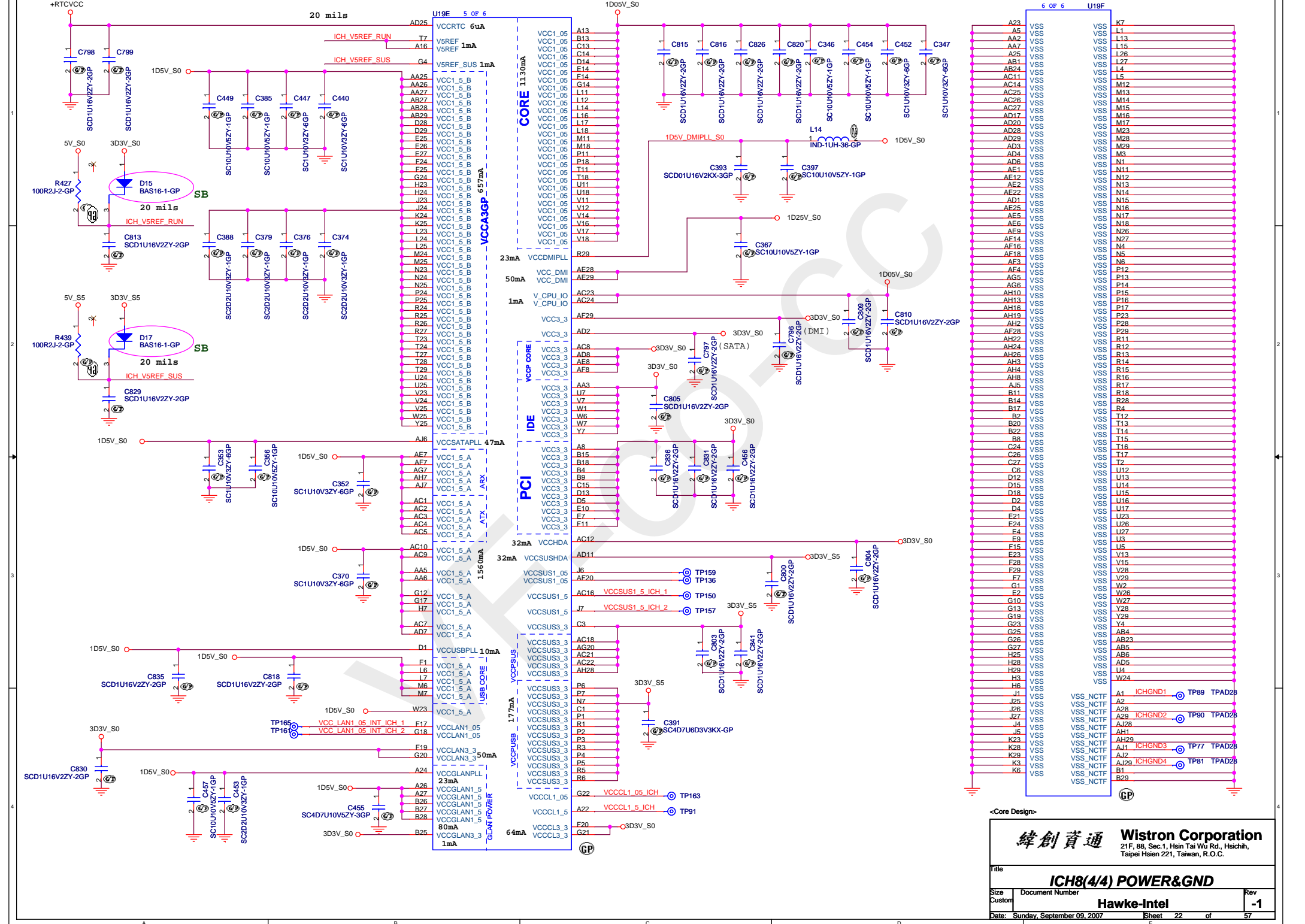
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Title: **ICH8(2/4) LAN,HD,IDE,LPC**

Size A3 Document Number: **Hawke-Intel** Rev: **-1**

Date: Sunday, September 09, 2007 Sheet 20 of 57

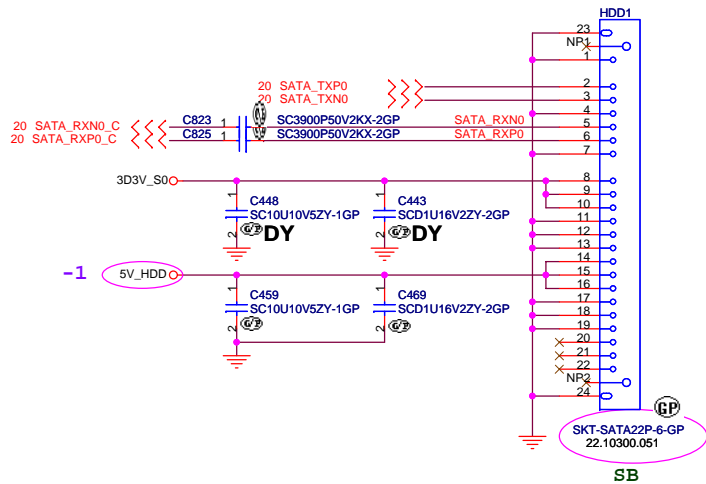


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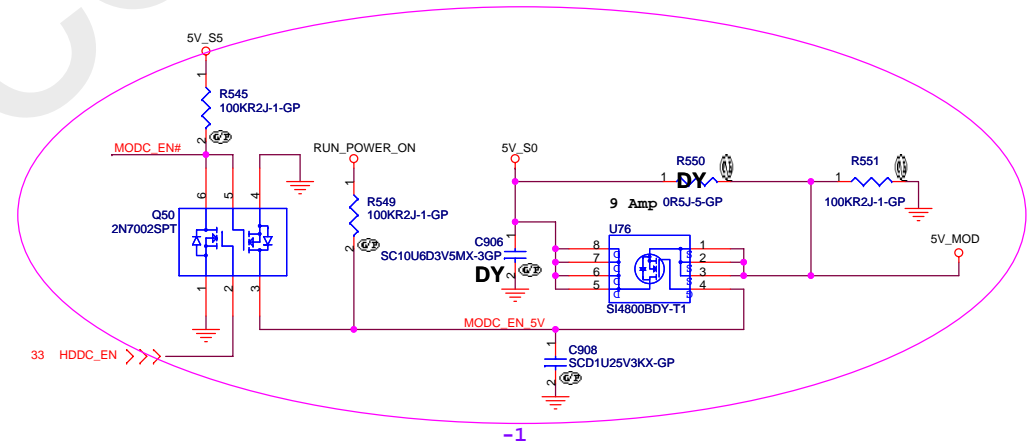
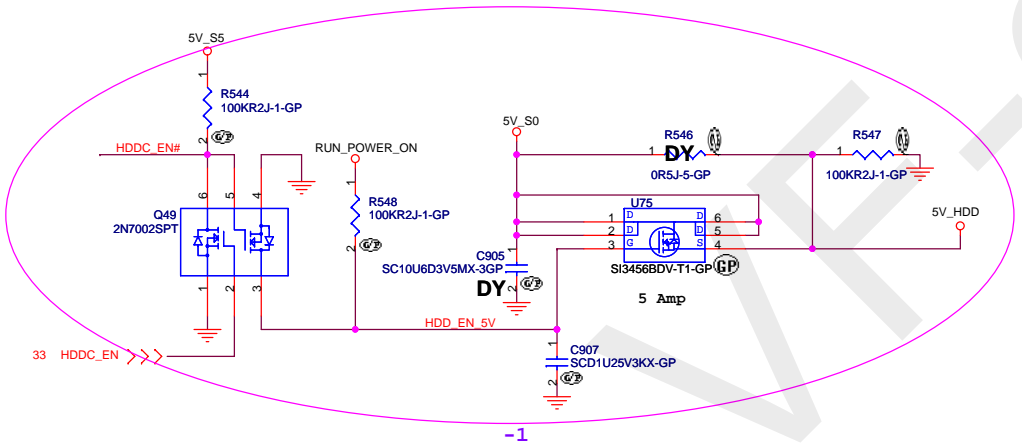
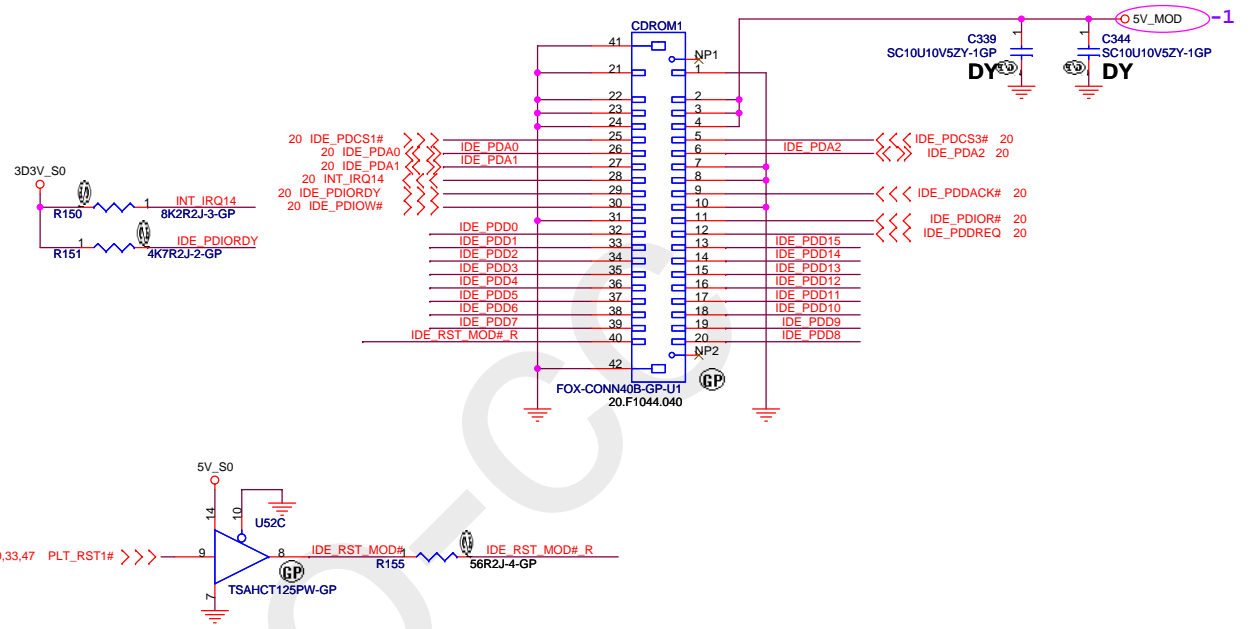
緯創資通 **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

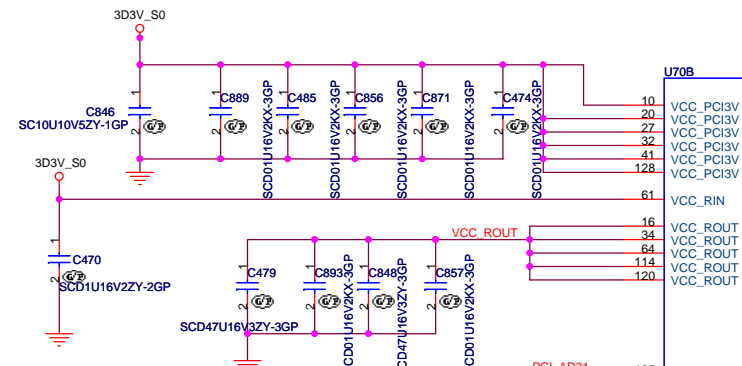
File	ICH8(4/4) POWER&GND	
Size	Document Number	Rev
Custom	Hawke-Intel	-1
Date:	Sunday, September 09, 2007	Sheet 22 of 57

SATA HDD Connector



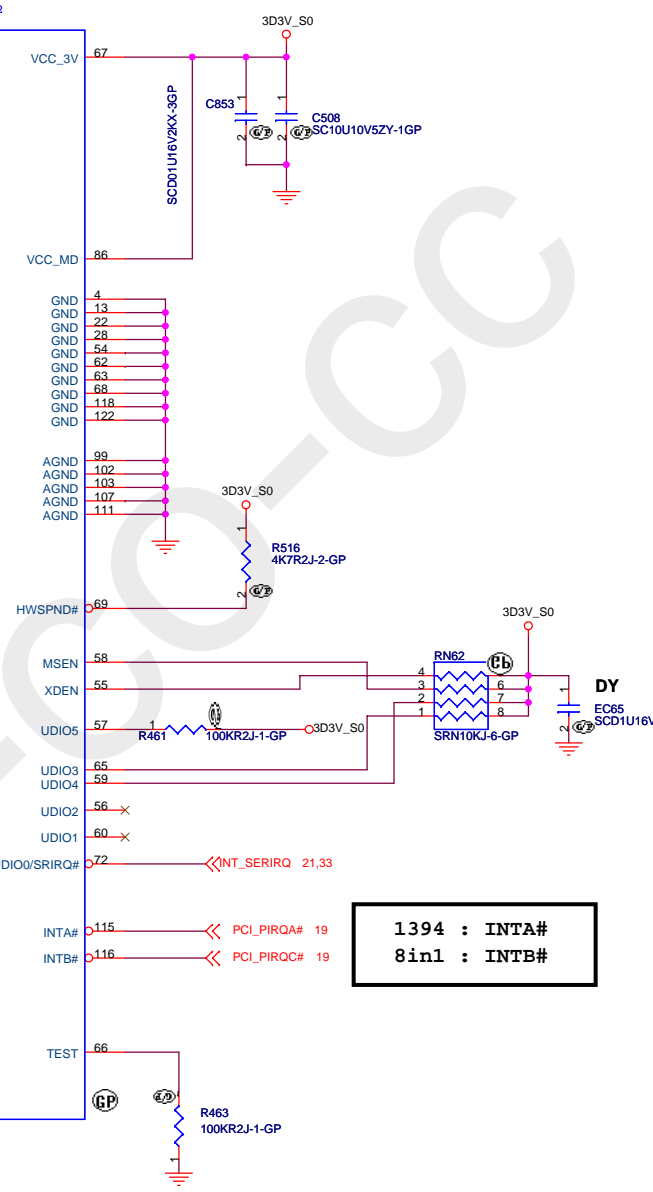
ODD Connector



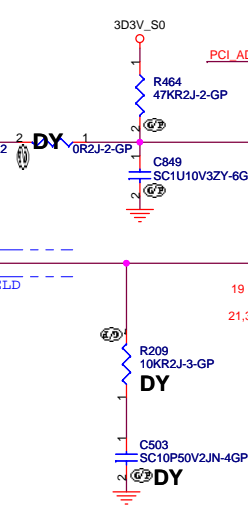


- PCI_AD31 125 AD31
- PCI_AD30 126 AD30
- PCI_AD29 127 AD29
- PCI_AD28 1 AD28
- PCI_AD27 2 AD27
- PCI_AD26 3 AD26
- PCI_AD25 5 AD25
- PCI_AD24 6 AD24
- PCI_AD23 9 AD23
- PCI_AD22 11 AD22
- PCI_AD21 12 AD21
- PCI_AD20 14 AD20
- PCI_AD19 15 AD19
- PCI_AD18 17 AD18
- PCI_AD17 18 AD17
- PCI_AD16 19 AD16
- PCI_AD15 36 AD15
- PCI_AD14 37 AD14
- PCI_AD13 38 AD13
- PCI_AD12 39 AD12
- PCI_AD11 40 AD11
- PCI_AD10 42 AD10
- PCI_AD9 43 AD9
- PCI_AD8 44 AD8
- PCI_AD7 46 AD7
- PCI_AD6 47 AD6
- PCI_AD5 48 AD5
- PCI_AD4 49 AD4
- PCI_AD3 50 AD3
- PCI_AD2 51 AD2
- PCI_AD1 52 AD1
- PCI_AD0 53 AD0
- PCI_C/BE#3 33 C/BE#3
- PCI_C/BE#2 21 C/BE#2
- PCI_C/BE#1 35 C/BE#1
- PCI_C/BE#0 45 C/BE#0
- R5C834_IDSEL 8 IDSEL
- 19 PCI_REQ#0 124 REQ#
- 19 PCI_GNT#0 123 GNT#
- 19 PCI_FRAME# 23 FRAME#
- 19 PCI_IRDY# 24 IRDY#
- 19 PCI_TRDY# 25 TRDY#
- 19 PCI_DEVSEL# 26 DEVSEL#
- 19 PCI_STOP# 29 STOP#
- 19 PCI_PERR# 30 PERR#
- 19 PCI_SERR# 31 SERR#
- GBRST# 71 GBRST#
- PCIRST# 119 PCIRST#
- PCICLK 121 PCICLK
- 19 ICH_PME# 70 PME#
- 21,33 PM_CLKRUN# 117 CLKRUN#

2 OF 2



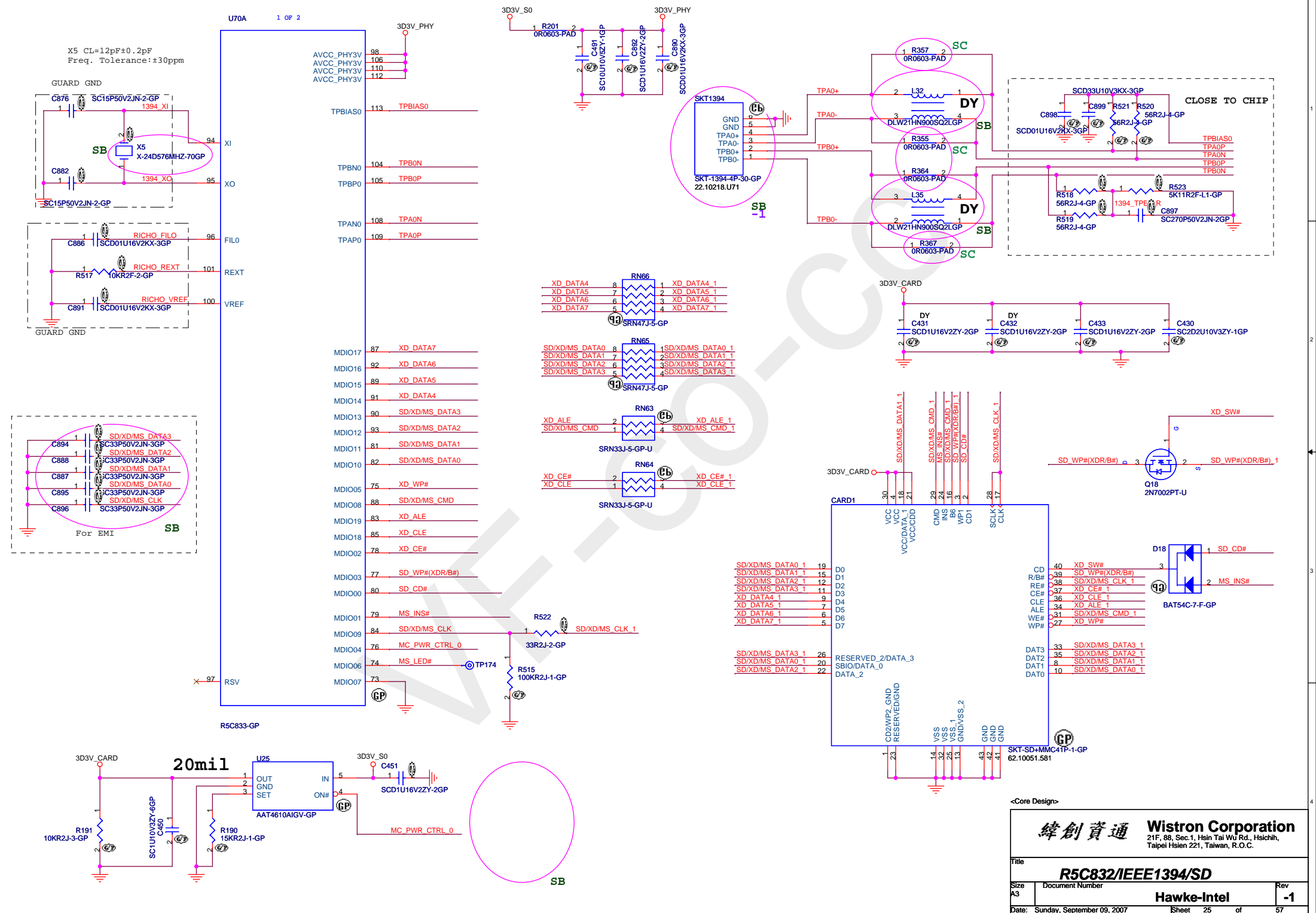
1394 : INTA#
8in1 : INTB#



- 19 PCI_AD[0..31] <<>>
- 19 PCI_PAR <<>>
- 19 PCI_C/BE#3 <<>>
- 19 PCI_C/BE#2 <<>>
- 19 PCI_C/BE#1 <<>>
- 19 PCI_C/BE#0 <<>>
- 19 PCI_REQ#0 <<>>
- 19 PCI_GNT#0 <<>>
- 19 PCI_FRAME# <<>>
- 19 PCI_IRDY# <<>>
- 19 PCI_TRDY# <<>>
- 19 PCI_DEVSEL# <<>>
- 19 PCI_STOP# <<>>
- 19 PCI_PERR# <<>>
- 19 PCI_SERR# <<>>
- 19,26 PCIRST# <<>>
- 19 ICH_PME# <<>>
- 21,33 PM_CLKRUN# <<>>

<Core Design>

<p>緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>		
<p>Title R5C833/PCI</p>		
Size A3	Document Number Hawke-Intel	Rev -1
Date: Sunday, September 09, 2007	Sheet 24	of 57



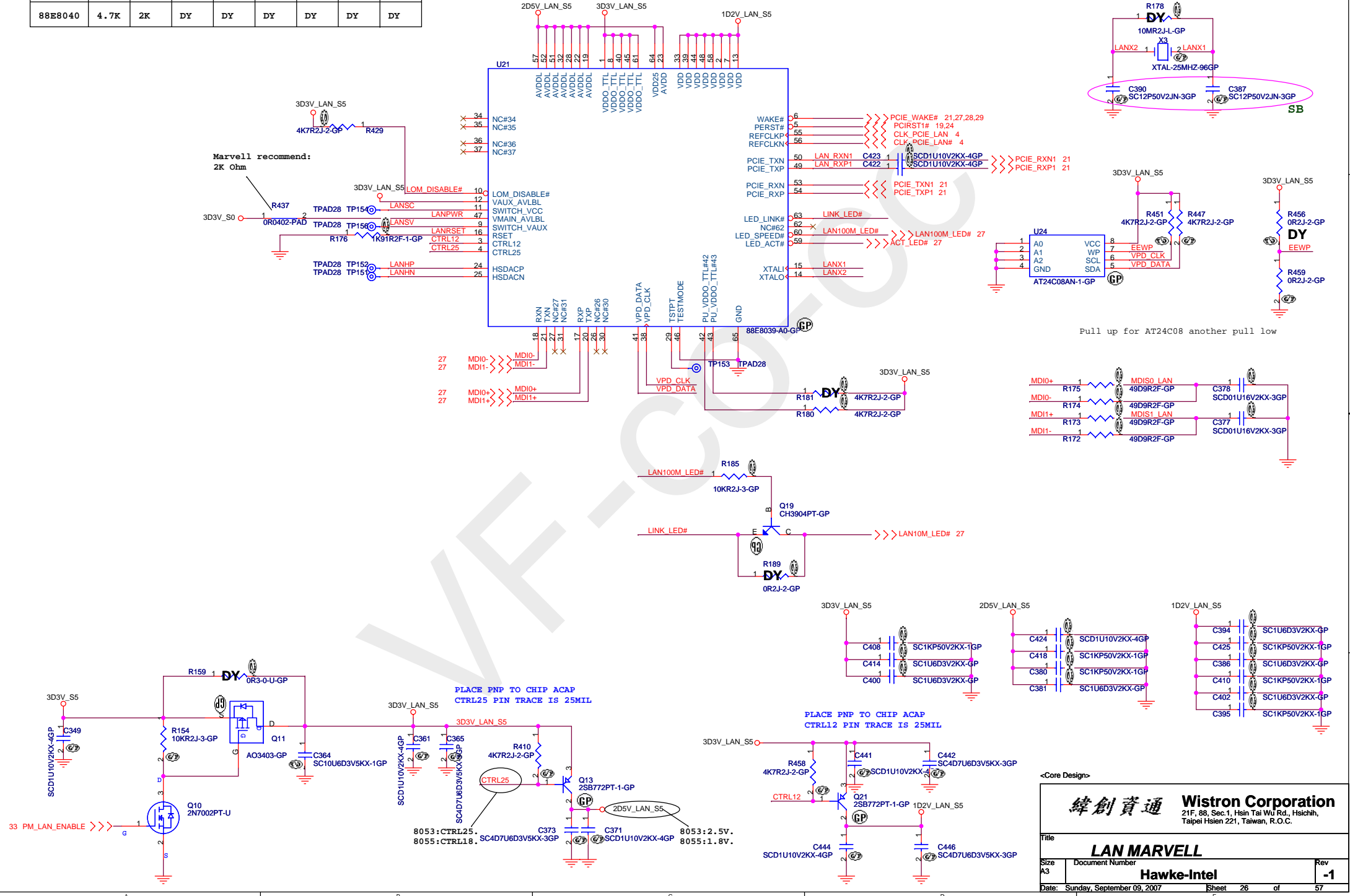
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緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **R5C832/IEEE1394/SB**

Size A3	Document Number Hawke-Intel	Rev -1
Date: Sunday, September 09, 2007 Sheet 25 of 57		

	R181	R176	R172	R173	R174	R175	C377	C378
88E8039	DY	1.91K	49.9	49.9	49.9	49.9	0.01u	0.01u
88E8040	4.7K	2K	DY	DY	DY	DY	DY	DY



X3 CL=12pF±0.2pF
Freq. Tolerance:±30ppm

Marvell recommend:
2K Ohm

Pull up for AT24C08 another pull low

PLACE PNP TO CHIP ACAP
CTRL25 PIN TRACE IS 25MIL

PLACE PNP TO CHIP ACAP
CTRL12 PIN TRACE IS 25MIL

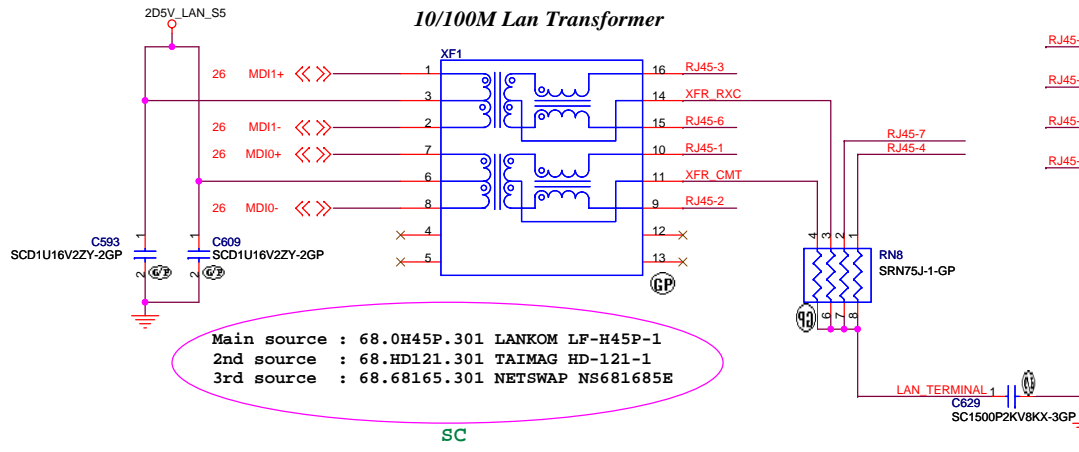
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緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

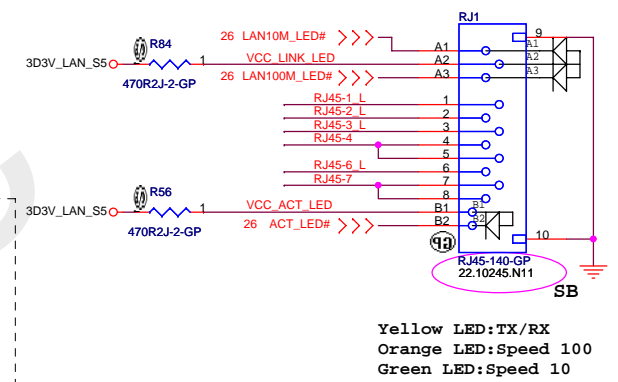
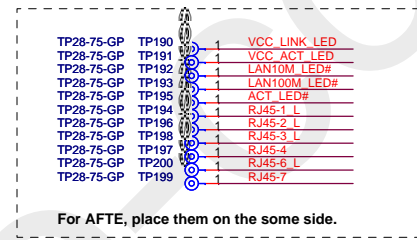
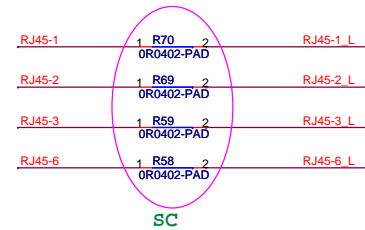
Title		LAN MARVELL	
Size	Document Number	Rev	
A3	Hawke-Intel	-1	
Date:	Sunday, September 09, 2007	Sheet	26 of 57

RJ45 Connector

1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

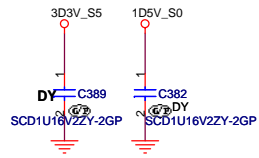


Main source : 68.0H45P.301 LANKOM LF-H45P-1
 2nd source : 68.HD121.301 TAIMAG HD-121-1
 3rd source : 68.68165.301 NETSWAP NS681685E

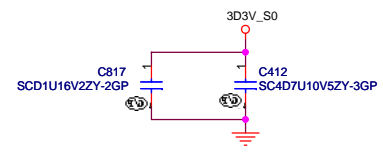
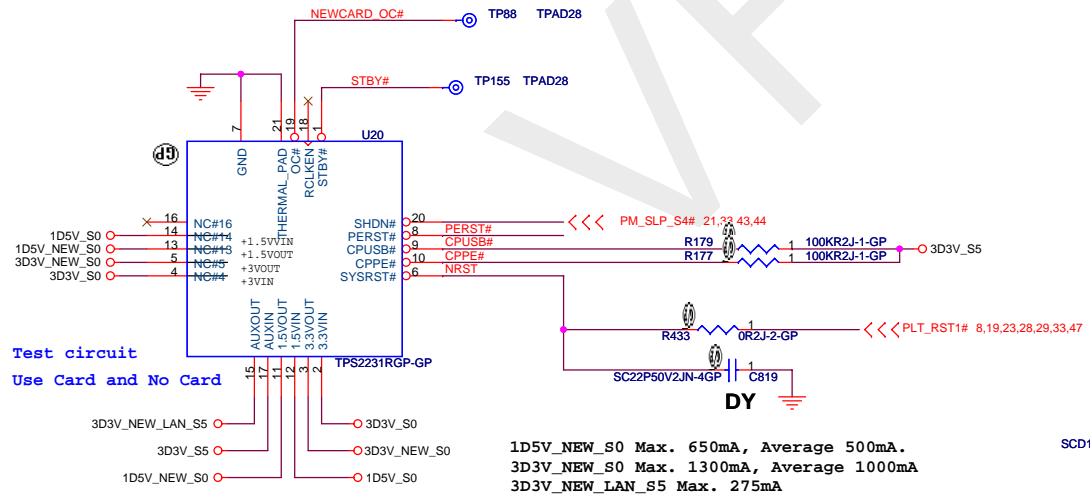
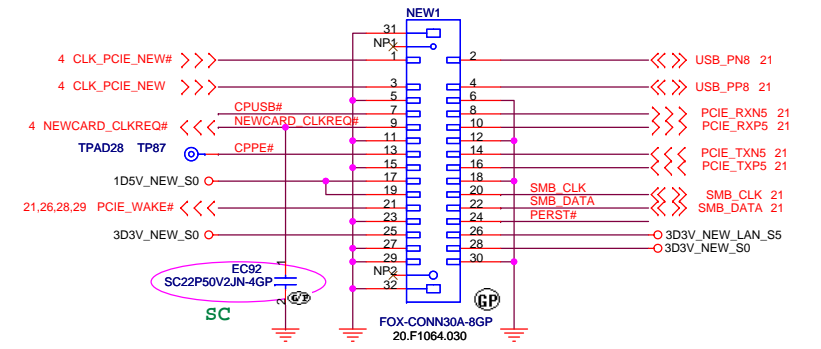
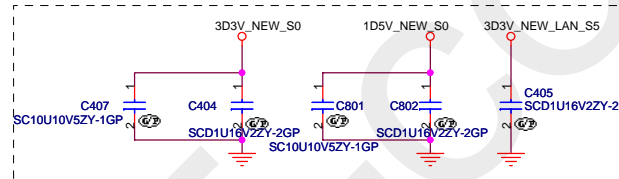


NEWCARD Connector

Place them Near to Chip



Place them Near to Connector



<Core Design>

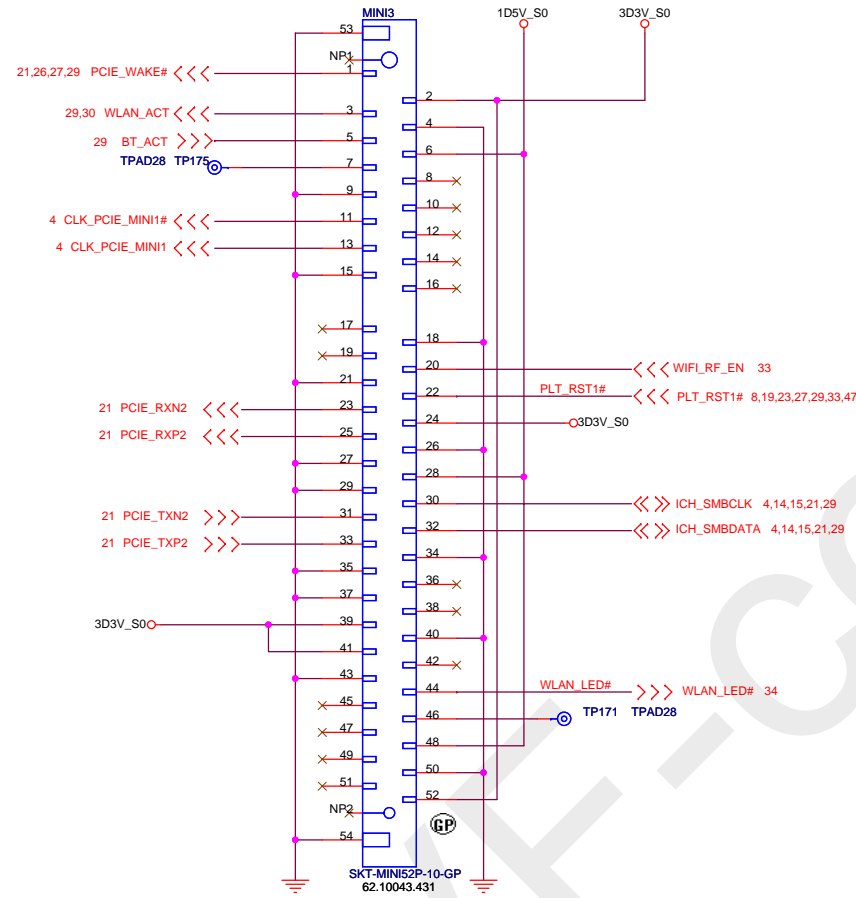
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN connector/NEW CARD**

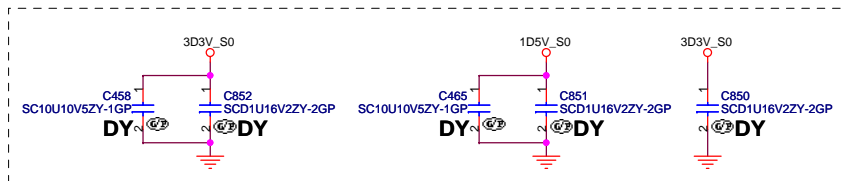
Size A3	Document Number	Rev -1
Hawke-Intel		

Date: Sunday, September 09, 2007 Sheet 27 of 57

Mini Card Connector 1(802.11a/b/g)



Main source : 20.F0992.052 P-Two A54452-A0G16-N
 2nd source : 62.10043.551 Tyco 1759553-1

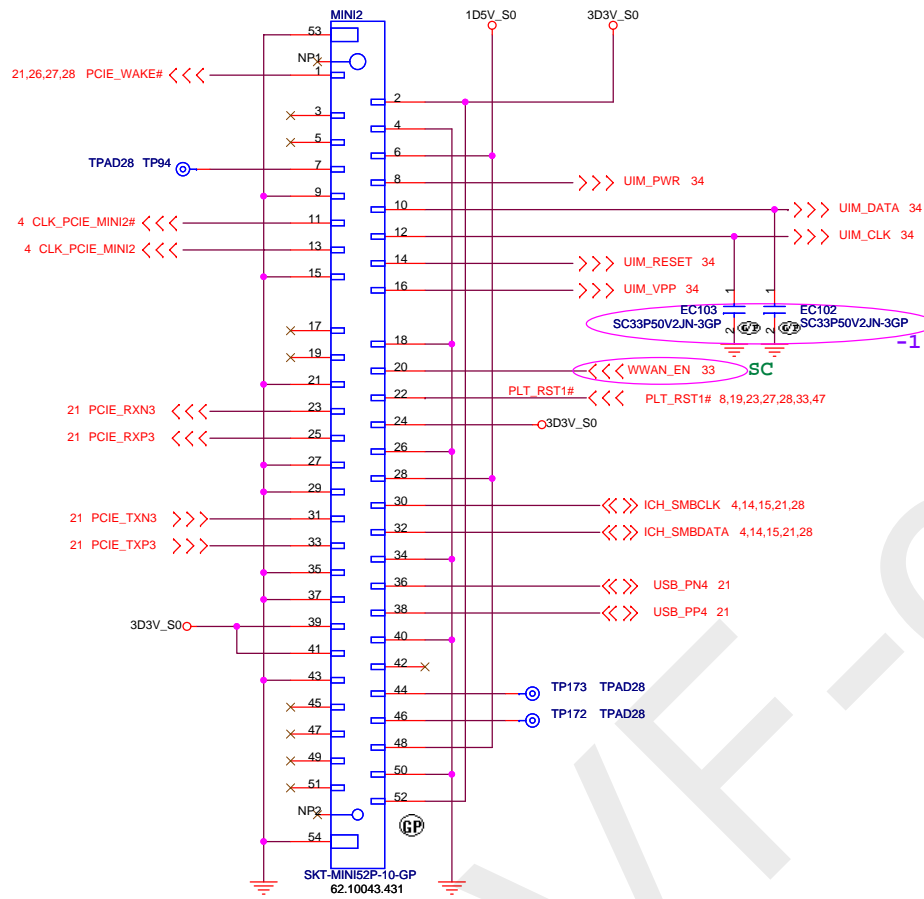


<Core Design>

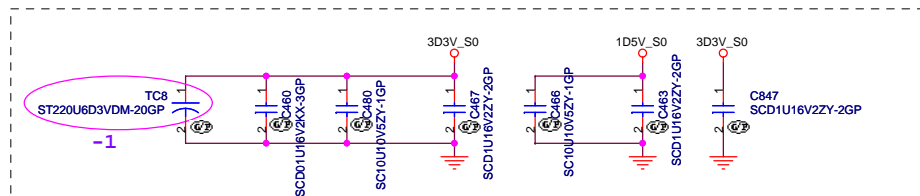
 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
MINI CARD CONN 1		
Size A3	Document Number Hawke-Intel	Rev -1
Date: Sunday, September 09, 2007		
Sheet		57

Mini Card Connector

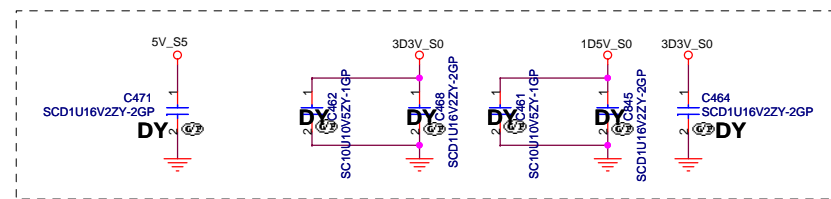
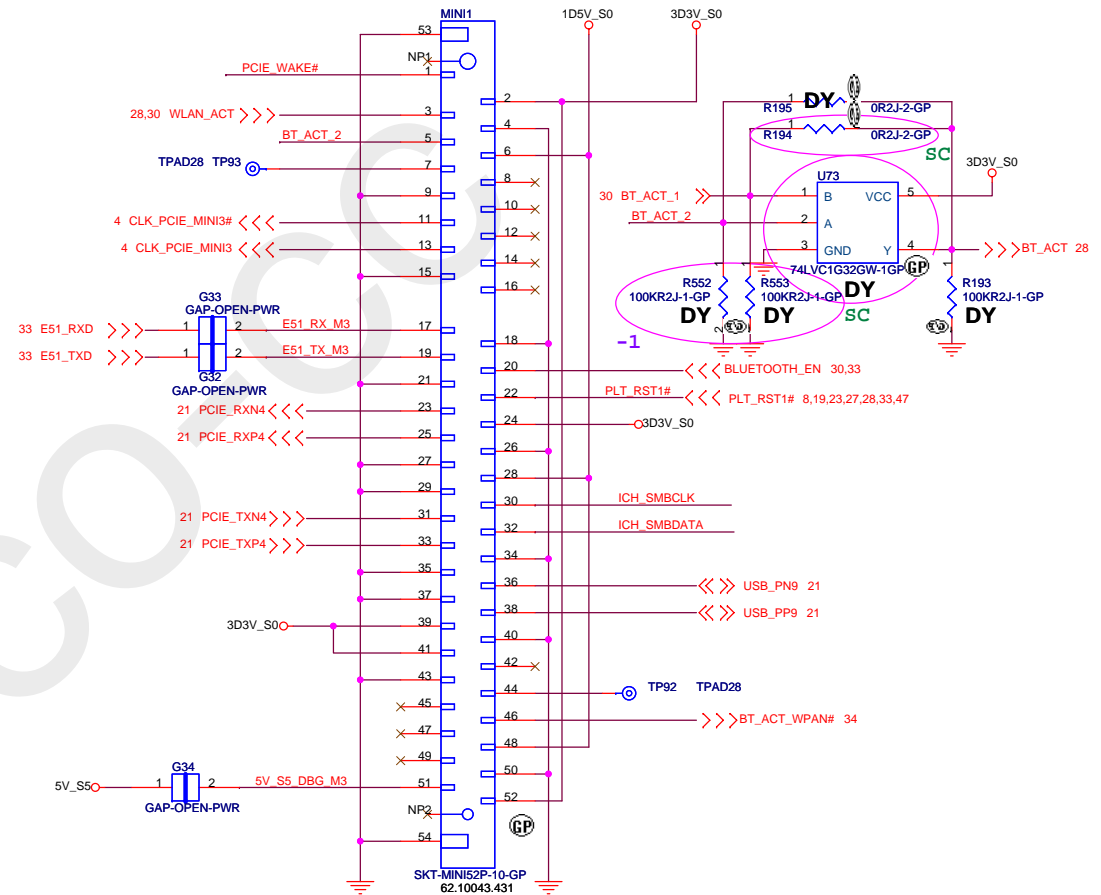
Mini Card Connector 2(WWAN)



Main source : 20.F0992.052 P-Two A54452-A0G16-N
 2nd source : 62.10043.551 Tyco 1759553-1



Mini Card Connector 3(Robson/BT)



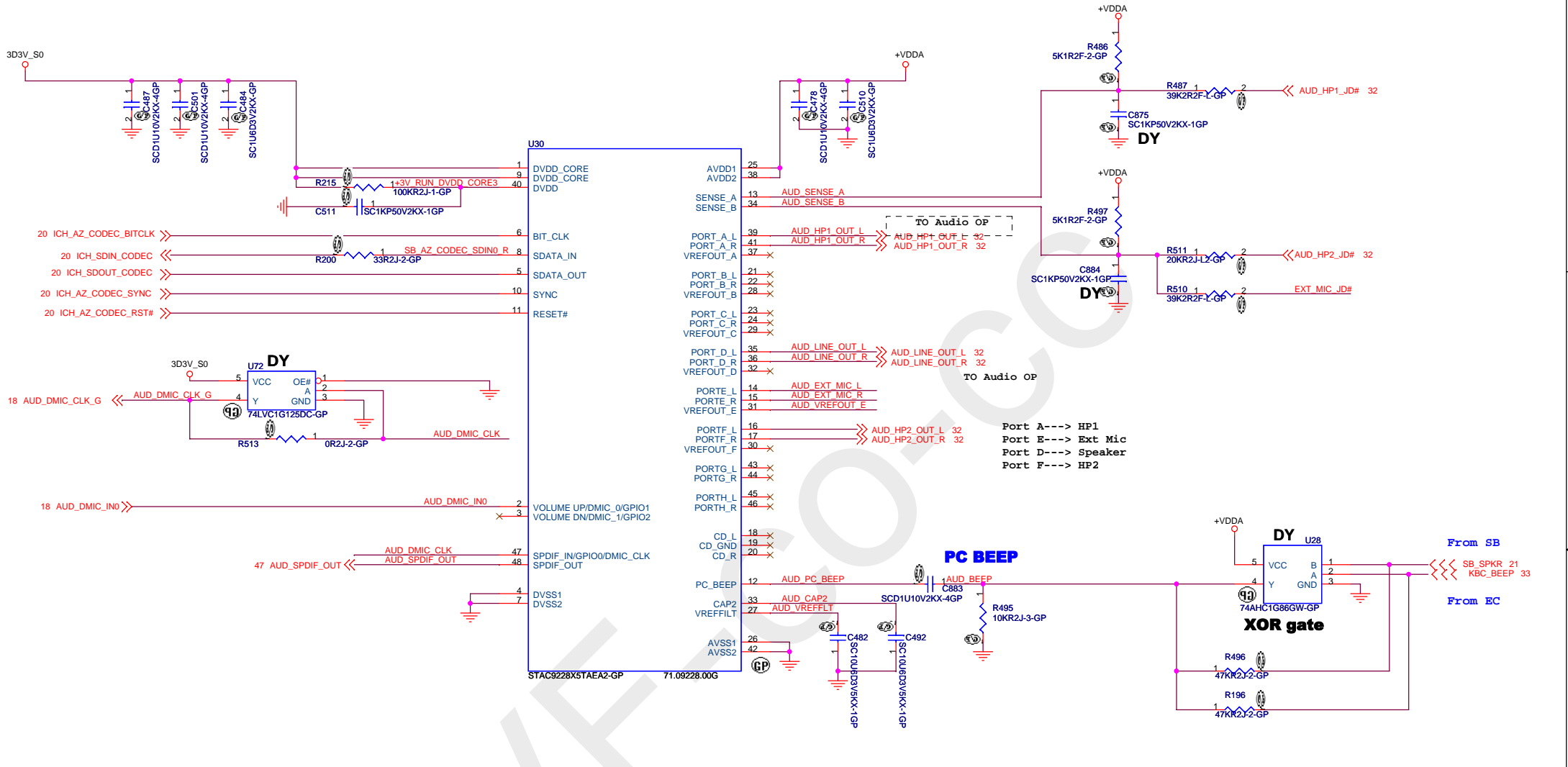
<Core Design>

緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

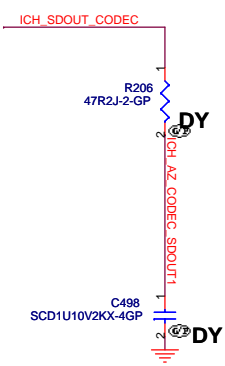
Title: **MINI CARD CONN 2 & 3**

Size A3	Document Number	Rev
	Hawke-Intel	-1

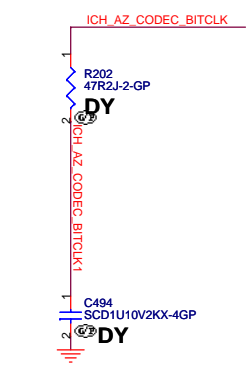
Date: Sunday, September 09, 2007 Sheet 29 of 57



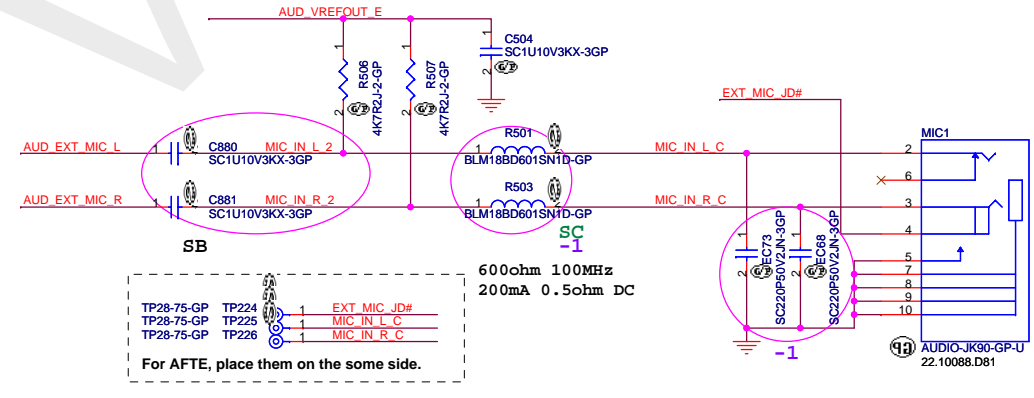
Azalia I/F EMI



Azalia I/F EMI



MIC IN

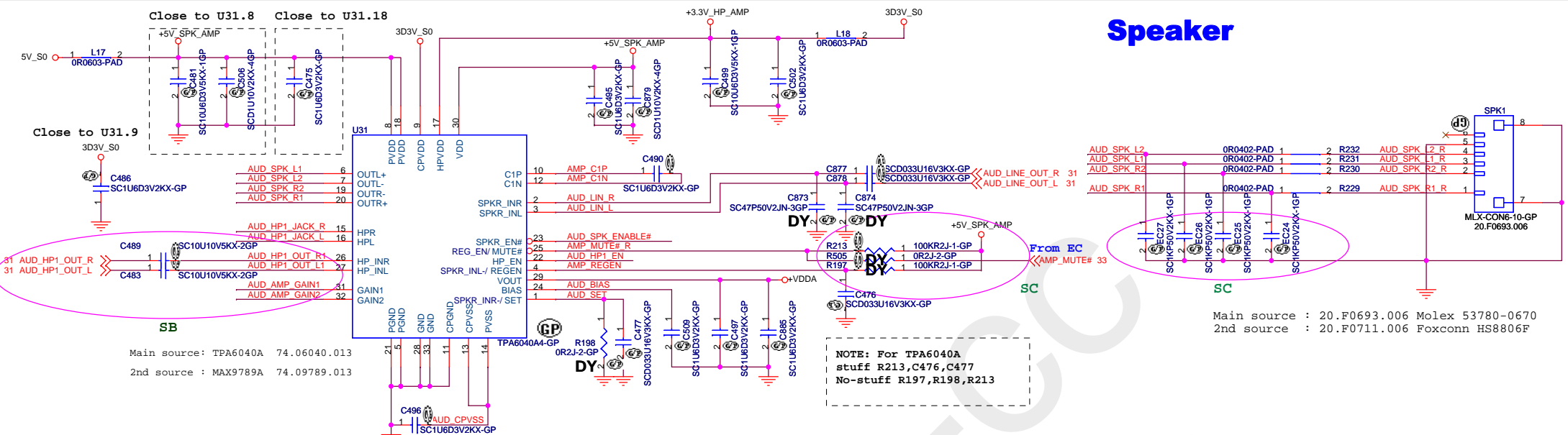


<Core Design>

緯創資通 Wistron Corporation
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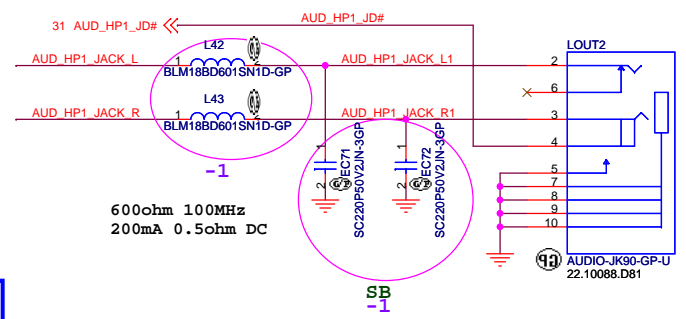
Title: **AUDIO CODEC STAC9228**

Size A3	Document Number	Rev -1
Date: Sunday, September 09, 2007	Hawke-Intel	Sheet 31 of 57

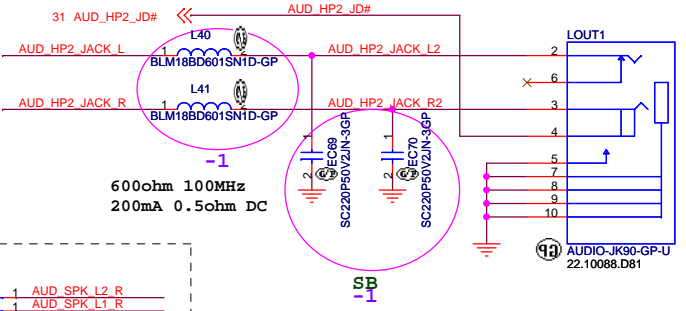


Speaker

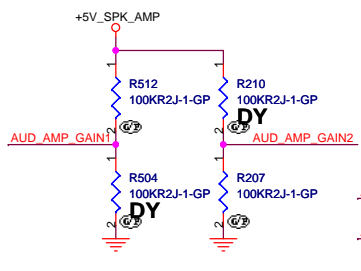
LINE1 OUT



LINE2 OUT

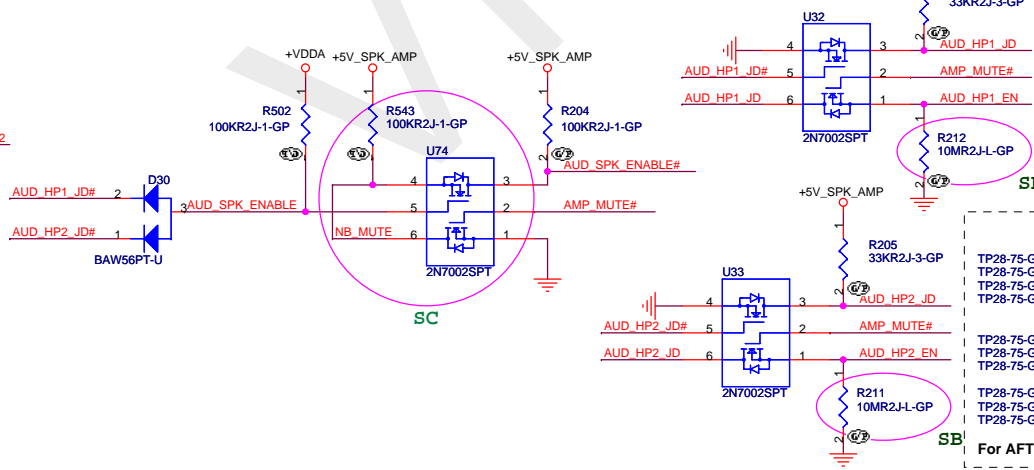


GAIN SETTING



GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

Signal inverter for speaker shutdown

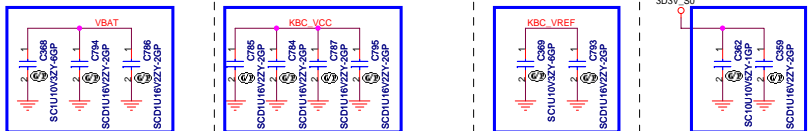


<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	AUDIO AMP/SPEAKER		Rev	-1
Size	A3	Document Number	Hawke-Intel	
Date:	Sunday, September 09, 2007	Sheet	32	of 57

For AFTE, place them on the some side.



PLACE CAP NEAR PIN80 AND PIN102 PLACE CAP NEAR PIN46,19,115,76,88 PLACE CAP NEAR PIN104 PLACE CAP Close to Pin 4

WPC8763L STRAP PIN

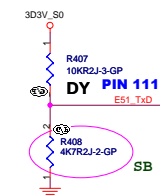
JEN0 (Pin 24)	JENK (Pin 53)	Functionality of Pins 17, 20, 21, 23, 25, 27	Functionality of Pins 47, 48, 50, 51, 52
NO PD RES	NO PD	GPIO Port	Keyboard Scan
10K PD	NO PD	GPIO signals	Keyboard Scan
NO PD	10K PD	GPIO Port	JTAG signals

TRIS#(Pin 110) TRI-STATE

Forces the device to float all its output and I/O pins, if an external 10 KΩ pull-down resistor is connected.

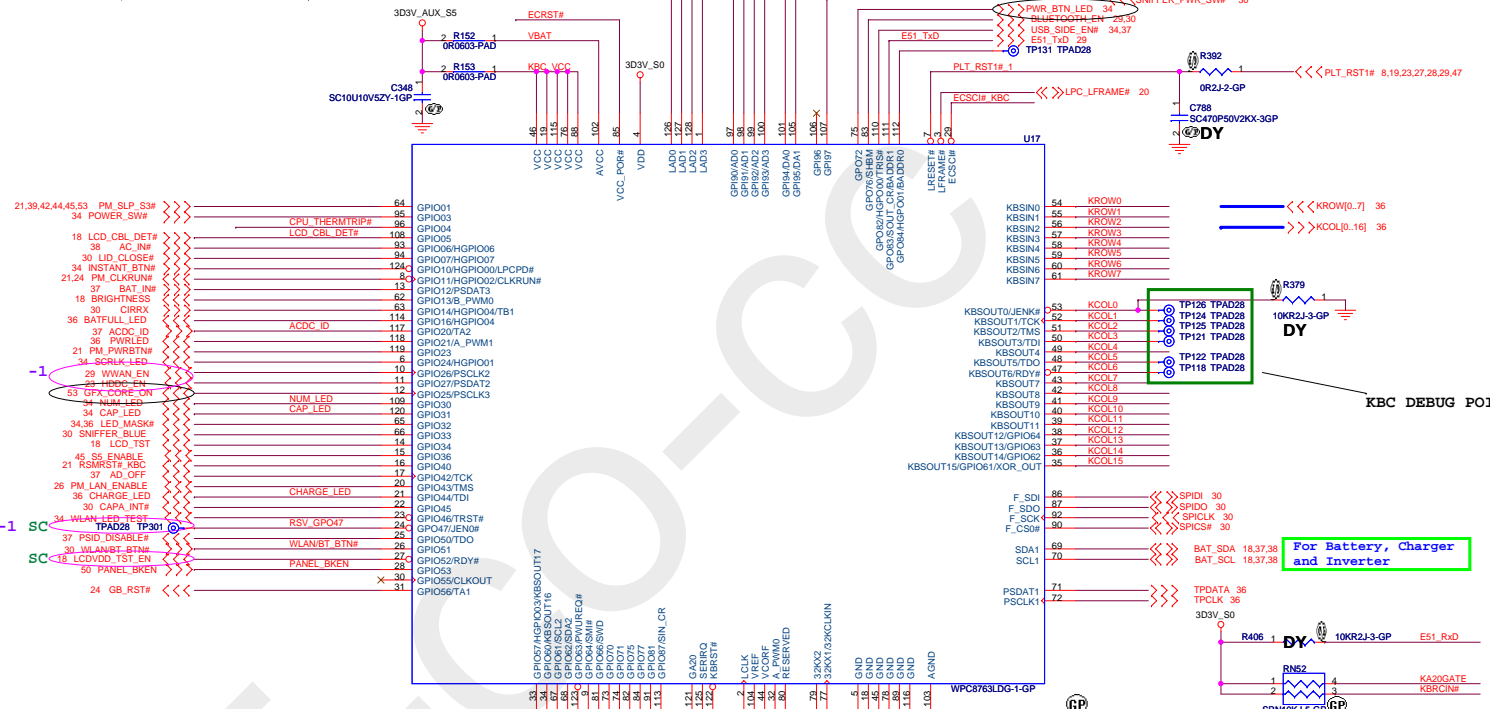
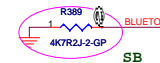
BADDR1-0 (PIN 111, 112) I/O Base Address.

10KΩ external pull-down resistor on BADDR1: Core defined



SHBM PIPN83 Shared Host BIOS Memory.

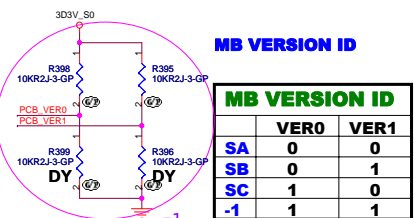
HIGH:NO SHARED(internal resistor)
LOW:SHARED BIOS memory.



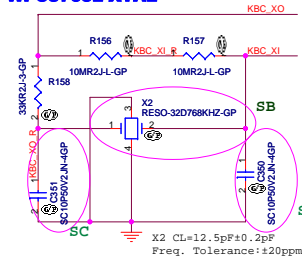
For Thermal and Capacity button module

For Battery, Charger and Inverter

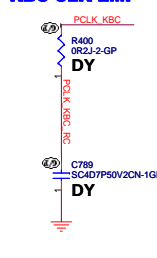
KBC DEBUG POINT



WPC8763L XTAL



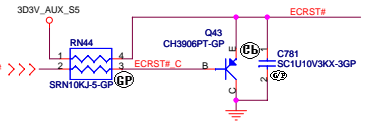
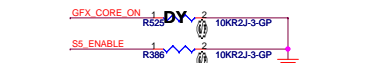
KBC CLK EMI



5.8,20,45 H_THERMTRIP# >>>



- ADIA#:to Charger
- ACDC_ID#:from Adapter Conn
- KBC_PWRBTN#:from power button
- BAT_IN#:from Battery Conn
- DC_BATFULL#:for Battery charge LED 1
- CHARGE_LED#:for Battery charge LED 2
- WLAN_TEST#:for WKS test WLAN LED
- AD_OFF:enable AC adapter power source
- WLAN/BT_BTN#:from Wlan on/off button
- GMCH_BL_ON:Sense The Backlight On/Off Status from VGA Chip
- WIRELESS_EN:Disable/Enable Wireless Module
- BLUETOOTH_EN:Disable/Enable Bluetooth
- USB_PWR_EN#:to on/off USB power switch
- AC_IN#:From Charge



Core Design:

緯創資通 Wistron Corporation
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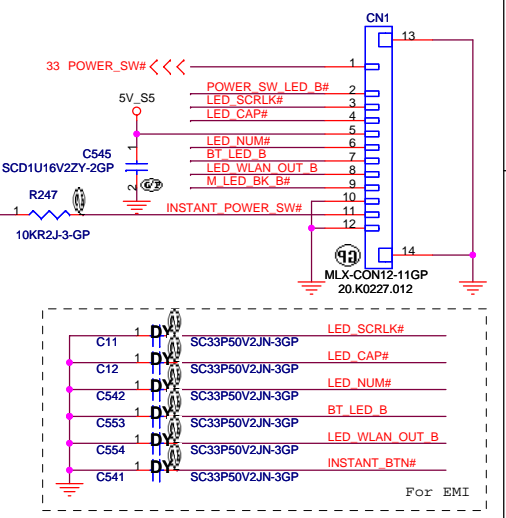
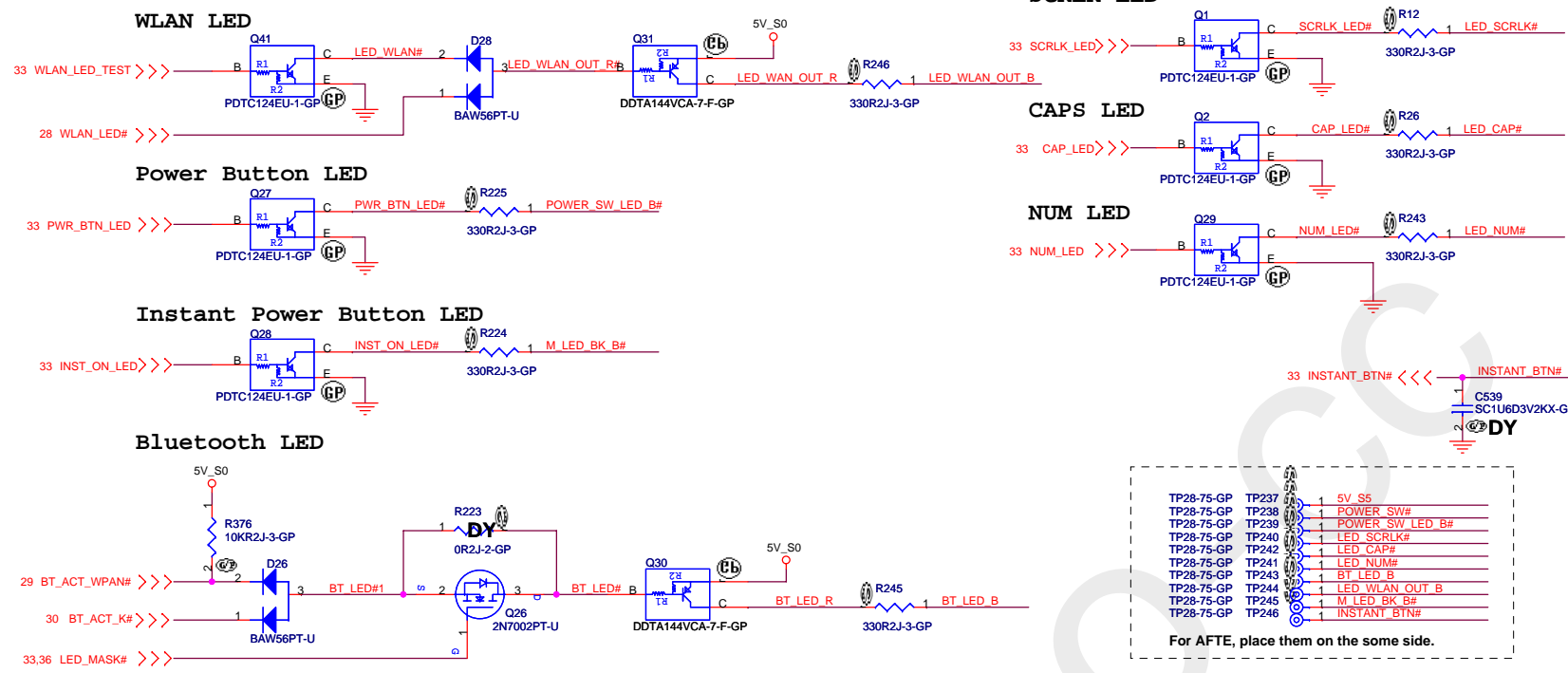
File: **KBC Winbond WPC8763L**

Doc: Document Number **Hawke-Intel** Rev: **-1**

Date: Sunday, September 09, 2007 Sheet: 33 of 57



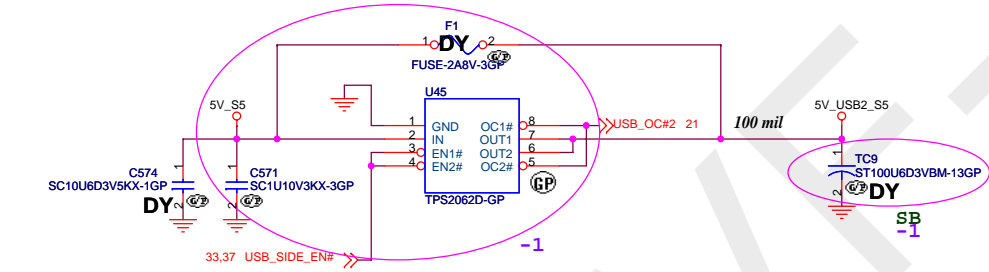
To LED Board



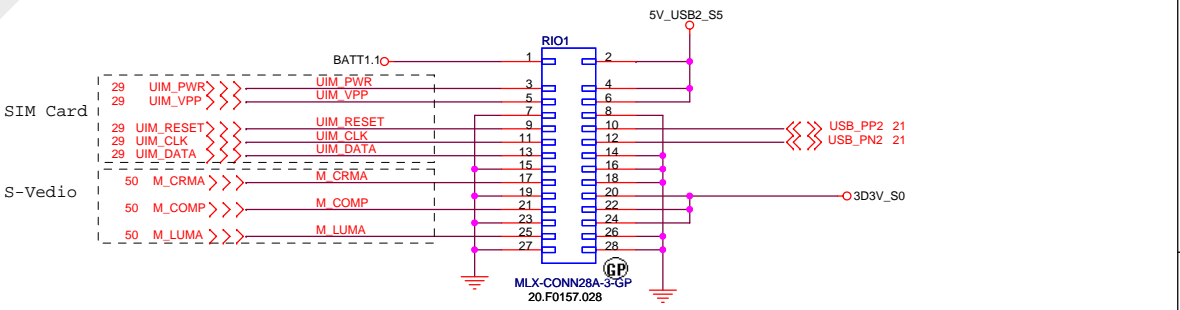
TP28-75-GP	TP237	1	5V_S5
TP28-75-GP	TP238	1	POWER_SW#
TP28-75-GP	TP239	1	POWER_SW_LED_B#
TP28-75-GP	TP240	1	LED_SCRLK#
TP28-75-GP	TP242	1	LED_CAP#
TP28-75-GP	TP241	1	LED_NUM#
TP28-75-GP	TP243	1	BT_LED_B
TP28-75-GP	TP244	1	LED_WLAN_OUT_B
TP28-75-GP	TP245	1	M_LED_BK_B#
TP28-75-GP	TP246	1	INSTANT_BTN#

For AFTE, place them on the same side.

USB POWER

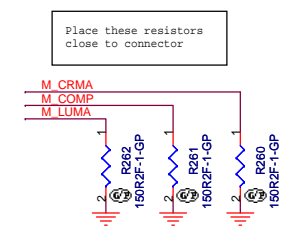


To Right I/O Board



TP28-75-GP	TP247	1	BATT1.1
TP28-75-GP	TP248	1	5V_USB2_S5
TP28-75-GP	TP250	1	USB_PP2
TP28-75-GP	TP249	1	USB_PN2
TP28-75-GP	TP251	1	UIM_PWR
TP28-75-GP	TP253	1	UIM_VPP
TP28-75-GP	TP252	1	UIM_RESET
TP28-75-GP	TP254	1	UIM_CLK
TP28-75-GP	TP255	1	UIM_DATA
TP28-75-GP	TP256	1	M_CRMA
TP28-75-GP	TP257	1	M_COMP
TP28-75-GP	TP258	1	M_LUMA

For AFTE, place them on the same side.



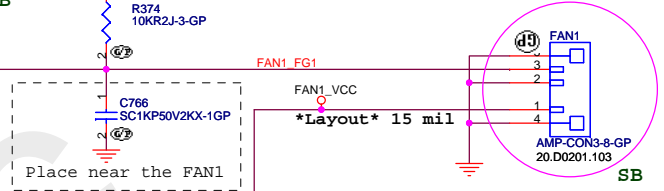
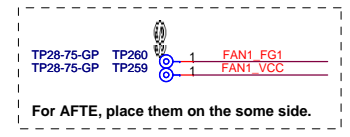
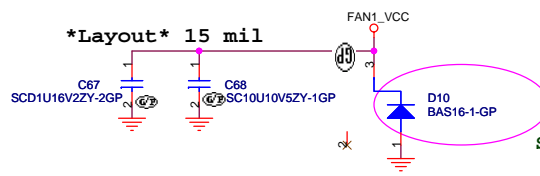
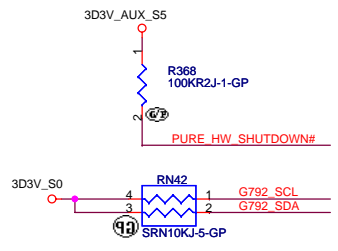
<Core Design>

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

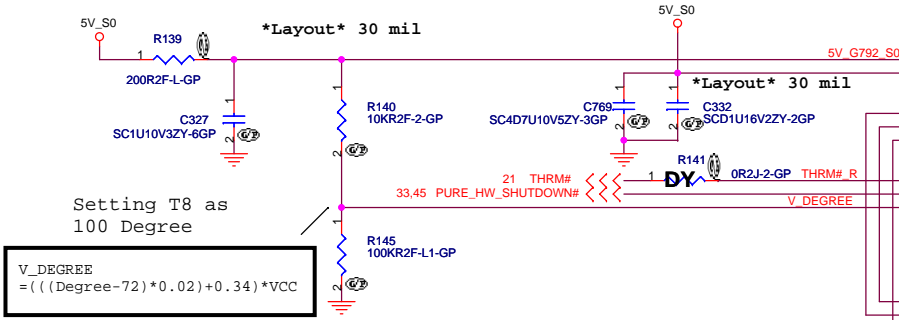
Title: **Right I/O/ Power Dash**

Size A3 Document Number: **Hawke-Intel** Rev: **-1**

Date: Sunday, September 09, 2007 Sheet 34 of 57

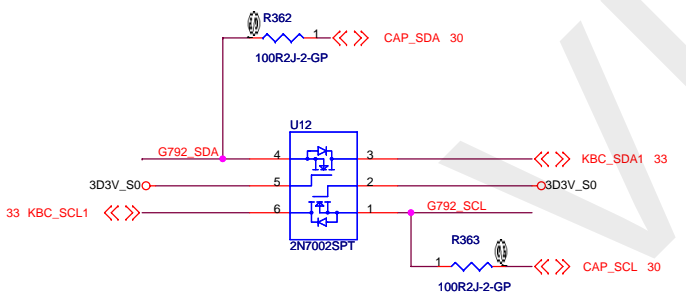
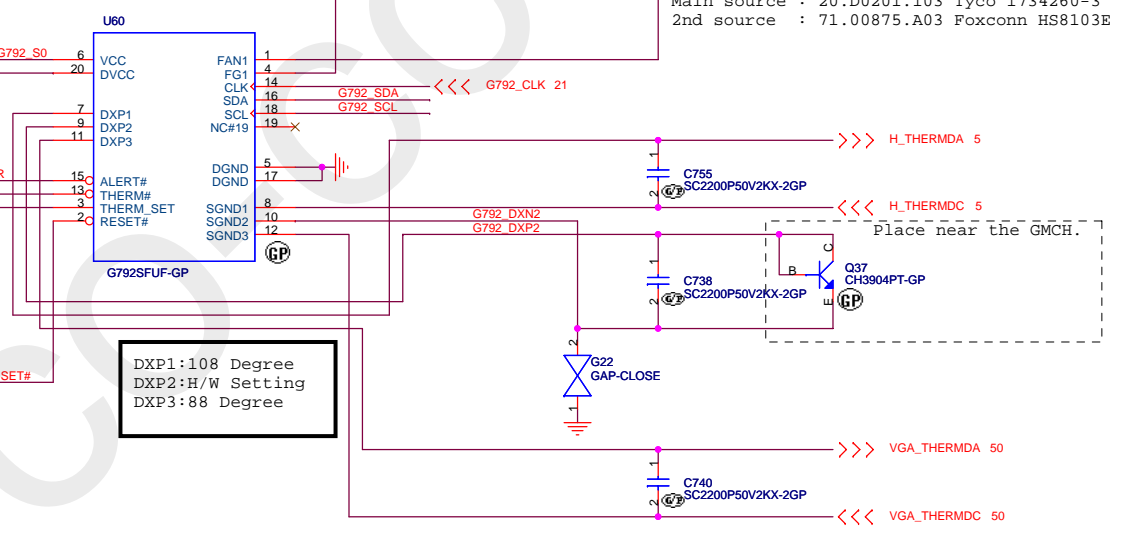


Main source : 20.D0201.103 Tyco 1734260-3
2nd source : 71.00875.A03 Foxconn HS8103E

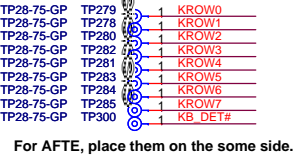
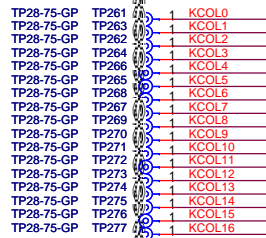
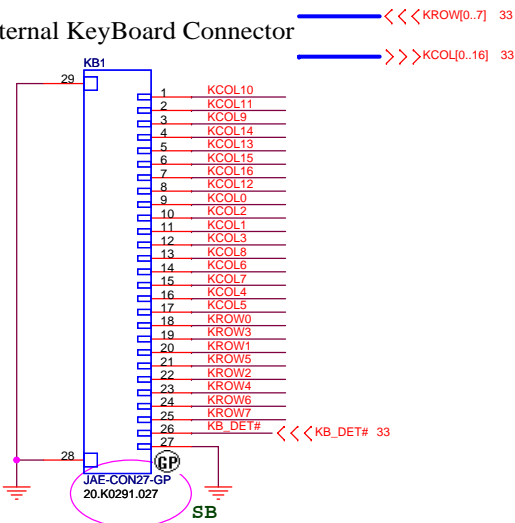


$$V_DEGREE = (((Degree - 72) * 0.02) + 0.34) * VCC$$

DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree

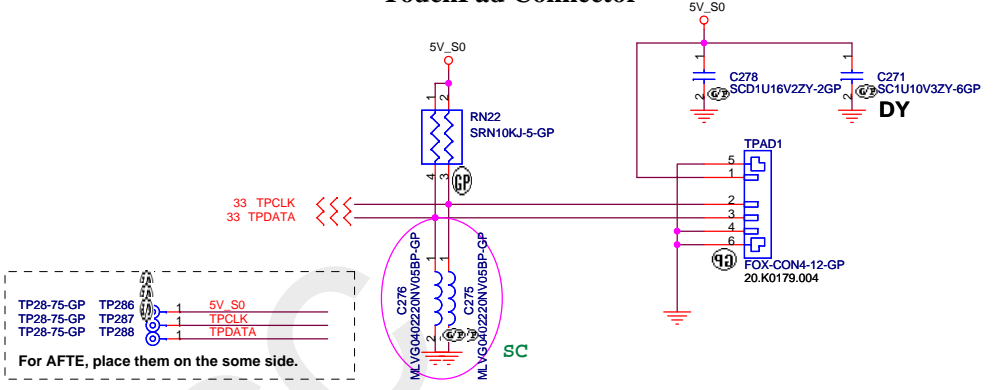


Internal Keyboard Connector



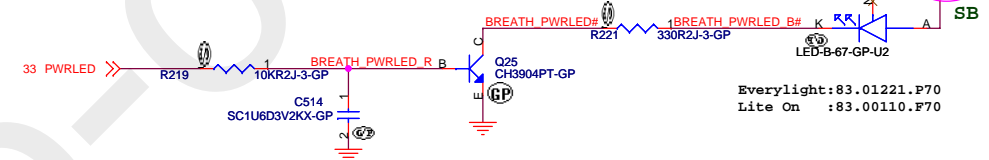
For AFTE, place them on the same side.

TouchPad Connector



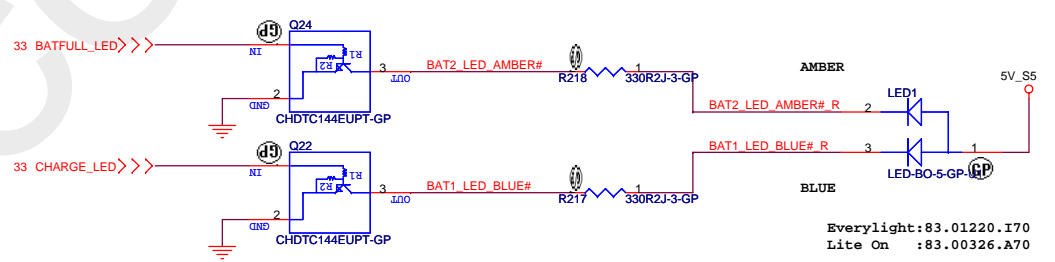
For AFTE, place them on the same side.

Power & Suspend LED



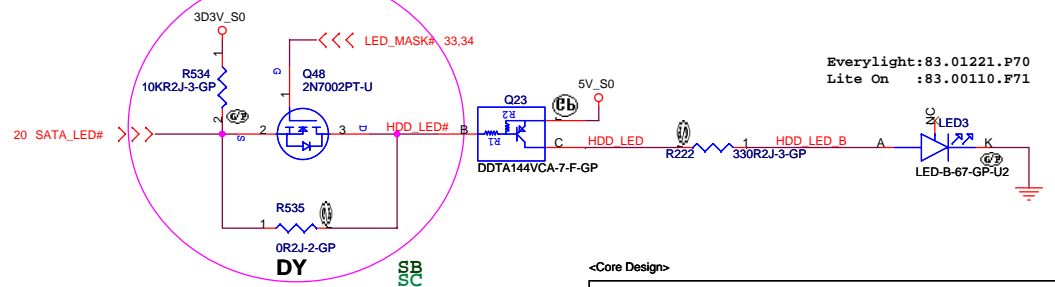
Everylight: 83.01221.P70
Lite On : 83.00110.F70

Battery LED

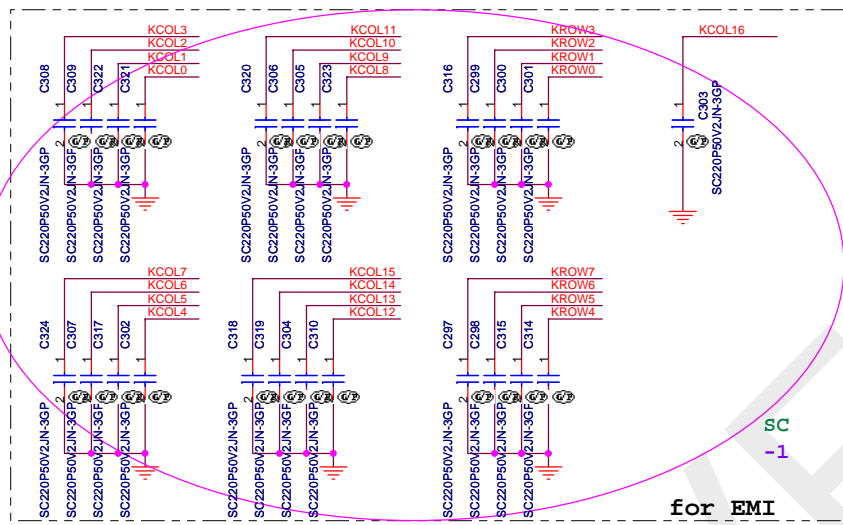


Everylight: 83.01220.I70
Lite On : 83.00326.A70

HDD LED



Everylight: 83.01221.P70
Lite On : 83.00110.F71



for EMI

LED NAME ACTIVE SIGNAL

Power Button LED	PWR_BTN_LED	*
Instant Power Button LED	INST_ON_LED	*
WLAN LED	WLAN_LED_TEST (from KBC)	
	WLAN_LED# (from Mini)	
Bluetooth LED	BT_ACT_WPAN# (from Mini)	
	BT_ACT_K# (from BT)	
NUM LED	NUM_LED (from KBC)	
SCRLK LED	SCRLK_LED (from KBC)	
CAPS LED	CAP_LED (from KBC)	

LED Board

Main Board

Power & Suspend LED	PWRLED	(from KBC)
HDD LED	SATA_LED#	(from ICH)
Battery LED	BATFULL_LED	(from KBC)

<Core Design>

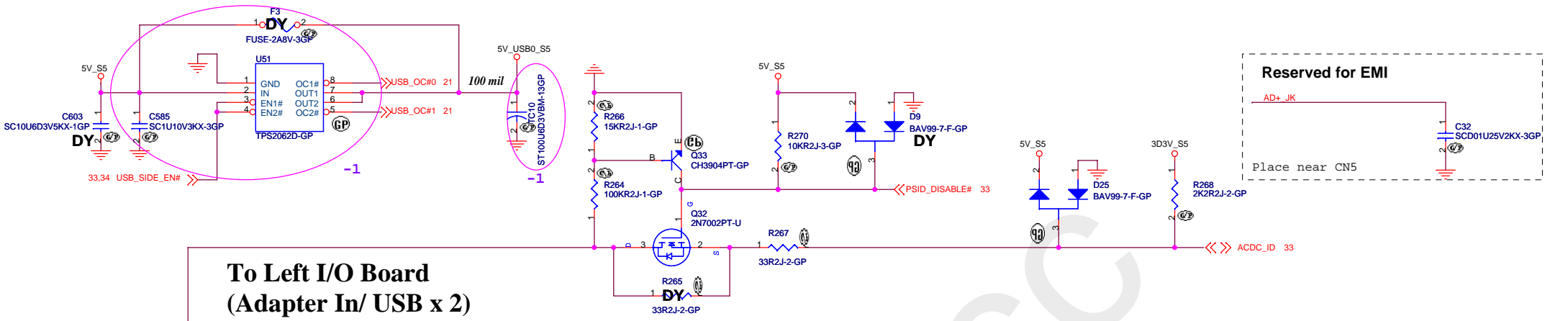
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

File: **Keyboard/Touchpad**

Size A3 Document Number **Hawke-Intel** Rev **-1**

Date: Sunday, September 09, 2007 Sheet 36 of 57

USB POWER



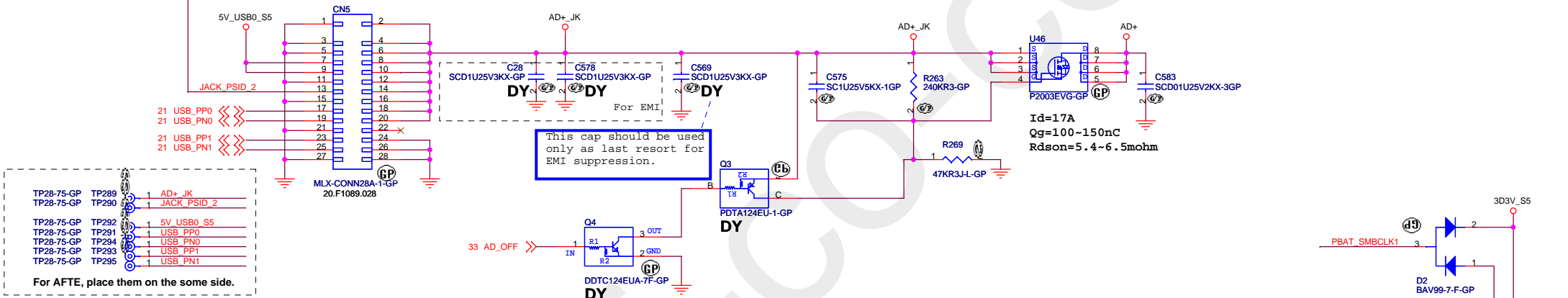
Reserved for EMI

AD+_JK

Place near CN5

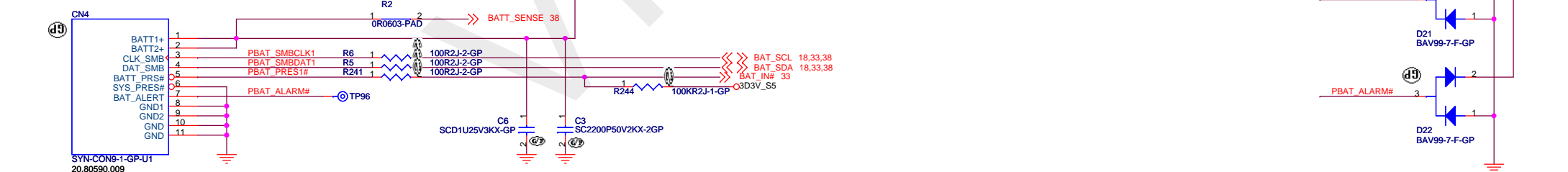
C32 SCD01U25V2KX-3GP

To Left I/O Board (Adapter In/ USB x 2)



- TP28-75-GP TP289 1 AD+_JK
 - TP28-75-GP TP290 1 JACK PSID_2
 - TP28-75-GP TP292 1 5V_USB0_S5
 - TP28-75-GP TP291 1 USB_PP0
 - TP28-75-GP TP294 1 USB_PN0
 - TP28-75-GP TP293 1 USB_PP1
 - TP28-75-GP TP295 1 USB_PN1
- For AFTE, place them on the same side.

Batt Connector



SYN-CON9-1-GP-U1
20.80590.009
Main source : 20.80590.009
2nd source : 20.80626.009
Suyin 200275MR009G548ZL
Foxconn BP02093-P5351-7F

- TP28-75-GP TP296 1 BT+
 - TP28-75-GP TP297 1 PBAT_SMBCLK1
 - TP28-75-GP TP298 1 PBAT_SMBDAT1
 - TP28-75-GP TP299 1 PBAT_PREST1#
- For AFTE, place them on the same side.

- PBAT_SMBCLK1 C5 1 SC33P50V2JN-3GP
 - PBAT_SMBDAT1 C4 1 SC33P50V2JN-3GP
 - PBAT_PREST1# C526 1 SC33P50V2JN-3GP
- For EMI

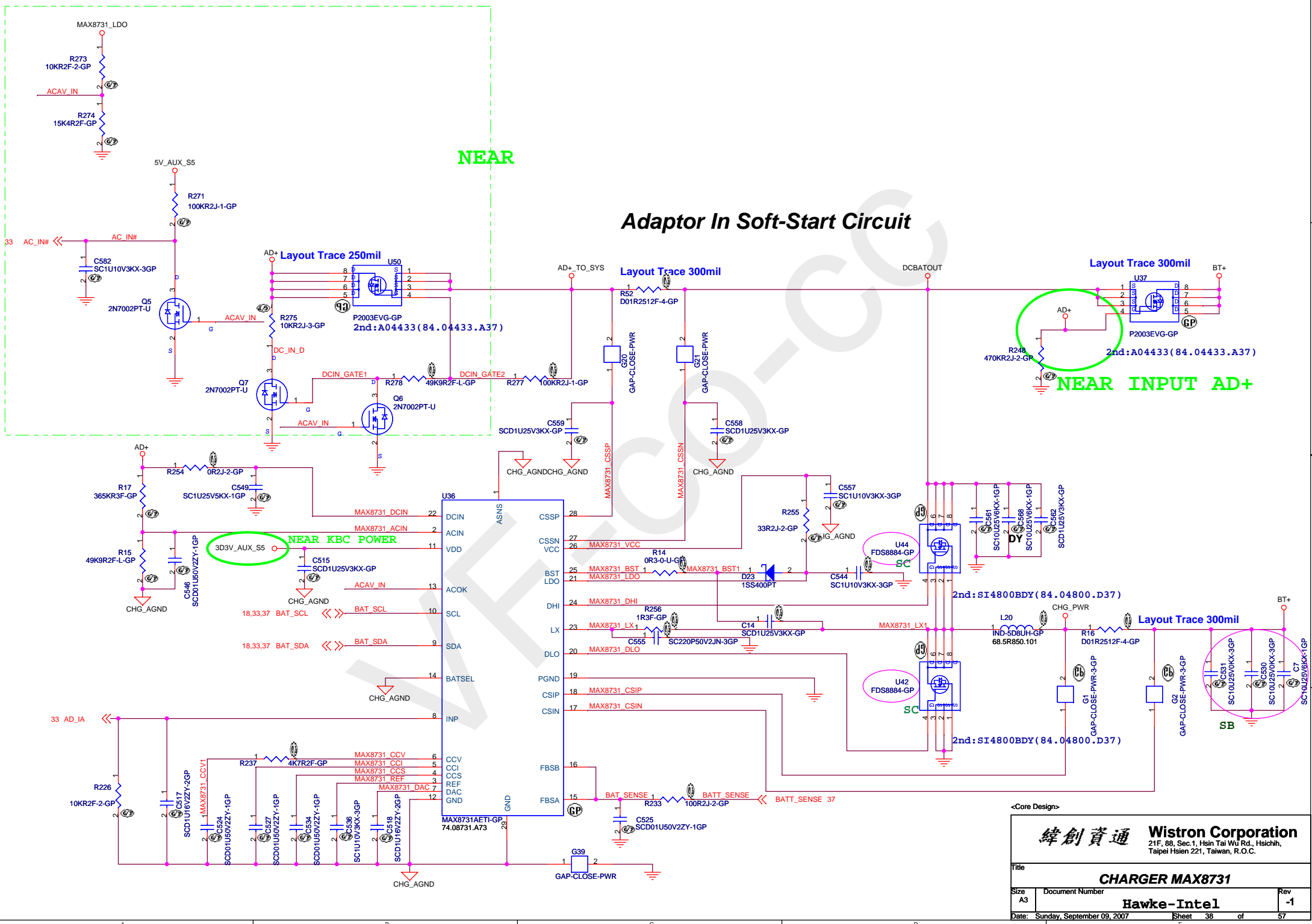
<Core Design>

緯創資通 Wistron Corporation
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Title: **AD/BATT CONN**

Size A3 Document Number: **Hawke-Intel** Rev: **-1**

Date: Sunday, September 09, 2007 Sheet 37 of 57

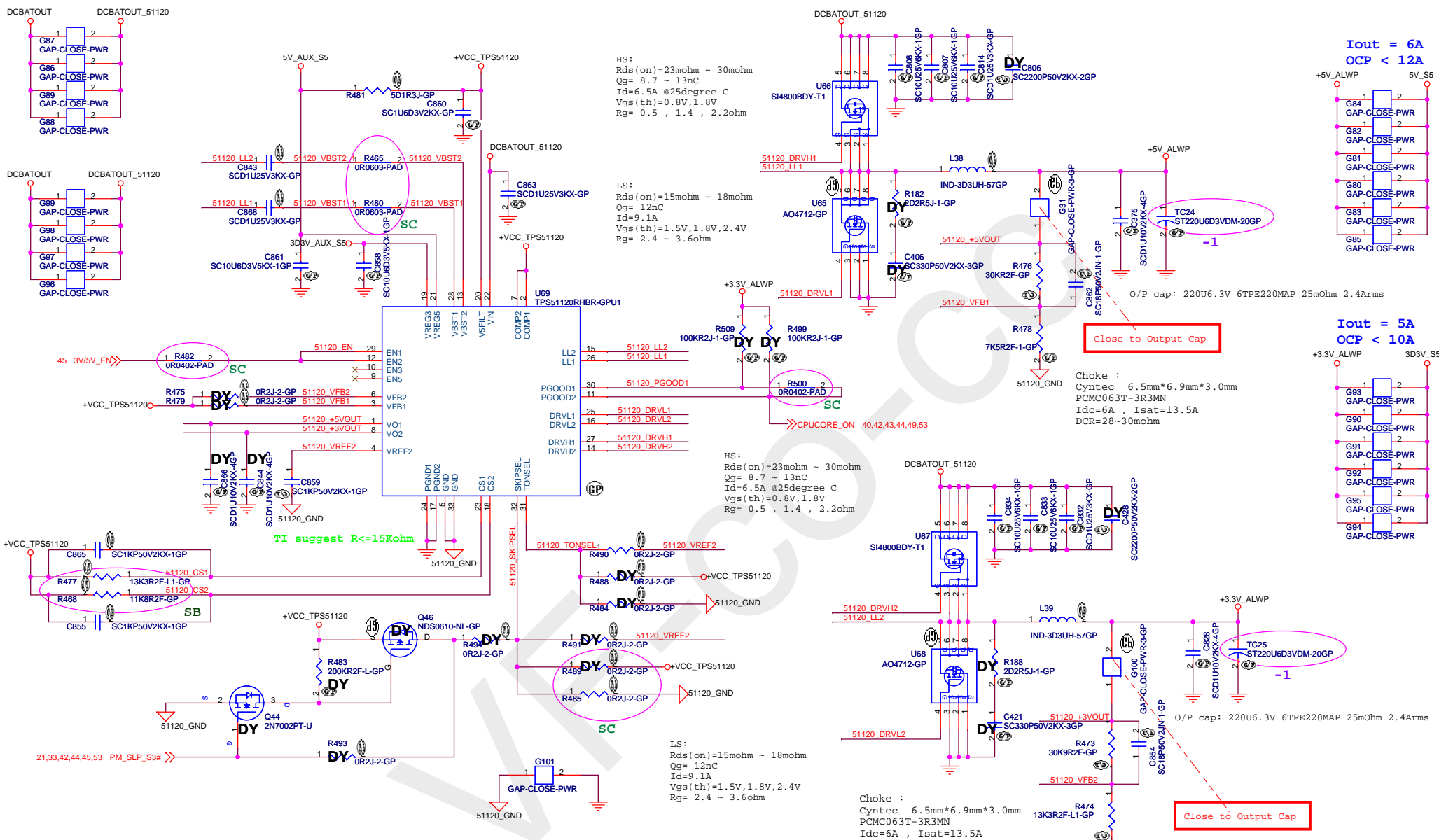


Adaptor In Soft-Start Circuit

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 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

File: **CHARGER MAX8731**

Size A3	Document Number	Rev -1
Date: Sunday, September 09, 2007		Sheet 38 of 57



HS:
 Rds(on)=23mohm ~ 30mohm
 Qg= 8.7 ~ 13nC
 Id=6.5A @25degree C
 Vgs(th)=0.8V,1.8V
 Rg= 0.5 , 1.4 , 2.2ohm

LS:
 Rds(on)=15mohm ~ 18mohm
 Qg= 12nC
 Id=9.1A
 Vgs(th)=1.5V,1.8V,2.4V
 Rg= 2.4 ~ 3.6ohm

HS:
 Rds(on)=23mohm ~ 30mohm
 Qg= 8.7 ~ 13nC
 Id=6.5A @25degree C
 Vgs(th)=0.8V,1.8V
 Rg= 0.5 , 1.4 , 2.2ohm

LS:
 Rds(on)=15mohm ~ 18mohm
 Qg= 12nC
 Id=9.1A
 Vgs(th)=1.5V,1.8V,2.4V
 Rg= 2.4 ~ 3.6ohm

Iout = 6A
 OCP < 12A

Iout = 5A
 OCP < 10A

Close to Output Cap

Choke :
 Cyntec 6.5mm*6.9mm*3.0mm
 PCMC063T-3R3MN
 Idc=6A , Isat=13.5A
 DCR=28~30mohm

Choke :
 Cyntec 6.5mm*6.9mm*3.0mm
 PCMC063T-3R3MN
 Idc=6A , Isat=13.5A
 DCR=28~30mohm

$$V_{out} = 1V \cdot (R1 + R2) / R2$$

	GND	VREF2	FLOA1	VSFILT
SKIPSEL	AUTOSKIP	AUTOSKIP / FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 580k/CH2	280k/CH1 430k/CH2	220k/CH1 330k/CH2	180k/CH1 2870k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1, EN2	Switcher OFF	not use	Switcher ON	Switcher ON
EN3, EN5	LDO OFF	not use	LDO ON	VREG3 on

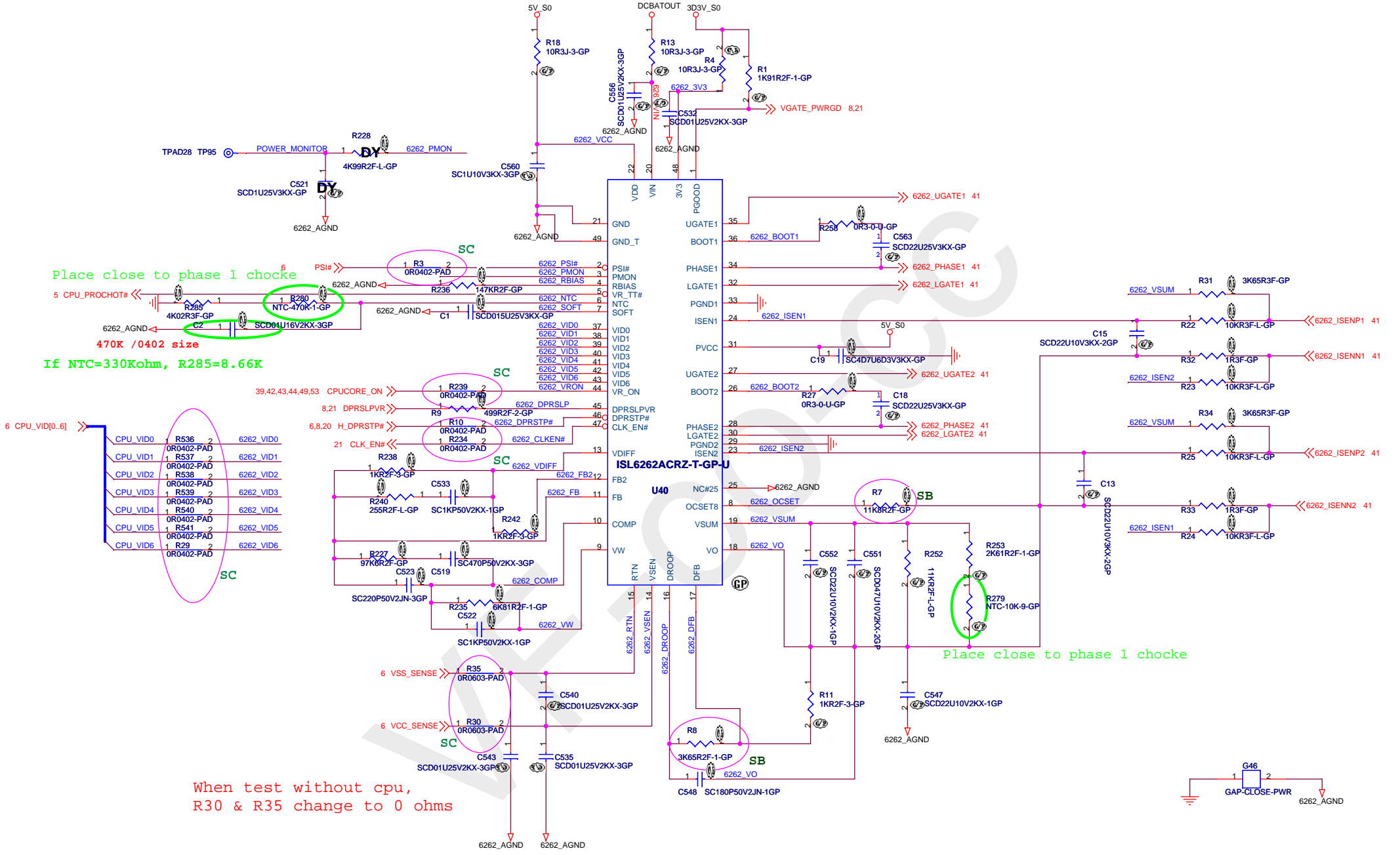
<Core Design>

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 Taipei Hsien 221, Taiwan, R.O.C.

Title: **DC to DC 3.3V & 5V**

Size: Custom Document Number
 Date: Sunday, September 09, 2007 Sheet 39 of 57

Rev: **-1**



Place close to phase 1 choke
 5 CPU_PROCHOT# <<<
 470K / 0402 size
 If NTC=330Kohm, R285=8.66K

Place close to phase 1 choke

When test without cpu,
 R30 & R35 change to 0 ohms

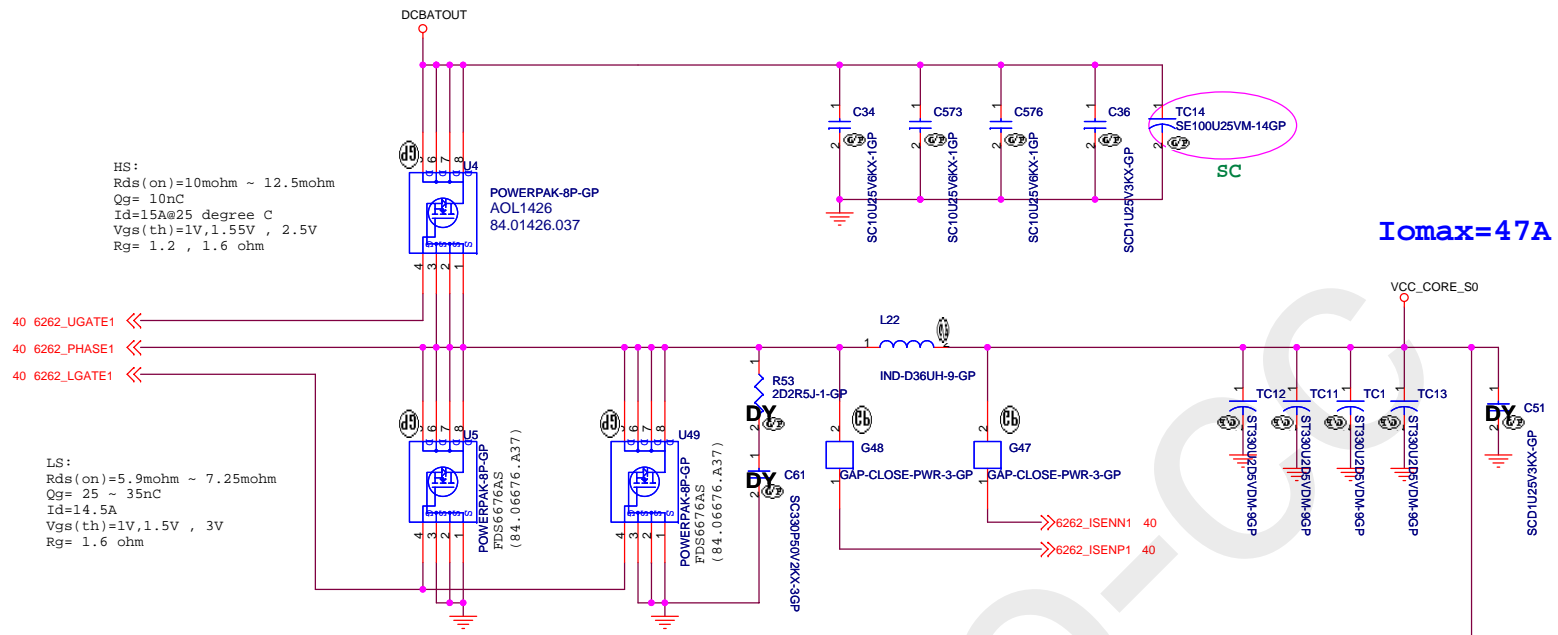
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緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **DC-DC VCCCPUCORE 1/2**

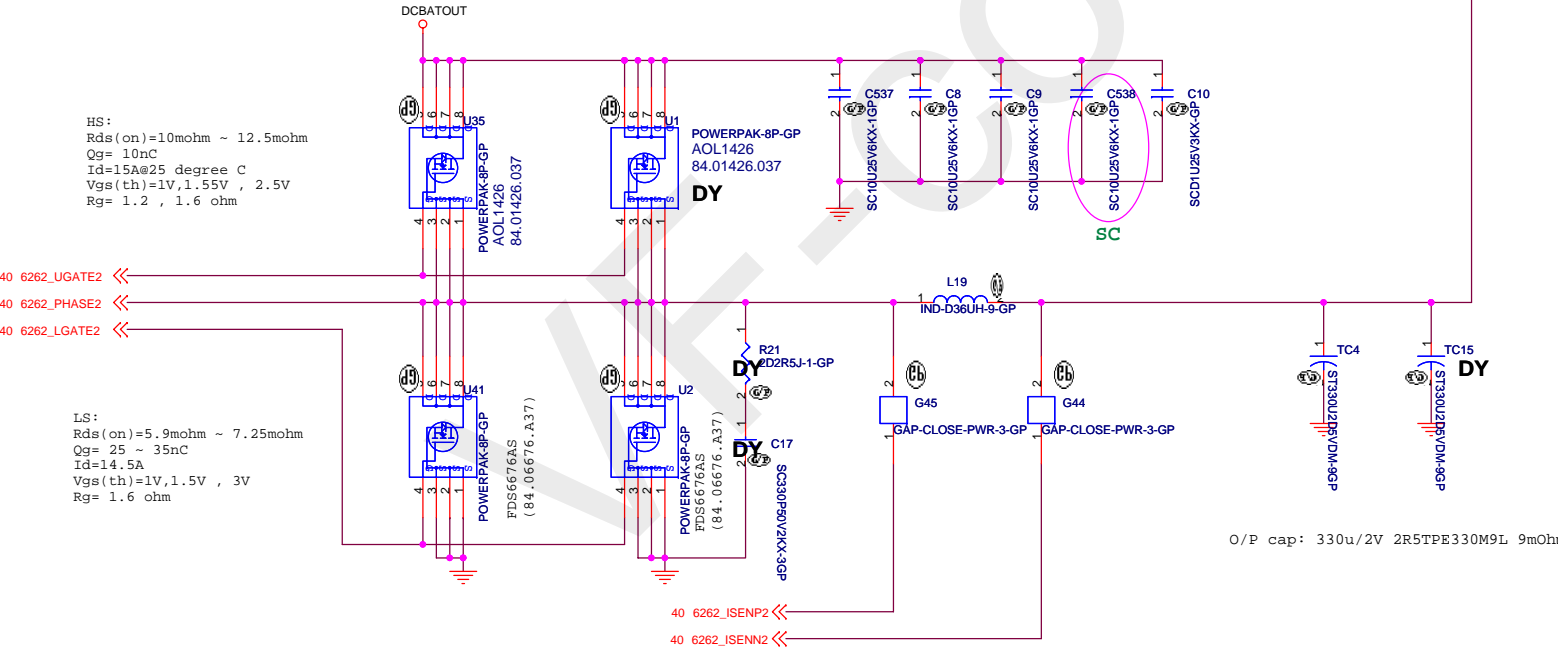
Size A3	Document Number	Rev -1
Date: Sunday, September 09, 2007		Sheet 40 of 57

Hawke-Intel



HS:
 $R_{ds(on)} = 10\text{m}\Omega \sim 12.5\text{m}\Omega$
 $Q_g = 10\text{nC}$
 $I_d = 15\text{A}@25^\circ\text{C}$
 $V_{gs(th)} = 1\text{V}, 1.55\text{V}, 2.5\text{V}$
 $R_g = 1.2, 1.6\ \Omega$

LS:
 $R_{ds(on)} = 5.9\text{m}\Omega \sim 7.25\text{m}\Omega$
 $Q_g = 25 \sim 35\text{nC}$
 $I_d = 14.5\text{A}$
 $V_{gs(th)} = 1\text{V}, 1.5\text{V}, 3\text{V}$
 $R_g = 1.6\ \Omega$



HS:
 $R_{ds(on)} = 10\text{m}\Omega \sim 12.5\text{m}\Omega$
 $Q_g = 10\text{nC}$
 $I_d = 15\text{A}@25^\circ\text{C}$
 $V_{gs(th)} = 1\text{V}, 1.55\text{V}, 2.5\text{V}$
 $R_g = 1.2, 1.6\ \Omega$

LS:
 $R_{ds(on)} = 5.9\text{m}\Omega \sim 7.25\text{m}\Omega$
 $Q_g = 25 \sim 35\text{nC}$
 $I_d = 14.5\text{A}$
 $V_{gs(th)} = 1\text{V}, 1.5\text{V}, 3\text{V}$
 $R_g = 1.6\ \Omega$

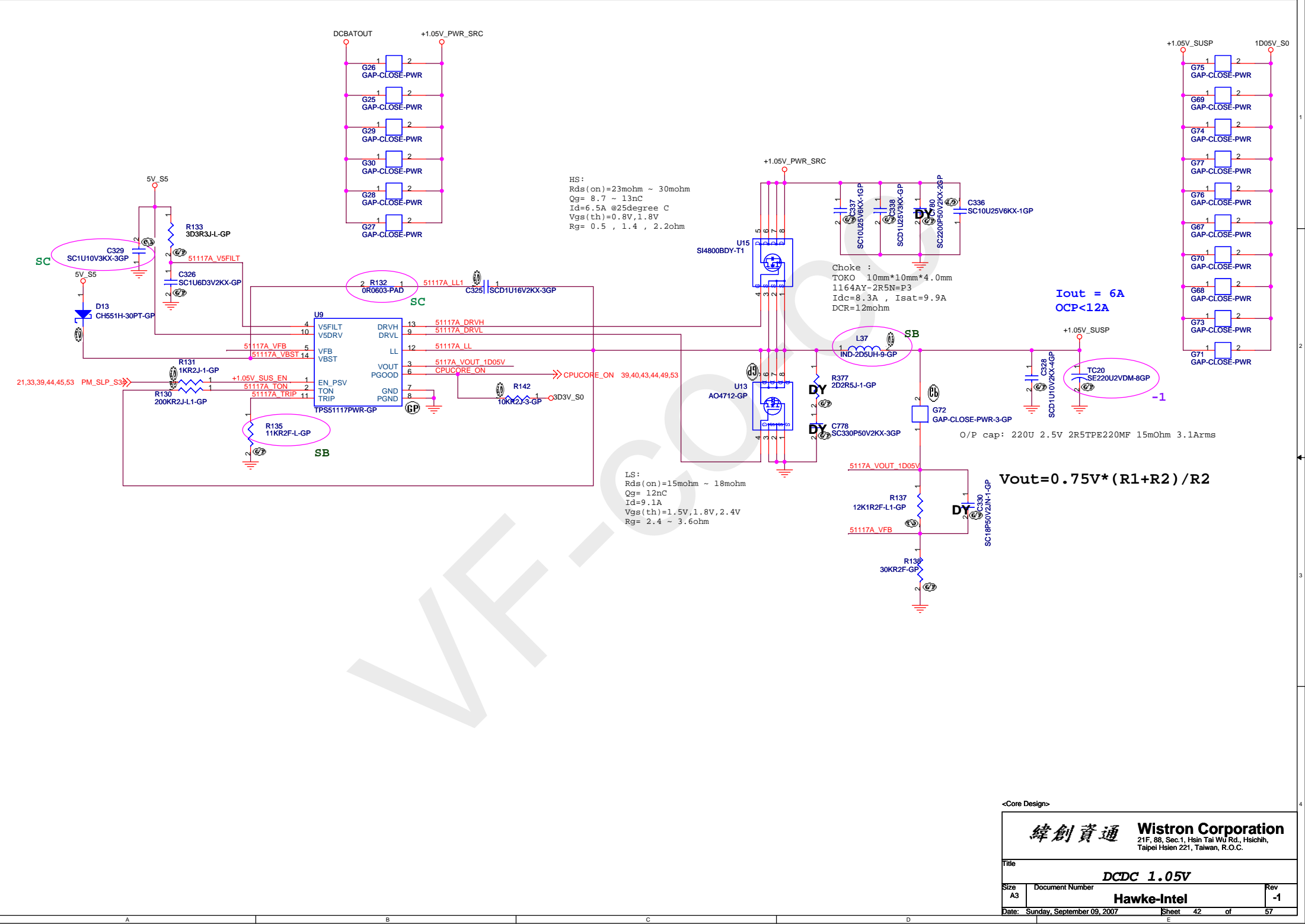
If VCC_SENSE and VSS_SENSE pins have pulled resistors to VCC_CORE_S0
 ==> Remove R44/R45/R46/R47.

<Core Design>

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Title: **DC-DC VCCCPUCORE 2/2**

Size A3	Document Number	Rev -1
Date: Thursday, September 20, 2007		Sheet 41 of 57



HS:
 Rds(on)=23mohm ~ 30mohm
 Qg= 8.7 ~ 13nC
 Id=6.5A @25degree C
 Vgs(th)=0.8V, 1.8V
 Rg= 0.5 , 1.4 , 2.2ohm

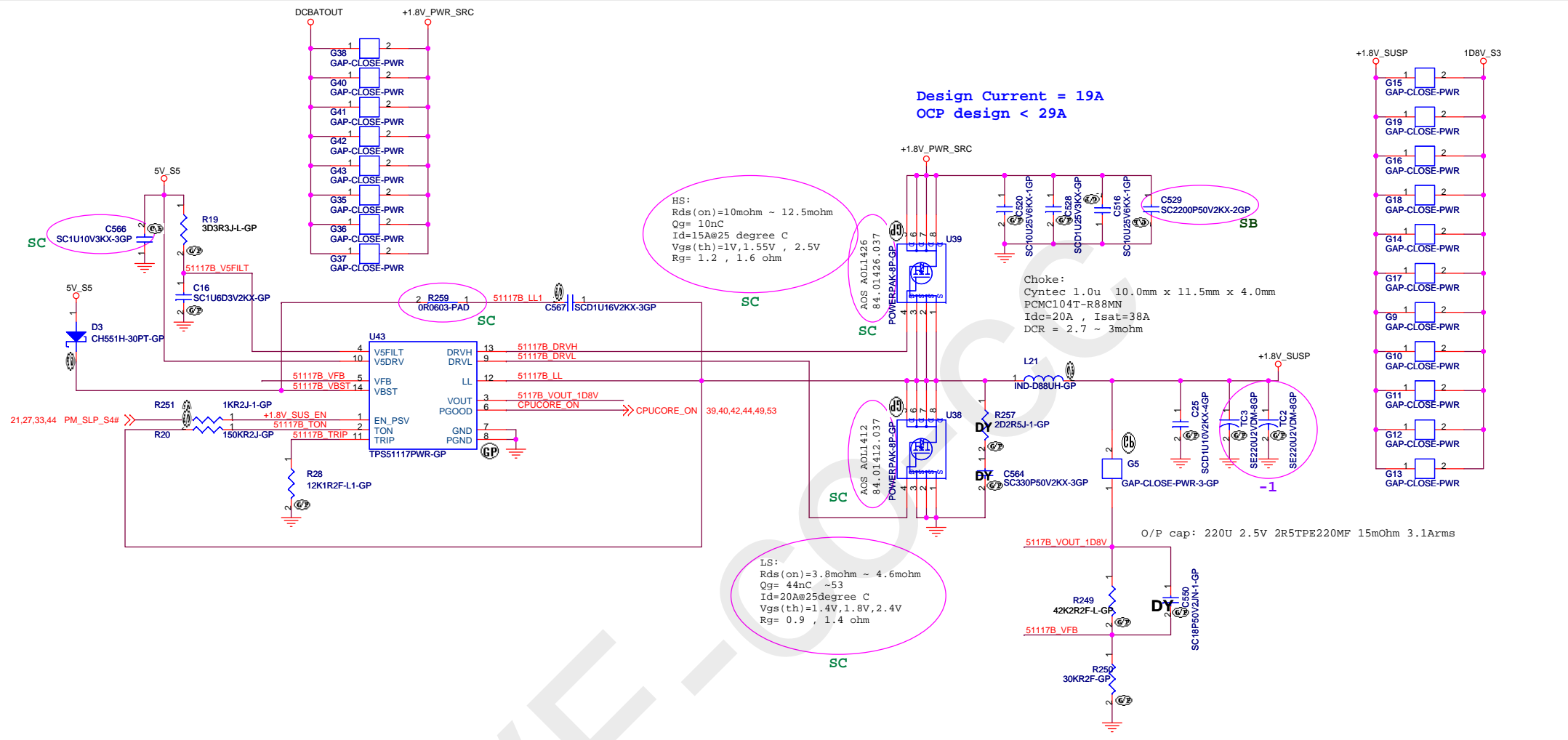
Choke :
 TOKO 10mm*10mm*4.0mm
 1164AY-2R5N=P3
 Idc=8.3A , Isat=9.9A
 DCR=12mohm

LS:
 Rds(on)=15mohm ~ 18mohm
 Qg= 12nC
 Id=9.1A
 Vgs(th)=1.5V, 1.8V, 2.4V
 Rg= 2.4 ~ 3.6ohm

$$V_{out} = 0.75V * (R1 + R2) / R2$$

Iout = 6A
 OCP < 1.2A

O/P cap: 220U 2.5V 2R5TPE220MF 15mOhm 3.1Arms



Design Current = 19A
 OCP design < 29A

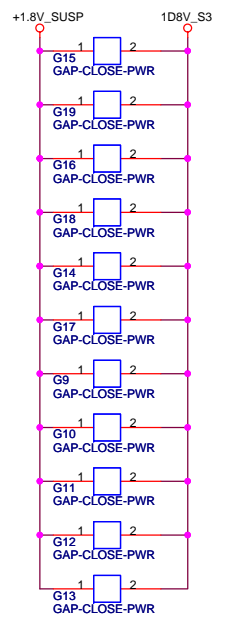
HS:
 Rds(on)=10mohm ~ 12.5mohm
 Qg= 10nC
 Id=15A@25 degree C
 Vgs(th)=1V, 1.55V , 2.5V
 Rg= 1.2 , 1.6 ohm

Choke:
 Cyttec 1.0u 10.0mm x 11.5mm x 4.0mm
 PCMC104T-R88MN
 Idc=20A , Isat=38A
 DCR = 2.7 ~ 3mohm

LS:
 Rds(on)=3.8mohm ~ 4.6mohm
 Qg= 44nC ~53
 Id=20A@25degree C
 Vgs(th)=1.4V, 1.8V, 2.4V
 Rg= 0.9 , 1.4 ohm

O/P cap: 220U 2.5V 2R5TPE220MF 15mOhm 3.1Arms

$$V_{out} = 0.75V * (R1 + R2) / R2$$

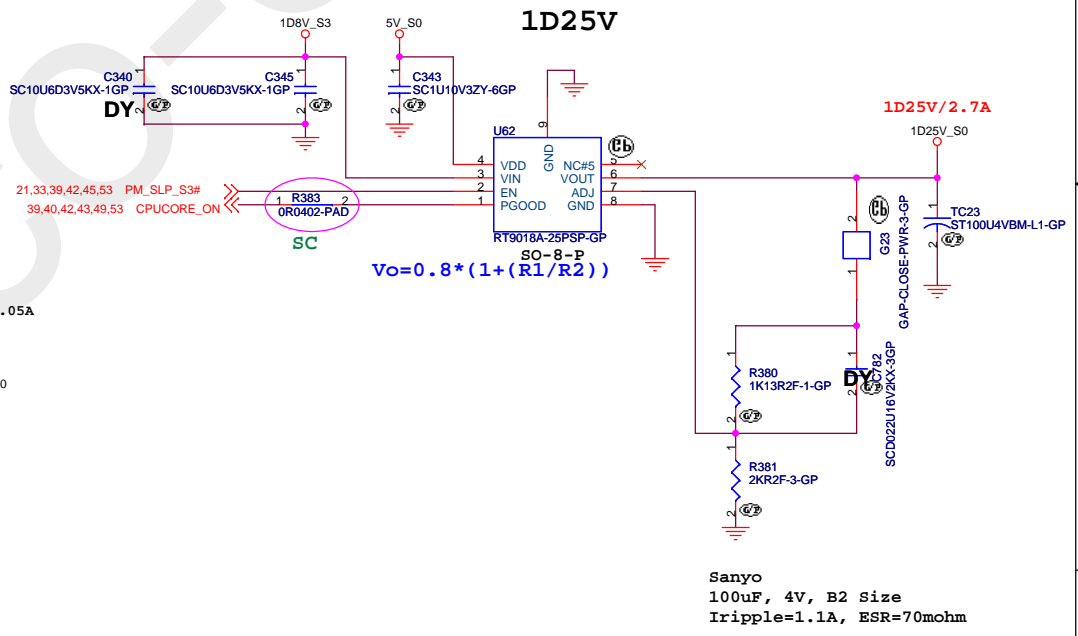
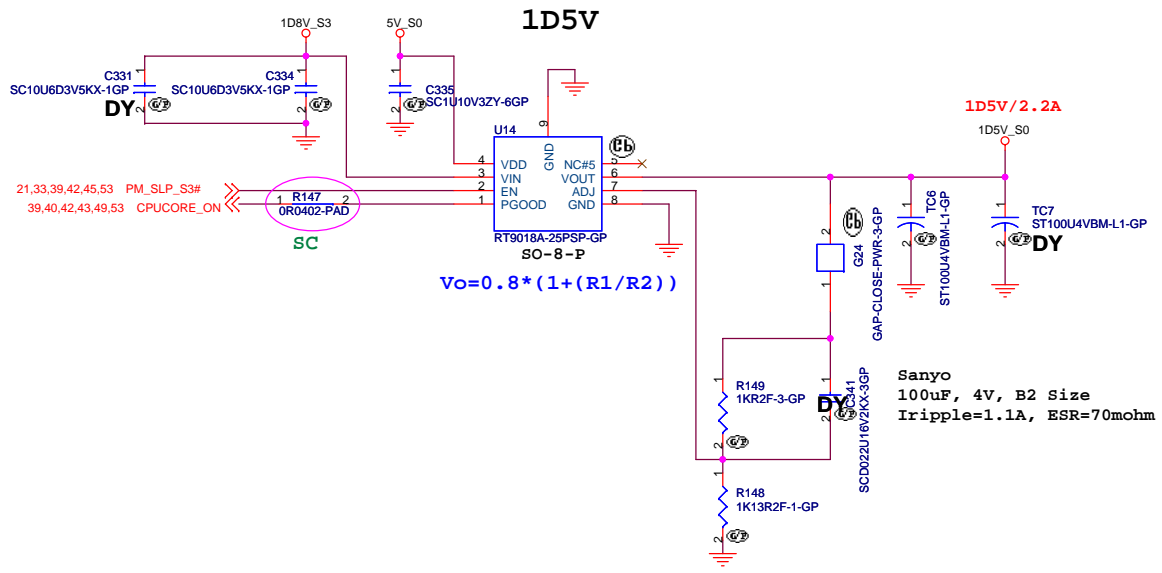


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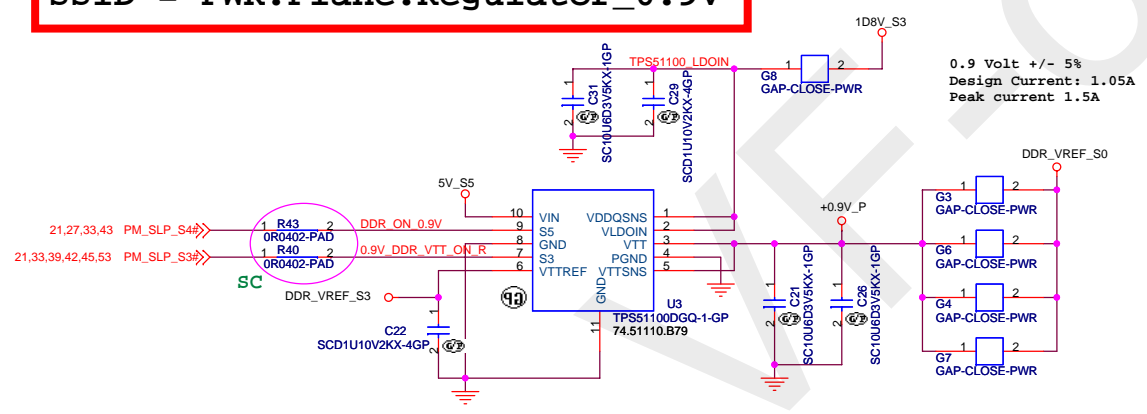
緯創資通 Wistron Corporation
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 Taipei Hsien 221, Taiwan, R.O.C.

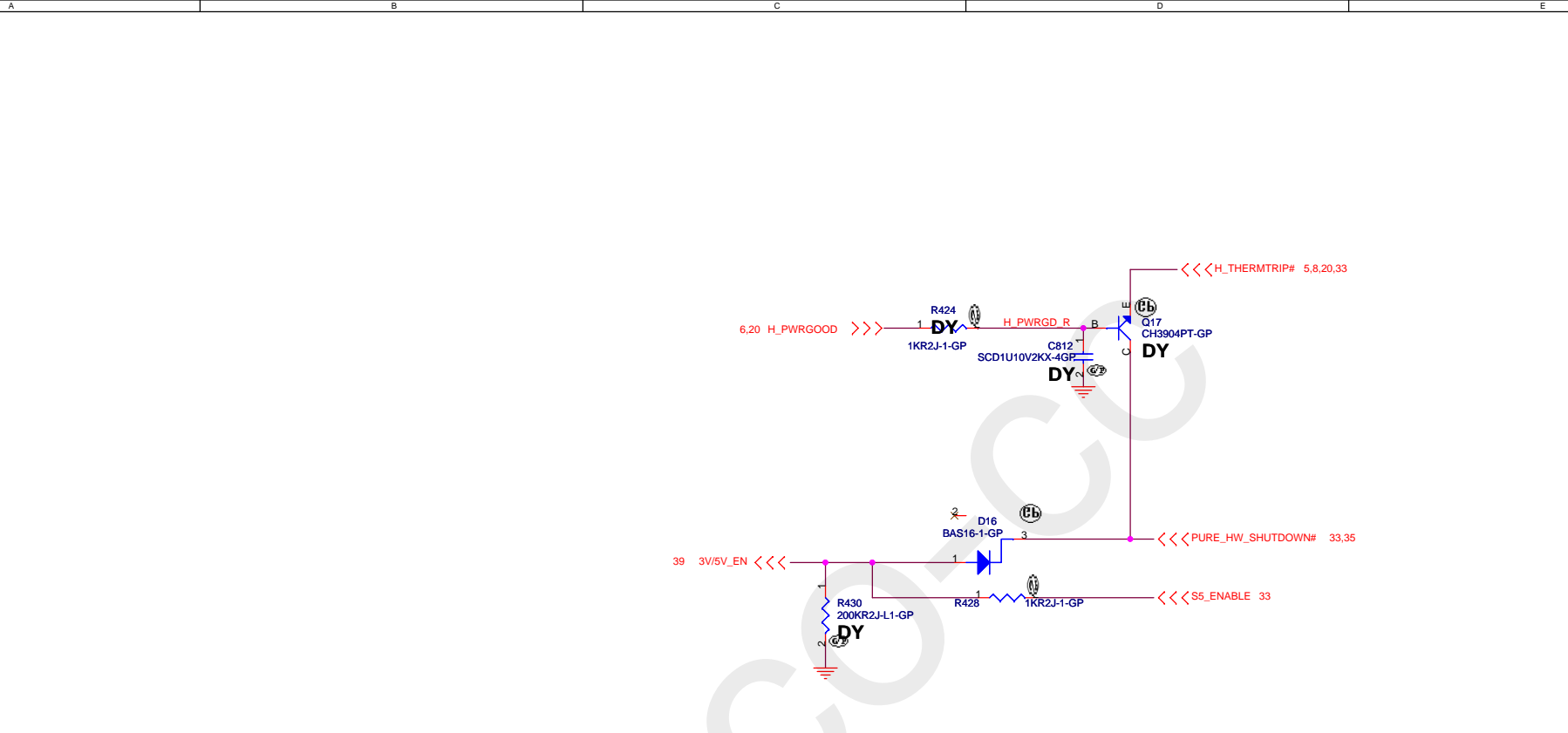
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Size A3	Document Number	Rev
	Hawke-Intel	-1
Date: Sunday, September 09, 2007	Sheet 43 of	57

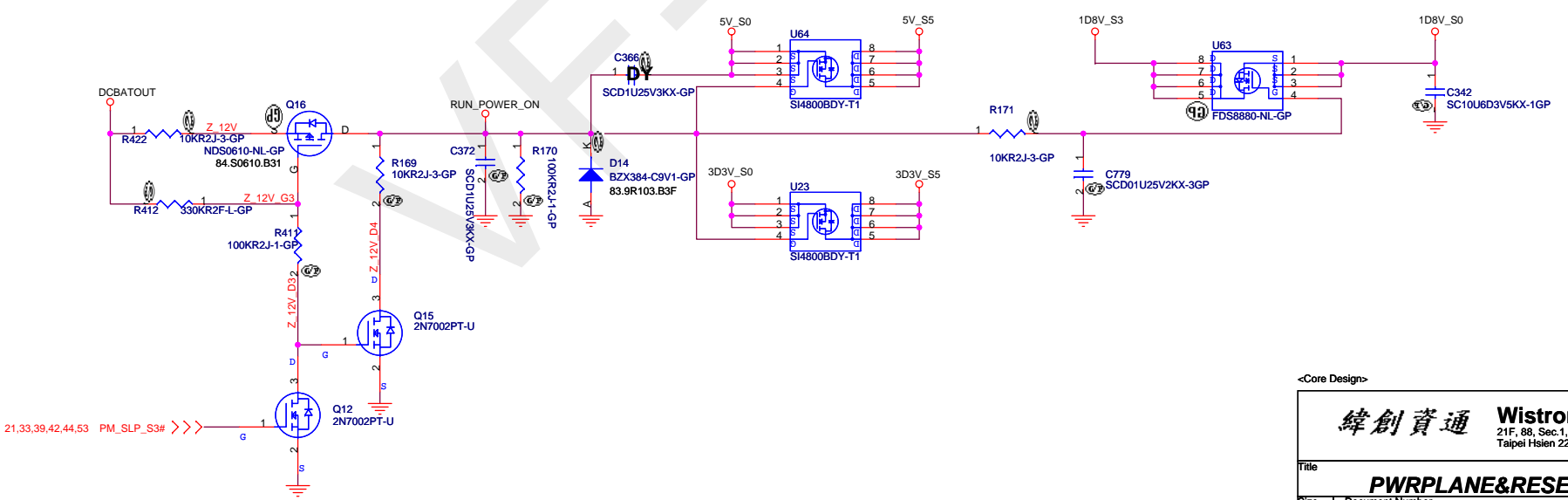


SSID = PWR.Plane.Regulator_0.9V





Run Power



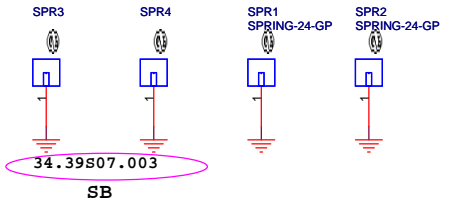
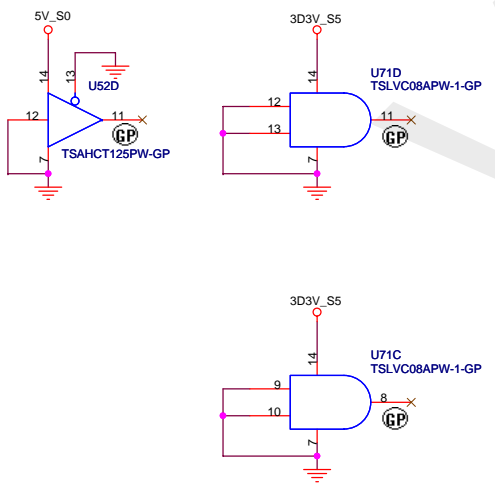
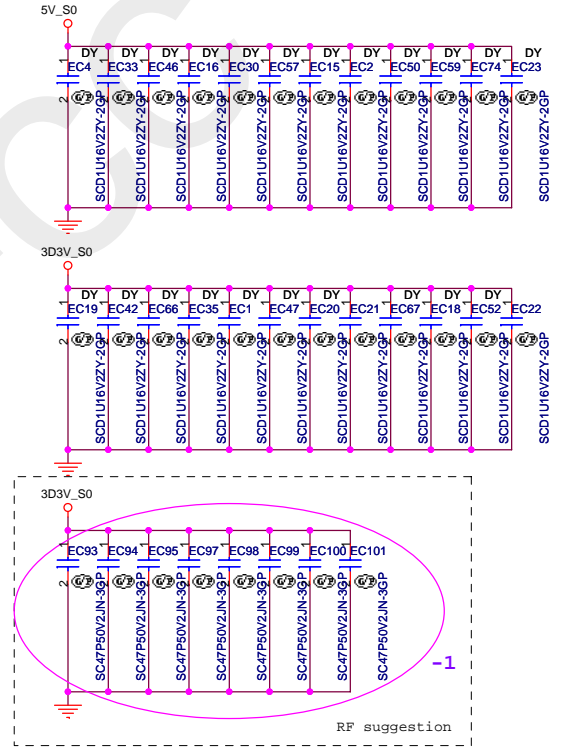
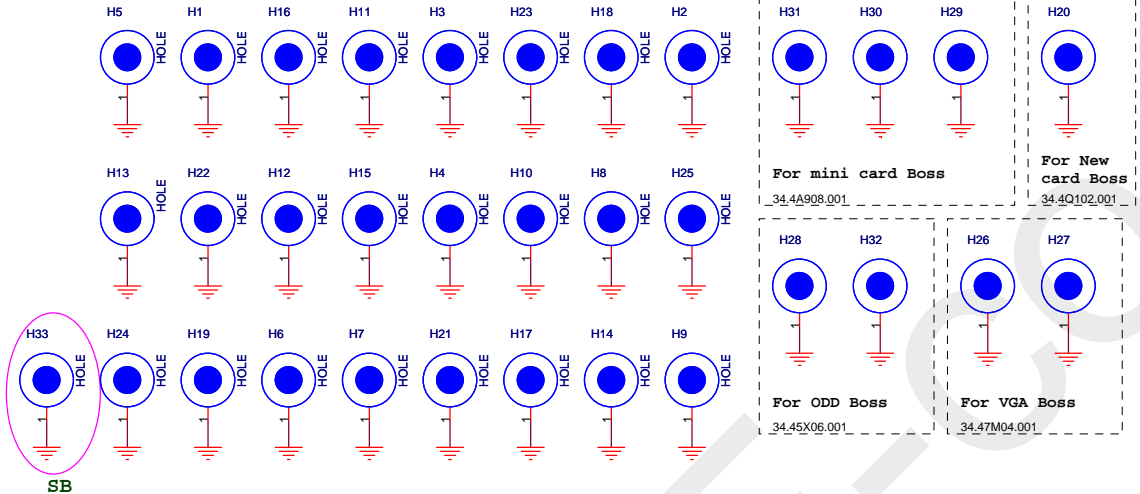
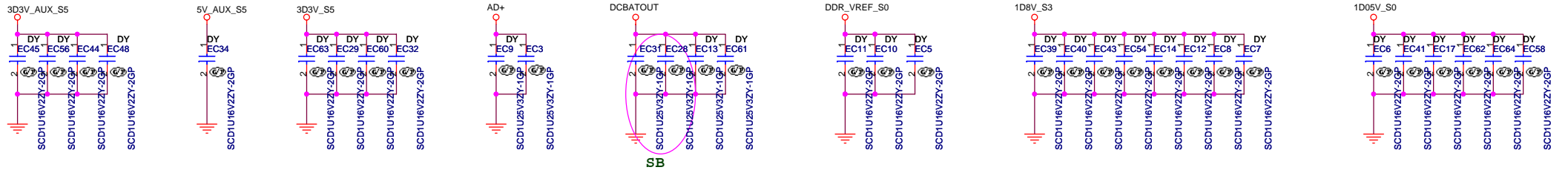
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Title: **PWRPLANE&RESETLOGIC**

Size A3	Document Number	Rev
	Hawke-Intel	-1

Date: Sunday, September 09, 2007 Sheet 45 of 57



PCIE_MRX_GTX_N0_15] >>> PCIE_MRX_GTX_N0_15] 10
 PCIE_MRX_GTX_P0_15] >>> PCIE_MRX_GTX_P0_15] 10
 PCIE_MTX_GRX_N0_15] <<< PCIE_MTX_GRX_N0_15] 10
 PCIE_MTX_GRX_P0_15] <<< PCIE_MTX_GRX_P0_15] 10

8.19.23.27.28.29.33 PLT_RST1# >>> PLT_RST1# AH15

R326 200R2F-L-GP PEX_TEST_PLL_CLK_OUT# AM12
 R326 200R2F-L-GP PEX_TEST_PLL_CLK_OUT# AM11

PCIE_MRX_GTX_P0_C174 4 CLK_PCIE_VGA# AH14
 PCIE_MRX_GTX_N0_C168 4 CLK_PCIE_VGA# AH14
 SCD1U10V2KX-4GP PCIE_MRX_GTX_P0_A315
 SCD1U10V2KX-4GP PCIE_MRX_GTX_N0_A315

PCIE_MRX_GTX_P1_C655 1 SCD1U10V2KX-4GP PCIE_MRX_GTX_P0_A315
 PCIE_MRX_GTX_N1_C658 1 SCD1U10V2KX-4GP PCIE_MRX_GTX_N0_A315

PCIE_MRX_GTX_P2_C665 1 SCD1U10V2KX-4GP PCIE_MRX_GTX_P0_A315
 PCIE_MRX_GTX_N2_C663 1 SCD1U10V2KX-4GP PCIE_MRX_GTX_N0_A315

PCIE_MRX_GTX_P3_C670 1 SCD1U10V2KX-4GP PCIE_MRX_GTX_P0_A315
 PCIE_MRX_GTX_N3_C676 1 SCD1U10V2KX-4GP PCIE_MRX_GTX_N0_A315

PCIE_MRX_GTX_P4_C200 1 SCD1U10V2KX-4GP PCIE_MRX_GTX_P0_A315
 PCIE_MRX_GTX_N4_C205 1 SCD1U10V2KX-4GP PCIE_MRX_GTX_N0_A315

PCIE_MRX_GTX_P5_C682 1 SCD1U10V2KX-4GP PCIE_MRX_GTX_P0_A315
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PCIE_MRX_GTX_P6_C687 1 SCD1U10V2KX-4GP PCIE_MRX_GTX_P0_A315
 PCIE_MRX_GTX_N6_C685 1 SCD1U10V2KX-4GP PCIE_MRX_GTX_N0_A315

PCIE_MRX_GTX_P7_C698 1 SCD1U10V2KX-4GP PCIE_MRX_GTX_P0_A315
 PCIE_MRX_GTX_N7_C695 1 SCD1U10V2KX-4GP PCIE_MRX_GTX_N0_A315

PCIE_MRX_GTX_P8_C216 1 SCD1U10V2KX-4GP PCIE_MRX_GTX_P0_A315
 PCIE_MRX_GTX_N8_C224 1 SCD1U10V2KX-4GP PCIE_MRX_GTX_N0_A315

PCIE_MRX_GTX_P9_C705 1 SCD1U10V2KX-4GP PCIE_MRX_GTX_P0_A315
 PCIE_MRX_GTX_N9_C709 1 SCD1U10V2KX-4GP PCIE_MRX_GTX_N0_A315

PCIE_MRX_GTX_P10_C250 1 SCD1U10V2KX-4GP PCIE_MRX_GTX_P0_A315
 PCIE_MRX_GTX_N10_C232 1 SCD1U10V2KX-4GP PCIE_MRX_GTX_N0_A315

PCIE_MRX_GTX_P11_C258 1 SCD1U10V2KX-4GP PCIE_MRX_GTX_P0_A315
 PCIE_MRX_GTX_N11_C225 1 SCD1U10V2KX-4GP PCIE_MRX_GTX_N0_A315

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PCIE_MRX_GTX_P15_C281 1 SCD1U10V2KX-4GP PCIE_MRX_GTX_P0_A315
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U55A

1 OF 14

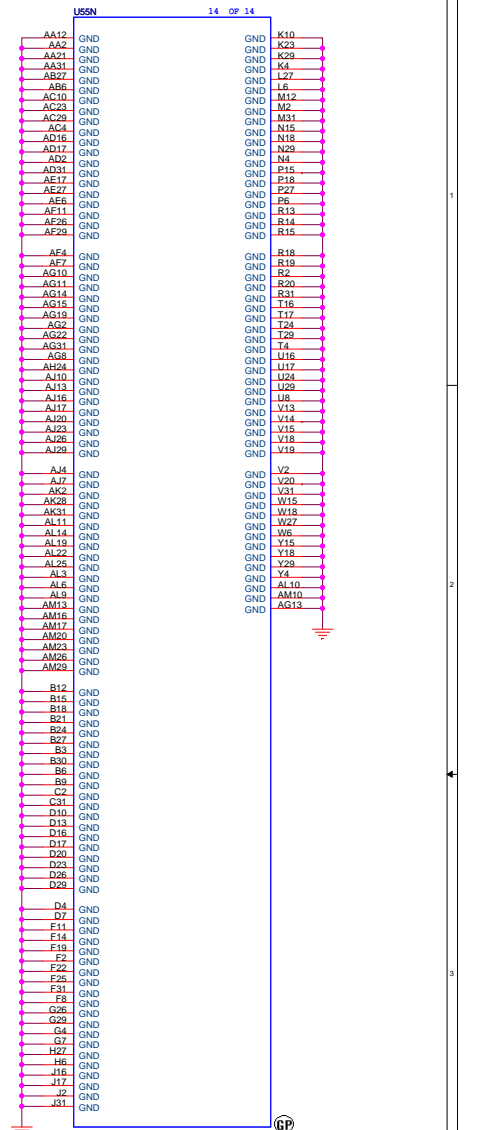
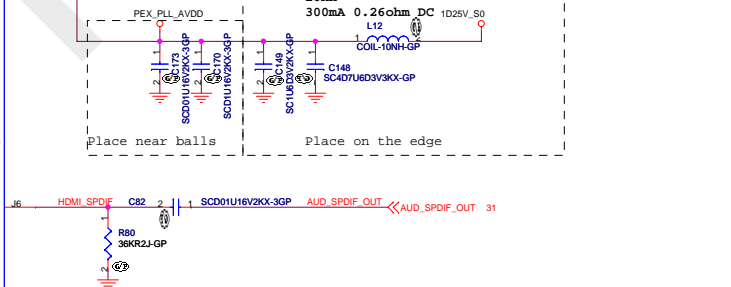
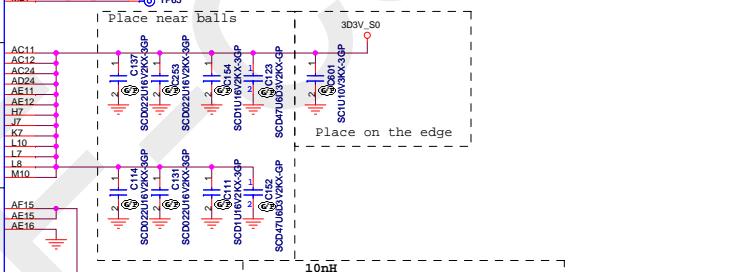
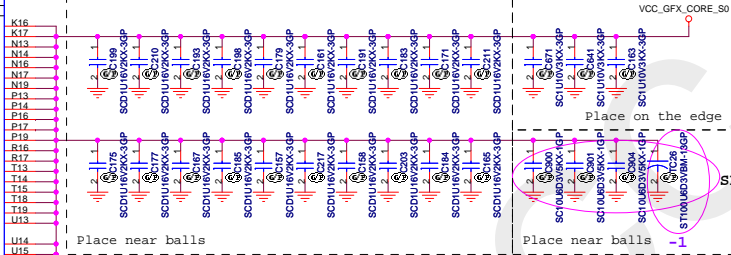
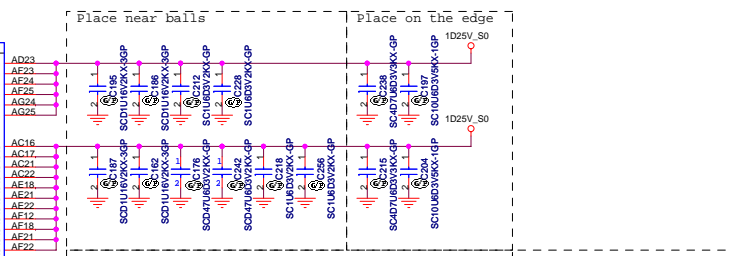
PEX_IOVDD/Q 1.5A

PEX_IOVDD/Q 1.5A

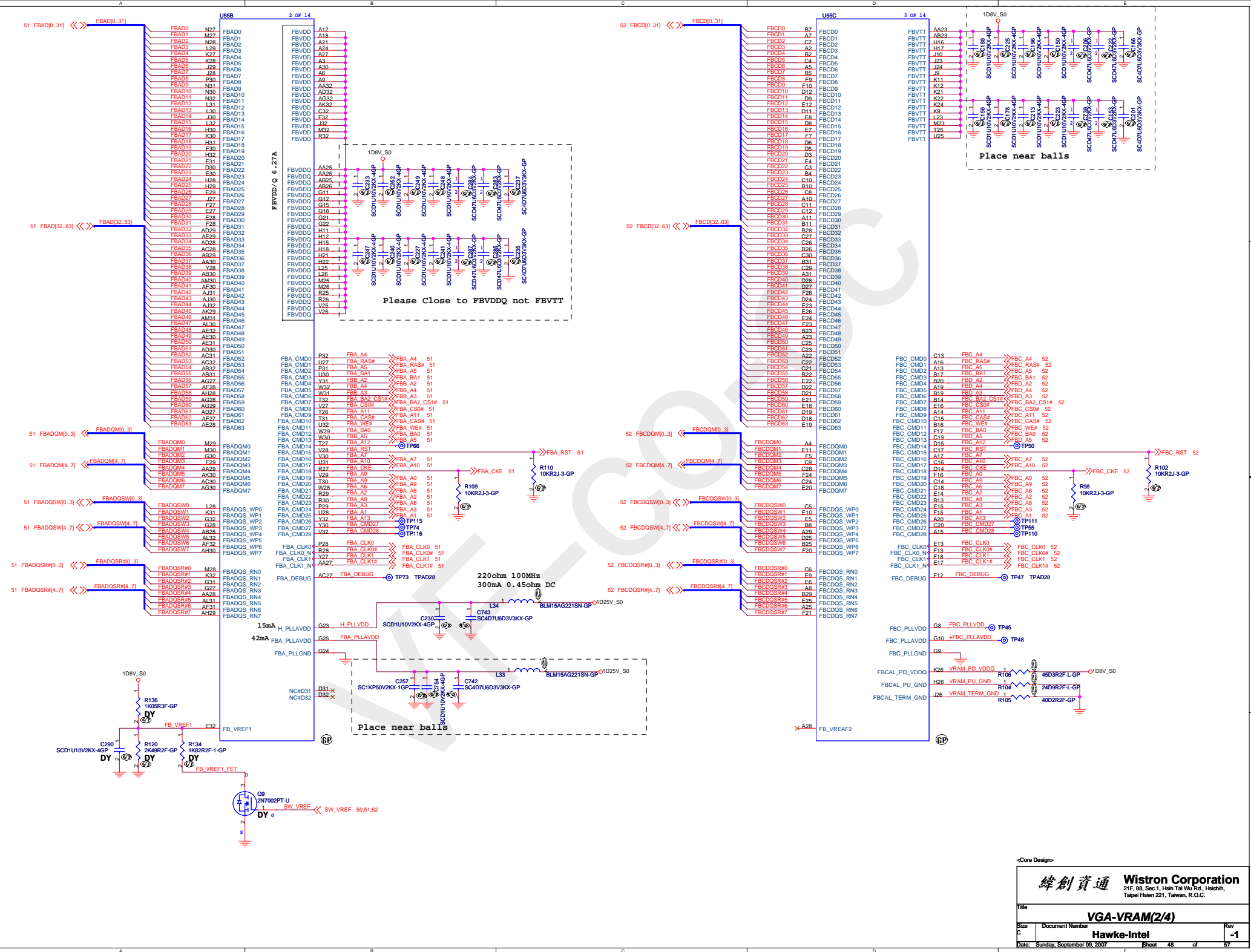
VDD33 0.11A

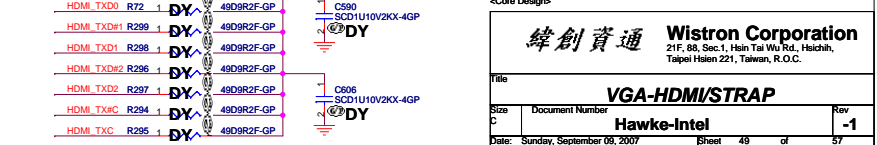
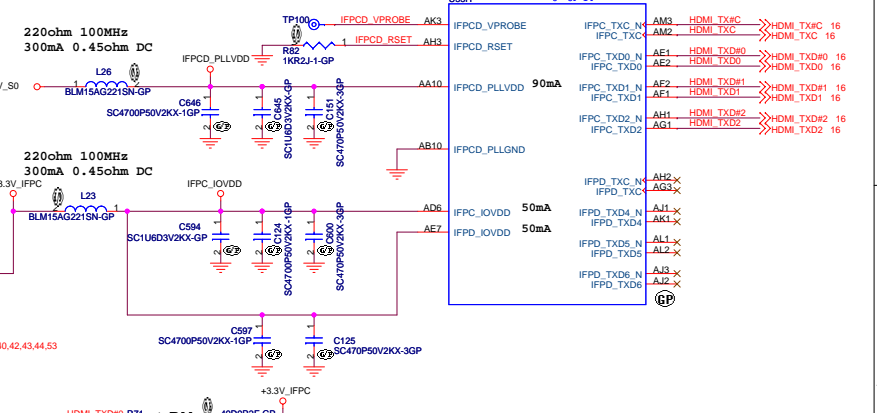
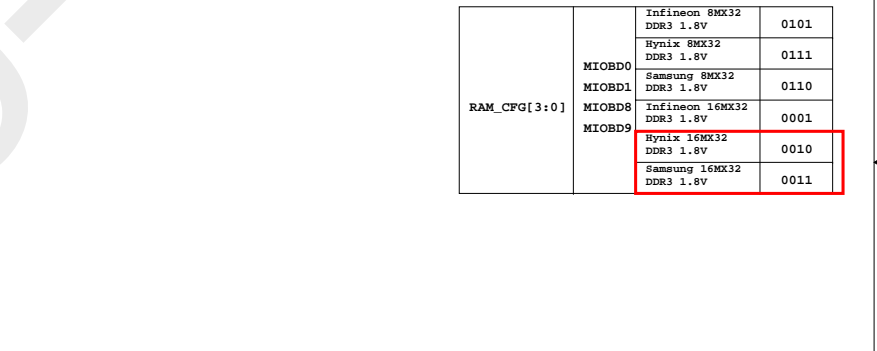
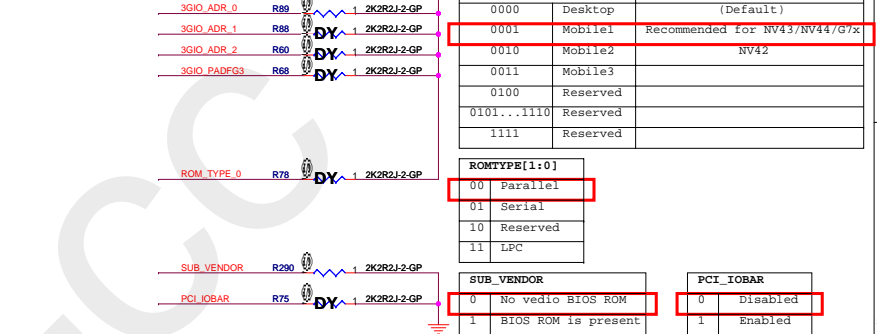
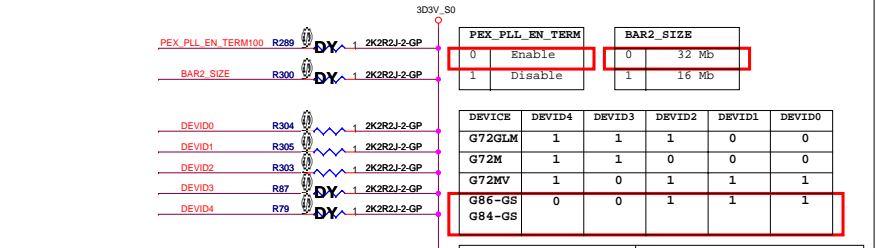
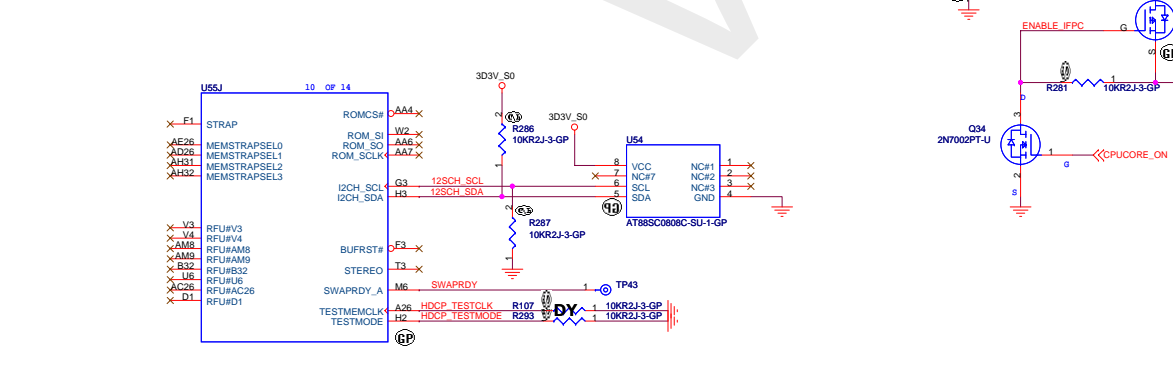
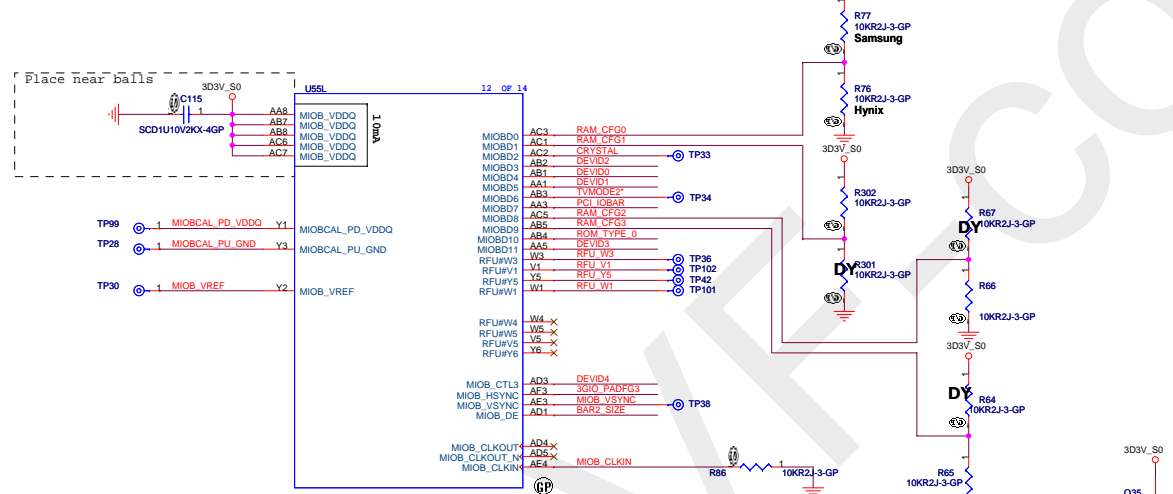
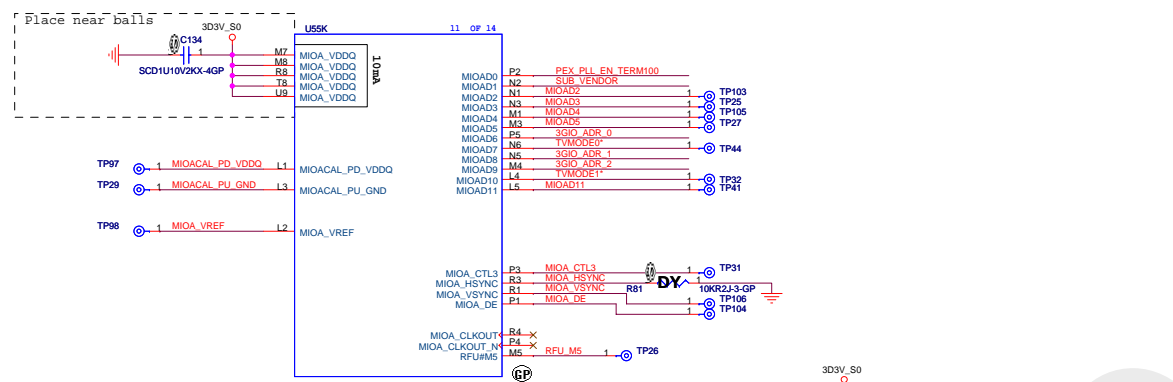
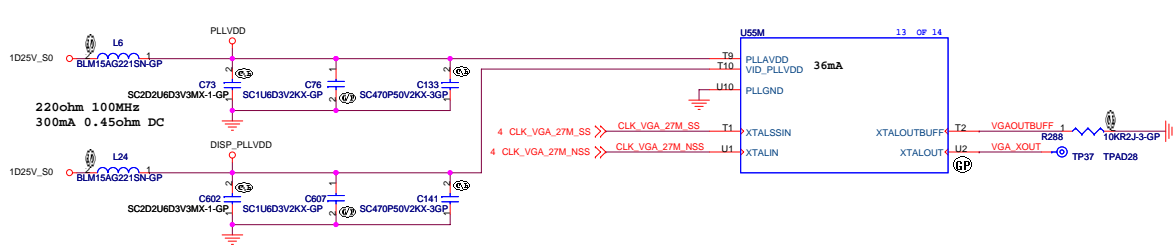
0.11A

PEX_PLLAVDD
 PEX_PLLDVDD
 PEX_PLLGND



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PEX_PLL_EN_TERM		BAR2_SIZE	
0	Enable	0	32 Mb
1	Disable	1	16 Mb

DEVID0	DEVID4	DEVID3	DEVID2	DEVID1	DEVID0
G72GLM	1	1	1	0	0
G72M	1	1	0	0	0
G72MV	1	0	1	1	1
G86-GS	0	0	1	1	1
G84-GS					

3GIO_PADCFG[3:0]		Notes
0000	Desktop	(Default)
0001	Mobile1	Recommended for NV43/NV44/G7X
0010	Mobile2	NV42
0011	Mobile3	
0100	Reserved	
0101...1110	Reserved	
1111	Reserved	

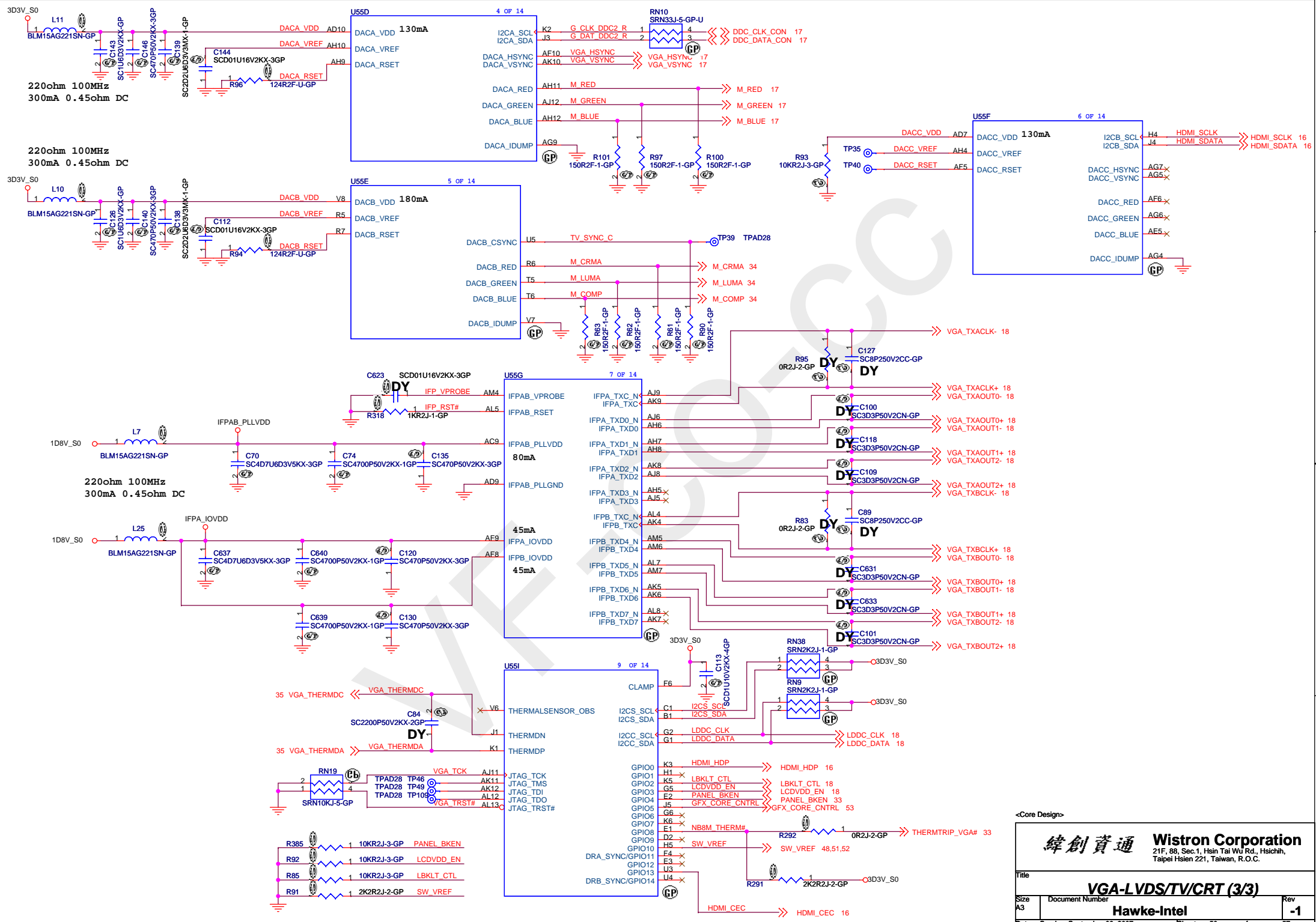
ROMTYPE[1:0]	
00	Parallel
01	Serial
10	Reserved
11	LPC

SUB_VENDOR		PCI_IOBAR	
0	No video BIOS ROM	0	Disabled
1	BIOS ROM is present	1	Enabled

RAM_CFG[3:0]		
MIOBD0	Infineon 8MX32 DDR3 1.8V	0101
MIOBD1	Hynix 8MX32 DDR3 1.8V	0111
MIOBD8	Samsung 8MX32 DDR3 1.8V	0110
MIOBD9	Infineon 16MX32 DDR3 1.8V	0001
	Hynix 16MX32 DDR3 1.8V	0010
	Samsung 16MX32 DDR3 1.8V	0011

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Core Design:
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VGA-HDMI/STRAP
Hawke-Intel
 Date: Sunday, September 06, 2007 Sheet 49 of 57

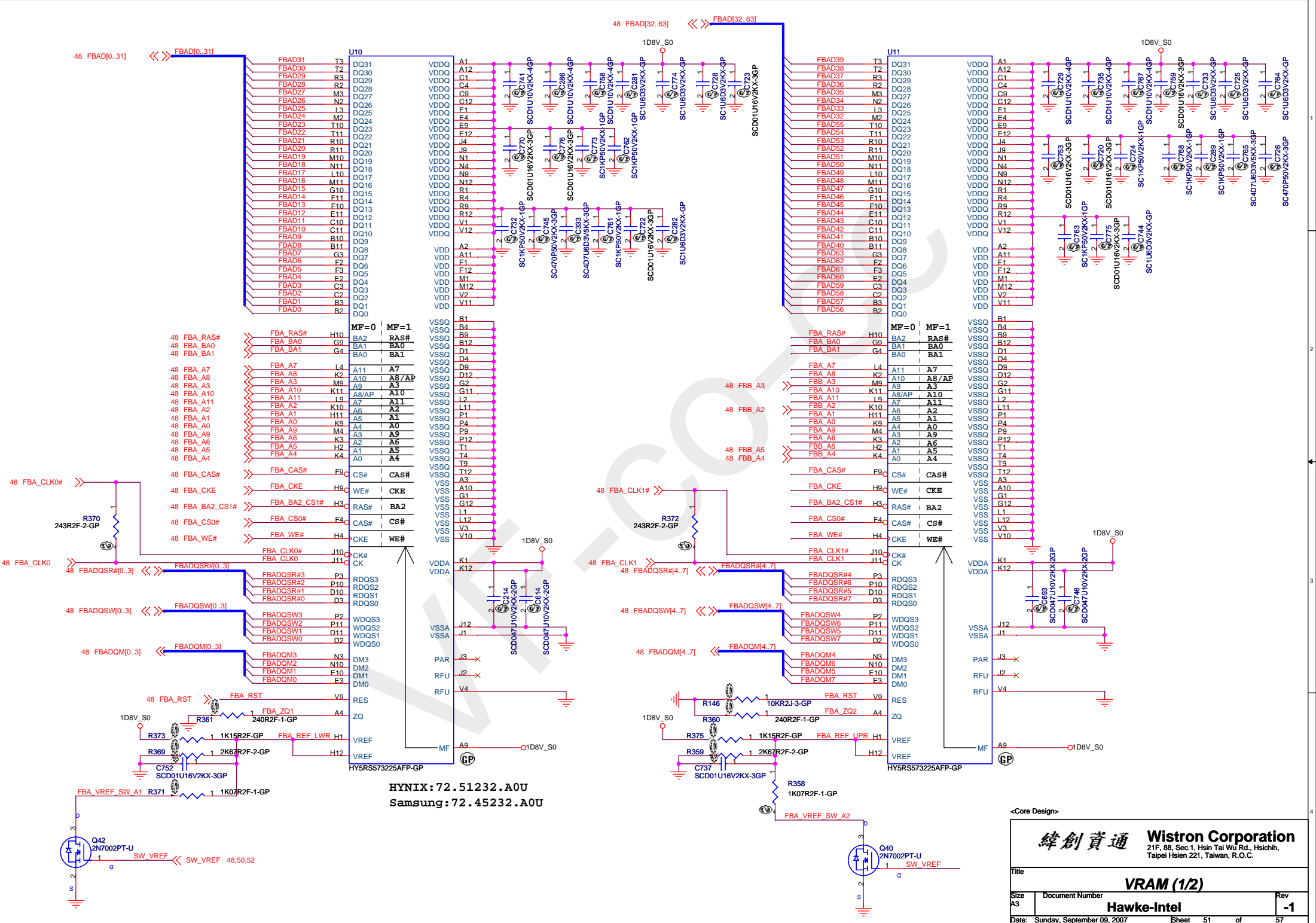


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File: **VGA-LVDS/TV/CRT (3/3)**

Size A3 Document Number **Hawke-Intel** Rev **-1**

Date: Sunday, September 09, 2007 Sheet 50 of 57



HYNIX: 72.51232.A0U
 Samsung: 72.45232.A0U

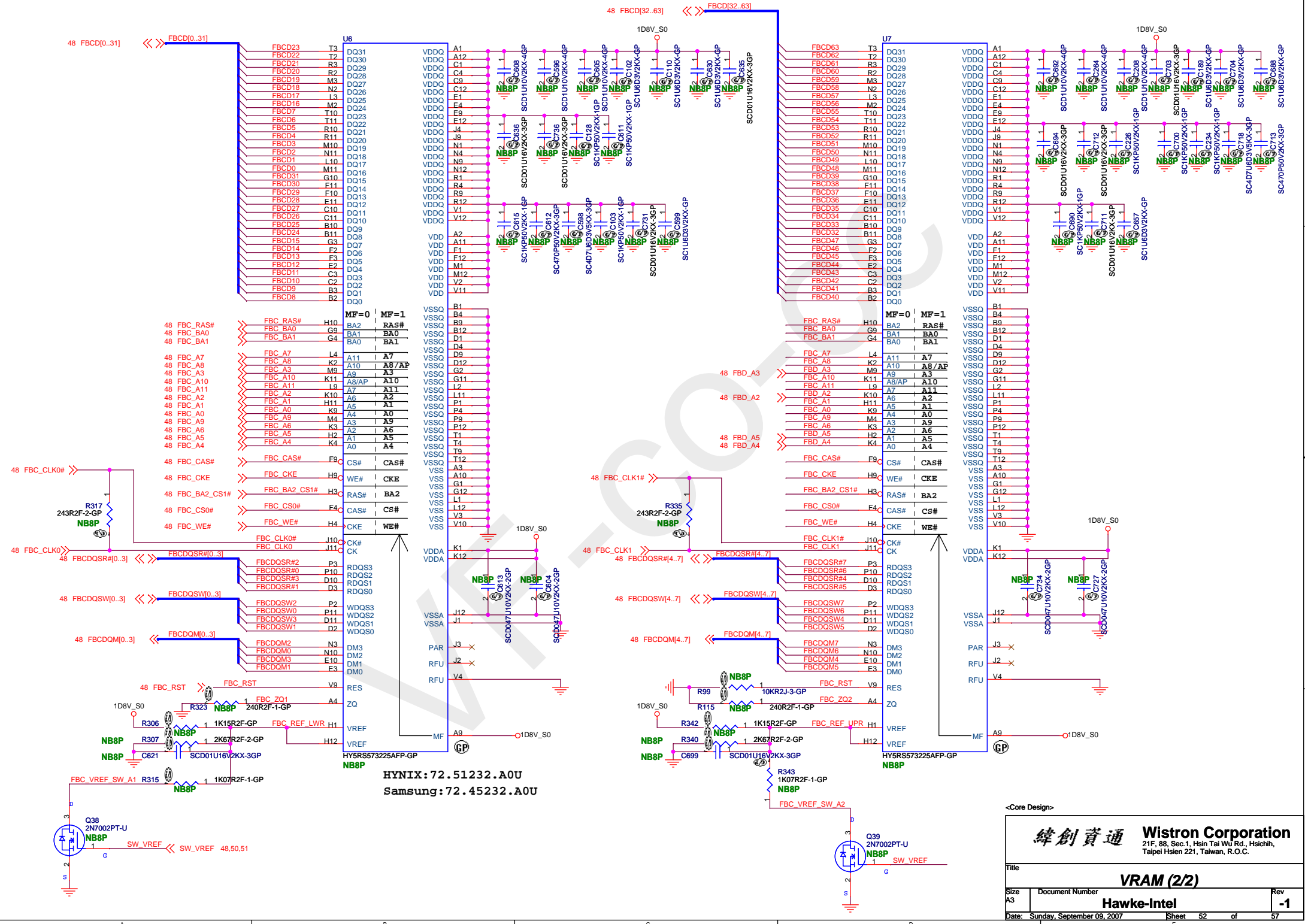
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Title: **VRAM (1/2)**

Size A3	Document Number	Rev
	Hawke-Intel	-1

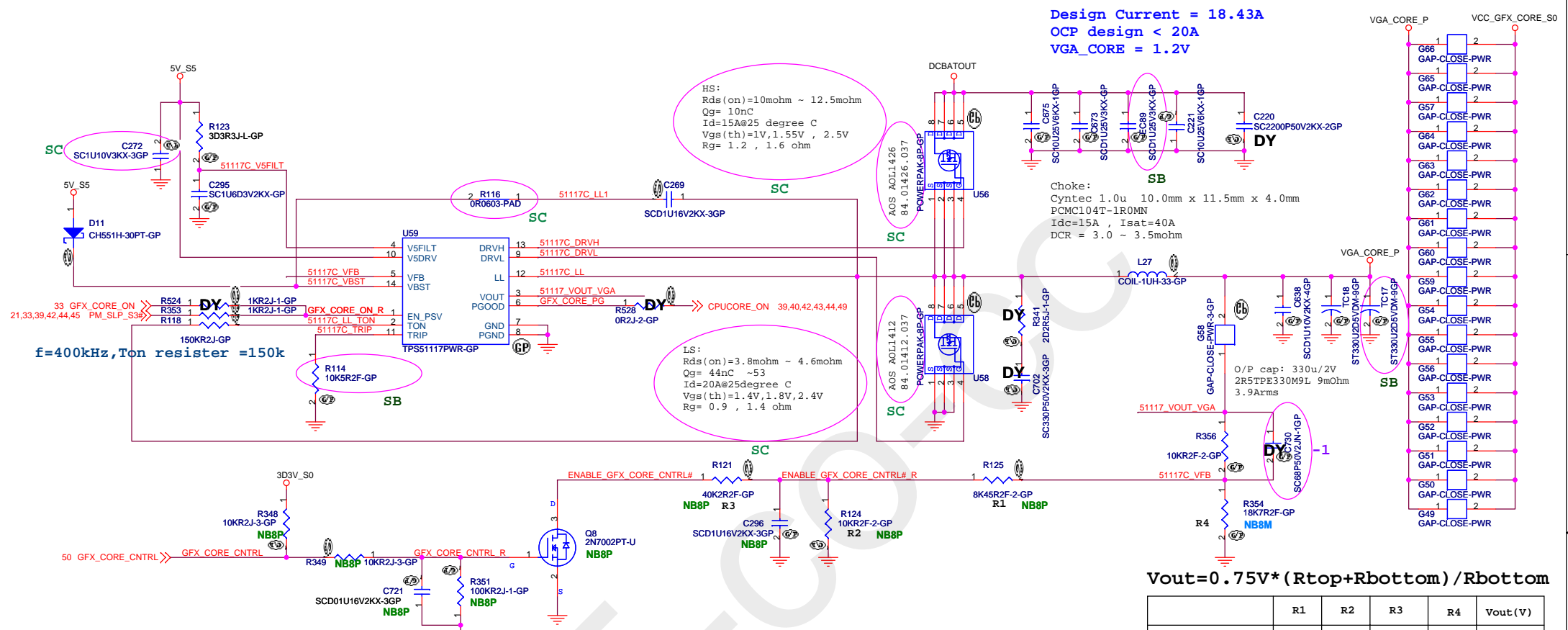
Date: Sunday, September 09, 2007 51 of 57



<Core Design>

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VRAM (2/2)		
Title	Document Number	Rev
	Hawke-Intel	-1
Date: Sunday, September 09, 2007		
Sheet	52	of
		57



HS:
 Rds(on)=10mohm ~ 12.5mohm
 Qg= 10nC
 Id=15A@25 degree C
 Vgs(th)=1V,1.55V , 2.5V
 Rg= 1.2 , 1.6 ohm

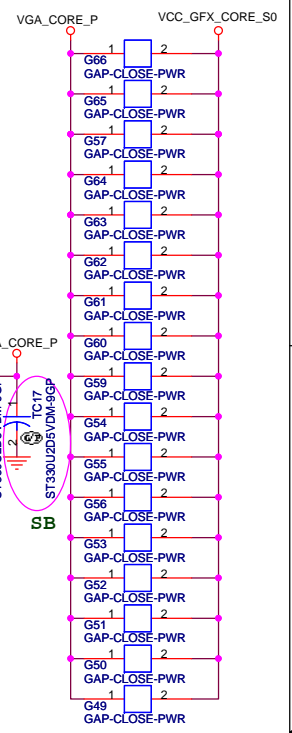
LS:
 Rds(on)=3.8mohm ~ 4.6mohm
 Qg= 44nC ~53
 Id=20A@25degree C
 Vgs(th)=1.4V,1.8V,2.4V
 Rg= 0.9 , 1.4 ohm

Design Current = 18.43A
 OCP design < 20A
 VGA_CORE = 1.2V

f=400kHz, Ton resistor =150k

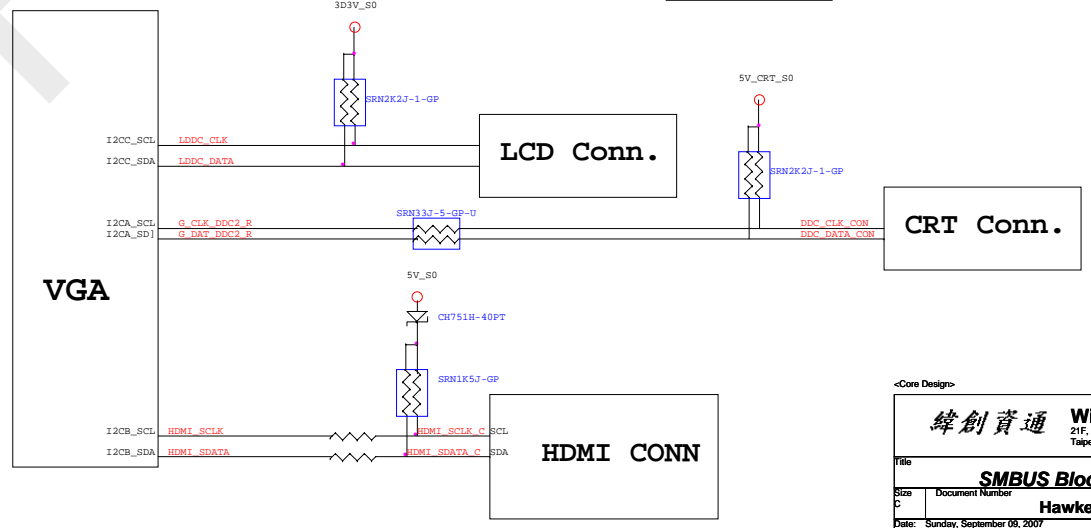
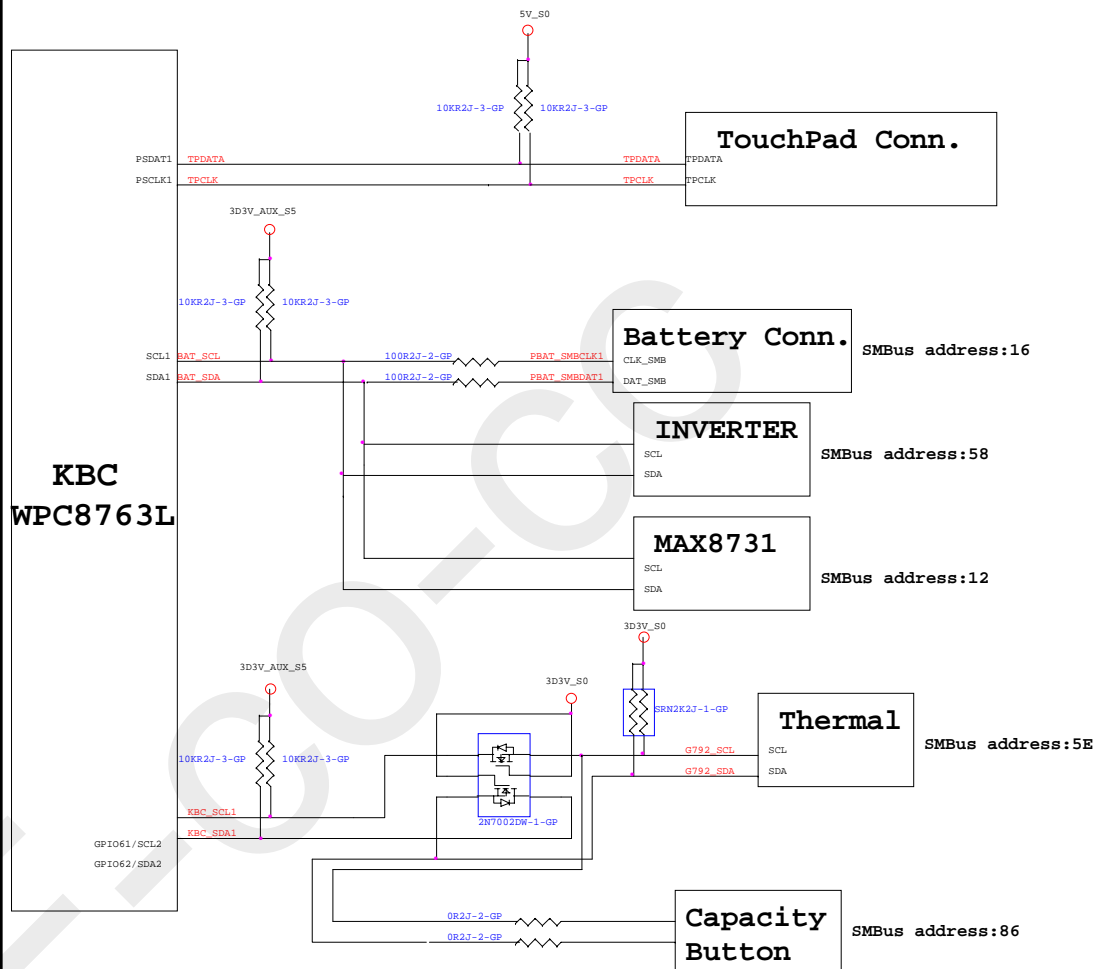
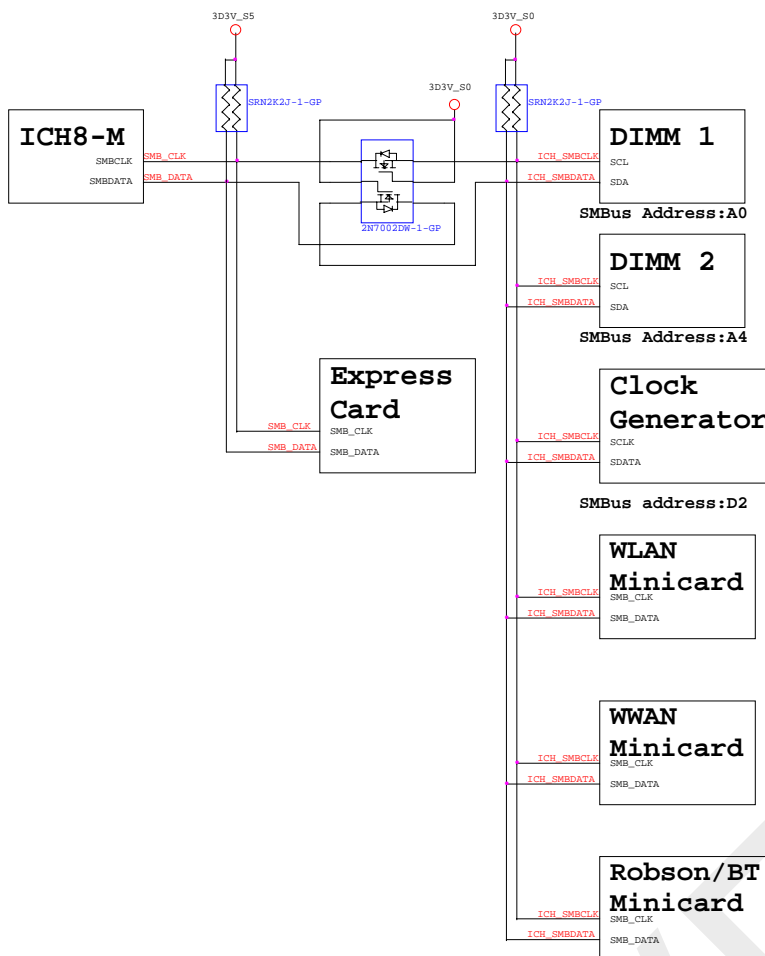
$$V_{out} = 0.75V * (R_{top} + R_{bottom}) / R_{bottom}$$

	R1	R2	R3	R4	Vout (V)
GFX_CORE_CNTRL NA	DY	DY	DY	18.7K	1.15V
GFX_CORE_CNTRL Low	8.45K	10K	40.2K to FET	DY	1.15V
GFX_CORE_CNTRL High	8.45K	10K	40.2K to GND	DY	1.2V

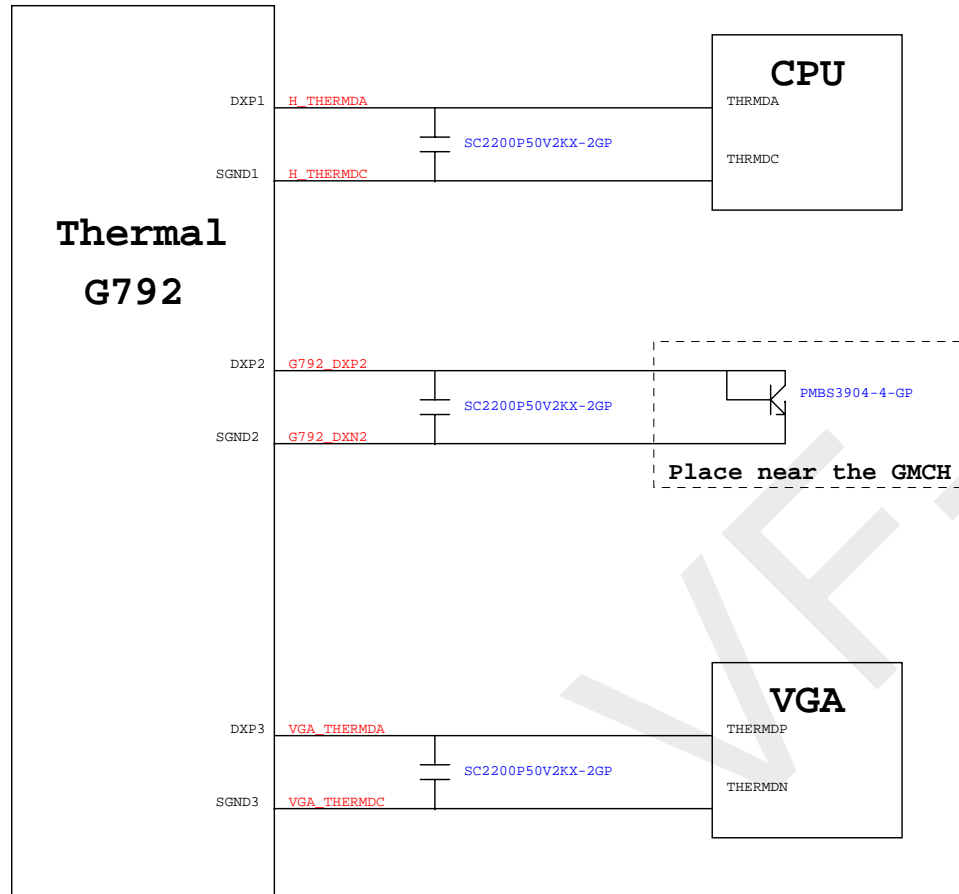


ICH8 SMBus Block Diagram

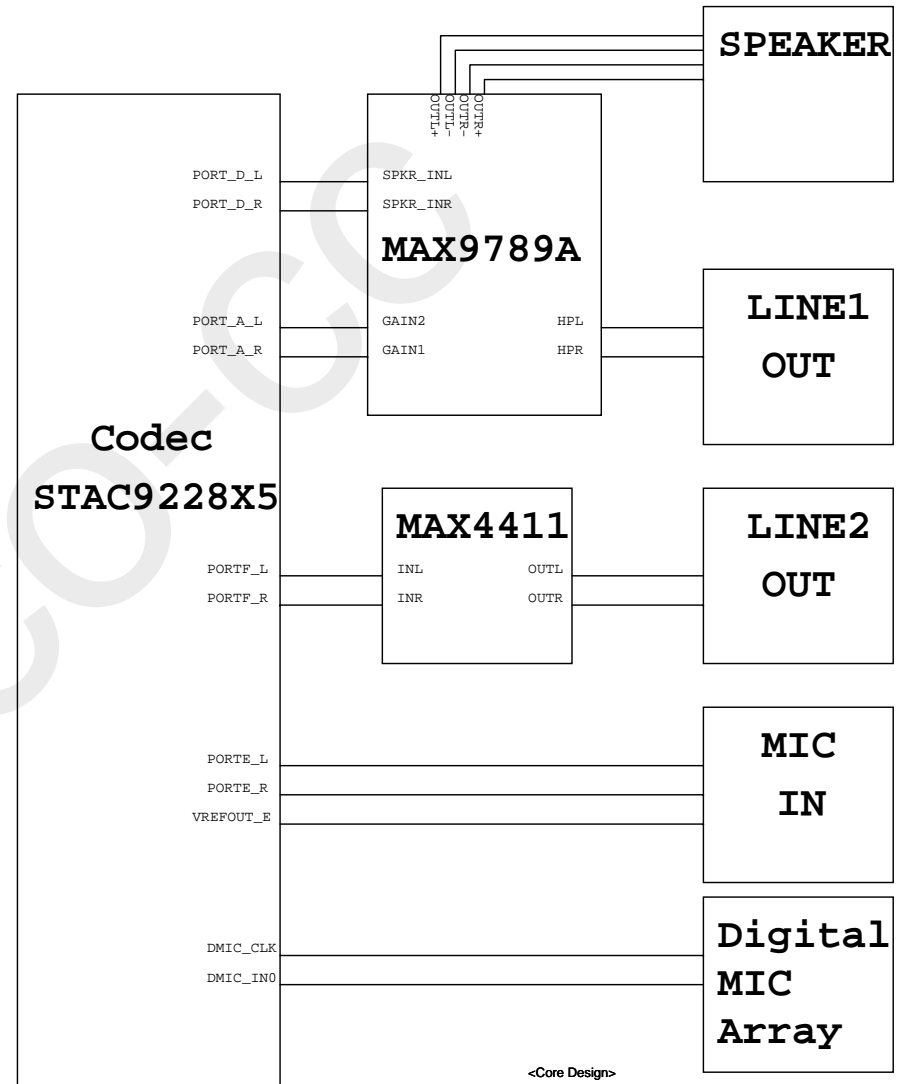
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



<Core Design>

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Title		
Thermal/Audio Block Diagram		
Size	Document Number	Rev
B	Hawke-Intel	-1
Date:	Sunday, September 09, 2007	Sheet 55 of 57

DATE	VERSION	ITEM	PAGE	Modify List	Issue Description	OWNER
		1	4	Changed R431 from 10K ohm to 2.2K ohm.	Follow M08 design.	EE
		2	4	Changed X4's CL from 20pF to 10pF and changed C392 and C399 from 27pF to 12pF.	By the Xtal vendor's FAE suggestion.	EE
		3	4	Changed RN27, RN28, RN29 and RN31 from 0 ohm to 22 ohm.	To solved these clock signals' Slew Rate are over spec.	EE
		4	18	Changed LVDS connector from 42-pin to 40-pin.	By ME suggestion.	ME
		5	18,33	Connected the LCD1 pin 3 to GND and connected pin 6 to WPC8763's GPIO05 (pin 108 of U17) with 10K ohm pull up to 3D3V_AUX_S5.	Supported the LCD cable PAID.	EE
		6	18	Added EC75-EC78 near CAMERA1.	By EMC team suggestion.	EMC
		7	20	Change C354 and C355 from 15pF to 12pF and changed X1 package from DMX26S to SM-14J.	By the Xtal vendor's FAE suggestion.	EE
		8	21	Added R526 10K ohm between GPIO026 and 3D3V_S0, removed R404.	To solved 3D3V_S0 has leakage when S3 and S5.	EE
		9	21	Added the reserved Q47, D31, R530, R531 and R532.	For test EC_RMRST#_R circuit.	EE
		10	21	Changed R442 from 22.6 ohm to 20 ohm.	To sloved the left side USB ports and Camera USB's eye diagram fail.	EE
		11	23	Changed HDD connector.	By ME suggestion.	ME
		12	25	Changed 1394 connector.	To used reverse type by ME suggestion.	ME
		13	25	Changed X5's CL from 20pF to 12pF.	By the Xtal vendor's FAE suggestion.	EE
		14	25	Removed R466, U26, R192 and D19, and connected the net MC_PWR_CTRL_0 to U25 pin 4.	For these materials are no used.	EE
2007/07/06	X00 to X01	15	25	Populated C887, C888 and C894-C896.	By EMC team suggestion.	EMC
		16	26	Changed C387 and C390 from 27pF to 12pF.	By the Xtal vendor's FAE suggestion.	EE
		17	27	Changed RJ1 connector.	By ME suggestion.	ME
		18	30	Changed U61 from 8Mbits to 16Mbits SPI ROM.	By customer requirement.	EE
		19	30	Added EC79-EC82 near CAP1.	By EMC team suggestion.	EMC
		20	30	Added EC83-EC88 near BT1.	By EMC team suggestion.	EMC
		21	30	Added EC90-EC91 near CN2 (Biometric).	By EMC team suggestion.	EMC
		22	31	Changed C880 and C881 from 0402 size to 0603 size.	Follow Thurman design.	EE
		23	32	Swaped the nets AUD_HP1_OUT_R1, AUD_HP1_OUT_L1 with AUD_AMP_GAIN1, AUD_AMP_GAIN2.	To sloved the HP1 hadn't output.	EE
		24	32	Changed R211 and R212 from 100K ohm to 10M ohm.	To sloved the AUD_HP1_EN and AUD_HP2_EN volatge level lower than 2V.	EE
		25	33	De-pop R396 and populated R395.	To changed the MB version id to SB.	EE
		26	33	Changed R391 and R405 from 10K ohm to 100K ohm.	To sloved the INSTANT_BTN# and SNIFFER_PWR_SW# can't work.	EE
		27	33	Added R527 100K ohm between WLAN/BT_BTN# and 3D3V_AUX_S5.	To sloved the WLAN/BT_BTN# can't work.	EE
		28	33	Changed X2 package from DMX26S to SM-14J.	By the Xtal vendor's FAE suggestion.	EE
		29	33,36	Changed KB1 from 25-pin to 27-pin connector, connected the KB1 pin 27 to GND and connected pin 26 to WPC8763's GPI92 (pin 99 of U17) with 10K ohm pull up to 3D3V_AUX_S5.	Supported the KB cable PAID.	ME,EE
		30	33	Changed R408 and R389 from 10K ohm to 4.7K ohm.	By Vendor's FAE suggestion.	EE
		31	35	Changed FAN1 from 4-pin to 3-pin connector.	By ME suggestion.	ME
		32	36	Added R534, Q48 and R535 off SATA_LED# and Q23.	Supported the HDD LED is dim when sinffer switch press.	EE
		33	36	Connected LED2 pin A from 5V_S0 to 5V_S5.	To sloved the Power LED can't breath when system enter S3.	EE
		34	38	Changed C530 and C531 from 1206 size to 1210 size and populated C7.	To solved noise when battery full load.	Power
		35	39	Changed R477 from 12.1K ohm to 13.3K ohm and changed R468 from 12.1K ohm to 11.8K ohm.	To adjust 3.3V and 5V current limit by power team suggestion.	Power
		36	40	Changed R7 from 12.7K ohm to 11.8K ohm and changed R468 from 3.24K ohm to 3.65K ohm.	To adjust CPU Vcore current limit by power team suggestion.	Power
		37	42	Changed R135 from 12.1K ohm to 11K ohm .	To adjust 1.05V current limit by power team suggestion.	Power
		38	43	Populated C529.	By EMC team suggestion.	EMC
		39	46	Added more one hole H33.	By EMC team suggestion.	EMC
		40	46	Populated EC28 and EC31.	By EMC team suggestion.	EMC
		41	47	Added C900, C901, C904 10uF and TC26 100uF.	To sloved VGA Vcore had OVP when run 3Dmark.	Power
		42	53	Changed R135 from 12.1K ohm to 10.5K ohm .	To adjust CPU Vcore current limit by power team suggestion.	Power
		43	53	Added EC89 0.1uF between DCBATOUT and GND.	By EMC team suggestion.	EMC

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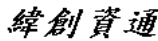
Title
HISTORY from X00 to X01

Size A3 Document Number **Hawke-Intel** Rev **-1**

Date: Sunday, September 09, 2007 Sheet 56 of 57

DATE	VERSION	ITEM	PAGE	Modify List	Issue Description	OWNER
		1	4	Changed U22 from ICS 9LPRS365BKLF to Realtek RTM875M-606-LF.	Changed clock gen symbol from ICS 9LPRS365BKLF to Realtek RTM875M-606-LF.	EE
		2	15	Changed HDMI power rail from +5V_HDMI to 5V_S0.	Follow Thurman design.	EE
		3	17	Populated D4, D5, D6, D7 and D8.	By NV GPU ESD requirement.	EMC
		4	17	Changed L1, L2 and L4 from BLM18BA100SN1 to BLM18BB470SN1	To solve the ring on RGB signal.	EE
		5	18,33	Added D32, connected pin 1 to LCDVDD_TST_EN, pin 2 to LCDVDD_EN and pin 3 to ENVDD. Changed R276 from 0 to 100k ohm and changed R276.1 to GND	Added LCDVDD_TST_EN from U17.27 to control U53.3	EE
		6	18	Disconnted LCD1 pin 3 and pin 10	To prevent the power short to GND.	EE
		7	21	Added R542 for ECSCI# need to pull up 3D3V_S0	To solve one of CPU core always loading 100%.	EE
		8	27	Added EC92 22pF between NEWCARD_CLKREQ# and GND	By EMC team suggestion.	EE
		9	27	Added note for transformer source part number.	By EMC team suggestion.	EE
		10	29	1.Changed D20 to U73 for Bluetooth Action circuit. 2.Reserved U73, R193 and R195, populated R194.	1.It can be used both BT module and BT mini-card. 2.Keep BT module now.	EE
		11	29, 33	Connect MINI2 pin 20 to U17.24 (GPO47 of KBC).	Changed WWAN enable WiFi RF controlled by another GPIO pin (U17.24 is GPO47 of KBC).	EE
		12	30, 33	Rename SNIFFER_YELLOW# to SNIFFER_YELLOW, SNIFFER_BLUE# to SNIFFER_BLUE.	These pins are High active.	EE
		13	30	Disconnted SNIFFER_BD1 pin 8 and CAP1 pin 7.	To prevent power short to GND.	EE
2007/08/17	X01 to X02	14	30	Changed EC90 and EC91 from 22pF to MLVG0402220NV05BP.	By EMC team suggestion.	EMC
		15	32	Populated EC24, EC25, EC26 and EC27 and change to 1000pF.	By EMC team suggestion.	EMC
		16	32	Changed Q45 to U47 and added R543.	To add AUD_SPK_ENABLE# controlled by AMP_MUTE#.	EE
		17	32	Changed R197 from 0 ohm to 100K ohm and pull up to +5V_SPK_AMP, dispopulated R505 and populated R213.	To solve HP1, HP2 and Speaker have "BoBo" noisy when power on, off, enter S3.	EE
		18	33	Populated R396 and R398, dispopulated R395 and R399.	Change Board ID to version SC.	EE
		19	36	Populated Q48 and R534, dispopulated R535.	HDD LED should be dim when power on by Sniffer button.	EE
		20	36	Changed C275 and C276 from reserved 33pF to MLVG0402220NV05BP, and populated them	By EMC team suggestion.	EMC
		21	36	Changed KB EMI caps from 220pF to 180pF.	To solved the word has repeat symptom when key-in.	EE
		22	38	The U42 and U44 were swap the main source and 2nd source.	To prevented used AO4468 that SI4800BDY 2nd source on charger H/S and L/S MOS.	EE
		23	39	Populated R485 and dispopulated R489.	To changed 3V and 5V PWM to Skip mode.	EE
		24	42, 43, 53	Changed C329, C566 and C272 rated voltage from 6.3V to 10V.	For derating issues by power team requirment.	EE
		25	43, 53	Change the U56 and U39 from 2nd source to main source, and swap the U38 and U58's the main source and 2nd source	To combined U39 and U56 material item of BOM with CPU H/S MOS (U4 and U35).	EE
		26	20	Changed C354 and C355 from 12pF to 8.2pF.	For Negative Resistance of X1 isn't enough.	EE
		27	33	Changed C350 and C351 from 15pF to 10pF.	For Negative Resistance of X2 isn't enough.	EE

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HISTORY from X01 to X02	
Size A3	Document Number
Hawke-Intel	
Date: Sunday, September 09, 2007	Sheet 57 of 57
Rev -1	