

Alba UMA Schematics

uFCPGA Mobile Penryn


Intel Cantiga-GM + ICH9M

2009-04-06

REV : -1

DY : Nopop Component

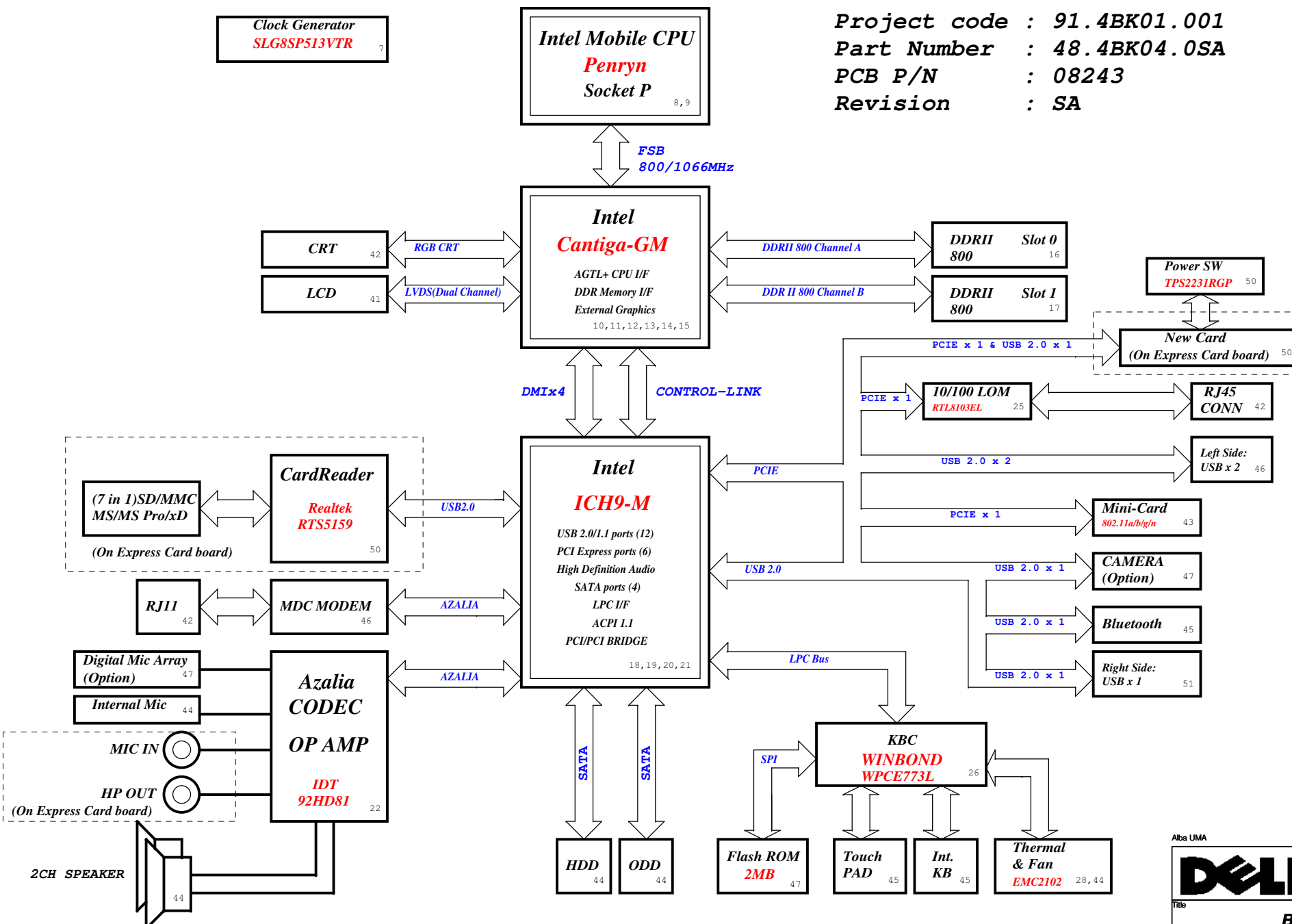
Alba UMA

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
Cover Page					
Size Custom	Document Number Alba UMA				Rev -1
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ALBA UMA Block Diagram

Project code : 91.4BK01.001
 Part Number : 48.4BK04.0SA
 PCB P/N : 08243
 Revision : SA

PCB LAYER	
L1:	Top
L2:	GND
L3:	Signal
L4:	Signal
L5:	VCC
L6:	Signal
L7:	GND
L8:	Bottom



ISL6266A/CPU_CORE	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

TPS51117/1.05V	
INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VCCP

TPS51125/3V, 5V	
INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW2 +3.3V_RTC_LDO +5V_ALW +3.3V_ALW

TPS51116/1.8V, 0.9V	
INPUTS	OUTPUTS
+PWR_SRC	+1.8V_SUS +0.9V_DDR_VTT +V_DDR_MCH_REF

L6935TR/1.5V	
INPUTS	OUTPUTS
+1.8V_SUS	+1.5V_RUN

MAX8731A/CHARGER	
INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC

RUN PWR/3V, 5V	
INPUTS	OUTPUTS
+5V_ALW +3.3V_ALW	+5V_RUN +3.3V_RUN

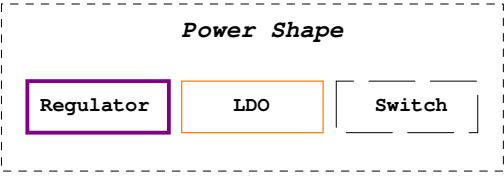
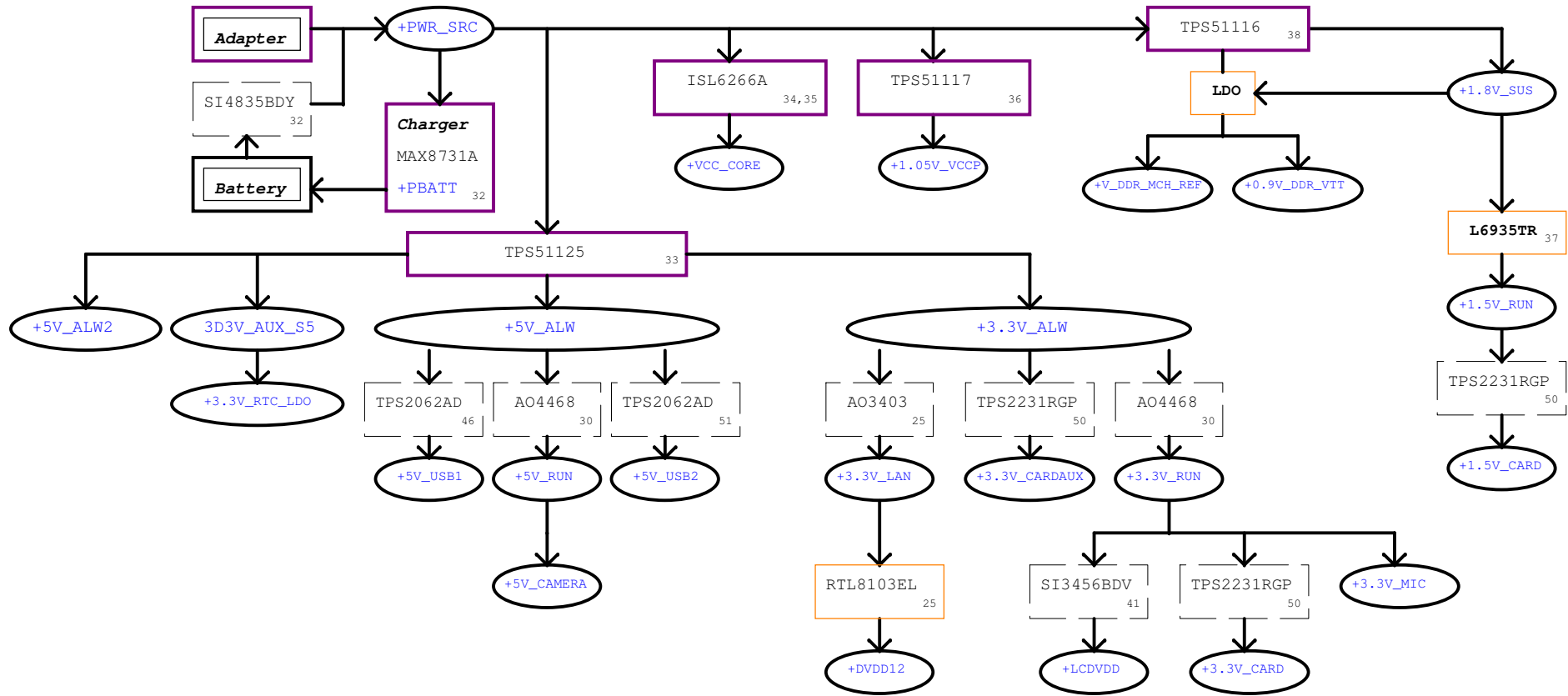
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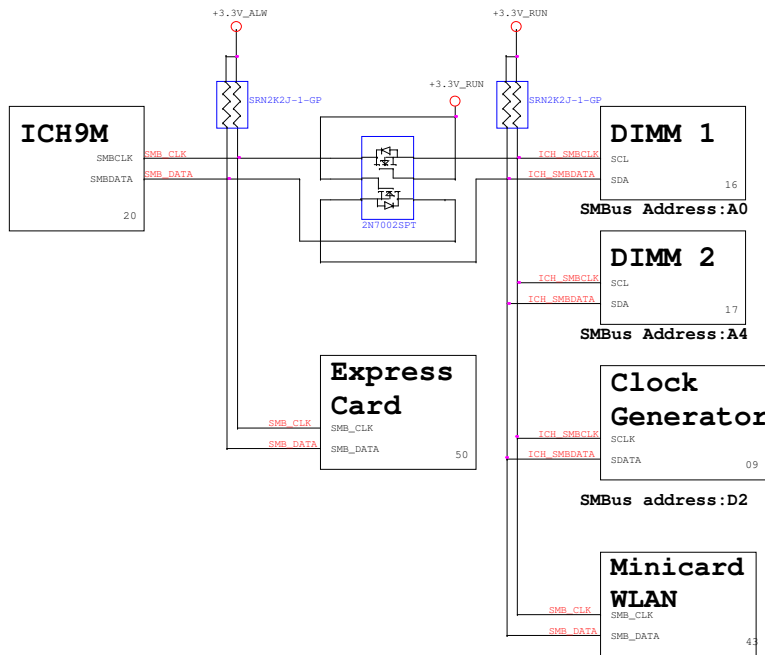
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Size: Custom Document Number: **Alba UMA** Rev: **-1**

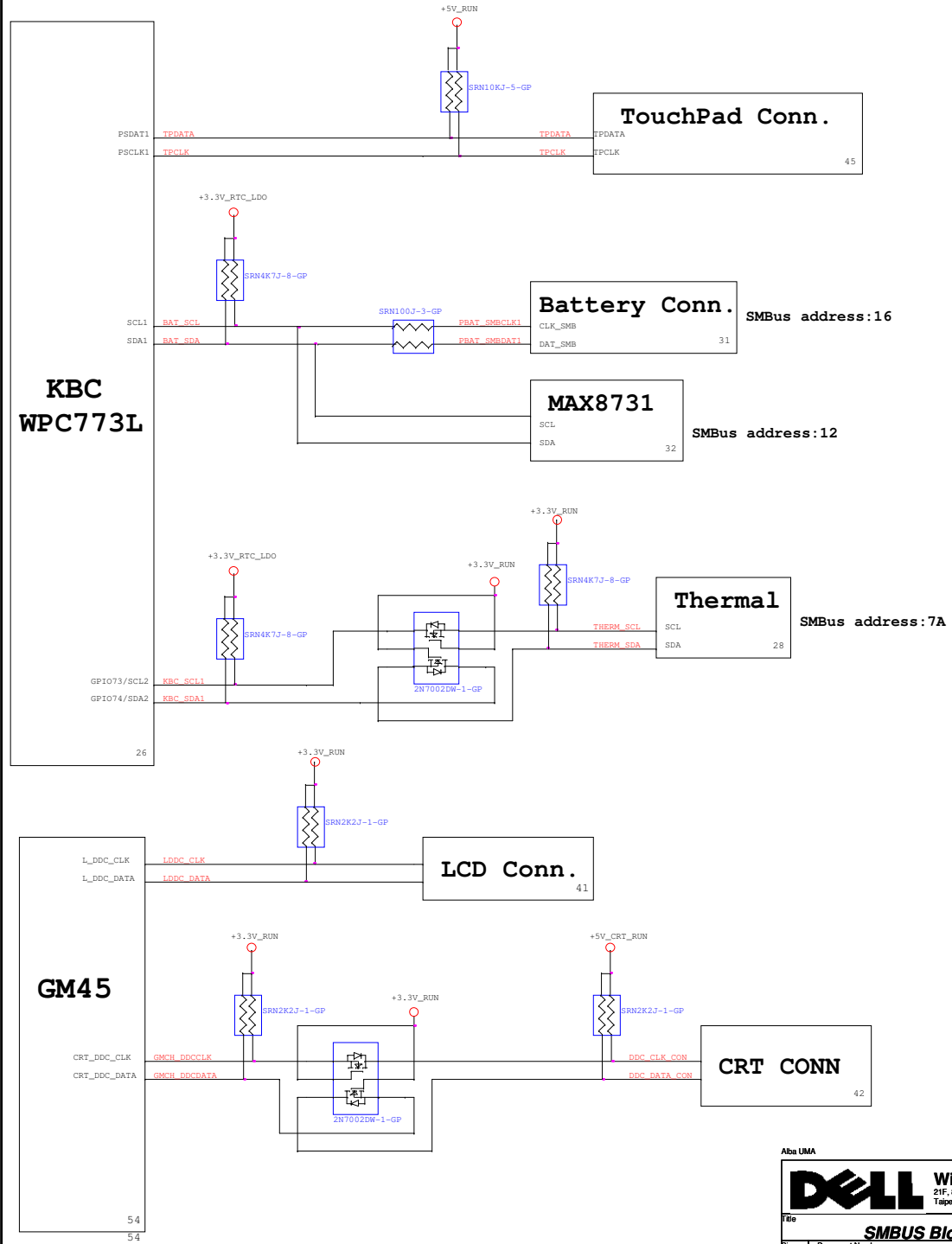
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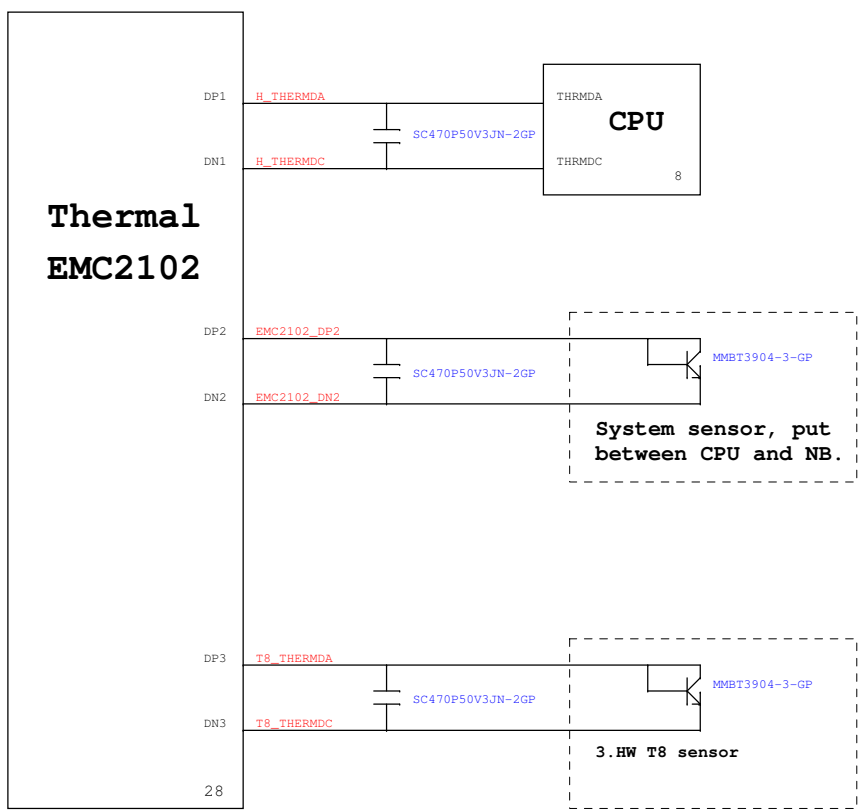
ICH9M SMBus Block Diagram



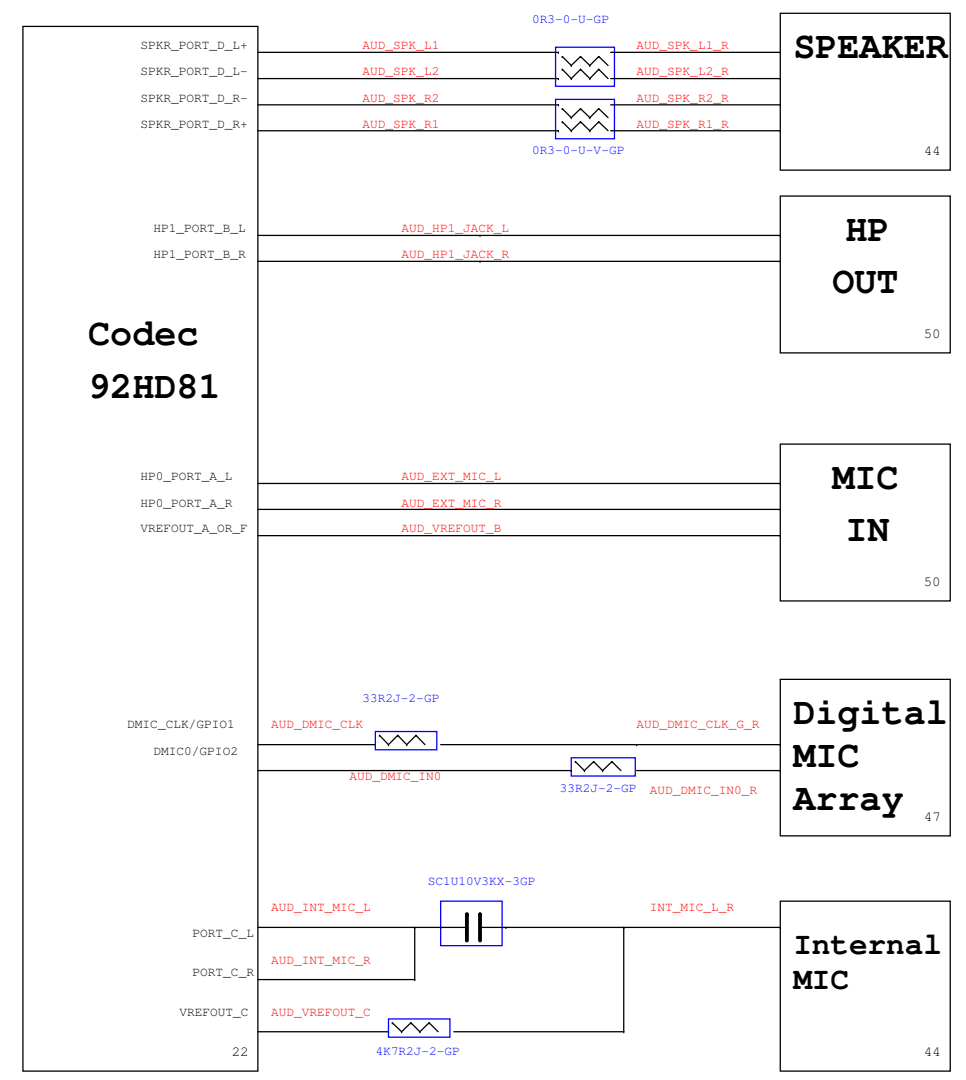
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5

ICH9 Integrated pull-up and pull-down Resistors

ICH9 EDS 642879 Rev.1.5

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 Rev.0.5

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/PCIE Port Config1 bit1, Rising Edge of PWROK.	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC (Config Registers: offset 224h). This signal has weak internal pull-down.
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of PRC.PC (Config Registers: Offset 224h).
GNT2#/GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of PRC.PC2 (Config Registers: Offset 224h).
GPIO20	Reserved.	This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK.	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/GPIO55	Top-Block Swap override. Rising Edge of PWROK.	Sampled low: Top-Block Swap mode (inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers: Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disable. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage. Rising Edge of CLPWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR (Device 28: Function 0:Offset D8).
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode (ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/HDA_DOCK_EN#	Flash Descriptor Security Override Strap. Rising Edge of PWROK.	Sampled low: the Flash Descriptor Security will be overridden. If high, the security measures will be in effect. This should only be enabled in manufacturing environments using an external pull-up resistor.

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLEVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller.
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO20	PULL-DOWN 20K
GPIO49	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0 = The iTPM Host Interface is enabled (Note 2) 1 = The iTPM Host Interface is disabled (default)
CFG7	Intel Management engine crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (Default)
CFG9	PCIE Graphics Lane	0 = Reserved Lanes, 15->0, 14->1 ect.. 1 = Normal operation (Default): Lane Numbered in Order
CFG10	PCIE Loopback enable	0 = Enable (Note 3) 1 = Disable (Default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enable (Note 3) 11 = Disabled (Default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation (Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode [MCH->ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [MCH->ICH]: (3->0, 2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display Port or PCIE is operational (Default) 1 = Digital display Port and PCIE are operating simultaneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1 = LFP Card Present; PCIE disabled

NOTE:

- All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
- iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

PCIE Routing

LANE2	MiniCard WLAN
LANE3	LAN
LANE5	New Card

USB Table

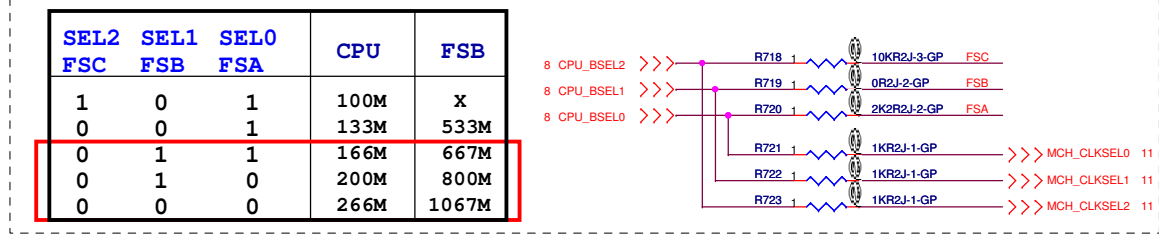
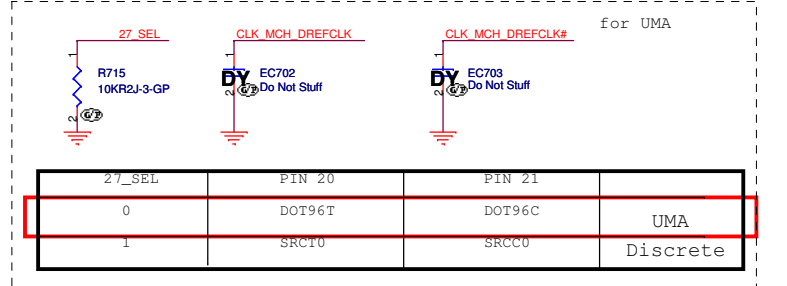
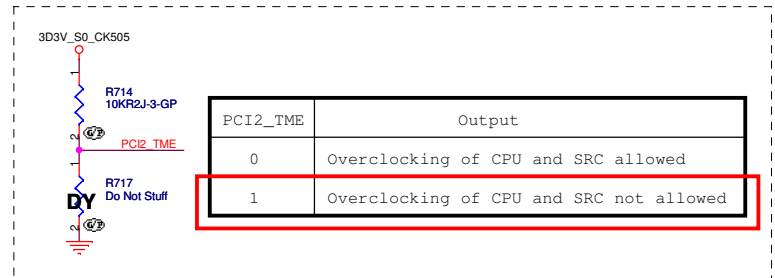
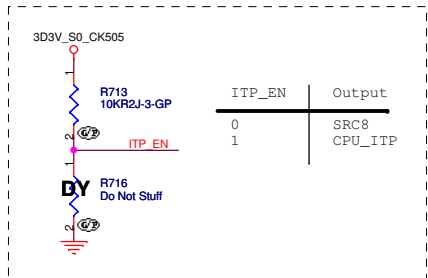
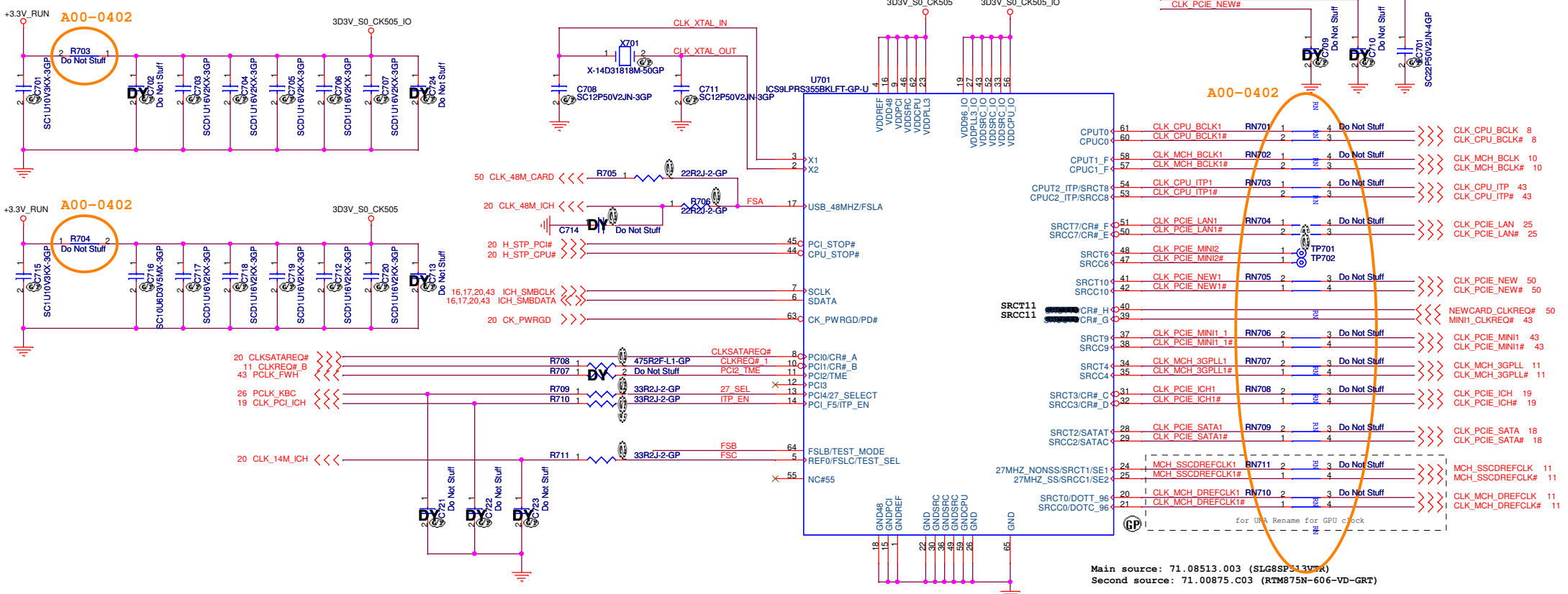
USB	
Pair	Device
0	USB1
1	USB2
2	USB3
3	RESERVED
4	MINI CARD
5	RESERVED
6	BLUETOOTH
7	NEW CARD
8	RESERVED
9	RESERVED
10	Card Reader
11	CAMERA

Alba UMA



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SSID = CLOCK



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Title: **Clock Generator SLG8SP513VTR**

Size	Document Number	Rev
Custom	Alba UMA	-1

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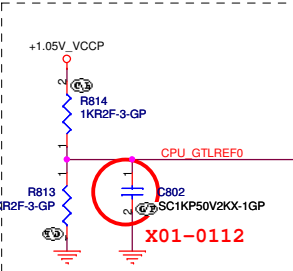
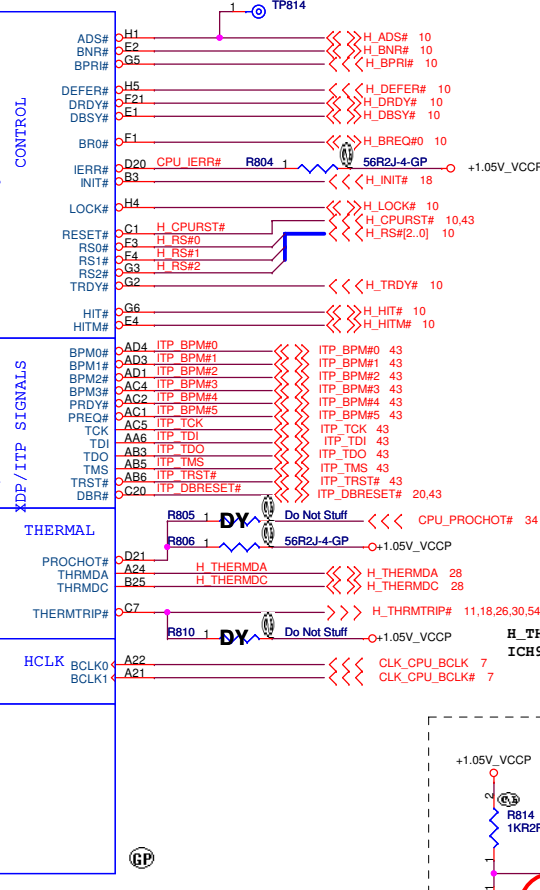
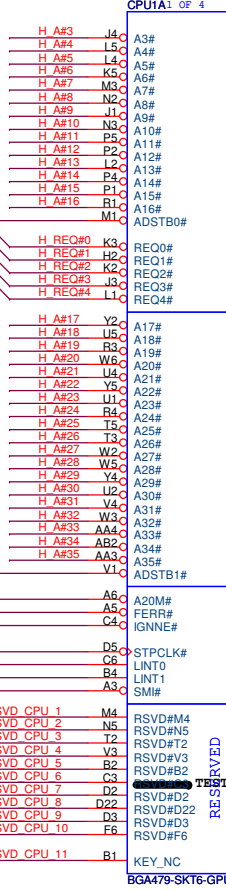
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10 H_ADSTB#1 <<<

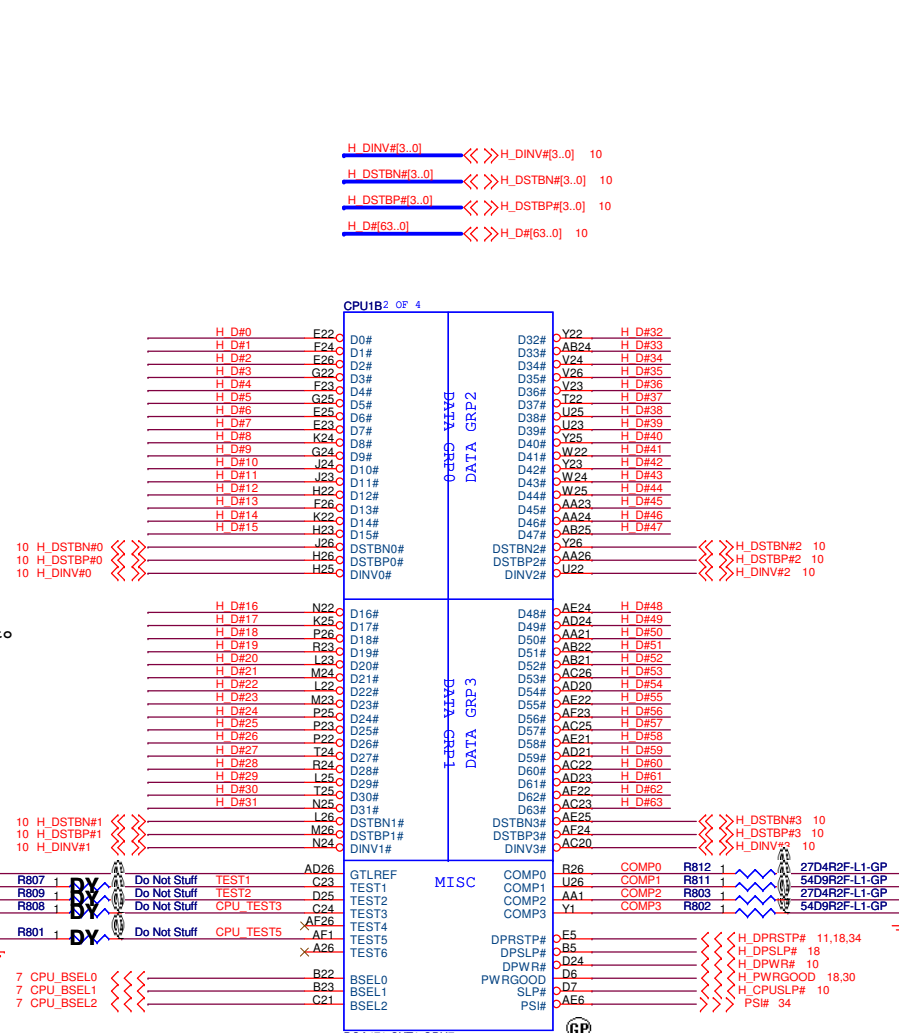
18 H_A20M# <<< H_FERR# <<< H_IGNNE# <<<

18 H_STPCLK# <<< H_INTR# <<< H_NMI# <<< H_SMI# <<<

TP807 CPU 1 M4
TP808 CPU 2 N5
TP802 CPU 3 T2
TP804 CPU 4 V3
TP803 CPU 5 B2
TP805 CPU 6 B2
TP805 CPU 7 D2
TP810 CPU 8 D22
TP808 CPU 9 D3
TP809 CPU 10 F6
TP801 CPU 11 B1

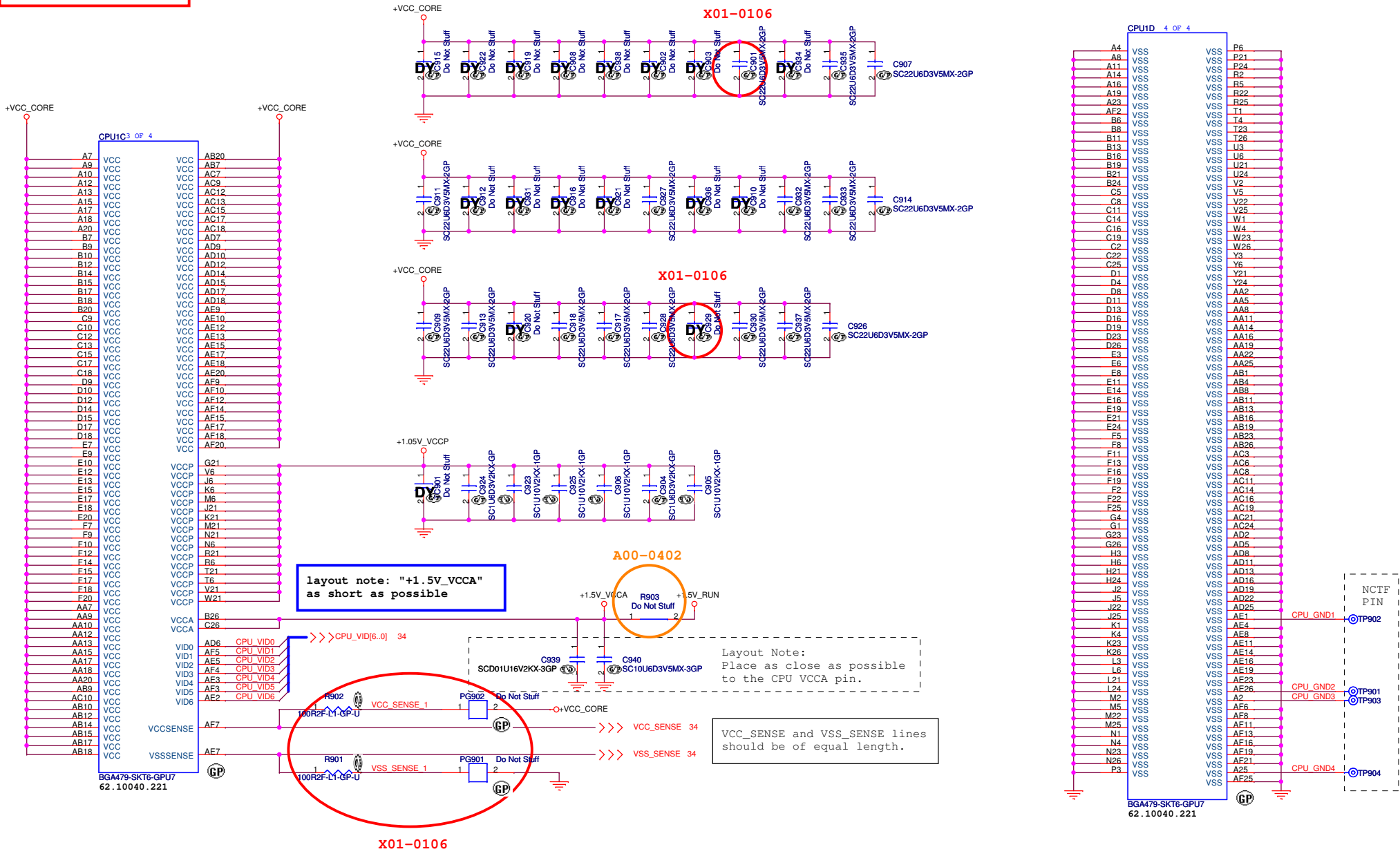


Layout notes
Z= 55 Ohm 0.5" MAX for CPU_GTLREF0



Layout Note:
Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5".
Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5".

SSID = CPU

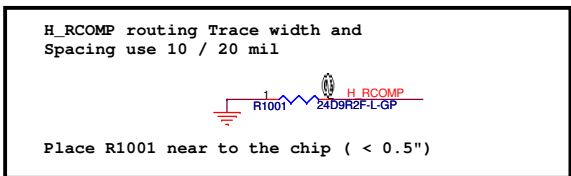
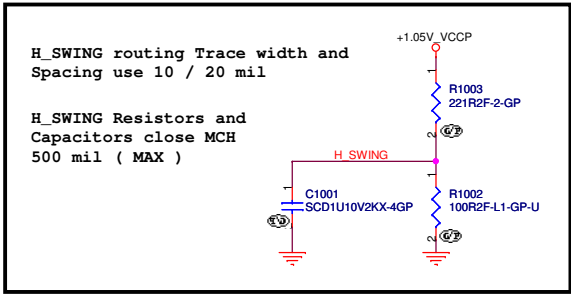
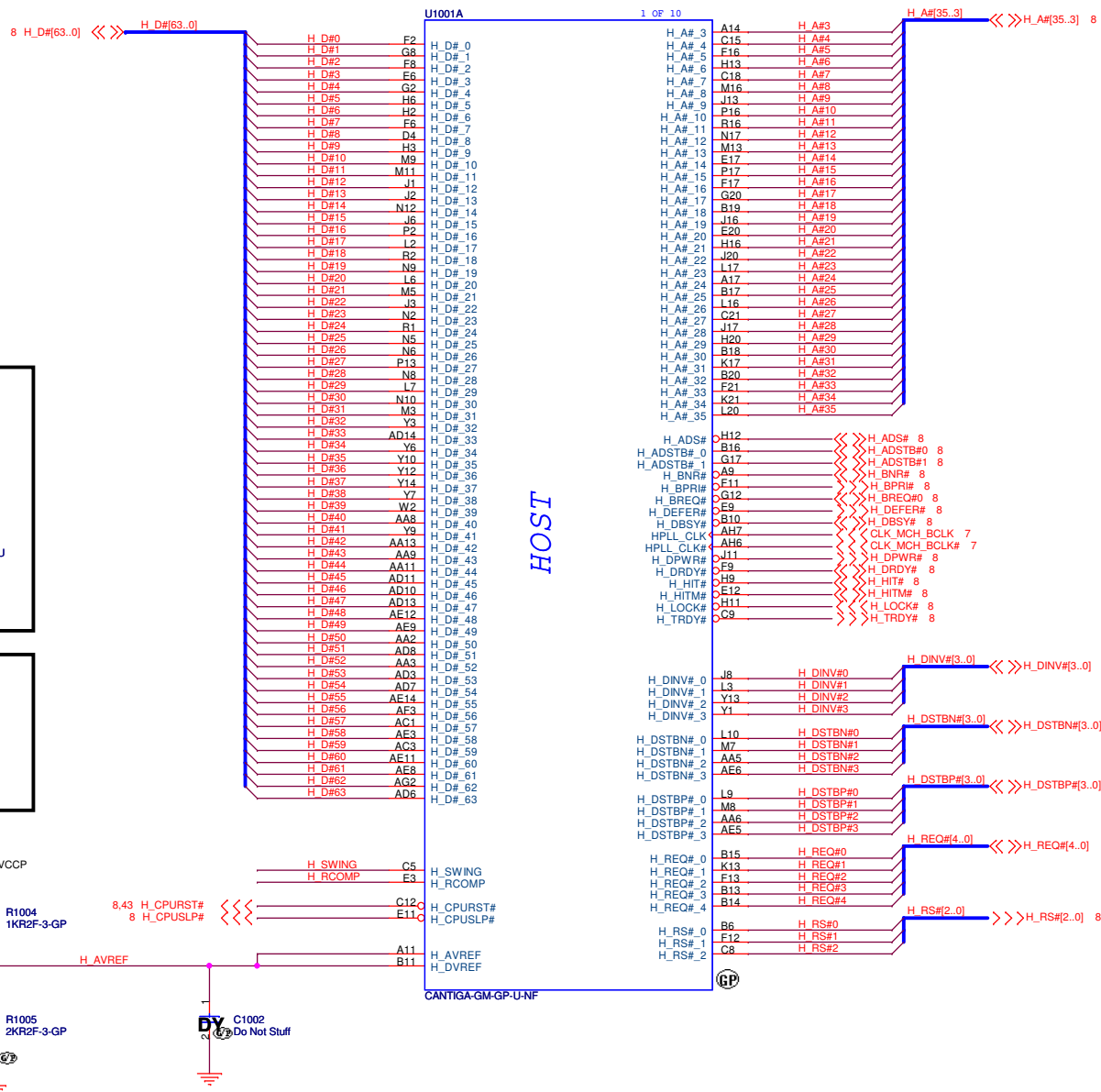


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Title: **CPU-Power(2/2)**

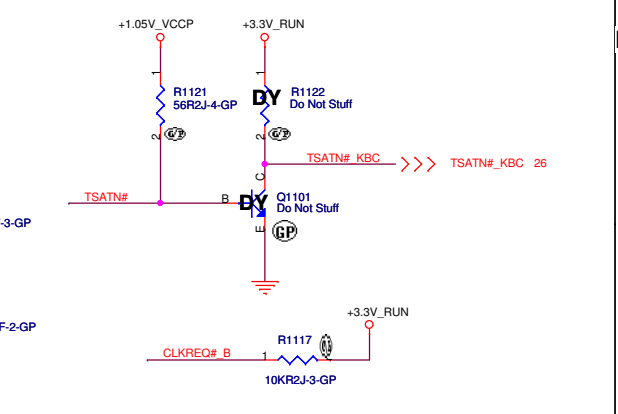
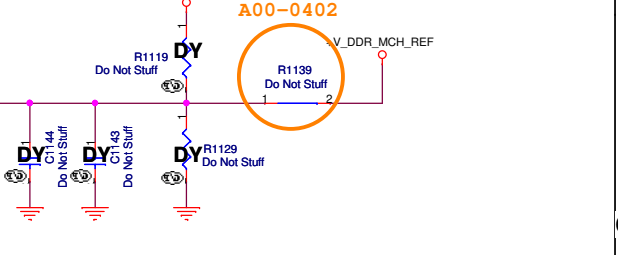
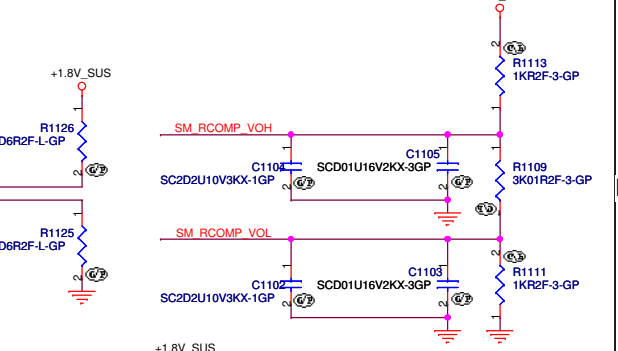
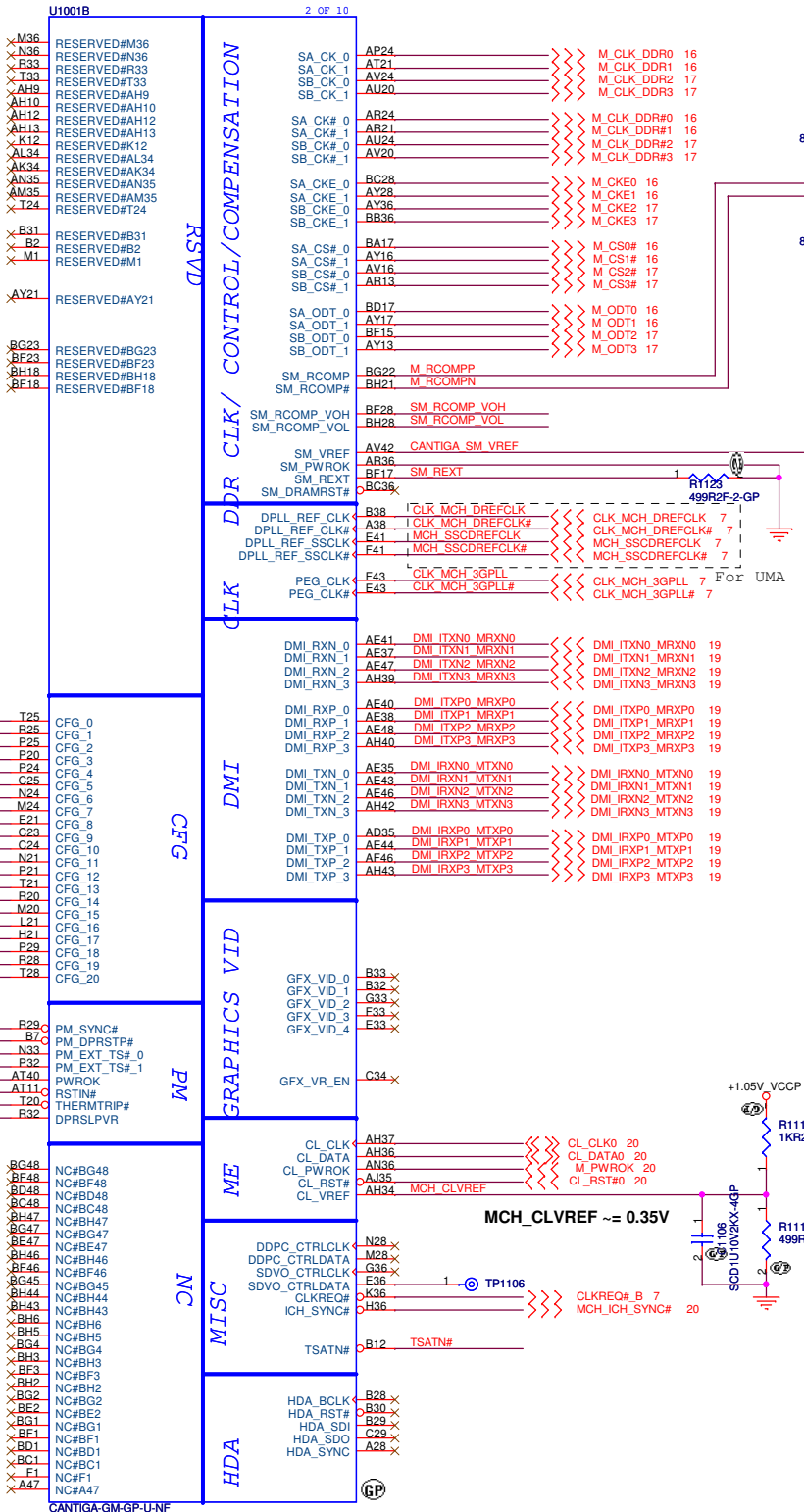
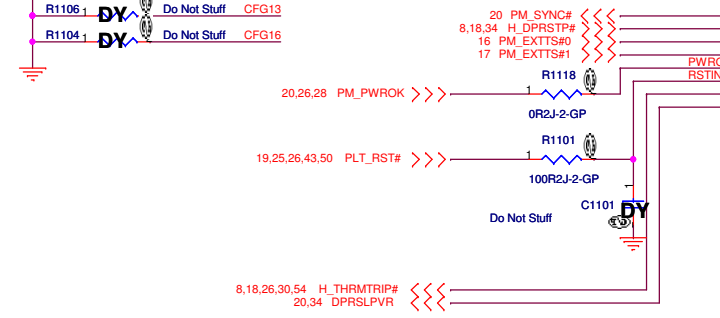
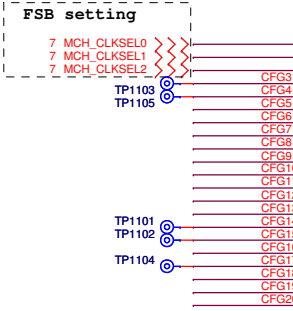
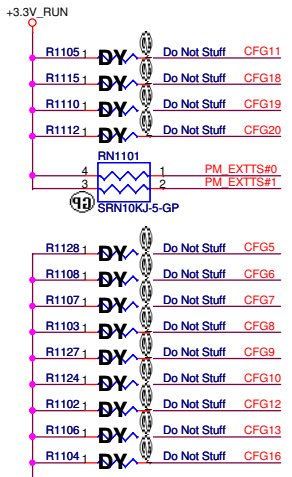
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SSID = MCH

* is current setting

CFG Strap	Low	High
CFG 5	DMI X 2	DMI X 4 *
CFG 6	ITPM enable	ITPM disable *
CFG 7	TLS cipher suite with no confidentiality	TLS cipher suite with confidentiality *
CFG 9	PCIE GFX lane reversed	PCIE GFX lane numbered in order *
CFG 10	PCIE loopback enable	PCIE loopback disable *
CFG 12	ALLZ mode enable	ALLZ mode disable *
CFG 13	XOR mode enable	XOR mode disable *
CFG 16	FSB dynamic ODT disable	FSB Dynamic ODT enable *
CFG 19	DMI Lane Reserved	Reverse DMI lanes
CFG 20	SDVO concurrent with PCIE	PCIE and SDVO are operating simultaneously via the PEG port *
SDVO_CTRLDATA	SDVO interface disable*	SDVO interface enable
L_DDC_DATA	LFP disable *	LFP card present
DDPC_CTRLDATA	SDVO/iHDMI/DP interface disabled *	SDVO/iHDMI/DP interface enabled



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Title: **Cantiga-DMI/CFG(2/6)**

Size: Custom Document Number

Rev: **Alba UMA**

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16 M_A_DQ[63..0] <<< M_A_DQ[63..0]

U1001D		
M_A_DQ0	AJ38	SA_DQ_0
M_A_DQ1	AJ41	SA_DQ_1
M_A_DQ2	AN38	SA_DQ_2
M_A_DQ3	AM38	SA_DQ_3
M_A_DQ4	AJ36	SA_DQ_4
M_A_DQ5	AJ49	SA_DQ_5
M_A_DQ6	AM44	SA_DQ_6
M_A_DQ7	AM42	SA_DQ_7
M_A_DQ8	AN43	SA_DQ_8
M_A_DQ9	AN44	SA_DQ_9
M_A_DQ10	AJ40	SA_DQ_10
M_A_DQ11	AI38	SA_DQ_11
M_A_DQ12	AN41	SA_DQ_12
M_A_DQ13	AN39	SA_DQ_13
M_A_DQ14	AU44	SA_DQ_14
M_A_DQ15	AU42	SA_DQ_15
M_A_DQ16	AV39	SA_DQ_16
M_A_DQ17	AY44	SA_DQ_17
M_A_DQ18	BA40	SA_DQ_18
M_A_DQ19	BD43	SA_DQ_19
M_A_DQ20	AV41	SA_DQ_20
M_A_DQ21	AV43	SA_DQ_21
M_A_DQ22	BD43	SA_DQ_22
M_A_DQ23	BC40	SA_DQ_23
M_A_DQ24	AY37	SA_DQ_24
M_A_DQ25	BD38	SA_DQ_25
M_A_DQ26	AV37	SA_DQ_26
M_A_DQ27	AI36	SA_DQ_27
M_A_DQ28	AY38	SA_DQ_28
M_A_DQ29	BB38	SA_DQ_29
M_A_DQ30	AV36	SA_DQ_30
M_A_DQ31	AW36	SA_DQ_31
M_A_DQ32	BD13	SA_DQ_32
M_A_DQ33	AU11	SA_DQ_33
M_A_DQ34	BC11	SA_DQ_34
M_A_DQ35	BA12	SA_DQ_35
M_A_DQ36	AU13	SA_DQ_36
M_A_DQ37	AV13	SA_DQ_37
M_A_DQ38	BD12	SA_DQ_38
M_A_DQ39	BC12	SA_DQ_39
M_A_DQ40	BB9	SA_DQ_40
M_A_DQ41	BA9	SA_DQ_41
M_A_DQ42	AU10	SA_DQ_42
M_A_DQ43	AV9	SA_DQ_43
M_A_DQ44	BA11	SA_DQ_44
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M_A_DQ48	AV5	SA_DQ_48
M_A_DQ49	AV7	SA_DQ_49
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M_A_DQ55	AN10	SA_DQ_55
M_A_DQ56	AM11	SA_DQ_56
M_A_DQ57	AM5	SA_DQ_57
M_A_DQ58	AJ9	SA_DQ_58
M_A_DQ59	AJ8	SA_DQ_59
M_A_DQ60	AN12	SA_DQ_60
M_A_DQ61	AM13	SA_DQ_61
M_A_DQ62	AJ11	SA_DQ_62
M_A_DQ63	AJ12	SA_DQ_63

DDR SYSTEM MEMORY A

4 OF 10		
SA_BS_0	BD21	M_A_BS#0 16
SA_BS_1	BG18	M_A_BS#1 16
SA_BS_2	AT25	M_A_BS#2 16
SA_RAS#	BB20	M_A_RAS# 16
SA_CAS#	BD20	M_A_CAS# 16
SA_WE#	AY20	M_A_WE# 16
SA_DM_0	AM37	M_A_DM[7..0] 16
SA_DM_1	AT41	M_A_DM1
SA_DM_2	AY41	M_A_DM2
SA_DM_3	AU39	M_A_DM3
SA_DM_4	BB12	M_A_DM4
SA_DM_5	AV6	M_A_DM5
SA_DM_6	AT7	M_A_DM6
SA_DM_7	AJ5	M_A_DM7
SA_DQS_0	AJ44	M_A_DQS0
SA_DQS_1	AT44	M_A_DQS1
SA_DQS_2	BA43	M_A_DQS2
SA_DQS_3	BC37	M_A_DQS3
SA_DQS_4	AW12	M_A_DQS4
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SA_MA_3	BH24	M_A_A3
SA_MA_4	BG25	M_A_A4
SA_MA_5	BA24	M_A_A5
SA_MA_6	BD24	M_A_A6
SA_MA_7	BG27	M_A_A7
SA_MA_8	BF26	M_A_A8
SA_MA_9	AW24	M_A_A9
SA_MA_10	BC21	M_A_A10
SA_MA_11	BG26	M_A_A11
SA_MA_12	BH26	M_A_A12
SA_MA_13	BH17	M_A_A13
SA_MA_14	AY26	M_A_A14

CANTIGA-GM-GP-U-NF



17 M_B_DQ[63..0] <<< M_B_DQ[63..0]

U1001E		
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M_B_DQ1	AH46	SB_DQ_1
M_B_DQ2	AP47	SB_DQ_2
M_B_DQ3	AP46	SB_DQ_3
M_B_DQ4	AJ46	SB_DQ_4
M_B_DQ5	AJ48	SB_DQ_5
M_B_DQ6	AM48	SB_DQ_6
M_B_DQ7	AP48	SB_DQ_7
M_B_DQ8	AU47	SB_DQ_8
M_B_DQ9	AU46	SB_DQ_9
M_B_DQ10	BA48	SB_DQ_10
M_B_DQ11	AY48	SB_DQ_11
M_B_DQ12	AT47	SB_DQ_12
M_B_DQ13	AR47	SB_DQ_13
M_B_DQ14	BA47	SB_DQ_14
M_B_DQ15	BC47	SB_DQ_15
M_B_DQ16	RC46	SB_DQ_16
M_B_DQ17	BC44	SB_DQ_17
M_B_DQ18	BG43	SB_DQ_18
M_B_DQ19	BF43	SB_DQ_19
M_B_DQ20	BE45	SB_DQ_20
M_B_DQ21	BC41	SB_DQ_21
M_B_DQ22	BF40	SB_DQ_22
M_B_DQ23	BF41	SB_DQ_23
M_B_DQ24	BG38	SB_DQ_24
M_B_DQ25	BF38	SB_DQ_25
M_B_DQ26	BH35	SB_DQ_26
M_B_DQ27	BG35	SB_DQ_27
M_B_DQ28	BH40	SB_DQ_28
M_B_DQ29	BG39	SB_DQ_29
M_B_DQ30	BG34	SB_DQ_30
M_B_DQ31	BH34	SB_DQ_31
M_B_DQ32	BH14	SB_DQ_32
M_B_DQ33	BG12	SB_DQ_33
M_B_DQ34	BH11	SB_DQ_34
M_B_DQ35	BG8	SB_DQ_35
M_B_DQ36	BH12	SB_DQ_36
M_B_DQ37	BF11	SB_DQ_37
M_B_DQ38	BF8	SB_DQ_38
M_B_DQ39	BC7	SB_DQ_39
M_B_DQ40	BC5	SB_DQ_40
M_B_DQ41	BC6	SB_DQ_41
M_B_DQ42	AY3	SB_DQ_42
M_B_DQ43	AY1	SB_DQ_43
M_B_DQ44	BF6	SB_DQ_44
M_B_DQ45	BF5	SB_DQ_45
M_B_DQ46	BA1	SB_DQ_46
M_B_DQ47	BD3	SB_DQ_47
M_B_DQ48	AV2	SB_DQ_48
M_B_DQ49	AU3	SB_DQ_49
M_B_DQ50	AR3	SB_DQ_50
M_B_DQ51	AN2	SB_DQ_51
M_B_DQ52	AY2	SB_DQ_52
M_B_DQ53	AV1	SB_DQ_53
M_B_DQ54	AP3	SB_DQ_54
M_B_DQ55	AR1	SB_DQ_55
M_B_DQ56	AL1	SB_DQ_56
M_B_DQ57	AL2	SB_DQ_57
M_B_DQ58	AJ1	SB_DQ_58
M_B_DQ59	AH1	SB_DQ_59
M_B_DQ60	AM2	SB_DQ_60
M_B_DQ61	AM3	SB_DQ_61
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M_B_DQ63	AJ3	SB_DQ_63

DDR SYSTEM MEMORY B

CANTIGA-GM-GP-U-NF



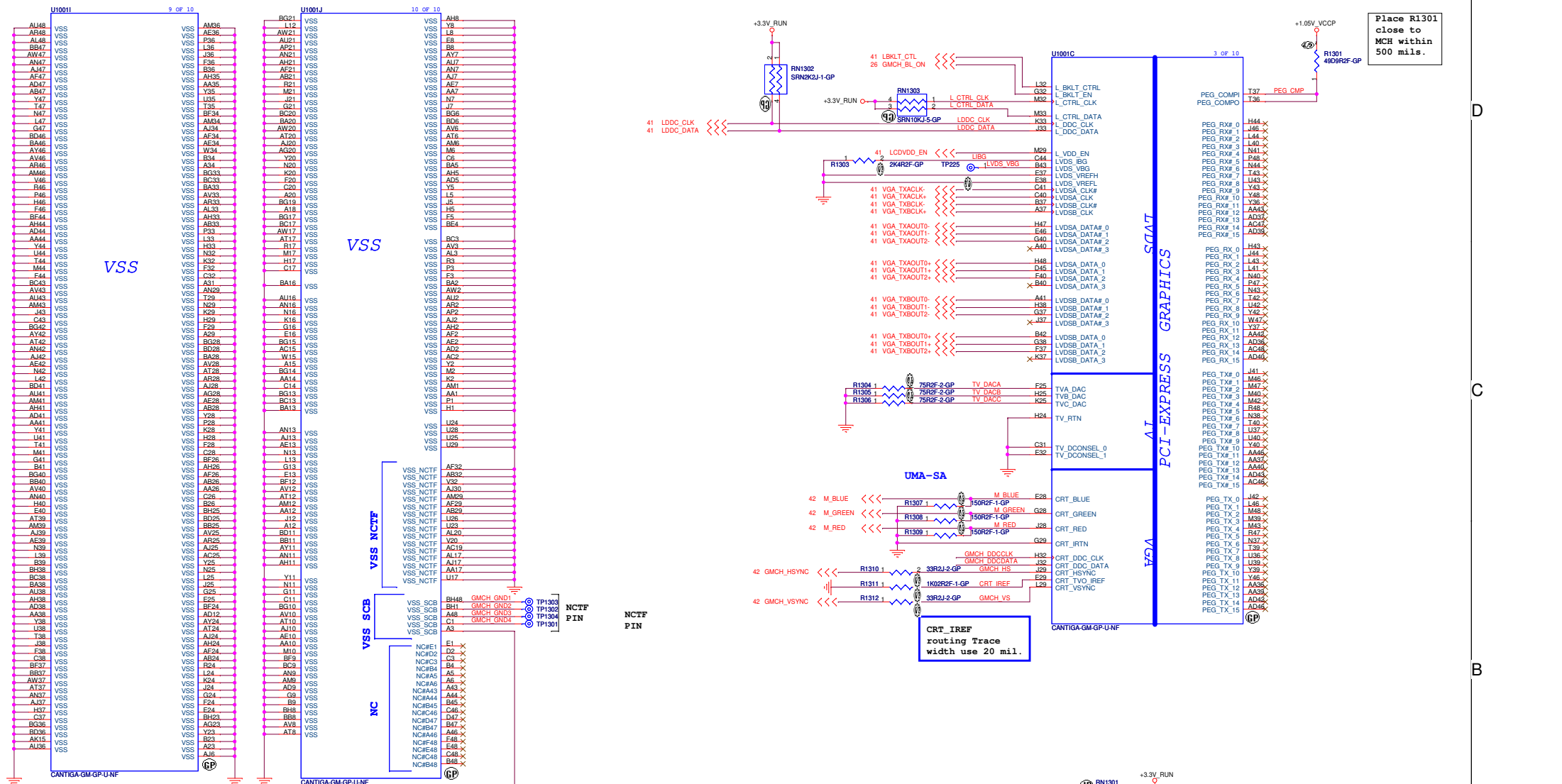
5 OF 10

U1001E		
SB_BS_0	BC16	M_B_BS#0 17
SB_BS_1	BB17	M_B_BS#1 17
SB_BS_2	BB33	M_B_BS#2 17
SB_RAS#	AU17	M_B_RAS# 17
SB_CAS#	BG16	M_B_CAS# 17
SB_WE#	BF14	M_B_WE# 17
SB_DM_0	AM47	M_B_DM[7..0] 17
SB_DM_1	AY47	M_B_DM1
SB_DM_2	BD40	M_B_DM2
SB_DM_3	BF35	M_B_DM3
SB_DM_4	BG11	M_B_DM4
SB_DM_5	BA3	M_B_DM5
SB_DM_6	AP1	M_B_DM6
SB_DM_7	AK2	M_B_DM7
SB_DQS_0	AL47	M_B_DQS0
SB_DQS_1	AV46	M_B_DQS1
SB_DQS_2	BG41	M_B_DQS2
SB_DQS_3	BG37	M_B_DQS3
SB_DQS_4	BH9	M_B_DQS4
SB_DQS_5	BB2	M_B_DQS5
SB_DQS_6	AU1	M_B_DQS6
SB_DQS_7	AN6	M_B_DQS7
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SB_DQS#_1	AV47	M_B_DQS#1
SB_DQS#_2	BH41	M_B_DQS#2
SB_DQS#_3	BH37	M_B_DQS#3
SB_DQS#_4	BG9	M_B_DQS#4
SB_DQS#_5	BC2	M_B_DQS#5
SB_DQS#_6	AT2	M_B_DQS#6
SB_DQS#_7	AN5	M_B_DQS#7
SB_MA_0	AV17	M_B_A0
SB_MA_1	BA25	M_B_A1
SB_MA_2	RC25	M_B_A2
SB_MA_3	AU25	M_B_A3
SB_MA_4	AW25	M_B_A4
SB_MA_5	BB28	M_B_A5
SB_MA_6	AU28	M_B_A6
SB_MA_7	AT33	M_B_A7
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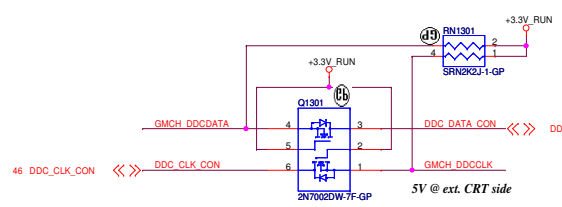
Alba UMA

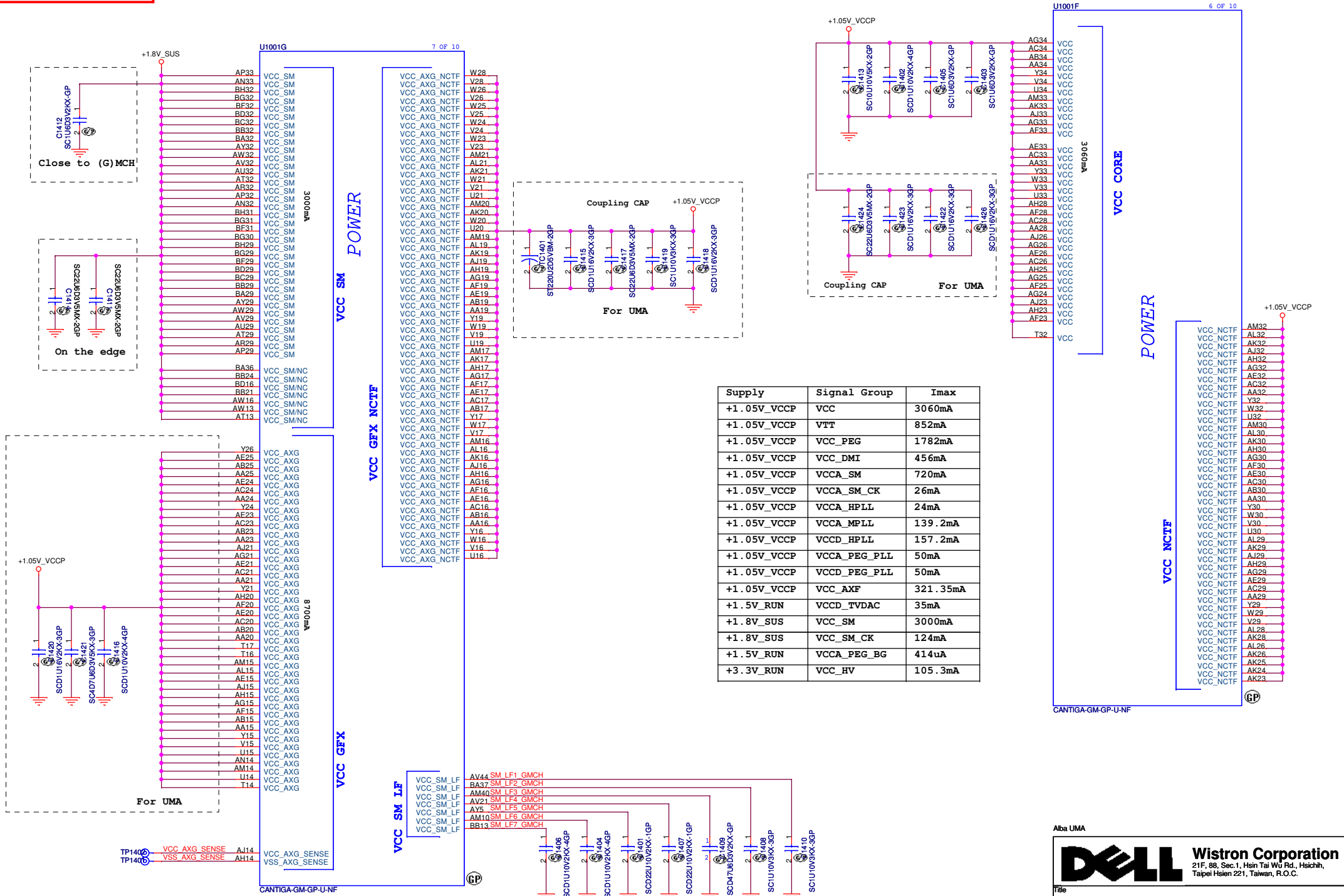


SSID = MCH



CRT_IREF routing Trace width use 20 mil.





Supply	Signal Group	Imax
+1.05V_VCCP	VCC	3060mA
+1.05V_VCCP	VTT	852mA
+1.05V_VCCP	VCC_PEG	1782mA
+1.05V_VCCP	VCC_DMI	456mA
+1.05V_VCCP	VCCA_SM	720mA
+1.05V_VCCP	VCCA_SM_CK	26mA
+1.05V_VCCP	VCCA_HPLL	24mA
+1.05V_VCCP	VCCA_MPLL	139.2mA
+1.05V_VCCP	VCCD_HPLL	157.2mA
+1.05V_VCCP	VCCA_PEG_PLL	50mA
+1.05V_VCCP	VCCD_PEG_PLL	50mA
+1.05V_VCCP	VCC_AXF	321.35mA
+1.5V_RUN	VCCD_TV DAC	35mA
+1.8V_SUS	VCC_SM	3000mA
+1.8V_SUS	VCC_SM_CK	124mA
+1.5V_RUN	VCCA_PEG_BG	414uA
+3.3V_RUN	VCC_HV	105.3mA

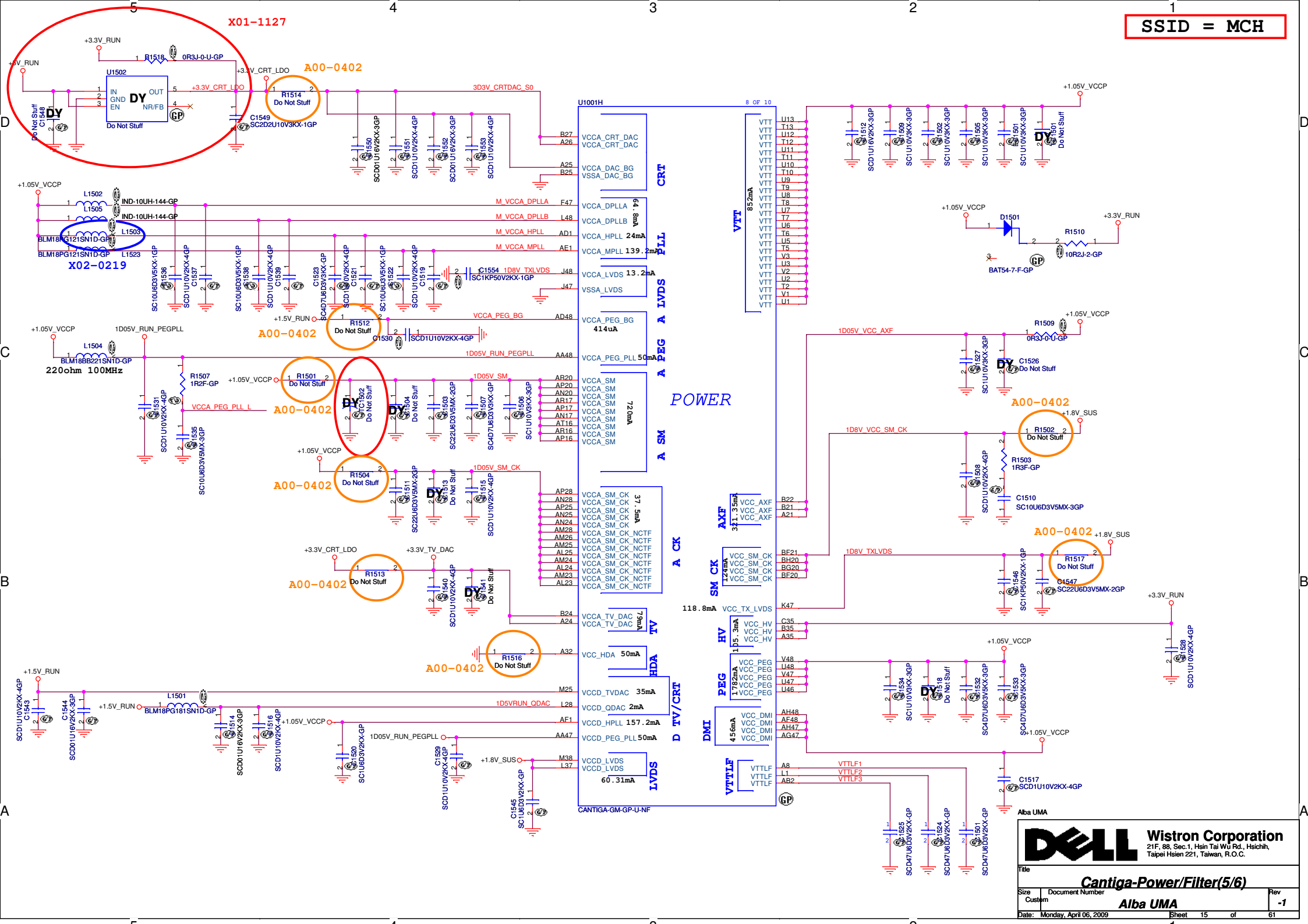
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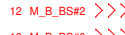
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Size	Document Number	Rev
Custom	Alba UMA	-1

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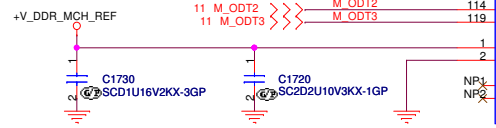
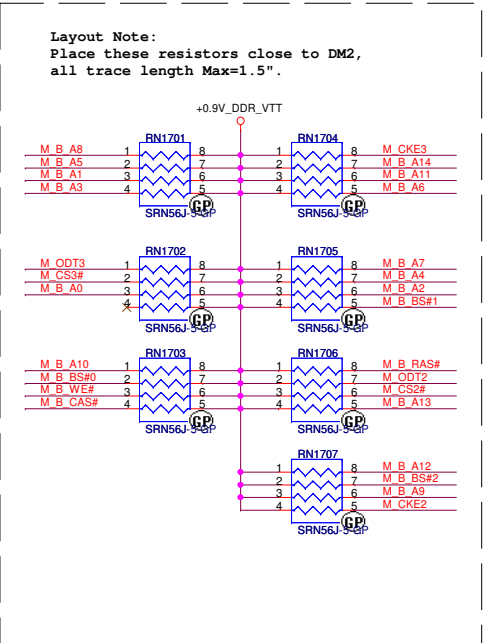
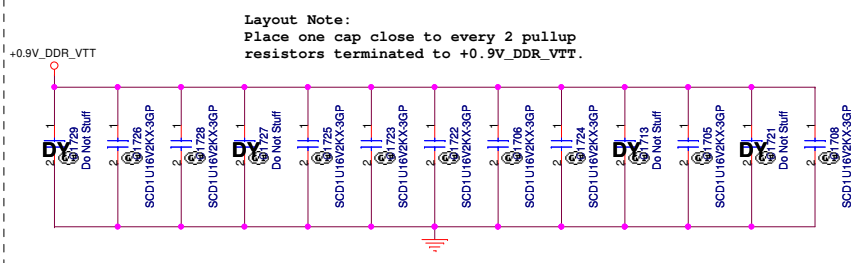
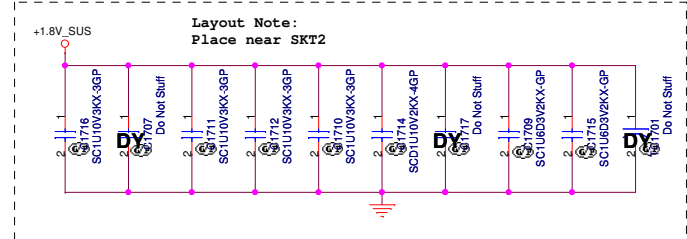
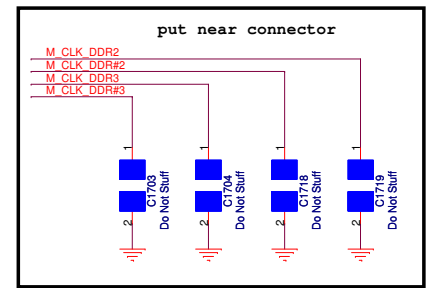
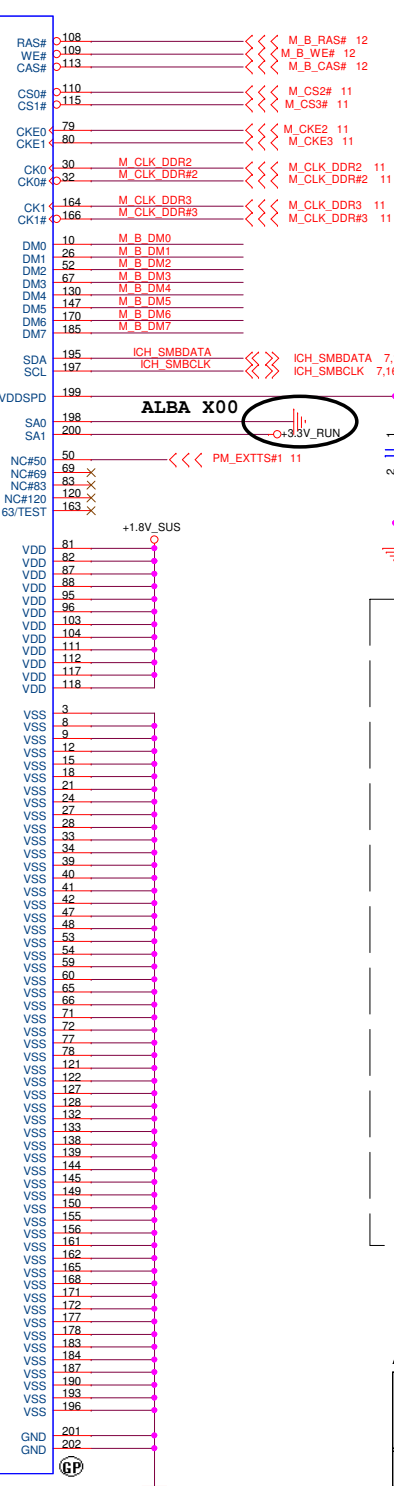


SSID = MEMORY



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M B A1	101	A1
M B A2	100	A2
M B A3	98	A3
M B A4	98	A4
M B A5	97	A5
M B A6	94	A6
M B A7	92	A7
M B A8	93	A8
M B A9	91	A9
M B A10	105	A10/AP
M B A11	90	A11
M B A12	89	A12
M B A13	116	A13
M B A14	88	A14
M B A15	84	A15
M B BS#2	85	A16/BA2
M B BS#0	107	BA0
M B BS#1	106	BA1
M B DQ0	5	DQ0
M B DQ1	7	DQ1
M B DQ2	17	DQ2
M B DQ3	19	DQ3
M B DQ4	4	DQ4
M B DQ5	6	DQ5
M B DQ6	14	DQ6
M B DQ7	16	DQ7
M B DQ8	23	DQ8
M B DQ9	25	DQ9
M B DQ10	35	DQ10
M B DQ11	37	DQ11
M B DQ12	20	DQ12
M B DQ13	22	DQ13
M B DQ14	36	DQ14
M B DQ15	38	DQ15
M B DQ16	43	DQ16
M B DQ17	45	DQ17
M B DQ18	55	DQ18
M B DQ19	57	DQ19
M B DQ20	44	DQ20
M B DQ21	46	DQ21
M B DQ22	58	DQ22
M B DQ23	58	DQ23
M B DQ24	61	DQ24
M B DQ25	63	DQ25
M B DQ26	73	DQ26
M B DQ27	75	DQ27
M B DQ28	62	DQ28
M B DQ29	64	DQ29
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M B DQ31	76	DQ31
M B DQ32	123	DQ32
M B DQ33	125	DQ33
M B DQ34	135	DQ34
M B DQ35	137	DQ35
M B DQ36	124	DQ36
M B DQ37	126	DQ37
M B DQ38	134	DQ38
M B DQ39	136	DQ39
M B DQ40	141	DQ40
M B DQ41	143	DQ41
M B DQ42	151	DQ42
M B DQ43	153	DQ43
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M B DQ45	142	DQ45
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M B DQ47	154	DQ47
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M B DQ60	180	DQ60
M B DQ61	182	DQ61
M B DQ62	192	DQ62
M B DQ63	194	DQ63
M B DQS#0	110	DQS0#
M B DQS#1	290	DQS1#
M B DQS#2	49	DQS2#
M B DQS#3	68	DQS3#
M B DQS#4	129	DQS4#
M B DQS#5	146	DQS5#
M B DQS#6	167	DQS6#
M B DQS#7	186	DQS7#
M B DQS0	13	DQS0
M B DQS1	31	DQS1
M B DQS2	51	DQS2
M B DQS3	70	DQS3
M B DQS4	131	DQS4
M B DQS5	148	DQS5
M B DQS6	169	DQS6
M B DQS7	188	DQS7
M ODT2	114	ODT0
M ODT3	119	ODT1
VREF	1	VREF
VSS	2	VSS
NP1	NP1	NP1
NP2	NP2	NP2

Height 1mm



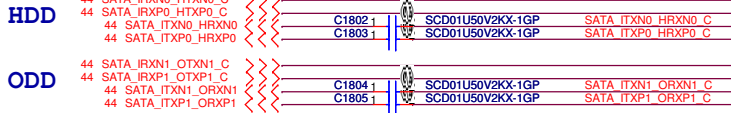
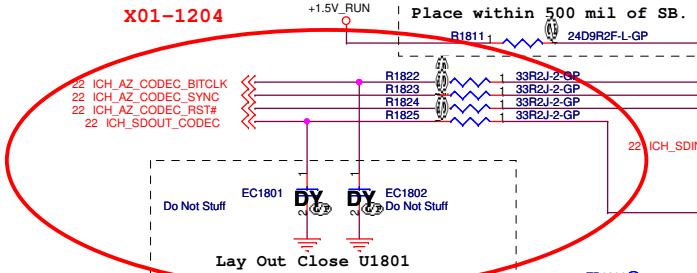
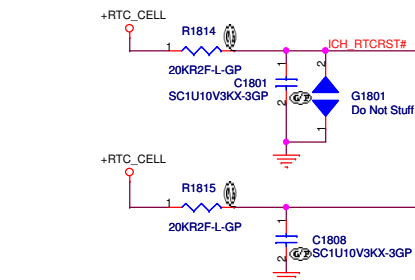
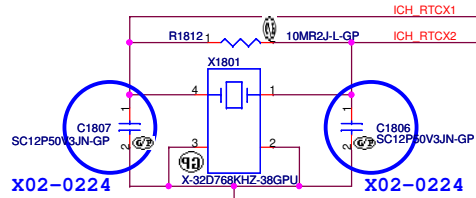
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Title: **DDR2-SODIMM SLOT2**

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Custom	Alba UMA	-1
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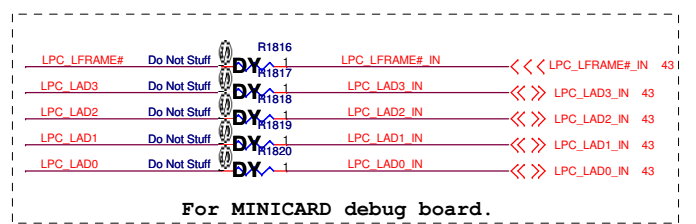
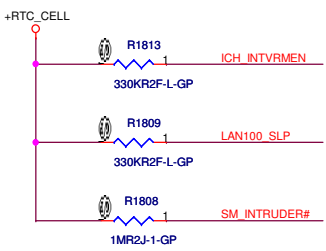
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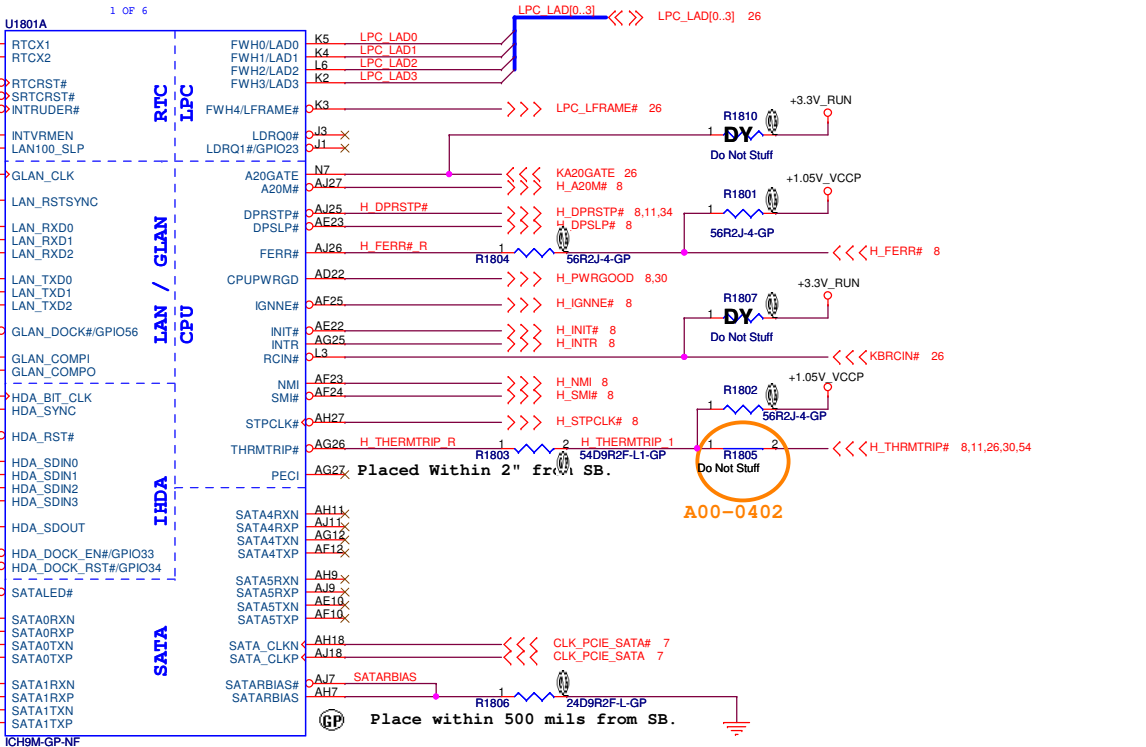
HDD

ODD

integrated VccSus1_05,VccSus1_5,VccCL1_5	
INTVRMEN	High=Enable Low=Disable
integrated VccLan1_05VccCL1_05	
LAN100_SLP	High=Enable Low=Disable



For MINICARD debug board.



Alba UMA

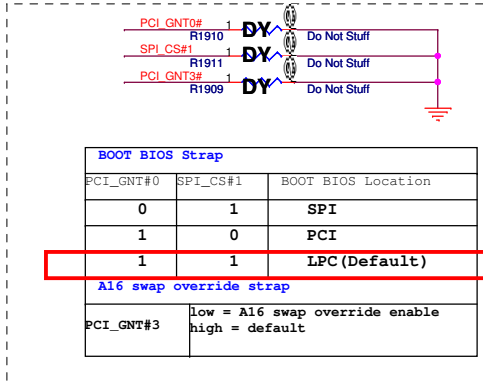
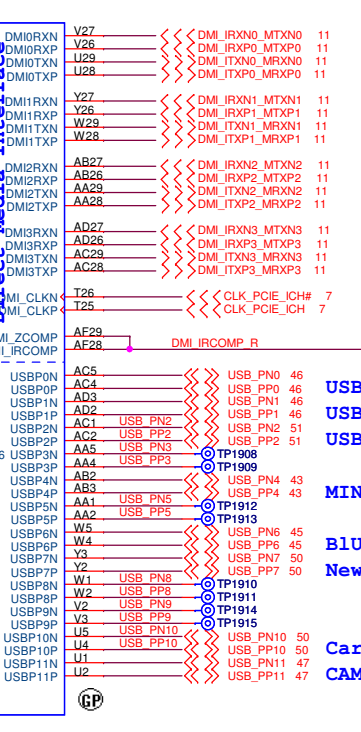
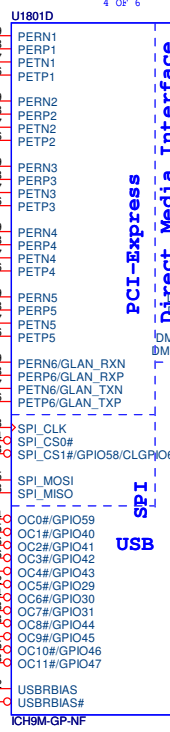
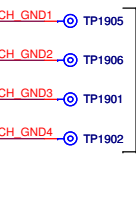
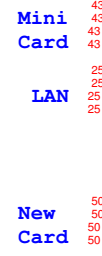
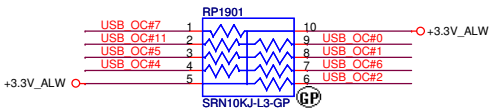
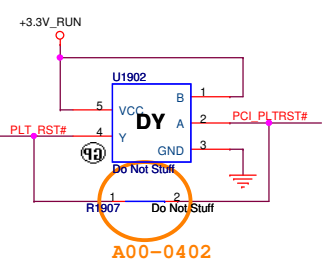
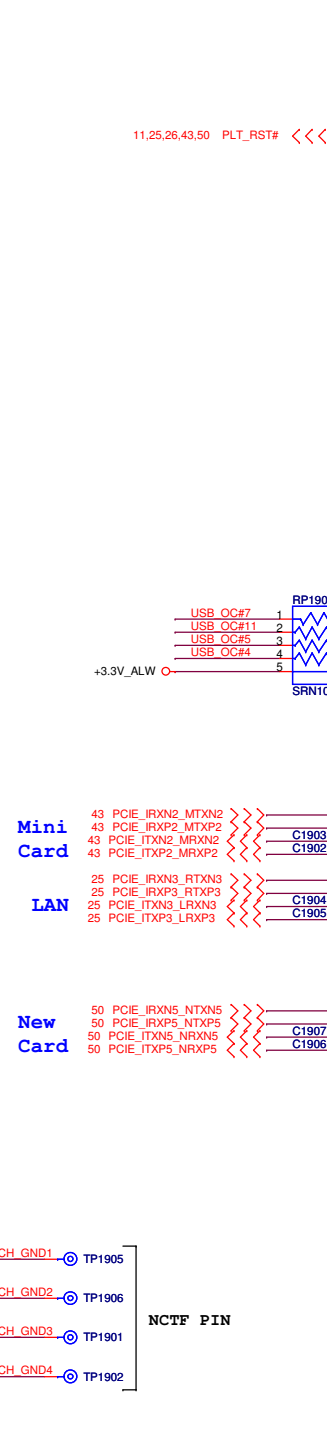
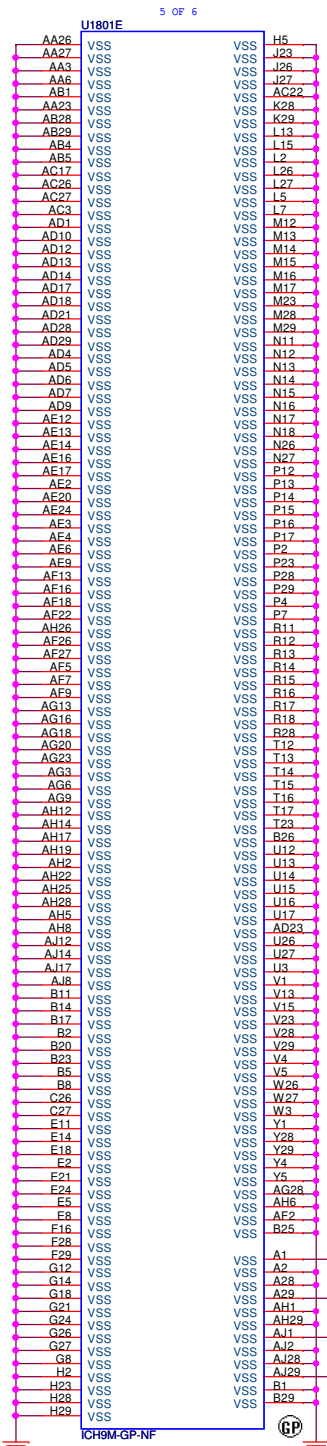
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Title: **ICH9-LAN/HDA/SATA/LPC(1/4)**

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Date: Monday, April 06, 2009 Sheet 18 of 61

SSID = ICH



USB Pair	Device
0	USB1
1	USB2
2	USB3
3	RESERVED
4	MINI CARD
5	RESERVED
6	BLUETOOTH
7	NEW CARD
8	RESERVED
9	RESERVED
10	Card Reader
11	CAMERA

Alba UMA

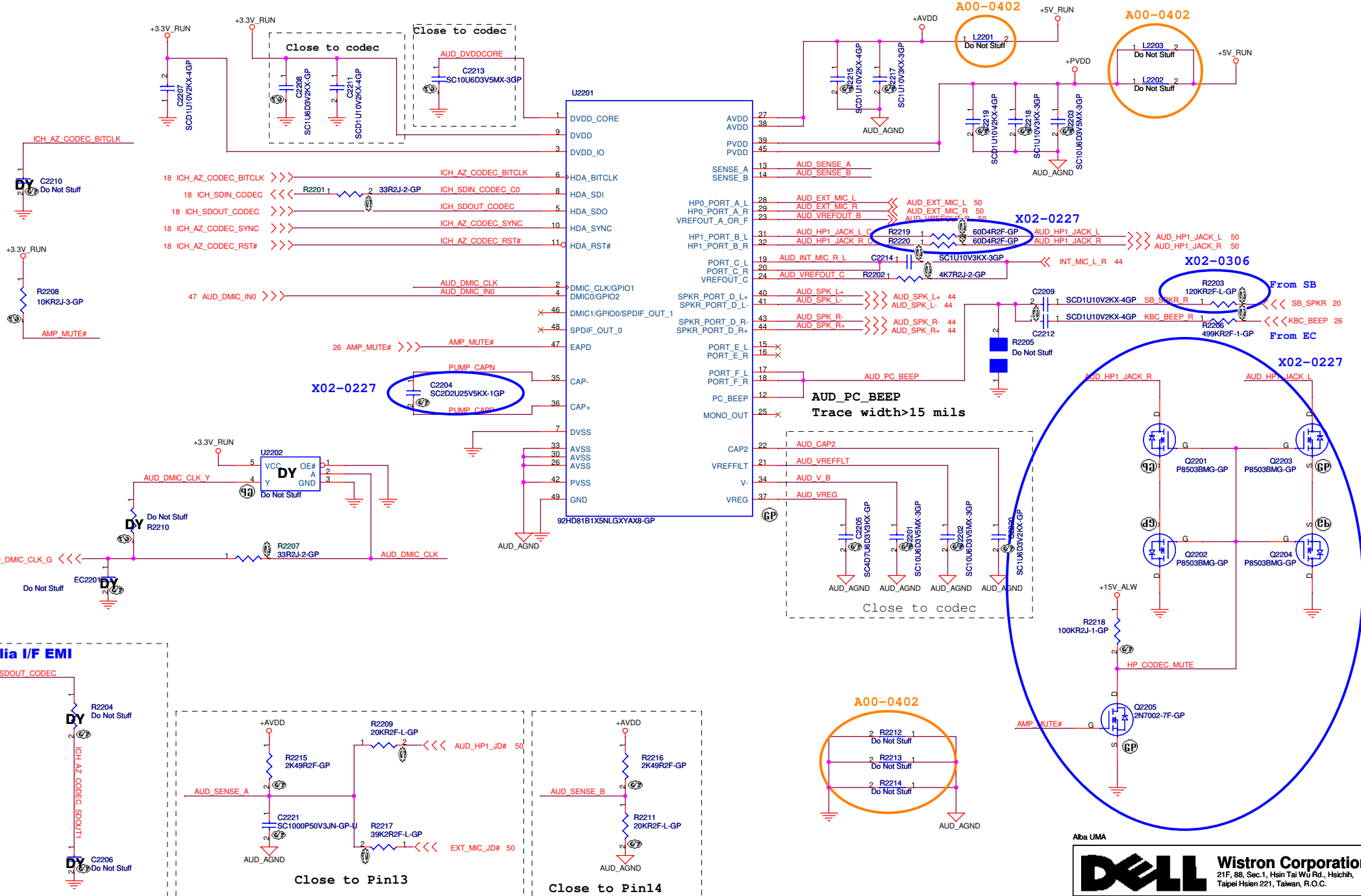
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Model: **ICH9-PCI/PCIE/DMI/USB/GND(2/4)**

Size: Custom Document Number
Date: Monday, April 06, 2009


Alba UMA
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SSID = AUDIO




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Alba UMA

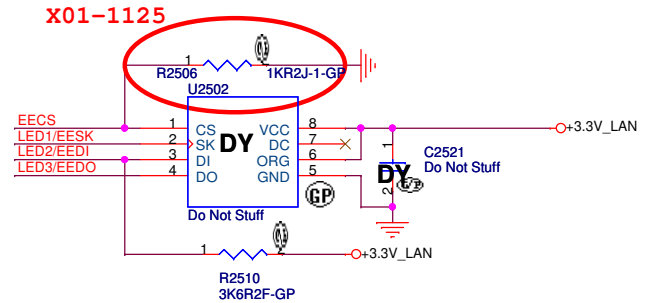
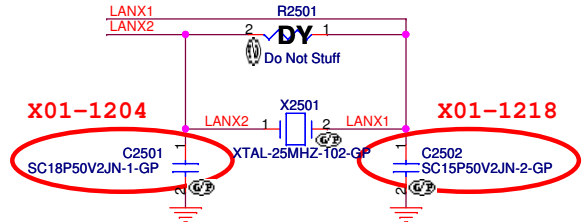
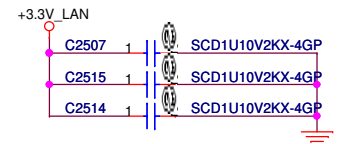
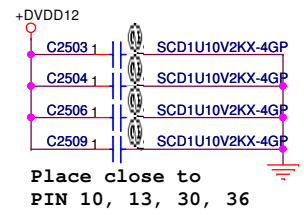
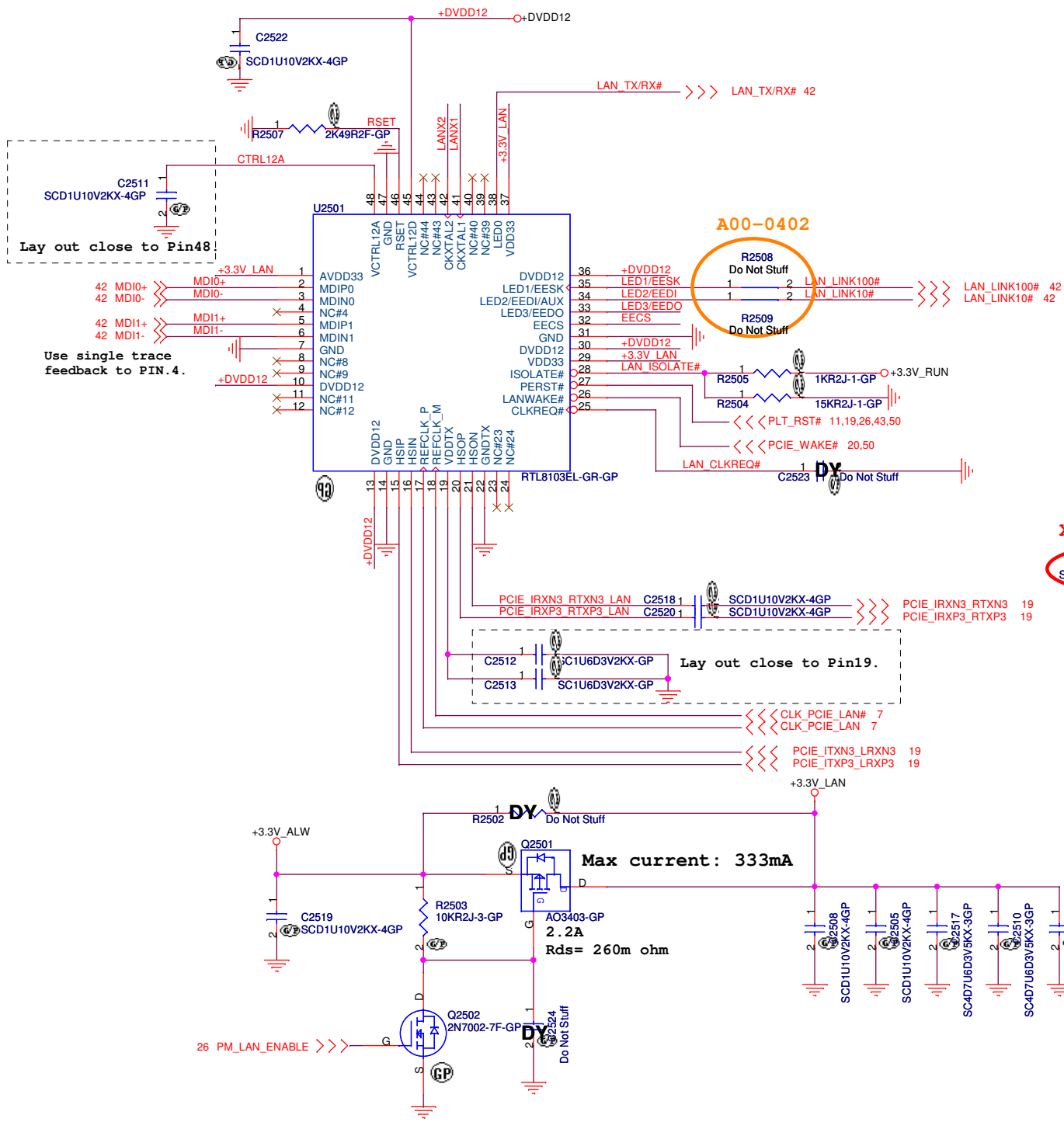
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Size	Document Number				Rev
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SSID = LOM



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Title: **LAN Realtek-RTL8102EL**

Size	Document Number	Rev
Custom		-1

Date: Monday, April 06, 2009 Sheet 25 of 61

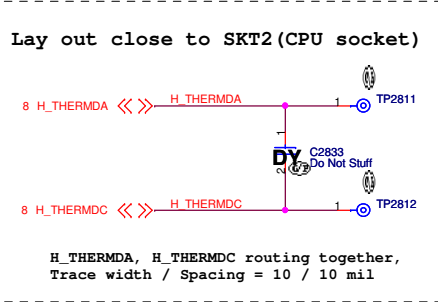
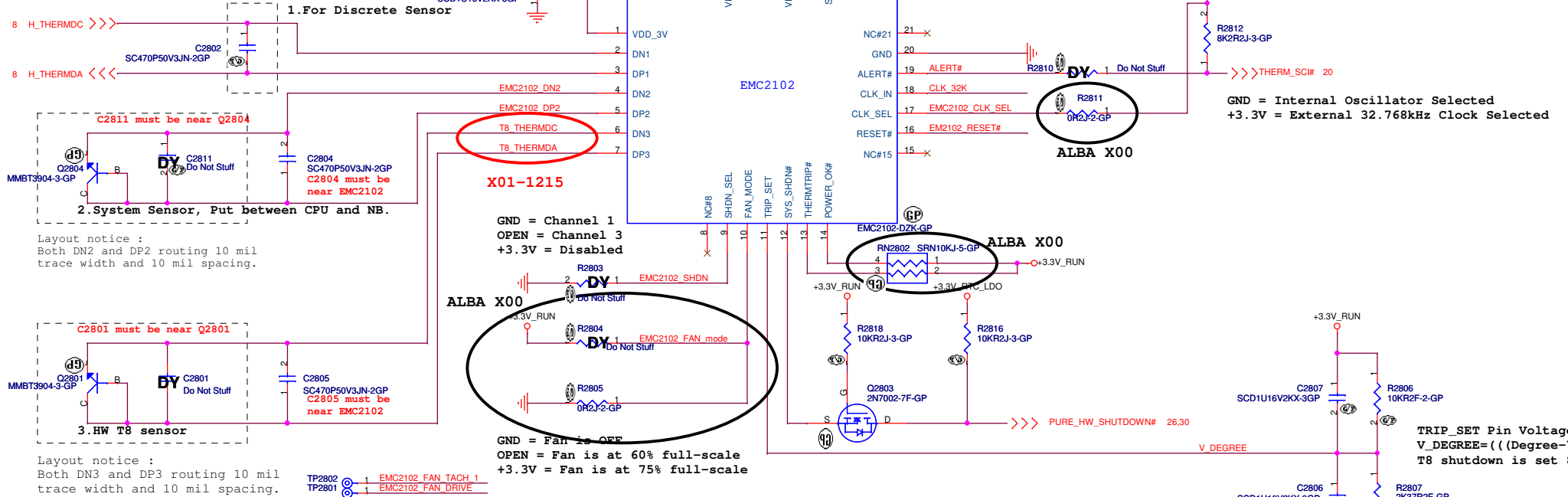
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Alba UMA

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Title					
(Reserve)					
Size	Document Number				Rev
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Date: Monday, April 06, 2009					
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SSID = Thermal

Layout notice :
Both VGA_THERMDA and THERMDC routing
10 mil trace width and 10 mil spacing.



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Title: **Thermal/Fan Controller EMC2102**

Size: Custom
Document Number: **Alba UMA**
Rev: -1

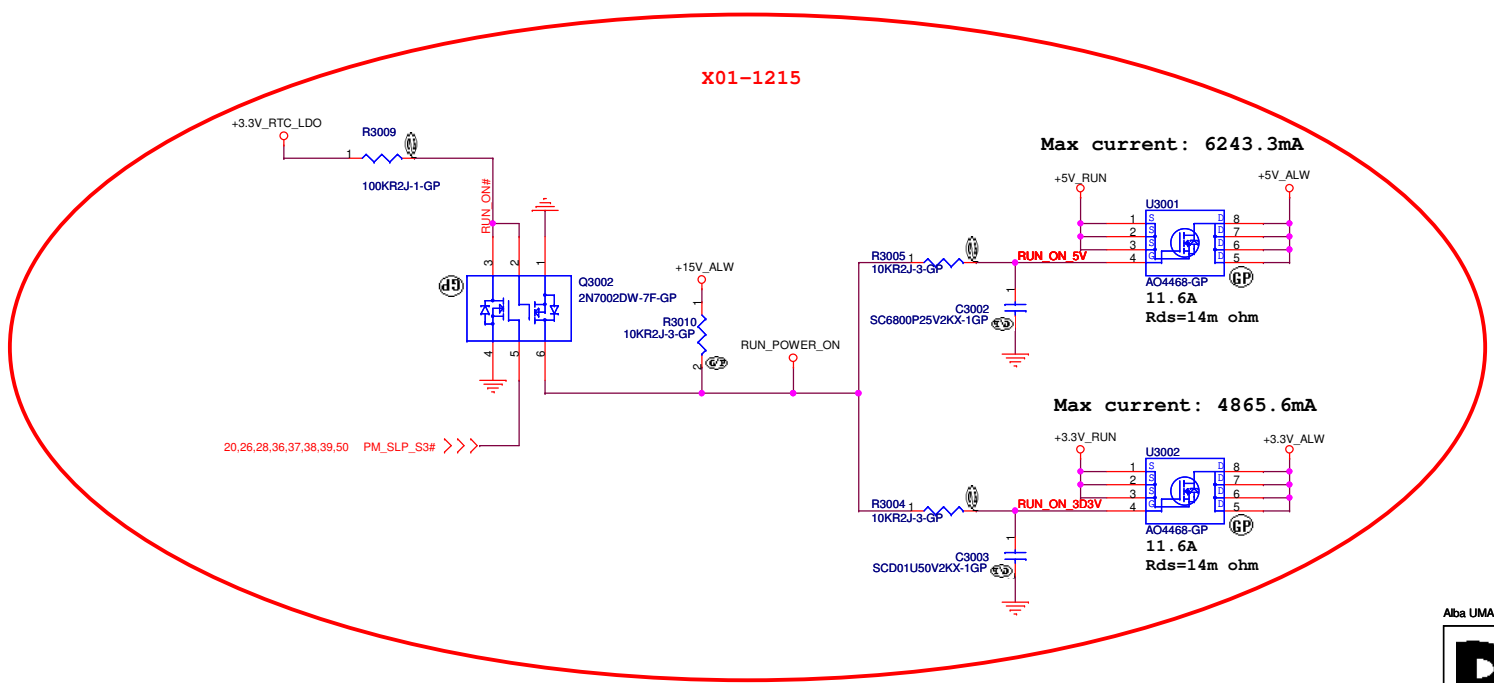
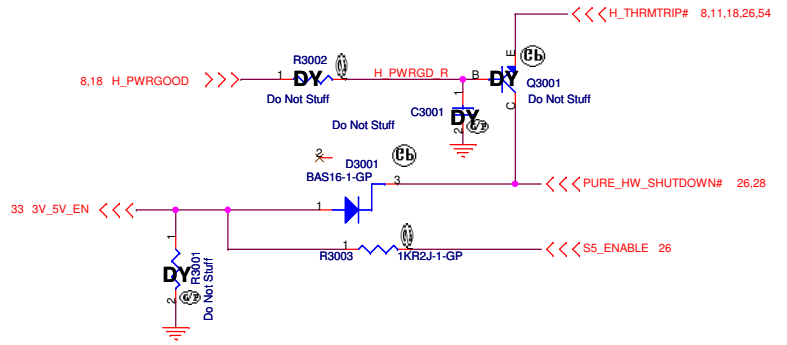
Date: Monday, April 06, 2009 Sheet 28 of 61

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Alba UMA

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Title			(Reserve)
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Custom	Alba UMA	-1	
Date: Monday, April 06, 2009			Sheet 29 of 61

SSID = Reset . Suspend



SSID = Charger

Adaptor In Soft-Start Circuit

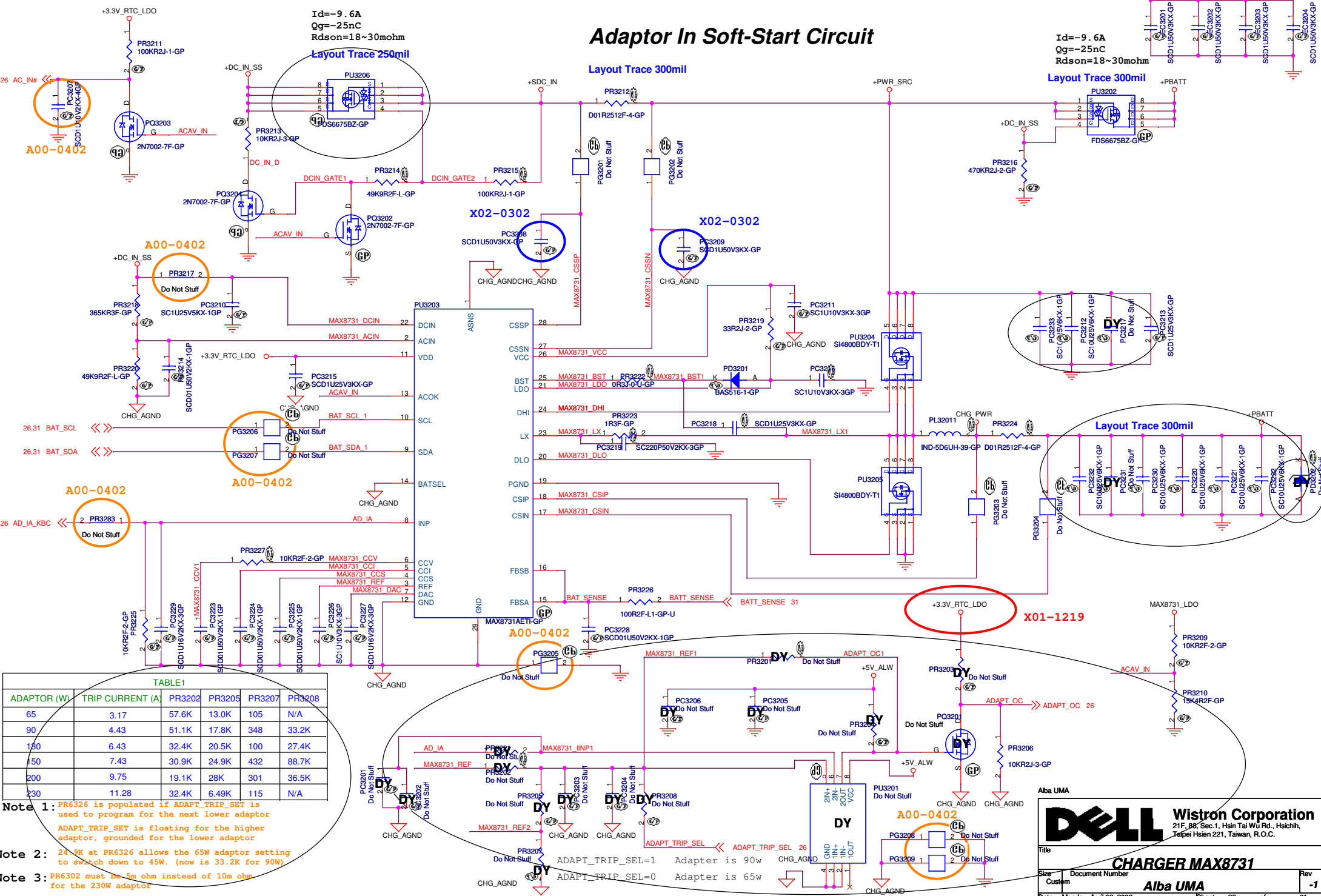


TABLE 1

ADAPTOR (W)	TRIP CURRENT (A)	PR3202	PR3205	PR3207	PR3208
65	3.17	57.6K	13.0K	105	N/A
90	4.43	51.1K	17.8K	348	33.2K
150	6.43	32.4K	20.5K	100	27.4K
150	7.43	30.9K	24.9K	432	88.7K
200	9.75	19.1K	28K	301	36.5K
230	11.28	32.4K	6.49K	115	N/A

Note 1: PR6326 is populated if ADAPT_TRIP_SET is used to program for the next lower adaptor. ADAPT_TRIP_SET is floating for the higher adaptor, grounded for the lower adaptor.

Note 2: 24.9K at PR6326 allows the 65W adaptor setting to switch down to 45W. (now is 33.2K for 90W)

Note 3: PR6302 must be 5m ohm instead of 10m ohm for the 230W adaptor.

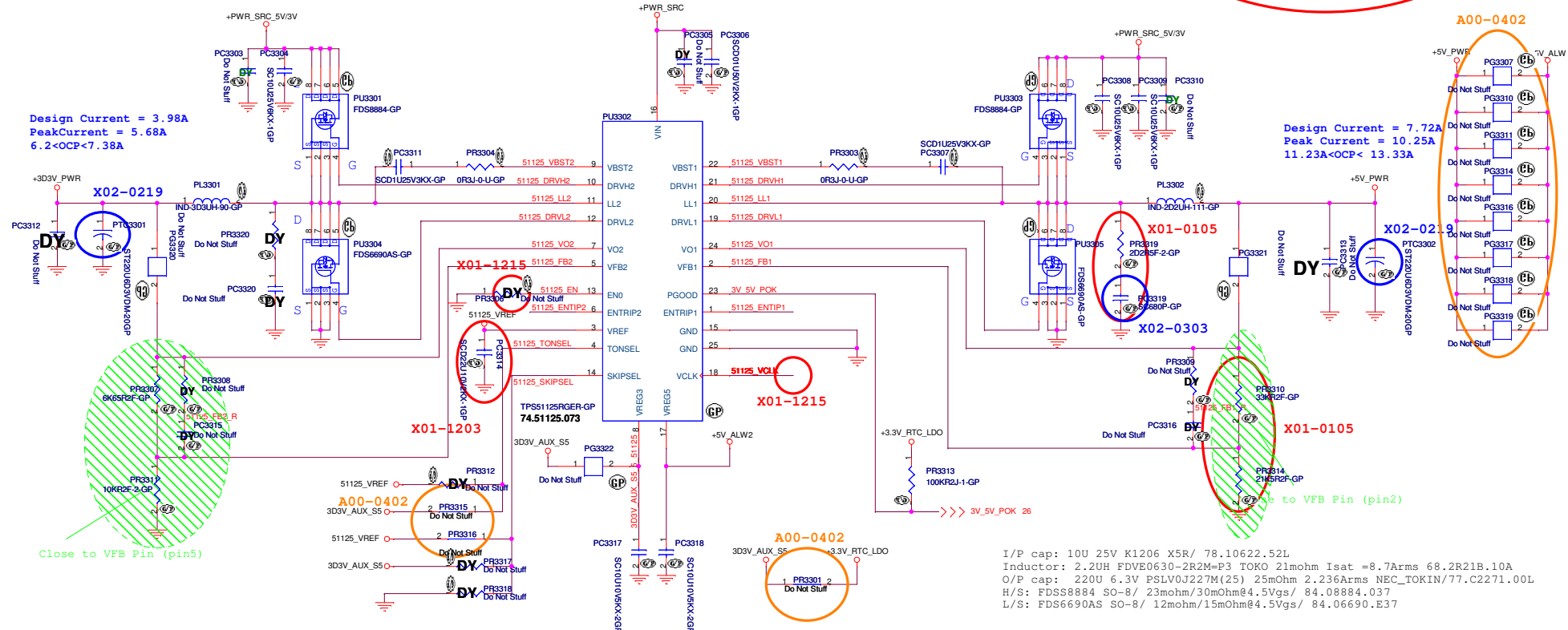
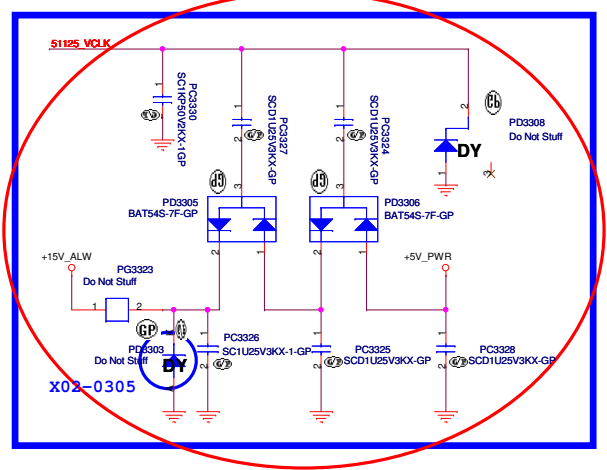
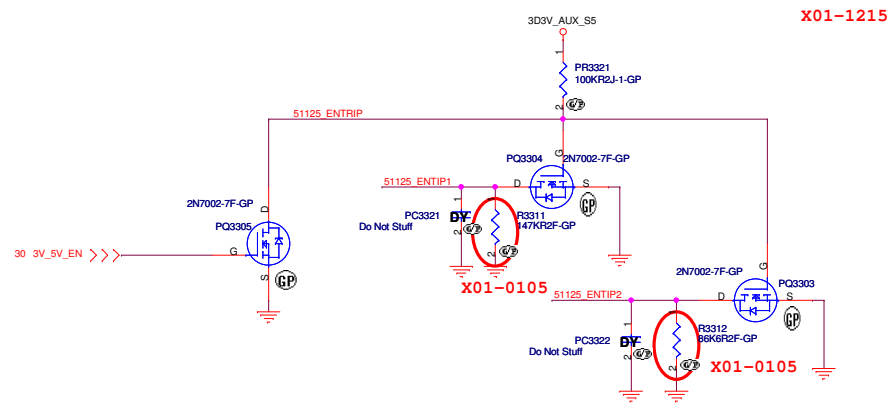
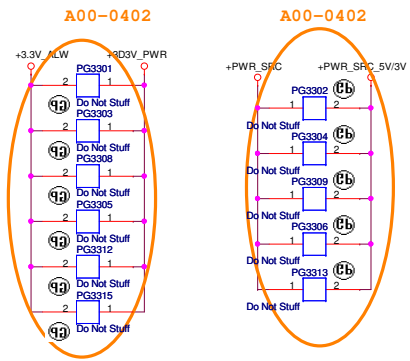
Alba UMA

Wistron Corporation
21F, B8, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CHARGER MAX8731**

Size: Custom Document Number: Alba UMA

Date: Monday, April 06, 2009 Sheet 32 of 61



Design Current = 3.98A
Peak Current = 5.68A
6.2<OCP<7.38A

Design Current = 7.22A
Peak Current = 10.25A
11.23A<OCP<13.33A

Close to VFB Pin (pin5)

Close to VFB Pin (pin2)

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 3.3UH FDV0630-3R3M=P3 TOKO 31mohm Isat =6.9Arms 68.3R31A.10A
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
H/S: FDS8884 SO-8/ 23mohm/30mOhm@4.5Vgs/ 84.08884.037
L/S: FDS6690AS SO-8/ 12mohm/15mOhm@4.5Vgs/ 84.06690.E37

Pin	CH1	CH2	SKIPSEL	VREG3 or VREG5	VREF (2V)	GND
TONSEL						
GND	200kHz	265kHz	Operating Mode	OOA Auto Skip	Auto Skip	PWM only
VREF	245kHz	305kHz				
VREG3	300kHz	375kHz				
VREG5	365kHz	460kHz				

EN0	Operating Mode	VCLK	VREG
Open	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	820kΩ to GND

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 2.2UH FDVE0630-2R2M=P3 TOKO 21mohm Isat =8.7Arms 68.2R21B.10A
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
H/S: FDS8884 SO-8/ 23mohm/30mOhm@4.5Vgs/ 84.08884.037
L/S: FDS6690AS SO-8/ 12mohm/15mOhm@4.5Vgs/ 84.06690.E37

Alba UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsieh, Taipei Hsien 221, Taiwan, R.O.C.

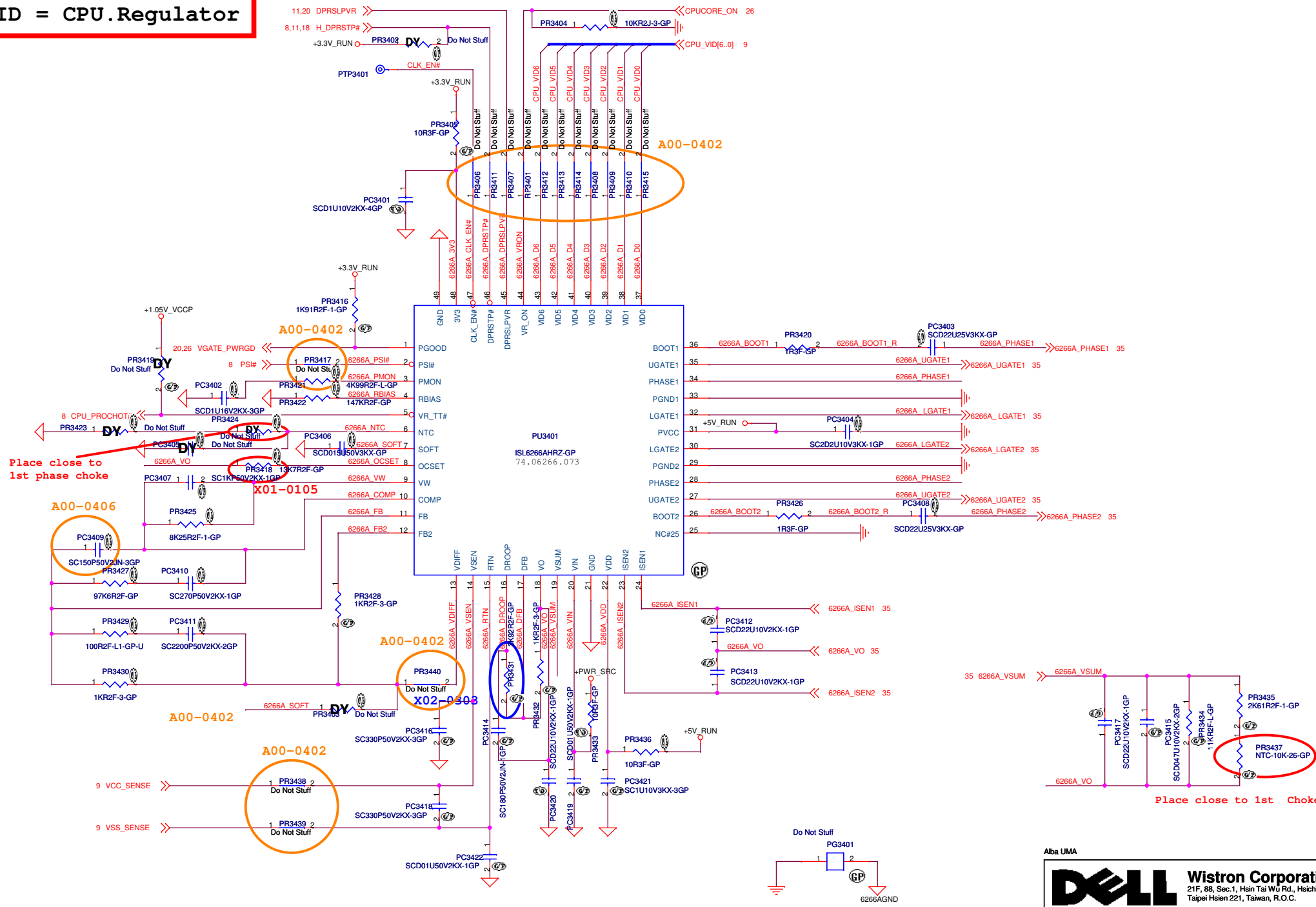
Title: **DCDC 5V/3D3V (TPS51125)**

Size: Custom Document Number


Date: Monday, April 06, 2009

Sheet 33 of 61

SSID = CPU.Regulator



Alba UMA



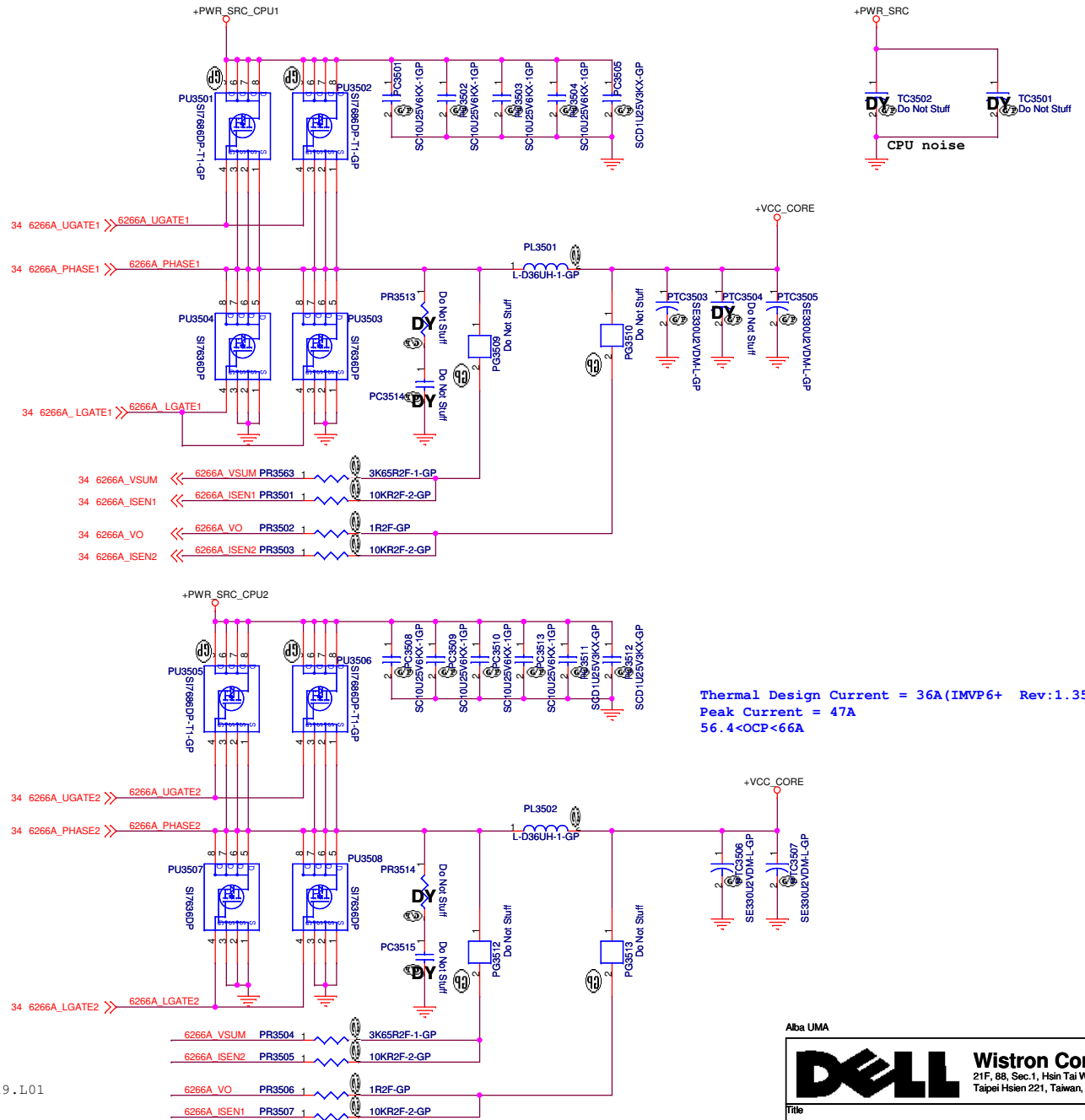
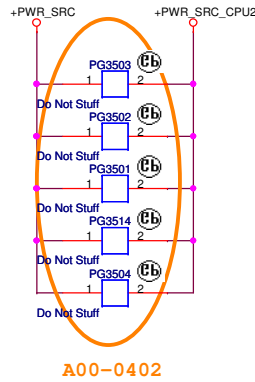
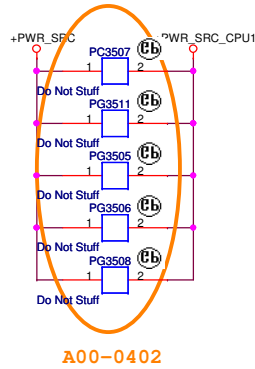
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU VCORE POWER(1/2)**

Size: Custom	Document Number: Alba UMA	Rev: -1
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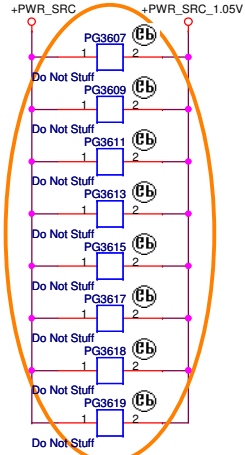
Date: Monday, April 06, 2009 Sheet 34 of 61

SSID = CPU.Regulator



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
 Inductor: 0.36UH ETQP4LR36WFC PANASONIC 1.1mohm
 O/P cap: 330U 2V EEF5X0D331ER 9mOhm 3.0Arms Panasonic/79.33719.L01
 H/S: SI7686DP/ POWERPAK-8/ 14mOhm/ 4.5Vgs/ 84.07686.037
 L/S: SI7636ADP/ POWERPAK-8/ 4.8mOhm/ 4.5Vgs/ 84.07636.037

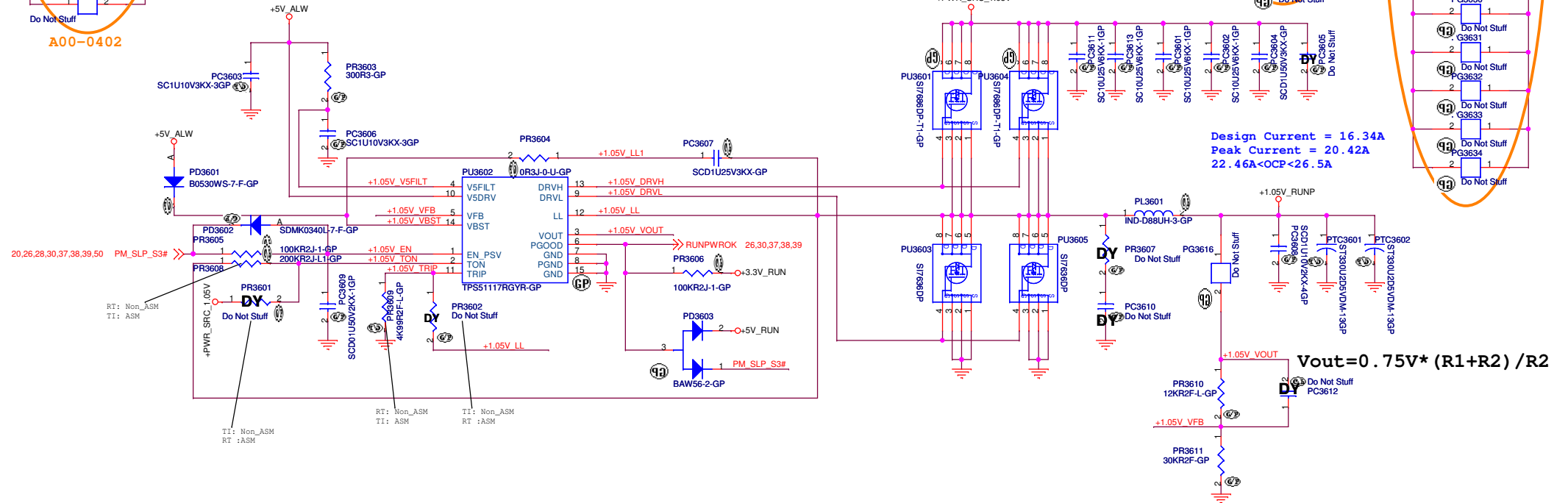
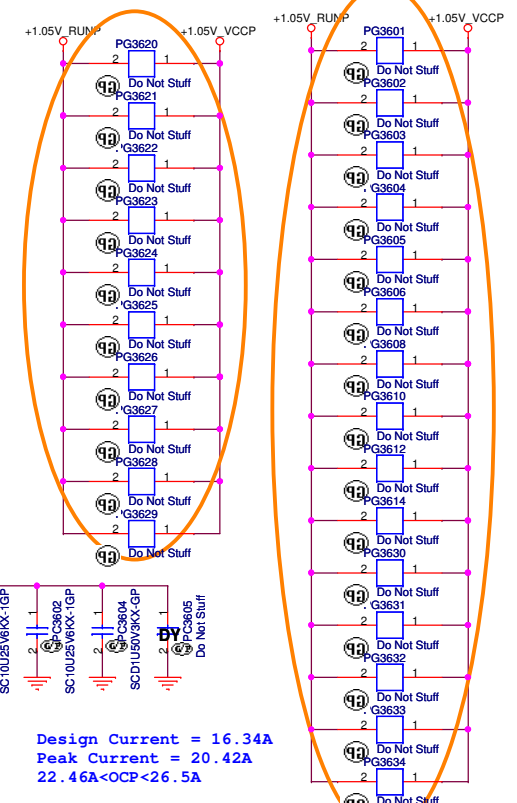
SSID = PWR.Plane.Regulator_lp05v



A00-0402

A00-0402

A00-0402



Design Current = 16.34A
Peak Current = 20.42A
22.46A < OCP < 26.5A

$$V_{out} = 0.75V \cdot (R1+R2) / R2$$

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.88UH FDU1040D-R88M=P3 TOKO DCR:2.3mohm Isat =22.2Arms 68.R8810.10B
O/P cap: 330U 2.5V PSLV0E337M(15) 15mOhm 2.886Arms NEC_TOKIN/ 77.C3371.10L
H/S: SI7686DP/ POWERPAK-8/ 14mOhm/ 4.5Vgs/ 84.07686.037
L/S: SI7636ADP/ POWERPAK-8/ 4.8mOhm/ 4.5Vgs/ 84.07636.037
Switching freq-->350KHz

Alba UMA

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **DC to DC 1.05V**

Size Custom	Document Number Alba UMA	Rev -1
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Date: Monday, April 06, 2009 Sheet 36 of 61

SSID = PWR.Plane.Regulator_1p5v/1p1v

Vendor	PIN6	PIN11	PIN20
L6935	VBIAS	N.C.	SS
RTXX35	N.C.	VBIAS	N.C.

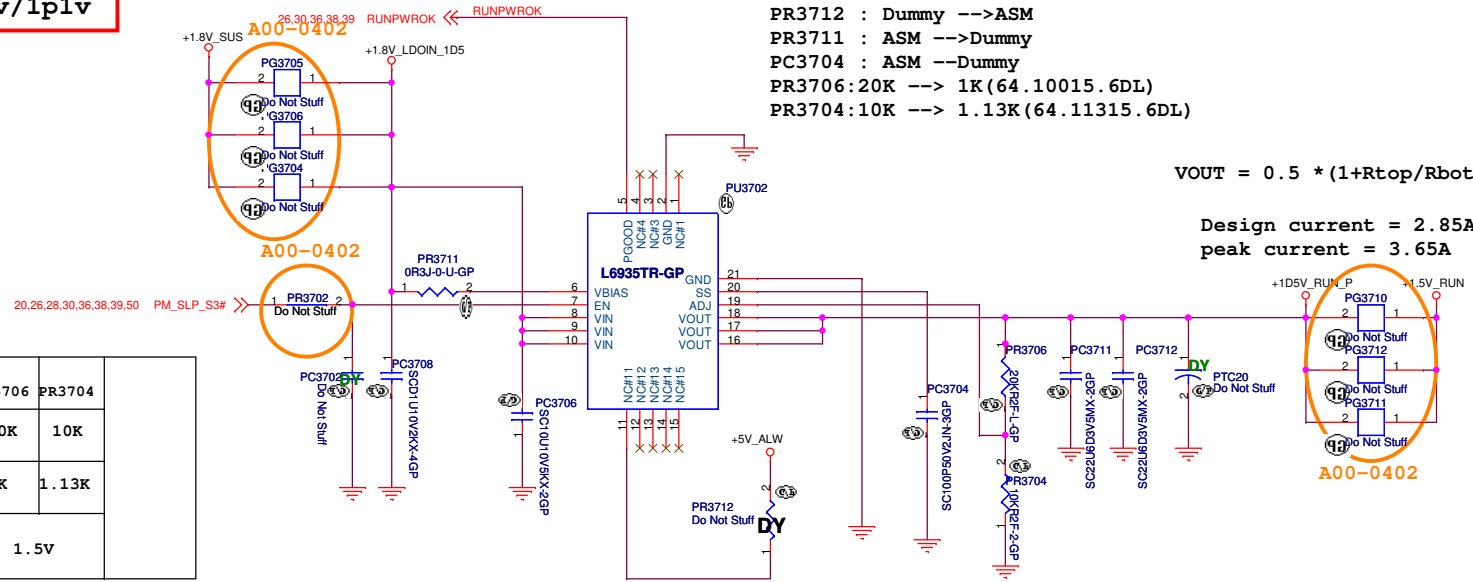
Vendor	PR3712	PR3711	PR3706	PR3704
L6935	DY	ASM	20K	10K
RTXX35	ASM	DY	1K	1.13K
			1.5V	

2nd Source BOM Control:

- PR3712 : Dummy -->ASM
- PR3711 : ASM -->Dummy
- PC3704 : ASM --Dummy
- PR3706:20K --> 1K(64.10015.6DL)
- PR3704:10K --> 1.13K(64.11315.6DL)

$$V_{OUT} = 0.5 * (1 + R_{top}/R_{bot})$$

Design current = 2.85A
peak current = 3.65A

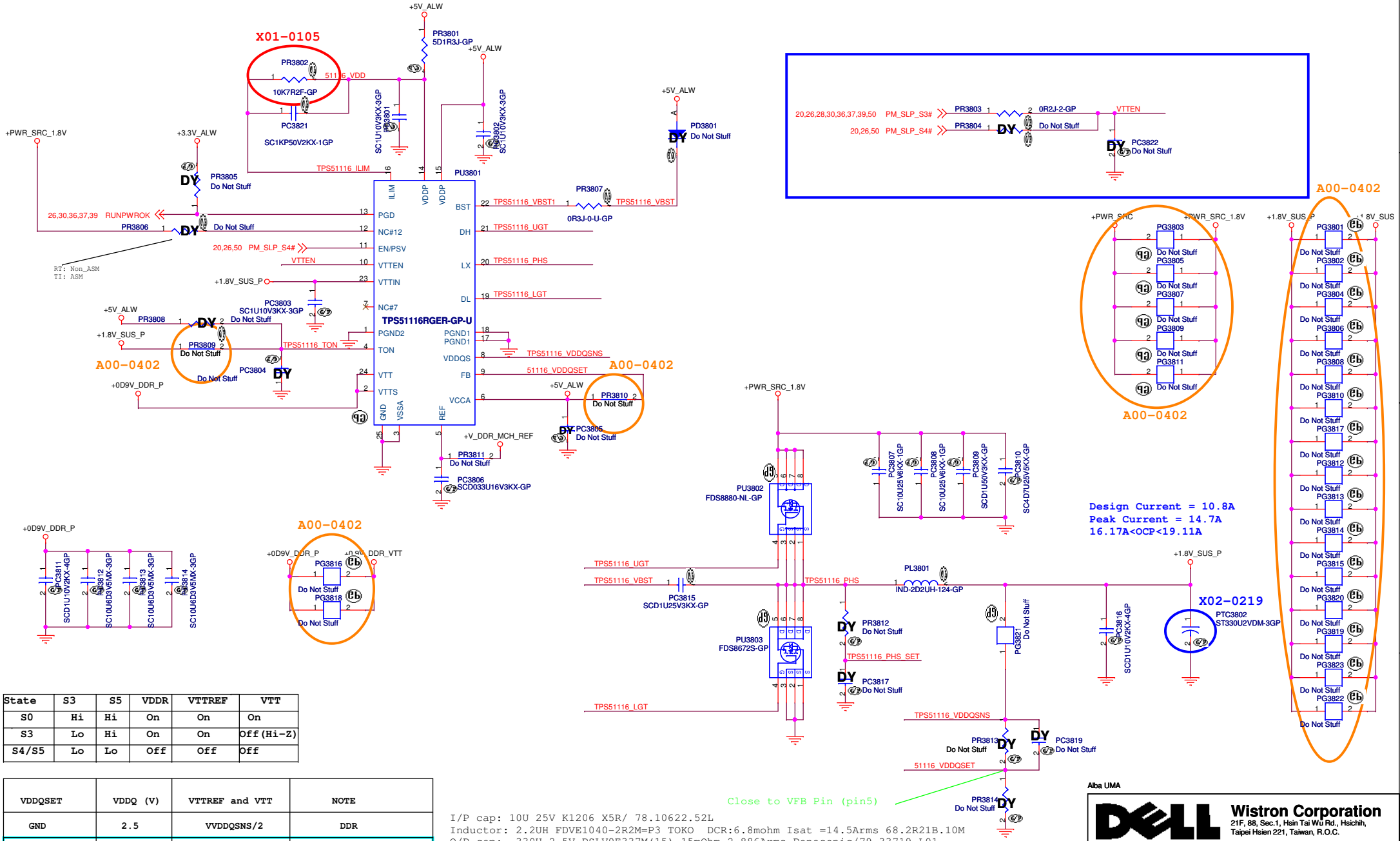


Alba UMA

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Title DC to DC L6935 1.5V / L6935 1.1V	
Size	Document Number	Rev	
Custom	Alba UMA	-1	
Date:	Monday, April 06, 2009	Sheet	37 of 61

SSID = PWR.Plane.Regulator_1p8v0p9v

TI TPS51116 for 1.8V and 0.9V



Design Current = 10.8A
Peak Current = 14.7A
16.17A < OCP < 19.11A

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 2.2UH FDVE1040-2R2M=P3 TOKO DCR:6.8mohm Isat =14.5Arms 68.2R21B.10M
O/P cap: 330U 2.5V PSLV0E337M(15) 15mOhm 2.886Arms Panasonic/79.33719.L01
H/S: FDS8880 SO-8/ 9.6mOhm/12mOhm @4.5Vgs/ 84.08880.037
L/S: FDS8672S SO-8/ 5.3mOhm/7.0mOhm@4.5Vgs/ 84.08672.A3784.07636.037

Alba UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.


Title: **DC to DC 1.8V/0.9V**

Size Custom	Document Number	Rev -1
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Date: Monday, April 06, 2009 Sheet 38 of 61

SSID = PWR.Plane.Regulator_gfx

Altair® Design

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		VGA_CORE	
Size	Document Number	Rev	
A3	Alba UMA	-1	
Date: Monday, April 06, 2009	Sheet 39	of	61

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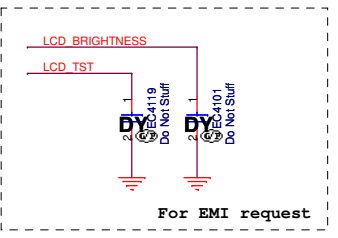
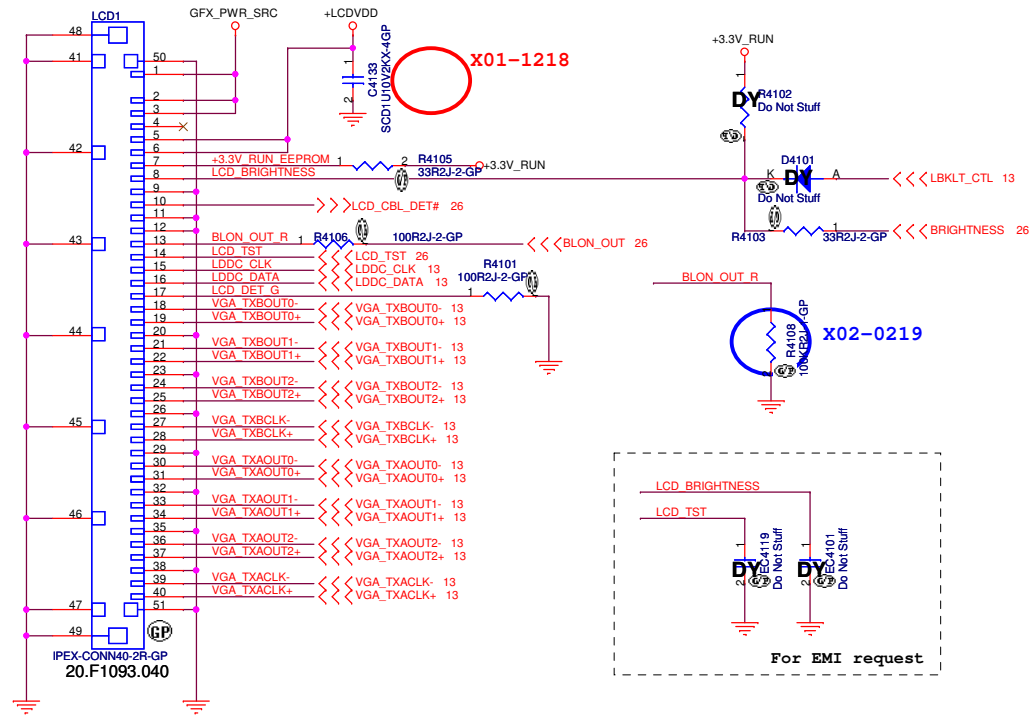
Alba UMA

	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
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Title		
(Reserve)		
Size	Document Number	Rev
Custom	Alba UMA	-1
Date: Monday, April 06, 2009		
Sheet 40 of 61		

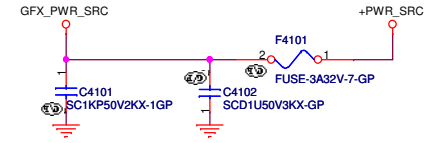
SSID = VIDEO

LVDS CONNECTOR

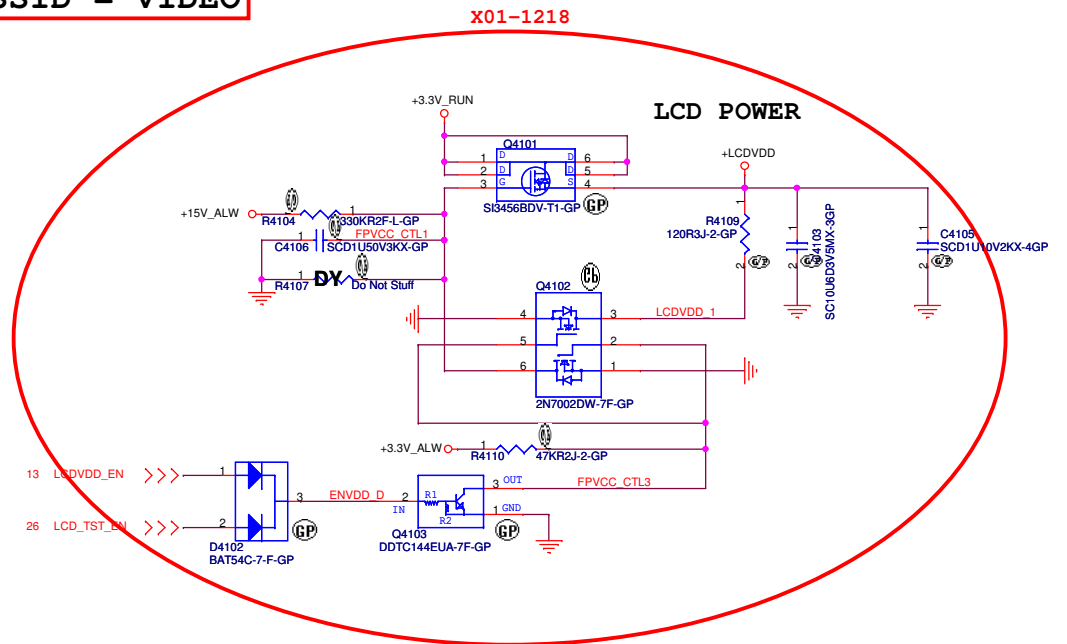


SSID = Inverter

INVERTER POWER



SSID = VIDEO



Aba UMA

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **LCD/Inverter Connector**

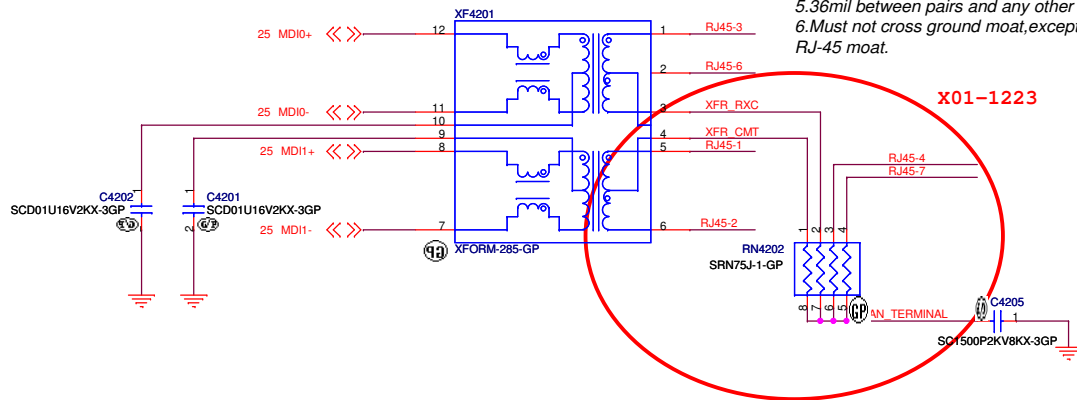
Size: Document Number
Custom: **Aba UMA**

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Rev: -1

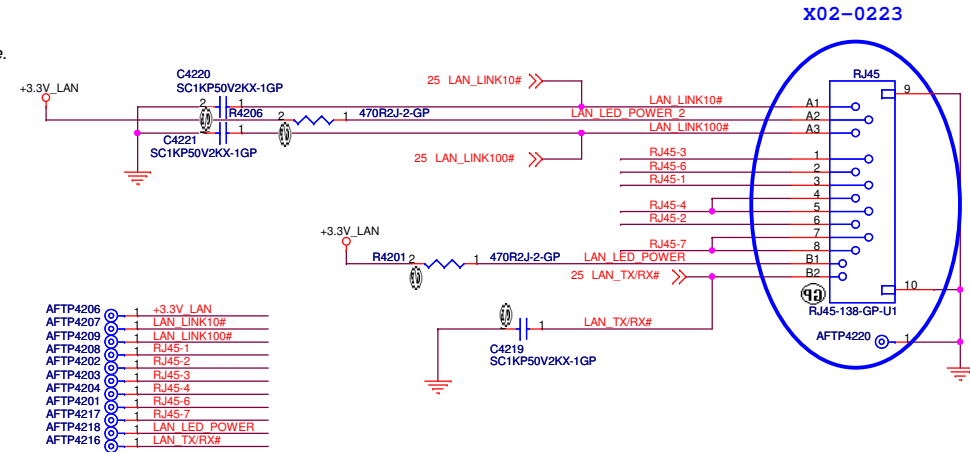
SSID = LOM

10/100M Lan Transformer



1. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
2. No vias, No 90 degree bends.
3. pairs must be equal lengths.
4. 6mil trace width, 12mil separation.
5. 36mil between pairs and any other trace.
6. Must not cross ground moat, except RJ-45 moat.

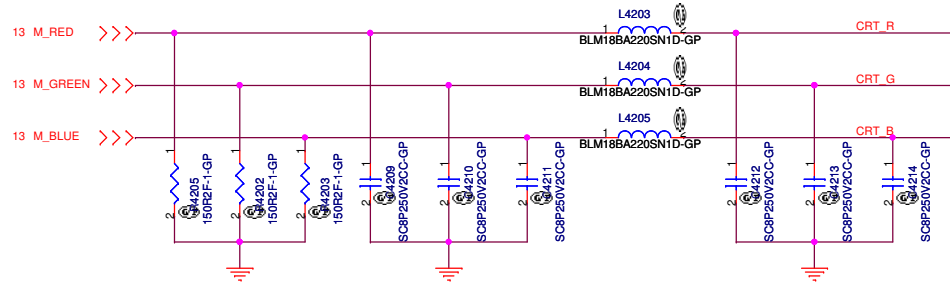
RJ45 Connector



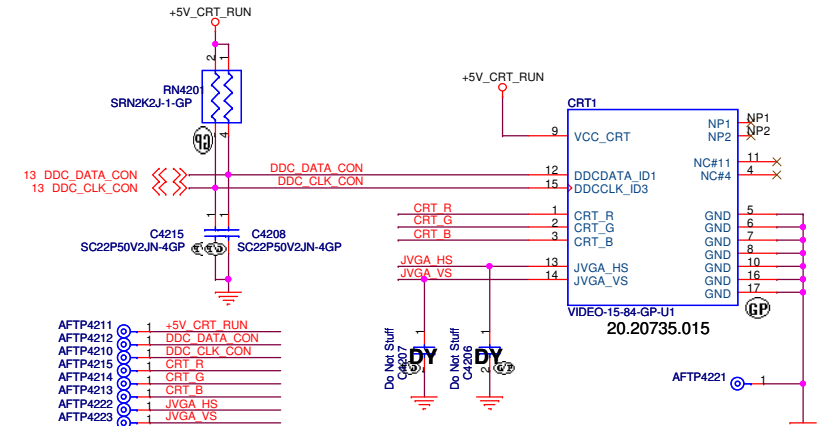
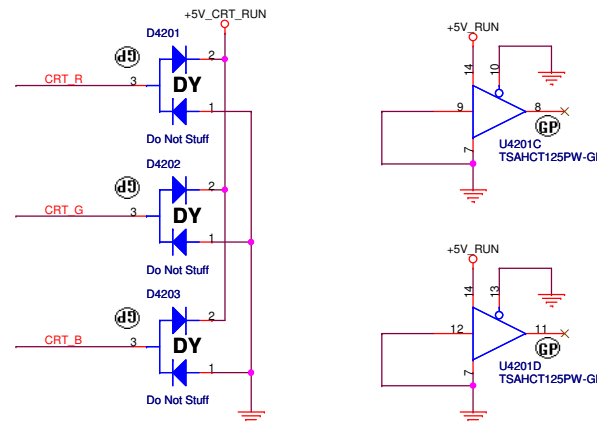
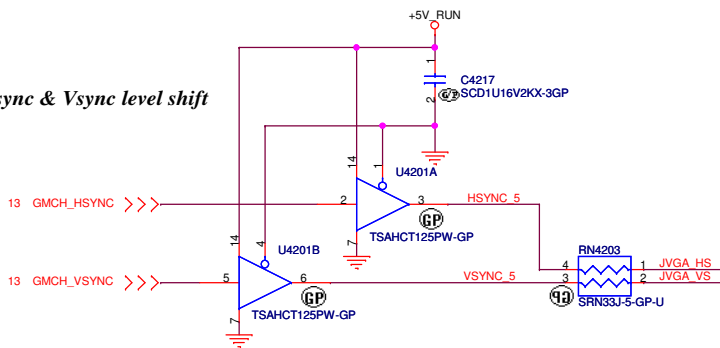
SSID = VIDEO

Layout Note:

- *Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
- * RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.

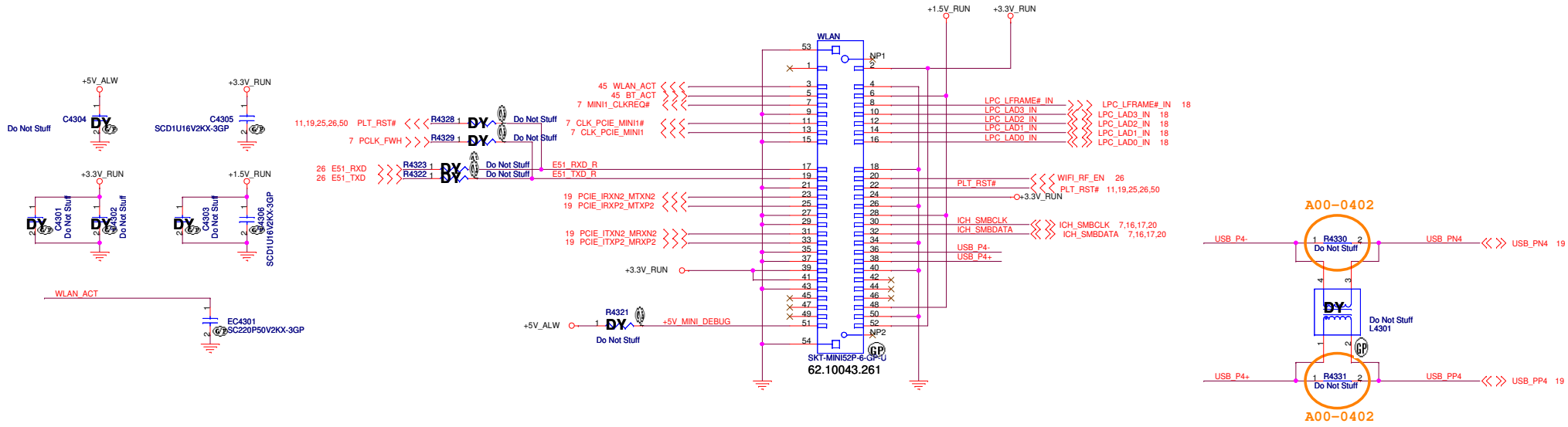


Hsync & Vsync level shift



SSID = Wireless

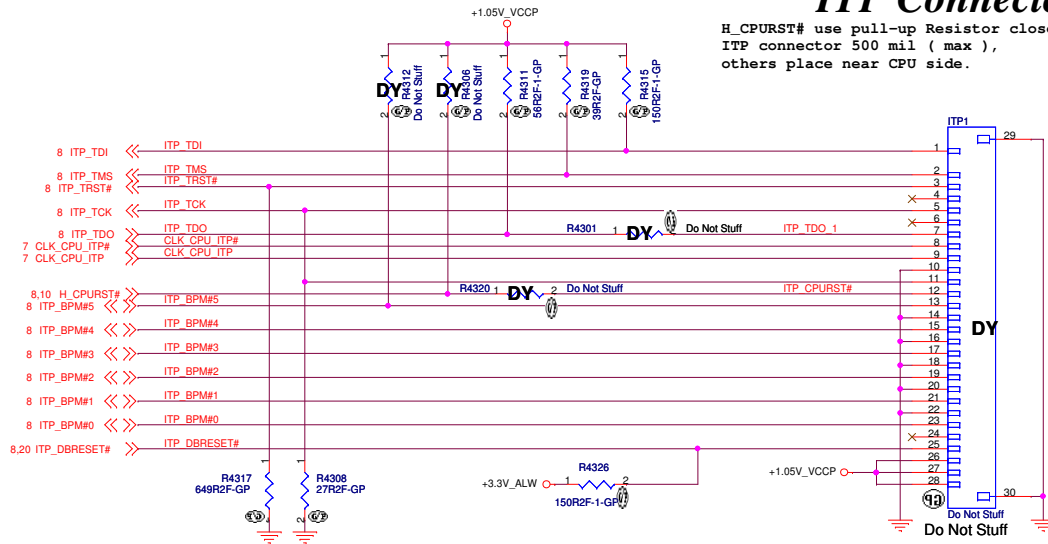
Mini Card Connector(802.11a/b/g/n)



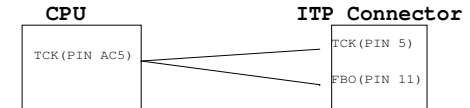
SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close ITP connector 500 mil (max), others place near CPU side.

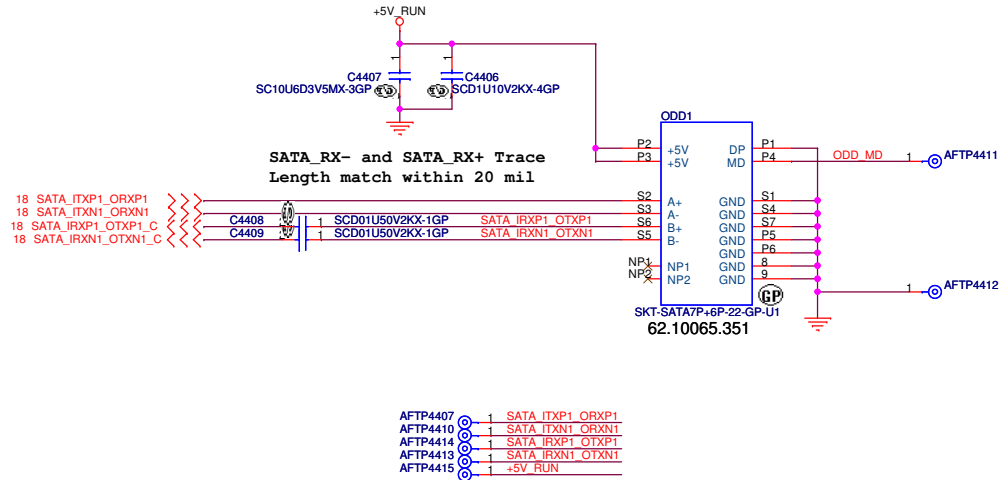


+1.05V_VCCP use Decoupling Capacitor close ITP connector 100 mil (max)



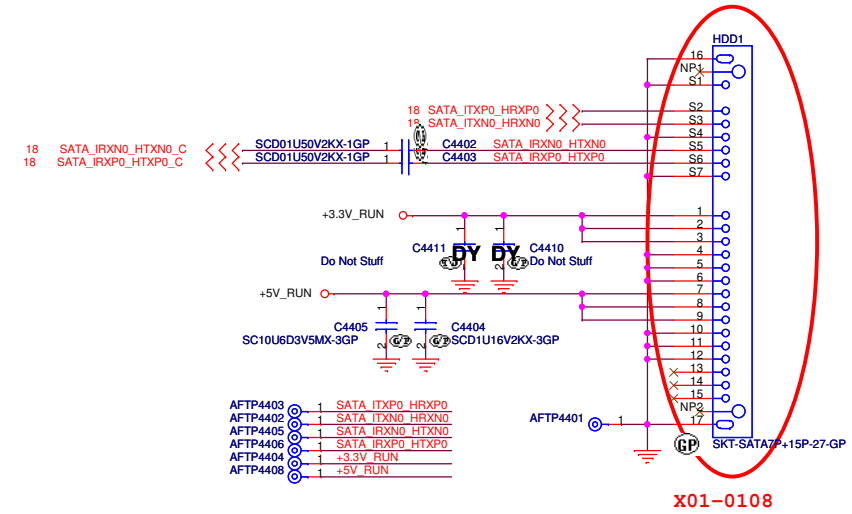
SSID = SATA

ODD Connector



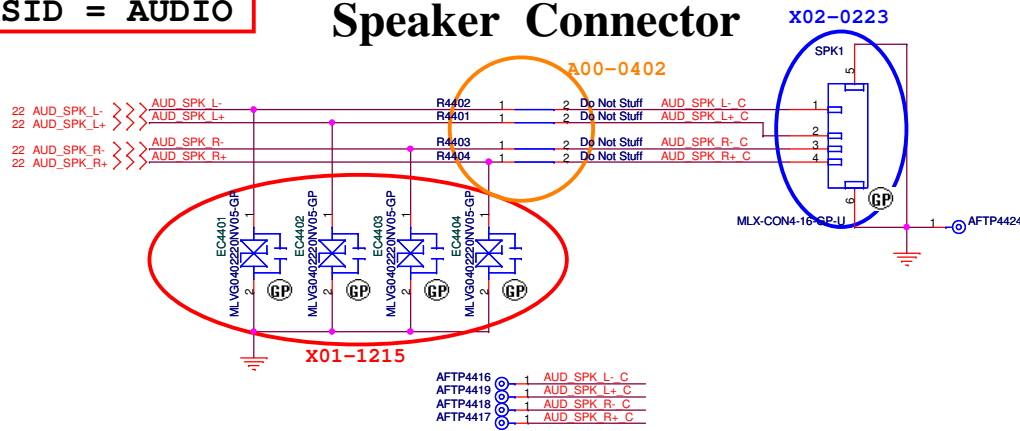
SSID = SATA

SATA HDD Connector



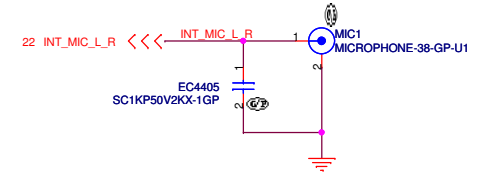
SSID = AUDIO

Speaker Connector



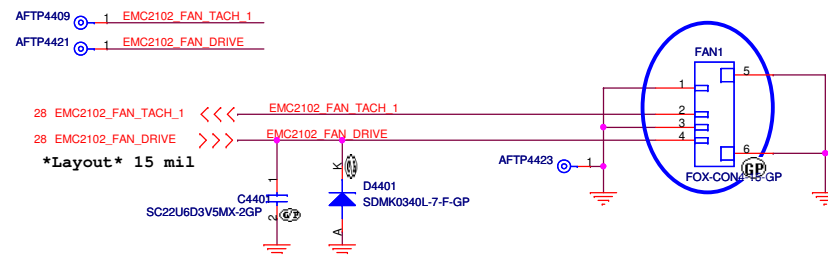
SSID = AUDIO

Internal MIC



SSID = Thermal

Fan Connector

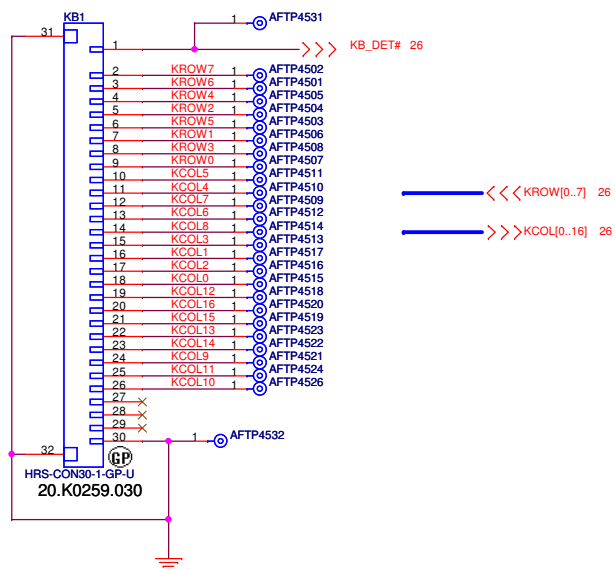


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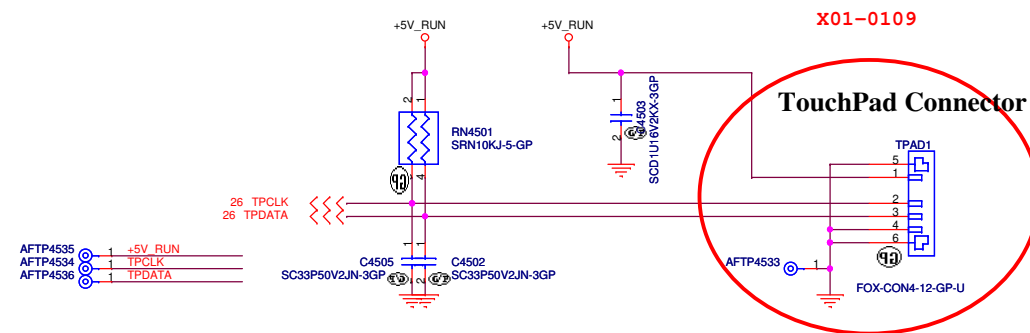


SSID = KBC

Internal KeyBoard Connector

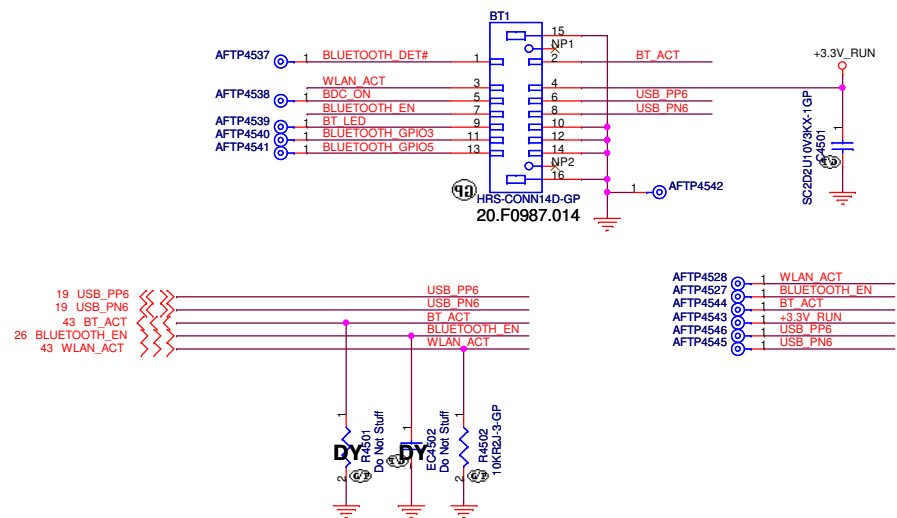


SSID = Touch.Pad



SSID = User.Interface

Bluetooth Module conn.



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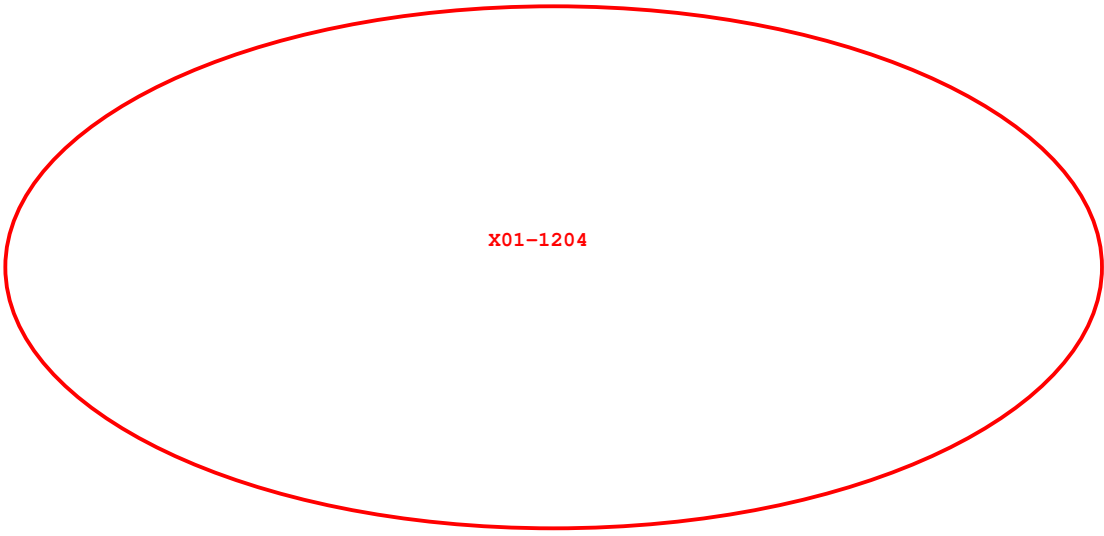
DELL Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title
Keyboard/TouchPad/BT

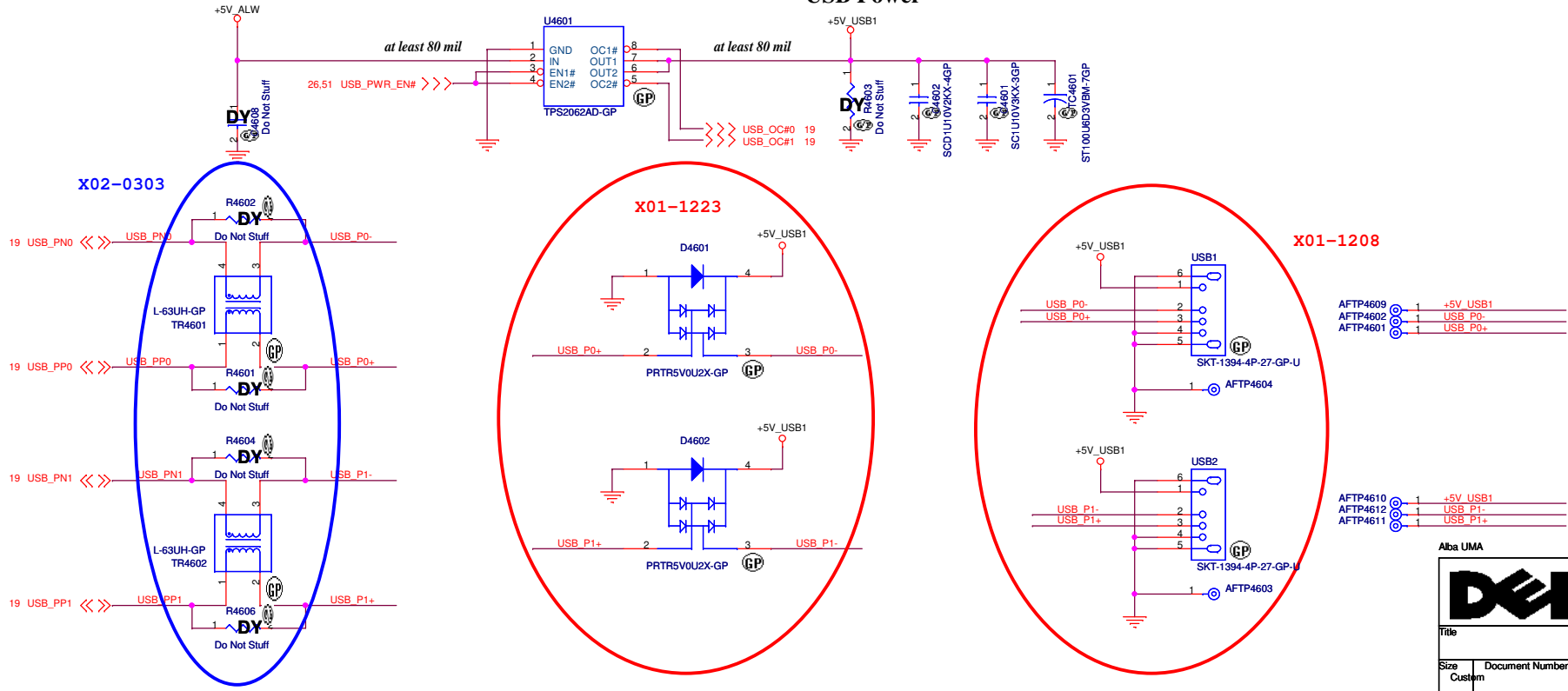
Size Document Number
 Custom **Alba UMA** Rev
 -1

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SSID = Modem

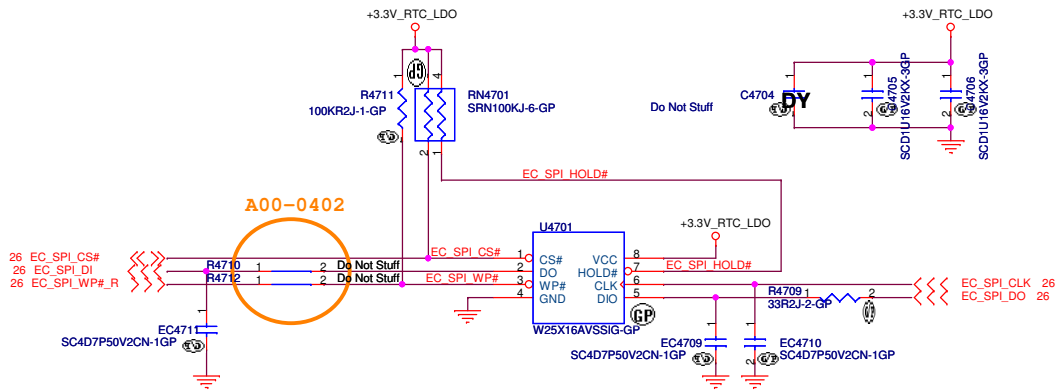


USB Power



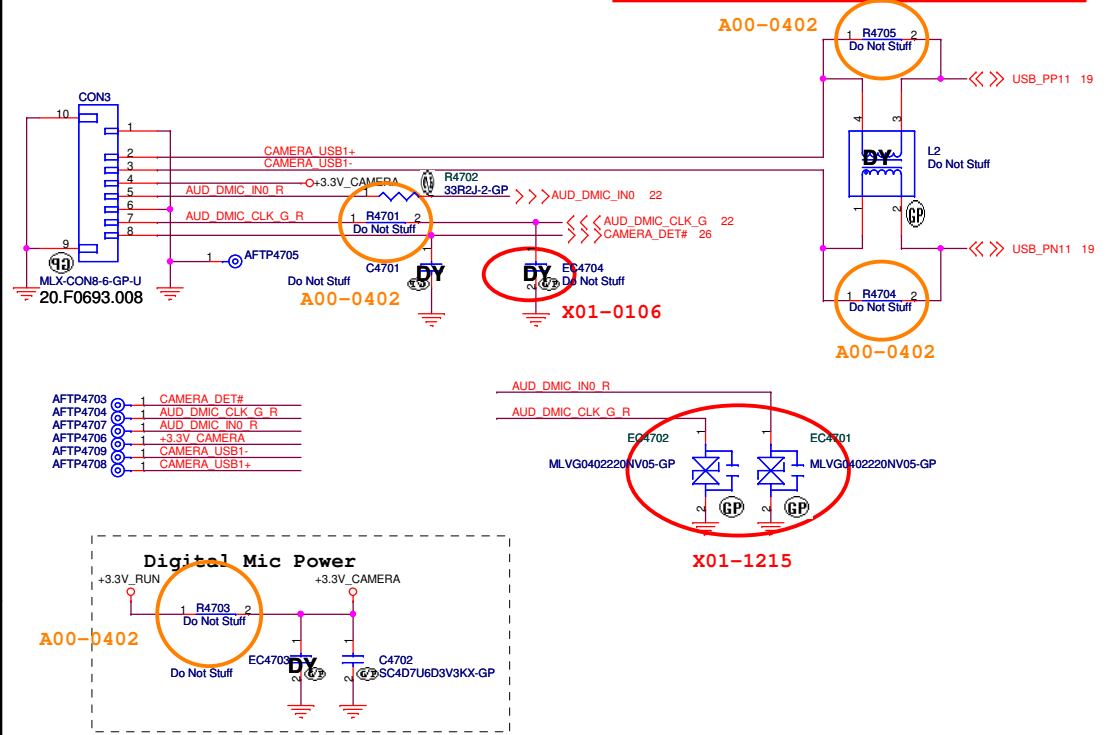
SSID = Flash.ROM

SPI FLASH ROM (16M bits)



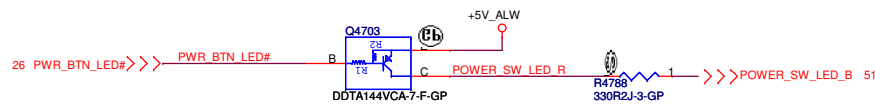
Camera Connector

SSID = User.Interface

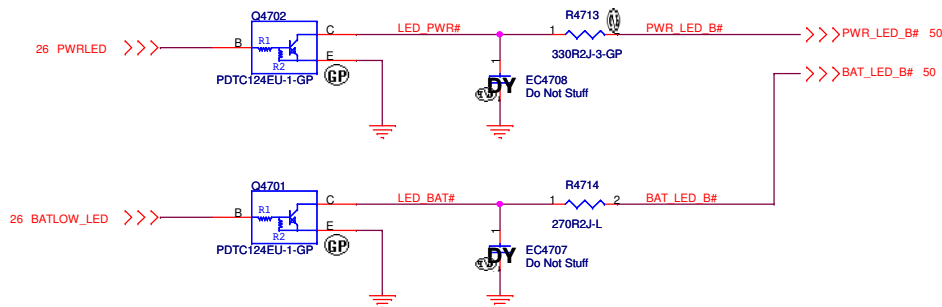


SSID = User.Interface

Power Button LED

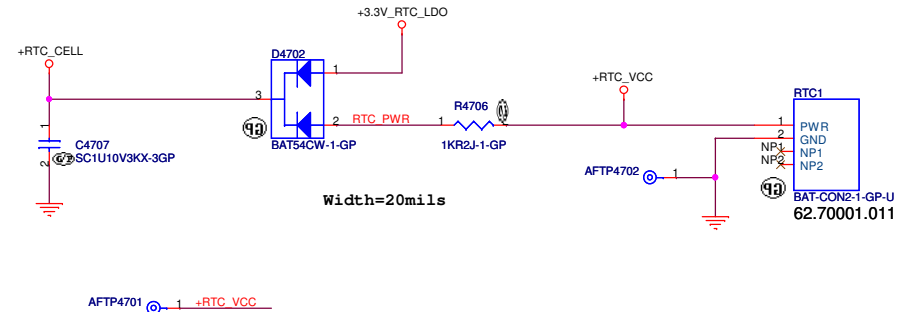


Power/Battery LED




SSID = RBATT

RTC Connector




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Title					
(Reserve)					
Size	Document Number				Rev
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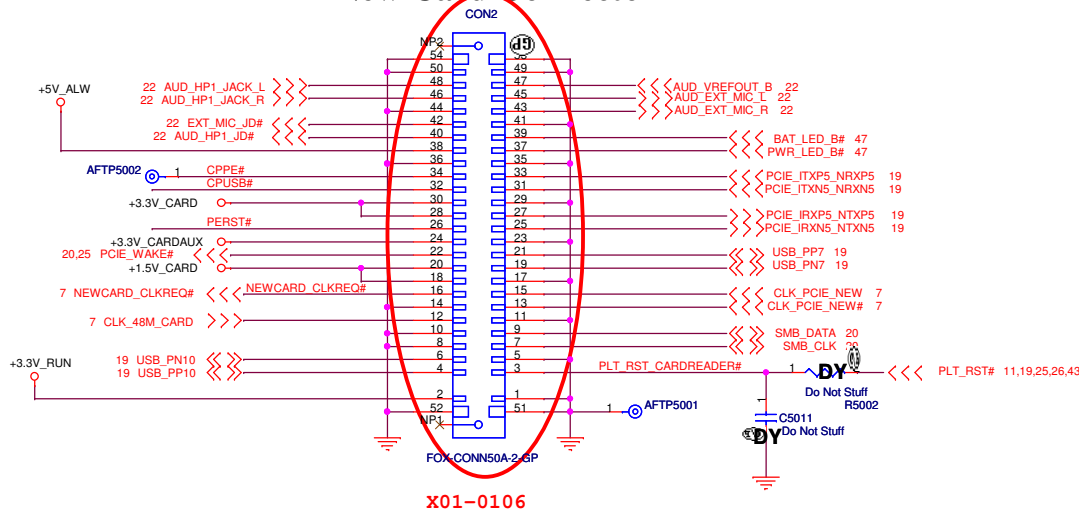
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			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title			(Reserve)
Size Custom	Document Number Alba UMA	Rev -1	
Date: Monday, April 06, 2009			Sheet 49 of 61

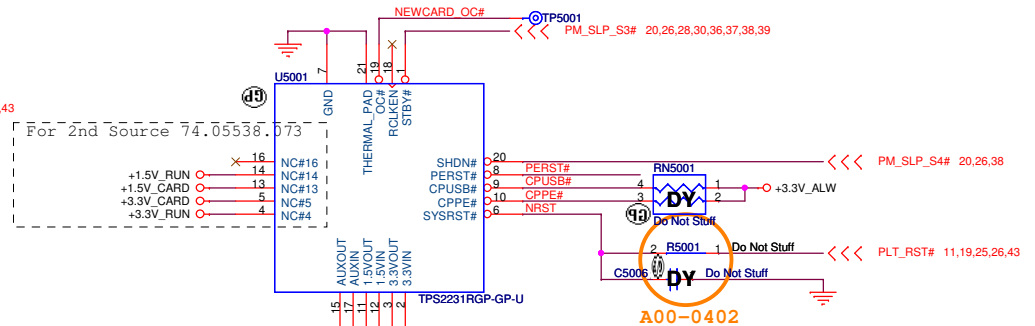
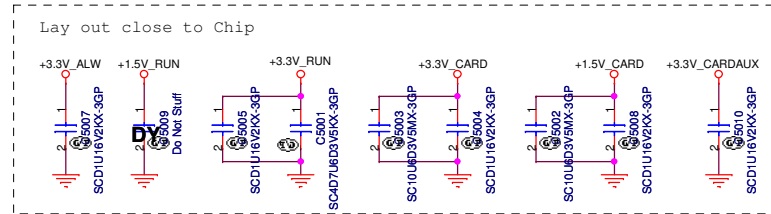
SSID = ExpressCard

New Card Connector



X01-0106

AFTP5029	1	PWR_LED_B#
AFTP5032	1	BAT_LED_B#
AFTP5031	1	+5V_ALW
AFTP5030	1	PLT_RST_CARDREADER#
AFTP5028	1	PCIE_ITXP5_NRXPS
AFTP5025	1	PCIE_ITXNS_NRXNS
AFTP5025	1	PCIE_IRXP5_NTXPS
AFTP5024	1	PCIE_IRXNS_NTXNS
AFTP5026	1	AUD_VREFOUT_B
AFTP5004	1	AUD_HP1_JACK_L
AFTP5006	1	AUD_HP1_JACK_R
AFTP5007	1	+3.3V_RUN
AFTP5008	1	CPUSB#
AFTP5005	1	USB_PP7
AFTP5008	1	USB_PN7
AFTP5011	1	AUD_EXT_MIC_L
AFTP5010	1	AUD_EXT_MIC_R
AFTP5011	1	EXT_MIC_JD#
AFTP5013	1	AUD_HP1_JD#
AFTP5014	1	CLK_48M_CARD
AFTP5012	1	NEWCARD_CLKREQ#
AFTP5015	1	+3.3V_CARD
AFTP5015	1	PERST#
AFTP5022	1	+3.3V_CARDAUX
AFTP5021	1	PCIE_WAKE#
AFTP5016	1	+1.5V_CARD
AFTP5018	1	SMB_DATA
AFTP5003	1	SMB_CLK
AFTP5021	1	USB_PN10
AFTP5028	1	USB_PP10



+1.5V_CARD Max. 650mA, Average 500mA.
 +3.3V_CARD Max. 1300mA, Average 1000mA
 +3.3V_CARDAUX Max. 275mA

Alba UMA

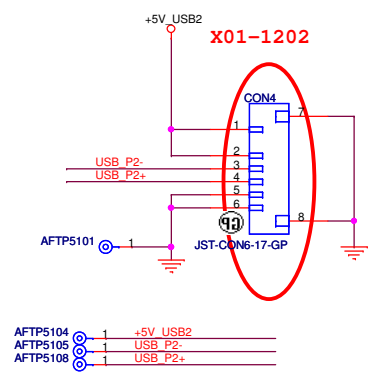
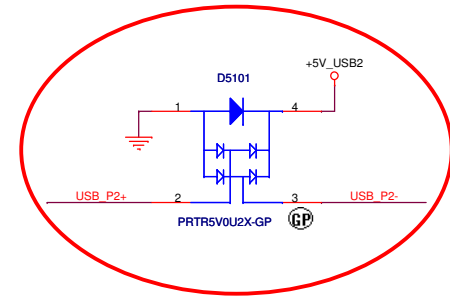
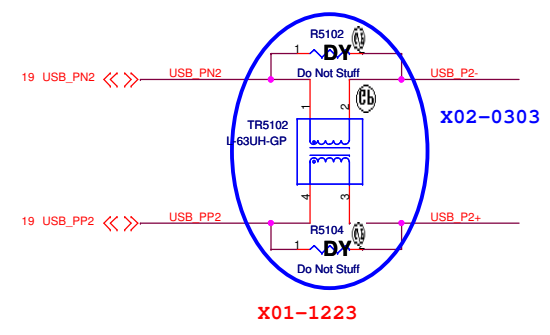
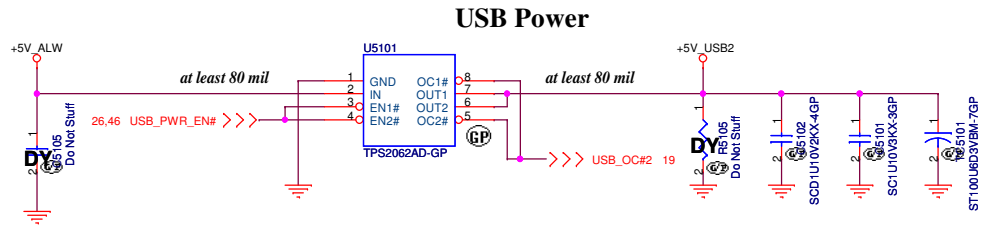
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Title: **Express Card Board CONN**

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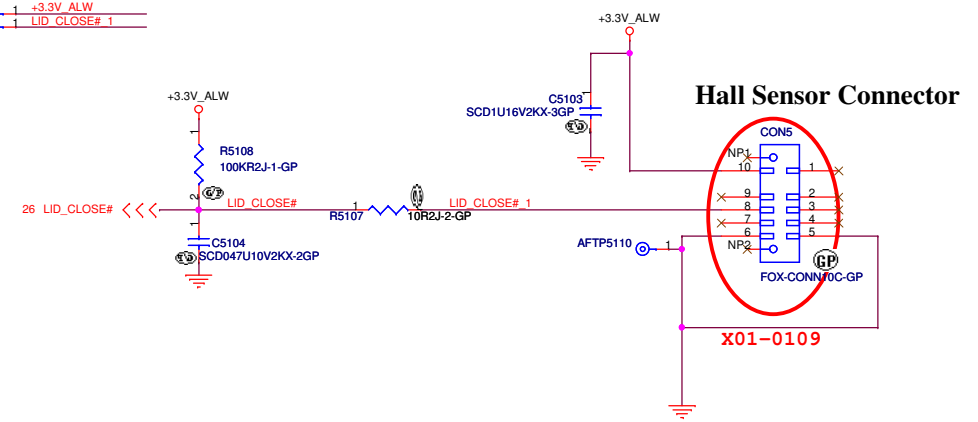
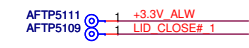
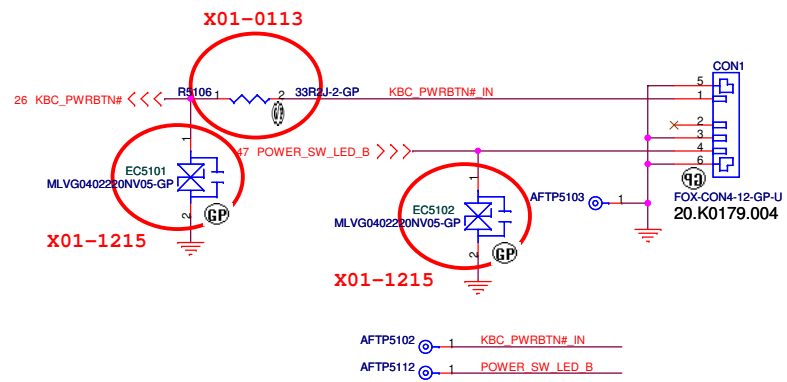
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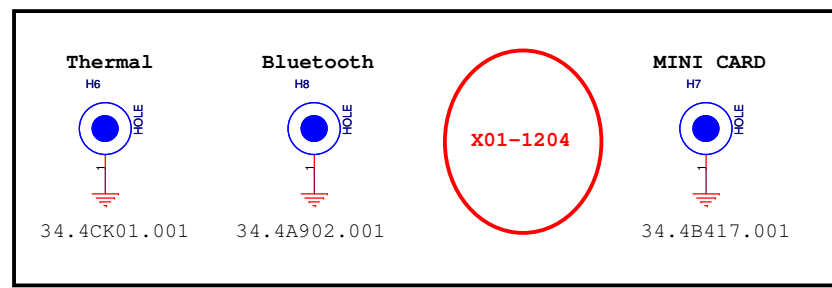
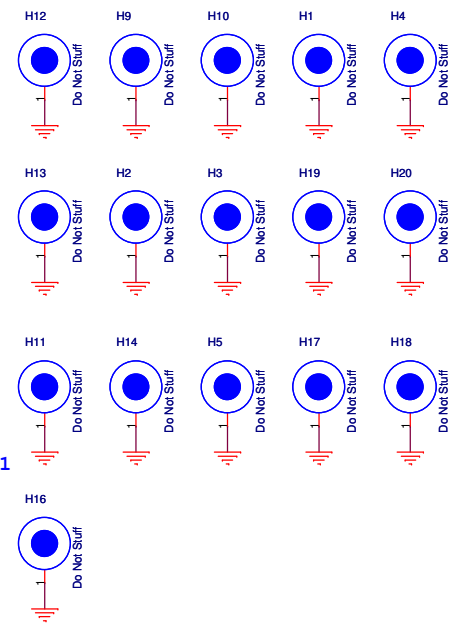
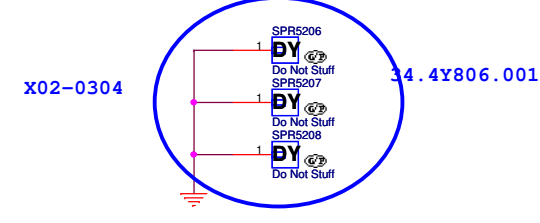
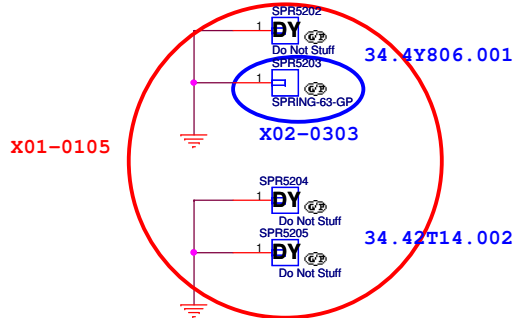
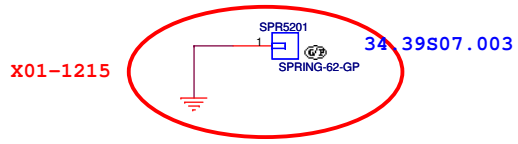
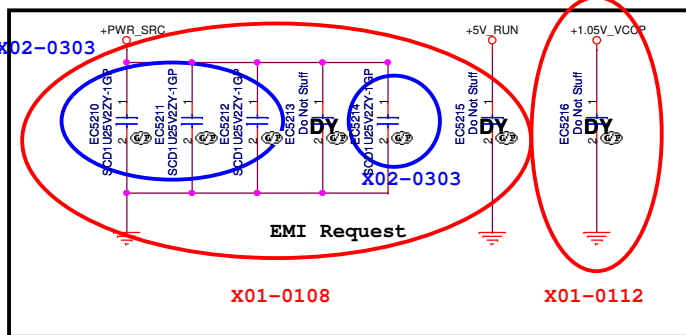
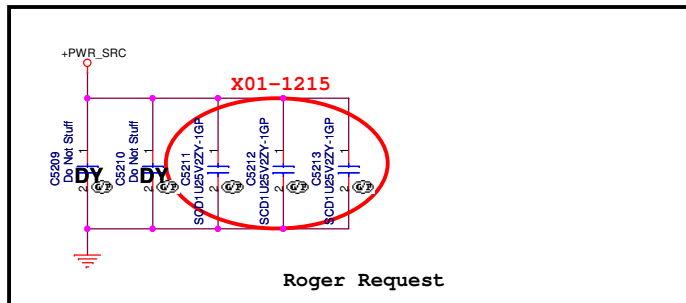
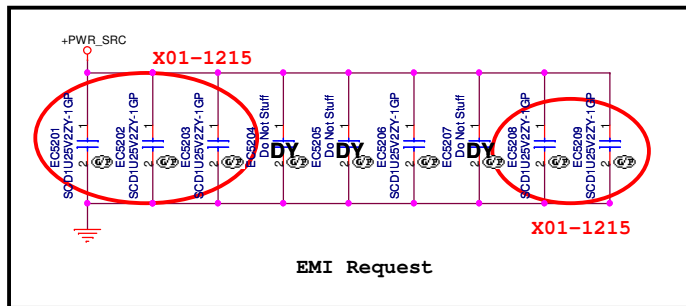
SSID = USB



SSID = User.Interface

Power Button Board CONN





SSID = VIDEO

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Title					
VGA-PCIE/LVDS(1/4)					
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SSID = VIDEO

Aba UMA

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Title **VGA-TV/CRT/DP PORT**

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SSID = VIDEO

SSID = VIDEO

SSID = VIDEO

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Title					
VRAM					
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Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
1	20,26	2008/11/03	Wistron	UMA no need.	ICH gpio6 NC,KBC gpio45 NC,Remove R2030,R2635	X01
2	34	2008/11/19	Wistron	LoadLine is too low.	Change PR3431 to 3.48K ohm.	X01
3	25	2008/11/25	Realtek	Prevent for capacitance effect.	Change R2506 to 1K ohm.	X01
4	22	2008/11/27	IDT	PC beep issue.	Change R2203,R2206 to 10K ohm. Add R2218,R2219.	X01
5	26	2008/11/27	Wistron	MB version changed.	Change R2609 pop,R2608 dummy.	X01
6	15	2008/11/27	Wistron	Reserve +3.3V_RUN trace.	Add R1518.	X01
7	25	2008/12/18	KDS	Follow crystal vendor test result.	Change C2501 to 18pF,C2502 to 15pF	X01
8	18,46,52	2008/12/04	Dell	Remove MDC function.	Remove MDC schematics,holding,stand off.	X01
9	46	2008/12/04	Wistron	ID modify,Change USB connector.	Change USB connector from one dual port to two single port.(22.10218.T51)	X01
10	45	2008/12/04	Wistron	Change touch pad connector.	Change touch pad connector to 20.K0179.004	X01
11	42	2008/12/08	Wistron	Change RJ45 connector.	Change RJ45 connector to 22.10177.C81	X01
12	33	2008/12/15	Wistron	Add 15_ALW Schematics.	Add 15_ALW Schematics.	X01
13	30	2008/12/15	Wistron	Modify 3V 5V schematics.	Modify 3V 5V schematics.	X01
14	22	2008/12/15	Wistron	Dianoetic mode sound is too slow.	Modify PC Beep schematics.	X01
15	26,41	2008/12/15	Wistron	For Panel Test.	Add LCD_TST_EN for panel test. R2638 POP.	X01
16	52	2008/12/15	Wistron	EMI issue.	Add SPR5201.	X01
17	28	2008/12/15	Wistron	Rename trace name.	Rename T8_THERMDC and T8_THERMDA.	X01
18	41	2008/12/17	Wistron	CMO panel white screen issue.	Reserve R4108.	X01
19	41	2008/12/18	Wistron	LCD Power Sequence Issue.	Modify LCD Power schematics. Change LCD CONN part.	X01
20	52	2008/12/18	Wistron	EMI Issue.	Add SPR5202.	X01
21	42	2008/12/19	Wistron	CRT R.G.B EA test issue.	Change bead to 47ohm and depop capacitors for pi filter.	X01
22	32	2008/12/10	Wistron	Prevent leakage from KBC.	Change PR3203 pull high from +3.3V_ALW to +3.3V_RTC_LDO.	X01


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Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
23	44, 52 51, 47	2008/12/15	Wistron	Modify based on EMI test result.	EC5203/C5212/EC5202/C5211/C5213/EC5206/EC5201/EC5208 use 0.1u-Cap EC4701/EC4702/EC4401/EC4402/EC4403/EC4404/EC5101 use 22P5V-Varistor POWER_SW_LED_B add one 22P5V-Varistor Add EC5209 0.1uF cap.	X01
24	20, 42, 46	2008/12/23	Wistron	Layout request.	Swap TR4602, RN2001, RN4202, TR4601 net.	X01
25	46, 51	2008/12/23	Wistron	For EMI request.	Add D4601, D4602, D5101	X01
26	52	2009/01/05	Wistron	Reserve 3 Spring.	Add SPR5203, SPR5204, SPR5205. Dummy SPR5202.	X01
27	15	2008/12/30	Wistron	Remove R1515. For layout get good performance.	Remove R1515, change R1549 to 2.2uF.	X01
28	50	2009/01/06	Wistron	Change CON2 connector.	Change CON2 connector to 20.F1400.050.	X01
29	9	2009/01/06	Wistron	For VCC_CORE sense.	Add PG901, PG902. Dummy C925, Pop C901	X01
30	47, 52	2009/01/06	Wistron	For EMI request.	Reserve EC4704, EC5210, EC5211, EC5212, EC5213, EC5214	X01
31	26	2009/01/06	Wistron	Keyboard detect.	Pop R2625.	X01
32	52	2009/01/08	Wistron	For EMI request.	Reserve EC5215 for +5V_RUN	X01
33	44, 51	2009/01/08	Wistron	Change HDD1, CON5 connector.	Modify HDD1, CON5 symbol.	X01
34	51	2009/01/09	Wistron	CON5 symbol layout concern.	Change CON5 pin5 to GND, pin7 to NC.	X01
35	45	2009/01/09	Wistron	Touch pad cable change.	Modify TPAD1 pin define.	X01
36	52	2009/01/12	Wistron	For EMI request.	Reserve EC5216.	X01
37	8	2009/01/12	Wistron	GTL issue.	Pop C802.	X01
38	22	2009/01/13	Wistron	Pop noise.	Add KBC GPIO33.	X01
39	51	2009/01/13	Wistron	KBC burn issue.	Change R5106 to 33 ohm.	X01
40	41	2009/02/19	Wistron	CMO panel white screen issue.	Pop R4108.	X02
41	26	2009/02/19	Wistron	Change board ID.	Pop R2601, R2608. Dummy R2602, R2609.	X02
42	31, 42, 44	2009/02/23	Wistron	Change connector.	Change SPK1, FAN1, RJ45 connector.	X02
43	18, 26	2009/02/24	Wistron	Change 32.768K crystal cap size.	Change C1806, C1807, C2607, C2608 to 0603 size.	X02

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Title
Change List 2- EE

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Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
44	22	2009/02/27	Wistron	Codec pop noise.	Add Q2201~Q2205. Change C2204 to 2.2uF. Move 60.4 ohm from small board to MB.	X02
45	46, 51, 52	2009/03/03	Wistron	Modify based on EMI test result.	EC5212, EC5211, EC5210, EC5214 -- 0.1u cap on board TR4602, TR4601, TR5102 -- 67ohm common mode on board spr5203--spring on board	X02
46	26	2009/03/03	Wistron	Remove PAID for KB detection	Dummy R2625.	X02
47	52	2009/03/04	Wistron	For EMI request.	Add SPR5206, SPR5207, SPR5208.	X02
48	26	2009/04/02	Wistron	Board ID Changed.	Pop R2604, Dummy R2603.	X02

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Change List 3 - EE		
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Item	Page#	Date	Request By	Issue description	Solution D	
1	33	2008/12/15	Wistron	3D3V OCP over spec.	Change R3312 from 160K to	
2	33	2009/01/05	Wistron	5V output voltage is too high.	Change PR3310 from 30.9K to Change PR3314 from 20K to	
3	33	2009/01/05	Wistron	5V H/S MOSFET VDS over spec.	Add Snubber PR3319 to 2.2K ohm, PC3319 to 560pF.	X01
4	33	2009/01/05	Wistron	5V OCP over spec.	Change R3311 from 160K to 147K ohm.	X01
5	33	2008/12/15	Wistron	Add 15V_ALW schematics	Add 15V_ALW schematics. DY PR3306	X01
6	34	2008/11/27	Wistron	LoadLine is too low.	Change PR3431 from 3.92K to 3.48K ohm.	X01
7	34	2009/01/05	Wistron	CPU_CORE OCP is too low.	Change PR3418 from 12.1K to 13.7K ohm.	X01
8	38	2009/01/05	Wistron	UMA 1D8V OCP is too low.	Change PR3802 from 8.06K to 10.7K ohm.	X01
9	39	2009/02/19	Wistron	Change main source.	Change PTC3301,PTC3302 to 77.22271.27L.	X02
10	38	2009/02/19	Wistron	Change main source.	Change PTC3802 to 79.33719.20D.	X02
11	32	2009/03/02	Wistron	Change cap from 25V to 50V.	Change PC3208,PC3209 to 78.10424.2BL	X02
12	31	2009/03/02	Wistron	Change main source.	Change PD3107 to 83.22R03.03G.	X02
13	33	2009/03/03	Wistron	Phase voltage is too high.	PC3319 change from 560pF to 680pF	X02
14	34	2009/03/03	Wistron	LoadLine is too high.	PR3431 change from 3.48K ohm to 3.92K ohm.	X02
15	33	2009/03/05	Wistron	15_ALW no need to install PD3303.	Dummy PD3303.	X02
16	32	2009/04/02	Wistron	Sequence issue.	Change PC3207 from 1uF to 0.1uF.	A00
17	32	2009/04/06	Wistron	For CPU transition response.	Change PC3409 from 100p to 150p.	A00

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Title
Change List - Power

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