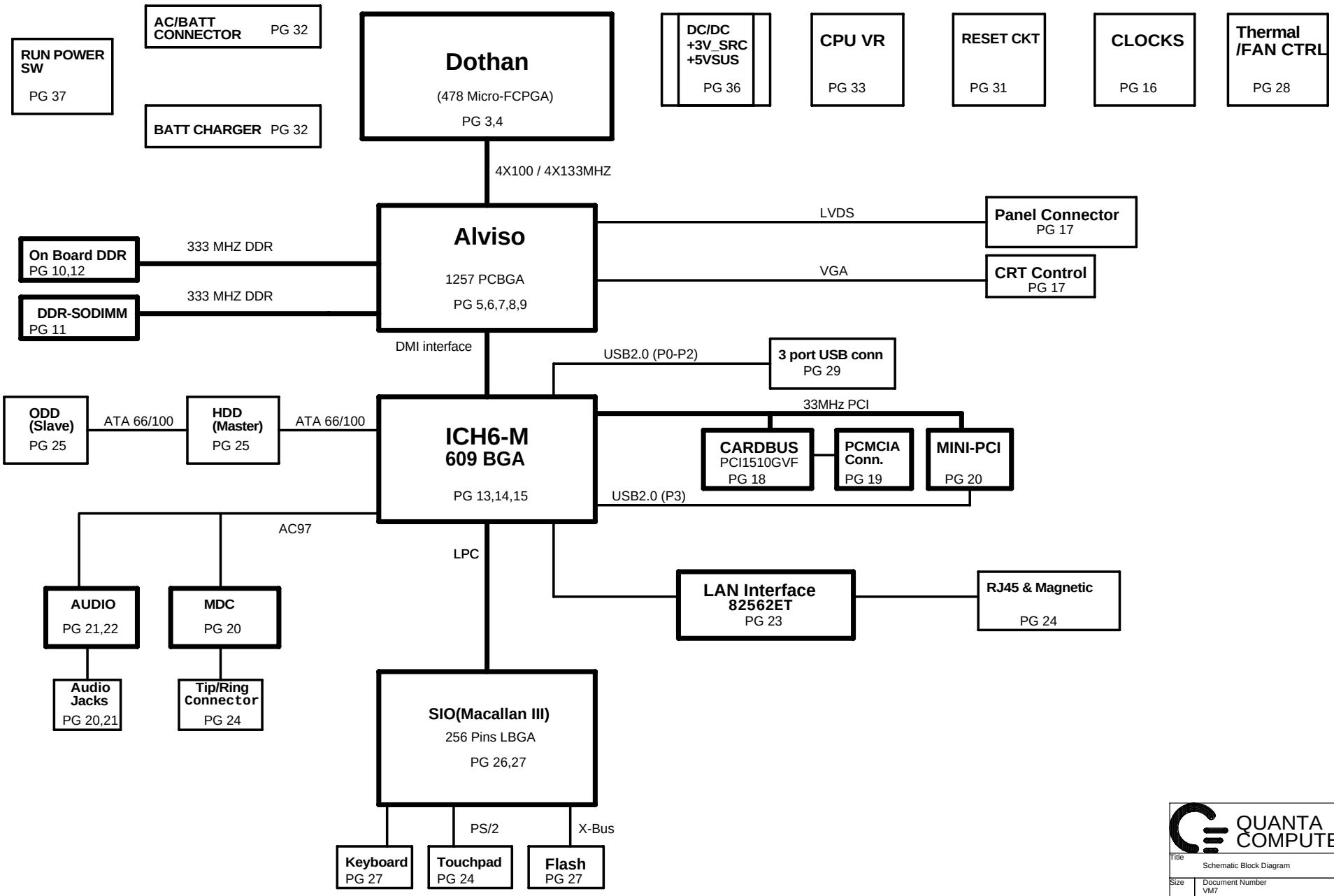
Tonga & Tyler (T2)

VER : 3C



QUANTA COMPUTER

Title	Schematic Block Diagram	
Size	Document Number VM7	Rev 3C
Date: Thursday, July 14, 2005	Sheet 1 of 45	

Alviso Strapping Signals and Configuration

Page.5

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = Reserved 001 = FSB533 010 = FSB800 011-100 = Reversed 101 = FSB400 110-111 = Reversed
CFG[3:4]	Reversed	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4** (Default)
CFG6	DDR I / DDR II	0 = DDR II 1 = DDR I (Default)
CFG7	CPU Strap	0 = Prescott **1 = Dothan** (Default)
CFG[8:11]	Reversed	
CFG[12:13]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled **11 = Normal Operation** (Default)
CFG[14:15]	Reversed	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled** (Default)
CFG17	Reversed	
CFG18	CPU core VCC Select	**0 = 1.05V** (Default) 1 = 1.5V
CFG19	CPU VTT Select	**0 = 1.05V** (Default) 1 = 1.2V
CFG20	Reversed	
SDVOCRTL_DATA	SDVO Present	**0 = No SDVO device present** (Default) 1= SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORK In signal.

For Dothan A stepping

	CPU		NB			CLOCK		
	BSEL1	BSEL0	CFG2	CFG1	CFG0	FS_C	FS_B	FS_A
100MHZ	0	0	1	0	1	1	0	1
133MHZ	0	1	0	0	1	0	0	1

For Dothan B stepping

	CPU		NB			CLOCK		
	BSEL1	BSEL0	CFG2	CFG1	CFG0	FS_C	FS_B	FS_A
100MHZ	0	1	1	0	1	1	0	1
133MHZ	0	0	0	0	1	0	0	1

PCI TABLE

DEVICE	IDSEL	IRQ	REQ# / GNT#
PCMCIA controller	AD17	PIRQA# PIRQC#	REQ1#/GNT1#
MINIPCI SLOT	AD19	PIRQB# PIRQD#	REQ3#/GNT3#

ICH6-M Integrated Pull-up and Pull-down Resistors

ICH6-M EDS 15825 1.5V2

EE_DIN, EE_DOUT, GNT[3:0], GPIO[25], GNT[4]#/GPO[48], GNT[5]#/GPO[17], GNT[6]#/GPO[16], LAD[3:0]#/FB[3:0]#, LAN_RXD[2:0], LDRQ[1]/GPI[41], PME#, LDRQ[0], PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
ACZ_BIT_CLK, ACZ_RST#, ACZ_SDIN[2:0], ACZ_SDOUT, ACZ_SYNC, DPRSTP#/TP[4], DPRSLPVR/TP[1], EE_CS, SPKR	ICH6 Internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

ICH6-M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

ICH6-M Strapping Signals and Configuration

Pin Name	Strap Description	Note
ACZ_SDOUT	0=PCI Express Port Config bit 1(default) 1=XOR Chain Entrance Test mode	
ACZ_SYNC	0=PCI Express Port Config bit 1(default) 1=Reserved	
DPRSLPVR	Reserved	This Signal should not be pulled high.
EE_CS	Reserved	This Signal should not be pulled high.
EE_DOUT	Reserved	This Signal should not be pulled low.
GNT[5]#/GPO[17]#	Boot BIOS Destination Selection	This functionality intended for debug/testing only.
GNT(6)#/GPO(16)#	0="Top block swap" mode 1=Normal(default)	"Top block swap" ICH6 inverts A16 for all cycles targeting FWH BIOS space
GPIO[25]	0=Enable Internal Vcc2_5V VRM(default) 1=Disable Internal Vcc2_5V VRM	This Signal has a weak inernal PU during RSMRST# and is disabled within 100ms after RSMRST# deasserts.
INTVRMEN	0=Disable Internal VccSus 1.5V VRM(default) 1=Enable Internal VccSus 1.5V VRM	
LINKALERT#	Reserved	This Signal requires an external PU
REQ[4:1]#	XOR Test Chain Selection	
SATALED#	Reserved	This Signal should not be pulled low.
SPKR	0=Normal(default) 1=NO Reboot	This Signal should not be pulled high.
TP[3]	0=XOR Chain Entrance Test mode 1=Normal(default)	This Signal should not be pulled low unless using XOR Chain testing.

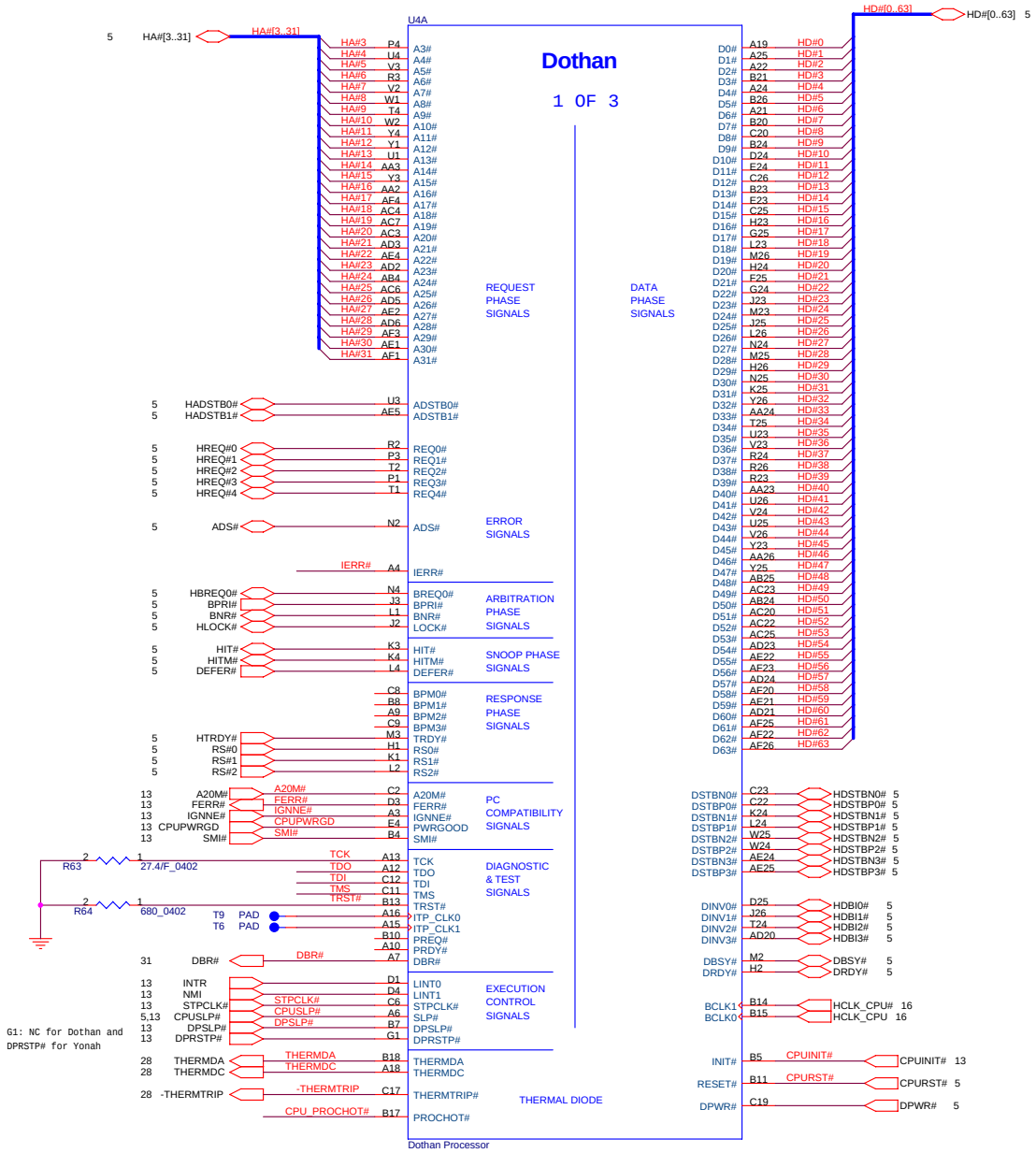
NOTE: All strap signals are sampled on the rising edge of the ICH6-M's PWROK signal.

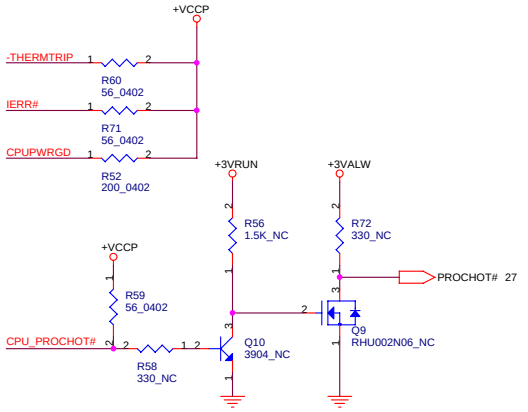
Power Name	Page#
+1_5V_LAN	P.15
+1_5V_PCIE	P.15
+1_5VRUN	P.4,8,14,15,30,37
+1_5VSUS	P.15,20,30,31,35,37
+2.5VRUN	P.6,8,15,17,37
+2.5VSUS	P.6,8,9,10,11,12,34,37
+3V562ET	P.23
+3VLAN	P.14,15,20,23,24
+3V_SRC	P.15,23,36,37
+3VALW	P.3,17,20,24,26,27,28,30,31,32,36,38
+3VRUN	P.3,8,11,12,13,14,15,16,17,18,20,21,22,24,25,26,27,28,30,31,33,37
+3VSUS	P.3,14,15,17,18,19,20,22,24,26,28,31,34,35,36
+5VALW	P.15,17,36,37,38
+5VRUN	P.15,17,20,21,22,24,25,27,28,30,33,37
+5VSUS	P.15,19,20,28,29,34,35,36,37
+15V	P.17,28,36,37
+AVDD	P.21
+DC_IN	p.32

Power Name	Page#
+RTC_PWR3_3V	P.26,36,38
+VCCP	P.3,4,5,6,8,9,13,15,16,28,35,37
+VCCRTC	P.13,15,26,28
CRTVCC	P.17
DCIN+	P.32
DC_IN+	P.32
PBATT+	P.32,38
PWR_SRC	P.17,26,30,32,33,34,35,36,37,38
USBVCC0,USBVCC1,USBVCC2	P.29
VHCORE	P.4,33

QUANTA COMPUTER

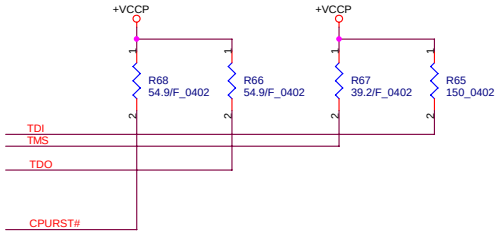
Title	Dothan Processor (Host BUS)	
Size	Document Number VM7	Rev 2A
Date: Thursday, July 14, 2005	Sheet 2 of 45	

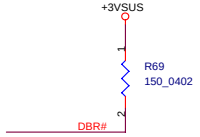




ITP disable guidelines

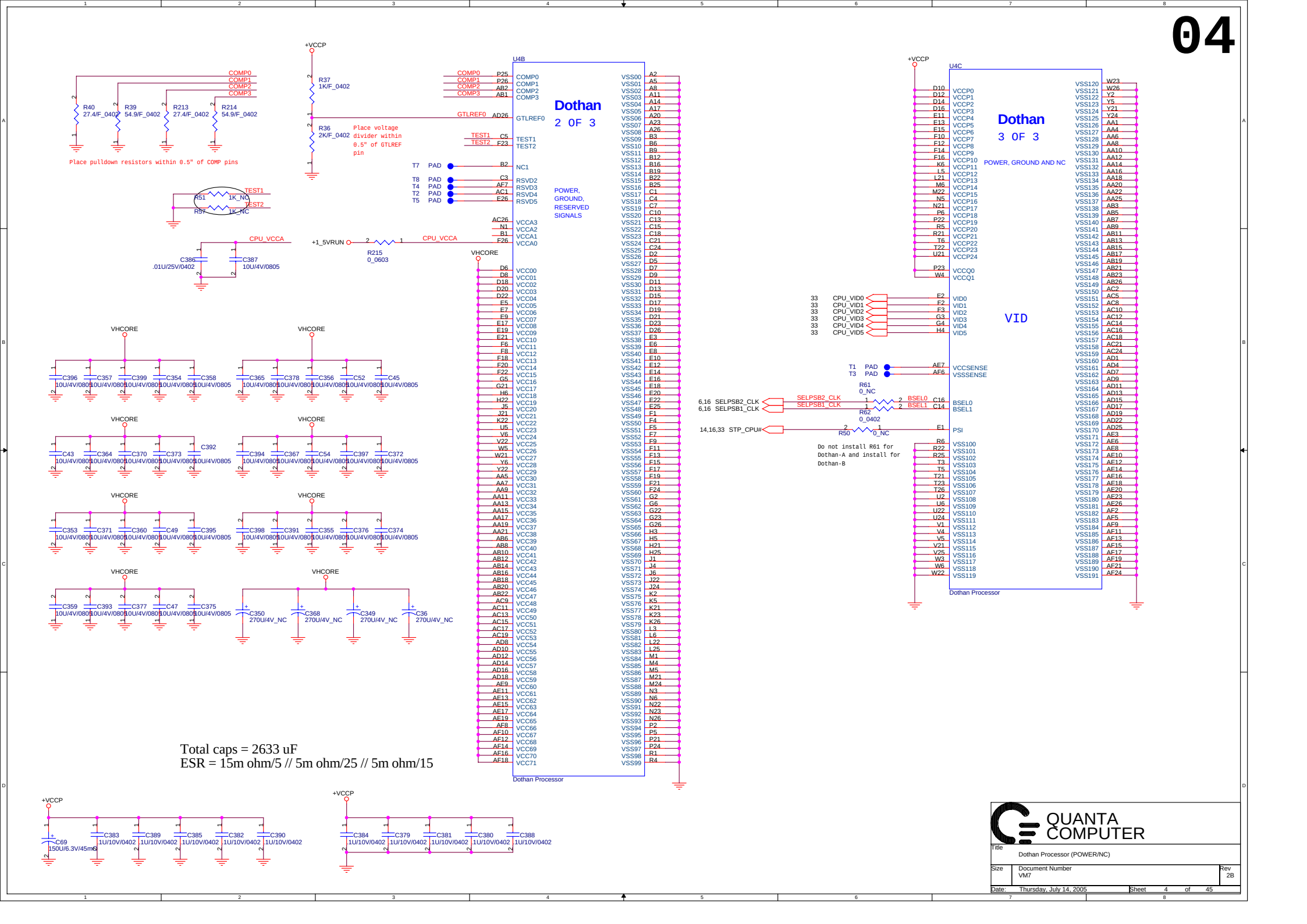
Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VCCP	Within 2.0" of the CPU
TMS	39 ohm +/- 5%	VCCP	Within 2.0" of the CPU
TRST#	680 ohm +/- 5%	GND	Within 2.0" of the CPU
TCK	27 ohm +/- 5%	GND	Within 2.0" of the CPU
TDO	Open	VCCP	Within 2.0" of the CPU



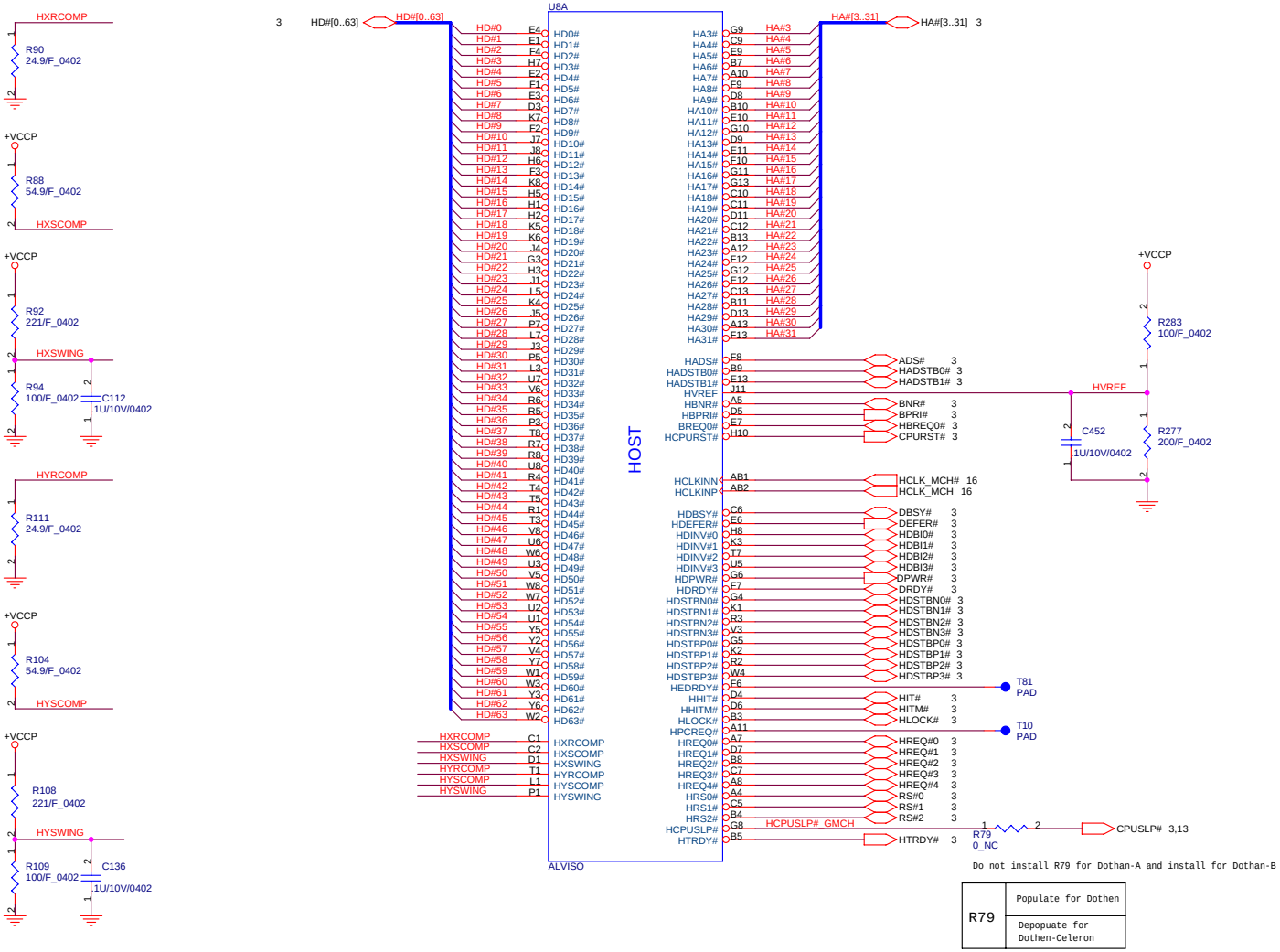


QUANTA COMPUTER

Title	Dothan Processor (Host BUS)		
Size	Document Number VM7		Rev 2B
Date:	Thursday, July 14, 2005	Sheet 3 of 45	

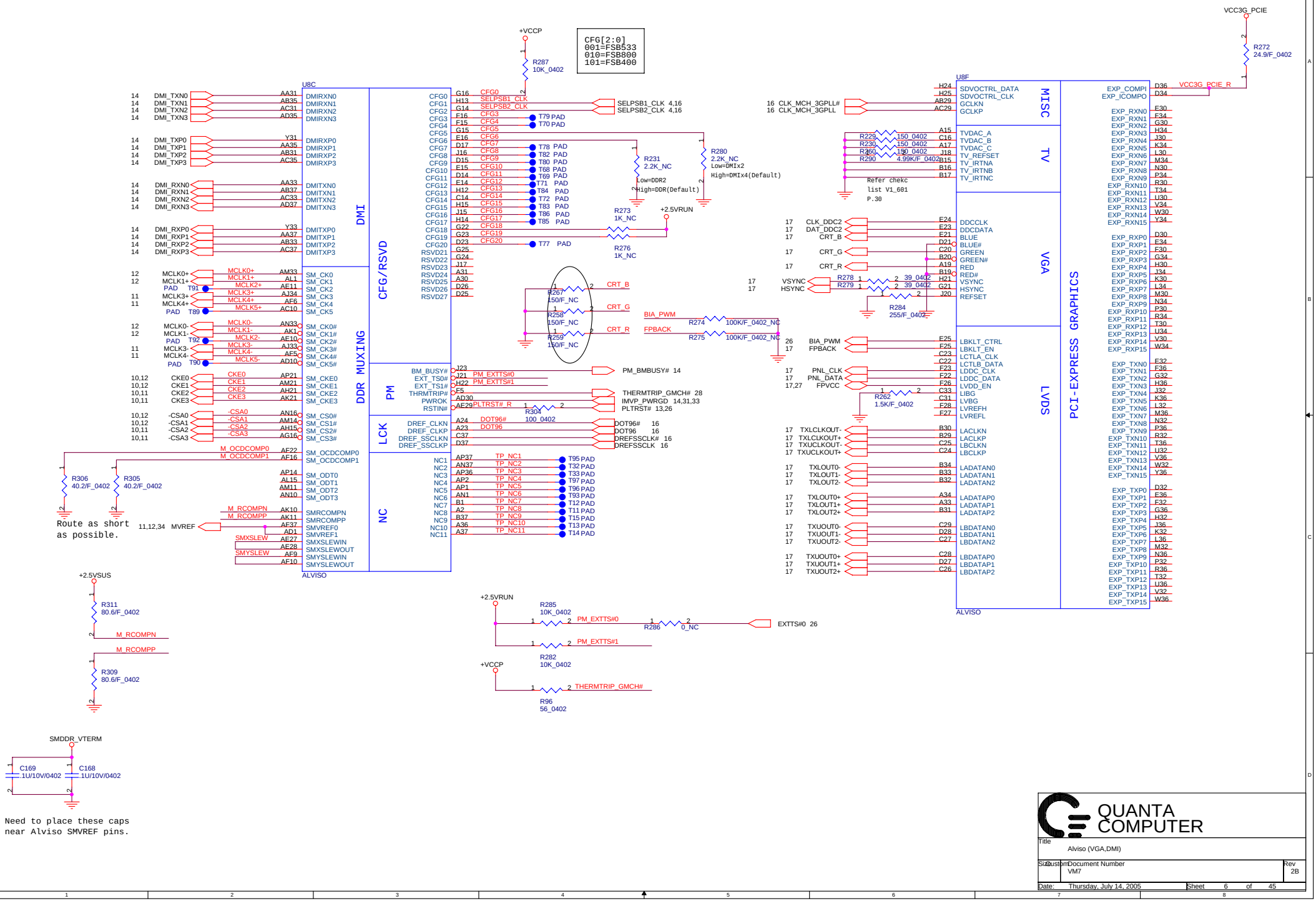


QUANTA COMPUTER
Title: Dothan Processor (POWER/NC)
Size: Document Number VM7
Rev: 2B
Date: Thursday, July 14, 2005
Sheet 4 of 45



QUANTA COMPUTER

Title	Alviso (Host)	
Size	Document Number VM7	Rev 2B
Date: Thursday, July 14, 2005	Sheet 5 of 45	



QUANTA COMPUTER

Title	Alviso (VGA,DMI)		
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MAB[0..13] → MAB[0..13] 10,11
MAA[0..13] → MAA[0..13] 10,12
-CSA[0..3] → -CSA[0..3] 6,10,11,12
CKE[0..3] → CKE[0..3] 6,10,11,12

RMD[0..63] → RMD[0..63] 10,11,12
RDQM[0..7] → RDQM[0..7] 10,11,12
RDQS[0..7] → RDQS[0..7] 10,11,12

U8B

DDR SYSTEM MEMORY A

MD0	AG35	SADQ0	SA_BS0#	AK15	A_BS0# 10,12
MD1	AH35	SADQ1	SA_BS1#	AK16	A_BS1# 10,12
MD2	AL35	SADQ2	SA_BS2#	AL21	
MD3	AL37	SADQ3			
MD4	AH36	SADQ4	SA_DM0	AJ37	DQM0
MD5	AJ35	SADQ5	SA_DM1	AP35	DQM1
MD6	AK37	SADQ6	SA_DM2	AL29	DQM2
MD7	AL34	SADQ7	SA_DM3	AP24	DQM3
MD8	AM36	SADQ8	SA_DM4	AP9	DQM4
MD9	AN35	SADQ9	SA_DM5	AP4	DQM5
MD10	AP32	SADQ10	SA_DM6	AJ2	DQM6
MD11	AM31	SADQ11	SA_DM7	AD3	DQM7
MD12	AM34	SADQ12			
MD13	AM35	SADQ13	SA_DQS0	AK36	DQS0
MD14	AL32	SADQ14	SA_DQS1	AP33	DQS1
MD15	AM32	SADQ15	SA_DQS2	AN29	DQS2
MD16	AN31	SADQ16	SA_DQS3	AP23	DQS3
MD17	AP31	SADQ17	SA_DQS4	AM8	DQS4
MD18	AN28	SADQ18	SA_DQS5	AM4	DQS5
MD19	AP28	SADQ19	SA_DQS6	AJ1	DQS6
MD20	AL30	SADQ20	SA_DQS7	AE5	DQS7
MD21	AM30	SADQ21			
MD22	AM28	SADQ22	SA_DQS0#	AK35	
MD23	AL28	SADQ23	SA_DQS1#	AP34	
MD24	AP27	SADQ24	SA_DQS2#	AN30	
MD25	AM27	SADQ25	SA_DQS3#	AN23	
MD26	AM23	SADQ26	SA_DQS4#	AN8	
MD27	AM22	SADQ27	SA_DQS5#	AM5	
MD28	AL23	SADQ28	SA_DQS6#	AH1	
MD29	AM24	SADQ29	SA_DQS7#	AE4	
MD30	AN22	SADQ30			
MD31	AP22	SADQ31	SA_MA0	AL17	MAA0
MD32	AM9	SADQ32	SA_MA1	AP17	MAA1
MD33	AL9	SADQ33	SA_MA2	AP18	MAA2
MD34	AL6	SADQ34	SA_MA3	AM17	MAA3
MD35	AP7	SADQ35	SA_MA4	AN18	MAA4
MD36	AP11	SADQ36	SA_MA5	AM18	MAA5
MD37	AP10	SADQ37	SA_MA6	AL19	MAA6
MD38	AL7	SADQ38	SA_MA7	AP20	MAA7
MD39	AM7	SADQ39	SA_MA8	AM19	MAA8
MD40	AN5	SADQ40	SA_MA9	AL20	MAA9
MD41	AN6	SADQ41	SA_MA10	AM16	MAA10
MD42	AN3	SADQ42	SA_MA11	AN20	MAA11
MD43	AP3	SADQ43	SA_MA12	AM20	MAA12
MD44	AP6	SADQ44	SA_MA13	AM15	MAA13
MD45	AM6	SADQ45			
MD46	AL4	SADQ46	SA_CAS#	AN15	-DCASA 10,12
MD47	AM3	SADQ47	SA_RAS#	AP16	-DRASA 10,12
MD48	AK2	SADQ48	SA_RCVENIN#	AF29	
MD49	AK3	SADQ49	SA_RCVENOUT#	AF28	
MD50	AG2	SADQ50	SA_WE#	AP15	-DMWA 10,12
MD51	AG1	SADQ51			
MD52	AL3	SADQ52			
MD53	AM2	SADQ53			
MD54	AH3	SADQ54			
MD55	AG3	SADQ55			
MD56	AF3	SADQ56			
MD57	AE3	SADQ57			
MD58	AD6	SADQ58			
MD59	AC4	SADQ59			
MD60	AF2	SADQ60			
MD61	AF1	SADQ61			
MD62	AD4	SADQ62			
MD63	AD5	SADQ63			

ALVISO

U8G

DDR SYSTEM MEMORY B

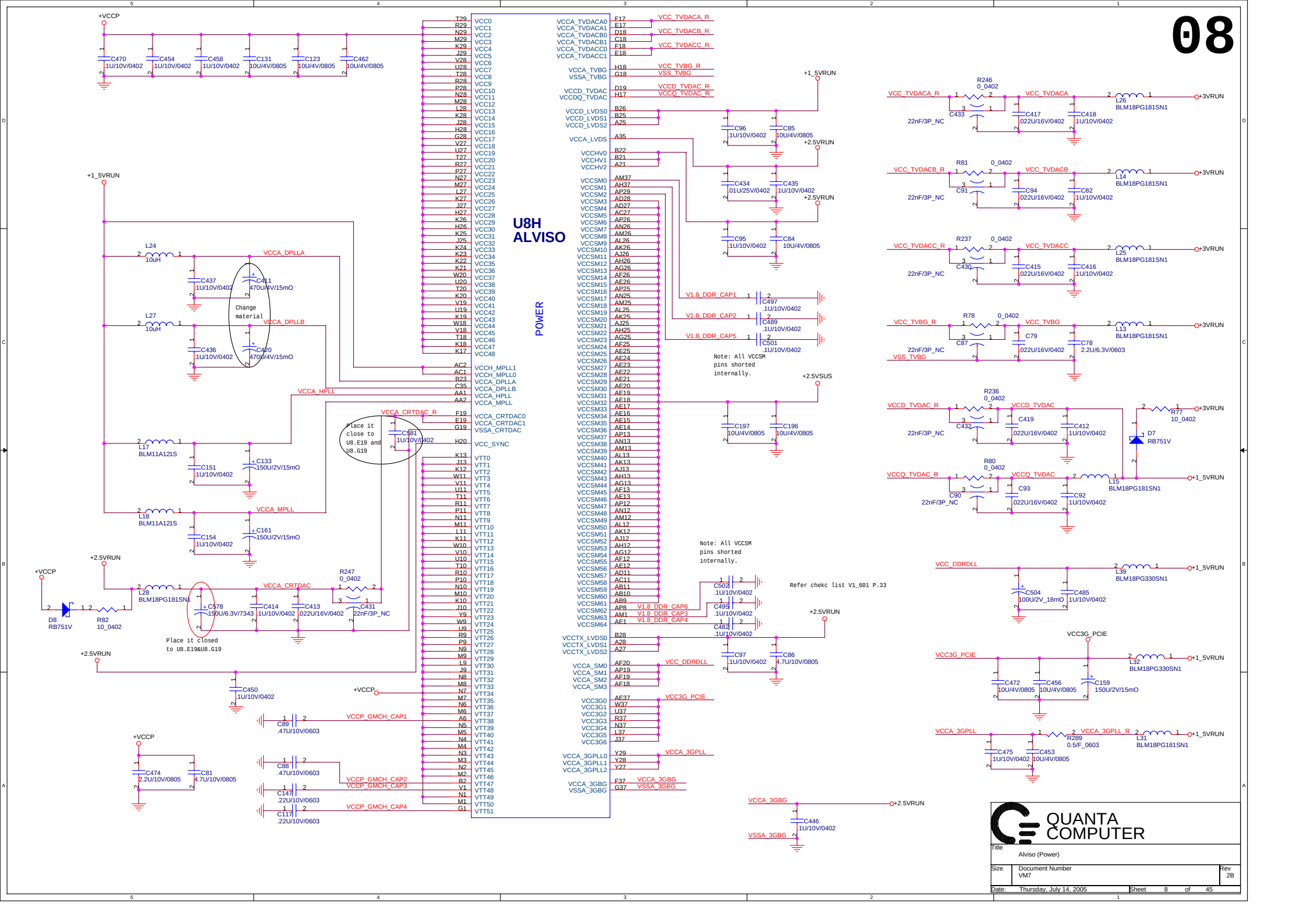
AE31	SBDQ0	SB_BS0#	AJ15	B_BS0# 10,11	
AE32	SBDQ1	SB_BS1#	AG17	B_BS1# 10,11	
AG32	SBDQ2	SB_BS2#	AG21		
AG36	SBDQ3				
AE34	SBDQ4	SB_DM0	AF32		
AE33	SBDQ5	SB_DM1	AK34		
AF31	SBDQ6	SB_DM2	AK27		
AF30	SBDQ7	SB_DM3	AK24		
AH33	SBDQ8	SB_DM4	AJ10		
AH32	SBDQ9	SB_DM5	AK5		
AK31	SBDQ10	SB_DM6	AE7		
AG30	SBDQ11	SB_DM7	AB7		
AG34	SBDQ12				
AG33	SBDQ13	SB_DQS0	AF34		
AH31	SBDQ14	SB_DQS1	AK32		
AJ31	SBDQ15	SB_DQS2	AJ28		
AK30	SBDQ16	SB_DQS3	AK23		
AJ30	SBDQ17	SB_DQS4	AM10		
AH29	SBDQ18	SB_DQS5	AH6		
AH28	SBDQ19	SB_DQS6	AF8		
AK29	SBDQ20	SB_DQS7	AB4		
AH30	SBDQ21				
AH27	SBDQ22	SB_DQS0#	AF35		
AG28	SBDQ23	SB_DQS1#	AK33		
AF24	SBDQ24	SB_DQS2#	AK28		
AG23	SBDQ25	SB_DQS3#	AJ23		
AJ22	SBDQ26	SB_DQS4#	AL10		
AK22	SBDQ27	SB_DQS5#	AH7		
AH24	SBDQ28	SB_DQS6#	AF7		
AH23	SBDQ29	SB_DQS7#	AB5		
AG22	SBDQ30				
AJ21	SBDQ31	SB_MA0	AH17	MAB0	
AG10	SBDQ32	SB_MA1	AK17	MAB1	
AG9	SBDQ33	SB_MA2	AH18	MAB2	
AG8	SBDQ34	SB_MA3	AJ18	MAB3	
AH8	SBDQ35	SB_MA4	AK18	MAB4	
AH11	SBDQ36	SB_MA5	AJ19	MAB5	
AH10	SBDQ37	SB_MA6	AK19	MAB6	
AJ9	SBDQ38	SB_MA7	AH19	MAB7	
AK9	SBDQ39	SB_MA8	AJ20	MAB8	
AJ7	SBDQ40	SB_MA9	AH20	MAB9	
AK6	SBDQ41	SB_MA10	AJ16	MAB10	
AJ4	SBDQ42	SB_MA11	AG18	MAB11	
AH5	SBDQ43	SB_MA12	AG20	MAB12	
AK8	SBDQ44	SB_MA13	AG15	MAB13	
AJ8	SBDQ45				
AJ5	SBDQ46	SB_CAS#	AH14	-DCASB 10,11	
AK4	SBDQ47	SB_RAS#	AK14	-DRASB 10,11	
AG5	SBDQ48	SB_RCVENIN#	AF15		
AG4	SBDQ49	SB_RCVENOUT#	AF14		
AD8	SBDQ50	SB_WE#	AH16	-DMWB 10,11	
AD9	SBDQ51				
AH4	SBDQ52				
AG6	SBDQ53				
AE8	SBDQ54				
AD7	SBDQ55				
AC5	SBDQ56				
AB8	SBDQ57				
AB6	SBDQ58				
AA8	SBDQ59				
AC8	SBDQ60				
AC7	SBDQ61				
AA4	SBDQ62				
AA5	SBDQ63				

ALVISO

RN3 10X4: RMD59 8, RMD63 6, RMD58 4, RMD62 2 → 7 MD59, 5 MD63, 3 MD58, 1 MD62
RN17 10X4: RMD26 8, RMD31 6, RMD30 4, RMD27 2 → 7 MD26, 5 MD31, 3 MD30, 1 MD27
RN4 10X2: RDQS7 4, RDQM7 2 → 3 DQS7, 1 DQM7
RN18 10X2: RDQS3 4, RDQM3 2 → 3 DQS3, 1 DQM3
RN5 10X4: RMD60 8, RMD57 6, RMD61 4, RMD56 2 → 7 MD60, 5 MD57, 3 MD61, 1 MD56
RN19 10X4: RMD29 8, RMD28 6, RMD25 4, RMD24 2 → 7 MD29, 5 MD28, 3 MD25, 1 MD24
RN6 10X4: RMD51 8, RMD55 6, RMD54 4, RMD50 2 → 7 MD51, 5 MD55, 3 MD54, 1 MD50
RN20 10X4: RMD23 8, RMD22 6, RMD18 4, RMD19 2 → 7 MD23, 5 MD22, 3 MD18, 1 MD19
RN7 10X2: RDQM6 4, RDQS6 2 → 3 DQM6, 1 DQS6
RN21 10X2: RDQM2 4, RDQS2 2 → 3 DQM2, 1 DQS2
RN8 10X4: RMD48 8, RMD53 6, RMD52 4, RMD49 2 → 7 MD48, 5 MD53, 3 MD52, 1 MD49
RN22 10X4: RMD20 8, RMD21 6, RMD16 4, RMD17 2 → 7 MD20, 5 MD21, 3 MD16, 1 MD17
RN9 10X4: RMD43 8, RMD47 6, RMD42 4, RMD46 2 → 7 MD43, 5 MD47, 3 MD42, 1 MD46
RN23 10X4: RMD11 8, RMD14 6, RMD10 4, RMD15 2 → 7 MD11, 5 MD14, 3 MD10, 1 MD15
RN10 10X2: RDQM5 4, RDQS5 2 → 3 DQM5, 1 DQS5
RN24 10X2: RDQM1 4, RDQS1 2 → 3 DQM1, 1 DQS1
RN11 10X4: RMD45 8, RMD40 6, RMD41 4, RMD44 2 → 7 MD45, 5 MD40, 3 MD41, 1 MD44
RN25 10X4: RMD12 8, RMD13 6, RMD9 4, RMD8 2 → 7 MD12, 5 MD13, 3 MD9, 1 MD8
RN12 10X4: RMD38 8, RMD39 6, RMD35 4, RMD34 2 → 7 MD38, 5 MD39, 3 MD35, 1 MD34
RN26 10X4: RMD7 8, RMD2 6, RMD3 4, RMD6 2 → 7 MD7, 5 MD2, 3 MD3, 1 MD6
RN13 10X2: RDQM4 4, RDQS4 2 → 3 DQM4, 1 DQS4
RN27 10X2: RDQS0 4, RDQM0 2 → 3 DQS0, 1 DQM0
RN14 10X4: RMD32 8, RMD33 6, RMD37 4, RMD36 2 → 7 MD32, 5 MD33, 3 MD37, 1 MD36
RN28 10X4: RMD5 8, RMD4 6, RMD0 4, RMD1 2 → 7 MD5, 5 MD4, 3 MD0, 1 MD1

QUANTA COMPUTER

Title	Alviso (DDR)		
Size	Document Number VM7		Rev 2B
Date:	Thursday, July 14, 2005	Sheet 7 of 45	


08
U8H
ALVISO
POWER
Change material
Place it close to U8.E19 and U8.G19
Place it closed to U8.E19&U8.G19
Note: All VCCSM pins shorted internally.
Note: All VCCSM pins shorted internally.
Refer chekc list V1_601 P.33
QUANTA COMPUTER
Title
Alviso (Power)
Size
Document Number
VM7
Rev
2B
Date: Thursday, July 14, 2005
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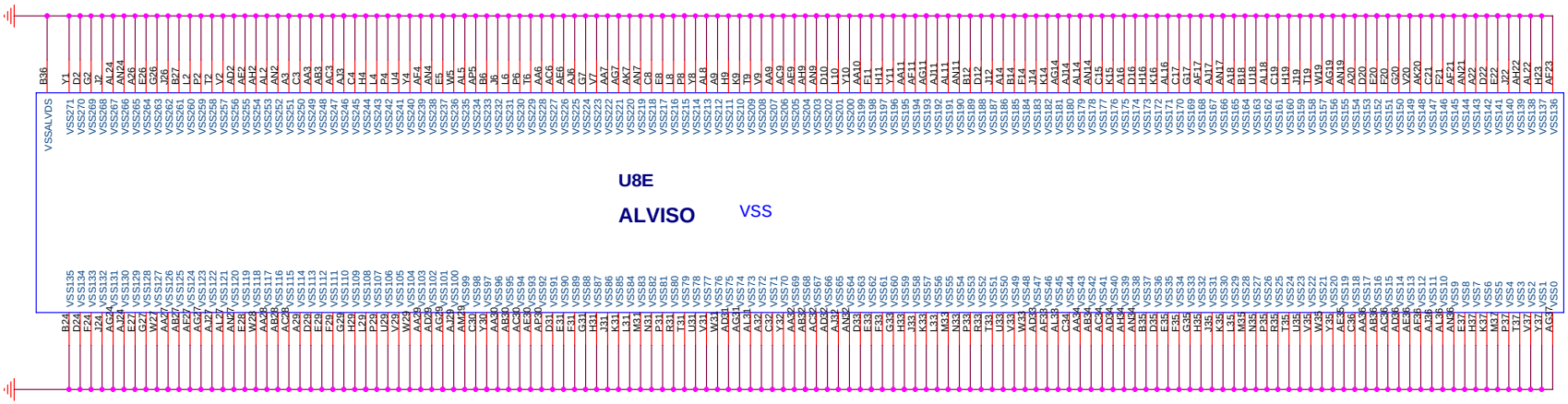

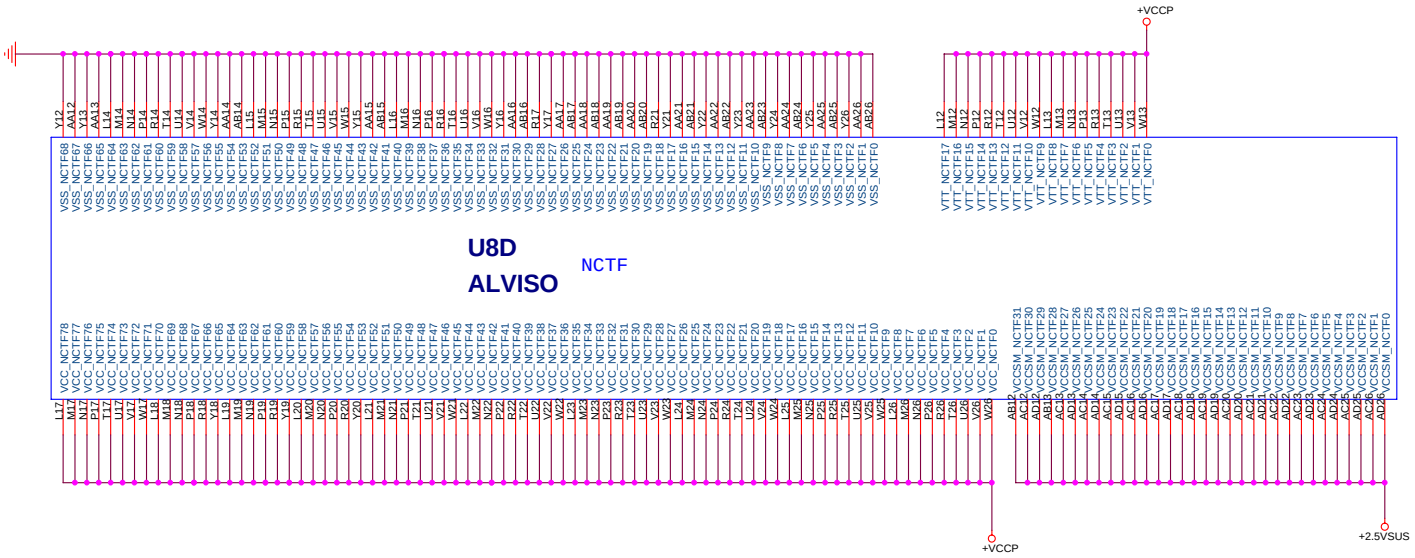

Title	Alviso (VSS/NC)		
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QUANTA COMPUTER

DDR TERMINATOR

RMD[0..63] RMD[0..63] 7,11,12
RDQM[0..7] RDQM[0..7] 7,11,12
RDQS[0..7] RDQS[0..7] 7,11,12

MAA[0..13] MAA[0..13] 7,12
-CSA[0..3] -CSA[0..3] 6,11,12
MAB[0..13] MAB[0..13] 7,11
CKE[0..3] CKE[0..3] 6,11,12

SMDDR_VTERM

RN35 56X4: RMD62 RMD59 RMD63 RMD58 / RMD61 RMD57 RMD60 RMD56
RN37 56X4
RN40 56X4: RMD49 RMD52 RMD53 RMD48 / RMD55 RMD51 RMD54 RMD50
RN38 56X4
RN41 56X4: RMD46 RMD43 RMD47 RMD42 / B_BS1# B_BS0# -CSA3 -DCASB → B_BS1# 7,11; B_BS0# 7,11; -DCASB 7,11
RN29 56X4
RN44 56X4: RMD34 RMD35 RMD39 RMD38 / RMD40 RMD41 RMD44 RMD45
RN43 56X4
RN47 56X4: MAA3 MAA10 A_BS1# MAA2 / RMD32 RMD33 RMD37 RMD36 (7,12 A_BS1#)
RN46 56X4
RN53 56X4: RMD24 RMD29 RMD28 RMD25 / RMD12 RMD13 RMD8 RMD9
RN59 56X4
RN51 56X4: RMD27 RMD26 RMD30 RMD31 / MAB12 MAB13 X CKE3
RN34 56X4
RN56 56X4: RMD16 RMD17 RMD20 RMD21 / A_BS0# -DMWA -CSA0 -CSA1 → A_BS0# 7,12; -DMWA 7,12
RN15 56X4
RN57 56X4: RMD15 RMD10 RMD14 RMD11 / MAA4 MAA0 MAA5 MAA7
RN48 56X4
RN62 56X4: RMD4 RMD0 RMD5 RMD1 / -DCASA -DRASA X MAA1 → -DCASA 7,12; -DRASA 7,12
RN16 56X4
RN33 56X4: MAB9 MAB7 MAB5 MAB3 / RMD23 RMD22 RMD18 RMD19
RN54 56X4
RN30 56X4: MAB0 -DRASB MAB4 MAB2 / RMD7 RMD2 RMD6 RMD3 (7,11 -DRASB)
RN60 56X4
RN32 56X4: MAB1 MAB10 -DMWB -CSA2 / MAB6 MAB8 MAB11 CKE2 (7,11 -DMWB)
RN31 56X4
RN49 56X4: MAA12 MAA11 MAA6 MAA8 / MAA9 MAA13 CKE1 CKE0
RN50 56X4

RN39 56X2: RDQM6 RDQS6 / RDQM7 RDQS7
RN36 56X2
RN45 56X2: RDQM4 RDQS4 / RDQM5 RDQS5
RN42 56X2
RN55 56X2: RDQS2 RDQM2 / RDQM3 RDQS3
RN52 56X2
RN61 56X2: RDQM0 RDQS0 / RDQM1 RDQS1
RN58 56X2

SMDDR_VTERM

C295 .1U/10V/0402
C297 .1U/10V/0402
C299 .1U/10V/0402
C301 .1U/10V/0402
C240 .1U/10V/0402
C284 .1U/10V/0402
C285 .1U/10V/0402
C290 .1U/10V/0402
C296 .1U/10V/0402
C298 .1U/10V/0402
C300 .1U/10V/0402
C302 .1U/10V/0402
C250 .1U/10V/0402
C257 .1U/10V/0402
C286 .1U/10V/0402
C239 .1U/10V/0402

C303 .1U/10V/0402
C305 .1U/10V/0402
C309 .1U/10V/0402
C313 .1U/10V/0402
C283 .1U/10V/0402
C306 .1U/10V/0402
C310 .1U/10V/0402
C314 .1U/10V/0402
C304 .1U/10V/0402
C307 .1U/10V/0402
C311 .1U/10V/0402
C315 .1U/10V/0402
C275 .1U/10V/0402
C308 .1U/10V/0402
C312 .1U/10V/0402
C294 .1U/10V/0402

C316 .1U/10V/0402
C320 .1U/10V/0402
C324 .1U/10V/0402
C328 .1U/10V/0402
C317 .1U/10V/0402
C321 .1U/10V/0402
C325 .1U/10V/0402
C330 .1U/10V/0402
C318 .1U/10V/0402
C322 .1U/10V/0402
C326 .1U/10V/0402
C331 .1U/10V/0402
C319 .1U/10V/0402
C323 .1U/10V/0402
C327 .1U/10V/0402
C332 .1U/10V/0402

+2.5VSUS

C245 .1U/10V/0402
C249 .1U/10V/0402
C260 .1U/10V/0402
C269 .1U/10V/0402
C246 .1U/10V/0402
C273 .1U/10V/0402
C254 .1U/10V/0402
C270 .1U/10V/0402
C247 .1U/10V/0402
C251 .1U/10V/0402
C252 .1U/10V/0402
C274 .1U/10V/0402
C248 .1U/10V/0402
C258 .1U/10V/0402
C253 .1U/10V/0402
C271 .1U/10V/0402

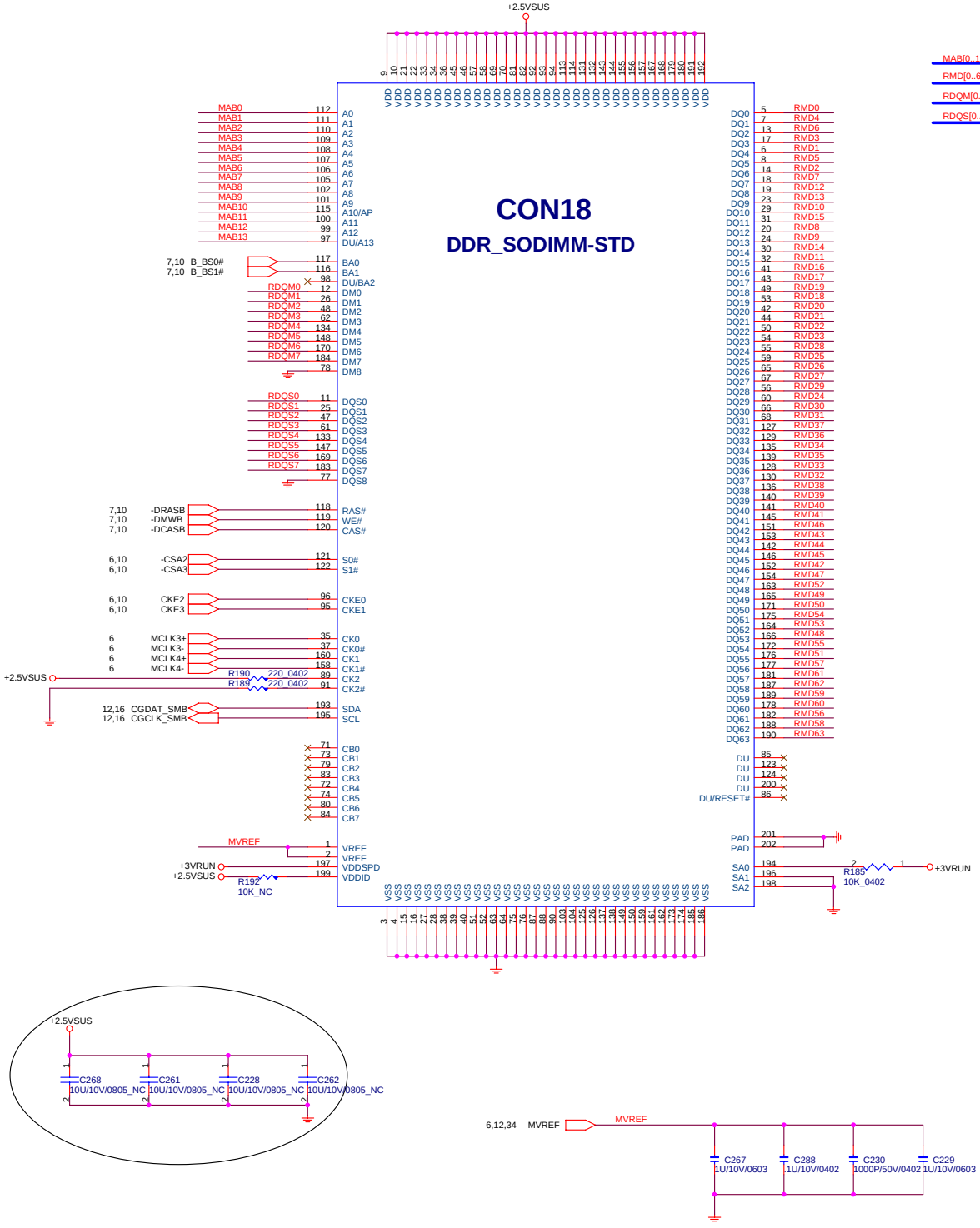
C272 .1U/10V/0402
C263 150U/6.3V/45mO
Footprint wrong

C278 .1U/10V/0402
C277 .1U/10V/0402
C259 .1U/10V/0402
C333 .1U/10V/0402
C266 .1U/10V/0402
C281 .1U/10V/0402
C282 .1U/10V/0402
C256 .1U/10V/0402
C293 .1U/10V/0402
C280 .1U/10V/0402
C329 .1U/10V/0402
C265 .1U/10V/0402
C291 .1U/10V/0402
C279 .1U/10V/0402
C276 .1U/10V/0402
C238 .1U/10V/0402

QUANTA COMPUTER

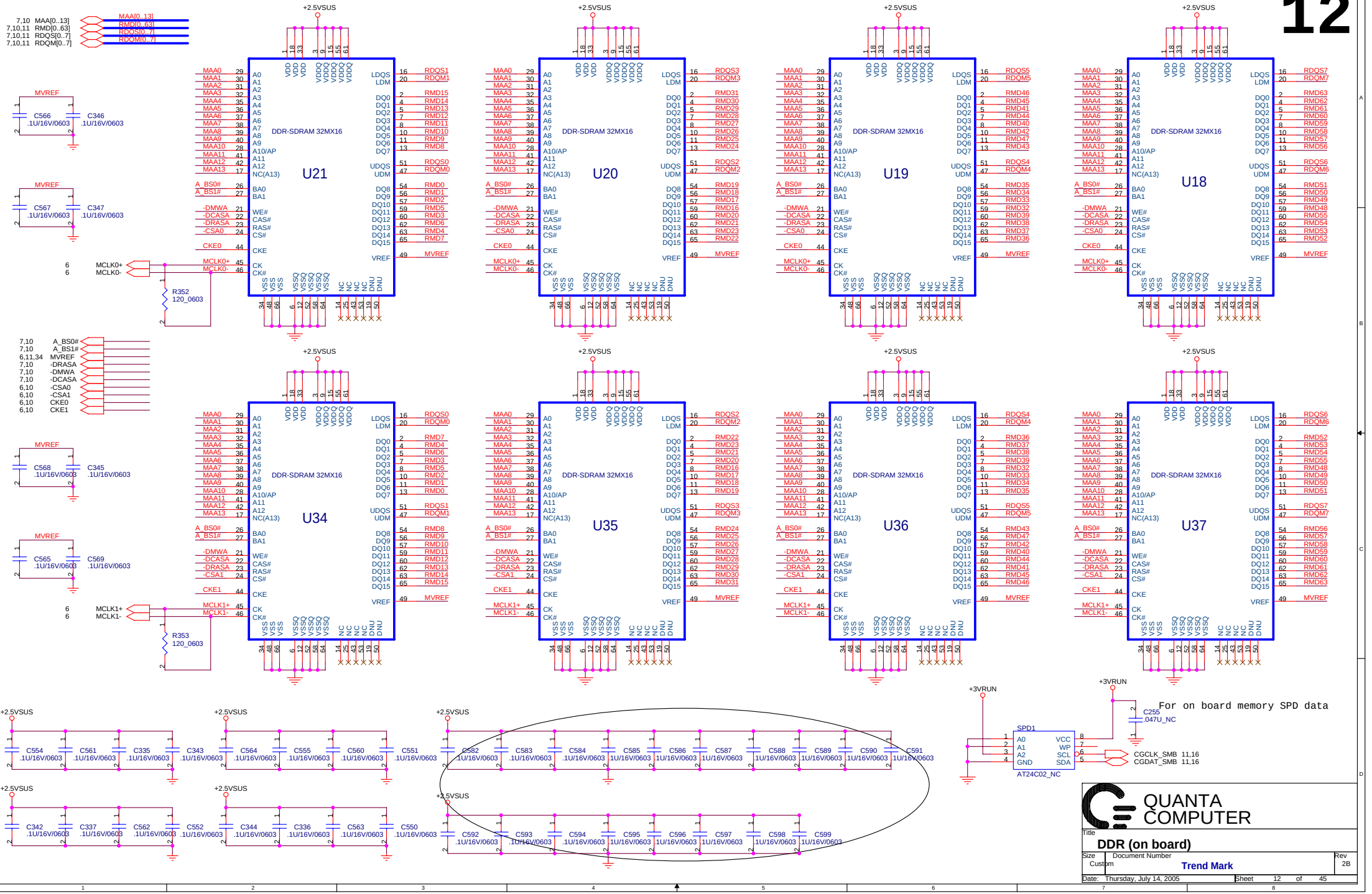
Title: DDR Terminators
Size: Custom | Document Number: Trend Mark | Rev: 2B
Date: Thursday, July 14, 2005 | Sheet 10 of 45

DDR - Modules



Title	Memory - SODIMM
Size	Custom
Document Number	Trend Mark
Rev	2B
Date	Thursday, July 14, 2005
Sheet	11 of 45

QUANTA COMPUTER

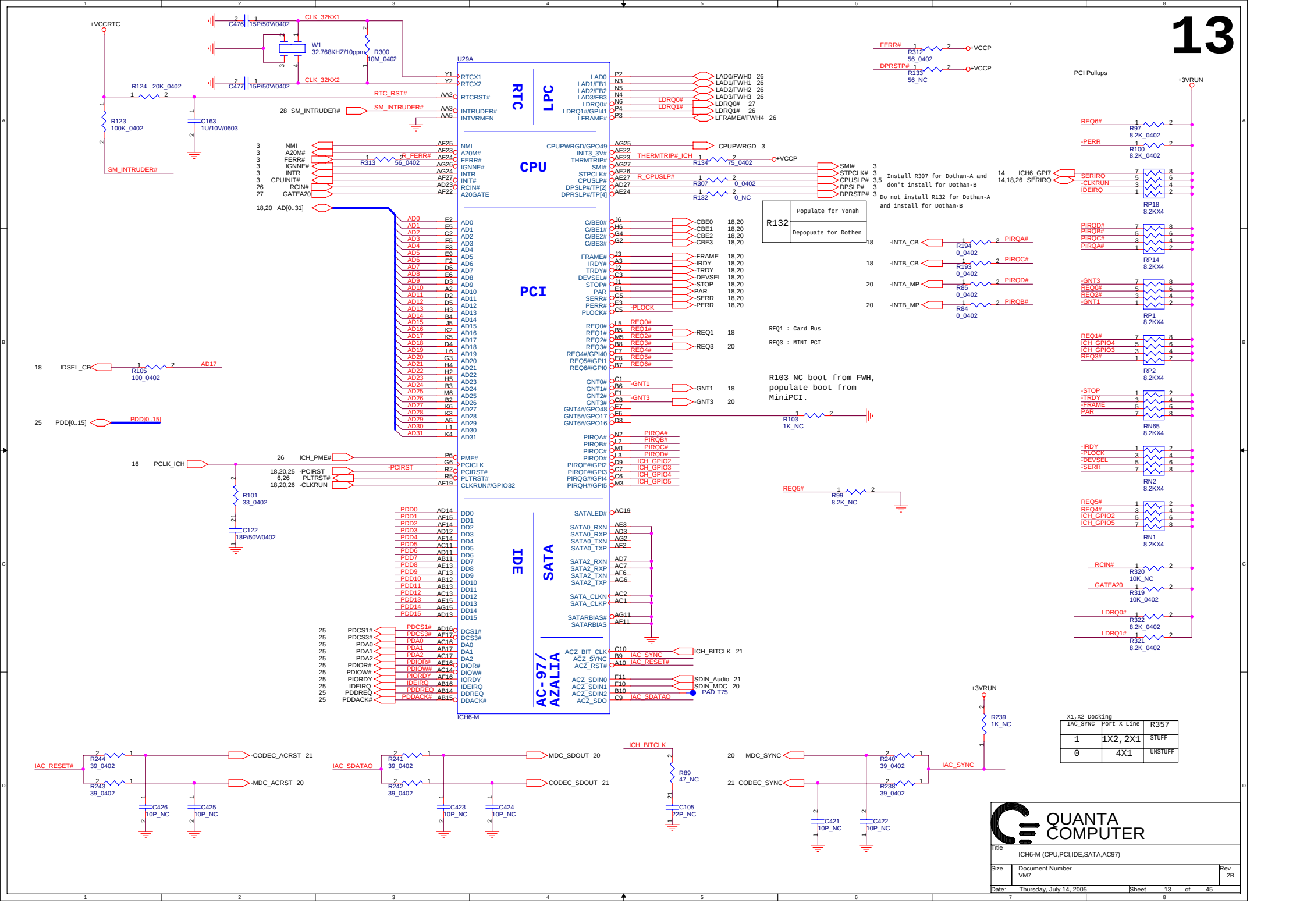


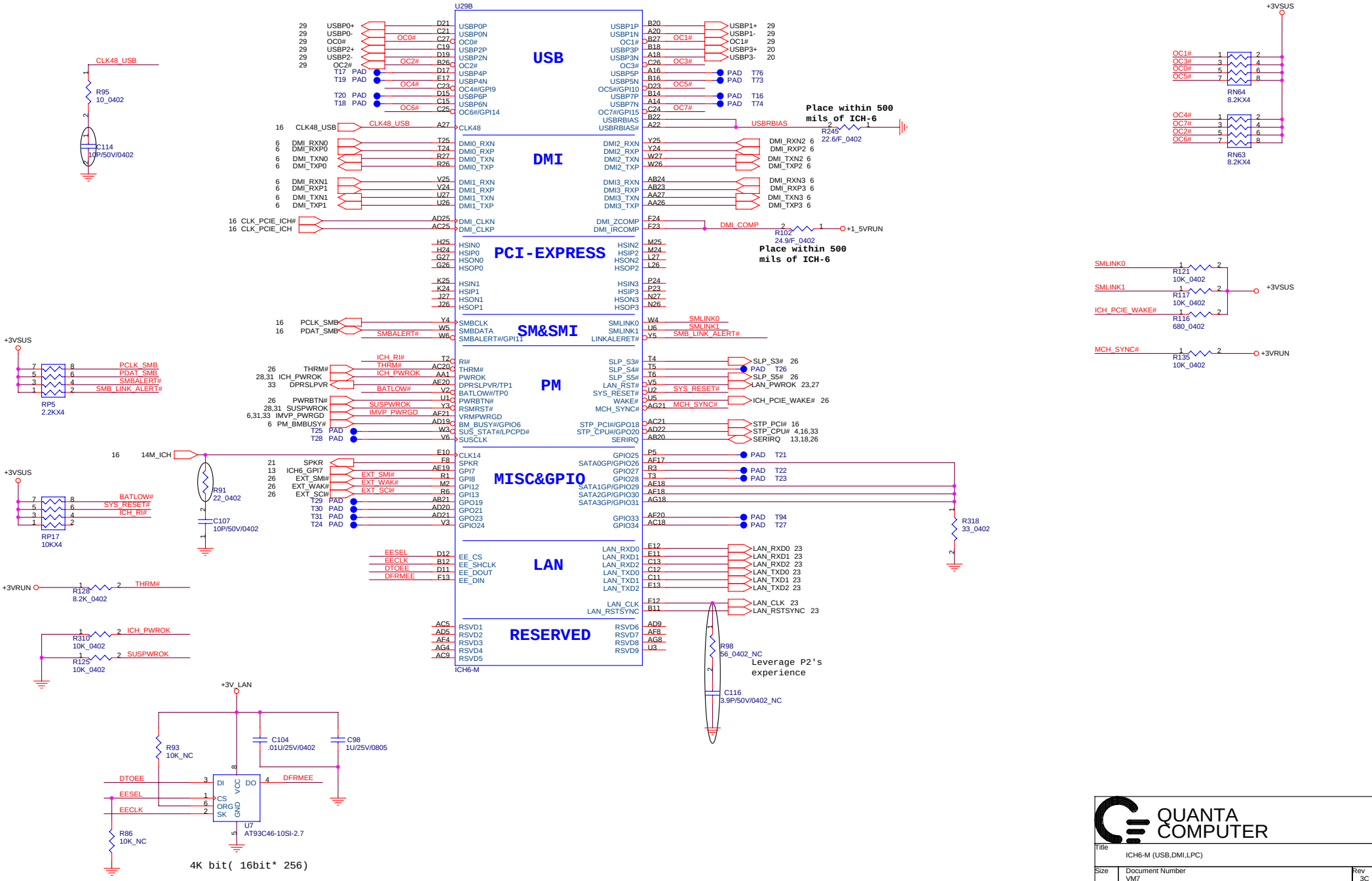
QUANTA COMPUTER

Title: DDR (on board)

Size	Document Number	Rev
Custom	Trend Mark	2B

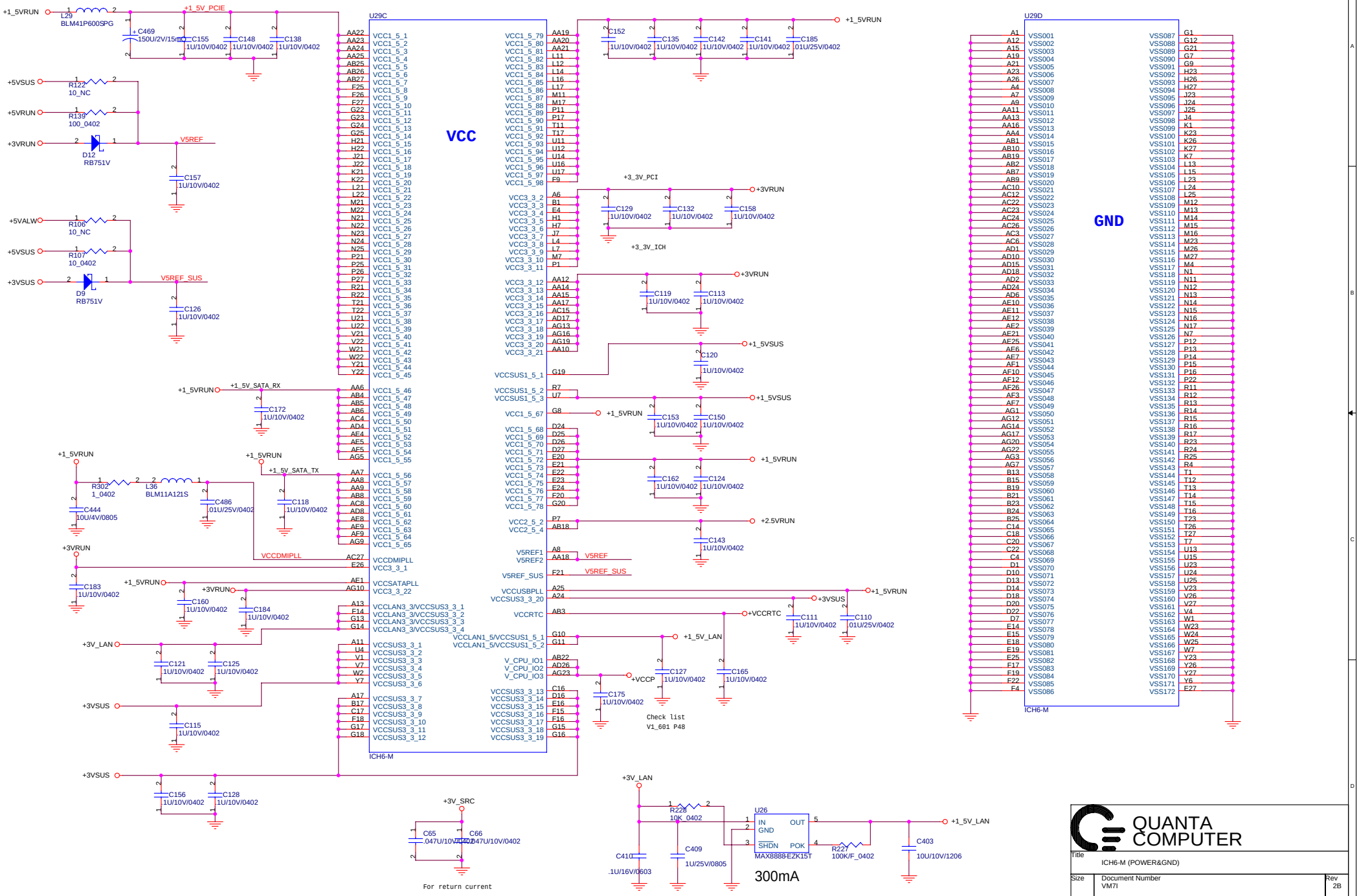
Date: Thursday, July 14, 2005 Sheet 12 of 45


13
U29A
RTC
LPC
CPU
PCI
IDE
SATA
AC-97/
AZALIA
ICH6-M
+VCCRTC
W1
32.768KHZ/10ppm
C476 15P/50V/0402
C477 15P/50V/0402
R300
10M_0402
CLK_32KX1
CLK_32KX2
R124 20K_0402
R123
100K_0402
C163
1U/10V/0603
RTC_RST#
SM_INTRUDER#
28 SM_INTRUDER#
RTCX1
RTCX2
RTCRST#
INTRUDER#
INTVRMEN
LAD0
LAD1/FB1
LAD2/FB2
LAD3/FB3
LDRQ0#
LDRQ1#/GPI41
LFRAME#
LAD0/FWH0 26
LAD1/FWH1 26
LAD2/FWH2 26
LAD3/FWH3 26
LDRQ0# 27
LDRQ1# 26
LFRAME#/FWH4 26
NMI
A20M#
FERR#
IGNNE#
INTR
INIT#
RCIN#
A20GATE
CPUPWRGD/GPO49
INIT3_3V#
THRMTRIP#
SMI#
STPCLK#
CPUSLP#
DPSLP#/TP[2]
DPRSLP#/TP[4]
CPUPWRGD 3
THERMTRIP#_ICH
R134 75_0402
SMI# 3
STPCLK# 3
CPUSLP# 3,5
DPSLP# 3
DPRSTP# 3
R_FERR#
R313 56_0402
R_CPUSLP#
R307 0_0402
R132 0_NC
Install R307 for Dothan-A and don't install for Dothan-B
Do not install R132 for Dothan-A and install for Dothan-B
R132
Populate for Yonah
Depopulate for Dothen
FERR#
DPRSTP#
R312 56_0402
R133 56_NC
+VCCP
PCI Pullups
+3VRUN
18,20 AD[0..31]
AD0..AD31
C/BE0#
C/BE1#
C/BE2#
C/BE3#
-CBE0 18,20
-CBE1 18,20
-CBE2 18,20
-CBE3 18,20
FRAME#
IRDY#
TRDY#
DEVSEL#
STOP#
PAR
SERR#
PERR#
PLOCK#
-FRAME 18,20
-IRDY 18,20
-TRDY 18,20
-DEVSEL 18,20
-STOP 18,20
-PAR 18,20
-SERR 18,20
-PERR 18,20
-PLOCK
REQ0#
REQ1#
REQ2#
REQ3#
REQ4#/GPI40
REQ5#/GPI1
REQ6#/GPI0
-REQ1 18
-REQ3 20
REQ1 : Card Bus
REQ3 : MINI PCI
R103 NC boot from FWH, populate boot from MiniPCI.
R103 1K_NC
GNT0#
GNT1#
GNT2#
GNT3#
GNT4#/GPO48
GNT5#/GPO17
GNT6#/GPO16
-GNT1
-GNT3
-GNT1 18
-GNT3 20
PIRQA#
PIRQB#
PIRQC#
PIRQD#
PIRQE#/GPI2
PIRQF#/GPI3
PIRQG#/GPI4
PIRQH#/GPI5
ICH_GPIO2
ICH_GPIO3
ICH_GPIO4
ICH_GPIO5
REQ5# R99 8.2K_NC
18 IDSEL_CB
R105 100_0402
AD17
25 PDD[0..15]
PDD[0..15]
16 PCLK_ICH
R101 33_0402
C122 18P/50V/0402
26 ICH_PME#
18,20,25 -PCIRST
6,26 PLTRST#
18,20,26 -CLKRUN
PME#
PCICLK
PCIRST#
PLTRST#
CLKRUN#/GPIO32
-PCIRST
PDD0..PDD15
DD0..DD15
SATALED#
SATA0_RXN
SATA0_RXP
SATA0_TXN
SATA0_TXP
SATA2_RXN
SATA2_RXP
SATA2_TXN
SATA2_TXP
SATA_CLKN
SATA_CLKP
SATARBIAS#
SATARBIAS
25 PDCS1#
25 PDCS3#
25 PDA0
25 PDA1
25 PDA2
25 PDIOR#
25 PDIOW#
25 PIORDY
25 IDEIRQ
25 PDDREQ
25 PDDACK#
DCS1#
DCS3#
DA0
DA1
DA2
DIOR#
DIOW#
IORDY
IDEIRQ
DDREQ
DDACK#
ACZ_BIT_CLK
ACZ_SYNC
ACZ_RST#
ACZ_SDIN0
ACZ_SDIN1
ACZ_SDIN2
ACZ_SDO
IAC_SYNC
IAC_RESET#
IAC_SDATAO
ICH_BITCLK 21
SDIN_Audio 21
SDIN_MDC 20
PAD T75
-INTA_CB 18
-INTB_CB 18
-INTA_MP 20
-INTB_MP 20
R194 0_0402
R193 0_0402
R85 0_0402
R84 0_0402
PIRQA#
PIRQC#
PIRQD#
PIRQB#
SERIRQ
-CLKRUN
IDEIRQ
14 ICH6_GPI7
14,18,26 SERIRQ
RP18 8.2K4
RP14 8.2K4
RP1 8.2K4
RP2 8.2K4
RN65 8.2K4
RN2 8.2K4
RN1 8.2K4
REQ6#
-PERR
-GNT3
REQ0#
REQ2#
-GNT1
REQ1#
ICH_GPIO4
ICH_GPIO3
REQ3#
-STOP
-TRDY
-FRAME
PAR
-IRDY
-PLOCK
-DEVSEL
-SERR
REQ5#
REQ4#
ICH_GPIO2
ICH_GPIO5
R97 8.2K_0402
R100 8.2K_0402
RCIN#
GATEA20
LDRQ0#
LDRQ1#
R320 10K_NC
R319 10K_0402
R322 8.2K_0402
R321 8.2K_0402
X1,X2 Docking
IAC_SYNC | Port X Line | R357
1 | 1X2,2X1 | STUFF
0 | 4X1 | UNSTUFF
R239 1K_NC
R244 39_0402
R243 39_0402
R241 39_0402
R242 39_0402
R89 47_NC
R240 39_0402
R238 39_0402
-CODEC_ACRST 21
-MDC_ACRST 20
MDC_SDOUT 20
CODEC_SDOUT 21
20 MDC_SYNC
21 CODEC_SYNC
C426 10P_NC
C425 10P_NC
C423 10P_NC
C424 10P_NC
C105 22P_NC
C421 10P_NC
C422 10P_NC
QUANTA COMPUTER
Title
ICH6-M (CPU,PCI,IDE,SATA,AC97)
Size
Document Number
VM7
Rev
2B
Date: Thursday, July 14, 2005
Sheet 13 of 45



Title	ICH6-M (USB,DMI,LPC)
Size	Document Number VM7
Rev	3C
Date:	Thursday, July 14, 2005
Sheet	14 of 45

QUANTA COMPUTER


U29C
VCC
ICH6-M
U29D
GND
ICH6-M
+1_5VRUN
+1_5V_PCIE
L29
BLM41P600SPG
+5VSUS
+5VRUN
+3VRUN
R122
10_NC
R139
100_0402
D12
RB751V
V5REF
+5VALW
R106
10_NC
R107
10_0402
D9
RB751V
V5REF_SUS
+1_5V_SATA_RX
+1_5V_SATA_TX
R302
1_0402
L36
BLM11A121S
VCCDMIPLL
+3V_LAN
+3VSUS
+3V_SRC
+3_3V_PCI
+3_3V_ICH
+2.5VRUN
+1_5V_LAN
+VCCP
+VCCRTC
+3VSUS
Check list
V1_601 P48
For return current
U26
MAX8888-EZK15T
300mA
R228
10K_0402
R227
100K/F_0402
C410
.1U/16V/0603
C409
1U/25V/0805
C403
10U/10V/1206
QUANTA COMPUTER
Title
ICH6-M (POWER&GND)
Size
Document Number
VM7I
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2B
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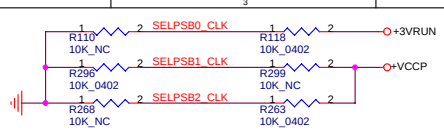
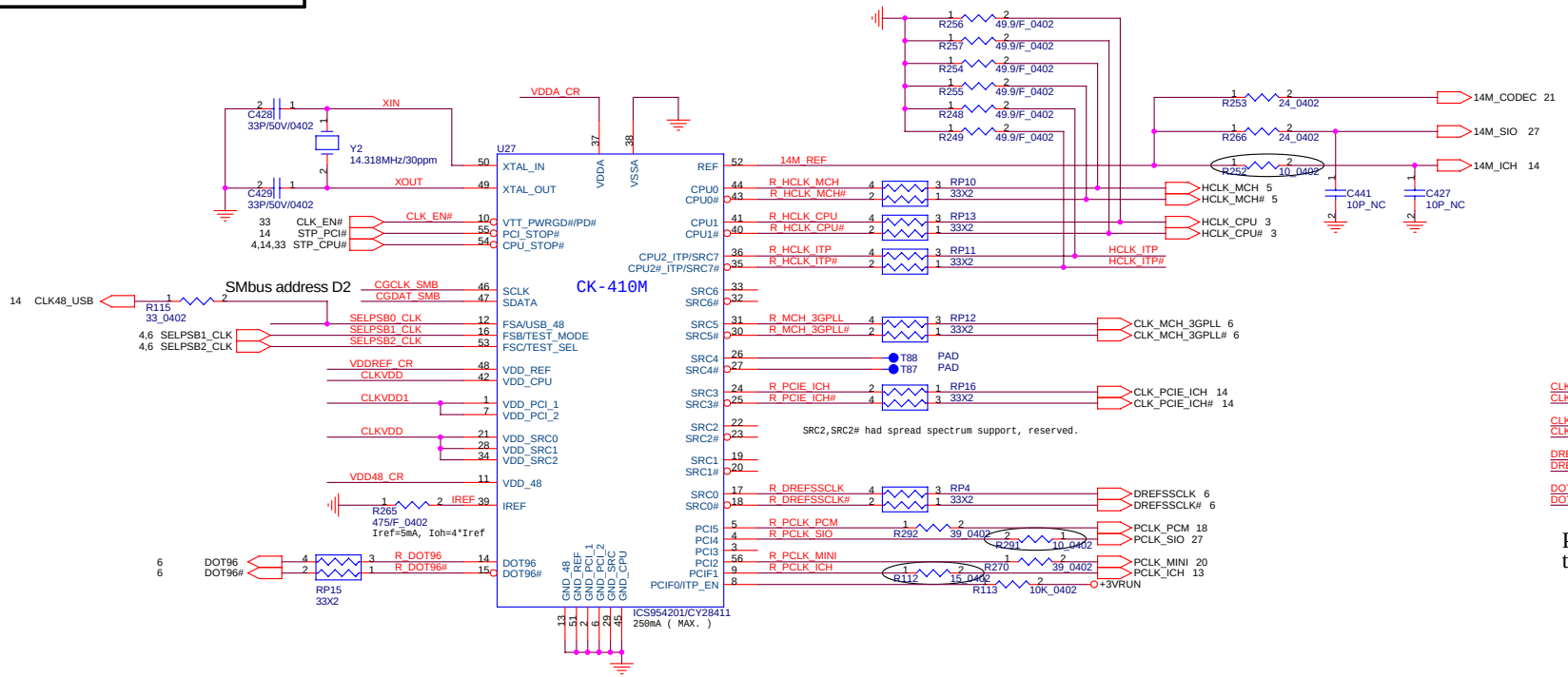
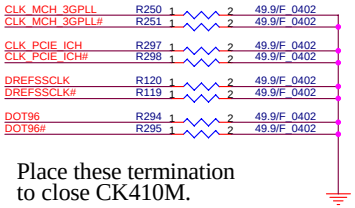
FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33



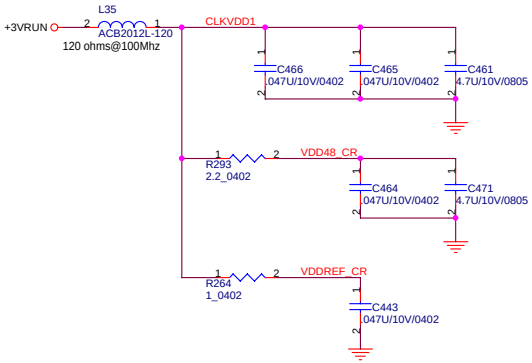
Depop R299 for Dothan-B

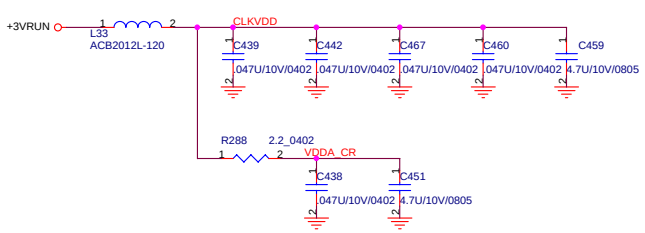
Place these termination to close CK410M.

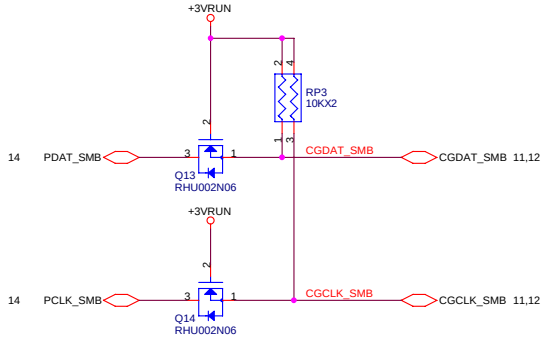




Place these termination to close CK410M.



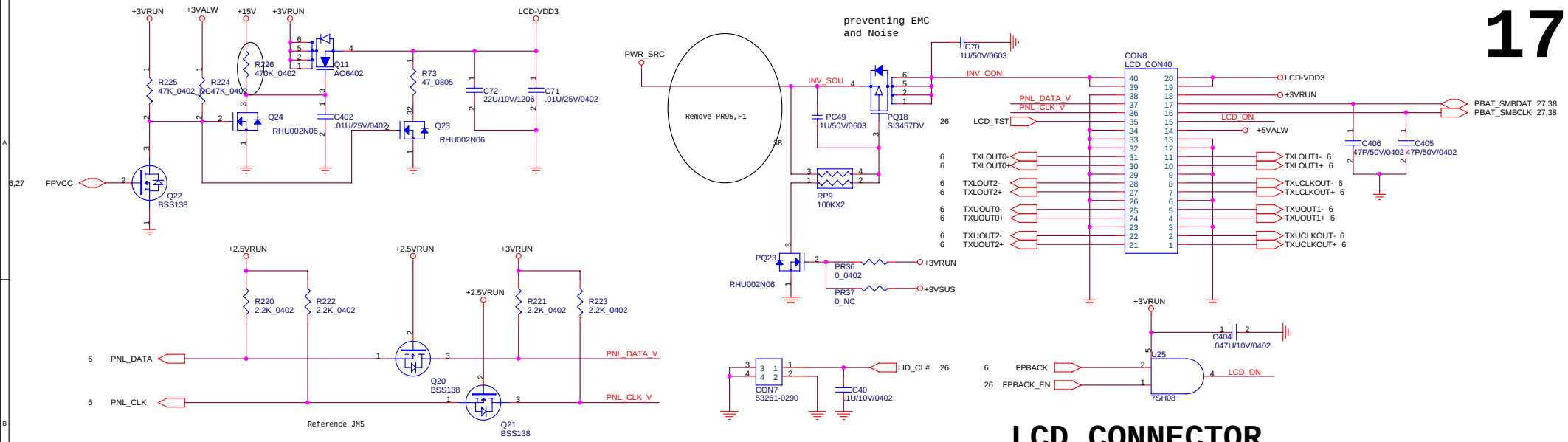




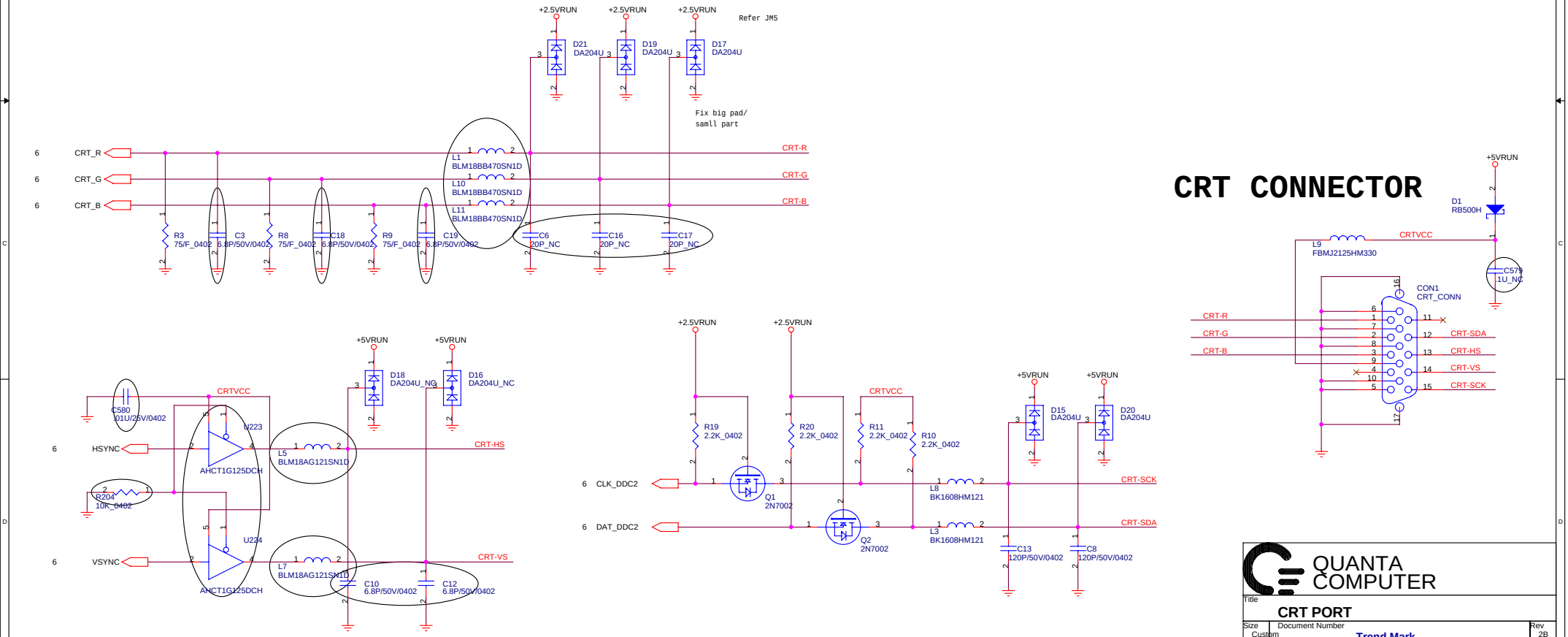
These are for backdrive issue

QUANTA COMPUTER

Title	CLOCK GENERATOR		
Size	Document Number VM7		Rev 2B
Date: Thursday, July 14, 2005		Sheet 16 of 45	



LCD CONNECTOR



CRT CONNECTOR

QUANTA COMPUTER

Title: CRT PORT

Size	Document Number	Rev
Custom	Trend Mark	2B

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PCAD[0..15] 19

PCAA[0..25] 19

13,20 AD[0..31]

U32A
PCI1510GVF

AD0 R9
AD1 U9
AD2 V9
AD3 W9
AD4 V8
AD5 U8
AD6 R8
AD7 W7
AD8 U7
AD9 P8
AD10 R7
AD11 V6
AD12 U6
AD13 V5
AD14 P7
AD15 R6
AD16 P1
AD17 N6
AD18 N3
AD19 N2
AD20 M5
AD21 M6
AD22 M3
AD23 M2
AD24 L3
AD25 L2
AD26 K6
AD27 K5
AD28 K3
AD29 K2
AD30 J6
AD31 J5

AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15 AD16 AD17 AD18 AD19 AD20 AD21 AD22 AD23 AD24 AD25 AD26 AD27 AD28 AD29 AD30 AD31

VCC1 A5
VCC2 A8
VCC3 A13
VCC4 E19
VCC5 G1
VCC6 H19
VCC7 L19
VCC8 M1
VCC9 R1
VCC10 W8

+3VSUS

VCCP L1
VCCP W5

1 R383 2 0_0402 +3VSUS
1 R384 2 0_0402_NC +3VRUN

AVD2 R11
AVD3 U13
AVD4 U14

PLLVDD P15

VCCCB A11
VCCCB G14

A_VCC

VCC1.8V G2
VCC1.8V L18

C341 .1U/10V/0402

VCCD# E6 -VCCD0
VCCD1# B5 -VCCD1
VPPD0 A4 VPPD0
VPPD1 C5 VPPD1

-VCCD0 19
-VCCD1 19
VPPD0 19
VPPD1 19

GND E1
GND K1
GND N1
GND W6
GND P19
GND K19
GND G19
GND A15
GND A10
GND A7

AGND2 U11
AGND3 R12
AGND4 R13

PLLGND N14

TEST0 U10
TEST1 R10

MFUNC0 F5 -INTA_CB 13
MFUNC1 G6 -INTB_CB 13
MFUNC2 F3 SERIRQ 13,14,26
MFUNC3 F2
MFUNC4 G5
MFUNC5 F1 -CLKRUN 13,20,26
MFUNC6 H6
CLK_48_RSVD F6

13,20 -CBE0 V7
13,20 -CBE1 U5
13,20 -CBE2 P2
13,20 -CBE3 L6

C/BE0# C/BE1# C/BE2# C/BE3#

13 IDSEL_CB L5
IDSEL

16 PCLK_PCM H1
PCLK

13,20 PAR W4
13,20 -SERR T1
13,20 -PERR R3
13,20 -STOP P5
13,20 -IRDY P3
13,20 -TRDY P6
13,20,25 -PCIRST H3
13,20 -DEVSEL R2
13,20 -FRAME N5
13 -GNT1 J1
13 -REQ1 J2

PAR SERR# PERR# STOP# IRDY# TRDY# PRST# DEVSEL# FRAME# GNT# REQ#

26 CBUS_GRST# 1 R347 2 0_0402 CBUS_GRST#_R
GRST# H2

-VR_EN H5
VR_EN# / RI# / PME# J3
SUSPEND# G3
SPKROUT E2
PHY_TEST_MA P18

+3VSUS +3VRUN
1 R196 2 47K_0402
21 -PCMSPK
1 R351 2 4.7K_0402

+3VSUS +3VSUS
R197 10K_0402
-PME/RI
20,26,27 PCI_PME# 3
Q17 2N7002

CON19 PCMCIA_Cage

U32B
PCI1510GVF

V12 TPA0P
W12 TPA0N
V11 TPB0P
W11 TPB0N
U12 TPBIAS0

V15 TPA1P
W15 TPA1N
V14 TPB1P
W14 TPB1N
U15 TPBIAS1

V10 PC0
W10 PC1
P9 PC2
W13 R0
V13 R1
P17 CNA
P10 CPS
T19 FILTER0
R17 FILTER1

R18 XI

R19 XO

B7 SC_CD#
F7 SC_CLK
A6 SC_DATA
C6 SC_FCB
E3 SCL
E7 SC_MODE
B6 SC_PWR
C7 SC_RST
D1 SDA

N15 MC_RSVD0
M14 MC_RSVD1
N17 MC_RSVD2
N18 MC_RSVD3
N19 MC_RSVD4
M15 MC_RSVD5
M17 MC_RSVD6
M18 MC_RSVD7
M19 MC_RSVD8

F5 NC
P11 NC
P12 NC
P13 NC
P14 NC
R14 NC
W16 NC

A_D0/CAD27 F9 PCAD0
A_D1/CAD29 B8 PCAD1
A_D2/RSVD F8 PCAD2
A_D3/CAD0 L15 PCAD3
A_D4/CAD1 K18 PCAD4
A_D5/CAD3 K15 PCAD5
A_D6/CAD5 J19 PCAD6
A_D7/CAD7 J17 PCAD7
A_D8/CAD28 E9 PCAD8
A_D9/CAD30 C8 PCAD9
A_D10/CAD31 E8 PCAD10
A_D11/CAD2 L14 PCAD11
A_D12/CAD4 K17 PCAD12
A_D13/CAD6 K14 PCAD13
A_D14/RSVD J18 PCAD14
A_D15/CAD8 J14 PCAD15

A_A0/CAD26 F11 PCAA0
A_A1/CAD25 E11 PCAA1
A_A2/CAD24 C11 PCAA2
A_A3/CAD23 A12 PCAA3
A_A4/CAD22 C12 PCAA4
A_A5/CAD21 E12 PCAA5
A_A6/CAD20 C13 PCAA6
A_A7/CAD18 E13 PCAA7
A_A8/CC/BE1# G15 PCAA8
A_A9/CAD14 F19 PCAA9
A_A10/CAD9 H18 PCAA10
A_A11/CAD12 H15 PCAA11
A_A12/CC/BE2# C14 PCAA12
A_A13/CPAR F14 PCAA13
A_A14/CPERR# F15 PCAA14
A_A15/CIRDY# F13 PCAA15
A_A16/CCLK C15 PCAA16
A_A17/CAD16 F18 PCAA17
A_A18/RSVD F17 PCAA18
A_A19/CBLOCK# E18 PCAA19
A_A20/CSTOP# E17 PCAA20
A_A21/CDEVSEL# A16 PCAA21
A_A22/CTRDY# E14 PCAA22
A_A23/CFRAME# B15 PCAA23
A_A24/CAD17 B14 PCAA24
A_A25/CAD19 A14 PCAA25

1 R350 2 22_0402 PCAA16
C549 22P_NC
PCAA16 19

A_BVD1/CSTSCHG A9 A_BVD1
A_BVD2/CAUDIO F10 A_BVD2
A_CD1#/CCD1# L17 -A_CD1
A_CD2#/CCD2# C9 -A_CD2
A_READY/CINT# C10 A_RDY
A_WAIT#/CSERR# E10 -A_WAIT
A_WP/CCLKRUN# B9 A_WP
A_INPACK/CREQ# B12 -A_INPACK

A_BVD1 19
A_BVD2 19
-A_CD1 19
-A_CD2 19
A_RDY 19
-A_WAIT 19
A_WP 19
-A_INPACK 19

A_CE1#/CC/BE0# J15 -A_CE1
A_CE2#/CAD10 H17 -A_CE2
A_WE#/CGNT# D19 -A_WE
A_IORD#/CAD13 G18 -AIORD
A_IOWR#/CAD15 G17 -AIOWR
A_OE#/CAD11 H14 -AOE
A_VS1#/CVS1 B10 A_VS1
A_VS2#/CVS2 E12 A_VS2
A_REG#/CC/BE3# B11 -AREG
A_RESET/CRST# B13 A_RESET

-A_CE1 19
-A_CE2 19
-A_WE 19
-AIORD 19
-AIOWR 19
-AOE 19
A_VS1 19
A_VS2 19
-AREG 19
A_RESET 19

A_VCC
A_WP 1 R349 2 47K_0402

PCLK_PCM 1 R354 2 33_NC
C571 9P_NC

+3VSUS 1 R199 2 10K_NC
1 R198 2 10K_0402 -VR_EN

MFUNC2 1 R195 2 10K_0402
MFUNC5 1 R348 2 10K_0402
+3VSUS

CBUS_GRST#_R 1 R191 2 0_NC -PCIRST

+3VSUS
C532 4.7U/10V/0805
C287 1U/10V/0402
C527 1U/10V/0402
C289 1U/10V/0402
C292 1U/10V/0402
C529 1U/10V/0402
C531 1U/10V/0402
C528 1U/10V/0402
C530 1U/10V/0402
C538 1U/10V/0402
C544 1U/10V/0402
C338 1U/10V/0402
C339 1U/10V/0402
C340 1U/10V/0402

A_VCC
C543 1000P/50V/0402
C334 1U/10V/0402

QUANTA COMPUTER

Title: PCI1510GVF

Size: Custom | Document Number: Trend Mark | Rev: 2B

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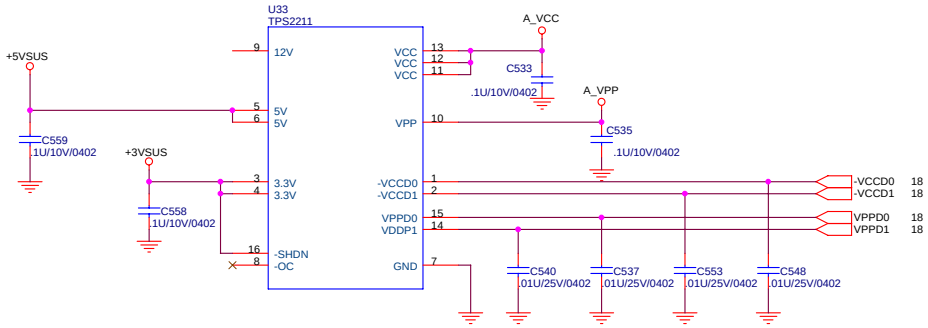
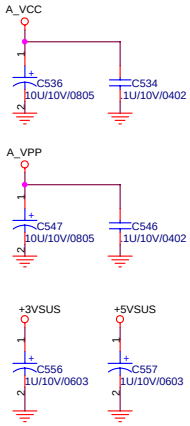
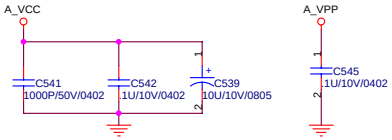
PCMCIA POWER SWITCH

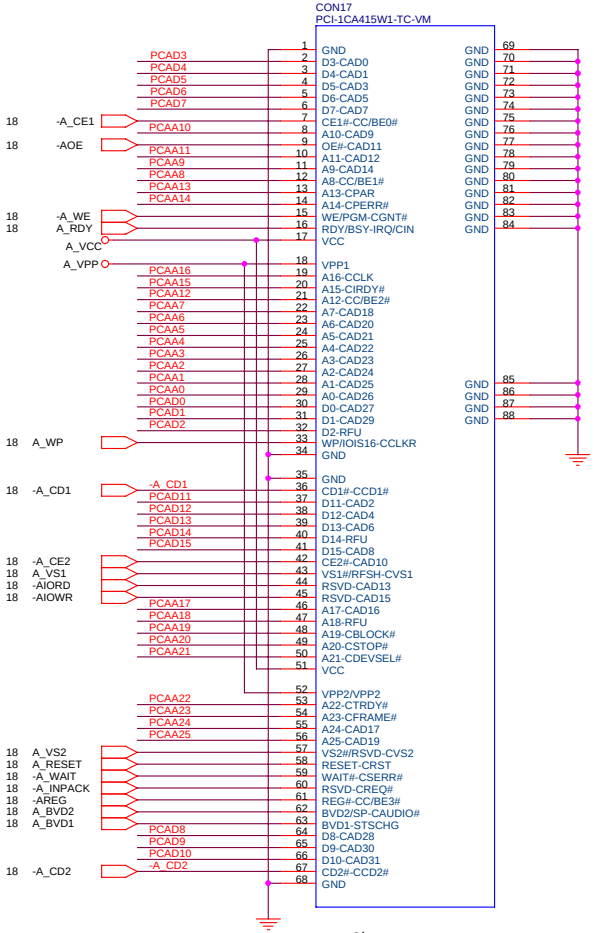


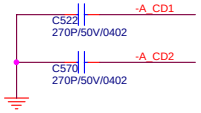


PCMCIA SOCKET

18 PCAA[0..25] PCAA[0..25]
18 PCAD[0..15] PCAD[0..15]



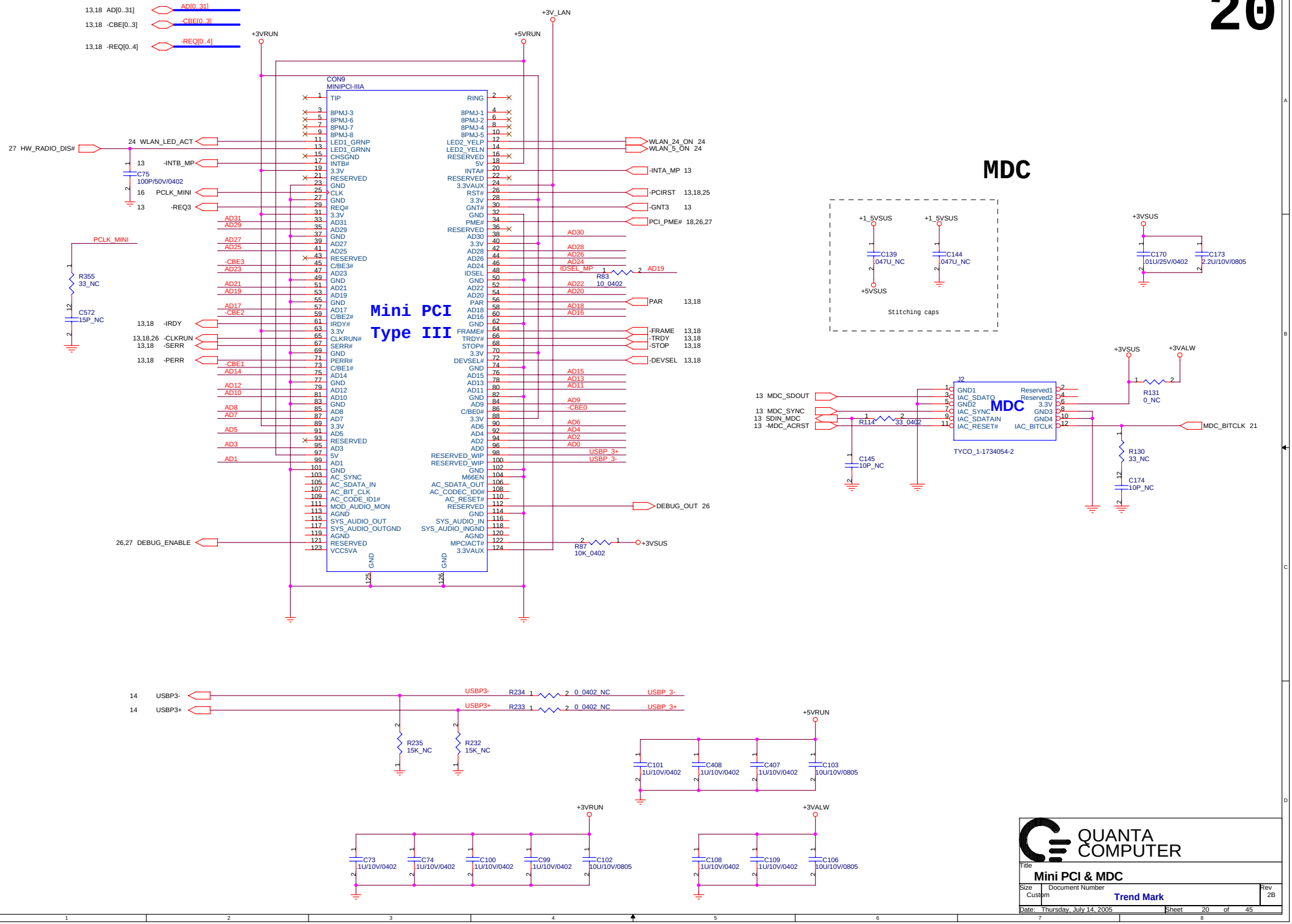




Change
PCMCIA Conn.

QUANTA COMPUTER

Title: PCMCIA SOCKET&POWER		
Size: Custom	Document Number: Trend Mark	Rev: 2B
Date: Thursday, July 14, 2005	Sheet 19 of 45	

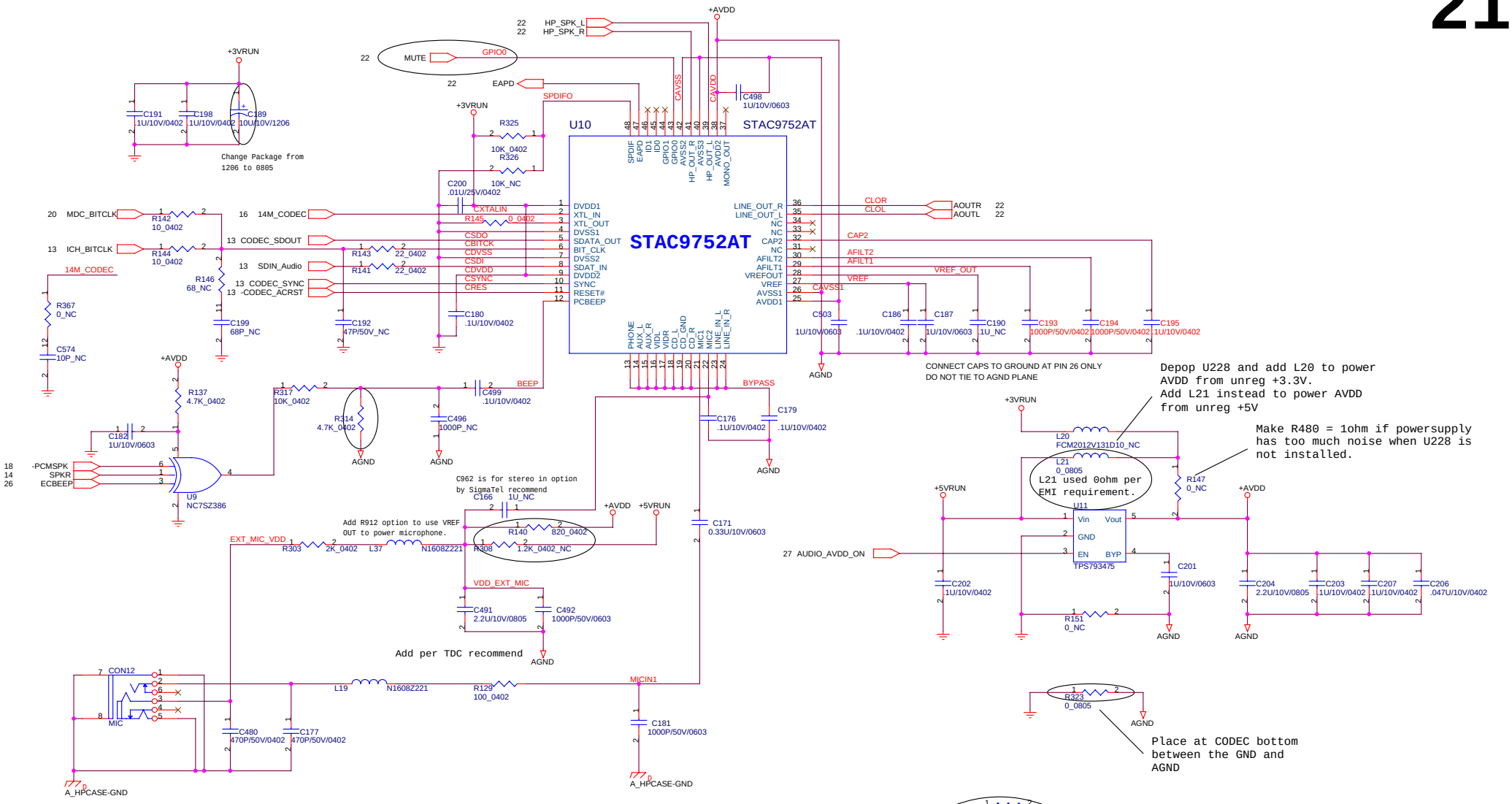


QUANTA COMPUTER

Title: Mini PCI & MDC

Size: Custom | Document Number: Trend Mark | Rev: 2B

Date: Thursday, July 14, 2005 | Sheet 20 of 45



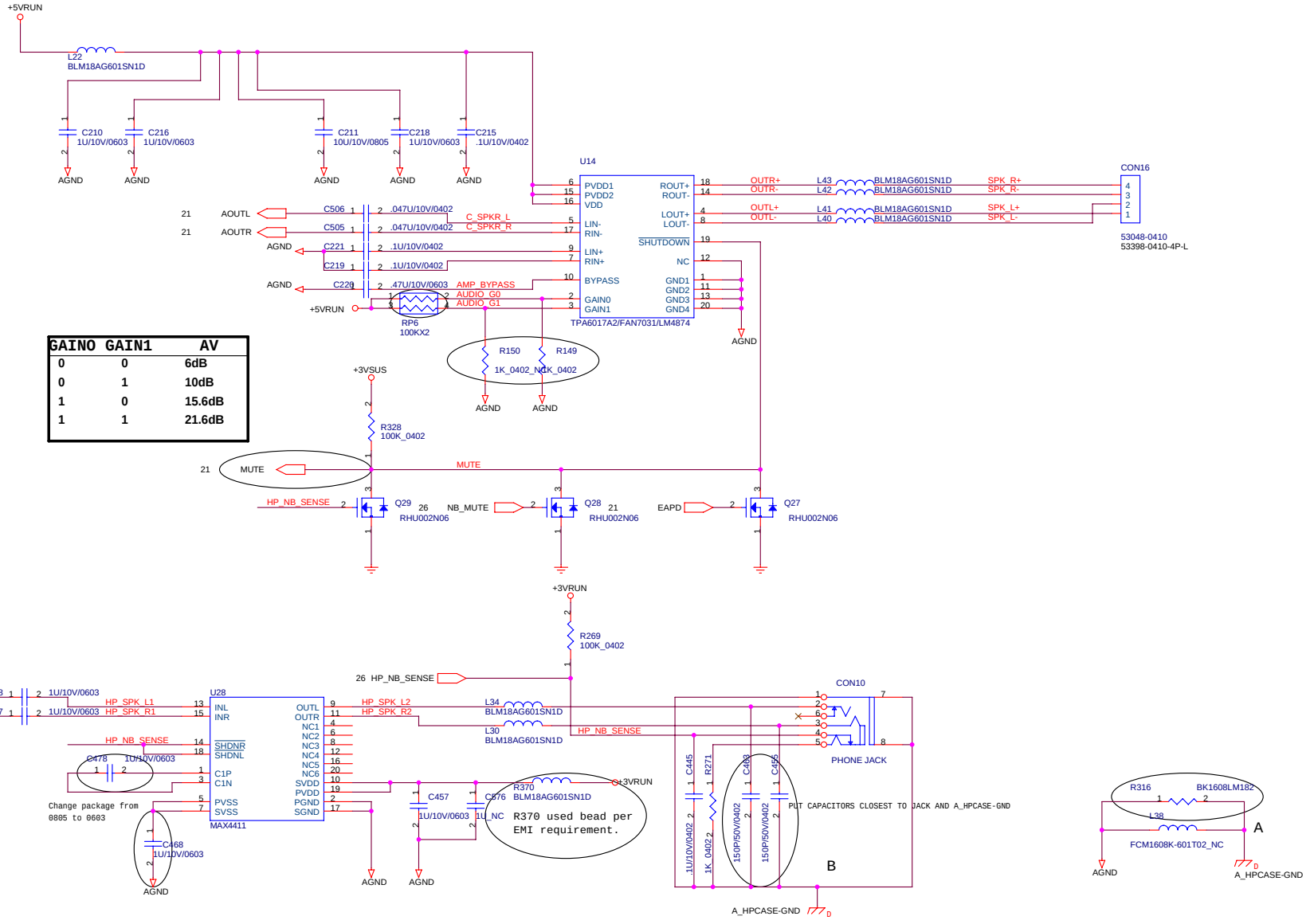
STAC9752A 48/32 DUAL LAYOUT

QUANTA COMPUTER

Title: **Audio Codec STAC9753A**

Size	Document Number	Rev
Custom	Trend Mark	2B

Date: Thursday, July 14, 2005 Sheet 21 of 45



GAINO	GAIN1	AV
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

QUANTA COMPUTER

Title: **AUDIO AMP&BUZZER&HP-Out**

Size	Document Number	Rev
Custom	Trend Mark	2B

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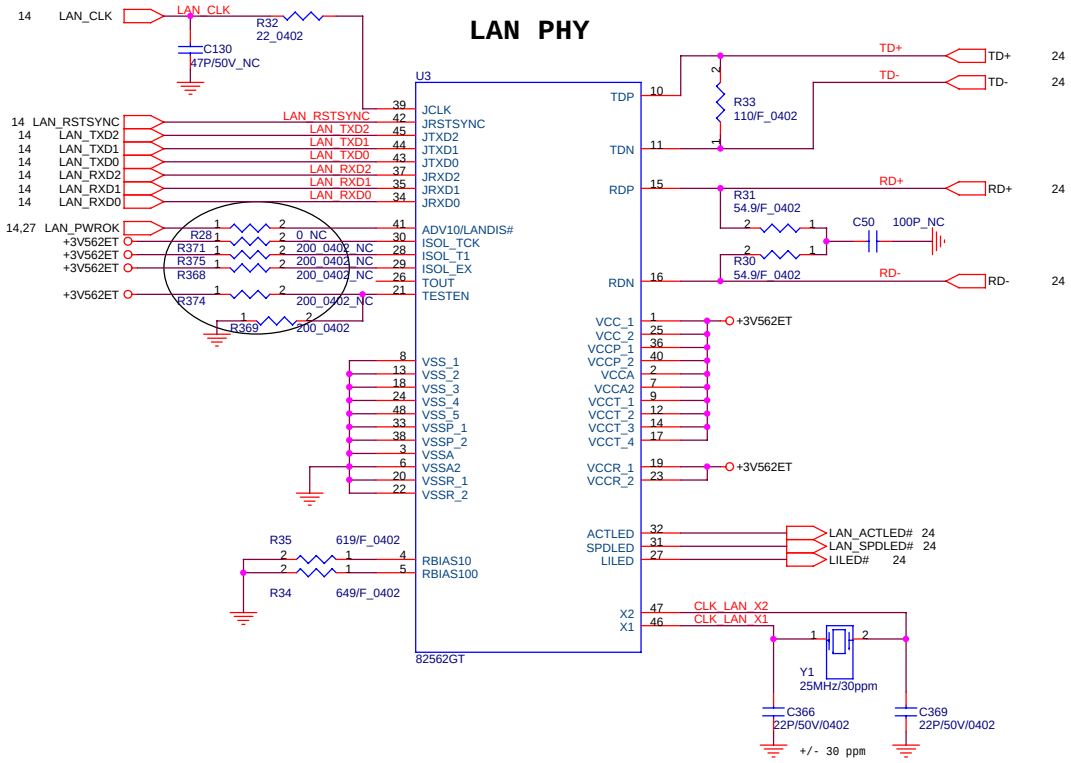
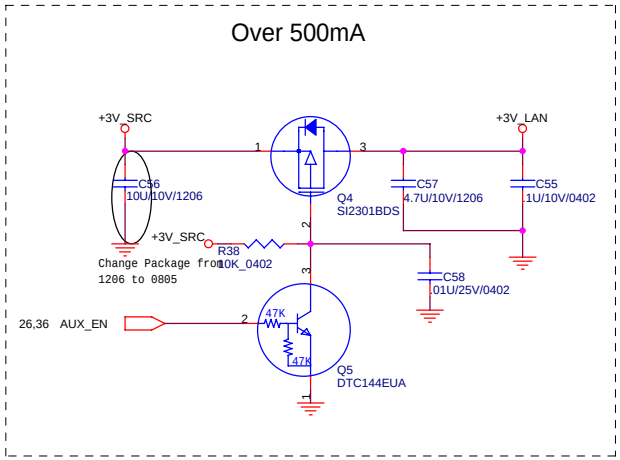
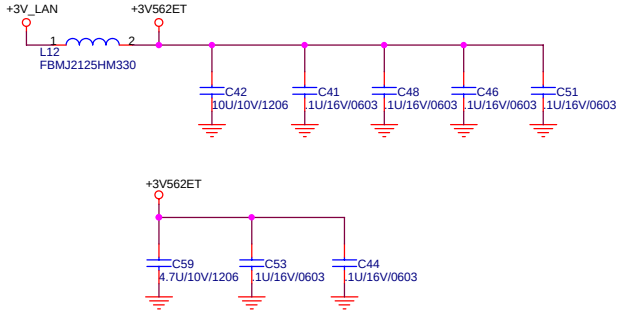
LAN PHY







QUANTA COMPUTER

Title	LAN INTERFACE	
Size: Custom	Document Number: VM7	Rev: 2B
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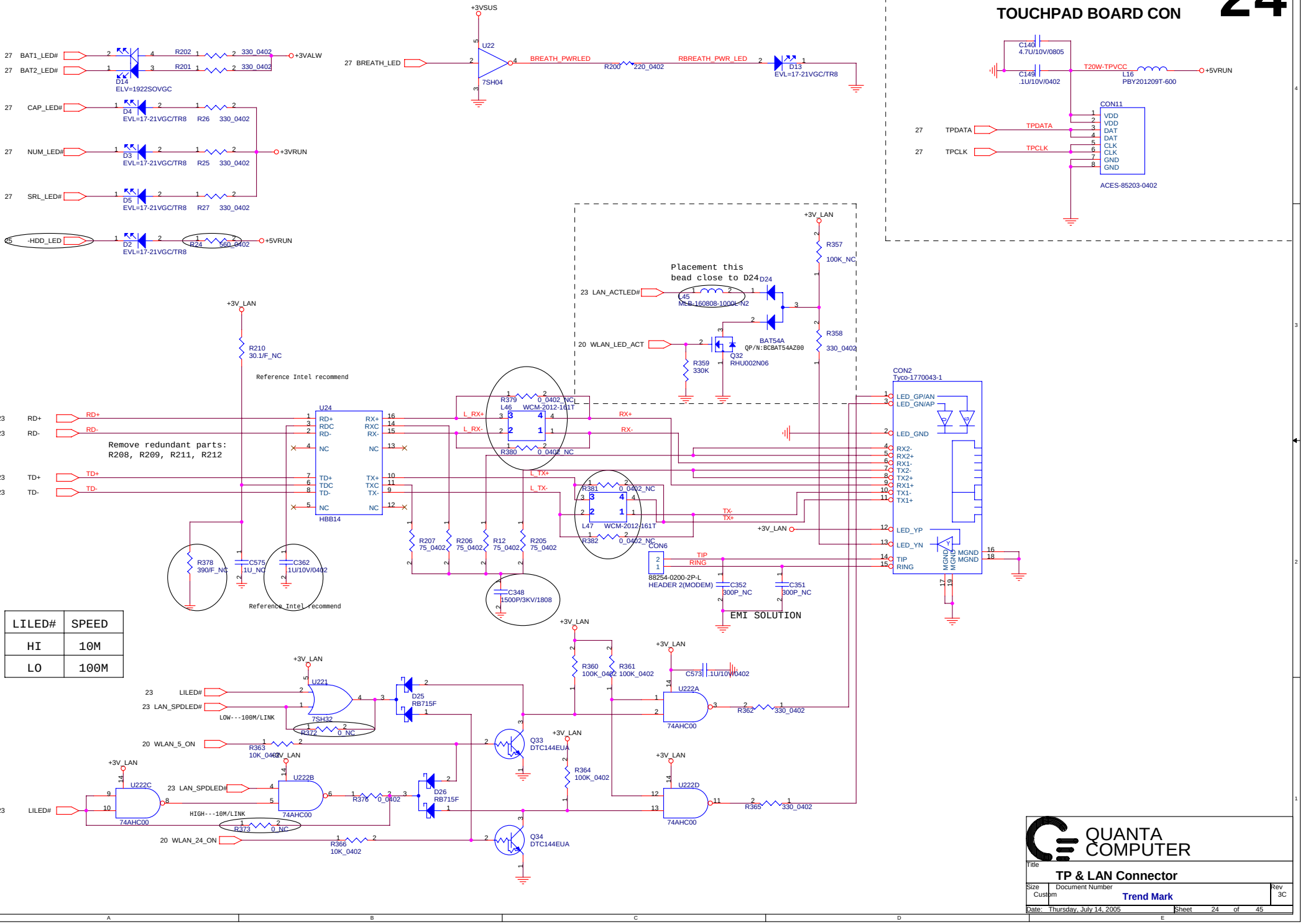
TOUCHPAD BOARD CON



LILED#	SPEED
HI	10M
LO	100M

QUANTA COMPUTER

Title: **TP & LAN Connector**

Size: Custom | Document Number: Trend Mark | Rev: 3C

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Del D10

13 PDD0
13 PDD1
13 PDD2
13 PDD3

13 PDD4
13 PDD5
13 PDD6
13 PDD7

13 PDD8
13 PDD9
13 PDD10
13 PDD11

13 PDD12
13 PDD13
13 PDD14
13 PDD15

13 PDA1
13 PDCS3#
13 PDCS1#
13 PDA0
13 PDA2
13 PDDREQ
13 PDIOW#
13 PDIOR#
13 PIORDY
13 PDDACK#
13 IDEIRQ

Delete RN66, R156, R159, R160, R161, R138 0ohm.

PDD[0..15] PDD[0..15] 13

+3VRUN

Check list V1_601 P45

PIORDY R155 4.7K_0402

PDD7 R157 5.6K_0402

IDEIRQ R136 10K_NC

PDDREQ R158 5.6K_NC

+5VRUN

C208 10U/10V/1206
C214 1U/10V/0402
C213 1U/10V/0402

13,18,20 -PCIRST
26 HDDRSTEN
R385 0_0402
R386 0_NC
R148 0_NC
U13 7S08
R153 0_0402
R152 0_0402
-IDERST1
-IDERST2

Add R385,R386

C164 10U/10V/1206
C487 1U/10V/0402
C488 1U/10V/0402

CON15
-IDERST1
PDD7 PDD6 PDD5 PDD4 PDD3 PDD2 PDD1 PDD0
PDDREQ PDIOW# PDIOR# PIORDY PDDACK# IDEIRQ PDA1 PDA0 PDCS1#
-HDD_LED
PDD8 PDD9 PDD10 PDD11 PDD12 PDD13 PDD14 PDD15
PDA2 PDCS3#
HDD_CON

R162 470_0402
C212 100P/50V/0402
C512 100U/10V/7343

Per fix HDD&ODD issue.

CON13
-IDERST2
PDD7 PDD6 PDD5 PDD4 PDD3 PDD2 PDD1 PDD0
PDIOW# PIORDY IDEIRQ PDA1 PDA0 PDCS1#
-HDD_LED
PDD8 PDD9 PDD10 PDD11 PDD12 PDD13 PDD14 PDD15
PDDREQ PDIOR#
PDDACK#
PDA2 PDCS3#
CON50_LP

R315 10K_NC
R126 470_0402
R127 470_NC

Pin.47 Cable select
H=Slave,L=Master

Del R163,R329 per HDD&ODD power link to '+5VRUN'

Del Q30,Q31,Q25,Q26,C509,C508,C493,C490,C483,R330,R301.

-HDD_LED Del D10 -HDD_LED 24

Del D11

QUANTA COMPUTER

Title: IDE HDD,ODD Connector

Size: Custom | Document Number: Trend Mark | Rev: 3C

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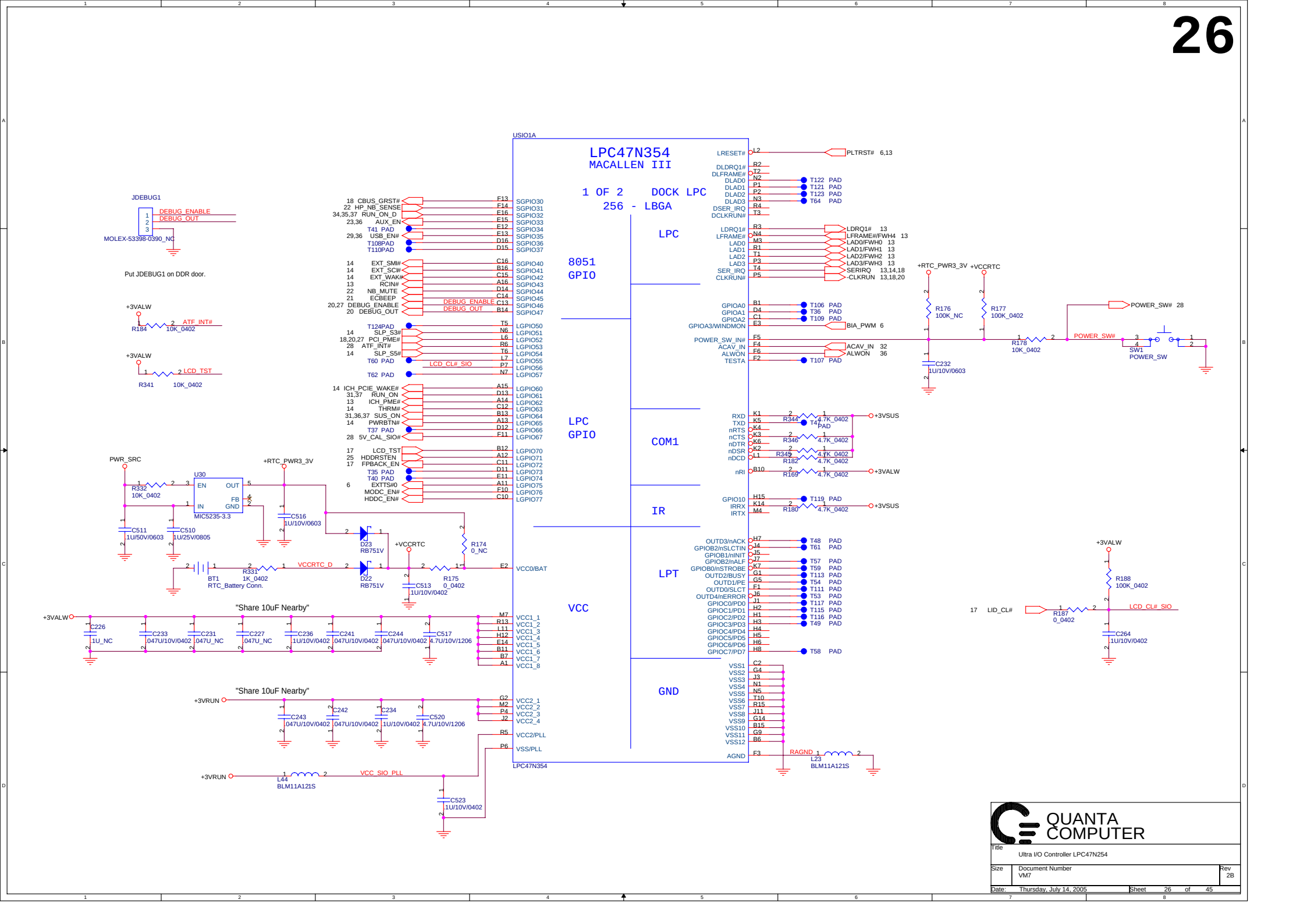
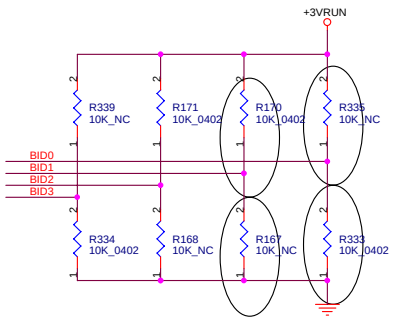
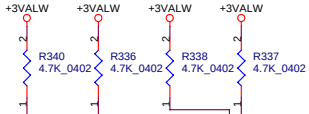


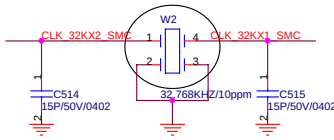
QUANTA COMPUTER

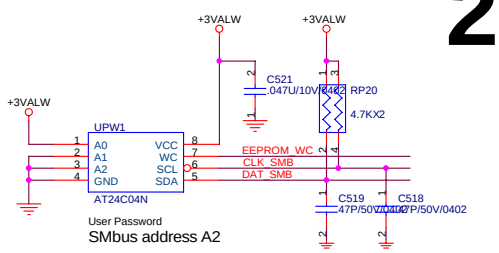
Title	Ultra I/O Controller LPC47N254	
Size	Document Number VM7	Rev 2B
Date: Thursday, July 14, 2005	Sheet 26 of 45	

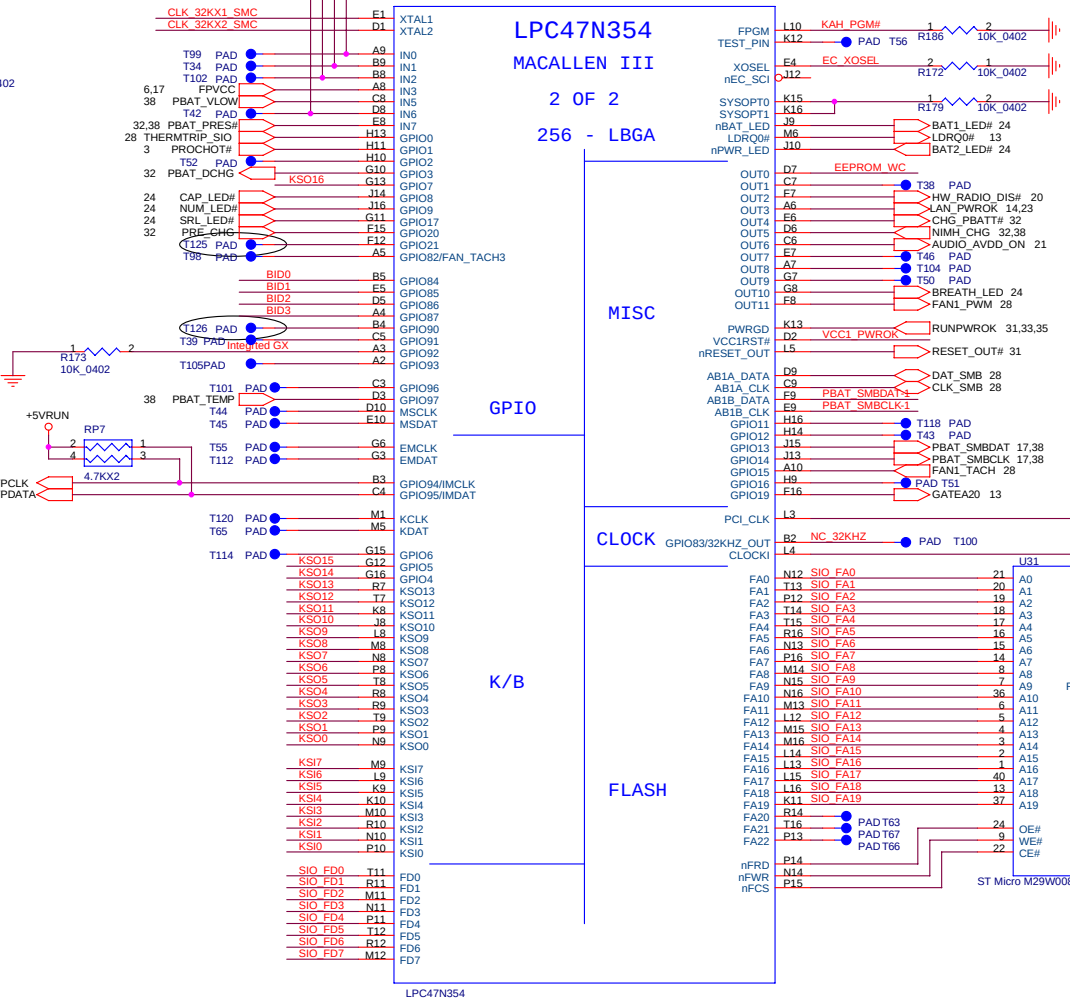
BID3	BID2	BID1	BID0	Board Revision
0	0	0	0	PROTO1
0	0	0	1	PROTO1.5
0	0	1	0	PROTO2
0	1	0	0	PROTO3
0	1	0	1	QT
0	1	1	0	A01

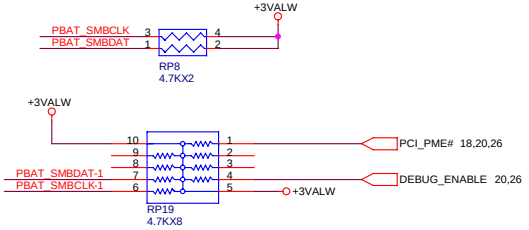


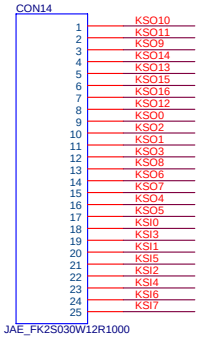


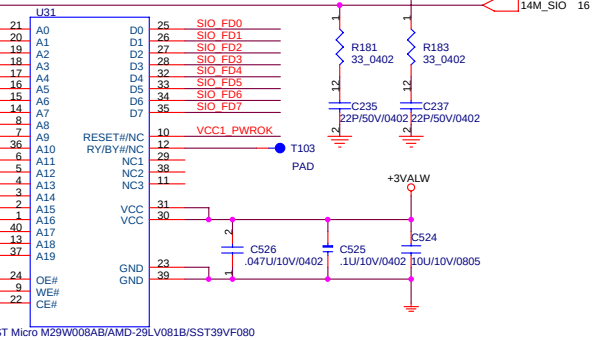




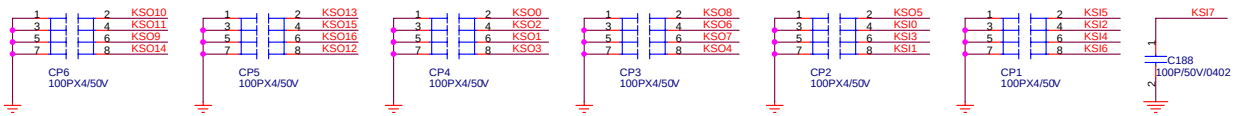








Int. keyboard



QUANTA COMPUTER

Title	Ultra I/O Controller LPC47N254(GPIO/KB/MISC/FLASH)	
Size	Document Number VM7	Rev 3C
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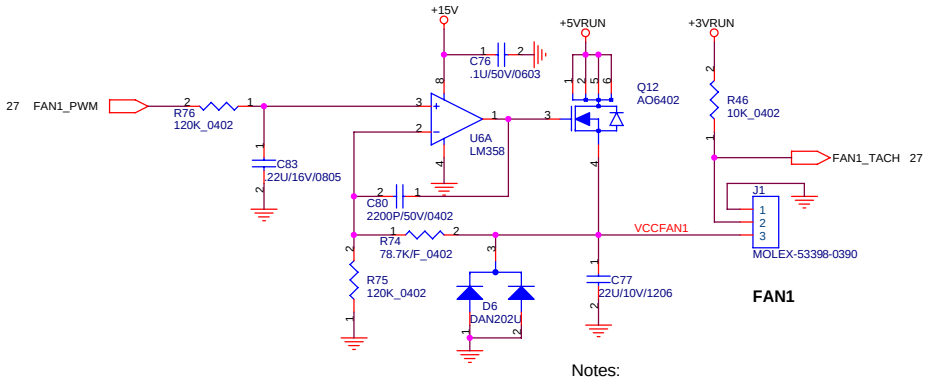


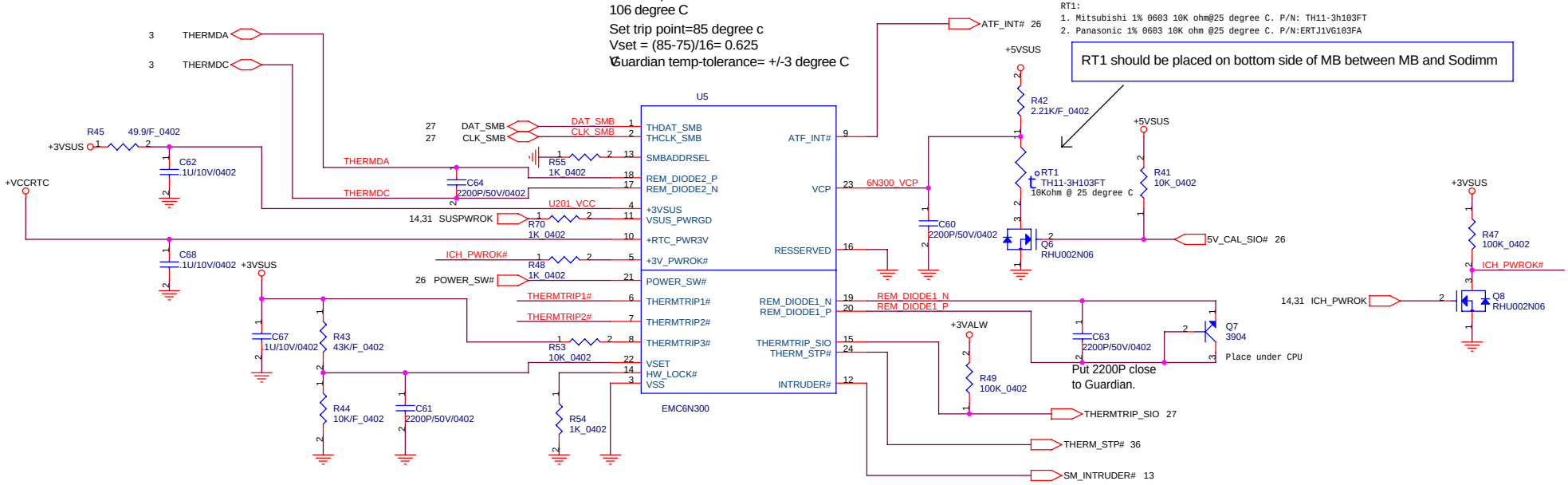
Notes:

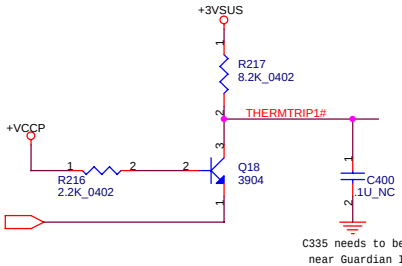
Vset=(Tp-75)/16
Where Tp=75 to 106 degree C

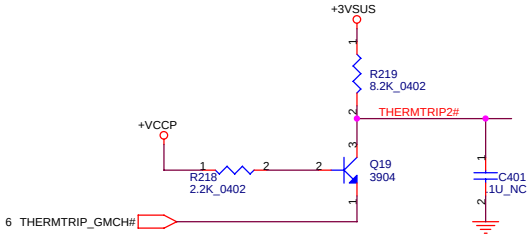
Set trip point=85 degree c
Vset = (85-75)/16= 0.625
Guardian temp-tolerance= +/-3 degree C

RT1:
1. Mitsubishi 1% 0603 10K ohm@25 degree C. P/N: TH11-3h103FT
2. Panasonic 1% 0603 10K ohm @25 degree C. P/N:ERTJ1VG103FA

RT1 should be placed on bottom side of MB between MB and Sodimm

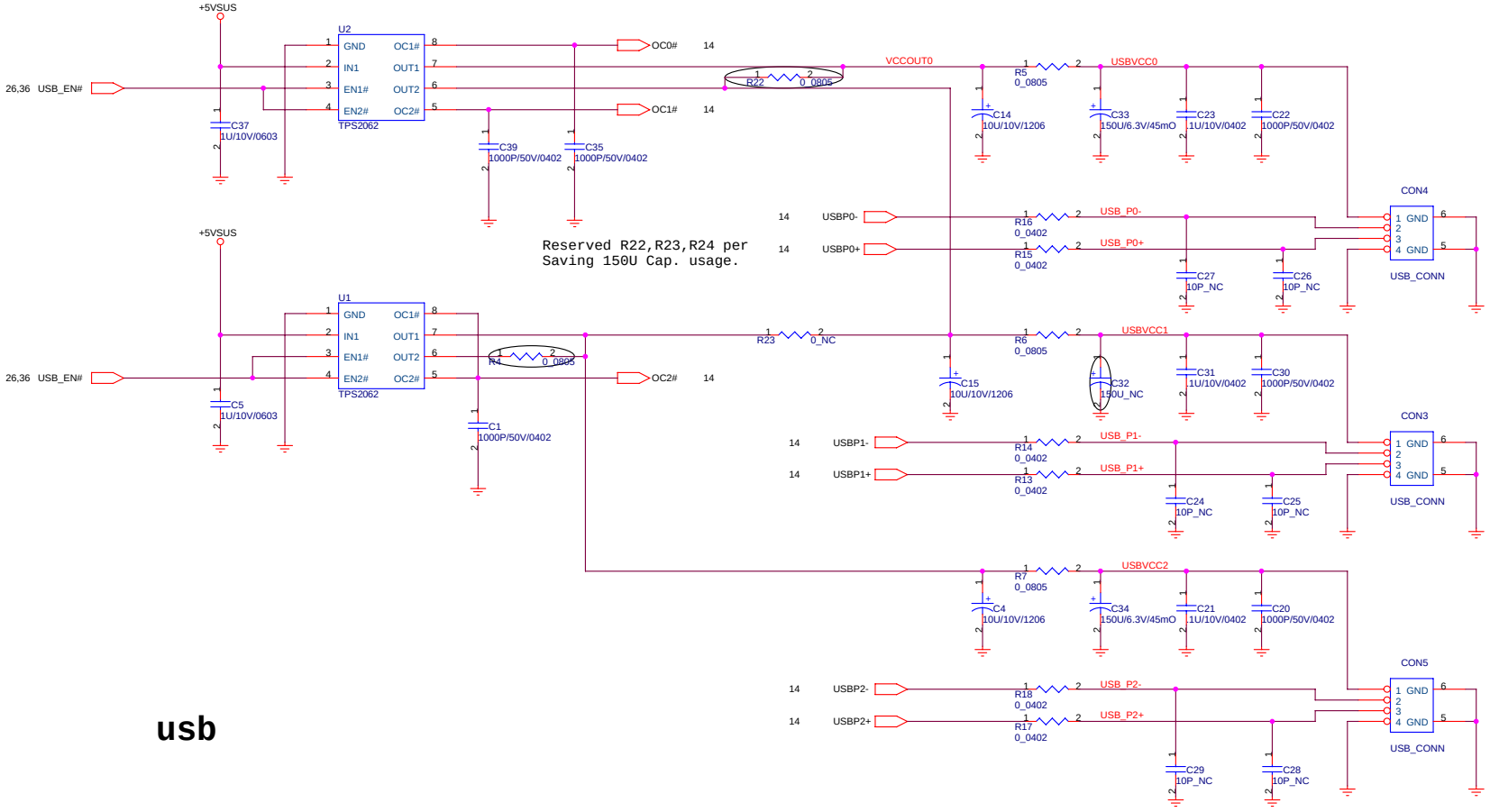






QUANTA COMPUTER

Title	FAN & THERMAL	
Size	Document Number VM7	Rev 2B
Date: Thursday, July 14, 2005	Sheet 28 of 45	



usb

QUANTA COMPUTER

Title: **USB Connector**

Size	Document Number	Rev
Custom	Trend Mark	2B

Date: Thursday, July 14, 2005 Sheet 29 of 45

PV25 PAD138X98 GND
PV24 PAD138X98 GND
PV2 PAD138X98 GND
PV6 PAD138X98 GND
PV7 PAD138X98 GND
PV1 PAD138X98 GND
PV5 PAD138X98 GND
PV3 PAD138X98 GND
PV4 PAD138X98 GND
PV9 PAD138X98 GND
PV15 PAD138X98_NC GND
PV12 PAD138X98 GND
PV11 PAD138X98_NC GND
A_HPCASE-GND
PV13 PAD138X98_NC GND
PV14 PAD138X98_NC GND
PV17 PAD138X98_NC GND
PV18 PAD138X98_NC GND
PV21 PAD138X98_NC GND
PV20 PAD138X98 GND
PV23 PAD138X98 GND
PV22 PAD138X98 GND
PV8 PAD138X98 GND
PV16 PAD138X98_NC GND

EMI SOLUTION

PV19 PAD138X98 GND
PV10 PAD138X98_NC GND

EMI added

TH1 H-C236D126P2-4
TH2 H-C236D126P2-4
TH9 H-C315D126P2-4
TH7 H-C315D126P2-4
TH4 H-C315D126P2-4
TH17 H-C315D126P2-4
TH16 H-C315D126P2-4
TH22 H-C315D126P2-4
TH8 H-C276D126P2-4
TH13 H-C394D138P2-4

ODD module Nut

TH18 H-C315D118P2-4
TH19 H-C315D140P2-4
TH20 H-C315D140P2-4
TH21 H-C315D140P2-4

TH12 H-C197D63P2
TH15 H-C197D63P2

NB Nut

TH5 H-TC394BC315D154P2-4
TH6 H-TC394BC315D154P2-4
TH10 H-TC394BC315D154P2-4
TH11 H-TC394BC315D154P2-4

CPU Cooler Hole

TH14 H-C197D63P2
TH23 MDC_NUT

MDC Nut

TH29 PCMCIA_SCREW
TH28 PCMCIA_SCREW
TH31 PCMCIA_SCREW
TH30 PCMCIA_SCREW

TH26 HDD_SCREW
TH27 HDD_SCREW
TH24 ODD_SCREW
TH25 ODD_SCREW

+3VALW +3VRUN C137 1000P_NC
+5VRUN C484 1000P_NC
+5VRUN C481 1000P_NC
+3VALW C178 1000P_NC
+5VRUN C479 1000P_NC
+3VALW C167 1000P_NC

PWR_SRC C217 4700P/50V/0603
+3VRUN C494 4700P/25V/0402

+3VRUN C146 4700P/25V/0402 +1_5VSUS
+3VRUN C500 4700P/25V/0402 +5VRUN
+3VRUN C134 4700P/25V/0402 +3VALW
PWR_SRC C507 4700P/25V/0402 +3VALW

+1_5VRUN C449 4700P/25V/0402
+1_5VRUN C440 4700P/25V/0402

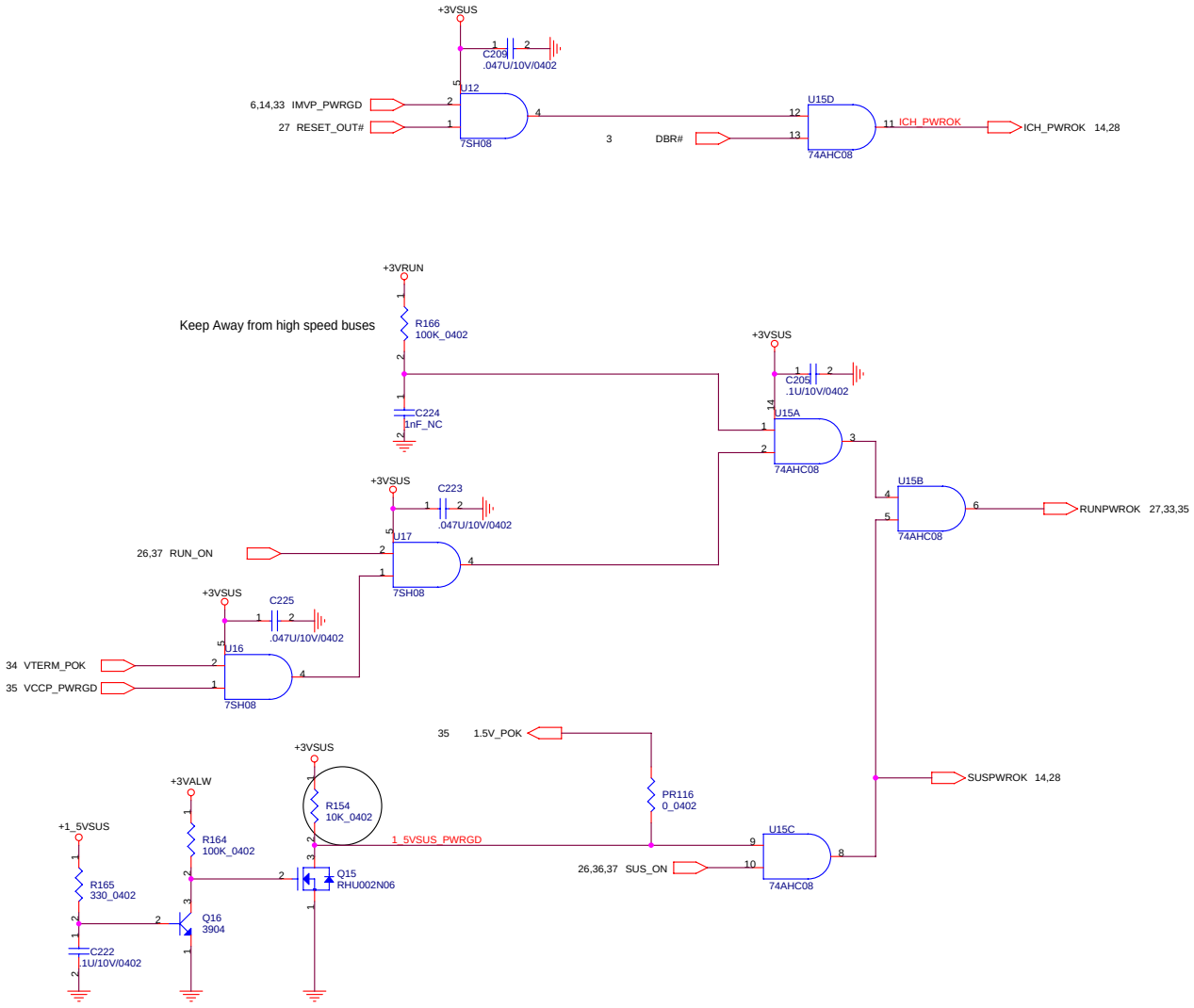
EMI require in 0810

QUANTA COMPUTER

Title: INT. KEYBOARD

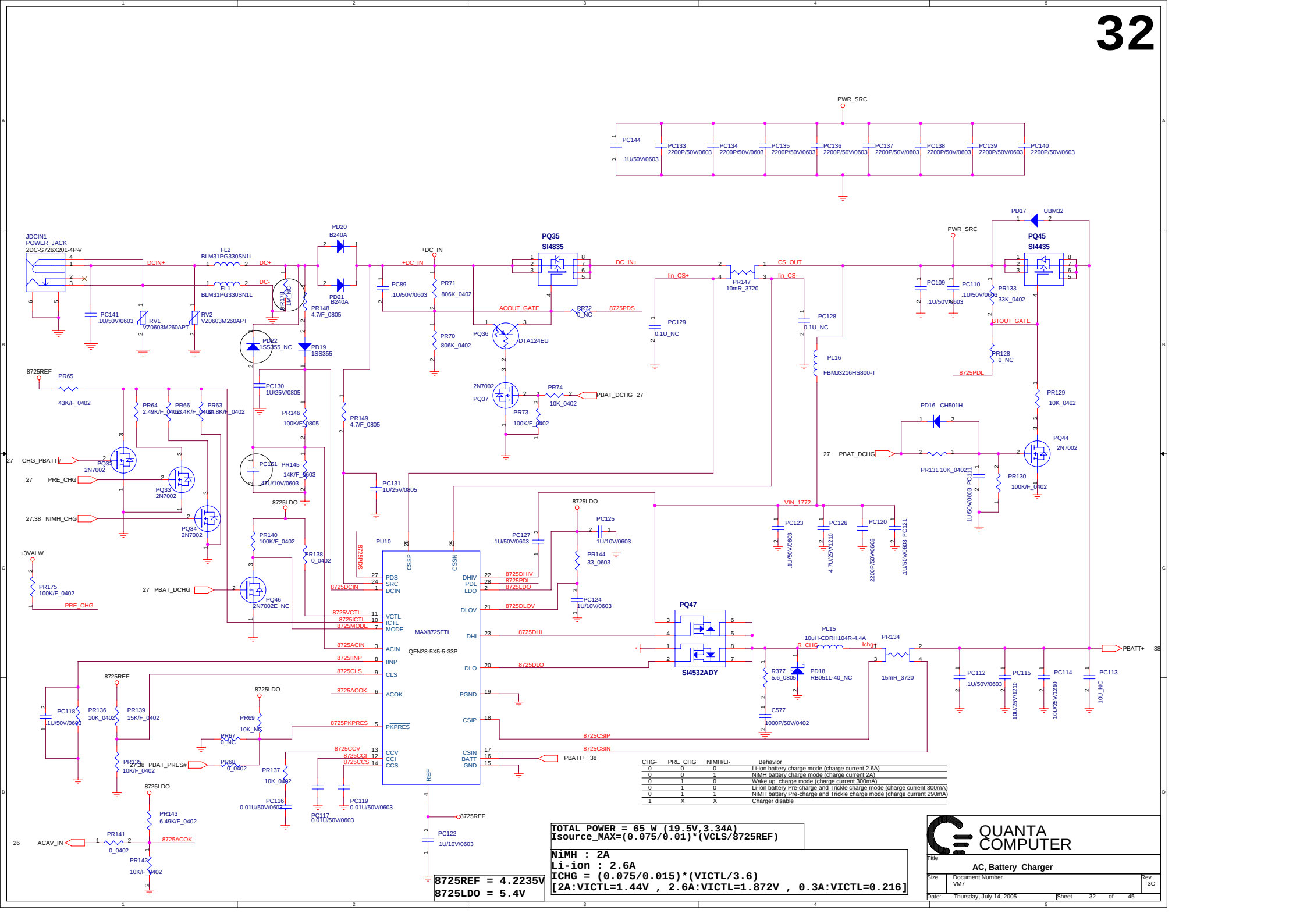
Size: Custom | Document Number: Trend Mark | Rev: 3C

Date: Thursday, July 14, 2005 | Sheet 30 of 45



QUANTA COMPUTER

Title	Power Good Circuit	
Size	Document Number VM7	Rev 3C
Date: Thursday, July 14, 2005	Sheet 31 of 45	



CHG-	PRE_CHG	NIMH/LI-	Behavior
0	0	0	Li-ion battery charge mode (charge current 2.6A)
0	0	1	NiMH battery charge mode (charge current 2A)
0	1	0	Wake up charge mode (charge current 300mA)
0	1	0	Li-ion battery Pre-charge and Trickle charge mode (charge current 300mA)
0	1	1	NiMH battery Pre-charge and Trickle charge mode (charge current 290mA)
1	X	X	Charger disable

TOTAL POWER = 65 W (19.5V,3.34A)
Isource_MAX=(0.075/0.01)*(VCLS/8725REF)

NiMH : 2A
Li-ion : 2.6A
ICHG = (0.075/0.015)*(VICTL/3.6)
[2A:VICTL=1.44V , 2.6A:VICTL=1.872V , 0.3A:VICTL=0.216]

8725REF = 4.2235V
8725LDO = 5.4V

QUANTA COMPUTER

Title: AC, Battery Charger

Size | Document Number: VM7 | Rev: 3C

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value provied
2.67% offset;
old value was
for old 4.62%
offset.

SC451
TSSOP28-6_4-65

SI7336DP-T1
SOIC8-9P

9mOhm 7343 POSC | 9mOhm 7343 POSC | 9mOhm 7343 POSC | 9mOhm 7343 POSC

P/N: CH747RY8800

Added filter for PBOOT

D5	D4	D3	D2	D1	D0	Output	D5	D4	D3	D2	D1	D0	Output
1	0	0	0	0	0	1.196V	0	0	0	0	0	0	1.708V
1	0	0	0	0	1	1.180V	0	0	0	0	0	1	1.692V
1	0	0	0	1	0	1.164V	0	0	0	0	1	0	1.676V
1	0	0	0	1	1	1.148V	0	0	0	0	1	1	1.660V
1	0	0	1	0	0	1.132V	0	0	0	1	0	0	1.644V
1	0	0	1	0	1	1.116V	0	0	0	1	0	1	1.628V
1	0	0	1	1	0	1.100V	0	0	0	1	1	0	1.612V
1	0	0	1	1	1	1.084V	0	0	0	1	1	1	1.596V
1	0	1	0	0	0	1.068V	0	0	1	0	0	0	1.580V
1	0	1	0	0	1	1.052V	0	0	1	0	0	1	1.564V
1	0	1	0	1	0	1.036V	0	0	1	0	1	0	1.548V
1	0	1	0	1	1	1.020V	0	0	1	0	1	1	1.532V
1	0	1	1	0	0	1.004V	0	0	1	1	0	0	1.516V
1	0	1	1	0	1	0.988V	0	0	1	1	0	1	1.500V
1	0	1	1	1	0	0.972V	0	0	1	1	1	0	1.484V
1	0	1	1	1	1	0.956V	0	0	1	1	1	1	1.468V
1	1	0	0	0	0	0.940V	0	1	0	0	0	0	1.452V
1	1	0	0	0	1	0.924V	0	1	0	0	0	1	1.436V
1	1	0	0	1	0	0.908V	0	1	0	0	1	0	1.420V
1	1	0	0	1	1	0.892V	0	1	0	0	1	1	1.404V
1	1	0	1	0	0	0.876V	0	1	0	1	0	0	1.388V
1	1	0	1	0	1	0.860V	0	1	0	1	0	1	1.372V
1	1	0	1	1	0	0.844V	0	1	0	1	1	0	1.356V
1	1	0	1	1	1	0.828V	0	1	0	1	1	1	1.340V
1	1	1	0	0	0	0.812V	0	1	1	0	0	0	1.324V
1	1	1	0	0	1	0.796V	0	1	1	0	0	1	1.308V
1	1	1	0	1	0	0.780V	0	1	1	0	1	0	1.292V
1	1	1	0	1	1	0.764V	0	1	1	0	1	1	1.276V
1	1	1	1	0	0	0.748V	0	1	1	1	0	0	1.260V
1	1	1	1	0	1	0.732V	0	1	1	1	0	1	1.244V
1	1	1	1	1	0	0.716V	0	1	1	1	1	0	1.228V
1	1	1	1	1	1	0.700V	0	1	1	1	1	1	1.212V

$$VDPR = \frac{PR10}{PR10+PR11+PR14}$$

$$VDPR = \frac{PR10+PR11}{PR10+PR11+PR14}$$

QUANTA COMPUTER

Title: CPU POWER

Size | Document Number: VM7 | Rev: 2B

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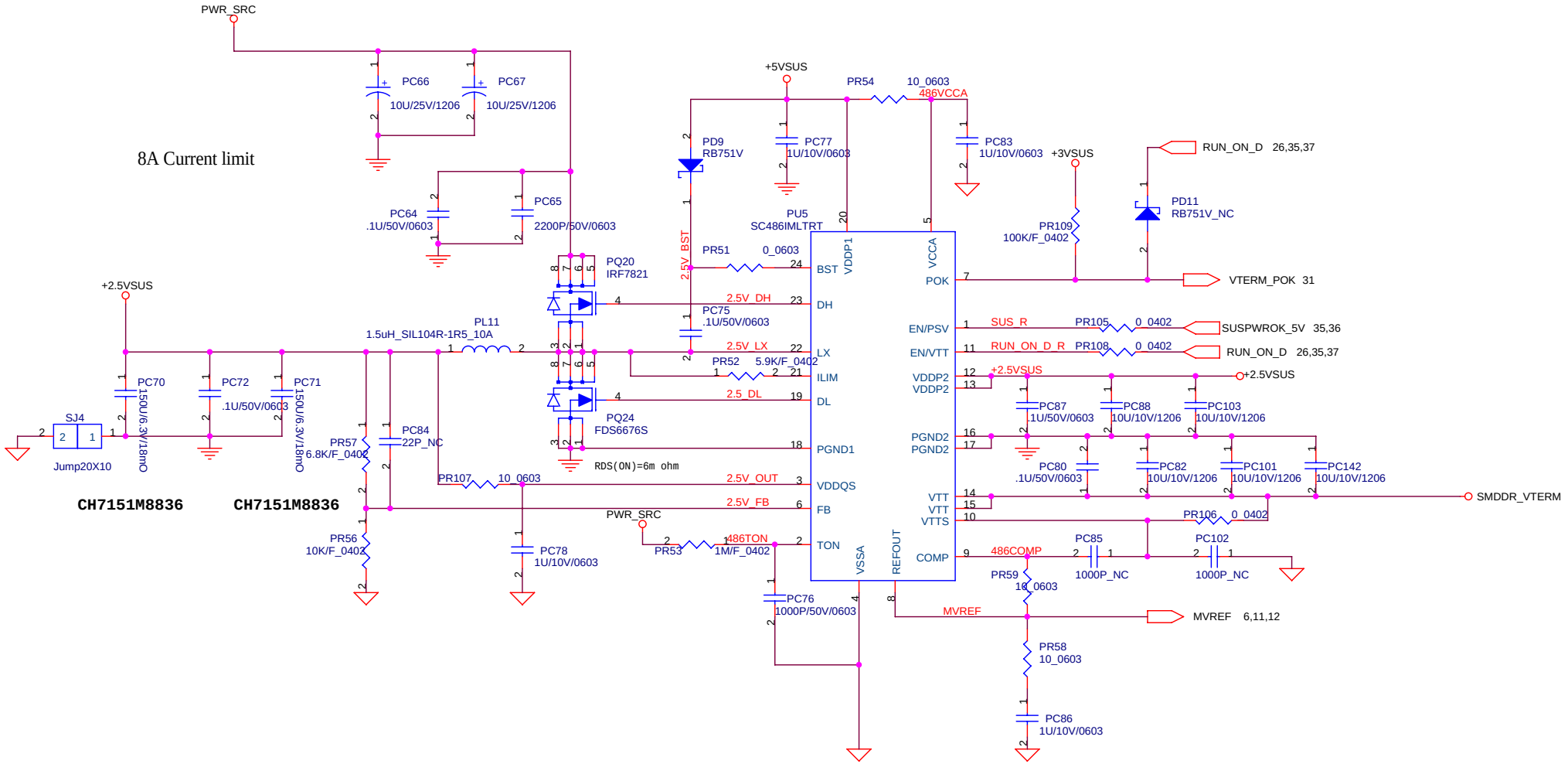
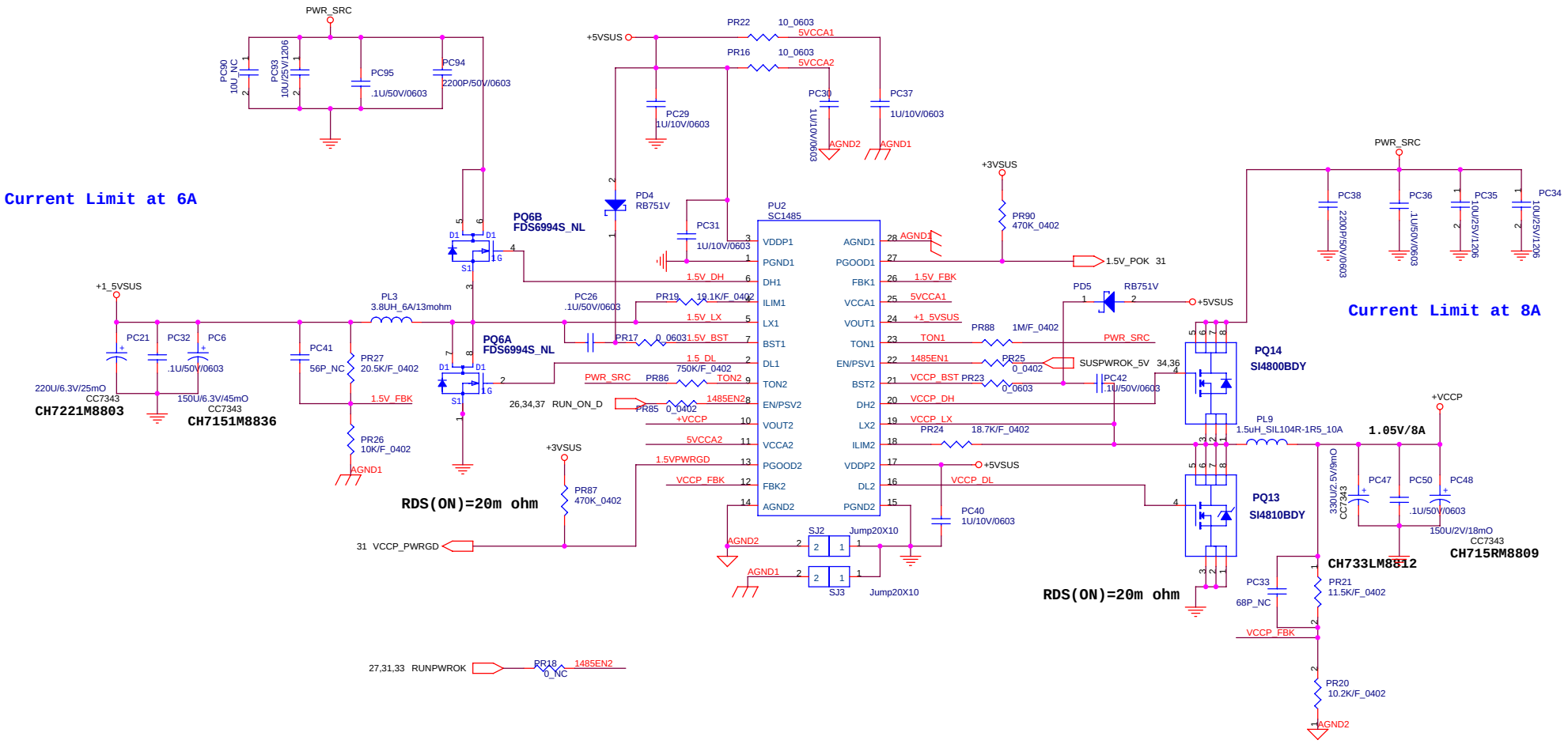


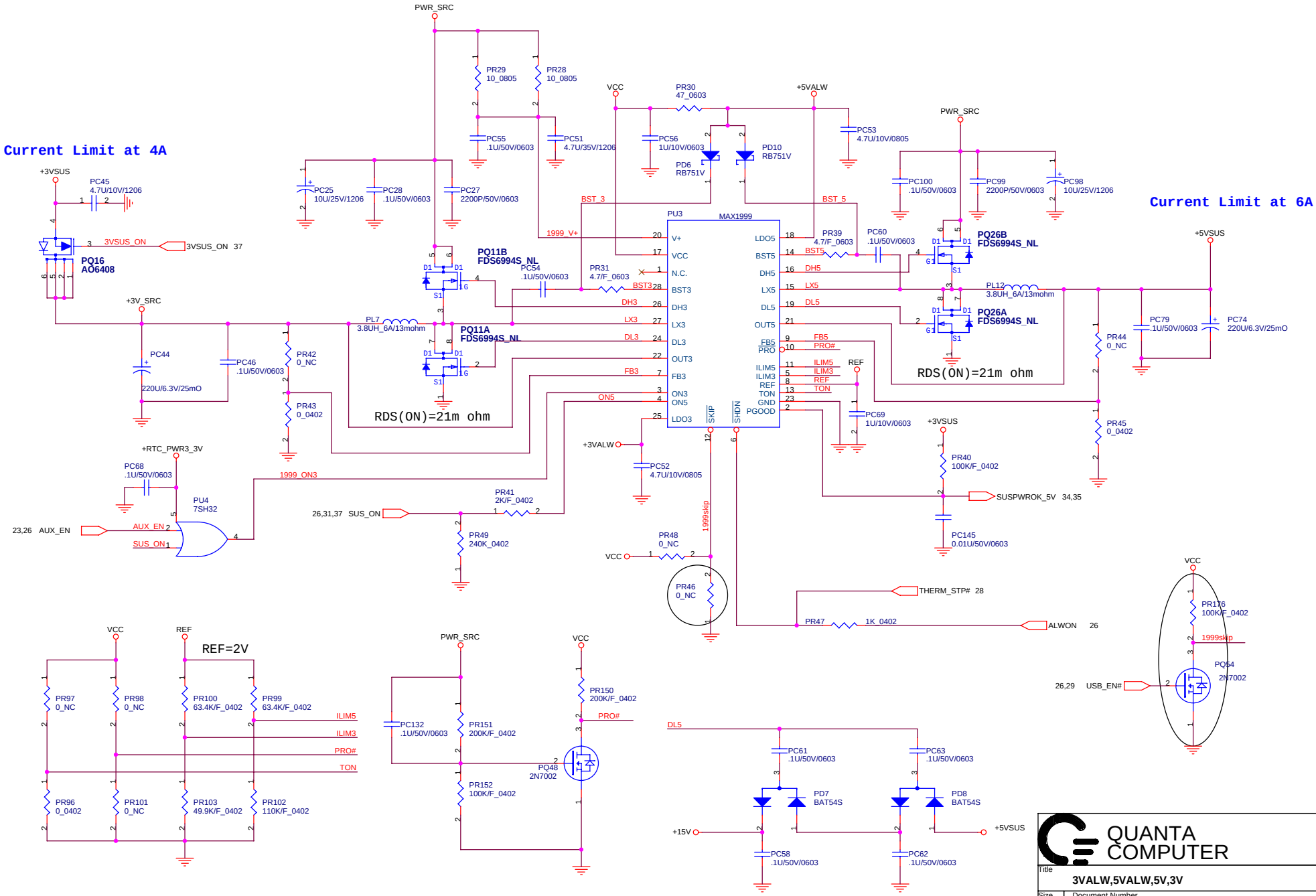
QUANTA COMPUTER

Title	2.5VSUS,SMDDR_VTER	
Size	Document Number VM7	Rev 2B
Date: Thursday, July 14, 2005	Sheet 34 of 45	



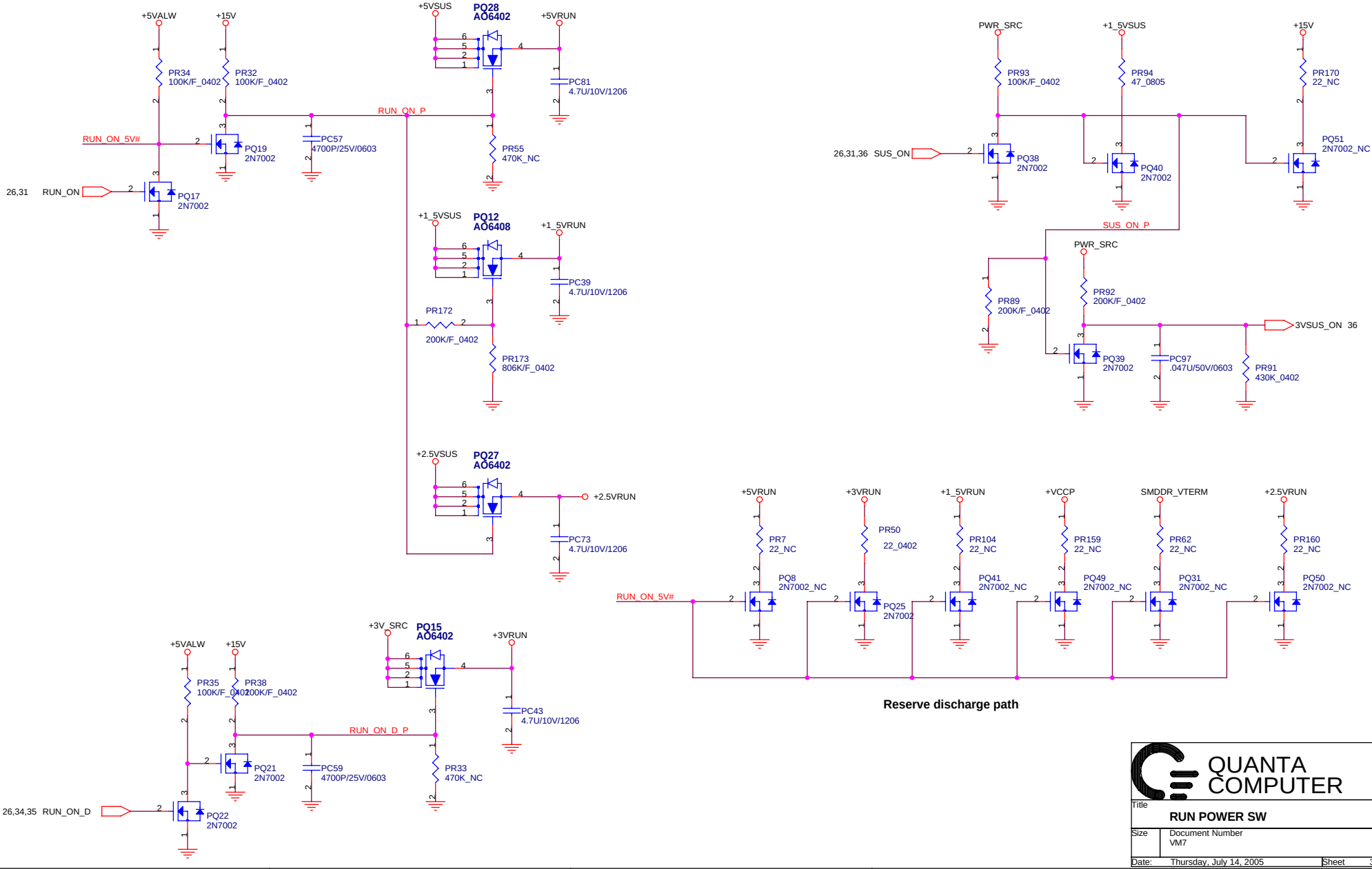
X6S

QUANTA COMPUTER		
Title: 1.5VSUS,VCCP(1.05V)		
Size	Document Number: VM7	Rev: 2B
Date: Thursday, July 14, 2005	Sheet 35 of 45	



QUANTA COMPUTER

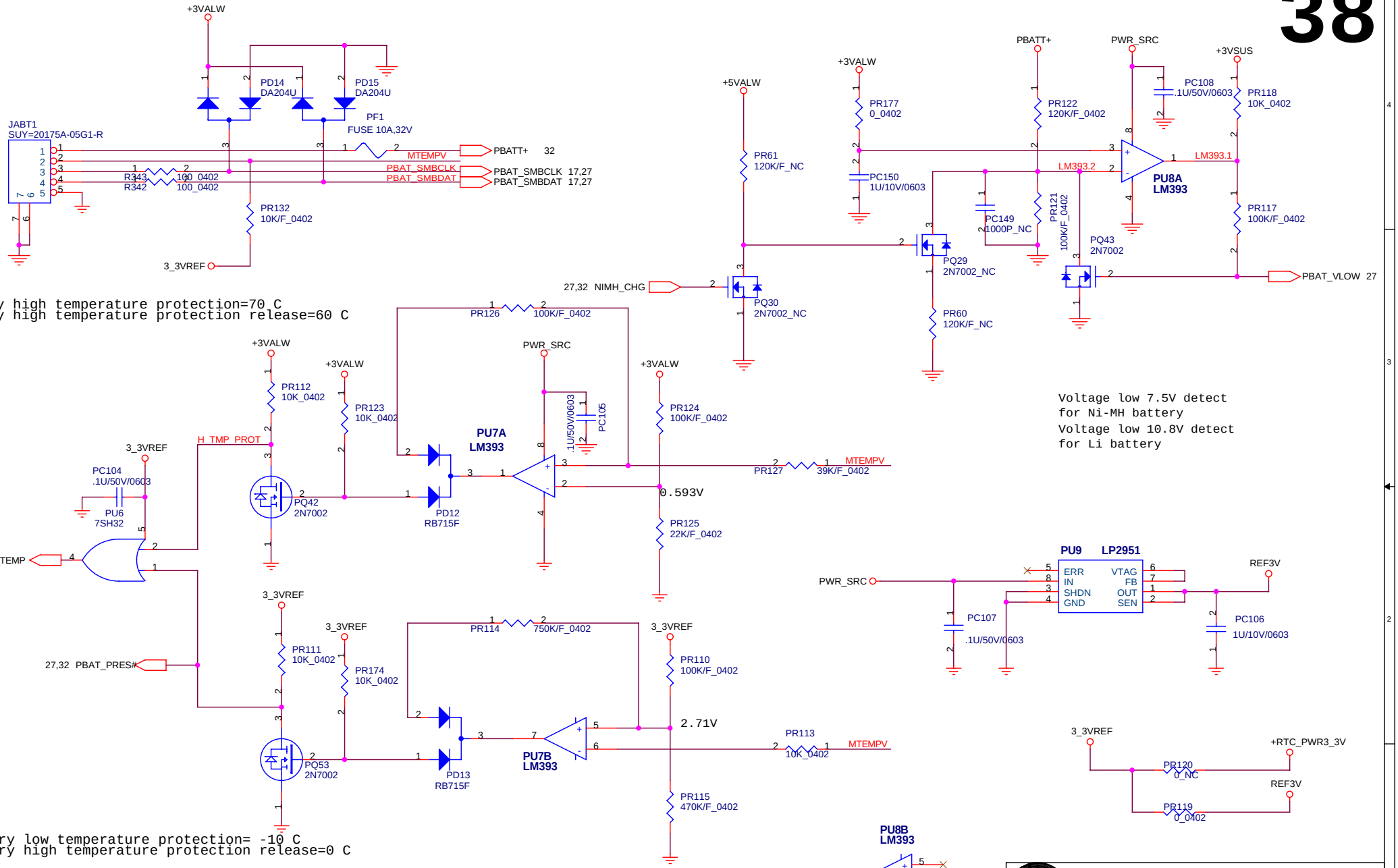
Title	3VALW,5VALW,5V,3V	
Size	Document Number VM7	Rev 2B
Date: Thursday, July 14, 2005	Sheet 36 of 45	



Reserve discharge path

QUANTA COMPUTER

Title	RUN POWER SW	
Size	Document Number VM7	Rev 2B
Date: Thursday, July 14, 2005	Sheet 37 of 45	



	PWR_SRC +3VAL	+3VALL	BAT 25C	BAT-20C	BAT 80C	BAT NOT IN	PBAT_PRES#	PBAT_TEMP	PBAT_VLOW
When Battery Only	V	-	X	X	X	-	Lo	Not Active	Not Active
When AC and Battery in	V	V	V			-	Lo	Lo	Active
	V	V		V		-	Hi	Hi	Active
	V	V			V	-	Lo	Hi	Active
When AC In , Battery Not In	V	V	X	X	X	V	Hi	X	X

When BATTERY not insert MTEMPV 3.3V
When BATTERY -10 C => NTC=46.6k MTEMPV 2.71V
When BATTERY 0C => NTC=28.8k MTEMPV=2.45V
When BATTERY 25 C => NTC=10K MTEMPV=1.65V
When BATTERY 60 C => NTC=3k MTEMPV=0.76V
When BATTERY 70 C => NTC=2.19K MTEMPV=0.593V

QUANTA COMPUTER

Title: Battery connector & Protection

Size | Document Number: VM7 | Rev: 2B

Date: Thursday, July 14, 2005 | Sheet 38 of 45

MODEL	Date	VM7I schematics change list
VM7I	**07/26**	P.24 Add MOD&HDD power switch circuit(reserved). P.25 Add MOD&HDD Enable pin. P.26 Add TP SMBUS pull up(RP36) P.31 Update Charge circuit per power update
	07/27	P.5 Add C117,C119 per JM5 Schemtic change list update. P.7. Change L18,L19 to 10uH and C134,C146,C132 to 150V/2V and C95 to 2.2U/6.3V per JM5 Schemtic change list update. P.12 Change R326 to 20K, R323 to 100K C946 to 1U/10V per JM5 Schemtic change list update. P.13 Delete net"-PCICRI" per T2 non support it. P.14 Add C142,C143 per JM5 Schemtic change list update. P.17 Delete net"-PCICRI" and Q56,R438 per T2 non support it. P.20 Del net "ENPCMSPK" and D35,D36,R461 per non-need this function on T2 P.23 Change D39 to EVL=17-21SOC/TR8 and del net "-PWRLED2" per T2 support Signal power LED. P.25 USIO1.B12(GPIO70) add a net "HDDRSTEN" per primely HDD rst signal, Add a SPD1(ST34C02) per support on board DDR requirement. P.26 Del net "ENPCMSPK" per T2 non-need it and Add C121,C123 per JM5 schematic change update. P.27 Change R624 to 43K/F and R627 to 10K/F per JM5 schematic change update.
	07/28	P.11 Moved SPD EEPROM circuit of DDRAM from P.26 and changed SMBUS to PDAT_SMB&PCLK_SMB. P.19 Removed RF switch function, Del net"-RF_SW", D33 P.23 Removed RF switch function, Del net"-RF_SW", SW1,Q59,R486,C801,D40,R489 P.26 Add USIO1.F12(GPIO20) for DC/C-, USIO1.B9(IN1) for H-Temp,USIO1.B8(IN2) for BL/C-, USIO1.E8(IN7) for PBAT_PRES#, USIO1.E6(OUT4) for CHG-, USIO1.D6(OUT5) for NIMH/LI-, USIO1.A7(OUT8) for PRE_CHG, Del USIO1.F7(OUT)"-SW_RF". P.31,32,37 Update power change page.
	07/29	P.4 Add C125 per refer the JM5 Schematic update. P.5 Add R1,R2,R3 del R62,C149,C152 per refer the JM5 Schematic update. P.25 Change net "H-Temp" & "BL/C-" pin of SMsC per SW requirement. P.26 Change net "DC/C-" & "PRE_CHG" pin of SMsC per SW requirement. but "CHG-" wasn't defined.
	07/30	P.14 Chnage C546 from 220U to 150U per refer JM5 Schematic update. P.20 Update MIC JACK circuit per refer JM5 Schematic design. P.23 Update LAN JACK symbol to combo with LED. P.25 Del R577,add R107,R108 per refer to JM5 shematic. P.26 Del R247 per power had pull up resistor. Update GPIO pins definition per SW update.
	08/02	P.9 Add RN57 per "A_BS0#","A_BS1#","B_BS0#","B_BS1#" pull Hi, delete RN77 per duplicate net of "-CSA0","-CSA1","-CSA2","-CSA3" P10 Depopulate R195 per refer Intel checkliet recommend. P.16 Change LCD panel control signal by SMBUS and add "LCD_TST" delete "VBRI".Add C76,C77 per refer JM5 schematic. P.24 +5VRUN via R104 to +5VMOD net mane corrected. P.25 Add "LCD_TST" and change "H-Temp" to "PBAT_TEMP" P.26 Change "DC/C-" to "PBAT_DCHG","BL/C-" to "PBAT_VLOW","CHG-" to "CHG_PBAT","NIMH/LI-" to "NIMH_CHG" P.27 Deleted RTC reserved circuit. P.31 Change "DC/C-" to "PBAT_DCHG","CHG-" to "CHG_PBAT","NIMH/LI-" to "NIMH_CHG" P.37 Change "BL/C-" to "PBAT_VLOW","H-Temp" to "PBAT_TEMP"
	08/03	P.5 Add R225 to +VCCP per refer chekc list V1_601 P.31 & JM5. Connection TV I/F pins to GND per refer chekc list V1_601 P.30.Deleted R1,R2,R3 pull down resistor per ducplicate R207,R208,R199. P.7 VCCTX_LVDS change power from +2.5VSUS to +2.5VRUN per refer chekc list V1_601 P.33 P.12 Update SATA I/F pins link per refer Design Guide V1.0 P.241 P.13 WAKE# pull hi to +3VRUN with R310 per refer check list V1_601 P.43 P14 Add U8,R1,R2,C64,C65,C66 to generate +1_5V_LAN per used Intel LAN I/F power & LAN power change from RUN plane to LAN plane per refer to DM1. P.15 Delete R263 per the"PCLK_SIO" should link to U35.4. P.16 Add R415,R416,R421,R422,Q1,Q2 per reference JM5 P.17 Deleted some pins which 1510 hadn't.And deleted R430,R431,L82,L83,C701,C702,C703,C706,C707

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QUANTA COMPUTER

PROJECT :	DOC. NO.	REV: 2B	ASSY:	
APPROVED BY :	CHECKED BY:	DRAWN BY : J.M Yang	DATE : Feb. 27 , 2004	SHEET 1 OF <CoverPageCount>

MODEL	Date	VM7I schematics change list
VM7I	**08/03**	P.22 Deleted LED control signal O/P pins per LAN jack non support. P.23 Change D38 to daual color LED per BATT LED dispaly requirement and deleted LAN LED circiut per LAN jack non support. P.25 Add R3 per link to SMsC RTC power pin. Depopulated R231 per R108 had populated. P.26 Add "-BATLOWLED" per BAT LED support dual color.
	08/04	P.14 Add C402 per refer Intel check list V1_601 P48 P.16 Populate PR139 and depopulate PR140. P.24 Populate R507 per refer Intel check list V1_601 P45 P.25 Add RP35 per refer JM5. Add R9,R13,R14,R15,R18,R19 per SIO non used pins pull up.Change R233 from 0 to 10K per SMsC recommend. P.26 Add R6,R7,R8 per SIO non used pins pull up. P.31 Change PR10,PC210,PC5 footprint from 1206 to 0805. Add PD30 P.35 Add PL30
	08/05	P.9 C196 Footprint change from 0402 to 7343 per footprint wrong P11. Change SPD1 power tie in from +3VALW to +3VSUS P.12 Delete U40,C499,R384,R385, "DELAY_PLTRST#","PLTRST#_1" per "LAN_PWROK" control by ICH6. REQ6 tie in to +3VRUN per check list V1_601 P36 P.13 "LAN_PWROK" link to ICH6.U2, add "ICH_PCIE_WAKE#" per refer JM5, delete "DELAY_PLTRST#". P.19 Refer JM5 Mini-PCI pin assignment, add C1,R47,"HW_RADIO_DIS#", delete non used "USBP3-","USBP3+" P.20 MIC jack powered to +VDDA,R12 change to 2.2K. C62 change to 0.1U, reserved C764,C912,C962 by SigmaTel recommend. U228 Change to TPS793475. P.21 delete R8301,R471,R472 per SigmaTel recommend for saving cost. P.23 Change C806 to 3KV cap. P.26 Update KB conn(CON41) to 26 pins. P.28 Change OC portection IC to TPS2062 X 2. And reserved 0R link to all of O/P pins per will check to saving 150U cap.
	08/06	P.10,11 DDR SPD's SMBUS had corrected as JM5 P.10 MVREF was generated by SC486.Del R168,R174,C802,C191,C249,C223 P.15 Change U35.22,U35.23 function to U35.17,U35.18 per TDC recommend. P.19 Reserved USB per test USB wirless. P.20 Codec power had changed to +5VRUN and change PCBEEP control same as JM5. PCBEEP link to PHONE had confirmed with Vendor. P.20 Add C1009 for bypass caps of TI-793475. P.23 Update LED control net name per SIO definition.Chnage LED resistor. P.25 Update SIO pinde per reference the GIOP table update. P.26 Update SIO pinde per reference the GIOP table update. P.31 Add R62,C67 per EMI requirement P.33 Add PC4,PC15 per reduce ripple. P.37 Add R65,R66 serial terminator on Battery SMBUS.
	08/09	P.5 Reserve R1484 0 ohms for Thermal team concern DDR Ram door skin temperature. P.10 Delete R168 per MVREF refer from SC486. P.16 Delete D23 and D32 for cost saving and change power of R419, R420 and U224 to CRTVCC. P.16 Change ESD protector D24~D28, D30, D31 connecting power to +5VRUN;Add +2.5VRUN to Q2 gate pin per losting. P.16 Change CON23 pin15 to +5VALW for inverter. P.19 Add R1481 and R1482 to reserve USB interface for future option USB wireless LAN;Pin-104 tie to ground per leverage Azeda. P.20 Change R12 PU from +AVDD to +5VRUN and R12 to 1.2K, R10 1.0K per total MIC PU resistor is 2.2K. P.20 Correct codec digital power to +3VRUN; Pin13 "phone" tie to Bypass; Change R4481 to R1483. P.23 Add U249 for breath LED; D38, D41, D42 and D43 PU to 330 ohms; Change D44 PU to 470 ohms per leverage fromAzeda. P.26 Add RP64 4.7KX2 for tunning SMB rise/fall time. P.35 Correct PR100 to 1K ohms per leverage from Azeda.

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QUANTA COMPUTER

PROJECT :	DOC. NO.	REV: 2B	ASSY:	
APPROVED BY :	CHECKED BY:	DRAWN BY : J.M Yang	DATE : AUG. 9 , 2004	SHEET 2 OF <CoverPageCount>

MODEL	Date	VM7I schematics change list
VM7I	**08/10**	P.12 Correct signal net from "-GNT0" to "-GNT3" P.13 Delete signal net "-PCICRI" P.20 U229 VDD from "+5VRUN" change to "+AVDD". Change R10 from 1K to 2K. P.25 Add a test pad(T126) on USIO1.K5(TXD) per reserved debug function requirement. P.26 Delete signal net & non used test pad(T22) P.27 Corrected thermal sensor control signal power name from "VTT" to "+VCCP" P.31 Corrected on of net name from "CHG_PBAT" to "CHG_PBATT"
	08/11	P.12 Add R27 per support on board memory SPD judgement. P.13 Add R48,C6 per leverage P2's experience P.16 Add C4 per preventing EMC and Noise P.19 Delete L85 and leaved CON26.113,117,118,119,120 to NC per TDC recommend. P.20 Change C63 to 4.7uF. Change R11 to 100 ohm. add R77,R78,R79,R80 per GND and AGND bridge. Change C776 to 2.2uF and add C5. P.29 Add PV24 per EMIrequirement.
	08/12	P.3. Delete R45 per PWM controller not support PSI function. P.5 Unpopulate R807, R808 per check with JM5. P.7 Unpopulate R199, R203, R207 per EA test in Azeda. P.9 Follow change L55 and L23 per Azeda originally used the same BLM18PG181SN1 ferrites, but saw a large voltage drop across these ferrites. We changed to the BLM18PG330SN1 ferrite, which has a lower DCR. P.16: Add R1486 for a pullup on Q91.3 to +3VALW. Azeda did this to address a glitch seen on LCDVCC when entering and resuming from S3. P.16 Change R423, R424, R425 per EA test in Azeda. P.21 Add RP65, R1490 R1491 for audio gain selection. P.22. Add R1488 & change R706 PU to +3V_SRC; Delete R602 and Tie Pin 21 to LAN ; change R608 to 619 and R609 to 649 Per Intel review. P.22.Change R604 to 110; R605 & R606 to 54.9 and depopulate C892 Per Intel review. P.23. Depopulate R493, R494, R499, R500, C802 and C803; Add R1489 to U231 Pin6 per INtel reveiw. P.25 Add R1485 for LCD_RST PU and R1487 for ATF_INF# PU. And add T132~T148 per suggestion from ADC. P.25 Correct R9,R13,R14,R15 Pu to +3VSUS and R19 to +3VALW per reveiw with SMsC. P.26. Chnage R6, R8 and R103 PU to +3VALW and R7 PU to +5VALW per Peer review in ADC. P.26. ADD AB1B CLK/DATA PU to +3VALW per ADC peer review. P.27 Redefine J7 pin out per FAN follow Rocket design.
	08/16	P.26 Delete RP8 per un-used. P.31 Change PR148 from 0603 to 0805. P.34 Change Pu2.23 signal from "1485_VIN_B" to "1485_VIN_A"
	08/20	P.17Add AC terminator R354,C571 for "PCLK_PCM" P.19 Add AC terminator R355,C572 for "PCLK_MINI". Add LAN LED control O/P signal "WLAN_LED_ACT", "WLAN_5_ON", "WLAN_24_ON" P.20 Add AC terminator R367,C574 for "P14M_CODEC". P.22 Add LAN LDE control O/P signal "LAN_ACTLED#", "LAN_SPDLED#", "LILED#" P.23 Add LAN LDE control circuit. P.26 Upcate KB connector to 25Pins. P.31 Change Power Jack and update chagre circuit. P.35 update DC/DC circuit. Delete PR6 and PR14 per power team request.
	08/26	P.16 Correct Q23,Q24 symbol P.21 Correct Q27,Q28,Q29 symbol P.22 Update U3.41 name from "ADV10" to "ADV10/LANDIS#". Add R368,R369 per Intel recommend. P.23 Change "LAN_SPDLED" & "LILED" Function per Intel recommend. P.31 Correct "DC_IN+".

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QUANTA COMPUTER

PROJECT :	DOC. NO.	REV: 2B	ASSY:	
APPROVED BY :	CHECKED BY:	DRAWN BY : J.M Yang	DATE : AUG. 9 , 2004	SHEET 3 OF <CoverPageCount>

MODEL	Date	VM7I schematics change list
VM7I	**08/30**	P.13 Corrected "USBP0+","USBP0-","USBP0+","USBP0-". P.18 Correct CON17 library,add 4 pins GND per connector fix block. P.26 Add rp8 per PBAT SMBUS pull up. Change BID to proto1.5. Correct KB library(delete fix block) P.29 Add TH23 per MDC connector NUT. P.37 Correct BAT connector SMBUS data & clock pin define.
	08/31	P.23 Depopulte R210 and Populate C362,C575 per Intel recommend P.26 Corrected BID table. P.29 Update CPU cooler hole diameter per ME requirement. P.30 Populate R154,R164,R165,Q15,Q16,C222 per power sequene circuit update.
	09/02	P.11 Depopulate SPD1&C255 per no need support on board memory SPD. P.23 Poplate C351,C352. P.27 Change R42 from 22.1K/F to 2.21K/F per Schematic error. P.29 Update MDC nut, MDC cable nut, ODD module nut P/N. Add PV19 per EMI reqiurement.
	09/16	P.12 Depopulate R320 P.16 Correct L2,L4,L6 value from 0_0805 to 0_0603 P.22 Depopulate R368 per LAN issues. P.23 Depopulate C362,C575 per proto1 LAN function issues and correct LILED#&LAN_SPDLED# circuit. P.31~P.37 Change all of resistors package from 0603 to 0402. P.32 Add PR153,PR154,PR155,PR156,PR157,PR158,Reserve for test. PC7,PC8,PC9,PC10 change package from 1210 to 1206. PQ4,PQ5 change value form TPCA8005A-H to SI7336DP.Change PC24 package from 0603 to 0402. P.34 PC93 change package from 1210 to 1206. P.35 PC25,PC98 change package from 1210 to 1206.
	09/23	P.3 Populate R61 per used Dothan B CPU. P.7 C411,C420 change material. P.9 RN39,RN36,RN45,RN42,RN52,RN55,RN61,RN58 Change part value from 10X2 to 56X2. P.15 Change R291 value from 39 to 10 per fix EA rise/fall rate violate spec. P.20 C189 change package from 1206 to 0805.Depopulate R261,R281,R323 per fix HP noise issue. P.21 Change C468,C478 package from 0805 to 0603.Reserve R370,C576. P.22 Reserve "LAN_PWROK".Change C56 package from 1206 to 0805. P.23 Change net name from "-ODD_LED" to HDD_LED". Del R203,C2 and MGEND. P.24 Per fix HDD & ODD issues, change "-ODD_LED" to "-HDD_LED" chnage connector net name to "-HDDLED" ,Del D11. P.26 Update BID,Populate R170,R333 depopulate R335,R167. Del net "PS_ID","PS_ID_DISABLE#" and add T125,T126 P.28 Populate R22,R4 depopulate C32 per TDC recommend. P.31 AddPC133,PC134,PC135,PC136,PC137,PC138,PC139,PC140 per EMI requirement. P.32 Add R21,C38 per EMI requirement.
	09/24	P.3 Depopulate R51,R57 P.15 R112 change value from 39 to 15 per fix EA test fail. P.16 Remove PR95,F1 P.23 LAN jack connect to MGND P.29 TH3 contact to MGND
	09/27	P.22 Add R371,R374 and R375 to reserved for LAN test. P.23 Add R372 and R373 to reserved for LAN LED cost down test. P.24 Reserver R315 per ODD power supplier

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QUANTA COMPUTER

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MODEL	Date	VM7I schematics change list
VM7I	**09/30**	P.11 Change R140 PU to +AVDD.
	10/01	P23. Add R376 for LAN LED and remove C2 and R203. P28. Depopulate C24, C25, C26, C27, C28 and C29 per USB eyes diagram issue. P29. Add PV25 for EMI request to place close ODD connector. P.31 Add PC144 0.1U mount on Power Source for EMI require. P.32 Power change PQ52 Value to 2N7002
	10/04	P.31 for EMI require add R377 2.7/F and C577 0.01U P.23 Reserve R378 for Lan function P.20 C171 change from 1U to 0.33U P.21 C505 C506 change from 0.1uF to 0.047uF P.23 C362 need mount 0.1uF
	11/03	P.5 Depopulate R258,R259,R267. P.4,5,6,7,8 change NB P/N from AJ829100T11 to AJ829100T20 per NB change ver from B0 to B1. P.16 C6,C16,C17 change value from 22P to 20P, L2,L4,L6 change Value from 0R to BLM18BD600SN1D, R3,R8,R9 change value from 150R to 75R. PR36 change part number from CS00004JA07 to CS00002JB03 per proto2 SMT issues. CON1 change P/N from DFDS15FR441 to DFDS15FR0Q8. CON8 change P/N from DFHD30MS361 to DFHD30MS697. CON7 change P/N from DFWF02MS037 to DFWF02MS029. P.23 D24 change value from BAT54S to BAT54A. CON6 Change P/N form DFHD02MR281 to DFHD02MR346. C573 change package from 0603 to 0402 per proto2 SMT issues. P.29 Remove PV11,PV15 P.30 PR116 change part number from CS00004JA07 to CS00002JB03 per proto2 SMT issues. P.31 R377 chane value from 2.7R to 5.6R, C577 change value from .01U to 1000P, PD16 change value from RB500V to CH501H.PR68,PR138,PR141 change part number from CS00004JA07 to CS00002JB03 per proto2 SMT issues. JDCIN1 change P/N from DFPJ04MR101 to DFPJ04FR086 P.32 R21 chane value from 2.7R to 5.6R, C38 change value from .01U to 1000P.PR1,PR79,PR164 change part number from CS00004JA07 to CS00002JB03 per proto2 SMT issues. PC24 change package from 0603 to 0402 per proto2 SMT issues. P.33 PR105,PR106,PR108 change part number from CS00004JA07 to CS00002JB03 per proto2 SMT issues. P.34 PR25,PR85 change part number from CS00004JA07 to CS00002JB03 per proto2 SMT issues. P.35 PR43,PR45,PR46,PR96 change part number from CS00004JA07 to CS00002JB03 per proto2 SMT issues. P.37 PR119 change part number from CS00004JA07 to CS00002JB03 per proto2 SMT issues.
	11/17	P.2 Add R379 per support CPU FSB 400 only. P.13 Change R91 from 33ohm to 22ohm per fine tune 14M_ICH signal issues. P.15 Change R252 from 24ohm to 10ohm per fine tune 14M_ICH signal issues. P.16 Depopulate D16,D18 and delete L2,L4,L6,C7,C9,C11. P.23 Change CON2 footprint from LAN-1770112-15P-H to LAN-1770043-1-15P P.25 Delete Q30,Q31,Q25,Q26,C509,C508,C493,C490,C483,R330,R301 per not support ODD hot plug. P.26 W2 change to same as W1 per cost down. P.35 Change PR40 pull up source from "+3V_SRC" to "+3VSUS" per solved timing issues of "SUSPWROK".
	11/18	P.7 Add C578 100uF per fix CRT water wave issues. P.16 Change Q1,Q2 from 2N7002E to 2N7002,Change R73 from 4.7K_0402 to 47_0805 for shortening LCD_VDD3 discharge time. P.17 Change Q17 from 2N7002E to 2N7002. P.20 change U10.43 from "HP_NB_SENCE" to "MUTE" P.21 Change R370 from 0ohm to BLM18AG601SN1D, Change C455,C463 from 4700pF to 150pF.Depopulate R150 and populate R149 per down Amp gain. P.29 Add TH24,TH25,TH26,TH27(HDD&ODD screw) into schematic per BOM export requirement.
	11/19	P.3 Delete R379 per had PU in P15. P.10 Delete C268, C261, C228, C262 per cost down. P.16 Change L1,L10,L100 from CX8LL121002 to BLM18BB470SN1D. Change C3,C18,C19 from 10pF to 6.8pF. Delete CRT-GND. P.20 Depopulate R324. P.26 Depopulate R168, R170,populate R167, R171per update BID. P.31-P.35 Power update schematic and removed power jump.
	11/22	P.16 Depopulate C6,C16,C17. P.20 change MIC bias voltage to AVDD mount R140, unmount R308. P.24 Delete RN66, R156, R159, R160, R161, R138 0ohm.

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MODEL	Date	VM7I schematics change list	Model / Page	DM3 MB FM	DM3 MB TO
VM7I	**11/24**	P.7 Add C581 during U8.E19 and U8.G19 per fix CRT water wave issues.	1		
		P.16 Change CRT H/VSYNC buffer from TC7W126FU to AHCT1G125, chnage L5,L7 from BK1608HM121 to BLM18AG121SN1D, Change C10,C12 from 120pF to 6.8pF. reserver C580,C581 per refer to JM5 CRT design.	2		
		P.21 Change R150 PW to +AGND for setting amplifier to be 6db..	3		
		P.24 Delete D10 and link "HDD_LED" to SIO directly.	4		
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	11/25	P.21 Change R140 vlaue from 1.2K to 820 per 'EXT_MIC_VDD' source change to '+AVDD'	6		
		P.22 Depopulate RP6.	7		
		P.24 Del R163,R329 per HDD&ODD power link to '+5VRUN'	8		
		P.31 PU PR175 to "+3VALW" per SMSC GPIO pin define error, change R377 package from 0402 to 0805 per EMI requirement.	9		
		P.32 Chnage R21 package from 0402 to 0805 per EMI requirement, add PC146,PC147,PC148 per fix noise issues.	10		
	11/26	P.16 change R226 value from 100K to 470K	11		
		P.24 Add R379-383 per EMI requirement to verify LAN. Change R24 from 470 to 560	12		
	12/20	P.8 C578 change Value from 100U to 150U per fix NB VGA codec power issues.	13		
		P.17 Update C579 property per C579 is non populated parts.	14		
		P.24 Depopulate C351,C352 per EMI confirm to removed it.	15		
		P.32 Change R371 P/N to lead free per Vendor recommend.	16		
		P.33 Change R21 P/N to lead free per Vendor recommend.	17		
	12/23	P.24 Correct R358 pad from 0603 to 0402	18		
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	12/29	P.14 C114 Change vlaue from 4.7pF to 10pF per fine tune CLK48_USB.	20		
		P.21 R314 change value from 8.2K to 4.7K per decrease beep sound.	21		
		P.24 Add L45, reserve L46,L47 per EMI requirement.	22		
		P.30 Add PV22,PV23,PV24 removed TH3 per ME update PCB requirement.	23		
		P.32 Add PQ54 PR176 for USB leakage voltage protection circuit.	24		
		P.38 Update battery UVP circuit, Add PR177,PC149,PC150, reserve PQ29,PQ30,PR60,PR61.	25		
	12/30	P.11 Reserve C268, C261, C228, C262	26		
		P.12 Add C582~C599 per TDC reqiurement.	27		
		P.18 Add R383, reserve R384 per verify PCI1510 leakage voltage issues.	28		
		P.27 Change BID to QT phase, populate R335, depopulate R333	29		
	01/03	P.21 R231,R261,R324 populated 4.7nF, R327 populate BK1608LM182 per EMI requirement.	30		
		P.22 Populate BK1608LM182 on R316 per EMI requirement.	31		
		P.37 Populate PQ25,PR50 for leakage of U32	32		
	01/05	P.25 Cutoff net HDDRSTEN, short U13.1 and U13.2	33		
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	01/11	P.21 Add remark of R231,R261,R324 used 4.7nF, R327 used BK1608LM182.	35		
		P.22 Add remark of R316 used BK1608LM182.	36		
		P.36 Populate PR46, depopulate PQ54,PR176 per TDC requirement.	37		
	01/14	P.13 R83 value change from 100R to 10R.	38		
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	01/27	P.11 Change CON18 P/N from DGMK0005376 to DGMK0000099 per material issues.	40		
		P.27 Change CON14 P/N from DFHS25FR191 to DFHS25FR212 per material issues.	41		
		P.35 Change PQ6 P/N from BAM48220015 to BAM69940017 per material issues.	42		
		P.36 Change PQ11,PQ26 P/N from BAM48220015 to BAM69940017 per material issues.	43		
	01/28	P.5-9 Change U8 P/N from AJ829100T20 to AJSL8AE0T70 per Vendor update to product P/N.	44		
		P.13-15 Change U29 P/N from AJ82801ZT70 to AJSL7W60T03 per Vendor update to product P/N.	45		
	02/21	P.24 Delete L46,L47 per LAN Hipot test issue.	46		
		P.32 Add PC151, reserved PD22,PR178 per battery caused system shut down issue.	47		
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MODEL	Date	VM7 schematics change list
VM7	**03/01**	P.14 R98&C116 link to LAN_CLK P.24 Reserve C361,C363 to TD+,TD- per EMI requirement. Change R379-R382 package from 0805 to 0402.
	3C	BID change from "0101 to "0110" for A01 Page27 : Depopulate R335,and R167 , populate R170, R333. For IDE reset Page25 : Add R385 0_0402 Page30 : Remove TH3 mdc nut Getting lower sink current of SC1485 Page31 : Change R154 from 330 to 10K. USB issue Page36 : Depopulate PR46, populate PR176,PQ54. LAN Page24 : Change C348 from 1000p/3KV to 1500p/3KV(CH2150GKI11). Page24 : Populate L46, L47 with WCM-2012-161T ; depopulate R379,R380,R381,R382. Page14 : Depopulate R98, C116. Page32 : Populate PC151 from .47u/16V_NC to .47u/10V.

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PROJECT : VM7	DOC. NO. 204	REV: 3C	ASSY: 31VM7MB0036	
APPROVED BY : Mike Hwang	CHECKED BY: Mike Hwang	DRAWN BY : Guresu Lo	DATE : Jul., 14, 2005	SHEET 7 OF <CoverPageCount>