

Compal Confidential

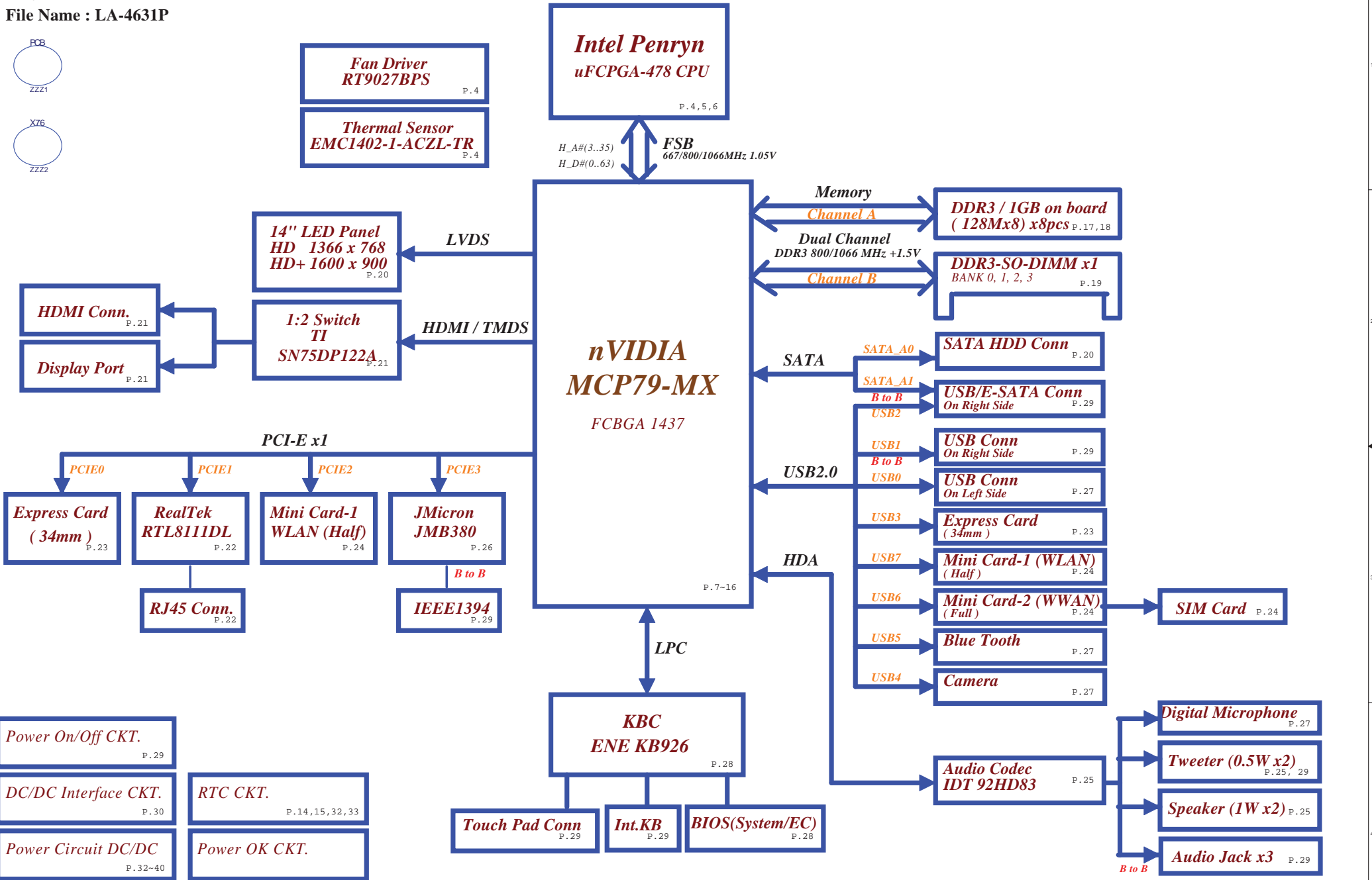
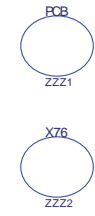
Schematic Document

MCP79-MX

2009 / 02 / 19 Rev:1.0

Security Classification	Compal Secret Data			Title	
Issued Date	2009/02/19	Deciphered Date	2009/12/31	<i>Cover Sheet</i>	
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Braxton 14"

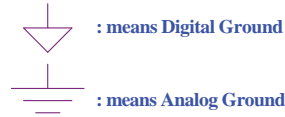


Security Classification		Compal Secret Data		Title	
Issued Date	2009/02/19	Deciphered Date	2009/12/31	Block Diagram	
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Voltage Rails ○ MEANS ON ✗ MEANS OFF

power plane State	+B	+5VALW +3VALW +1.1VALW	+1.5V	+5VS +3VS +1.8VS +1.1VS +VCCP +1.0VS +0.75VS +CPU_CORE +1.5VS
s0	○	○	○	○
s1	○	○	○	○
s3	○	○	○	✗
s5 s4/AC	○	○	✗	✗
s5 s4/ Battery only	○	✗	✗	✗
s5 s4/AC & Battery don't exist	✗	✗	✗	✗

Symbol Note :



@ : means just reserve , no build
 DEBUG@ : means just reserve for debug.

Board ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	18K +/- 5%	0.436 V	0.503 V	0.538 V
2	33K +/- 5%	0.712 V	0.819 V	0.875 V
3	56K +/- 5%	1.036 V	1.185 V	1.264 V
4	100K +/- 5%	1.453 V	1.650 V	1.759 V
5	200K +/- 5%	1.935 V	2.200 V	2.341 V
6	NC	2.500 V	3.300 V	3.300 V
7				

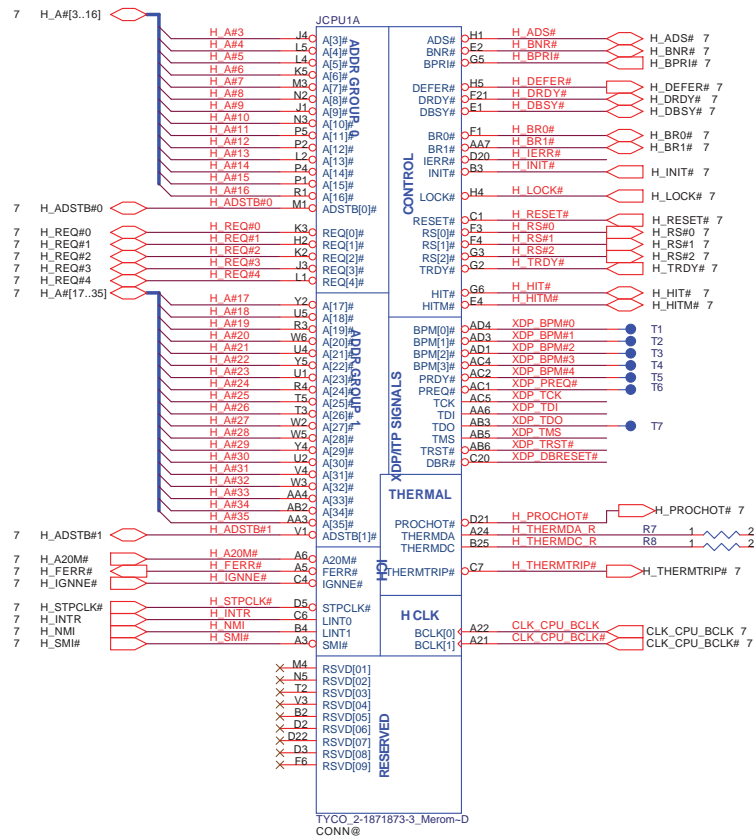
BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	0.5
5	1.0
6	
7	

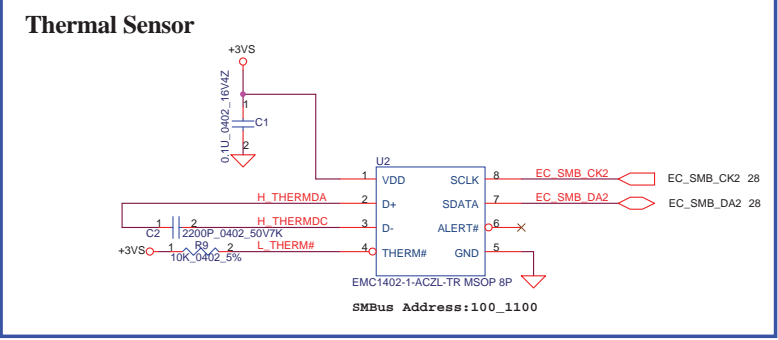
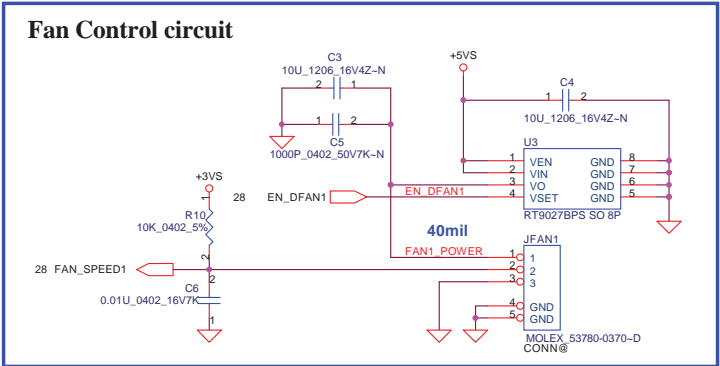
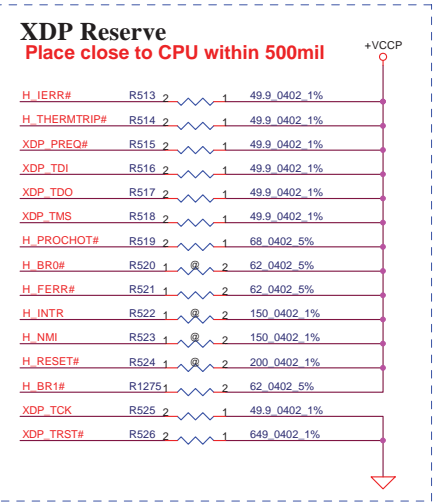
SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL REPRM	THERMAL SENSOR (CPU)	SODIMM	EXP CARD	MINI CARD1	MINI CARD2
EC_SMB_CK1 EC_SMB_DA1	KB926	✗	✓	✗	✗	✗	✗	✗	✗
EC_SMB_CK2 EC_SMB_DA2	KB926	✗	✗	✗	✓	✗	✗	✗	✗
MEM_SMBCLK MEM_SMBDATA	MCP79	✗	✗	✗	✗	✓	✗	✗	✗
MCP_SMB_CLK MCP_SMB_DATA	MCP79	✗	✗	✗	✗	✗	✓	✓	✓

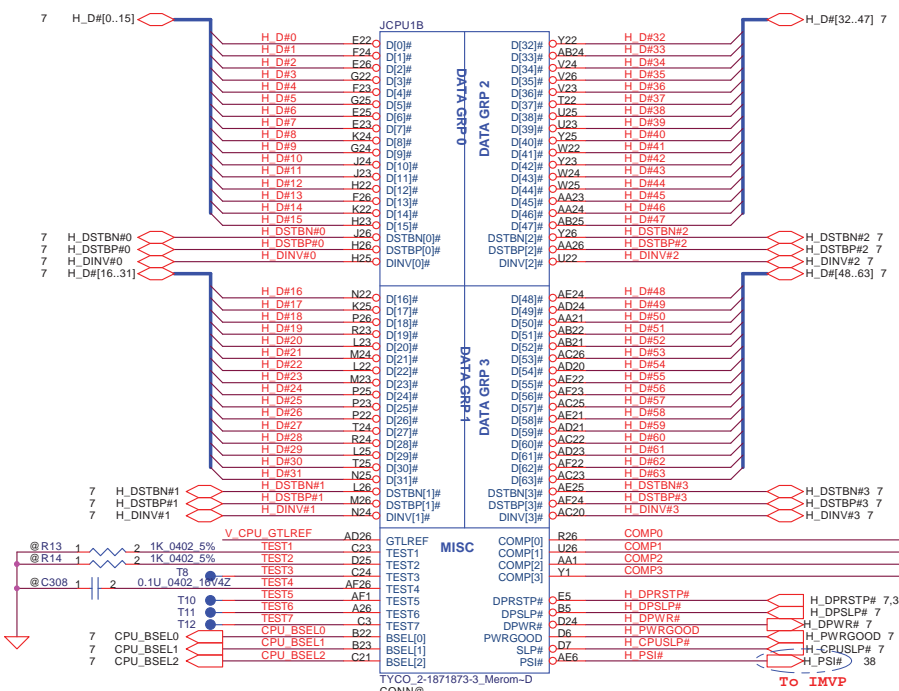
MINI CARD 1 RESERVED +3VALW TO PULL HIGH



**H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil**

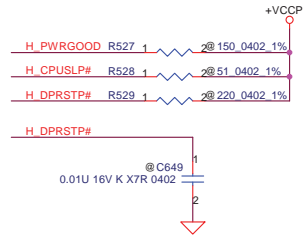


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				Penryn(I/3)-AGTL+/ITP-XDP	
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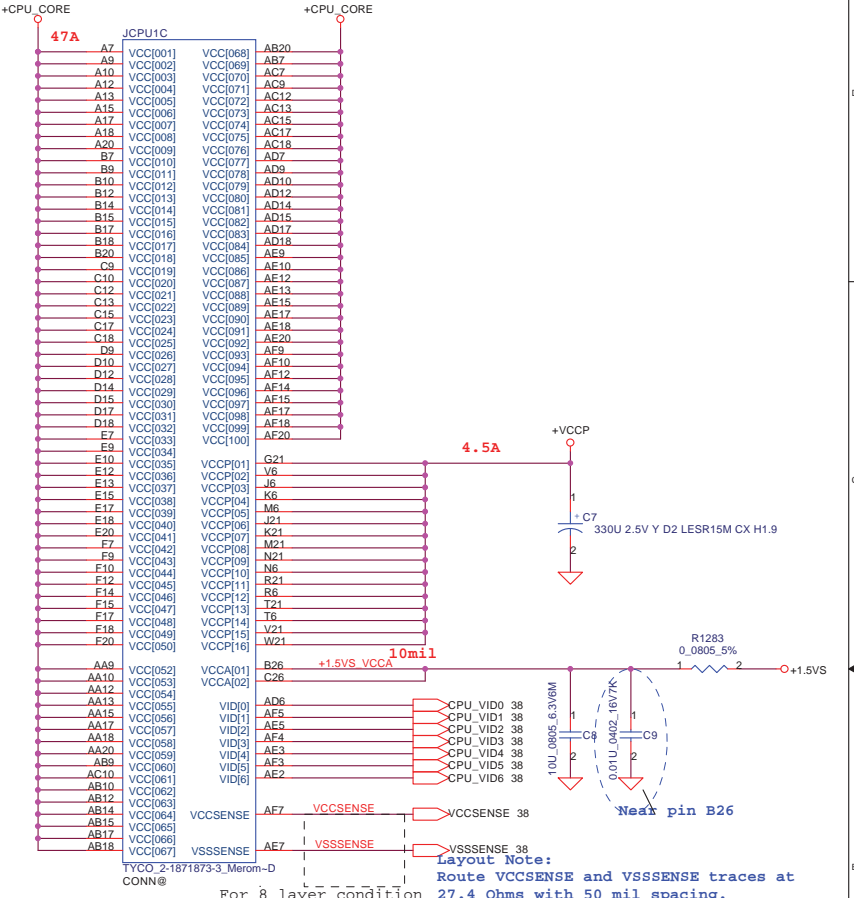
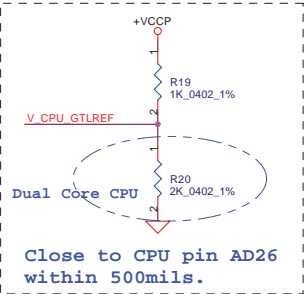


layout note: Rout H_DPRSTP# from ICH9 to IMPV6 then to GMCH & CPU
 layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

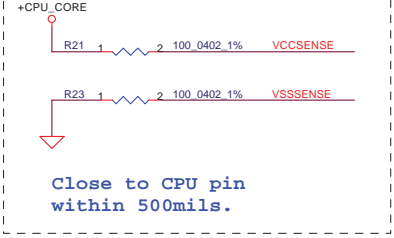


49.9 25.5 29.9 25.5
 Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4



Length match within 25 mils. The trace width/space/other is 20/7/25.

For 6 layer
 Z=27.4 ohm
 VCCSENSE, VSSSENSE/ 14mils (MS),
 16mils (SL) width, 7mils space, 25mils space to other signals Mismatch =25mils.

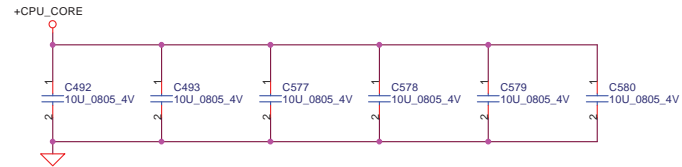
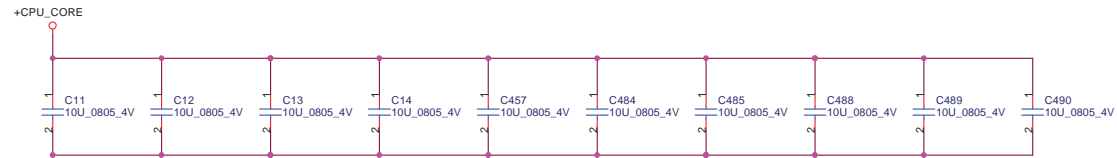


Near CPU CORE regulator

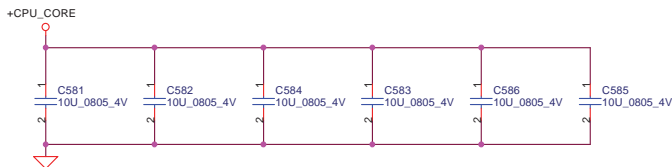
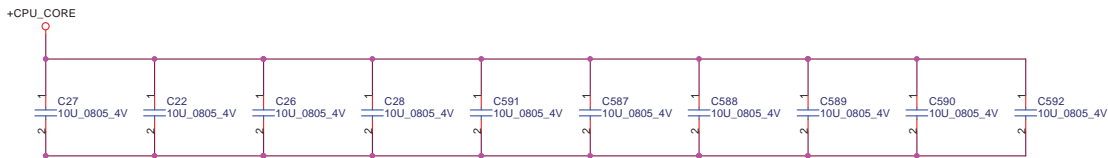
ESR <= 1.5m ohm
Capacitor > 1980uF

JCPU1D		
A4	VSS1001	P6
A8	VSS1002	P21
A11	VSS1003	P24
A14	VSS1004	R2
A16	VSS1005	R5
A19	VSS1006	R22
A23	VSS1007	R25
A6	VSS1008	T1
B6	VSS1008	T4
B8	VSS1009	T23
B11	VSS1010	T26
B13	VSS1011	U3
B16	VSS1012	U6
B19	VSS1013	U21
B21	VSS1014	U24
B24	VSS1015	U26
C5	VSS1016	V2
C8	VSS1017	V5
C11	VSS1018	V22
C14	VSS1019	V25
C16	VSS1020	W1
C19	VSS1021	W4
C2	VSS1022	W23
C22	VSS1023	W26
C25	VSS1024	Y3
D1	VSS1025	Y6
D4	VSS1026	Y21
D8	VSS1027	Y24
D11	VSS1028	AA2
D13	VSS1029	AA5
D16	VSS1030	AA8
D19	VSS1031	AA11
D23	VSS1032	AA14
D26	VSS1033	AA17
E3	VSS1034	AA19
E6	VSS1035	AA22
E8	VSS1036	AA25
E11	VSS1037	AB1
E14	VSS1038	AB4
E16	VSS1039	AB8
E19	VSS1040	AB11
E21	VSS1041	AB13
E24	VSS1042	AB16
F5	VSS1043	AB19
F8	VSS1044	AB23
F11	VSS1045	AB26
F13	VSS1046	AC3
F16	VSS1047	AC6
F19	VSS1048	AC8
F2	VSS1049	AC11
F22	VSS1050	AC14
F25	VSS1051	AC16
G4	VSS1052	AC19
G1	VSS1053	AC21
G23	VSS1054	AC24
G26	VSS1055	AD2
H3	VSS1056	AD5
H6	VSS1057	AD8
H21	VSS1058	AD11
H24	VSS1059	AD13
J2	VSS1060	AD16
J5	VSS1061	AD19
J22	VSS1062	AD22
J25	VSS1063	AE1
K1	VSS1064	AE4
K4	VSS1065	AE8
K23	VSS1066	AE11
K26	VSS1067	AE14
L3	VSS1068	AE16
L6	VSS1069	AE19
L21	VSS1070	AE23
L24	VSS1071	AE26
M2	VSS1072	A2
M5	VSS1073	AF6
M22	VSS1074	AF9
M25	VSS1075	AF11
N1	VSS1076	AF13
N4	VSS1077	AF16
N23	VSS1078	AF19
N26	VSS1079	AF21
P3	VSS1080	A25
	VSS1081	AF25

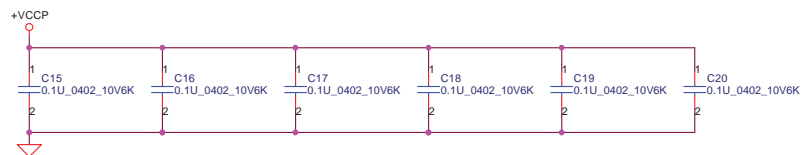
TYCO_2-1871873-3_Merom-D
CONN@



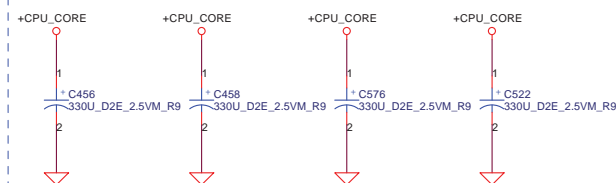
16pcs on TOP side



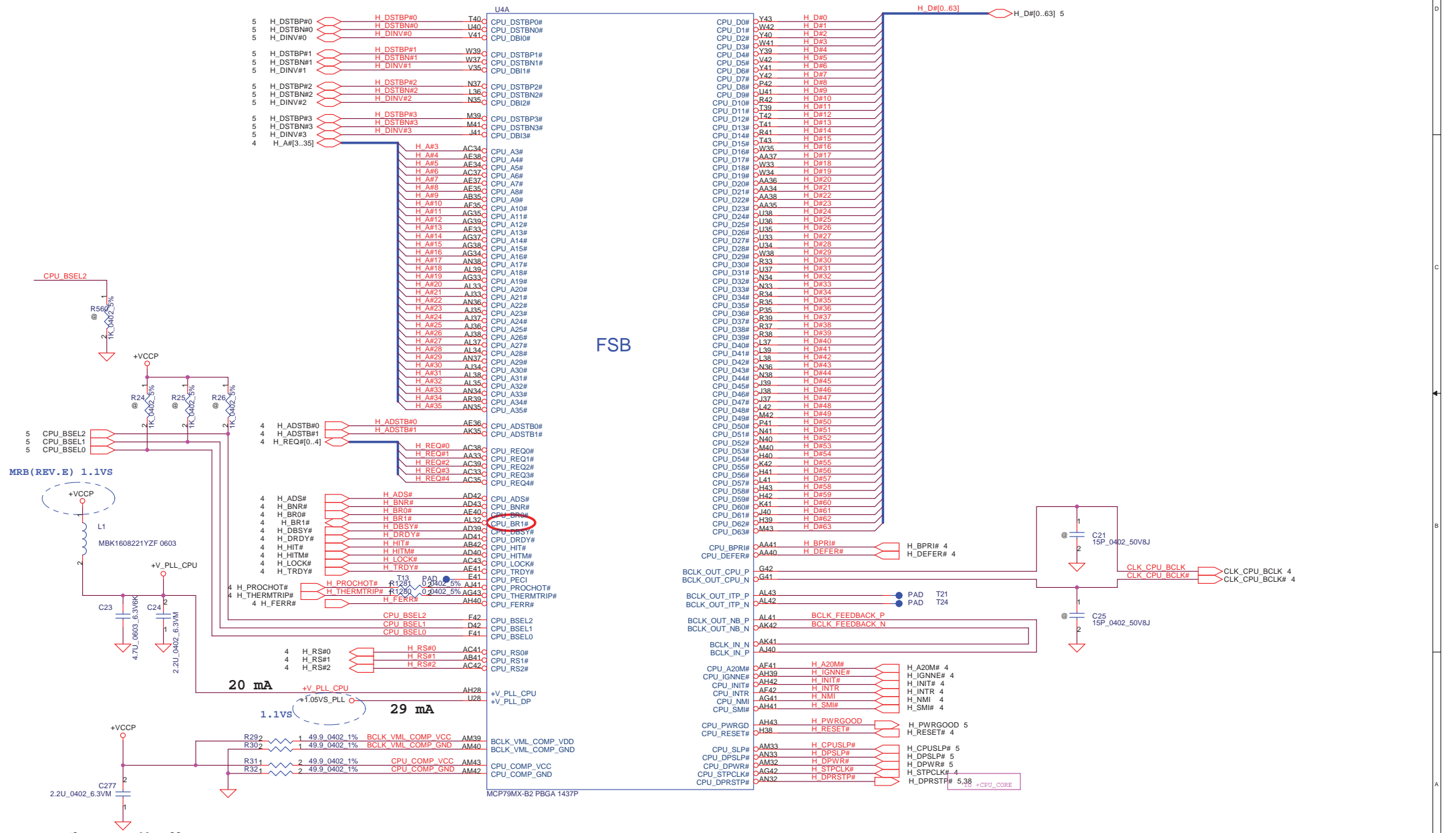
16pcs on bottom side



Place these caps inside the
socket cavity on Bottom side.
(North side Secondary)



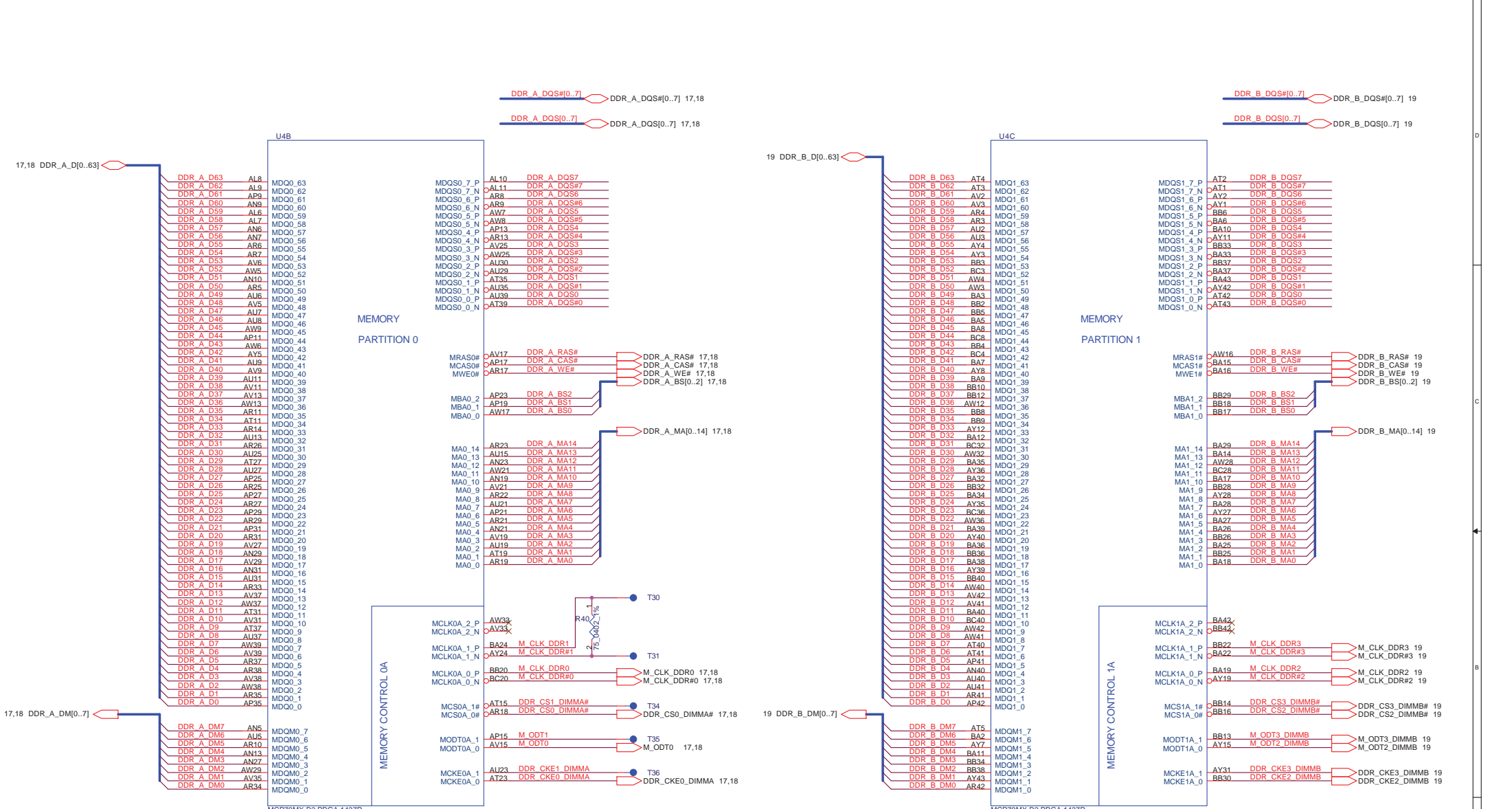
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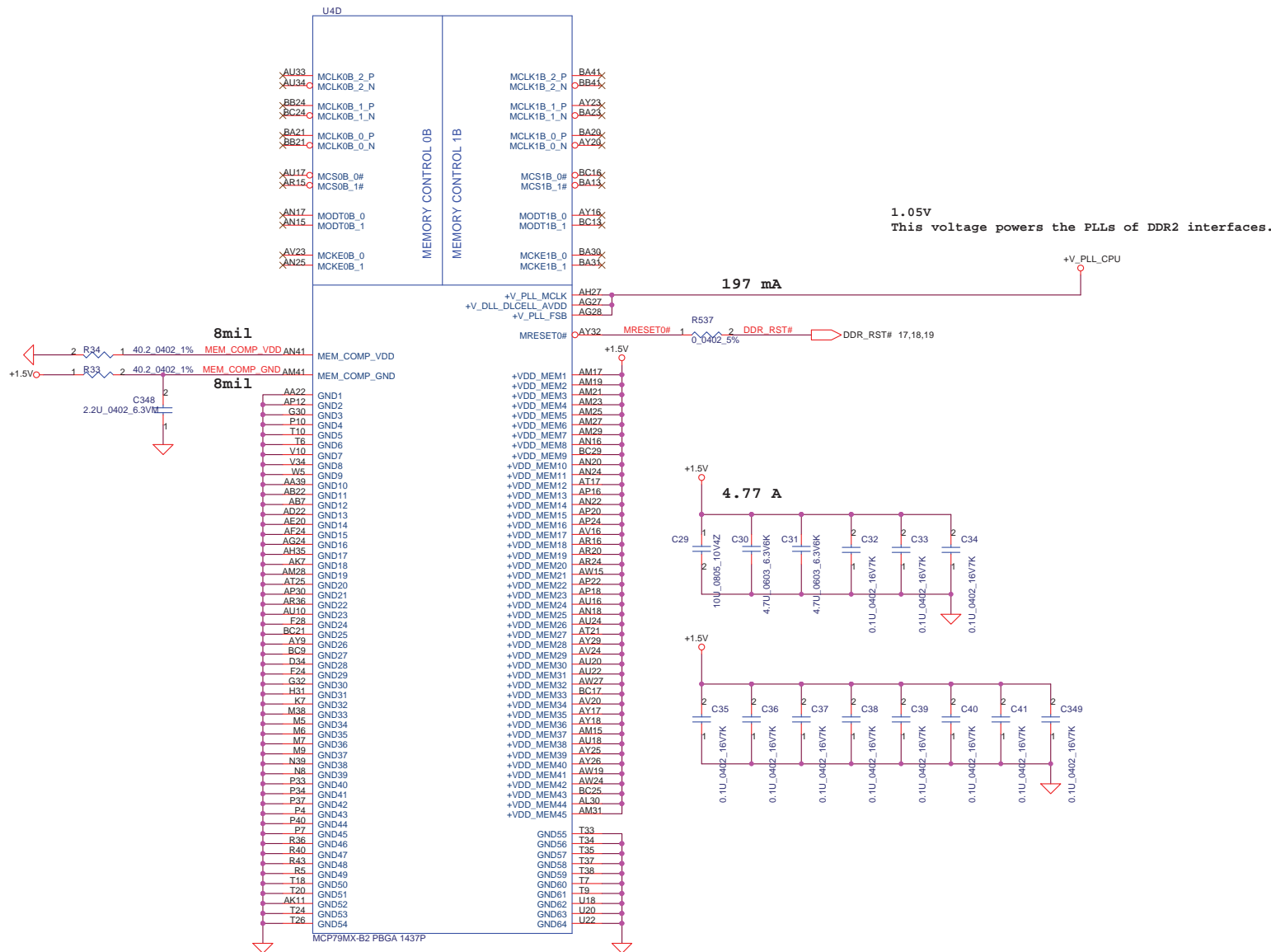
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MCP79(1/10)-FRONT SIDE BUS		
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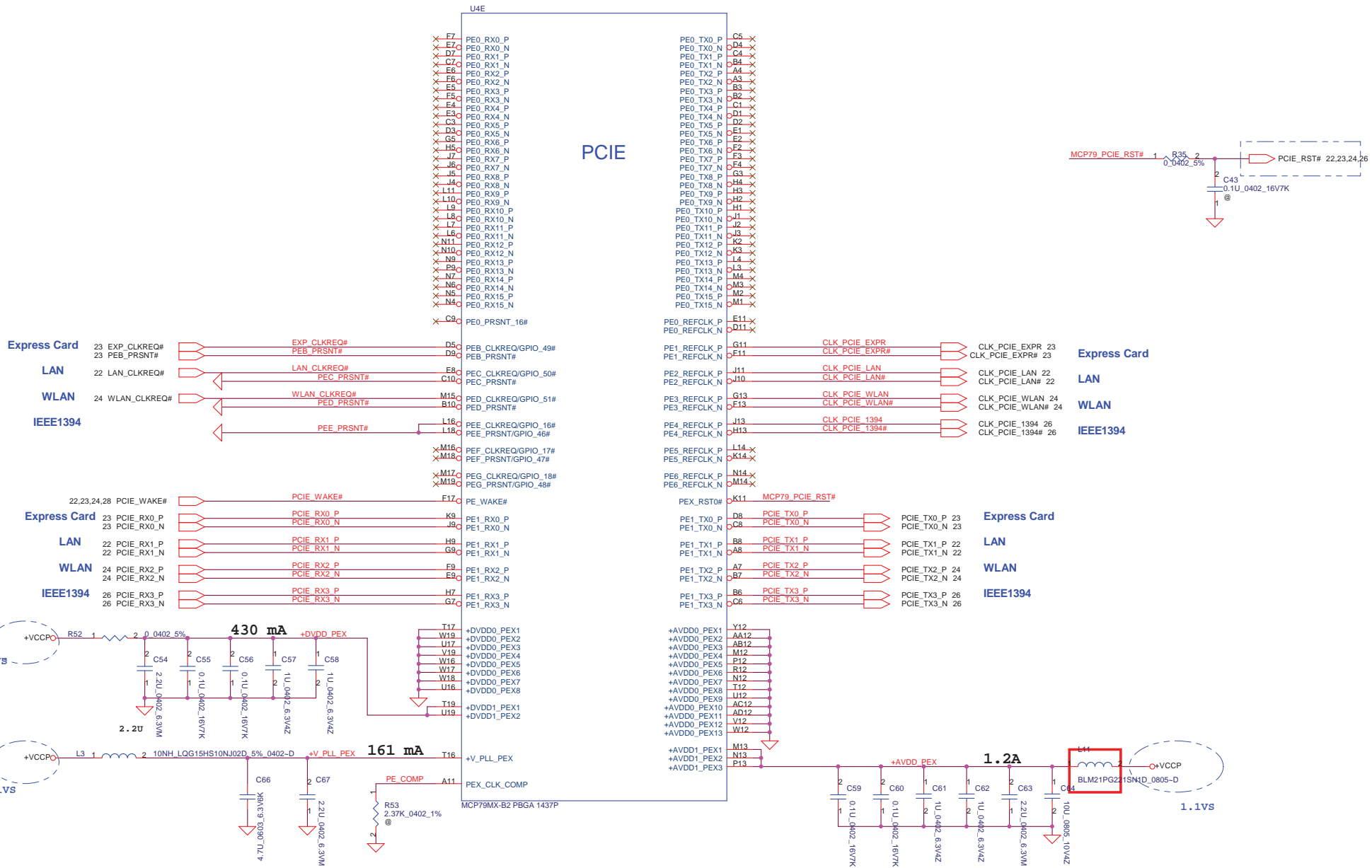


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Issued Date	2009/02/19	Deciphered Date	2009/12/31	Title
				MCP79(2/10)-MEM PARTS 0 & 1
				Size Document Number
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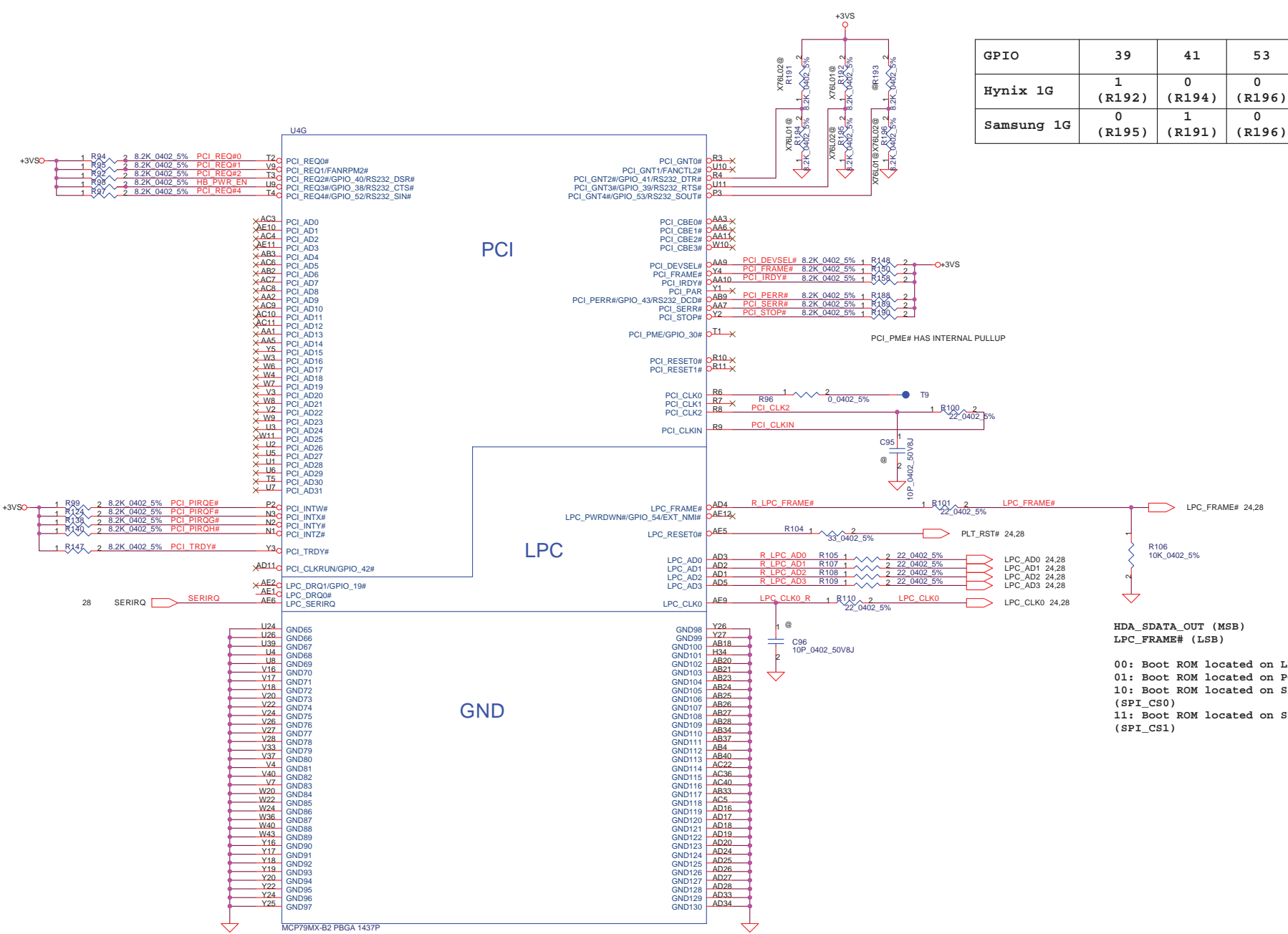
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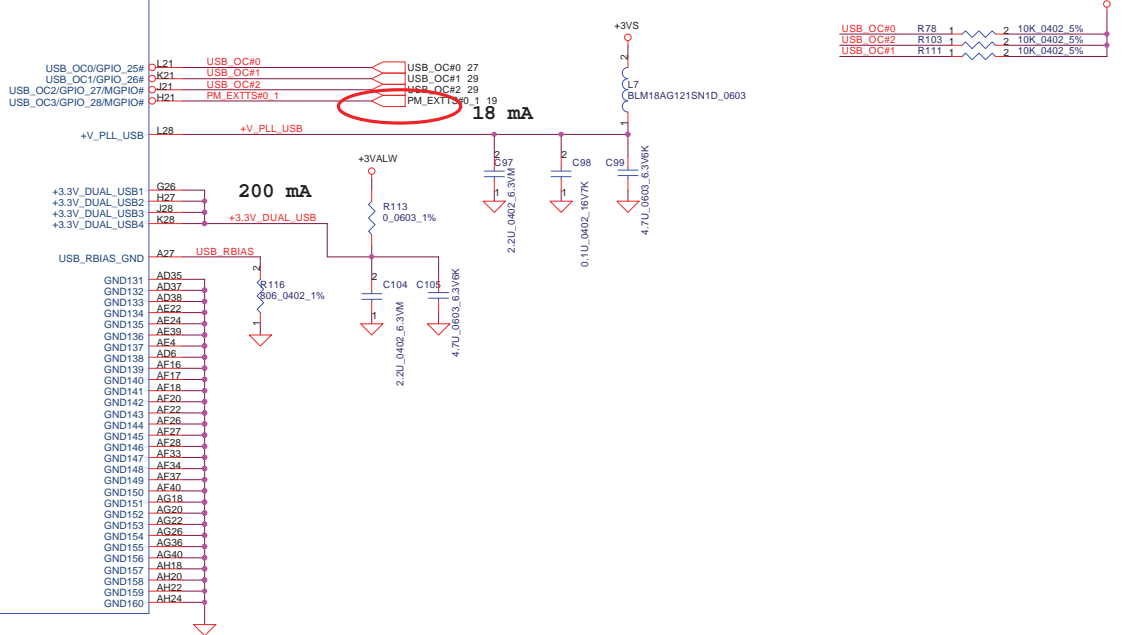
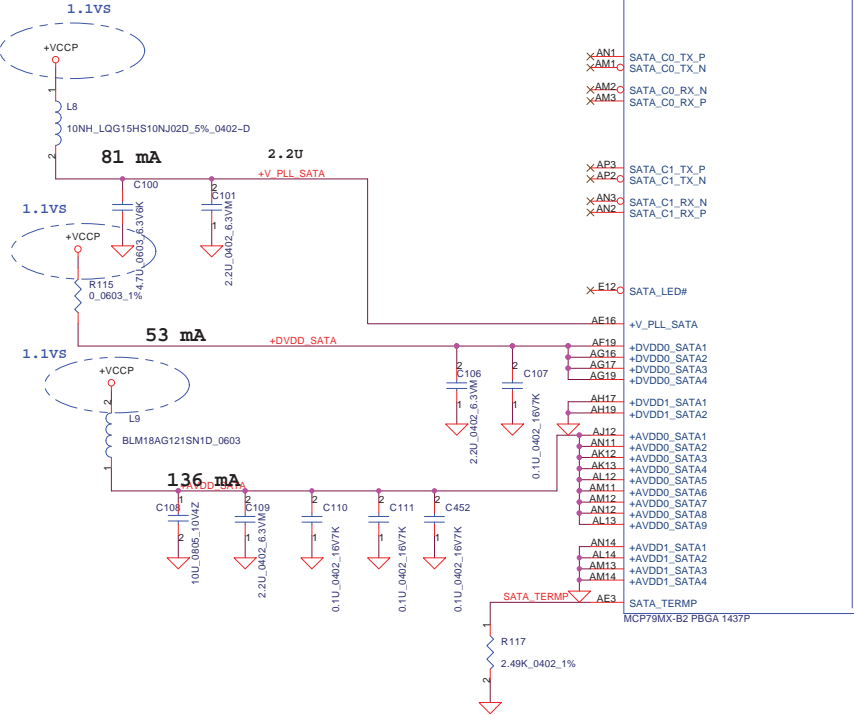
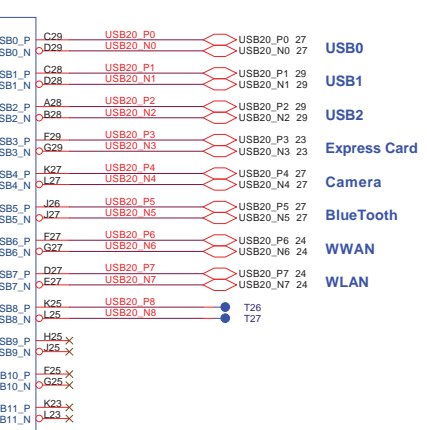
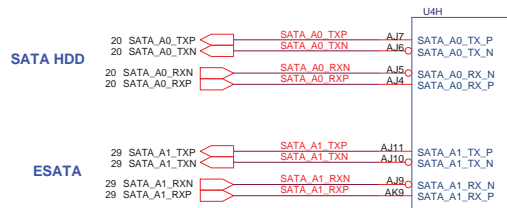


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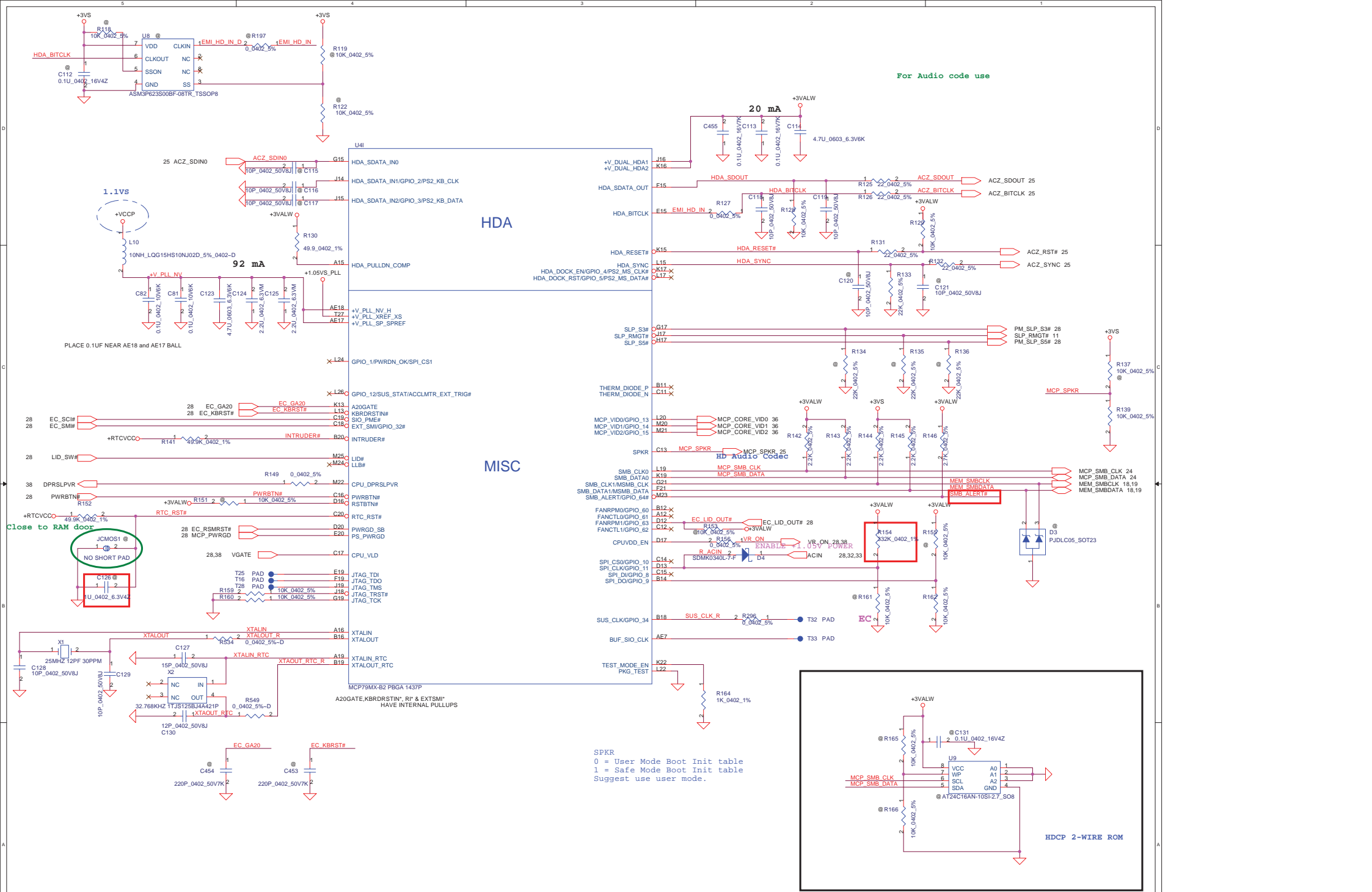


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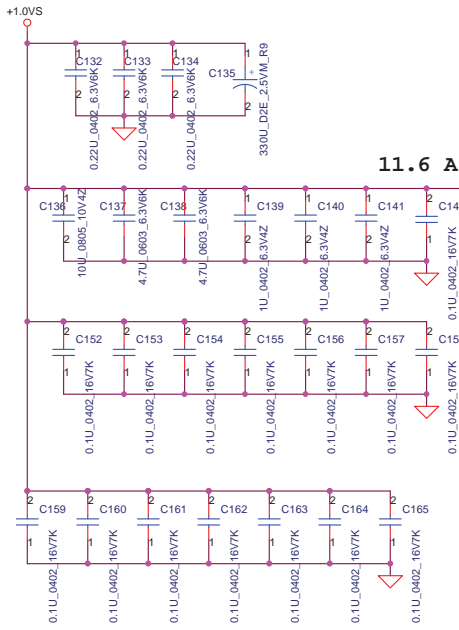


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0.75V ~ 1.05 V



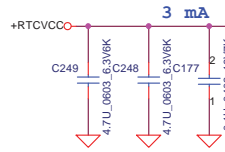
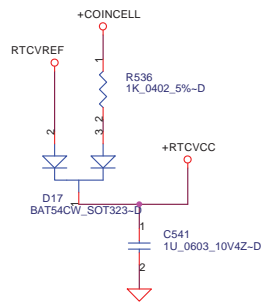
11.6 A

- AA25 +VDD CORE1
- AC23 +VDD CORE2
- U25 +VDD CORE3
- AH12 +VDD CORE4
- AG10 +VDD CORE5
- AG5 +VDD CORE6
- Y21 +VDD CORE7
- Y23 +VDD CORE8
- AA16 +VDD CORE9
- AA26 +VDD CORE10
- AA27 +VDD CORE11
- AA28 +VDD CORE12
- AC16 +VDD CORE13
- AC17 +VDD CORE14
- AC18 +VDD CORE15
- AC19 +VDD CORE16
- AC20 +VDD CORE17
- AC21 +VDD CORE18
- AA17 +VDD CORE19
- AC24 +VDD CORE20
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- AC26 +VDD CORE22
- AC27 +VDD CORE23
- AC28 +VDD CORE24
- AD21 +VDD CORE25
- AD23 +VDD CORE26
- W27 +VDD CORE27
- V25 +VDD CORE28
- AA18 +VDD CORE29
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- AA19 +VDD CORE39
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- AF7 +VDD CORE45
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- AF9 +VDD CORE47
- AA20 +VDD CORE48
- AG11 +VDD CORE49
- AG12 +VDD CORE50
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- AG7 +VDD CORE56
- AA21 +VDD CORE57
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- AH5 +VDD CORE72
- AH6 +VDD CORE73
- AH7 +VDD CORE74
- AH9 +VDD CORE75
- AA24 +VDD CORE76
- W21 +VDD CORE77
- W22 +VDD CORE78
- W23 +VDD CORE79
- W25 +VDD CORE80
- AF12 +VDD CORE81

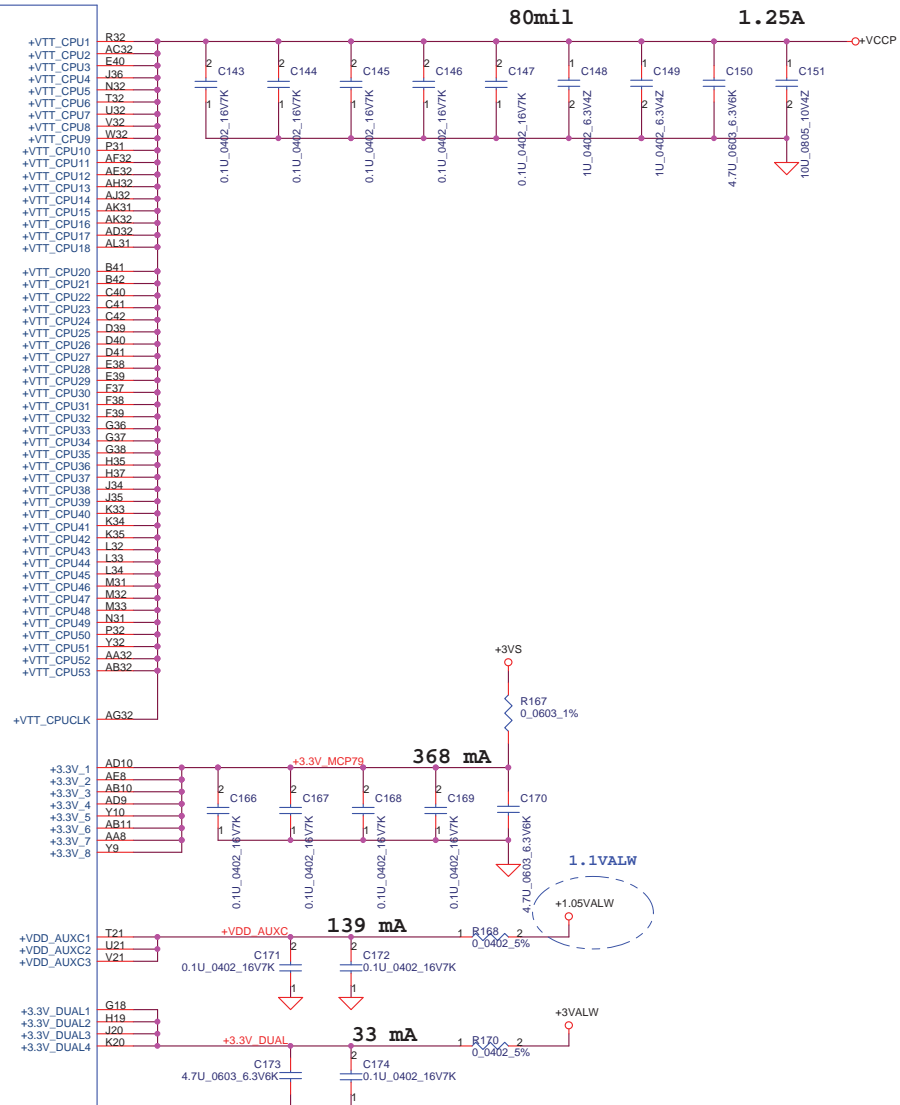
POWER

MCP79MX-B2 PBGA 1437P

RTC Battery



3 mA



80mil

1.25A

368 mA

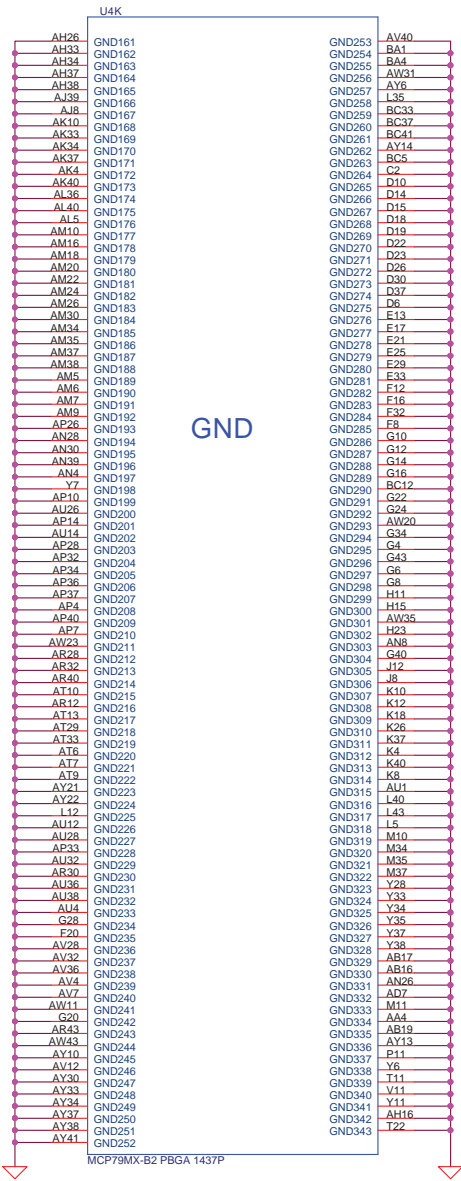
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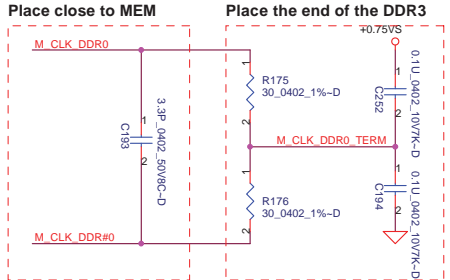
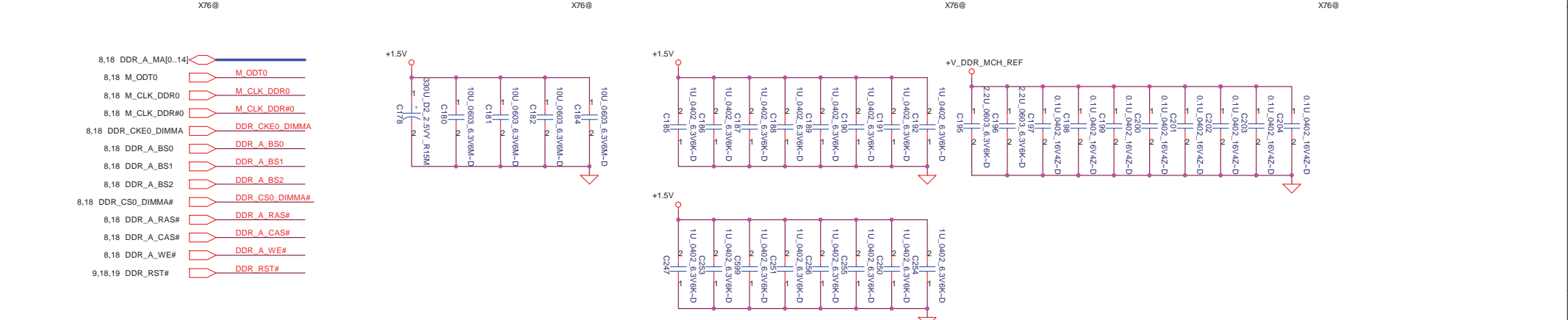
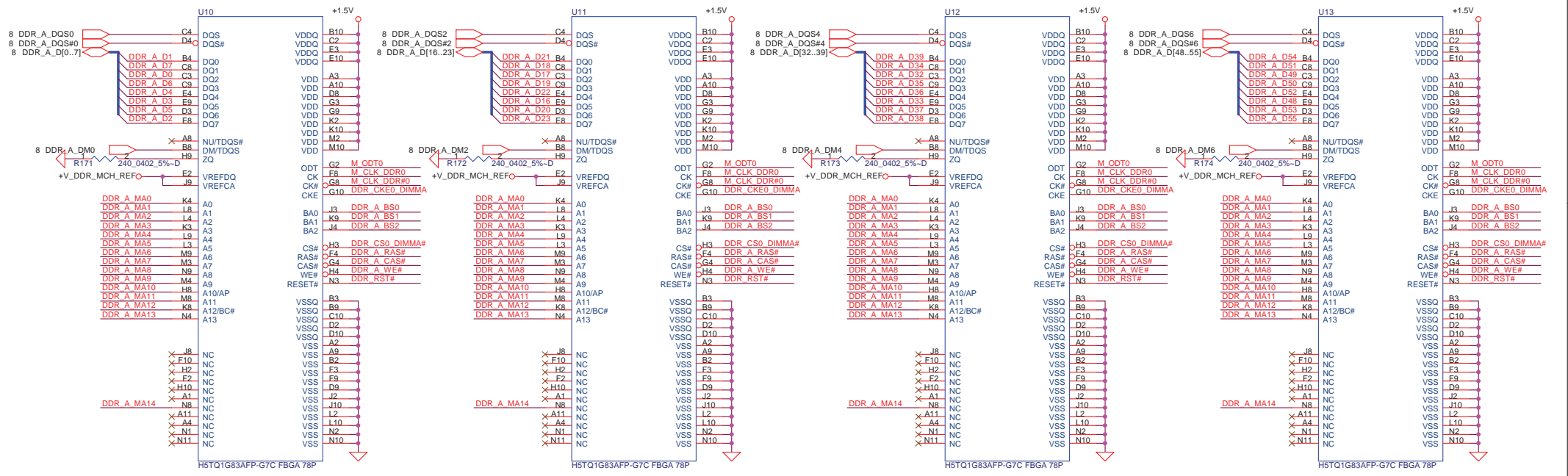
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+1.05VALW

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Issued Date	2009/02/19	Deciphered Date	2009/12/31	MCP79(9/10)-POWER&RTC Batt	
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Size	Document Number	Rev	1.0	
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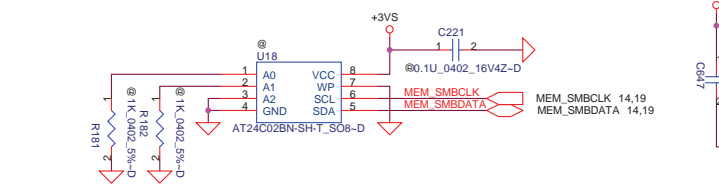
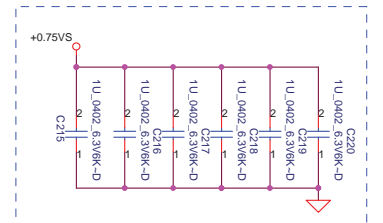
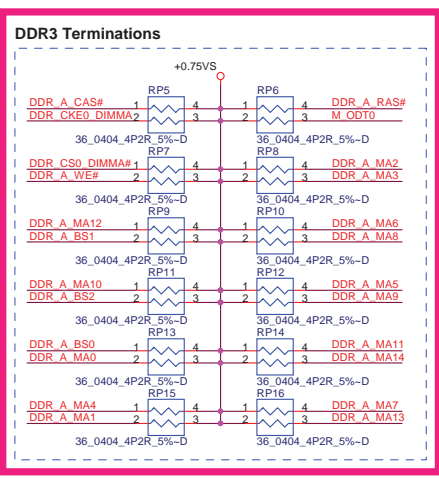
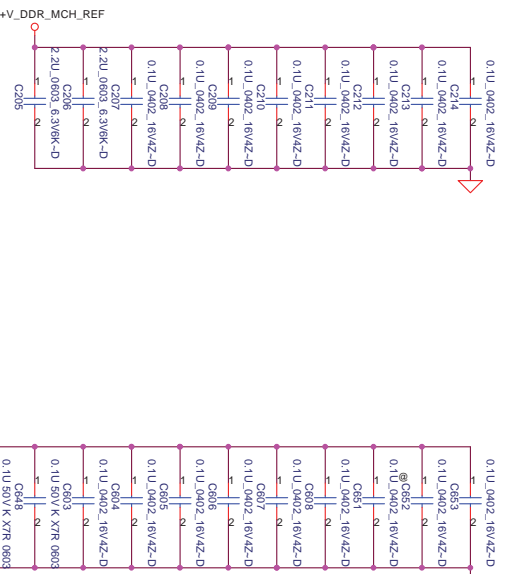
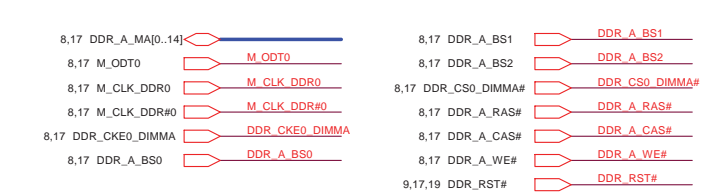
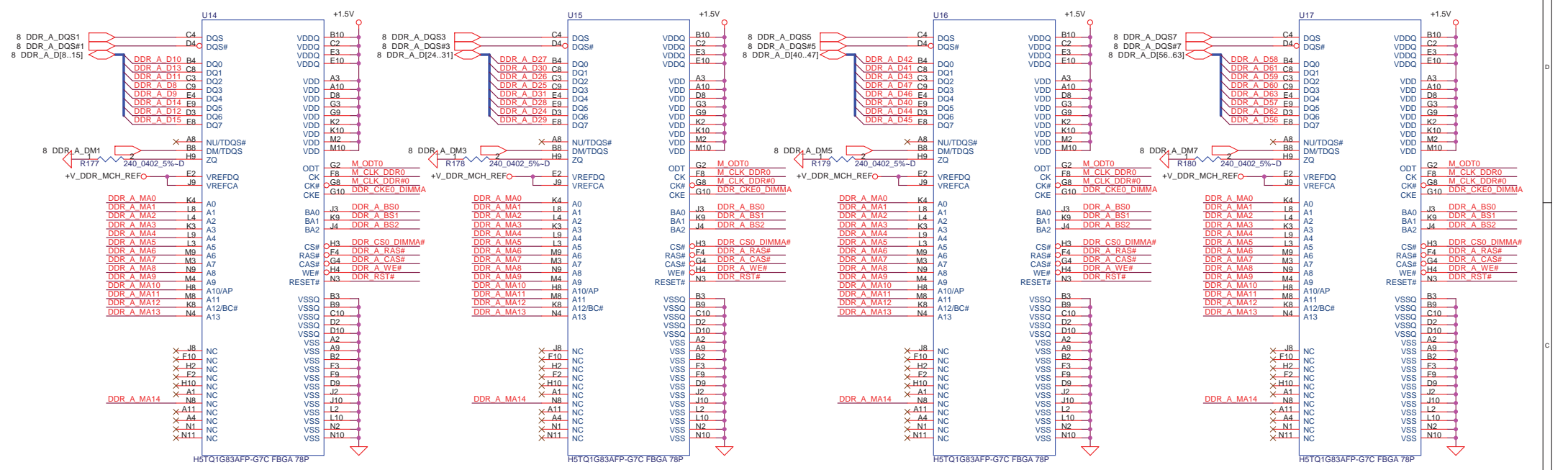


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Hynix	(8*11.5) Hynix DDR3 (1066): SA00002P00L (H5TQ1G83AFP-G7C FBGA 78P)

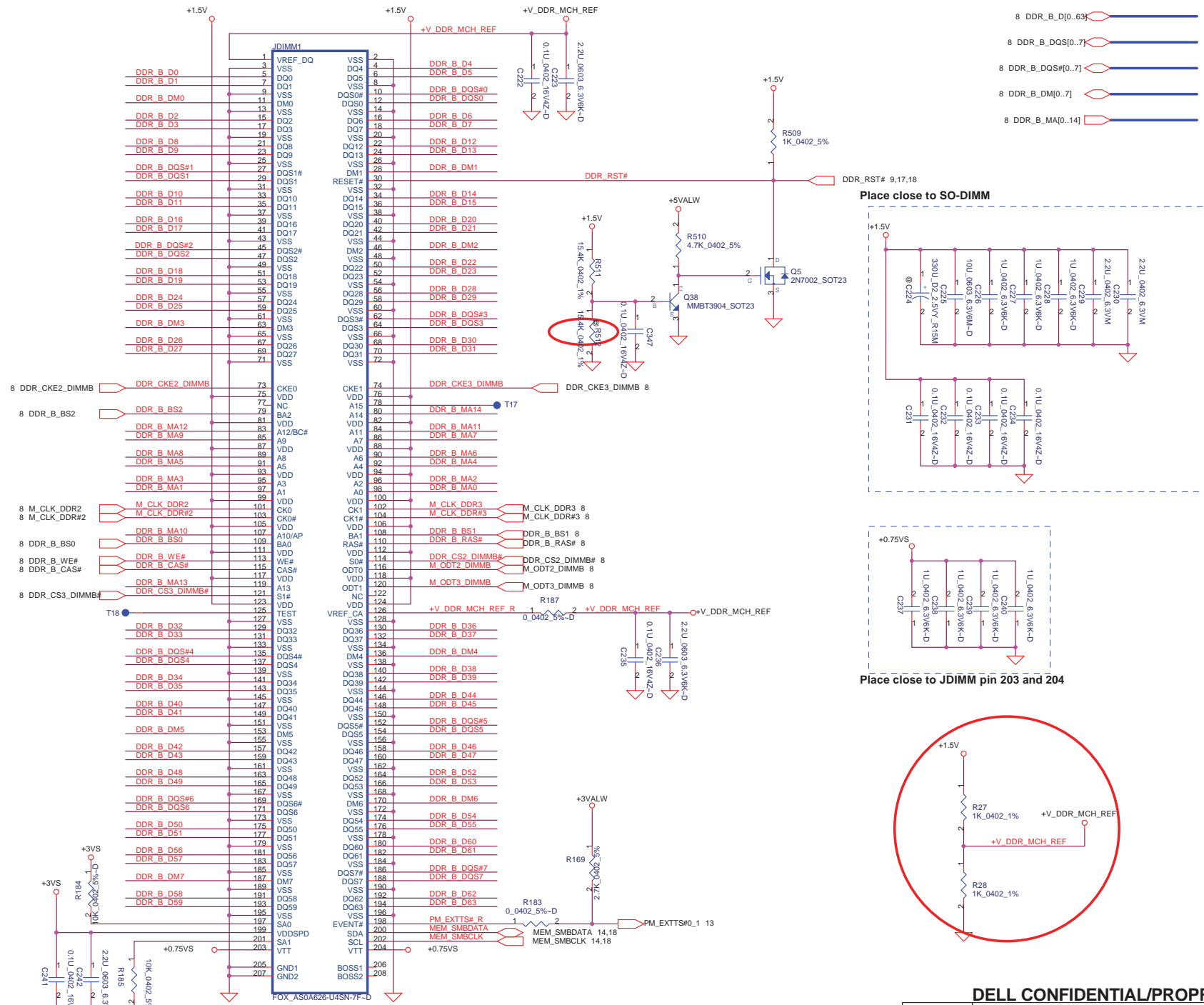
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Title DDR3II-Memory Down (Top)		
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Place decaps close end termination resistors, one decap for 4 resistors



DDR3 SO-DIMM/Standard Type

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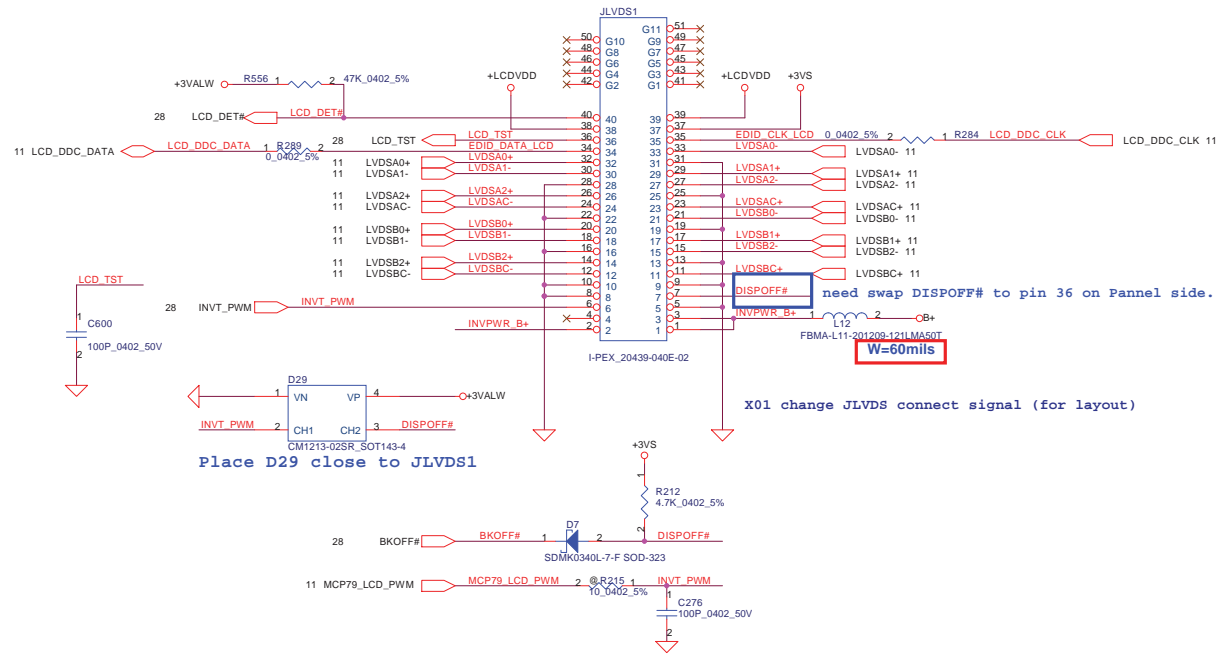
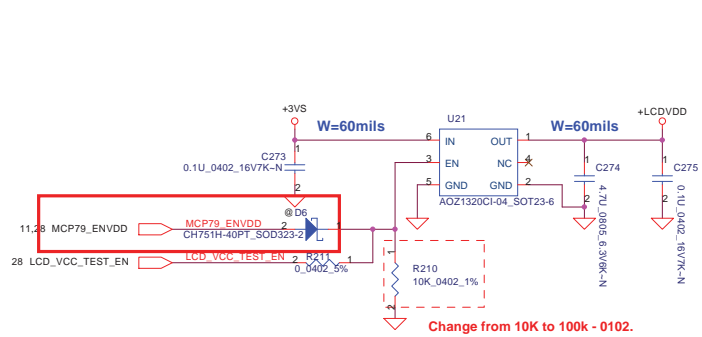
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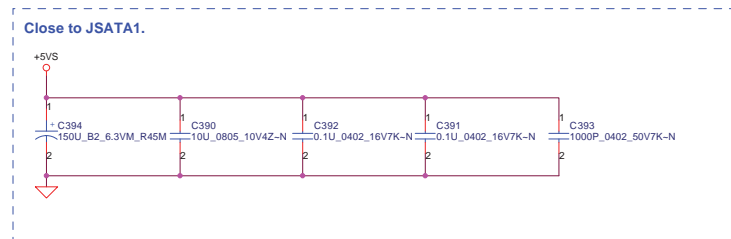
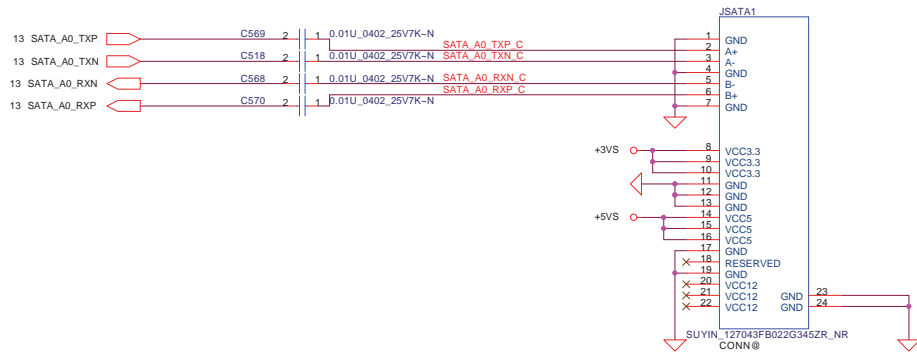


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LCD



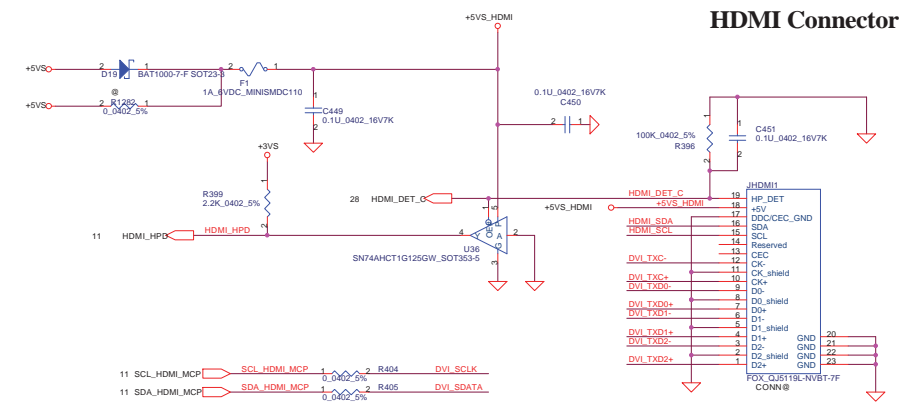
SATA HDD



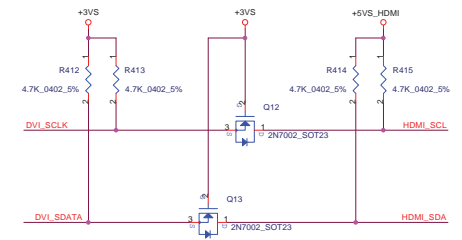
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LCD/SATA HDD	
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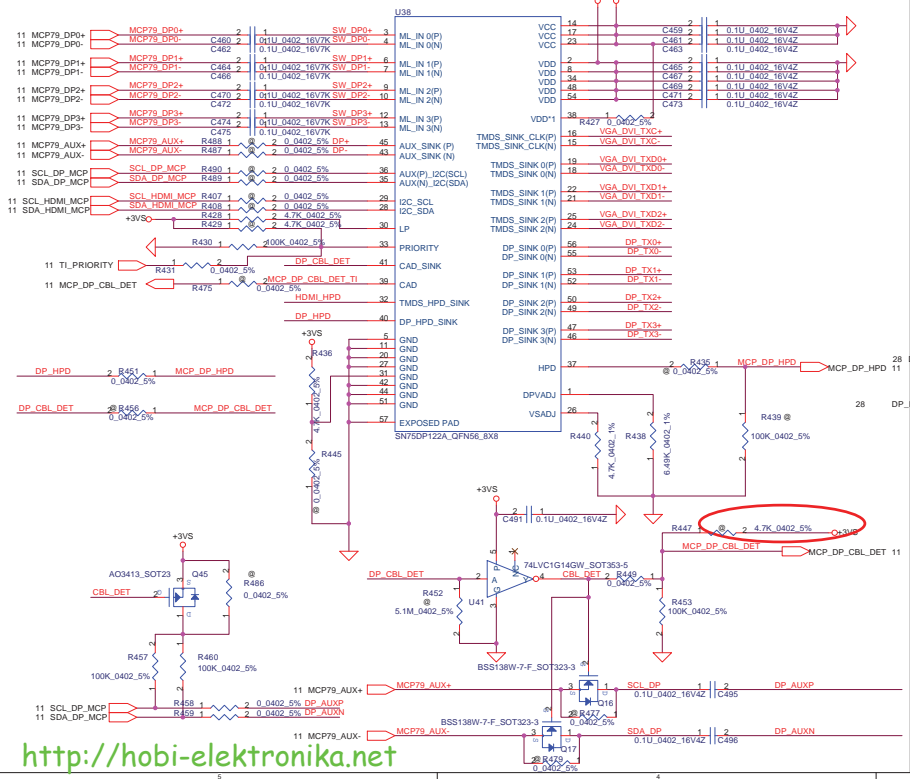
HDMI Connector



Close to JHDMI connector

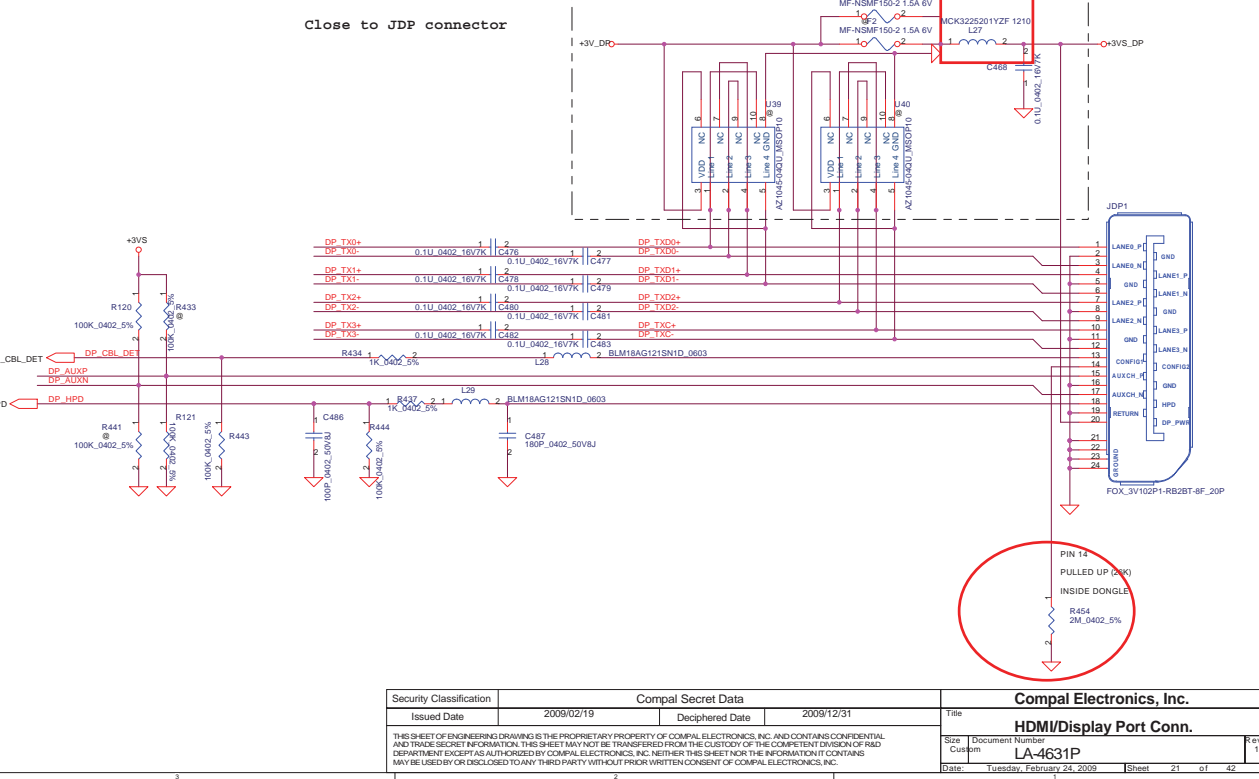


DisplayPort/TMDS 1:2 Switch/Translator

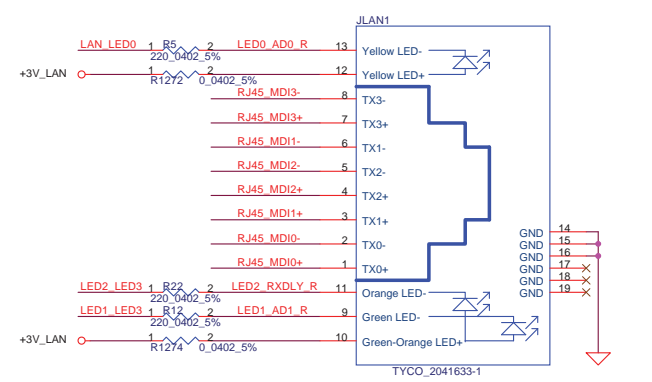
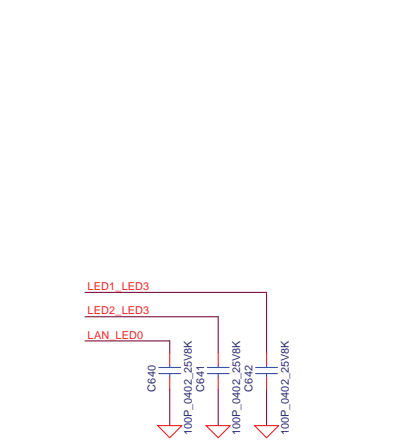
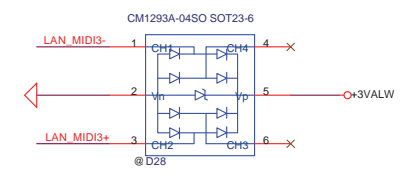
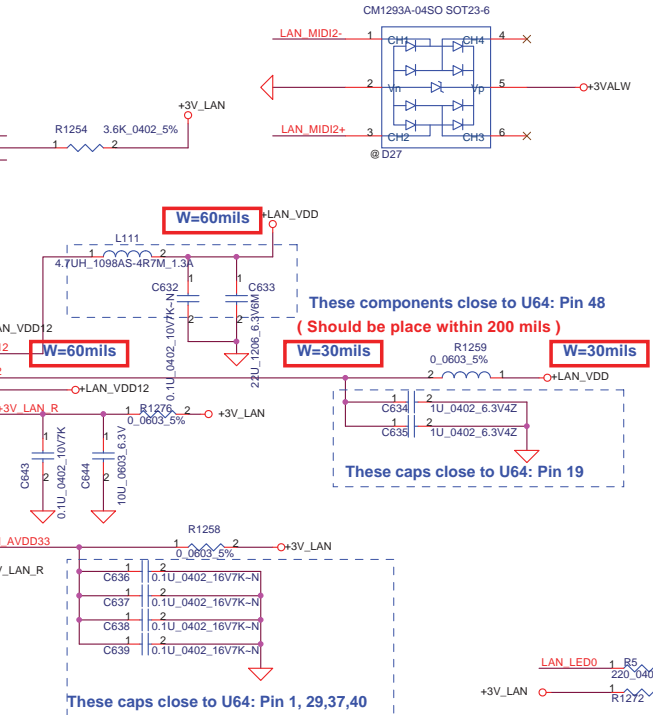
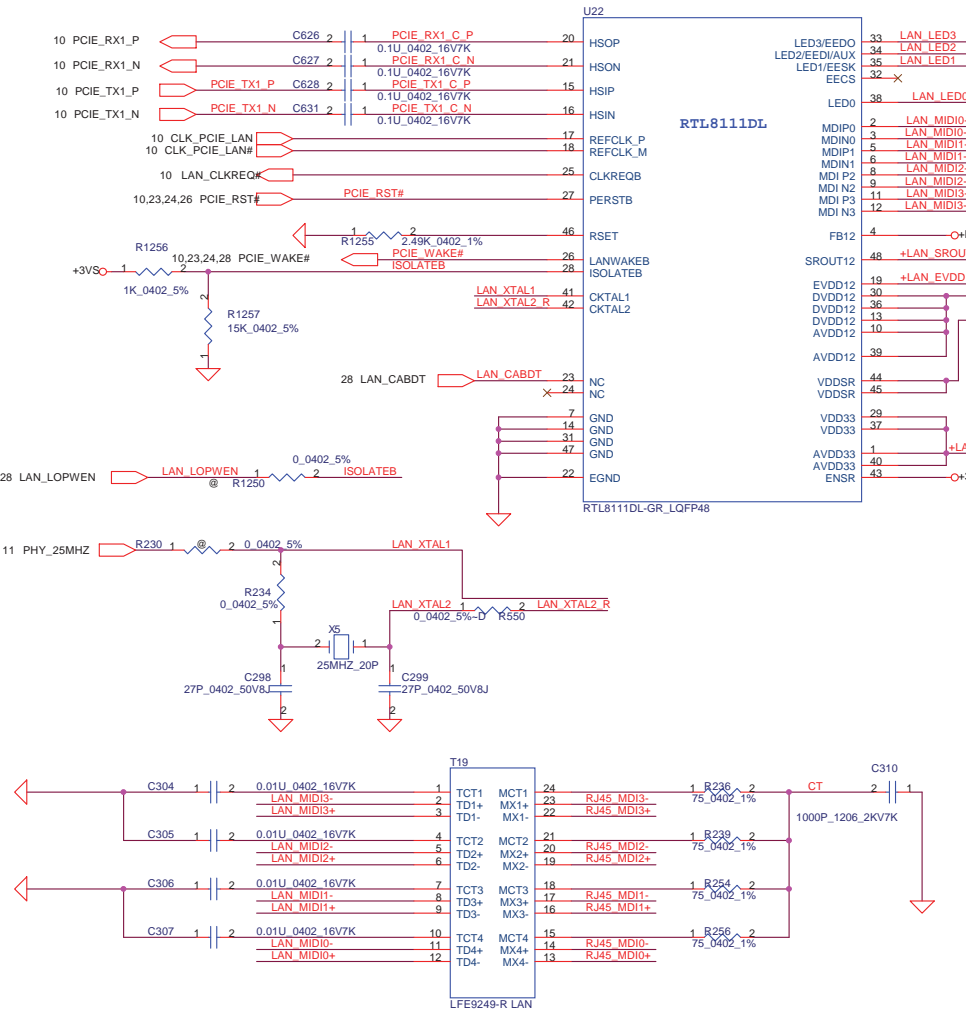
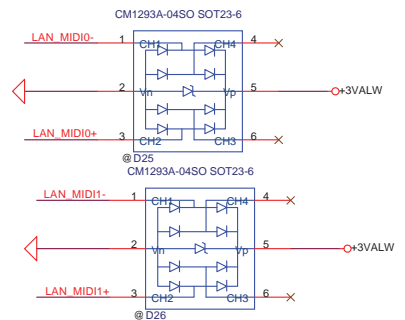
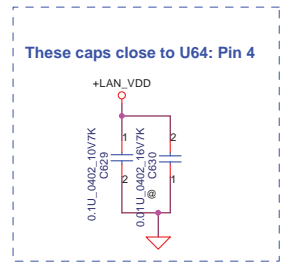
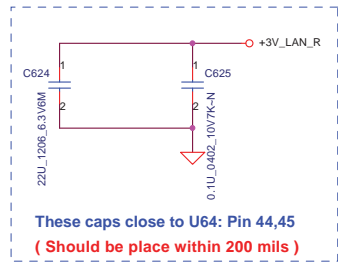
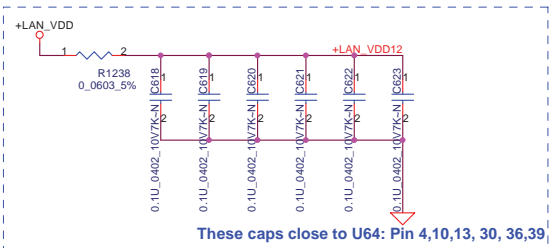
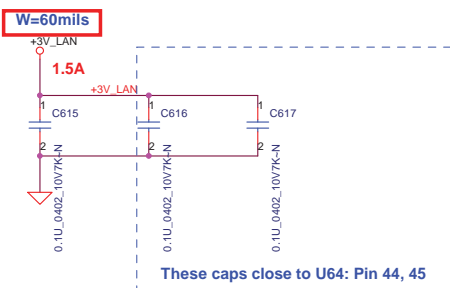


DisplayPort Connector

Close to JDP connector



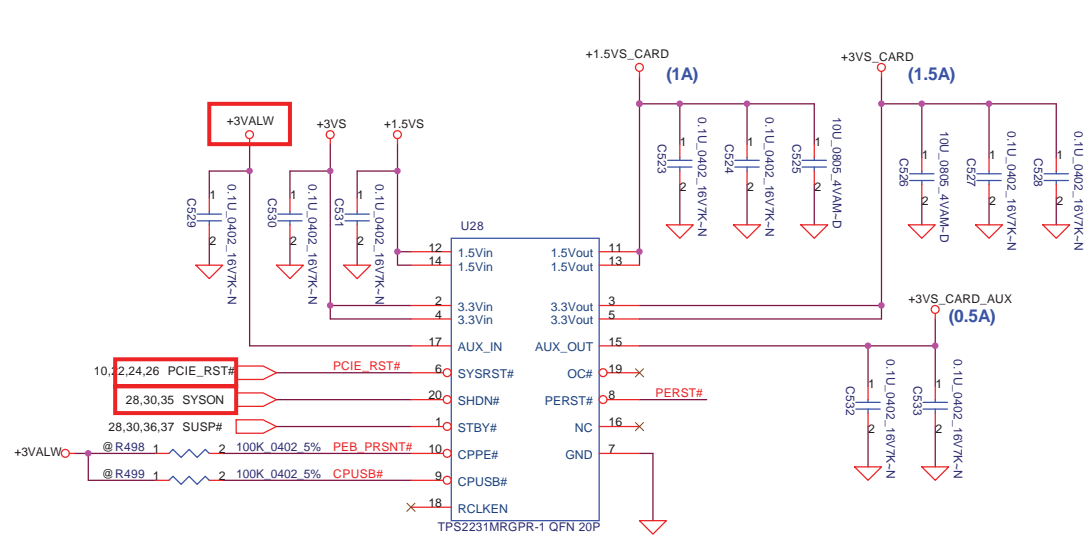
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				1.0
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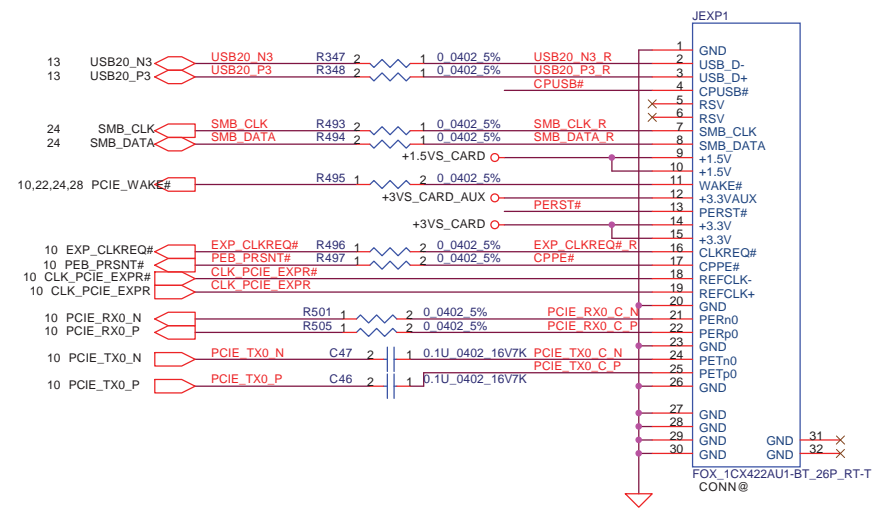
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Gigabit LAN RTL8111DL			
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Express Card Power Switch

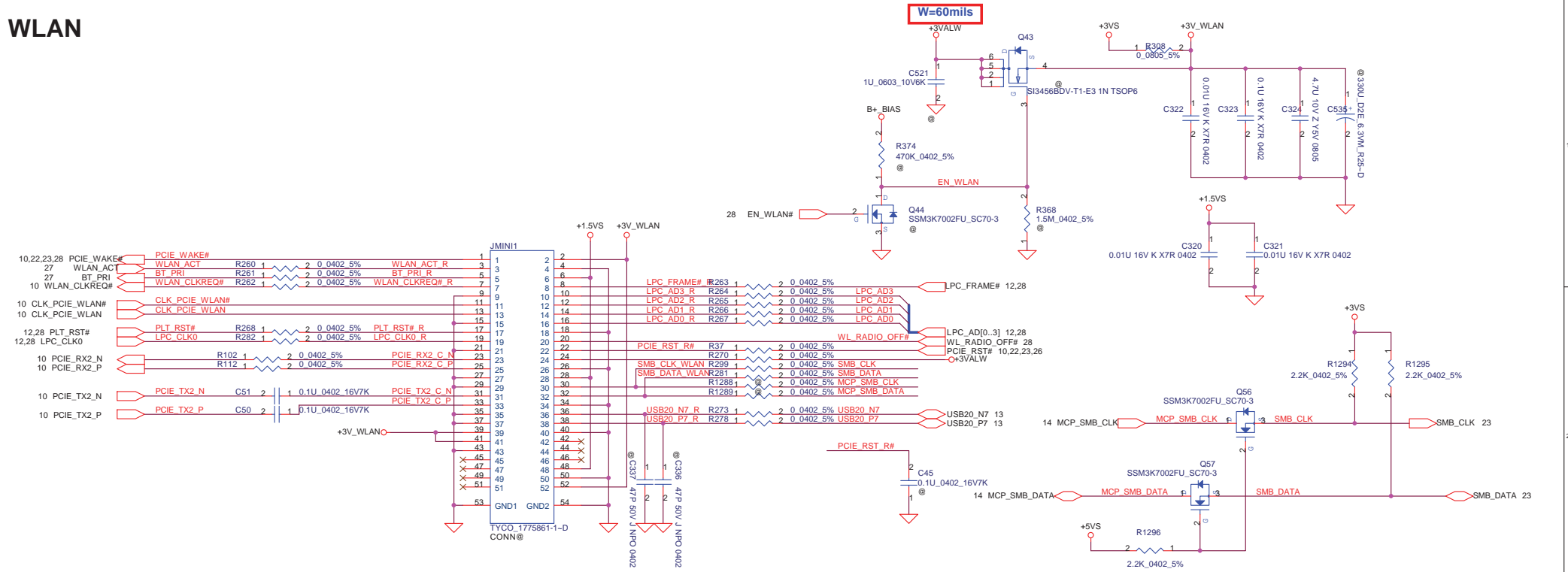


Express Card

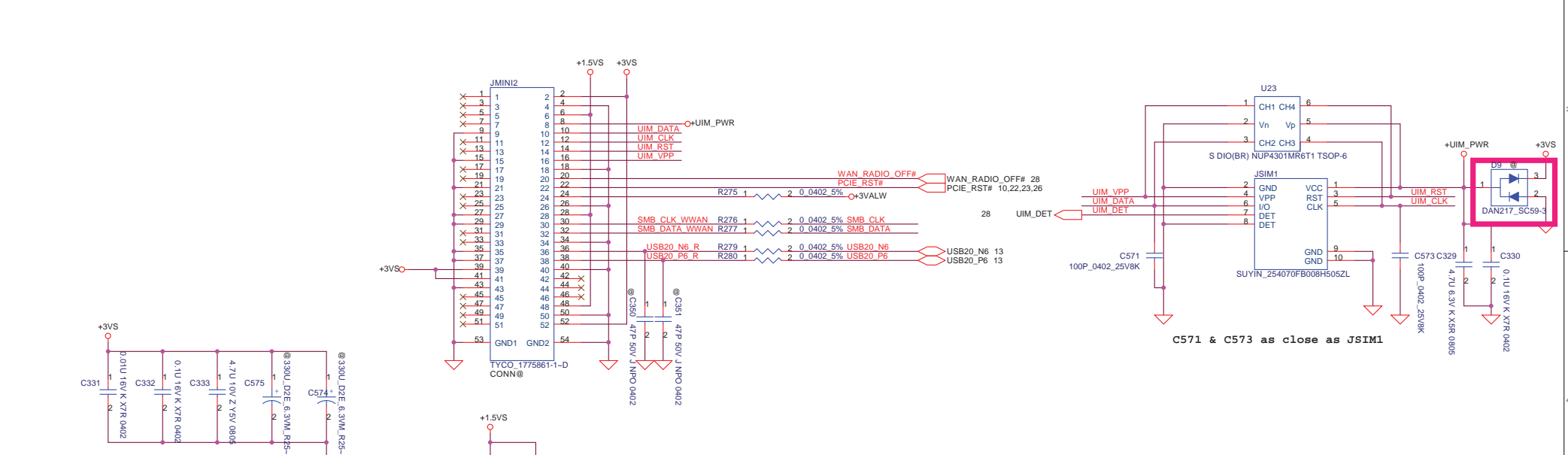


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WLAN



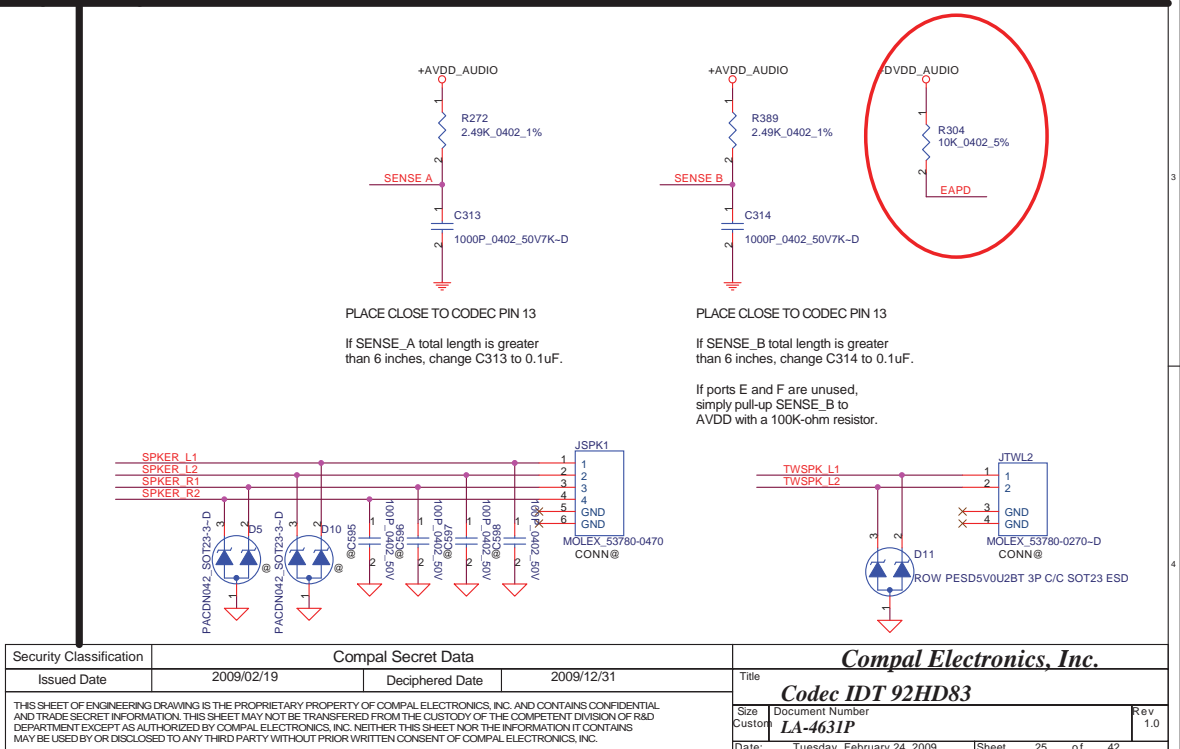
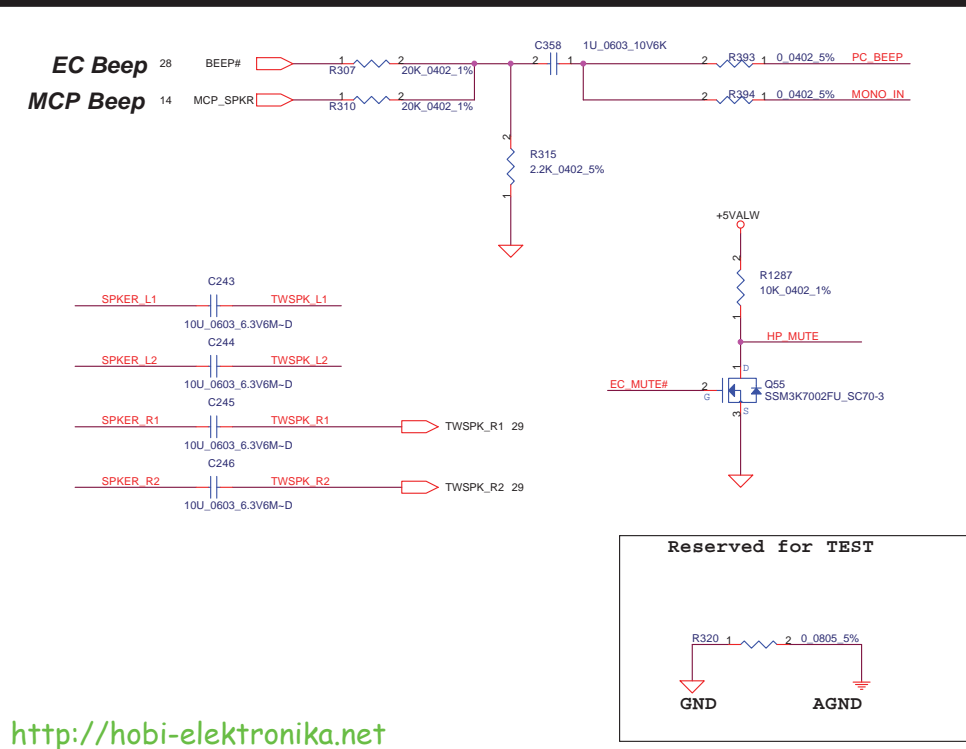
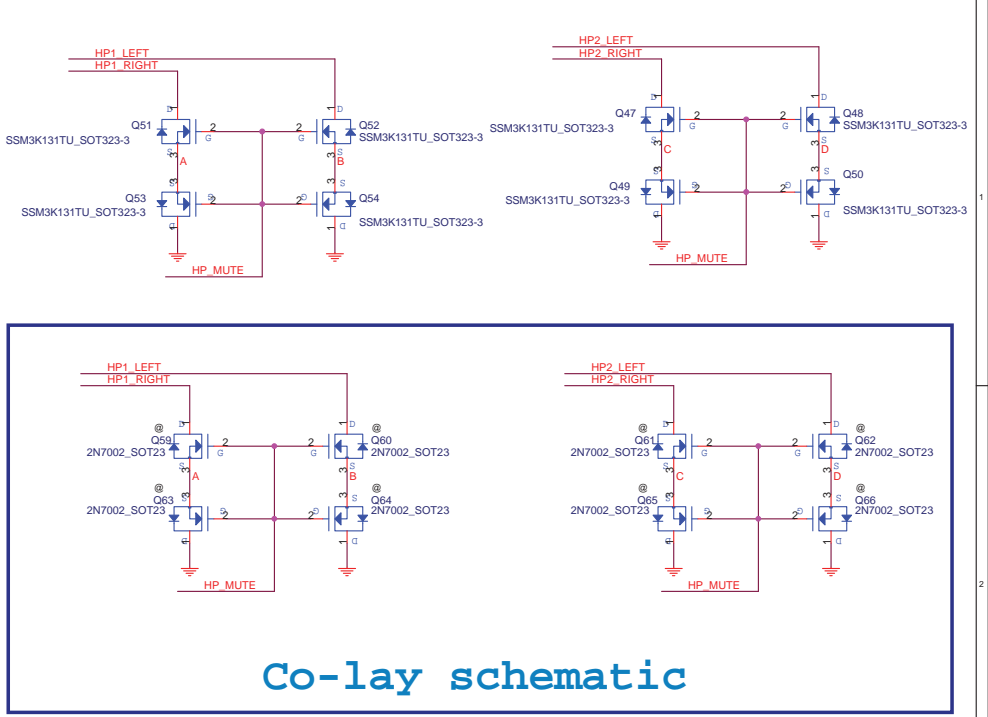
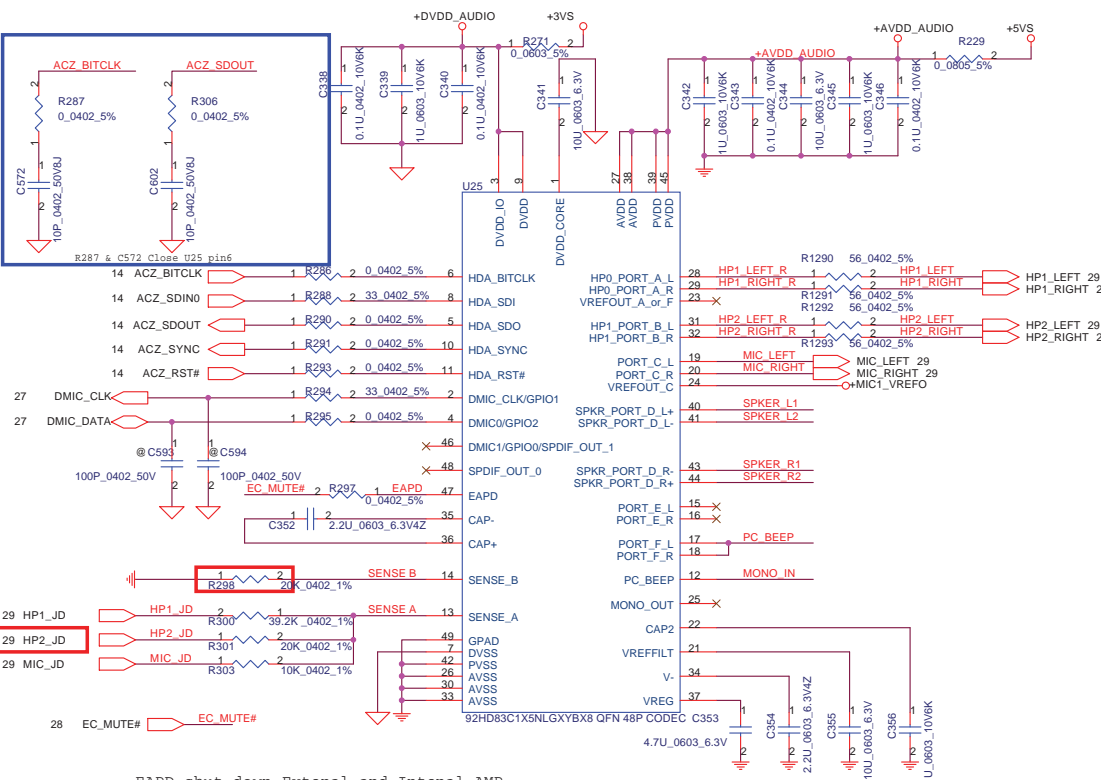
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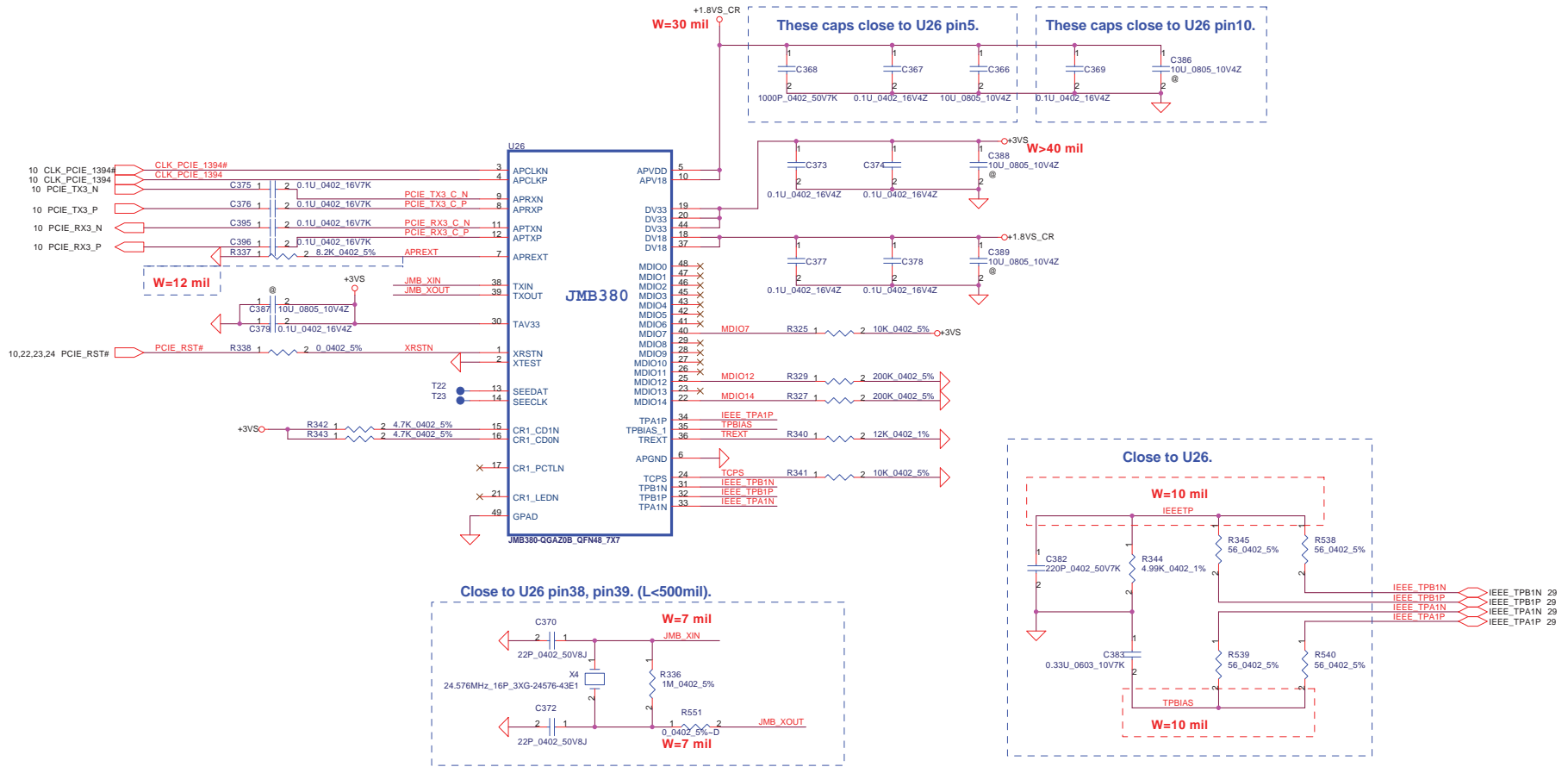
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Mini Card WLAN/WWAN		
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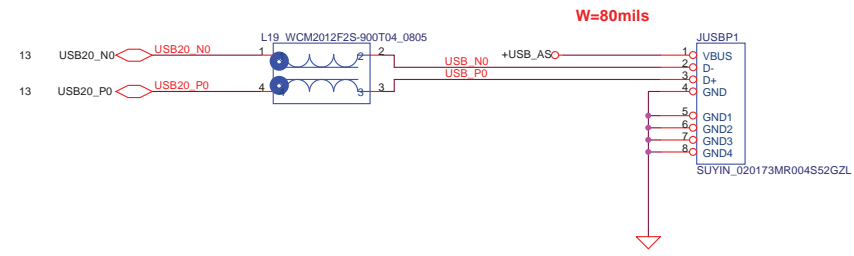
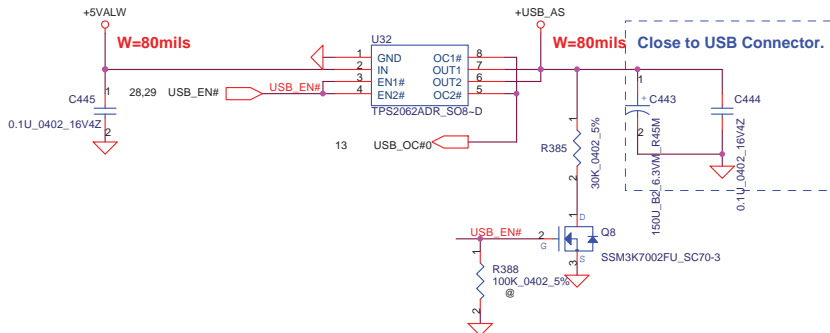


<http://hobi-elektronika.net>

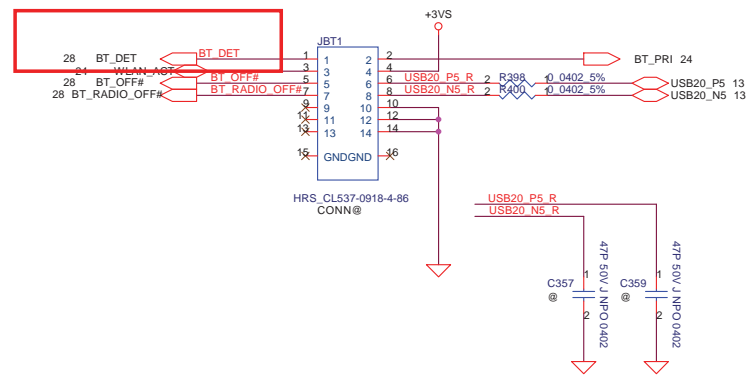
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Codec IDT 92HD83			Size
Custom			Document Number
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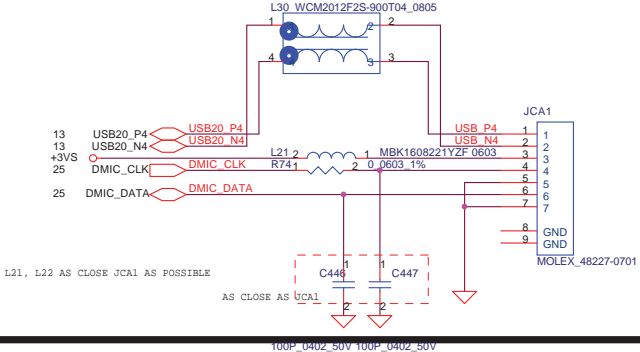
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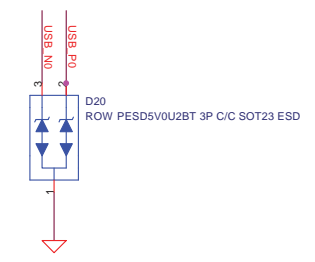
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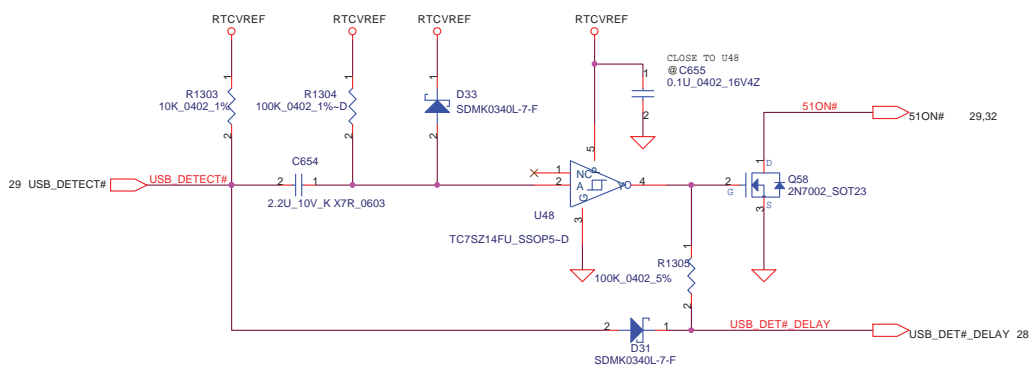
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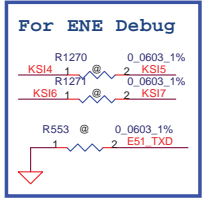
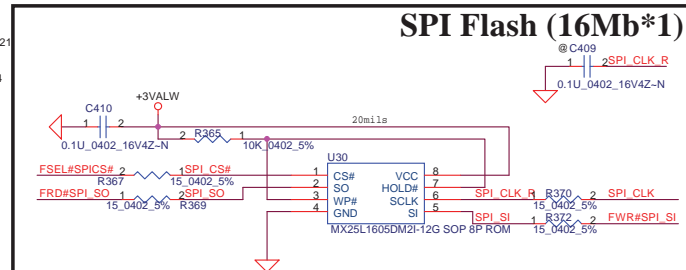
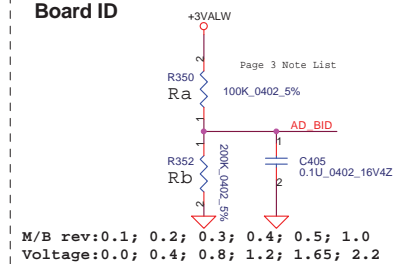
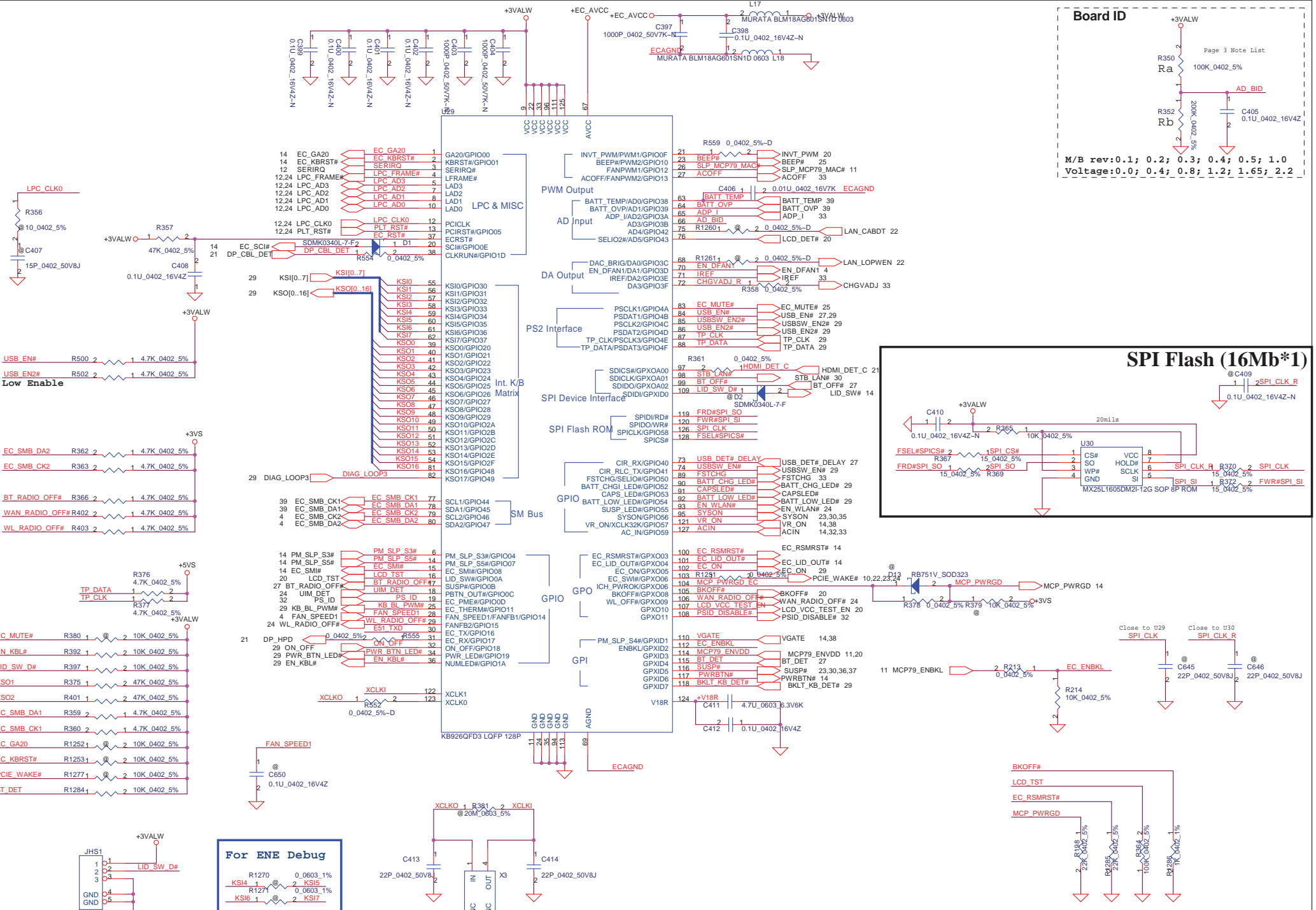
change JUSBP1 connect signal (for layout)



100P_0402_50V 100P_0402_50V



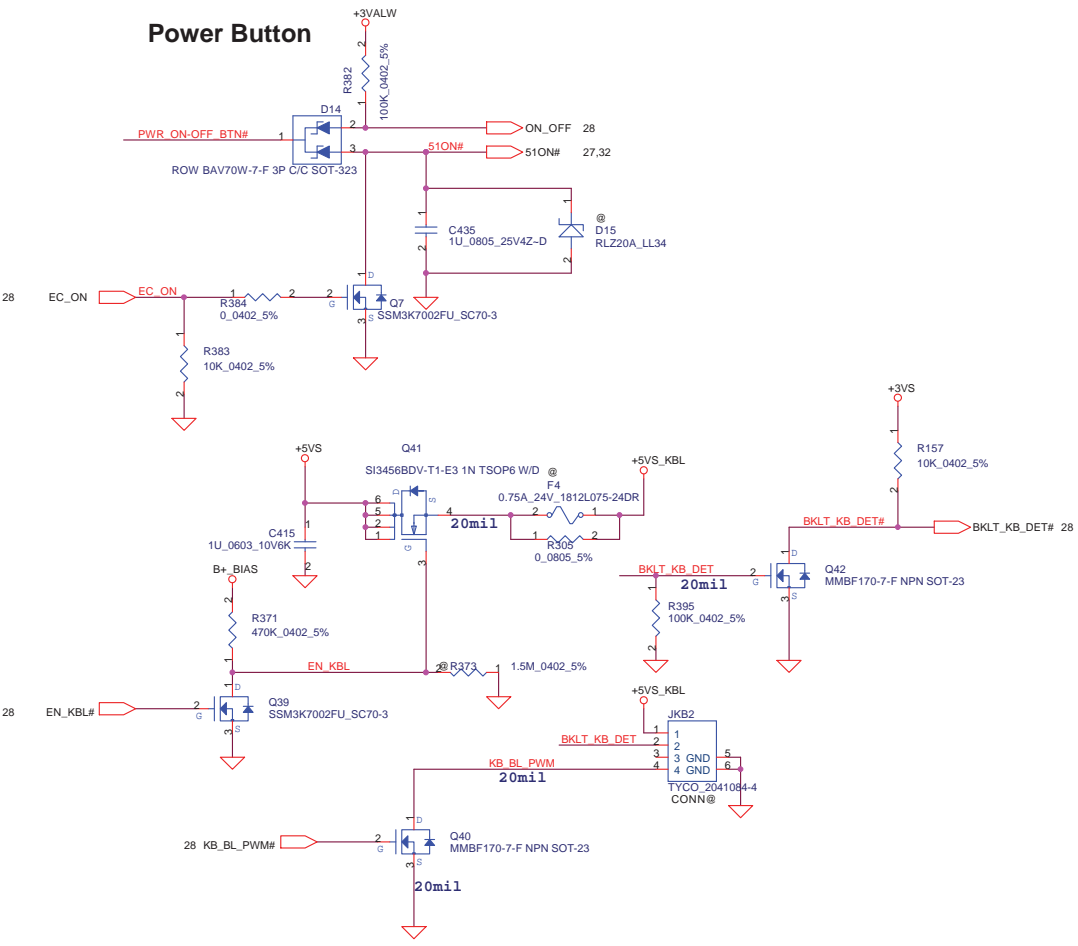
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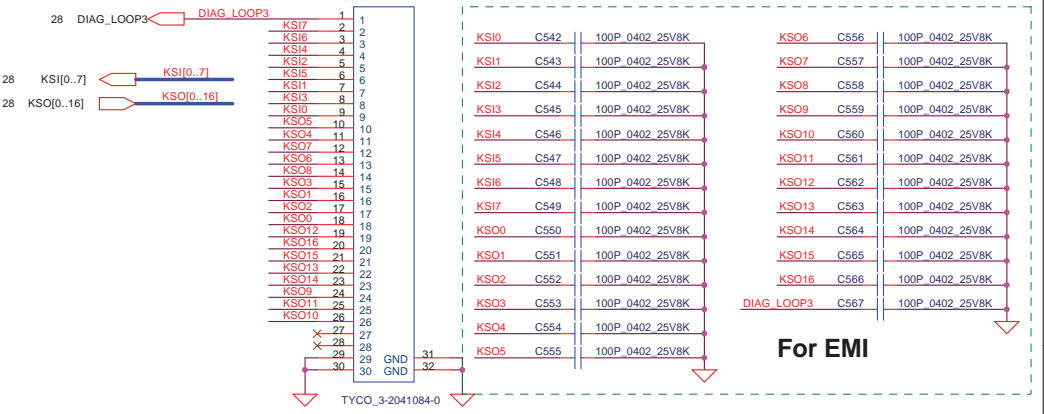
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Title		0.5A PC BIOS & EC I/O Port	
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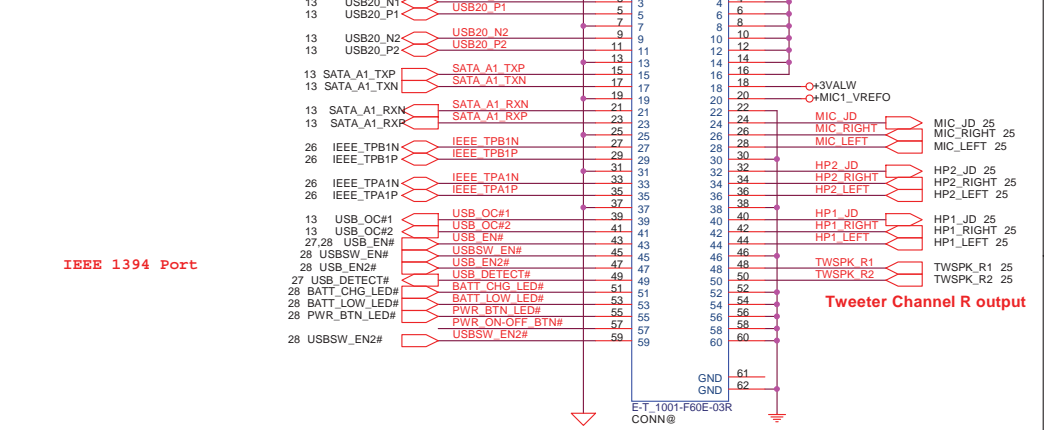
Power Button



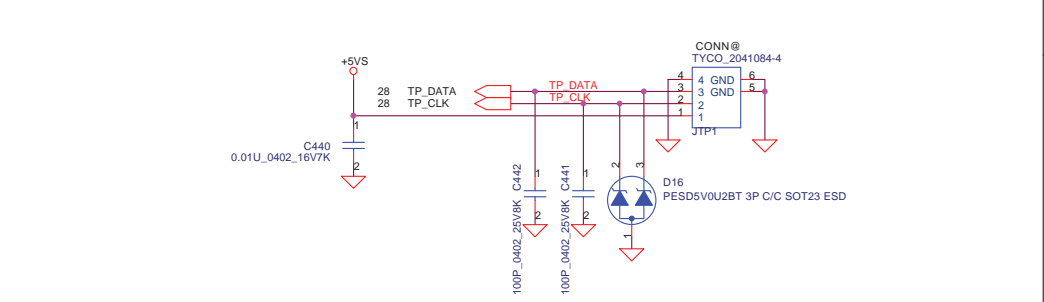
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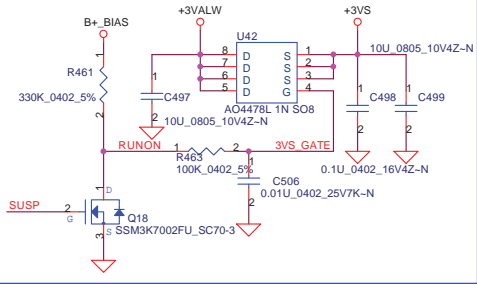
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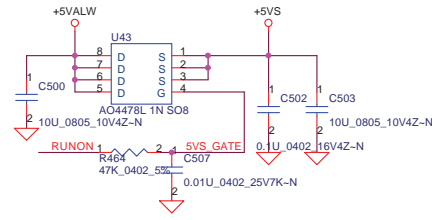
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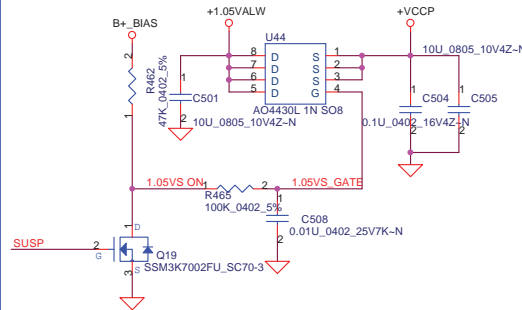
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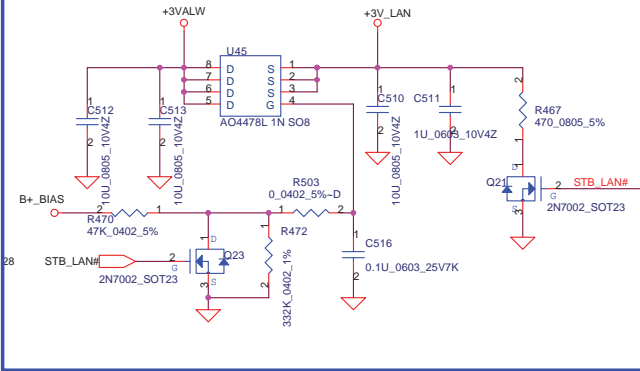
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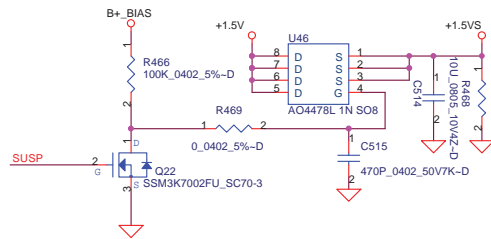
+1.05VALW to +VCCP Transfer



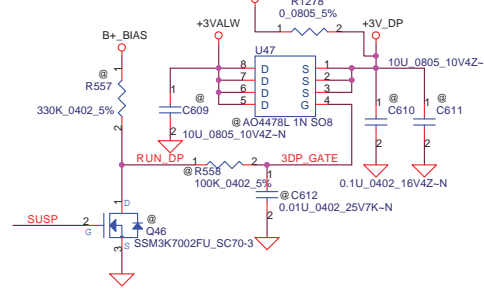
+3VALW TO +3V_LAN



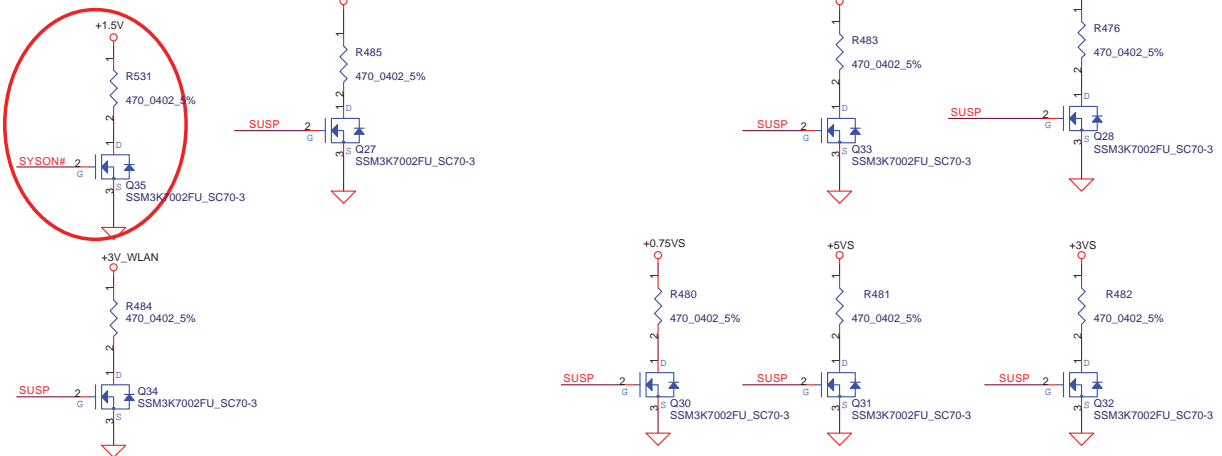
+1.5V to +1.5VS Transfer



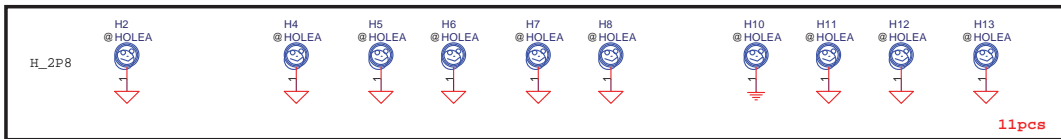
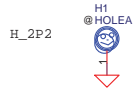
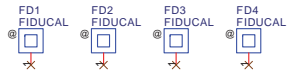
+3VALW to +3V_DP Transfer



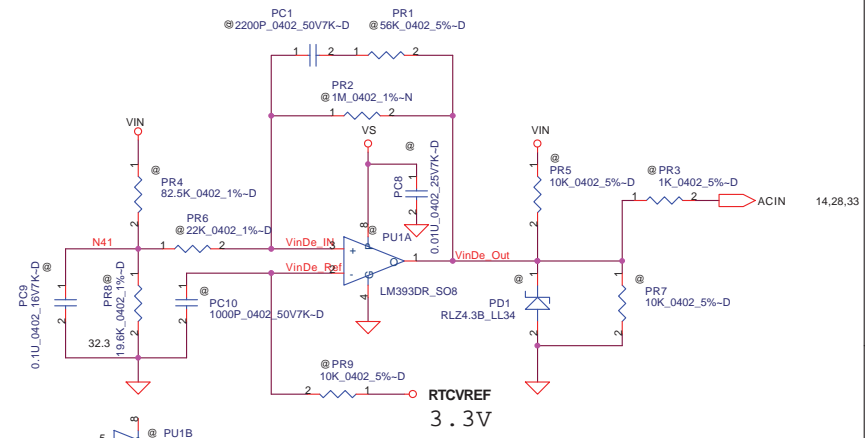
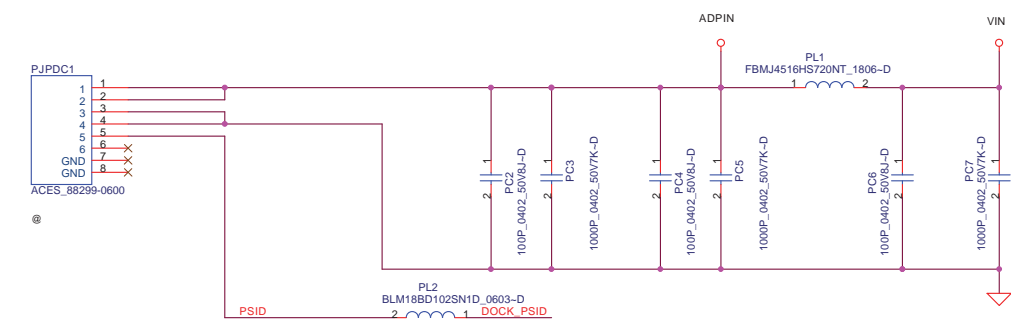
Discharge Circuit



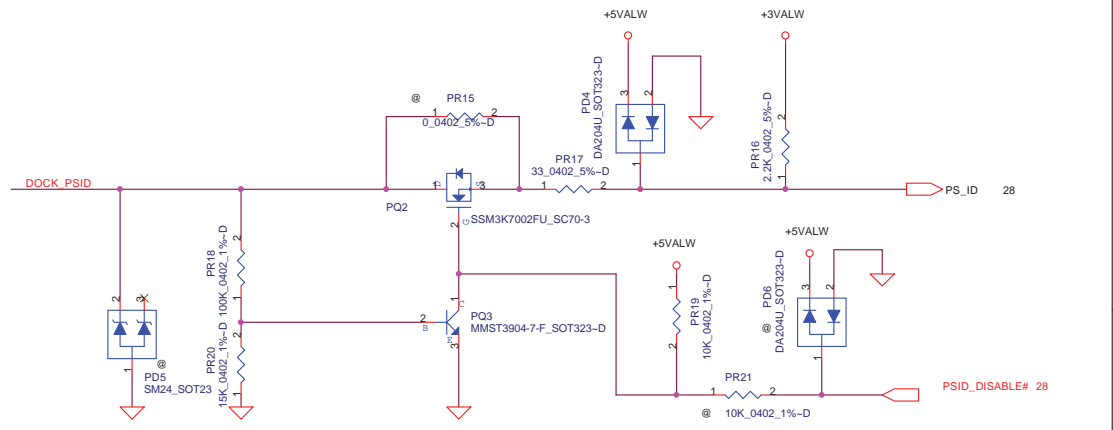
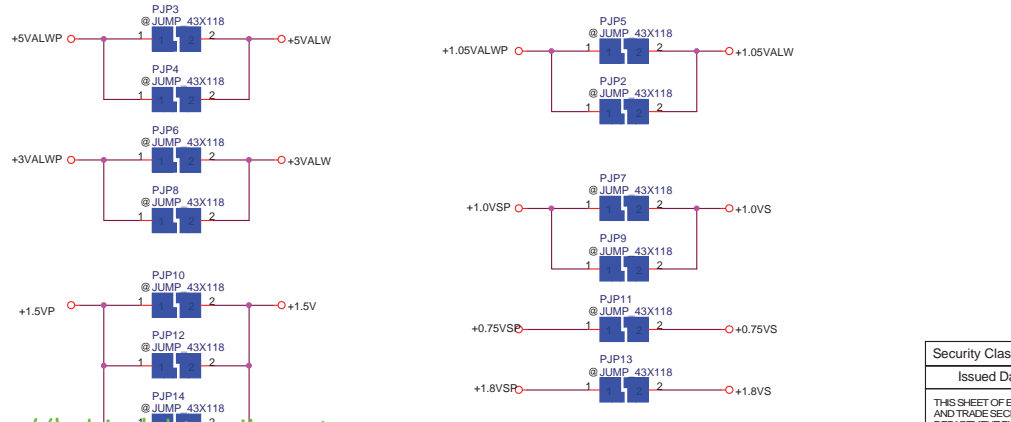
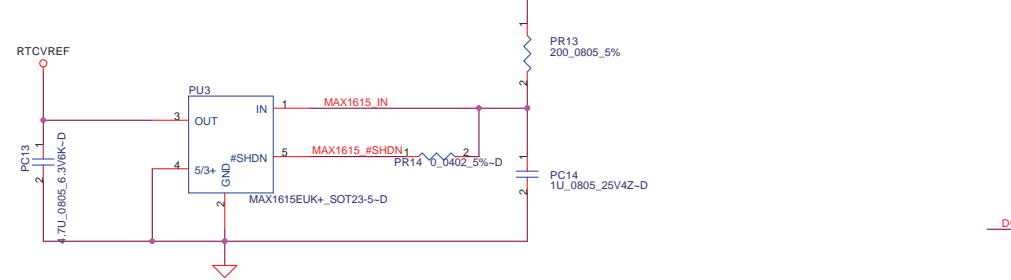
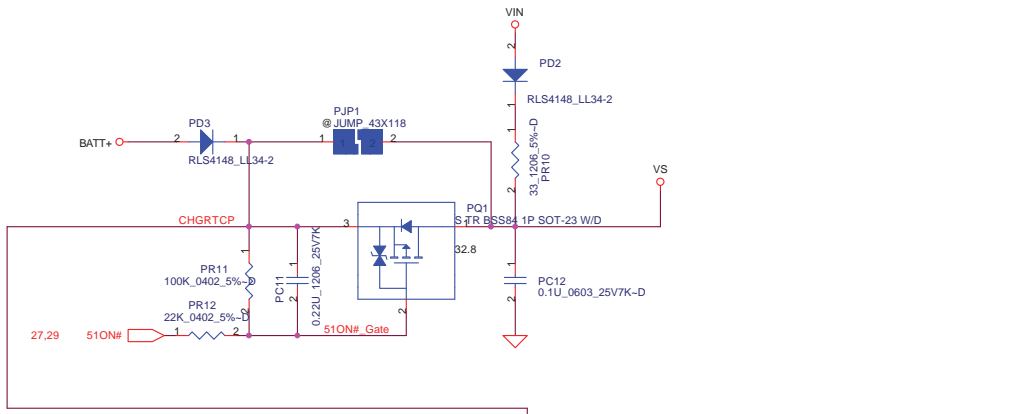
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Date: Thursday, February 19, 2009				Sheet	31 of 42

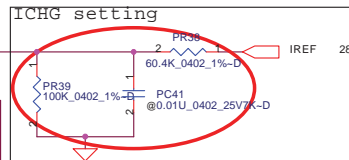
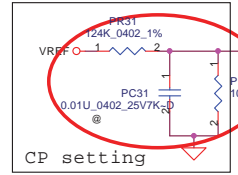
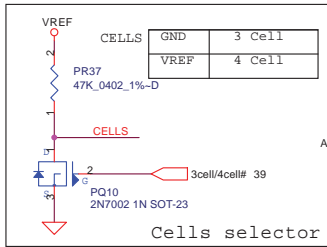


	Max.	typ.	Min.
L-->H	18.234	17.841	17.449
H-->L	17.597	17.210	16.813



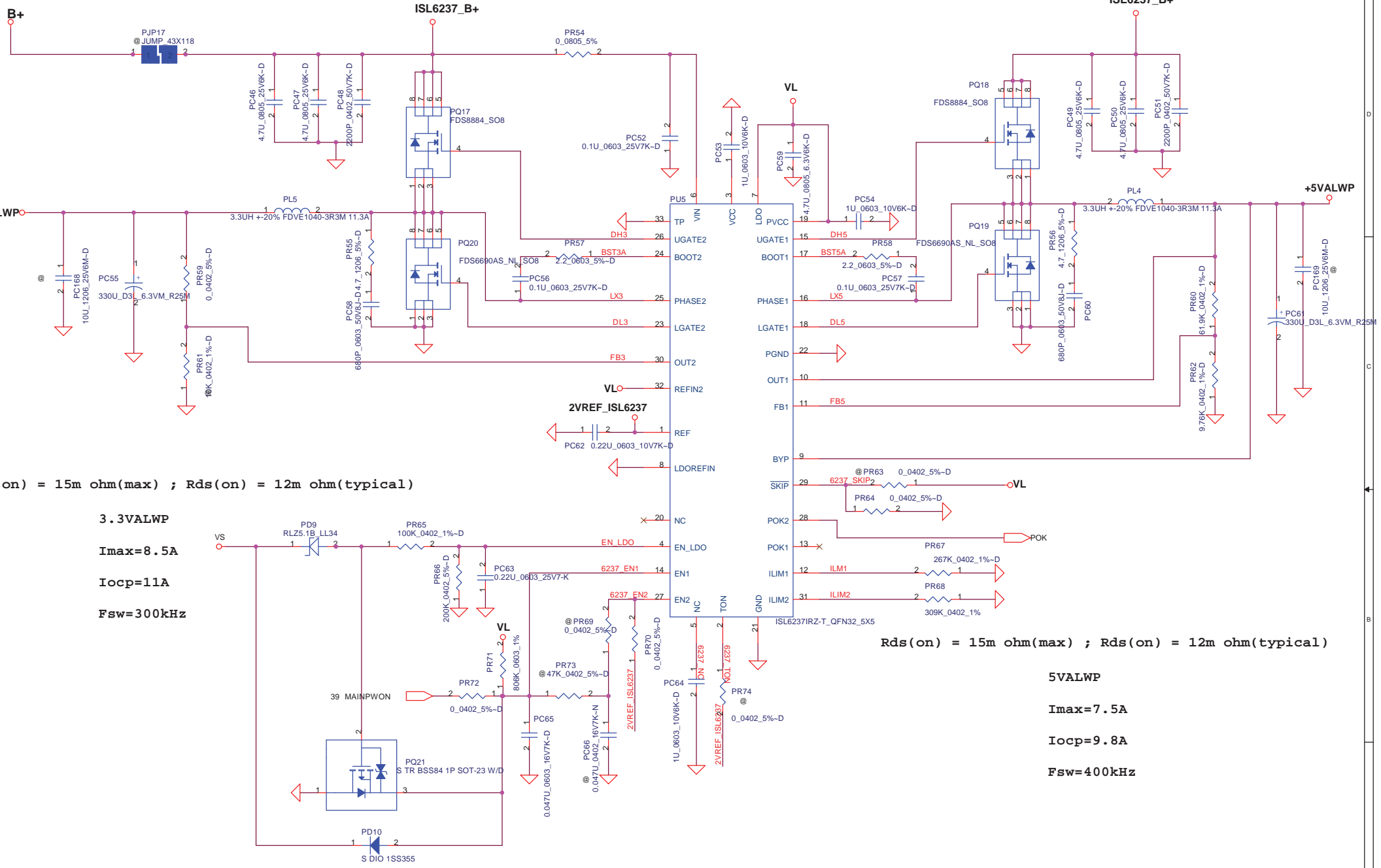
Security Classification	Compal Secret Data		Title	
Issued Date	2006/10/1	Deciphered Date	2007/5/01	DCIN / Precharge
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90W adapter
 $I_{charge} = (V_{srset}/V_{vdac}) * (0.1/PR222) = 3.3A$
 $I_{adapter} = (V_{vacset}/V_{vdac}) * (0.1/PR17) = 3.34A$
 Input OVP : 22.3V
 Input UVP : 16.98V
 Fsw : 300KHz



IREF	Current
0V	0A
3.3V	3A

CHGVADJ	Battery Voltage/per cell
0V	3V
3.3V	4.2V



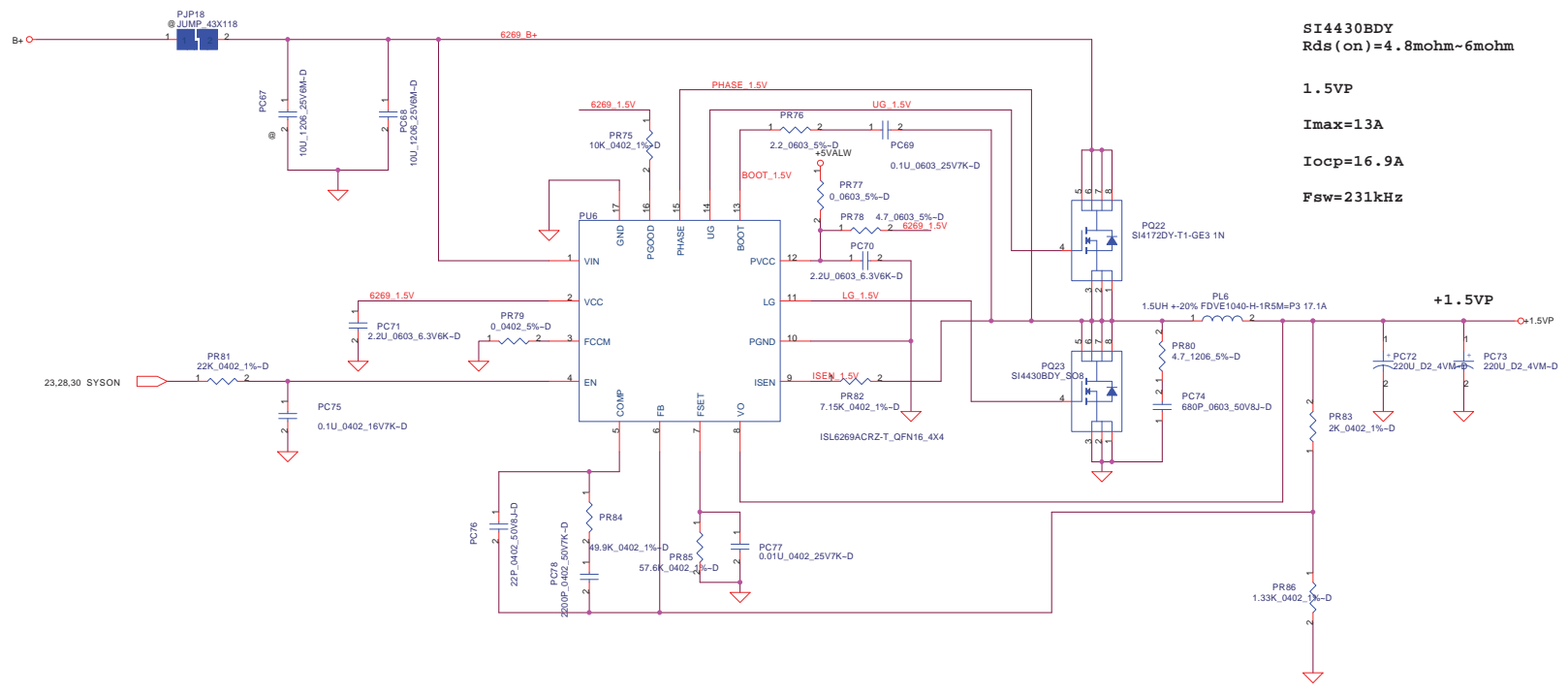
$R_{ds(on)} = 15\text{m ohm(max)} ; R_{ds(on)} = 12\text{m ohm(typical)}$

3.3VALWP
 $I_{max} = 8.5\text{A}$
 $I_{ocp} = 11\text{A}$
 $f_{sw} = 300\text{kHz}$

$R_{ds(on)} = 15\text{m ohm(max)} ; R_{ds(on)} = 12\text{m ohm(typical)}$

5VALWP
 $I_{max} = 7.5\text{A}$
 $I_{ocp} = 9.8\text{A}$
 $f_{sw} = 400\text{kHz}$

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SI4430BDY
R_{ds(on)} = 4.8mohm-6mohm

1.5VP

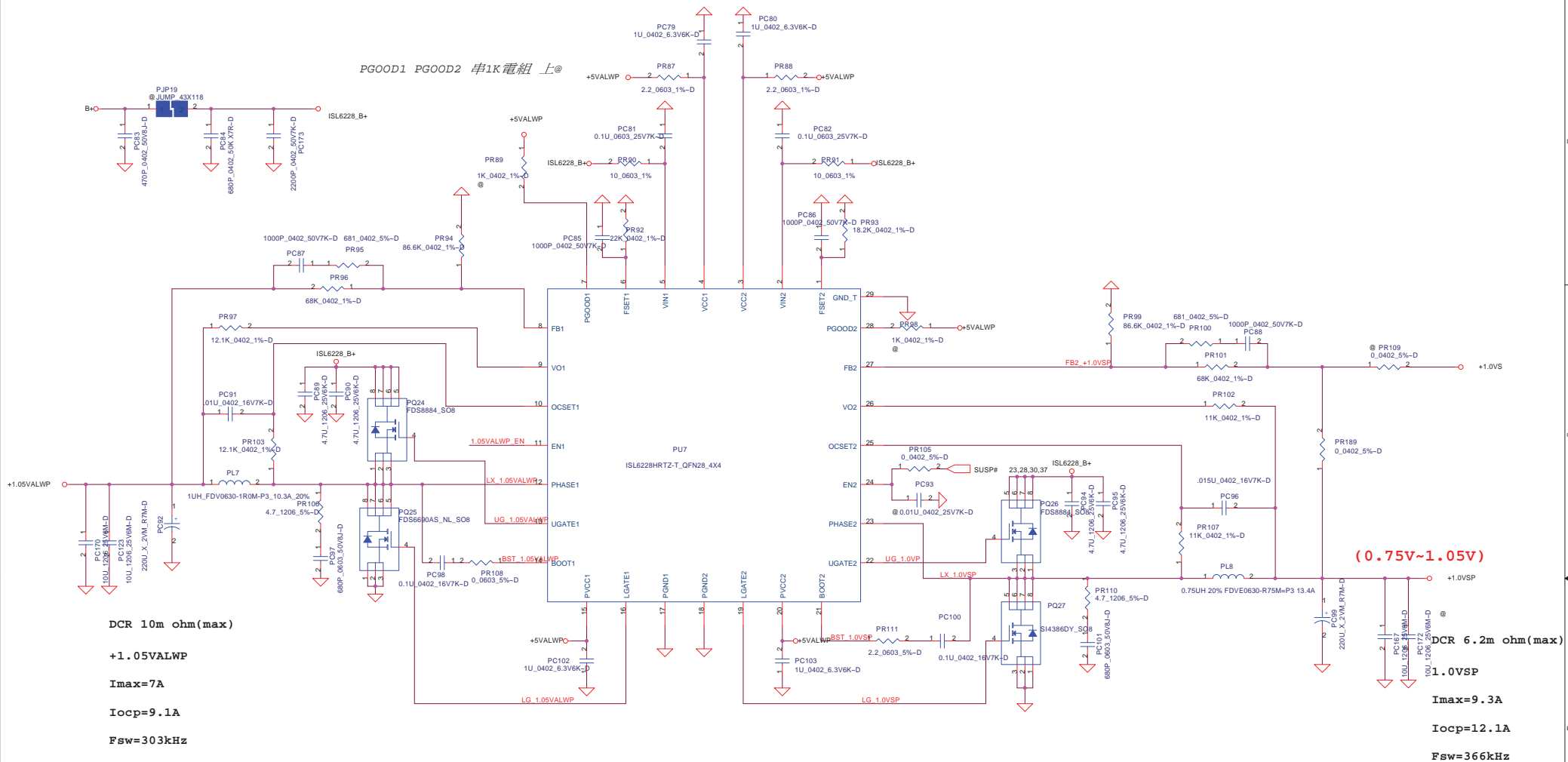
I_{max} = 13A

I_{ocp} = 16.9A

F_{sw} = 231kHz

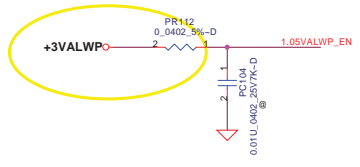
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Title	1.5VP			
Size	Document Number	KCM00		Rev
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PGOOD1 PGOOD2 串1K電組 上@

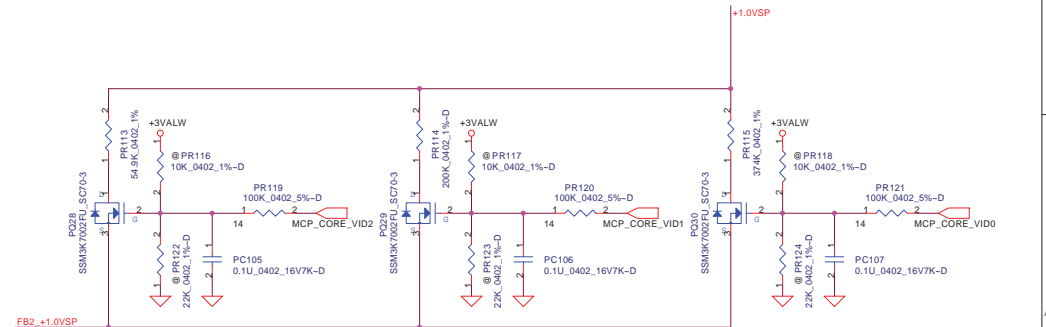


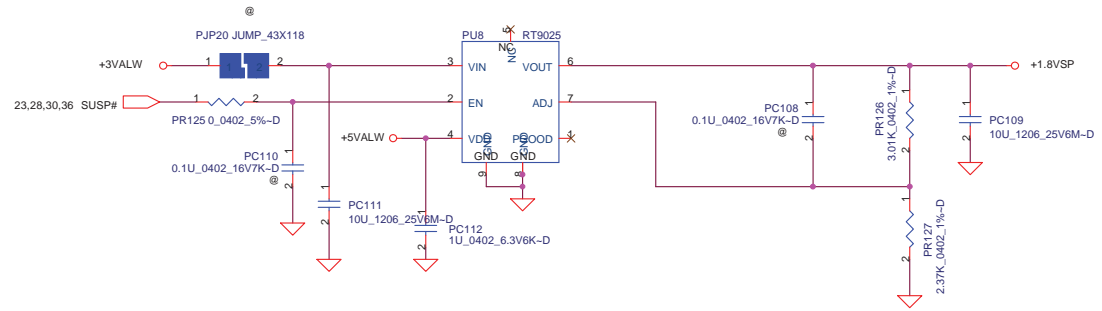
DCR 10m ohm(max)
 +1.05VALWP
 I_{max}=7A
 I_{ocp}=9.1A
 F_{sw}=303kHz

DCR 6.2m ohm(max)
 +1.0VSP
 I_{max}=9.3A
 I_{ocp}=12.1A
 F_{sw}=366kHz

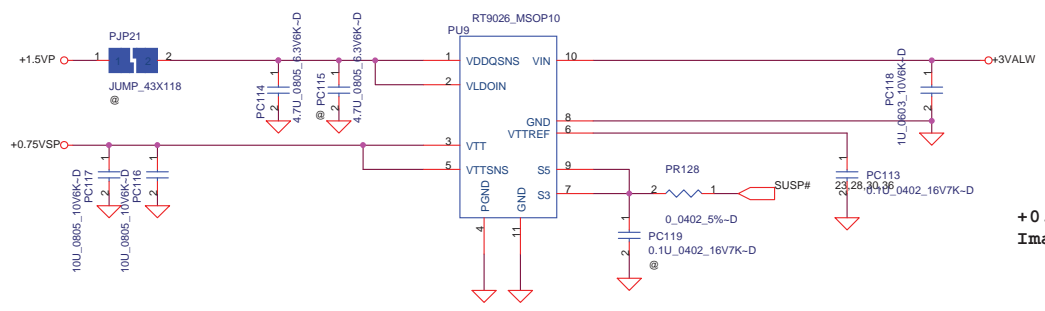


VID2	VID1	VID0	voltage
L	L	L	1.05
L	L	H	0.98
L	H	L	0.90
L	H	H	0.87
H	L	L	0.80
H	L	H	0.79
H	H	L	0.77
H	H	H	0.75



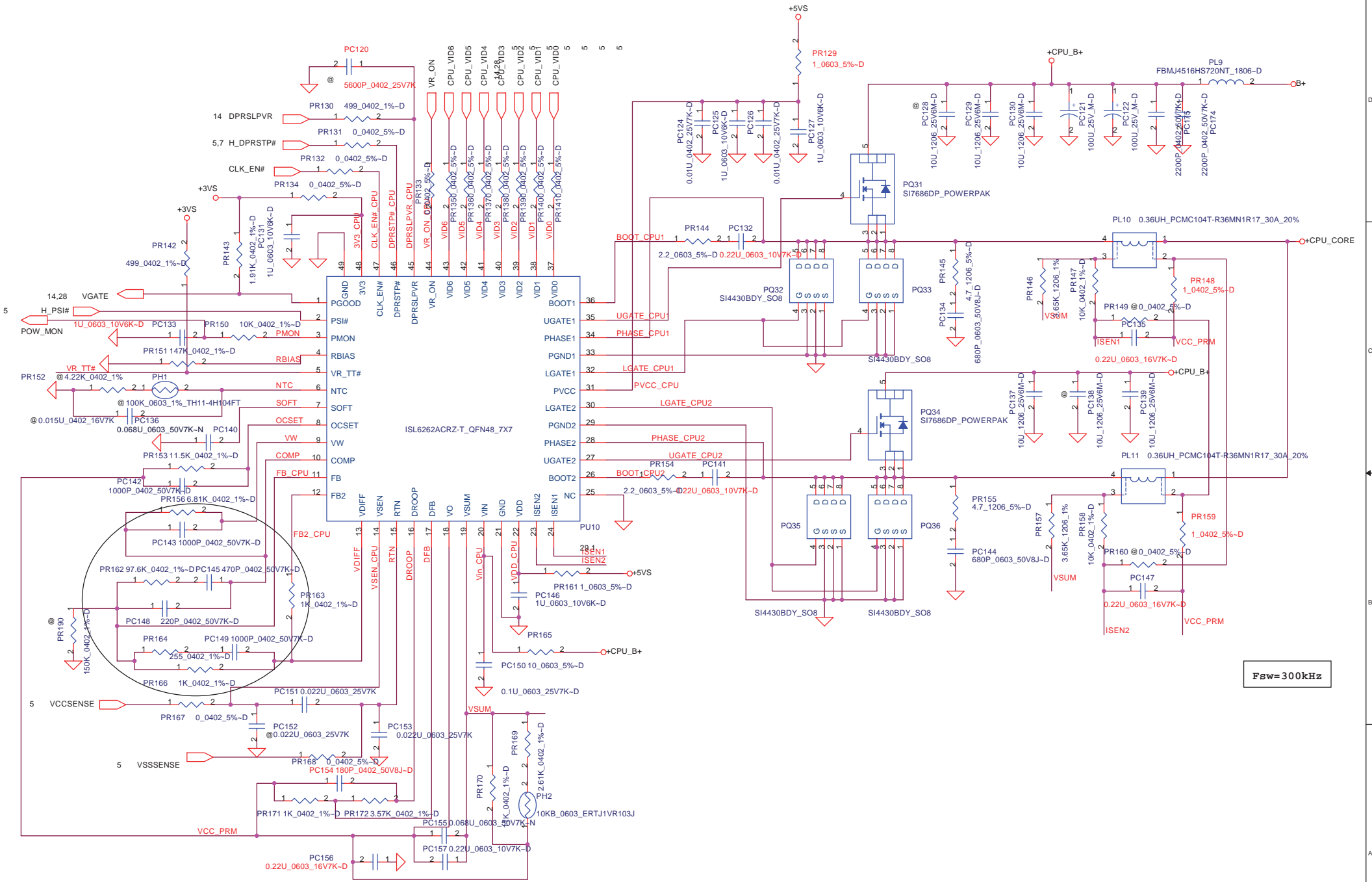


+1.8VSP
Imax=0.3A



+0.75VSP
Imax=1.5A

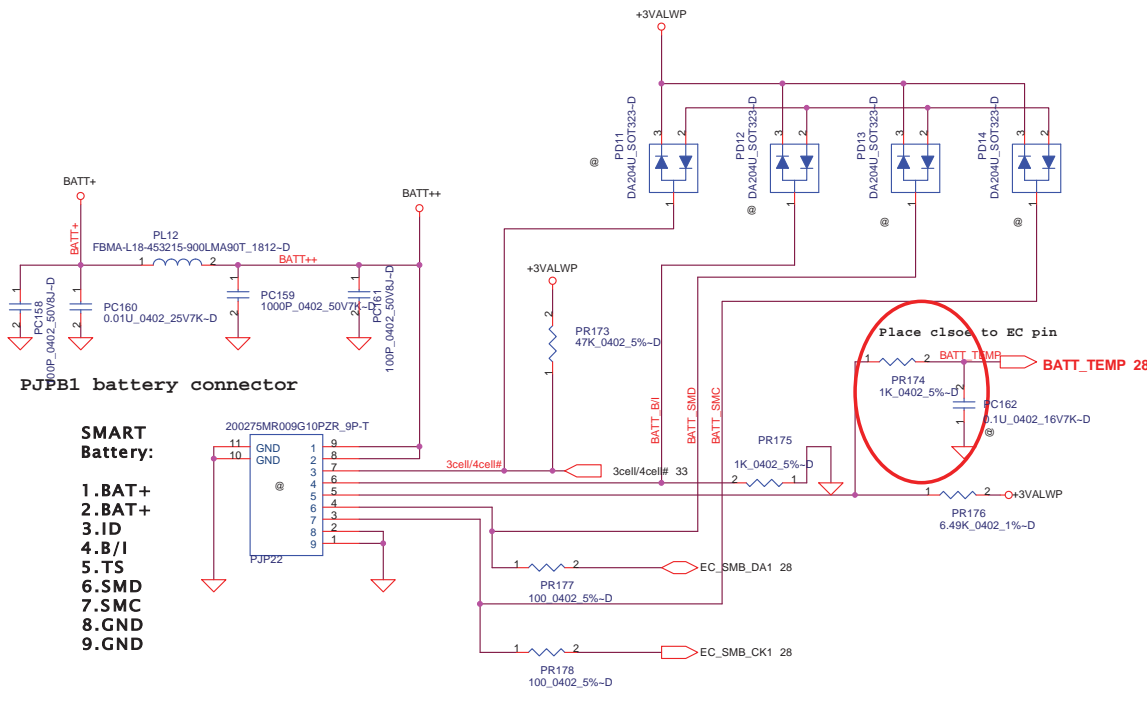
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F_{sw} = 300kHz

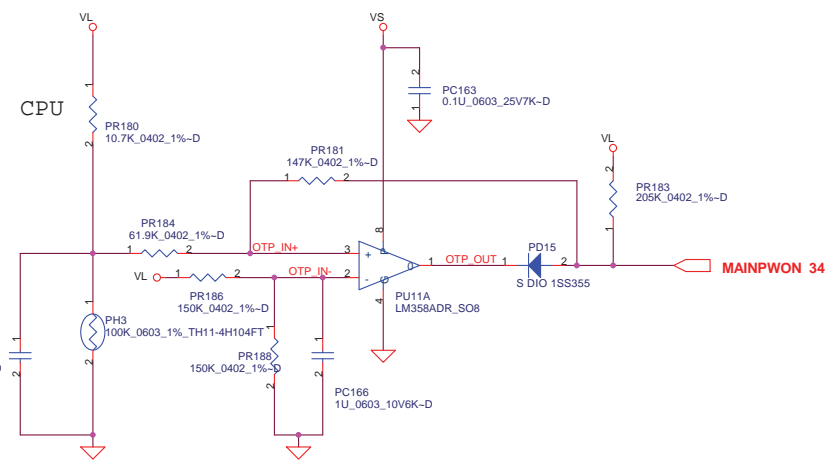
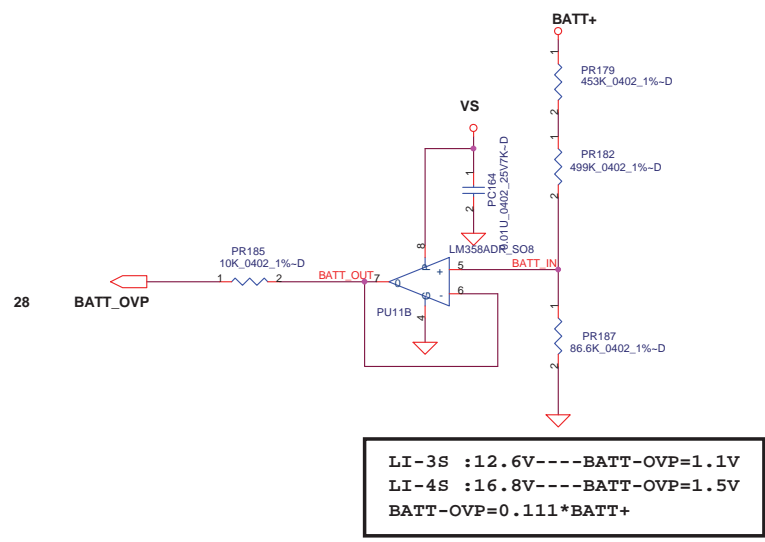
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Compal Electronics, Inc.		
+CPU CORE		
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Battery Connect/OTP

CPU
PH1 under CPU bottom side :
 CPU thermal protection at 90 +-3 degree C
 Recovery at 50 +-3 degree C

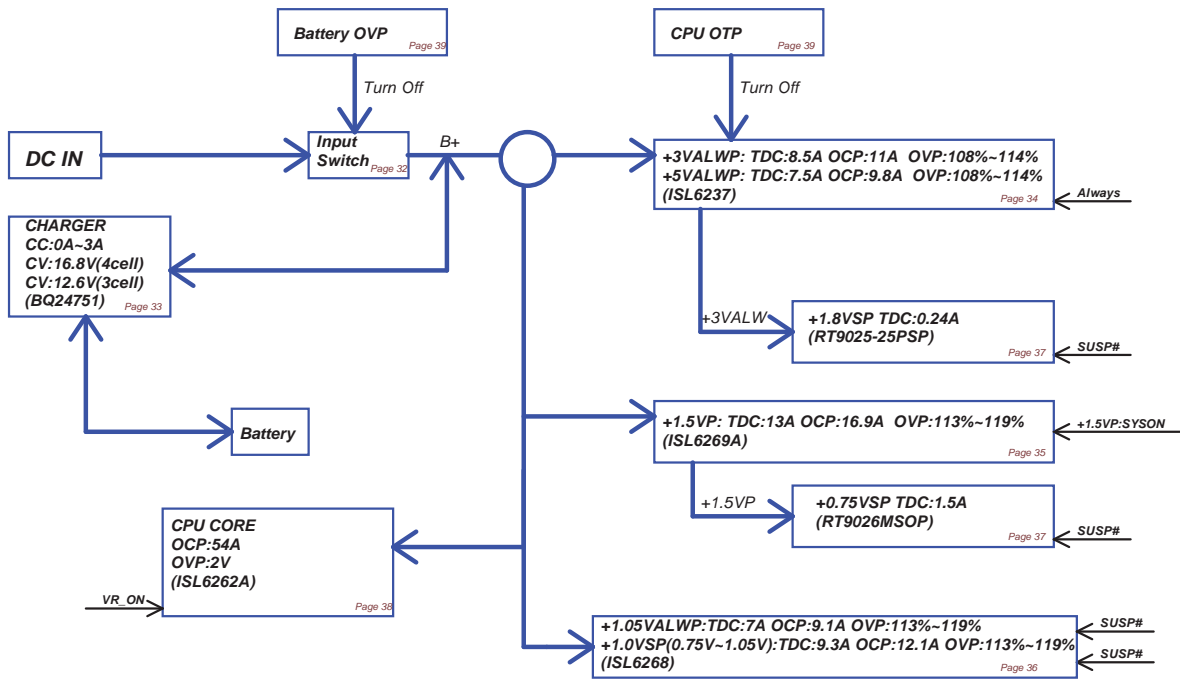


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				BATTERY CONN	
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	p37	+0.75VSP/1.8VSP	08/10/15	compal	source shortage	pu9	
2	p33	charger	08/10/15	compal	design change	PQ6 PQ8	
3	p32	DCIN / Precharge	08/10/15	compal	meet PSL	PQ2	
4	p33	charger	08/10/15	compal	meet PSL	PQ16	
5	p32	DCIN / Precharge	08/10/15	compal	meet PSL	PQ1	
6	p33	charger	08/10/15	compal	meet PSL	PQ12	
7	p34	+3VALWP/+5VALWP	08/10/15	compal	meet PSL	PQ21	
8	p33	charger	08/10/15	compal	meet PSL	PR22 PR29	
9	p37	+0.75VSP/1.8VSP	08/10/15	compal	adjust 1.8V output voltage	PR127 PR124	
10	p33	charger	08/10/15	compal	adjust charge current to 3.1A	PR38	
11	p33	charger	08/10/15	compal	adjust CP set for ICPP function	PR38	
12	p34	+3VALWP/+5VALWP	08/10/15	compal	meet choke component current limit	PL4 PL5	
13	p32	DCIN / Precharge	08/10/15	compal	meet PSL	PL1	
14	p38	CPU_CORE	08/10/15	compal	meet PSL	PL9	
15	p39	BATTERY CONN	08/10/15	compal	meet PSL	PL12	
16	p33	charger	08/10/22	compal	design change	PQ6 PQ8	
17	p35	+1.5VSP	08/10/22	compal	reduce L/S MOS Vds	PQ22	
18	p36	+1.05VALWP/1.0VP	08/10/22	compal	Add remote sense function	PR189	
19	p36	+1.05VALWP/1.0VP	08/10/22	compal	adjust output voltage	pr94	
20	p36	+1.05VALWP/1.0VP	08/10/22	compal	design change	PL8	
21	p35	+1.5VSP	08/10/22	compal	design change	PL6	
22	p33	charger	08/10/22	compal	EMI request	PL13	
23	ALL	every power	08/10/22	compal	reduce output ripple	PC123 PC167 PC168 PC169 PC170	
24	ALL	every power	08/10/22	compal	sunbber for EMI request	PR30 PR106 PR55 PR56 PR80 PR110 PR105 PR155	
25	ALL	every power	08/10/22	compal	sunbber for EMI request	PC33 PC58 PC60 PC74 PC97 PC101 PC134 PC144	
26	P34 P35	every power	08/10/22	compal	increase boost resistor value form 0 ohm to 2.2 ohm for EMI request	PR57 PR58 Pr76	
27	p39	BATTERY CONN	08/12/03	compal	adjust OTP set	PR183	
28	p33	charger	08/12/03	compal	DFX request	PQ10 PQ11 PQ13 PQ14 PQ15	
29	p36	+1.05VALWP/1.0VP	08/12/03	compal	adjust +1.0VSP OCP set	PR102 PR107	
30	p36	+1.05VALWP/1.0VP	08/12/03	compal	adjust +1.0VSP output voltage	PR99	
31	p35	+1.5VSP	08/12/12	compal	design change(already trail run in PT phase)	PQ22	
32	p39	BATTERY CONN	08/12/12	compal	adjust OTP set	PR183	
33	p33	charger	08/12/31	compal	reduce AC-IN inrush current	PR24 PR25	
34	p36	+1.05VALWP/1.0VP	08/12/31	compal	WWAN issue	PC173 PC174 PC175	
34	p34	+3VALWP/+5VALWP	08/12/31	compal	adjust +5VALWP voltage	PR62 change frome 10k to 9.62k	

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Braxton Power block



Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	19	P19-DDR3_SO-DIMM SLOT	2008/09/22	nVidia	can't use SO-DIMM	change SO-DIMM SA0 to pull high & SA1 to pull down	0.2
2	20	P20-LCD/SATA HDD	2008/09/25	Compal	can't read EDID for Panel	change JLVDS1 Pin 37 from +LCDVDD TO +3VS	0.2
3	21	P21-HDMI/Display Port	2008/10/07	Compal	Change DP122 to DP122A	change R440 from 4.64K to 5.11K and R438 from 5.11K to 6.49K	0.2
4	12	P12-MCP79(6/10)_PCI/LPC	2008/10/13	Compal	can't select on board SPD data	ADD R191,R192,R193 TO SELECT ON BOARD MEMORY VENDOR	0.2
5	28	P28-EC_KB926/BIOS/Reed SW	2008/10/20	Compal		Change EC_SMB_Da1 and EC_SMB_CK1 from +5VALW to +3VALW	0.2
6	18	P18-1GB/2GB_DDR3_On Board	2008/12/04	nVidia	On board Ram unstable	Add 0.1uF cap between Termination Resistor and +0.75VS	0.4
7	14	P14-MCP79(8/10)_HDA/MISC	2009/02/03	Dell	saving power consumption	change +3VALW to +3VS on MEM_SMBCLK & MEM_SMBDATA	1.0
8	24	P24-Mini Card_WLAN/WWAN	2009/02/04	Dell		reserve SMBus from MCP79	1.0
9							
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				Custom	1.0
				Date:	Thursday, February 19, 2009
				Sheet	42 of 42