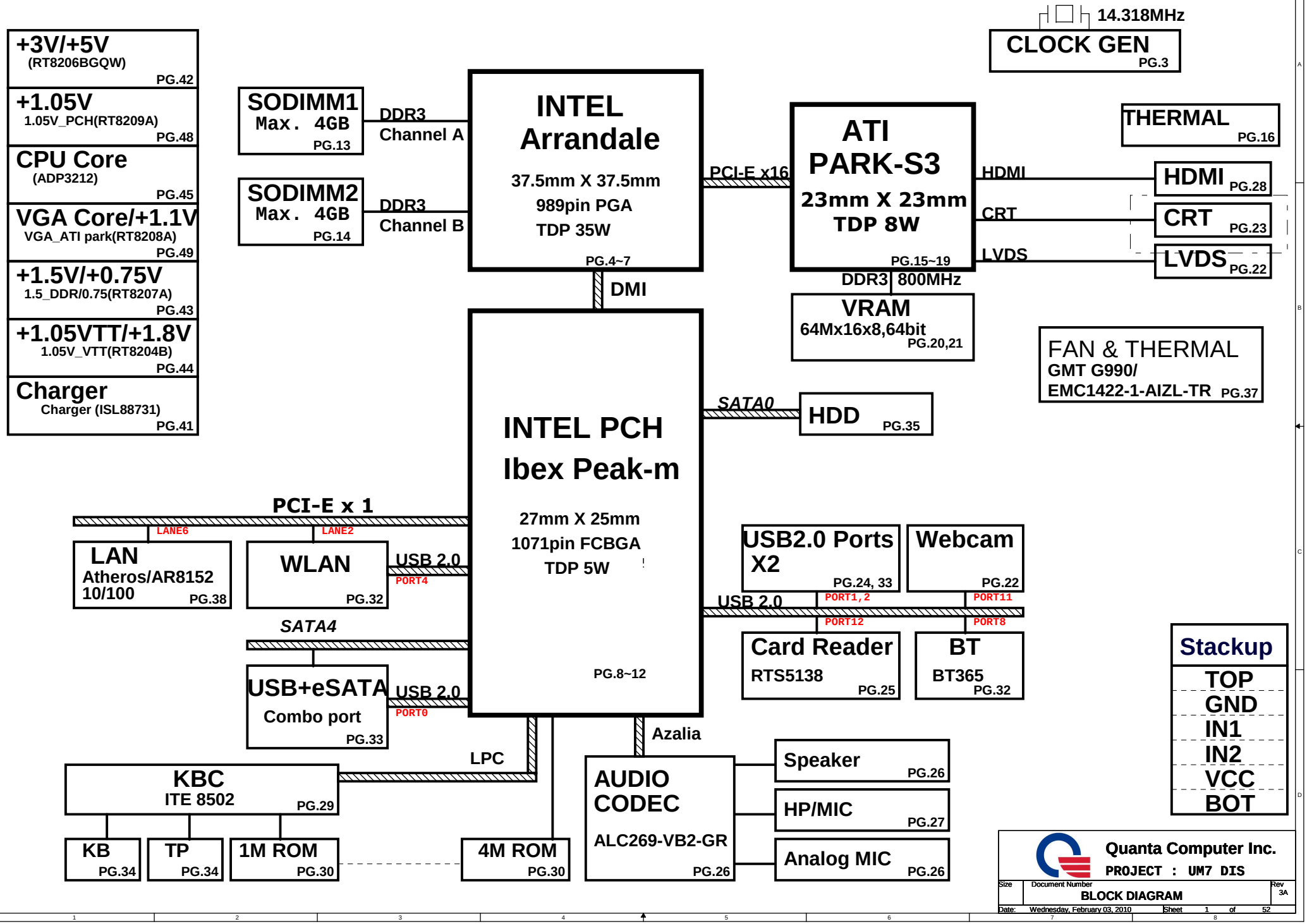
UM7B DISCRETE SYSTEM DIAGRAM



Quanta Computer Inc.
PROJECT : UM7 DIS

Size	Document Number	Rev
	BLOCK DIAGRAM	3A
Date: Wednesday, February 03, 2010	Sheet 1 of 52	

Table of Contents

Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	23,42,43,44,45,46,49,50	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	09,12,30,31	RTC		S0~S5
					S0~S5
+5V_ALW	+5V	37,43,44,47,48	LARGE POWER	ALW_ON	S0~S5
+3.3V_ALW	+3.3V	30,31,37,42,43,45,47,48	8051 POWER	3.3V_ALW_ON	S0~S5
+5V_SUS	+5V	12,25,34,37,43,44,45,46,47,49,50	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	03,08,09,10,11,12,23,35,37,39,41,46,47,50	SLP_S5# CTRLD POWER	SUS_ON	
+1.5V_SUS	+1.5V	04,06,14,15,44,47	SODIMM POWER	SUS_ON	
+0.75V_DDR_VTT	+0.75V	14,15,44	SODIMM POWER	RUN_ON	
+5V_RUN	+5V	08,12,23,24,27,28,29,35,36,3738,47	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,4,8,9,10,11,12,14,15,23,24,26,27,28,29,30 ,31,33,34,36,37,38,39,41,47	SLP_S3# CTRLD POWER	RUN_ON	
+1.8V_RUN	+1.8V	6,12,45	SDVO POWER	RUN_ON	
+1.05V_VTT	+1.1V	4,6,11,12,45,46	CPU POWER	RUN_ON	
+1.5V_RUN	+1.5V	12,33,47	PCH/Min Card	RUN_ON	
+1.05V_PCH	+1.05V	3,8,9,10,12,49	PCH POWER	RUN_ON	
+VCC_CORE	+0.7V~+1.77V	6,46	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	23	LCD Power	LCDVCC_TST_EN & ENVDD	

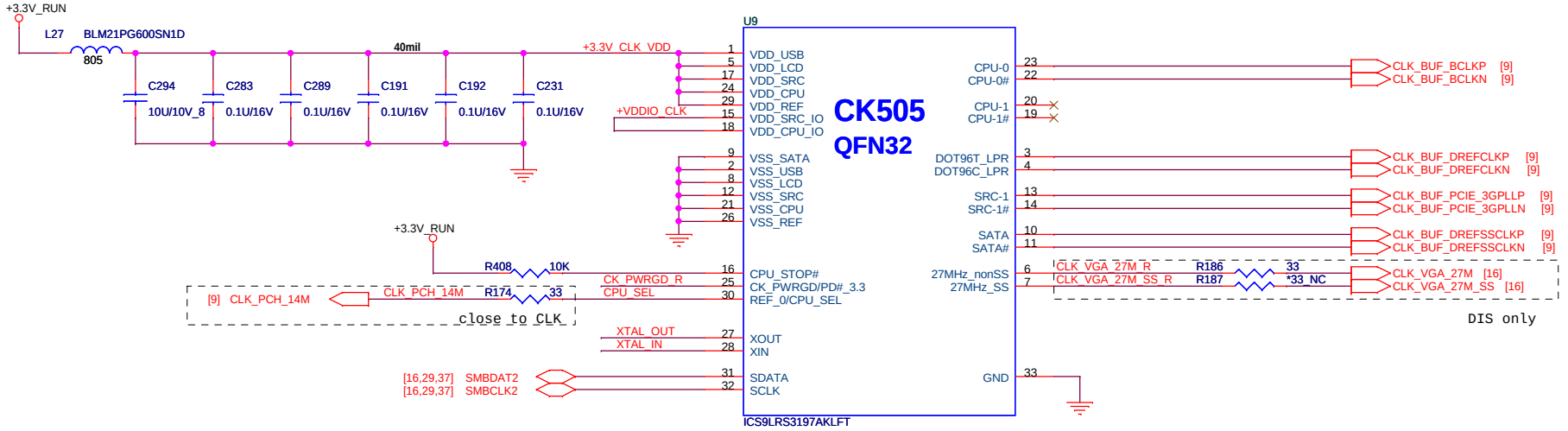
GND PLANE	PAGE	DESCRIPTION
GND	ALL	

Quanta Computer Inc.

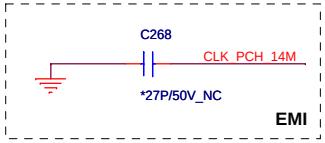
PROJECT : UM7 DIS

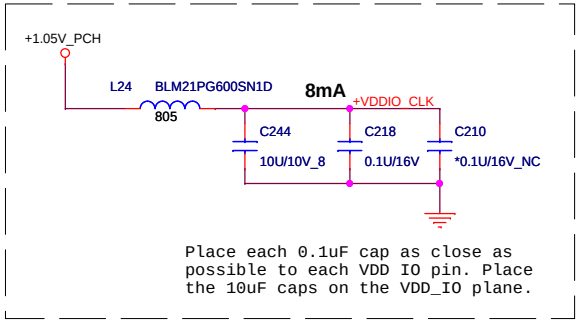
Size	Document Number	Rev
	BLOCK DIAGRAM	3A

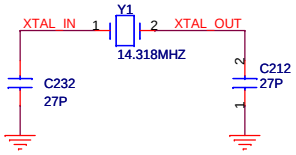
Date: Wednesday, February 03, 2010 Sheet 2 of 52

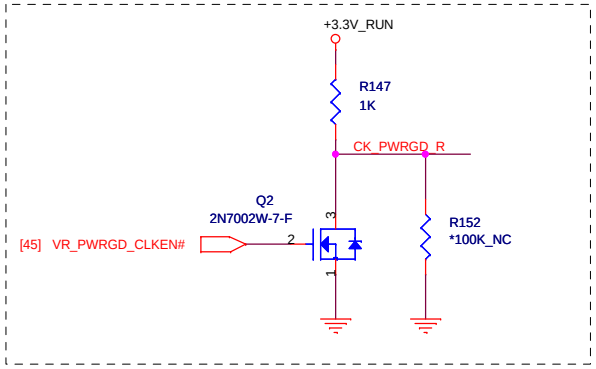


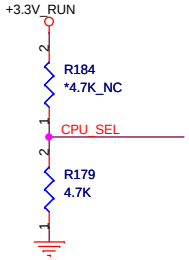
AL003197000IC OTHER(32P)ICS9LRS3197AKLFT(QFN)
~~AL8SP585000IC OTHER(32P)SLG8SP585VTR(QFN)~~
AL8SP590000IC OTHER(32P)SLG8SP590VTR(QFN)











PIN 30	CPU_0	CPU_1
0(default)	133MHz	133MHz
1(0.7V-1.5V)	100MHz	100MHz

Quanta Computer Inc.
PROJECT : UM7 DIS

Size	Document Number	Rev
	Clock Generator	3A
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change PN

U16A

DMI

Intel(R) FDI

PCI EXPRESS -- GRAPHICS

IC,AUB_CFD_rPGA,R1P0

U16B

MISC

THERMAL

CLOCKS

DDR3 MISC

PWR MANAGEMENT

JTAG & BPM

IC,AUB_CFD_rPGA,R1P0

PAD on trace

For ITP CLk

DIS connect GND

PREQ TP not too long

Discrete Only

FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (Check list 1.0).

CPU THERMTRIP

Q24 *2N7002W-7-F_NC

Q23 *MMST3904-7-F_NC

Use a voltage divider with VDDQ (1.5 V) rail ON in S3) and resistor combination of 1.5K ±1% (to VDDQ)/750±1% (to GND) to convert to processor VTT level.

JTAG

Intel Suggest to reserve 0 ohm below for CPU AP29 and AR29 pins.

Quanta Computer Inc.

PROJECT : UM7 DIS

Size	Document Number	Rev
	PROCESSER 1/4(HOST&PEX)	3A

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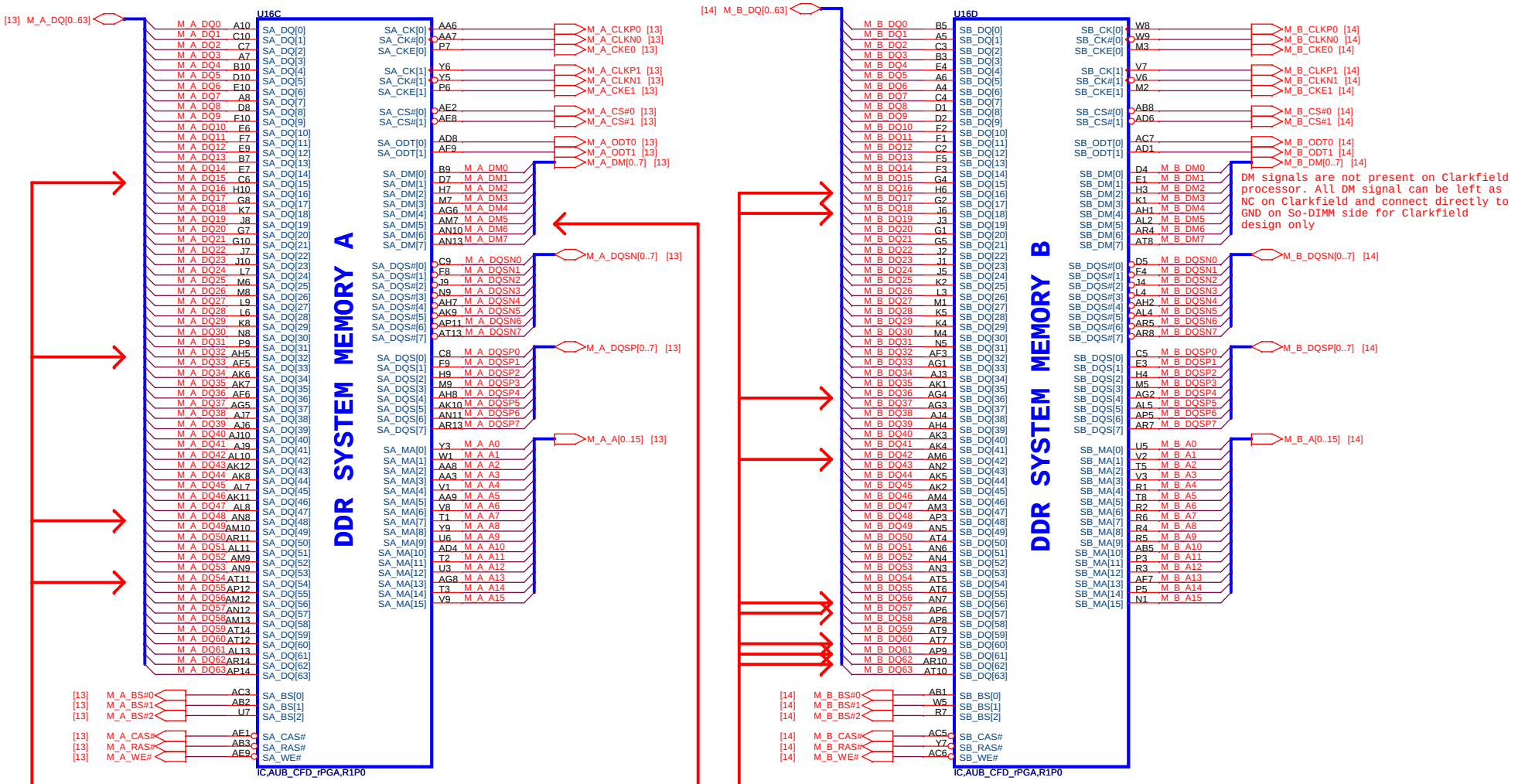
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

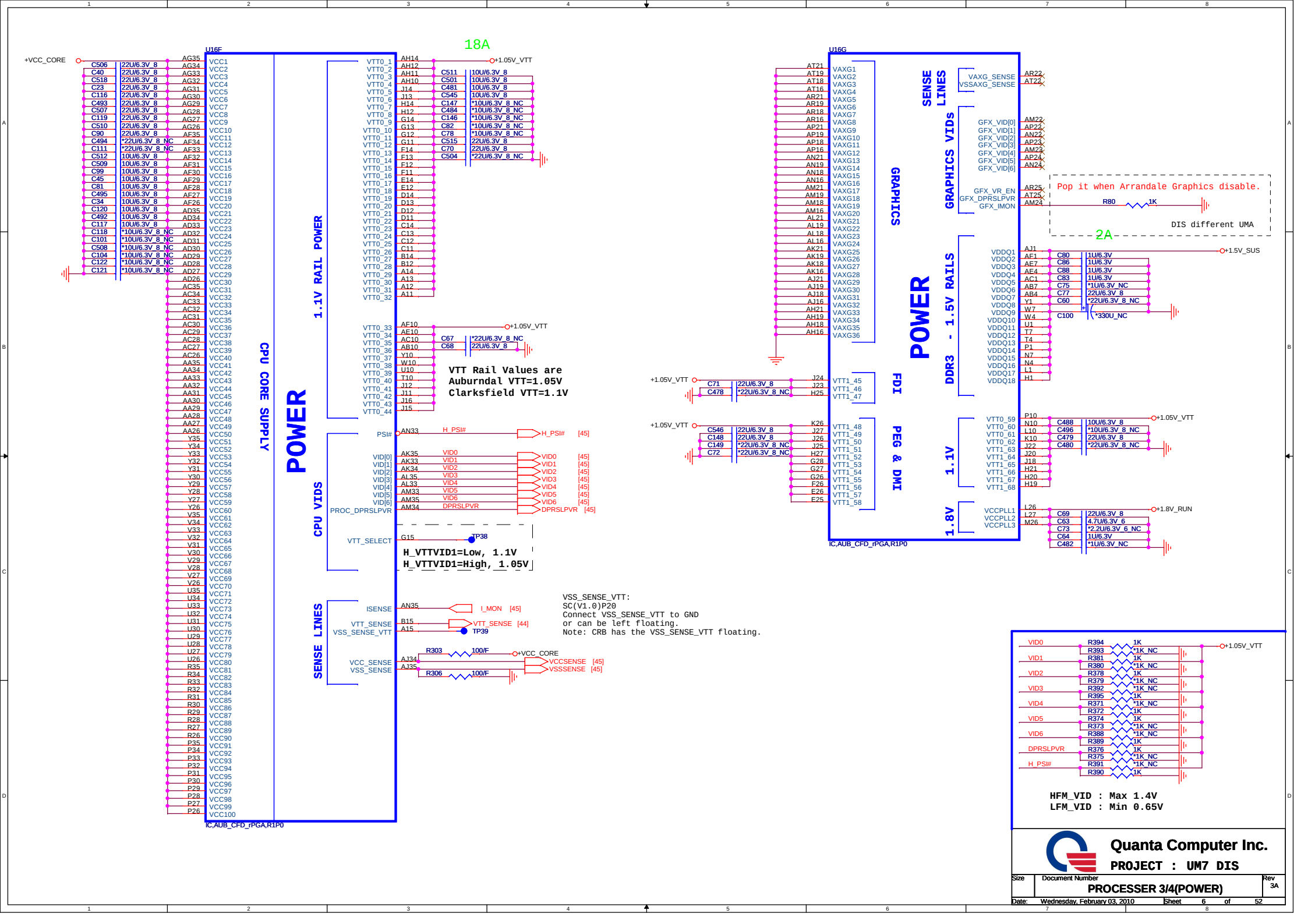


Quanta Computer Inc.

PROJECT : UM7 DIS

Size	Document Number	Rev
	PROCESSER 2/4(DDR)	3A

Date: Wednesday, February 03, 2010 Sheet 5 of 52


18A
U16F
POWER
CPU CORE SUPPLY
1.1V RAIL POWER
CPU VIDS
SENSE LINES
+VCC_CORE
+1.05V_VTT
VTT Rail Values are
Auburndal VTT=1.05V
Clarksfield VTT=1.1V
H_VTTVID1=Low, 1.1V
H_VTTVID1=High, 1.05V
VSS_SENSE_VTT:
SC(V1.0)P20
Connect VSS_SENSE_VTT to GND
or can be left floating.
Note: CRB has the VSS_SENSE_VTT floating.
IC,AUB_CFD_rPGA,R1P0
U16G
POWER
GRAPHICS
SENSE LINES
GRAPHICS VIDs
DDR3 - 1.5V RAILS
FDI
PEG & DMI
1.1V
1.8V
Pop it when Arrandale Graphics disable.
DIS different UMA
2A
+1.5V_SUS
+1.8V_RUN
HFM_VID : Max 1.4V
LFM_VID : Min 0.65V
Quanta Computer Inc.
PROJECT : UM7 DIS
PROCESSER 3/4(POWER)
Rev 3A
Wednesday, February 03, 2010
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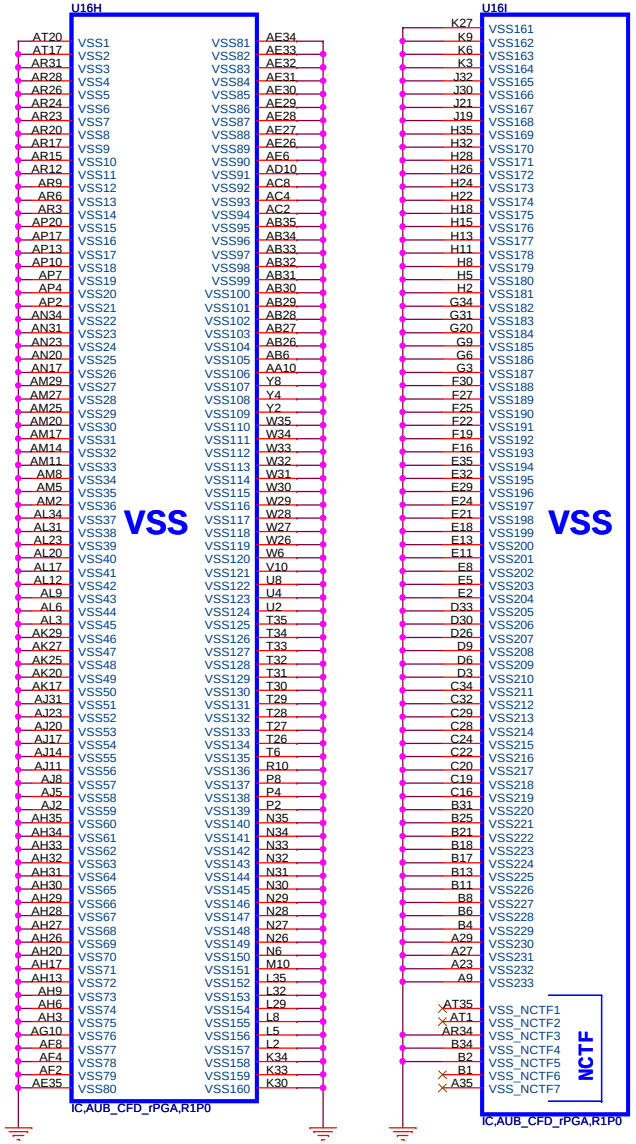
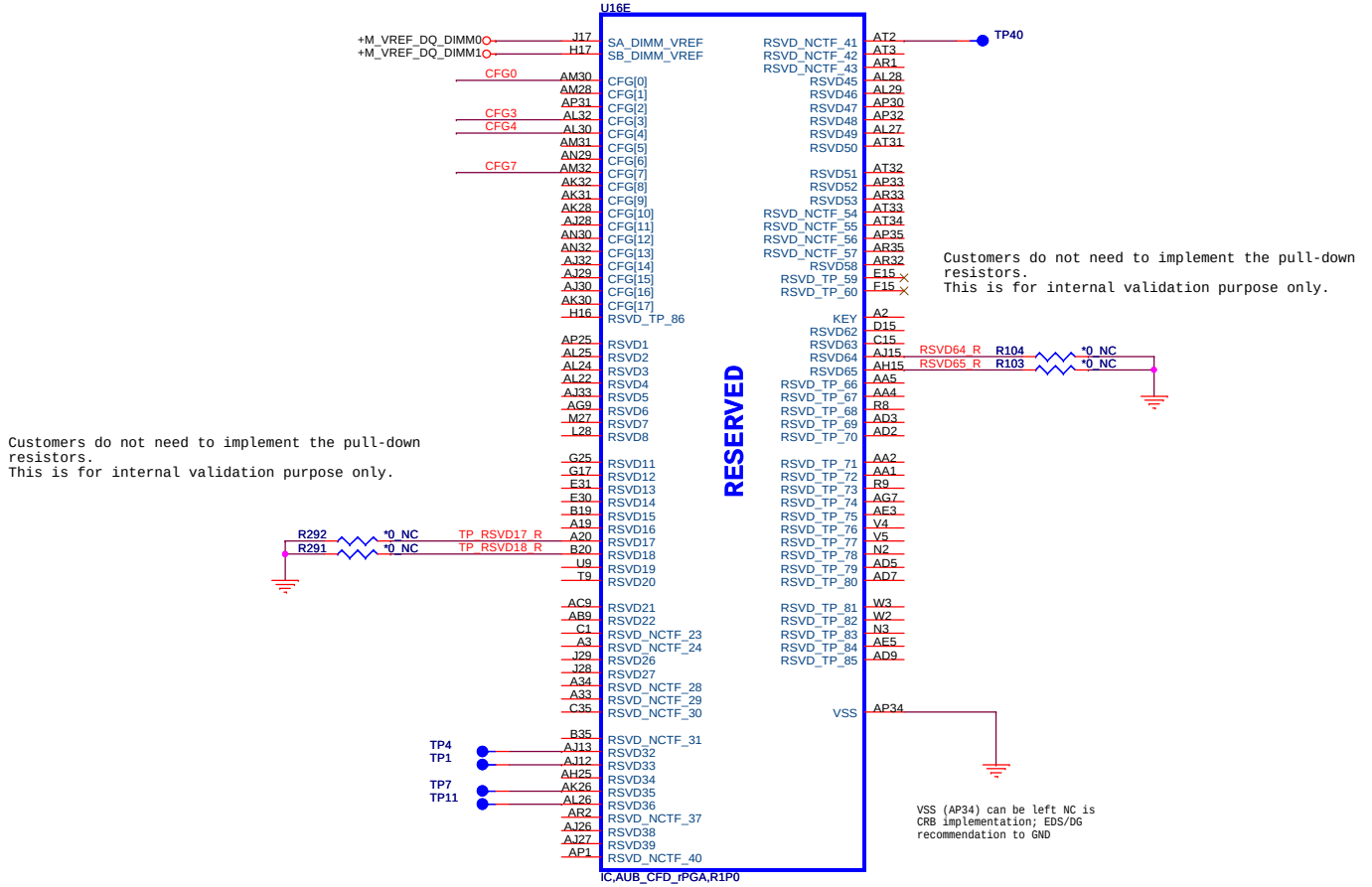
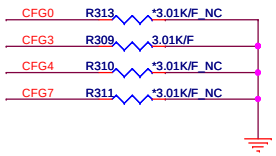
Arrandale PROCESSOR (GND)



Arrandale PROCESSOR(RESERVED, CFG)





The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

Quanta Computer Inc.
PROJECT : UM7 DIS

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	PROCESSER 4/4 (GND)	3A

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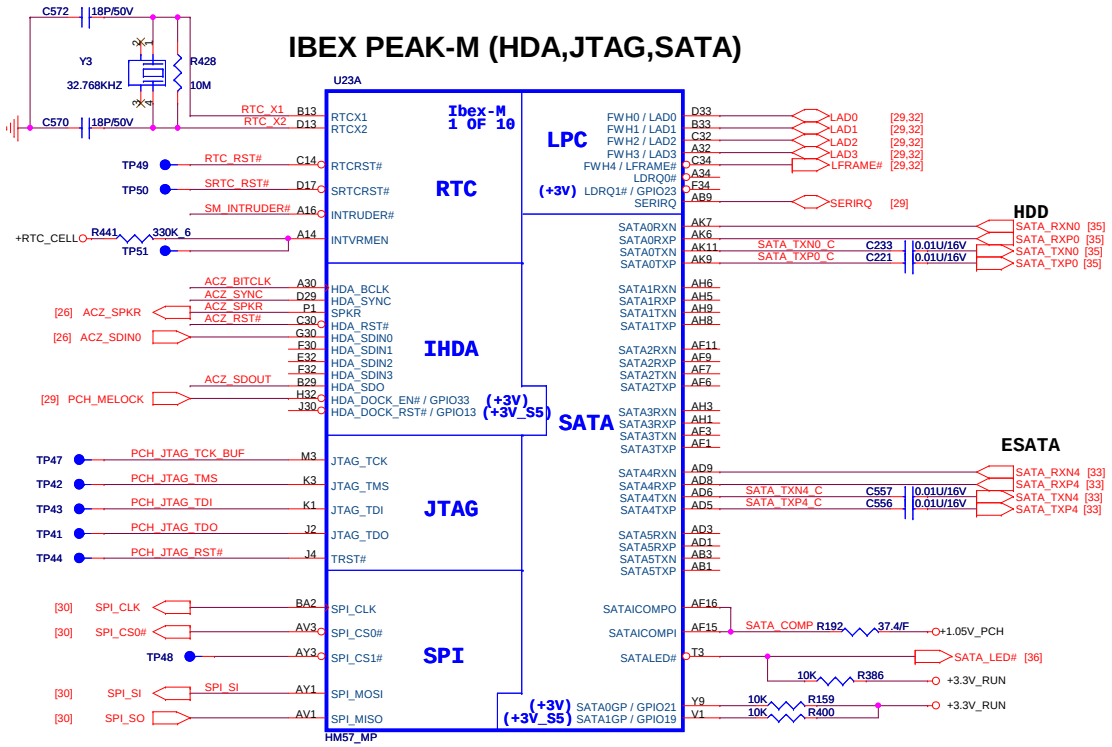
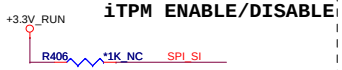
INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

IBEX PEAK-M (HDA,JTAG,SATA)

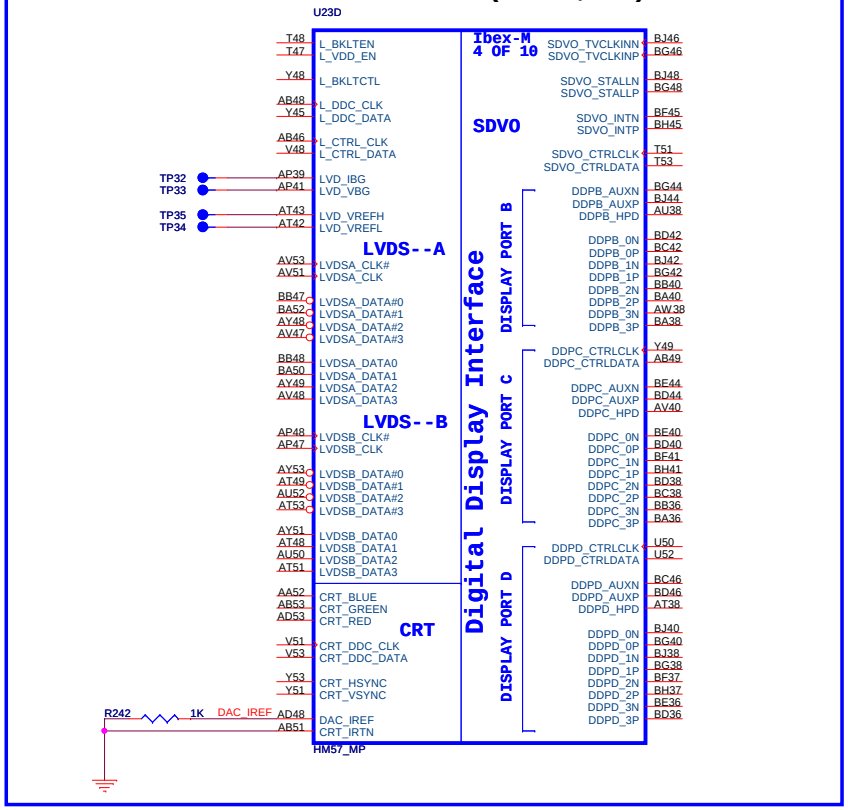


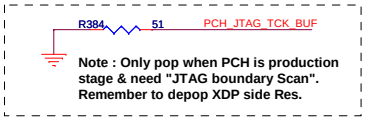
iTPM ENABLE/DISABLE



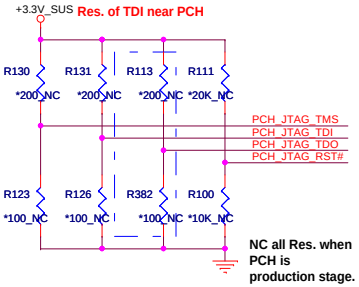
TPM Function	
Enable	Mount
Disable	NC (Default)

UMA CRT,LVDS&HDMI signals
IBEX PEAK-M (LVDS,DDI)





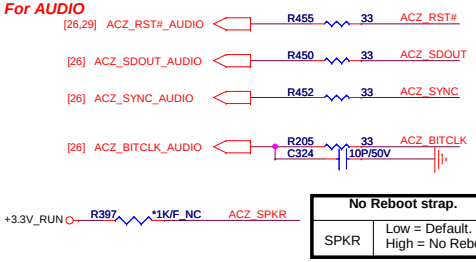
Note : Only pop when PCH is production stage & need "JTAG boundary Scan". Remember to depop XDP side Res.



NC all Res. when PCH is production stage.

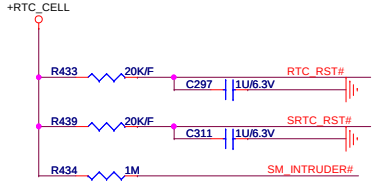
Res. of TDO
PCH ES1 stage : NC
PCH ES2 stage : pop

For AUDIO



No Reboot strap.	
SPKR	Low = Default. High = No Reboot

RTC 1mA



Quanta Computer Inc.
PROJECT : UM7 DIS

Size	Document Number	Rev
	PCH 1/5 (SATA,HDA,LPC)	3A

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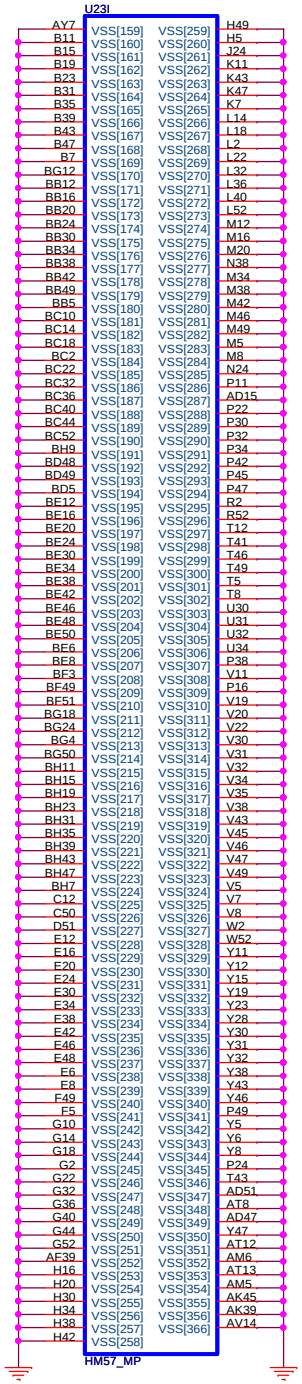
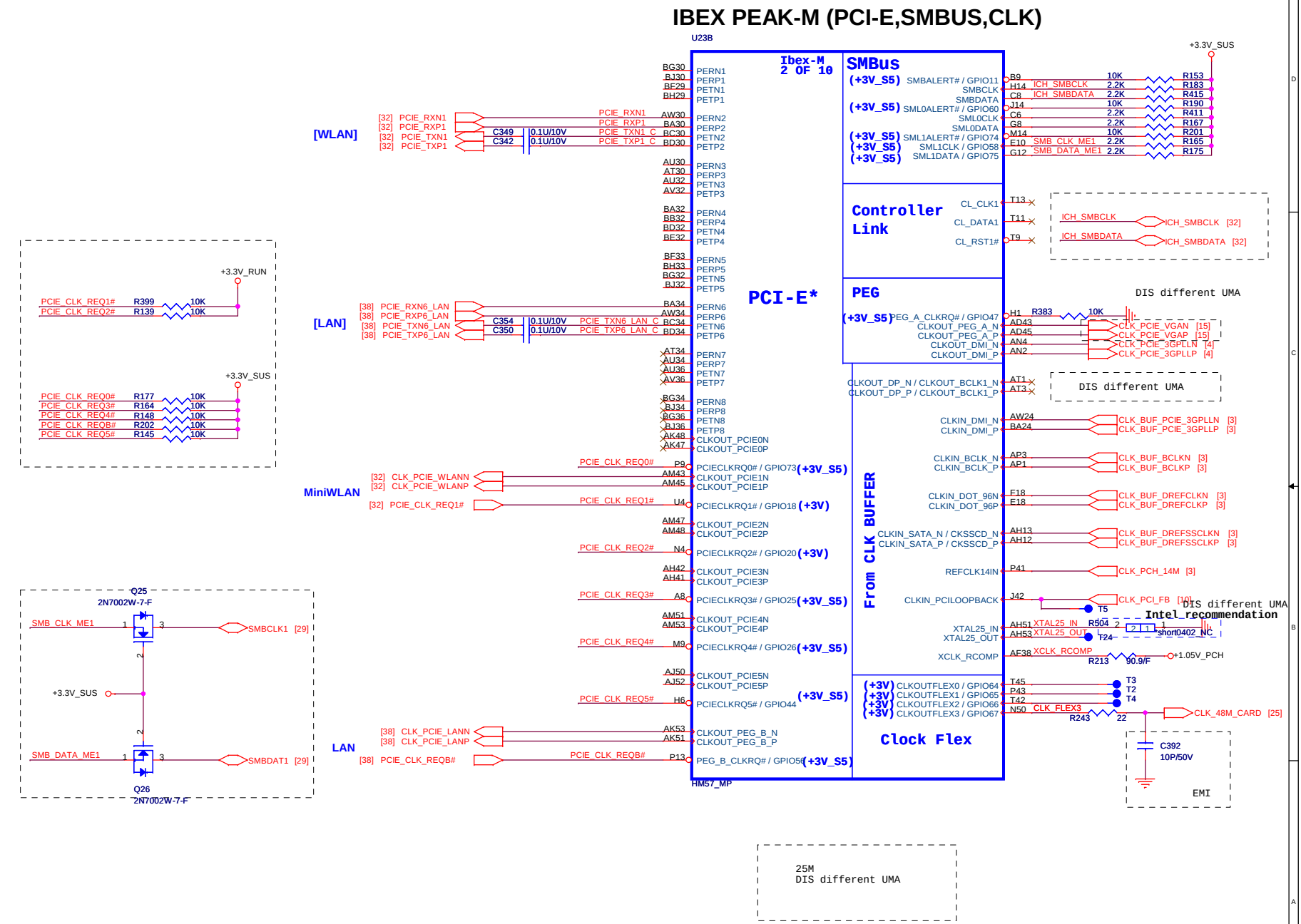
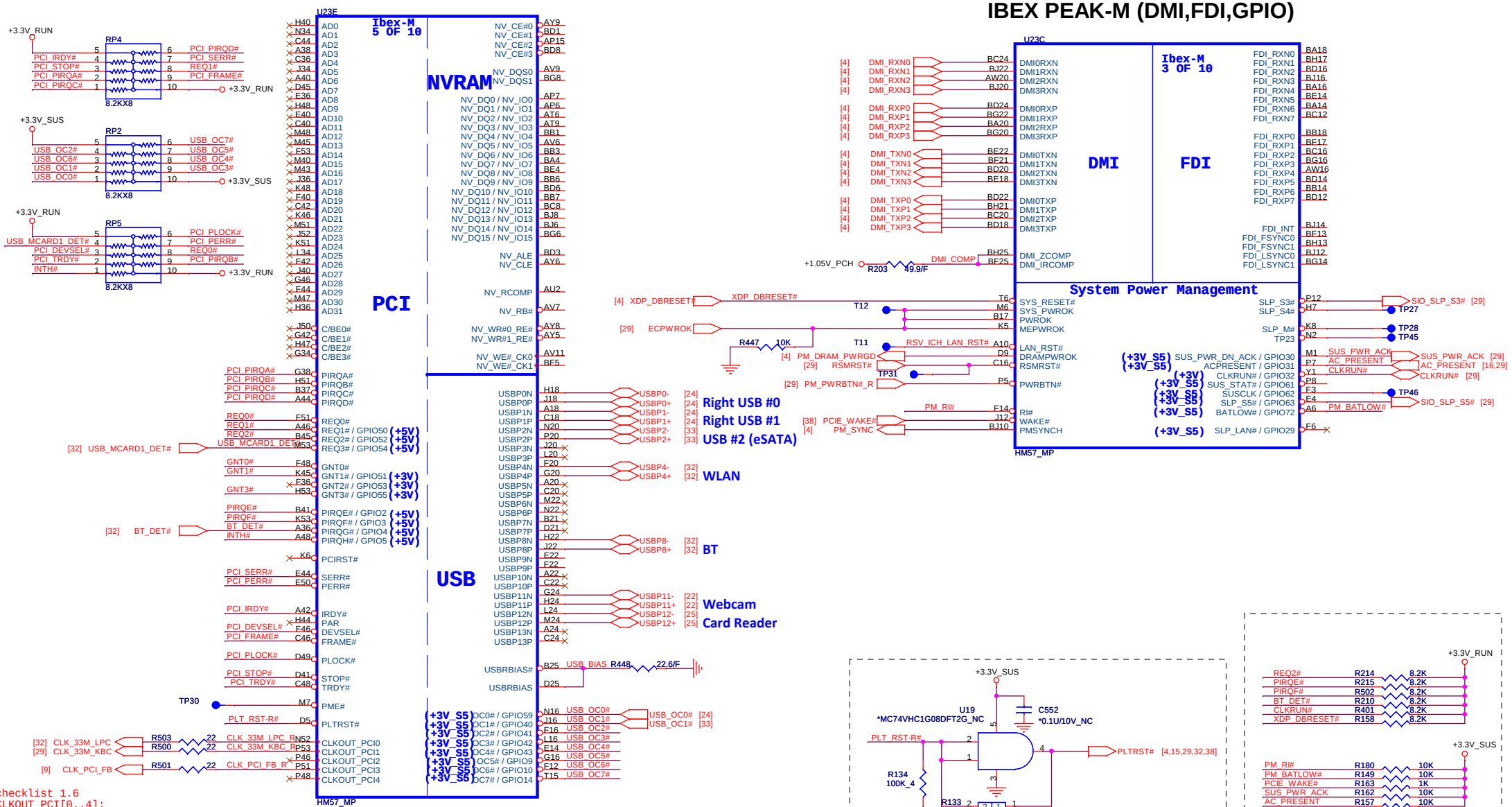
IBEX PEAK-M (GND)



IBEX PEAK-M (PCI-E,SMBUS,CLK)

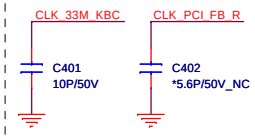


IBEX PEAK-M (PCI,USB,NVRAM)



checklist 1.6
CLKOUT_PCI[0..4]:
47 Ω to 30 Ω
(depends on number of loads)

Reserve capacitor pads for improving WWAN.



GNT0# R231 *1K_NC
GNT1# R499 *1K_NC

Boot BIOS Strap

PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

GNT3# R498 *4.7K_NC

A16 swap override Strap/Top-Block Swap Override jumper

GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

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Size	Document Number	Rev
	PCH 3/5 (PCI,ONFI,USB,DMI)	3A

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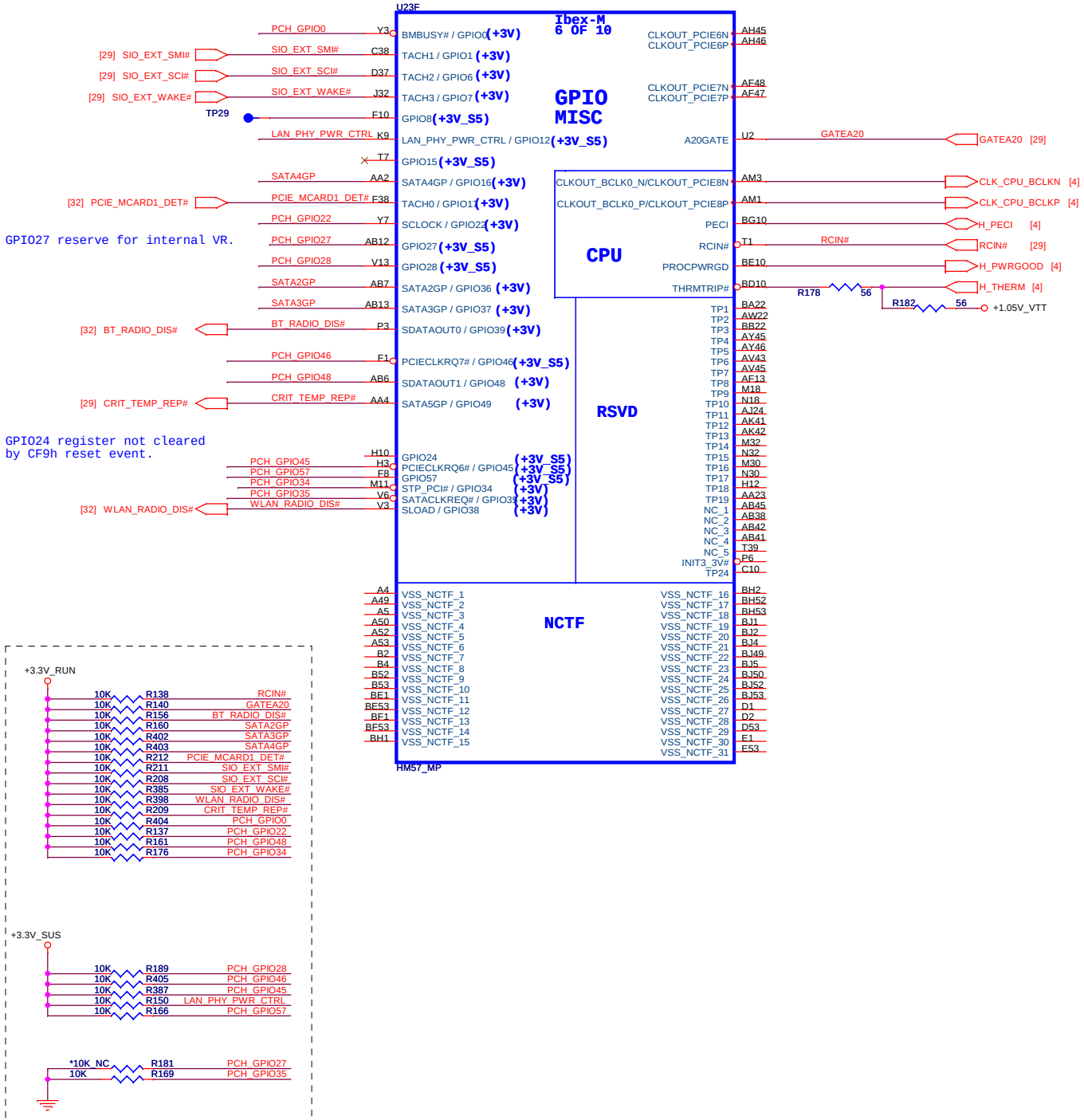
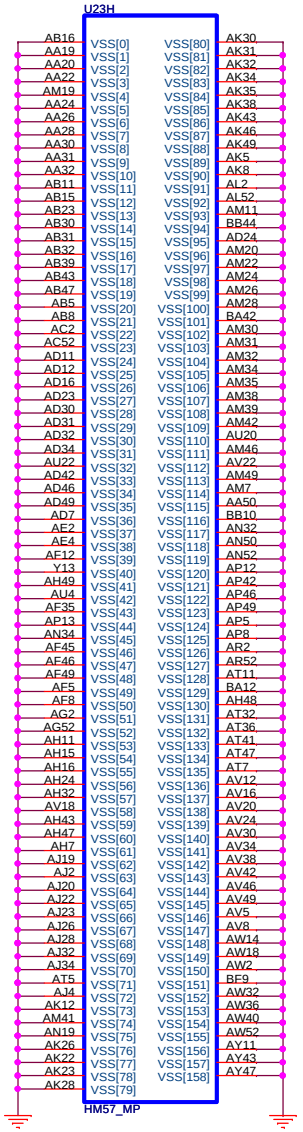
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



IBEX PEAK-M (GND)



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PROJECT : UM7 DIS	
Size	Document Number: PCH 4/5 (GPIO & Strap) — Rev 3A
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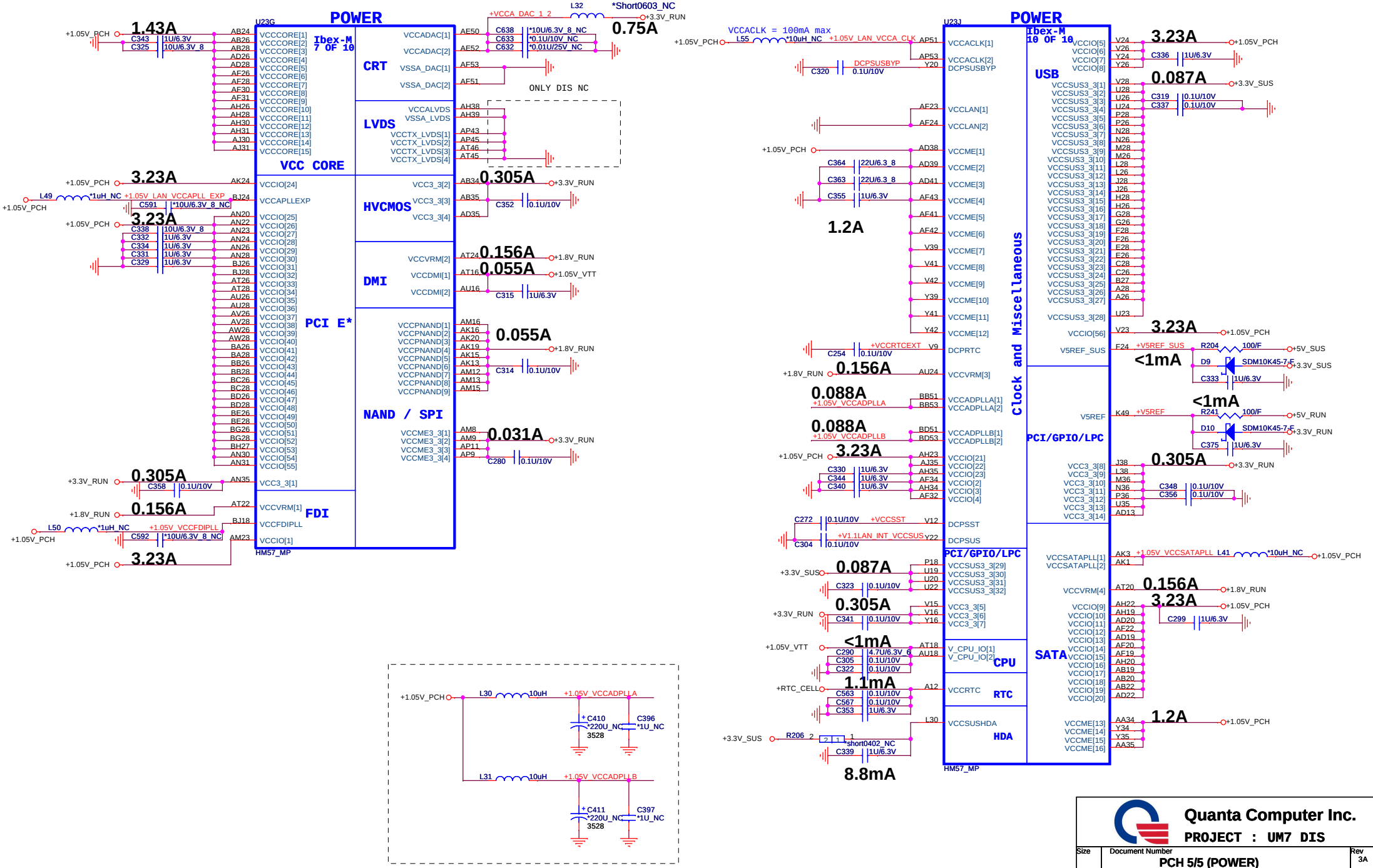
L32 UMA↓
EMI FILTER HCB1608KF-181T15(180,1.5A)
CX000181016

L32 DIS→SHORT



Quanta Computer Inc.			
PROJECT : UM7 DIS			
Size	Document Number		Rev
	PCH 5/5 (POWER)		3A
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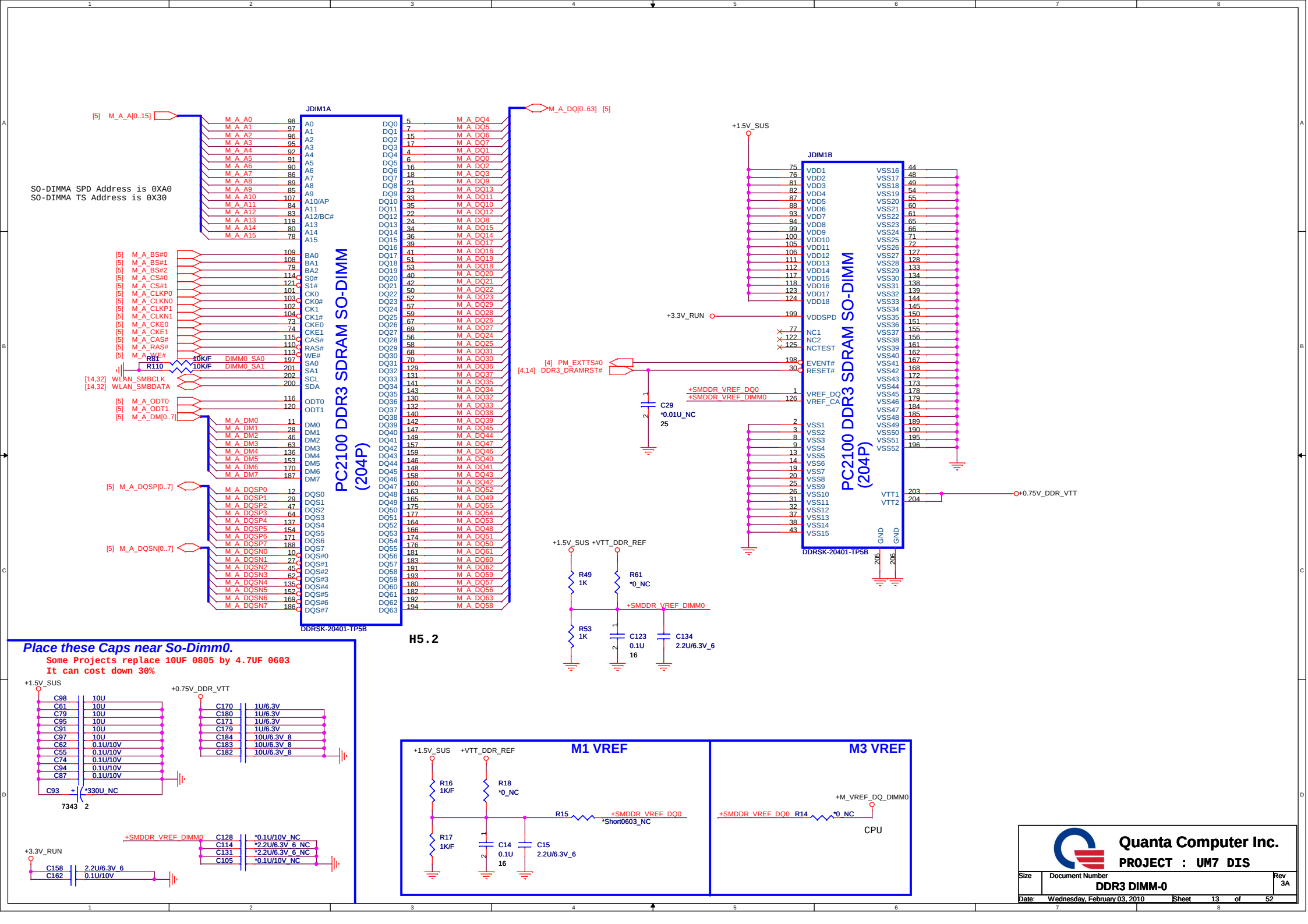
JDIM1A
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDRSK-20401-TP5B
SO-DIMMA SPD Address is 0XA0
SO-DIMMA TS Address is 0X30
[5] M_A_A[0..15]
M_A_DQ[0..63] [5]
[5] M_A_BS#0
[5] M_A_BS#1
[5] M_A_BS#2
[5] M_A_CS#0
[5] M_A_CS#1
[5] M_A_CLKP0
[5] M_A_CLKN0
[5] M_A_CLKP1
[5] M_A_CLKN1
[5] M_A_CKE0
[5] M_A_CKE1
[5] M_A_CAS#
[5] M_A_RAS#
[5] M_A_WE#
R81 10K/F DIMM0_SA0
R110 10K/F DIMM0_SA1
[14,32] WLAN_SMBCLK
[14,32] WLAN_SMBDATA
[5] M_A_ODT0
[5] M_A_ODT1
[5] M_A_DM[0..7]
[5] M_A_DQSP[0..7]
[5] M_A_DQSN[0..7]
H5.2
JDIM1B
+1.5V_SUS
+3.3V_RUN
[4] PM_EXTTS#0
[4,14] DDR3_DRAMRST#
+SMDDR_VREF_DQ0
+SMDDR_VREF_DIMM0
C29 *0.01U_NC 25
+0.75V_DDR_VTT
DDRSK-20401-TP5B
+1.5V_SUS +VTT_DDR_REF
R49 1K
R61 *0_NC
+SMDDR_VREF_DIMM0
R53 1K
C123 0.1U 16
C134 2.2U/6.3V_6
Place these Caps near So-Dimm0.
Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%
+1.5V_SUS
C98 10U
C61 10U
C79 10U
C95 10U
C91 10U
C97 10U
C62 0.1U/10V
C55 0.1U/10V
C74 0.1U/10V
C94 0.1U/10V
C87 0.1U/10V
C93 *330U_NC
7343 2
+0.75V_DDR_VTT
C170 1U/6.3V
C180 1U/6.3V
C171 1U/6.3V
C179 1U/6.3V
C184 10U/6.3V_8
C183 10U/6.3V_8
C182 10U/6.3V_8
+SMDDR_VREF_DIMM0
C128 *0.1U/10V_NC
C114 *2.2U/6.3V_6_NC
C131 *2.2U/6.3V_6_NC
C105 *0.1U/10V_NC
+3.3V_RUN
C158 2.2U/6.3V_6
C162 0.1U/10V
M1 VREF
+1.5V_SUS +VTT_DDR_REF
R16 1K/F
R18 *0_NC
R15 *Short0603_NC
+SMDDR_VREF_DQ0
R17 1K/F
C14 0.1U 16
C15 2.2U/6.3V_6
M3 VREF
+M_VREF_DQ_DIMM0
+SMDDR_VREF_DQ0 R14 *0_NC
CPU
Quanta Computer Inc.
PROJECT : UM7 DIS
Size
Document Number
DDR3 DIMM-0
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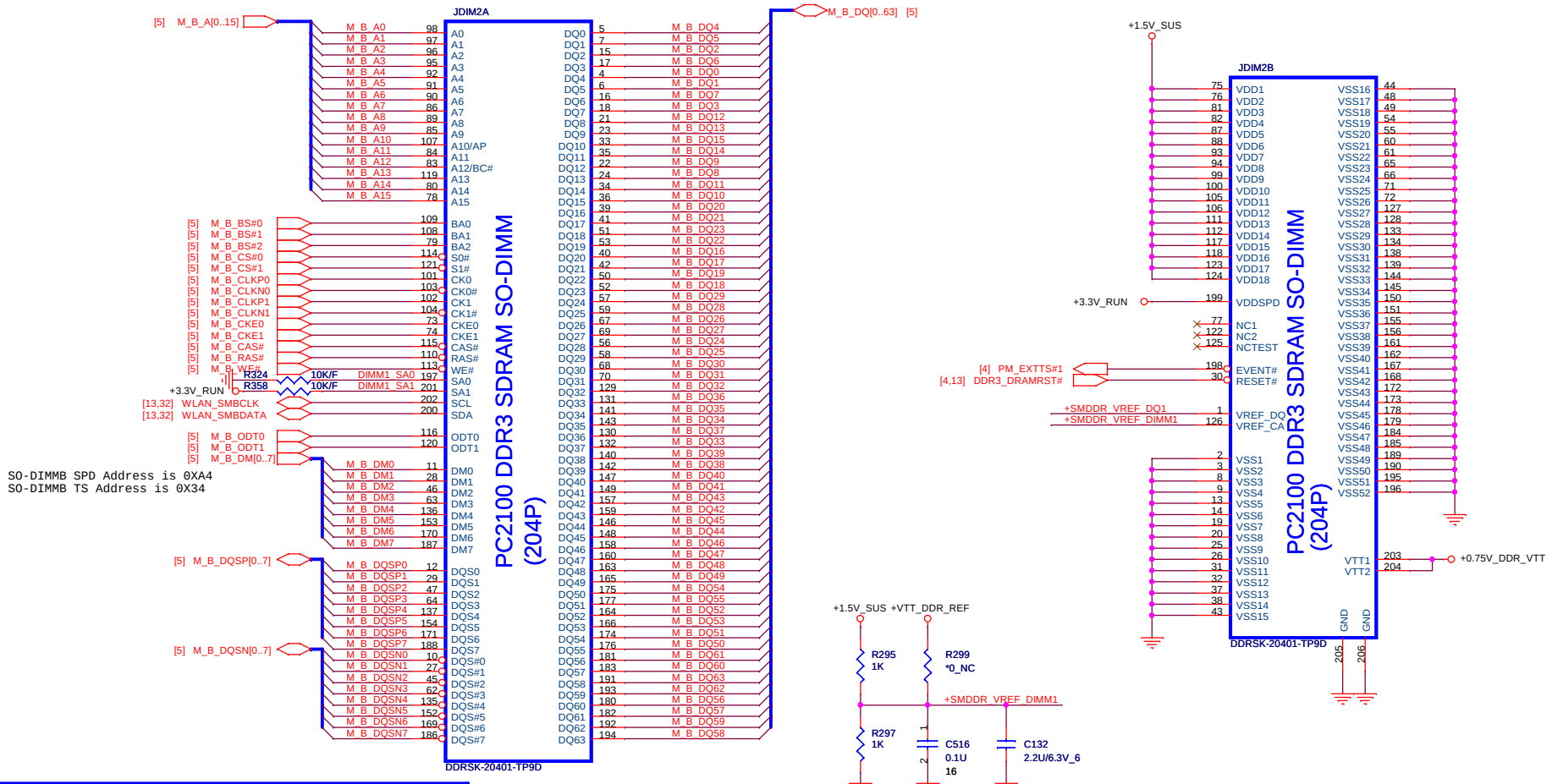
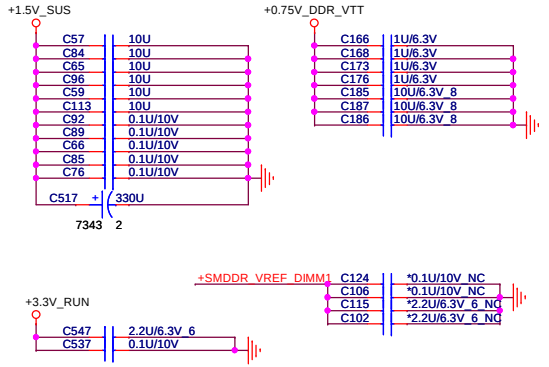
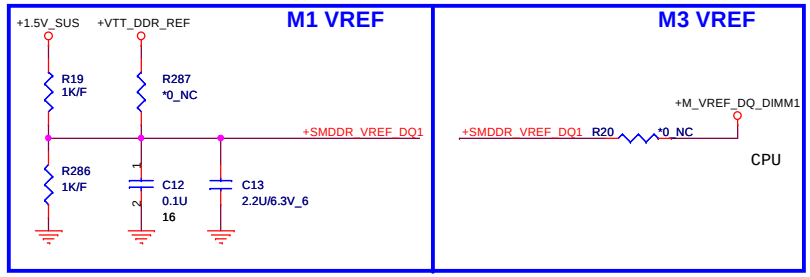


H9.2

Place these Caps near So-Dimm1.

Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%





Quanta Computer Inc.

PROJECT : UM7 DIS

Size	Document Number	Rev
	DDR3 DIMM-1	3A

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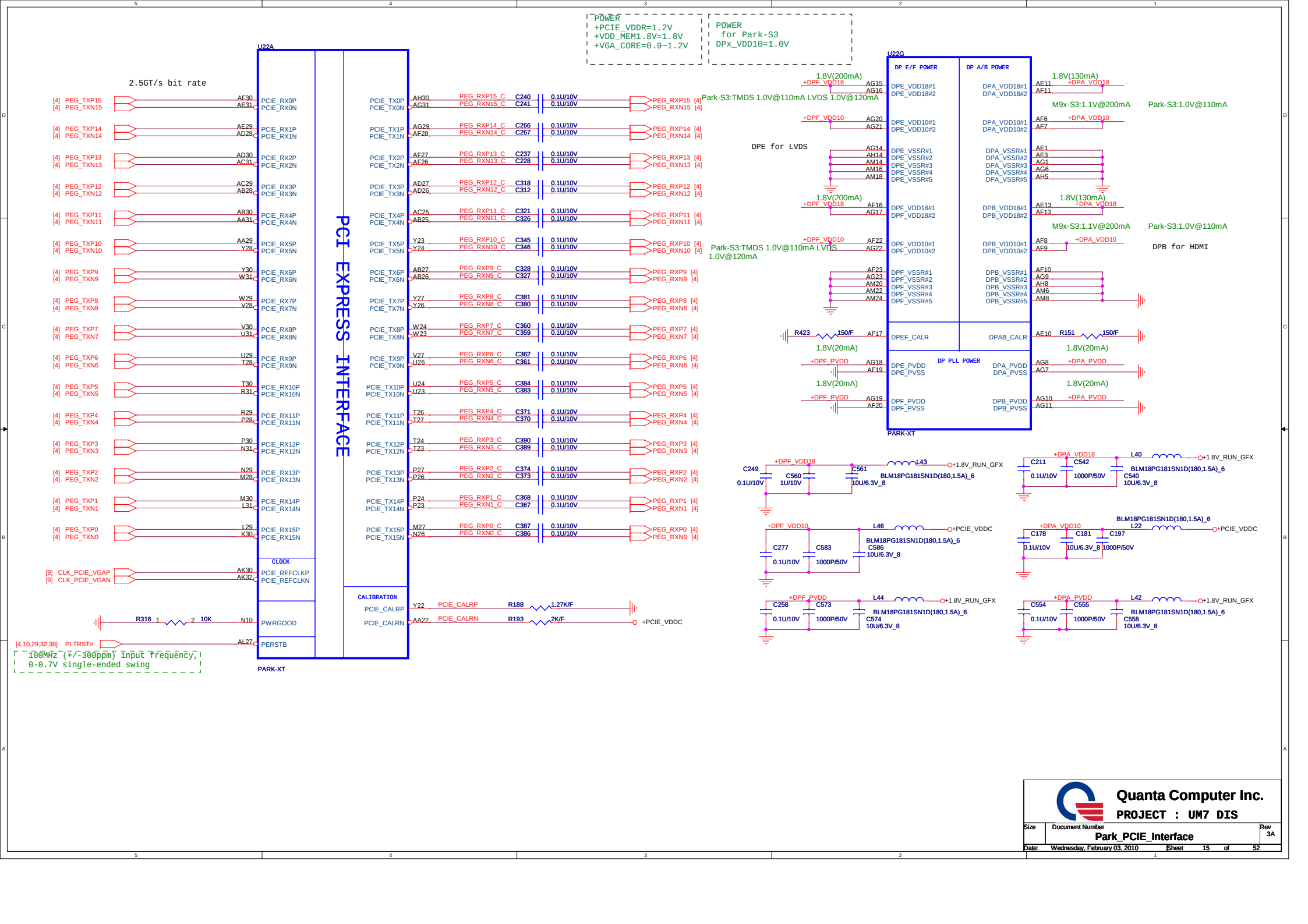
POWER
+PCIE_VDDR=1.2V
+VDD_MEM1.8V=1.8V
+VGA_CORE=0.9~1.2V
POWER
for Park-S3
DPx_VDD10=1.0V
U22A
2.5GT/s bit rate
PCI EXPRESS INTERFACE
CLOCK
CALIBRATION
PWRGOOD
PERSTB
PARK-XT
100MHz (+/-300ppm) input frequency,
0-0.7V single-ended swing
U22G
DP E/F POWER
DP A/B POWER
DP PLL POWER
DPE for LVDS
DPB for HDMI
Park-S3:TMDS 1.0V@110mA LVDS 1.0V@120mA
M9x-S3:1.1V@200mA
Park-S3:1.0V@110mA
1.8V(200mA)
1.8V(130mA)
1.8V(20mA)
PARK-XT
Quanta Computer Inc.
PROJECT : UM7 DIS
Park_PCIE_Interface
Size
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MEM_ID[3:0]	Vendor	Type	Vendor P/N	Quanta P/N
0000	Hynix Orion-die	64*16-800MHZ	H5TQ1G63BFR-12C	AKD5LZGTW00
0001	Samsung E-die	64*16-800MHZ	K4W1G1646E-HC12	AKD5LGGT502
0010	Samsung B-die	128*16-800MHZ	K4W2G1646B-HC12	AKD5M00T501
0011		Reserved		
0100		Reserved		
0101		Reserved		
0110		Reserved		
0111		Reserved		
1000		Reserved		
1001		Reserved		
1010		Reserved		
1011		Reserved		
1100		Reserved		
1101		Reserved		
1110		Reserved		
1111		Reserved		

Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

GPU Power-on sequence

Power-Up

- +3.3V_RUN → +VCC_GFX_CORE
- +PCIE_VDDC → +1.8V_RUN_GFX
- CLK_PCIE_VGAP/N → +1.8V_RUN_GFX
- +3.3V_RUN early +VCC_GFX_CORE /+1.8V_RUN_GFX or when +VCC_GFX_CORE /+1.8V_RUN_GFX up then +3.3V_RUN
- +VCC_GFX_CORE reach 90% and +1.8V_RUN_GFX

power-down

- +1.8V_RUN_GFX → +PCIE_VDDC

PCIe ref clock(CLK_PCIE_VGAA/B) early +1.8V

	BBEN	BBP
L	0	V-CORE
H	1	+1.8V

R475 =>
100/F for CLK_VGA_27M CLK Gen
0ohm for Crystal
CS11002FR22
RES CHIP 100 1/16W +-1%(0402)

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Size	Document Number	Rev
	Park_Main	3A
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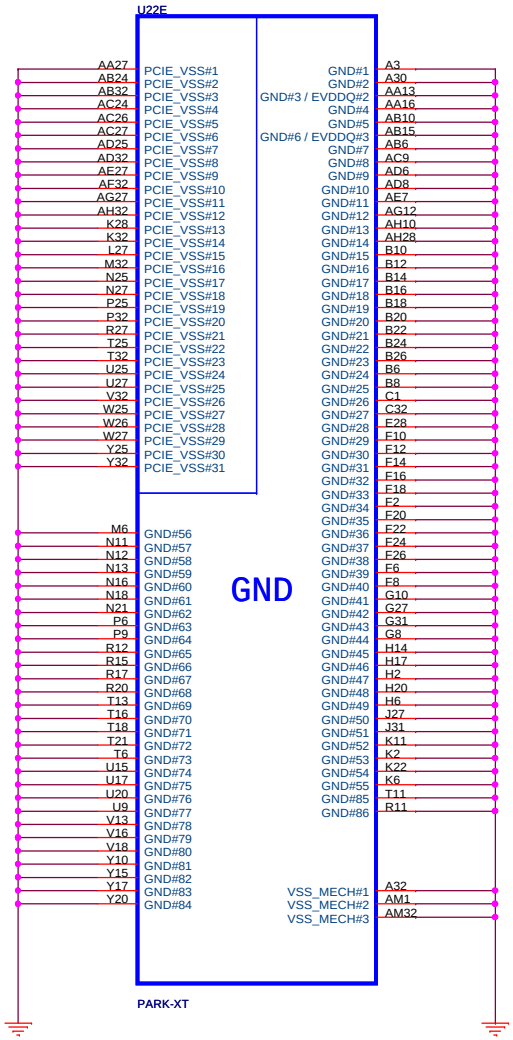

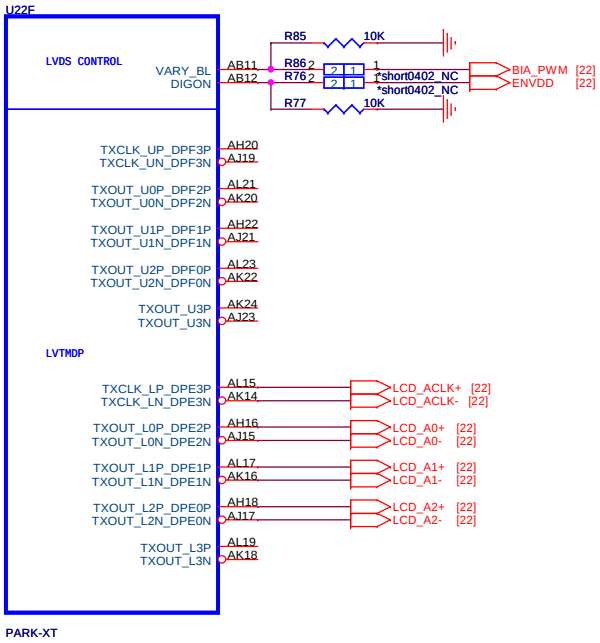

Strap Name		Pin Straps description	Default Value
TX_PWRS_ENB	GPIO0	**PCI Express Full TX Output Swing** 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	**PCI Express Transmitter De-emphasis Enable** 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on. 1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on. 5.0 GT/s capability will be controlled by software.	1
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	**Enable CLKREQ# Power Management** 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0 0 0
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	1
AUD[0] AUD(1)	VSYNC HSYNC	**AUD[1] AUD[0]** 00 No Audio function 01 Audio for DisplayPort and HDMI if dongle is detected 10 Audio for DisplayPort only 11 Audio for both DisplayPort and HDMI	1 1
VIP_DEVICE_STRAP_ENA	V2SYNC	If VIP_DEVICE_STRAP_EN is set to ?? then this pin is used to sense whether a VIP slave device is connected to the VIP Host interface. If VIP_DEVICE_STRAP_EN is set to ?? then this pin is not used as a strap at all (i.e. its value during reset is unimportant), and it can be used as a regular GPIO	0
RSVD	GENERICC		0

Quanta Computer Inc.
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Size	Document Number	Rev
	Park_GND / LVDS/ Straps	3A
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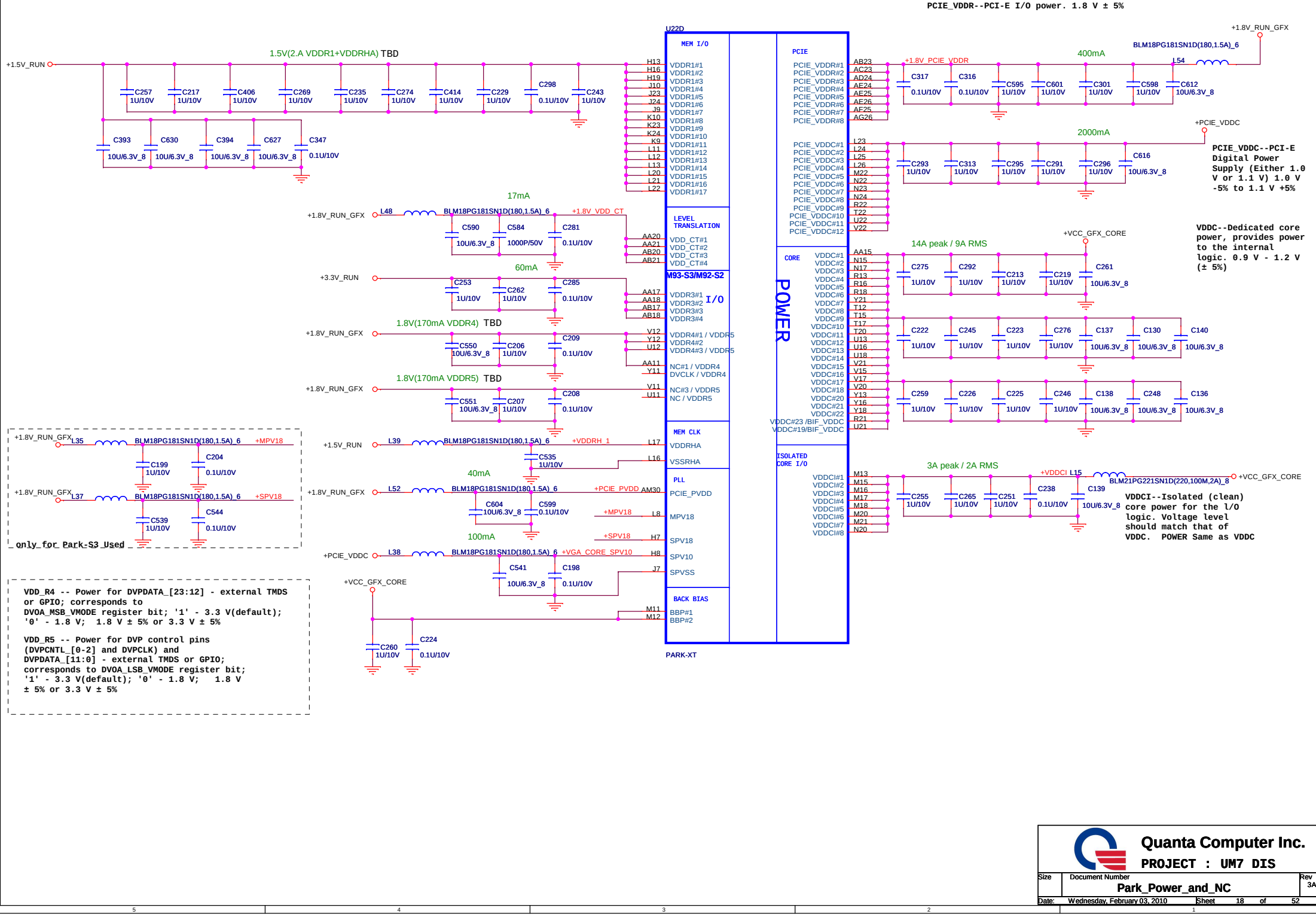
PCIE_VDDR--PCI-E I/O power. 1.8 V ± 5%
U22D
MEM I/O
LEVEL TRANSLATION
M93-S3/M92-S2 I/O
MEM CLK
PLL
BACK BIAS
PCIE
CORE
ISOLATED CORE I/O
POWER
PARK-XT
+1.5V_RUN
1.5V(2.A VDDR1+VDDRHA) TBD
+1.8V_RUN_GFX
17mA
+3.3V_RUN
60mA
1.8V(170mA VDDR4) TBD
1.8V(170mA VDDR5) TBD
40mA
100mA
+PCIE_VDDC
+VCC_GFX_CORE
+1.8V_PCIE_VDDR
400mA
2000mA
14A peak / 9A RMS
3A peak / 2A RMS
+VDDCI
+MPV18
+SPV18
+VDDRH_1
+PCIE_PVDD
+VGA_CORE_SPV10
only for Park-S3 Used
PCIE_VDDC--PCI-E Digital Power Supply (Either 1.0 V or 1.1 V) 1.0 V -5% to 1.1 V +5%
VDDC--Dedicated core power, provides power to the internal logic. 0.9 V - 1.2 V (± 5%)
VDDCI--Isolated (clean) core power for the I/O logic. Voltage level should match that of VDDC. POWER Same as VDDC
VDD_R4 -- Power for DVPDATA_[23:12] - external TMDS or GPIO; corresponds to DVOA_MSB_VMODE register bit; '1' - 3.3 V(default); '0' - 1.8 V; 1.8 V ± 5% or 3.3 V ± 5%
VDD_R5 -- Power for DVP control pins (DVPCNTL_[0-2] and DVPCLK) and DVPDATA_[11:0] - external TMDS or GPIO; corresponds to DVOA_LSB_VMODE register bit; '1' - 3.3 V(default); '0' - 1.8 V; 1.8 V ± 5% or 3.3 V ± 5%
Quanta Computer Inc.
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Park_Power_and_NC
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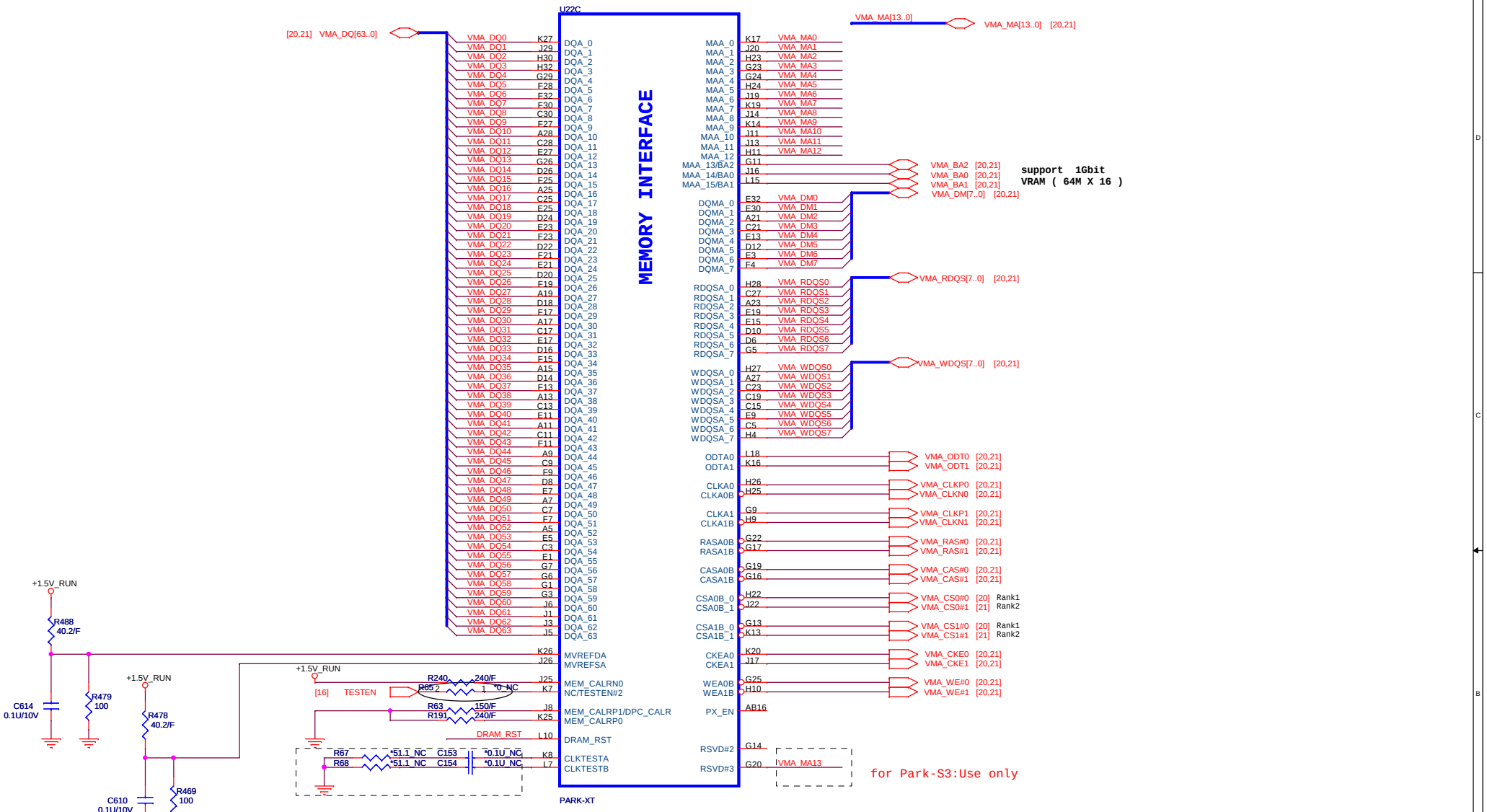
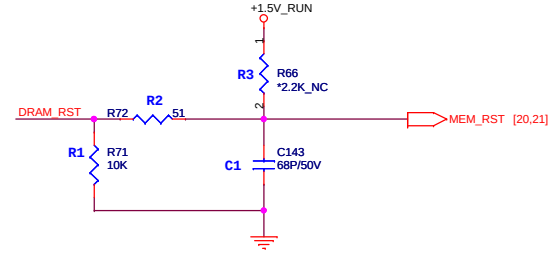


	M9x-S2/S3	Park-S3
MEM_CALRN0(J25) MEM_CALRP0(K25)	NC	240R
MEM_CALRP1(J8)	240R	150R
TESTEN2#2(K7)	NC	0R
R1	NC	10K
R2	0R	51R
R3	2.2K	NC
C1	2.2nF	68pF

240R:CS12402FB03
150R:CS11502FB21

0R:CS00002JB38
51R:CS05102JB35

2.2nF:CH22206KB16
68pF:CH06806JB01



Quanta Computer Inc.
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	Park_MEM_Interface	3A
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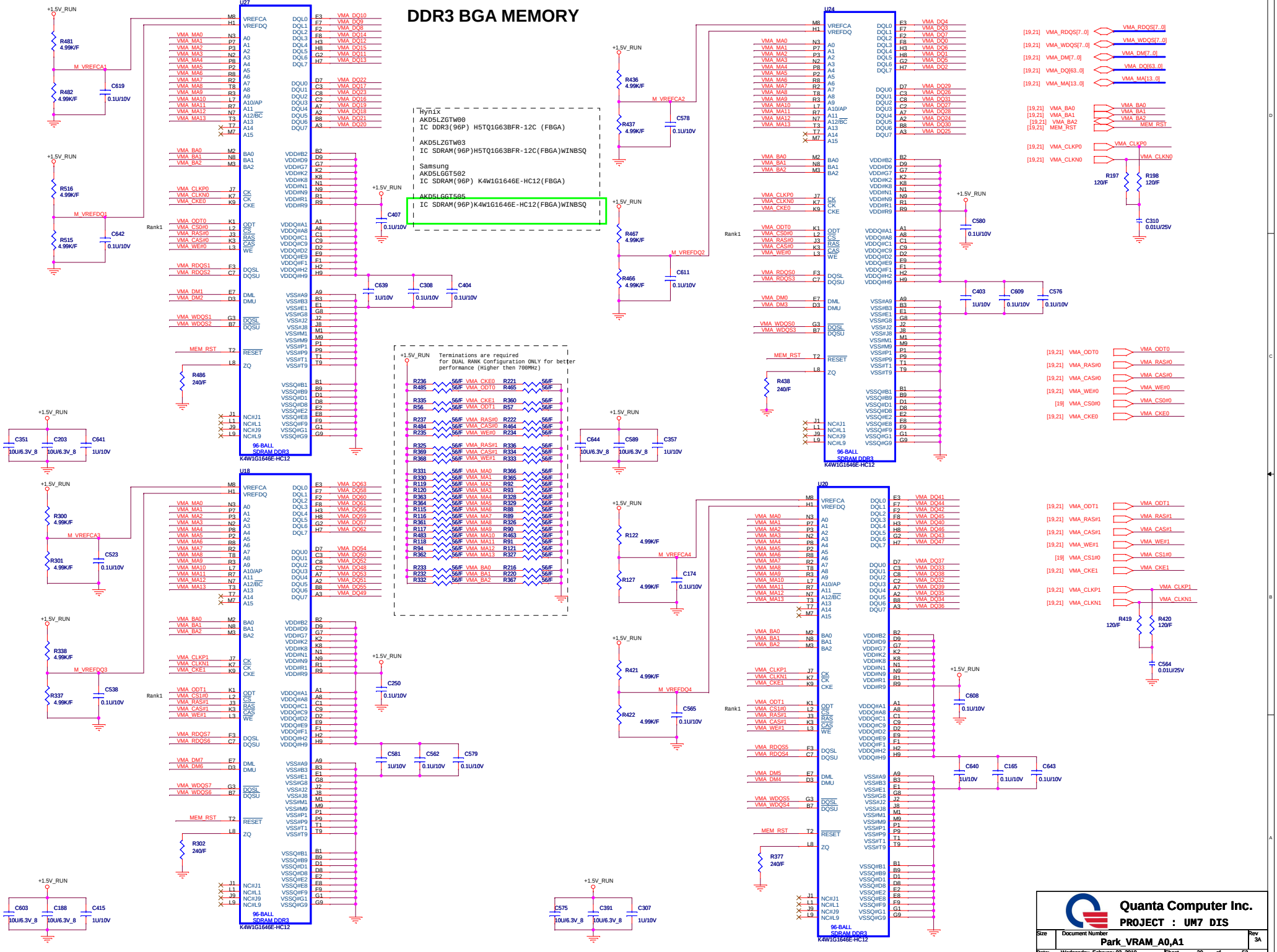
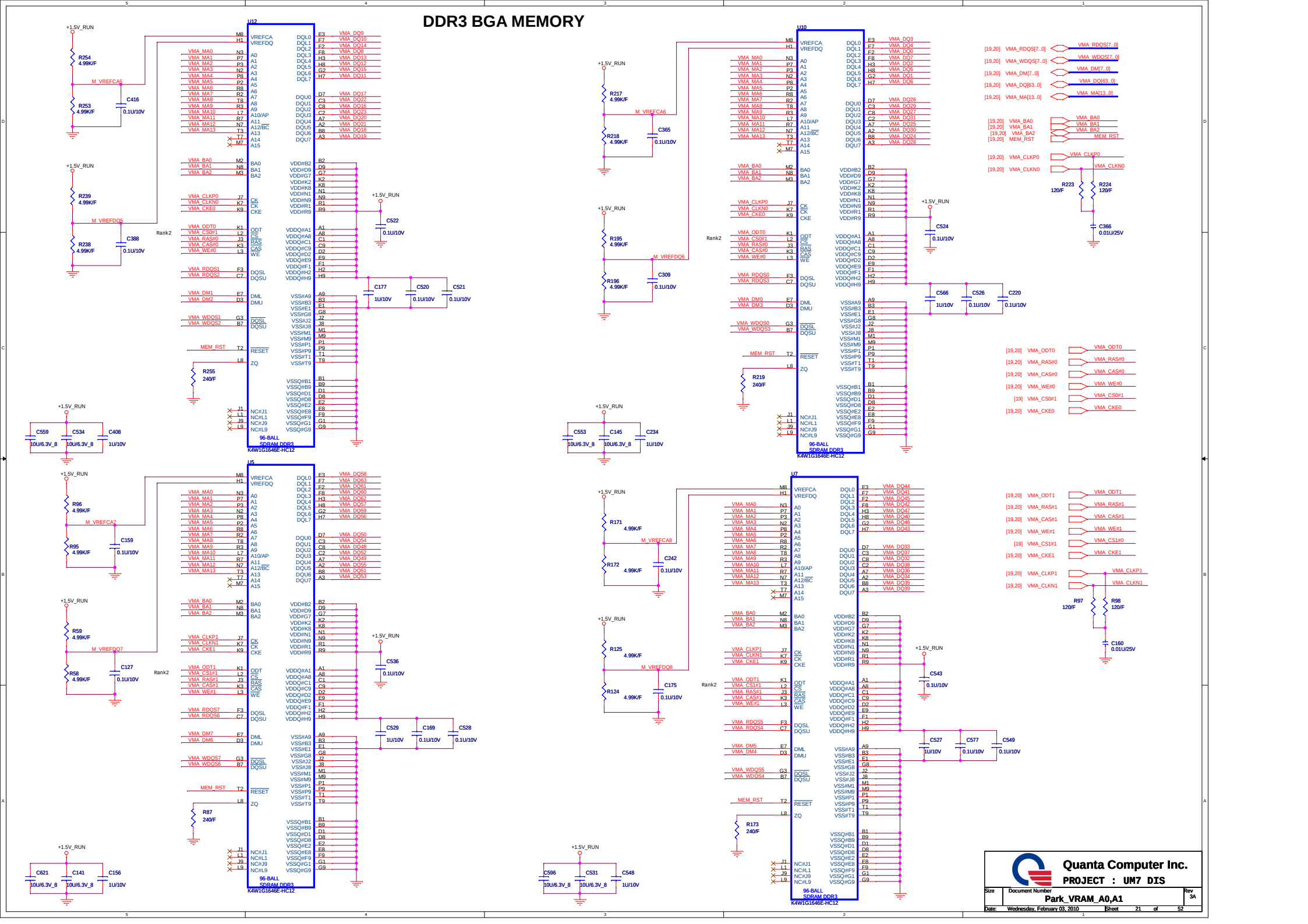
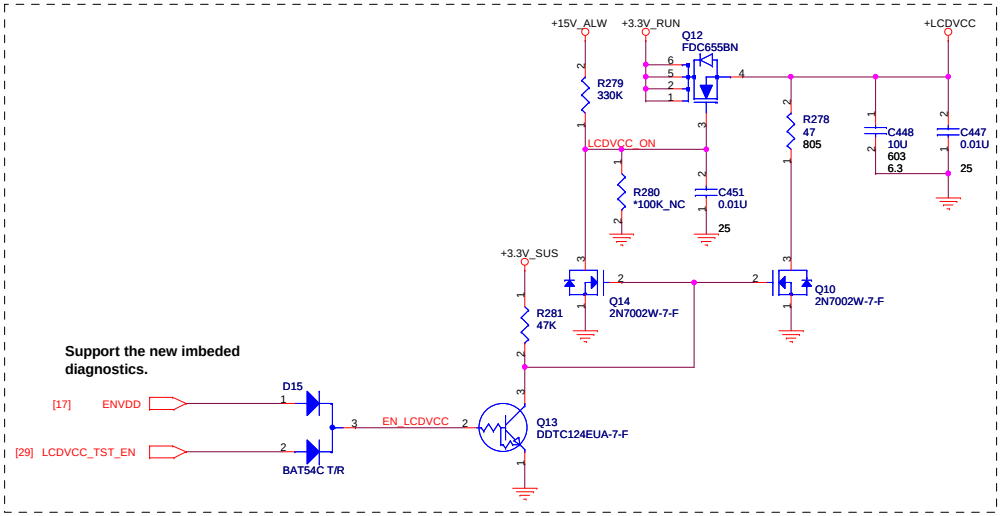
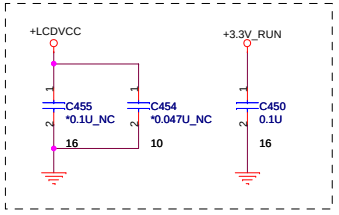
DDR3 BGA MEMORY

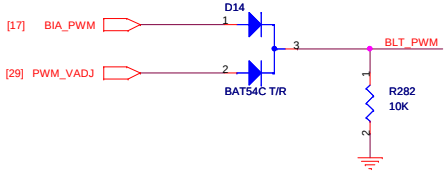


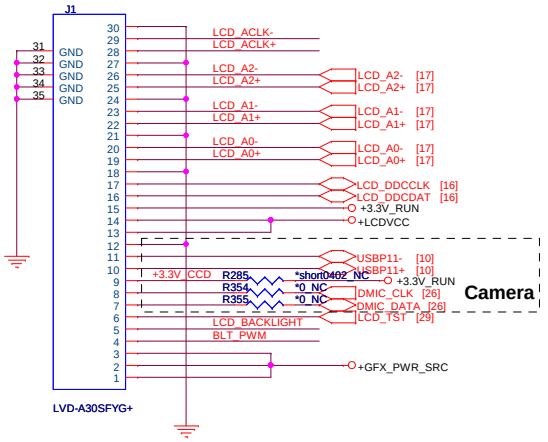
DDR3 BGA MEMORY

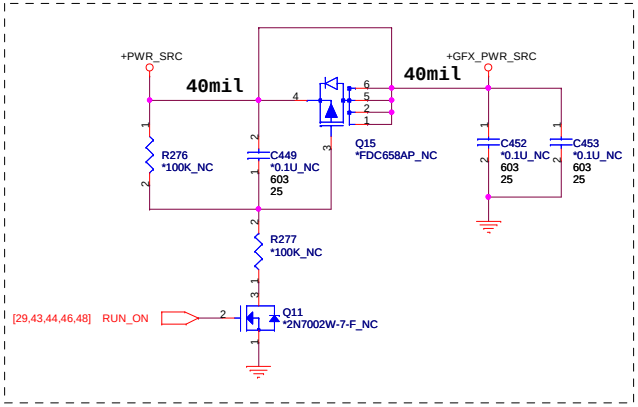


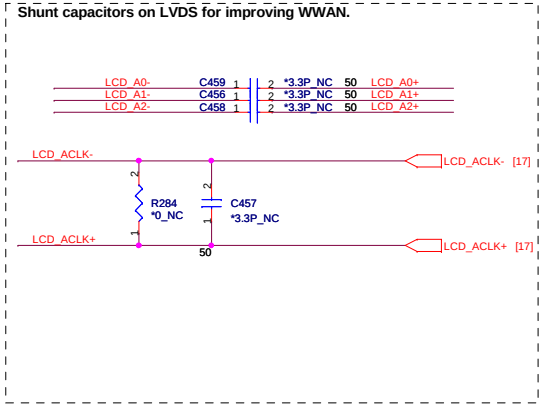


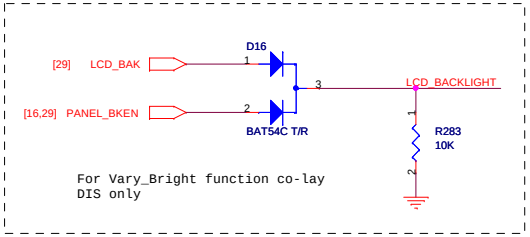












Quanta Computer Inc.

PROJECT : UM7 DIS

Size	Document Number	Rev
	LCD CONN / HDMI CONN	3A

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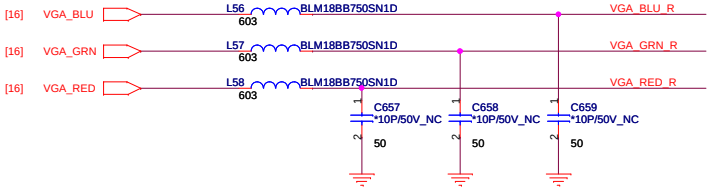

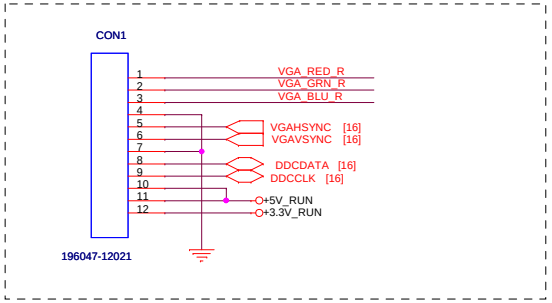

Quanta Computer Inc.

PROJECT : UM7 DIS

Size	Document Number	Rev
	CRT CONN	3A

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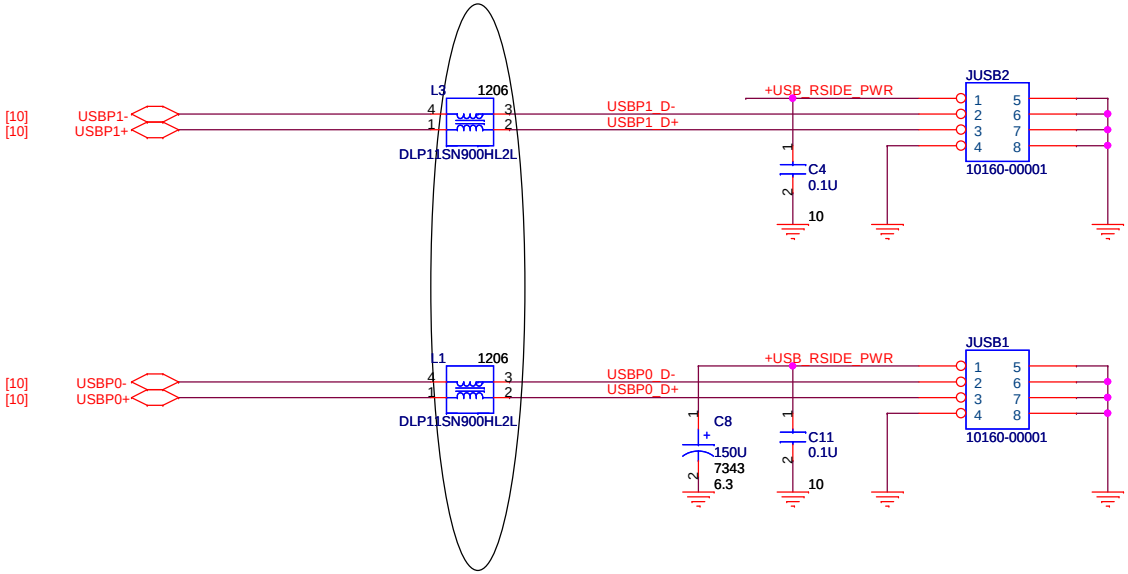
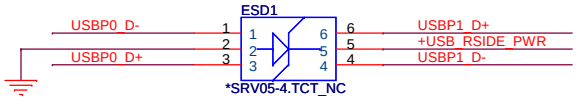


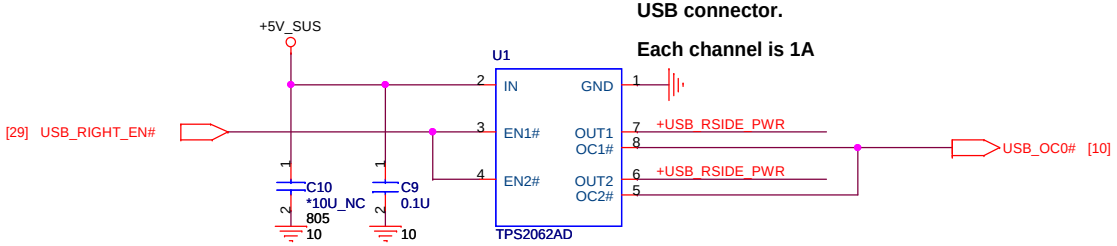
Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

Place ESD diodes as close as USB connector.



Place one 150uF cap by each USB connector.

Each channel is 1A



Quanta Computer Inc.		
PROJECT : UM7 DIS		
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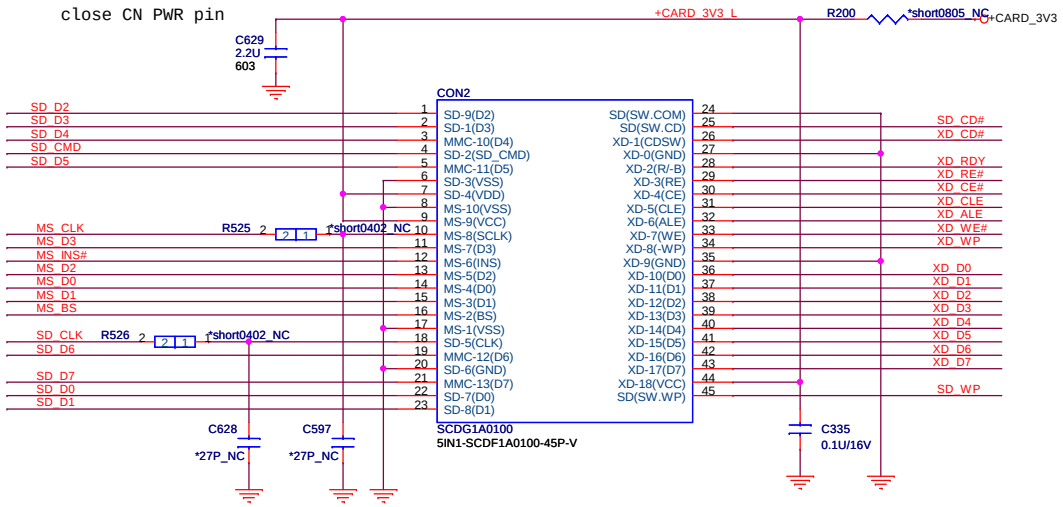
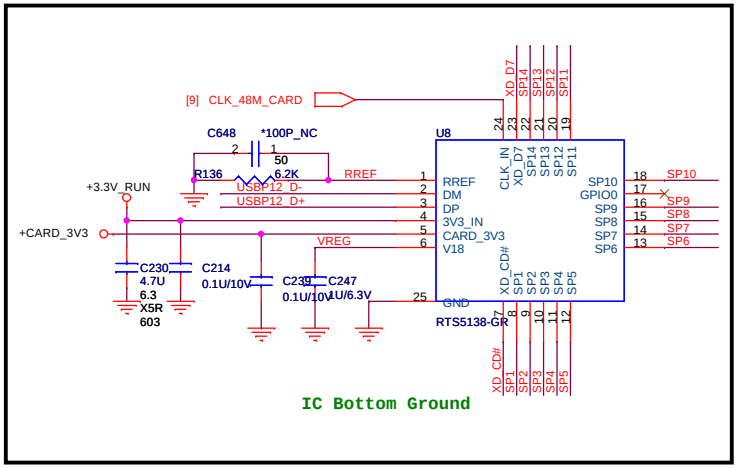
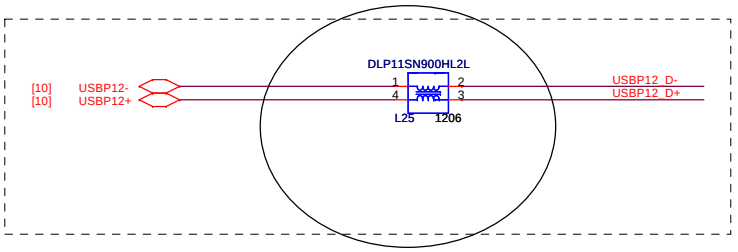




RTS5138-QFN24



SP1	XD_RDY	SD_WP	MS_CLK
SP2	XD_RE#		MS_INS#
SP3	XD_CE#	SD_D1	
SP4	XD_CLE	SD_D0	MS_D7
SP5	XD_ALE	SD_D7	MS_D3
SP6	XD_WE#	SD_CD#	
SP7	XD_WP	SD_D6	MS_D6
SP8	XD_D0	SD_CLK	MS_D2
SP9	XD_D1	SD_D5	MS_D0
SP10	XD_D2	SD_CMD	
SP11	XD_D3	SD_D4	MS_D4
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	MS_D5
SP14	XD_D6		MS_BS

Share Pin

Quanta Computer Inc.

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Size	Document Number	Rev
	Card Reader(RST5138)	3A
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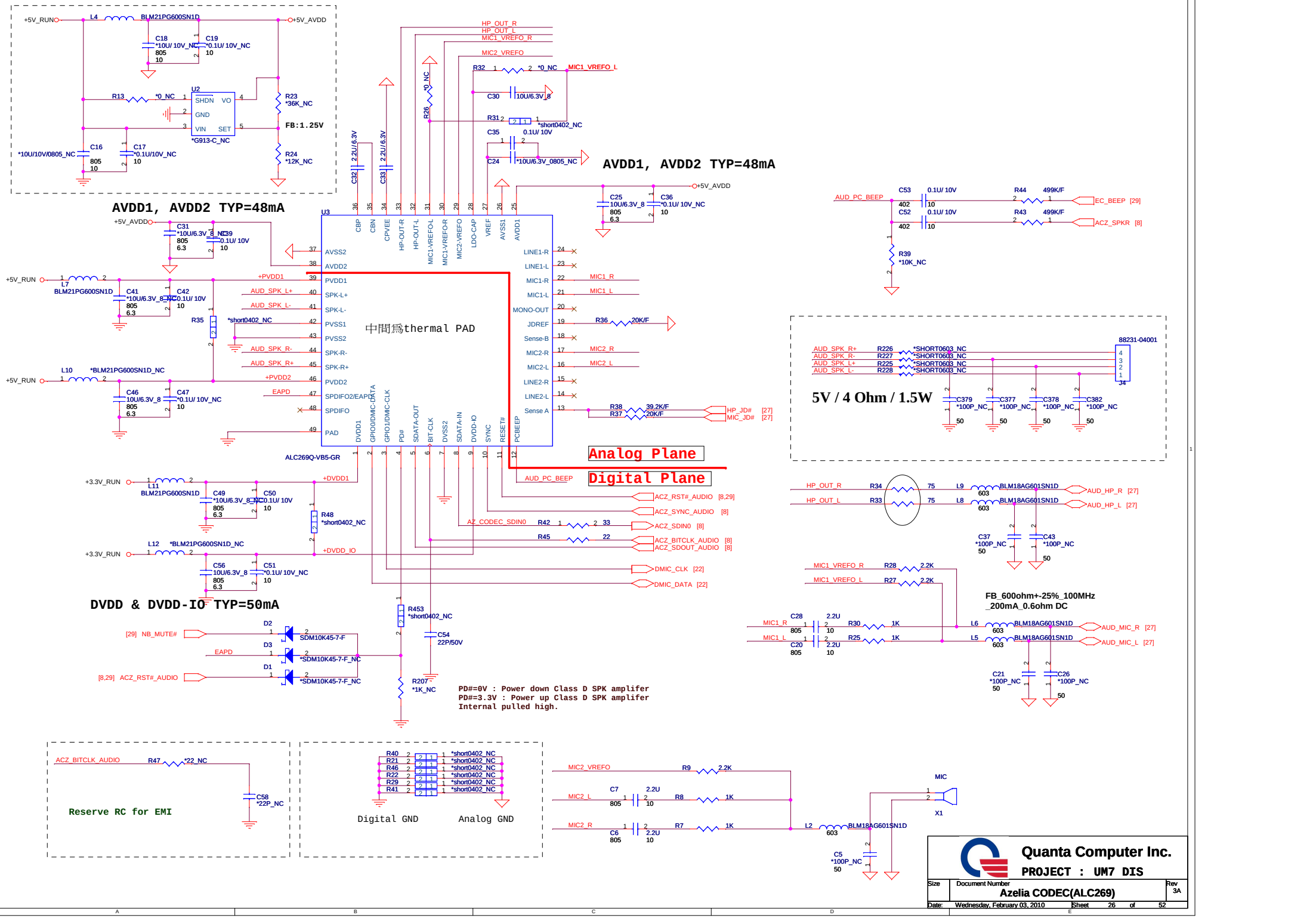
AVDD1, AVDD2 TYP=48mA
AVDD1, AVDD2 TYP=48mA
中間爲thermal PAD
ALC269Q-VB5-GR
Analog Plane
Digital Plane
DVDD & DVDD-IO TYP=50mA
5V / 4 Ohm / 1.5W
FB_600ohm+-25%_100MHz
_200mA_0.6ohm DC
PD#=0V : Power down Class D SPK amplifer
PD#=3.3V : Power up Class D SPK amplifer
Internal pulled high.
Reserve RC for EMI
Digital GND
Analog GND
Quanta Computer Inc.
PROJECT : UM7 DIS
Azelia CODEC(ALC269)
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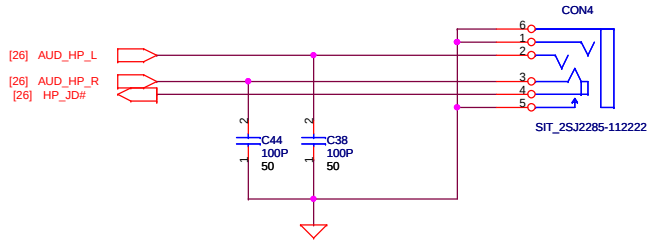
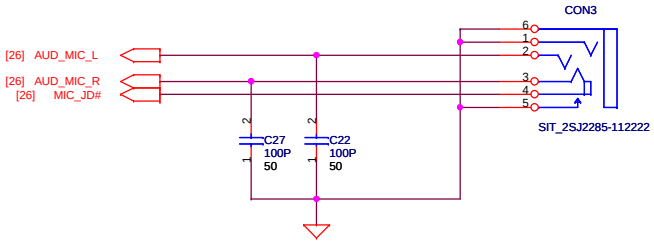
HP JACKN

SUYIN NORMAL OPEN



MIC JACK

SUYIN NORMAL OPEN



Quanta Computer Inc.

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Size	Document Number	Rev
	AUDIO CONN	3A
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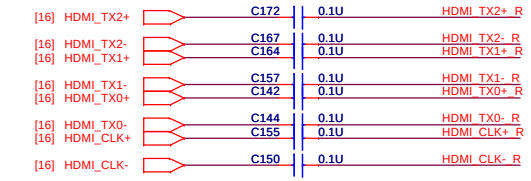

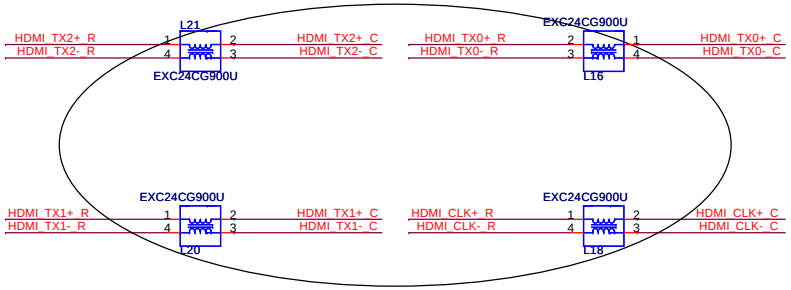

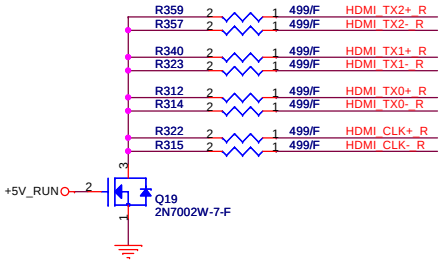

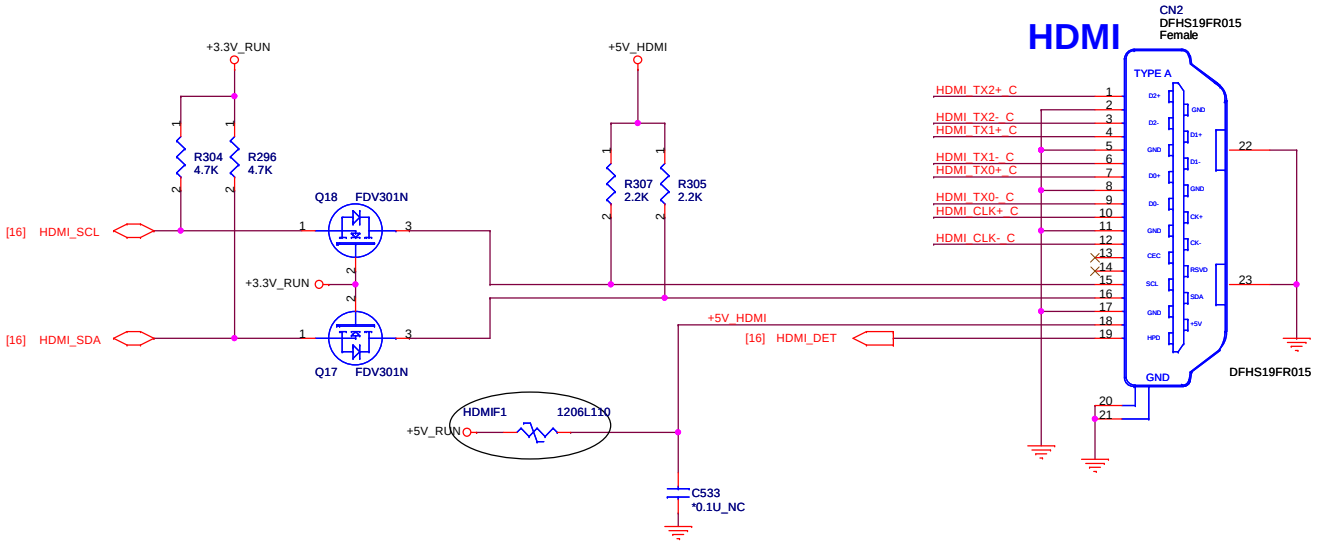

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PROJECT : UM7 DIS		
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ITE8502E LQFP-128L

U25

[34] KSO[0..16]
[34] KSI[0..7]

KSO16 KSO15 KSO14 KSO13 KSO12 KSO11 KSO10 KSO9 KSO8 KSO7 KSO6 KSO5 KSO4 KSO3 KSO2 KSO1 KSO0

KSI7 KSI6 KSI5 KSI4 KSI3 KSI2 KSI1 KSI0

KEYBOARD

KSO17/GPC5
KSO16/GPC3
KSO15
KSO14
KSO13
KSO12/SLCT
KSO11/ERR
KSO10/PE
KSO9/BUSY
KSO8/ACK
KSO7/PD7
KSO6/PD6
KSO5/PD5
KSO4/PD4
KSO3/PD3
KSO2/PD2
KSO1/PD1
KSO0/PD0

KSI7
KSI6
KSI5
KSI4
KSI3/SLIN
KSI2/INIT
KSI1/AFD
KSI0/STB

ADC/DAC

ADC0/GPI0
ADC1/GPI1
ADC2/GPI2
ADC3/GPI3
ADC4/GPI4
ADC5/GPI5
ADC6/GPI6
ADC7/GPI7

DAC0/GPJ0
DAC1/GPJ1
DAC2/GPJ2
DAC3/GPJ3
DAC4/GPJ4
DAC5/GPJ5

HWPG [37,40,45]
SUS_PWR_ACK [10]
LCD_CBL_DET#
V_ID1
PBAT_PRES# [47]
IINP [41]
SIO_SLP_S5# [10]
CRIT_TEMP_REP# [11]
SIO_EXT_WAKE# [11]
USB_LEFT_EN# [33]
FAN1_DA [37]
RSMRST# [10]
PM_PWRBTN#_R [10]
D23 SDM10K45-7-F

PWM

PWM0/GPA0
PWM1/GPA1
PWM2/GPA2
PWM3/GPA3
PWM4/GPA4
PWM5/GPA5
PWM6/GPA6
PWM7/GPA7

TACH0/GPD6
TACH1/GPD7

TMRI0/WUI2/GPC4
TMRI1/WUI3/GPC6

BREATH_LED [36]
FAN1_PWM [37]
PWM_VADJ [22]
EC_BEEP [26]
FAN1_TACH [37]
PANEL_BKEN [16,22]
LID_SW# [34]
SIO_SLP_S3# [10]

LPC

[4,10,15,32,38] PLTRST#
[10] CLK_33M_KBC
[8,32] LFRAME#
[8,32] LAD0
[8,32] LAD1
[8,32] LAD2
[8,32] LAD3

[10] CLKRUN#
[8] SERIRQ
[11] SIO_EXT_SMI#
[11] SIO_EXT_SCI#
[11] GATEA20
[22] LCD_TST

[11] RCIN#
[22] LCD_BAK
[26] NB_MUTE#

R458 *short0402_NC

SERIRQ
D22 SDM10K45-7-F
D20 SDM10K45-7-F
D26 SDM10K45-7-F
D25 SDM10K45-7-F
WRST#

SERIRQ
SC(V1.0)P38:
8.2-k pull-up to +V3.3S
CRB uses a 10-k pull-up to +V3.3S.

LPCRST/WUI4/GPD2
LPCCLK
LFRAME
LAD0
LAD1
LAD2
LAD3
CLKRUN/GPH0/ID0
SERIRQ
ECSMI/GPD4
ECSCI/GPD3
GA20/GPB5
LPCPD/WUI6/GPE6
KBRST/GPB6
WRST
PWUREQ/GPC7
L80HLAT/GPE0
L80LLAT/WUI7/GPE7

ICH_AZ_CODEC_RST0#

IR/UART

RXD/GPB0
TXD/GPB1
GPC0
CTX0/GPB2
CRX1/GPH1/ID1
CTX1/GPH2/ID2

H_CPUDET# [4]
IMVP_PWRGD [4,45]
RUN_ON [22,43,44,46,48]
BAT1_LED [36]
IMVP_VR_ON [45]
IMVP_VR_ON

[8,26] ACZ_RST#_AUDIO

SMBUS

Charge and BAT
PCH
VGA, LAN, Clock
Thermal IC

[41,47] SMBCLK0
[41,47] SMBDAT0
[9] SMBCLK1
[9] SMBDAT1
[3,16,37] SMBCLK2
[3,16,37] SMBDAT2

SMBCLK0
SMBDAT0
SMBCLK1
SMBDAT1
SMBCLK2
SMBDAT2

SMCLK0/GPB3
SMDAT0/GPB4
SMCLK1/GPC1
SMDAT1/GPC2
SMCLK2/GPF6
SMDAT2/GPF7

LPC/FWH FLASH

FLFRAME/GPG2/LF
FLRST/GPG0/TM
FLAD3/GPG6
FLAD2/SO
FLAD1/SI
FLAD0/SCE
FLCLK

SUS_ON
SUS_ON [42,43,46]
KB_DET# [34]
EC_FLASH_SPI_DO [30]
EC_FLASH_SPI_DIN [30]
EC_FLASH_SPI_CS# [30]
EC_FLASH_SPI_CLK [30]

PS/2

[8] PCH_MELOCK
[47] PS_ID
[34] CLK_TP_SIO
[34] DAT_TP_SIO

PCH_MELOCK R521 *short0402_NC

PS2CLK0/GPF0
PS2DAT0/GPF1
PS2CLK1/GPF2
PS2DAT1/GPF3
PS2CLK2/GPF4
PS2DAT2/GPF5

EGPC

EGAD/GPE1
EGCS/GPE2
EGCLK/GPE3

ECPWROK [10]
ALW_ON [36]
GFX_ON [49]

GPIO

GPH3/ID3
GPH4/ID4
GPH5/ID5
GPH6/ID6
GPG1/ID7

BID2
USB_RIGHT_EN#
BID1
LCD_SIZE_ID0
LCD_SIZE_ID1
USB_RIGHT_EN# [24]

R460 *100K_NC +3.3V_ALW
D21 SDM10K45-7-F

RI1/WUI0/GPD0
RI2/WUI1/GPD1
WUI5/GPE5
ACAV_IN [36,41]
BAT2_LED [36]

RING/PWRFAIL/LPCRST/GPB7
AC_PRESENT [10,16]

PWRSW/GPE4
SYS_PWR_SW# [36]

GINT/GPD5
LCDVCC_TST_EN [22]

CK32K
CK32KE
VCORE
VSS1
VSS3
VSS4
VSS5
VSS6
VSS7
AVCC
AVSS

ITE8502E/KXS-L
lqfp128-16x16-4

ITE8502_XTAL1
ITE8502_XTAL2
ITE8502IX_JX

+3.3V_ALW
R480 100K WRST#
C618 1U/ 10V 603 10
L51 BLM11A05S 603
C606 0.1U/16V 16

+RTC_CELL
C631 0.1U/16V 16

+3.3V_ALW
C585 10U/ 6.3V_6 603 6.3
C636 0.1U/16V 16
C622 0.1U/16V 16
C593 0.1U/16V 16
C637 0.1U/16V 16
SSI DELETE CAP TO VERIFY
Place these caps close to ITE8502.

32KHz Clock.

ITE8502_XTAL2
W1
ITE8502_XTAL1
C634 18P/50V 50
32.768KHZ
C635 18P/50V 50

CLK_33M_KBC
R490 *10_NC
C620 *2.2P_NC 50

ITE8502IX_JX
C624 0.1U/16V 16

+3.3V_ALW
SMBDAT0 SMBCLK0 RP8 2.2KX2
SMBDAT1 SMBCLK1 RP7 2.2KX2
USB_LEFT_EN# R462 *10K_NC

+3.3V_RUN
KB_DET# R511 10K
SERIRQ R495 10K
SMBDAT2 SMBCLK2 RP6 10KX2
ICH_AZ_CODEC_RST0# R524 *10K_NC
LCD_CBL_DET# R520 *10K_NC
PCH_MELOCK R527 *10K_NC
SUS_ON R506 100K
IMVP_VR_ON R493 *100K_NC
V_ID1 R451 10K
V_ID1 for Park

+3.3V_RUN
R468 *short0402_NC
R461 *100K_NC
R459 *390K_NC
Q28 *MMST3904-7-F_NC
Q29 *2N7002W-7-F_NC
C615 *0.1U/10V_NC 10
ICH_AZ_CODEC_RST0#

Discrete / Board ID Straps

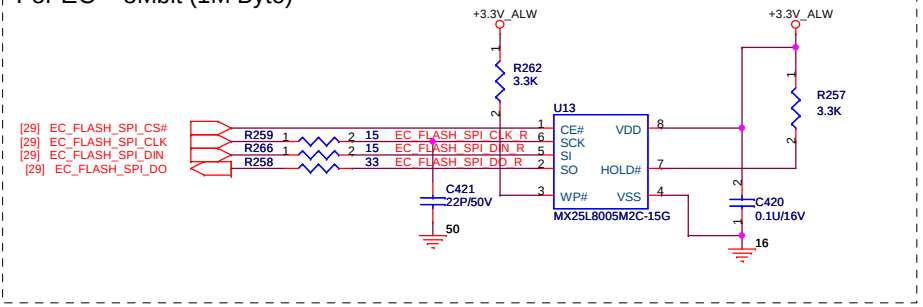
+3.3V_ALW
R497 10K
R510 10K
R512 *10K_NC
R513 10K
R514 10K
R496 *10K_NC
R505 *10K_NC
R507 10K
R508 *10K_NC
R509 10K_NC
USB_RIGHT_EN#
BID1
LCD_SIZE_ID0
LCD_SIZE_ID1
BID2
UMA

LCD_SIZE_ID0	LCD_SIZE_ID0	LCD_SIZE	BID1	USB_RIGHT_EN#	Build
0	0	13.3"	0	0	SSI (X00)
0	1	14"	0	1	PT (X01)
1	0	17"	1	0	ST (X02)
			1	1	OT (A00)
			0	0	RAMP(A00)

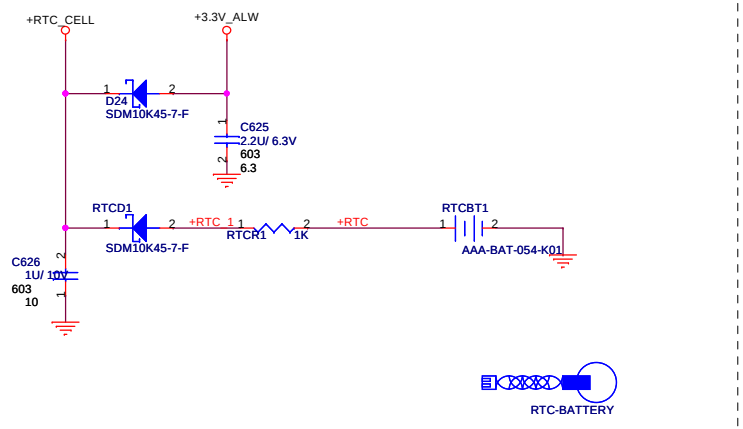
Quanta Computer Inc.
PROJECT : UM7 DIS

Size	Document Number	Rev
	SIO ITE8502	3A
Date: Wednesday, February 03, 2010	Sheet 29 of 52	

For EC 8Mbit (1M Byte)



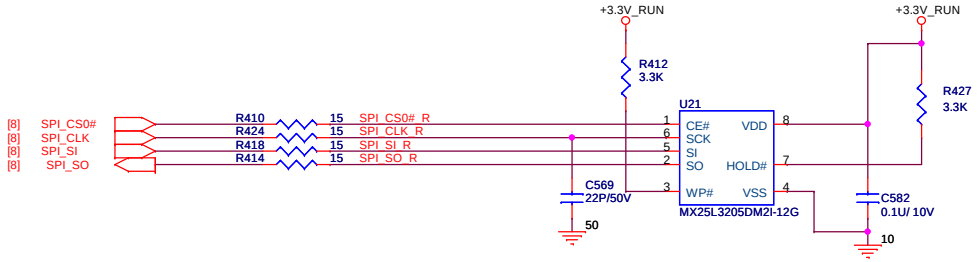
RTC BATTERY



For PCH

32Mbit (4M Byte)

2nd source:AKE39ZP0N00



Quanta Computer Inc.		
PROJECT : UM7 DIS		
Size	Document Number: FLASH/RTC	Rev: 3A
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Quanta Computer Inc.

PROJECT : UM7 DIS

Size	Document Number	Rev
	MINI-Card WWAN	3A

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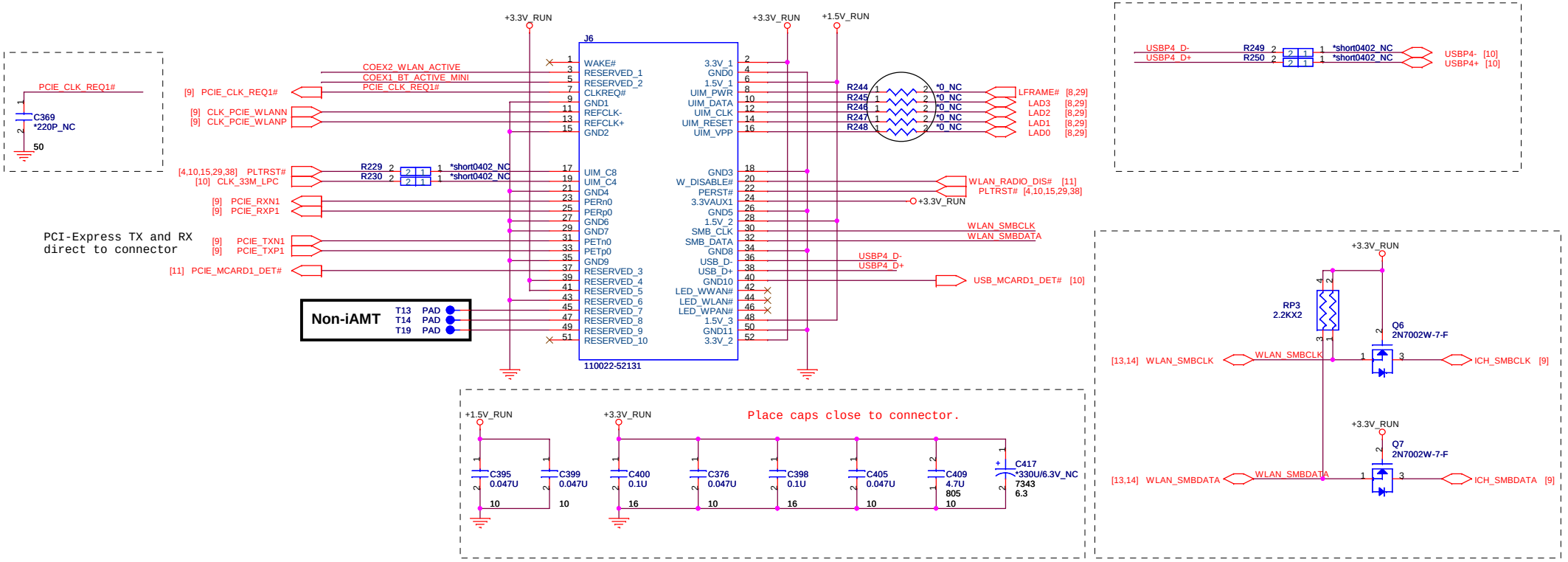
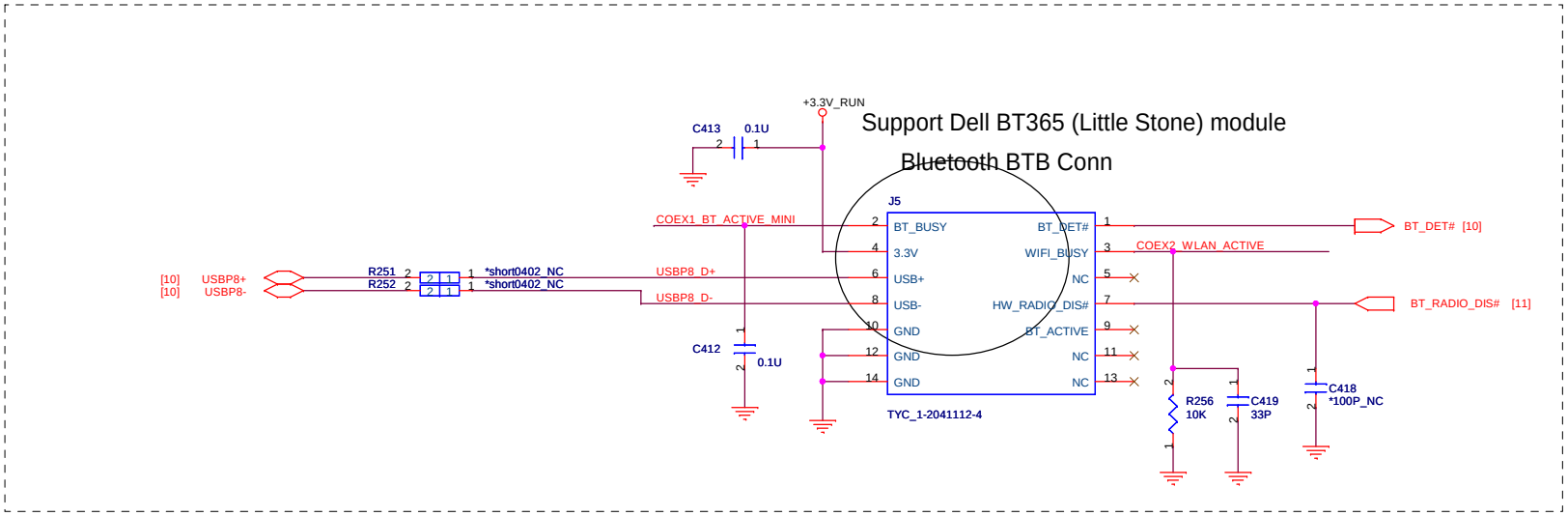
MiniCard WLAN connector



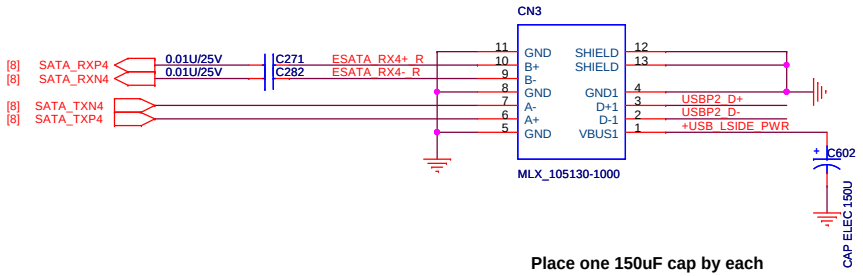


Quanta Computer Inc.

PROJECT : UM7 DIS

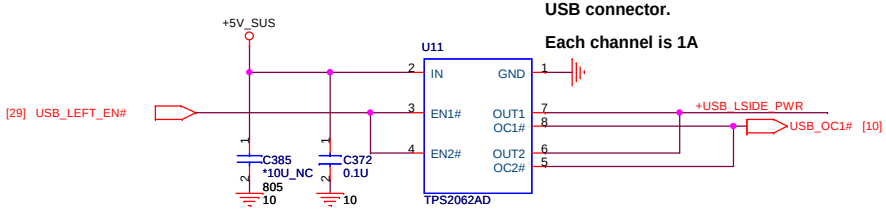
Size	Document Number	Rev
	MINI-Card WLAN / BT	3A
Date: Wednesday, February 03, 2010	Sheet 32 of 52	

USB and eSATA Conn.

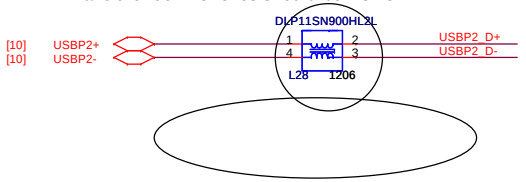


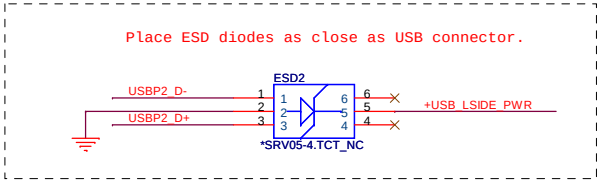
Place one 150uF cap by each USB connector.

Each channel is 1A

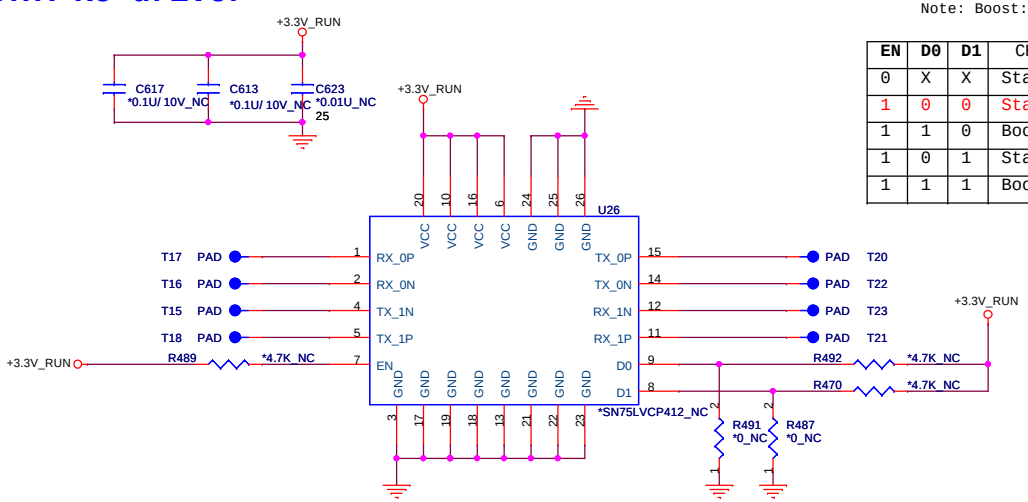


Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.





E-SATA Re-driver



Note: Boost:5dB, Standard SATA:0dB

EN	D0	D1	CH : 0	CH : 1
0	X	X	Standby	Standby
1	0	0	Standard SATA	Standard SATA
1	1	0	Boost	Standard SATA
1	0	1	Standard SATA	Boost
1	1	1	Boost	Boost

Quanta Computer Inc.

PROJECT : UM7 DIS

Size	Document Number	Rev
	eSATA & Right USB	3A

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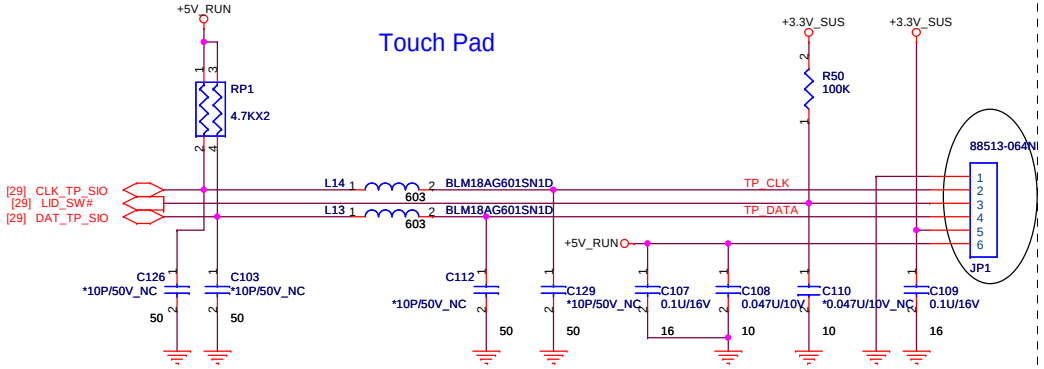
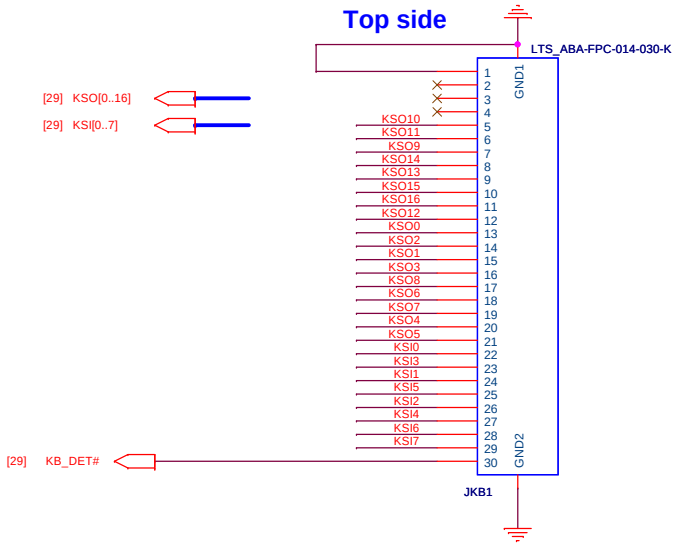
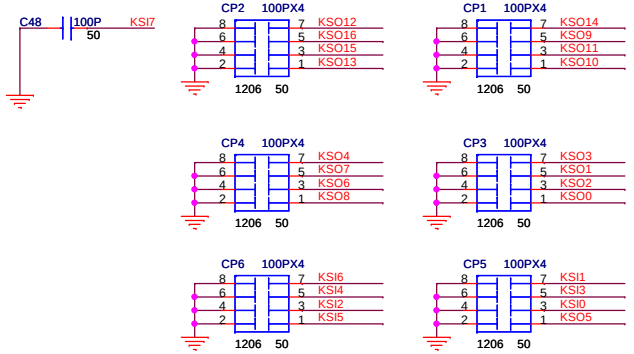
Touch Pad



KEYBOARD CONNECTOR

Top side

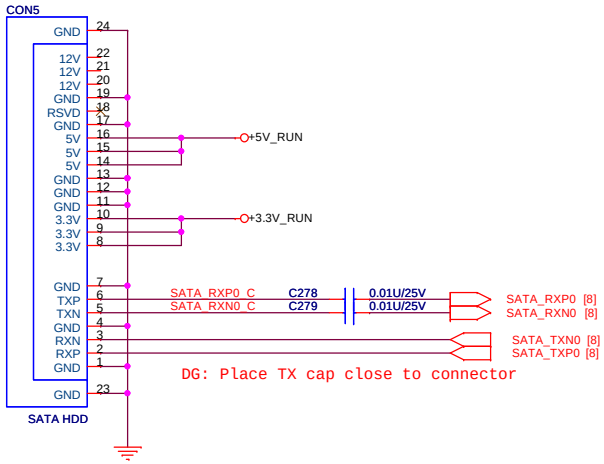


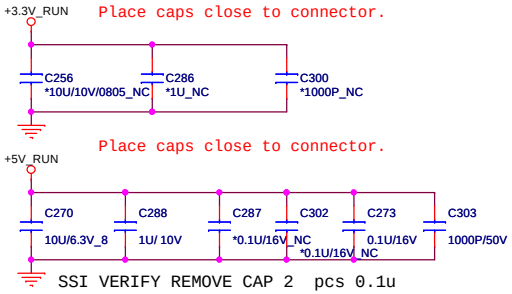


100P CAPS CLOSE TO JKB1

Quanta Computer Inc.		
PROJECT : UM7 DIS		
Size	Document Number: TOUCH PAD, KB	Rev: 3A
Date: Wednesday, February 03, 2010	Sheet 34 of 52	

SATA Connector.





Quanta Computer Inc.

PROJECT : UM7 DIS

Size	Document Number	Rev
	SATA (HDD&CD_ROM)	3A

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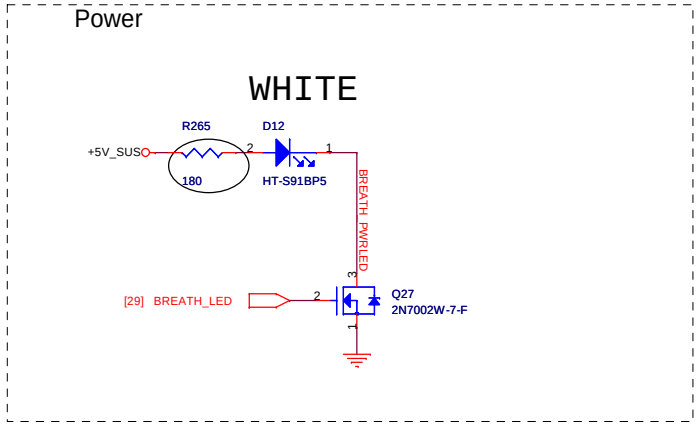
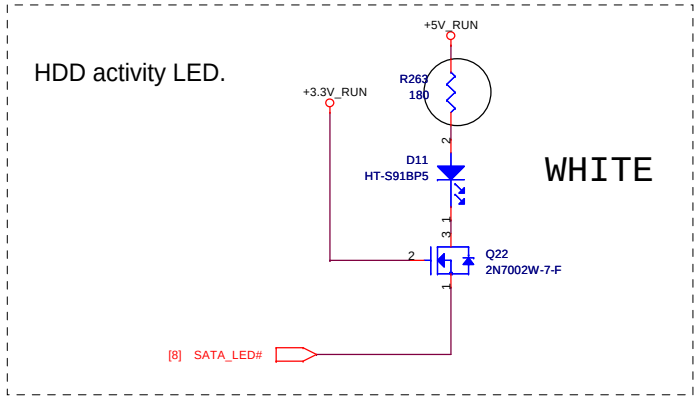
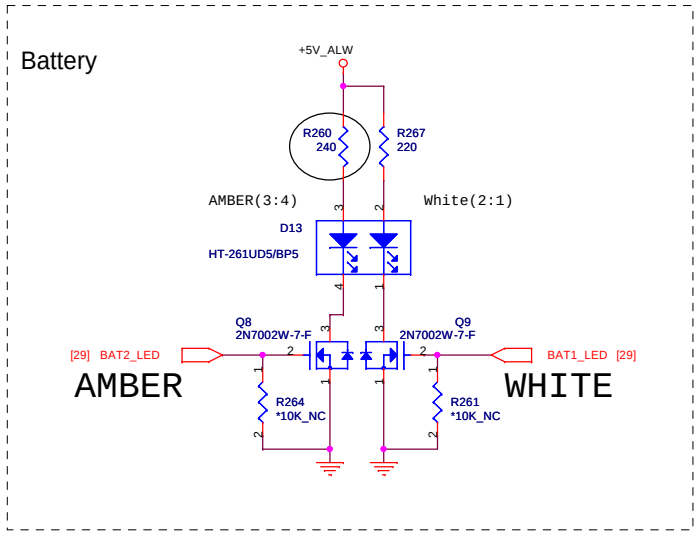
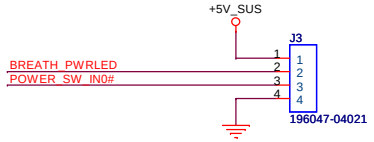
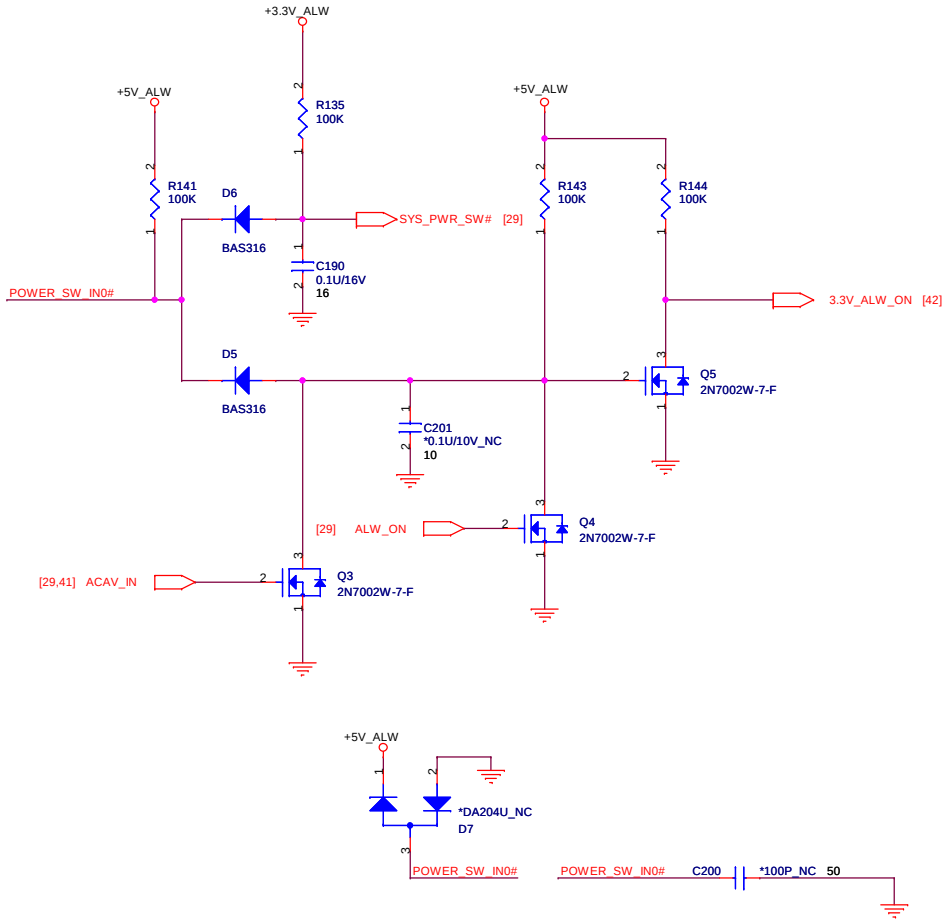








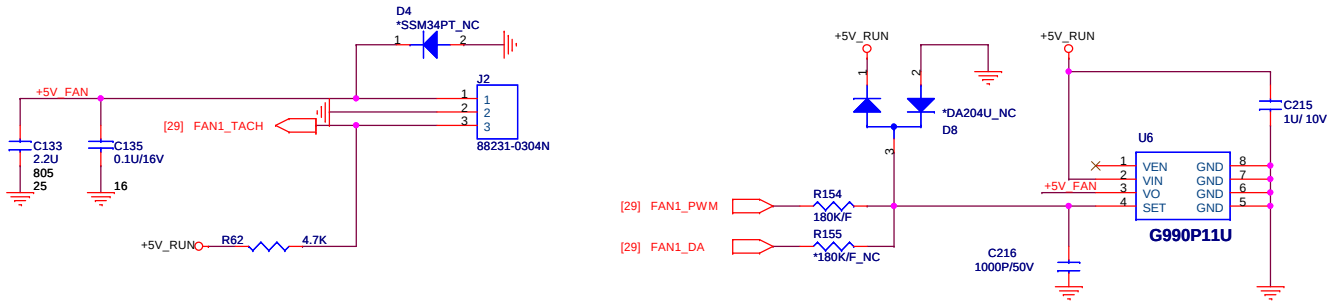


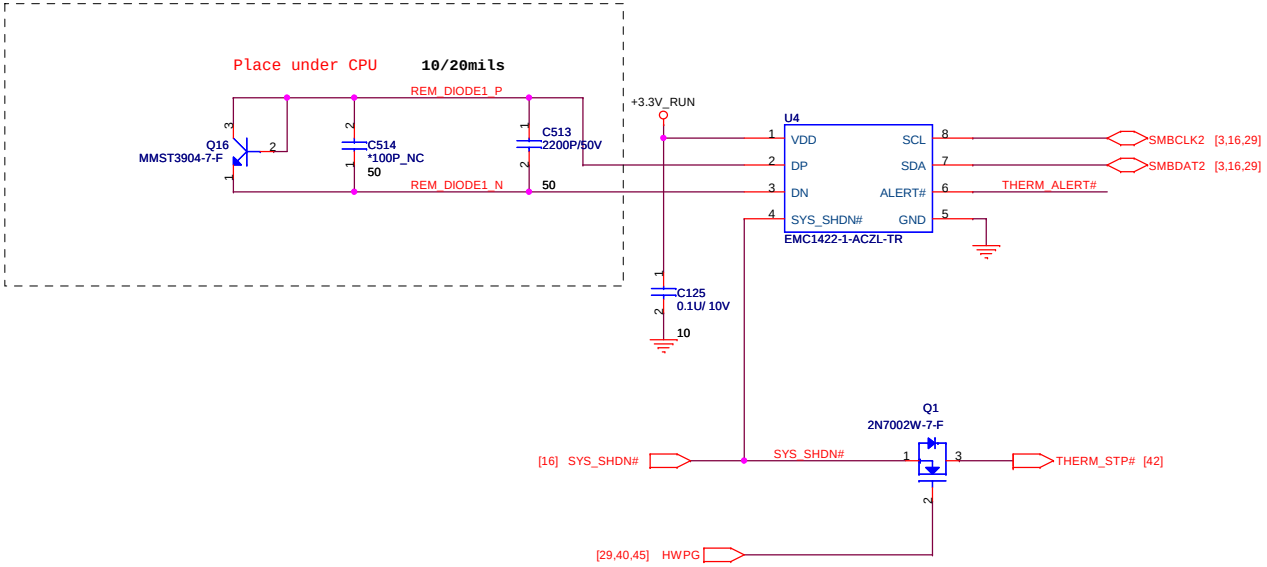
Quanta Computer Inc.

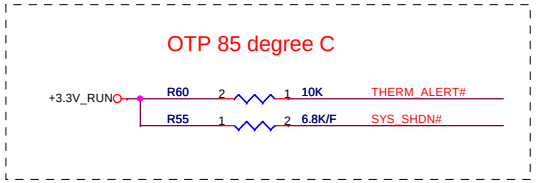
PROJECT : UM7 DIS

Size	Document Number	Rev
	SWITCH, LED	3A
Date: Wednesday, February 03, 2010	Sheet 36 of 52	

FAN CONTROL







Quanta Computer Inc.

PROJECT : UM7 DIS

Size	Document Number	Rev
	FAN & THERMAL	3A

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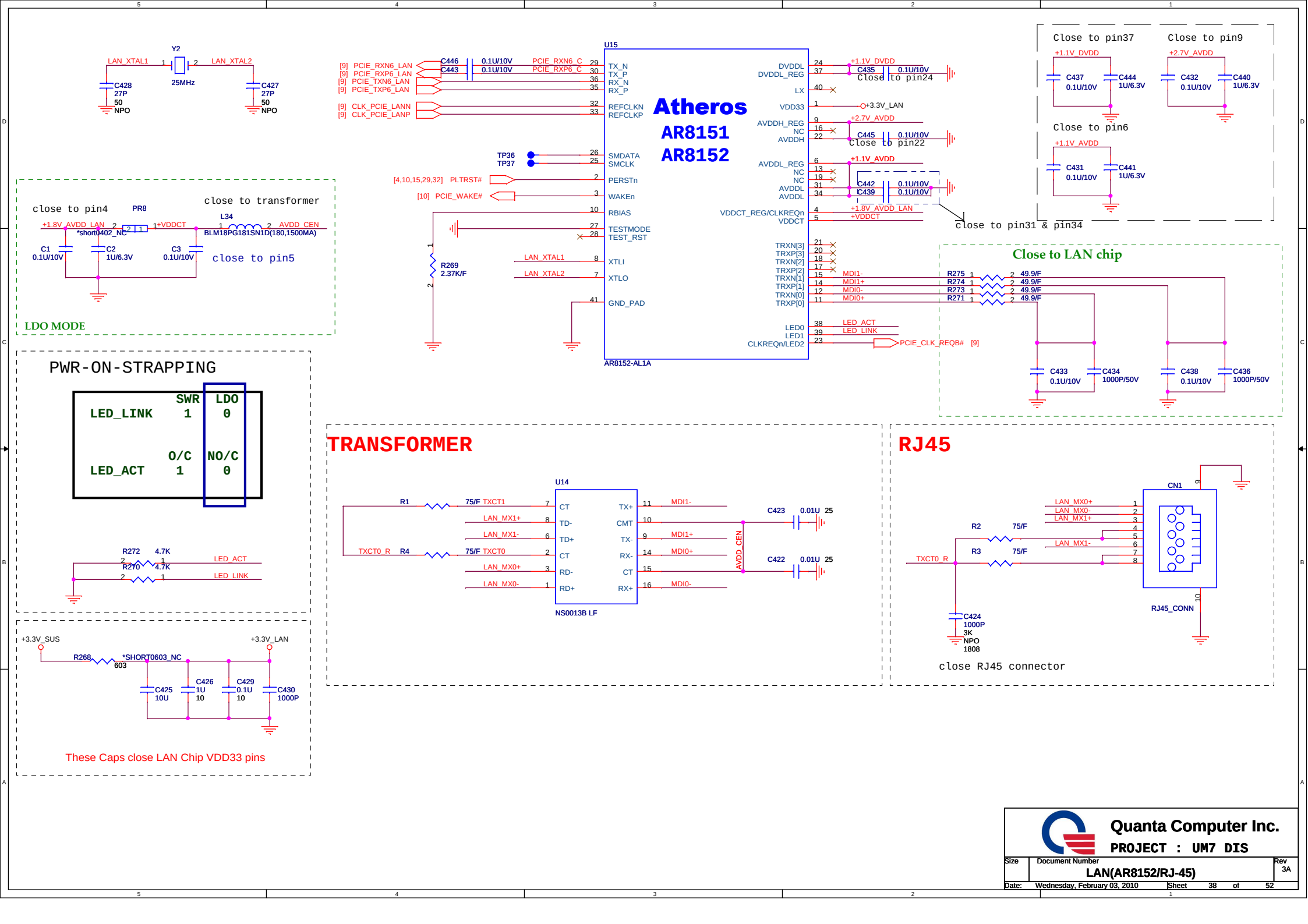
Y2
LAN_XTAL1
LAN_XTAL2
25MHz
C428 27P 50 NPO
C427 27P 50 NPO
U15
Atheros
AR8151
AR8152
AR8152-AL1A
TX_N
TX_P
RX_N
RX_P
REFCLKN
REFCLKP
SMDATA
SMCLK
PERSTn
WAKEn
RBIAS
TESTMODE
TEST_RST
XTLI
XTLO
GND_PAD
DVDDL
DVDDL_REG
LX
VDD33
AVDDH_REG
NC
AVDDH
AVDDL_REG
AVDDL
VDDCT_REG/CLKREQn
VDDCT
TRXN[3]
TRXP[3]
TRXN[2]
TRXP[2]
TRXN[1]
TRXP[1]
TRXN[0]
TRXP[0]
LED0
LED1
CLKREQn/LED2
[9] PCIE_RXN6_LAN
[9] PCIE_RXP6_LAN
[9] PCIE_TXN6_LAN
[9] PCIE_TXP6_LAN
[9] CLK_PCIE_LANN
[9] CLK_PCIE_LANP
PCIE_RXN6_C
PCIE_RXP6_C
C446 0.1U/10V
C443 0.1U/10V
TP36
TP37
[4,10,15,29,32] PLTRST#
[10] PCIE_WAKE#
R269 2.37K/F
+1.1V_DVDD
+3.3V_LAN
+2.7V_AVDD
+1.1V_AVDD
+1.8V_AVDD_LAN
+VDDCT
C435 0.1U/10V
C445 0.1U/10V
C442 0.1U/10V
C439 0.1U/10V
Close to pin24
Close to pin22
Close to pin31 & pin34
MDI1-
MDI1+
MDI0-
MDI0+
LED_ACT
LED_LINK
PCIE_CLK_REQB# [9]
R275 49.9/F
R274 49.9/F
R273 49.9/F
R271 49.9/F
C433 0.1U/10V
C434 1000P/50V
C438 0.1U/10V
C436 1000P/50V
Close to LAN chip
Close to pin37
Close to pin9
Close to pin6
C437 0.1U/10V
C444 1U/6.3V
C432 0.1U/10V
C440 1U/6.3V
C431 0.1U/10V
C441 1U/6.3V
close to pin4
PR8
close to transformer
+1.8V_AVDD_LAN
*short0402_NC
+VDDCT
L34
BLM18PG181SN1D(180,1500MA)
AVDD_CEN
C1 0.1U/10V
C2 1U/6.3V
C3 0.1U/10V
close to pin5
LDO MODE
PWR-ON-STRAPPING
SWR LDO
LED_LINK 1 0
O/C NO/C
LED_ACT 1 0
R272 4.7K
R270 4.7K
LED_ACT
LED_LINK
+3.3V_SUS
+3.3V_LAN
R268 603
*SHORT0603_NC
C425 10U
C426 1U 10
C429 0.1U 10
C430 1000P
These Caps close LAN Chip VDD33 pins
TRANSFORMER
U14
NS0013B LF
R1
R4
75/F TXCT1
75/F TXCT0
TXCT0_R
CT
TD-
TD+
RD-
RD+
TX+
CMT
TX-
RX-
RX+
AVDD_CEN
C423 0.01U 25
C422 0.01U 25
LAN_MX1+
LAN_MX1-
LAN_MX0+
LAN_MX0-
RJ45
CN1
RJ45_CONN
R2 75/F
R3 75/F
C424 1000P 3K NPO 1808
close RJ45 connector
Quanta Computer Inc.
PROJECT : UM7 DIS
Size
Document Number
LAN(AR8152/RJ-45)
Rev 3A
Date: Wednesday, February 03, 2010
Sheet 38 of 52

Quanta Computer Inc.

PROJECT : UM7 DIS

Size	Document Number	Rev
	BTB CONN	3A

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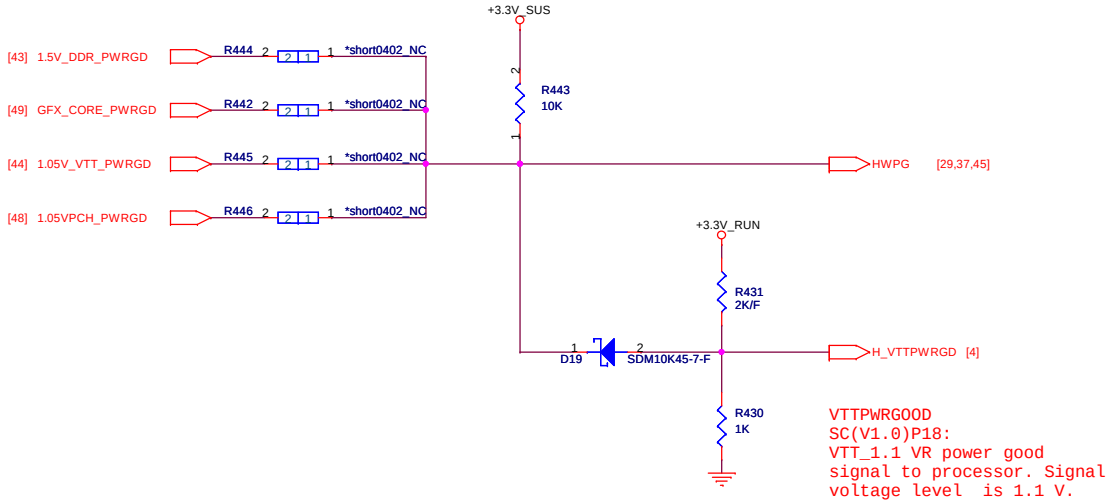

VTTPWRGOOD
SC(V1.0)P18:
VTT_1.1 VR power good
signal to processor. Signal
voltage level is 1.1 V.

Quanta Computer Inc.		
PROJECT : UM7 DIS		
Size	Document Number: System Reset Circuit	Rev: 3A
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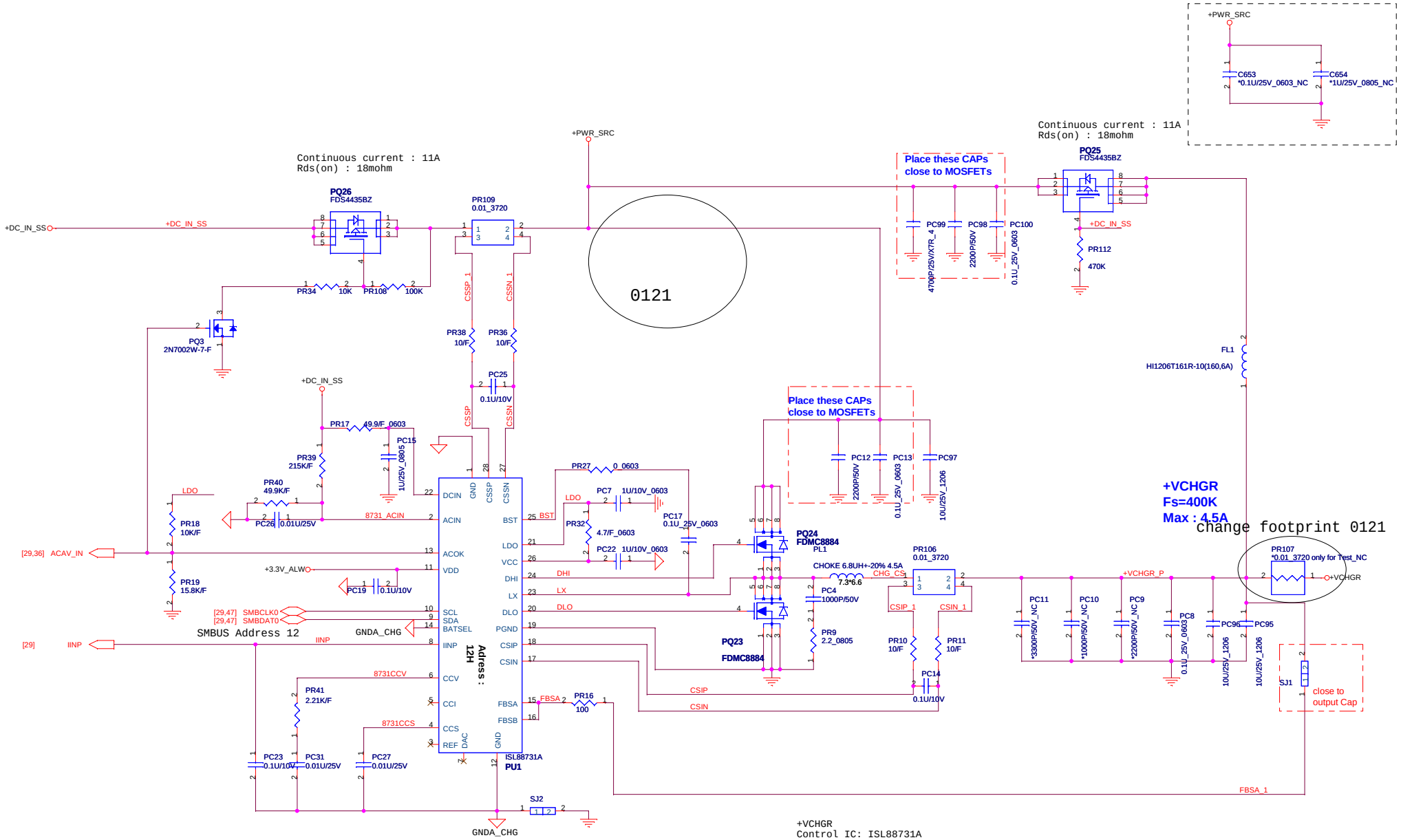

QUANTA COMPUTER

Title	Charger (ISL88731)	
Size	Document Number UM7 Dis	Rev 3A
Date: Wednesday, February 03, 2010	Sheet 41 of 52	

+5V_SUS
Fs=200K
TDC : 4.915A
OCP : 6.881A

+3.3V_ALW
Fs=250K
TDC : 4.477A
OCP : 6.268A

Place these CAPs close to MOSFETs

Place these CAPs close to MOSFETs

PJP4 POWER_JP
PJP5 POWER_JP
+PWR_SRC
+3V5V_PWR_SRC
PC64 10U/25V_1206
PC136 0.1U/25V_0603
PC135 2200P/50V
0121
0127
PR132 *short_NC
PD10 *UDZSTE-175.6B_NC
PR133 390K
PR135 150K/F_0603
ISL6237_ONLOD
PR134 *10_0603_NC
+5V_ALW
PC146 4.7U/6.3V_0603
PC145 0.1U/25V_0603
PC144 *1U/6.3V_NC
PR140 *short_NC
PC141 1U/6.3V
PC143 0.1U/10V
PR139 *0_NC
PC139 0.1U/25V_0603
PC140 2200P/50V
PC65 10U/25V_1206
+5V_SUS
PR149 *0.01_3720 only for Test_NC
PQ14 FDS8884
PL7 3.8UH,30%8A(TPRH10D45F-3R8Y-F02)
10*10.1
PC68 1000P/50V_4
+5V_DH
+5V_LX
+5V_DL
PR142 158K/F
POK
+5V_EN1
+5V_SUSP
PU7 RT8206BGQW
PAD PAD PAD PAD BYP OUT1 FB1 ILIM1 PGOOD1 ON1 DH1 LX1 PAD PAD PAD PAD
LDOREFIN LDO VIN RTC ONLDO VCC TON REF
REFIN2 ILIM2 OUT2 SKIP# PGOOD2 ON2 DH2 LX2
BST1 DL1 VDD SECFB AGND PGND DL2 BST2
PR143 162K/F
PR145 *short_NC
+3.3V_EN2
+3.3V_DH
PQ13 FDS8884
PL8 3.8UH,30%8A(TPRH10D45F-3R8Y-F02)
10*10.1
+3.3V_LX
+3.3V_ALWP
PC71 1000P/50V_4
PR92 2.2 805
SJ14
close to output Cap
PC151 0.1U/25V_0603
PC152 330U/ESR=17m
PR138 *0.01_3720 only for Test_NC
11/19
PC150 330U/ESR=17m
PC149 0.1U/25V_0603
SJ13
SJ12
PR141 *0_NC
close to output Cap
PR79 2.2 805
PQ15 FDS6690AS_NL
PR80 *short_NC
0127
PC155 0.1U/25V_0603
PC156 0.1U/25V_0603
PR154 1_603
PR155 603_1
+3.3V_DL
PQ16 FDS6690AS_NL
SJ6
PC158 1U/6.3V

+3.3V_ALW
Control IC: RT8206B
H/S MOSFET: FDS8884(Fairchild), Qg=13nC, Rds(on)=30mohm, PD:2.5W
L/S MOSFET: FDS6690AS_NL(Fairchild), Qg=23nC, Rds(on)=15mohm, PD:2.5W
Inductor: 3 3.8UH,30%8A(TPRH10D45F-3R8Y-F02)(TTA), DCR=21mohm
Output Cap: 1*330U,6.3V(20%ESR17,6.3*5.8)

+5V_ALW
Control IC: RT8206B
H/S MOSFET: FDS8884(Fairchild), Qg=13nC, Rds(on)=30mohm, PD:2.5W
L/S MOSFET: FDS6690AS_NL(Fairchild), Qg=23nC, Rds(on)=15mohm, PD:2.5W
Inductor: 3.8UH,30%8A(TPRH10D45F-3R8Y-F02)(TTA), DCR=21mohm
Output Cap: 1*330U,6.3V(20%ESR17,6.3*5.8)

Ton	GND	VREF2 or Float	5V
Channel1 Fs	400 kHz	300 kHz	200 kHz
Channel2 Fs	500 kHz	375 kHz	250 kHz

PC87 0.1U/10V
BAT54S-7-F PD7
PC79 0.1U/25V_0603
PC88 0.1U/25V_0603
PD8 BAT54S-7-F
PC80 0.1U/25V_0603
PC89 0.1U/25V_0603
+15V_ALW
PQ20 DDTA114YUA-7-F
47K 10K
+15V_ALWP
PQ18 2N7002W-7-F
PR146 100K
POK
PR148 39K/F
PR98 200K
[29,43,46] SUS_ON
[37] THERM_STP#
[36] 3.3V_ALW_ON
[4] PM_THRMTRIP#
PR87 *short_NC
PR89 *short_NC
PR150 *0_NC
0127

C655 *0.1U/25V_0603_NC
C656 *1U/25V_0805_NC
C660 *0.1U/25V_0603_NC
C661 *1U/25V_0805_NC

QUANTA COMPUTER

Title	3.3V_ALW / 5V_ALW(RT8206B)	
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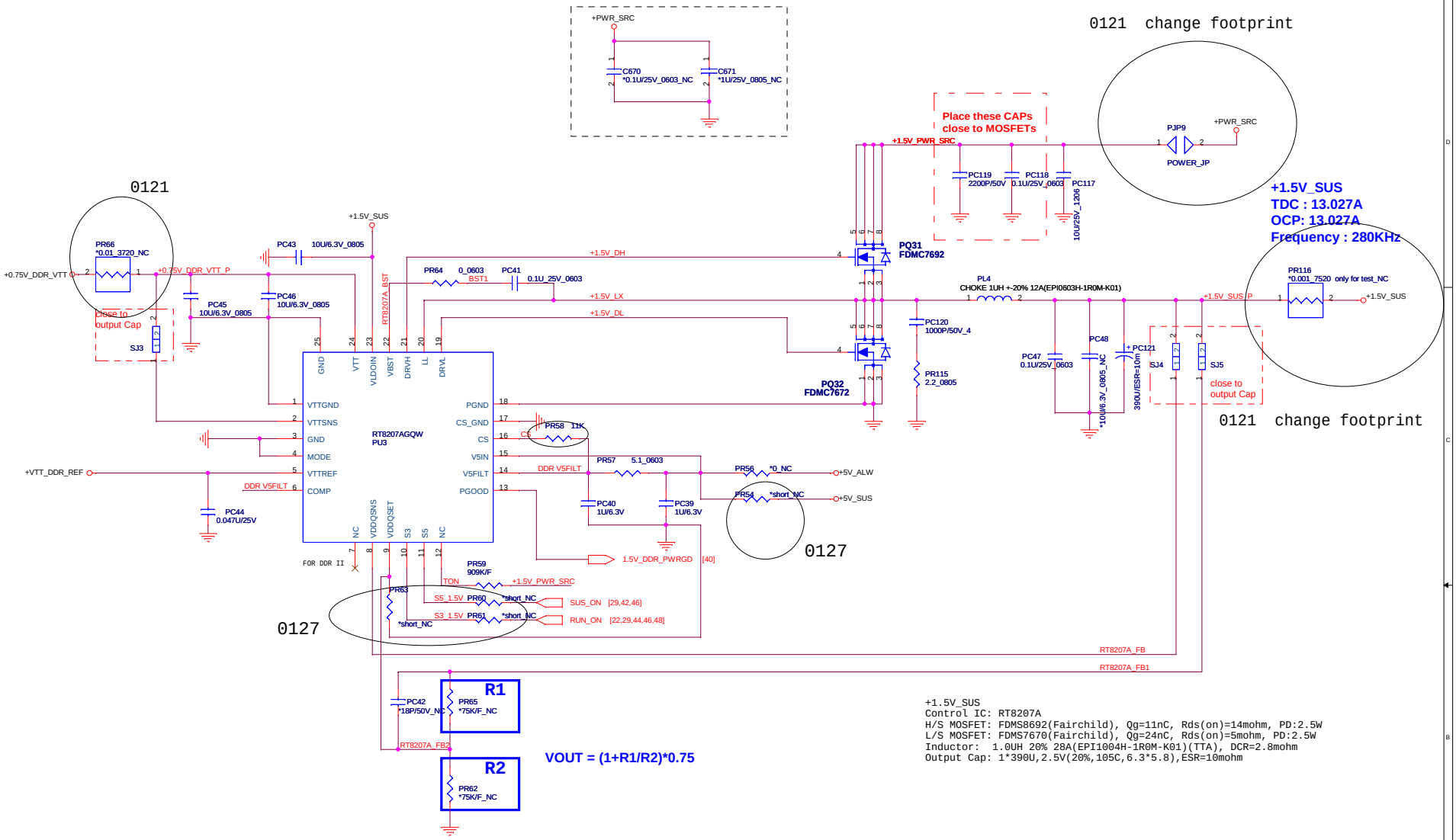

+1.5V_SUS
Control IC: RT8207A
H/S MOSFET: FDMS8692(Fairchild), Qg=11nC, Rds(on)=14mohm, PD:2.5W
L/S MOSFET: FDMS7670(Fairchild), Qg=24nC, Rds(on)=5mohm, PD:2.5W
Inductor: 1.0UH 20% 28A(EPI1004H-1R0M-K01)(TTA), DCR=2.8mohm
Output Cap: 1*390U,2.5V(20%,105C,6.3*5.8),ESR=10mohm

VDDQ and VTT discharge control

MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

VDDQ output voltage selection

VDDQSET	VDDQ(V)	VTTREF and VTT	NOTE
GND	1.5V	VDDQSNS/2	DDR3
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)

Title	DDR3 +1.5V_SUS(RT8207AGQW)		
Size	Document Number UM7 Dis		Rev 3A
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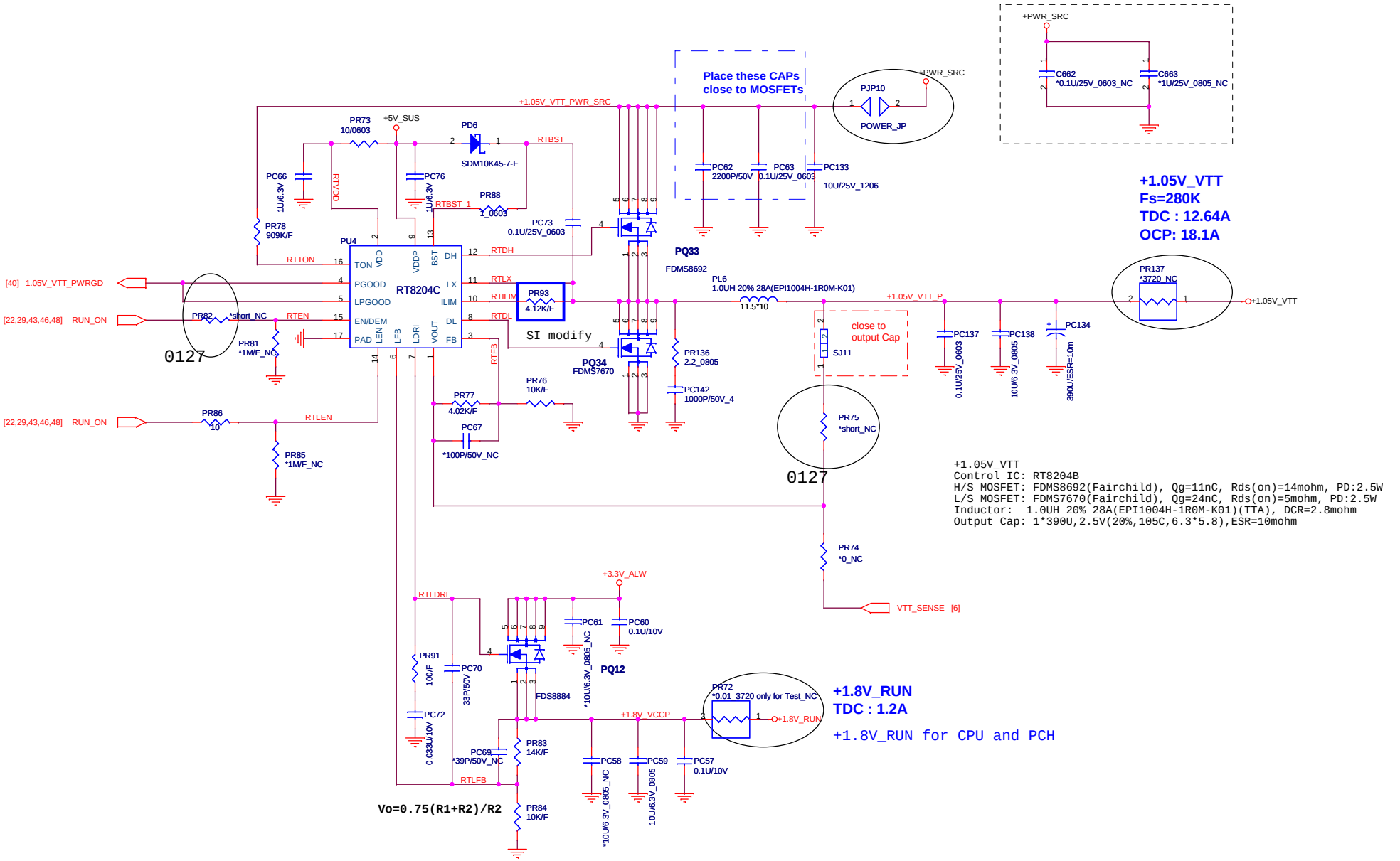

Title	+1.05V_VTT(RT8204B)	
Size	Document Number UM7 Dis	Rev 3A
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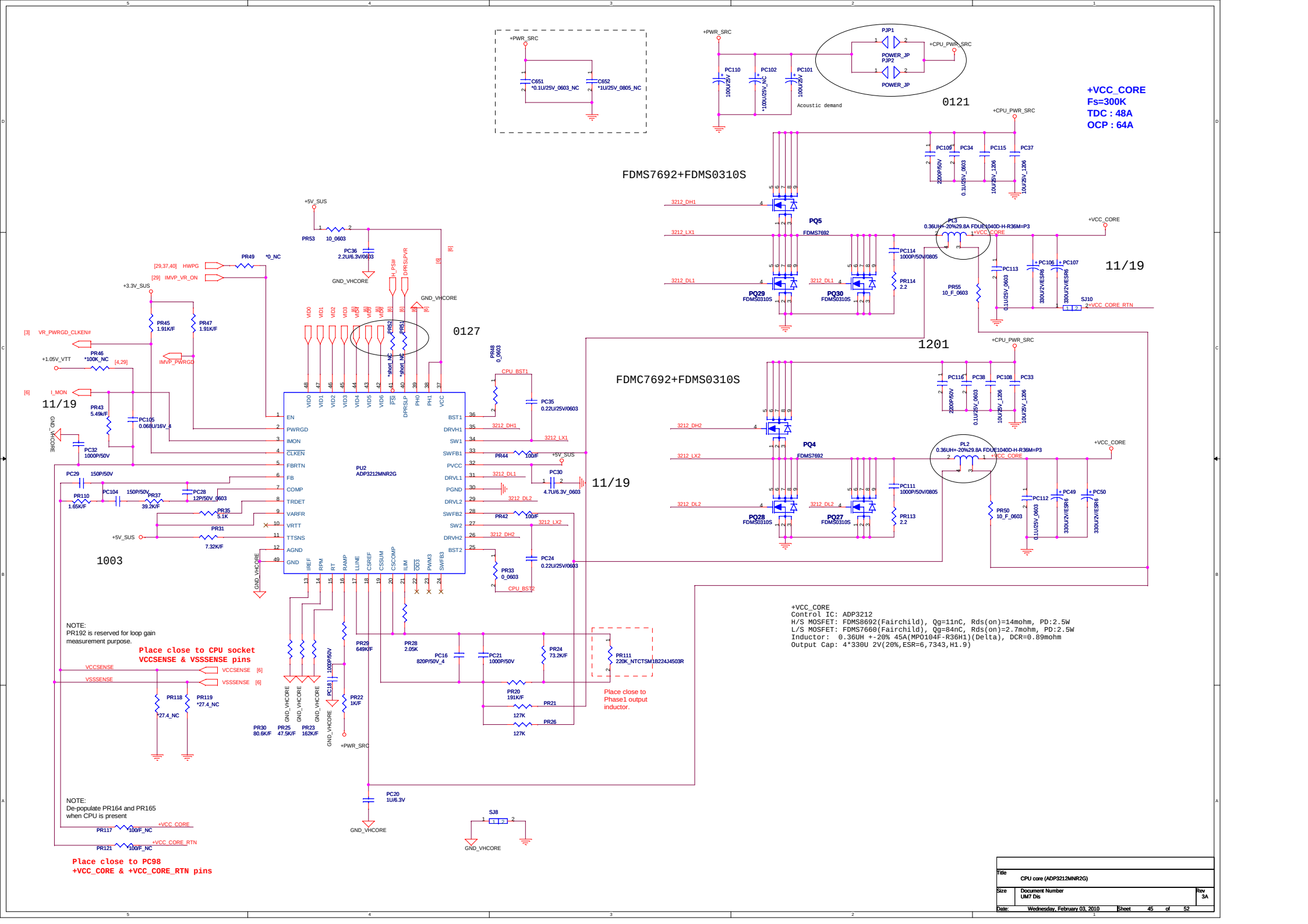
+VCC_CORE
Fs=300K
TDC : 48A
OCP : 64A
FDMS7692+FDMS0310S
FDMC7692+FDMS0310S
0121
0127
1003
11/19
1201
PU2
ADP3212MNR2G
PQ5
PQ4
PQ29
PQ30
PQ28
PQ27
PL3
PL2
0.36UH+-20%29.8A FDUE1040D-H-R36M=P3
+VCC_CORE Control IC: ADP3212
H/S MOSFET: FDMS8692(Fairchild), Qg=11nC, Rds(on)=14mohm, PD:2.5W
L/S MOSFET: FDMS7660(Fairchild), Qg=84nC, Rds(on)=2.7mohm, PD:2.5W
Inductor: 0.36UH +-20% 45A(MPO104F-R36H1)(Delta), DCR=0.89mohm
Output Cap: 4*330U 2V(20%,ESR=6,7343,H1.9)
NOTE:
PR192 is reserved for loop gain measurement purpose.
Place close to CPU socket
VCCSENSE & VSSSENSE pins
NOTE:
De-populate PR164 and PR165 when CPU is present
Place close to PC98
+VCC_CORE & +VCC_CORE_RTN pins
Place close to Phase1 output inductor.
Acoustic demand
Title
CPU core (ADP3212MNR2G)
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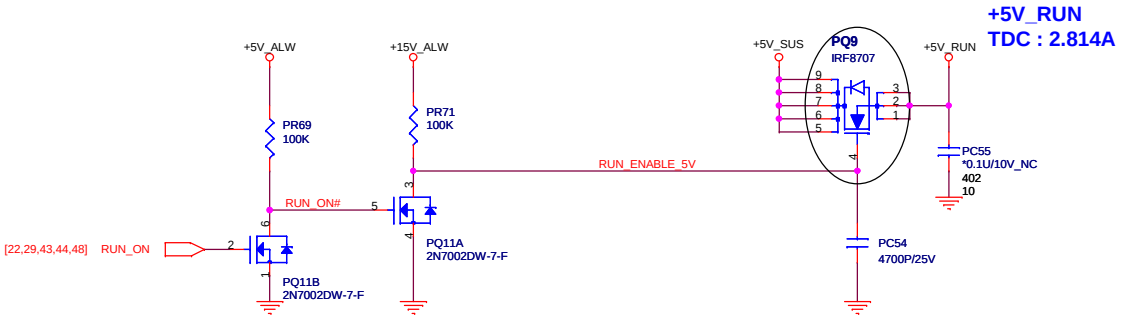
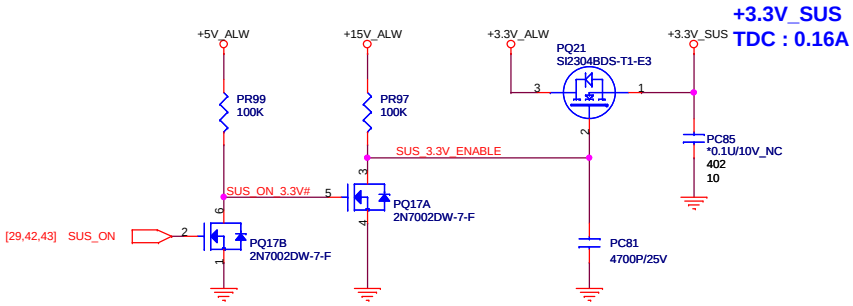
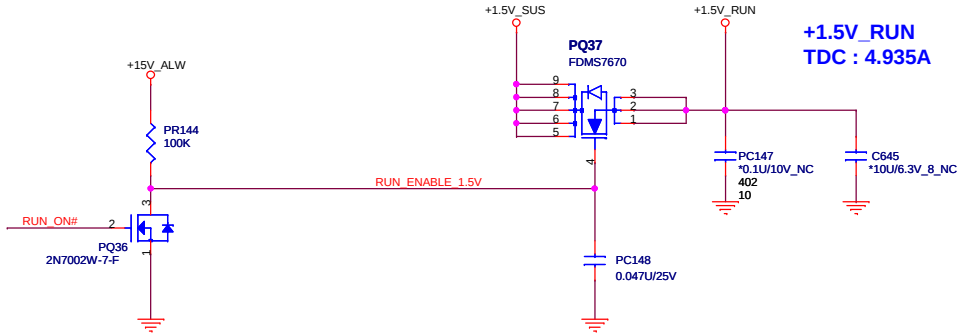
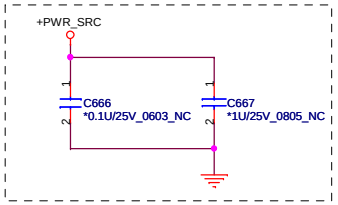
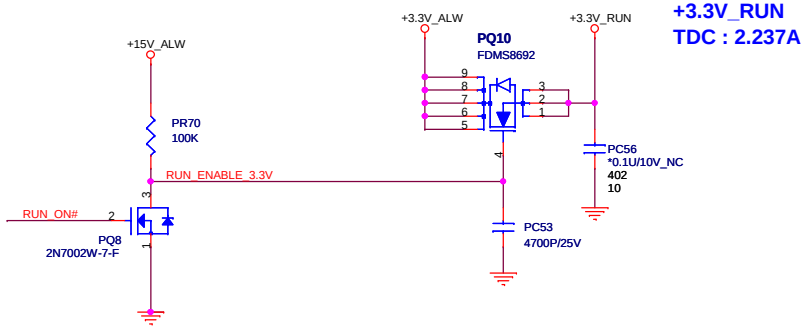


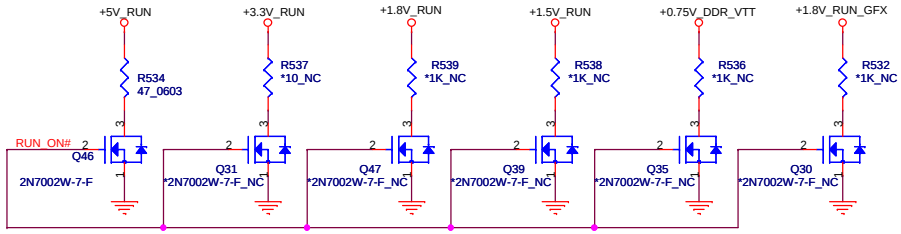


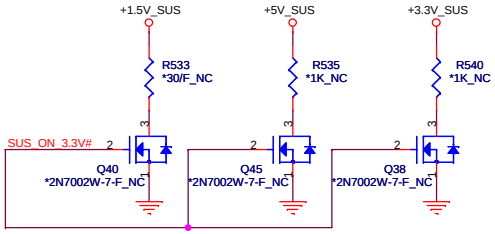






Reserve discharge path





QUANTA COMPUTER

Title	RUN / SUS POWER SW	
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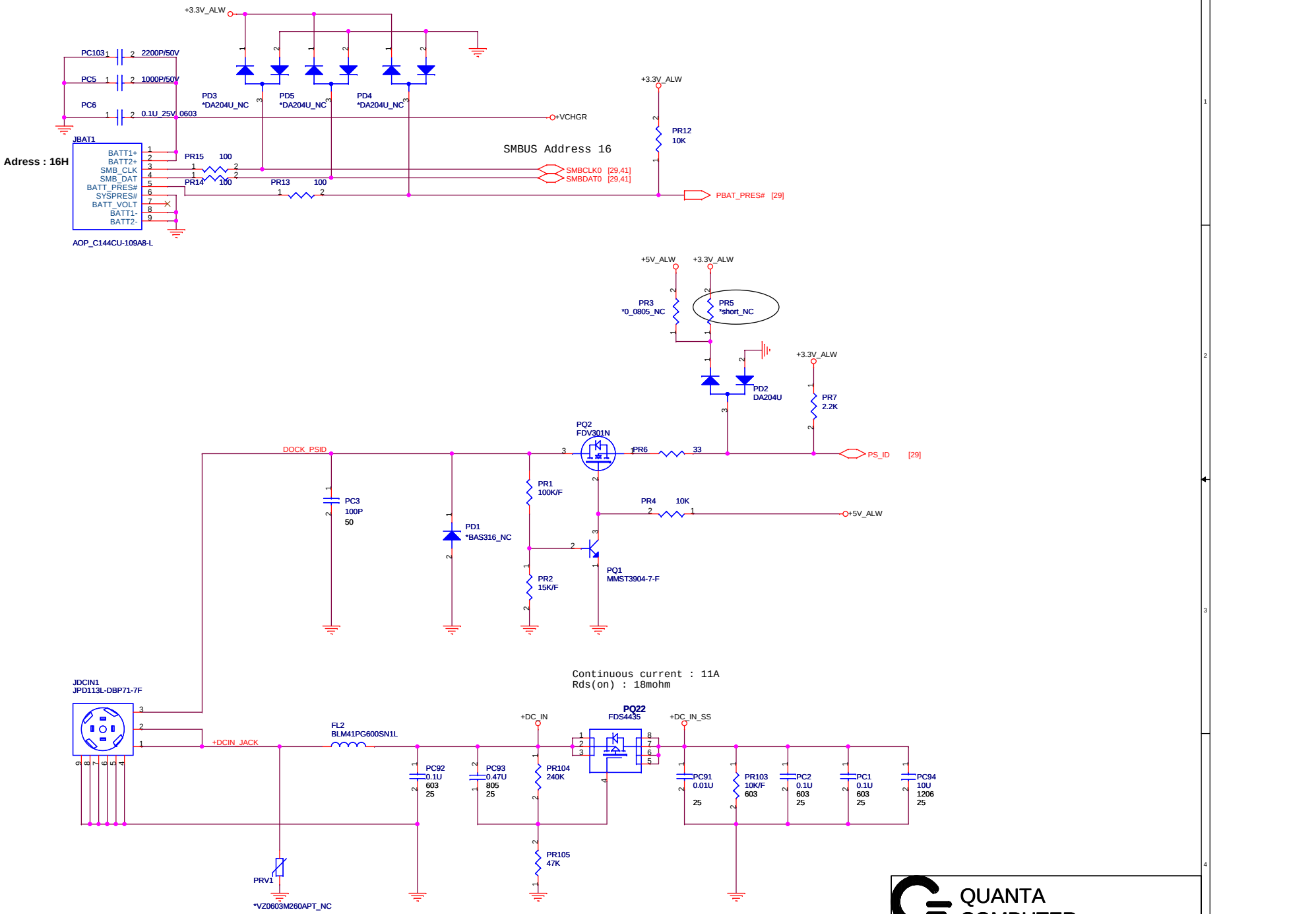

QUANTA COMPUTER

Title	DCIN,BATT CONNECTOR	
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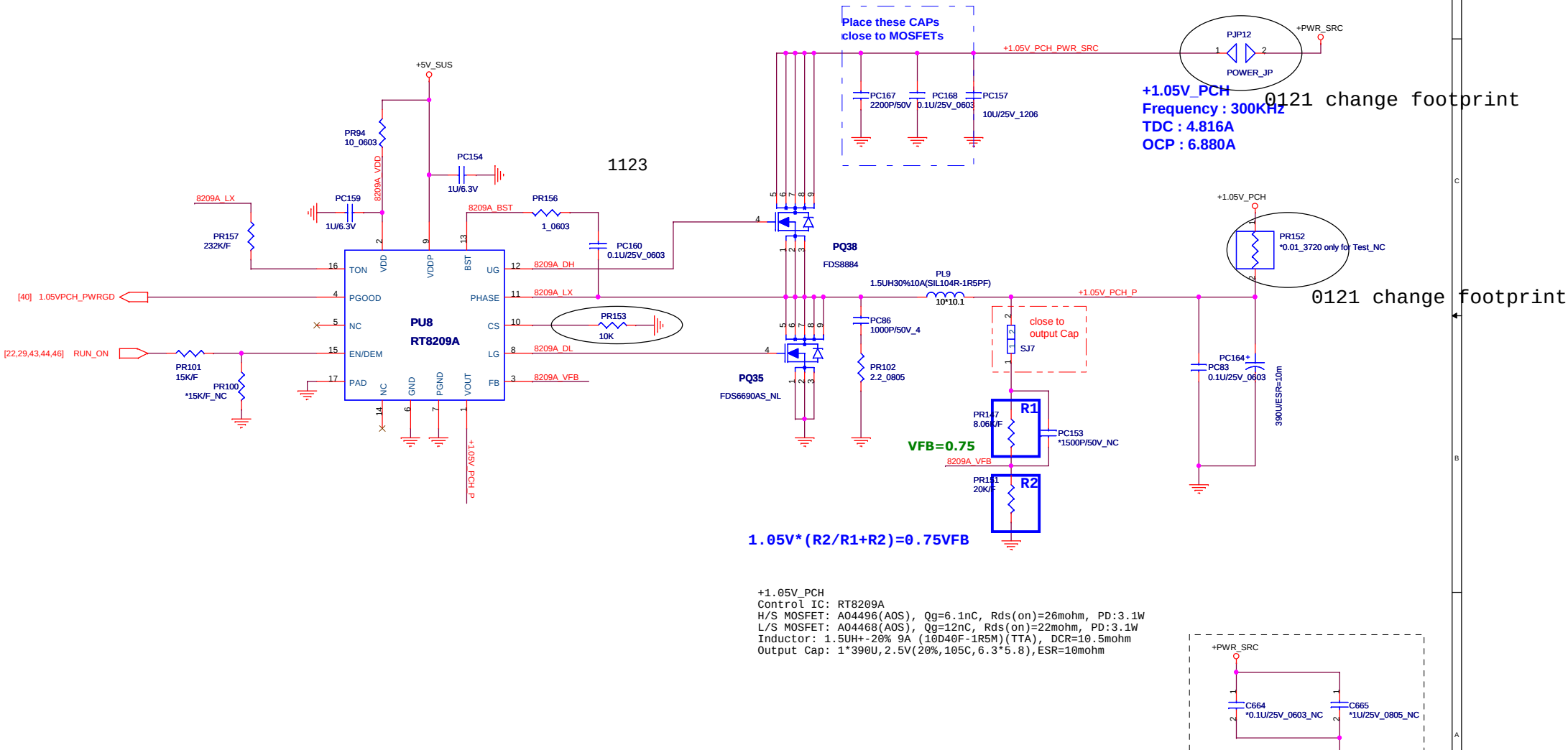
Place these CAPs close to MOSFETs
+1.05V_PCH_PWR_SRC
PJP12
POWER_JP
+PWR_SRC
PC167 2200P/50V
PC168 0.1U/25V_0603
PC157 10U/25V_1206
+1.05V_PCH
Frequency : 300KHz
TDC : 4.816A
OCP : 6.880A
0121 change footprint
1123
+5V_SUS
PR94 10_0603
8209A_VDD
PC154 1U/6.3V
PC159 1U/6.3V
8209A_LX
PR157 232K/F
8209A_BST
PR156 1_0603
PC160 0.1U/25V_0603
PU8
RT8209A
TON
VDD
VDDP
BST
UG
PGOOD
PHASE
NC
CS
EN/DEM
LG
PAD
GND
PGND
VOUT
FB
8209A_DH
8209A_LX
8209A_DL
8209A_VFB
[40] 1.05VPCH_PWRGD
[22,29,43,44,46] RUN_ON
PR101 15K/F
PR100 *15K/F_NC
PR153 10K
PQ38
FDS8884
PQ35
FDS6690AS_NL
PL9
1.5UH30%10A(SIL104R-1R5PF)
10*10.1
PC86 1000P/50V_4
PR102 2.2_0805
+1.05V_PCH_P
close to output Cap
SJ7
PR147 8.06K/F
R1
PC153 *1500P/50V_NC
VFB=0.75
8209A_VFB
PR151 20K/F
R2
1.05V*(R2/R1+R2)=0.75VFB
+1.05V_PCH
PR152 *0.01_3720 only for Test_NC
0121 change footprint
PC164+
PC83 0.1U/25V_0603
390UVESR=10m
+1.05V_PCH
Control IC: RT8209A
H/S MOSFET: AO4496(AOS), Qg=6.1nC, Rds(on)=26mohm, PD:3.1W
L/S MOSFET: AO4468(AOS), Qg=12nC, Rds(on)=22mohm, PD:3.1W
Inductor: 1.5UH+-20% 9A (10D40F-1R5M)(TTA), DCR=10.5mohm
Output Cap: 1*390U,2.5V(20%,105C,6.3*5.8),ESR=10mohm
+PWR_SRC
C664 *0.1U/25V_0603_NC
C665 *1U/25V_0805_NC
Title
+1.05V_PCH(RT8209A)
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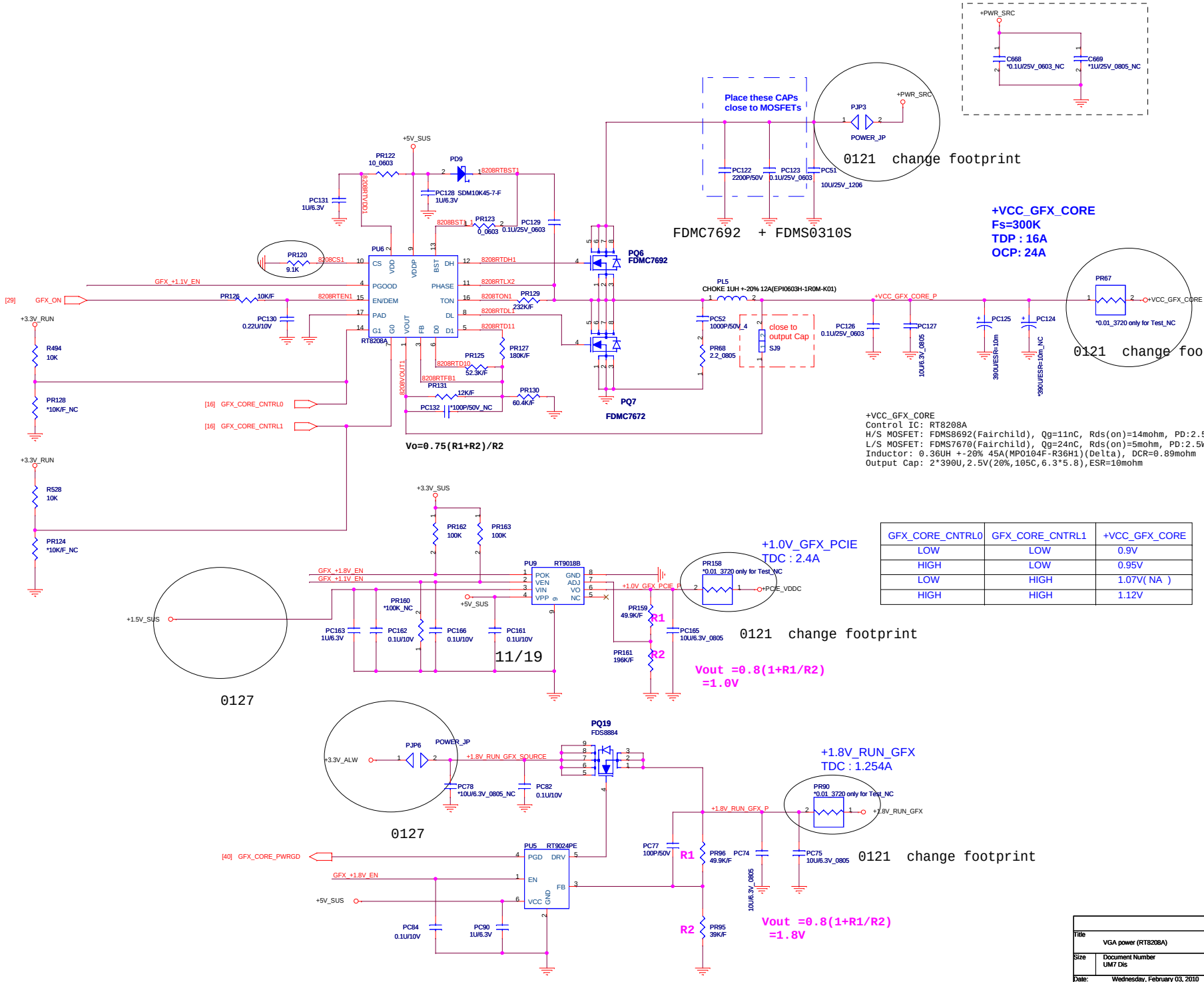

GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	+VCC_GFX_CORE
LOW	LOW	0.9V
HIGH	LOW	0.95V
LOW	HIGH	1.07V(NA)
HIGH	HIGH	1.12V

Title	VGA power (RT8208A)	
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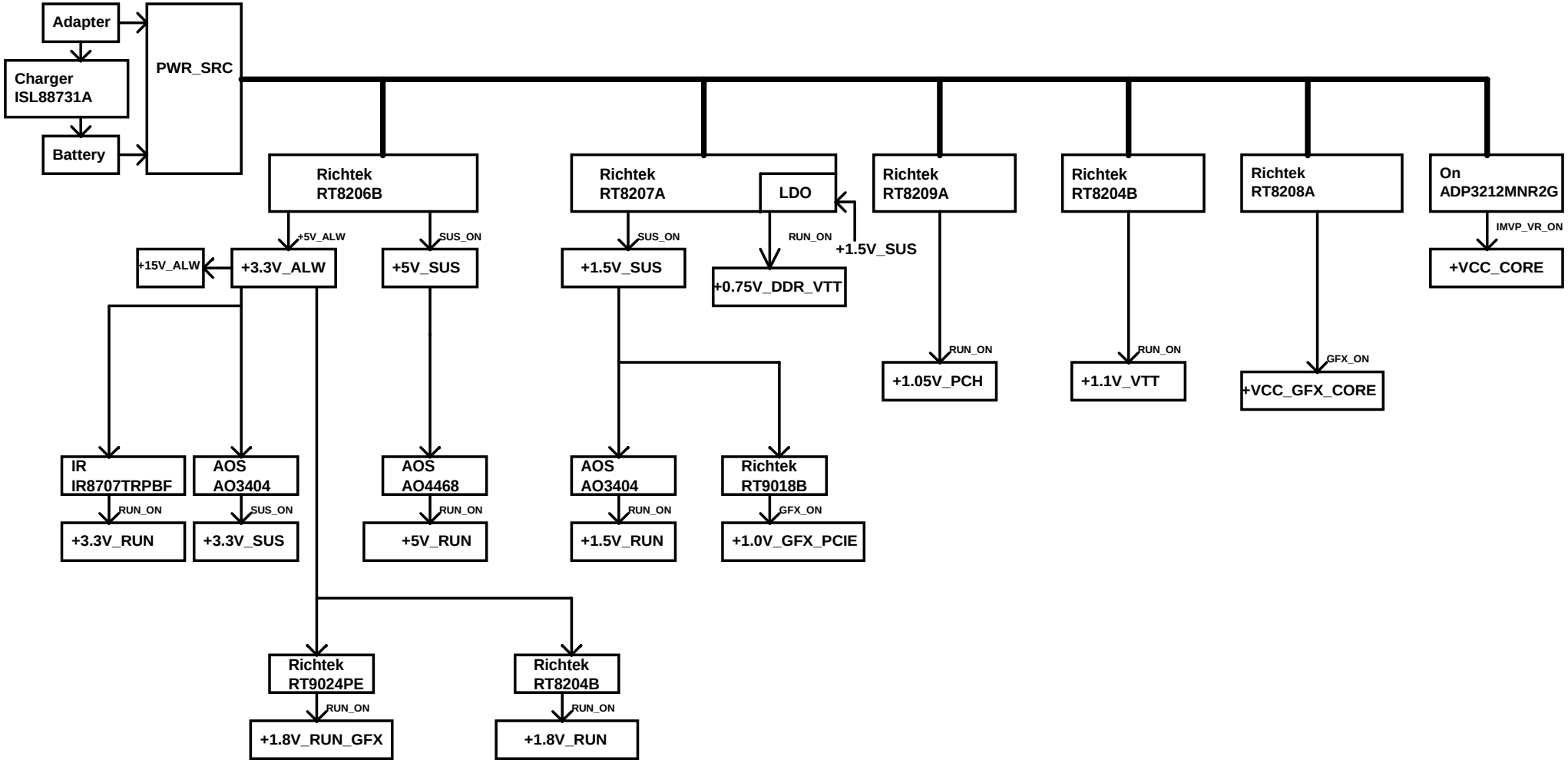

Quanta Computer Inc.

PROJECT : UM7 DIS

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	Schematic Block Diagram1	3A

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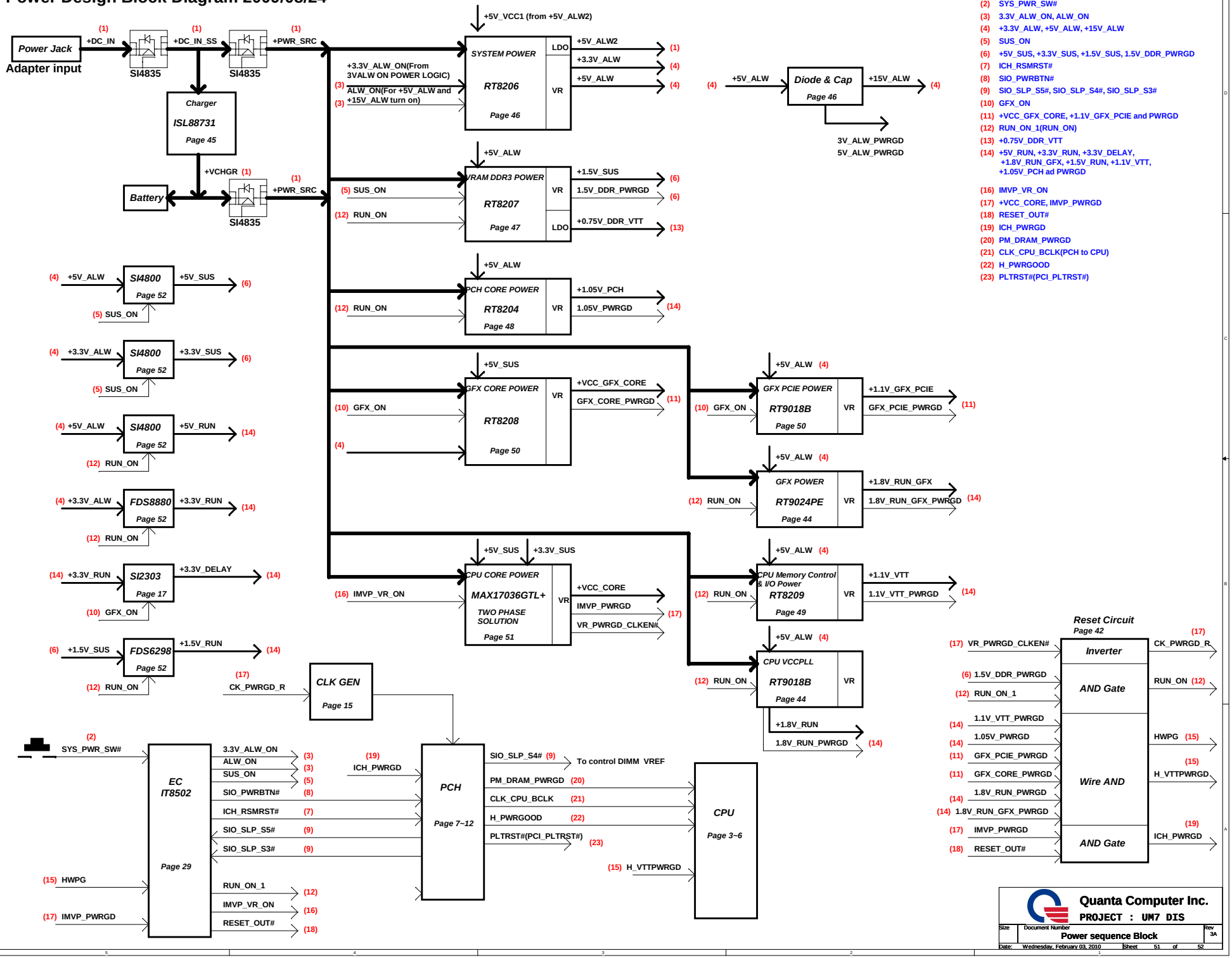
Power Design Block Diagram 2009/08/24



(1) AC : DC_IN -> DC_IN_SS -> +PWR_SRC
Bat : +VCHGR -> +PWR_SRC,+5V_ALW2,
(2) SYS_PWR_SW#
(3) 3.3V_ALW_ON, ALW_ON
(4) +3.3V_ALW, +5V_ALW, +15V_ALW
(5) SUS_ON
(6) +5V_SUS, +3.3V_SUS, +1.5V_SUS, 1.5V_DDR_PWRGD
(7) ICH_RSMRST#
(8) SIO_PWRBTN#
(9) SIO_SLP_S5#, SIO_SLP_S4#, SIO_SLP_S3#
(10) GFX_ON
(11) +VCC_GFX_CORE, +1.1V_GFX_PCIE and PWRGD
(12) RUN_ON_1(RUN_ON)
(13) +0.75V_DDR_VTT
(14) +5V_RUN, +3.3V_RUN, +3.3V_DELAY, +1.8V_RUN_GFX, +1.5V_RUN, +1.1V_VTT, +1.05V_PCH ad PWRGD
(16) IMVP_VR_ON
(17) +VCC_CORE, IMVP_PWRGD
(18) RESET_OUT#
(19) ICH_PWRGD
(20) PM_DRAM_PWRGD
(21) CLK_CPU_BCLK(PCH to CPU)
(22) H_PWRGOOD
(23) PLTRST#(PCI_PLTRST#)

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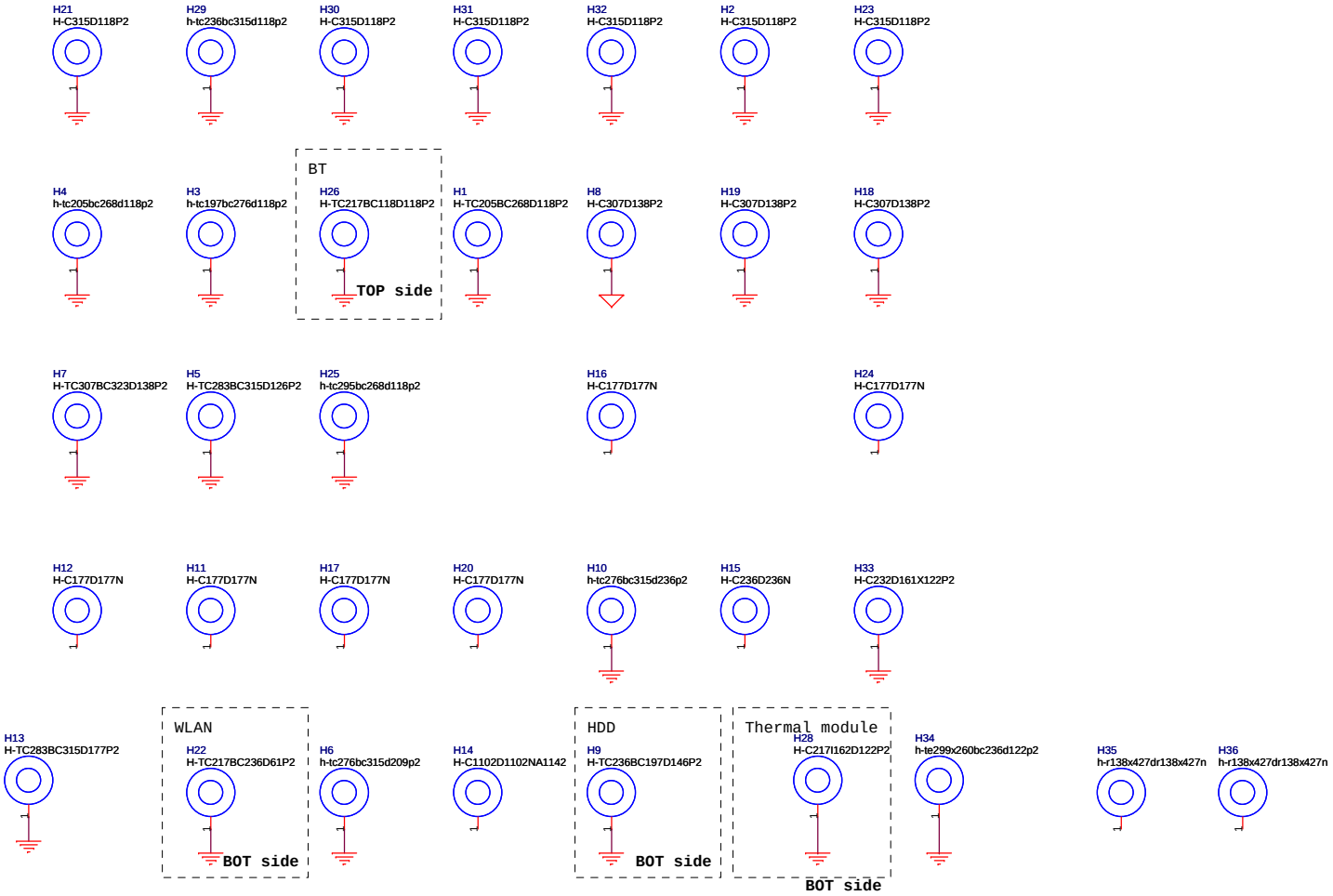

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