

Berry DG15 Discrete/UMA Schematics Document

Arrandale

Intel PCH

2010-02-03

REV : A00

DY :None Installed
UMA:UMA platform installed
PARK:DIS PARK platform installed
M96:DIS M96 platform installed
*VRAM_1G:VRAM 128M*16 installed*
Colay :Manual modify BOM

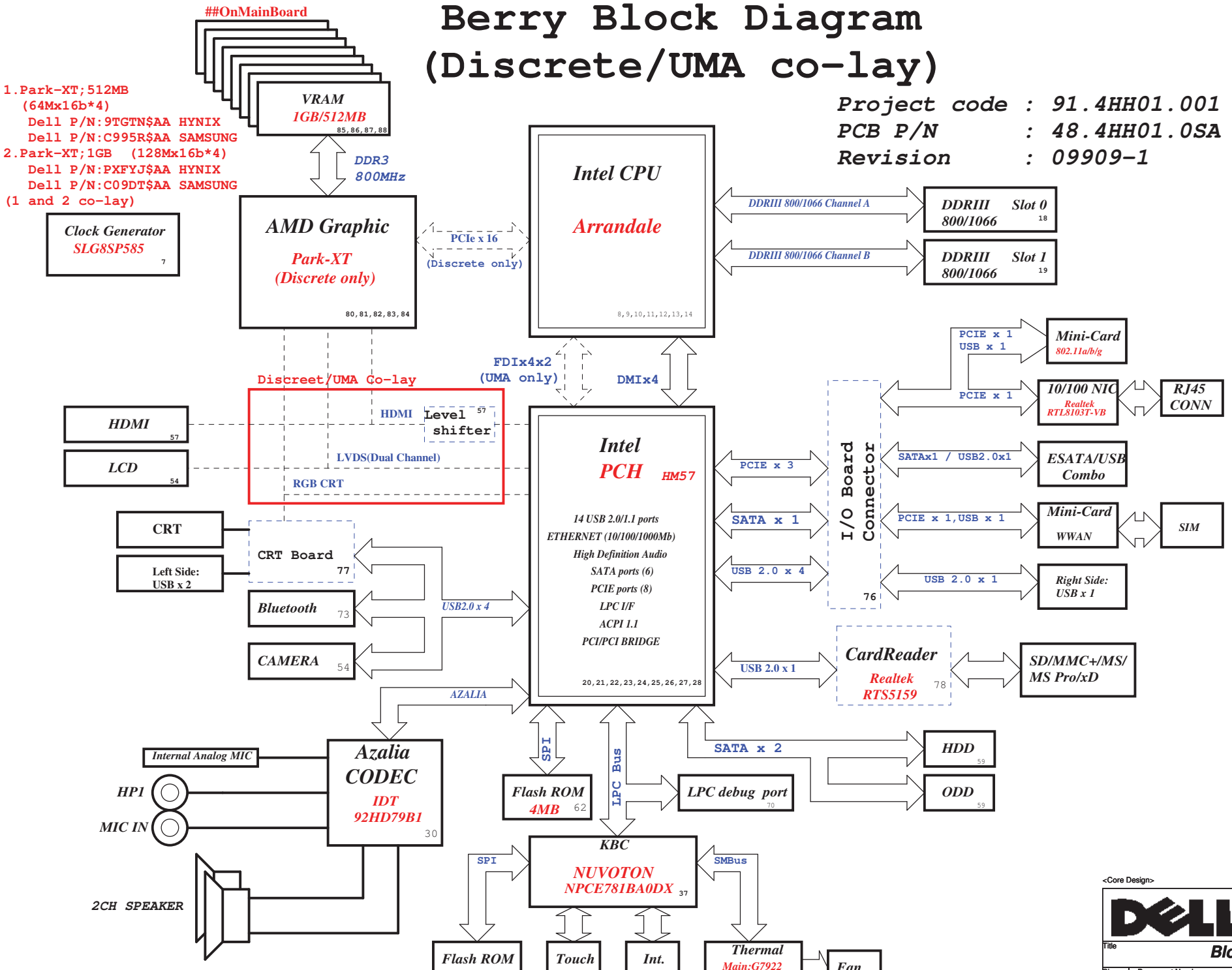
<Core Design>



Title		Cover Page	
Size A3	Document Number Berry	Rev A00	
Date: Wednesday, February 10, 2010	Sheet 1	of 92	

Berry Block Diagram (Discrete/UMA co-lay)

Project code : 91.4HH01.001
PCB P/N : 48.4HH01.0SA
Revision : 09909-1



CPU DC/DC ISL62883		47
INPUTS	OUTPUTS	
+PWR_SRC	+VCC_CORE	
SYSTEM DC/DC TPS51218		49
INPUTS	OUTPUTS	
+PWR_SRC	+1.05V_VTT	
SYSTEM DC/DC RT8205B		46
INPUTS	OUTPUTS	
+PWR_SRC	+5V_ALW2 +3.3V_RTC_LDO +5V_ALW +3.3V_ALW +15V_ALW	
SYSTEM DC/DC TPS51116		50
INPUTS	OUTPUTS	
+PWR_SRC	+1.5V_SUS +0.75V_DDR_VTT +V_DDR_REF	
SYSTEM DC/DC TPS51611		53
INPUTS	OUTPUTS	
+PWR_SRC	+CPU_GFX_CORE	
VGA RT8208B		89
INPUTS	OUTPUTS	
+PWR_SRC	+VGA_CORE	
TI CHARGER BQ24745		45
INPUTS	OUTPUTS	
+DC_IN +PBATT	+PWR_SRC	
SYSTEM DC/DC APL5930		51
INPUTS	OUTPUTS	
+3.3V_ALW	+1.8V_RUN +1.8V_RUN_VGA	
SYSTEM DC/DC APL5930		90
INPUTS	OUTPUTS	
+1.5V_SUS	+1.0V_RUN_VGA	
Switches		
INPUTS	OUTPUTS	
+1.5V_SUS +5V_ALW +3.3V_ALW	+1.5V_RUN +5V_RUN +3.3V_RUN	
PCB LAYER		
L1: Top		
L2: VCC		
L3: Signal		
L4: Signal		
L5: GND		
L6: Bottom		

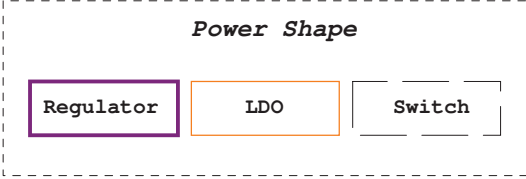
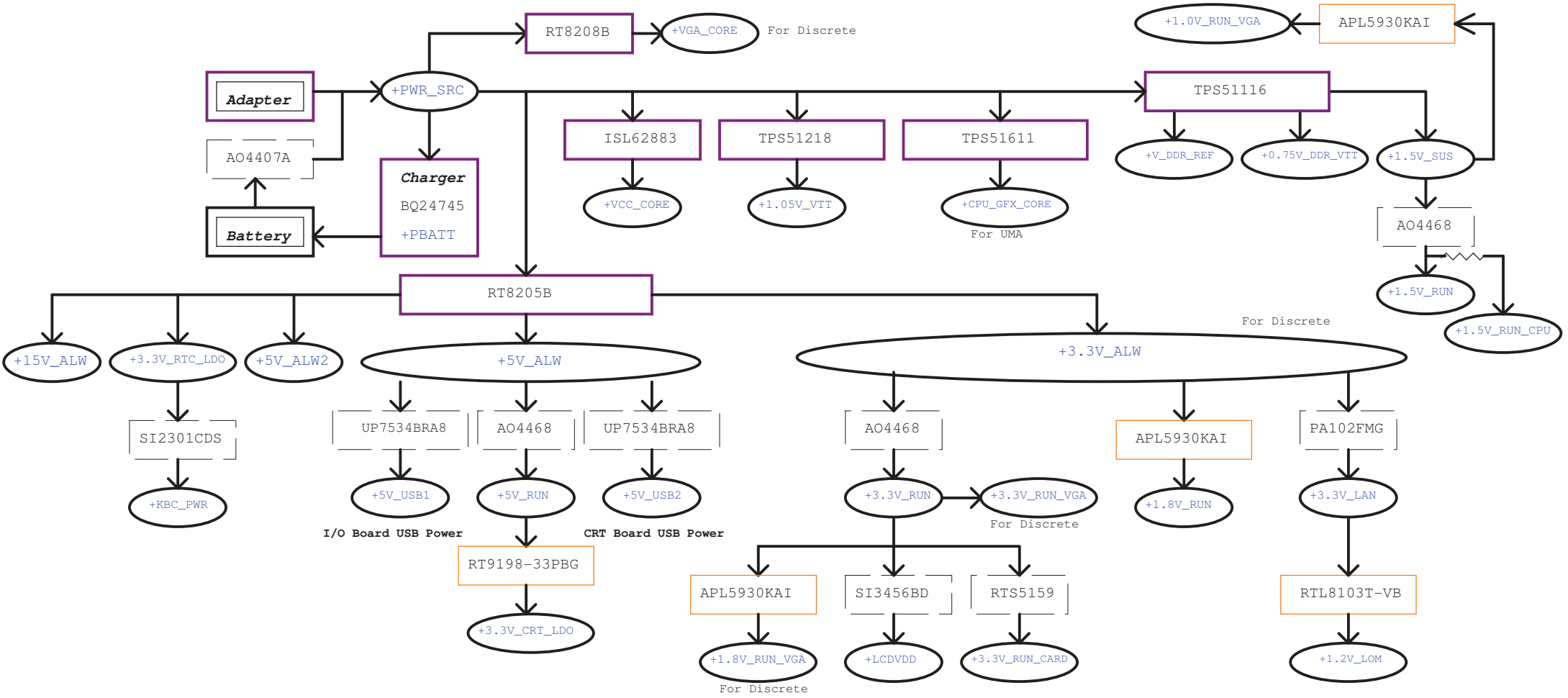
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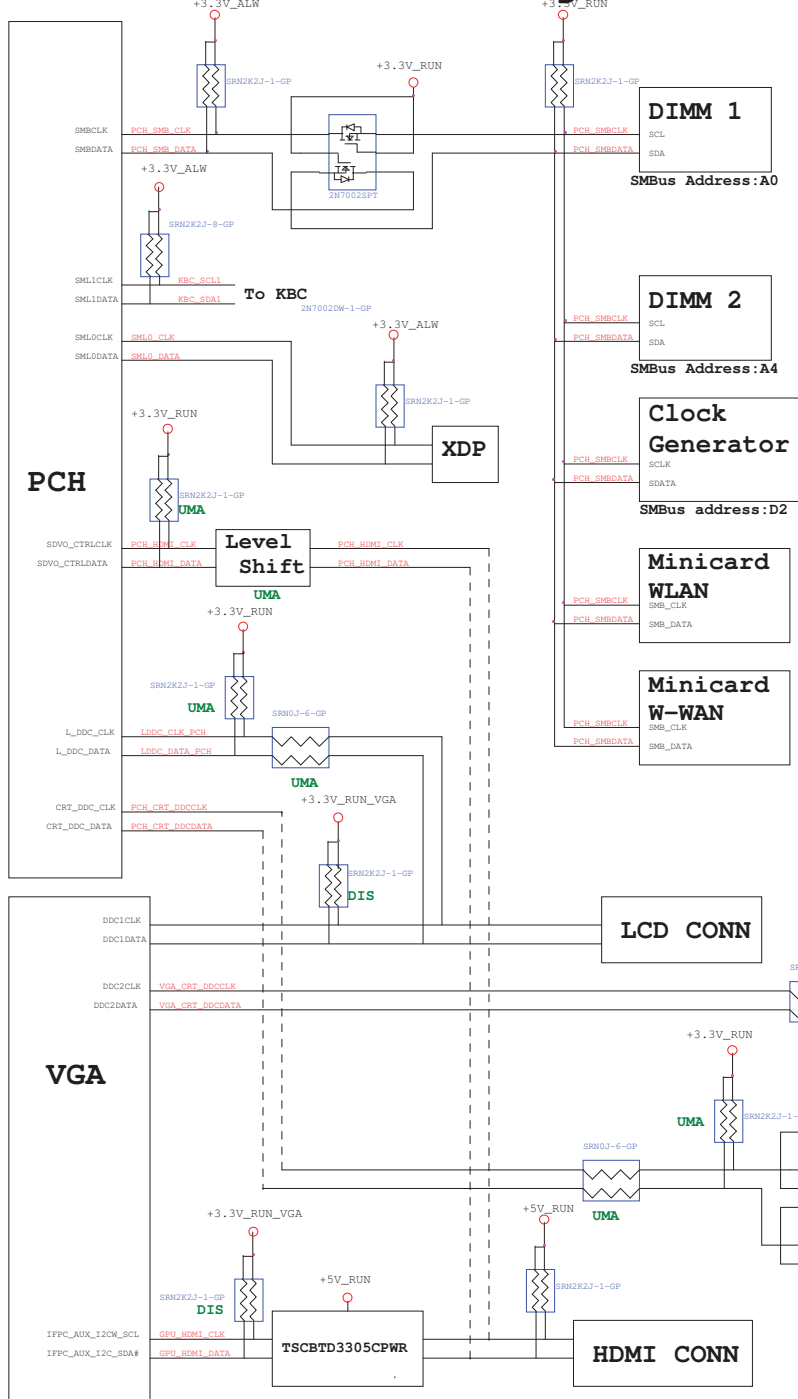
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Size A3	Document Number Berry	Rev A00
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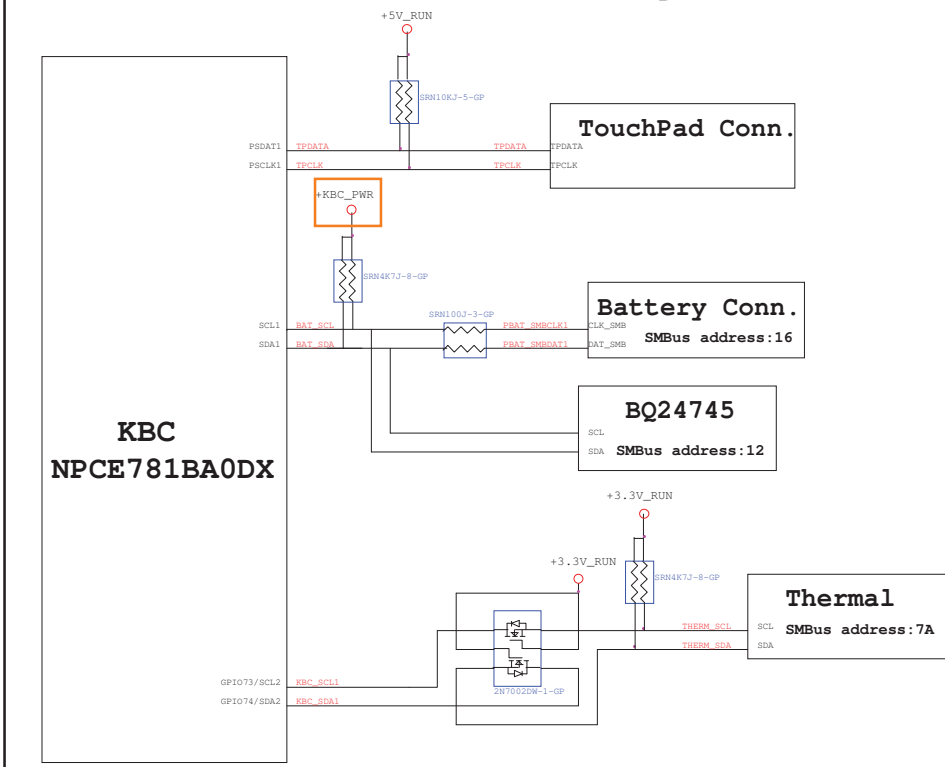
Date: Wednesday, February 10, 2010 Sheet 2 of 92



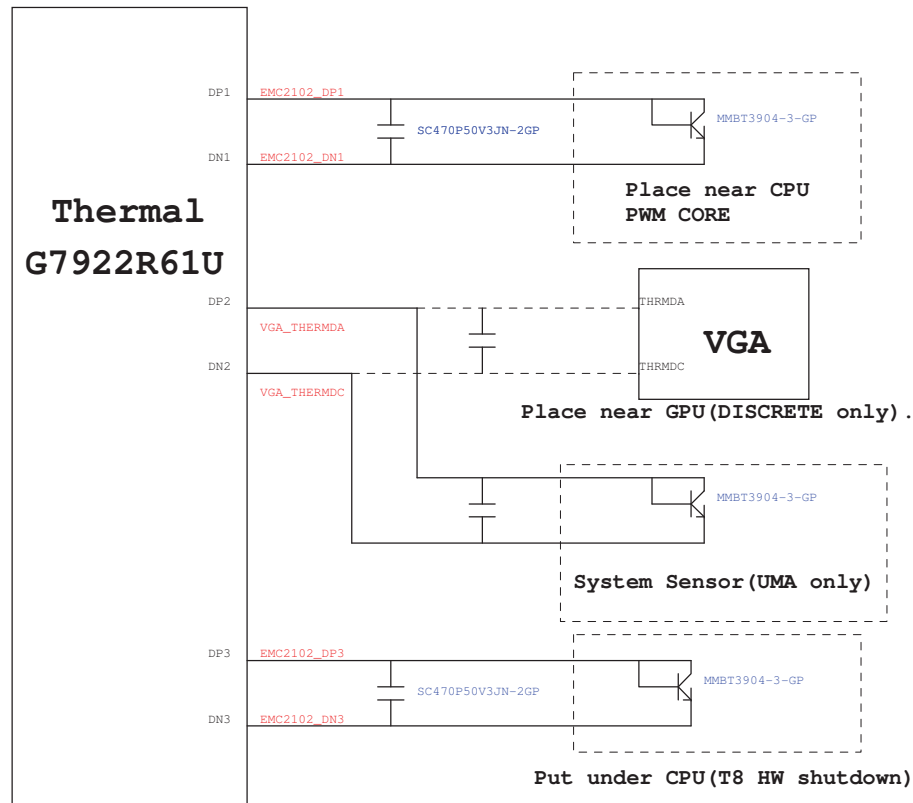
PCH SMBus Block Diagram



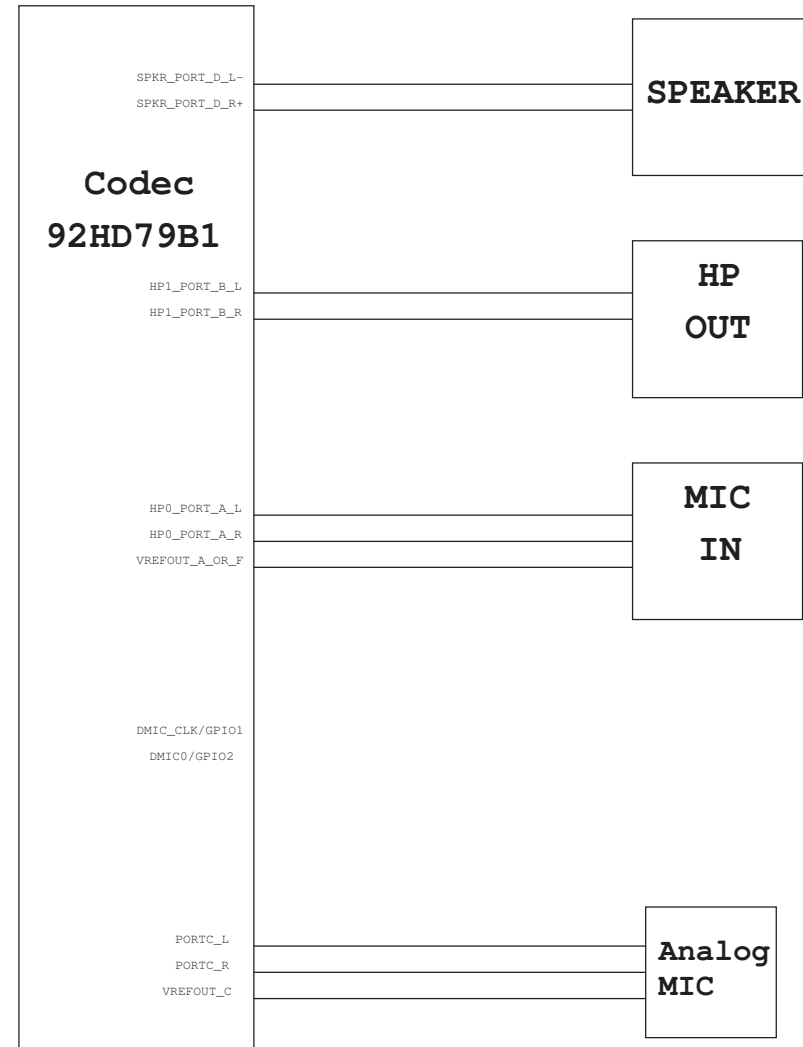
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



PCH Strapping

Calpella Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap Mode (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled
GNT0#, GNT1#/GPIO51	Default (SPI): Left both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/GPIO53	Default - Internal pull-up. Low (0) = Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	Default: Do not pull low. Disable ME in Manufacturing Mode: Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable iTPM: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0): Flash Descriptor Security will be overridden. High (1): Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

PCIe Routing

LANE1	RESERVED
LANE2	MiniCard WLAN
LANE3	LAN
LANE4	W-WAN
LANE5	RESERVED
LANE6	RESERVED
LANE7	H55/HM55 no support
LANE8	H55/HM55 no support

USB Table

Pair	Device
0	USB2 (CRT Board)
1	USB3 (CRT Board)
2	WLAN (I/O Board)
3	RESERVED
4	CARD READER
5	BLUETOOTH
6	HM55 no support
7	HM55 no support
8	USB1 (I/O Board)
9	USB0 (I/O Board ESATA)
10	RESERVED
11	W-WAN (I/O Board)
12	RESERVED
13	CAMERA

SATA Table

Pair	Device
0	HDD
1	ODD
2	HM55 no support
3	HM55 no support
4	ESATA
5	RESERVED

Processor Strapping

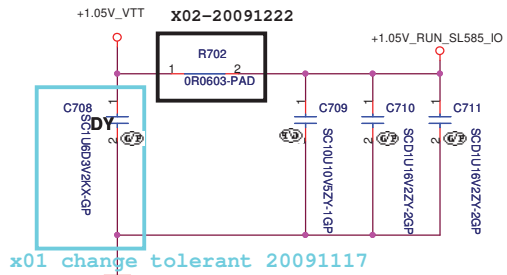
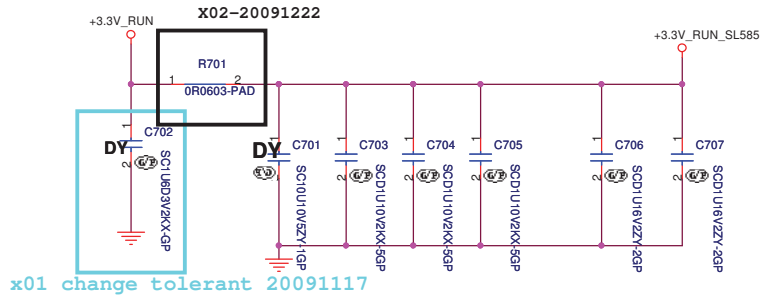
Calpella Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	Reserved - Temporarily used for early Clarksfield samples.	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor Note: Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

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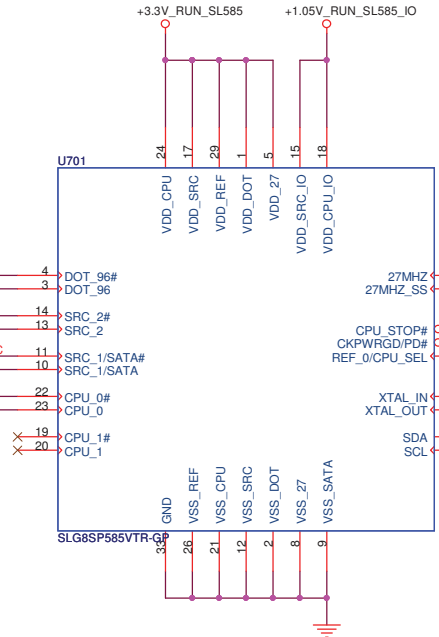
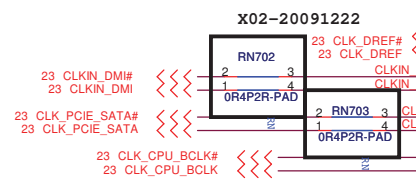
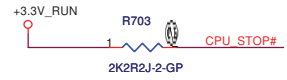
DELL		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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Size A3	Document Number Berry	Rev A00	
Date: Wednesday, February 10, 2010	Sheet 6	of	92

SSID = CLOCK

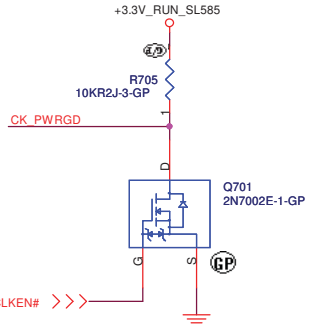
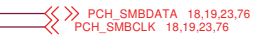
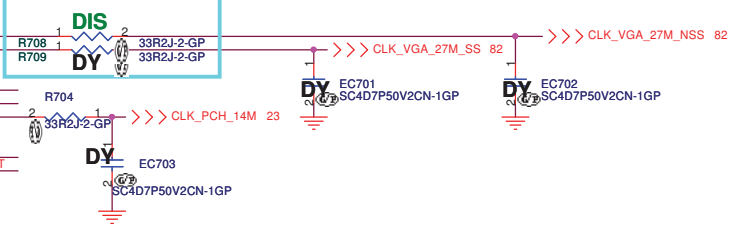


x01 change tolerant 20091117

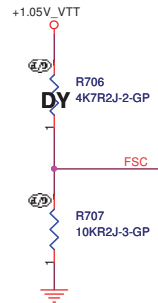
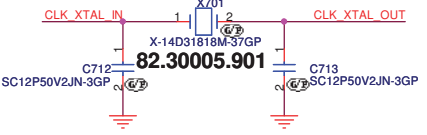
x01 change tolerant 20091117



X01-20091116



FSC	0	1
SPEED	133MHz (Default)	100MHz



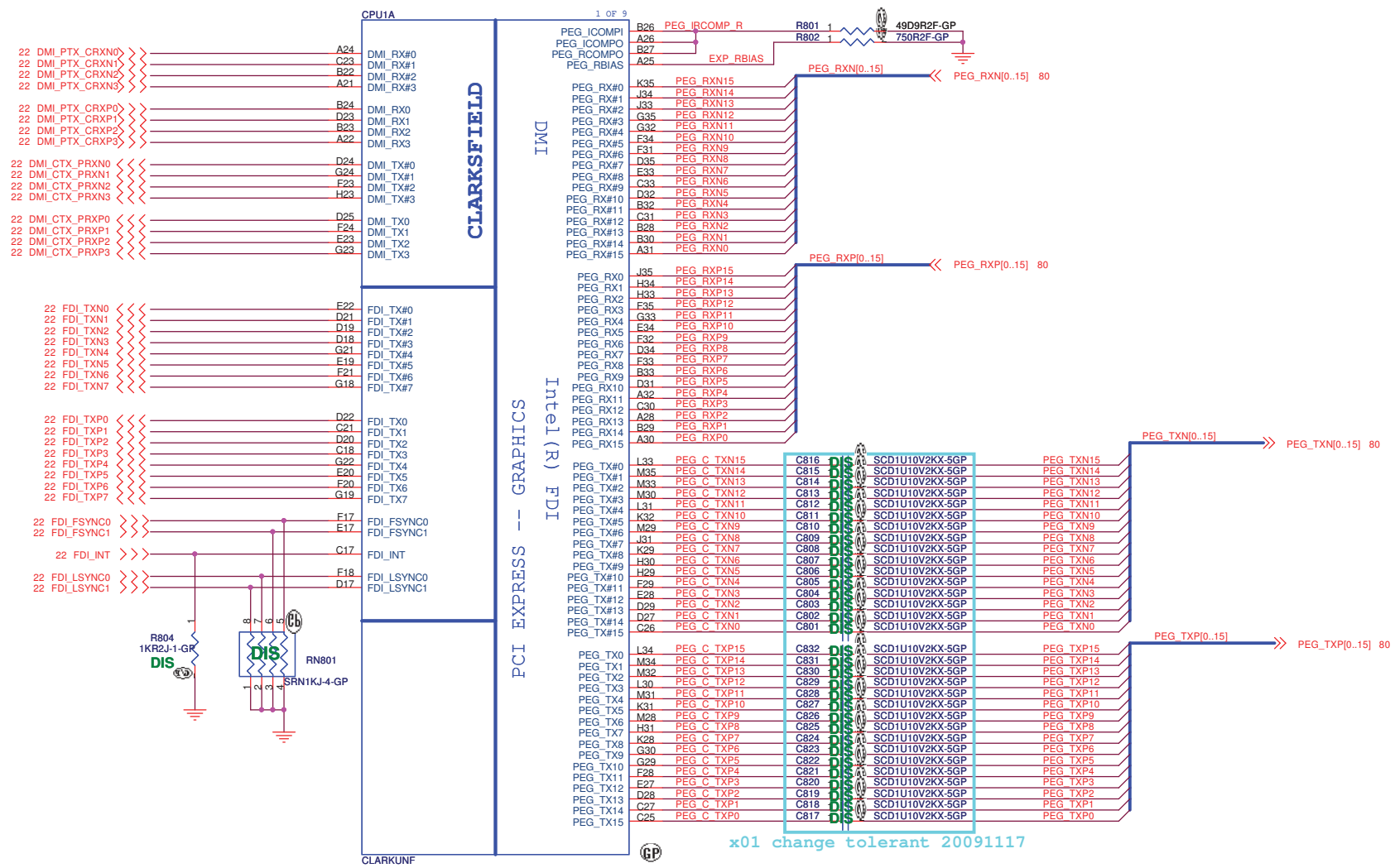
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Title
Clock Generator SLG8SP585

Size	Document Number	Rev
	Berry	A00

Date: Monday, March 29, 2010 Sheet 7 of 92



62.10055.341
 SEC. 62.10053.561

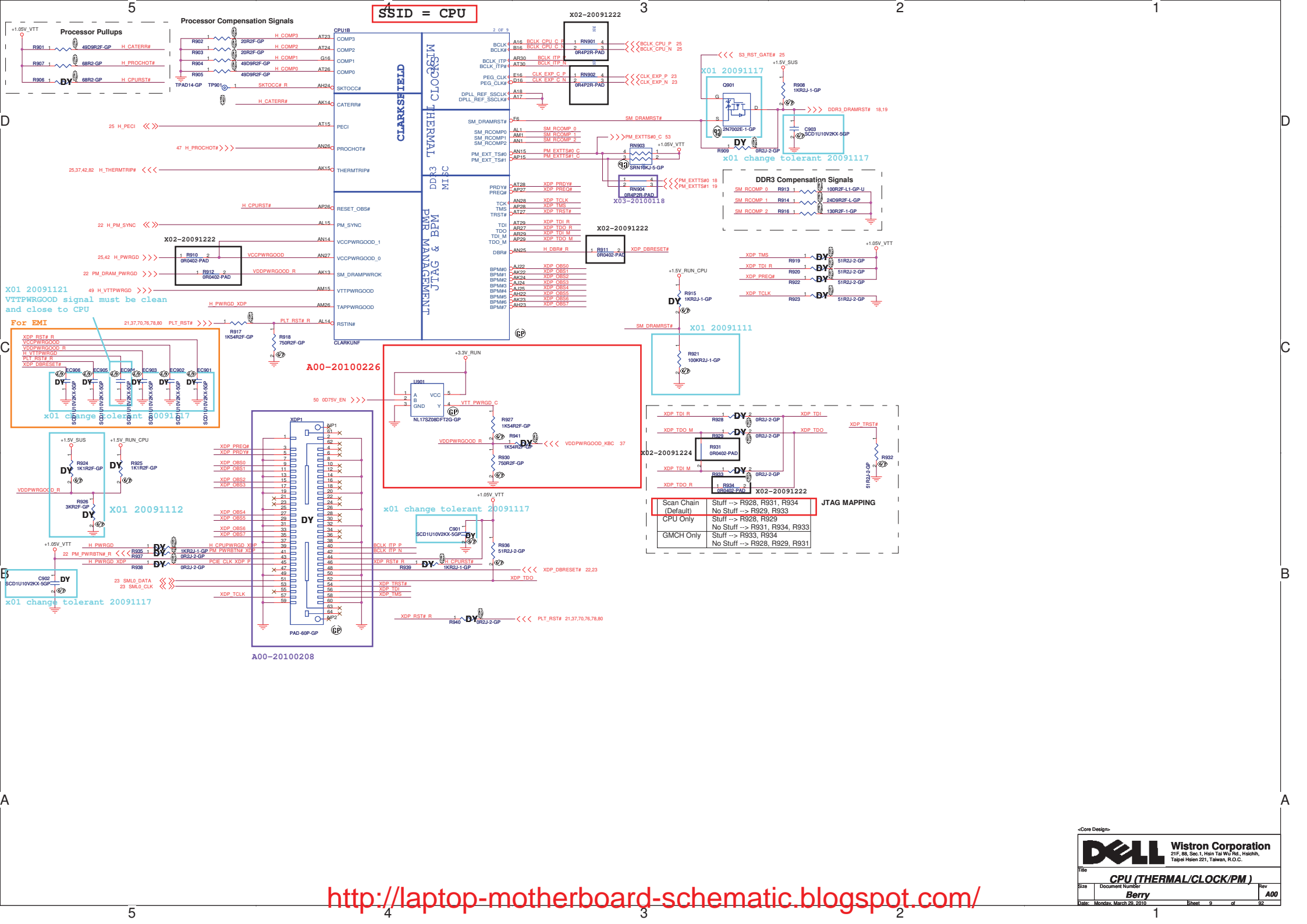
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Title: **CPU (PCIE/DMI/FDI)**

Size: Document Number **Berry** Rev **A00**

Date: Monday, March 29, 2010 Sheet 8 of 92



SSID = CPU

	Scan Chain (Default)	Scan Chain (No Stuff)	JTAG MAPPING
Scan Chain (Default)	Stuff -> R928, R931, R934	No Stuff -> R929, R934	
CPU Only	Stuff -> R928, R929	No Stuff -> R931, R934, R933	
GMCH Only	Stuff -> R933, R934	No Stuff -> R928, R929, R931	

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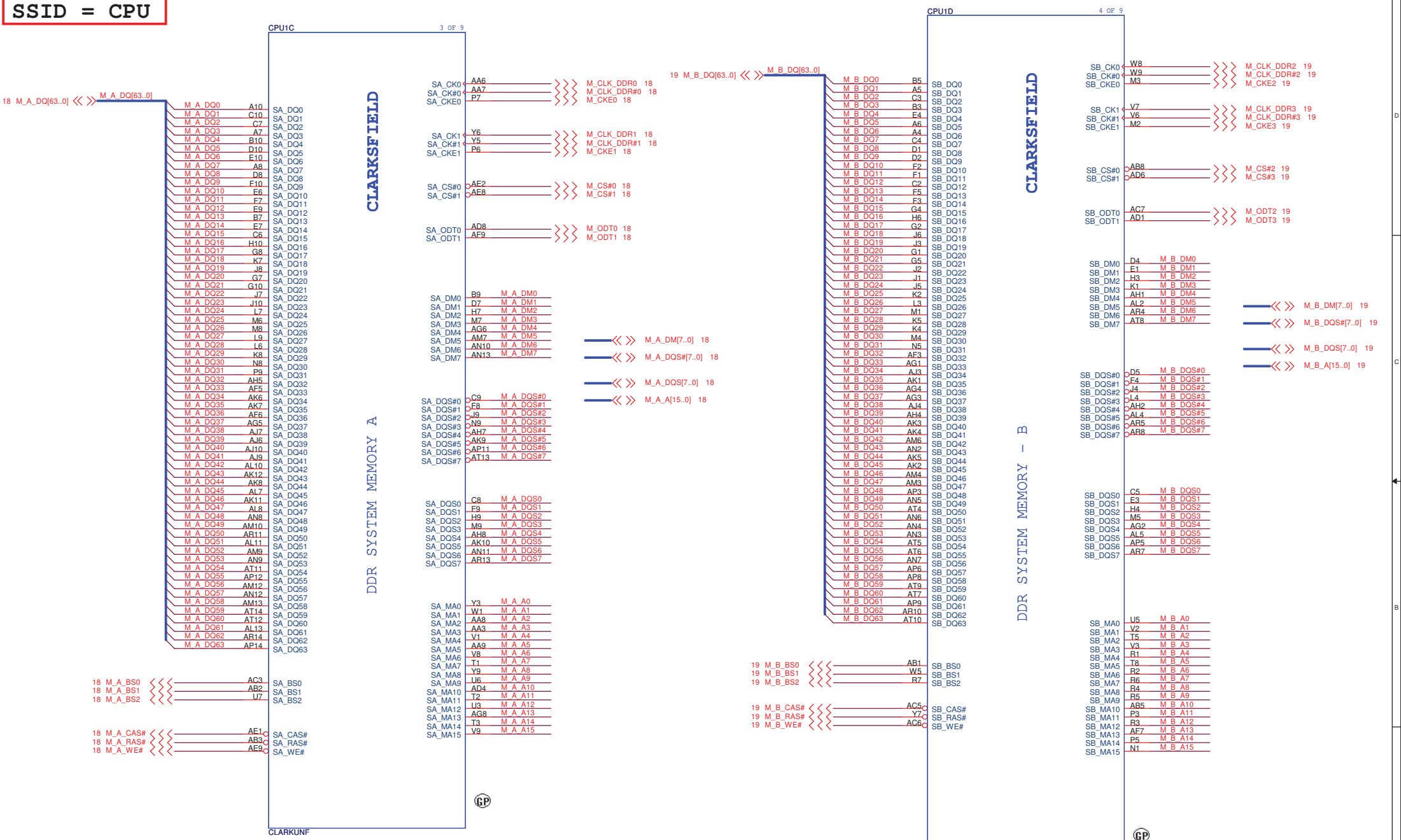
DELL Wistron Corporation
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File: **CPU (THERMAL/CLOCK/PM)**

Size: Document Number: **Berry** Rev: **A00**


Date: Monday, March 29, 2010 Sheet: 9 of 92

SSID = CPU



<http://laptop-motherboard-schematic.blogspot.com/>

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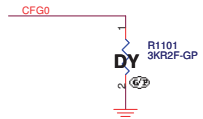


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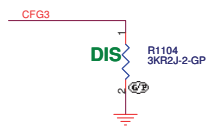
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Size	Document Number	Rev
	Berry	A00

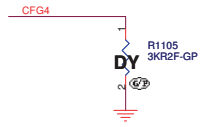
Date: Monday, March 29, 2010 Sheet 10 of 92



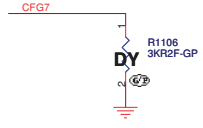
PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled



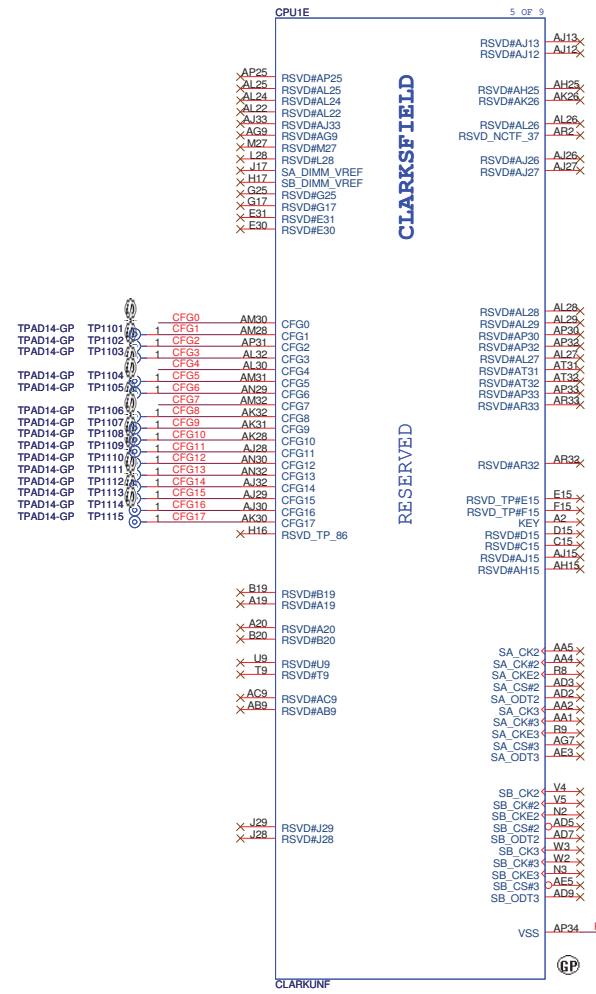
CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...



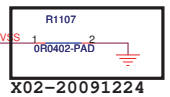
CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port



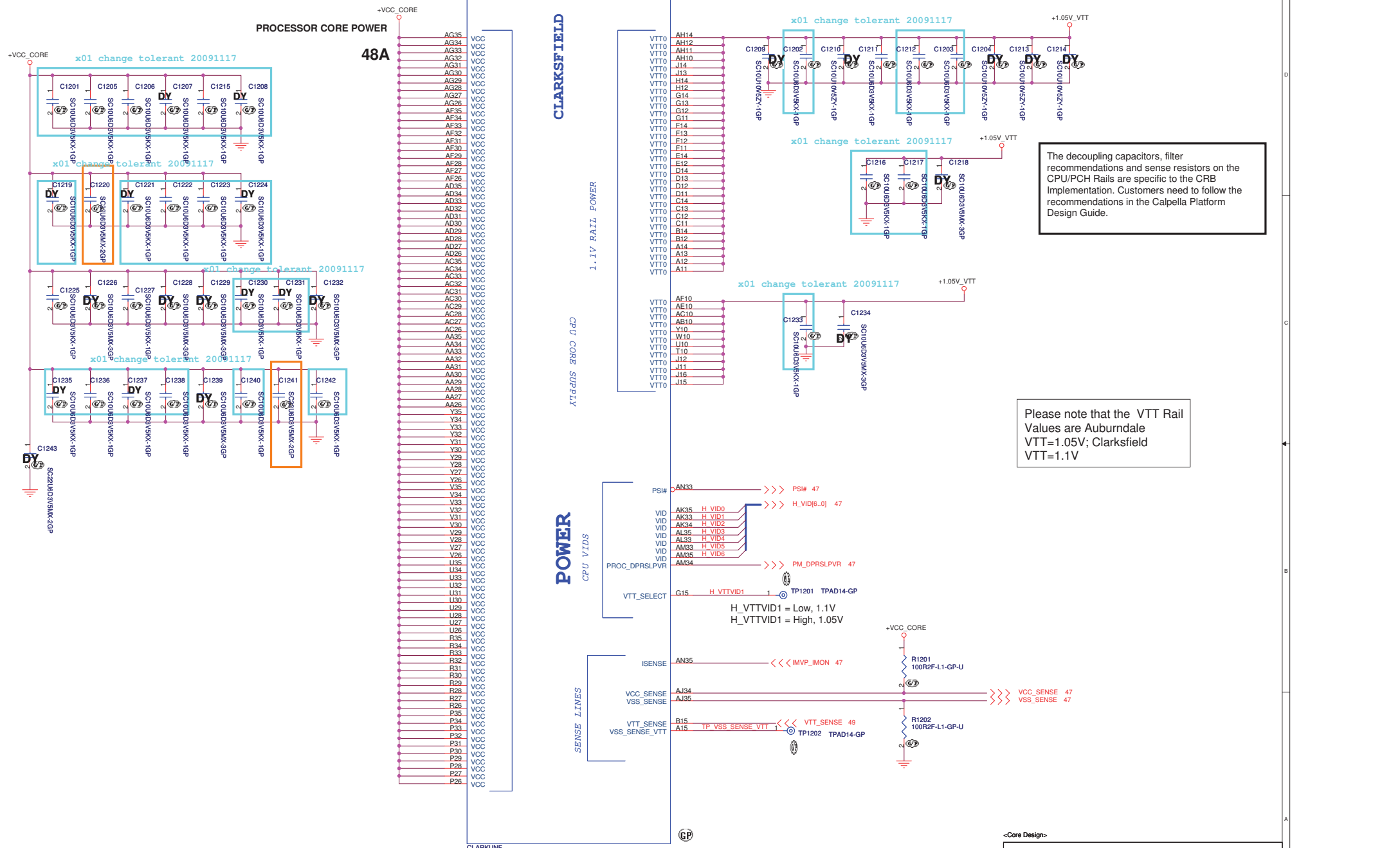
CFG7(Reserved) - Temporarily used for early Clarkfield samples.	
CFG7	Clarkfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.



VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.



SSID = CPU



The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V

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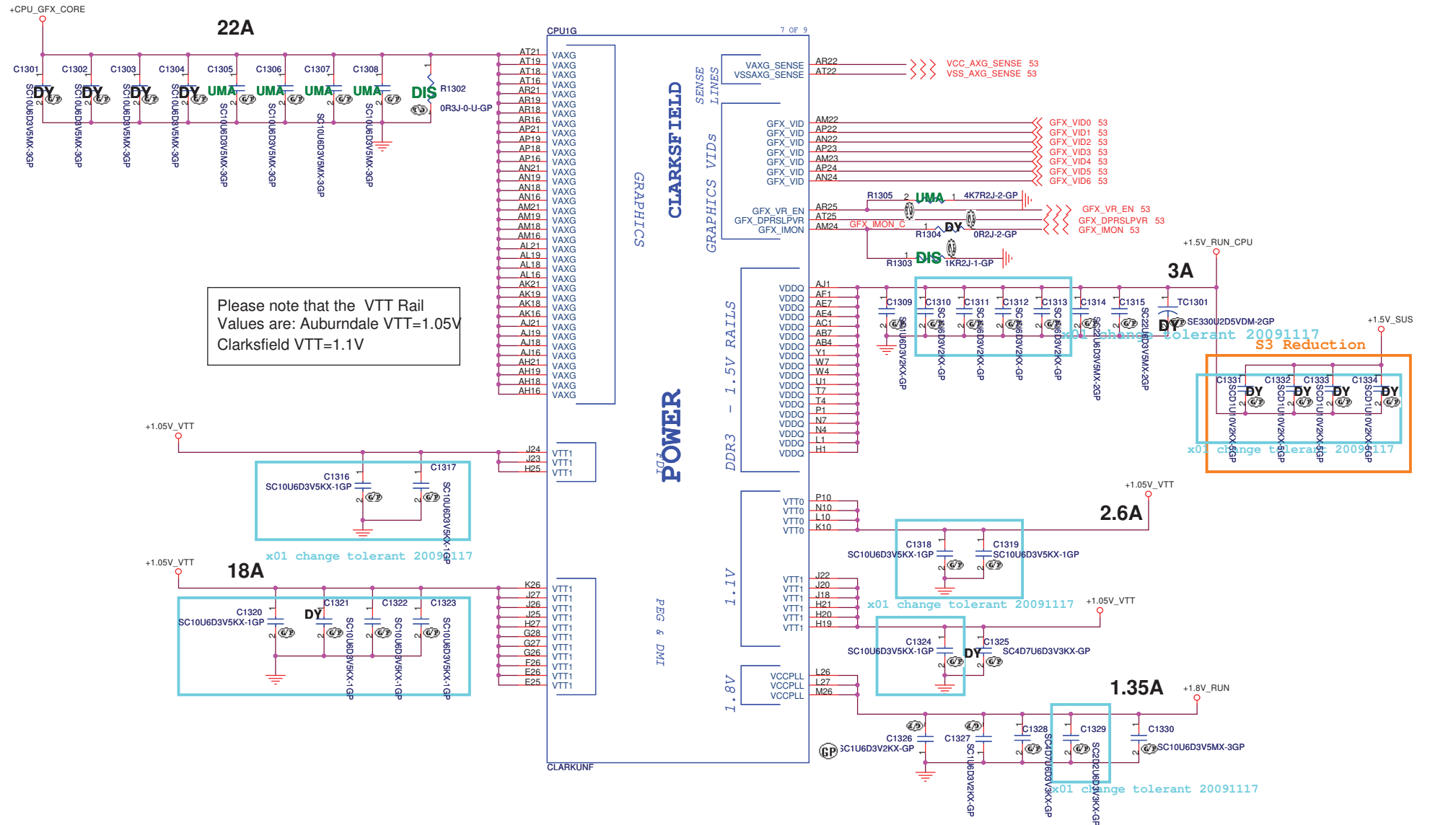
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Title: **CPU (VCC_CORE)**

Size	Document Number	Rev
		A00

Date: 10/23/2010 Sheet 12 of 92

SSID = CPU



Please note that the VTT Rail Values are: Auburndale VTT=1.05V
Clarksfield VTT=1.1V

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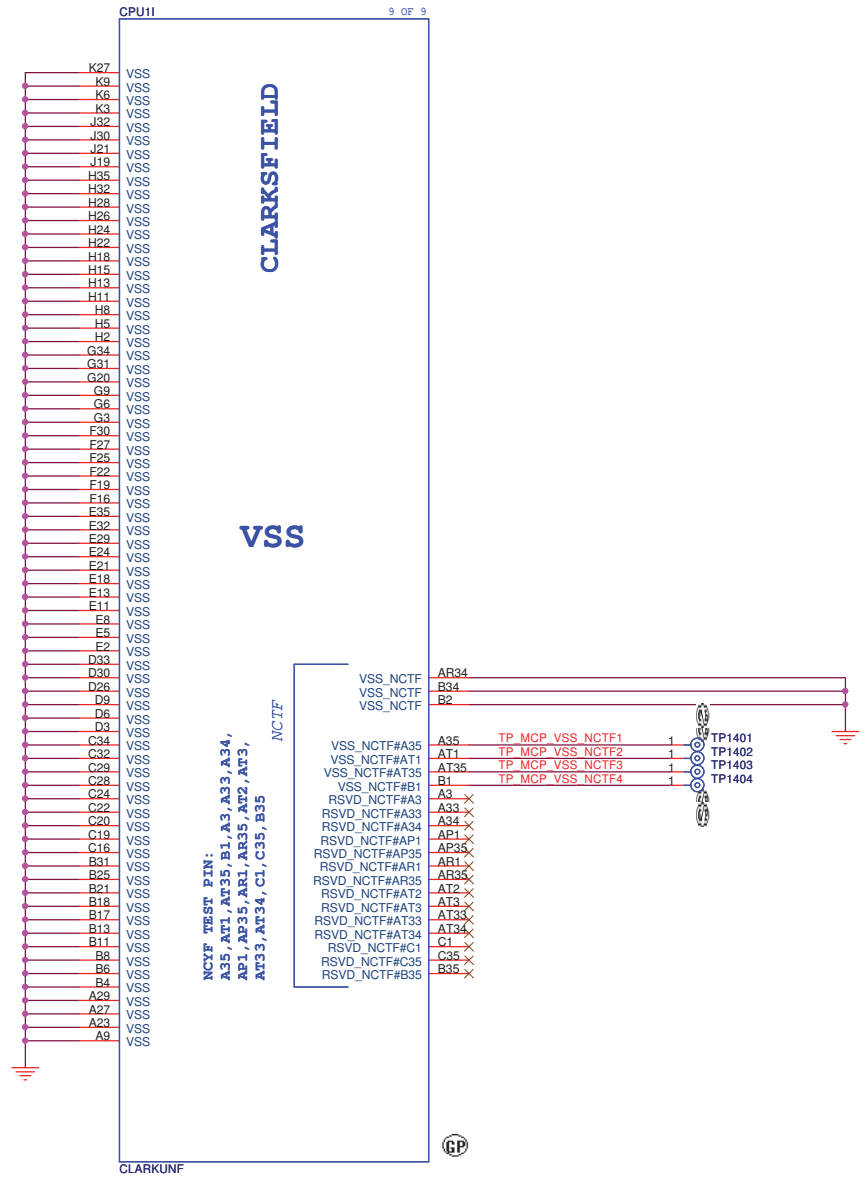
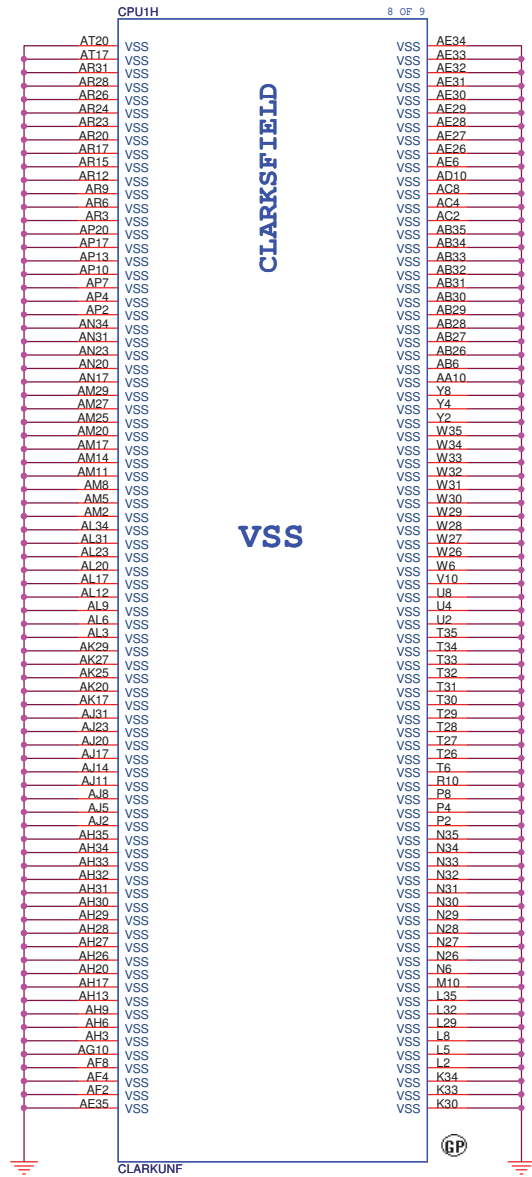
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Title: **CPU (VCC_GFXCORE)**

Size: Document Number **Berry** Rev: **A00**

Date: Monday, March 29, 2010 Sheet 13 of 92

SSID = CPU



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Title: **CPU (VSS)**

Size	Document Number	Rev
	Berry	A00

Date: Wednesday, February 10, 2010 Sheet 14 of 92

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Size	Document Number	Rev	
A3	Berry	A00	
Date:	Wednesday, February 10, 2010	Sheet	15 of 92

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Date: Wednesday, February 10, 2010		Sheet 16	of 92

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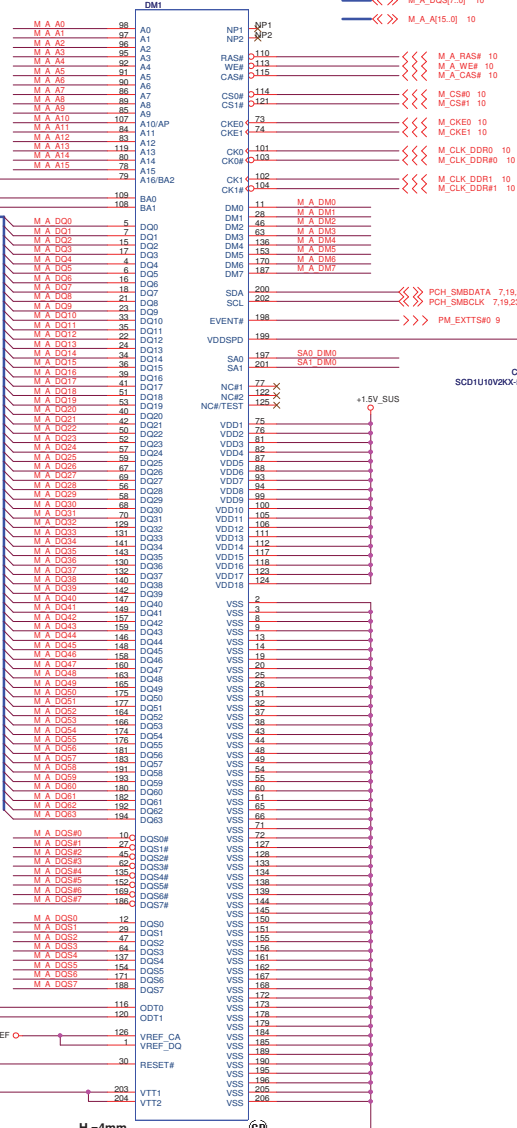
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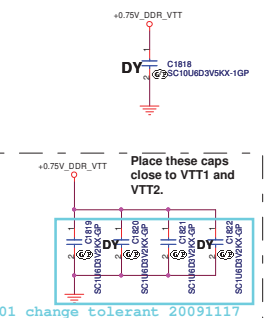
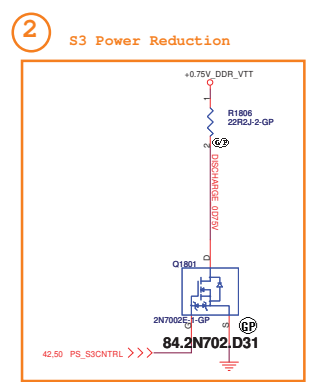
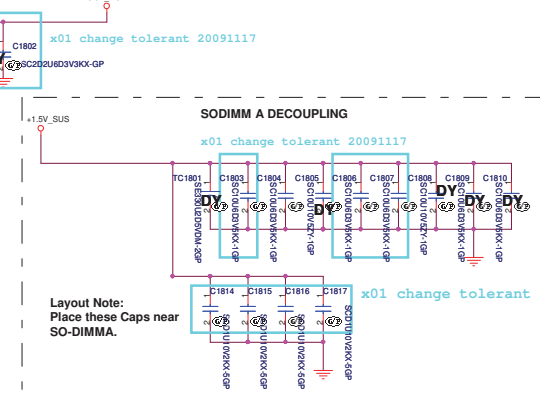
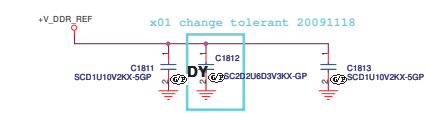
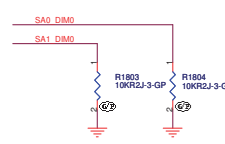
Date: Wednesday, February 10, 2010	Sheet 17 of 92
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M_A_DM7[7..0] 10
M_A_DQS[7..0] 10
M_A_DQS7[7..0] 10
M_A_A[15..0] 10



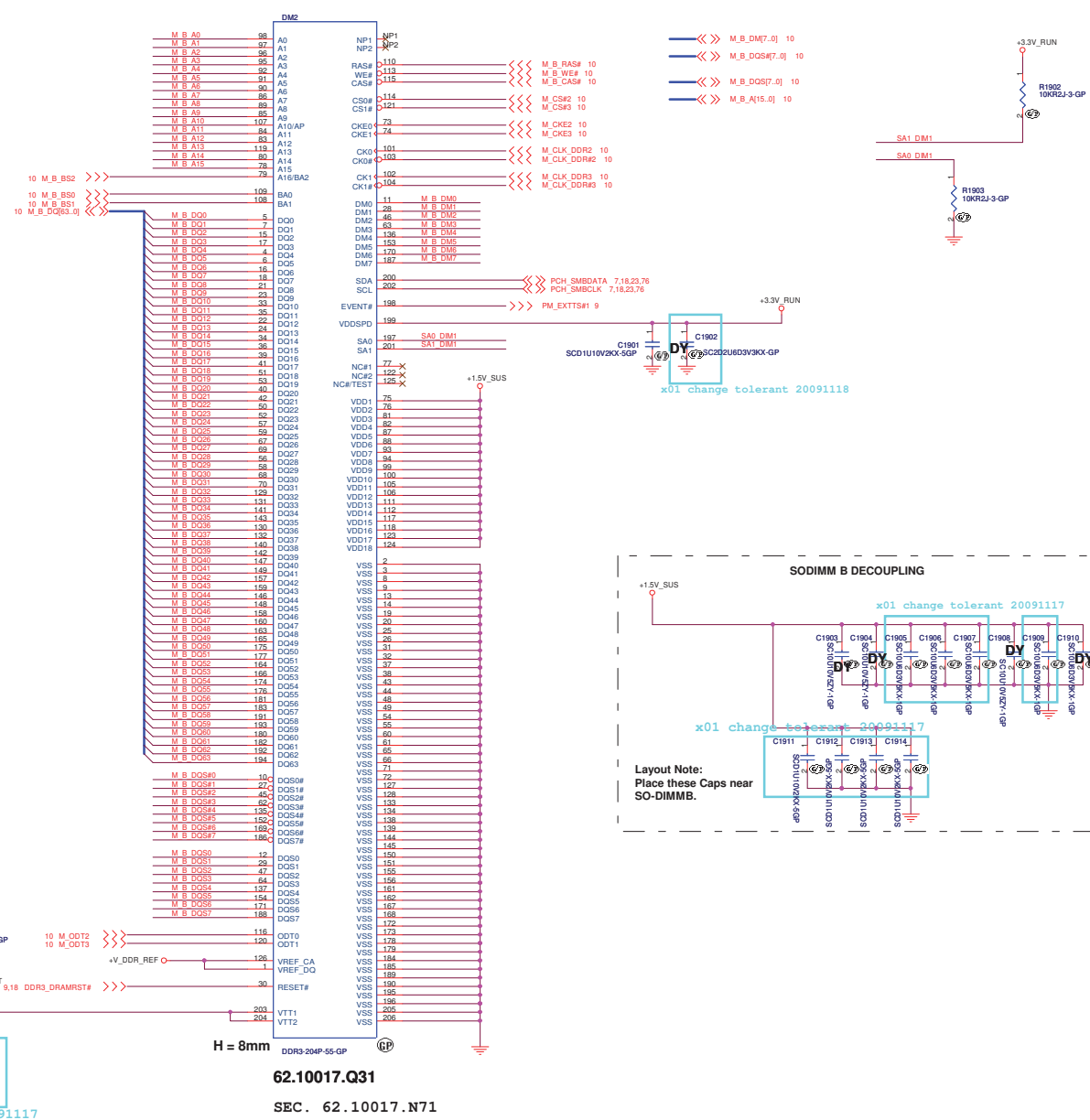
Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32



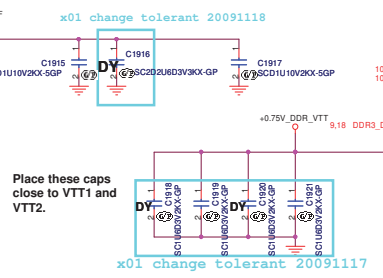
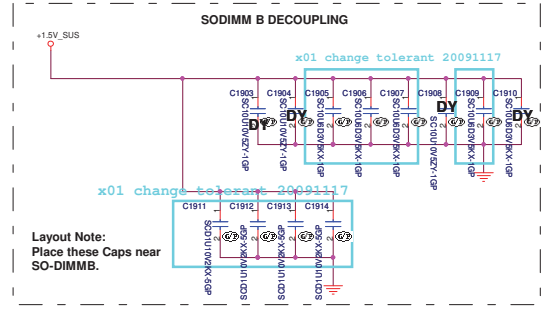
H=4mm
DDR3-204P-47-GP
62.10017.P31
SEC. 62.10017.P11

SSID = MEMORY



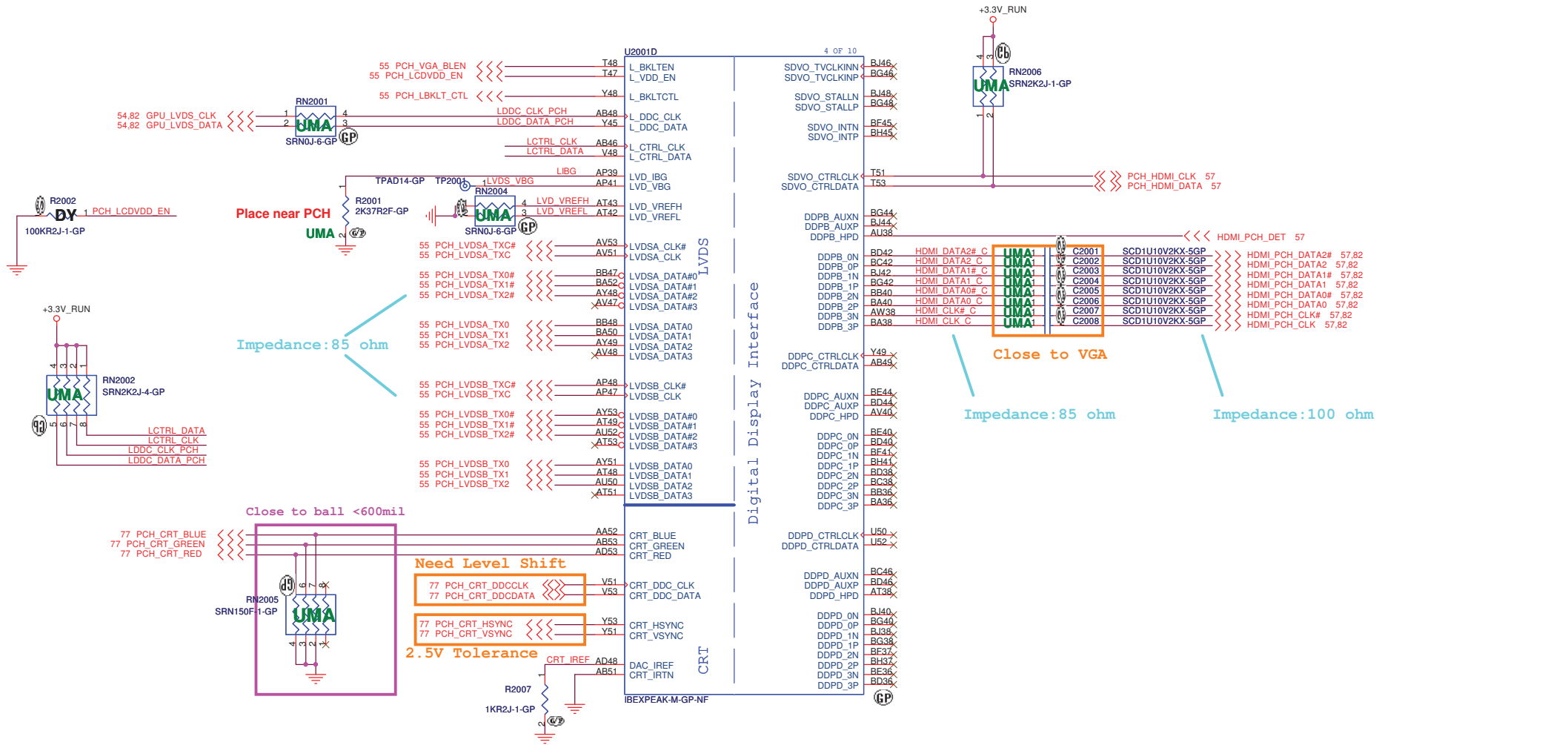
Note:
 If SA0_DIM0 = 0, SA1_DIM0 = 0
 SO-DIMMA SPD Address is 0xA0
 SO-DIMMA TS Address is 0x30

If SA0_DIM0 = 1, SA1_DIM0 = 0
 SO-DIMMA SPD Address is 0xA2
 SO-DIMMA TS Address is 0x32

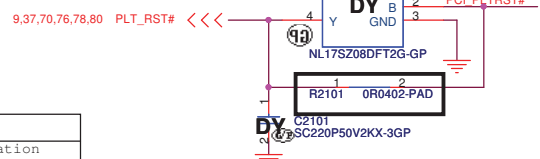
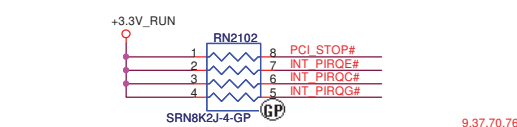
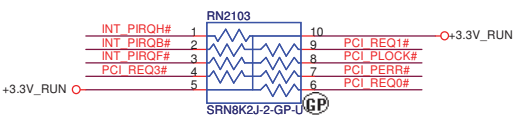
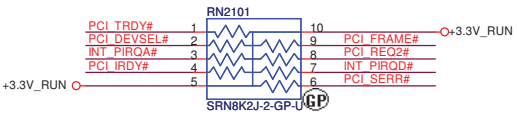


Note:
 SO-DIMMB SPD Address is 0xA4
 SO-DIMMB TS Address is 0x34

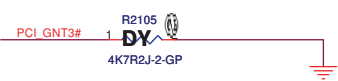
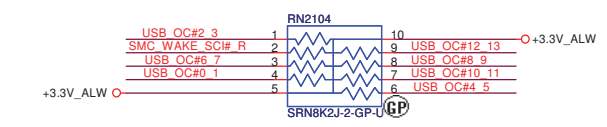
SO-DIMMB is placed farther from the Processor than SO-DIMMA



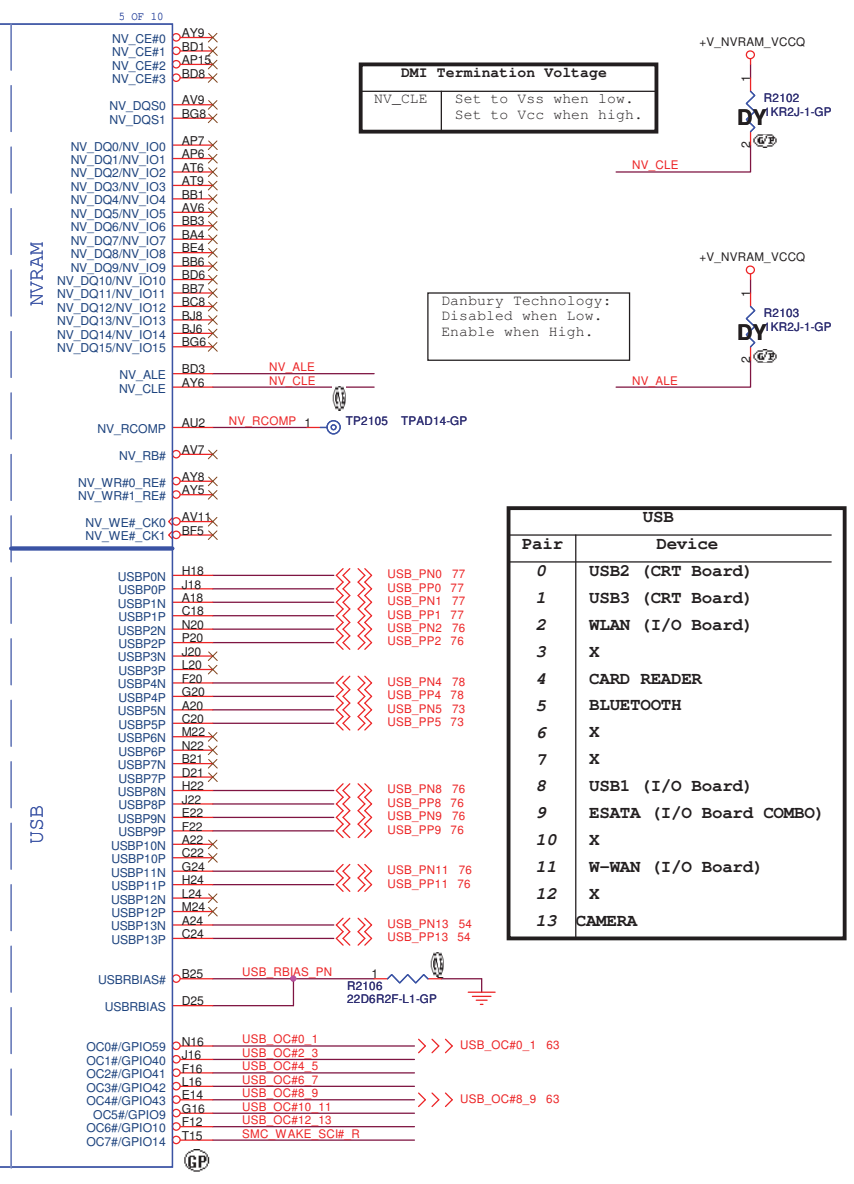
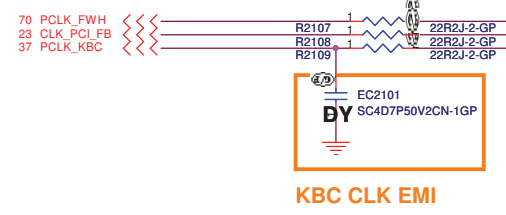
SSID = PCH



BOOT BIOS Strap		
PCI_GNT#1	PCI_GNT#0	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI (Default)



Al6 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = Al6 swap override/Top-Block Swap Override enabled High = Default



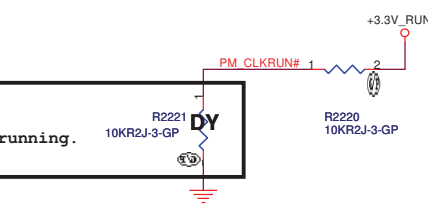
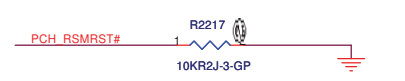
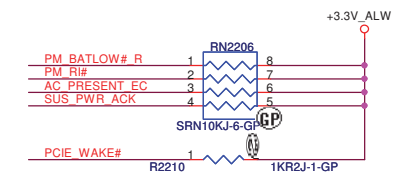
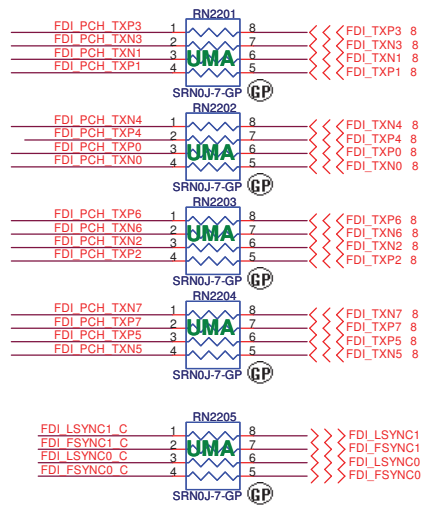
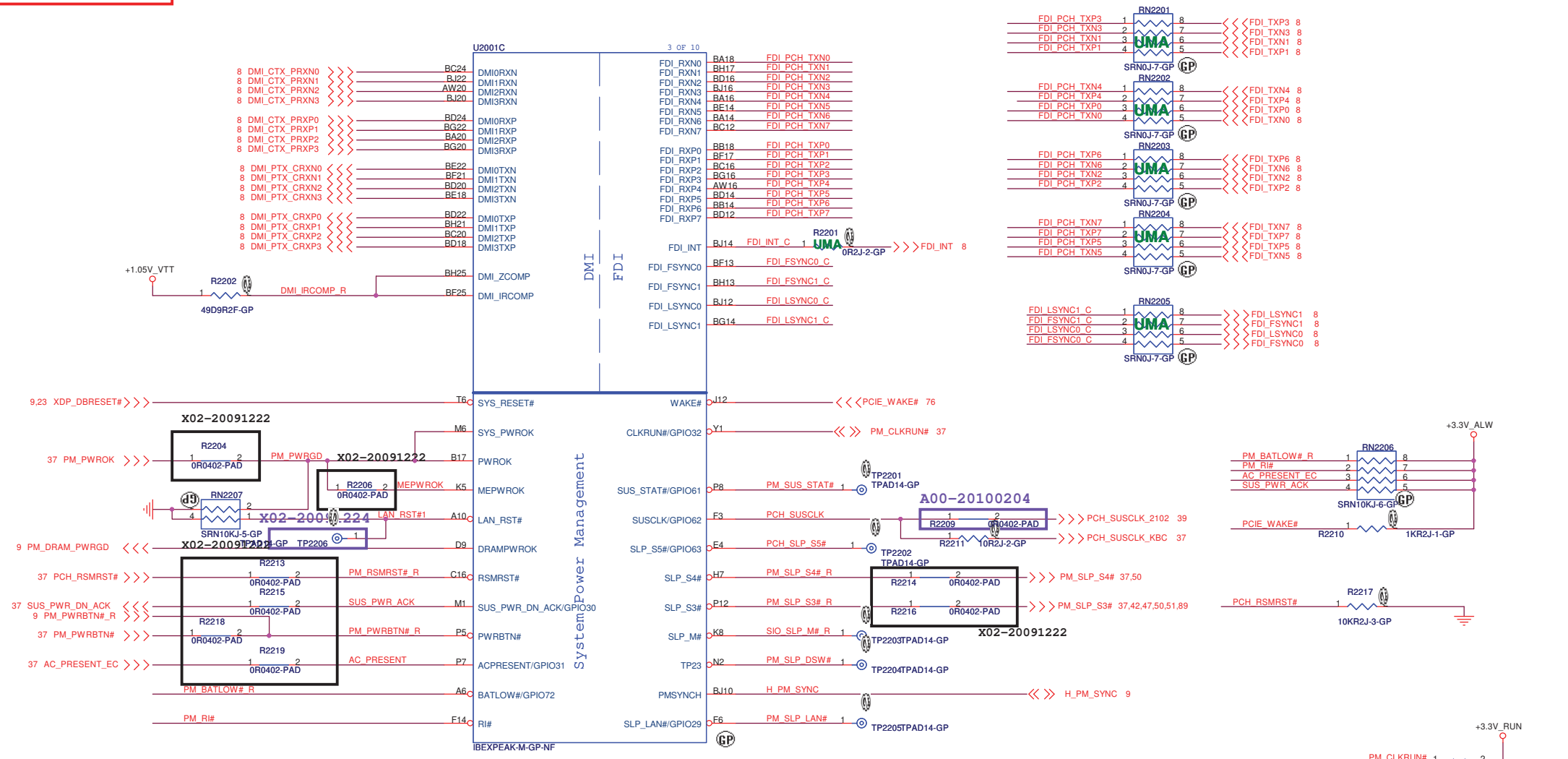
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Title: **PCH (PCI/USB/NVRAM)**

Size: Document Number **Berry** Rev: **A00**

Date: Monday, March 29, 2010 Sheet 21 of 92



Option to "Disable" clkrun.
Pulling it down will keep the clks running.

<Core Design>

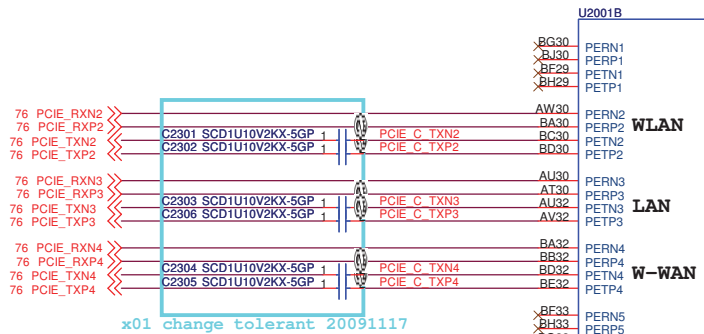
DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (DM I/FDI/PM)**

Size	Document Number	Rev
	Berry	A00

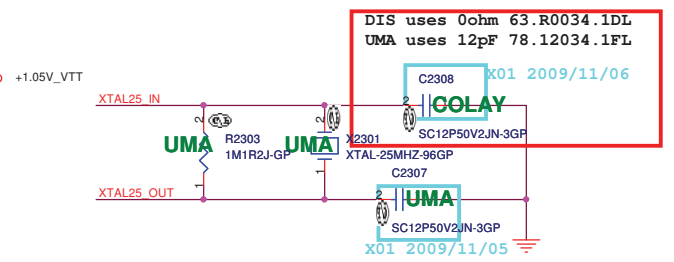
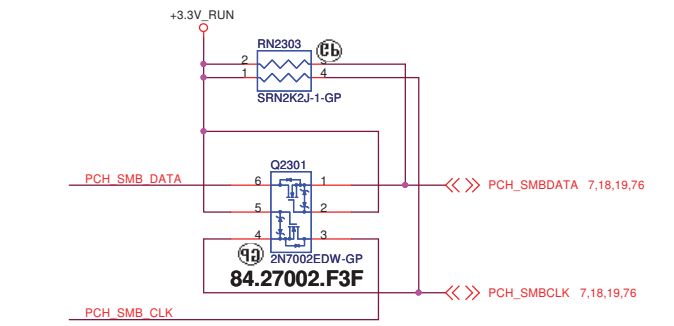
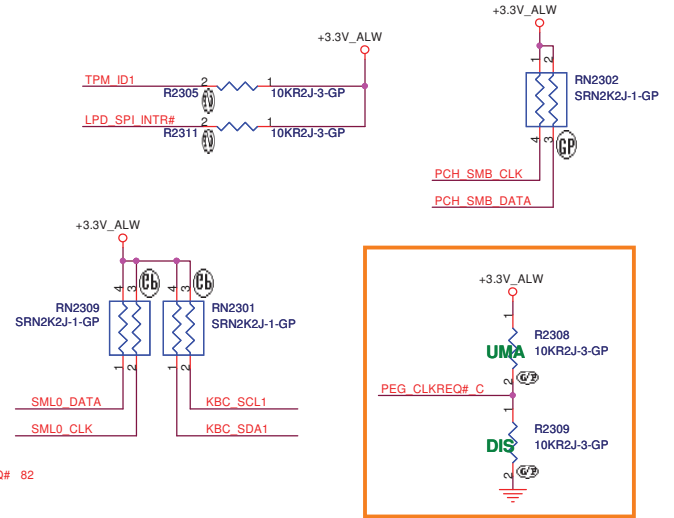
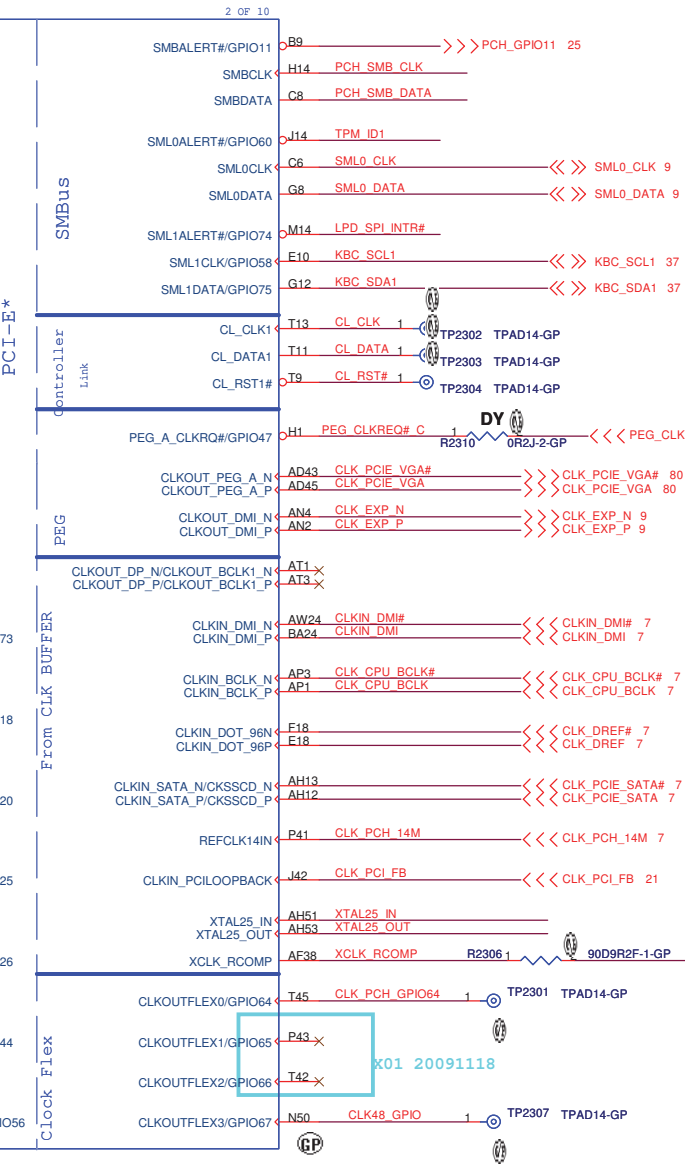
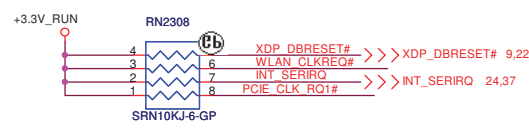
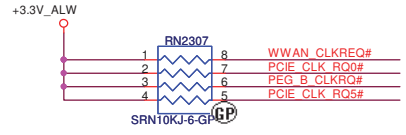
Date: Monday, March 29, 2010 Sheet 22 of 92

SSID = PCH



x01 change tolerant 20091117

PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3.3V_ALW.
PCIECLKRQ{1,2} should have a 10K pull-up to +3.3_RUN



DIS uses 0ohm 63.R0034.1DL
UMA uses 12pF 78.12034.1FL

<Core Design>

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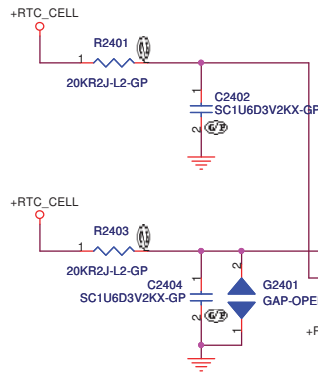
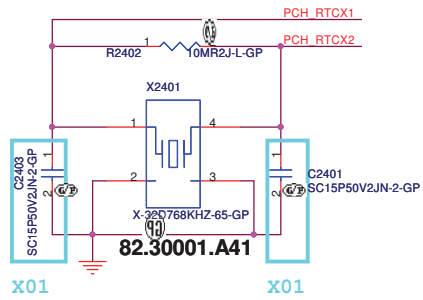
Title: **PCH (PCI-E/SMBus/CLOCK/CL)**

Size: Document Number **Berry** Rev: **A00**

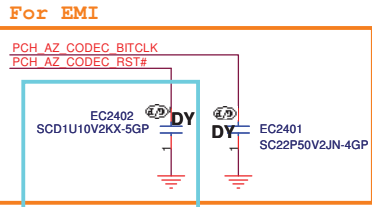
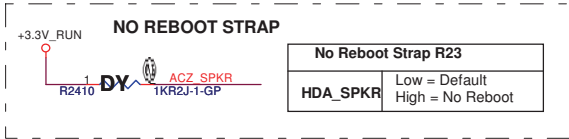
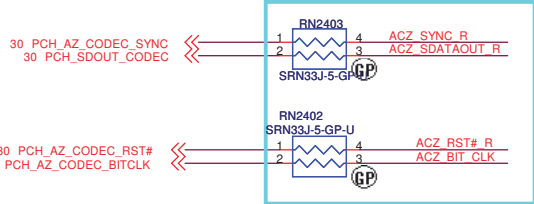
Date: Monday, March 29, 2010 Sheet 23 of 92

SSID = PCH

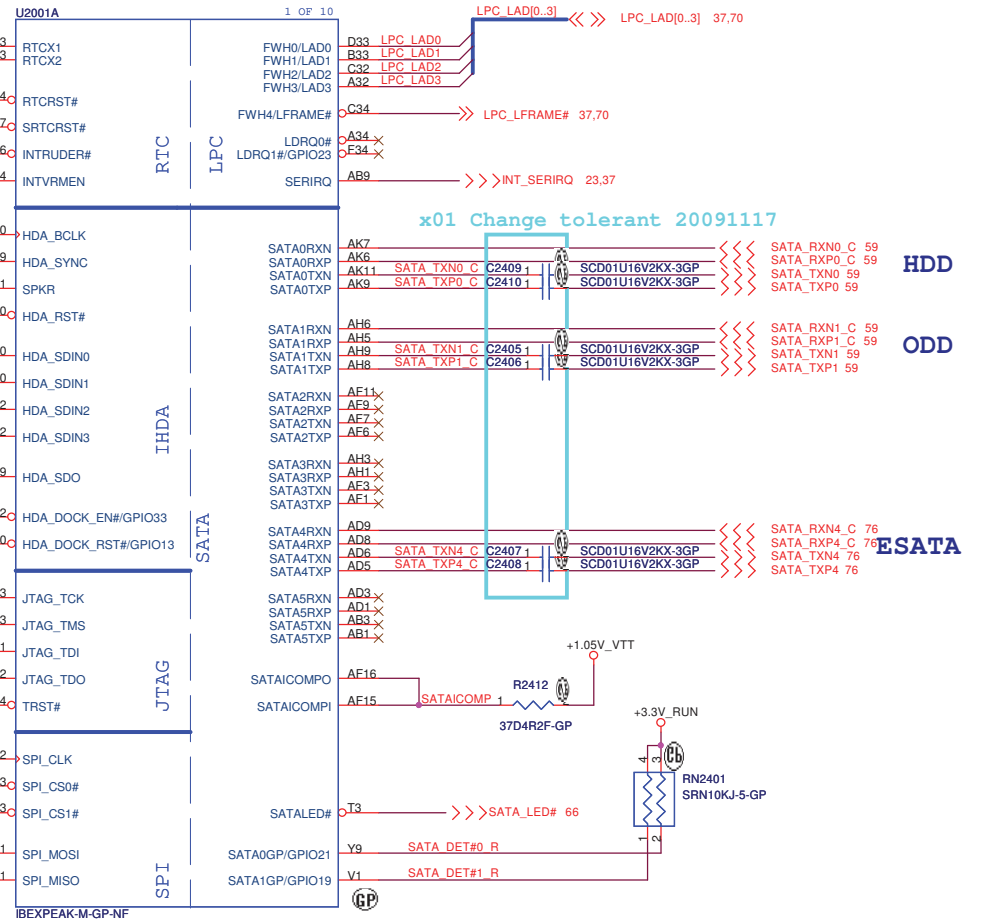
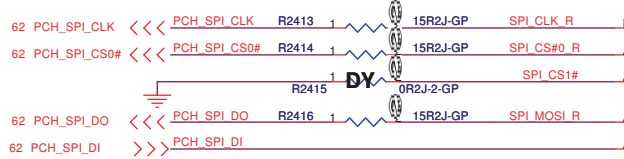
INTVRMEN- Integrated SUS
1.1V VRM Enable
High - Enable internal VRs



x01 20091118 layout swap

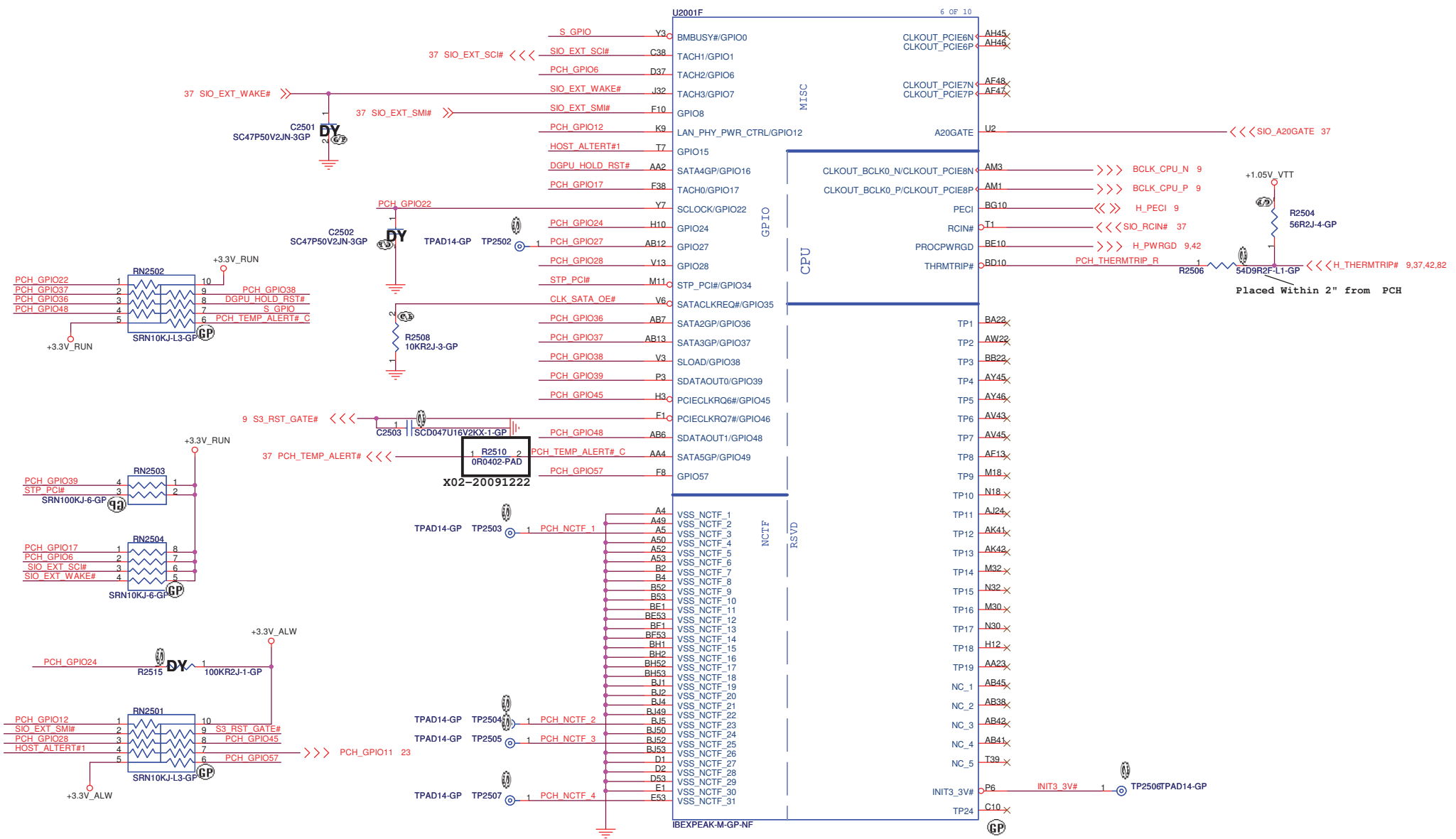


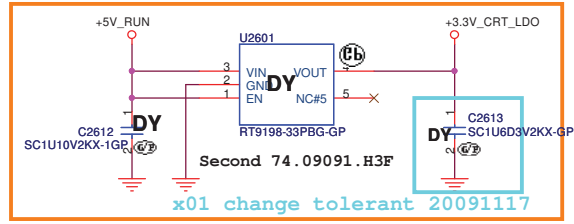
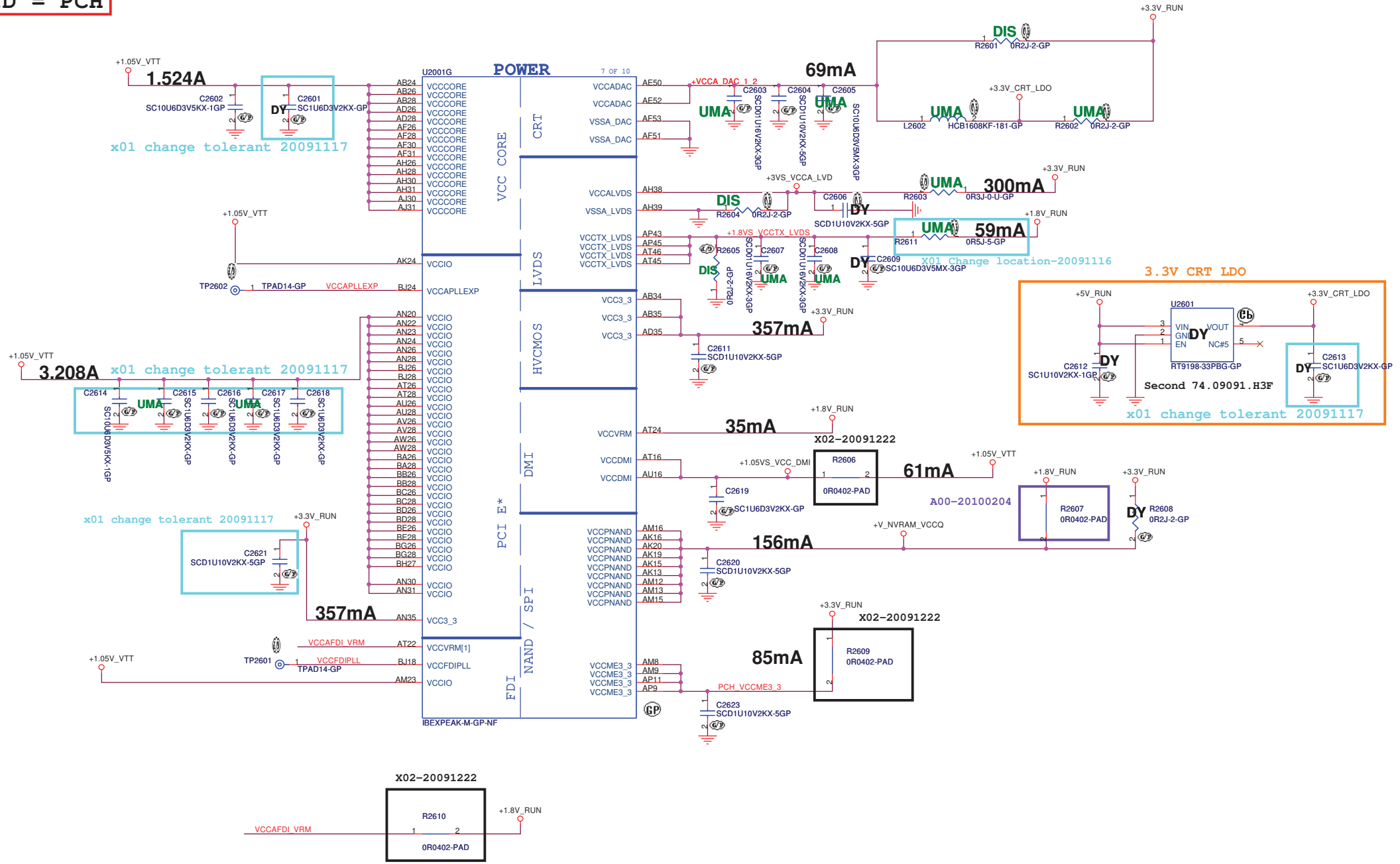
x01 Change tolerant 20091117



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Title: PCH (SPI/RTC/LPC/SATA/IHDA)
Size: Document Number
Date: Monday, March 29, 2010
Sheet 24 of 92

SSID = PCH





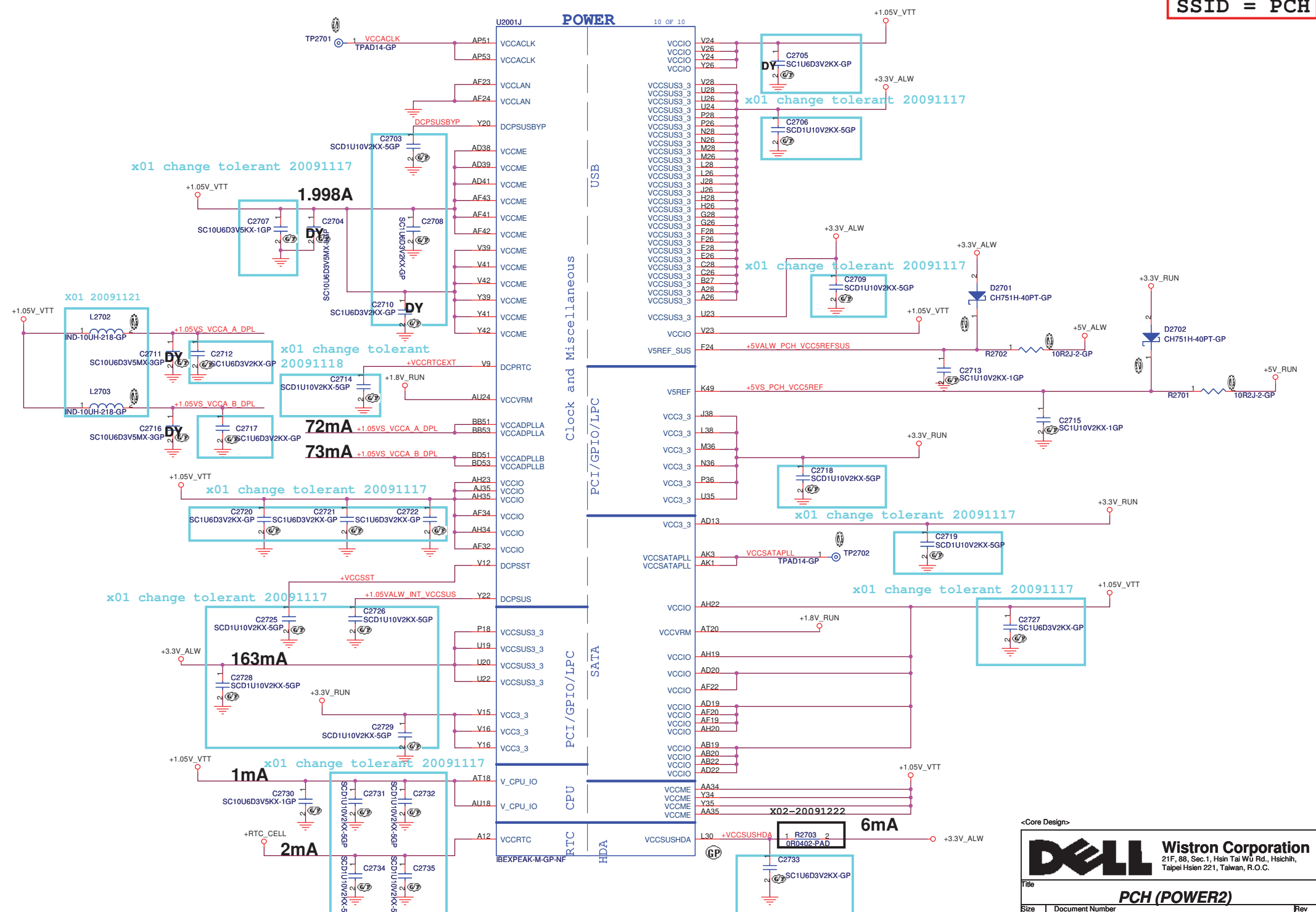
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Wistron Corporation
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Title: **PCH (POWER1)**

Size	Document Number	Rev
	Berry	A00

Date: Wednesday, February 10, 2010 Sheet 26 of 92



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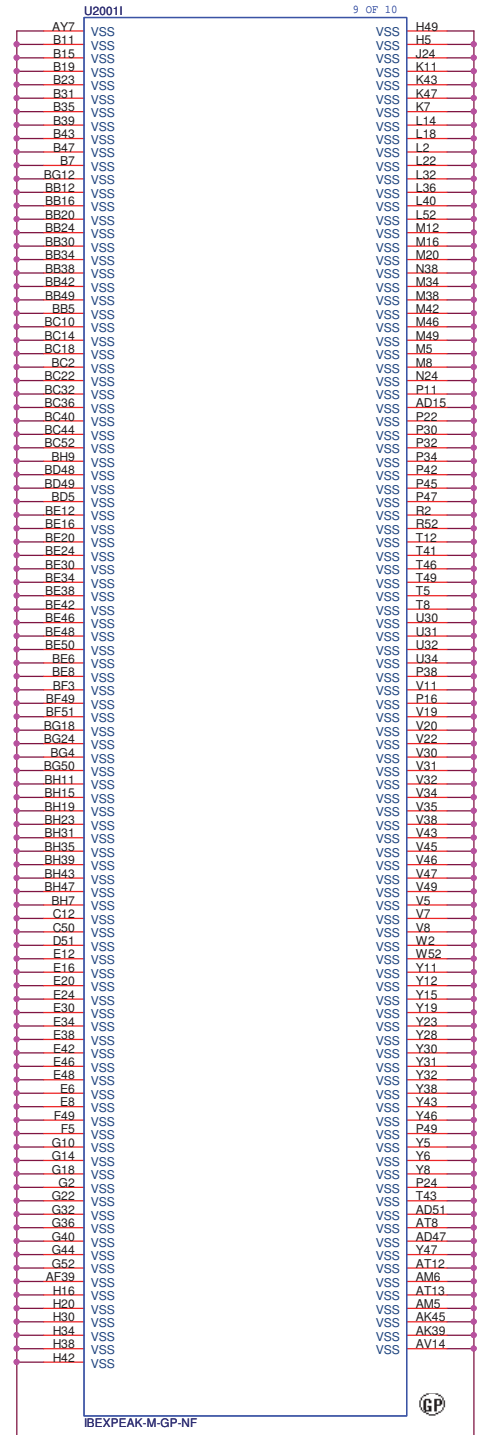
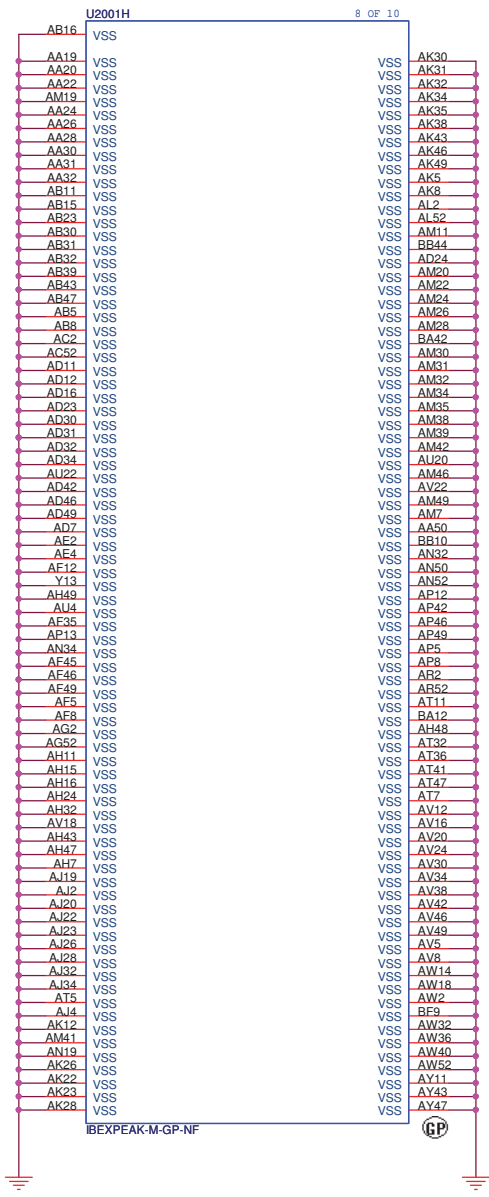
Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (POWER2)**

Size: Document Number: **Berry** Rev: **A00**

Date: Wednesday, February 10, 2010 Sheet 27 of 92

SSID = PCH



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<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.


Title: **PCH (VSS)**

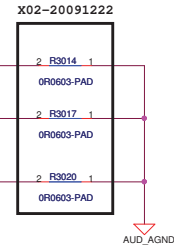
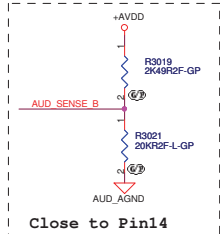
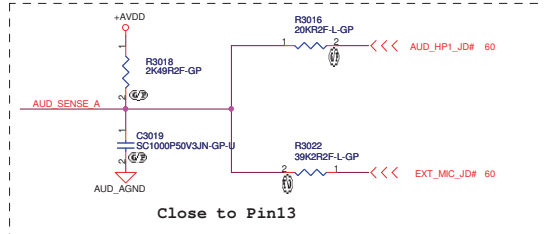
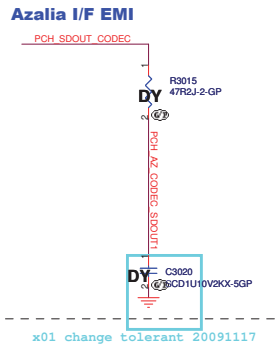
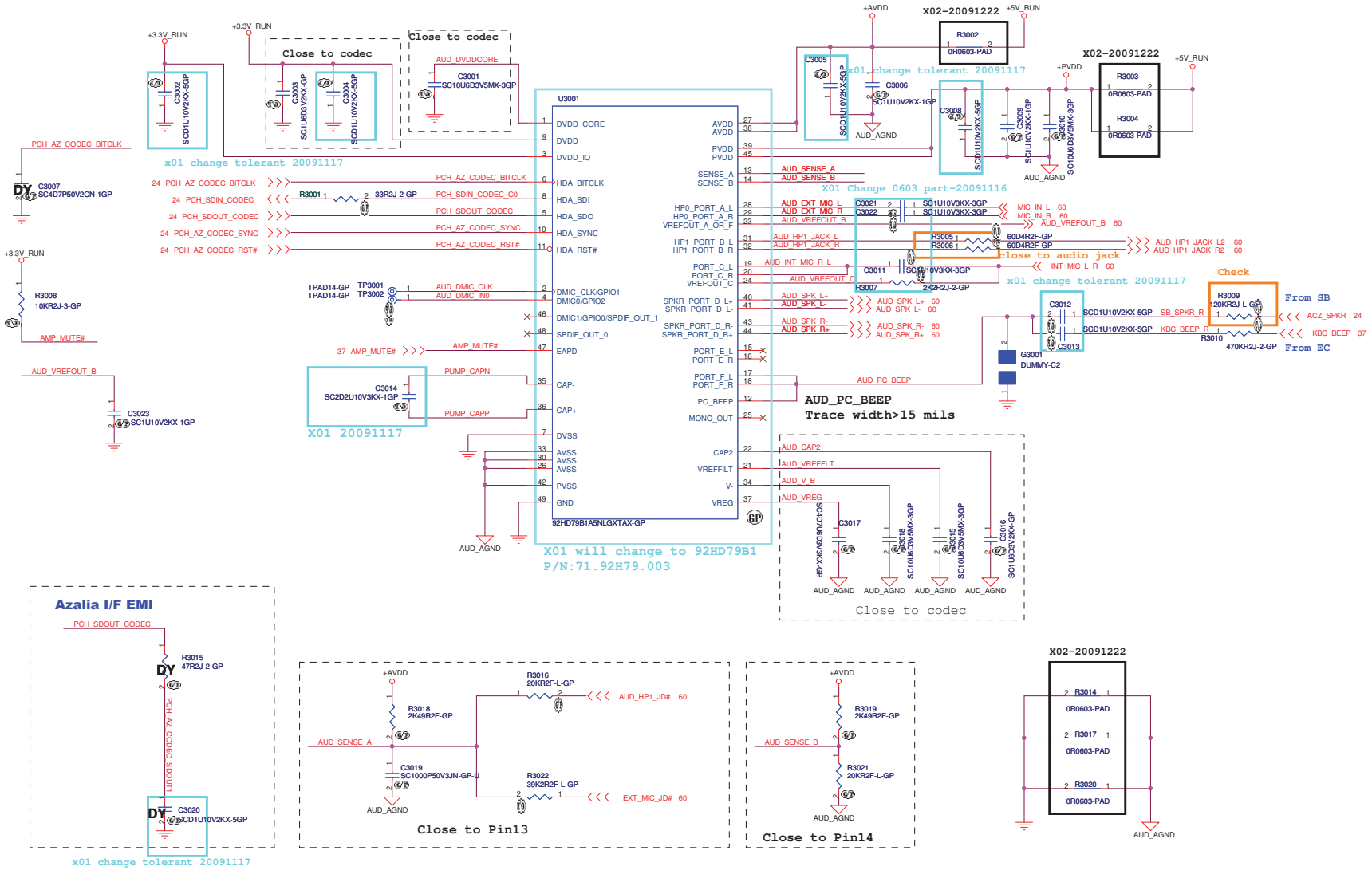
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Date: Wednesday, February 10, 2010 Sheet 28 of 92

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Date: Wednesday, February 10, 2010		Sheet 29	of 92



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Date: Wednesday, February 10, 2010		Sheet 31 of	92

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Date:	Wednesday, February 10, 2010			Sheet	32 of 92


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Date: Wednesday, February 10, 2010		Sheet 33 of	92


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Size A3	Document Number Berry	Rev A00	
Date: Wednesday, February 10, 2010		Sheet 34 of	92


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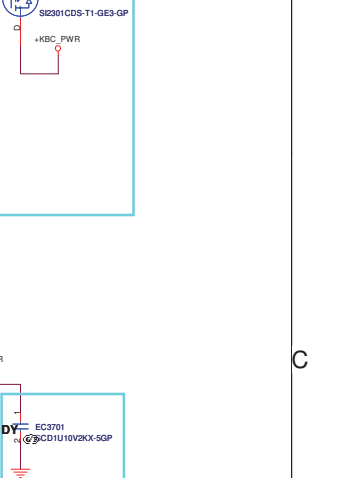
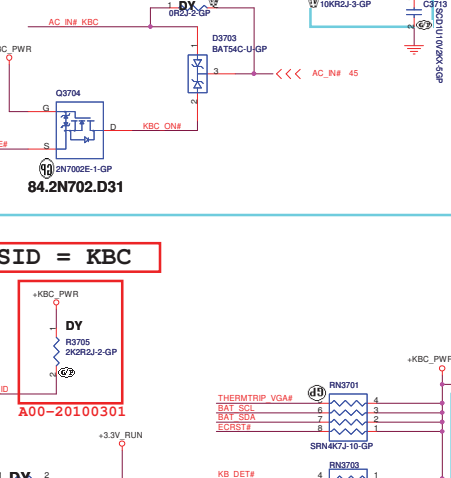
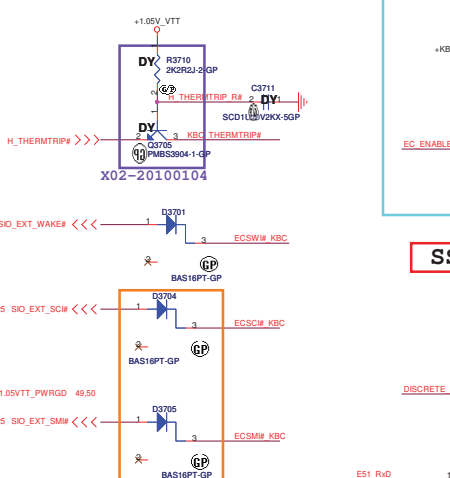
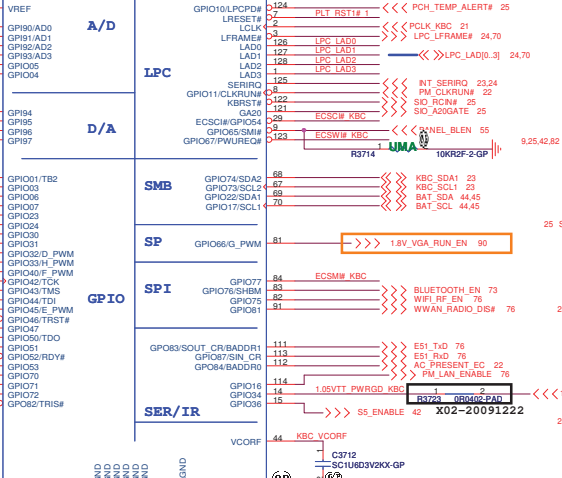
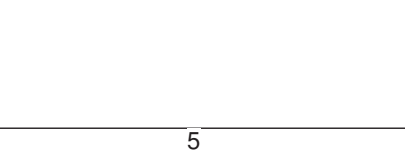
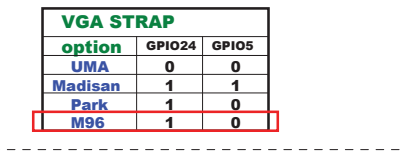
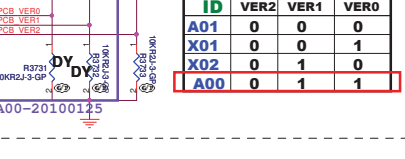
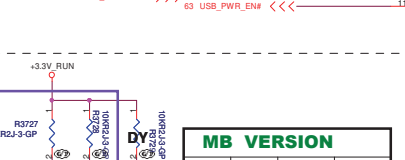
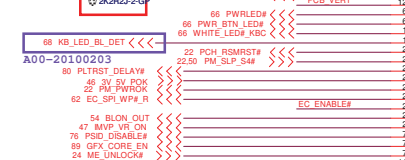
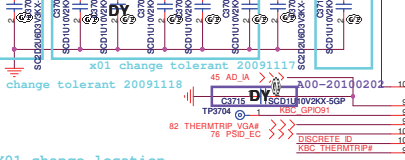
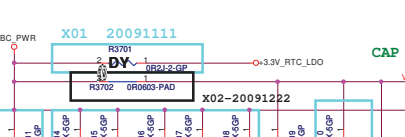
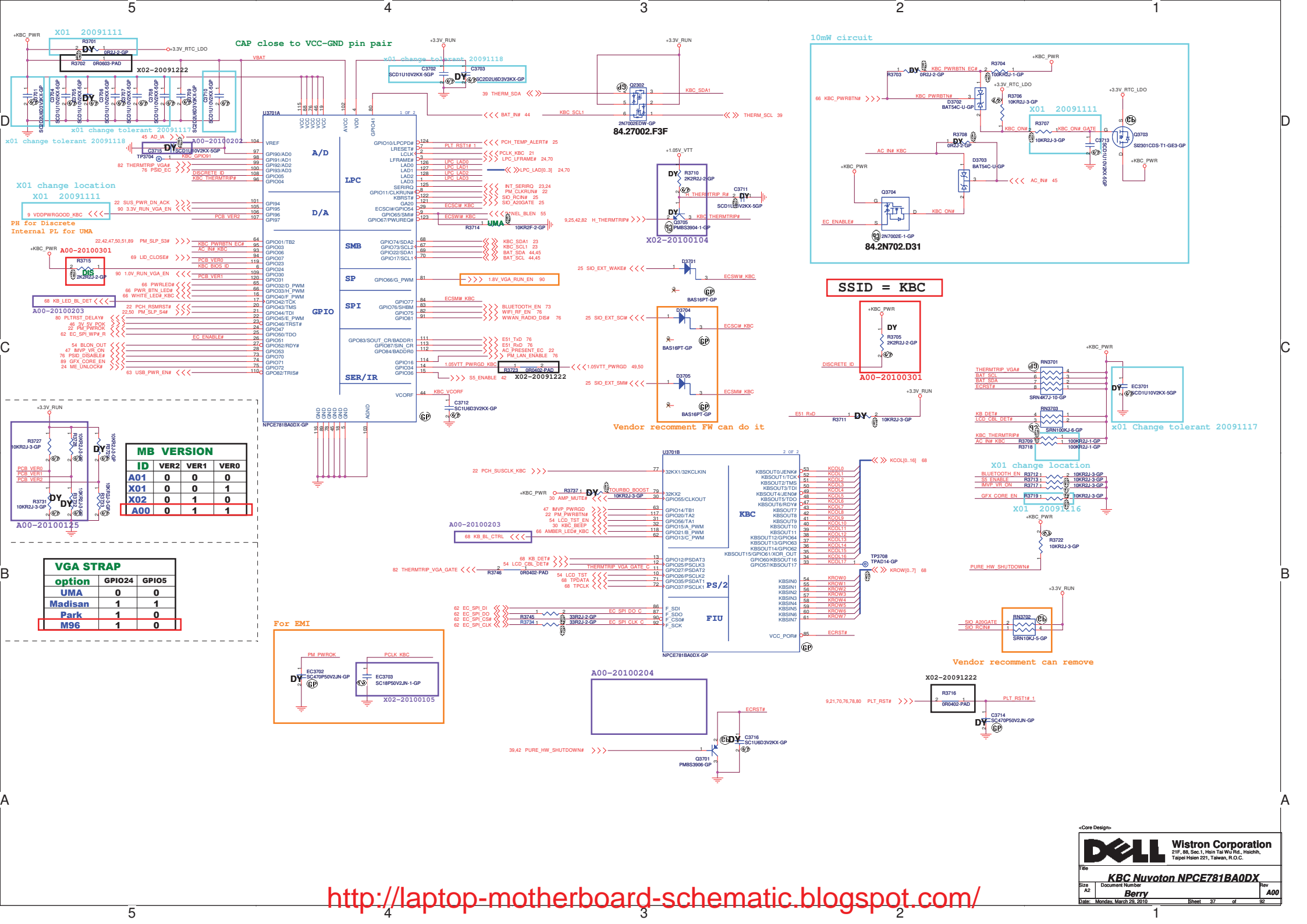
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Date: Wednesday, February 10, 2010		Sheet 35 of 92	

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Date: Wednesday, February 10, 2010		Sheet 36 of 92	

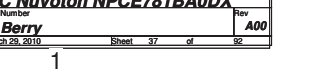
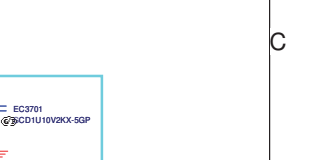
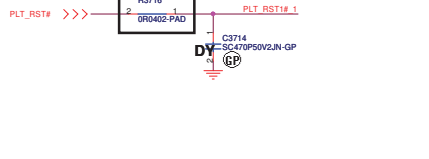
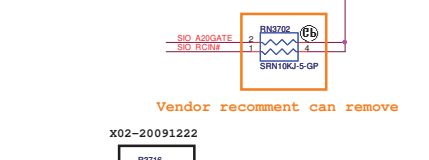
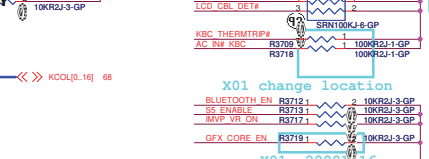
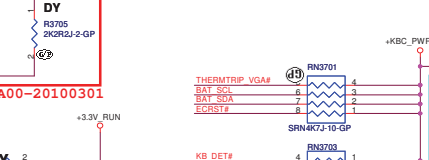
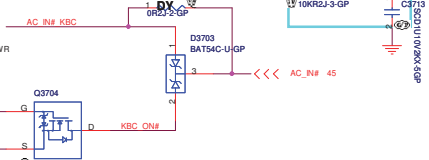
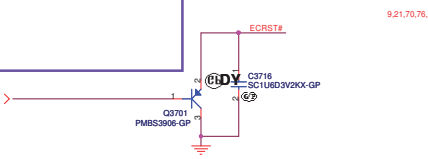
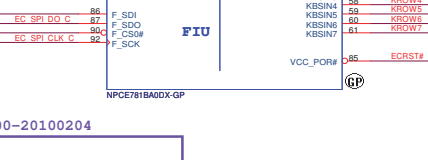
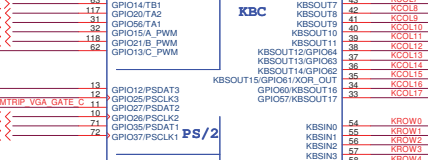
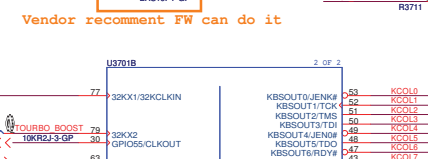
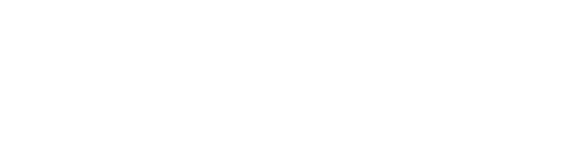
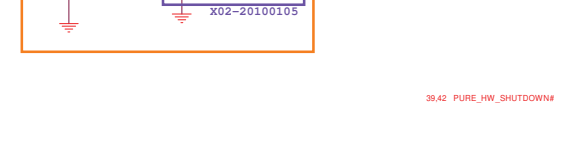
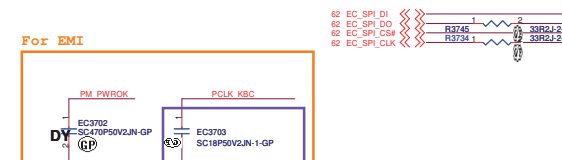
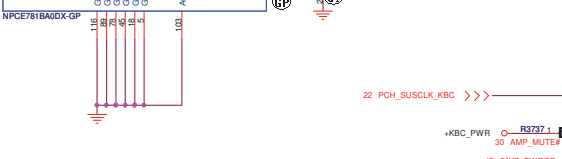


PH for Discrete Internal PL for UMA

Table with 4 columns: ID, VER2, VER1, VER0. Rows include A01, X01, X02, A00.

VGA STRAP table with 3 columns: option, GPIO24, GPIO5. Rows include UMA, Madisan, Park, M96.

Table with 4 columns: ID, VER2, VER1, VER0. Rows include A01, X01, X02, A00.



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Dell Wistron Corporation logo and document information including file name, date, and sheet number.

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Title

Reserved

Size
A4

Document Number

Berry

Rev
A00

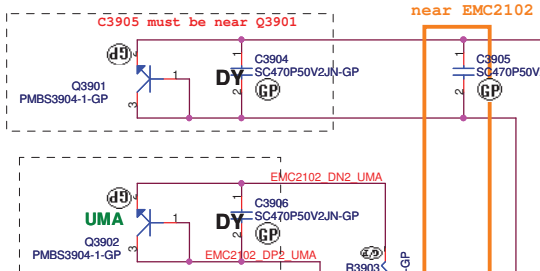
Date: Wednesday, February 10, 2010

Sheet 38 of 92

SSID = Thermal

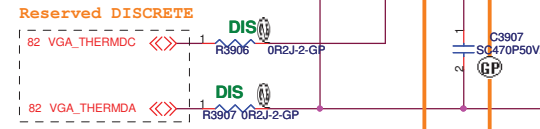
1. Place near CPU PWM CORE and PCH.

Layout notice :
Both DN1 and DP1 routing 10 mil trace width and 10 mil spacing.



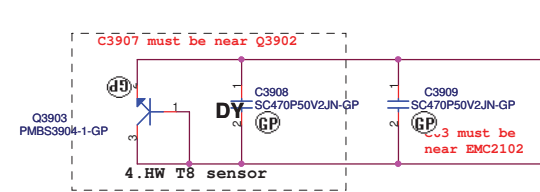
2. System Sensor (UMA Only)

Layout notice :
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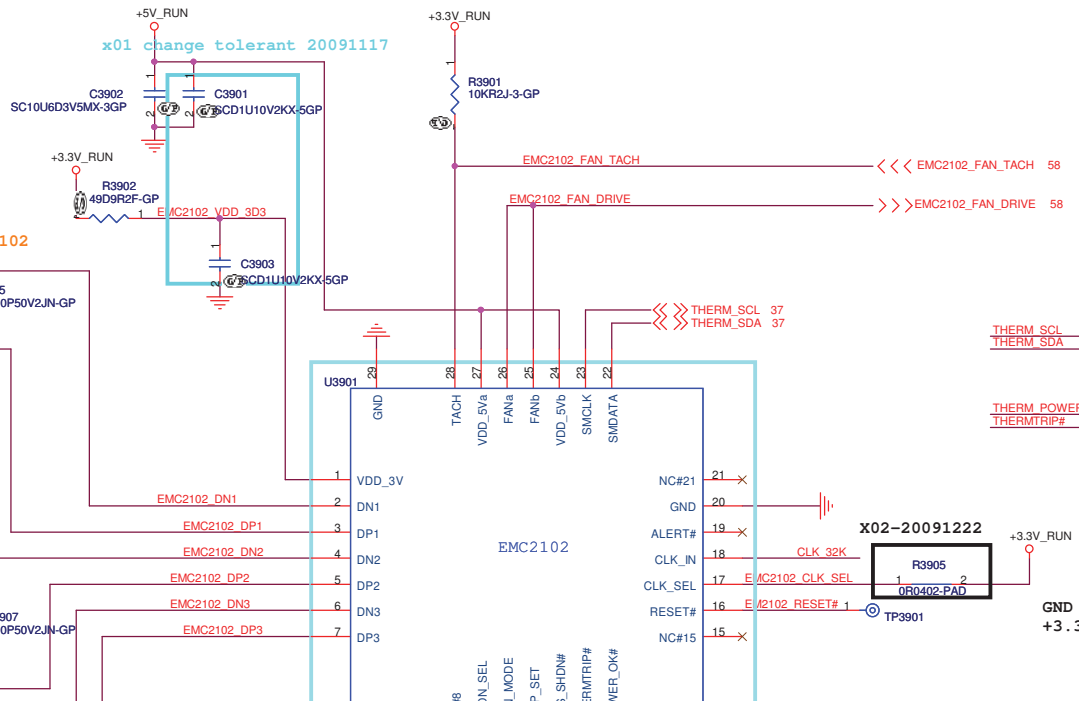
3. VGA Sensor (DISCRETE Only)

Layout notice :
Both VGA_THERMDA and VGA_THERMDC routing 10 mil trace width and 10 mil spacing.



4. HW T8 sensor

Layout notice :
Both DN3 and DP3 routing 10 mil trace width and 10 mil spacing.

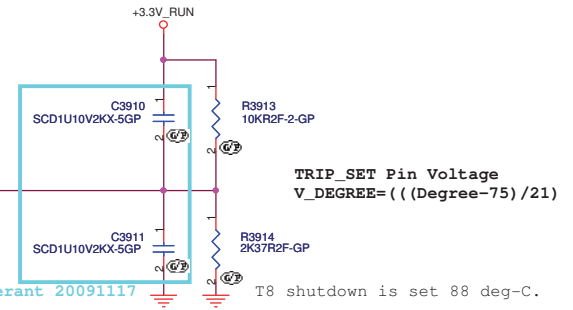
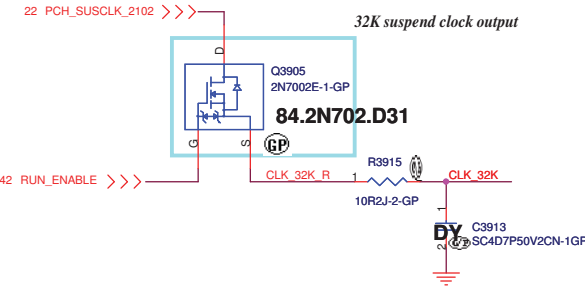


Main G7922R61U for GMT P/N:74.07922.0B3
SEC. EMC2102 for SMSC P/N:74.02102.A73

GND = Channel 1
OPEN = Channel 3
+3.3V = Disabled

GND = Fan is OFF
OPEN = Fan is at 60% full-scale
+3.3V = Fan is at 75% full-scale

GND = Internal Oscillator Selected
+3.3V = External 32.768kHz Clock Selected




TRIP_SET Pin Voltage
 $V_DEGREE = ((Degree-75)/21)$

T8 shutdown is set 88 deg-C.


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<Core Design>

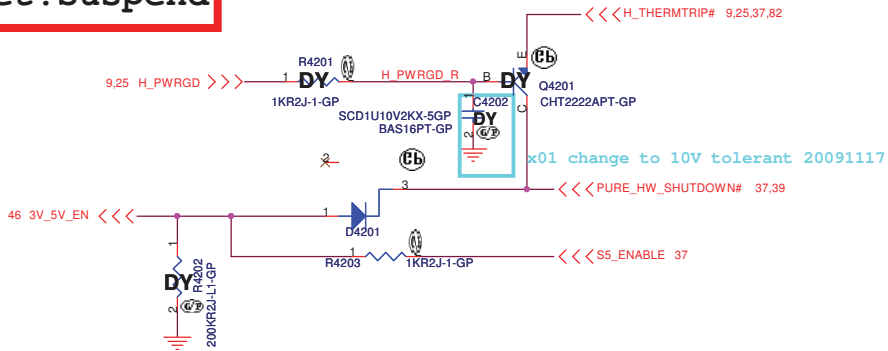
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Size	Document Number	Rev	
A3	Berry	A00	
Date:	Wednesday, February 10, 2010	Sheet 40 of 92	

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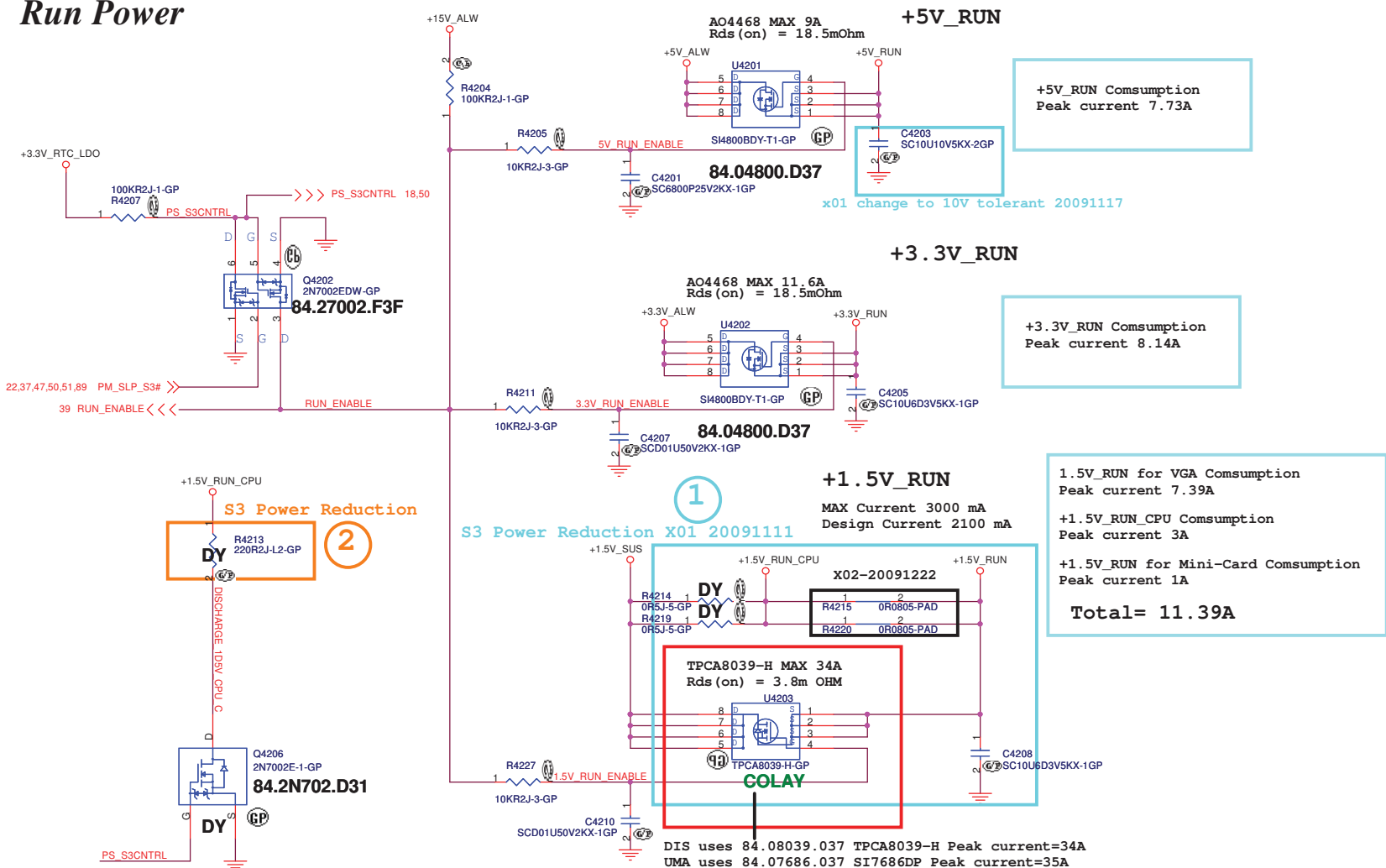
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Title		
Reserved		
Size A3	Document Number Berry	Rev A00
Date: Wednesday, February 10, 2010		Sheet 41 of 92

SSID = Reset.Suspend



Run Power



1

2

DIS uses 84.08039.037 TPCA8039-H Peak current=34A
 UMA uses 84.07686.037 SI7686DP Peak current=35A

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Title: **Power Plane Enable**

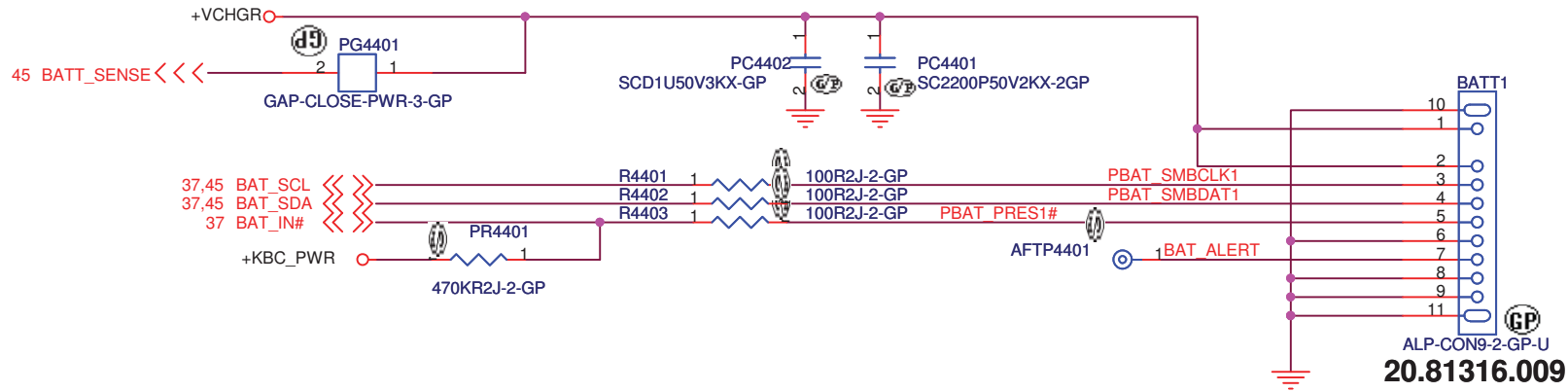
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Date: Monday, March 29, 2010	Sheet 42 of 92	

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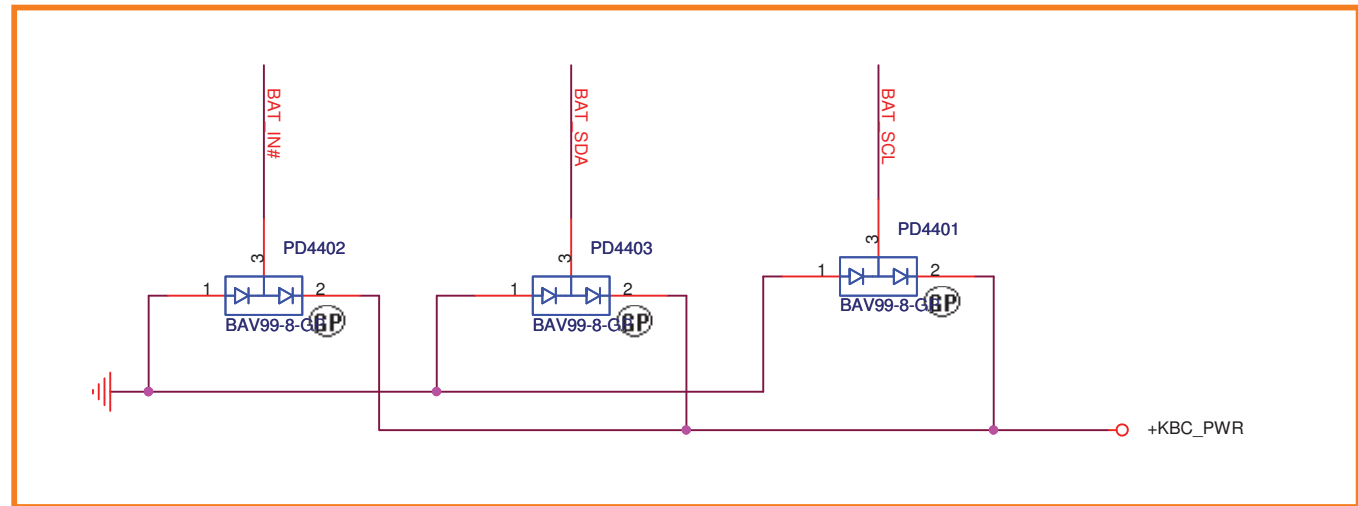
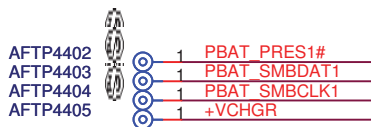
		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		Reserved
Size A3	Document Number Berry	Rev A00
Date: Wednesday, February 10, 2010		Sheet 43 of 92

Batt Connector



For actual location, need to be swap all pin

Close to Batt Connector



<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

BATT CONN

Size
A4

Document Number

Berry

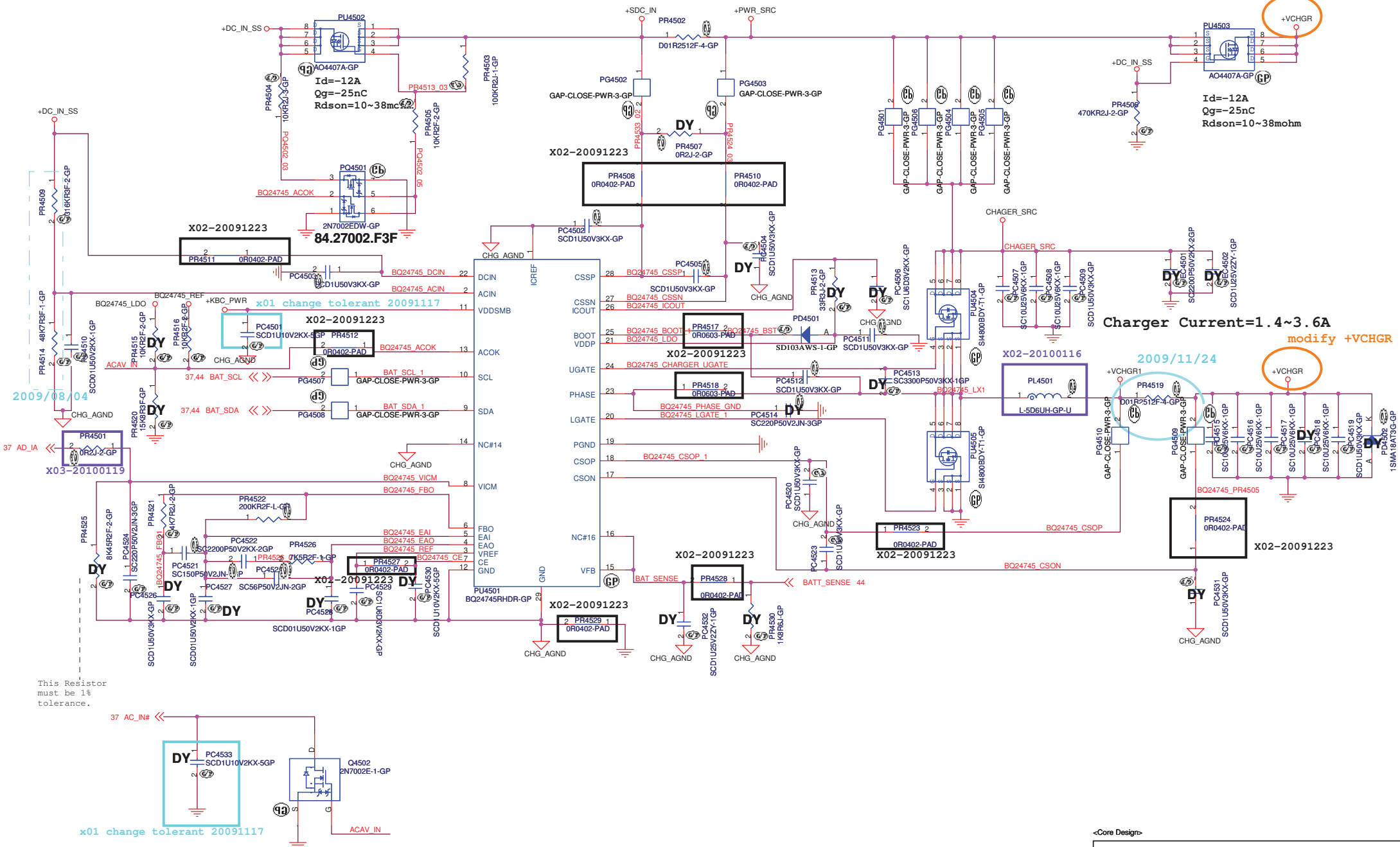
Rev

A00

Date: Monday, March 29, 2010

Sheet 44 of 92

SSID = Charger



This Resistor must be 1% tolerance.

x01 change tolerant 20091117

<http://laptop-motherboard-schematic.blogspot.com/>

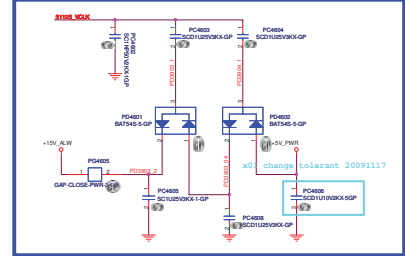
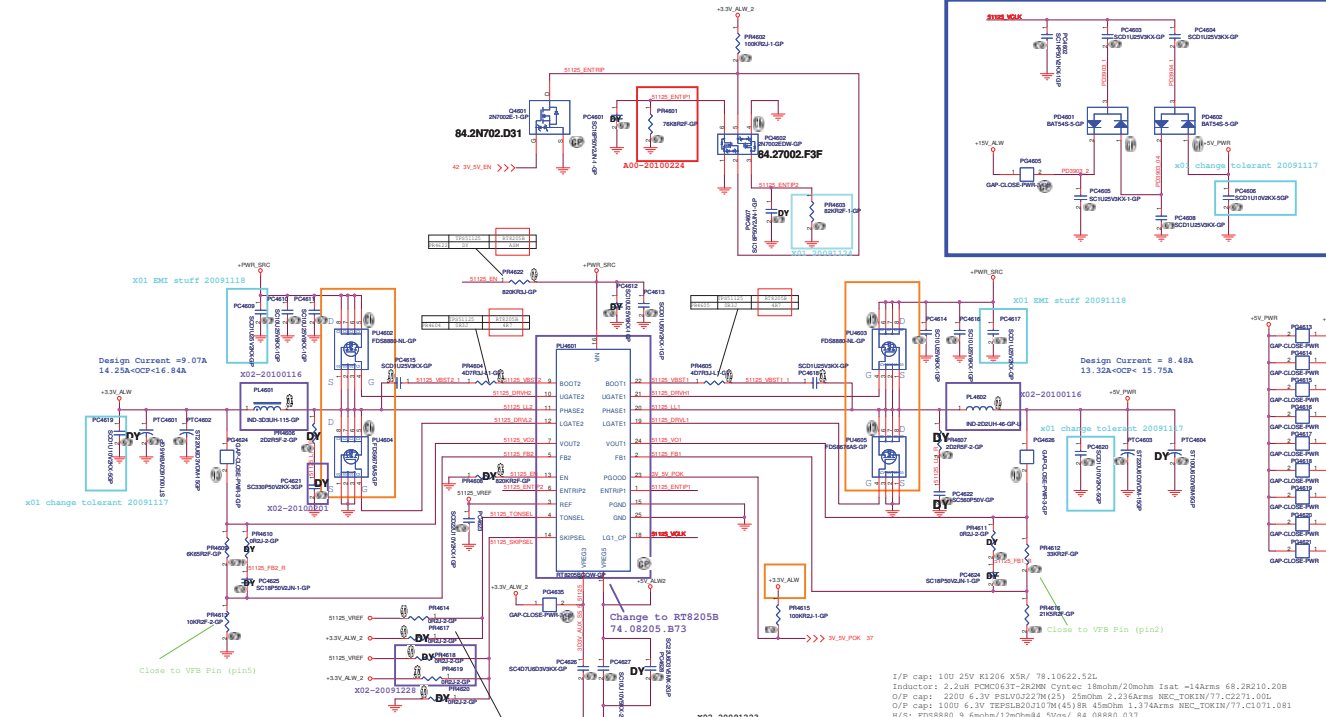
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Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **CHARGER BQ24745**

Size	Document Number	Rev
Custom	Berry	A00

Date: Monday, March 29, 2010 Sheet 45 of 92



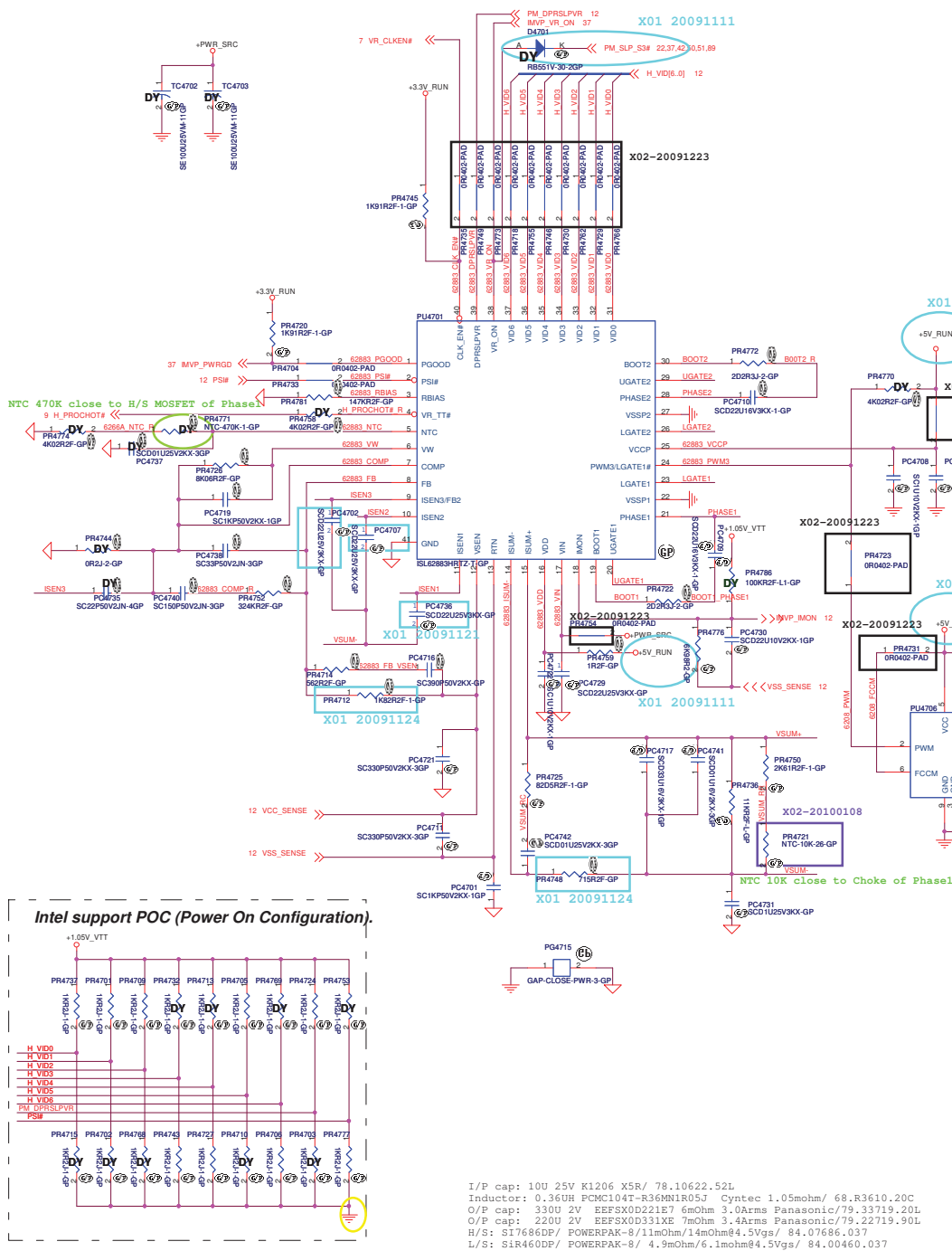
I/P cap: 10U 25V K1206 XSR/ 78.10622.52L
 Inductor: 3.20U PCMB1047-3K0M3 Cytotec 10.5mohm/11.8mohm Isat -16Arms 68.2R210.20C
 O/P cap: 220U 6.3V PSL10J227M(45) 250mohm 2.236Arms NEC_TORIN/77.C2271.00L
 O/P cap: 100U 6.3V TEPFLB20107M(45)8R 45mohm 1.374Arms NEC_TORIN/77.C1071.081
 W/S: FDS6890 9.6mohm/1.2mohm@4.5Vgs/ 84.06880.A37
 L/S: FDS6676AS 5.9mohm/7.25mohm@4.5Vgs/ 84.06676.A37

I/P cap: 10U 25V K1206 XSR/ 78.10622.52L
 Inductor: 2.20U PCMC6371-2R20R Cytotec 18mohm/20mohm Isat -14Arms 68.2R210.20B
 O/P cap: 220U 6.3V PSL10J227M(45) 250mohm 2.236Arms NEC_TORIN/77.C2271.00L
 O/P cap: 100U 6.3V TEPFLB20107M(45)8R 45mohm 1.374Arms NEC_TORIN/77.C1071.081
 W/S: FDS6890 9.6mohm/1.2mohm@4.5Vgs/ 84.06880.A37
 L/S: FDS6676AS 5.9mohm/7.25mohm@4.5Vgs/ 84.06676.A37

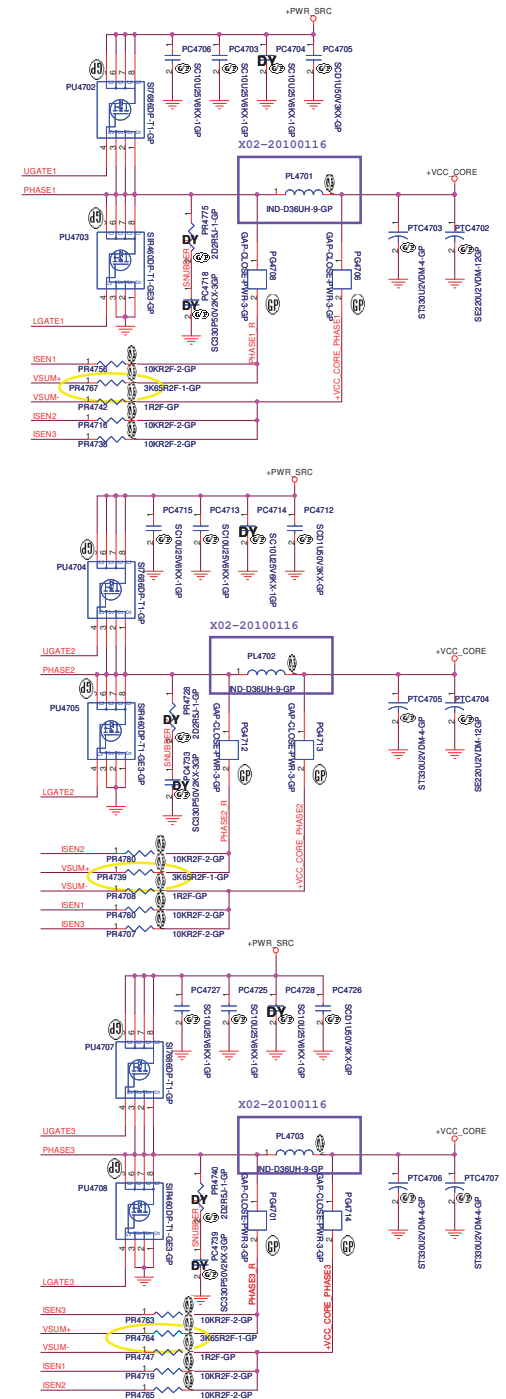
TONSEL	CH1	CH2	REFPSEL	VREG5 or VREG5	VREF (V)	GRD
GRD	200KHz	265KHz	OperatLing Mode	Onk Auto Skip	Auto Skip	PWM only
VREF	245KHz	305KHz				
VREG3	300KHz	375KHz				
VREG5	365KHz	460KHz				

ENO	Operating Mode	Open	820kΩ to GRD	GRD
		enable both ID0V_VCLK on and ready to turn on switcher channels	enable both ID0V_VCLK off and ready to turn on switcher channels	disable all circuit

TONSEL	CH1	CH2
GRD	200KHz	265KHz
VREF	300KHz	375KHz
VREG3	365KHz	460KHz
VREG5	365KHz	460KHz



I/P cap: 10u 25V K1206 X5R/ 78.10622.52L
 Inductor: 0.36uH PCMC104T-R36M1R05J Cynotec 1.05mohm/ 68.R3610.20C
 O/P cap: 330u 2V EEF5X0D221E7 6mOhm 3.0Arms Panasonic/79.33719.20L
 O/P cap: 220u 2V EEF5X0D331XE 7mOhm 3.4Arms Panasonic/79.22719.90L
 H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
 L/S: SIR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037




Design Current = 48A
 52.8A-OCp<67.2A

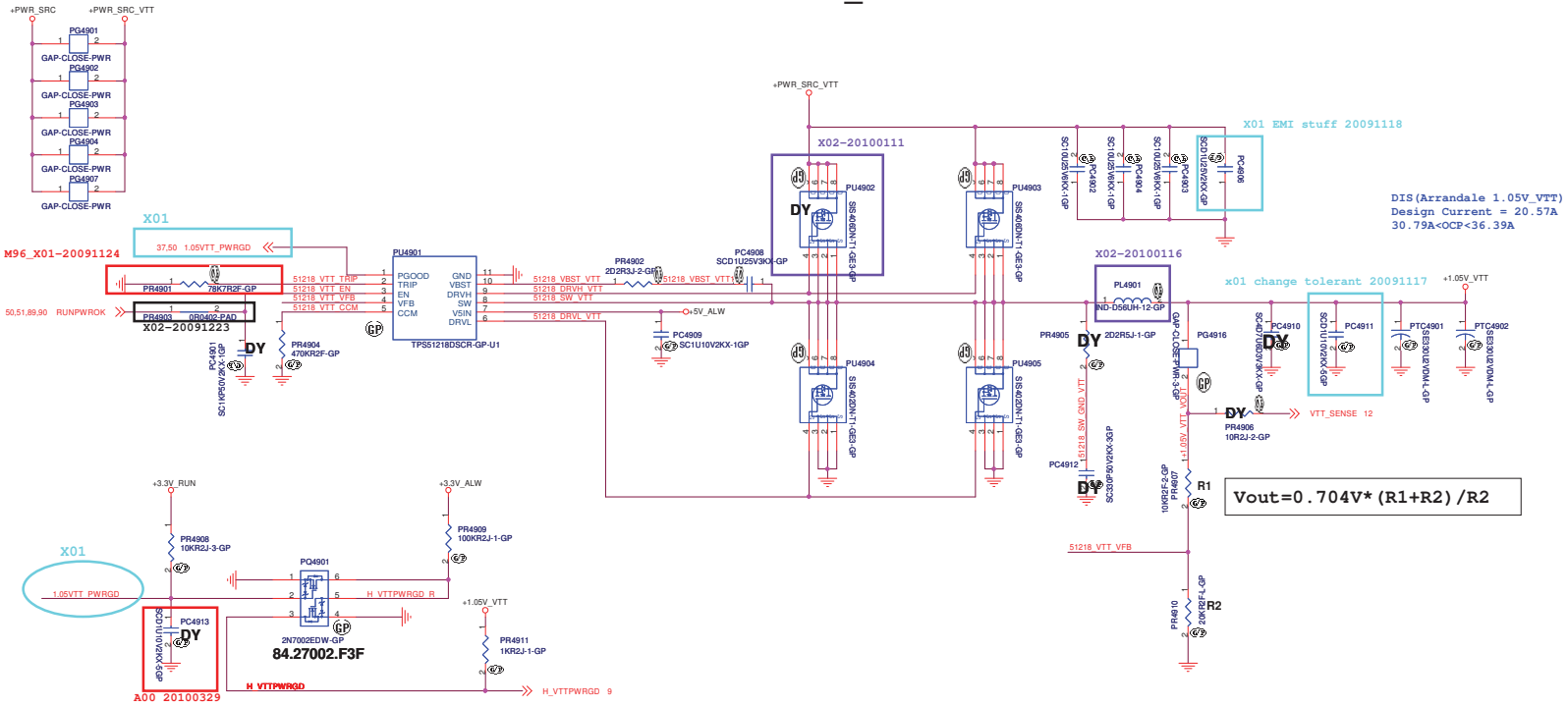
~Core Design~
DELL **Wistron Corporation**
 21F, 8L, Sec.1, Hsin Tai Wu Rd., Hsueh,
 Taipei Hsien 221, Taiwan, R.O.C.
 File
ISL62883_CPU_CORE
 Size A0 Document Number
 Berry
 Date: Monday, March 29, 2010 Sheet 47 of 92 Rev A00

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		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size A3	Document Number Berry	Rev A00	
Date: Wednesday, February 10, 2010		Sheet 48 of	92

TPS51218 for +1.05V_VTT



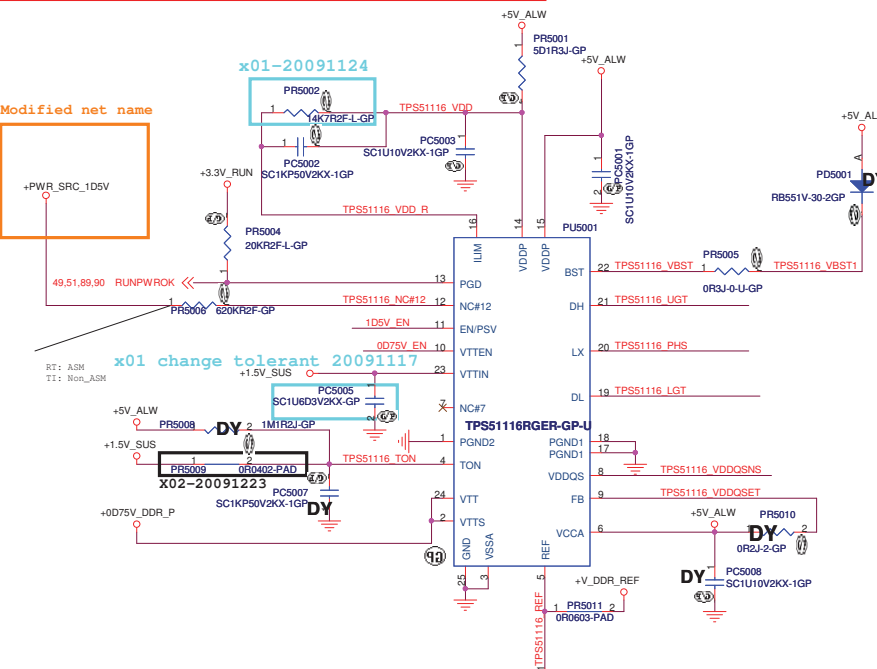
DIS (Arrandale 1.05V_VTT)
Design Current = 20.57A
30.79A<OCP<36.39A

$$V_{out} = 0.704V * (R1+R2) / R2$$

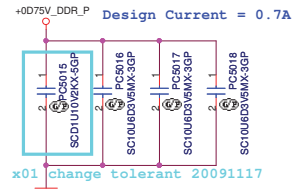
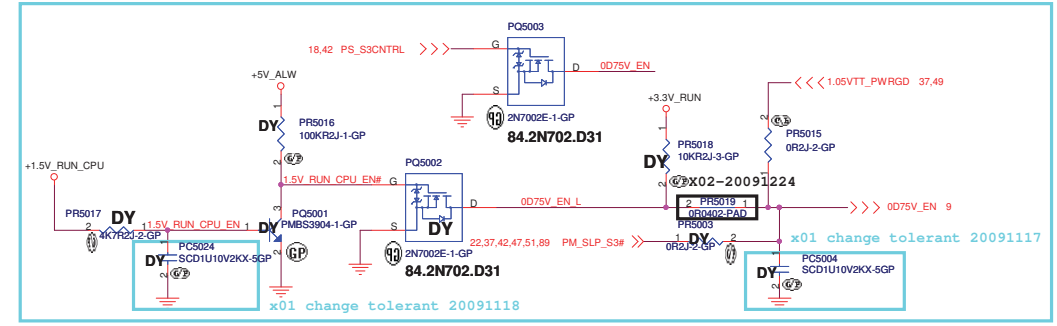
Frequency setting	
470K	-->290KHZ
200K	-->340KHZ
100K	-->380KHZ
39K	-->430KHZ

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R564M Cynotec DCR:1.6mohm/1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 330U 2.5V EEFSX0D331ER 9mOhm 3Arms PANASONIC/ 79.33719.L01
H/S: S1S406DN/ POWERPAK-8/ 11.5mOhm/14.5mOhm @4.5Vgs/ 84.00406.037
L/S: S1S402DN/ POWERPAK-8/ 6.4mOhm/8mohm@4.5Vgs/ 84.00402.037

SSID = PWR.Plane.Regulator_1p5v0p7



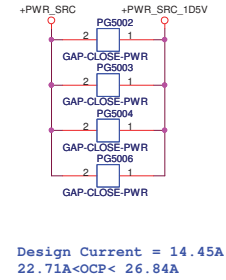
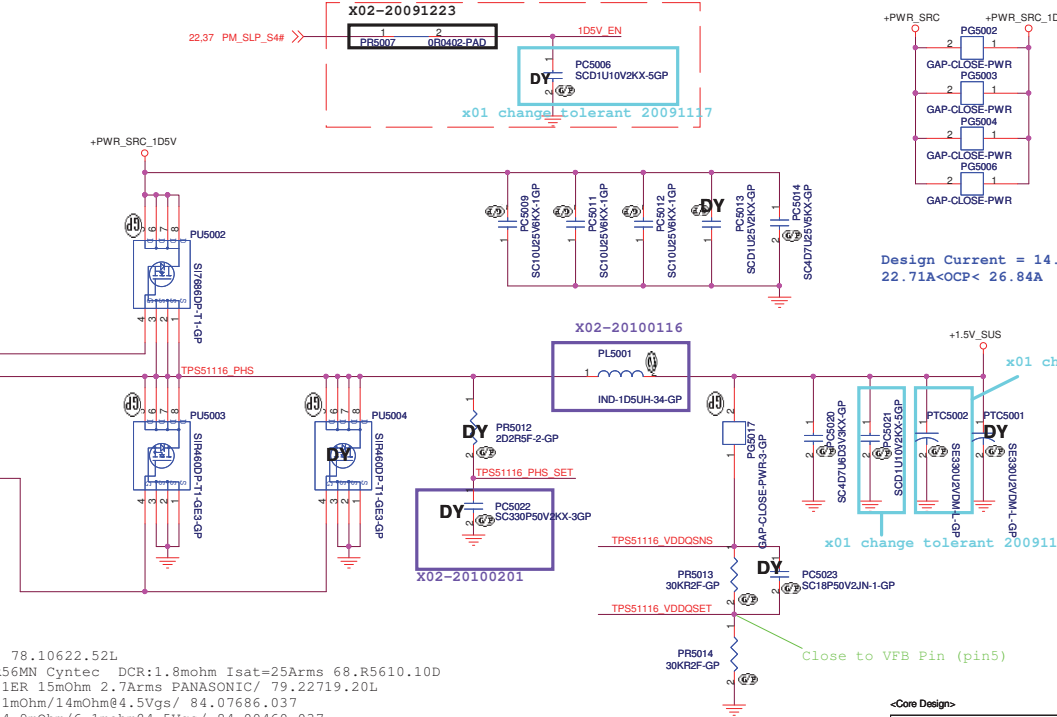
5 S3 Power Reduction X01 20091111



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VDDQSNS/2	DDR
V5IN	1.8	VDDQSNS/2	DDR2
FB Resistors	Adjustable	VDDQSNS/2	1.5 V < VDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
 Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.8mohm Isat=25Arms 68.R5610.10D
 O/P cap: 220U 2V EEFCX0D221ER 15mOhm 2.7Arms PANASONIC/ 79.22719.20L
 H/S: Si7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
 L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037
 Switching freq-->400KHz



Core Design

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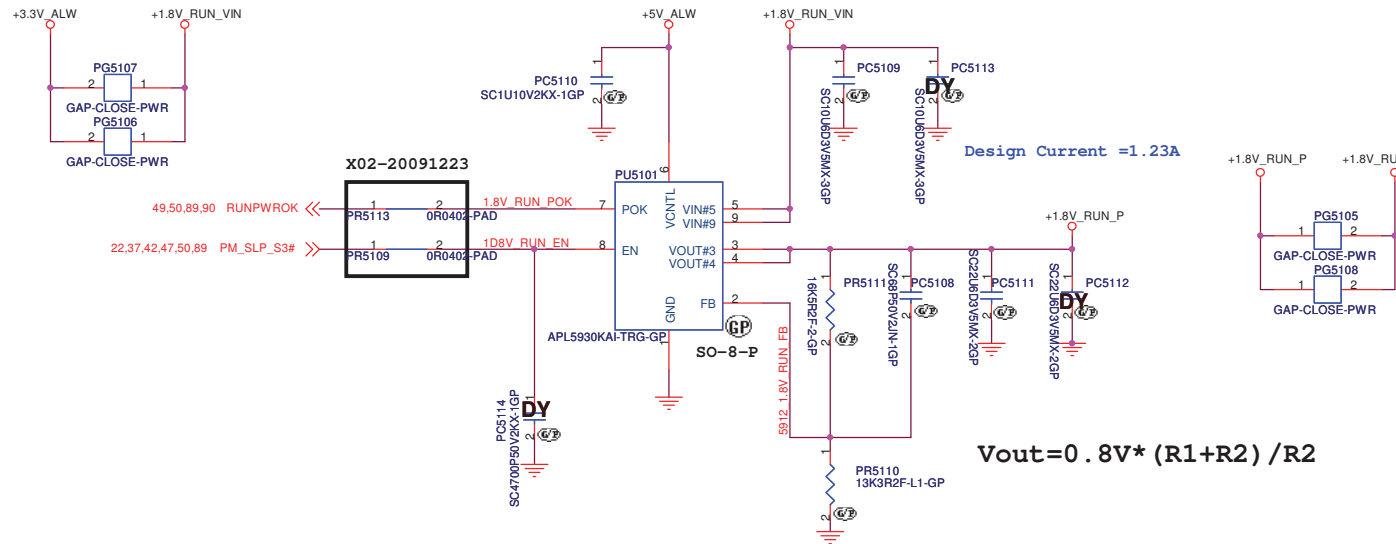
Title: **TPS51116 +1.5V_SUS**

Size: Document Number
 Custom: **Berry** Rev: **A00**

Date: Monday, March 29, 2010 Sheet 50 of 92


SSID = PWR.Plane.Regulator_1p8v

APL5930 for +1.8V_RUN




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<Core Design>

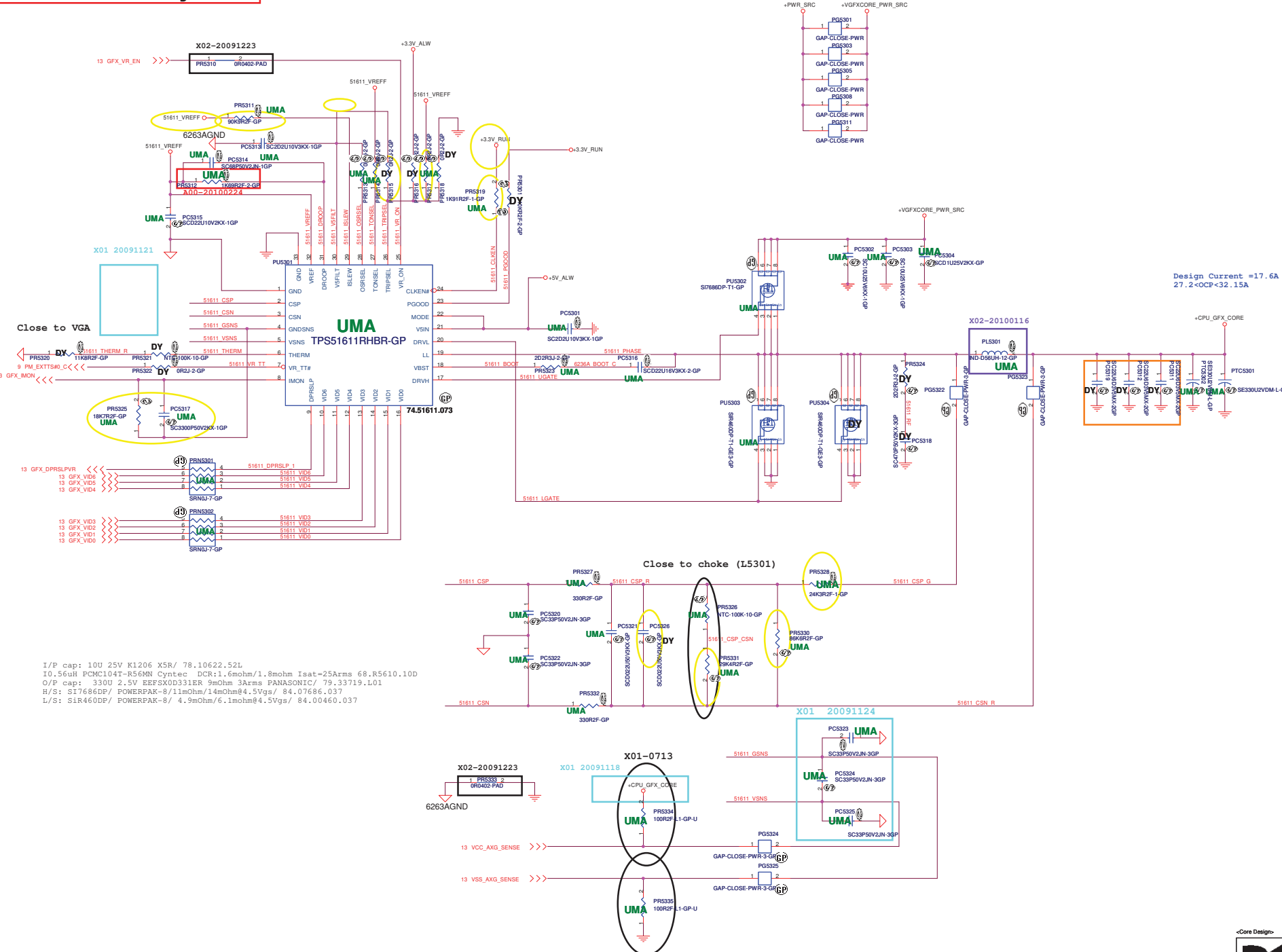
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Title: APL5930 +1.8V RUN		
Size: A3	Document Number: Berry	Rev: A00
Date: Monday, March 29, 2010		
Sheet 51 of 92		

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<Core Design>

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size A3	Document Number Berry	Rev A00	
Date: Wednesday, February 10, 2010		Sheet 52 of 92	

SSID = CPU.GFX.Regulator



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<Core Design>

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 Taipei Hsien 221, Taiwan, R.O.C.

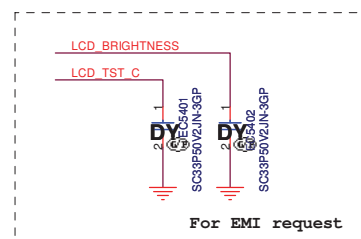
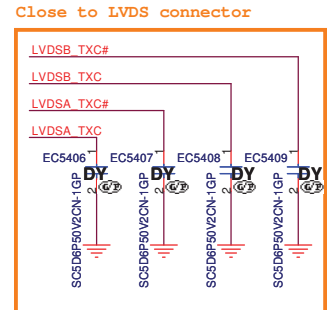
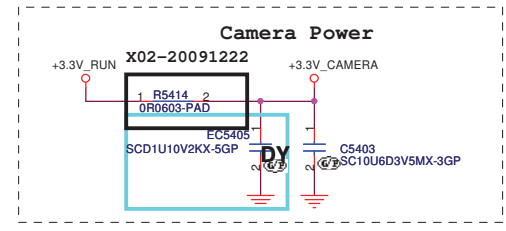
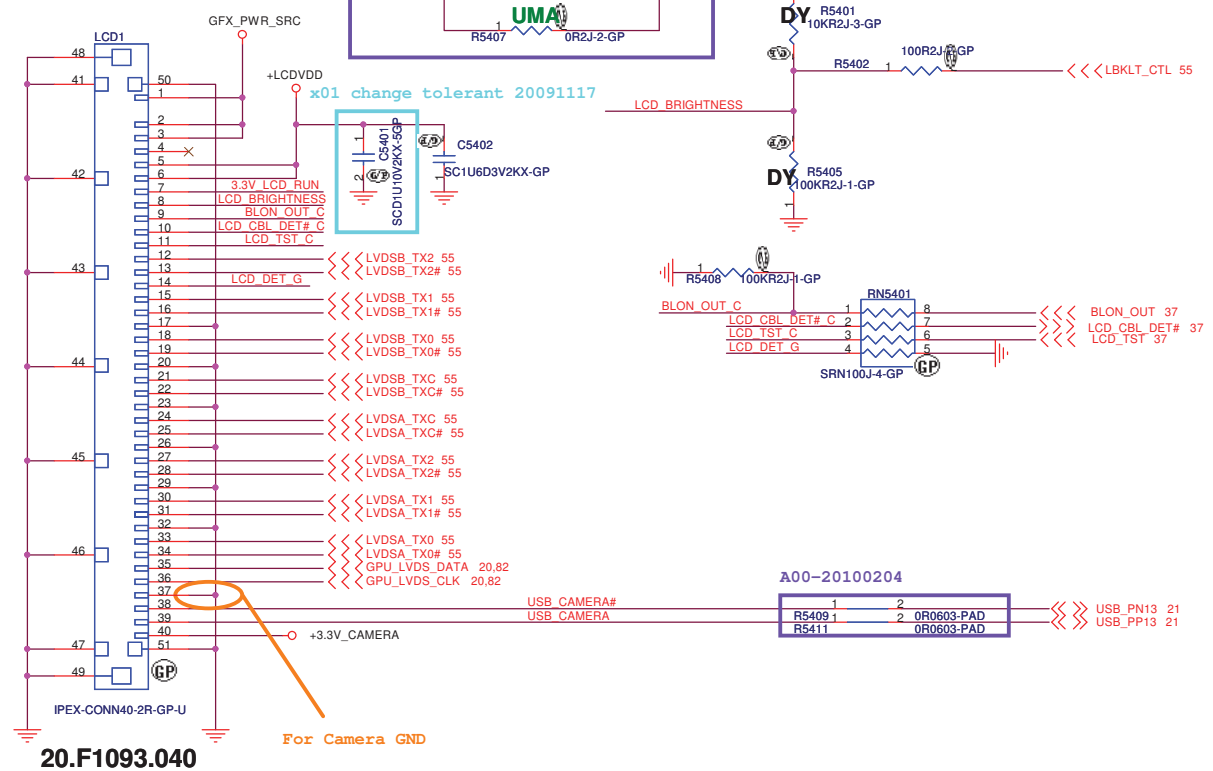
Title: **TPS51611_+GFX_CORE(UMA)**

Size: A4 Document Number: **Berry** Rev: **A00**

Date: Monday, March 29, 2010 Sheet: 63 of 92

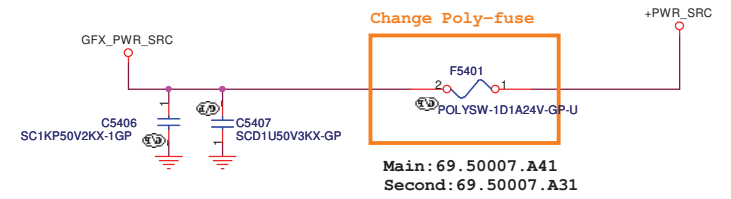
SSID = VIDEO

LVDS CONNECTOR



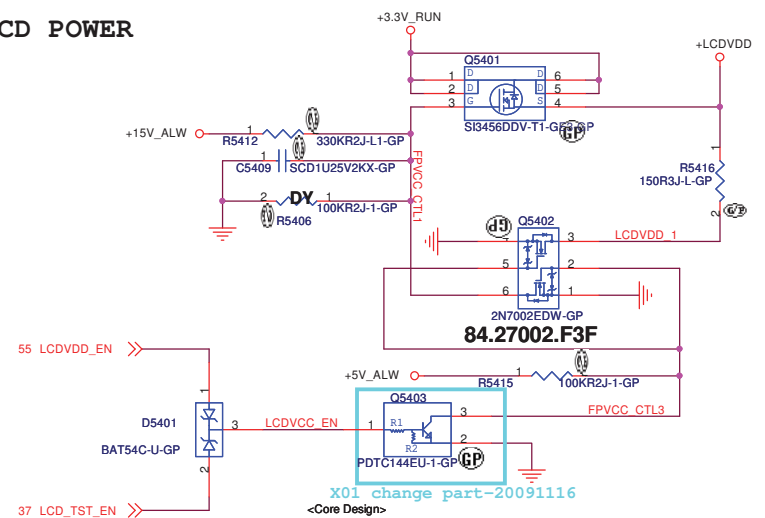
SSID = Inverter

INVERTER POWER



SSID = VIDEO

LCD POWER

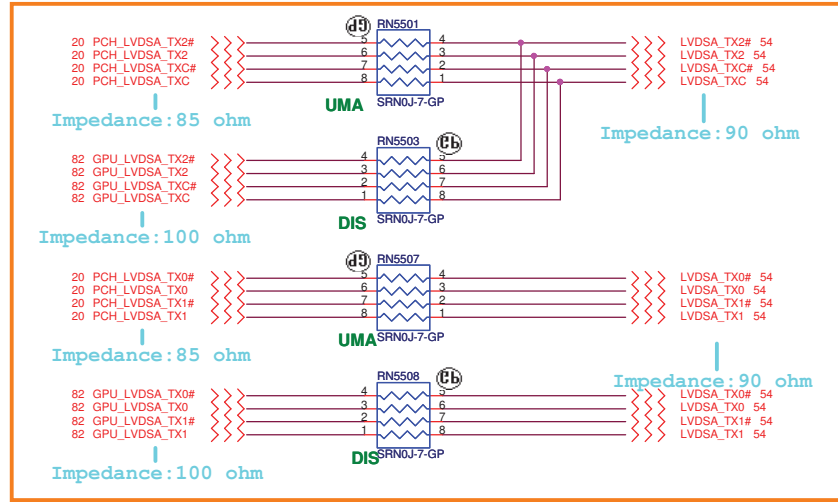


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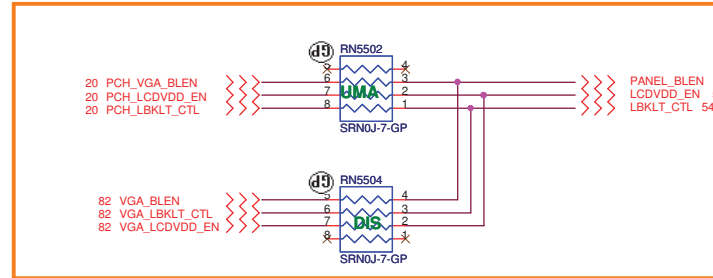
Title: **LCD/Inverter Connector**

Size A3	Document Number Berry	Rev A00
Date: Monday, March 29, 2010	Sheet 54 of	92

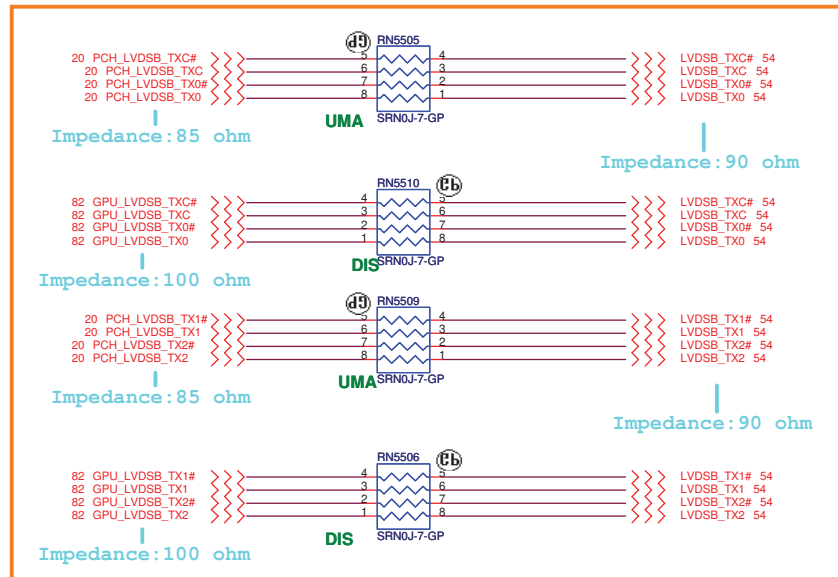
LVDS Channel A




Panel BL brightness/Power En/BL En



LVDS Channel B




<Core Design>

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Size	Document Number	Rev
	Berry	A00
Date: Monday, March 29, 2010	Sheet 55 of 92	

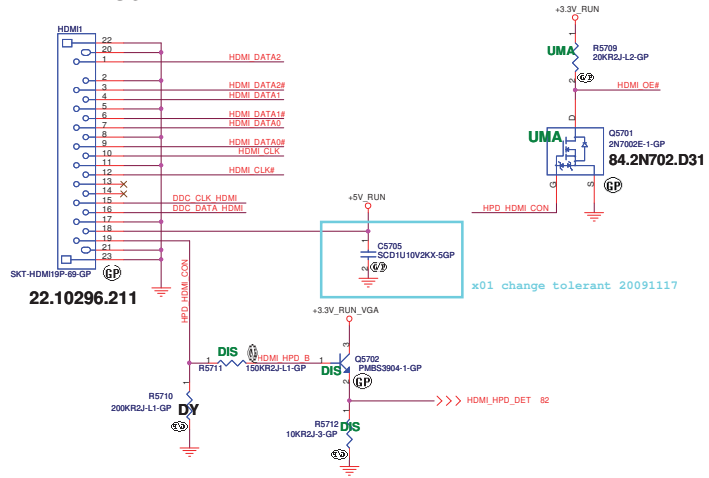
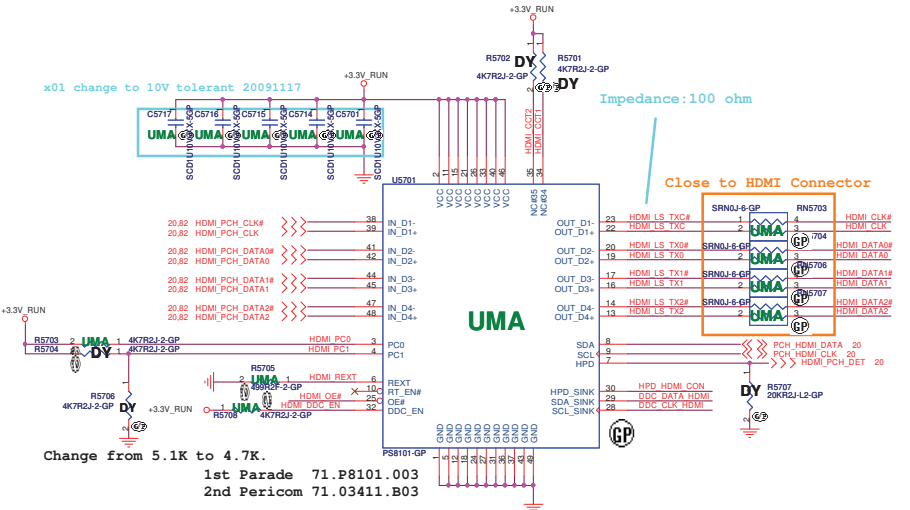
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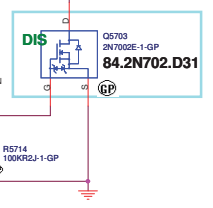
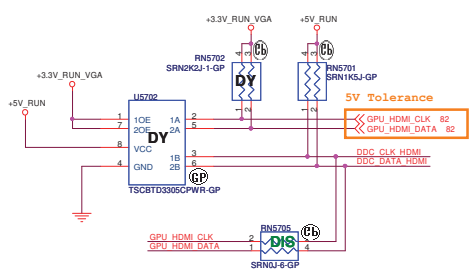
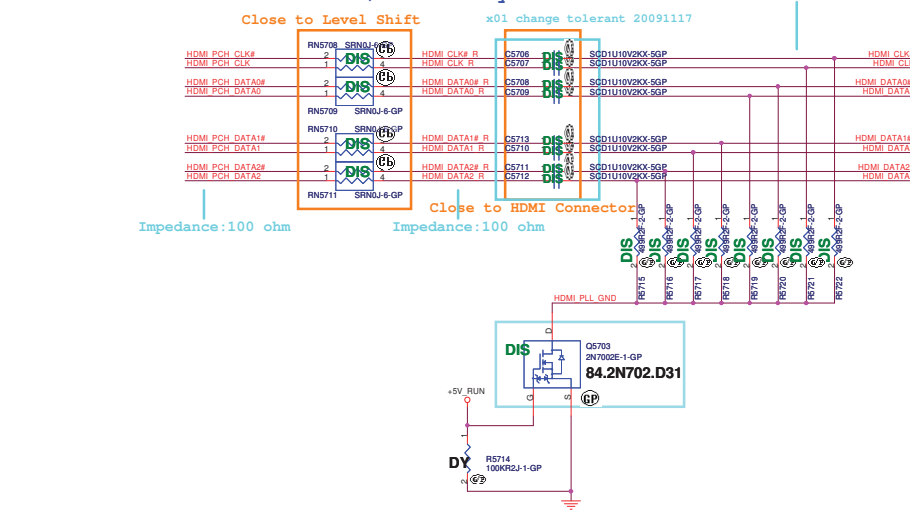
		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
LVDS Switch		
Size	Document Number	Rev
A3	Berry	A00
Date: Wednesday, February 10, 2010	Sheet 56 of 92	1

HDMI Level Shifter & CONNECTOR

HDMI CONN



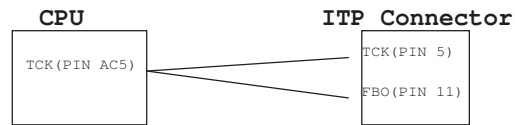
HDMI DISCRETE/ UMA Co-lay



SSID = User.Interface

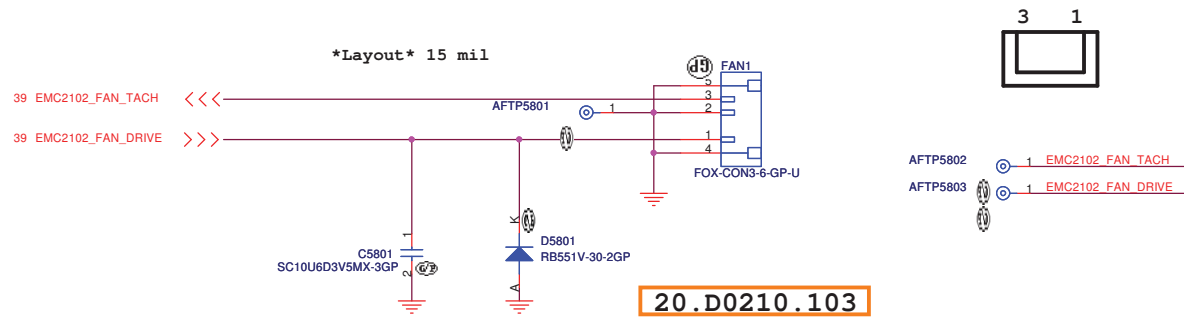
ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



SSID = Thermal

Fan Connector

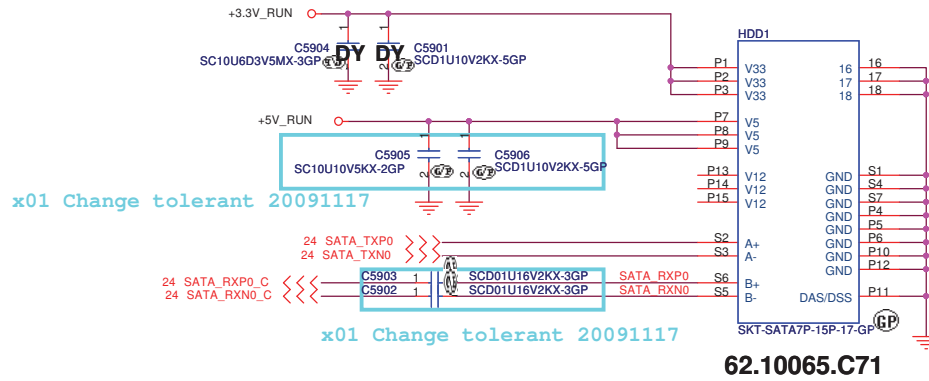


<Core Design>

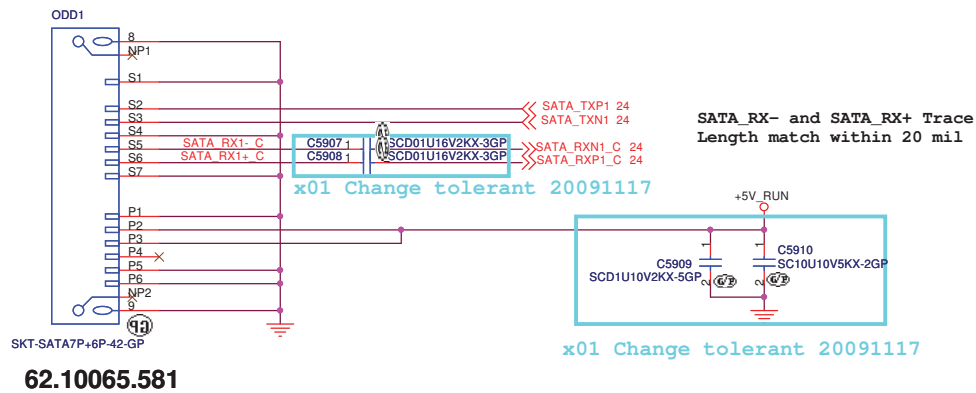
DELL Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
ITP/Fan Connector		
Size	Document Number	Rev
A3	Berry	A00
Date:	Monday, March 29, 2010	Sheet 58 of 92

SATA HDD Connector



ODD Connector



<Core Design>

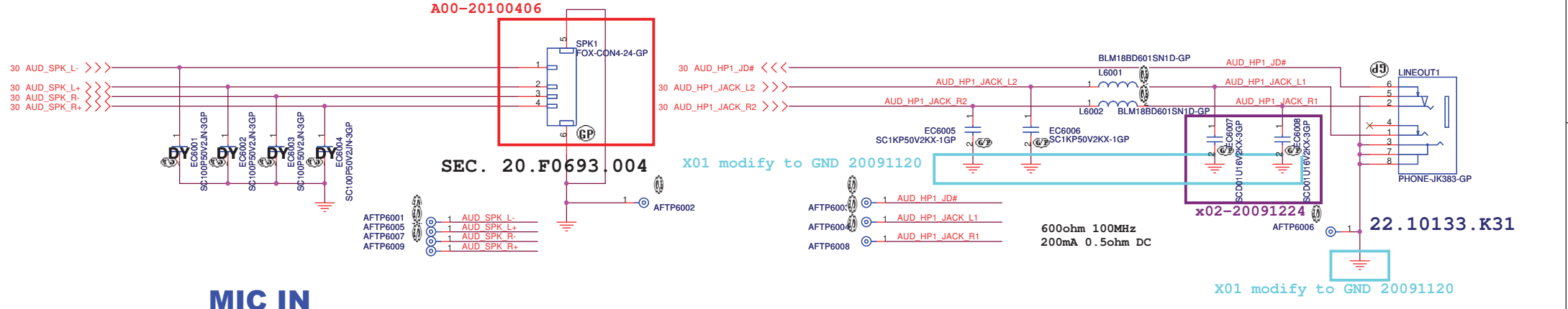


Title			HDD/ODD		
Size	Document Number	Rev			
A3	Berry				A00
Date:	Monday, March 29, 2010	Sheet	59	of	92

SSID = AUDIO

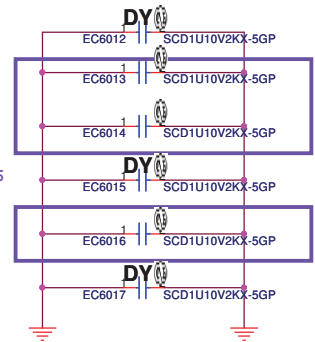
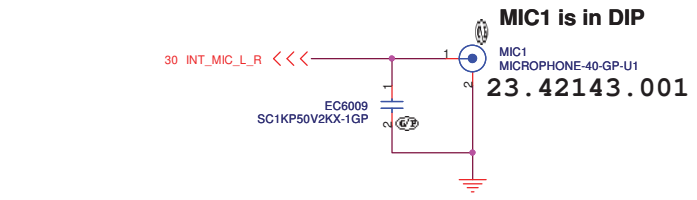
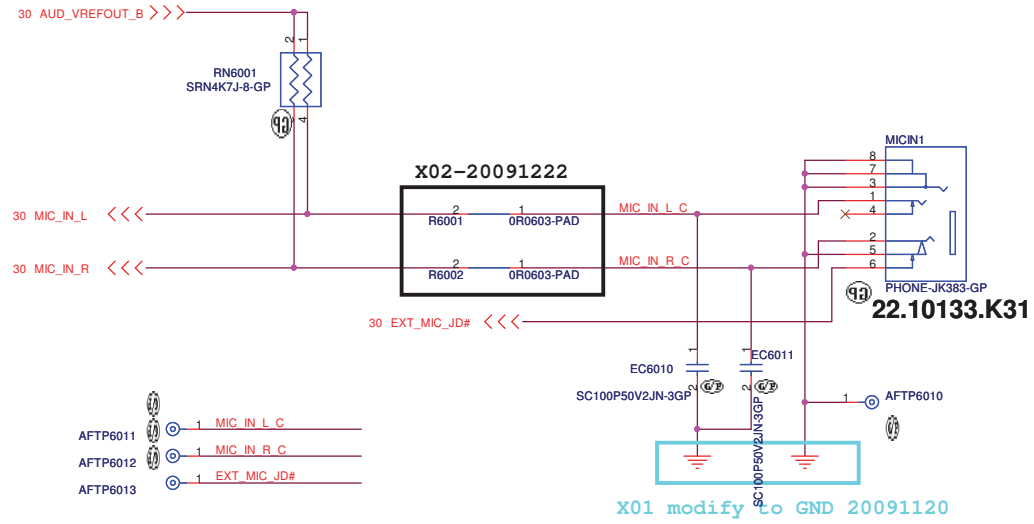
Speaker Connector

LINE1 OUT



MIC IN

Internal Microphone



<Core Design>


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Title: **Audio Jack**

Size A3	Document Number Berry	Rev A00
Date: Monday, April 26, 2010	Sheet 60 of 92	

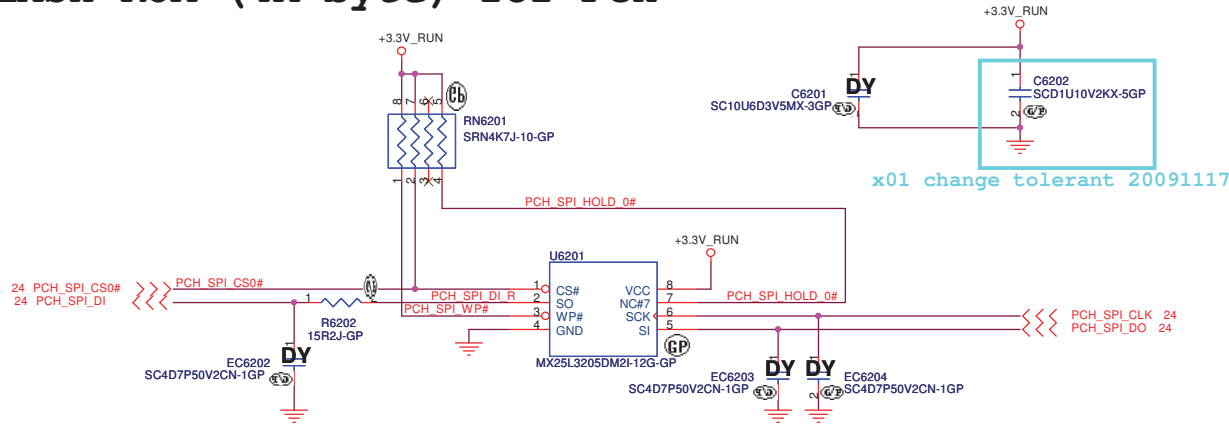
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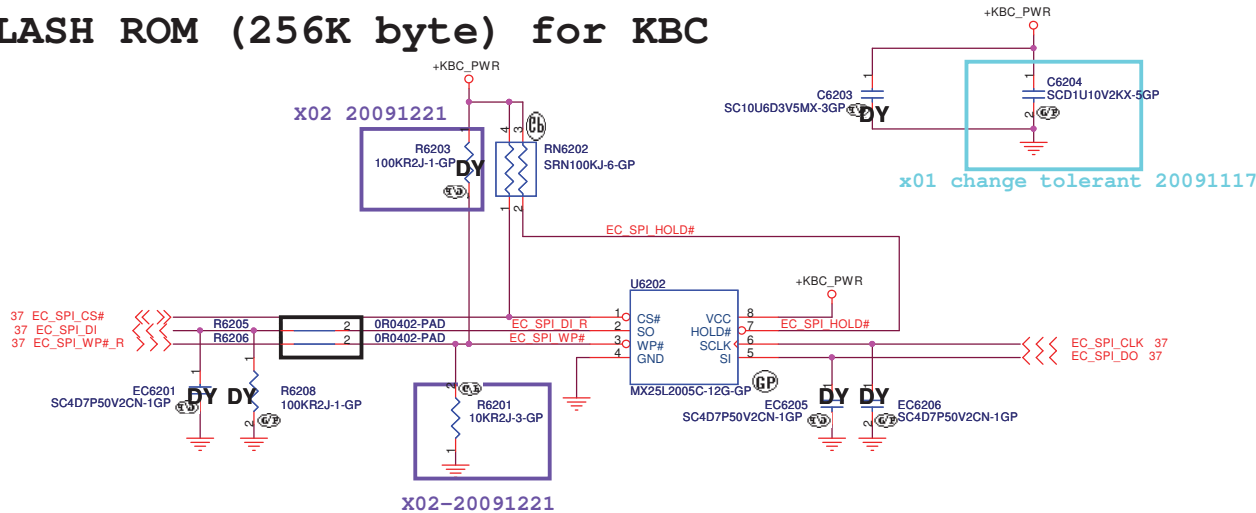
		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size	Document Number	Rev	
A3	Berry	A00	
Date: Wednesday, February 10, 2010		Sheet 61	of 92

SSID = Flash.ROM

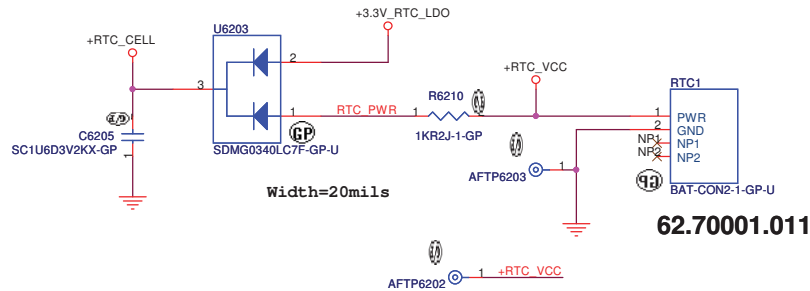
SPI FLASH ROM (4M byte) for PCH



SPI FLASH ROM (256K byte) for KBC



SSID = RBATT



<Core Design>

DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Flash/RTC**

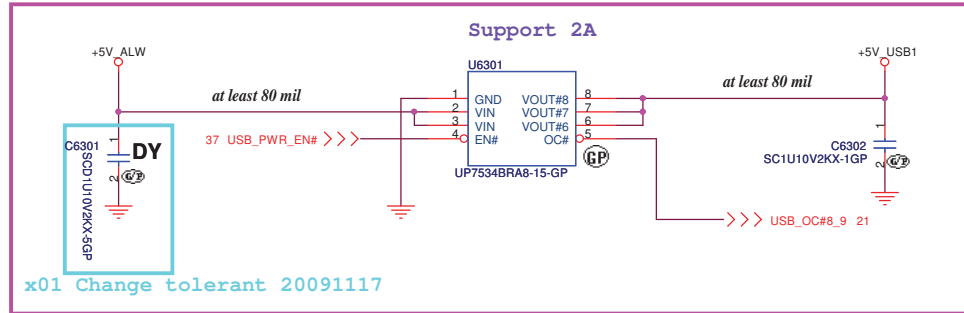
Size: A3	Document Number: Berry	Rev: A00
Date: Monday, March 29, 2010	Sheet: 62 of 92	

SSID = USB

IO Board USB Power

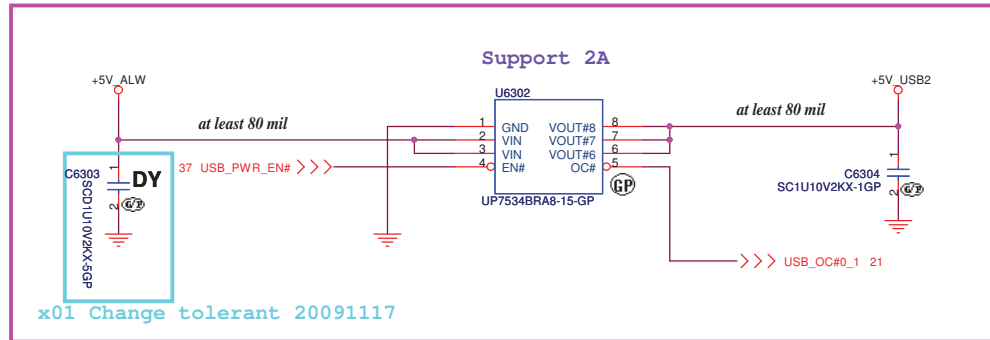
Close to I/O connector

USB POWER SW
Main UP7534BRA8-15 P/N:74.07534.079
SEC AP2101MPG-13 P/N: 74.02101.079



CRT Board USB Power

Close to CRT Board connector



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<Core Design>



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Title

Reserved

Size
A4

Document Number
Berry


Rev
A00

Date: Wednesday, February 10, 2010

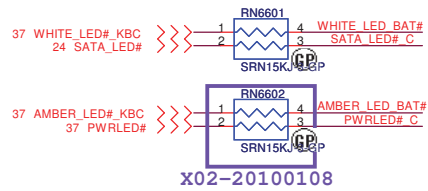
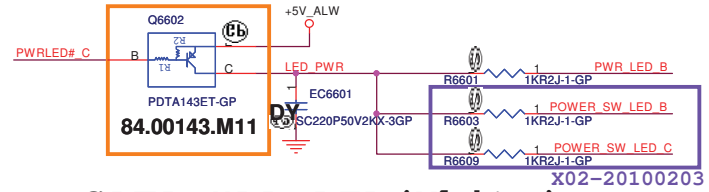
Sheet 64 of 92

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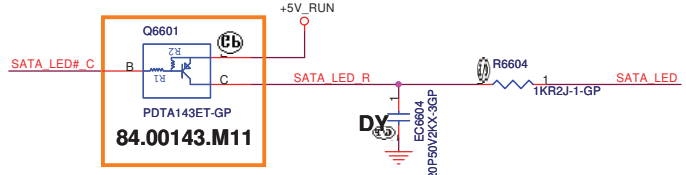
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		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size A3	Document Number Berry	Rev A00	
Date: Wednesday, February 10, 2010		Sheet 65 of	92

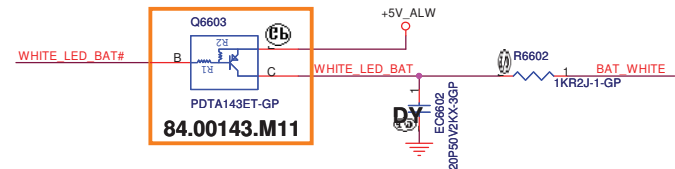
Power LED (White)



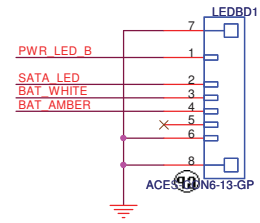
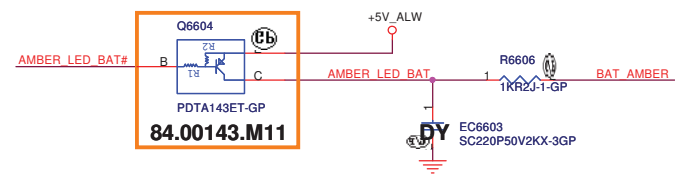
SATA HDD LED (White)



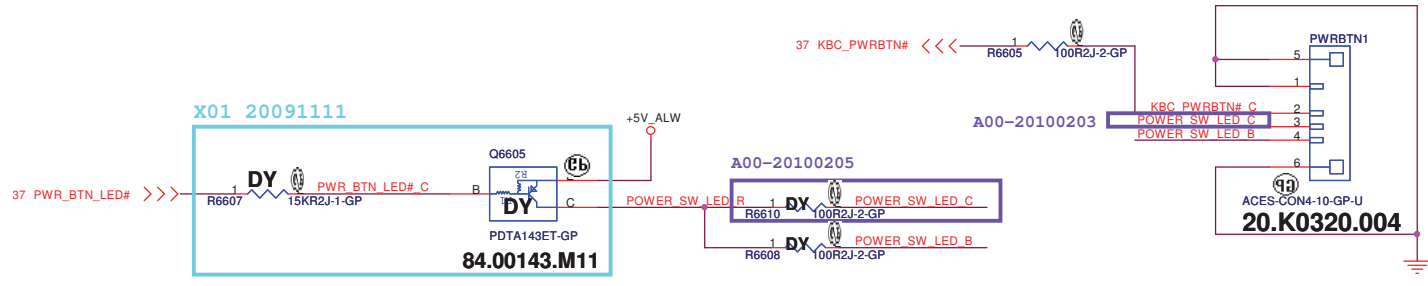
Battery LED1 (White)



Battery LED2 (Amber)



Power button LED (White)



<Core Design>


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Title: **LED Bard/Power Button**

Size: A3	Document Number: Berry	Rev: A00
Date: Monday, March 29, 2010	Sheet: 66	of: 92

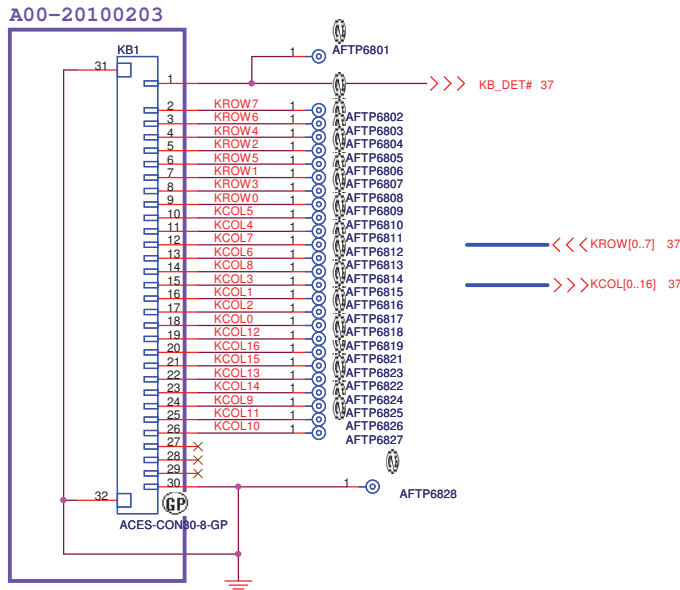
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<Core Design>

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Title			
Reserved			
Size A3	Document Number Berry	Rev A00	
Date: Wednesday, February 10, 2010		Sheet 67 of	92

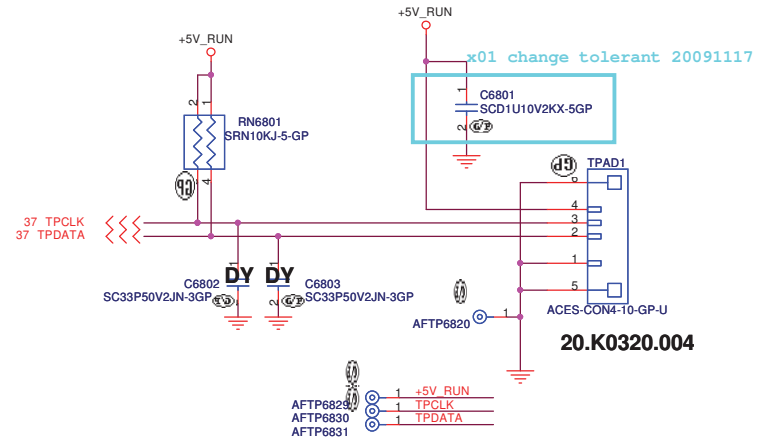
SSID = KBC

Internal Keyboard Connector

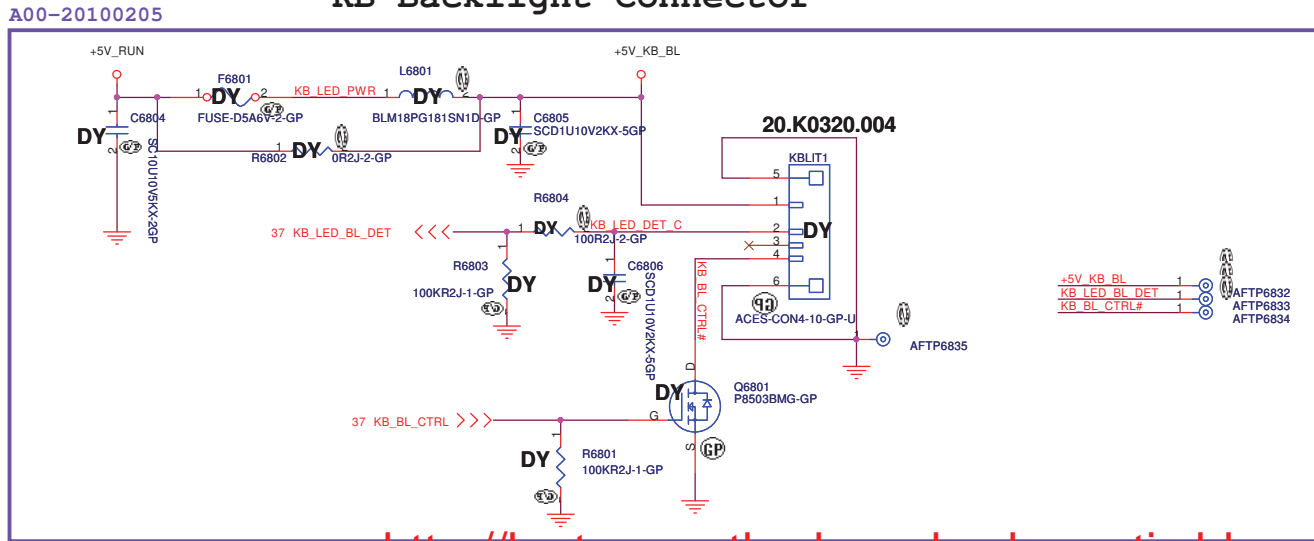


SSID = Touch.Pad

TouchPad Connector



KB Backlight Connector



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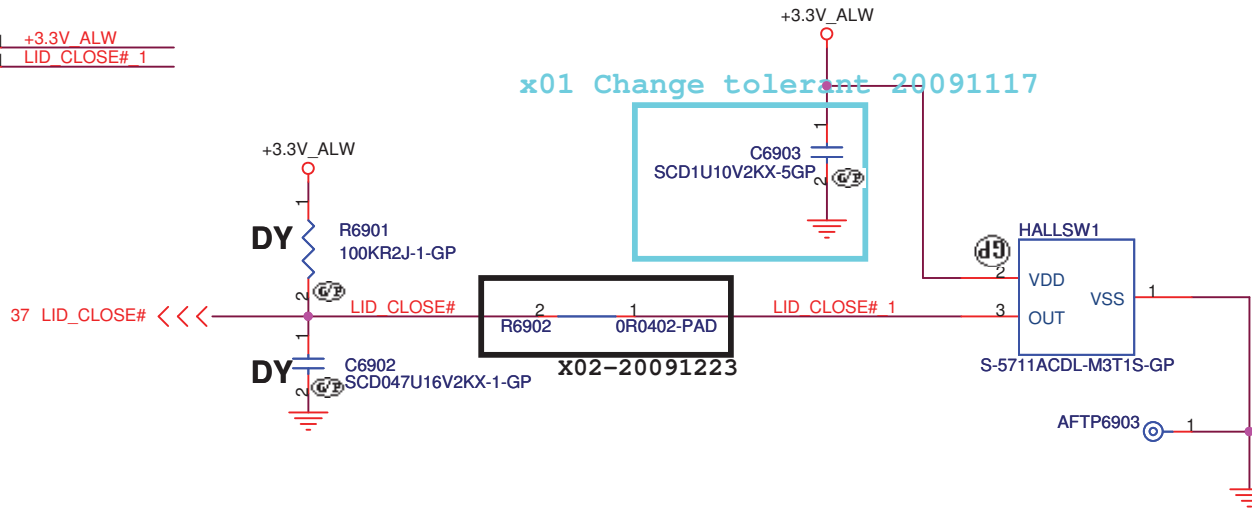
<Core Design>

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Title: **Key Board/Touch Pad**

Size: A3	Document Number: Berry	Rev: A00
Date: Monday, March 29, 2010	Sheet: 68	of: 92

AFTP6901 1 +3.3V_ALW
AFTP6902 1 LID_CLOSE# 1



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Title

Hall Sensor

Size
A4

Document Number

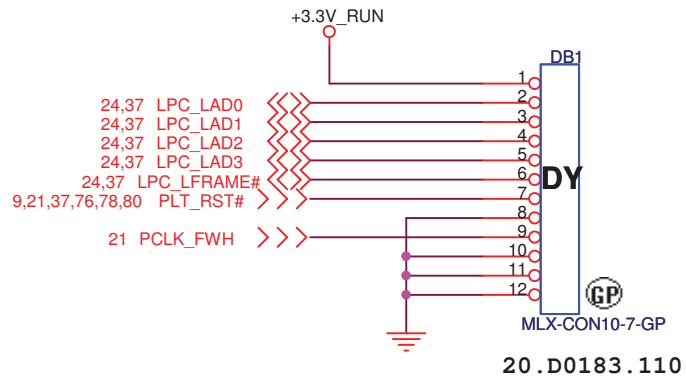
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Rev

A00

Date: Monday, March 29, 2010

Sheet 69 of 92



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Title

Dubug connector

Size
A4

Document Number

Berry

Rev
A00

Date: Monday, March 29, 2010

Sheet 70 of 92

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Title

RESERVED

Size
A4

Document Number
Berry

Rev
A00

Date: Wednesday, February 10, 2010

Sheet 71 of 92

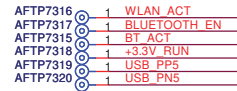
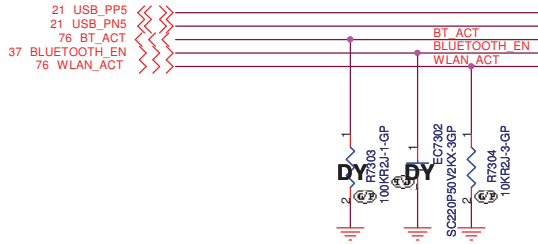
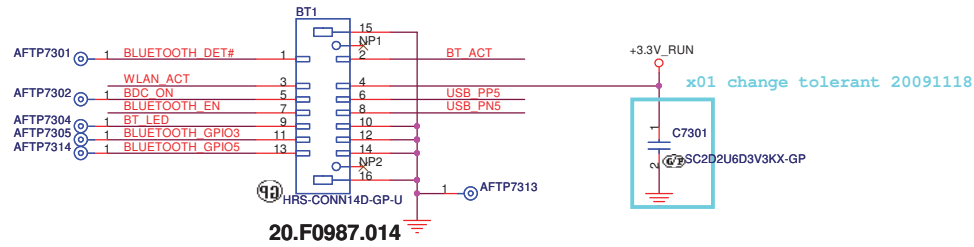
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		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		RESERVED
Size A3	Document Number Berry	Rev A00
Date: Wednesday, February 10, 2010		Sheet 72 of 92

SSID = User.Interface

Bluetooth Module conn.



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Title: **Bluetooth**

Size: A3	Document Number: Berry	Rev: A00
Date: Monday, March 29, 2010	Sheet: 73	of: 92

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Title			
Reserved			
Size A3	Document Number Berry	Rev A00	
Date: Wednesday, February 10, 2010		Sheet 74	of 92

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Title

Reserved

Size
A4

Document Number

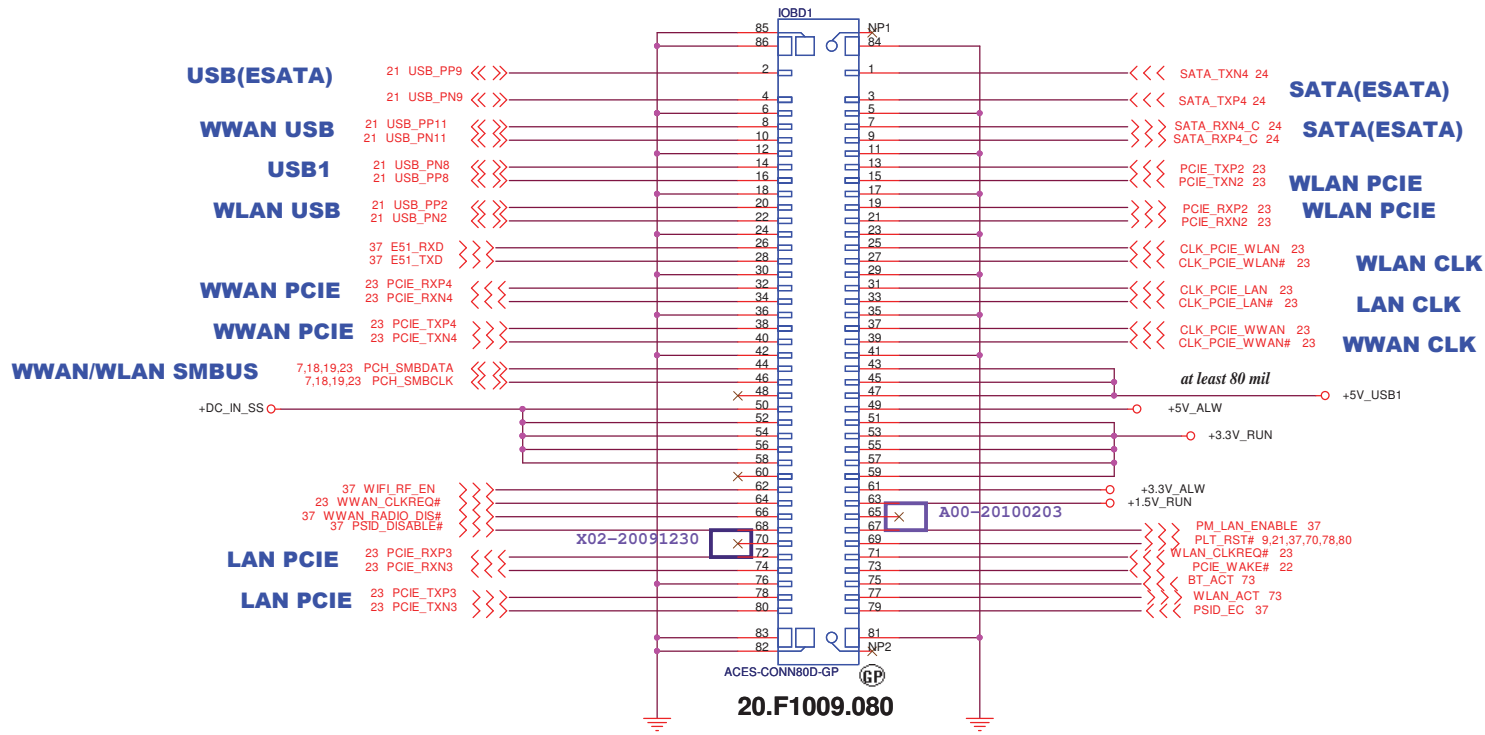
Berry

Rev
A00

Date: Wednesday, February 10, 2010

Sheet 75 of 92

IO Board CONN 80 pin



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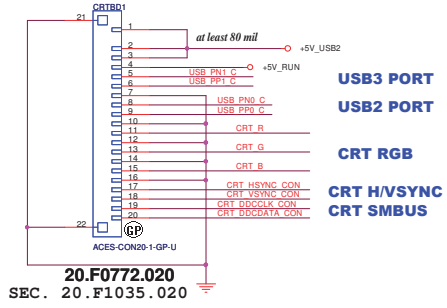
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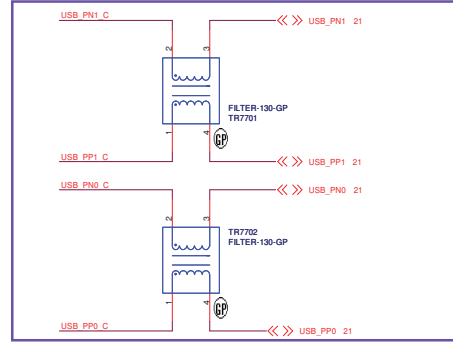
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Size: A3	Document Number: Berry	Rev: A00
Date: Monday, March 29, 2010	Sheet 76 of 92	

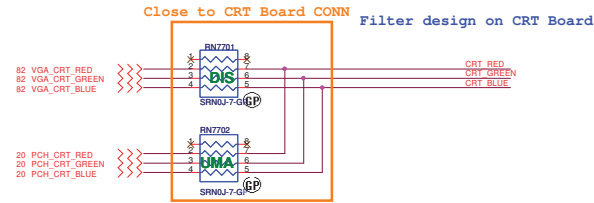
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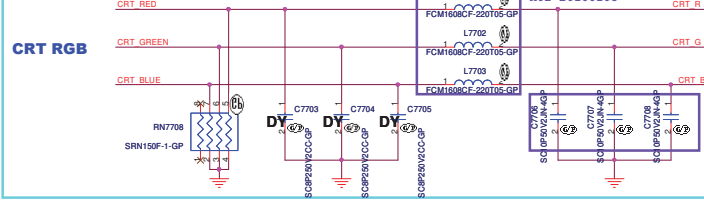
A00-20100120



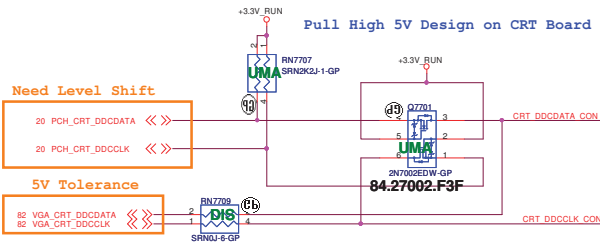
CRT RGB



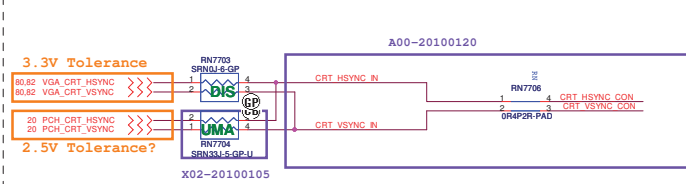
X01 20091111



CRT DDCDATA & DDCLK level shift

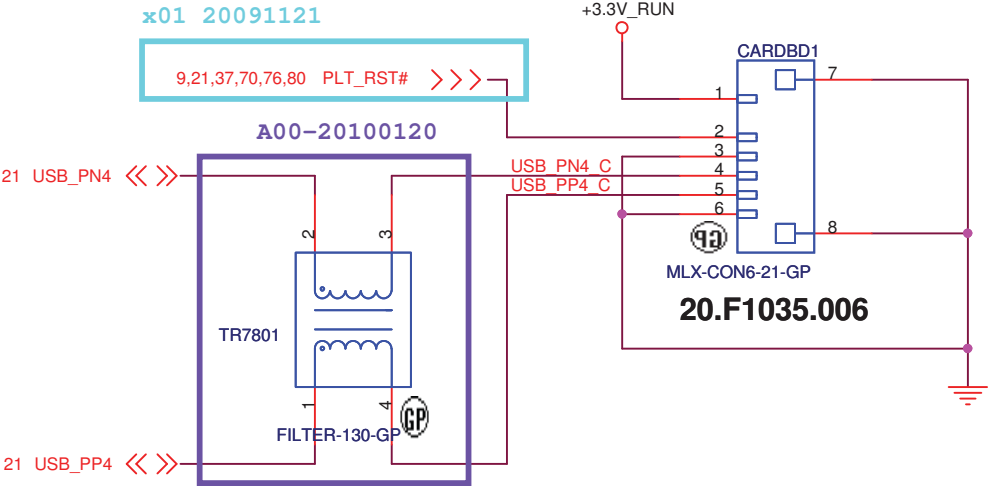


CRT Hsync & Vsync level shift



SSID = SDIO

Card Reader connector



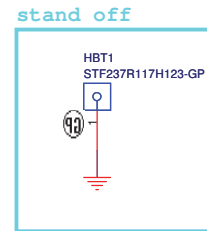
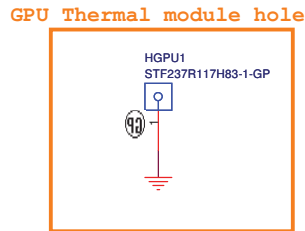
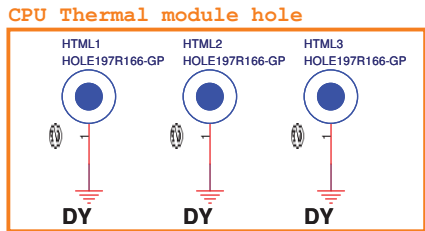
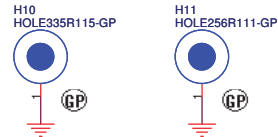
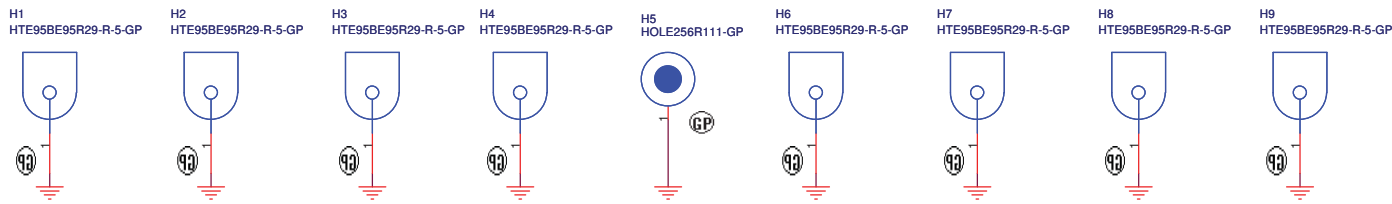
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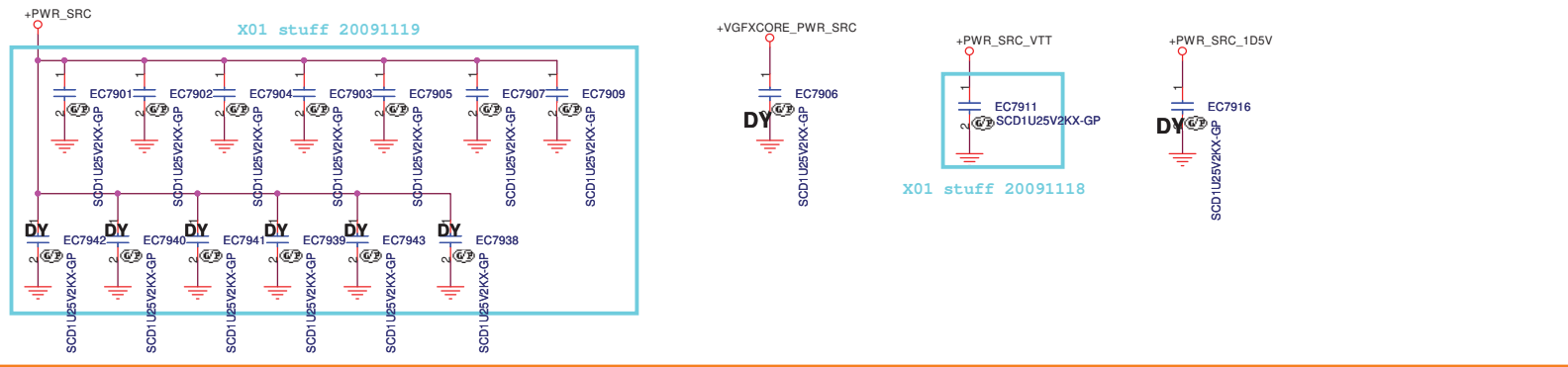
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CARD Reader CONN

Size A4 Document Number Rev
Berry **A00**

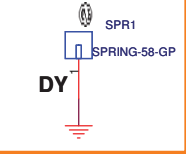
Date: Monday, March 29, 2010 Sheet 78 of 92



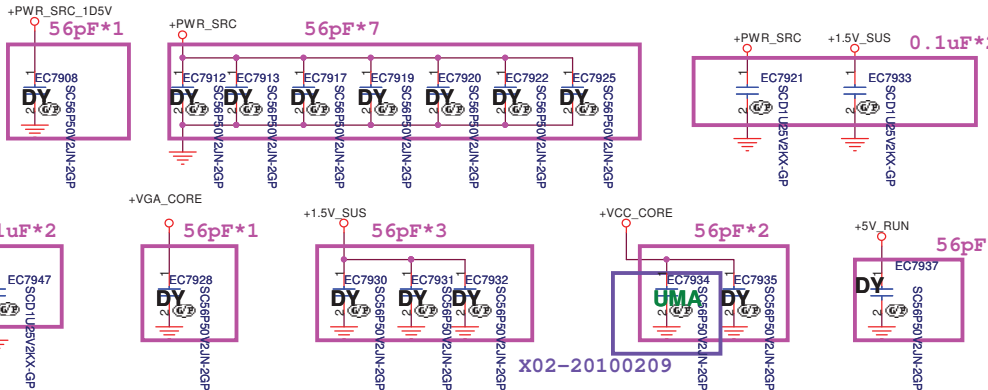
EMI Reserve



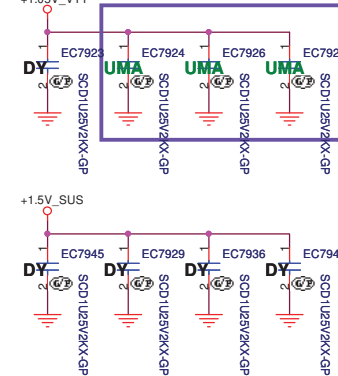
EMI Reserve



X01 RF Reserved-20091118



X02-20100208



X02-20100209



<Core Design>

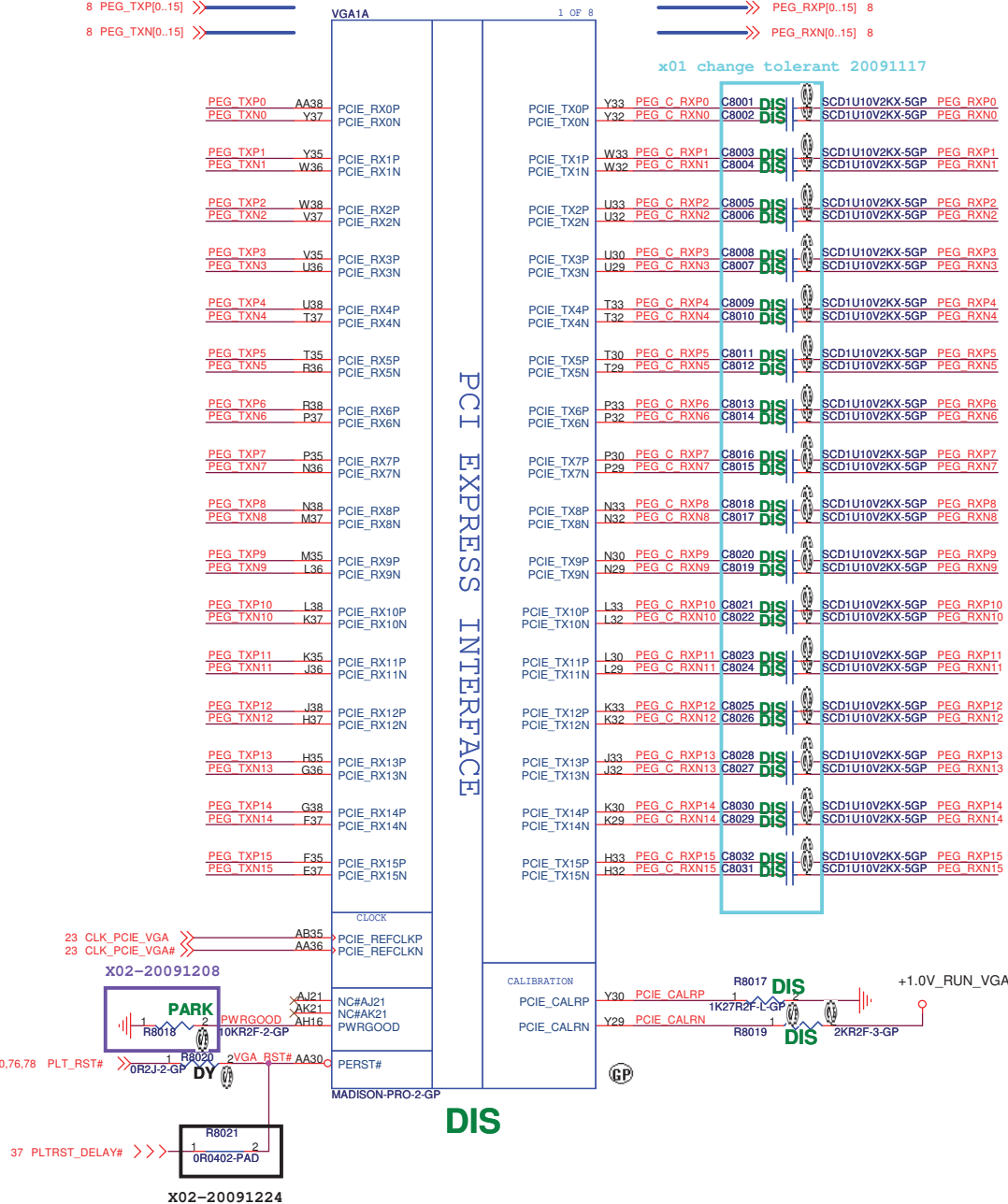


Title UNUSED PARTS/EMI Capacitors		
Size A3	Document Number Berry	Rev A00
Date: Wednesday, February 10, 2010	Sheet 79	of 92

8 PEG_TXP0[0..15] >>>
8 PEG_TXN0[0..15] >>>

PEG_RXP0[0..15] 8 >>>
PEG_RXN0[0..15] 8 >>>

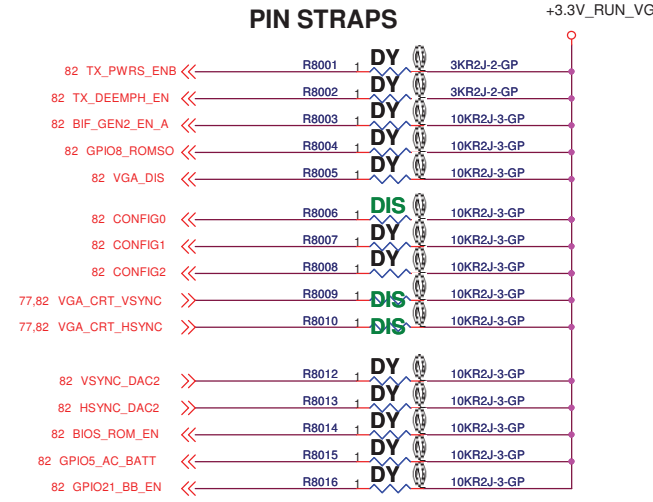
x01 change tolerant 20091117



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMEND	PLATFORM SETTING
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X	1
TX_DEEMPH_EN	GPIO1	PCIe TRANSMITTER DE-EMPHASIS ENABLED 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	X	1
BIF_GEN2_EN_A	GPIO2	0:Advertises the PCIe device as 2.5GT/s capable at power on. 1:Advertises the PCIe device as 5.0GT/s capable at power on.	0	0
GPIO5_AC_BATT	GPIO5	optional input allow the system to request a fast power reduction by setting GPIO5 to low.	?	0
RESERVED	GPIO8	RESERVED	0	0
VGA_DIS	GPIO9	0:VGA Controller capacity enabled 1:The device won't be recognized as the system's VGA controller	0	0
ROMIDCFG[2:0]	GPIO[13:11]	BIOS_ROM_EN=1, Config[2:0] defines the ROM type BIOS_ROM_EN=0, Config[2:0] defines the primary memory aperture size	X X X	0 0 1 (2.56MB)
RESERVED	GPIO21	RESERVED	0	0
BIOS_ROM_EN	GPIO_22_ROMCSB	0:Disable external BIOS ROM device 1:Enable external BIOS ROM device	X	0
VIP_DEVICE_STRAP_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver that it sense whether or not a VIP device is connected on the VIP Host interface.	X	0
RSVD	H2SYNC	RESERVED	0	0
RSVD	GENERICC	RESERVED	0	0
AUD[1]	HSYNC	AUD[1:0]:11-Audio for both DisplayPort and HDMI	X	1
AUD[0]	VSYNC		X	1



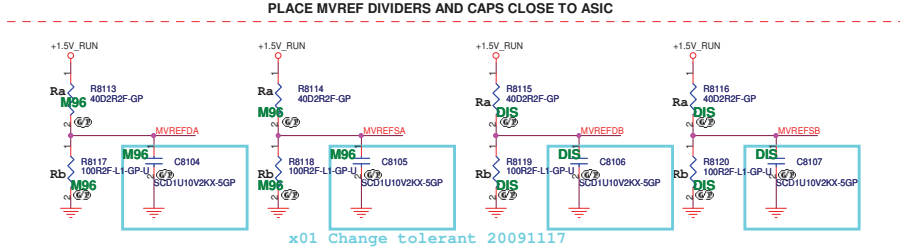
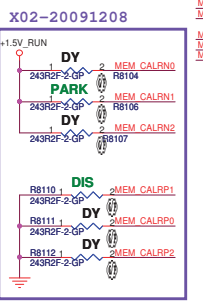
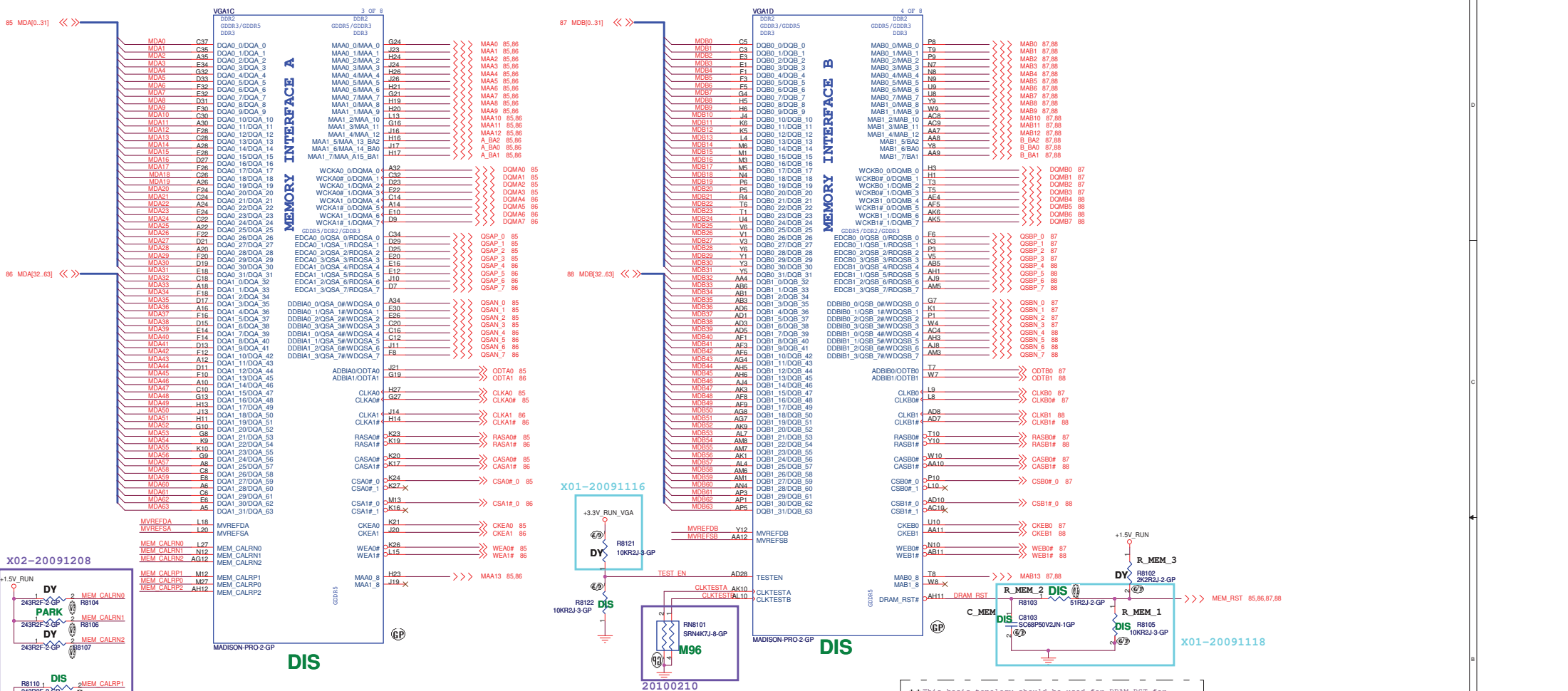
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Title: **GPU PCIE/STRAPPING(1/5)**

Size: **A3** Document Number: **Berry** Rev: **A00**

Date: Monday, March 29, 2010 Sheet 80 of 92



	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

	GDDR3	DDR3
MVDDQ	1.8V/1.5V	1.5V
Ra	40.2R	100R
Rb	100R	100R

***This basic topology should be used for DRAM_RST for DDR3/GDDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and | Cap values will depend on the DRAM load and will have to be calculated for different Memory, DRAM Load and board to pass Reset Signal Spec.

Designator	For Manhattan	For M96-M2/M92-M2
R_MEM_1	10K	2.2nF
R_MEM_2	51R	0R/Short
R_MEM_3	DNI	DNI
C_MEM	68pF	10K

<Core Design>

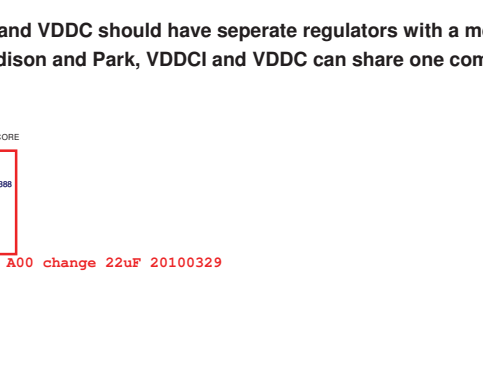
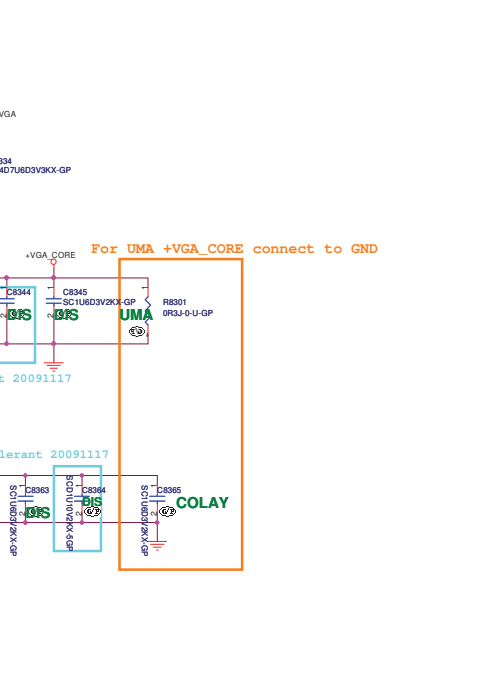
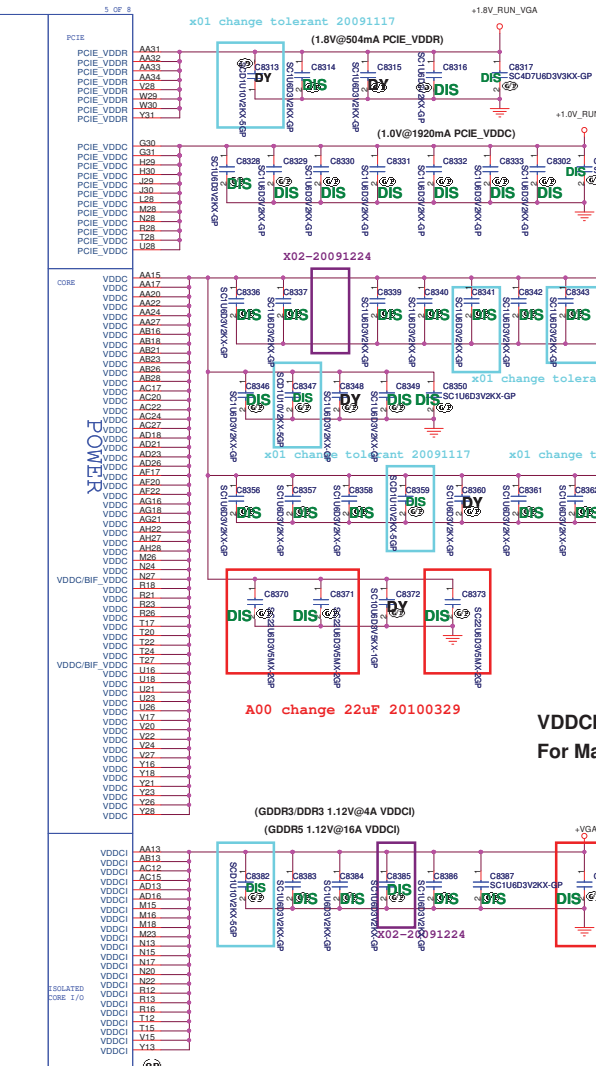
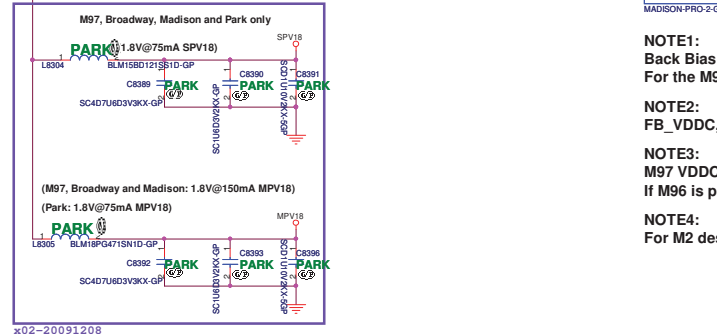
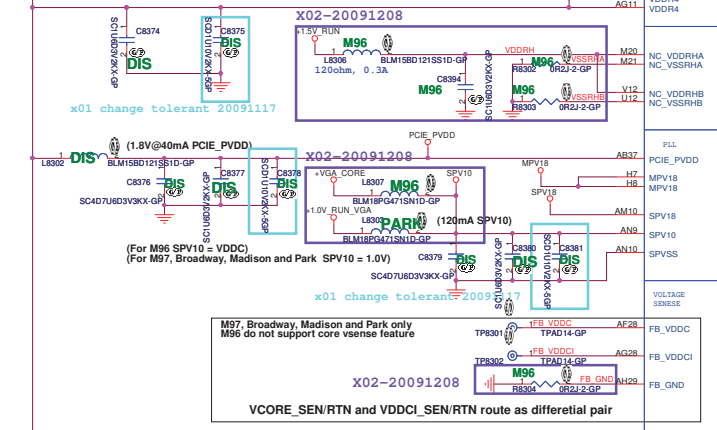
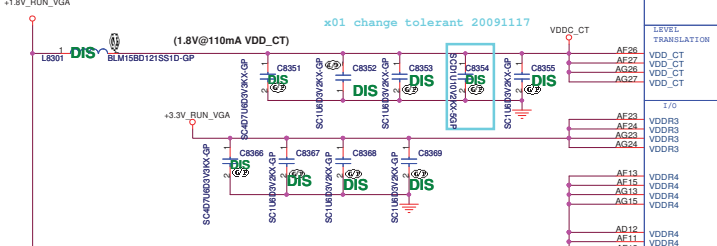
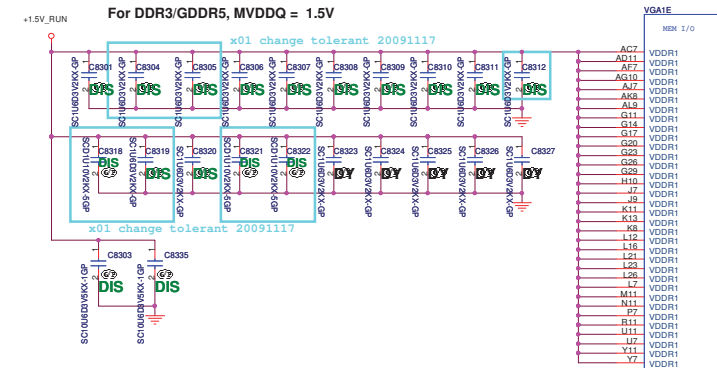
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GPU Memory(2/5)

Size C Document Number **Berry** Rev **A00**

Date: Monday, March 29, 2010 Sheet 81 of 92

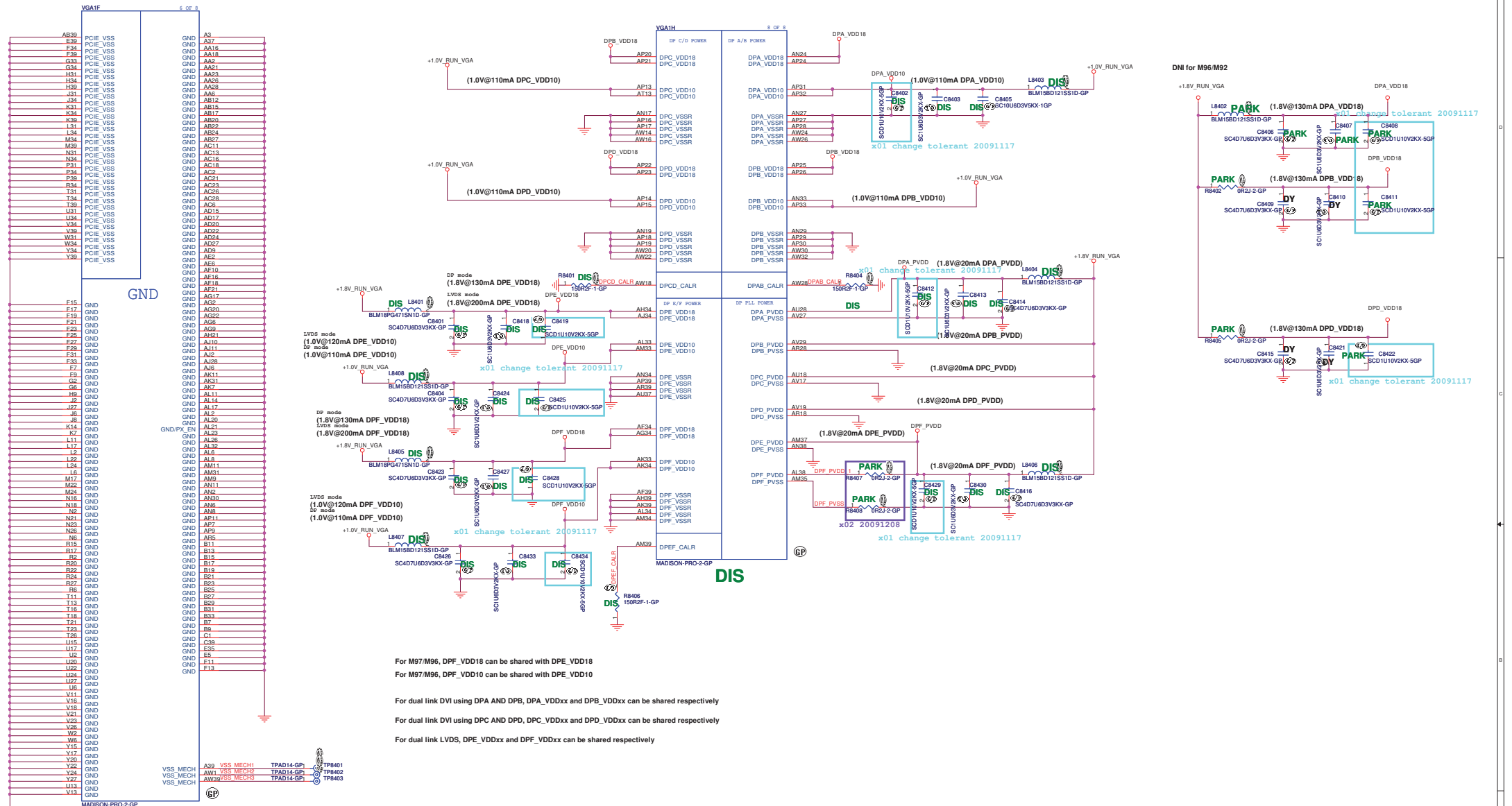


NOTE1:
Back Bias is not supported on M97, Broadway, Madison and Park
For the M96 Back Bias circuitry, refer to REF134

NOTE2:
FB_VDDC, FB_VDDCI and FB_GND are not supported on M96

NOTE3:
M97 VDDC and VDDCI ball assignments are different from M96.
If M96 is populated on this design, VDDC and VDDCI will be shorted on the substrate.

NOTE4:
For M2 design compatibility, refer to the document AN_M96_Ax and AN_M97_Ax

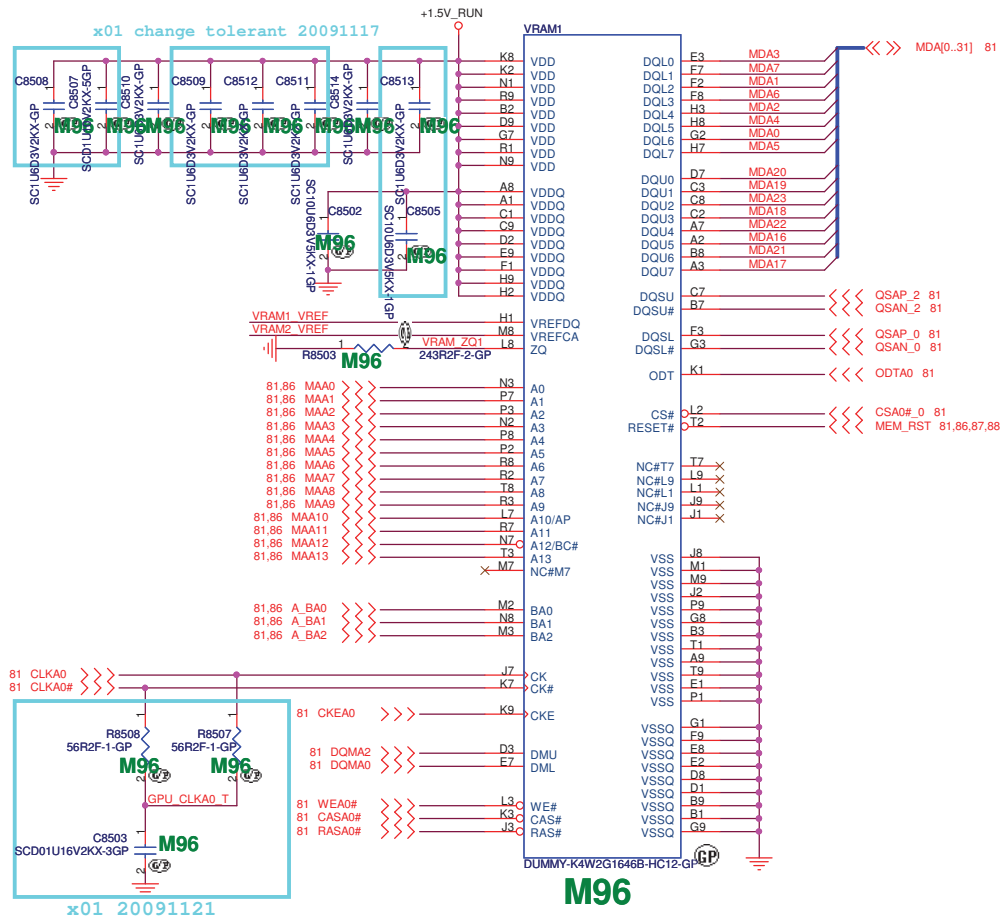


For M97/M96, DPF_VDD18 can be shared with DPE_VDD18
 For M97/M96, DPF_VDD10 can be shared with DPE_VDD10

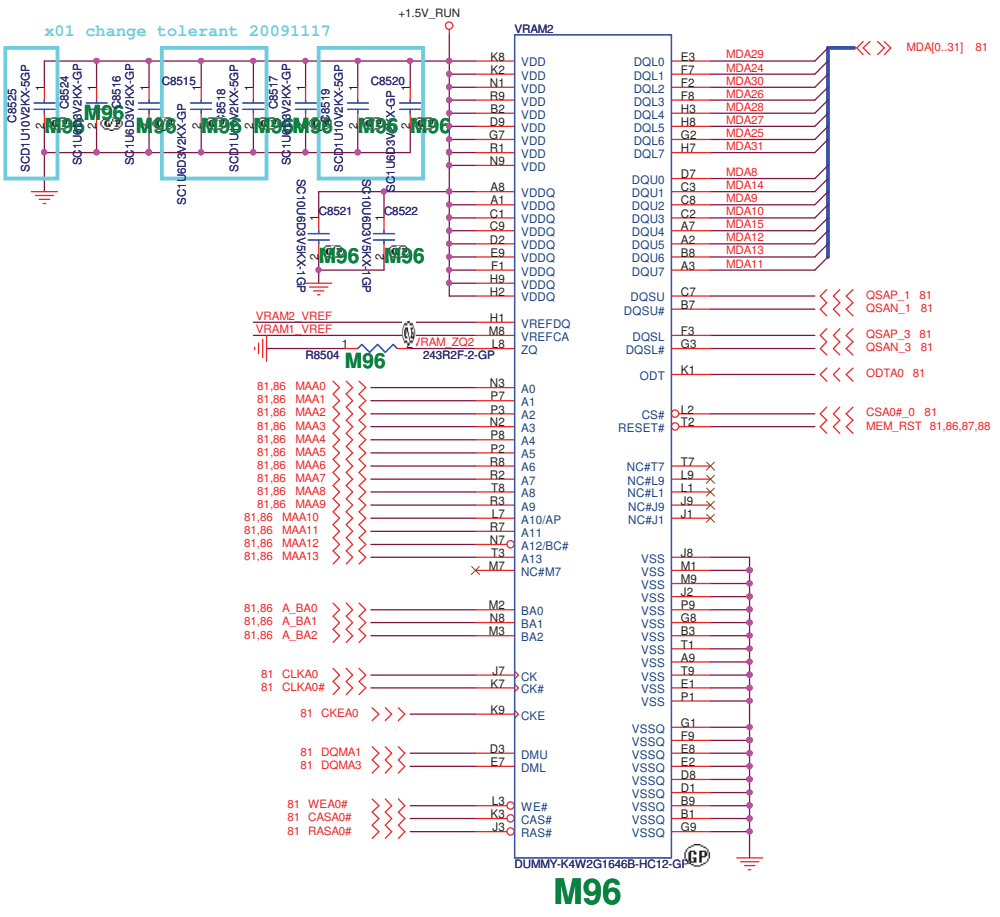
For dual link DVI using DPA AND DPB, DPA_VDDxx and DPB_VDDxx can be shared respectively
 For dual link DVI using DPC AND DPD, DPC_VDDxx and DPD_VDDxx can be shared respectively

For dual link LVDS, DPE_VDDxx and DPF_VDDxx can be shared respectively

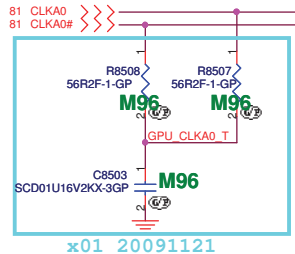
A39 VSS_MECH1 TPAD14-GP TP8401
 AW1 VSS_MECH2 TPAD14-GP TP8402
 AW3 VSS_MECH3 TPAD14-GP TP8403



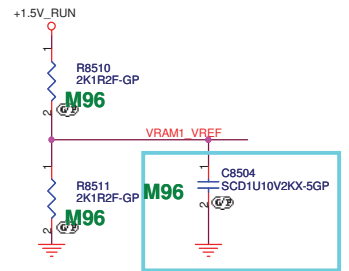
M96



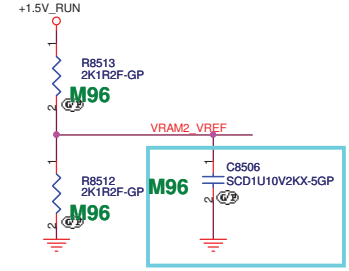
M96



x01 20091121



x01 change tolerant 20091117



x01 change tolerant 20091117

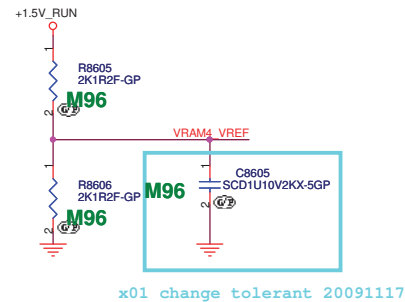
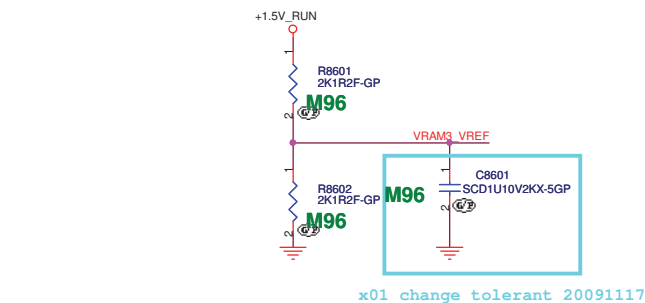
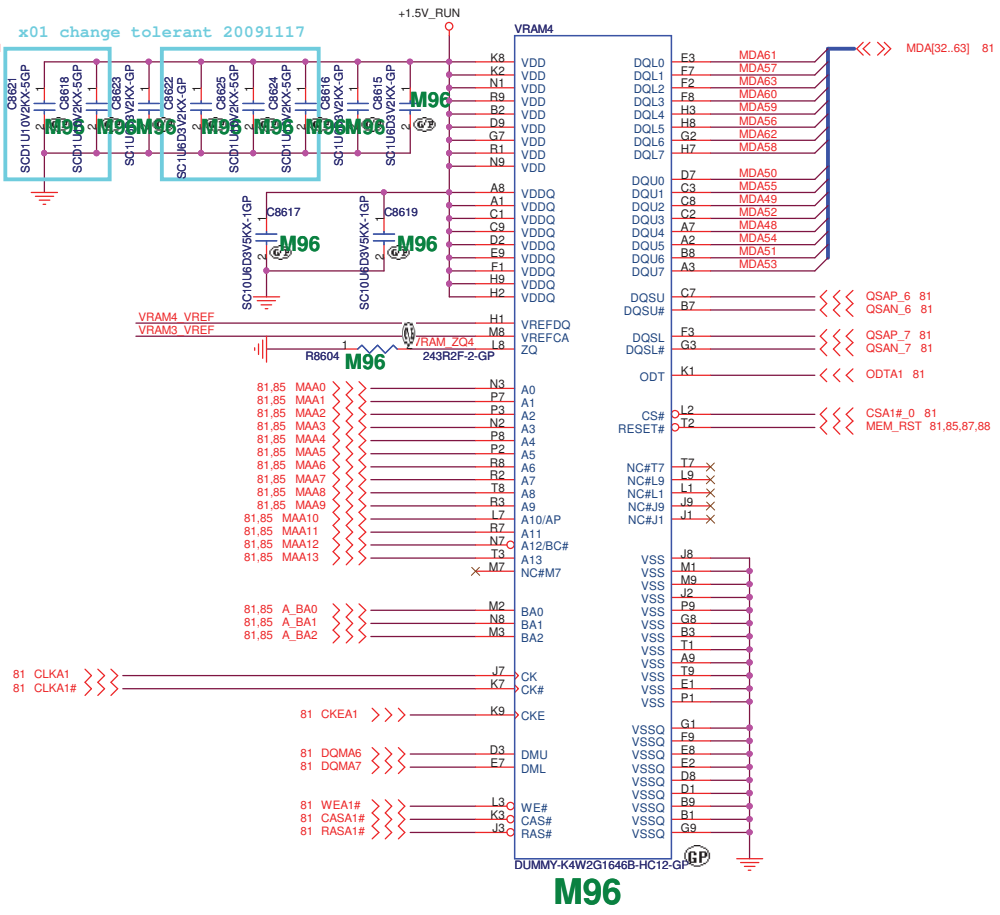
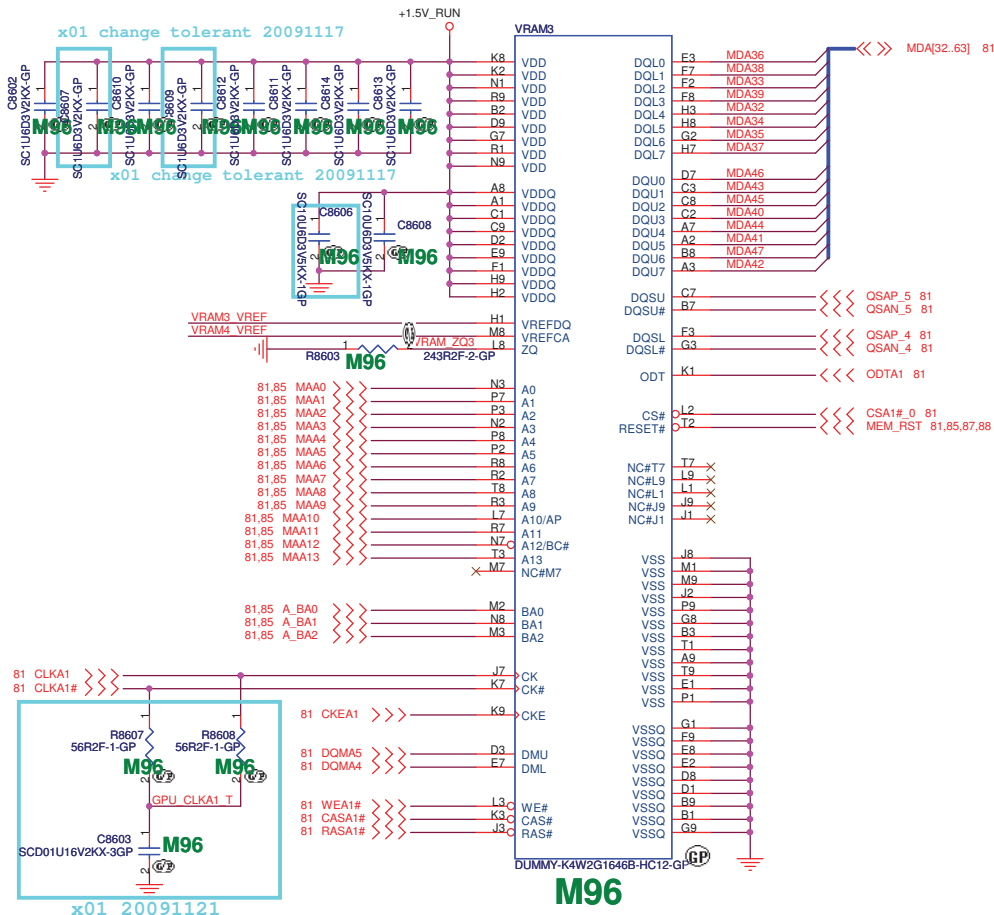
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Title: **GPU-VRAM1,2 (1/4)**

Size	Document Number	Rev
Custom	Berry	A00
Date:	Monday, March 29, 2010	Sheet 85 of 92



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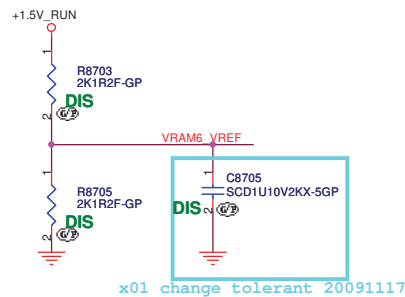
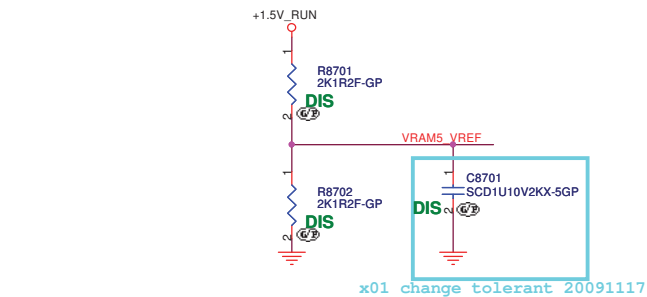
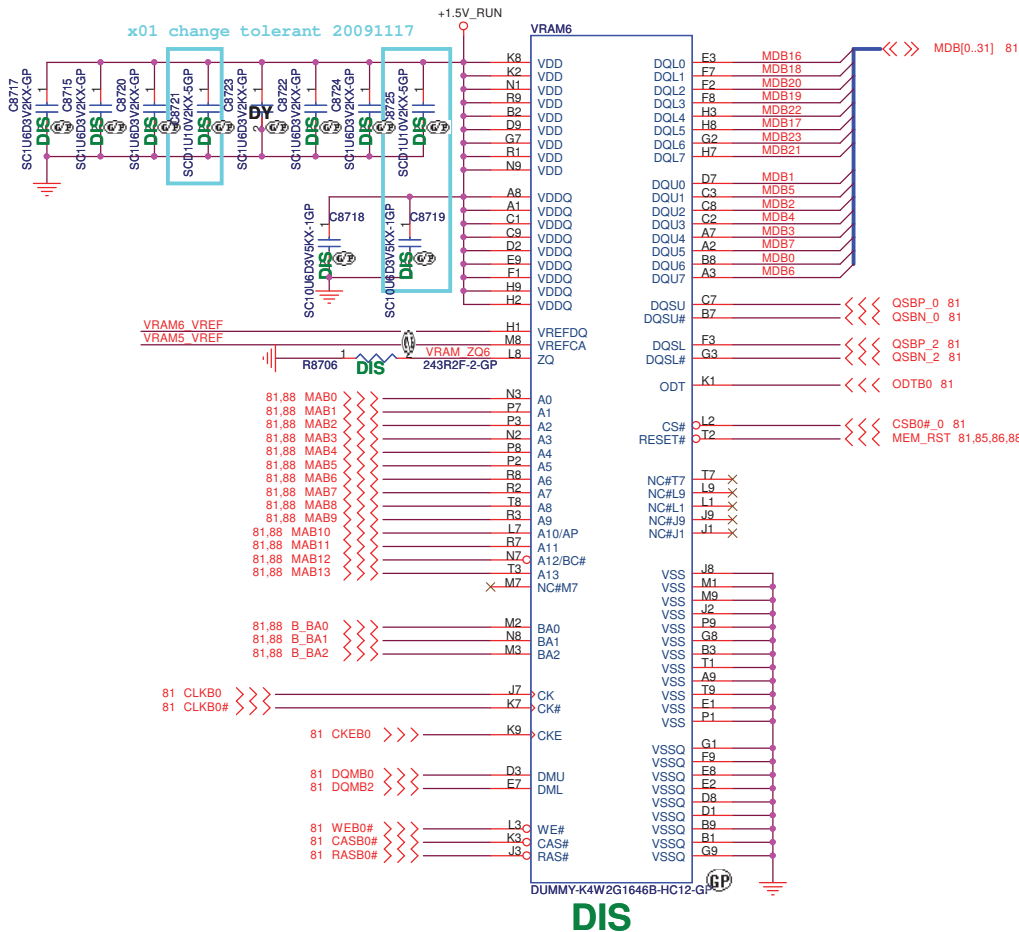
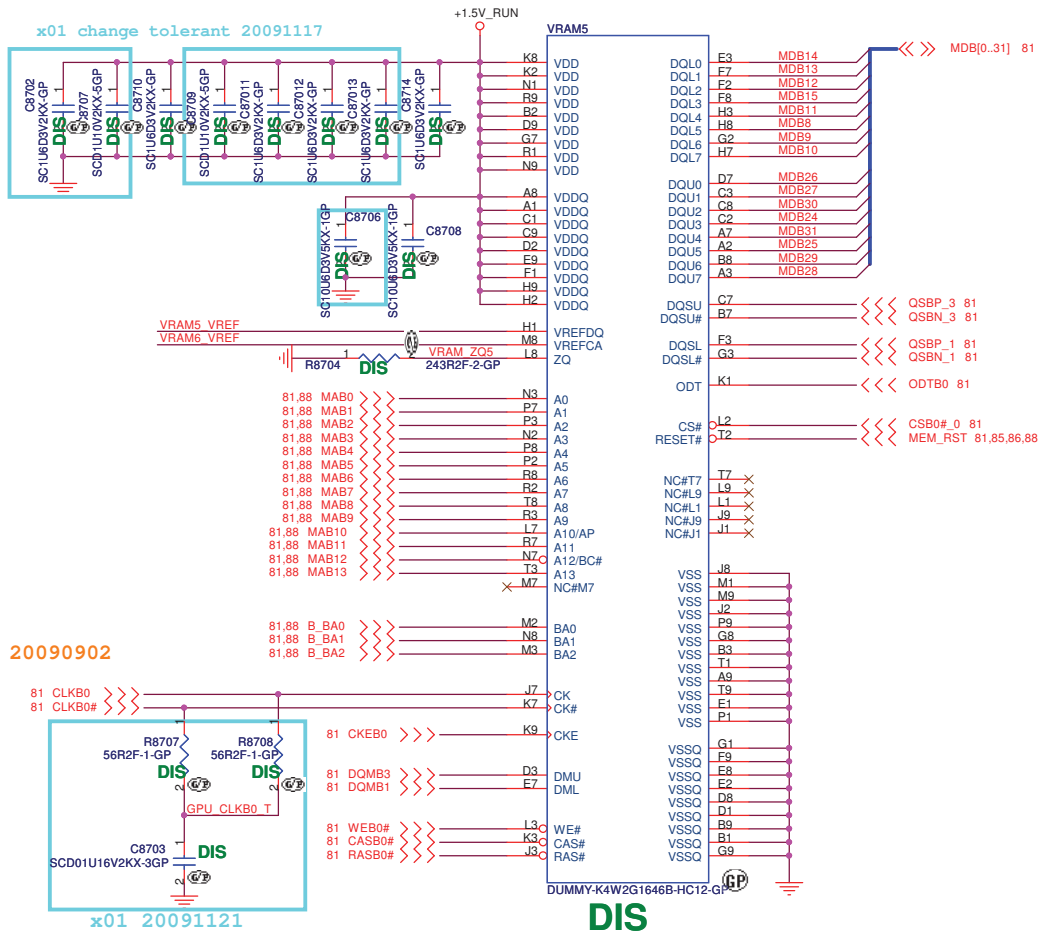
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Title: **GPU-VRAM3,4 (2/4)**

Size	Document Number	Rev
Custom	Berry	A00

Date: Monday, March 29, 2010 Sheet 86 of 92

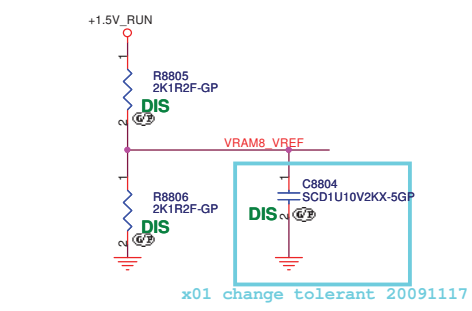
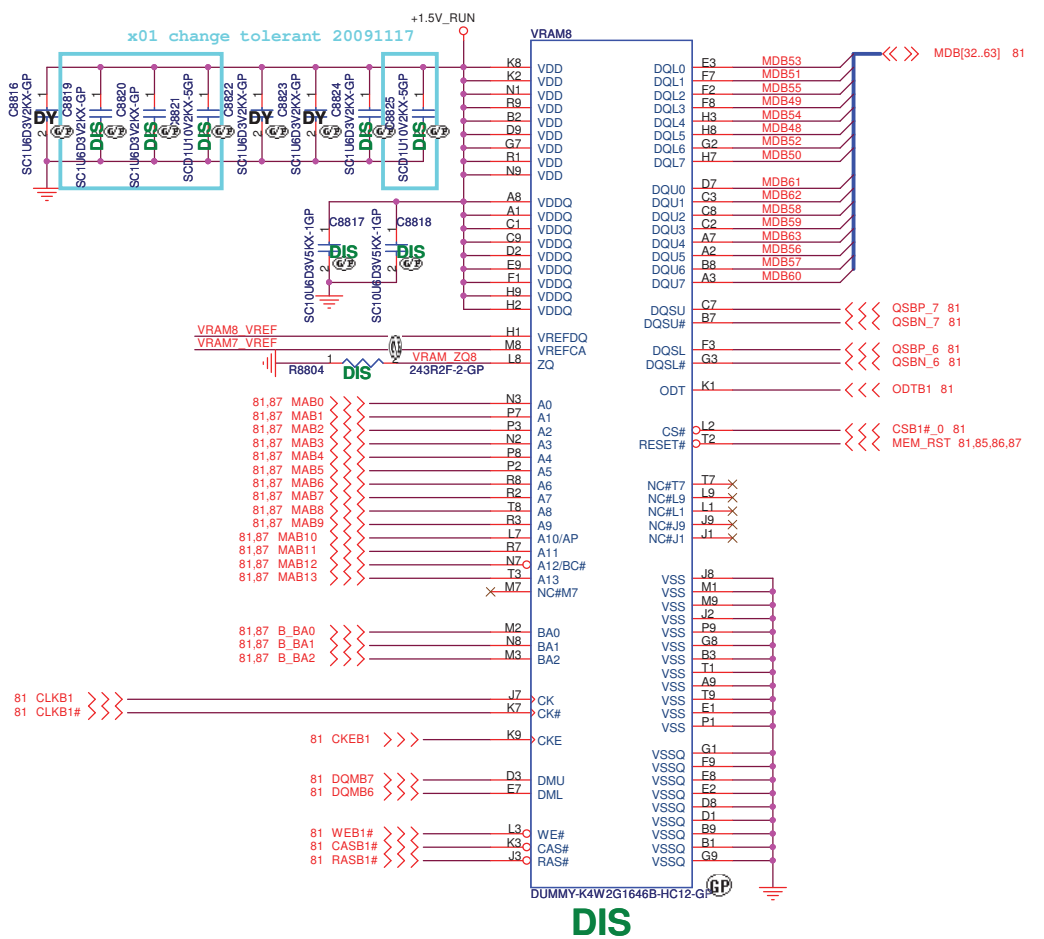
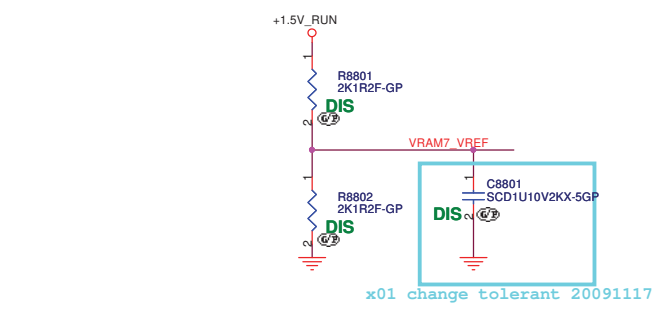
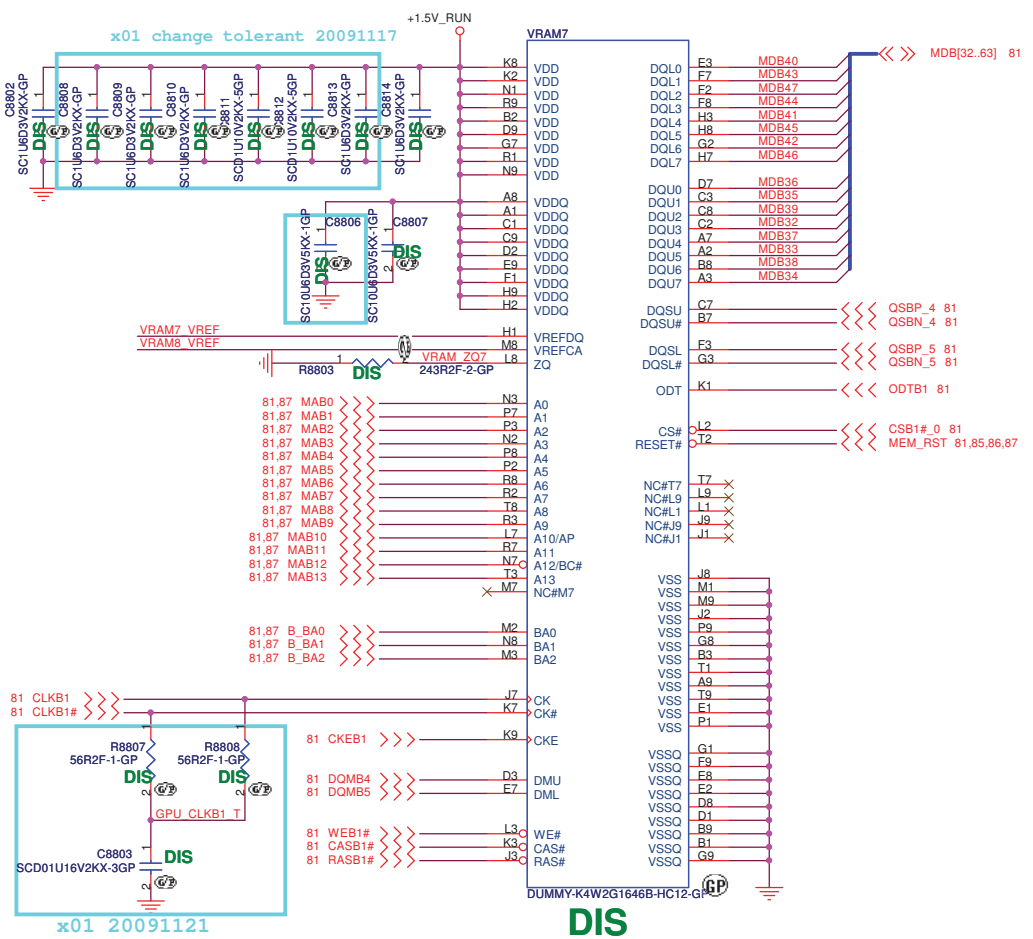


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Title: **GPU-VRAM5,6 (3/4)**

Size A3	Document Number Berry	Rev A00
Date: Monday, March 29, 2010	Sheet 87	of 92



DIS

DIS

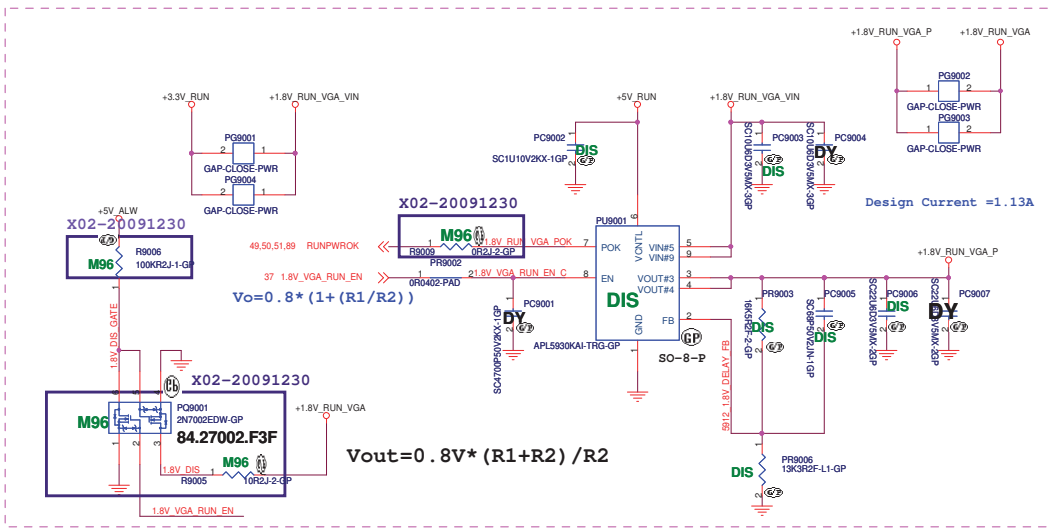
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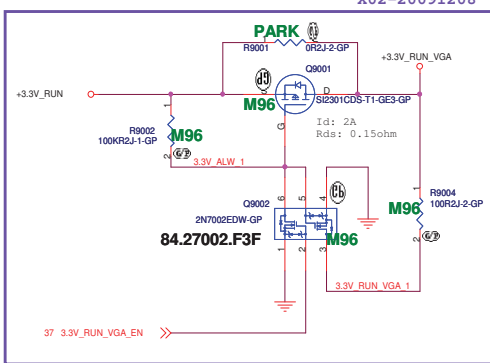
Title: **GPU-VRAM7,8 (4/4)**

Size A3	Document Number Berry	Rev A00
Date: Monday, March 29, 2010	Sheet 88	of 92

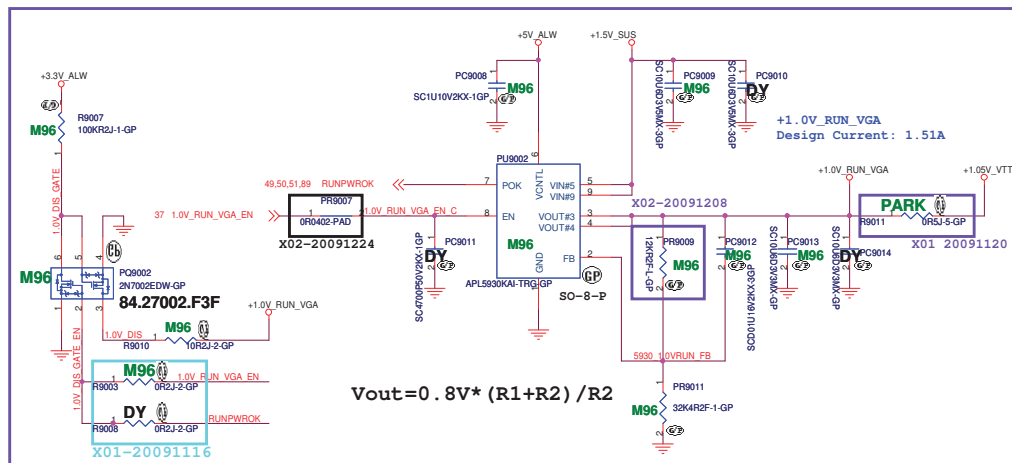
APL5930 for +1.8V_RUN_VGA



+3.3V_RUN_VGA



APL5930KAI for +1.0V_RUN_VGA



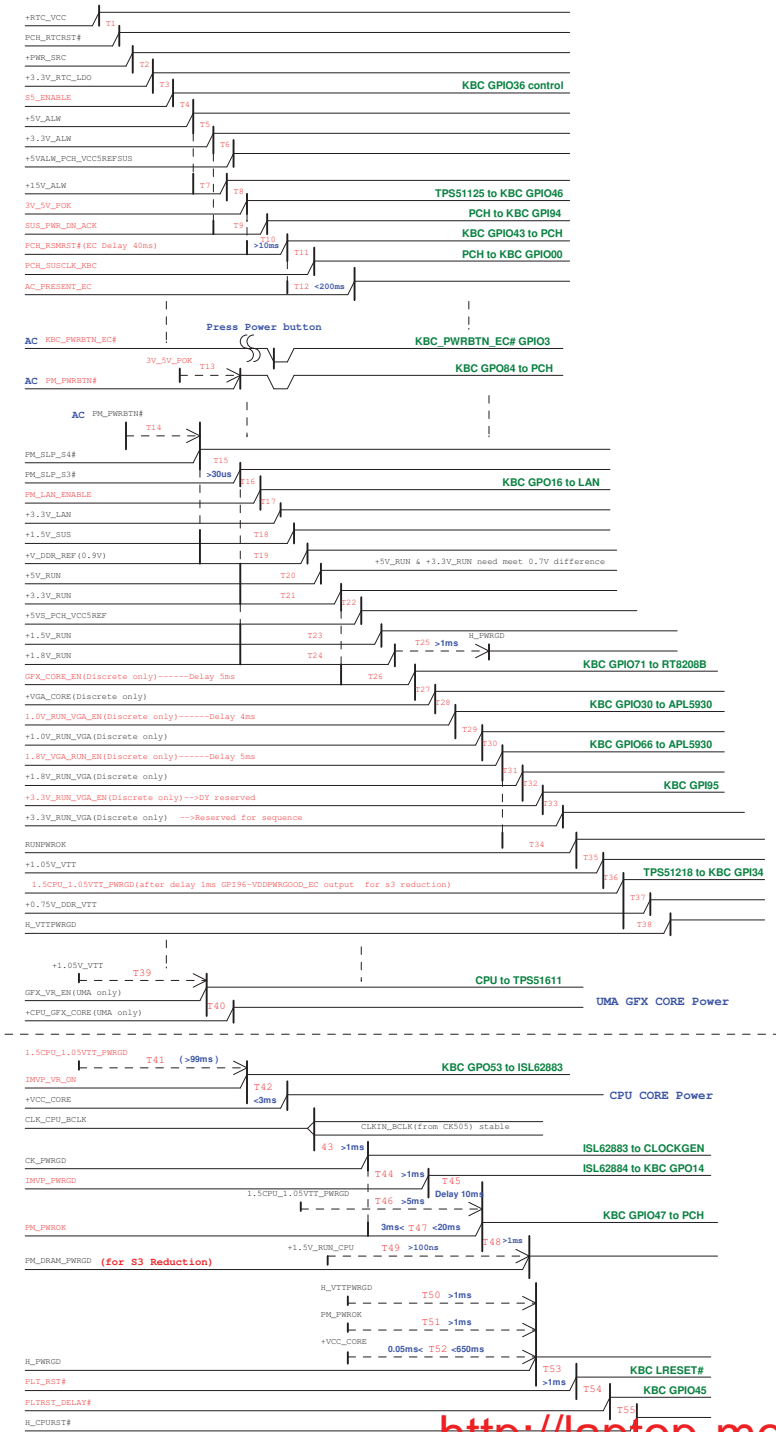
<Core Design>

Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
File	DISCRETE VGA POWER	
Size	Document Number Berry	Rev A00
Date:	Monday, March 29, 2010	Sheet 90 of 92

D15 Intel-Power Up Sequence

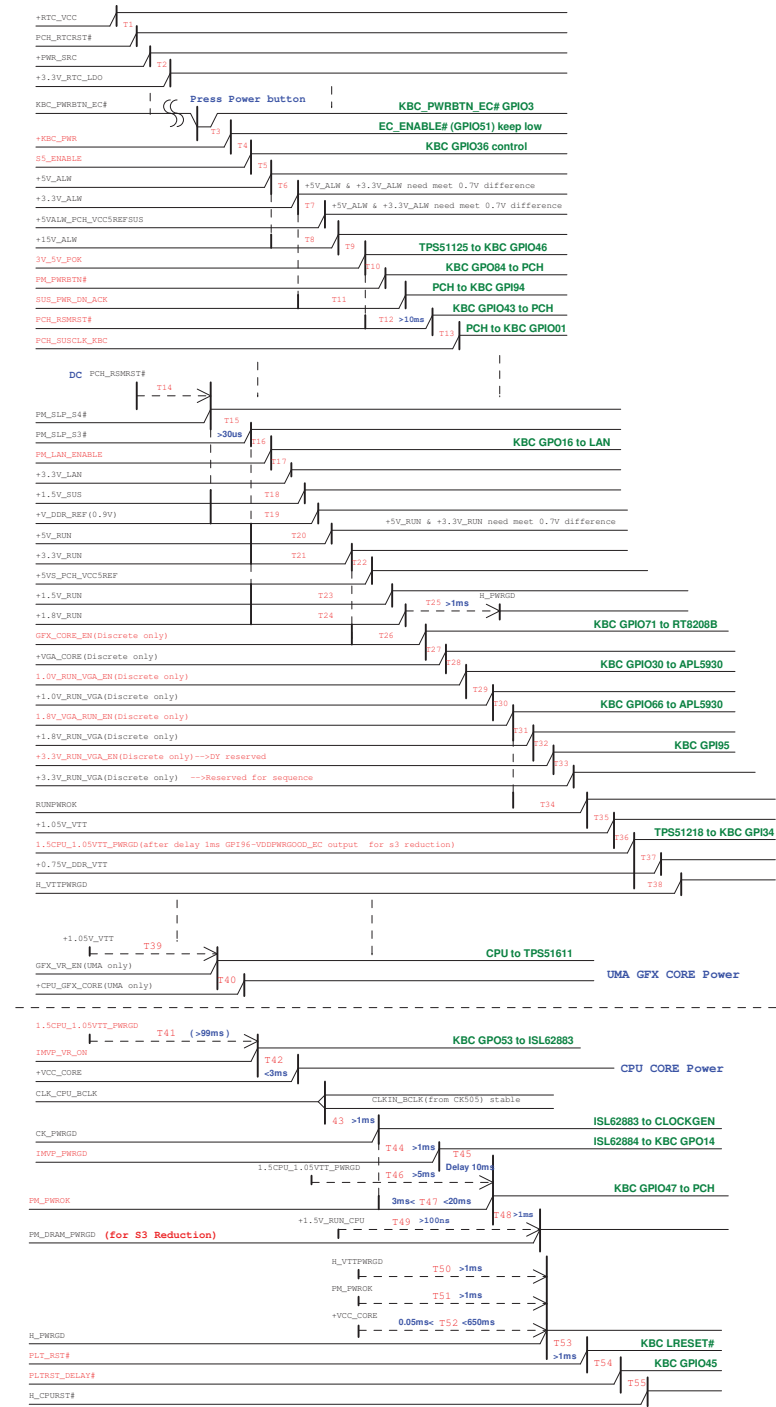
(AC mode)

red word: KBC GPIO



(DC mode)

red word: KBC GPIO



<http://laptop-motherboard-schematic.blogspot.com/>

(Blanking)

<Core Design>



Title		Change History	
Size	Document Number	Rev	
A3	Berry	A00	
Date:	Wednesday, February 10, 2010	Sheet	92 of 92