Ansenal DJ1 UMA Schematics Document

AMD Danube CPU S1G4

RS880M + SB820M

2010-05-25

REV : A00

DY : Nopop Component

<Core Design>

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Title	Cover Page	
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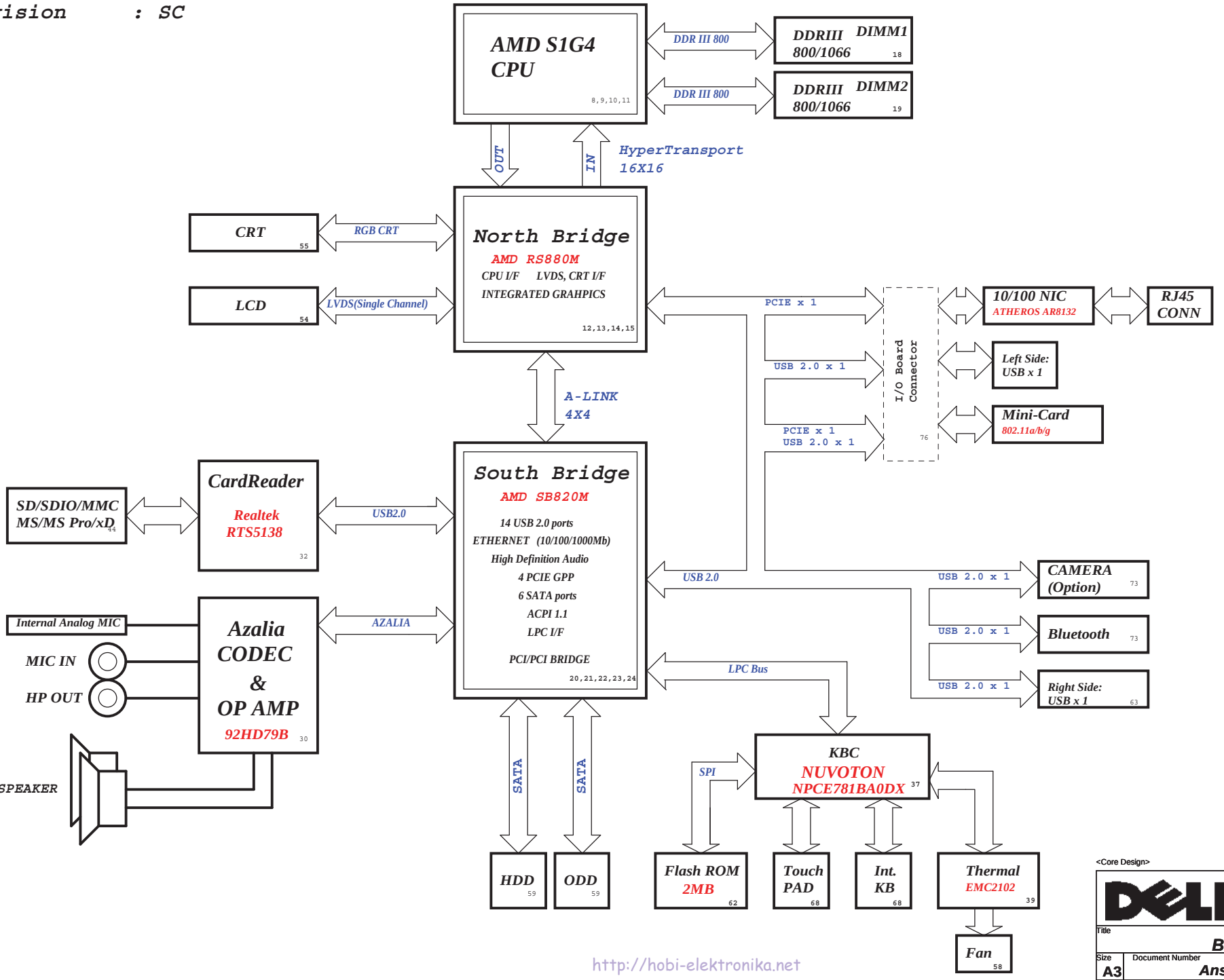
Project code : 91.4EK01.001
PCB P/N : 09940
Revision : SC

Ansenal DJ1 AMD UMA Block Diagram



CHARGER BQ24745RHDR	
INPUTS	OUTPUTS
+DC_IN_SS +CHAGER_SRC	+PWR_SRC

SYSTEM DC/DC RT8205BGQW-GP 46	
INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW2 +3.3V_RTC_LDO +5V_ALW +3.3V_ALW

SYSTEM DC/DC RT8209EGQW 50	
INPUTS	OUTPUTS
+PWR_SRC	+1.1V_RUN

CPU CORE ISL6265AHRTZ-T-GP 47	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE +VDDNB

DDR III SUS&VTT RT8207GQW-GP 49	
INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS

SYSTEM DC/DC APL5930KAI 52	
INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN

SYSTEM DC/DC Swithes/RT9013 42,53	
INPUTS	OUTPUTS
+3.3V_ALW	+3.3V_RUN
+5V_ALW	+5V_RUN
+1.5V_SUS	+1.5V_RUN
+3.3V_RUN	+2.5V_RUN

SYSTEM DC/DC RT9025 48,51	
INPUTS	OUTPUTS
+3.3V_ALW	+1.1V_ALW
+1.5V_SUS	+CPU_VDDR

PCB LAYER
L1: Top
L2: VCC
L3: Signal
L4: Signal
L5: GND
L6: Bottom

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Title: Block Diagram

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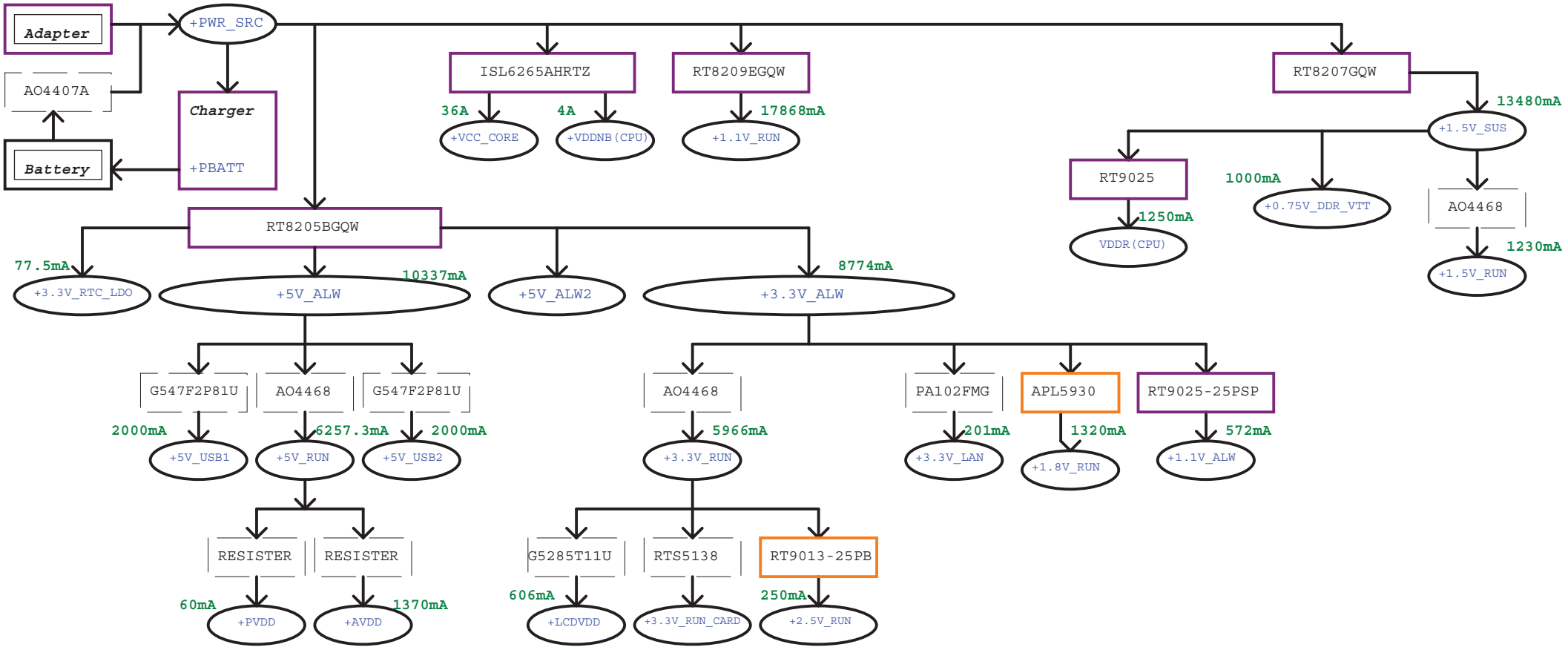
Power Block Diagram

Power Shape

Regulator | LDO | Switch



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Title	Power Block Diagram	
Size: Custom	Document Number: Ansenal DJ1 AMD UMA	Rev: A00
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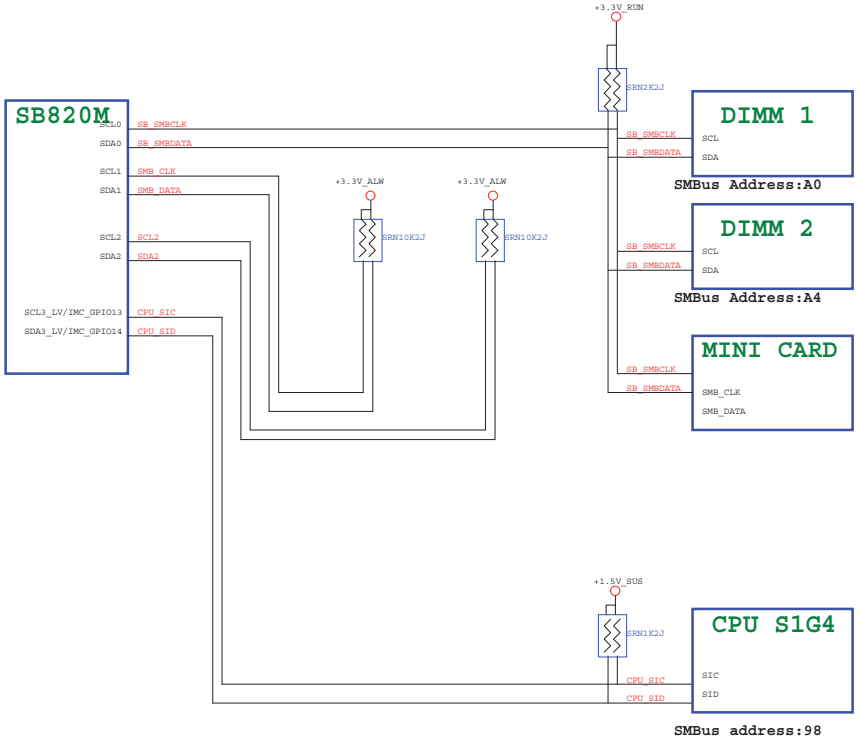
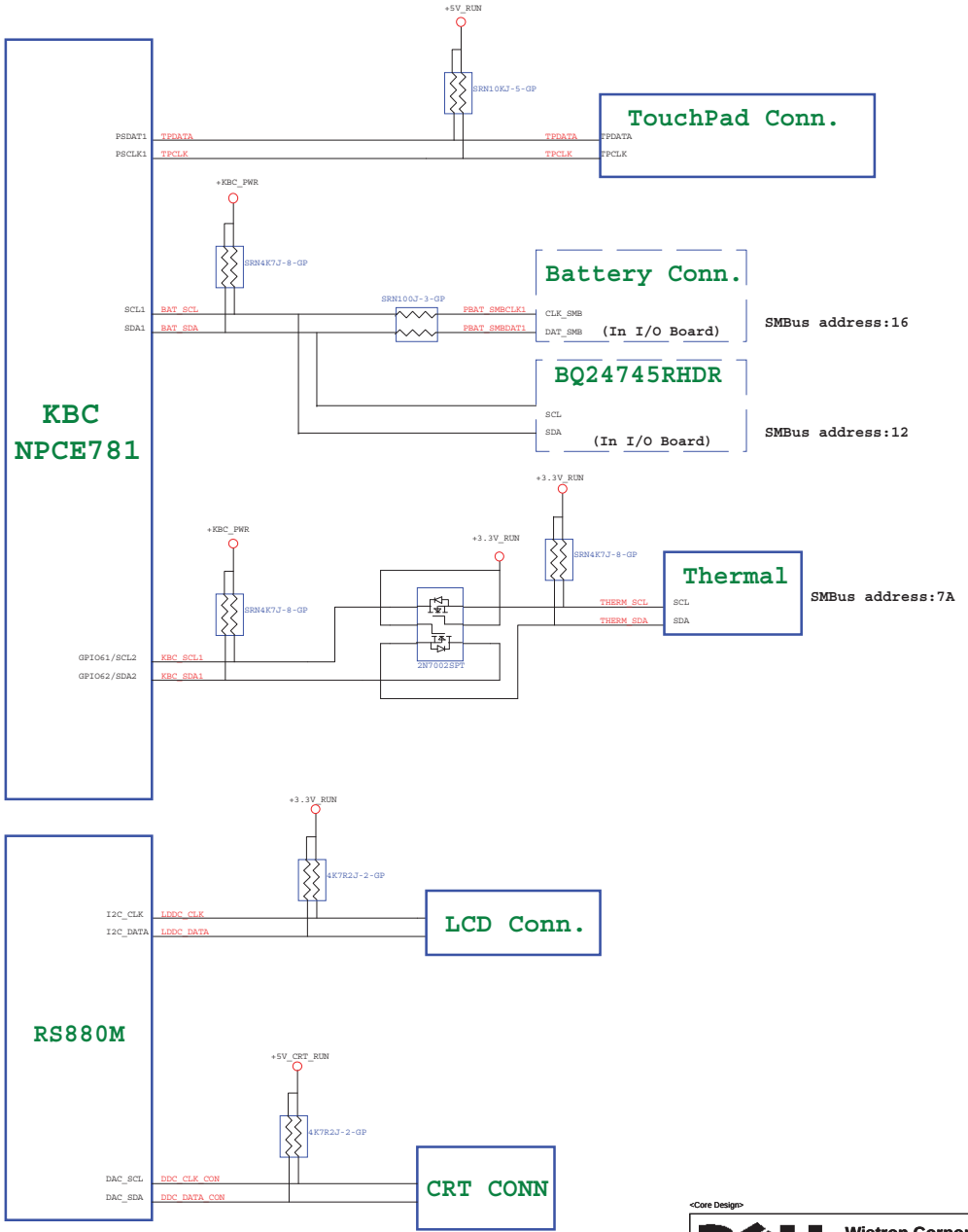
SB820M SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS BLOCK DIAGRAM

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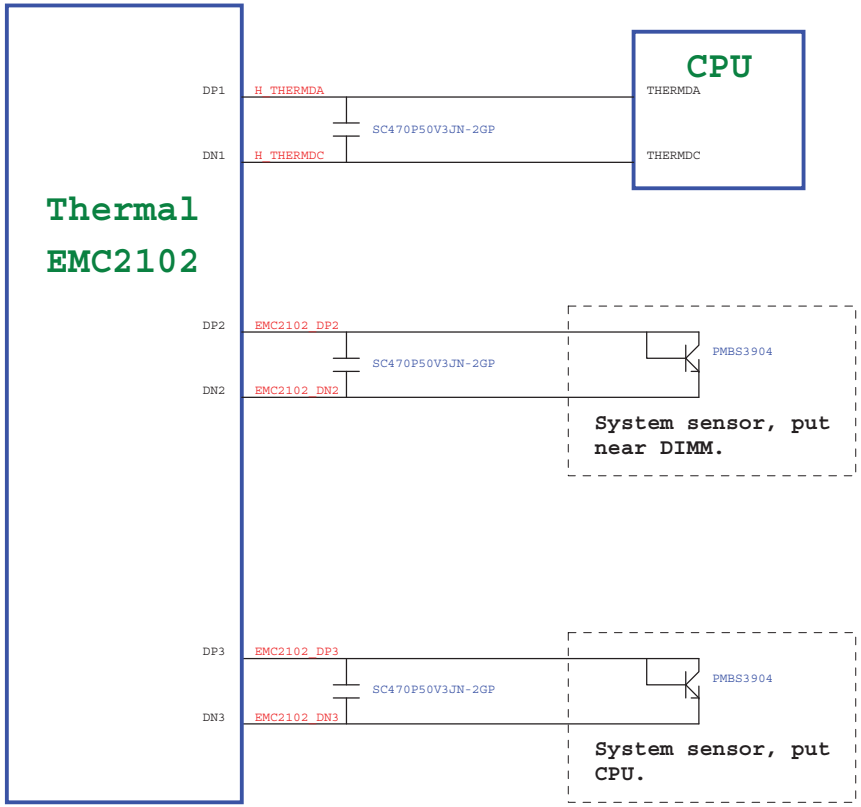
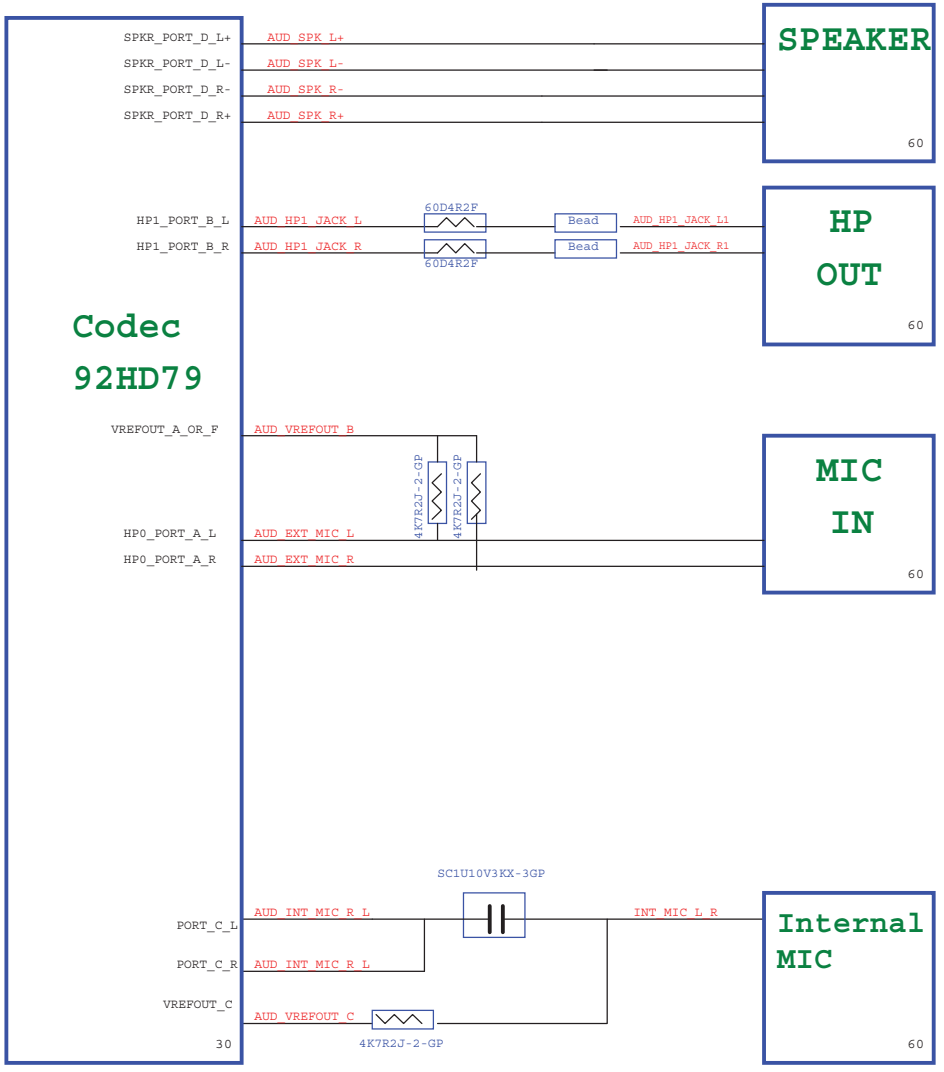
Thermal Block Diagram



Audio Block Diagram



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Title: THERMAL/AUDIO BLOCK DIAGRAM

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SB820M Strapping

Capture from 45484 Rev. 1.02 AMD SB8xx-Series Southbridge Design Guide

Name	Strap Name	Schematic Note
LPCCLK0	ECEnableStrap	Embedded Controller (EC) * 0 V - Disabled 3.3 V - Enabled
EC_PWM3 EC_PWM2	{ROMTYPE_1, ROMTYPE_0 }	ROMTYPE_1 / ROMTYPE_0 / ROM TYPE 3.3V / 0V / SPI ROM 3.3V / 3.3V / Reserved 0V / 0V / Firmware Hub * 0V / 3.3V / LPC ROM (supports both LPC and PMC ROM types)
LPCCLK1	CLKGEN	Defines clock generator 0V - External clock mode: Use 100-MHz PCIeR clock as reference clock and generate i nternal clocks only. * 3.3V- Integrated clock mode: Use 25-MHz crystal clock and generate both internal and external clocks
PCICLK1	BIF_GEN2_ COMPLIANCE_Strap	Set PCIe to Gen II mode 0V- Force PCIe interface at Gen I mode * 3.3V- PCIe interfacce is at Gen II mode Not Applicable to SB820M but provision for pull-down is required.
PCICLK2	BootFailTmrEn	Watchdog function * 0V- Disable the boot fail timer function 3.3V- Enable the boot fail timer function
PCICLK3	DefaultStrapMode	Default Debug Straps * 0V- Disable Debug Straps. 3.3V- Select external Debug Straps
PCICLK4	CPUClkSel	CPU/NB HT Clock Selection 0V- Reserved. * 3.3V- Required setting for integrated clock mode. This strap is not used if the strap CLKGEN is configured for external clock generator mode.
AZ_SDOUT	CoreSpeedMode	Slow down core clock for low power platform. * 0V- Performance mode 3.3V- Low Power mode

NB880M Strapping

Capture from 46113 rs880m ds nda 1.03

Name	Strap Function	Schematic Note
DAC_VSYNC	STRAP_DEBUG_BUS_GPIO _ENABLE#	Enables debug bus access through memory I/O pads and GPIOs. 0: Enable * 1: Disable
DAC_HSYNC	SIDE_PORT_EN#	Indicates if memory side-port is available or not 0: Available * 1: Not available
SUS_STAT#	LOAD_EEPROM_STRAPS#	Selects loading of strap values from EEPROM. 0: I2C master can load strap values from EEPROM if connected, or use default values if EEPROM is not connected. Please refer to RS880M's reference schematics for system level implementation details. * 1: Use default values

USB Table

USB	
Pair	Device
0	USB1
1	USB3
2	USB2 (I/O Board)
3	Reserve
4	WLAN
5	Reserve
6	Reserve
7	Reserve
8	Reserve
9	BLUETOOTH
10	CARD READER
11	CAMERA
12	Reserve
13	Reserve

PCIE Routing

LANE0	LAN
LANE1	MiniCard WLAN

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Title: Table of Content

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Title: Clock Generator ICS9LPRS480

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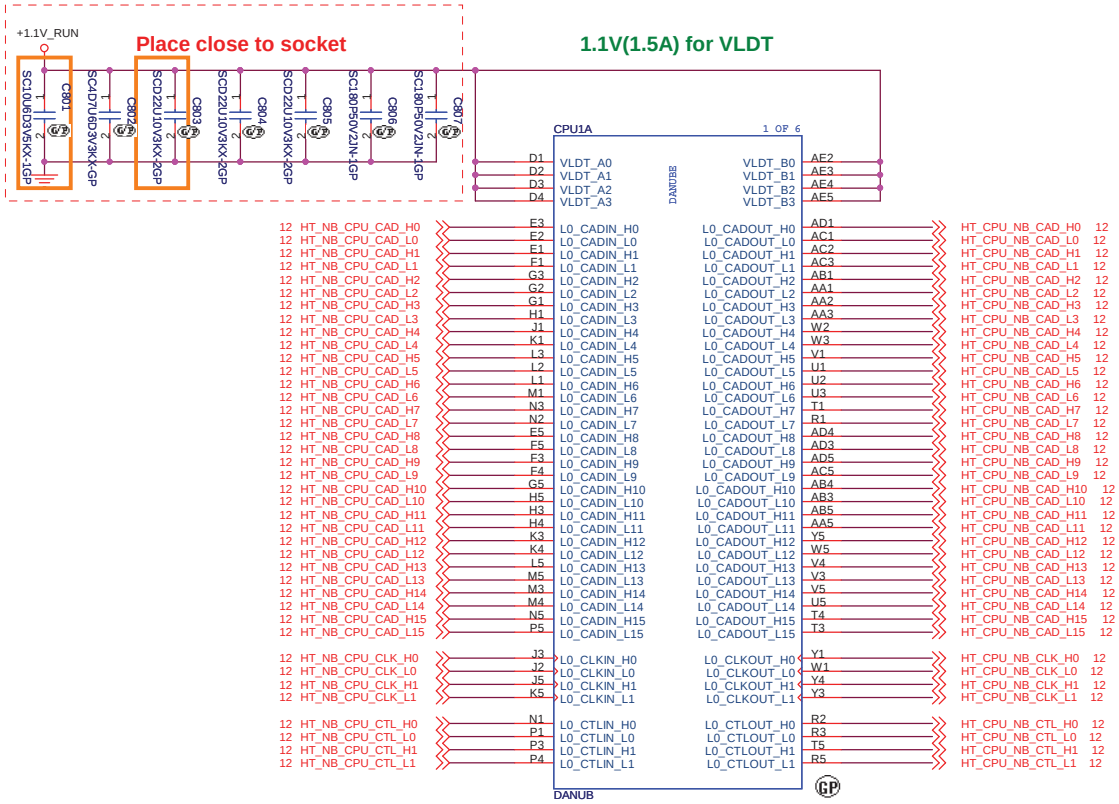
SSID = CPU



SKT-BGA638H176

1'nd 62.10055.111

2'nd 62.10055.171

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Title: CPU_HT_LINK I/F_(1/4)

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SSID = CPU

4.7UF*4
0.22UF*4
1000PF*4
180PF*4

Place near to CPU

+CPU_VDDR

SC4D7U6D3V3KX-GP C901
SC4D7U6D3V3KX-GP C902
SC4D7U6D3V3KX-GP C903
SC4D7U6D3V3KX-GP C915
SC22U10V3KX2GP C904
SC22U10V3KX2GP C914
SC22U10V3KX2GP C905
SC22U10V3KX2GP C906
SC1000P50V3JNGP-U C907
SC1000P50V3JNGP-U C915
SC1000P50V3JNGP-U C908
SC1000P50V3JNGP-U C909
SC180P50V2JN-1GP C910
SC180P50V2JN-1GP C911
SC180P50V2JN-1GP C916
SC180P50V2JN-1GP C912
DY

0.9V(1.25A) for VDDR
0.9V--DDR1066
1.05V---DDR1333 (1.75A)

+CPU_VDDR

CPU1B 2 OF 6 DANUBB

VDDR: D10, C10, B10, AD10, W10, AC10, AB10, AA10, A10
MEMZP AE10
MEMZN AE10
VDDR_SENSE Y10 TP_CPU_VDDR_SENSE
MEMVREF W17
MA_RESET# H16 ← 18 DDR3_A_DRAMRST#
MB_RESET# B18 → DDR3_B_DRAMRST#

+1.5V_SUS
R901 39D2R2F-L-GP MEMZP
R903 39D2R2F-L-GP MEMZN
C917 SC10U6D3V5KX-1GP

+0.75V_SUS_CPU_M_VREF
TP901
SC1U10V2KX-5GP C918
SC1U10V2KX-5GP C919
SC1U10V2KX-5GP C920
SC1000P50V3JN-GP-U C921
1KR3F-GP R902
1KR3F-GP R905
+1.5V_SUS
+V_DDR_REF
R904 0R3J-0-U-GP DY

CLOSE TO CPU

18 MEM_MA0_ODT0	T19	MA0_ODT0	MB_ODT0 W26 → MEM_MB0_ODT0 19
18 MEM_MA0_ODT1	V22	MA0_ODT1	MB_ODT1 W23 → MEM_MB0_ODT1 19
	U21	MA1_ODT0	MB0_ODT0 Y26
	V19	MA1_ODT1	MB1_ODT0
18 MEM_MA0_CS#0	T20	MA0_CS#0	MB_CS#0 V26 → MEM_MB0_CS#0 19
18 MEM_MA0_CS#1	U19	MA0_CS#1	MB_CS#1 W25 → MEM_MB0_CS#1 19
	U20	MA1_CS#0	MB1_CS#0 U22
	V20	MA1_CS#1	
18 MEM_MA_CKE0	J22	MA_CKE0	MB_CKE0 J25 → MEM_MB_CKE0 19
18 MEM_MA_CKE1	J20	MA_CKE1	MB_CKE1 H26 → MEM_MB_CKE1 19
18 MEM_MA_CLK0_P	N19	MA_CLK_H5	MB_CLK_H5 P22 → MEM_MB_CLK0_P 19
18 MEM_MA_CLK0_N	N20	MA_CLK_L5	MB_CLK_L5 R22 → MEM_MB_CLK0_N 19
	E16	MA_CLK_H1	MB_CLK_H1 A17
	F16	MA_CLK_L1	MB_CLK_L1 A18
	Y16	MA_CLK_H7	MB_CLK_H7 AF18
	AA16	MA_CLK_L7	MB_CLK_L7 AF17
18 MEM_MA_CLK1_P	P19	MA_CLK_H4	MB_CLK_H4 R26 → MEM_MB_CLK1_P 19
18 MEM_MA_CLK1_N	P20	MA_CLK_L4	MB_CLK_L4 R25 → MEM_MB_CLK1_N 19

18 MEM_MA_ADD[0..15] ↔ MEM_MB_ADD[0..15] 19

MEM_MA_ADD0	N21	MA_ADD0	MB_ADD0 P24 MEM_MB_ADD0
MEM_MA_ADD1	M20	MA_ADD1	MB_ADD1 N24 MEM_MB_ADD1
MEM_MA_ADD2	N22	MA_ADD2	MB_ADD2 P26 MEM_MB_ADD2
MEM_MA_ADD3	M19	MA_ADD3	MB_ADD3 N23 MEM_MB_ADD3
MEM_MA_ADD4	M22	MA_ADD4	MB_ADD4 N26 MEM_MB_ADD4
MEM_MA_ADD5	L20	MA_ADD5	MB_ADD5 L23 MEM_MB_ADD5
MEM_MA_ADD6	M24	MA_ADD6	MB_ADD6 N25 MEM_MB_ADD6
MEM_MA_ADD7	L21	MA_ADD7	MB_ADD7 L24 MEM_MB_ADD7
MEM_MA_ADD8	L19	MA_ADD8	MB_ADD8 M26 MEM_MB_ADD8
MEM_MA_ADD9	K22	MA_ADD9	MB_ADD9 K26 MEM_MB_ADD9
MEM_MA_ADD10	R21	MA_ADD10	MB_ADD10 T26 MEM_MB_ADD10
MEM_MA_ADD11	L22	MA_ADD11	MB_ADD11 L26 MEM_MB_ADD11
MEM_MA_ADD12	K20	MA_ADD12	MB_ADD12 L25 MEM_MB_ADD12
MEM_MA_ADD13	V24	MA_ADD13	MB_ADD13 W24 MEM_MB_ADD13
MEM_MA_ADD14	K24	MA_ADD14	MB_ADD14 J23 MEM_MB_ADD14
MEM_MA_ADD15	K19	MA_ADD15	MB_ADD15 J24 MEM_MB_ADD15

18 MEM_MA_BANK0	R20	MA_BANK0	MB_BANK0 R24 MEM_MB_BANK0 19
18 MEM_MA_BANK1	R23	MA_BANK1	MB_BANK1 U26 MEM_MB_BANK1 19
18 MEM_MA_BANK2	J21	MA_BANK2	MB_BANK2 J26 MEM_MB_BANK2 19
18 MEM_MA_RAS#	R19	MA_RAS#	MB_RAS# U25 MEM_MB_RAS# 19
18 MEM_MA_CAS#	T22	MA_CAS#	MB_CAS# U24 MEM_MB_CAS# 19
18 MEM_MA_WE#	T24	MA_WE#	MB_WE# U23 MEM_MB_WE# 19

DANUB

18 M_A_DQ[63..0] ↔ M_B_DQ[63..0] 19

CPU1C 3 OF 6 DANUBB

M_A_DQ0	G12	MA_DATA0	MB_DATA0	C11	M_B_DQ0
M_A_DQ1	F12	MA_DATA1	MB_DATA1	A11	M_B_DQ1
M_A_DQ2	H14	MA_DATA2	MB_DATA2	A14	M_B_DQ2
M_A_DQ3	G14	MA_DATA3	MB_DATA3	B14	M_B_DQ3
M_A_DQ4	H11	MA_DATA4	MB_DATA4	G11	M_B_DQ4
M_A_DQ5	H12	MA_DATA5	MB_DATA5	E11	M_B_DQ5
M_A_DQ6	C13	MA_DATA6	MB_DATA6	D12	M_B_DQ6
M_A_DQ7	E13	MA_DATA7	MB_DATA7	A13	M_B_DQ7
M_A_DQ8	H15	MA_DATA8	MB_DATA8	A15	M_B_DQ8
M_A_DQ9	E15	MA_DATA9	MB_DATA9	A16	M_B_DQ9
M_A_DQ10	F17	MA_DATA10	MB_DATA10	A19	M_B_DQ10
M_A_DQ11	H17	MA_DATA11	MB_DATA11	A20	M_B_DQ11
M_A_DQ12	E14	MA_DATA12	MB_DATA12	C14	M_B_DQ12
M_A_DQ13	F14	MA_DATA13	MB_DATA13	D14	M_B_DQ13
M_A_DQ14	C17	MA_DATA14	MB_DATA14	C18	M_B_DQ14
M_A_DQ15	G17	MA_DATA15	MB_DATA15	D18	M_B_DQ15
M_A_DQ16	G18	MA_DATA16	MB_DATA16	D20	M_B_DQ16
M_A_DQ17	C19	MA_DATA17	MB_DATA17	A21	M_B_DQ17
M_A_DQ18	D22	MA_DATA18	MB_DATA18	D24	M_B_DQ18
M_A_DQ19	E20	MA_DATA19	MB_DATA19	C25	M_B_DQ19
M_A_DQ20	E18	MA_DATA20	MB_DATA20	B20	M_B_DQ20
M_A_DQ21	F18	MA_DATA21	MB_DATA21	C20	M_B_DQ21
M_A_DQ22	B22	MA_DATA22	MB_DATA22	B24	M_B_DQ22
M_A_DQ23	C23	MA_DATA23	MB_DATA23	C24	M_B_DQ23
M_A_DQ24	F20	MA_DATA24	MB_DATA24	E23	M_B_DQ24
M_A_DQ25	F22	MA_DATA25	MB_DATA25	E24	M_B_DQ25
M_A_DQ26	H24	MA_DATA26	MB_DATA26	G25	M_B_DQ26
M_A_DQ27	J19	MA_DATA27	MB_DATA27	G26	M_B_DQ27
M_A_DQ28	F21	MA_DATA28	MB_DATA28	C26	M_B_DQ28
M_A_DQ29	F22	MA_DATA29	MB_DATA29	D26	M_B_DQ29
M_A_DQ30	H20	MA_DATA30	MB_DATA30	G23	M_B_DQ30
M_A_DQ31	H22	MA_DATA31	MB_DATA31	G24	M_B_DQ31
M_A_DQ32	Y24	MA_DATA32	MB_DATA32	AA24	M_B_DQ32
M_A_DQ33	AB24	MA_DATA33	MB_DATA33	AA23	M_B_DQ33
M_A_DQ34	AB22	MA_DATA34	MB_DATA34	AD24	M_B_DQ34
M_A_DQ35	AA21	MA_DATA35	MB_DATA35	AE24	M_B_DQ35
M_A_DQ36	W22	MA_DATA36	MB_DATA36	AA26	M_B_DQ36
M_A_DQ37	W21	MA_DATA37	MB_DATA37	AA25	M_B_DQ37
M_A_DQ38	Y22	MA_DATA38	MB_DATA38	AD26	M_B_DQ38
M_A_DQ39	AA22	MA_DATA39	MB_DATA39	AE25	M_B_DQ39
M_A_DQ40	Y20	MA_DATA40	MB_DATA40	AC22	M_B_DQ40
M_A_DQ41	AA20	MA_DATA41	MB_DATA41	AD22	M_B_DQ41
M_A_DQ42	AA18	MA_DATA42	MB_DATA42	AE20	M_B_DQ42
M_A_DQ43	AB18	MA_DATA43	MB_DATA43	AE20	M_B_DQ43
M_A_DQ44	AB21	MA_DATA44	MB_DATA44	AF24	M_B_DQ44
M_A_DQ45	AD21	MA_DATA45	MB_DATA45	AF23	M_B_DQ45
M_A_DQ46	AD19	MA_DATA46	MB_DATA46	AC20	M_B_DQ46
M_A_DQ47	Y18	MA_DATA47	MB_DATA47	AD20	M_B_DQ47
M_A_DQ48	AD17	MA_DATA48	MB_DATA48	AD18	M_B_DQ48
M_A_DQ49	W16	MA_DATA49	MB_DATA49	AE18	M_B_DQ49
M_A_DQ50	W14	MA_DATA50	MB_DATA50	AC14	M_B_DQ50
M_A_DQ51	Y14	MA_DATA51	MB_DATA51	AD14	M_B_DQ51
M_A_DQ52	Y17	MA_DATA52	MB_DATA52	AF19	M_B_DQ52
M_A_DQ53	AB17	MA_DATA53	MB_DATA53	AC18	M_B_DQ53
M_A_DQ54	AB15	MA_DATA54	MB_DATA54	AF16	M_B_DQ54
M_A_DQ55	AD15	MA_DATA55	MB_DATA55	AF15	M_B_DQ55
M_A_DQ56	AB13	MA_DATA56	MB_DATA56	AE13	M_B_DQ56
M_A_DQ57	AD13	MA_DATA57	MB_DATA57	AC12	M_B_DQ57
M_A_DQ58	W12	MA_DATA58	MB_DATA58	AB11	M_B_DQ58
M_A_DQ59	W11	MA_DATA59	MB_DATA59	Y11	M_B_DQ59
M_A_DQ60	AB14	MA_DATA60	MB_DATA60	AE14	M_B_DQ60
M_A_DQ61	AA14	MA_DATA61	MB_DATA61	AE14	M_B_DQ61
M_A_DQ62	AB12	MA_DATA62	MB_DATA62	AF11	M_B_DQ62
M_A_DQ63	AA12	MA_DATA63	MB_DATA63	AD11	M_B_DQ63

18 M_A_DM[7..0] ↔ M_B_DM[7..0] 19

M_A_DM0	E12	MA_DM0	MB_DM0	A12	M_B_DM0
M_A_DM1	C15	MA_DM1	MB_DM1	B16	M_B_DM1
M_A_DM2	E19	MA_DM2	MB_DM2	A22	M_B_DM2
M_A_DM3	F24	MA_DM3	MB_DM3	E25	M_B_DM3
M_A_DM4	AC24	MA_DM4	MB_DM4	AB26	M_B_DM4
M_A_DM5	Y19	MA_DM5	MB_DM5	AE22	M_B_DM5
M_A_DM6	AB16	MA_DM6	MB_DM6	AC16	M_B_DM6
M_A_DM7	Y13	MA_DM7	MB_DM7	AD12	M_B_DM7

18 M_A_DQS0	G13	MA_DQS_H0	MB_DQS_H0	C12	M_B_DQS0 19
18 M_A_DQS#0	H13	MA_DQS_L0	MB_DQS_L0	B12	M_B_DQS#0 19
18 M_A_DQS1	G16	MA_DQS_H1	MB_DQS_H1	D16	M_B_DQS1 19
18 M_A_DQS#1	G15	MA_DQS_L1	MB_DQS_L1	C16	M_B_DQS#1 19
18 M_A_DQS2	C22	MA_DQS_H2	MB_DQS_H2	A24	M_B_DQS2 19
18 M_A_DQS#2	C21	MA_DQS_L2	MB_DQS_L2	A23	M_B_DQS#2 19
18 M_A_DQS3	G22	MA_DQS_H3	MB_DQS_H3	F26	M_B_DQS3 19
18 M_A_DQS#3	G21	MA_DQS_L3	MB_DQS_L3	E26	M_B_DQS#3 19
18 M_A_DQS4	AD23	MA_DQS_H4	MB_DQS_H4	AC25	M_B_DQS4 19
18 M_A_DQS#4	AC23	MA_DQS_L4	MB_DQS_L4	AC26	M_B_DQS#4 19
18 M_A_DQS5	AB19	MA_DQS_H5	MB_DQS_H5	AF21	M_B_DQS5 19
18 M_A_DQS#5	AB20	MA_DQS_L5	MB_DQS_L5	AF22	M_B_DQS#5 19
18 M_A_DQS6	Y15	MA_DQS_H6	MB_DQS_H6	AE16	M_B_DQS6 19
18 M_A_DQS#6	W15	MA_DQS_L6	MB_DQS_L6	AD16	M_B_DQS#6 19
18 M_A_DQS7	W12	MA_DQS_H7	MB_DQS_H7	AF12	M_B_DQS7 19
18 M_A_DQS#7	W13	MA_DQS_L7	MB_DQS_L7	AE12	M_B_DQS#7 19

DANUB

<Core Design>

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Title: CPU_DDR(2/4)
Size: Custom | Document Number: Ansenal DJ1 AMD UMA | Rev: A00
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SSID = CPU

LYAOUT:ROUTE VDDA TRACE APPROX.
50mils WIDE(USE 2X25 mil TRACES TO
EXIT BALL FIELD) AND 500 mils LONG.

2.5V(250mA) for VDDA

CPU_CLK(200MHz)

For HDT DBG

Close CPU

Cloce To CPU

to power IC FB

For old HDT tool (3.3V level)

S1G4 not support MEMHOT

LAYOUT: Route FBCLKOUT_H/L
differentially impedance 80

HDT Connectors

<Core Design>

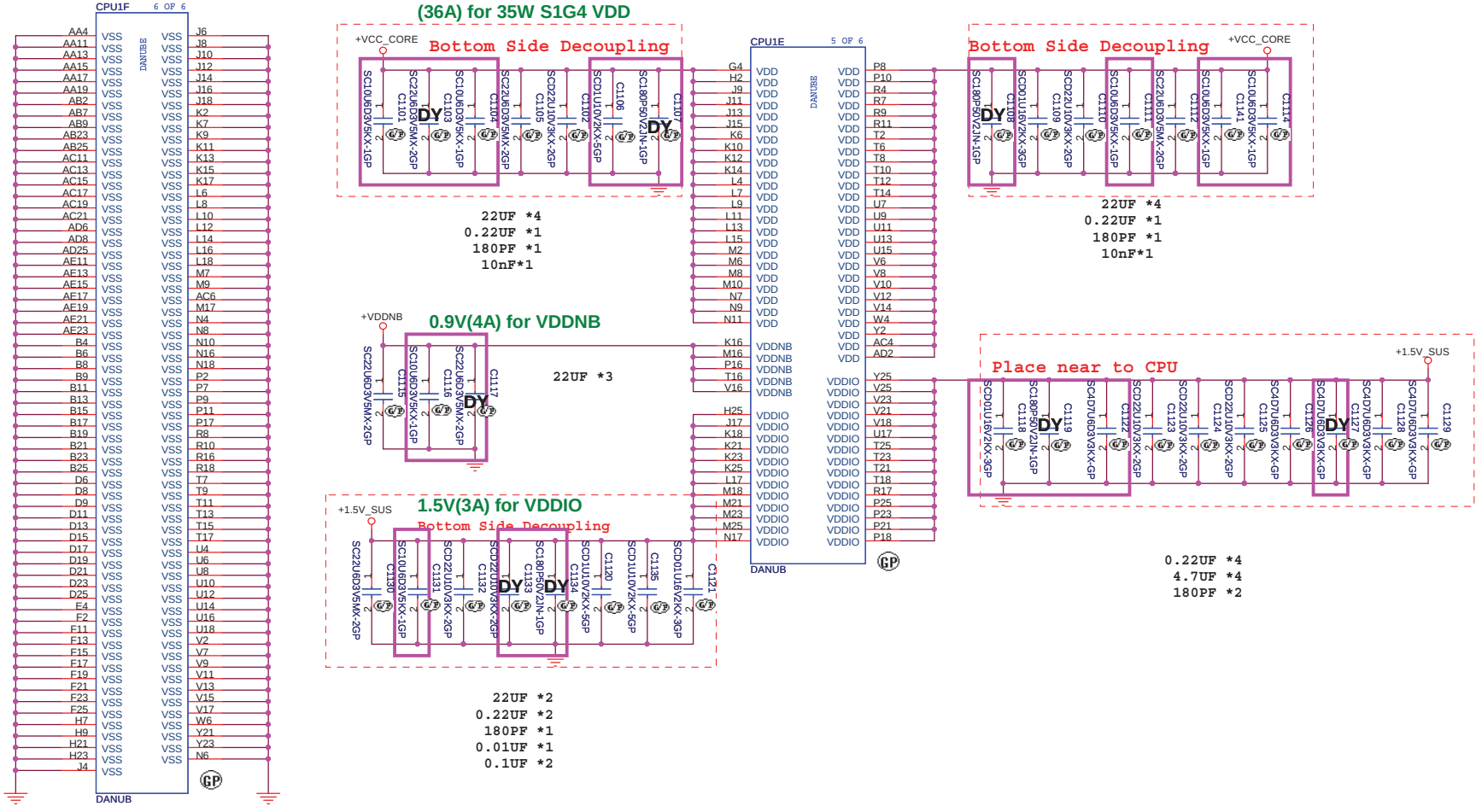
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_Control&Debug_(3/4)

Size: Custom | Document Number: Ansenal DJ1 AMD UMA | Rev: A00

Date: Thursday, May 27, 2010 | Sheet 10 of 90

SSID = CPU



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

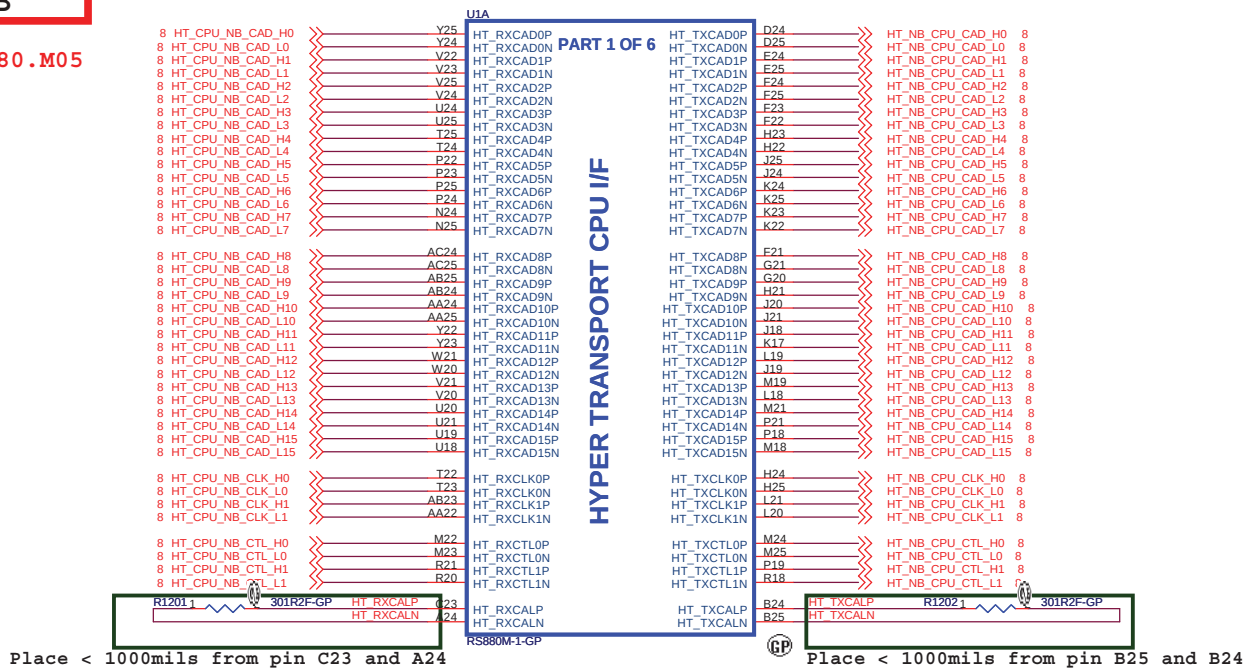
Title: CPU_Power_(4/4)

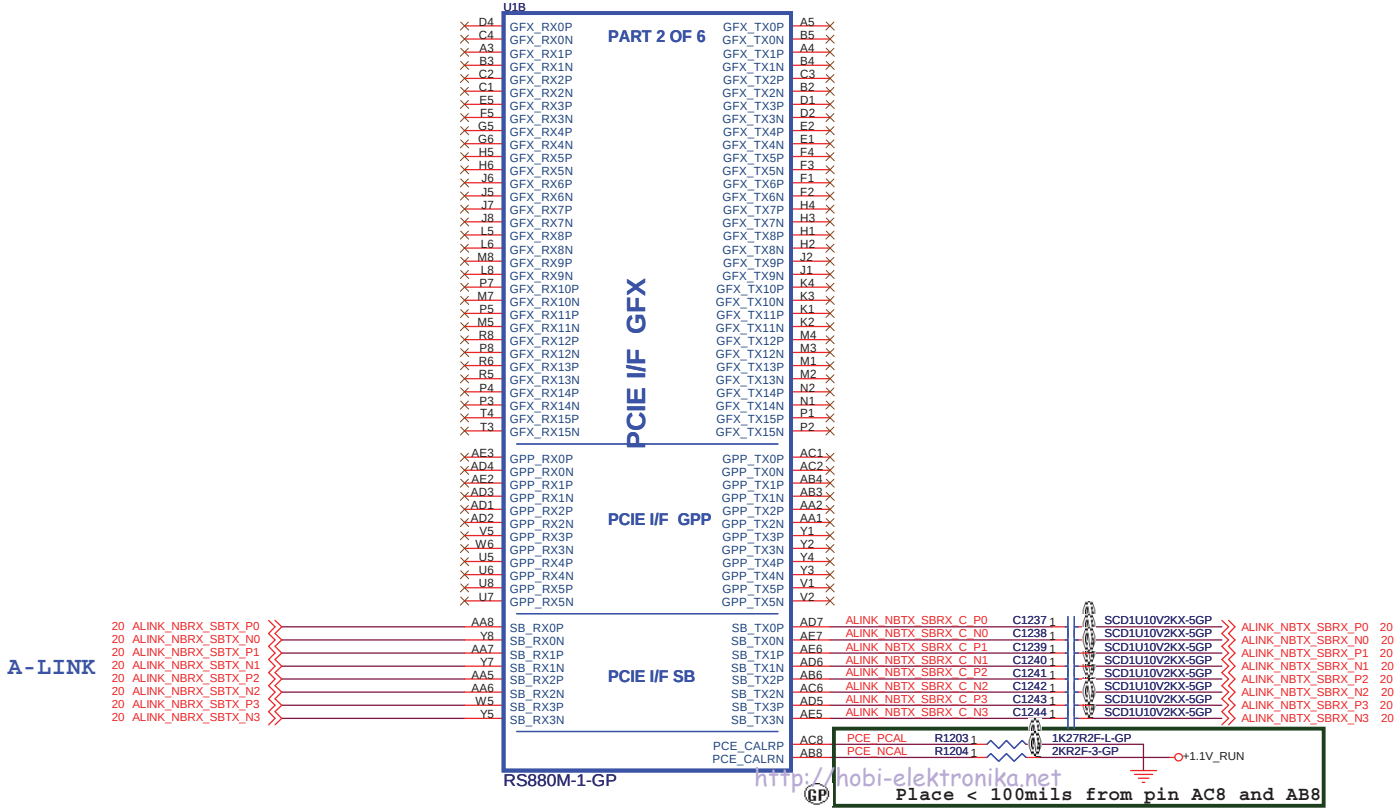
Size	Document Number	Rev
A3	Ansenal DJ1 AMD UMA	A00

Date: Thursday, May 13, 2010 Sheet 11 of 90

SSID = N.B

RS880M : 71.RS880.M05





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AMD-RS880M_HT LINK&PCIe(1/4)

Size: Custom | Document Number: Ansenal DJ1 AMD UMA | Rev: A00

Date: Thursday, May 27, 2010 | Sheet 12 of 90

SSID = N.B

RS880M : 71.RS880.M05

STRAP_DEBUG_BUS_GPIO_ENABLE# (RS880M use VGA_VSYNC)
Enables debug bus access through memory I/O pads and GPIOs.
*1 : Disable
0 : Enable

SIDE_PORT_EN# (RS880M use VGA_HSYNC)
*1 = Memory Side port Not available
0 = Memory Side port available

LOAD_EEPROM_STRAPS#(RS880M use SUS_STAT#)
Selects Loading of STRAPS From EEPROM
*1 : use Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

*DEFAULT

+1.1V_RUN — L1308 BLM15AG221SS1D-GP 220 ohm 300mA — 65mA — PLLVDD — C1312 SC2D2U6D3V3KX-GP

+1.8V_RUN -A00 R1323 0R0402-PAD — PLLVDD18 — C1311 SC1U10V3KX-3GP

+3.3V_RUN -A00 R1342 0R0603-PAD-1-GP — +3.3V_RUN_AVDD — 110mA — C1307 SC1U10V3KX-3GP

+1.8V_RUN — 20mA — C1306 SCD1U10V2KX-5GP

+1.8V_RUN — 4mA — C1308 SCD1U10V2KX-5GP

Layout Note
Trace at least 15 mil

+1.8V_RUN -A00 R1324 0R0402-PAD — +1.8V_VDDA18HTPLL — 20mA — C1302 SC2D2U6D3V3KX-GP DY — C1303 SCD1U10V2KX-5GP

+1.8V_RUN -A00 R1325 0R0402-PAD — +1.8V_VDDA18PCIEPLL — 120mA — C1304 SC2D2U6D3V3KX-GP DY — C1305 SCD1U10V2KX-5GP — C1301 SC22U6D3V5MX-2GP DY

UMA: DAC_CLK and DATA with 5V-tolerant.not need level shift

Trace at least 10 mil

+3.3V_RUN — R1302 3KR2J-2-GP — R1303 3KR2J-2-GP — VGA_VSYNC — VGA_HSYNC — R1304 3KR2J-2-GP DY — R1305 3KR2J-2-GP DY

X00
55 M_RED — R1326 150R2F-1-GP
55 M_GREEN — R1327 150R2F-1-GP
55 M_BLUE — R1328 150R2F-1-GP

55 VGA_HSYNC — VGA_HSYNC
55 VGA_VSYNC — VGA_VSYNC
55 DDC_CLK_CON — DDC_CLK_CON
55 DDC_DATA_CON — DDC_DATA_CON
R1306 715R2F-GP — DAC_RSET

20 PLTRST#_NB_GPU
41 NB_PWRGD_IN
NB_LDT_STOP#
NB_ALLOW_LDTSTOP

20 CLK_NBHT_CLK
20 CLK_NBHT_CLK#
20 NB_REFCLK_P
20 NB_REFCLK_N

X01
+3.3V_RUN — RN1302 SRN4K7J-8-GP
54 LDDC_CLK
54 LDDC_DATA
NB_GFX_CLK
NB_GFX_CLK#
TP1307 TP1308 NB_GPP_CLK NB_GPP_CLK#
20 NB_GPPSB_CLK
20 NB_GPPSB_CLK#
TP1301 TP1302 TP1303 TP1304 TP_NB_DDC_DATA0 TP_NB_DDC_CLK0 TP_NB_DDC_CLK1 TP_NB_DDC_DATA1
TP1305 TP_STRP_DATA TP_NB_RESERVED
R1318 2KR2J-1-GP
R1319 RS780_AUX_CAL 150R2F-1-GP

U1C — PART 3 OF 6 — RS880M-1-GP

CRT/TVOUT: AVDD1 AVDD2 AVDDDI AVSSDI AVDDQ AVSSQ — C_Pr Y COMP_Pb — RED REDb GREEN GREENb BLUE BLUEb — DAC_HSYNC DAC_VSYNC DAC_SCL DAC_SDA — DAC_RSET

PLL PWR LVTM: PLLVDD PLLVDD18 PLLVSS — VDDA18HTPLL 20mA — VDDA18PCIEPLL1 VDDA18PCIEPLL2 120mA

CLOCKs PM: SYSRESET# POWERGOOD LDTSTOP# ALLOW_LDTSTOP — HT_REFCLKP HT_REFCLKN — REFCLK_P/OSCIN REFCLK_N — GFX_REFCLKP GFX_REFCLKN — GPP_REFCLKP GPP_REFCLKN — GPPSB_REFCLKP GPPSB_REFCLKN

MIS.: I2C_CLK I2C_DATA DDC_DATA0/AUX0N DDC_CLK0/AUX0P DDC_CLK1/AUX1P DDC_DATA1/AUX1N — STRP_DATA — RESERVED — AUX_CAL

TXOUT_L0P TXOUT_L0N TXOUT_L1P TXOUT_L1N TXOUT_L2P TXOUT_L2N TXOUT_L3P TXOUT_L3N — TXOUT_U0P TXOUT_U0N TXOUT_U1P TXOUT_U1N TXOUT_U2P TXOUT_U2N TXOUT_U3P TXOUT_U3N — TXCLK_LP TXCLK_LN TXCLK_UP TXCLK_UN — VDDLTP18 VSSLTP18 — VDDLT18_1 VDDLT18_2 VDDLT33_1 VDDLT33_2 — VSSLT1 VSSLT2 VSSLT3 VSSLT4 VSSLT5 VSSLT6 VSSLT7 — LVDS_DIGON LVDS_BLON LVDS_ENA_BL — TMDS_HPD HPD — SUS_STAT# — THERMALDIODE_P THERMALDIODE_N — TESTMODE

VGA_TXAOUT0+ 54 — VGA_TXAOUT0- 54 — VGA_TXAOUT1+ 54 — VGA_TXAOUT1- 54 — VGA_TXAOUT2+ 54 — VGA_TXAOUT2- 54
VGA_TXACLK+ 54 — VGA_TXACLK- 54

+1.8V_RUN — 220 ohm 300mA — L1305 BLM15AG221SS1D-GP — 15mA — 300mA — R1329 0R0603-PAD-1-GP -A00 — VDDLTP18_R — VDDLT18_R — C1310 SCD1U10V2KX-5GP — C1313 SC4D7U6D3V3KX-GP DY — C1309 SC1U10V3KX-3GP

LCDVDD_EN_R — R1332 0R0402-PAD — LCDVDD_EN 54
BLON_R — R1331 0R0402-PAD — LBKLT_CTL 54
LVDS_BLEN — R1308 0R0402-PAD — PANEL_BKEN 37

RN1301 SRN4K7J-8-GP — X00

TMDS_HPD — TP1311
HPD — TP1306
NB_SUS_STAT# — R1317 0R0402-PAD — SUS_STAT# 21 — -A00
TESTMODE_NB — R1320 1K8R2F-GP

+1.5V_RUN — R1309 300R2J-4-GP
+1.8V_RUN — R1311 2K2R2J-GP
R1322 DY 0R2J-2-GP
U1301 SN74LVC2G07DCKR-GP
10,20 CPU_LDT_STOP# — NB_LDT_STOP# — C1314 SCD1U10V2KX-5GP

+1.8V_RUN — R1315 1KR2J-1-GP -A00 — 20 ALLOW_LDTSTOP — R1316 0R0402-PAD — NB_ALLOW_LDTSTOP

ALLOW_LDTSTOP:
1 = LDTSTOP# can be asserted
0 = LDTSTOP# has to be de-asserted

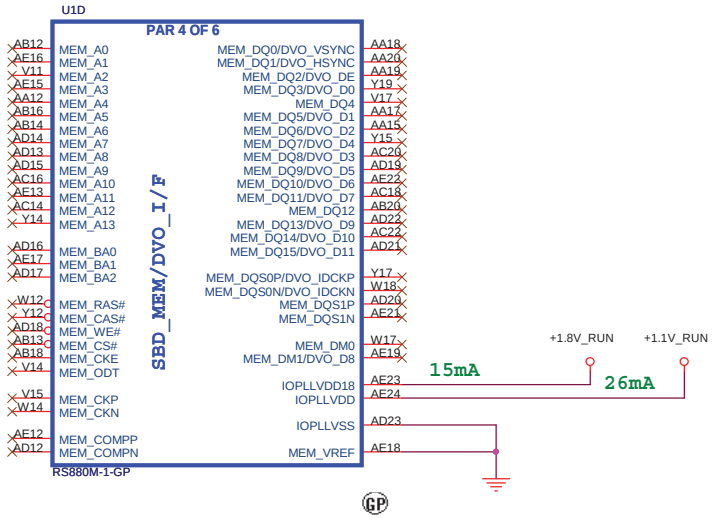
+3.3V_RUN — R1314 4K7R2J-2-GP — NB_SUS_STAT# — R1321 3KR2J-2-GP DY

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AMD-RS880M_LVDS&CRT_(2/4)
Size: Custom | Document Number: Ansenal DJ1 AMD UMA | Rev: A00
Date: Thursday, May 27, 2010 | Sheet 13 of 90

SSID = N.B



<Core Design>

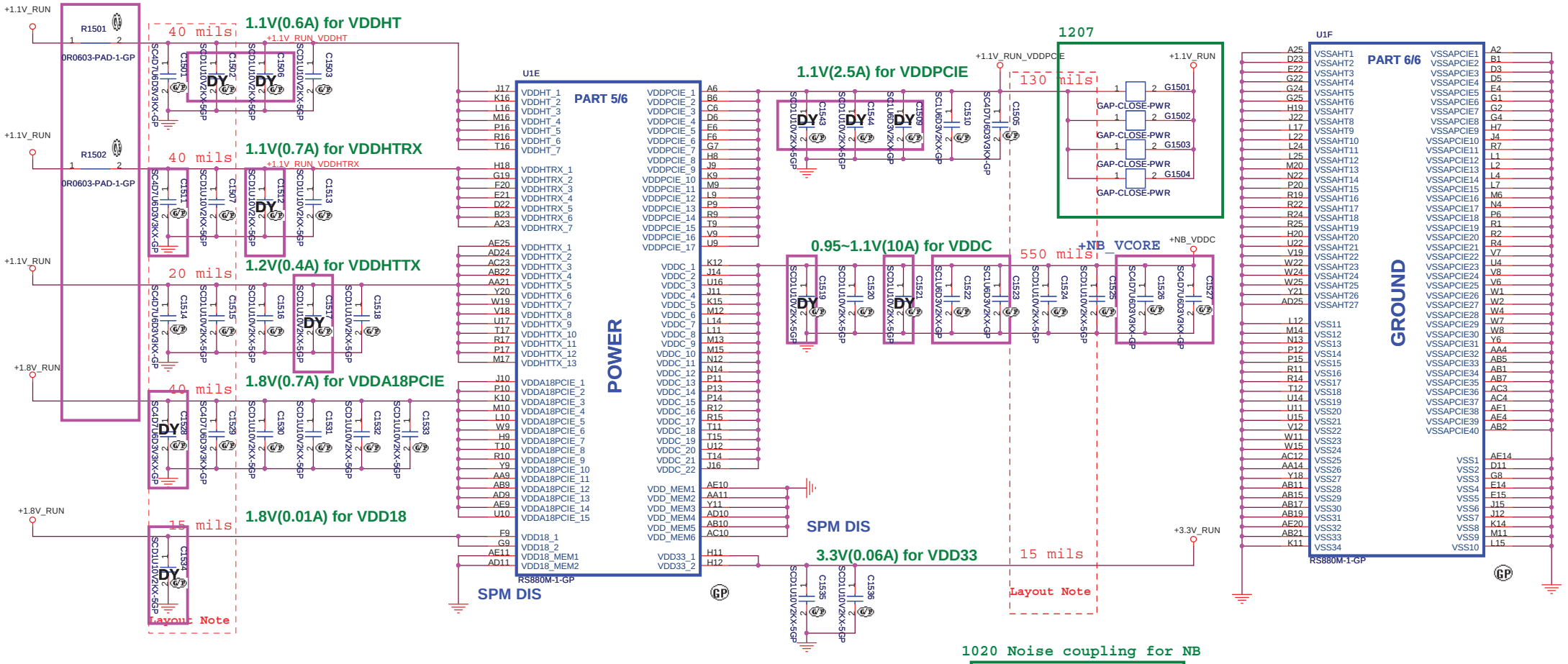
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AMD-RS880M_SidePort_(3/4)

Size	Document Number	Rev
A3	Ansenal DJ1 AMD UMA	A00

Date: Thursday, May 13, 2010 Sheet 14 of 90

SSID = N.B



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AMD-RS880M_PWR&GD_(4/4)

Size	Document Number	Rev
A3	Ansenal DJ1 AMD UMA	A00

Date: Thursday, May 13, 2010 Sheet 15 of 90

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: Ansenal DJ1 AMD UMA | Rev: A00

Date: Thursday, May 13, 2010 | Sheet 16 of 90

(Blanking)

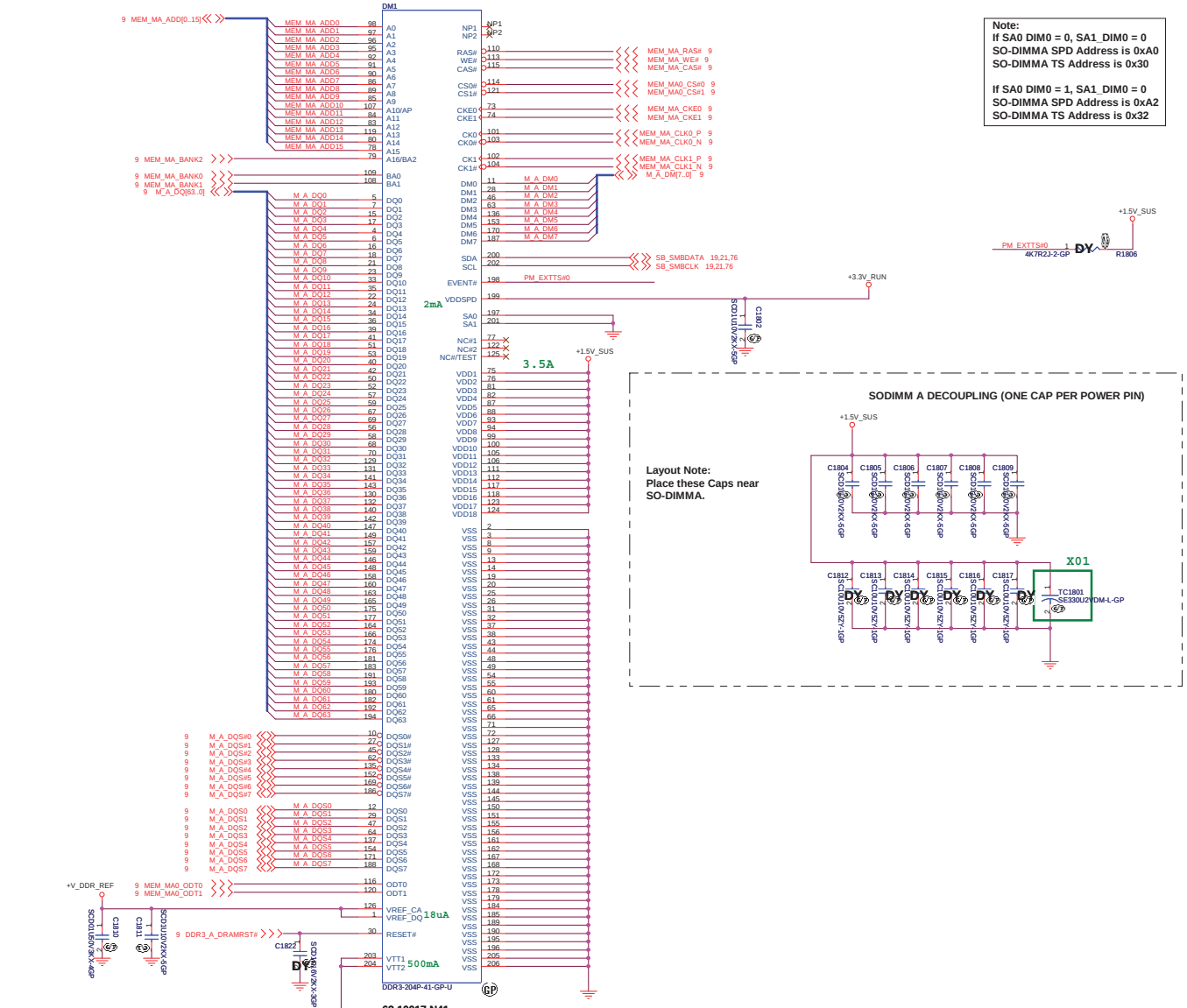
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: Ansenal DJ1 AMD UMA | Rev: A00

Date: Thursday, May 13, 2010 | Sheet 17 of 90



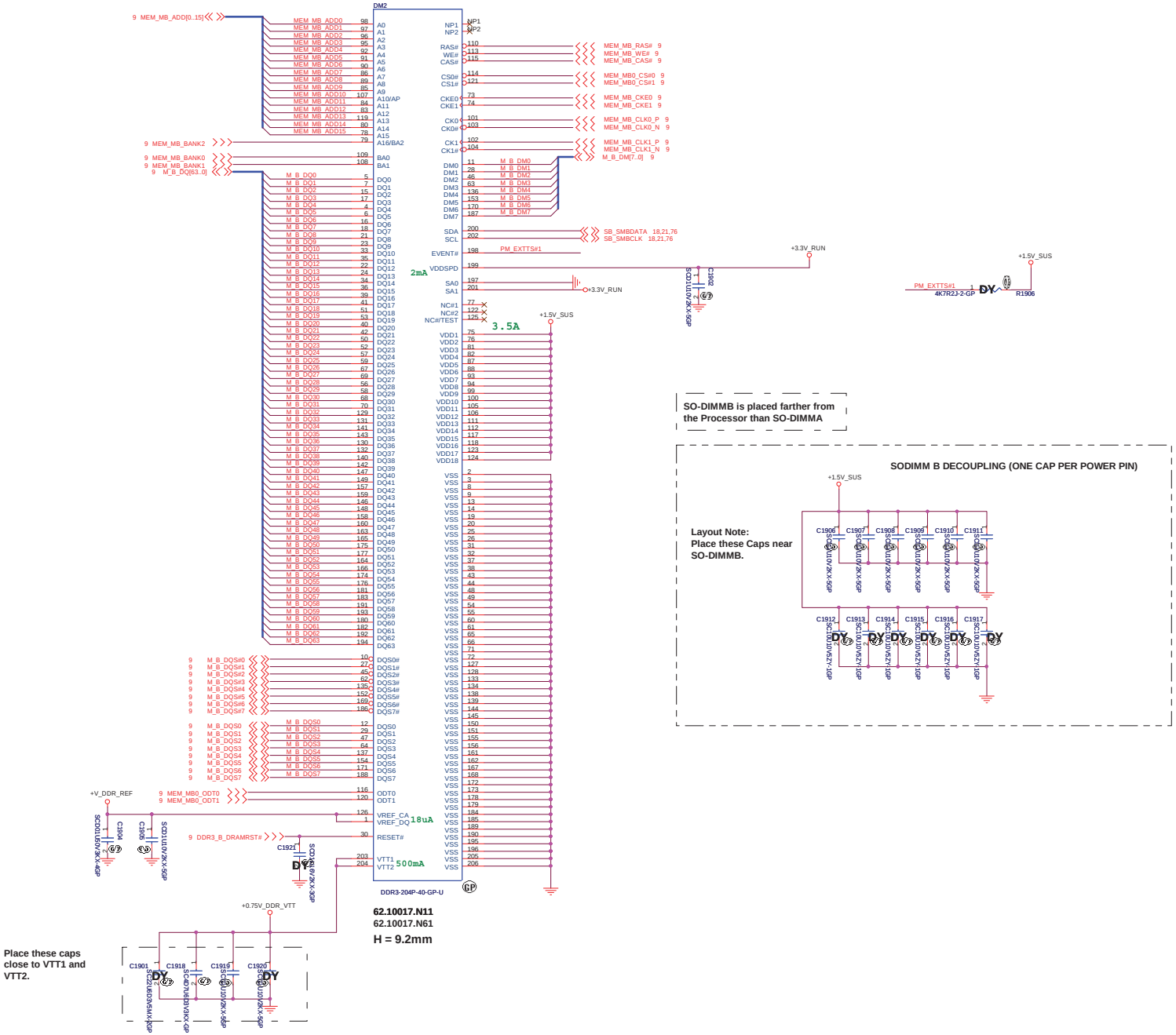
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM1

Size | Document Number: Ansenal DJ1 AMD UMA | Rev: A00

Date: Thursday, May 27, 2010 | Sheet 18 of 90



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM2

Size | Document Number: Ansenal DJ1 AMD UMA | Rev: A00

Date: Thursday, May 27, 2010 | Sheet 19 of 90

SSID = S.B

SB700 A12 : 71.SB8[illegible].M02

placed CAP closed SB820M

X01

PCI_CLK3

EC2002 SC10P50V2JN-4GP DY

U2A

Part 1 of 5

SB820M-1-GP

PCI EXPRESS INTERFACES

PCI CLKS

INTERFACE

CLOCK GENERATOR

LPC

CPU

RTC

STRAP PIN

1'nd 73.01G08.DHG
2'nd 73.01G08.L04

U2002 SNLVC1G08DCKRG4-GP

U2001 SNLVC1G08DCKRG4-GP

+3.3V_ALW

+3.3V_RUN

Place R <100mils form pins AD29,AD28

+1.1V_RUN_PCIE_VDDR

LAN

WLAN

X02

NOTE: SB8XX ONLY SUPPORTS 2 GPP PORT 2 AND 3 IS NOT SUPPORTED. (From CRB)

1nd 82.30020.851
2nd 82.30020.791

LPC Bus Routing first connects to MINICARD then connects to KBC

NB

KBC

Main Source

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB820M_PCIE&PCI_(1/5)

Size: A3 | Document Number: Ansenal DJ1 AMD UMA | Rev: A00

Date: Thursday, May 27, 2010 | Sheet 20 of 90

SSID = S.B

USB	
Pair	Device
0	USB1
1	USB3
2	USB2 (I/O Board)
3	RESERVED
4	WLAN
5	RESERVED
6	RESERVED
7	RESERVED
8	RESERVED
9	BLUETOOTH
10	CARD READER
11	CAMERA
12	RESERVED
13	RESERVED

X01

X00

1130

SBD DDR RESET

Close SB

GbE Controller Not Enabled

EC Not Implemented

JTAG_TDI
JTAG_RST#

EC Not Implemented

Not use

Strap Pin / define to use LPC or SPI ROM

<Core Design>

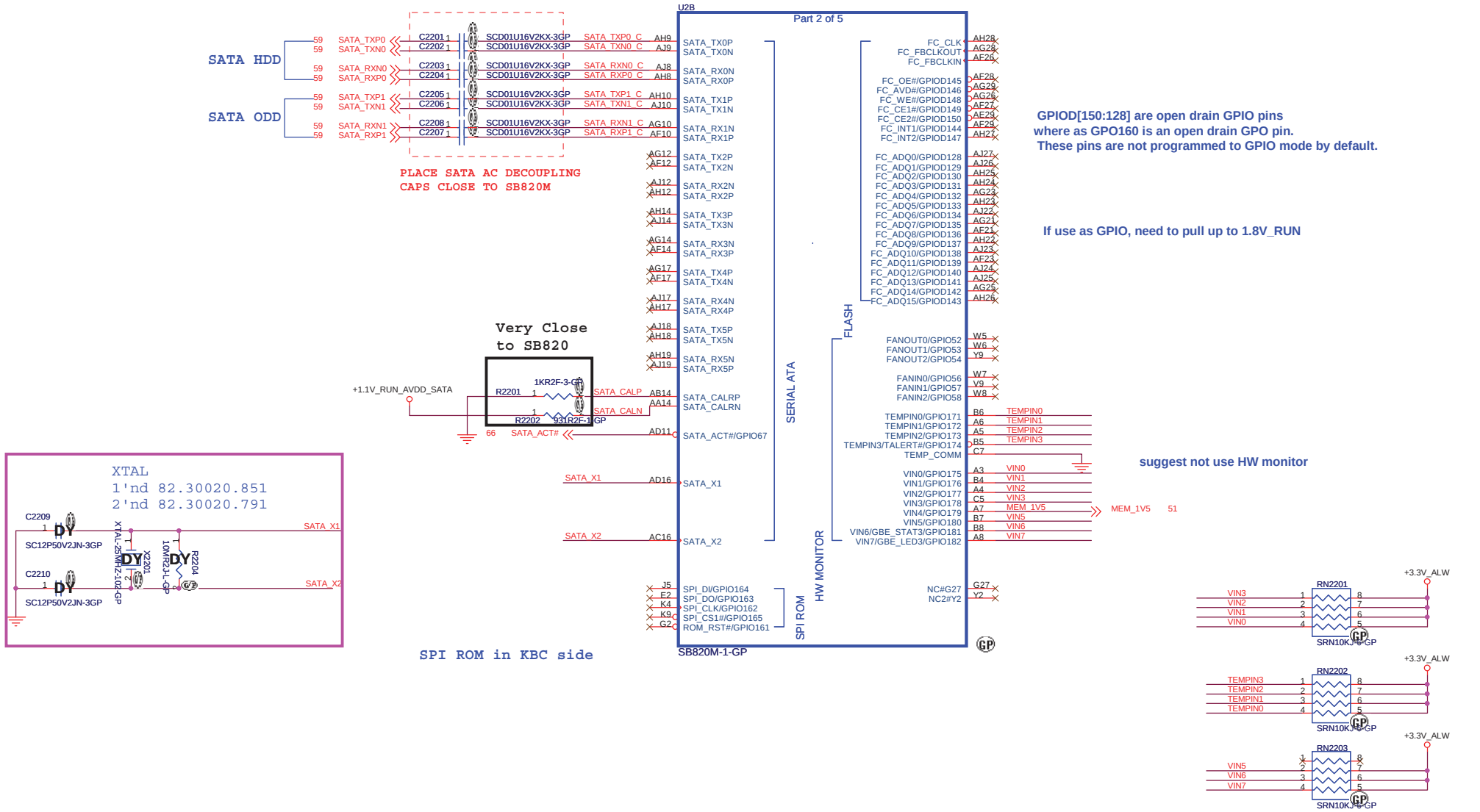
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB820M_USB&GPIO_(2/5)

Size: Custom | Document Number: Ansenal DJ1 AMD UMA | Rev: A00

Date: Thursday, May 27, 2010 | Sheet 21 of 90

SSID = S.B



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	SB820M_SATA-IDE_(3/5)	
Size: Custom	Document Number: Ansenal DJ1 AMD UMA	Rev: A00
Date: Thursday, May 27, 2010	Sheet 22 of 90	

SSID = S.B

U2C

Part 3 of 5

POWER

SB820M-1-GP

U2E

Part 5 of 5

GROUND

SB820M-1-GP

131mA

71mA

43mA

600mA

93mA

567mA

658mA

TBDmA

510mA

400 mA

32mA

113mA

TBDmA

197mA

17mA

5mA

62mA

47mA

WOL supported: Tied +3.3V_ALW
not supported: Tied +3.3V_RUN

WOL supported: Tied +1.1V_ALW
not supported: Tied +1.1V_RUN

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

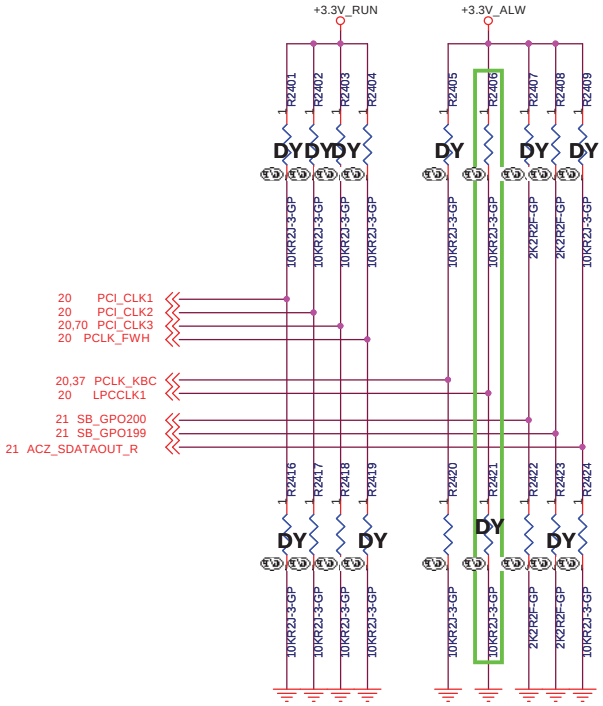
Title: SB820M_POWER&GND_(4/5)

Size: Custom | Document Number: Ansenal DJ1 AMD UMA | Rev: A00

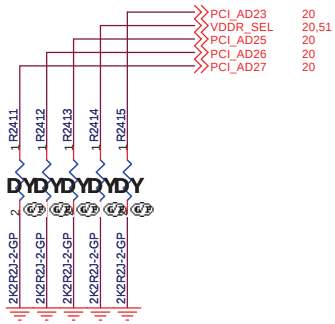
Date: Thursday, May 20, 2010 | Sheet 23 of 90

SSID = S.B

REQUIRED STRAPS



DEBUG STRAPS



REQUIRED SYSTEM STRAPS

USE this pin to determine INT/EXT CLK

	AZ_SDOUT#	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCLK_FWH (PCI_CLK4)	PCLK_KBC (LPCCLK0)	LPCCLK1	SB_GPO200 , SB_GPO199 ROM TYPE:
PULL HIGH	LOW POWER MODE	Allow PCIE GEN2 DEFAULT	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	non_Fusion CLOCK mode DEFAULT	ENABLE EC	DEFAULT CLKGEN ENABLED (Use Internal)	H, H = Reserved H, L = SPI ROM
PULL LOW	PERFORMANCE MODE DEFAULT	Force PCIE GEN1	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External)	L, H = LPC ROM DEFAULT L, L = FWH ROM

Not Applicable to SB820M
but provision for pull-down is required.

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL (DEFAULT)	Disable ILA AUTORUN (DEFAULT)	USE FC PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Disable PCI MEM BOOT (DEFAULT)
PULL LOW	BYPASS PCI PLL	Enable ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	Enable PCI MEM BOOT

Note: SB820 has 15K internal PU FOR PCI_AD[27:23]

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB820M_STRAPPING_(5/5)

Size: A3 | Document Number: Ansenal DJ1 AMD UMA | Rev: A00

Date: Thursday, May 27, 2010 | Sheet 24 of 90

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VCC_CORE)

Size | Document Number: Ansenal DJ1 AMD UMA | Rev: A00

Date: Thursday, May 13, 2010 | Sheet 25 of 90

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
CPU (VCC_GFXCORE)

Size | Document Number: Ansenal DJ1 AMD UMA | Rev: A00

Date: Thursday, May 13, 2010 | Sheet 26 of 90

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VSS)

Size | Document Number: Ansenal DJ1 AMD UMA | Rev: A00

Date: Thursday, May 13, 2010 | Sheet 27 of 90

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: Ansenal DJ1 AMD UMA | Rev: A00

Date: Thursday, May 13, 2010 | Sheet 28 of 90

(Blanking)

<Core Design>

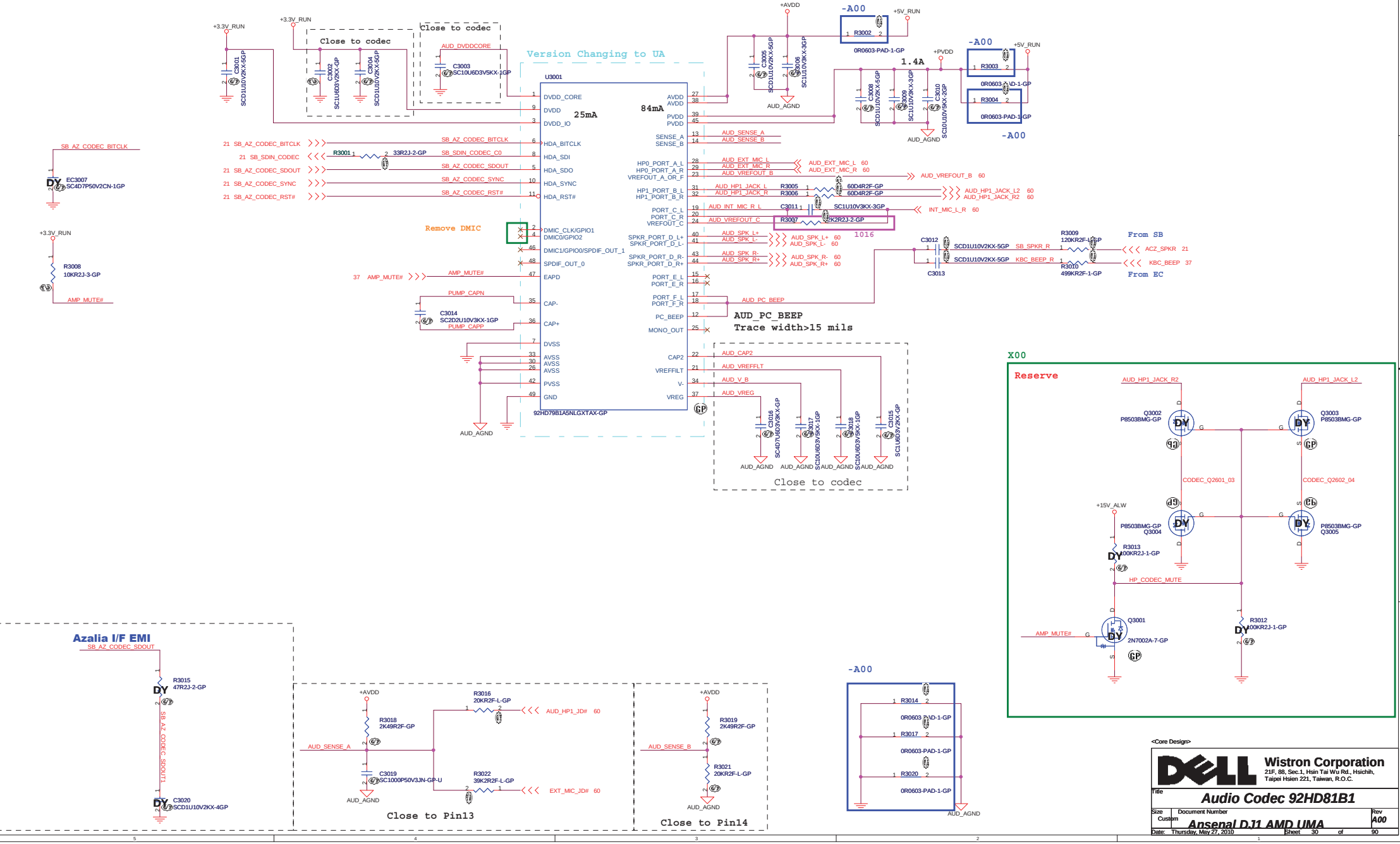
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: Ansenal DJ1 AMD UMA | Rev: A00

Date: Thursday, May 13, 2010 | Sheet 29 of 90

SSID = AUDIO



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<Core Design>

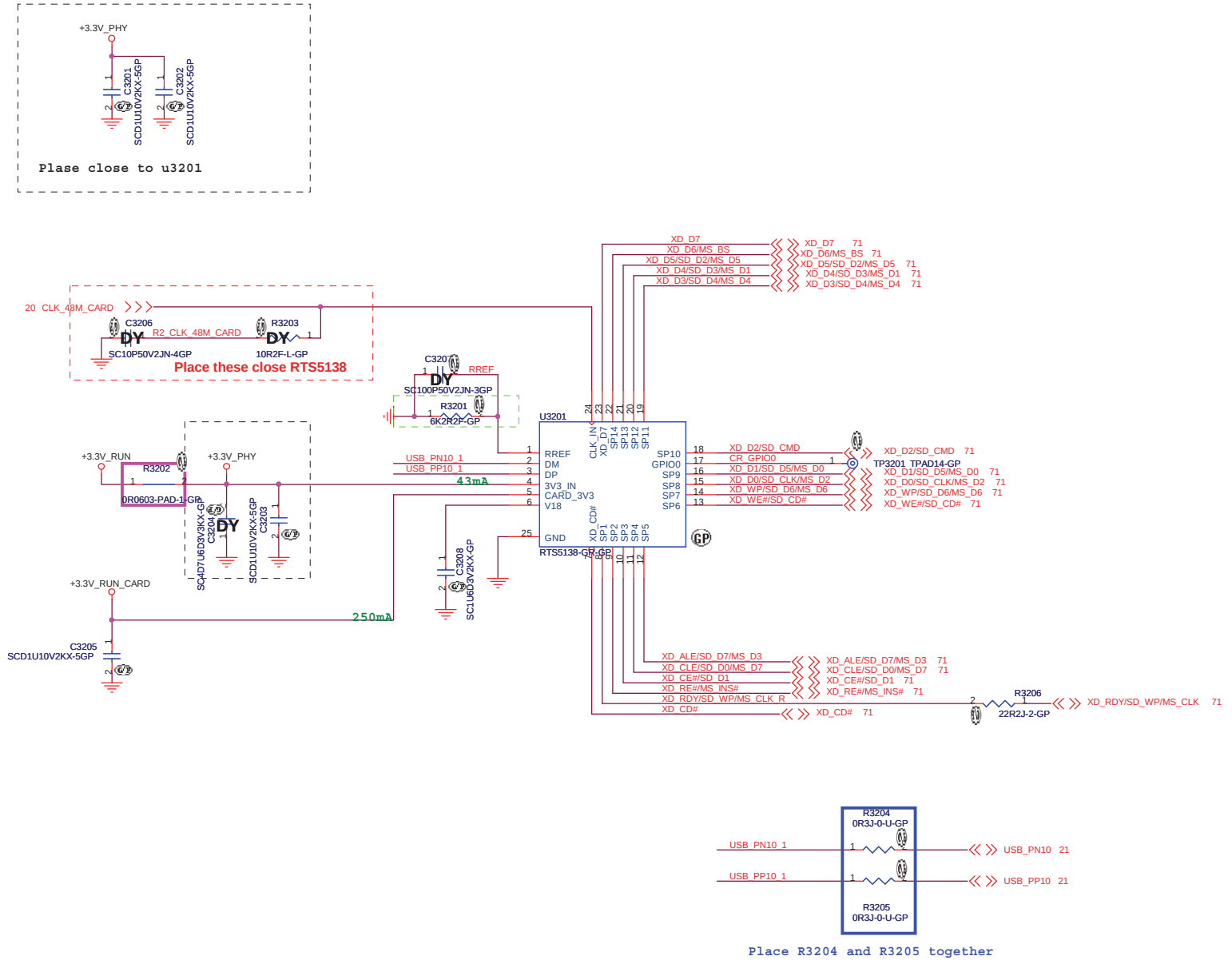
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: Ansenal DJ1 AMD UMA | Rev: A00

Date: Thursday, May 13, 2010 | Sheet 31 of 90

SSID = SDIO



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Card Reader-RTS5138

Size: Custom | Document Number: Ansenal DJ1 AMD UMA | Rev: A00

Date: Thursday, May 27, 2010 | Sheet 32 of 90

Close: UMA

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: Ansenal DJ1 AMD UMA | Rev: A00

Date: Thursday, May 13, 2010 | Sheet 33 of 90

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: Ansenal DJ1 AMD UMA | Rev: A00

Date: Thursday, May 13, 2010 | Sheet 34 of 90

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: Ansenal DJ1 AMD UMA | Rev: A00

Date: Thursday, May 13, 2010 | Sheet 35 of 90

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: Ansenal DJ1 AMD UMA | Rev: A00

Date: Thursday, May 13, 2010 | Sheet 36 of 90

SSID = KBC

CAP close to VCC-GND pin pair

U3701A

NPCE781BA0DX-GP

-A00

DJ PU
DG PD

UMA PD
DIS PU

X00

X01

X02

POP when support RCID function
2010/03/23

Place close to KBC

MB VERSION ID

	VER2	VER1	VER0
X00	0	0	0
X01	0	0	1
X02	0	1	0
A00	0	1	1

KBC CLK
EMI

Internal PU

0917
For EC to detect leakage

U3701B

PS/2

FIU

KBC

1207

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC Nuvoton NPCE781BA0DX

Size: A2 | Document Number: Ansenal DJ1 AMD UMA | Rev: A00

Date: Thursday, May 27, 2010 | Sheet 37 of 90

(Blanking)

<Core Design>

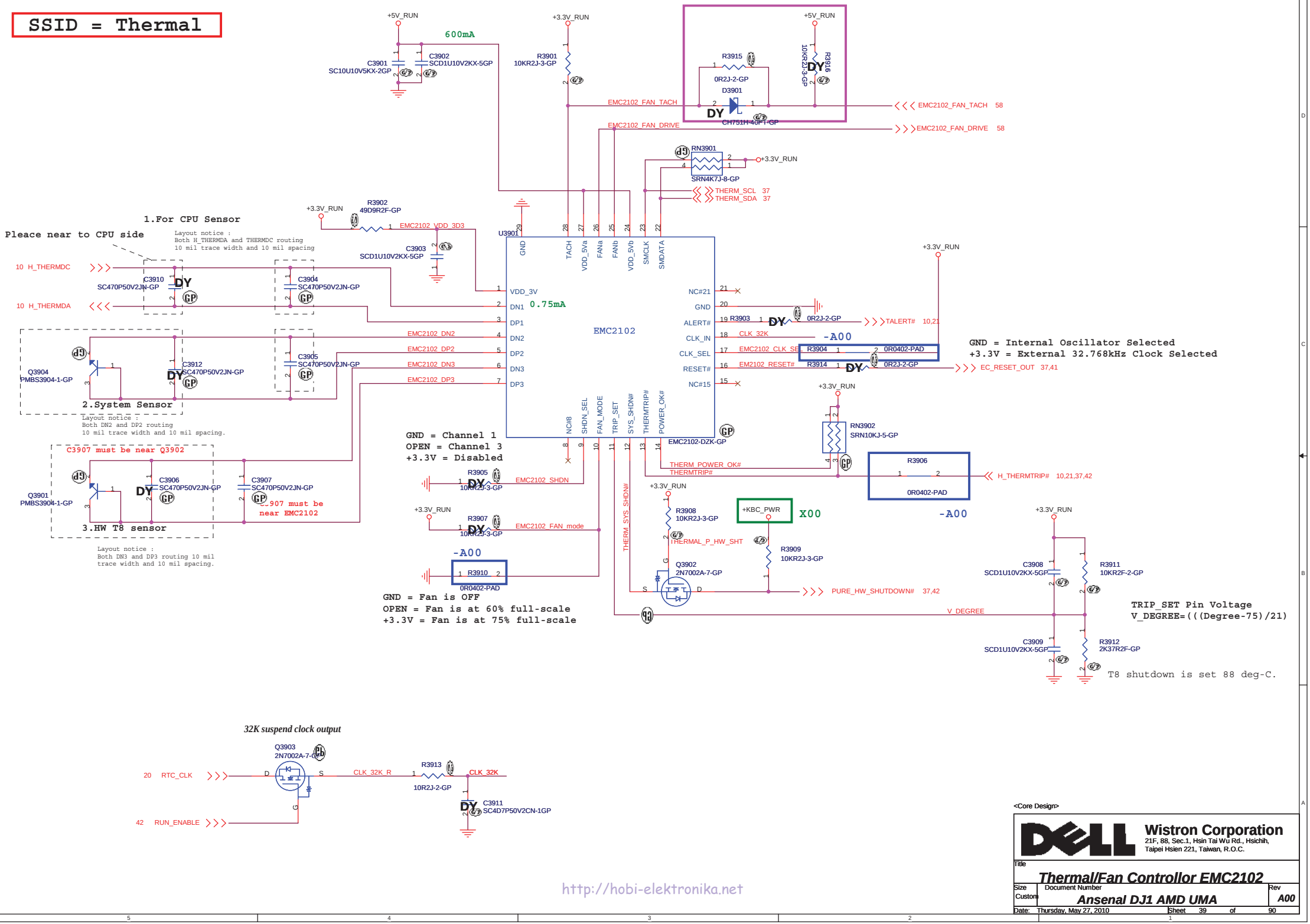
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: Ansenal DJ1 AMD UMA | Rev: A00

Date: Thursday, May 13, 2010 | Sheet 38 of 90

SSID = Thermal



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor EMC2102

Size: Custom | Document Number: Ansenal DJ1 AMD UMA | Rev: A00

Date: Thursday, May 27, 2010 | Sheet 39 of 90

(Blanking)

<Core Design>

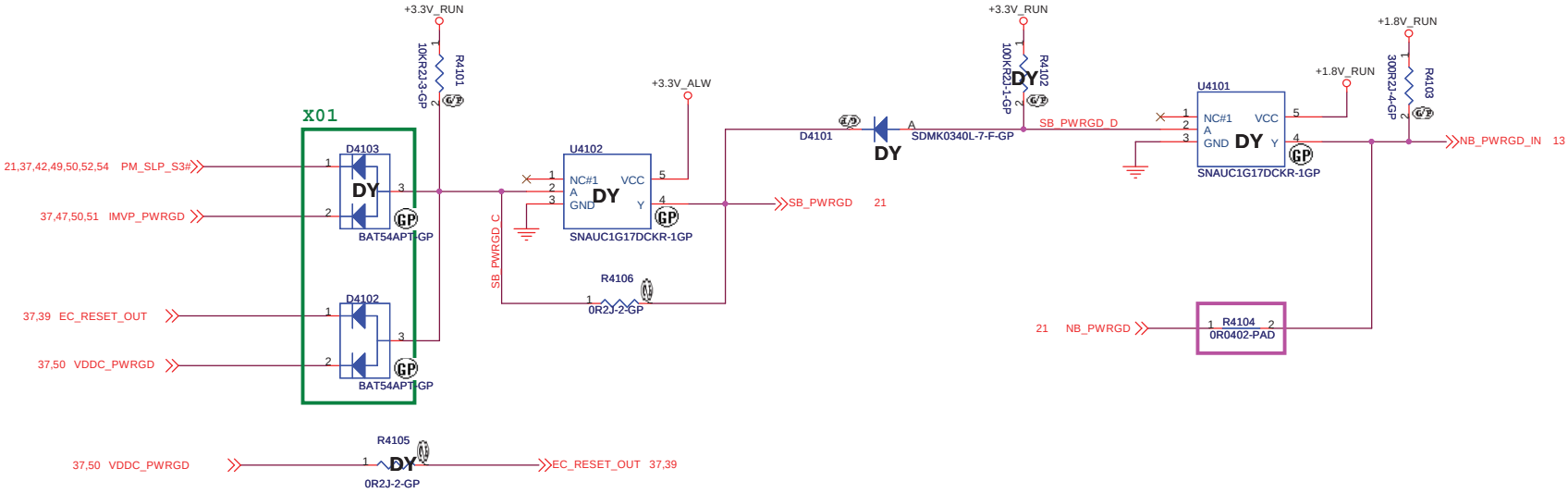
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: Ansenal DJ1 AMD UMA | Rev: A00

Date: Thursday, May 13, 2010 | Sheet 40 of 90

SSID = Reset.Suspend



<Core Design>

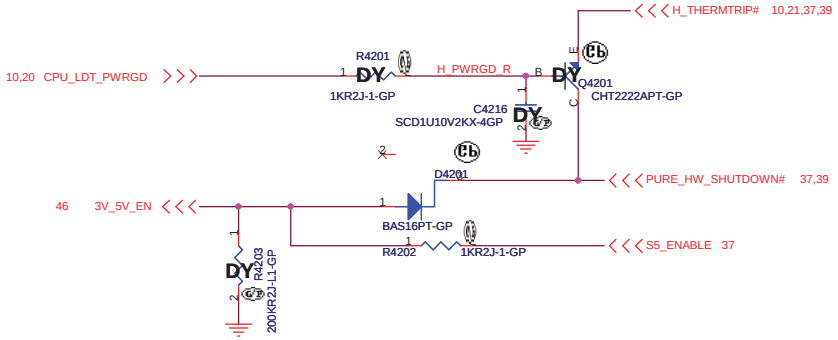
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power On Logic

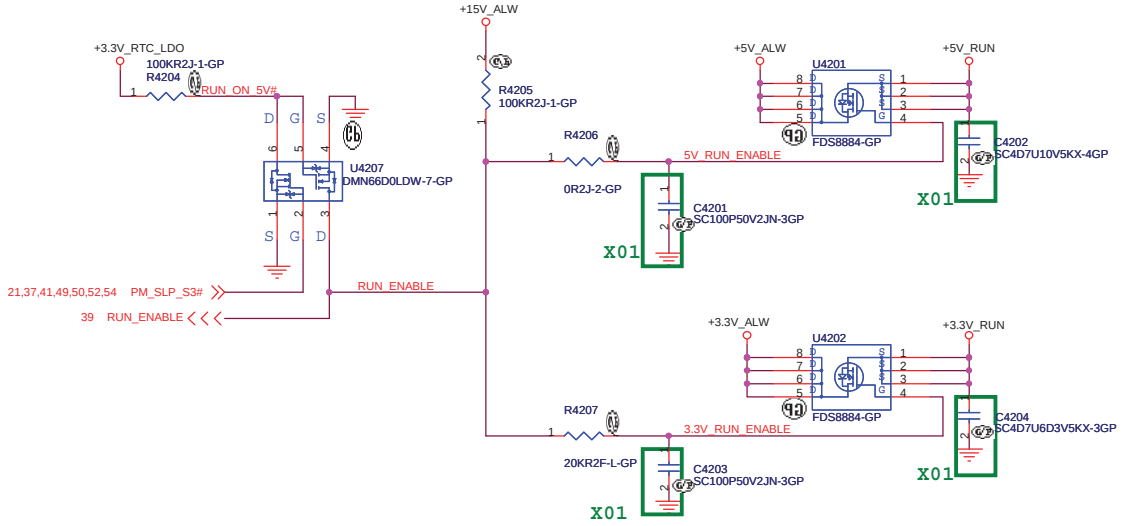
Size	Document Number	Rev
A3	Ansenal DJ1 AMD UMA	A00

Date: Thursday, May 27, 2010 Sheet 41 of 90

SSID = Reset.Suspend

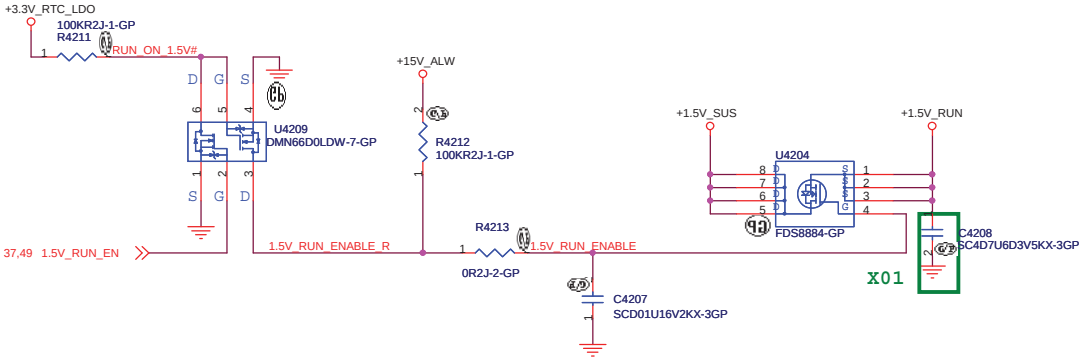


Run Power

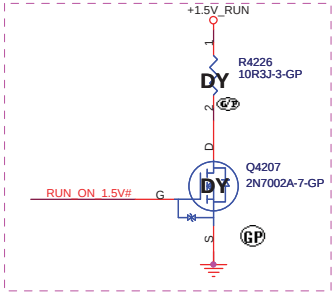


Peak current: 6257.3mA (HD:1100 ODD:2500)
Design current: 4380.11 mA
11.6A
Rds=14m ohm

Peak current: 5966mA
Design current: 4177 mA
11.6A
Rds=14m ohm



Peak current: 1230mA
Design current: 861 mA
11.6A
Rds=14m ohm



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable
Size: Custom | Document Number: Ansenal DJ1 AMD UMA | Rev: A00
Date: Friday, May 28, 2010 | Sheet 42 of 90

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Ansenal DJ1 AMD UMA* | Rev: *A00*

Date: Thursday, May 13, 2010 | Sheet 43 of 90

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: Ansenal DJ1 AMD UMA | Rev: A00

Date: Thursday, May 13, 2010 | Sheet 44 of 90

(Blanking)

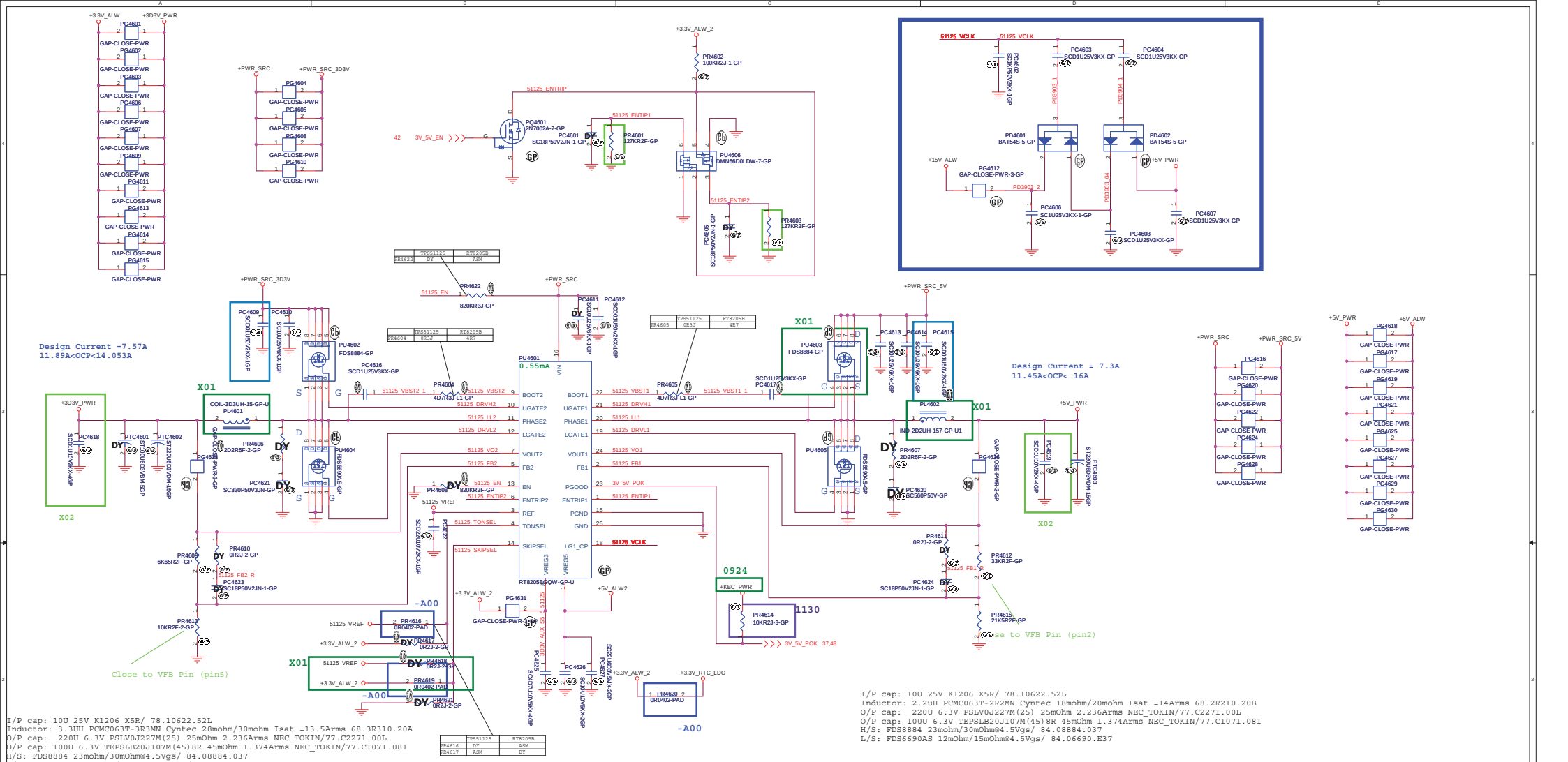
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Ansenal DJ1 AMD UMA* | Rev: *A00*

Date: Thursday, May 13, 2010 | Sheet 45 of 90



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 3.3UH PCMC063T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V TEPSLB20J107M(45)8R 45mOhm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: FDS8884 23mohm/30mOhm@4.5Vgs/ 84.08884.037
L/S: FDS6690AS 12mOhm/15mOhm@4.5Vgs/ 84.06690.E37

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 2.2uH PCMC063T-2R2MN Cyntec 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V TEPSLB20J107M(45)8R 45mOhm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: FDS8884 23mohm/30mOhm@4.5Vgs/ 84.08884.037
L/S: FDS6690AS 12mOhm/15mOhm@4.5Vgs/ 84.06690.E37

RT8205B(74.08208.A73):

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

RT8205B(74.08205.B73):

TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3	365kHz	460kHz
VREG5	365kHz	460kHz

TPS51125	74.51125.073
RT8205BGQW	74.08205.B73

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8205B_5V/3D3V

Size	Document Number	Rev
A2	Ansenal DJ1 AMD UMA	A00

Date: Thursday, May 27, 2010 Sheet 46 of 90

SSID = CPU.Regulator

ISL6265HRTZ-T for +VCC_CORE&+VDDNB

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor:4.7uH PCMC063T-4R7MN 35mohm Isat =10Arms CYNTEC/68.4R710.20D
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3.0Arms Panasonic/79.33719.L01
H/S:VISHAY SIS412DN-T1-GE3/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S:VISHAY SIS412DN-T1-GE3/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037

+VDDNB
Design Current: 2.8A
Peak current: 4A
4.4A<OCP<5.6A

+VCC_CORE
Design Current: 36A
39.6A<OCP<54A

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.36UH PCMC104T-R36MN1R05J CYNTEC DCR 1.05(+5%~-5%)mohm
Isat =60Arms 68.R3610.20C
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3.0Arms Panasonic/79.33719.L01
H/S: SiS406DN/ POWERPAK-8/ 11.5mOhm/14.5mOhm @4.5Vgs/ 84.00406.037
L/S: SiS402DN/ POWERPAK-8/ 6.4mOhm/8mohm@4.5Vgs/ 84.00402.037

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

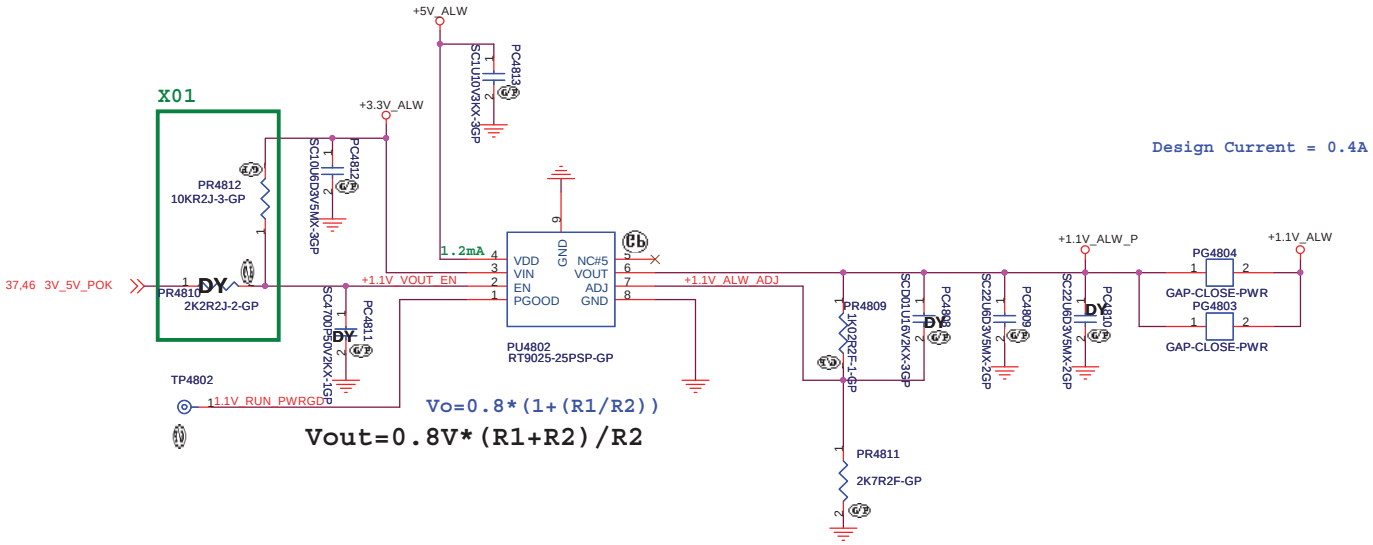
Title: VREG : +VCC_CORE&+VDDNB

Size: A2 | Document Number: Ansenal DJ1 AMD UMA | Rev: A00

Date: Thursday, May 27, 2010 | Sheet 47 of 90

SSID = PWR.Plane.Regulator_+1.1V_RUN

RT9025 for +1.1V_ALW

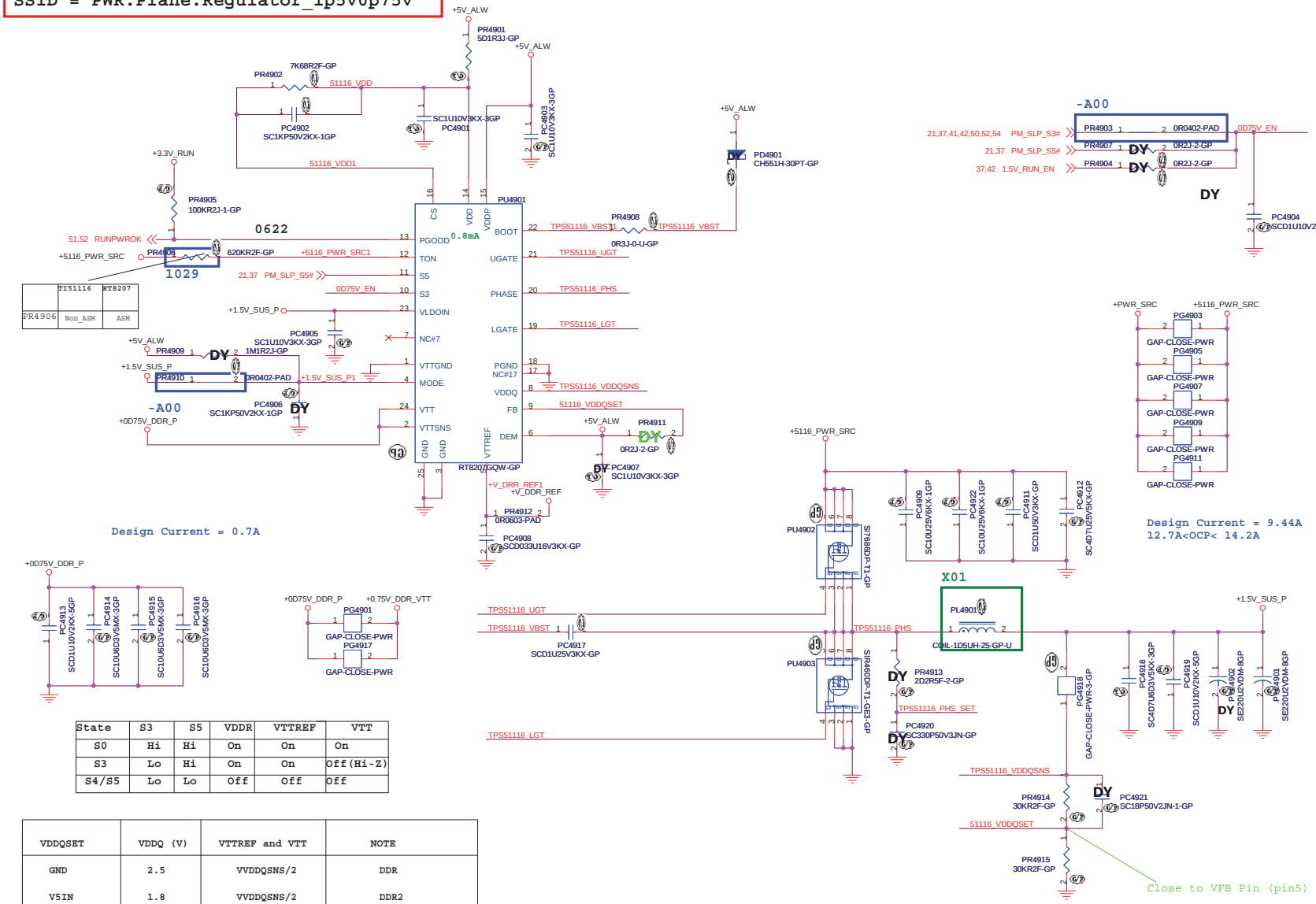


<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	RT9025_+1.1VALW	
Size A3	Document Number: Ansenal DJ1 AMD UMA	Rev A00
Date: Thursday, May 27, 2010	Sheet 48 of 90	

SSID = PWR.Plane.Regulator_1p5v0p75v



Design Current = 0.7A

Design Current = 9.44A
12.7A<OCP< 14.2A

PR4906	RT5116	RT8207
	Non_ASM	ASM

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UHPCMC104T-1R5MN DCR:3.8/4.2mohm Isat =33Arms Cyntec/ 68.1R510.10J
O/P cap: 220U 2V EEFCX0D221R 15mOhm 2.7Arms PANASONIC/ 79.22719.20L
H/S: FDS8880 9.6mohm/12mOhm@4.5Vgs/ 84.08880.037
L/S: FDS6676AS 5.9mOhm/7.25mOhm@4.5Vgs/ 84.06676.A37

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8207GQW_+1.5V_SUS

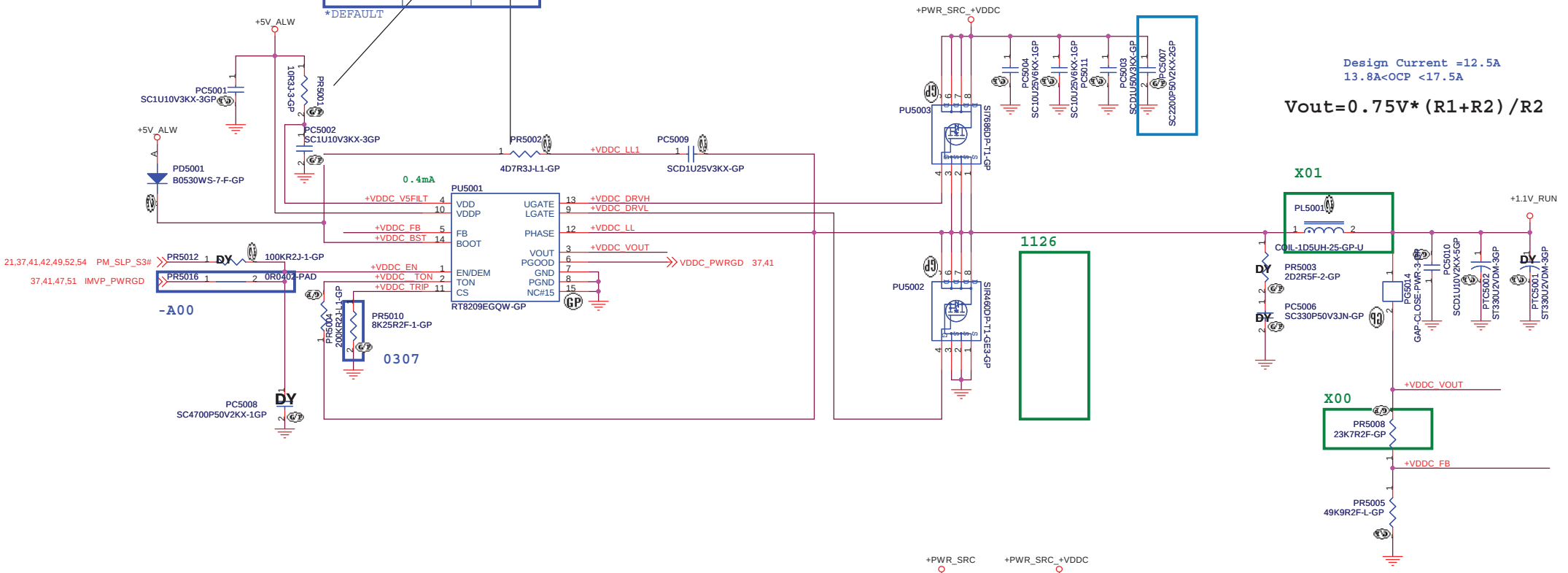
Size	Document Number	Rev
Custom	Ansenal DJ1 AMD UMA	X02

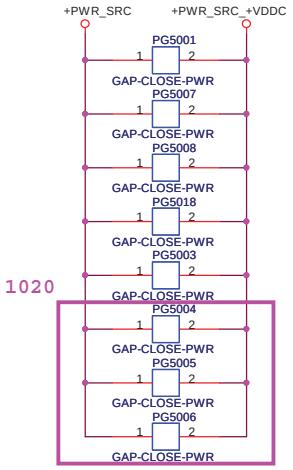
Date: Thursday, May 27, 2010 Sheet 49 of 90

SSID = PWR.Plane.Regulator_VDDC

PWM TYPE	PR5001	PR5002
*RT8209E	10 ohm	4.7 ohm
TPS51117	300 ohm	0 ohm

*DEFAULT





I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UHPCMC104T-1R5MN DCR:3.8/4.2mohm Isat =33Arms Cyntec/ 68.1R510.10
O/P cap: 330U 2.5V PSLV0E337M(15) 15mOhm 2.886Arms NEC_TOKIN/ 77.C3371.10L
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

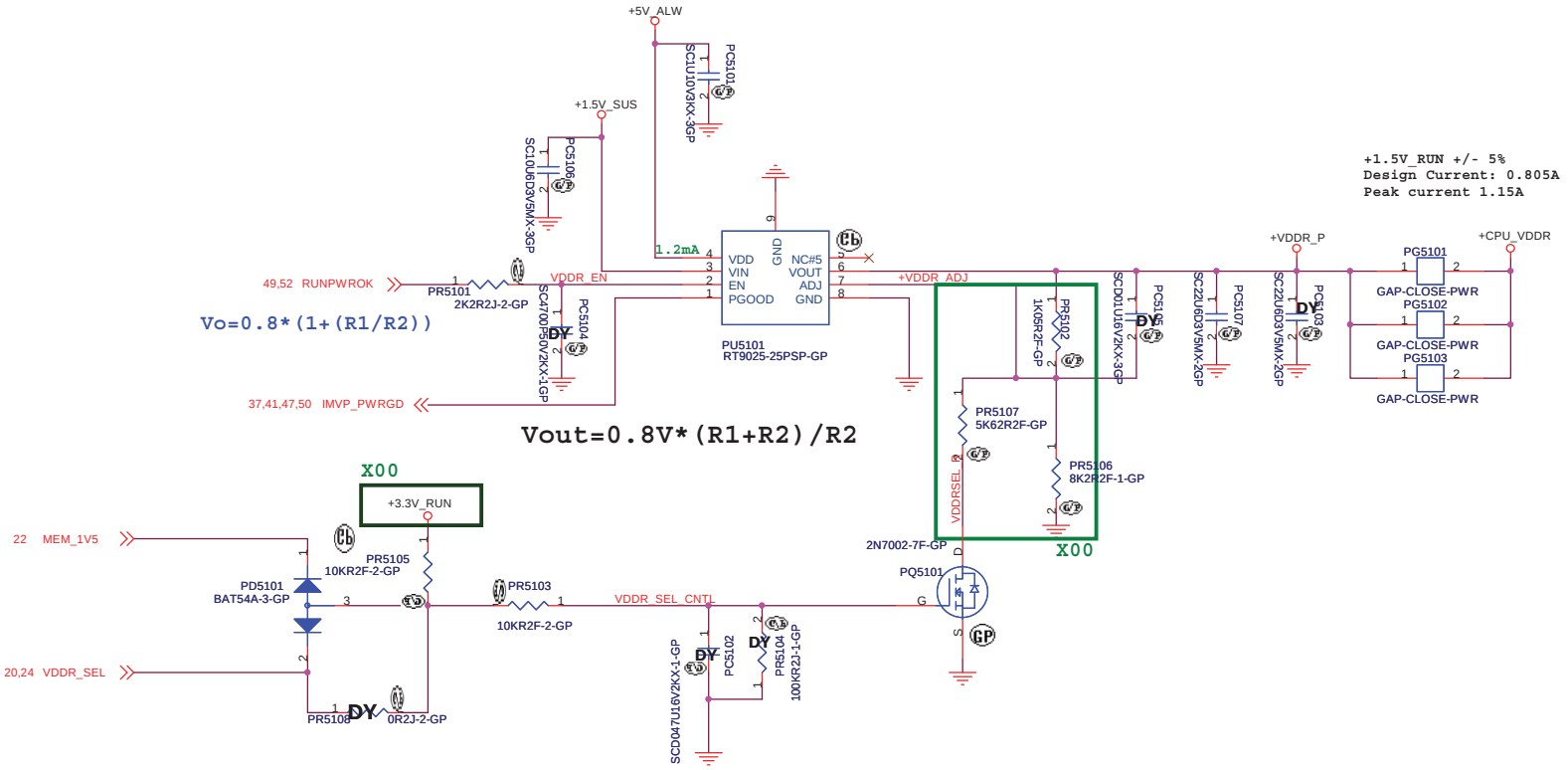
Title: RT8209 +1.1V RUN

Size: A3 | Document Number: Ansenal DJ1 AMD UMA | Rev: A00

Date: Thursday, May 27, 2010 | Sheet 50 of 90

SSID = PWR.Plane.Regulator_VDDR

RT9025 for +VDDR



VDDR_SEL	+CPU_VDDR
H	1.05V
L	0.9V

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT9025 +VDDR

Size: A3 | Document Number: Ansenal DJ1 AMD UMA | Rev: A00

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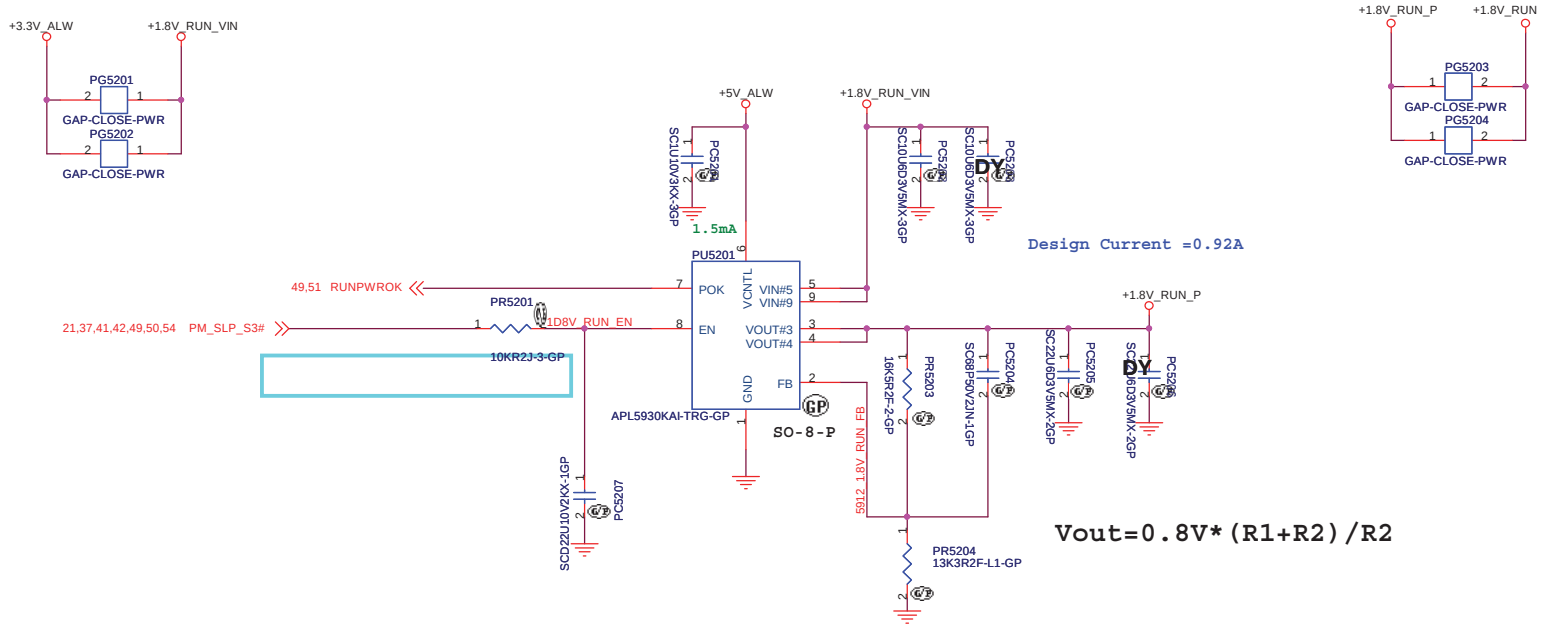
SSID = PWR.Plane.Regulator_1p8v

APL5930 for +1.8V_RUN



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: APL5930 +1.8V RUN

Size: A3 | Document Number: Ansenal DJ1 AMD UMA | Rev: A00

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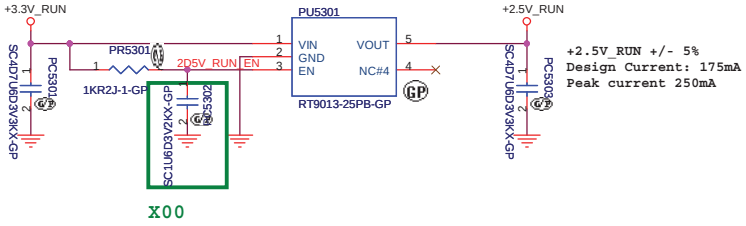
SSID = PWR.Plane.Regulator_2p5v

RT9013-25PB for +2.5V_RUN



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

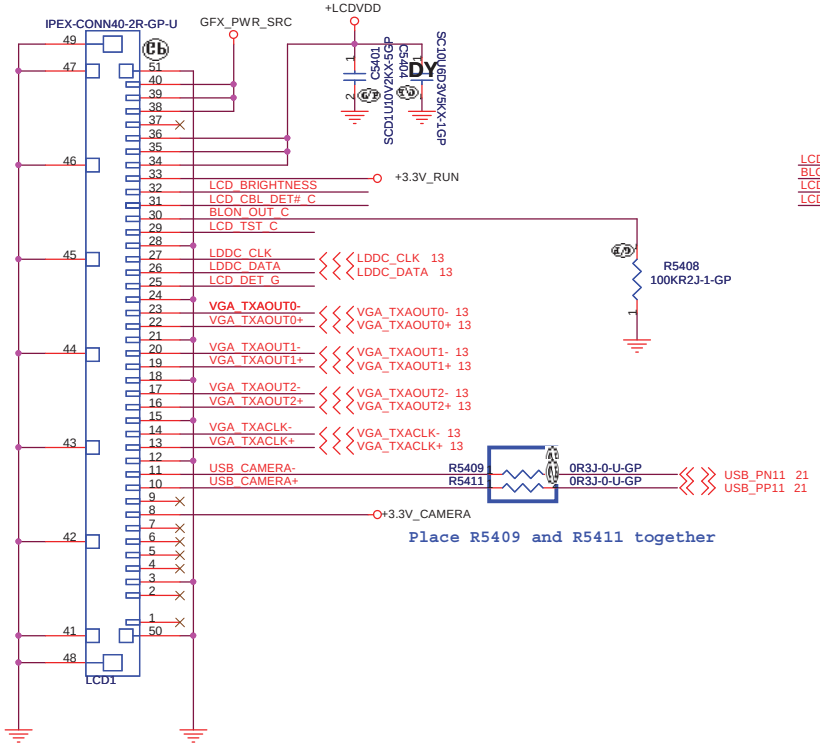
Title: VREG : +CPU_VDDR&+2.5V_RUN

Size: Custom | Document Number: Ansenal DJ1 AMD UMA | Rev: A00

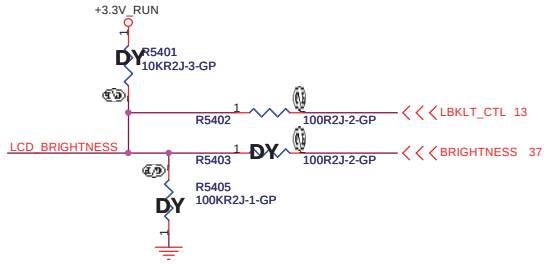
Date: Thursday, May 13, 2010 | Sheet 53 of 90

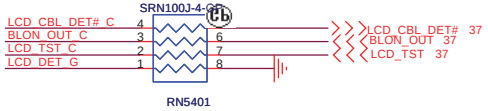
SSID = VIDEO

LVDS CONNECTOR

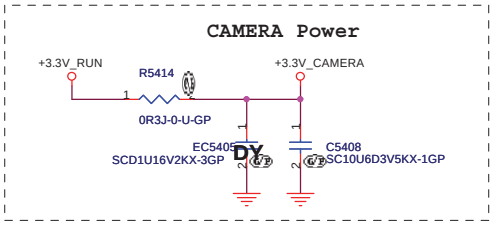


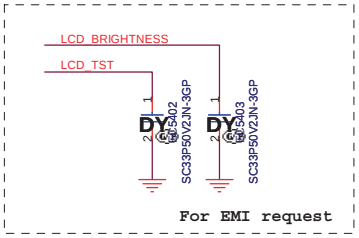
Place R5409 and R5411 together





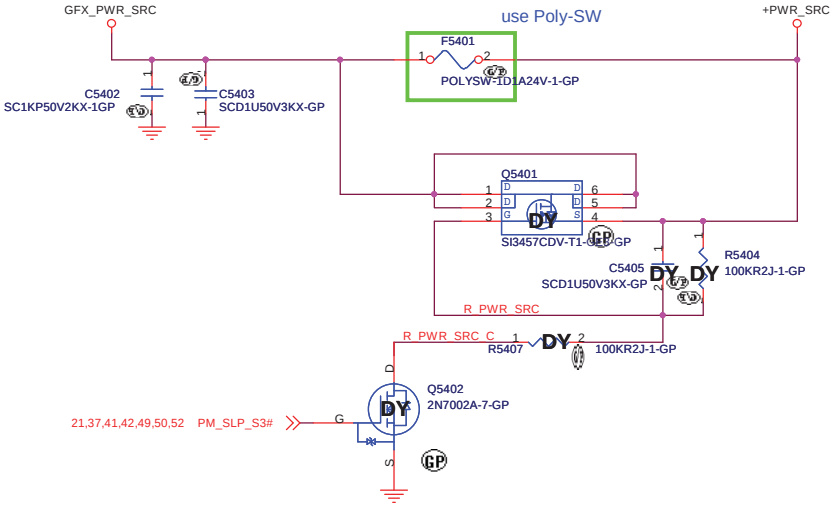
20.F1093.040
20.F1289.040





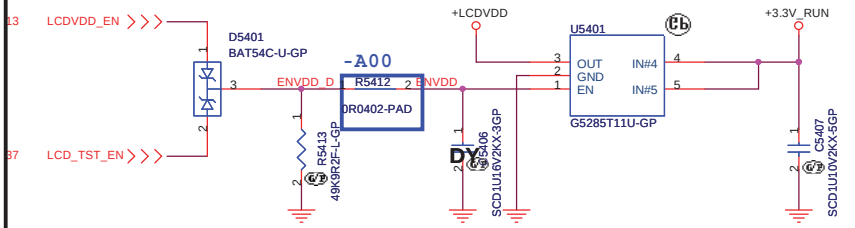
SSID = Inverter

INVERTER POWER



SSID = VIDEO

LCD POWER



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD/Inverter Connector

Size	Document Number	Rev
A3	Ansenal DJ1 AMD UMA	A00

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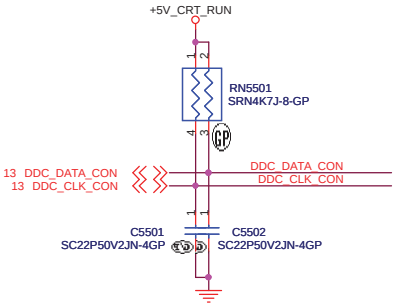
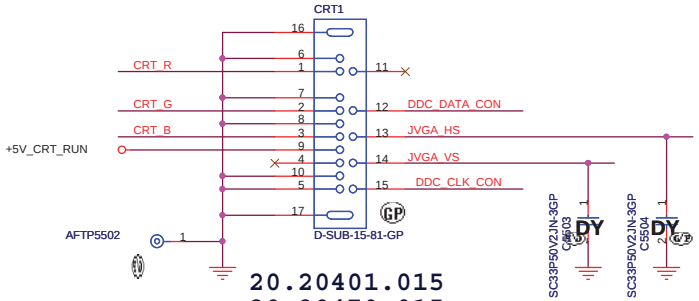
SSID = VIDEO

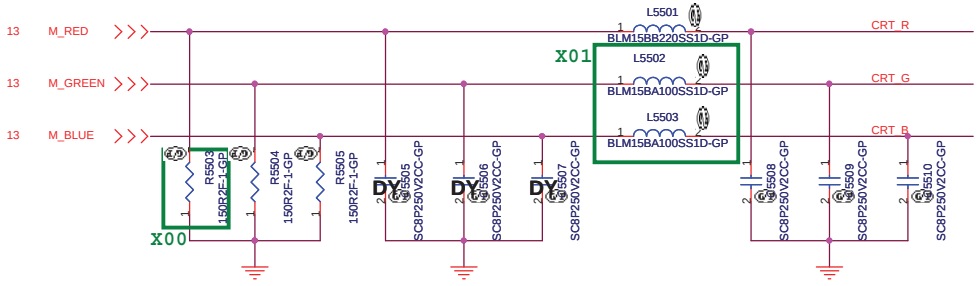
Layout Note:

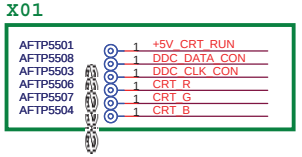
*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
* RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.

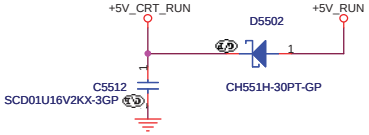


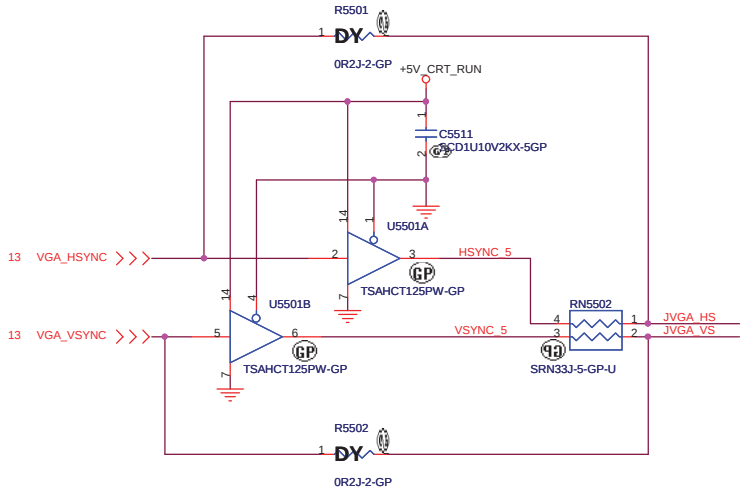


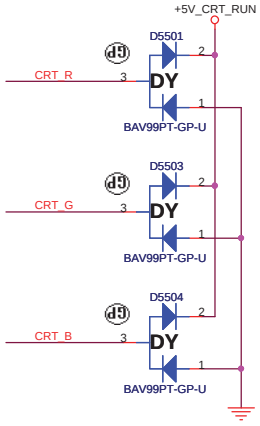
20.20401.015
20.20479.015

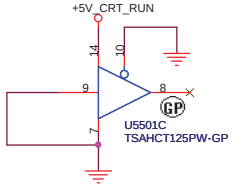


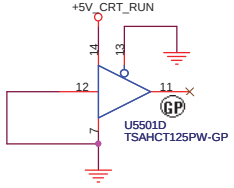












<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT Connector

Size | Document Number: Ansenal DJ1 AMD UMA | Rev: A00

Date: Thursday, May 27, 2010 | Sheet 55 of 90

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: Ansenal DJ1 AMD UMA | Rev: A00

Date: Thursday, May 13, 2010 | Sheet 56 of 90

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

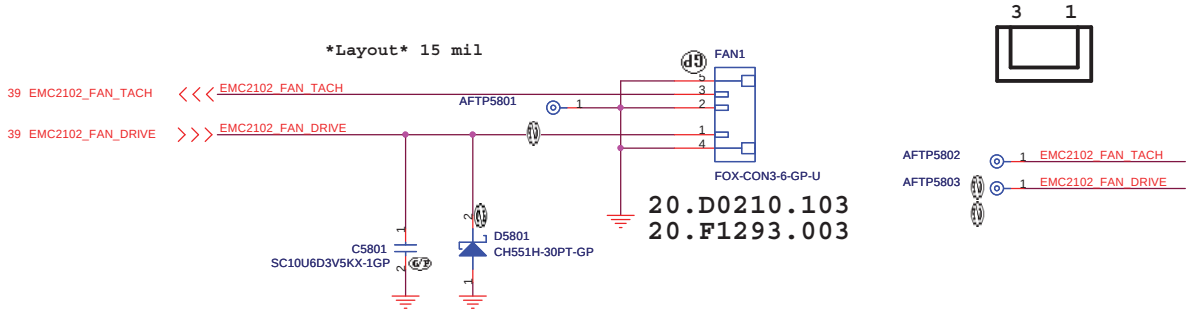
Title: HDMI (Reserved)

Size: A3 | Document Number: Ansenal DJ1 AMD UMA | Rev: A00

Date: Thursday, May 13, 2010 | Sheet 57 of 90

SSID = Thermal

Fan Connector



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ITP/Fan Connector

Size: A3 | Document Number: Ansenal DJ1 AMD UMA | Rev: A00

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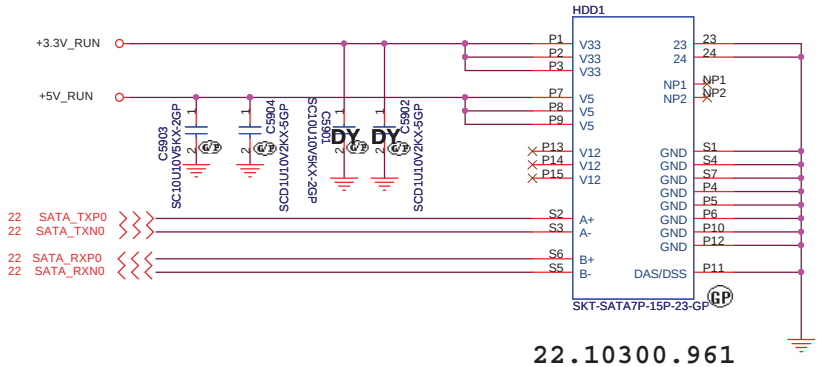
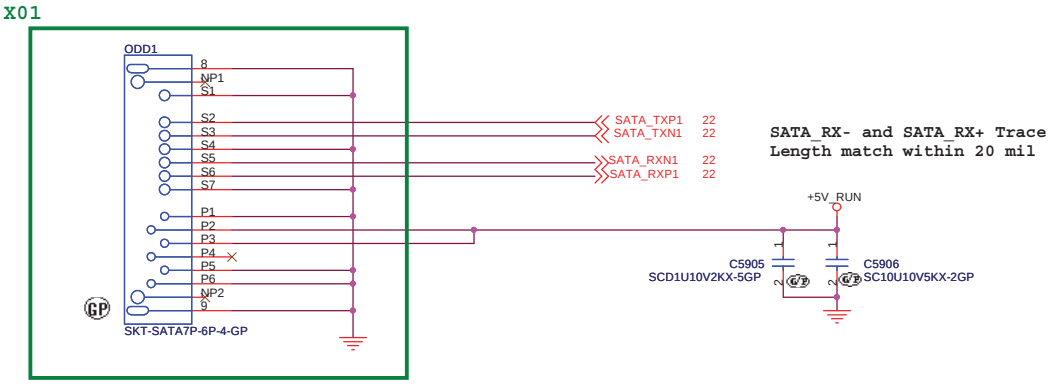
SSID = SATA

SATA HDD Connector



22.10300.961

ODD Connector



22.10300.811
22.10300.421
22.10300.471

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

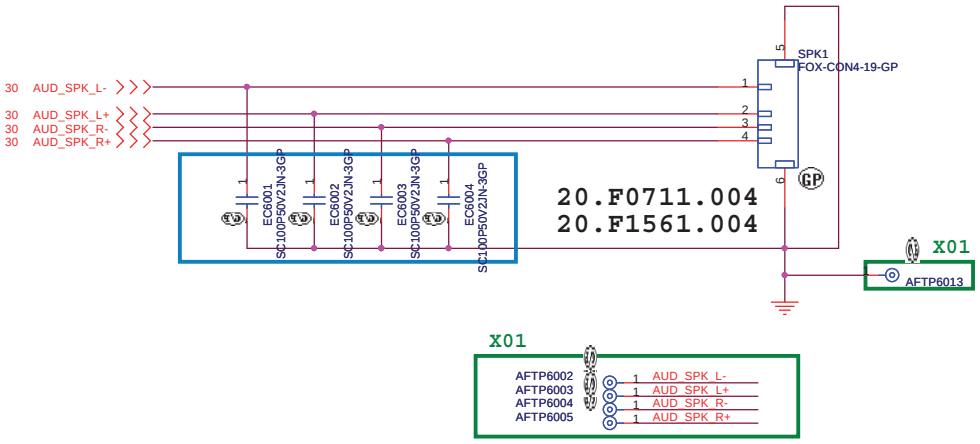
Title: HDD/ODD

Size	Document Number	Rev
A3	Ansenal DJ1 AMD UMA	A00

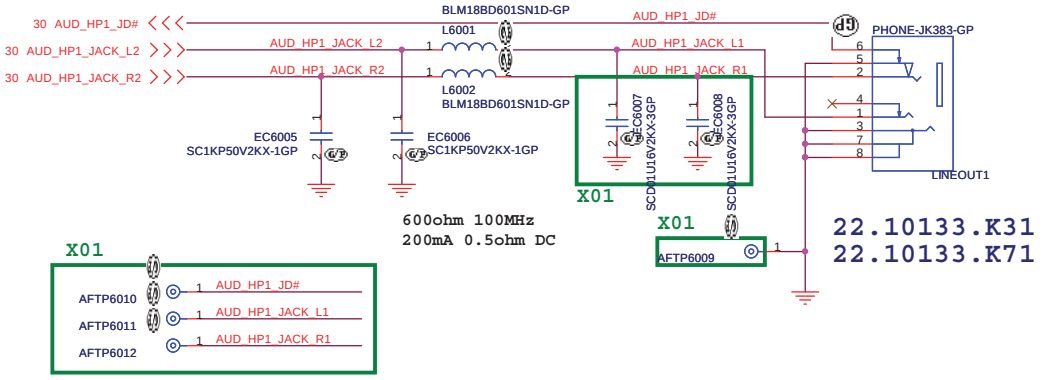
Date: Thursday, May 27, 2010 Sheet 59 of 90

SSID = AUDIO

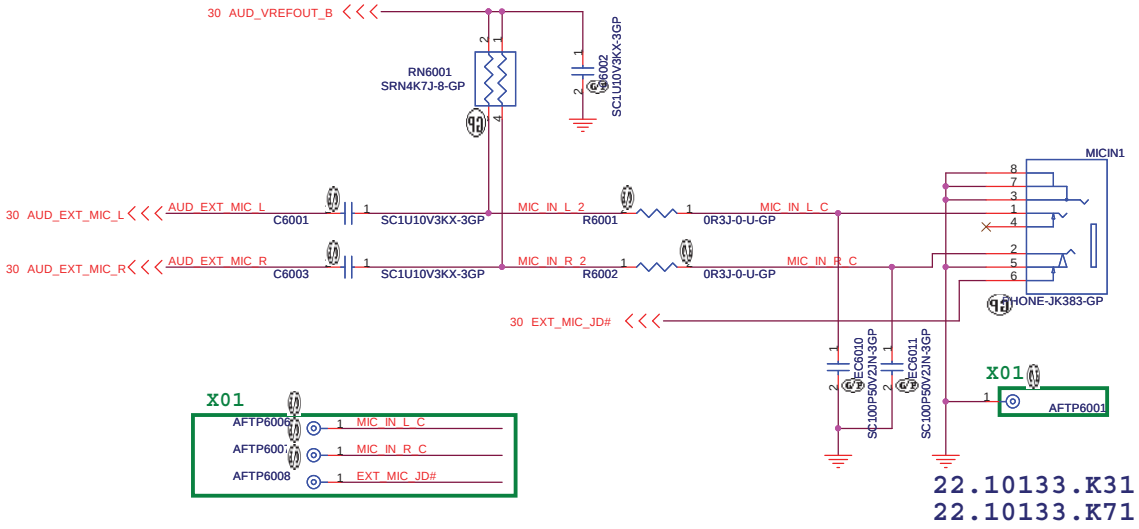
Speaker Connector



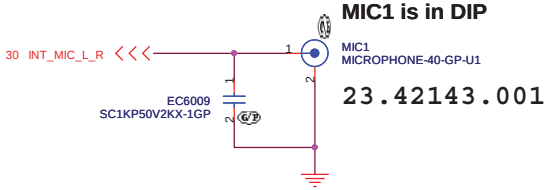
LINE1 OUT



MIC IN



Internal Microphone



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Jack

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: Ansenal DJ1 AMD UMA | Rev: A00

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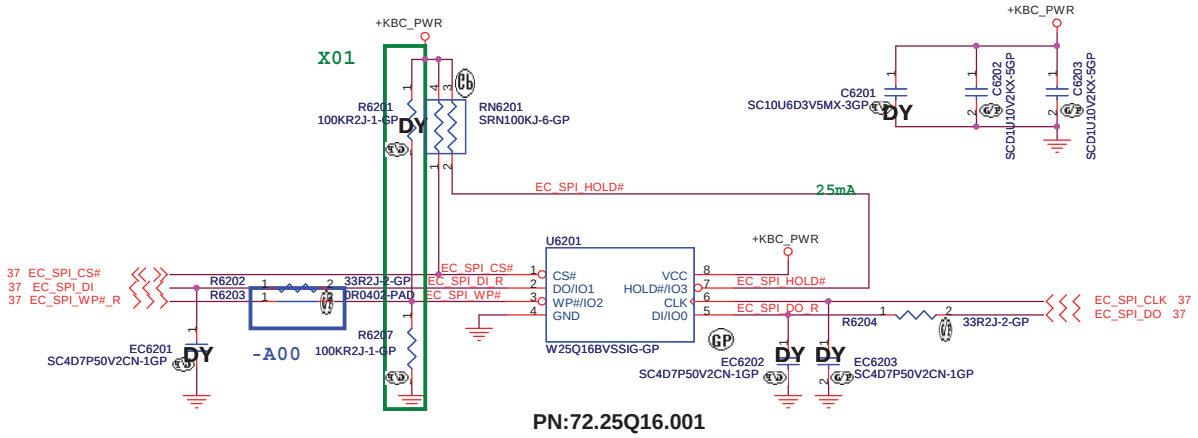
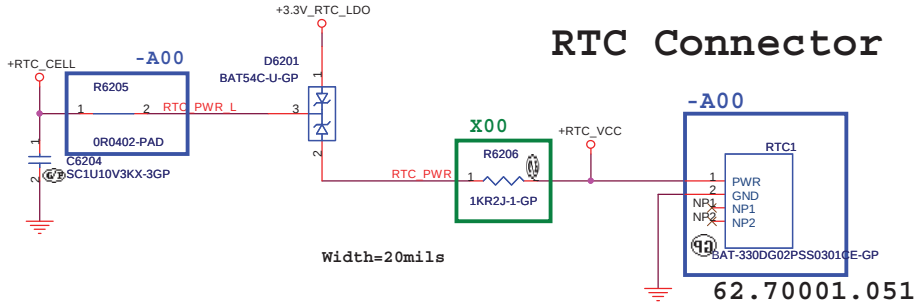
SSID = Flash.ROM

SPI FLASH ROM (16M bits) for KBC



PN:72.25Q16.001

SSID = RBATT



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash/RTC

Size: A3 | Document Number: Ansenal DJ1 AMD UMA | Rev: A00

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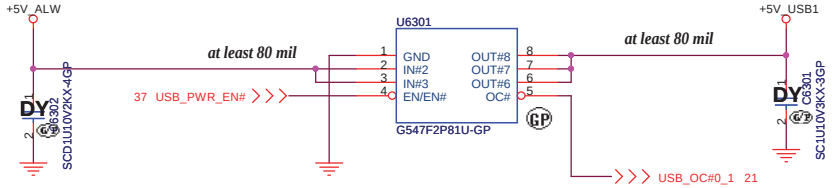
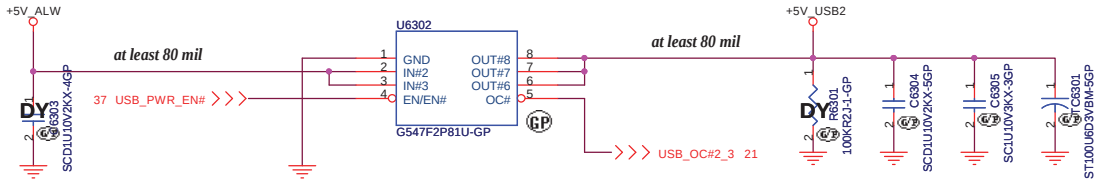
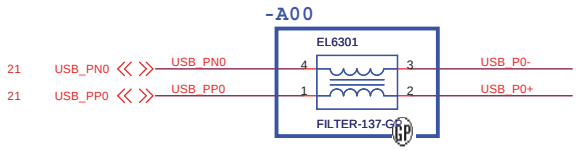
SSID = USB

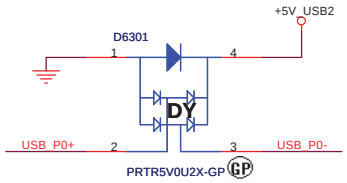
IO Board USB Power

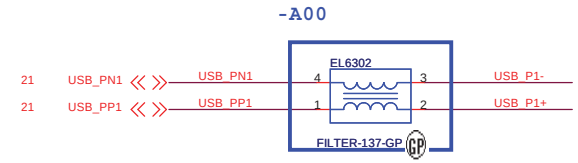


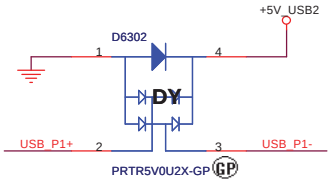
Right USB Power

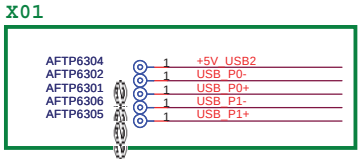


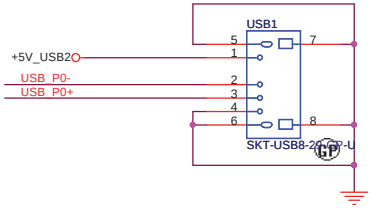




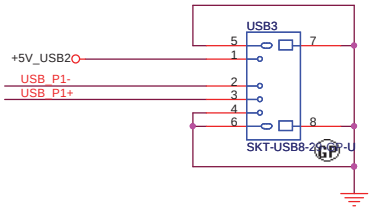








22.10254.451
22.10321.A21



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: USB

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<Core Design>

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Title: MINICARD

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<Core Design>

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Title: Reserved

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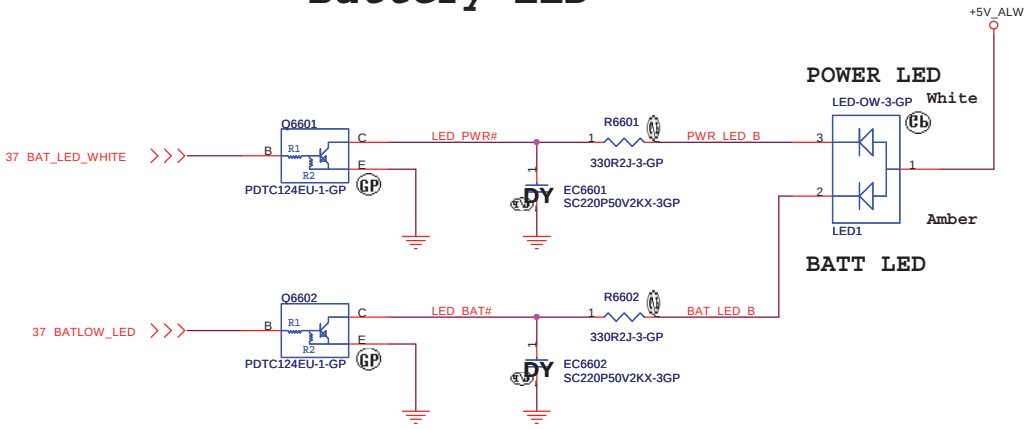
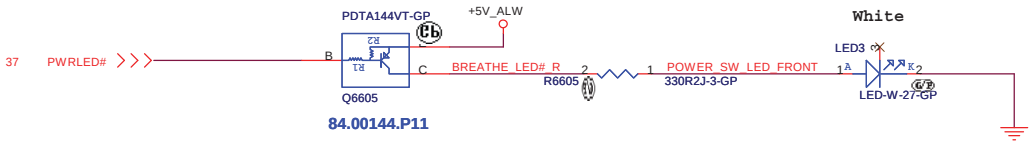
SSID = User.Interface

Battery LED



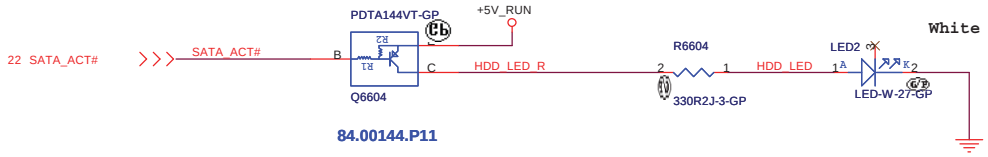
83.00326.G70
83.01222.K70

BREATHE PWR LED (Front)



84.00144.P11

HDD LED



84.00144.P11

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED

Size: A3 | Document Number: Ansenal DJ1 AMD UMA | Rev: A00

Date: Thursday, May 27, 2010 | Sheet 66 of 90

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

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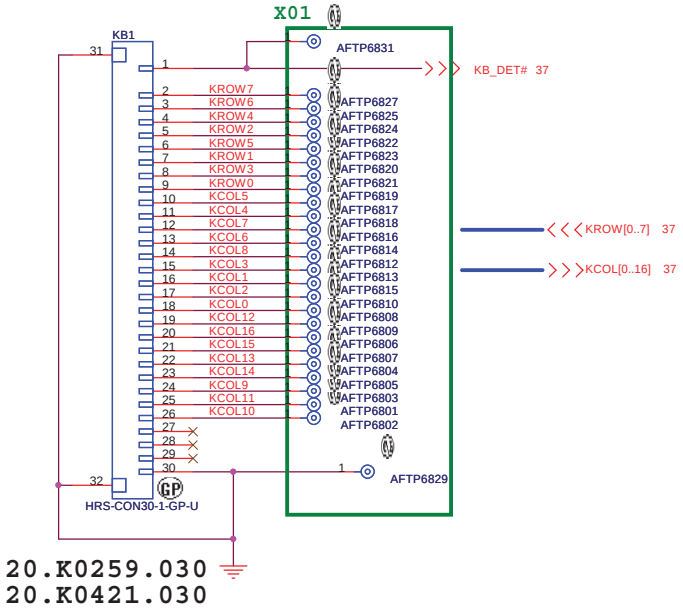
SSID = KBC

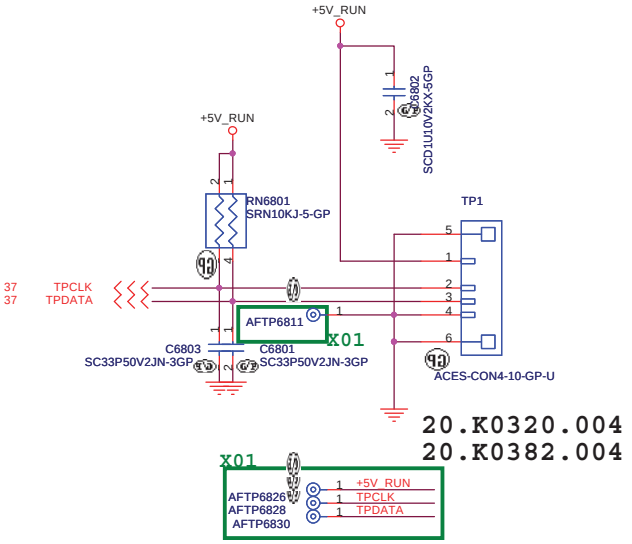
Internal KeyBoard Connector



20.K0259.030
20.K0421.030

SSID = Touch.Pad

TouchPad Connector



20.K0320.004
20.K0382.004

<Core Design>

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Title: Key Board/Touch Pad

Size: A3 | Document Number: Ansenal DJ1 AMD UMA | Rev: A00

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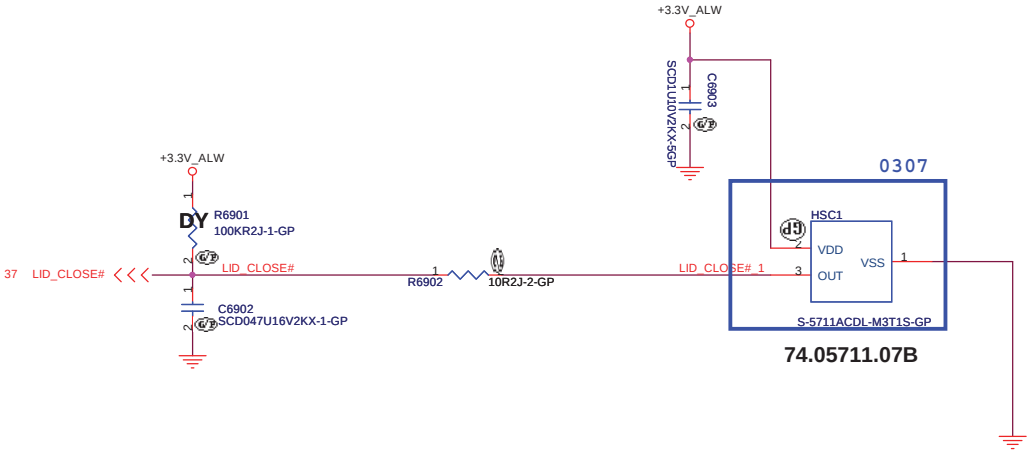

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: Hall Sensor

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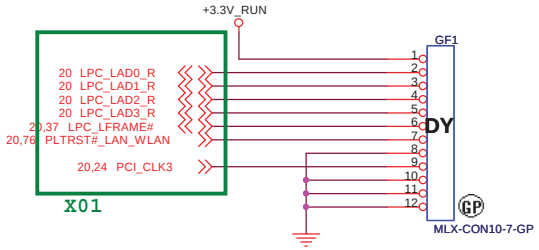

<Core Design>

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Title: Reserved

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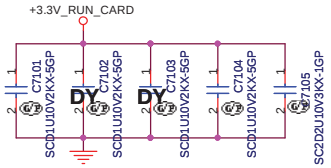
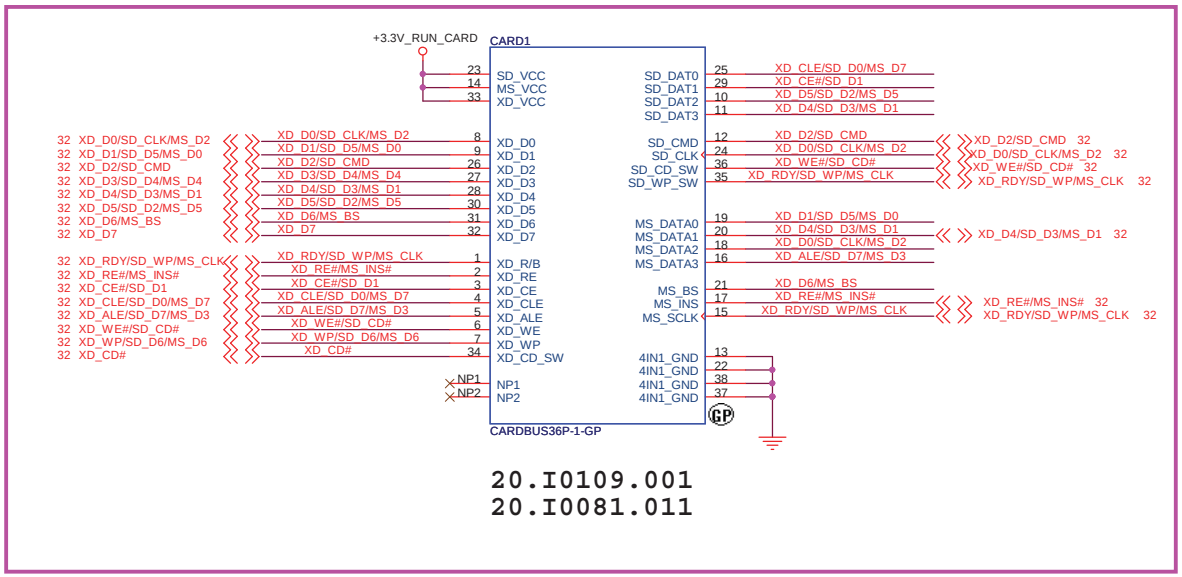
SSID = SDIO

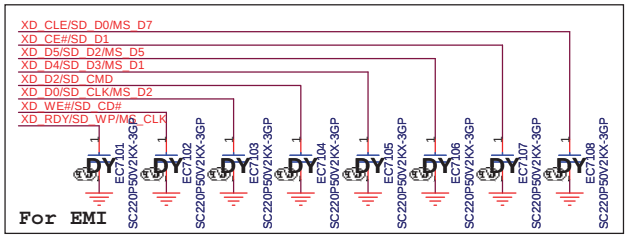
SD/XD/MS Card Reader



0826



20.I0109.001
20.I0081.011



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: CARD Reader CONN

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<Core Design>

Wistron Corporation
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Title
RESERVED

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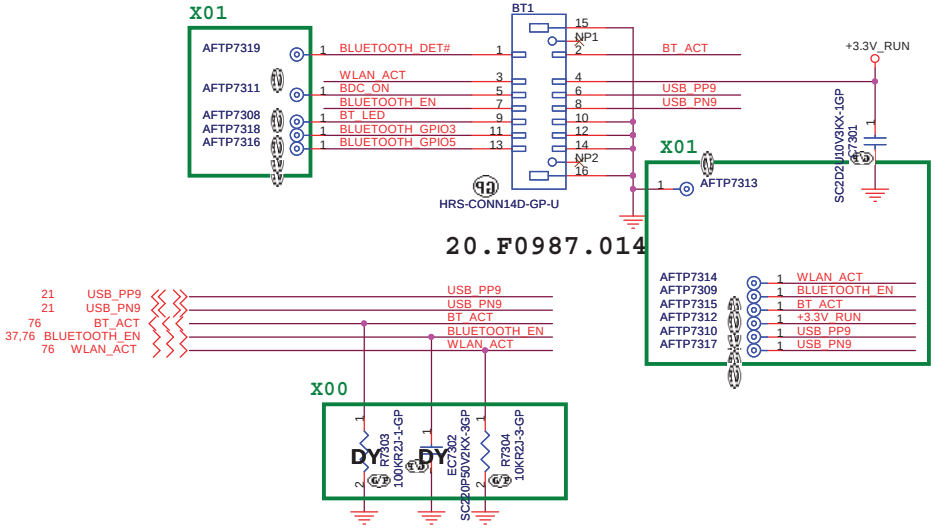
SSID = User.Interface

Bluetooth Module conn.



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Bluetooth

Size	Document Number	Rev
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<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

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<Core Design>

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Title: Reserved

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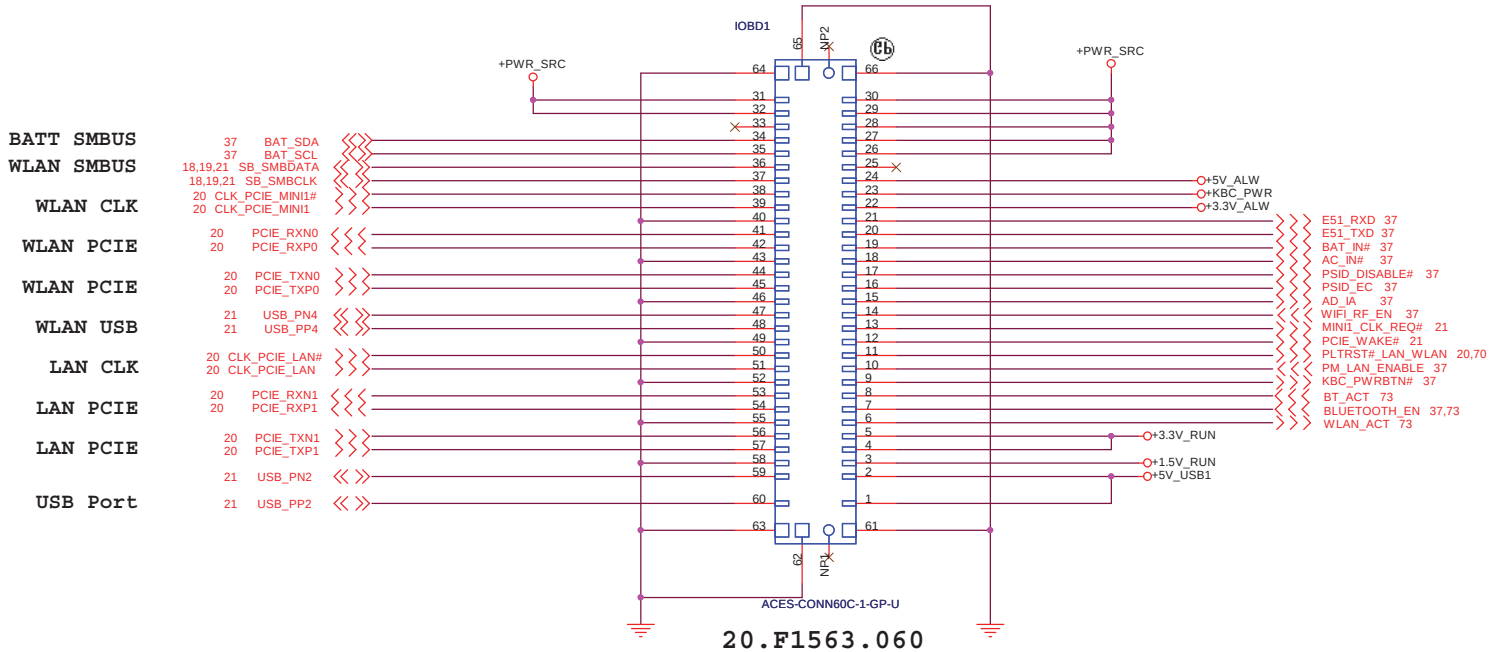
SSID = PWR.Support



20.F1563.060

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: IO Board Connector

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<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: Reserved

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<Core Design>

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Title: Reserved

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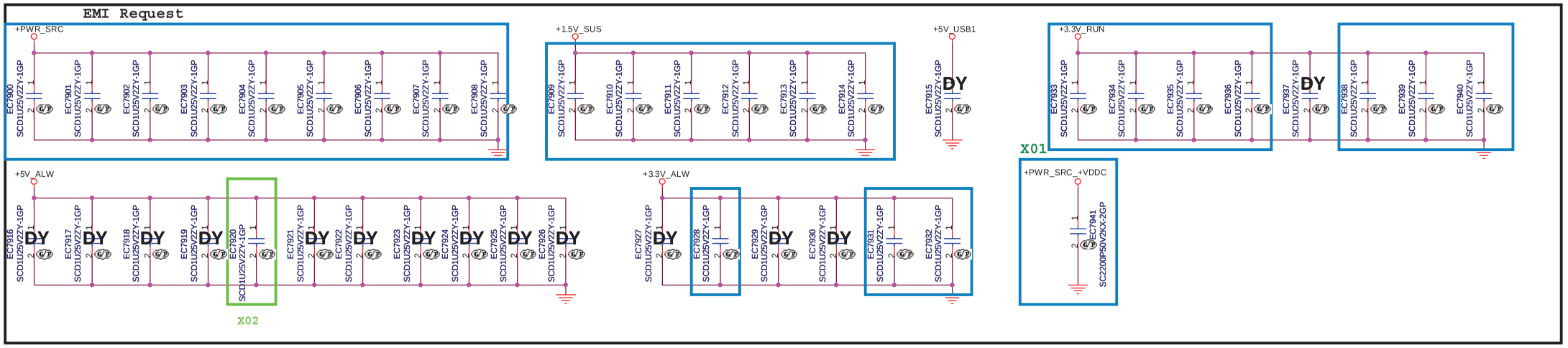
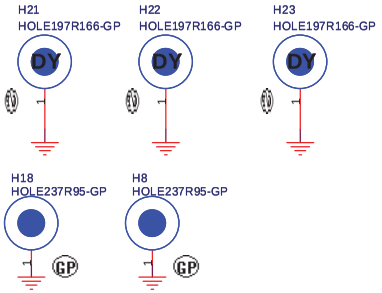
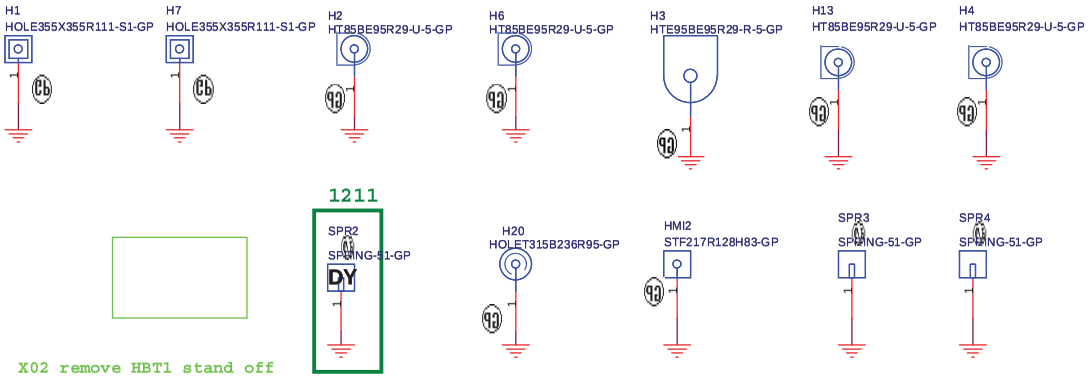
SSID = Mechanical







X02 remove HBT1 stand off
3/25

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS/EMI Capacitors

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A3	Ansenal DJ1 AMD UMA	A00

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA PCIE(1/4)

Size: A3 | Document Number: Ansenal DJ1 AMD UMA | Rev: A00

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA LVDS/TV/CRT(2/4)

Size: A3 | Document Number: Ansenal DJ1 AMD UMA | Rev: A00

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA POWER/GND(3/4)

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA MEMORY/STRAPS(4/4)

Size: A3 | Document Number: Ansenal DJ1 AMD UMA | Rev: A00

Date: Thursday, May 13, 2010 | Sheet 83 of 90

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM (1/2)

Size: A3 | Document Number: Ansenal DJ1 AMD UMA | Rev: A00

Date: Thursday, May 13, 2010 | Sheet 84 of 90

(Blanking)

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU-VRAM (2/2)

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
TPS51117_+VCC_GFXCORE

Size	Document Number	Rev
A3	*Ansenal DJ1 AMD UMA*	*A00*

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: APL5930_+1.1V_RUN

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: Ansenal DJ1 AMD UMA | Rev: A00

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Change notes - Page 1

DATE	VERSON	ITEM	PAGE	Modify List	Issue Description	OWNER
		1	10	change RN1006 pull-up power plane from +1.5V_RUN to +1.5V_SUS	avoid leakage in S3	EE
		2	20	RN2002 replace to 22R	NB_REFCLK votlage level too high	EE
		3	20	R2009 move to PCI_CLK3, change DF1 clk from PCLK_FWH to PCI_CLK3	PCLK_FWH in internal CLKGEN only support 14MHz DF1 clk need 33MHz	EE
		4	37	pop R3729 & depop R3733	MB version ID	EE
		5	37	reserve U3703, pop R6207 and depop R6201	avioding SPI ROM data loss	EE
		6	46	pop PR4619 & depop PR4618	modify operating mode for+15V_ALW voltage	EE
		7	37,10	add Q1005, pop R1039 and R1040	CPU PROCHOT connect from EC through a level shift allow EC to force CPU enter HTC state when power budge over the limit in DOS mode.	EE
		8	42	C4201, C4203 to 100pF	For power sequence	EE
		9	20	C2011, C2012 to 18pF	vendor measure feedback value	EE
		10	48	Add PR4812 PU +3.3V_ALW	For +1.1V_ALW rising issue	EE
		11	18	Change TC1801 to 330uF, 2V tolerance.	Implement common part for 1.5V power rail.	EE
		12	13 10	remove R1329,R1330 and add RN1302 remove R1323,R1324 and add RN1303 remove RN1007 and change RN1003 to 1K8P	Combine resistor	EE
	X01	13	55 60 63 68 73	arrange CRT conn. AFTP arrange SPKR, MIC, JACK conn. AFTP arrange USB conn. AFTP arrange KB, TP conn. AFTP arrange BT conn. AFTP	Sink with DJ1 CP	EE
		14	20	R2020 to RN2009	For SIV report LPC_LAD bus rising time fail	EE
		15	37	Add C3724, R3757	To set accurate current in EC.	EE
		16	10	Reserve R1041 for CPU_R_LDT_PWRGD	reseve POWOK level for 6265 IC	EE
		17	47	PR4732 and PR4750 to small size	power team request	power
		18	20	Del D2001	solve PLTRST# signal rising time too slow	EE
		19	41	Dummy D4103 and exchange IMVP and VDDC_PWRGD signal	For SB_PWRGD shotdown drop	EE
		20	47	Reserve PC4739, PC4740, PC4741,PC4742	Reserve for FB noise	EE
		21	79	Reserve EC7941	EMI request	EMI
		22	21	Reserve C2105	Reserve for SIO_RCIN# noise	EE
		23	47	PR4727 from 10ohm to 0 ohm	power team request	power
		24	64	DEL R6302,R6303, add EL6301 DEL R6304,R6305, add EL6302	EMI request	

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DATE	VERSON	ITEM	PAGE	Modify List	Issue Description	OWNER
		25	60	EC6007 and EC6008 from 100p to 0.01uF	codec vendor suggestion	EE
		26	37	R3737 from 0R to 33R	for SPI_CLK over and under shoot	EE
		27		PL4701,PL4703,PL4601,PL4602,PL5001,PL4901	Add glue for choke pad	power
		28	55	L5502,L5503 bead to 10ohm	for SIV CRT G, B report fail	EE
		29	42	C4202,C4204, C4208 to 4.7uF	For sequence	EE
	X02	1	50	Change PR5010 from 4.2KR to 8.25KR	Avoid +1.1V_RUN OCP	power
		2	69	Change HSC1 from 74.06781.07B(AKE) to 74.05711.07B(SEKIO)	Avoid AKE and SEKIO footprint not match	EE
		3	20	Exchange Lan & Wlan signal	For lan loop	EE
		4	37	Add one 2N7002 to pull low PSID_EC	For RCID function	EE
		5	37	Change KBC GPI81 from NB_VDDR_EN to KBC_RCID	For RCID function	EE
		6	79	Remove HBT1 stand off	For ME request	ME
		7	37	Change PCB version from X01 to X02	For version change	EE
		8	37	Remove NB_VDD_EN signal	For GPIO change	EE
	A00	1	60	Change RTC1 from 62.70001.011 to 62.70001.051	For CE request	CE
		2	60	Change MICIN1 from 22.10133.K31 to 22.10133.K71	For ME request	ME
		3	37	Add R3729 to pull high PCB_VER0	For MB VERSION ID change	EE
		4	63	Change EL6301 and EL6302 from 68.02012.201 to 69.10087.011	Add second source	EE
		5	49	PR4905 PWR change from +3.3V_ALW to +3.3V_RUN	PWR saving	EE
		6	39	Dummy D3901 paste R3915	For Fan	EE
		7		short PAD R1329 R2304 R3014 R3017 R3020 R3002 R3003 R3004 R1342	PSE request	EE
		8		short PAD R2303 R3732 R3751 R3757 R3906 R6203 R6205	PSE request	EE
		9		short PAD PR4616 PR4619 PR4620 PR4706 PR4709 PR4712 PR4719 PR4729 PR4730 PR4733 PR4734 PR4903 PR4910 PR5016	PSE request	EE
		10		short PAD R1316 R1317 R1323 R1324 R1325 R2305 R2308 R2306 R3744 R3904 R3910 R5412	PSE request	EE

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