

# COMPAL CONFIDENTIAL

MODEL NAME : *NAL60*

PCB NO : *LA-5691P (DAA00001K00)*

BOM P/N : *43178731L01/43178731L02*



笔记本技术联盟

www.bblianmeng.com

## M10 Lafite

**BGA Arrandale (34 x 28 mm) +  
SFF IBEXPEAK-M**

**2009-07-07**

**REV : 0.1(X00)**

**@ : Nopop Component**

MB Type	BOM P/N	CPU	With BLT	Non BLT	TCM		TPM		BOM CONFIG
			1@	2@	W(3@)	W/O(4@)	W(5@)	W/O(6@)	
BLT EN, TPM EN	43178731L01	SV 2.4G	*			*	*		1@, 4@, 5@
BLT EN, TPM EN	43178731L02	SV 2.0G	*		*			*	1@, 3@, 6@
BLT DIS, TCM EN	43178731L03	LV 1.8G		*		*	*		2@, 4@, 5@

MB PCB	
Part Number	Description
DAA00001K00	PCB 0AW LA-5691P REV0 M/B

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		<b>Compal Electronics, Inc.</b>	
		<b>Cover Sheet</b>	
Size	Document Number	Rev	
	<b>LA-5691P</b>	0.1	
Date	Monday, July 13, 2009	Sheet	1 of 51



### POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	ON
S4 (Suspend to DISK) / M1	LOW	LOW	HIGH	LOW	HIGH	ON	ON	OFF	OFF	ON
S5 (SOFT OFF) / M1	LOW	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	ON
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

### PM TABLE

State \ power plane	+15V_ALW +5V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_CORE +1.05V_RUN_VTT +1.05V_RUN	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

PCH	USB PORT#	DESTINATION
	0	USB Port (Ext Right Side)
	1	NA
	2	USB Port (Ext Left Side)
	3	NA
	4	WLAN
	5	WWAN
	6	Bloetooth
	7	USB->BIO
	8	DOCKING
	9	DOCKING
	10	Express Card
	11	Camera
	12	BKT
13	WPAN/NVMHCI	

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	Card Reader
Lane 4	EXPRESS CARD
Lane 5	MINI CARD-3 WPAN/NVMHCI
Lane 6	10/100/1G LAN
Lane 7	None
Lane 8	None

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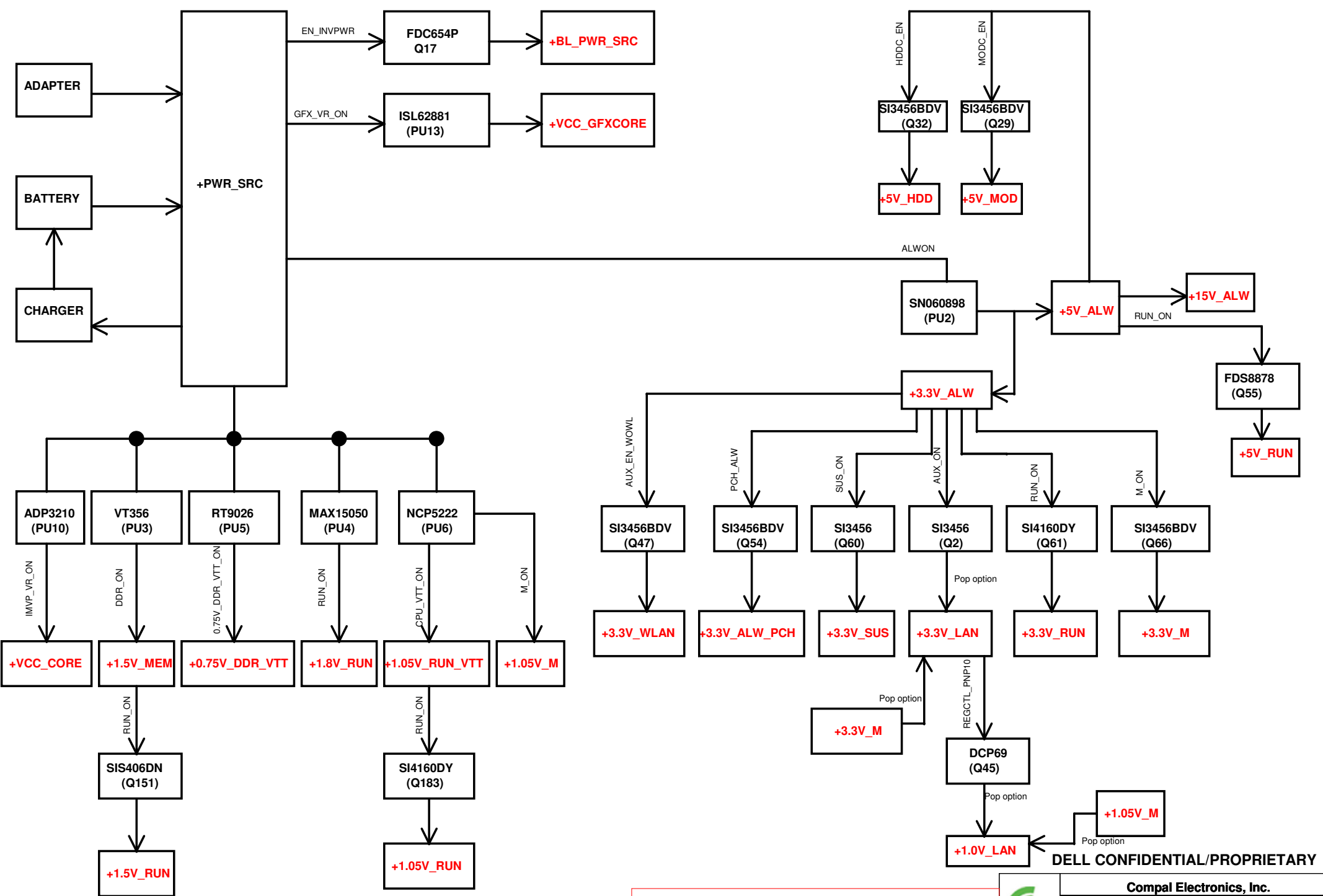
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Index and Config.



Title		
Size	Document Number <b>LA-5691P</b>	Rev 0.1
Date	Monday, July 13, 2009	Sheet 3 of 51

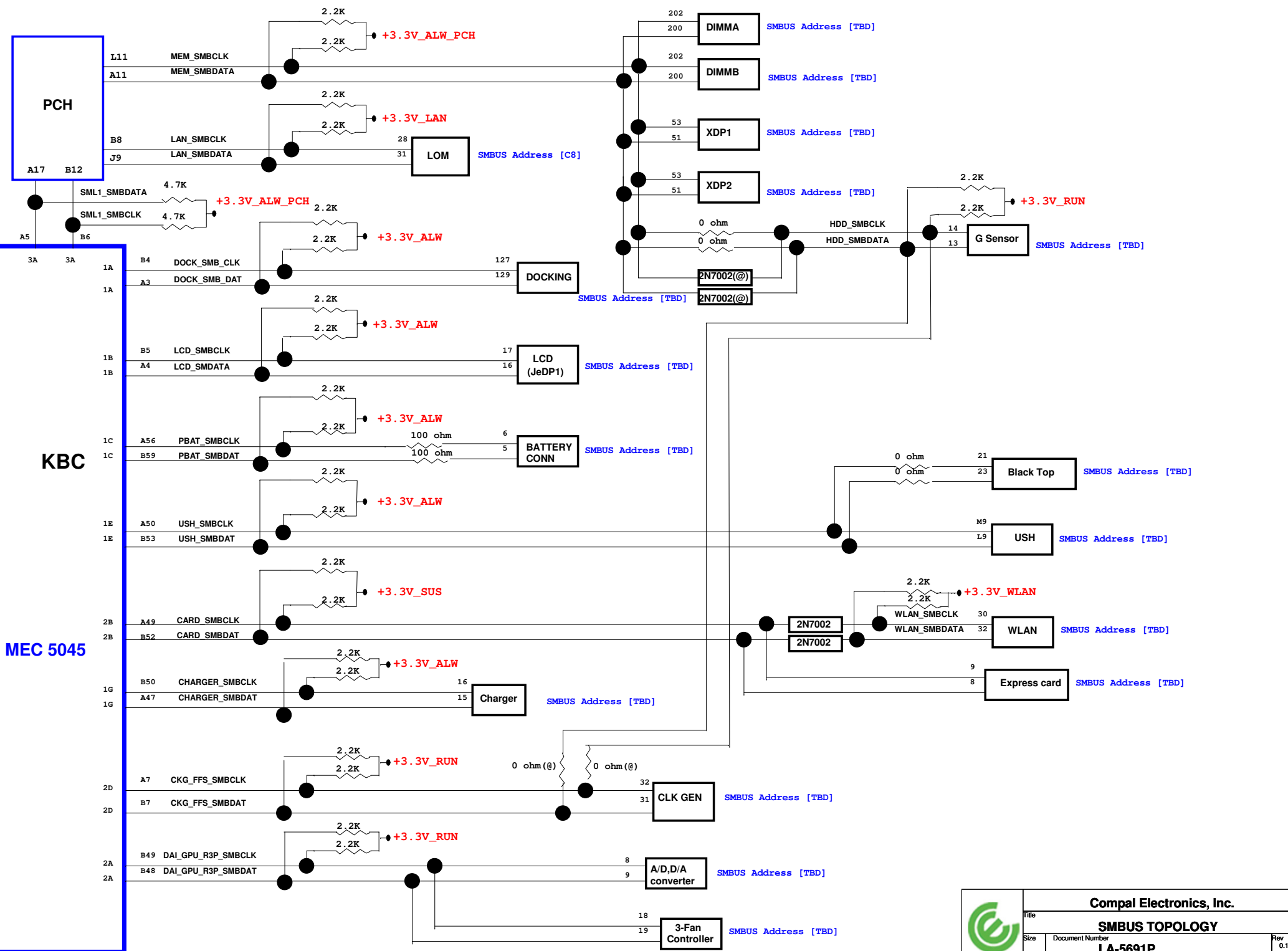
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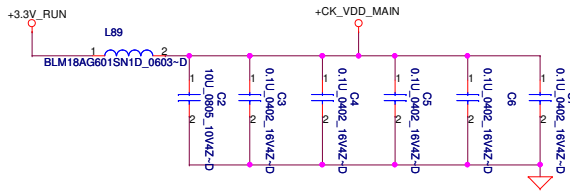


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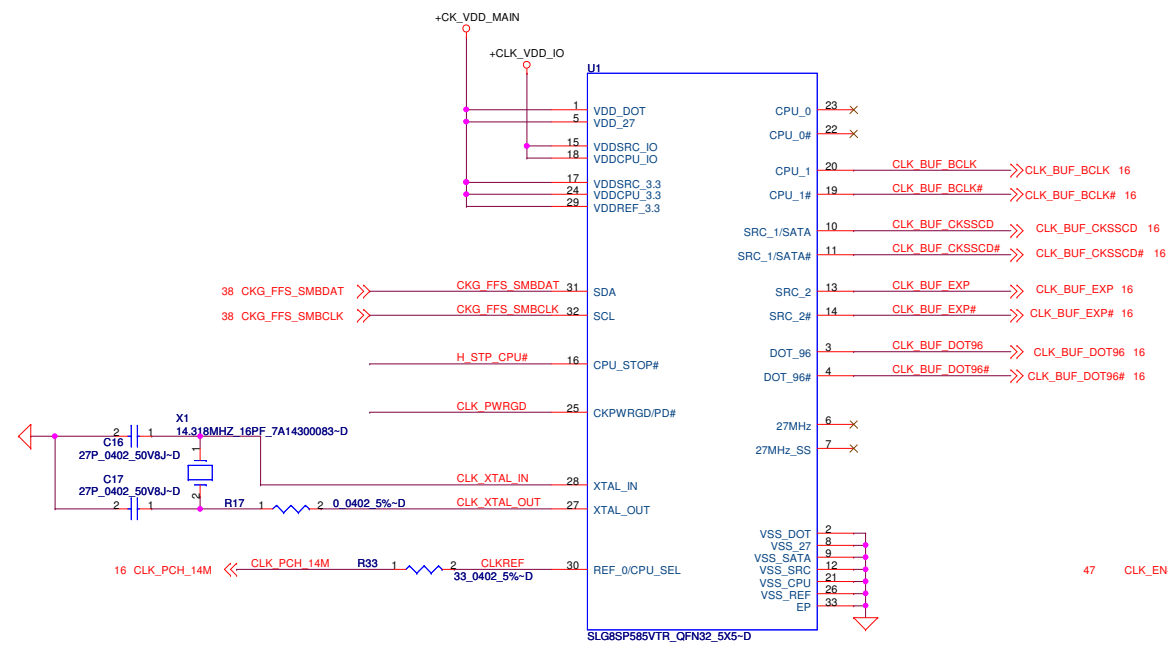
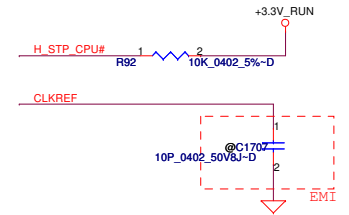
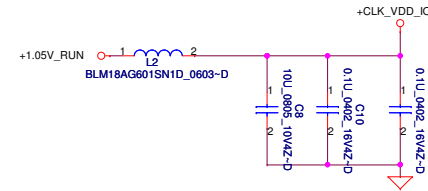
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<b>Power Rail</b>			
Size	Document Number	Rev	
	<b>LA-5691P</b>	0.1	
Date:	Monday, July 13, 2009	Sheet	4 of 51

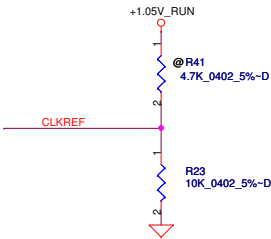
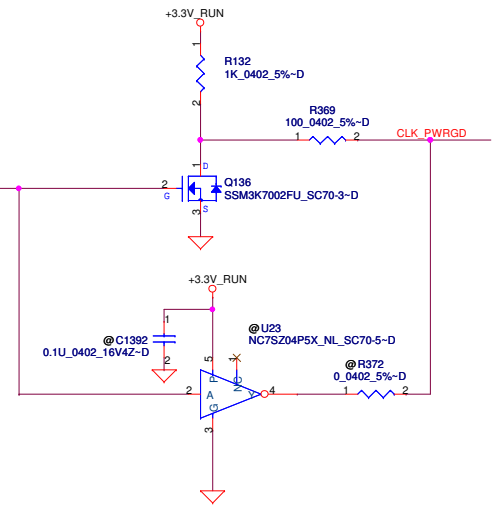




+CLK\_VDD\_IO CAN BE RANGE FROM 1.05V TO 3V



PIN 30	CPU0	CPU1
1 (0.7~1.5v)	100MHz	100MHz
0 (DEFAULT)	133MHz	133MHz



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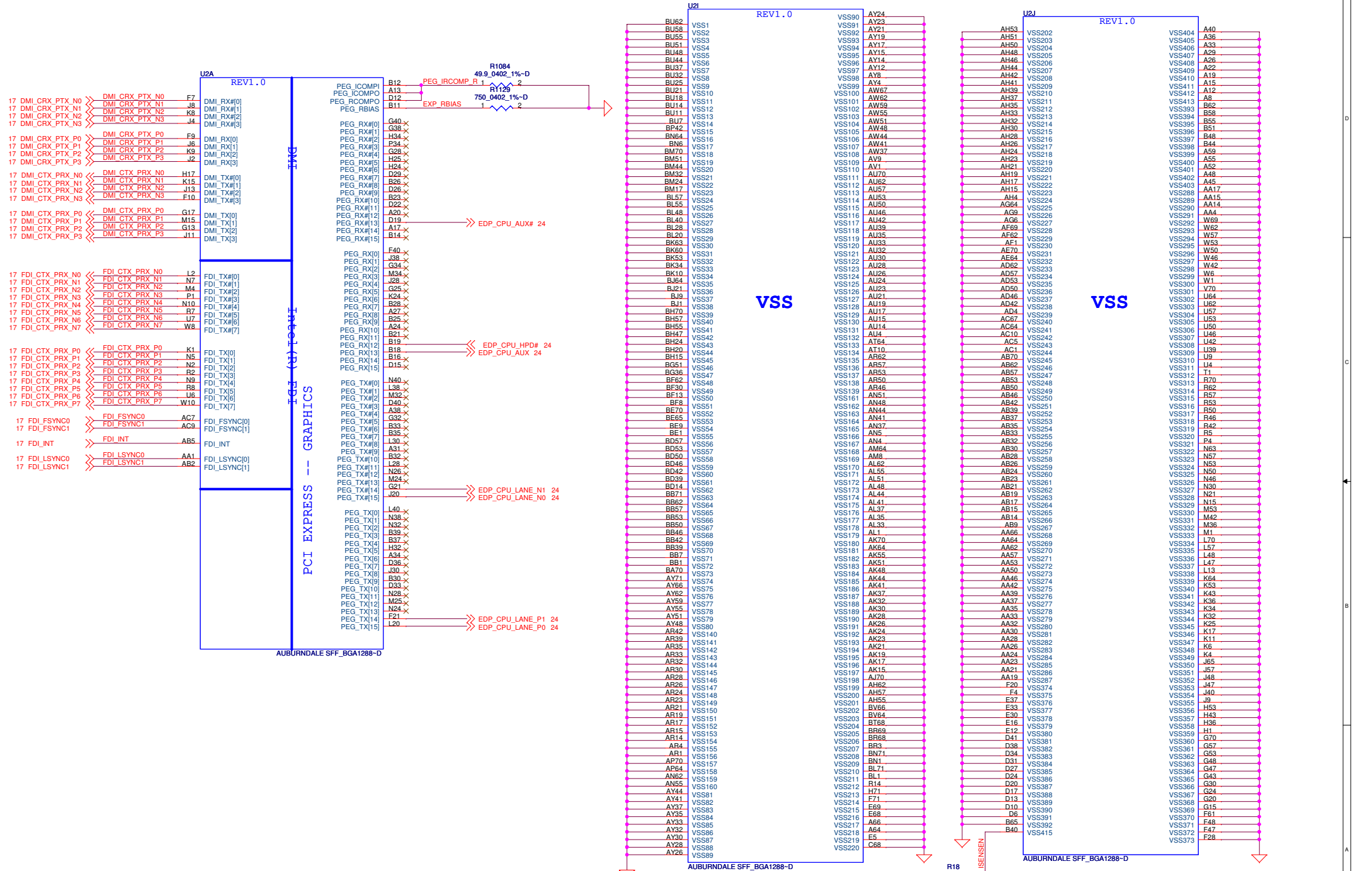
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**Clock Generator**

**LA-5691P**

Date: Monday, July 13, 2009 Sheet 6 of 51

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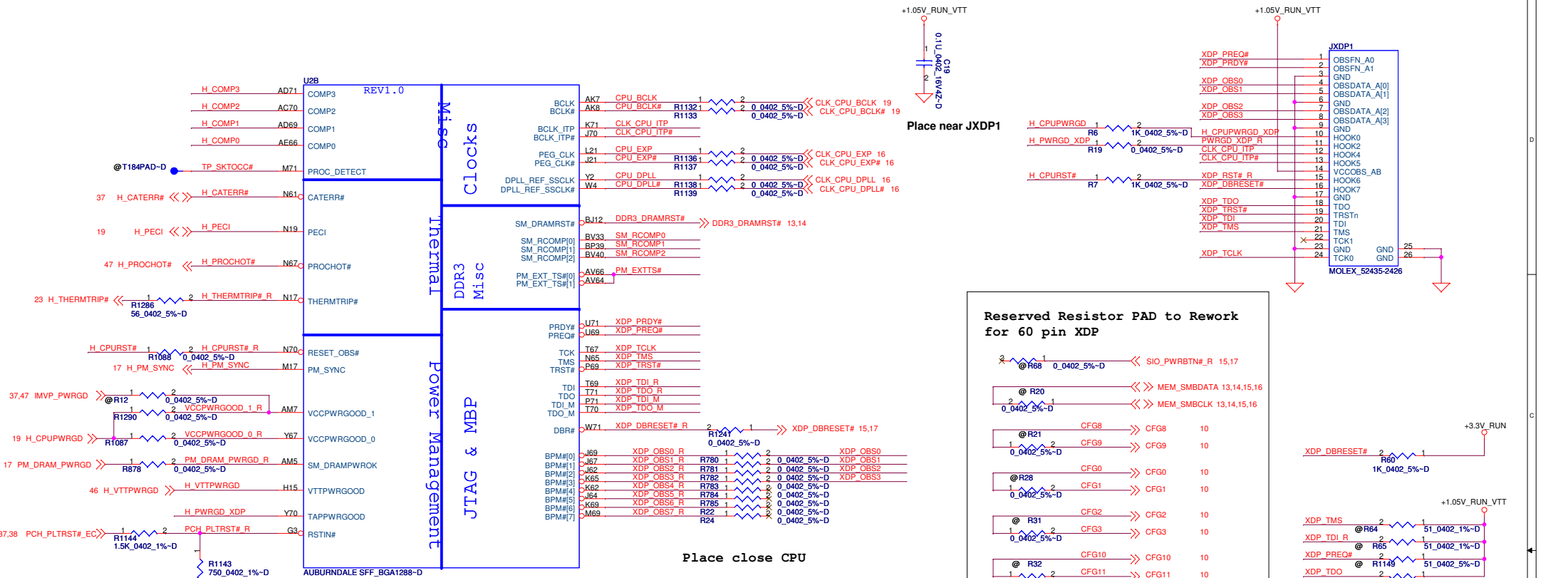
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**Auburndale (1/6)**

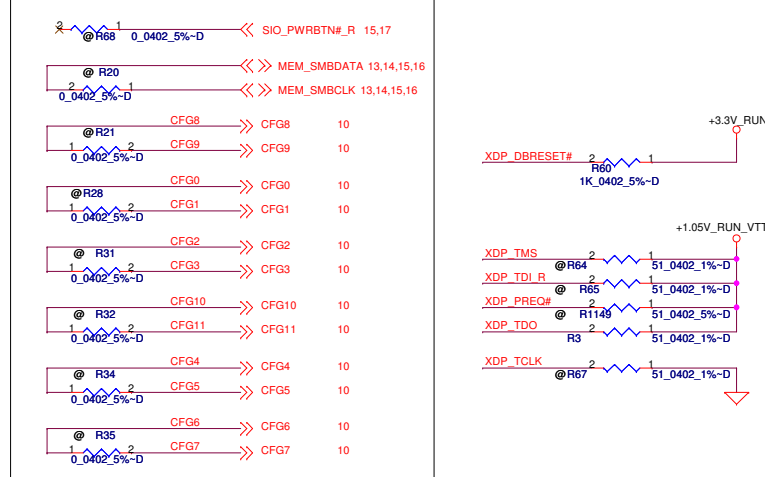
**LA-5691P**

Date: Monday, July 13, 2008 Sheet 7 of 51



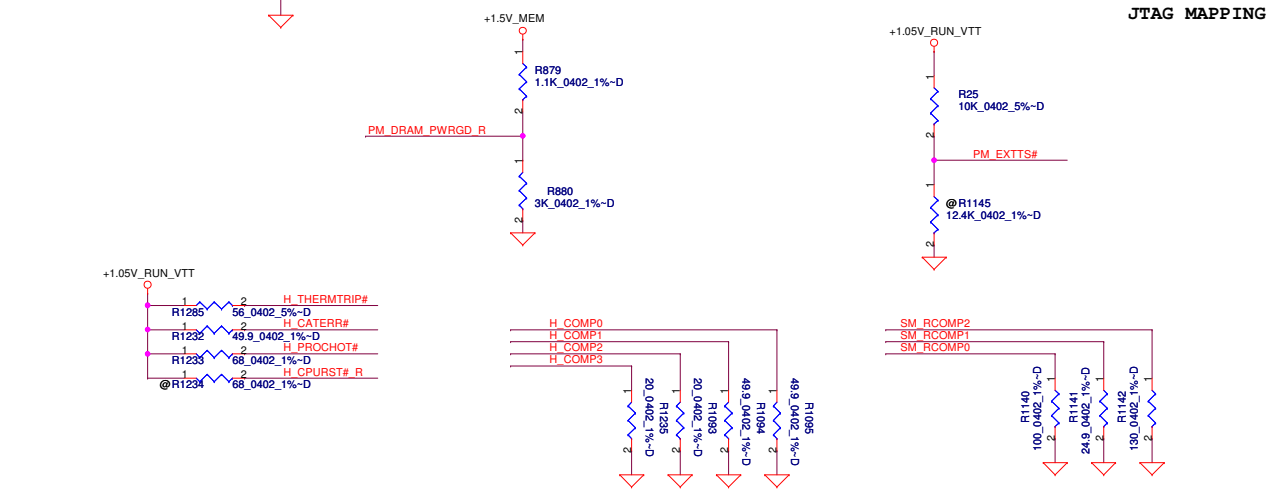
Place near JXDP1

**Reserved Resistor PAD to Rework for 60 pin XDP**

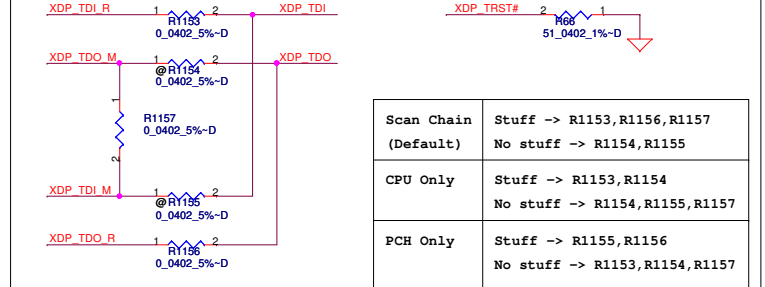


Place close CPU

**JTAG MAPPING**



**JTAG MAPPING**



Scan Chain	Stuff ->
(Default)	Stuff -> R1153, R1156, R1157 No stuff -> R1154, R1155
CPU Only	Stuff -> R1153, R1154 No stuff -> R1154, R1155, R1157
PCH Only	Stuff -> R1155, R1156 No stuff -> R1153, R1154, R1157

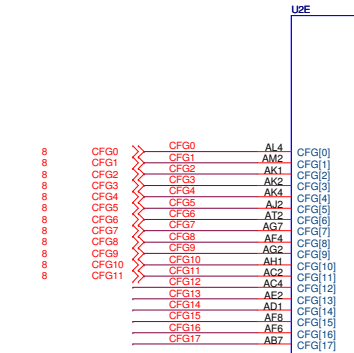
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**Auburndale (2/6)**  
**LA-5691P**  
 Date: Monday, July 13, 2009 Sheet 8 of 51

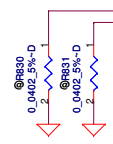
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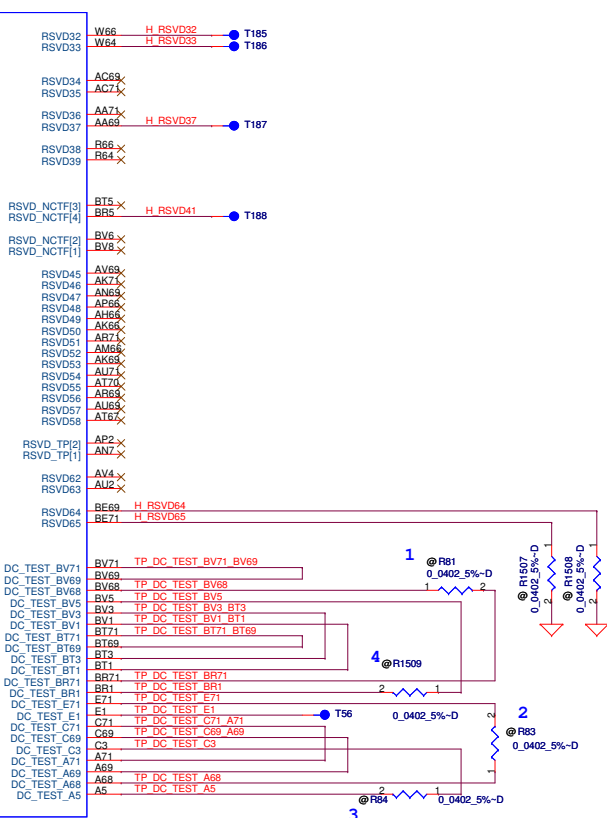




Reserve VIA on PCB

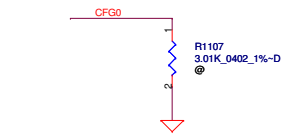


RESERVED

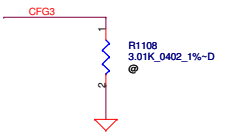


Package Daisy Chain:

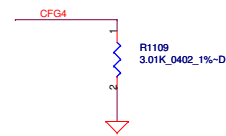
- 1: BR71 - pkg - BT71- board - BT69 - pkg - BV71 - board - BV69 - pkg - BV68
- 2: A68 - pkg - A69 - board - C69 - pkg - A71 - board - C71 - pkg - E71
- 3: A5 - pkg - C3
- 4: BR1 - pkg - BT1 - board - BV1 - pkg - BT3 - board - BV3 - pkg - BV5



PCI-Express Configuration Select	
CFG0	1 : Single PEG 0 : Bifurcation enable



PCI-Express Static Lane Reversal	
CFG3	1 : Normal Operation 0 : Lane Number Reversed 15->0, 14->1 ...



Display Port Presence	
CFG4*	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

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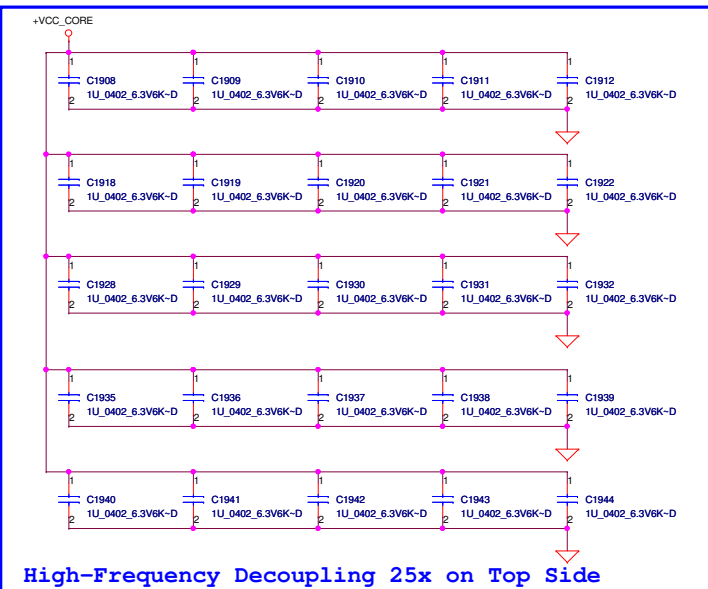
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Auburndale (4/6)

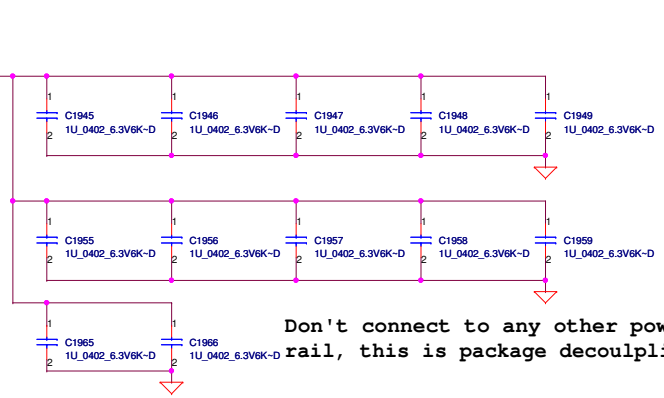
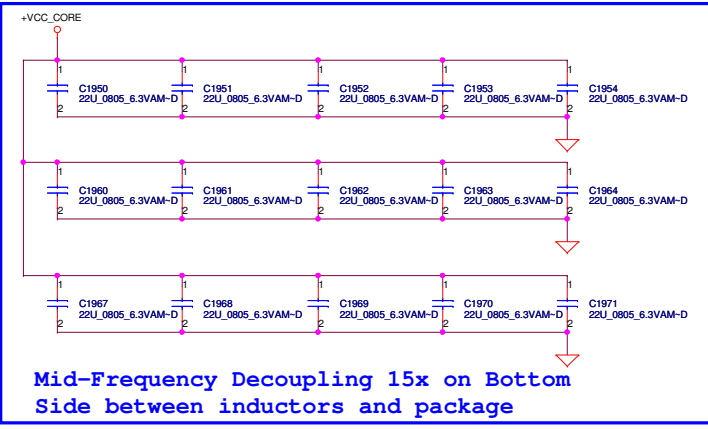
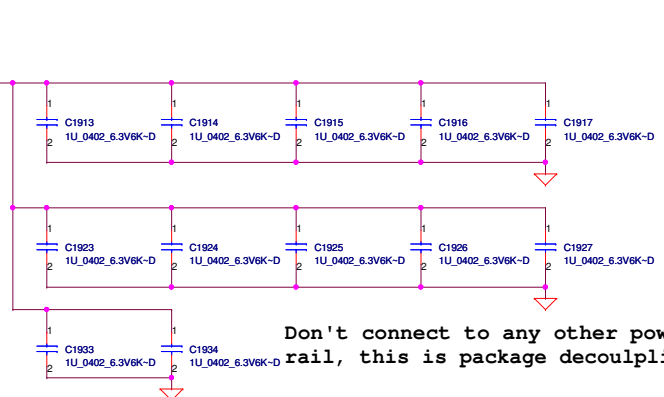
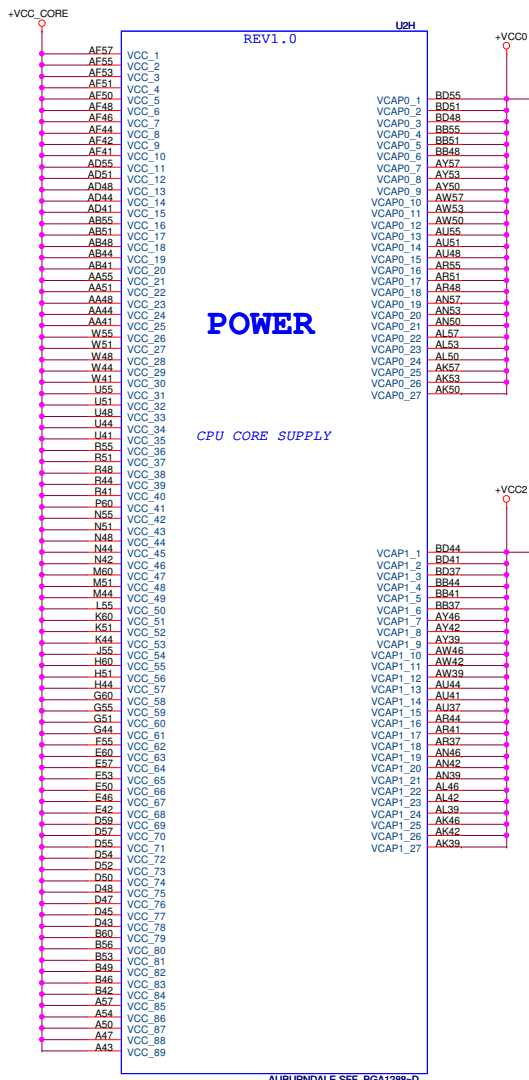


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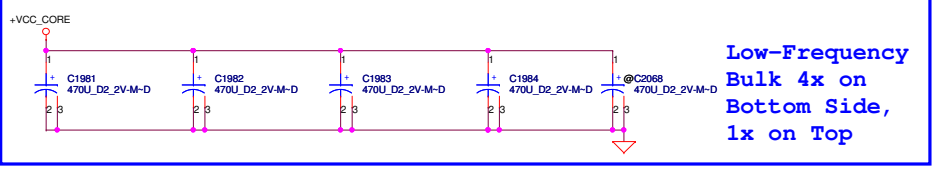
File	LA-5691P		Rev	0.1
Size	Document Number	LA-5691P	Date	Monday, July 13, 2008
			Sheet	10 of 51



Current =48A



PROCESSOR Power Rail Table (EDS V1.0)		
Voltage Rail	Voltage	S0 Iccmax Current (A)
VXNG	1.5	22
VccPLL	1.8	1.35
VCORE	0.75	48
VDDR	1.5	3
VTT	1.05	18



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Auburndale (5/6)

File  
Size Document Number  
Date: Monday, July 13, 2008 Sheet 11 of 51

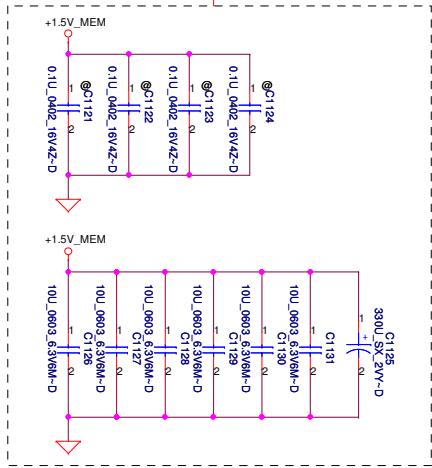
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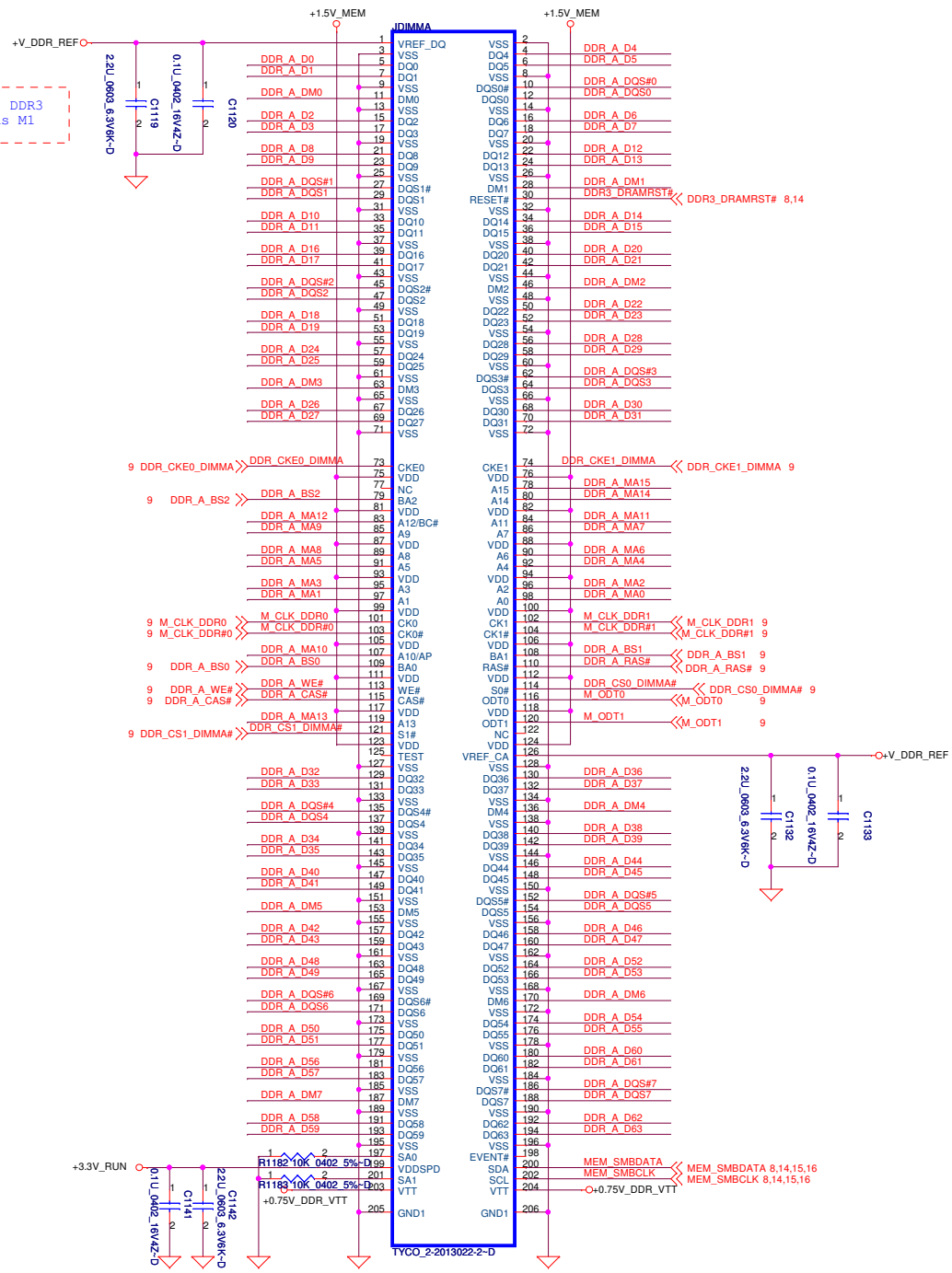
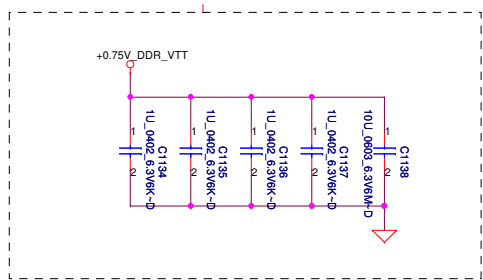
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- 9 DDR\_A\_D[0..63] <<>
- 9 DDR\_A\_DM[0..7] <<>
- 9 DDR\_A\_DQS#[0..7] <<>
- 9 DDR\_A\_MA#[0..15] <<>

Populate R87 for Intel DDR3 VREFDQ multiple methods M1

Layout Note:  
Place near JDIMMA



Layout Note:  
Place near JDIMMA. 203, 204



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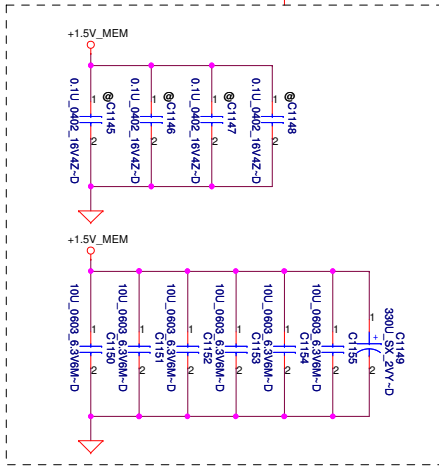
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Size	Document Number	Rev	0.1
LA-5691P			
Date:	Monday, July 13, 2009	Sheet	13 of 51

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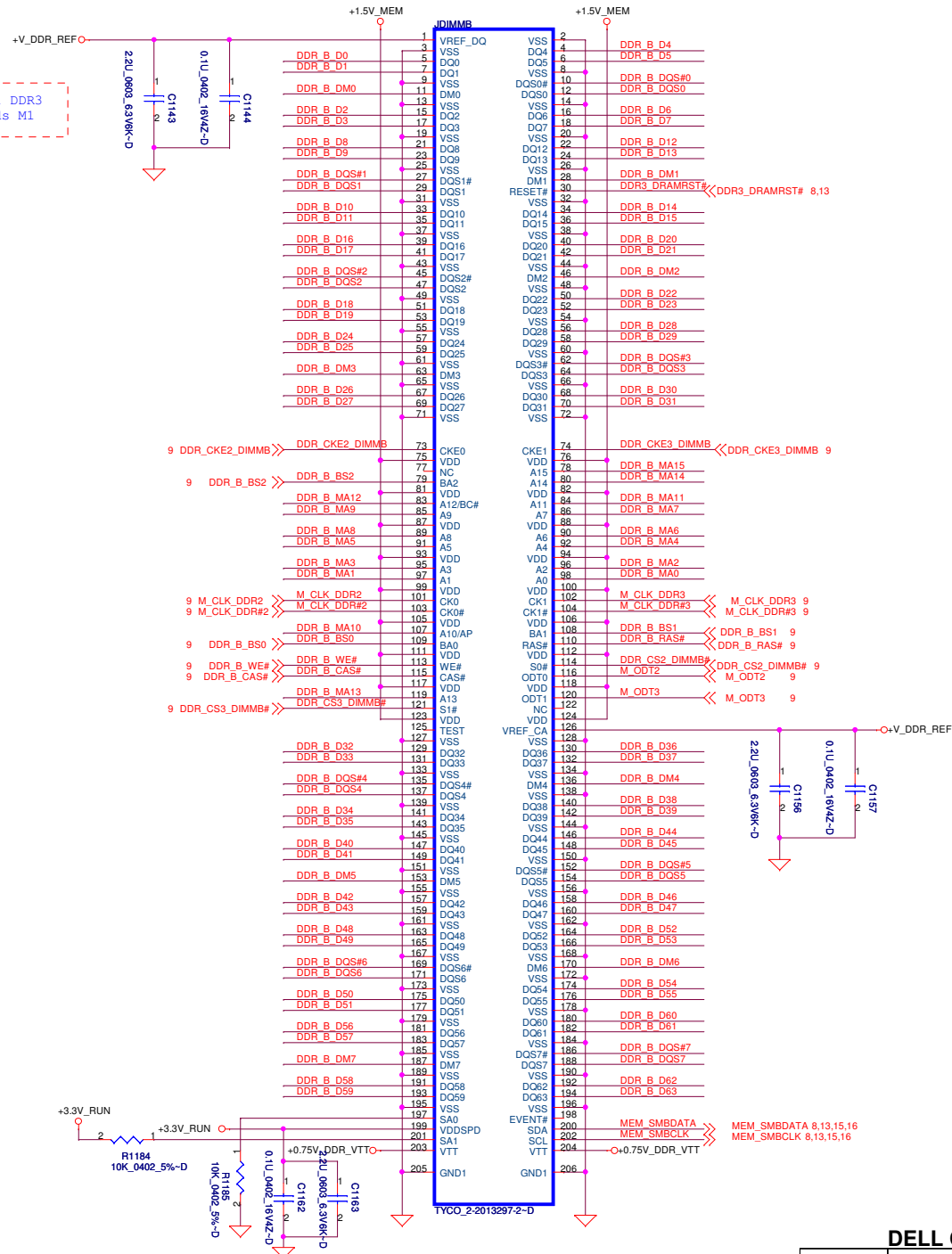
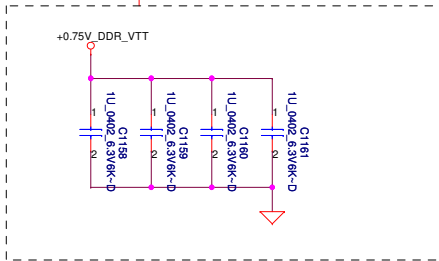
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- 9 DDR\_B\_DQ#0..63 <<>>
- 9 DDR\_B\_DM#0..7 <<>>
- 9 DDR\_B\_DQS#0..7 <<>>
- 9 DDR\_B\_MA#0..15 <<>>

Populate R88 for Intel DDR3  
VREFDQ multiple methods M1

Layout Note:  
Place near JDIMMB



Layout Note:  
Place near JDIMMB.203,204



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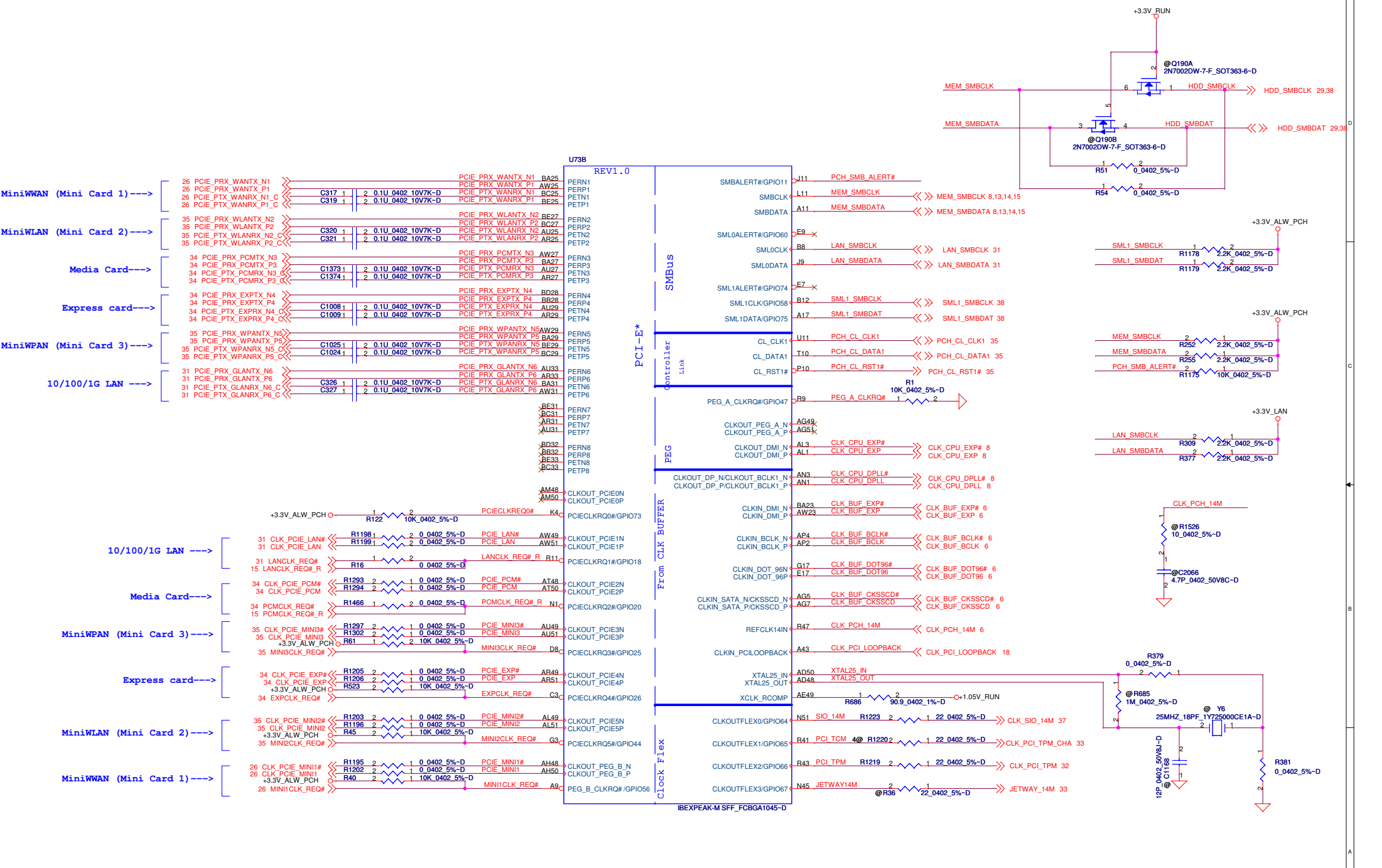


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<b>DDRIII-SODIMM SLOT2</b>			
File	Document Number		Rev
	<b>LA-5691P</b>		0.1
Date:	Monday, July 13, 2009	Sheet	14 of 51







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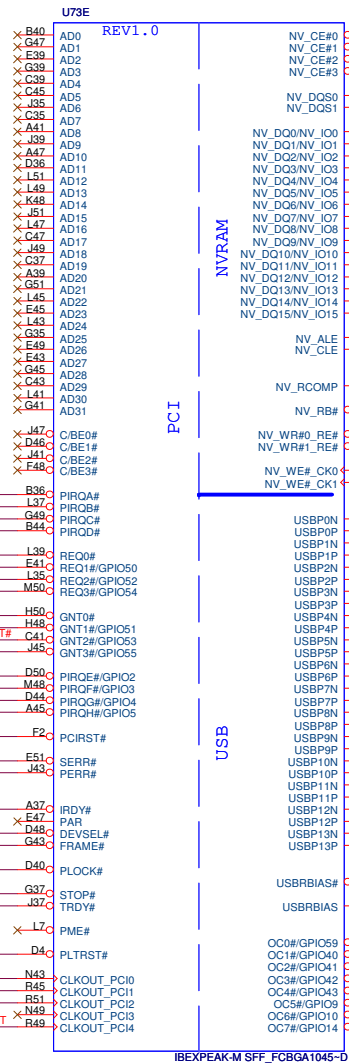
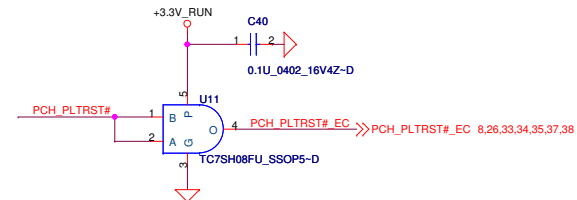
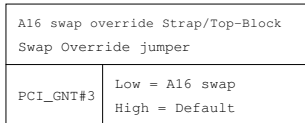
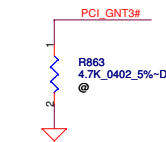
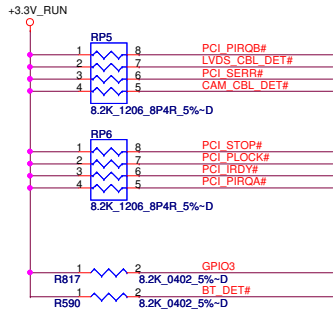
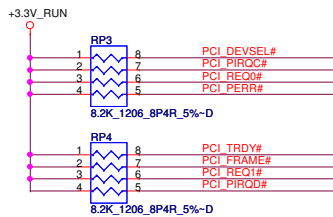
**PCH (2/8)**

Size: Document Number **LA-5691P** Rev: 0.1

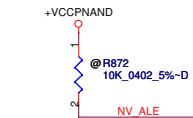
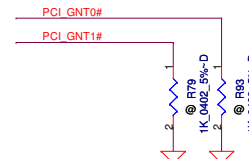
Date: Monday, July 13, 2009 Sheet: 16 of 51



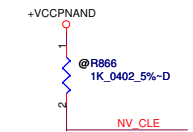




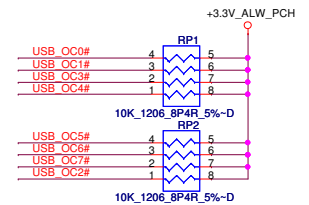
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0	1	Reserved (NAND)
1	0	PCI
1	1	SPI



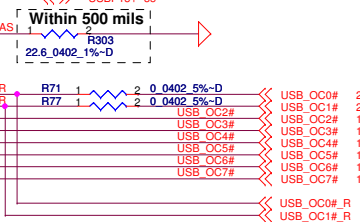
Danbury Technology Enabled	
NV_ALE	High = Enabled (Default) Low = Disabled



DMI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH



- >Right Side
- >Left Side
- >WLAN
- >WWAN
- >Blue Tooth
- >BIO
- >DOCK
- >Express Card
- >Camera
- >BKT
- >WPAN



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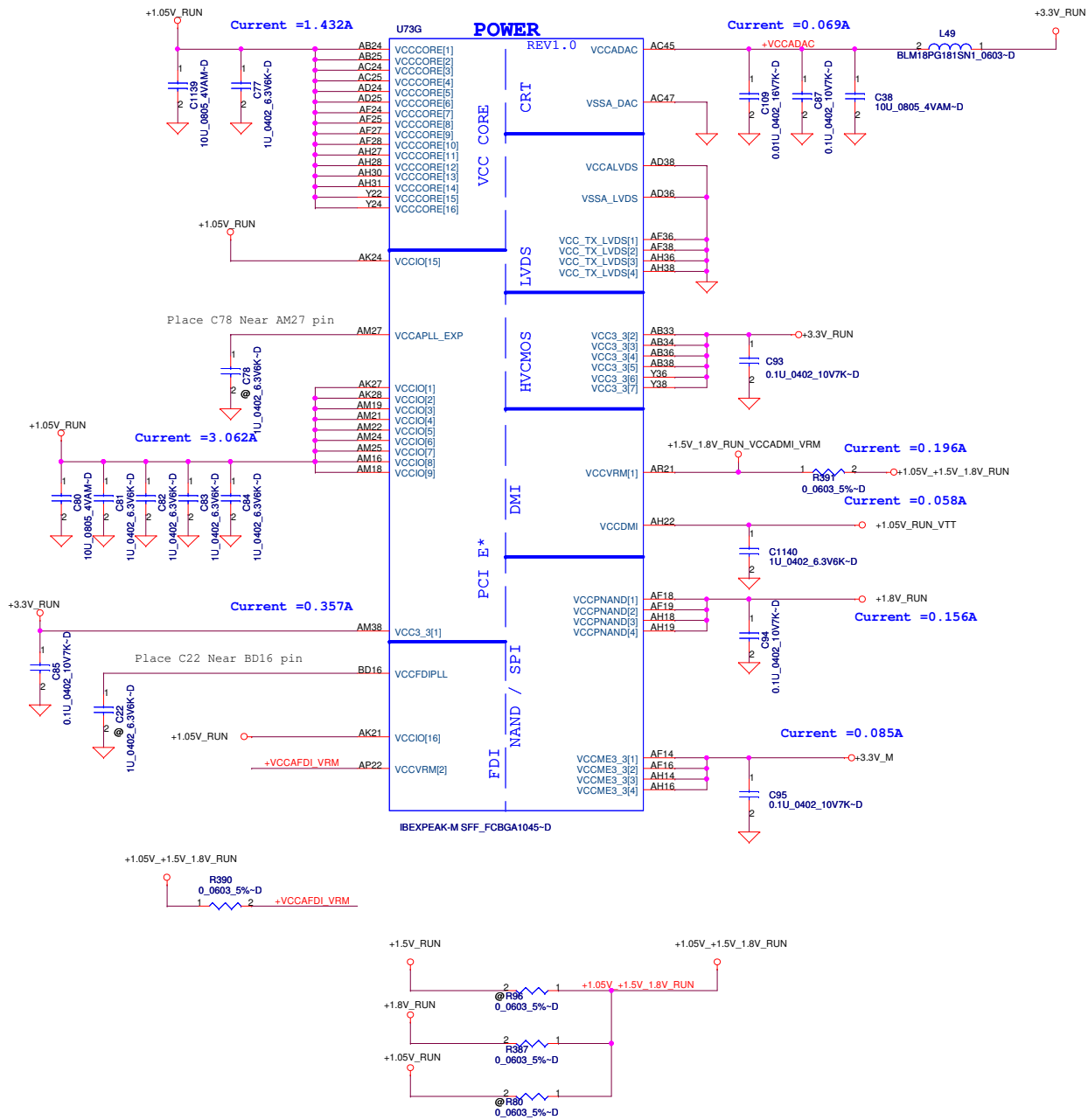
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Size: \_\_\_\_\_ Document Number: **LA-5691P** Rev: 0.1

Date: Monday, July 13, 2009 Sheet: 18 of 51





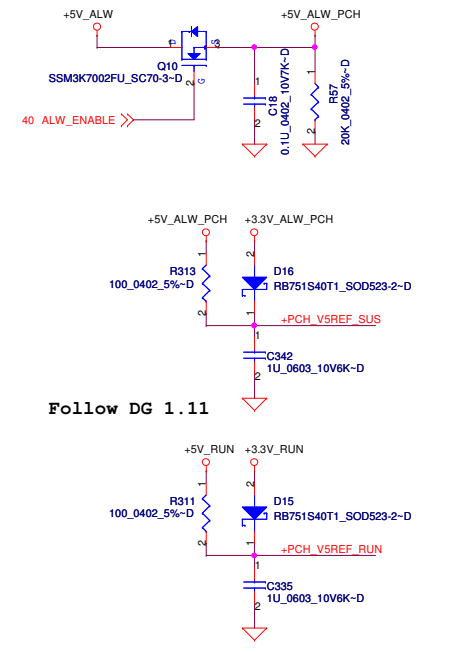
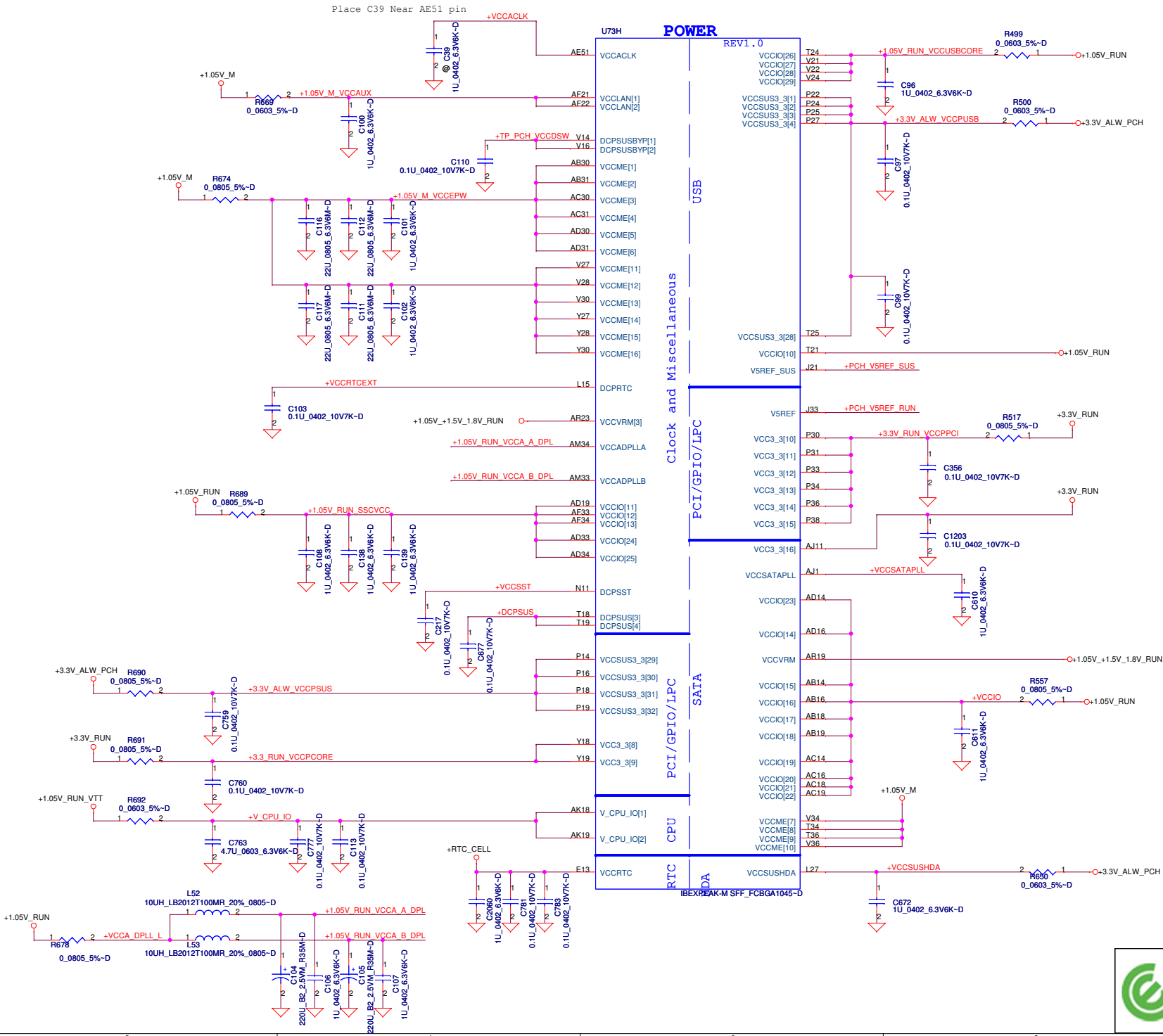
PCH Power Rail Table		
Voltage Rail	Voltage	SO Iccmax Current (A)
V_CPU_IO	1.1/1.05	< 1 (mA)
V5REF	5	< 1 (mA)
V5REF_Sus	5	< 1 (mA)
Vcc3_3	3.3	0.357
VccAClk	1.1	0.052
VccADAC	3.3	0.069
VccADPLLA	1.1	0.068
VccADPLLB	1.1	0.069
Vccap11EXP	1.1	0.04
VccCore	1.1	1.432
VccDMI	1.1	0.058
VccDMI	1.1	0.061
VccFDIPLL	1.1	0.037
VccIO	1.1	3.062
VccLAN	1.1	0.32
VccME	1.1	1.849
VccME3_3	3.3	0.085
VccpNAND	1.8	0.156
VccRTC	3.3	2 (mA)
VccSATAPLL	1.1	0.031
VccSus3_3	3.3	0.163
VccSusHDA	3.3	0.006
VccVRM	1.8 / 1.5	0.196
VccALVDS	3.3	< 1 (mA)
VccTX_LVDS	1.8	0.059

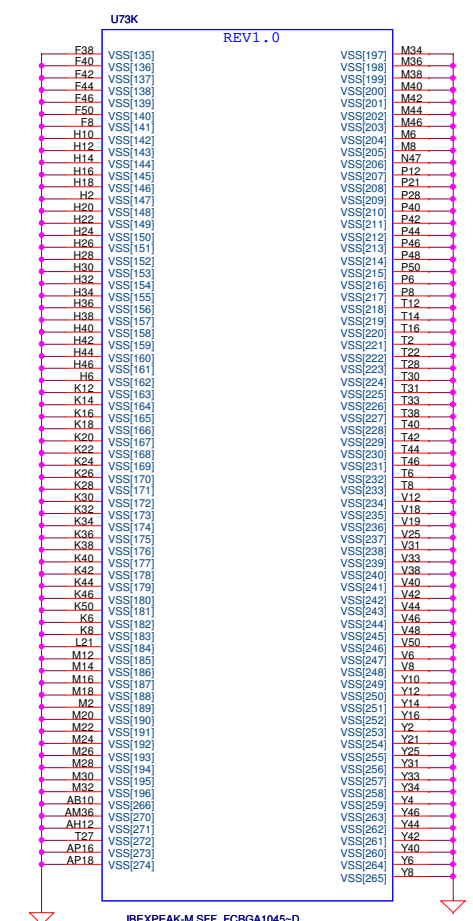
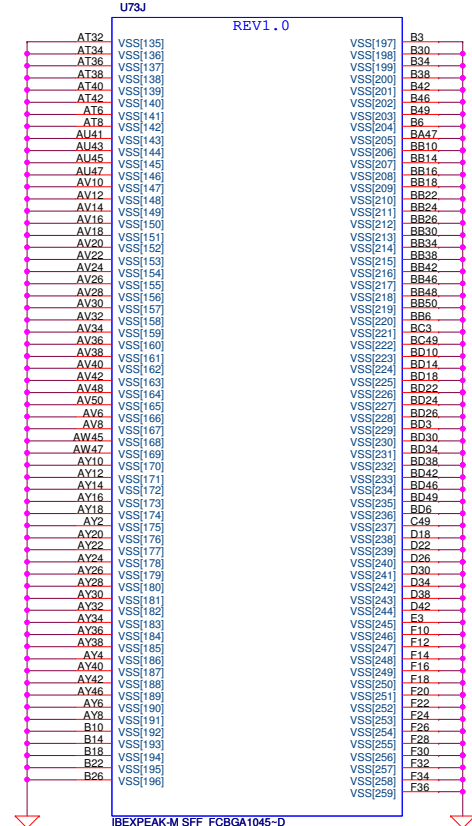
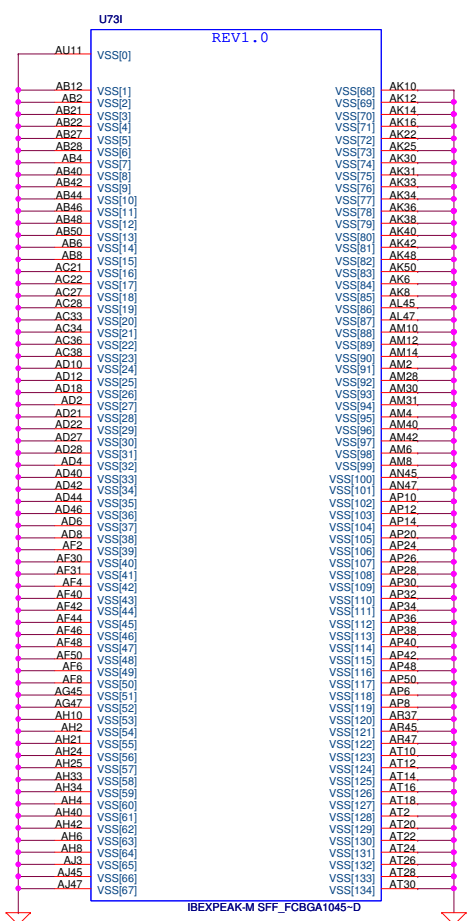
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Compal Electronics, Inc.



Title			PCH (6/8)		
Size	Document Number	Rev			0.1
	LA-5691P				
Date:	Monday, July 13, 2009	Sheet	20	of	51





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**Compal Electronics, Inc.**

Title: **PCH (8/8)**

Size: **LA-5691P**

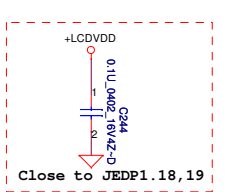
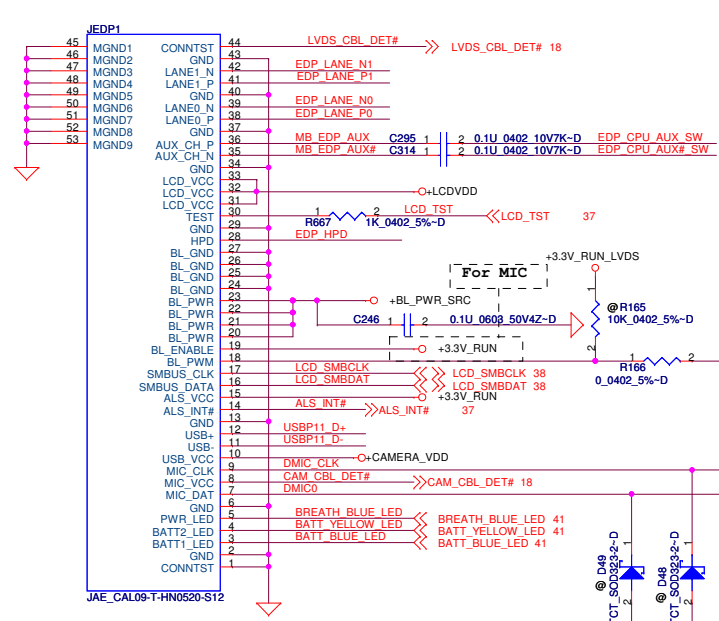
Date: **Monday, July 13, 2009**

Sheet: **22** of **51**

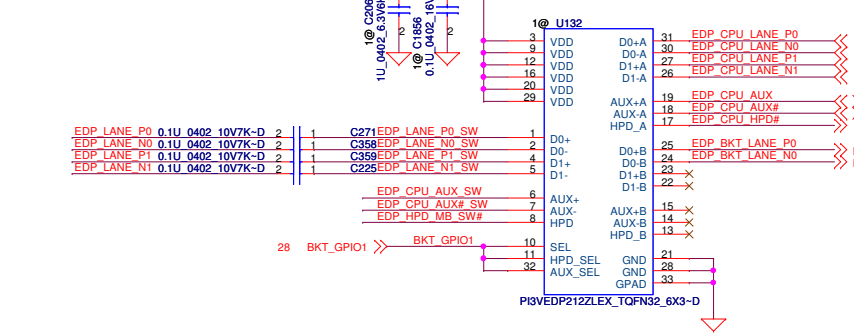
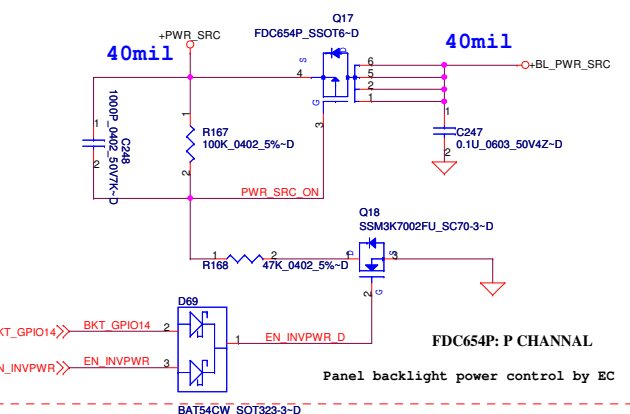
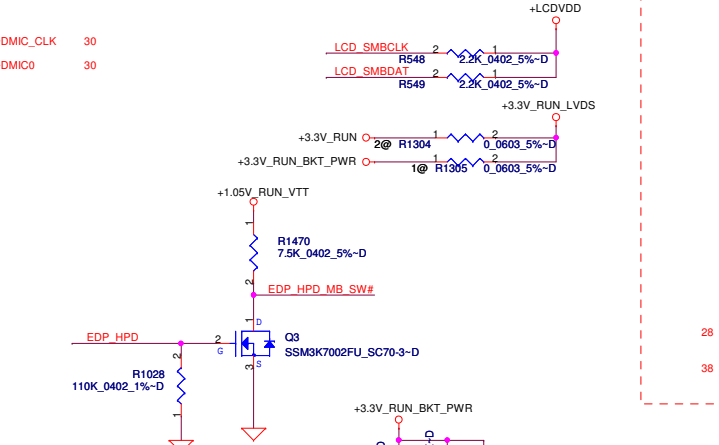
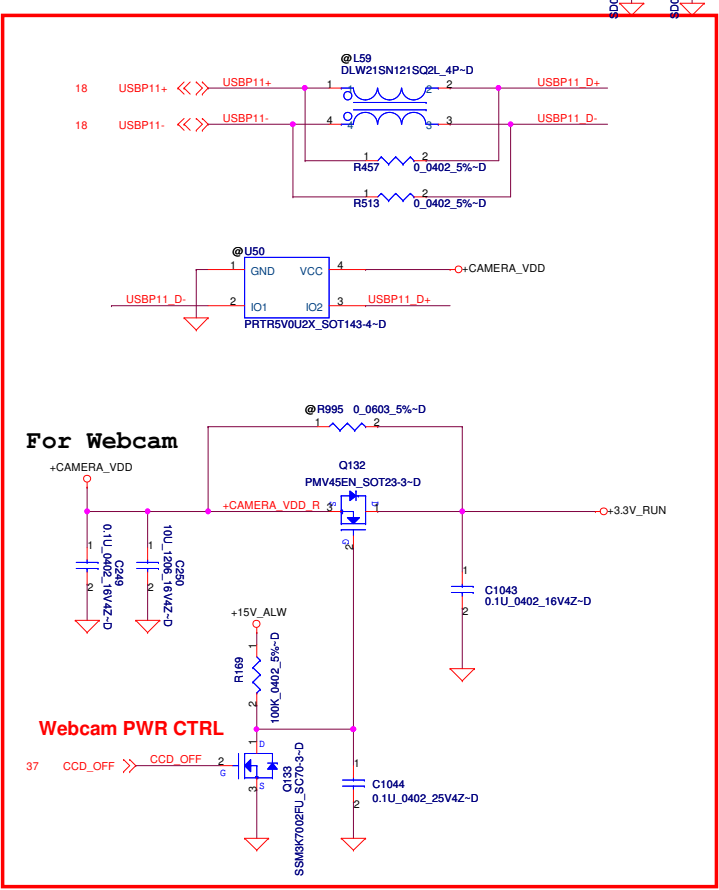
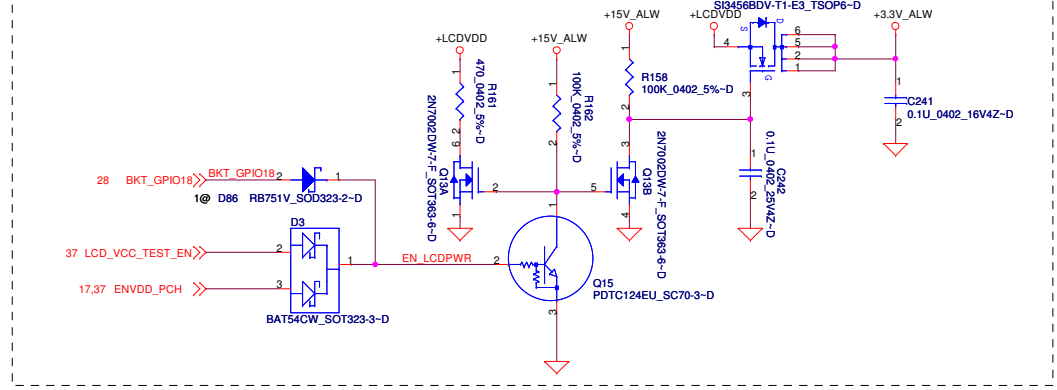
Rev: **0.1**



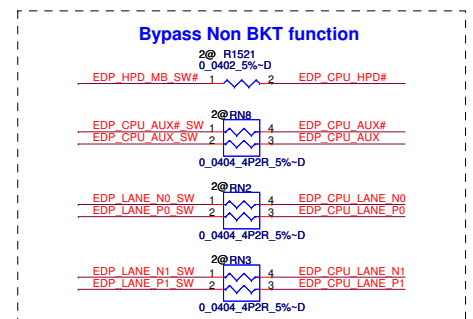




**LCD Power**



Function	SEL/HPD_SEL/AUX_SSEL
Port A active	L
Port B active	H



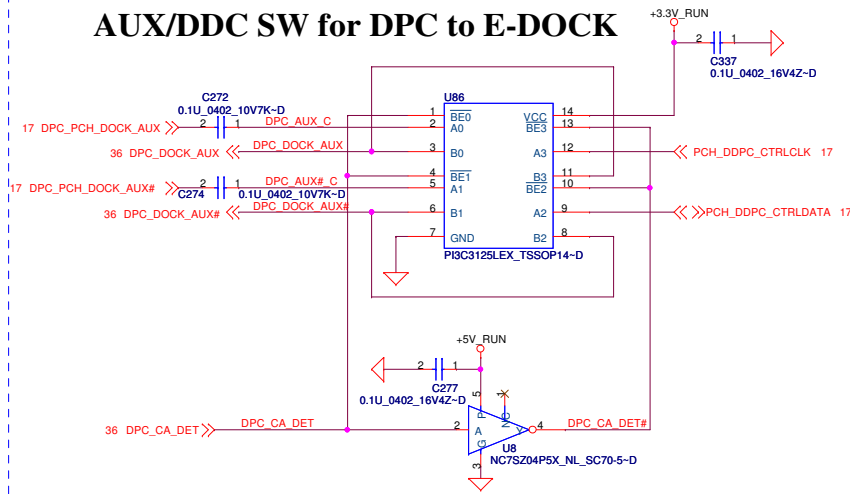
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**Compal Electronics, Inc.**  
**eDP & CAM Conn**

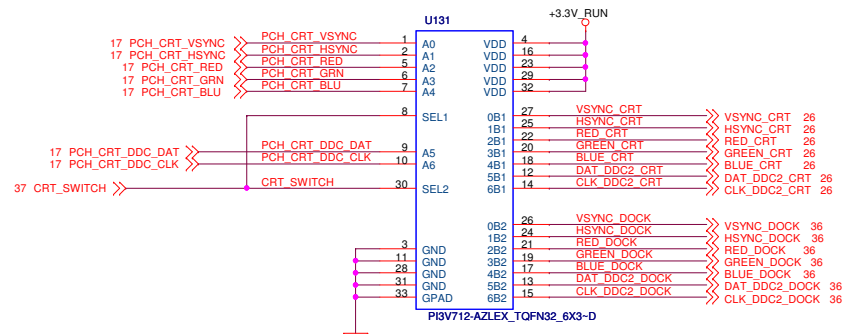
Size: Document Number **LA-5691P** Rev: 0.1  
 Date: Monday, July 13, 2009 Sheet: 24 of 51



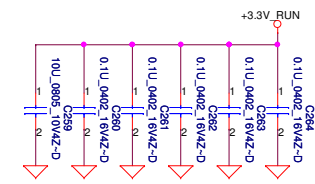
### AUX/DDC SW for DPC to E-DOCK



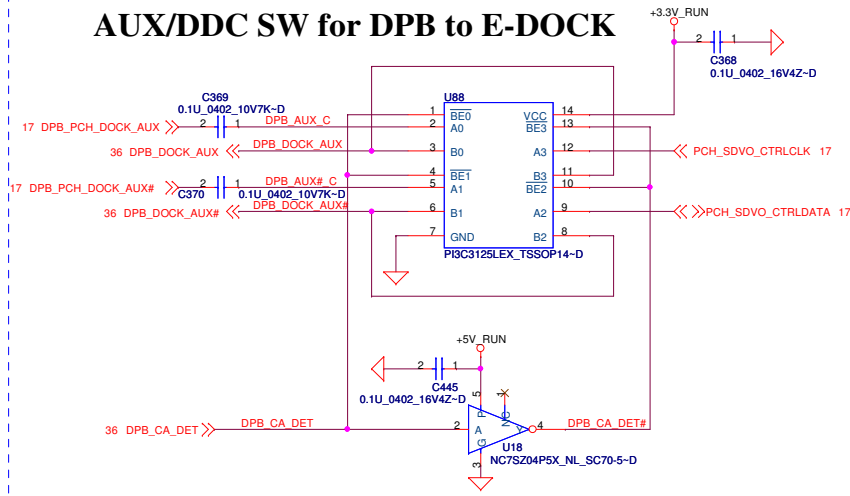
### VGA SW for MB/DOCK



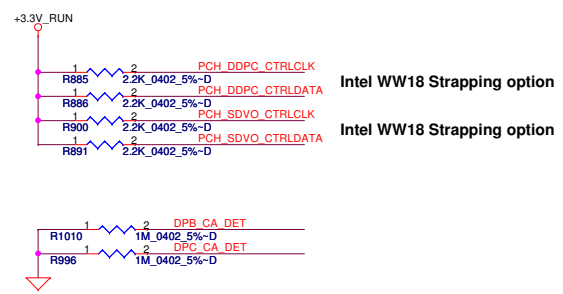
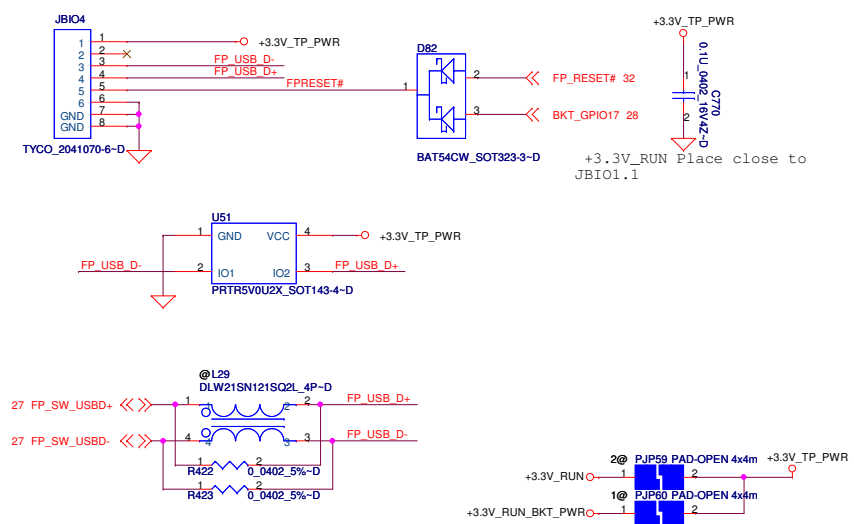
SEL1/SEL2	Chanel	Source
0	A=B1	MB
1	A=B2	APR/SPR



### AUX/DDC SW for DPB to E-DOCK



### Fingerprint CONN.



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**DPC DPD SW for DOCK**

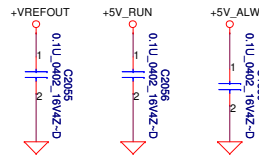
LA-5691P

Monday, July 13, 2009

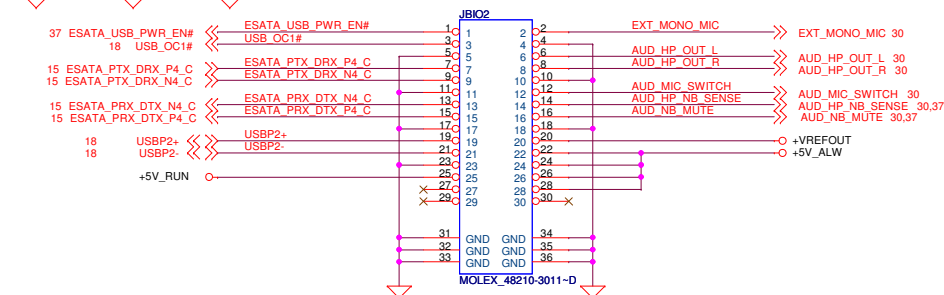


Size	Document Number	Rev
	LA-5691P	0.1
Date:	Monday, July 13, 2009	Sheet 25 of 51

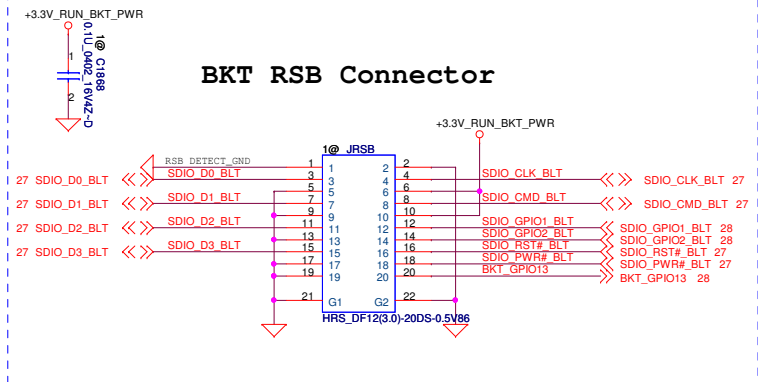
Close to JP1



E-SATA/Jack Connector

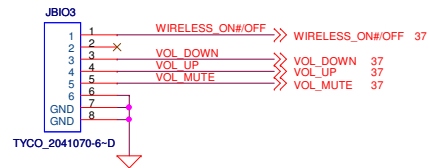


BKT RSB Connector

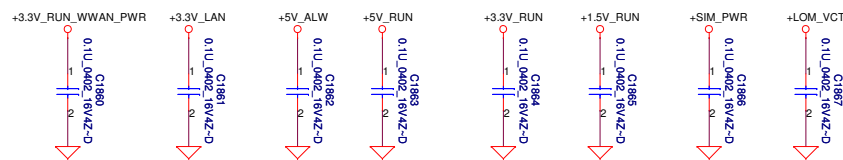
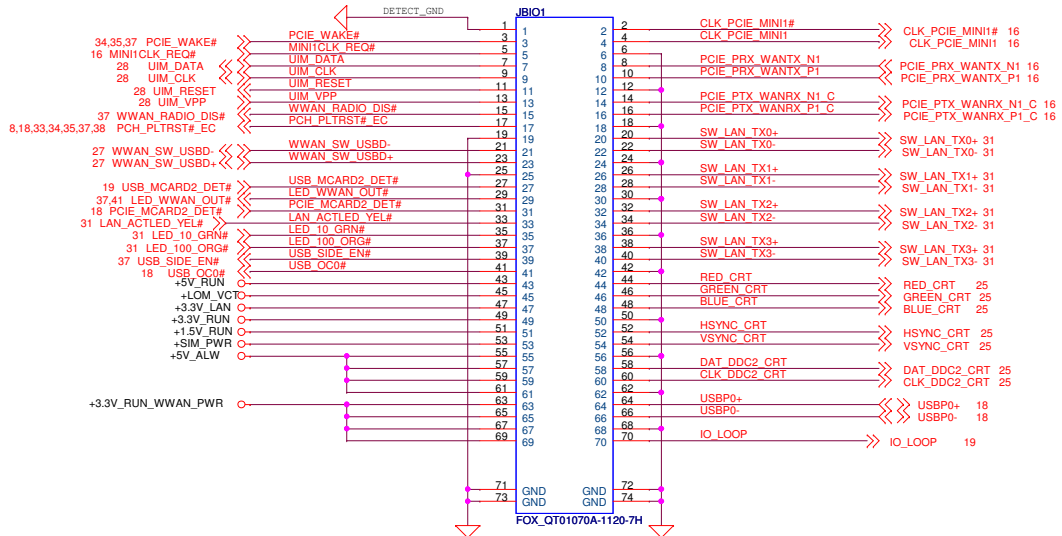


Volume + Sniffer

Change to 6 pins connector



BTB Connector

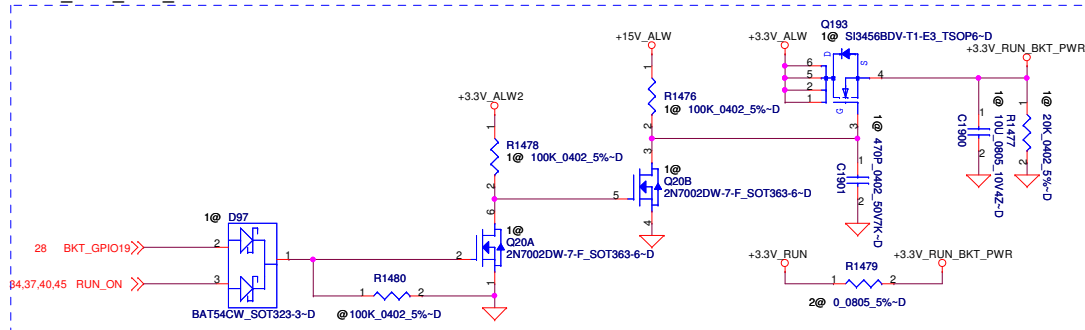


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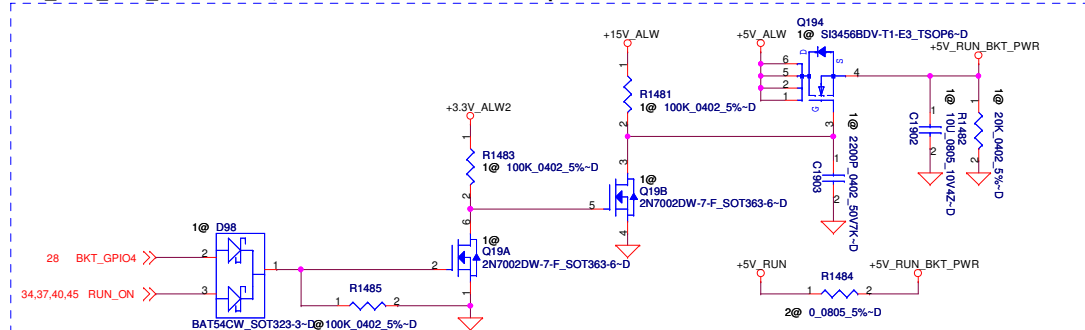
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<b>Compal Electronics, Inc.</b>		
<b>Display port</b>		
Size	Document Number	Rev
	<b>LA-5691P</b>	0.1
Date:	Monday, July 13, 2009	Sheet 26 of 51

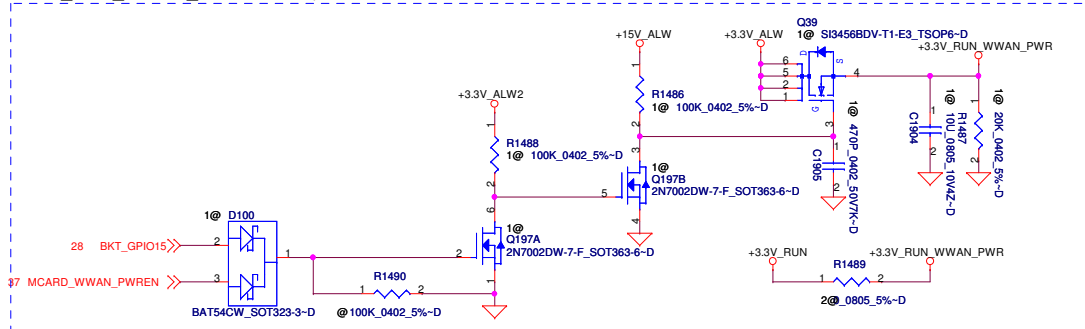
### +3.3V\_RUN\_BKT\_PWR Source



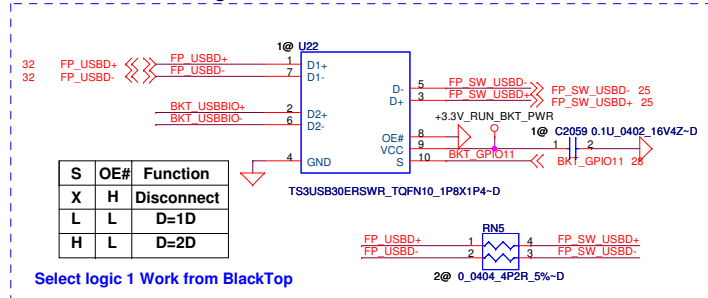
### +5V\_RUN\_BKT\_PWR Source, for Touch Pad and Audio Amplifier



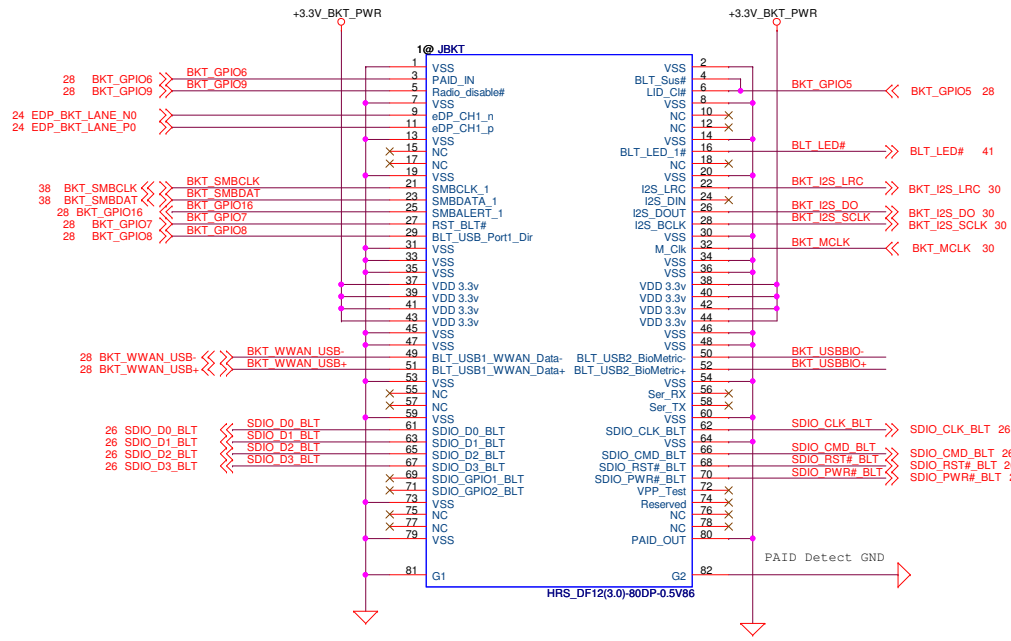
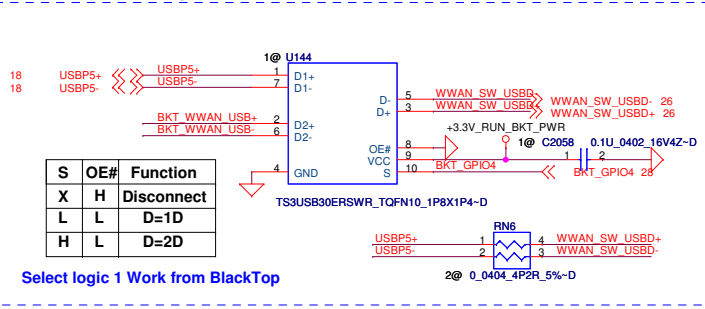
### +3.3V\_RUN\_WWAN\_PWR Source, for WWAN



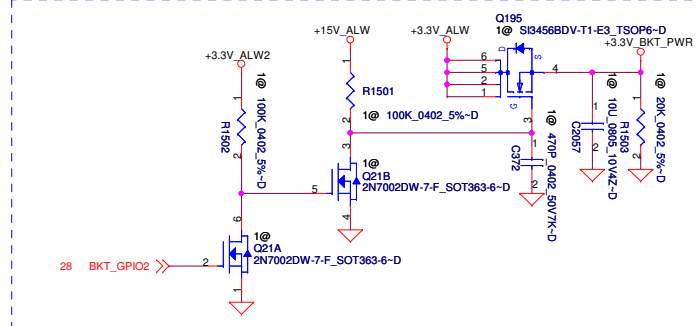
### For Biometric USB signals isolation



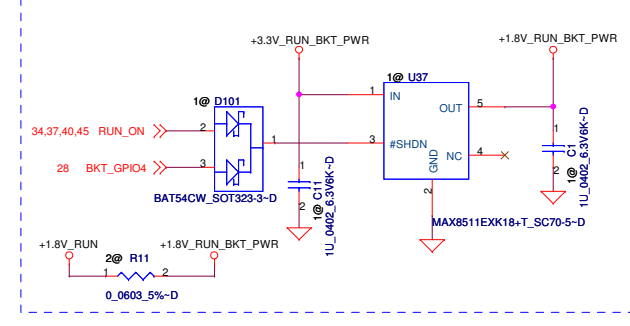
### For WWAN USB signals isolation



### Enable BlackTop POWER



### For Audio I2S



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**BlackTop POWER and CONN**

LA-5691P

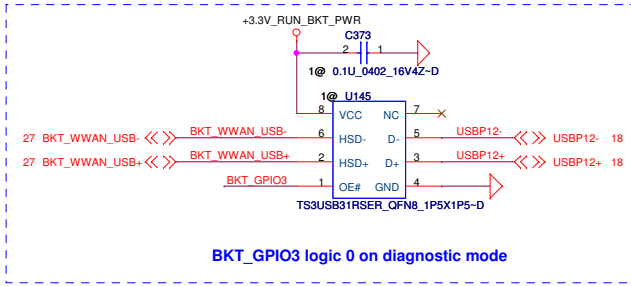
Monday, July 13, 2009

Sheet 27 of 51

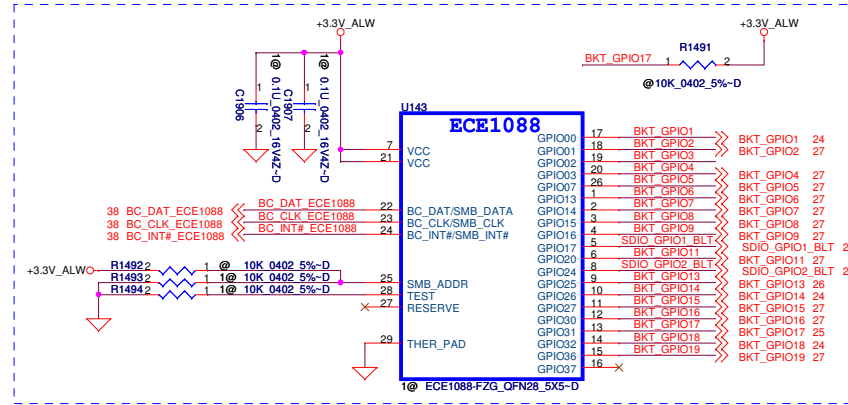
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# GPIO Expander for BlackTop

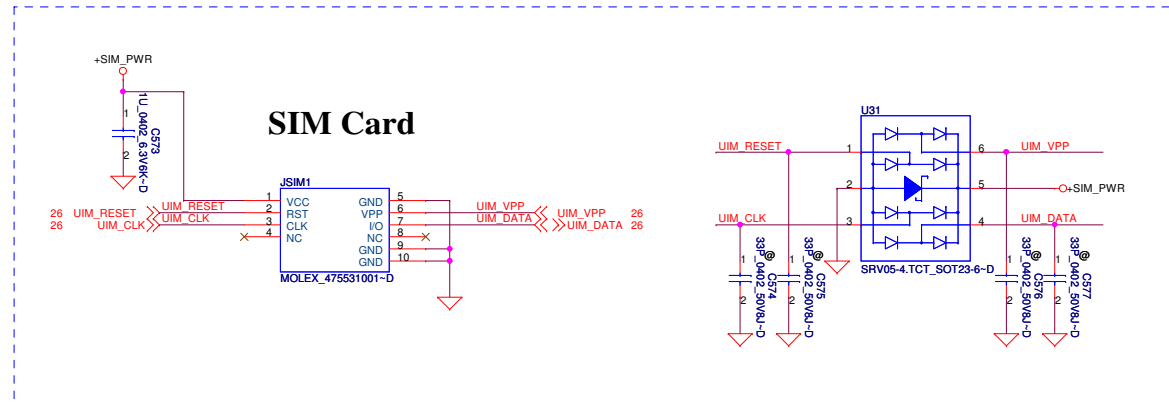
## Add BlackTop to PCH interface by USB signal when diagnostic mode



- BKT\_GPIO1 → For eDP signals switch
- BKT\_GPIO2 → For BKT power switch
- BKT\_GPIO3 → For TP power switch&USB signal switch
- BKT\_GPIO4 → For AMP/TP power source&USB signal switch
- BKT\_GPIO5 → For LID\_Closed
- BKT\_GPIO6 → For PAD\_Out
- BKT\_GPIO7 → For BKT Reset
- BKT\_GPIO8 → For USB\_SEL\_BLK
- BKT\_GPIO9 → For Radio\_OFF
- BKT\_GPIO11 → Biometric mux switch
- BKT\_GPIO12 → For WLAN antenna mux control
- BKT\_GPIO13 → RSB\_DET#
- BKT\_GPIO14 → For Inverter Power
- BKT\_GPIO15 → For WWAN Power
- BKT\_GPIO16 → For SMBALERT
- BKT\_GPIO17 → For Biometric reset signal
- BKT\_GPIO18 → For LVDS Power switch
- BKT\_GPIO19 → For TP Power



## SIM Card



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Title Braidwood/ SATA repeater & PCIE SATA SW

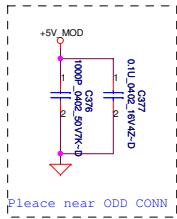
Size Document Number

LA-5691P

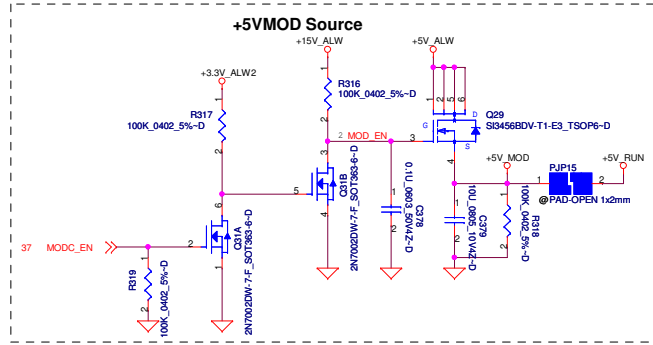
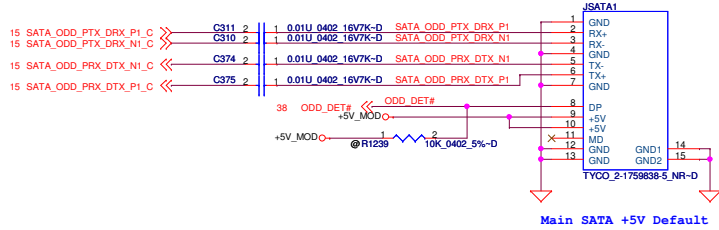
Date: Monday, July 13, 2009 Sheet 28 of 51

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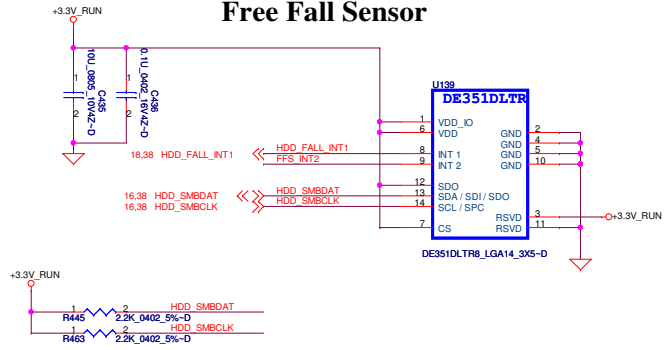




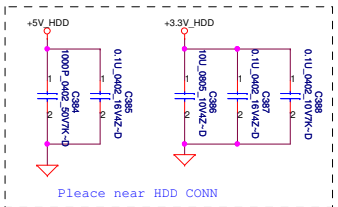
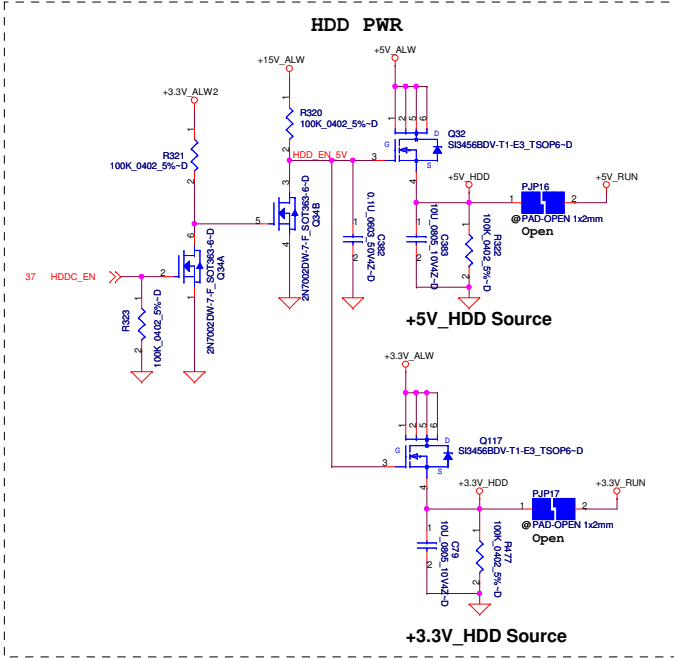
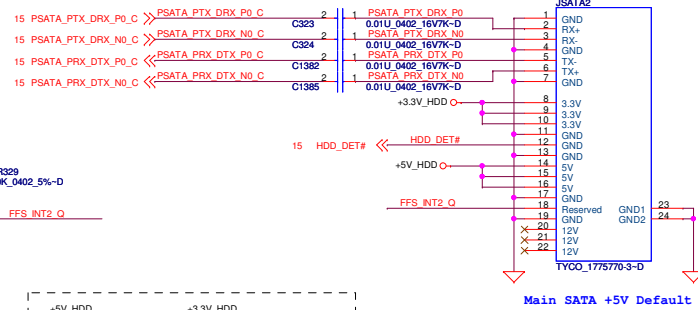
### For ODD



### Free Fall Sensor



### For HDD



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Compal Electronics, Inc.

File		ODD/HDD CONNECTOR	
Size	Document Number	LA-5691P	
Date	Monday, July 13, 2009	Sheet	29 of 51

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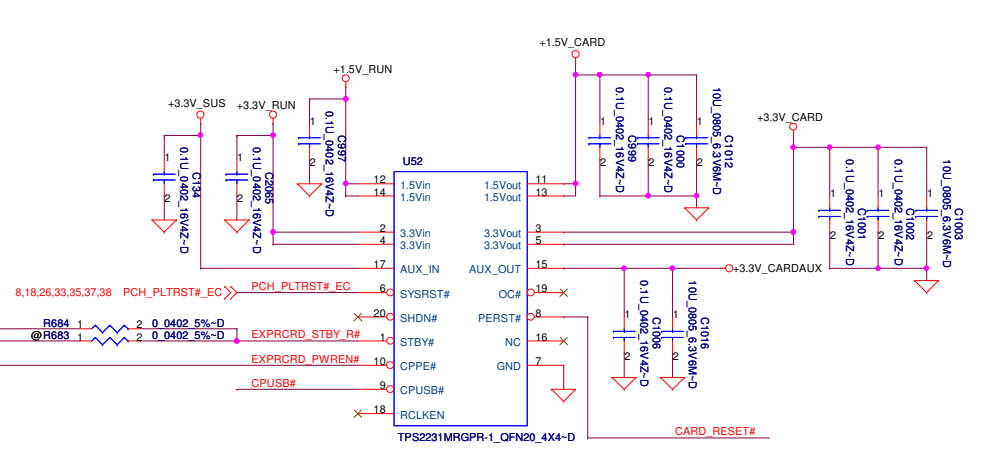
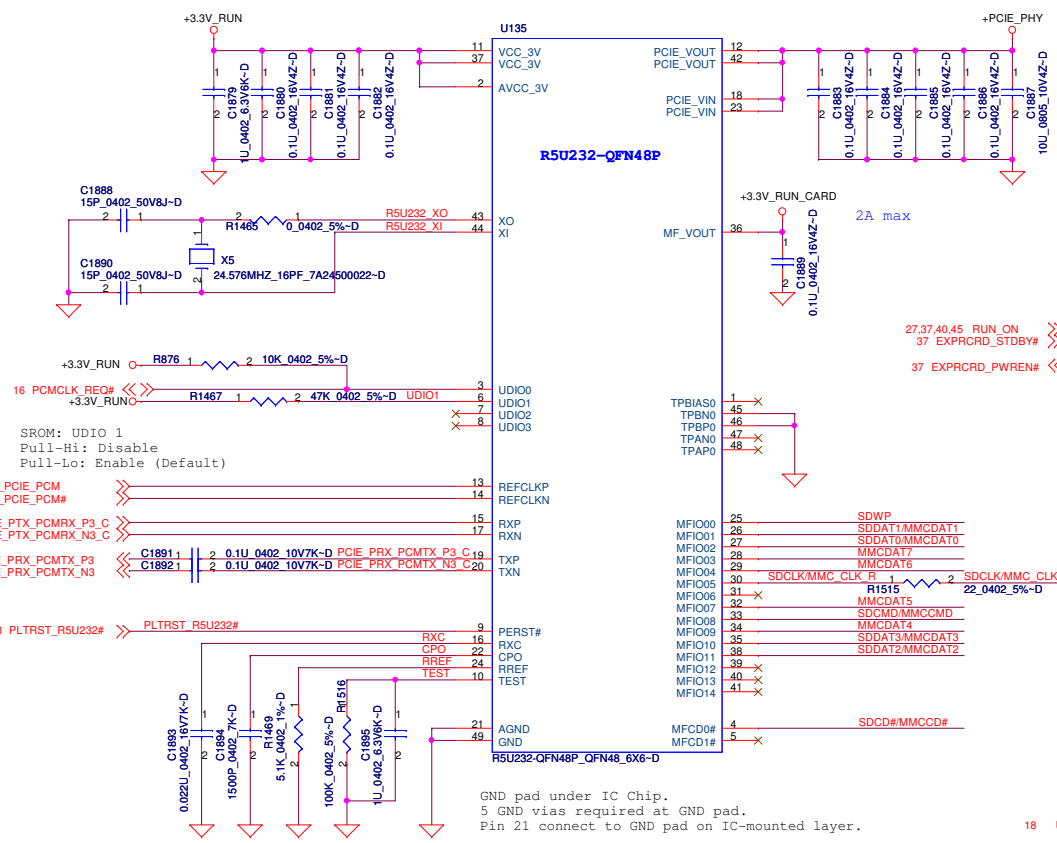




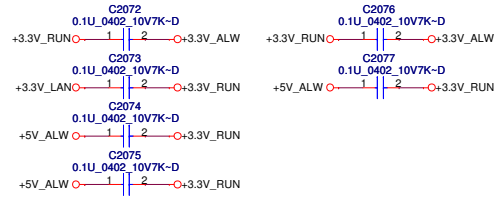




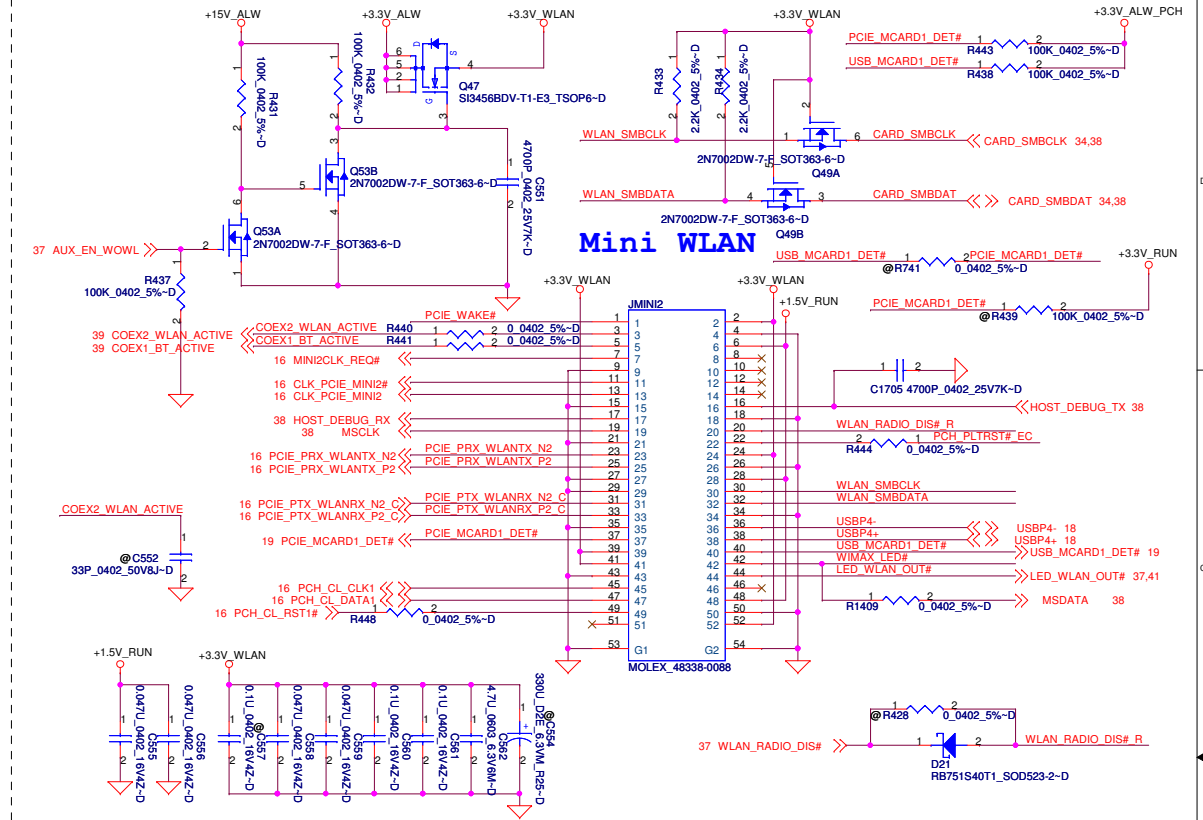




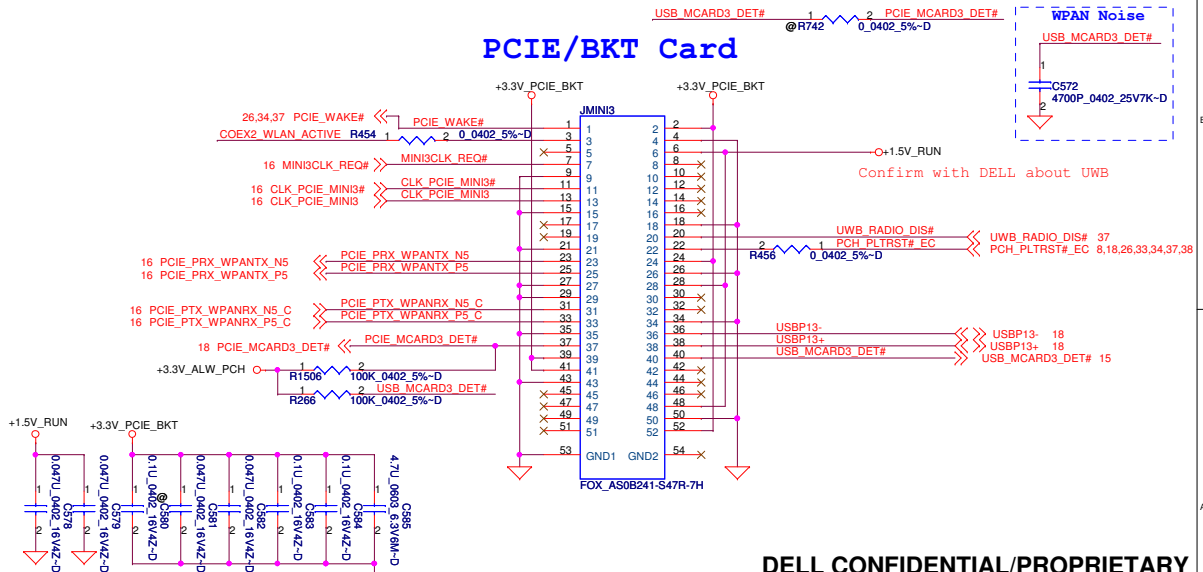
### Stitching caps for MDI



### Stitching caps for PCIe6



### PCIe/BKT Card



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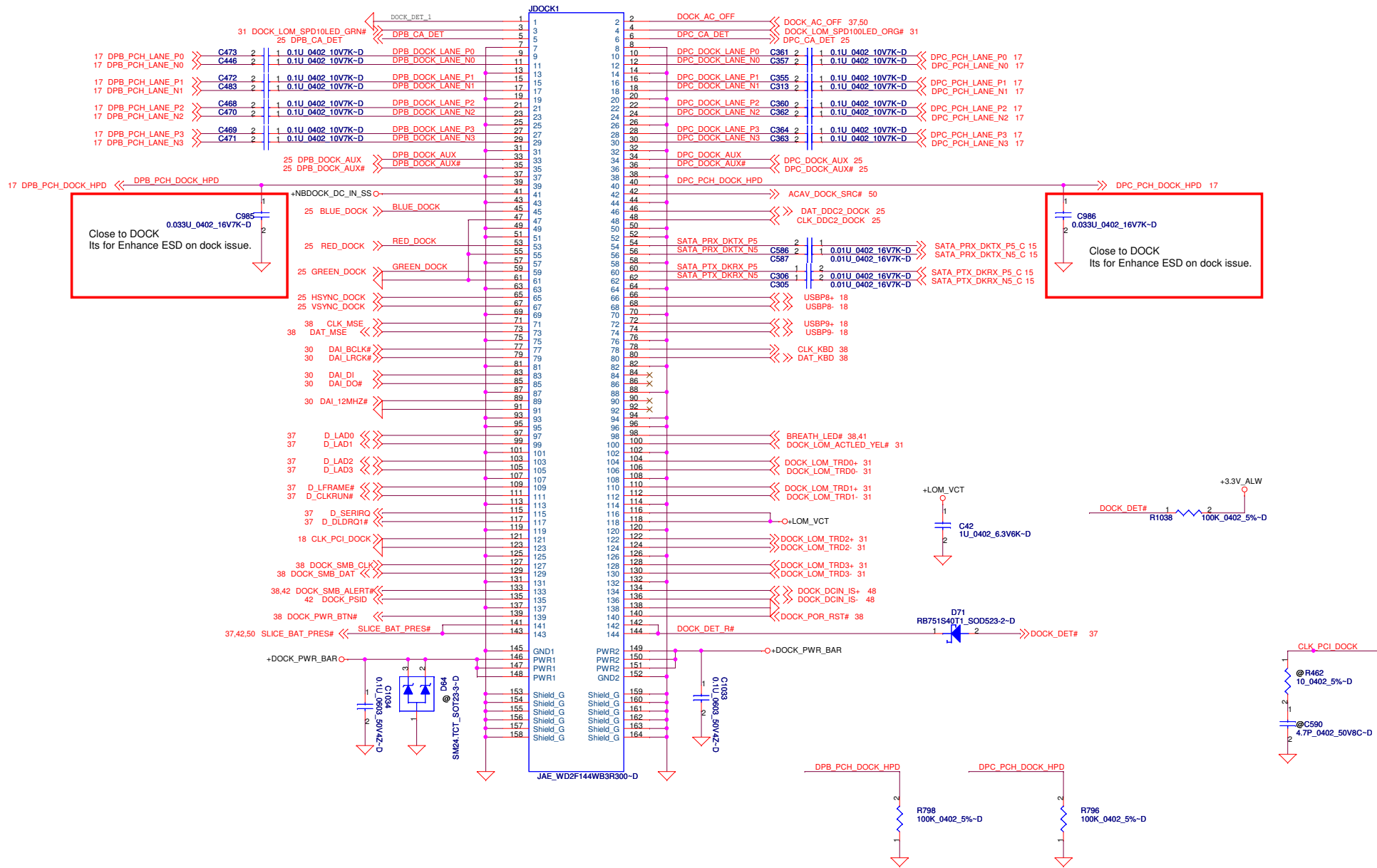
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Mini Card

LA-5691P

Monday, July 13, 2008 Sheet 35 of 51



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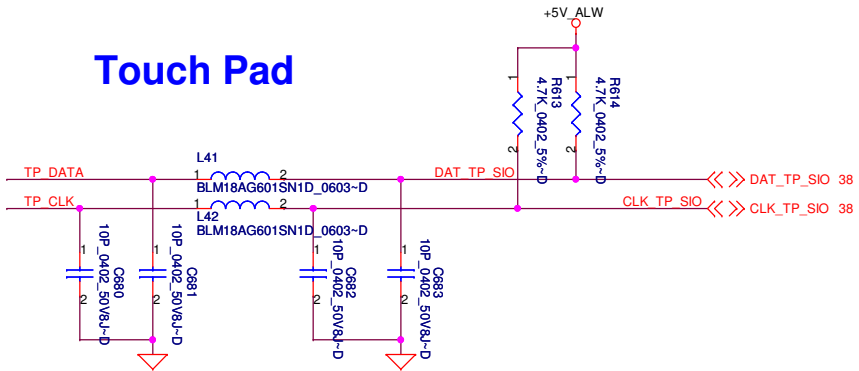
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<b>DOCKING CONN</b>			
<b>LA-5691P</b>			
Size	Document Number	Rev	0.1
Date:	Monday, July 13, 2009	Sheet	36 of 51



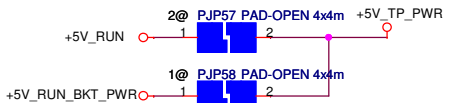
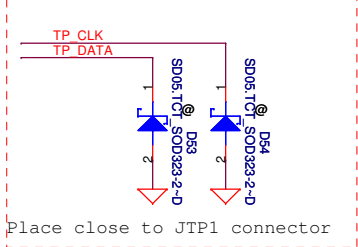
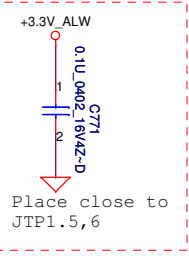
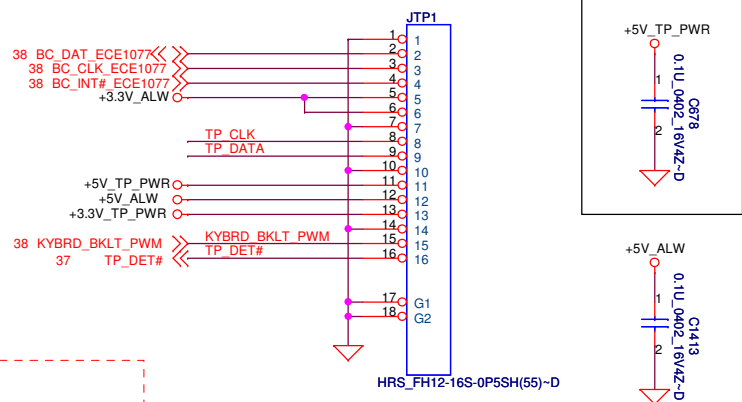




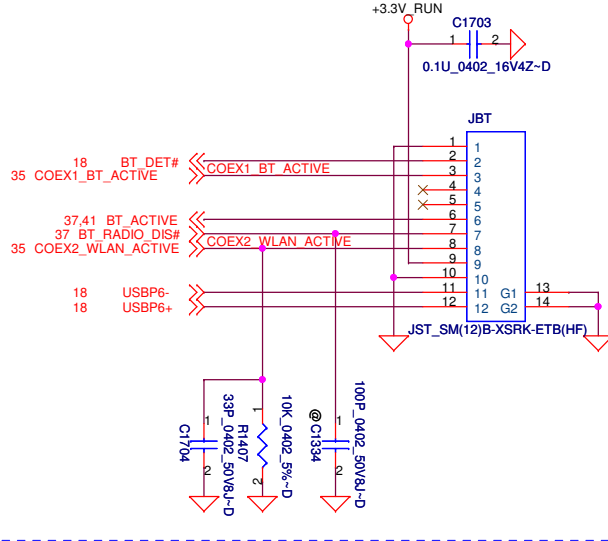
# Touch Pad



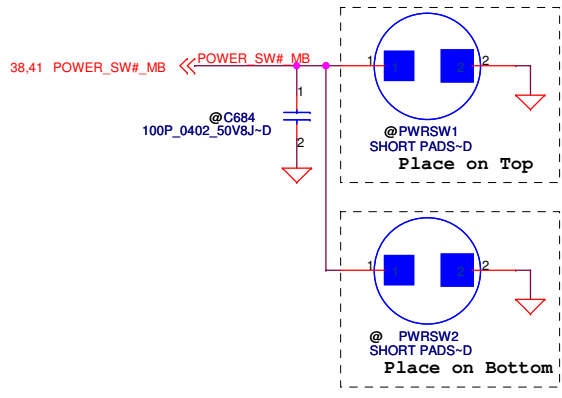
# New Keyboard connector assignment



# BlueTooth



# Power Switch for debug



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**@FAN**

Part Number	Description
DC28A000800	FAN SET DAQ20 DC5V AB7405HB-HB3 ADDA

**@Speak**

Part Number	Description
PK230003Q0L	SPK PACK ZJX 2.0W 4 OHM FG

**@SM CARD BODY**

Part Number	Description
SP070007V0L	\$ SOCKET TYCO 1770551-1 10P H5.9 SMART

**@PCMCIA BODY**

Part Number	Description
DC000001Q0L	PCMCIA TYCO 1759096-1

**@MDC wire set cable**

Part Number	Description
DC02000CS0L	H-CONN SET 2GX MB-MDC

**@T/P wire set cable**

Part Number	Description
DC02000840L	H-CONN SET ZJX MB-B/T-TP-FP

**@LVDS cable**

Part Number	Description
DC020003Y0L	H-CONN SET ZJX MB-LCD 14 WXGA+(-1ch)

**@LVDS cable**

Part Number	Description
DC02000870L	H-CONN SET ZJX MB-LCD 14 WXGA+(-2ch)

**@RTC BATT**

Part Number	Description
GC20323MX00	BATT CR2032 3V 220MAH MAXELL

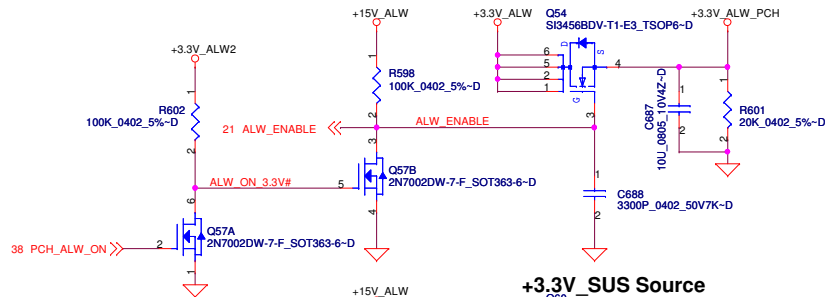
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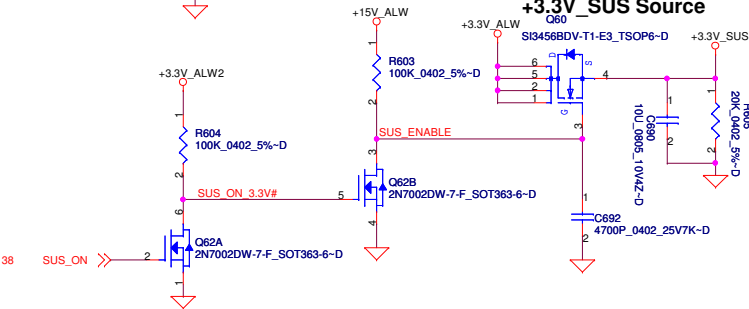
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<b>Title</b> Touch PAD/Int KB/LID		
<b>Size</b>	<b>Document Number</b> LA-5691P	<b>Rev</b> 0.1
<b>Date:</b> Monday, July 13, 2009	<b>Sheet</b> 39	<b>of</b> 51

# DC/DC Interface

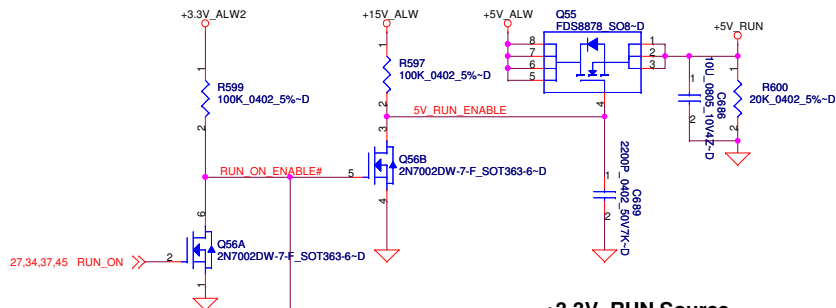
## +3.3V\_ALW\_PCH Source



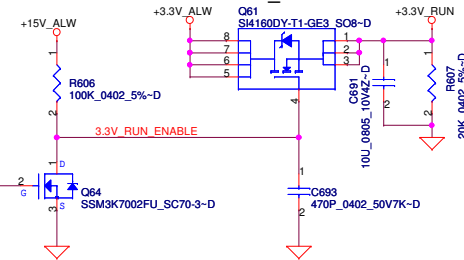
## +3.3V\_SUS Source



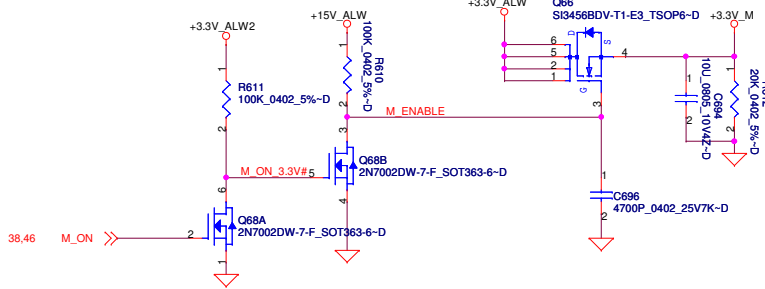
## +5VRUN Source



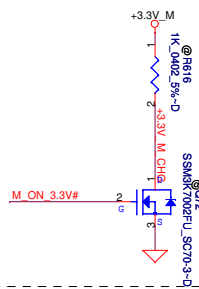
## +3.3V\_RUN Source



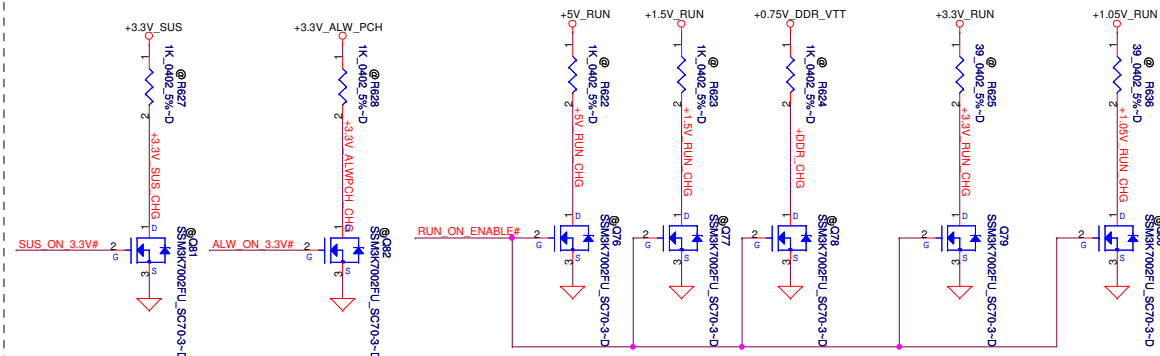
## +3.3VM Source



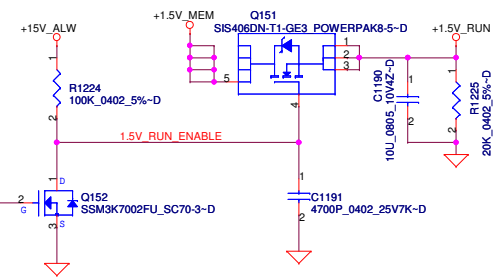
## Discharg Circuit



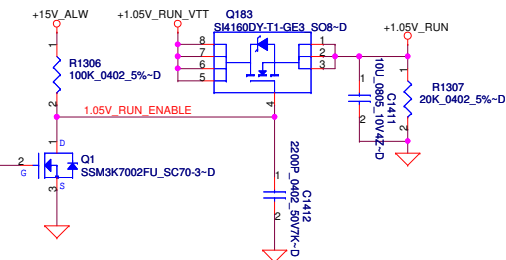
## Discharg Circuit



## +1.5V\_RUN Source



## +1.05V\_RUN Source



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POWER CONTROL

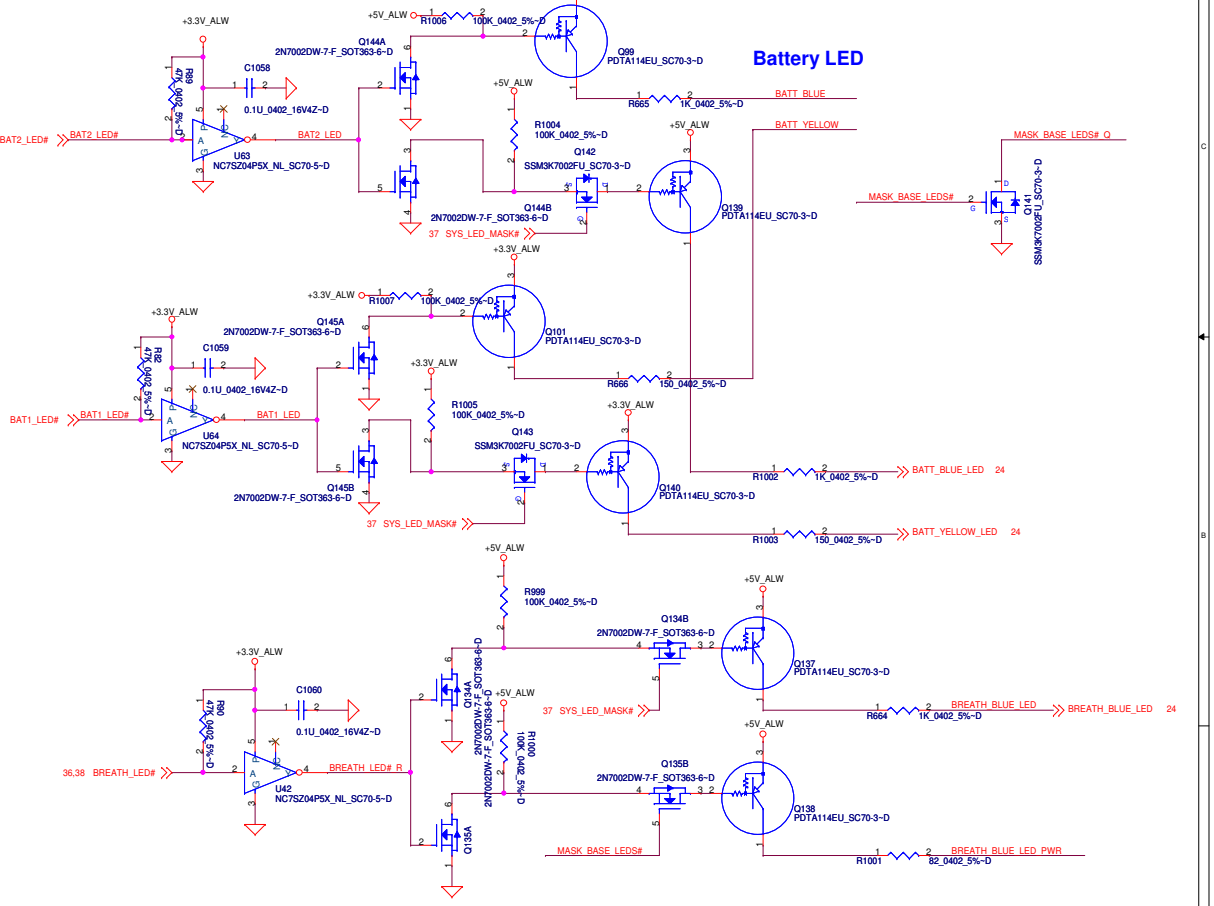
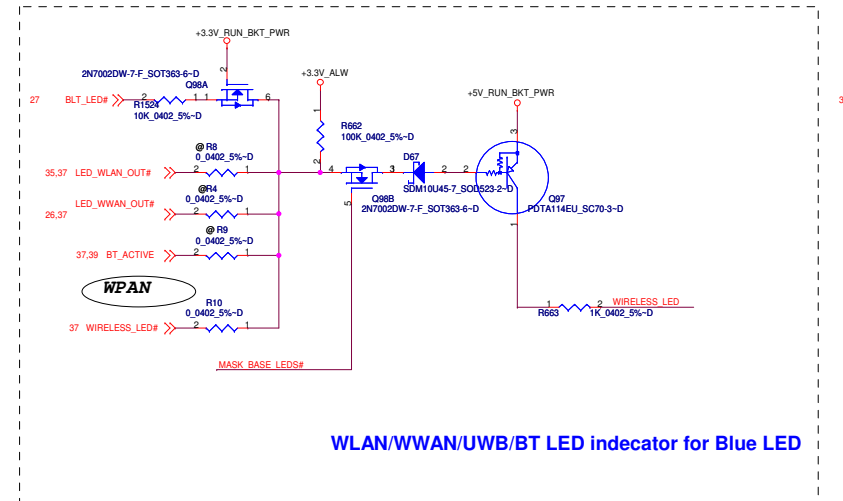
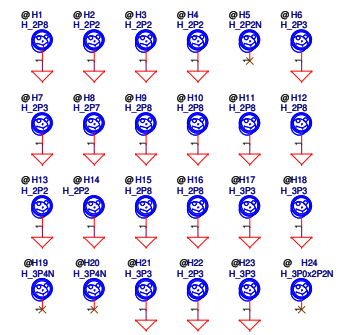
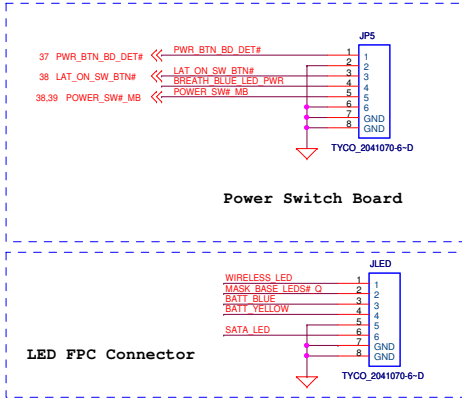
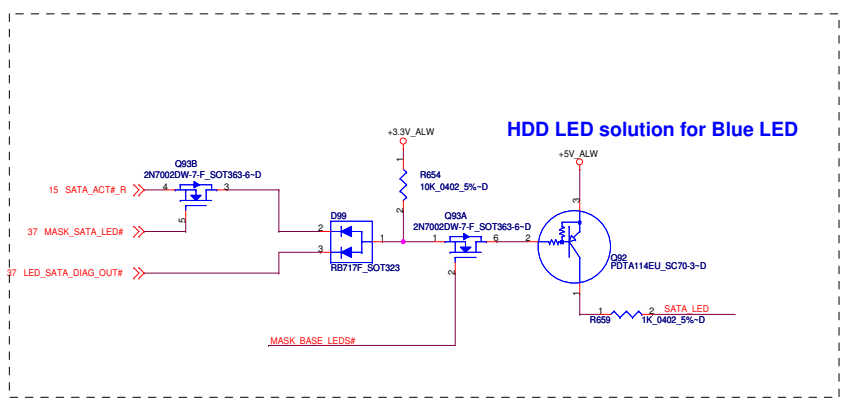
LA-5691P

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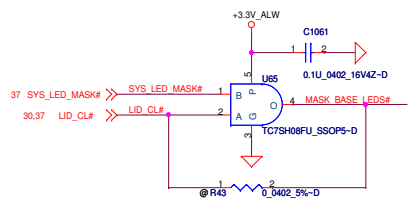


Size	Document Number	Rev
	LA-5691P	0.1
Date:	Monday, July 13, 2008	Sheet 40 of 51





LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



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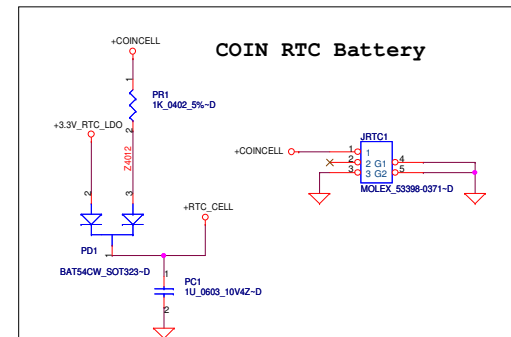
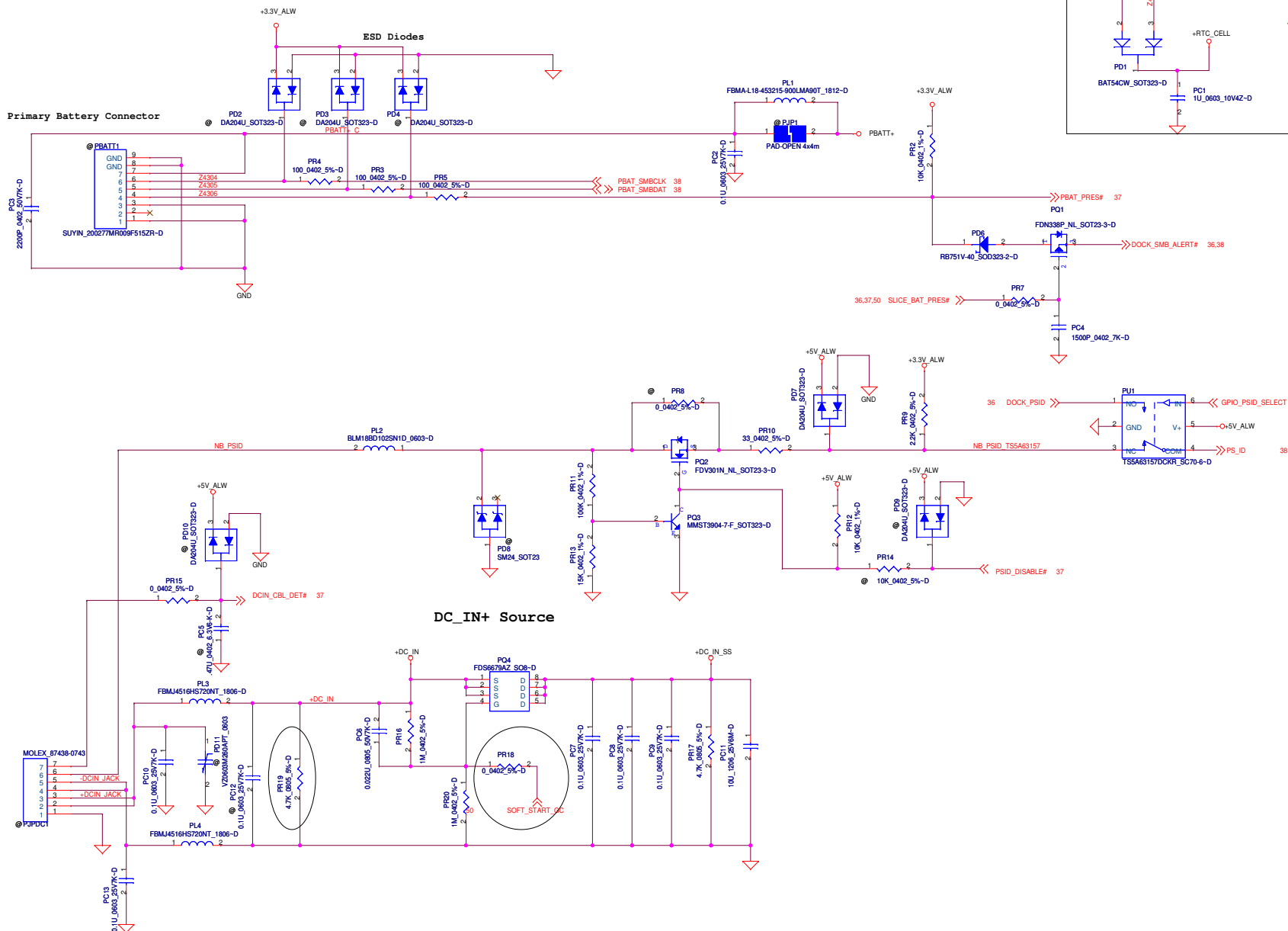
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**PAD and Standoff**

**LA-5691P**

Date: Monday, July 13, 2009 Sheet 41 of 51



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Title  
**+DCIN**

Size	Document Number <b>LA-5691P</b>	Rev 0.1
Date	Monday, July 13, 2009	Sheet 42 of 51

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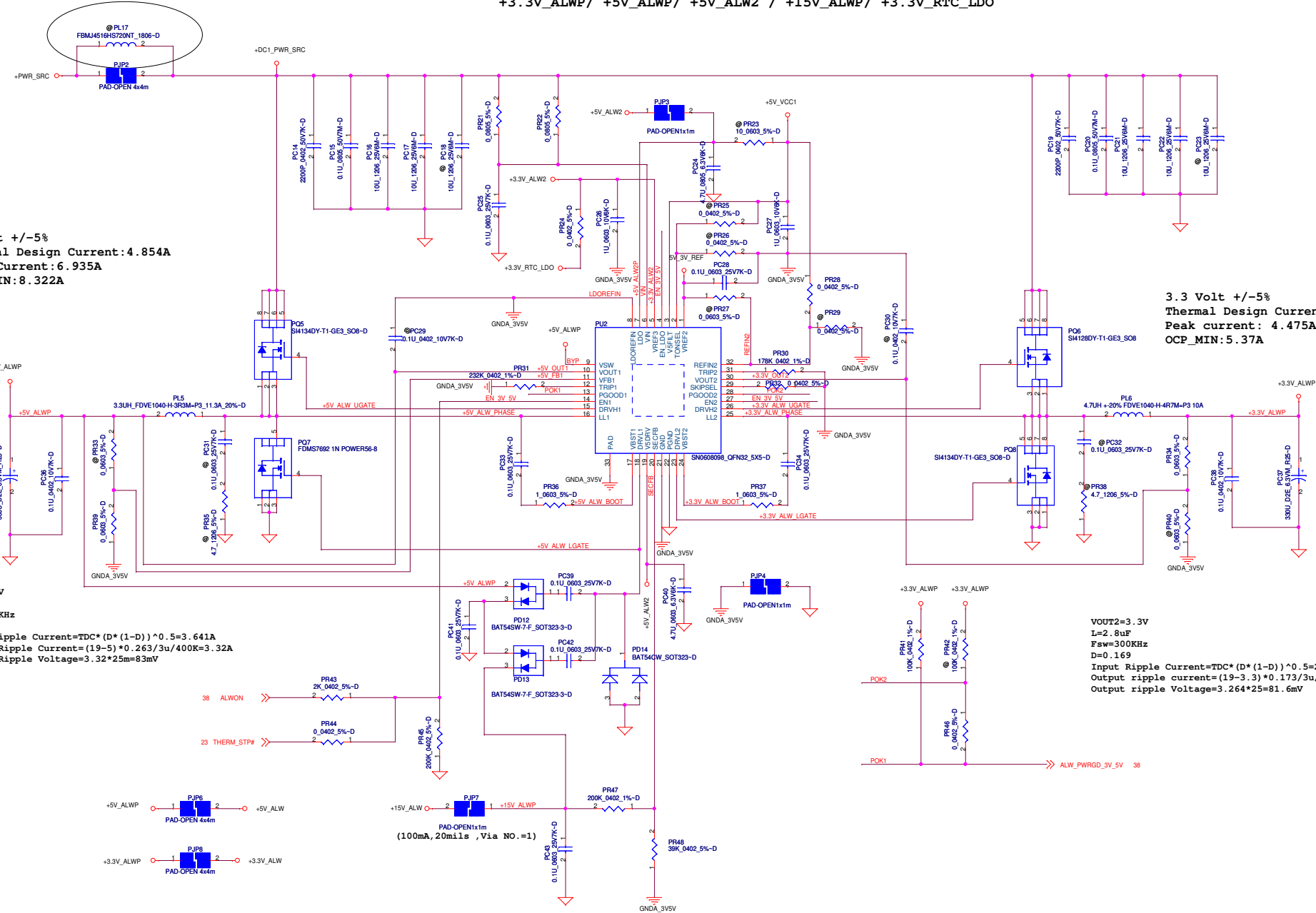
**+3.3V\_ALWP/ +5V\_ALWP/ +5V\_ALW2 / +15V\_ALWP/ +3.3V\_RTC\_LDO**

5 Volt +/-5%  
 Thermal Design Current: 4.854A  
 Peak Current: 6.935A  
 OCP\_MIN: 8.322A


3.3 Volt +/-5%  
 Thermal Design Current: 3.133A  
 Peak current: 4.475A  
 OCP\_MIN: 5.37A

VOUT2=5V  
 L=2.8uF  
 Fsw=400KHz  
 D=0.256  
 Input Ripple Current=TDC\*(D\*(1-D))^0.5=3.641A  
 Output Ripple Current=(19-5)\*0.263/3u/400K=3.32A  
 Output Ripple Voltage=3.32\*25m=83mV

VOUT2=3.3V  
 L=2.8uF  
 Fsw=300KHz  
 D=0.169  
 Input Ripple Current=TDC\*(D\*(1-D))^0.5=2.051A  
 Output ripple current=(19-3.3)\*0.173/3u/300K=3.264A  
 Output ripple Voltage=3.264\*25=81.6mV

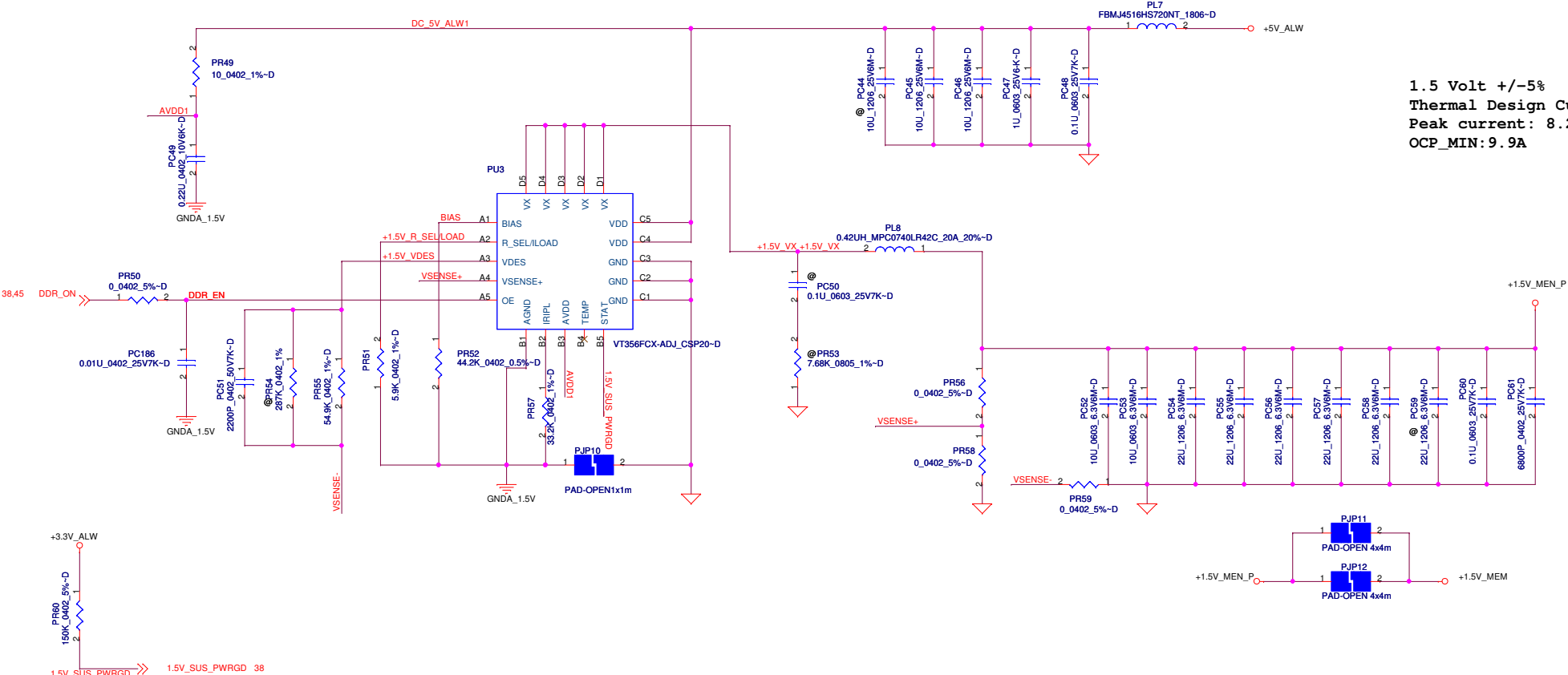


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Size	Document Number	LA-5691P	
Date: Monday, July 13, 2008	Sheet	43	of 51

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# +1.5V\_MEN\_P (VT356)



1.5 Volt +/-5%  
 Thermal Design Current: 5.775A  
 Peak current: 8.25A  
 OCP\_MIN: 9.9A

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**Compal Electronics, Inc.**

Title: **+1.5V\_MEM**

Size: **LA-5691P**

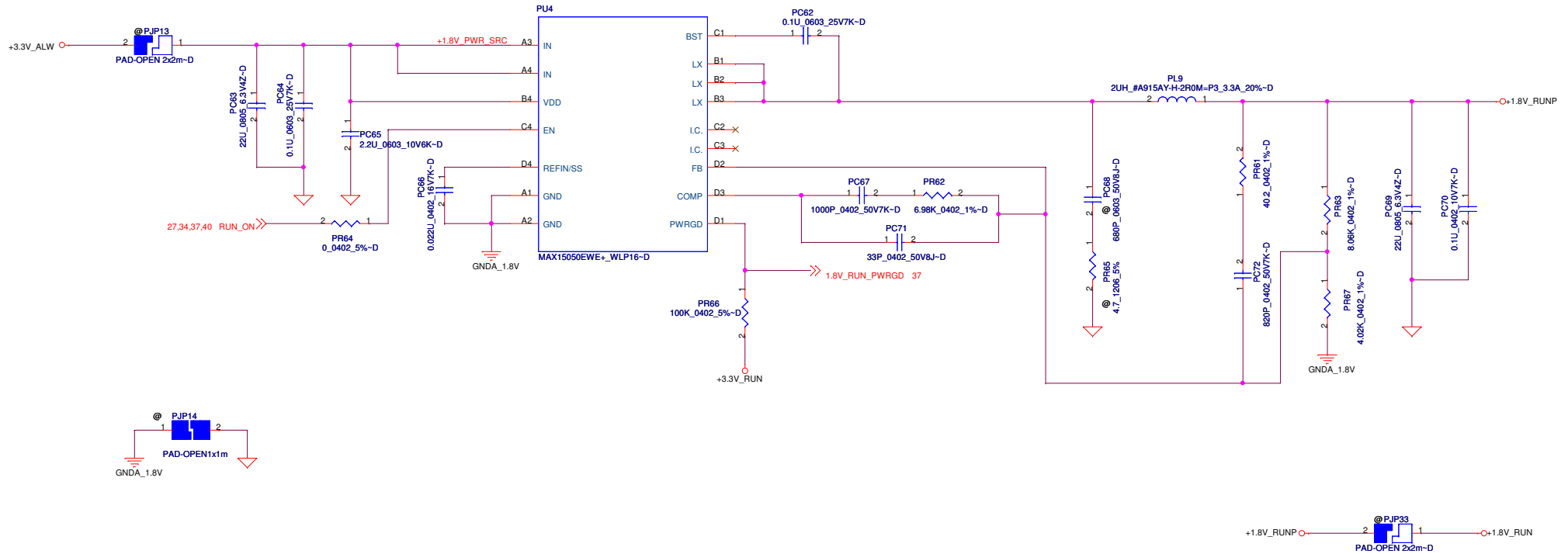
Date: Monday, July 13, 2009

Sheet 44 of 51

Rev 0.1

# +1.8V\_RUN

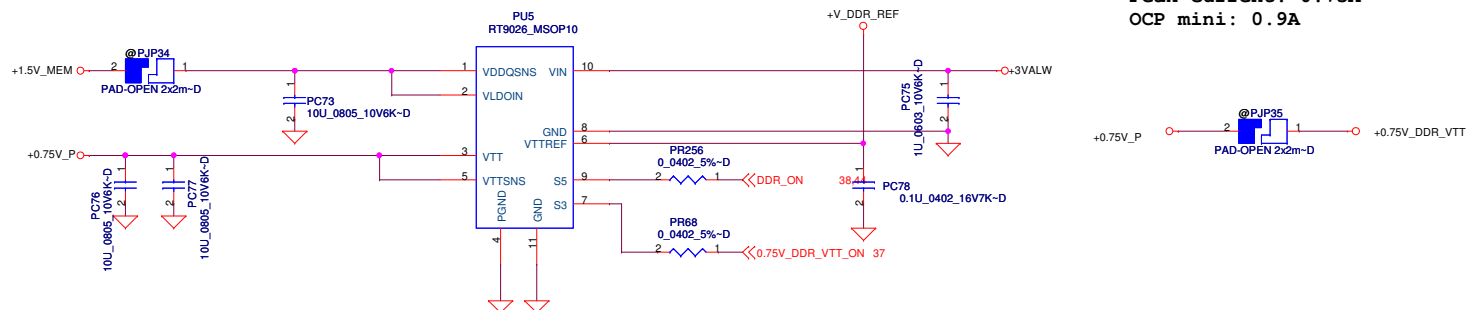
1.8 Volt +/-5%  
 Thermal Design Current: 0.894A  
 Peak current: 1.277A  
 OCP\_min:1.532A



# +0.75V\_DDR\_VTT

DDR3 Termination

0.75Volt +/-5%  
 Thermal Design Current: 0.525A  
 Peak current: 0.75A  
 OCP mini: 0.9A



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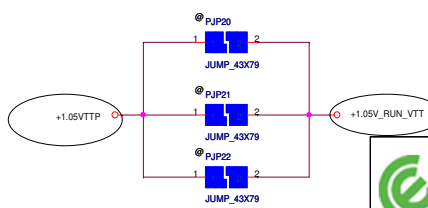
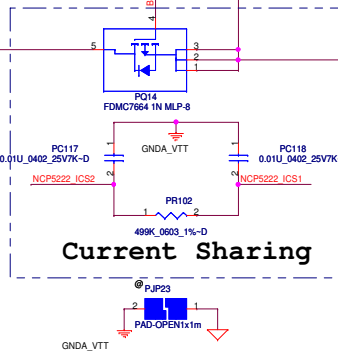
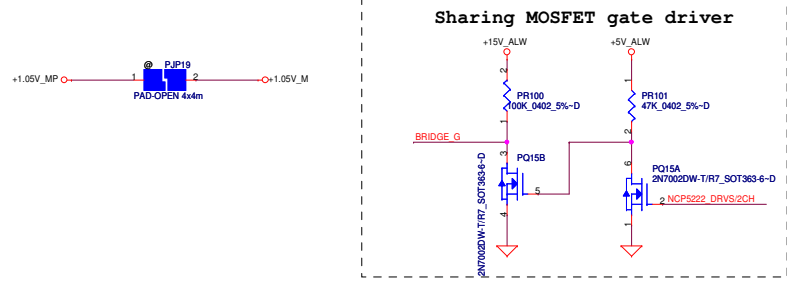
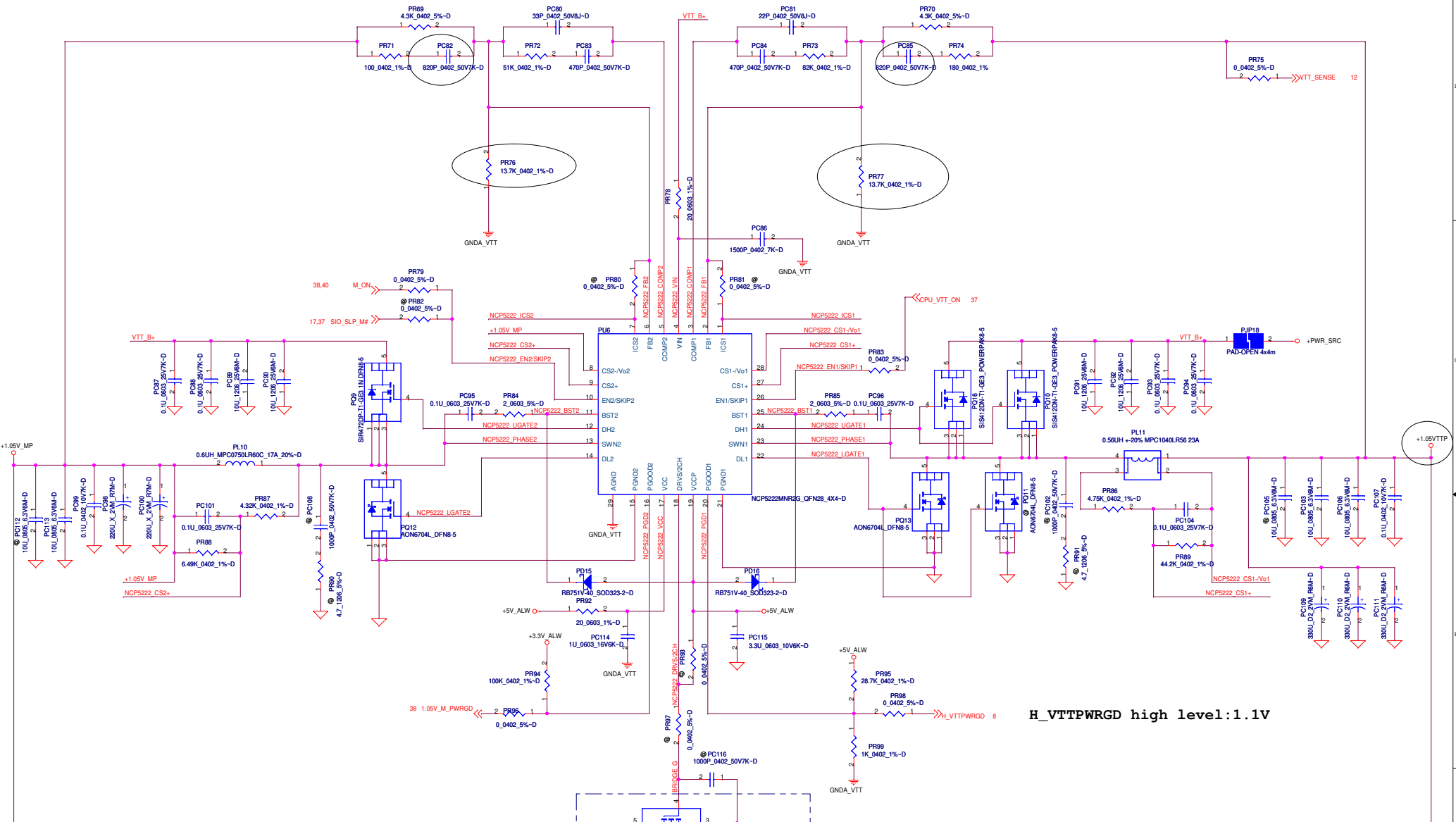
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<b>Compal Electronics, Inc.</b>			
<b>+1.8V_RUN/+0.75V_DDR_VT</b>			
<b>LA-5691P</b>			
Size	Document Number	Rev	
		0.1	
Date:	Monday, July 13, 2009	Sheet	45 of 51


1.05 Volt +/-5%  
 Thermal Design Current: 1.51A  
 Peak current: 2.17A

**+1.05V\_M/+1.05VTT\_RUN**

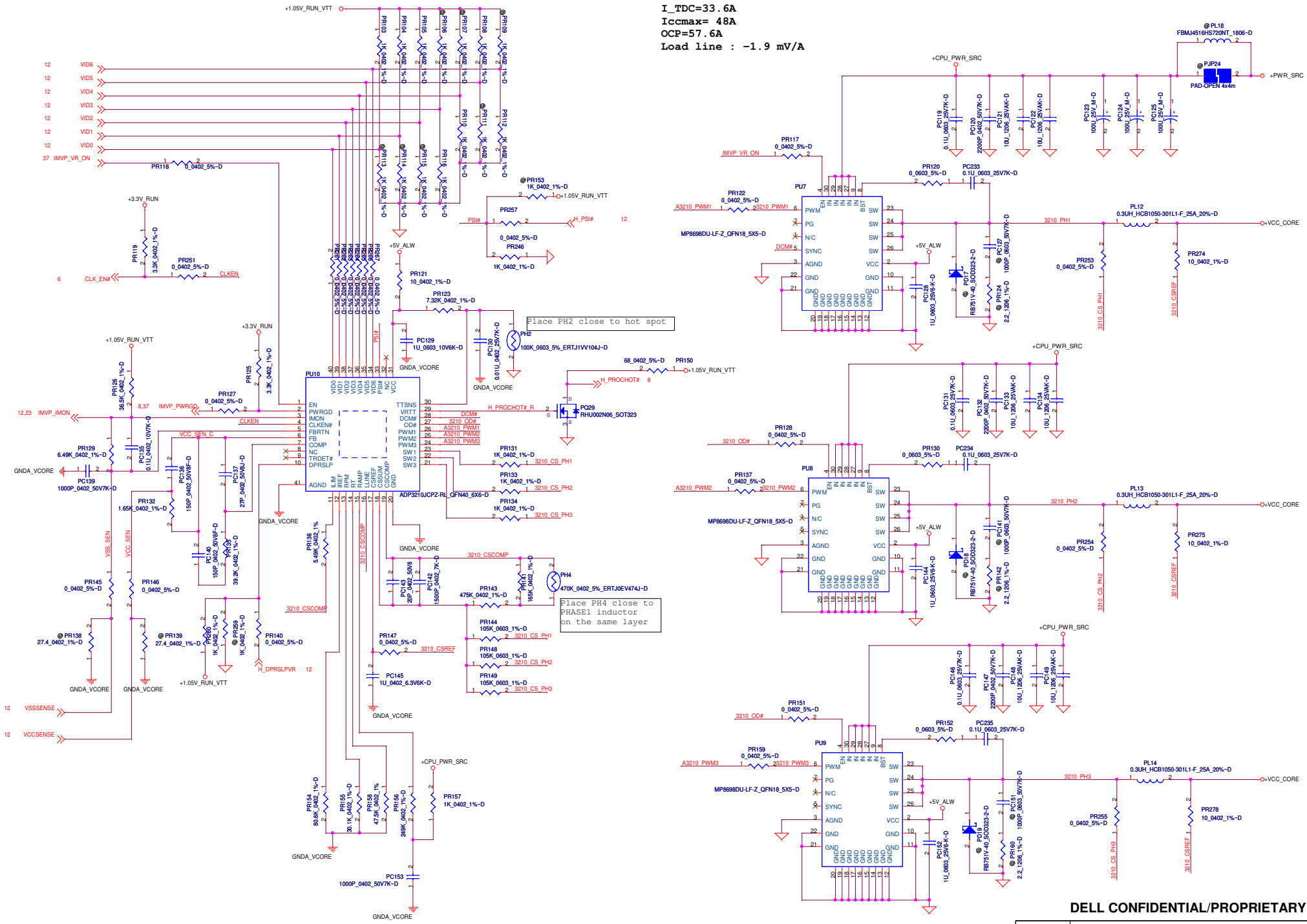
1.05 Volt +/-5%  
 Thermal Design Current: 15.9A  
 Peak current: 22.7A



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		<b>+1.05V_M/+1.05V_RUN_VTT</b>	
File	Document Number	Rev	0.1
<b>LA-5691P</b>		Date	Monday, July 13, 2009
Sheet	46	of	51

I\_TDC=33.6A  
 Iccmax= 48A  
 OCP=57.6A  
 Load line : -1.9 mV/A

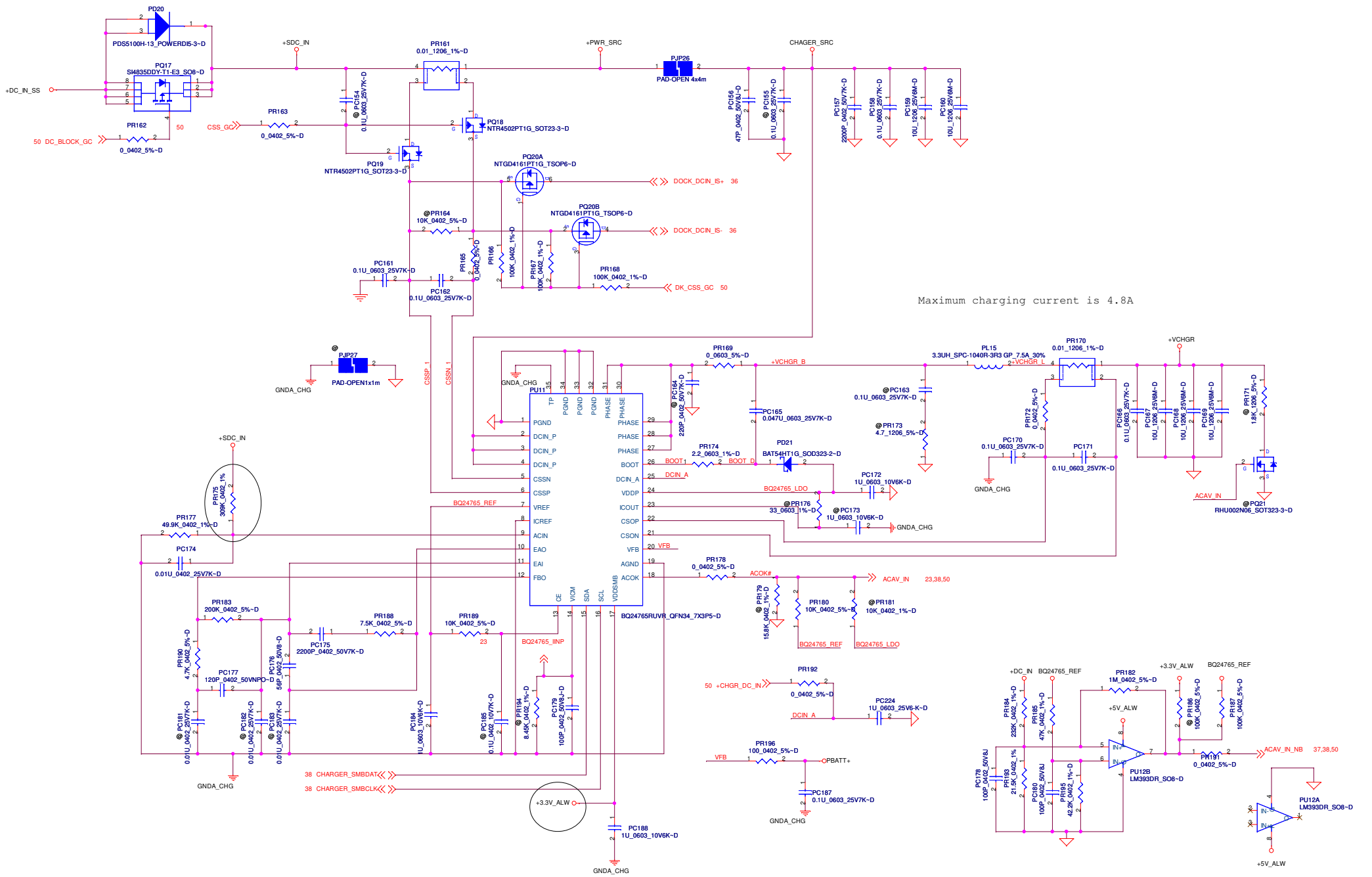


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		<b>+VCC CORE</b>	
Size	Document Number	<b>LA-5691P</b>	
Date: Monday, July 13, 2009	Sheet	47	of 51





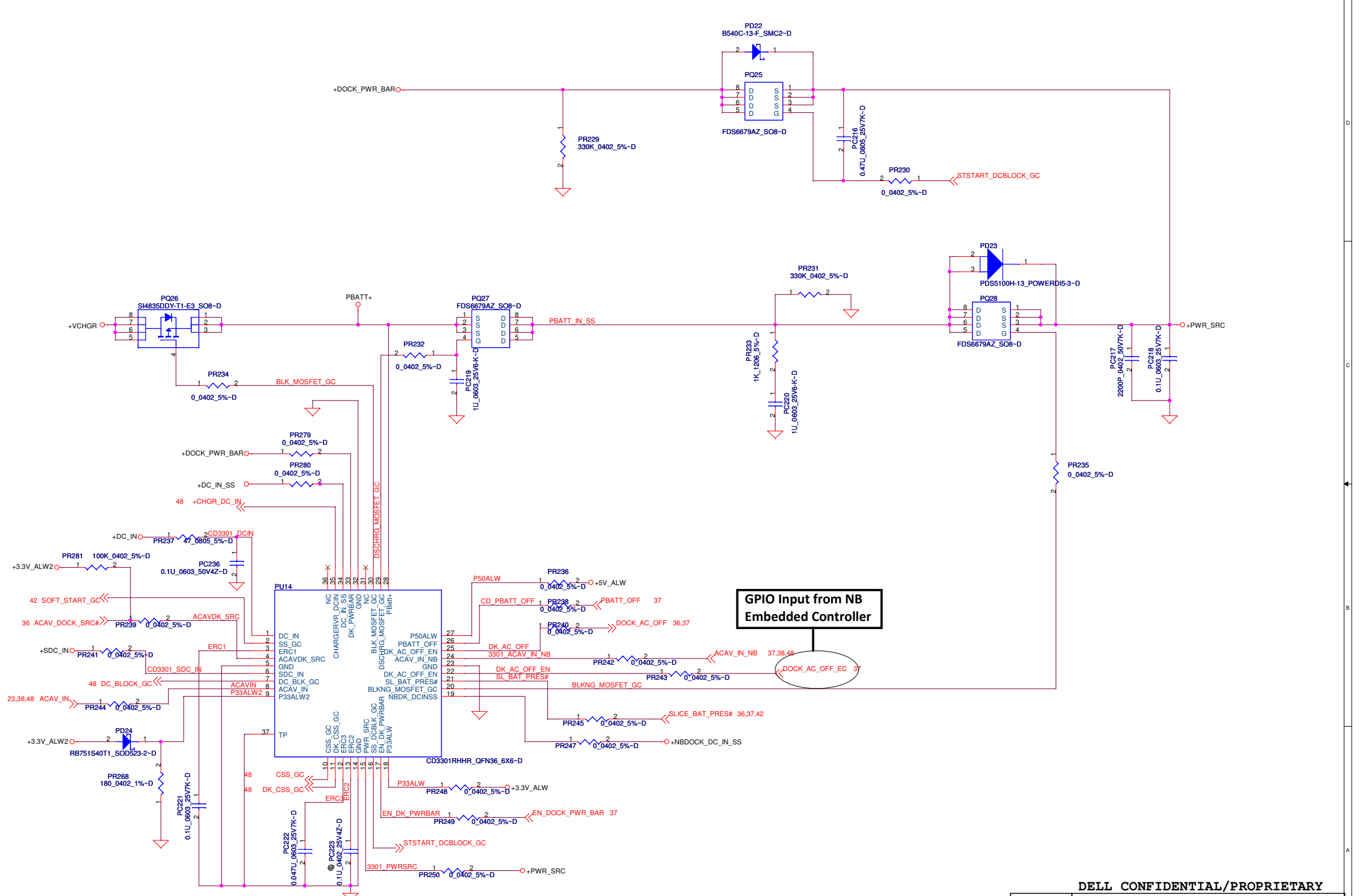
Maximum charging current is 4.8A

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			<b>Charger</b>	
Size	Document Number	Rev		0.1
Date: Monday, July 13, 2009		Sheet	48	of 51

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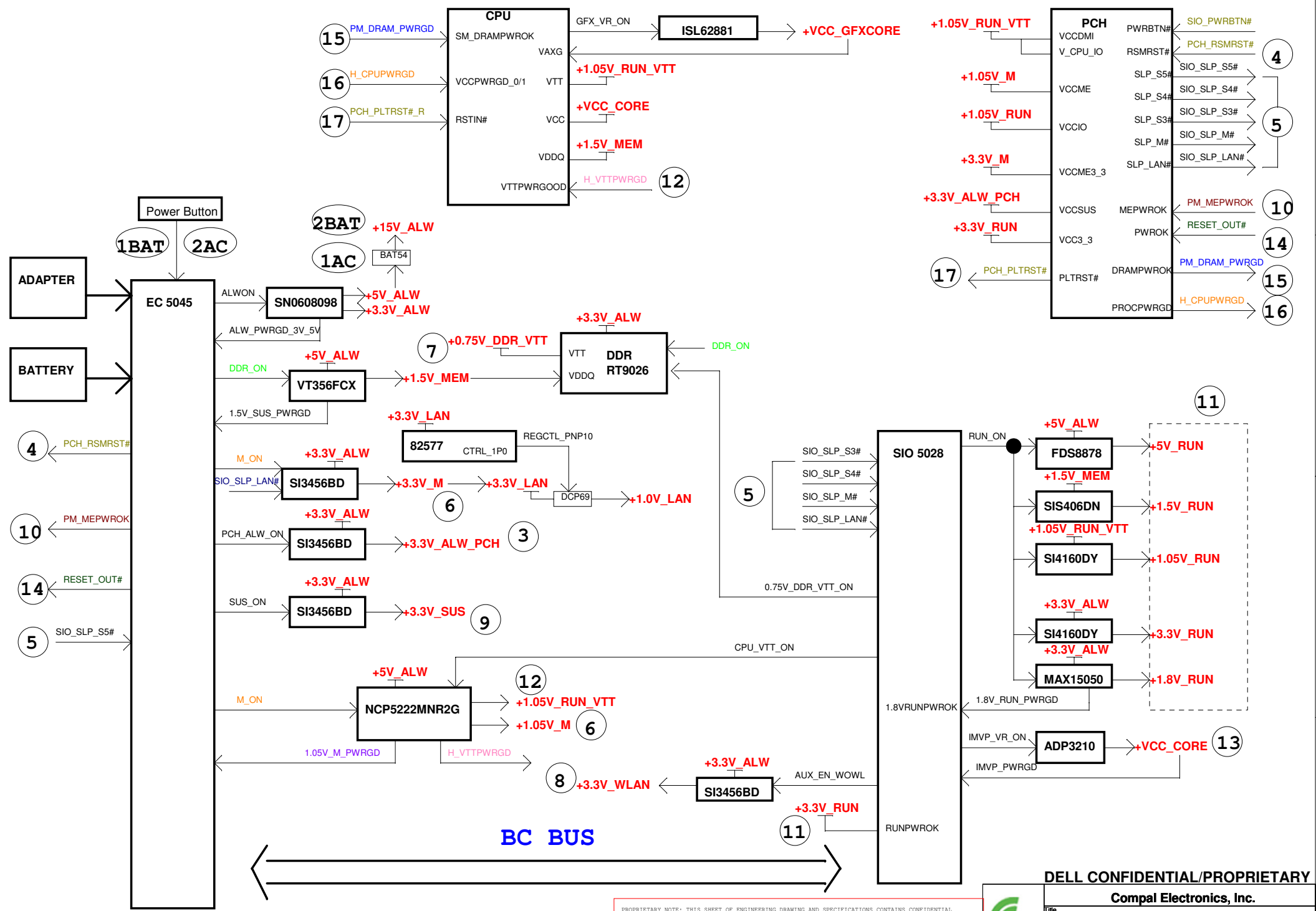
GPIO Input from NB Embedded Controller

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Size	Document Number	<b>LA-5691P</b>	
Date:	Monday, July 13, 2009	Sheet	50 of 51

Rev 0.1



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Title		Power Sequence	
Size	Document Number	Rev	
	LA-5691P	0.1	
Date:	Monday, July 13, 2009	Sheet	51 of 51