

# COMPAL CONFIDENTIAL

MODEL NAME : *NAL22/23/24*

PCB NO : *LA-5573P (DAA00001G00)*

BOM P/N : *43177531LXX*

## M10 Margaux DIS/ASICS rPGA Auburndale/Clarksville +FCBGA PCH IBEXPEAK-M + N10M-NS-B/N10P-GLM/N10P-GLM4

2010-01-21

REV : 1.0(A00)

@ : Nopop Component

7@ : N10P-GLM VID

8@ : N10M-NS-B & N10P-GLM4 VID

9@ : N10P-GLM4 only

MB Type	BOM P/N	Asics DIS N10P		Margaux DIS N10M		TCM		TPM		BOM CONFIG
		1@	2@	W(3@)	W/O(4@)	W(5@)	W/O(6@)			
Margaux DIS, TPM EN,TCM DIS	43177531L01		*		*	*				2@, 4@, 5@, 8@
Margaux DIS, TCM EN,TPM DIS	43177531L02		*	*			*			2@, 3@, 6@, 8@
Margaux DIS, ALL TPM DISABLE	43177531L03		*		*		*			2@, 4@, 6@, 8@
Asics GLM, TPM EN,TCM DIS	43177531L11	*			*	*				1@, 4@, 5@, 7@
Asics GLM, TCM EN,TPM DIS	43177531L12	*		*			*			1@, 3@, 6@, 7@
Asics GLM, ALL TPM DISABLE	43177531L13	*			*		*			1@, 4@, 6@, 7@
Asics GLM4, TPM EN,TCM DIS	43177531L21	*			*	*				1@, 4@, 5@, 8@, 9@
Asics GLM4, TCM EN,TPM DIS	43177531L22	*		*			*			1@, 3@, 6@, 8@, 9@
Asics GLM4, ALL TPM DISABLE	43177531L23	*			*		*			1@, 4@, 6@, 8@, 9@

MB PCB	
Part Number	Description
DAA00001G00	PCB 0AH LA-5573P REV0 M/B DIS

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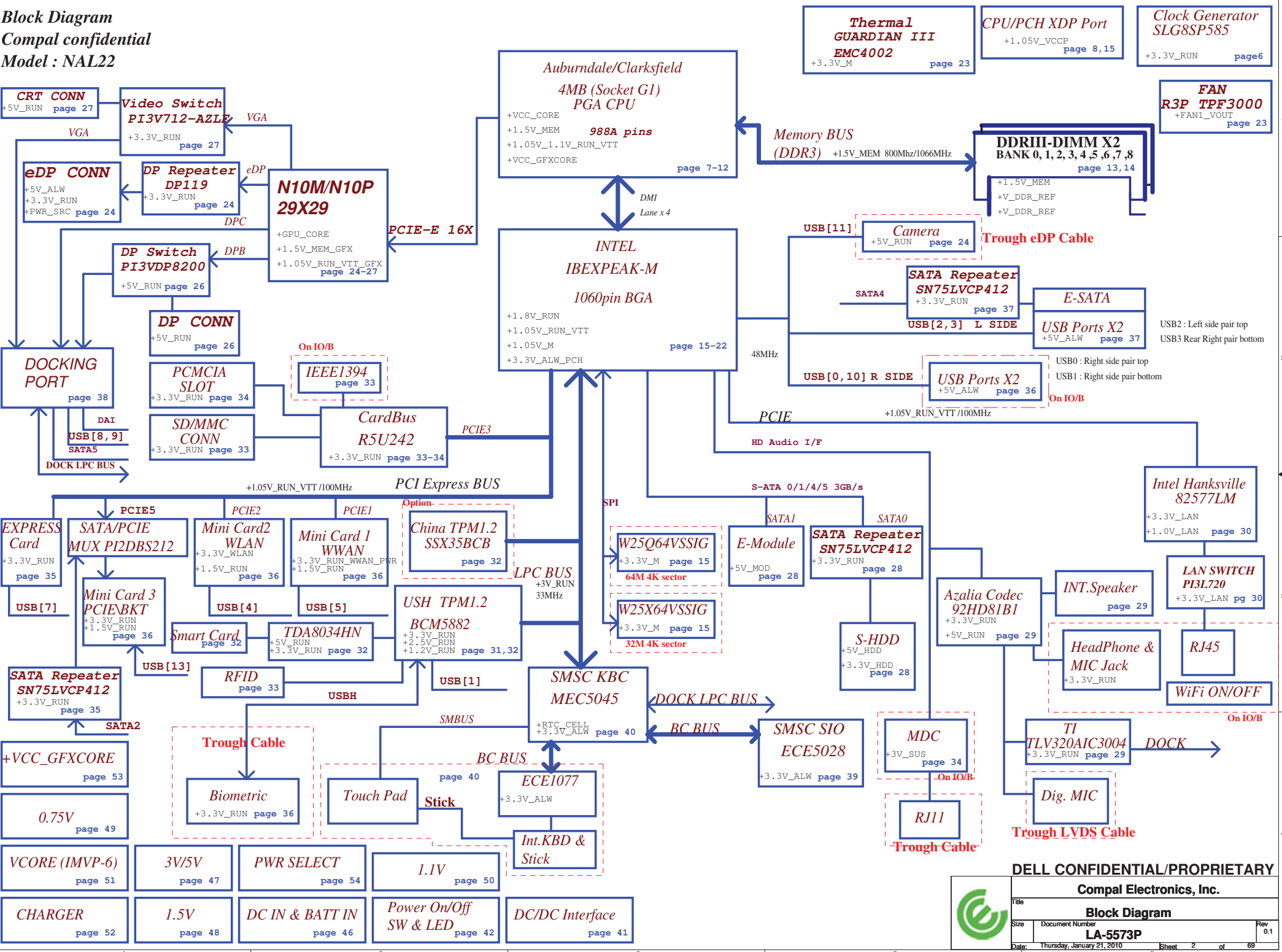
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**Block Diagram**  
 Compal confidential  
 Model : NAL22



**POWER STATES**

State \ Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M1	LOW	LOW	HIGH	LOW	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M1	LOW	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

**PM TABLE**

State \ power plane	+15V_ALW +5V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_CORE +1.05V_RUN_VTT +1.05V_RUN	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

PCH	USB PORT#	DESTINATION
	0	JUSB1 (Ext Right Side Bottom)
	1	JUSB1 (Ext Right Side Top)
	2	JESA1 (Ext Left Side Top)
	3	JESA1 (Ext Left Side Bottom)
	4	WLAN
	5	WWAN
	6	Bluetooth
	7	USH->BIO
	8	DOCKING
	9	DOCKING
	10	Express card
	11	Camera
	12	NA
13	WPAN/NVMHCI	

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	Card Bus
Lane 4	EXPRESS CARD
Lane 5	MINI CARD-3 PCIE/BKT
Lane 6	10/100/1G LAN
Lane 7	None
Lane 8	None

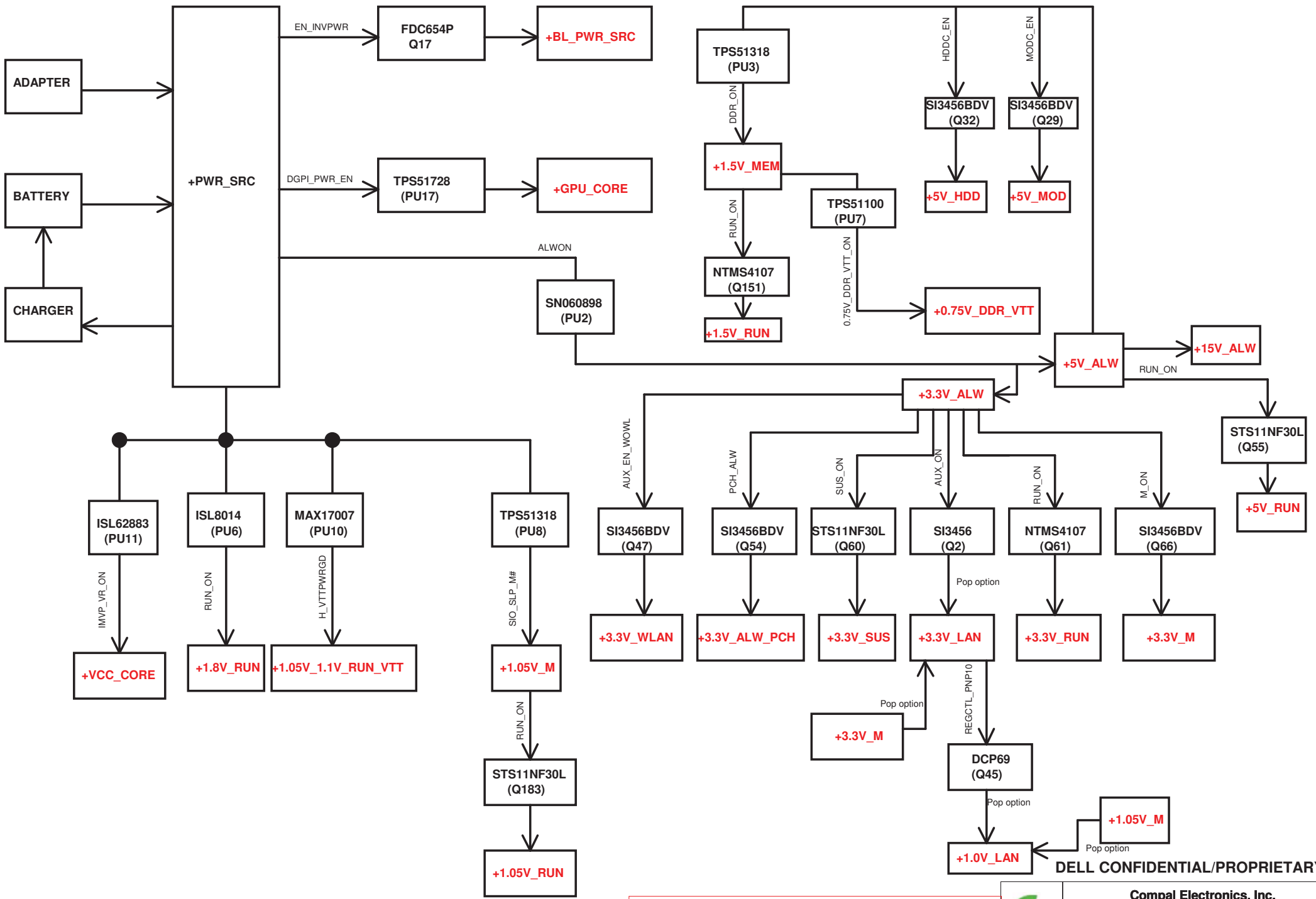
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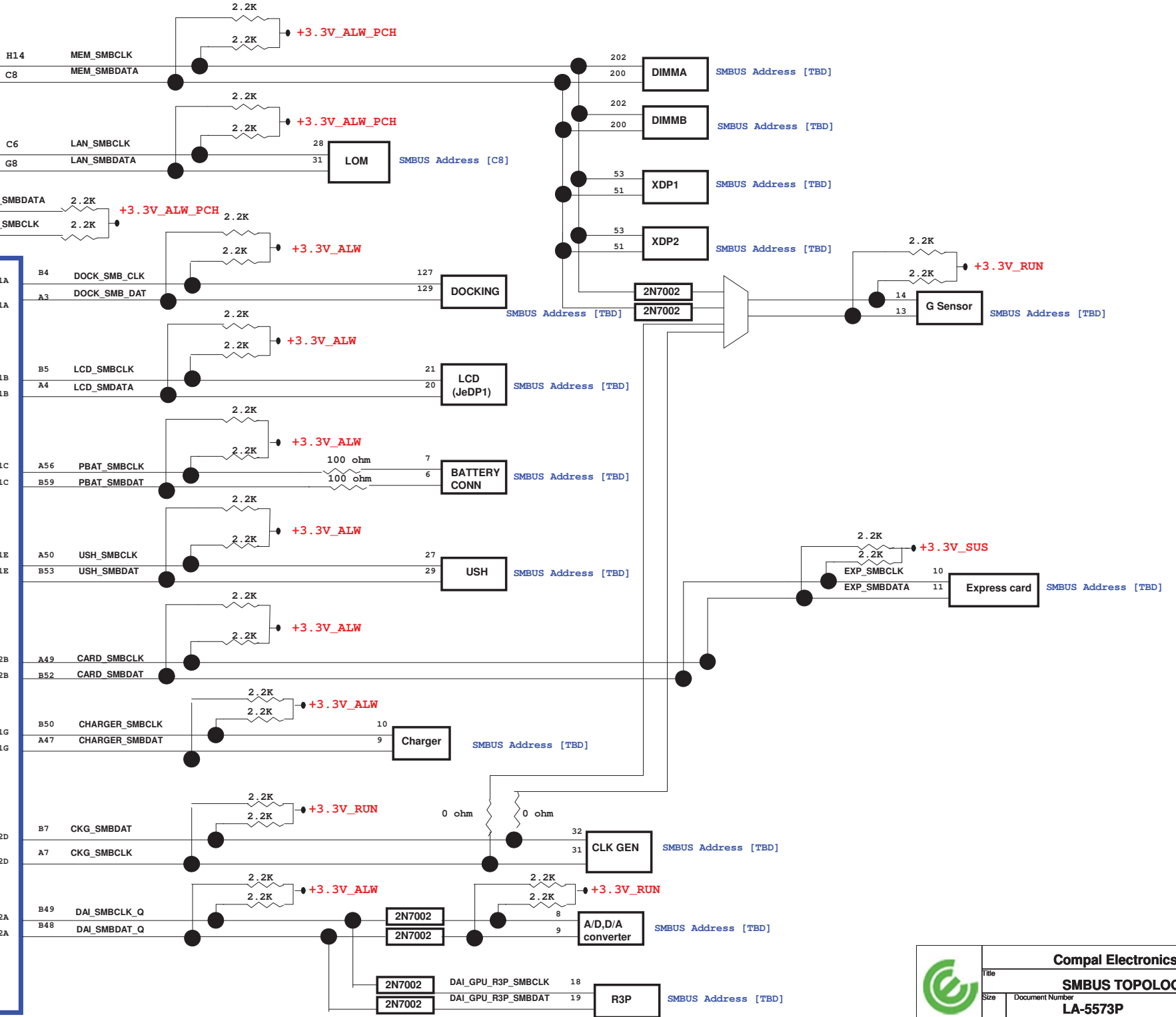
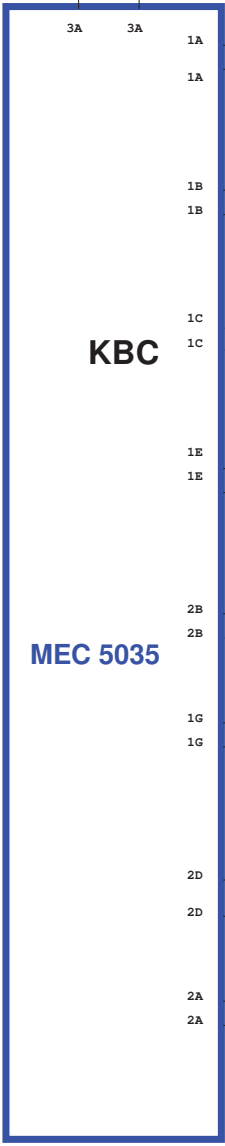
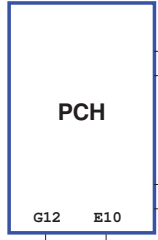


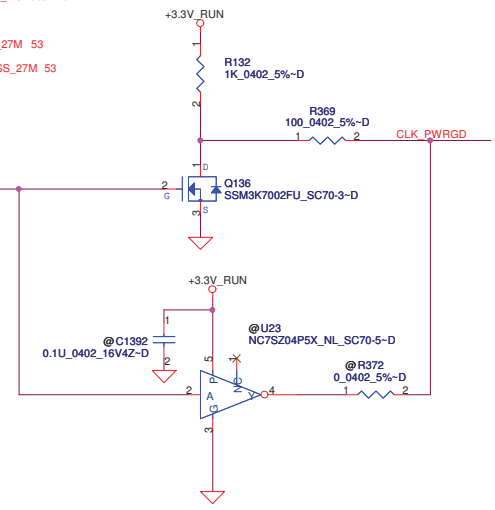
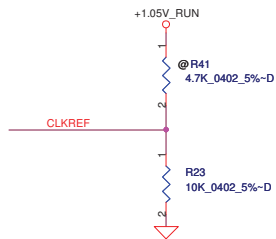
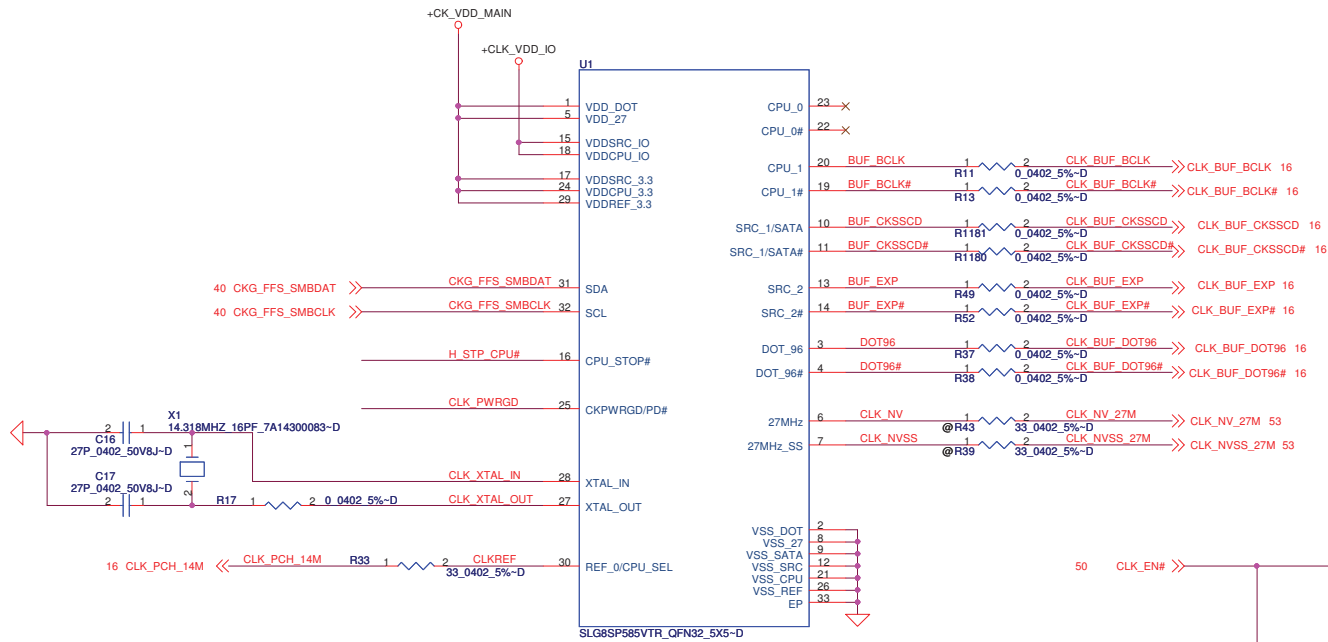
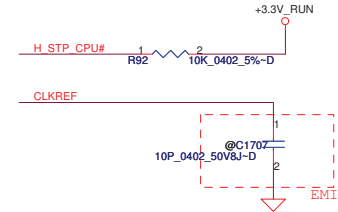
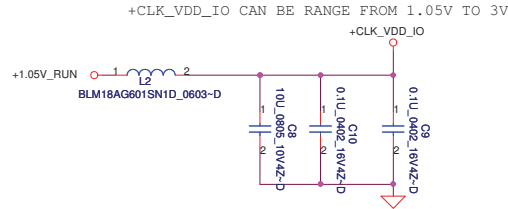
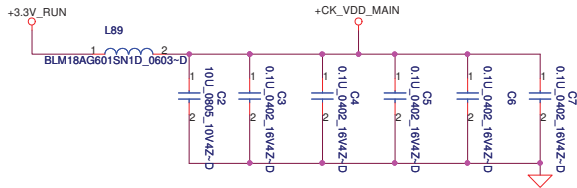
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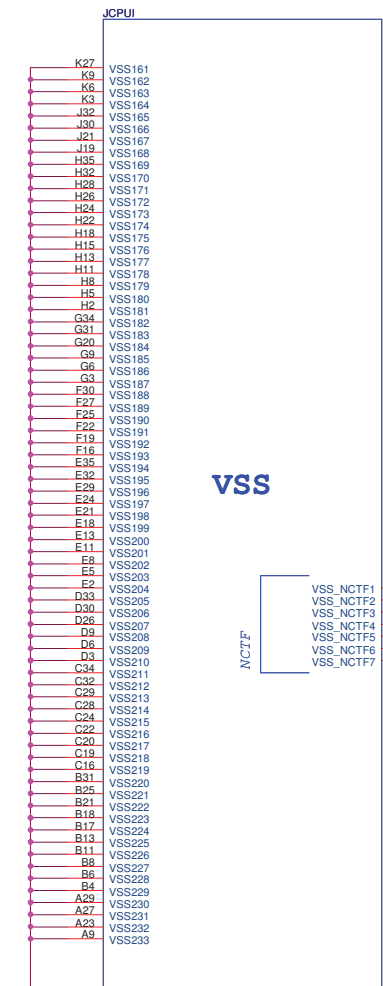
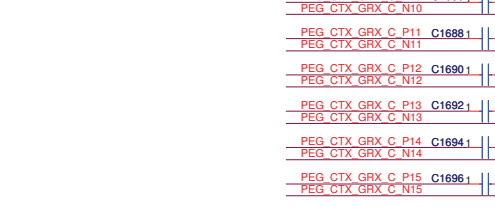
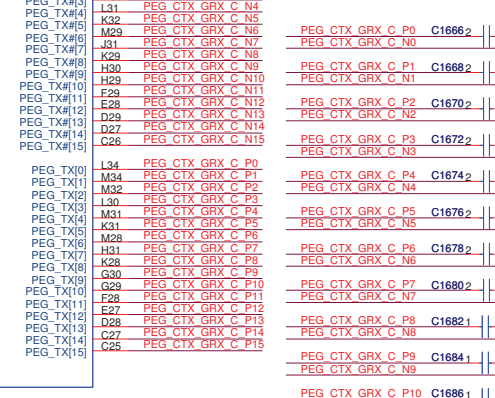
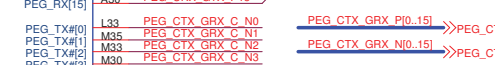
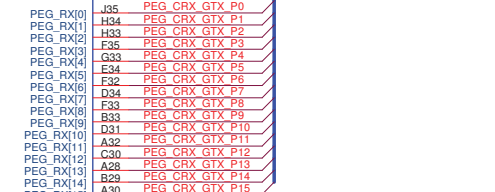
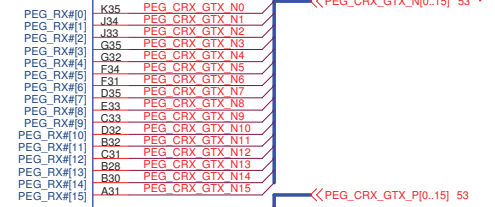
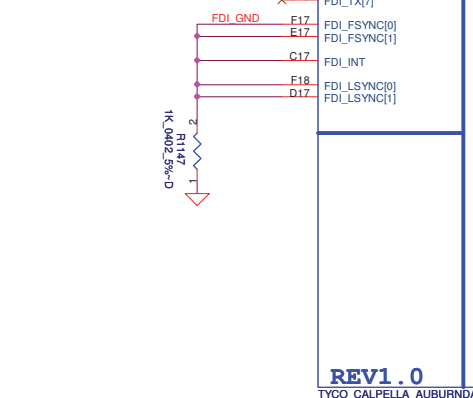
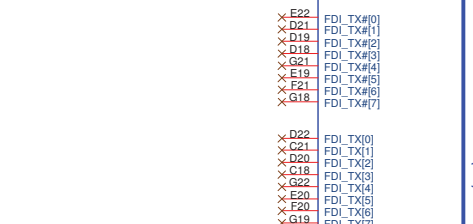
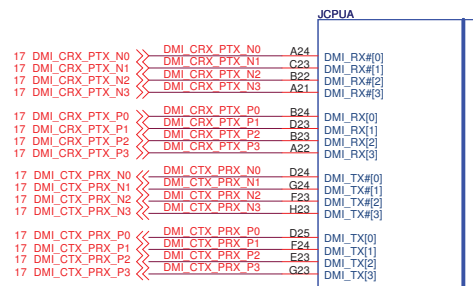
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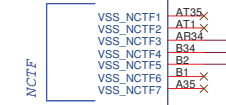
Clock Generator

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VSS



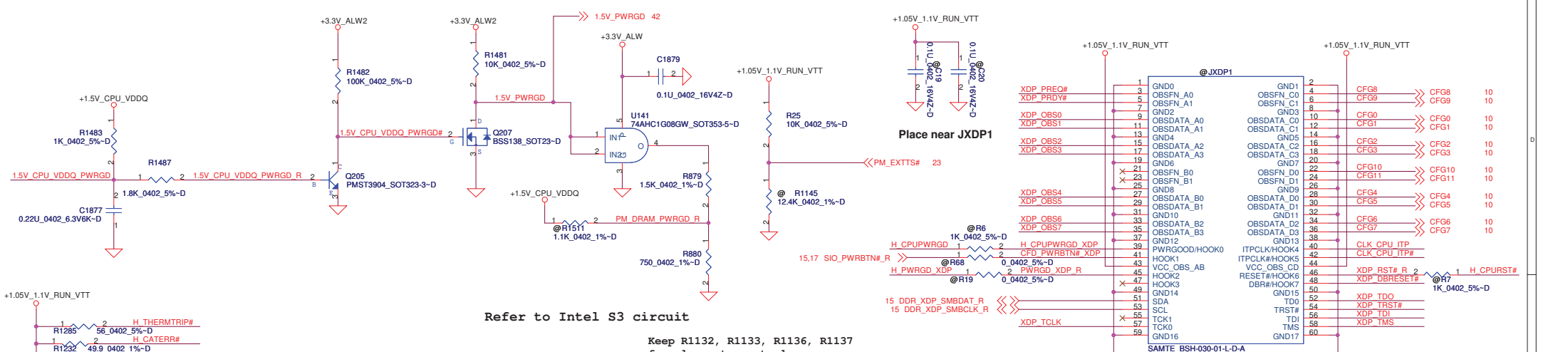
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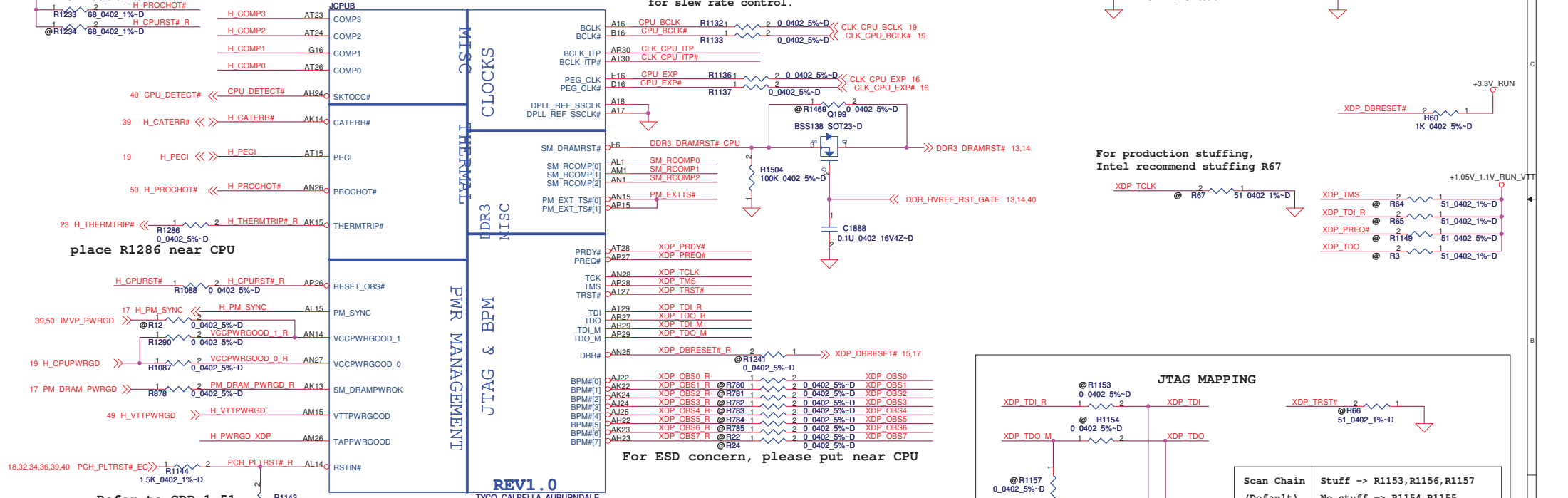
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Title Auburndale (1/6)			
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Refer to Intel S3 circuit

Keep R1132, R1133, R1136, R1137 for slew rate control.

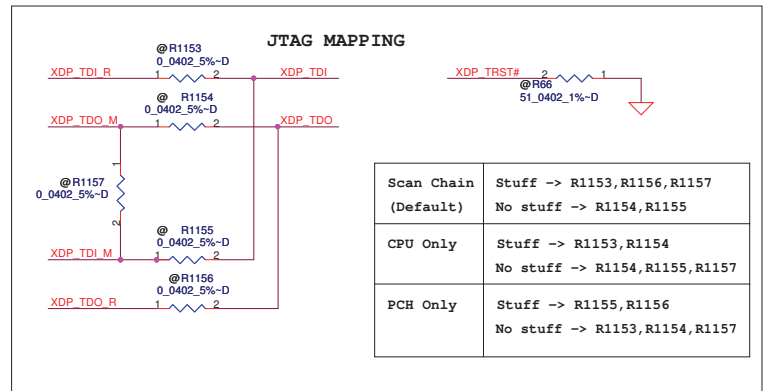


place R1286 near CPU

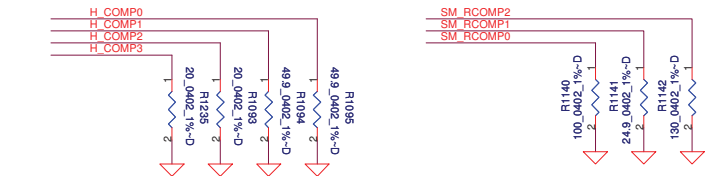
For production stuffing, Intel recommend stuffing R67

Refer to CRB 1.51

For ESD concern, please put near CPU



Scan Chain	Stuff ->
Scan Chain (Default)	Stuff -> R1153, R1156, R1157 No stuff -> R1154, R1155
CPU Only	Stuff -> R1153, R1154 No stuff -> R1154, R1155, R1157
PCH Only	Stuff -> R1155, R1156 No stuff -> R1153, R1154, R1157



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**Aururndale (2/6)**

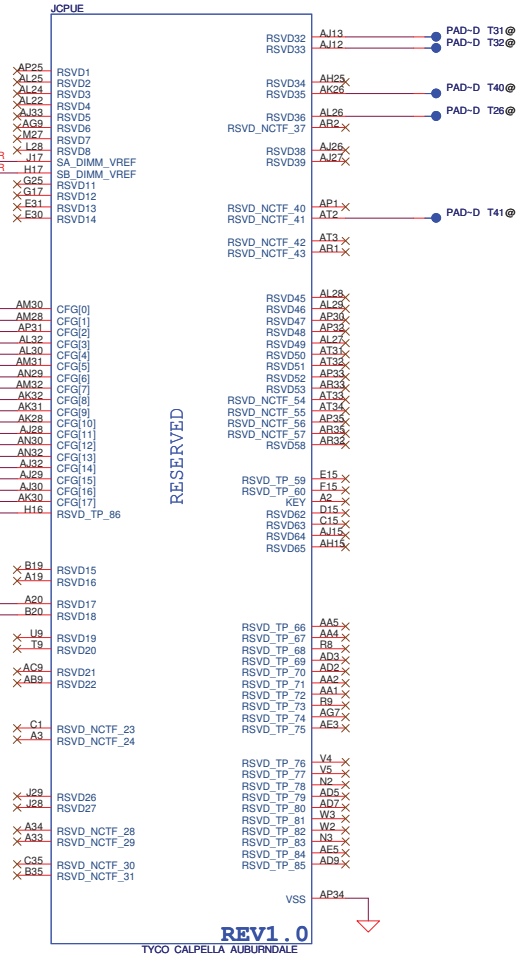
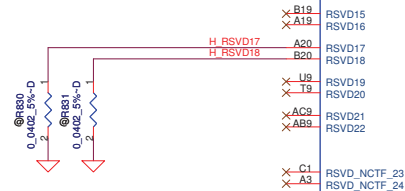
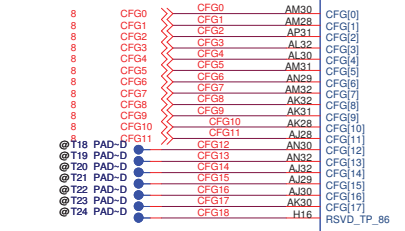
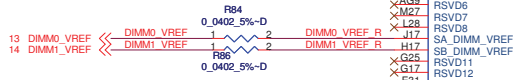
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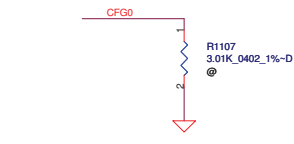




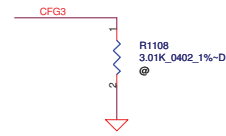
Populate R84,R86 for Intel DDR3 VREFDQ multiple methods M3



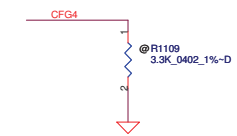
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PCI-Express Configuration Select	
CFG0	1 : Single PEG 0 : Bifurcation enable



PCI-Express Static Lane Reversal	
CFG3	1 : Normal Operation 0 : Lane Number Reversed 15->0, 14->1 ...



Display Port Presence	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

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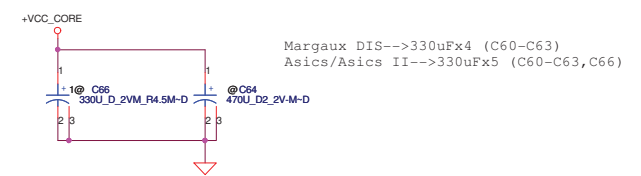
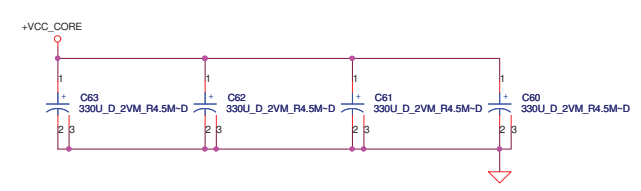
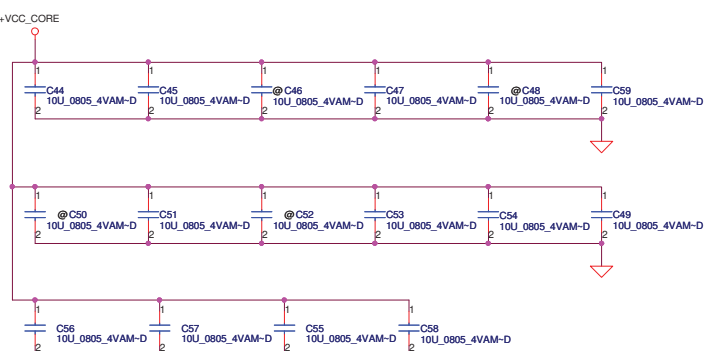
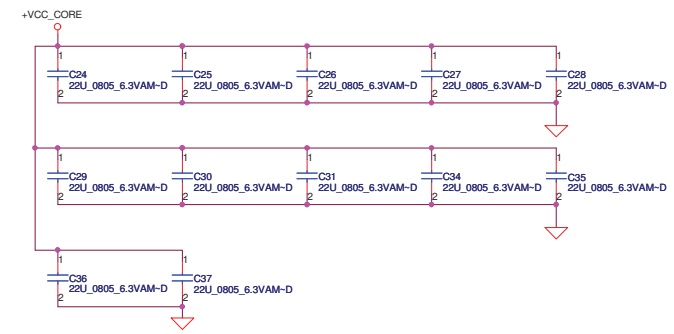
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Auburndale (4/6)

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Margaux DIS-->330uFx4 (C60-C63)  
Asics/Asics II-->330uFx5 (C60-C63,C66)

JCPUIF

AG35	VCC1
AG34	VCC2
AG33	VCC3
AG32	VCC4
AG31	VCC5
AG30	VCC6
AG29	VCC7
AG28	VCC8
AG27	VCC9
AG26	VCC10
AF35	VCC11
AF34	VCC12
AF33	VCC13
AF32	VCC14
AF31	VCC15
AF30	VCC16
AF29	VCC17
AF28	VCC18
AF27	VCC19
AF26	VCC20
AD35	VCC21
AD34	VCC22
AD33	VCC23
AD32	VCC24
AD31	VCC25
AD30	VCC26
AD29	VCC27
AD28	VCC28
AD27	VCC29
AD26	VCC30
AC35	VCC31
AC34	VCC32
AC33	VCC33
AC32	VCC34
AC31	VCC35
AC30	VCC36
AC29	VCC37
AC28	VCC38
AC27	VCC39
AC26	VCC40
AA35	VCC41
AA34	VCC42
AA33	VCC43
AA32	VCC44
AA31	VCC45
AA30	VCC46
AA29	VCC47
AA28	VCC48
AA27	VCC49
AA26	VCC50
Y35	VCC51
Y34	VCC52
Y33	VCC53
Y32	VCC54
Y31	VCC55
Y30	VCC56
Y29	VCC57
Y28	VCC58
Y27	VCC59
Y26	VCC60
V35	VCC61
V34	VCC62
V33	VCC63
V32	VCC64
V31	VCC65
V30	VCC66
V29	VCC67
V28	VCC68
V27	VCC69
V26	VCC70
U35	VCC71
U34	VCC72
U33	VCC73
U32	VCC74
U31	VCC75
U30	VCC76
U29	VCC77
U28	VCC78
U27	VCC79
U26	VCC80
R35	VCC81
R34	VCC82
R33	VCC83
R32	VCC84
R31	VCC85
R30	VCC86
P35	VCC87
P34	VCC88
P33	VCC89
P32	VCC90
P31	VCC91
P30	VCC92
P29	VCC93
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P22	VCC100

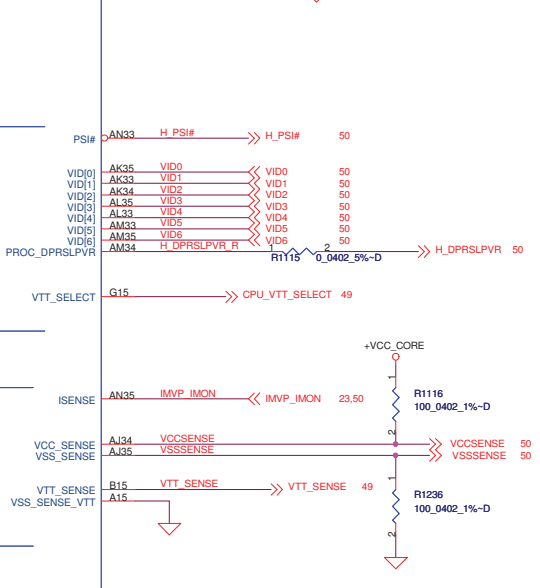
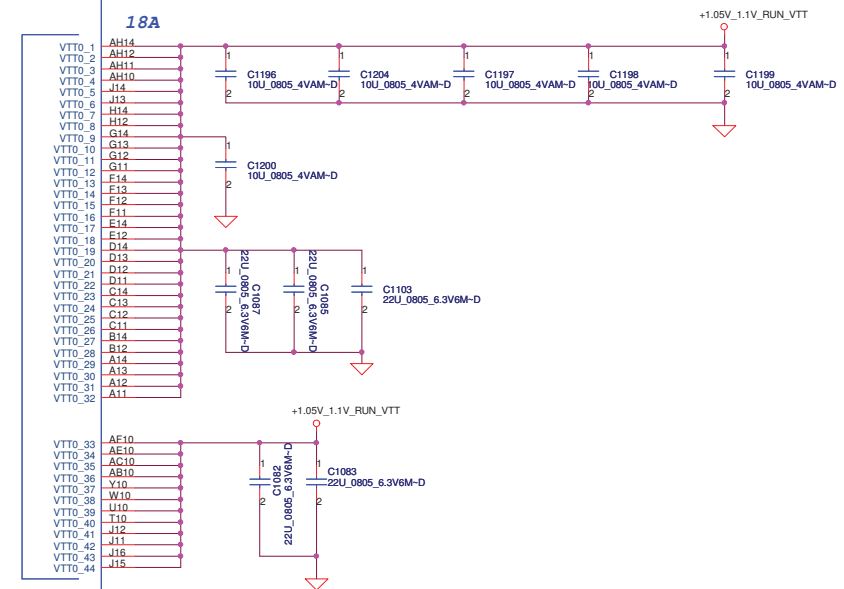
I. 1V RAIL POWER

CPU CORE SUPPLY

POWER

CPU VIDS

SENSE LINES



VTT\_SELECT = low, 1.1V  
VTT\_SELECT = high, 1.05V

Place R1116 and R1117 near CPU  
Route VCCSENSE and VSSSENSE trace at 27.4 ohms, 7 mils spacing

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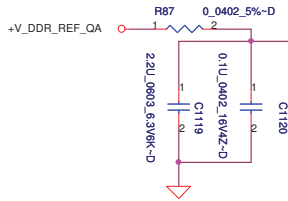
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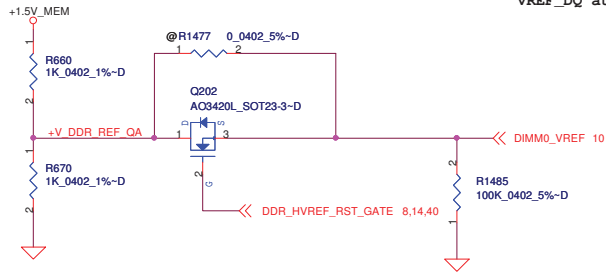


- 9 DDR\_A\_DQS#0[0..7] <<>>
- 9 DDR\_A\_D[0..63] <<>>
- 9 DDR\_A\_DM[0..7] <<>>
- 9 DDR\_A\_DQS[0..7] <<>>
- 9 DDR\_A\_MA[0..15] <<>>

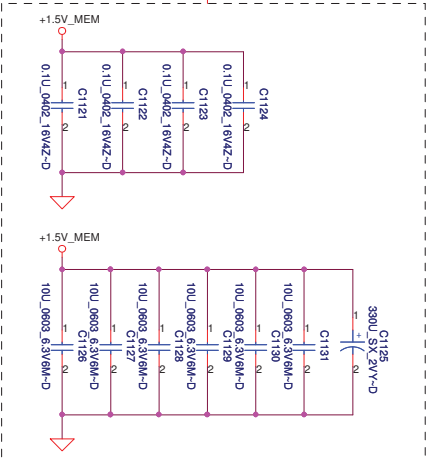
Populate R87 for Intel DDR3 VREFDQ multiple methods M1



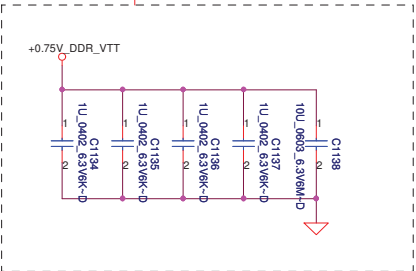
Note:  
Check voltage tolerance of VREF\_DQ at the DIMM socket



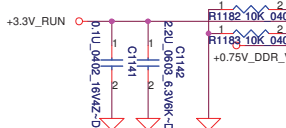
Layout Note:  
Place near JDIMMA



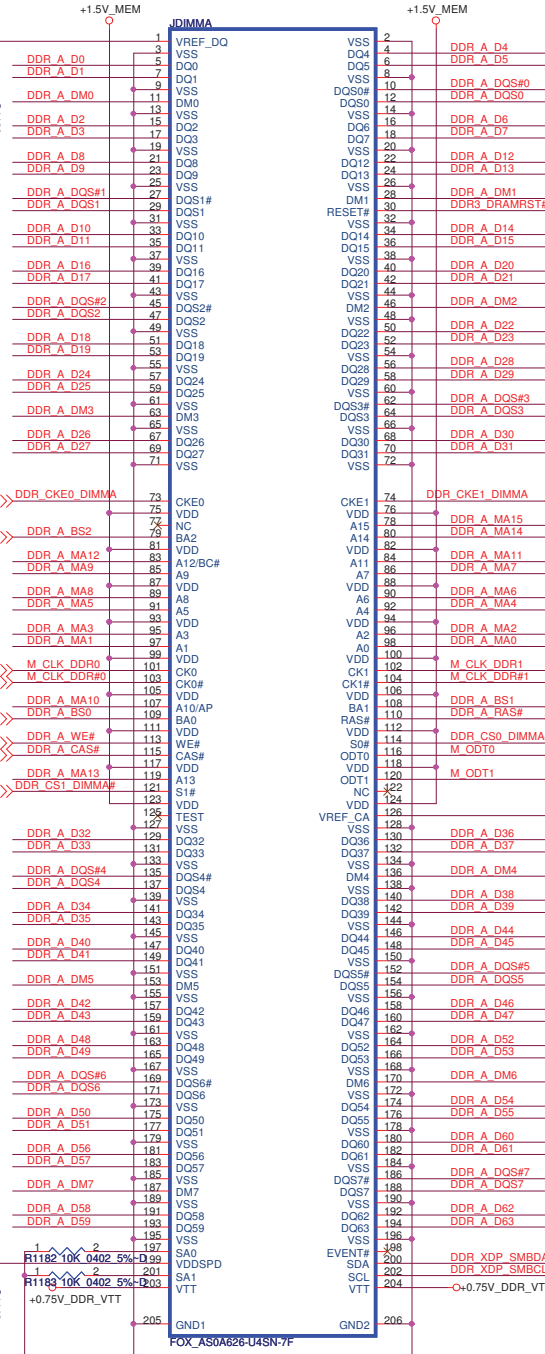
Layout Note:  
Place near JDIMMA.203,204



- 9 DDR\_CKE0\_DIMMA <<>> DDR\_CKE0\_DIMMA 73
- 9 DDR\_A\_BS2 <<>> DDR\_A\_BS2 75
- 9 DDR\_A\_MA12 <<>> DDR\_A\_MA12 83
- 9 DDR\_A\_MA9 <<>> DDR\_A\_MA9 85
- 9 DDR\_A\_MA8 <<>> DDR\_A\_MA8 87
- 9 DDR\_A\_MA5 <<>> DDR\_A\_MA5 91
- 9 DDR\_A\_MA3 <<>> DDR\_A\_MA3 95
- 9 M\_CLK\_DDR0 <<>> M\_CLK\_DDR0 101
- 9 M\_CLK\_DDR#0 <<>> M\_CLK\_DDR#0 103
- 9 DDR\_A\_MA10 <<>> DDR\_A\_MA10 107
- 9 DDR\_A\_BS0 <<>> DDR\_A\_BS0 109
- 9 DDR\_A\_WE# <<>> DDR\_A\_WE# 111
- 9 DDR\_A\_CAS# <<>> DDR\_A\_CAS# 115
- 9 DDR\_CS1\_DIMMA# <<>> DDR\_CS1\_DIMMA# 119
- DDR\_A\_D32 <<>> DDR\_A\_D32 127
- DDR\_A\_D33 <<>> DDR\_A\_D33 129
- DDR\_A\_DQS4 <<>> DDR\_A\_DQS4 135
- DDR\_A\_D34 <<>> DDR\_A\_D34 141
- DDR\_A\_D35 <<>> DDR\_A\_D35 143
- DDR\_A\_D40 <<>> DDR\_A\_D40 145
- DDR\_A\_D41 <<>> DDR\_A\_D41 147
- DDR\_A\_DM5 <<>> DDR\_A\_DM5 151
- DDR\_A\_D42 <<>> DDR\_A\_D42 155
- DDR\_A\_D43 <<>> DDR\_A\_D43 157
- DDR\_A\_D48 <<>> DDR\_A\_D48 161
- DDR\_A\_D49 <<>> DDR\_A\_D49 163
- DDR\_A\_DQS6 <<>> DDR\_A\_DQS6 167
- DDR\_A\_D50 <<>> DDR\_A\_D50 171
- DDR\_A\_D51 <<>> DDR\_A\_D51 173
- DDR\_A\_D56 <<>> DDR\_A\_D56 179
- DDR\_A\_D57 <<>> DDR\_A\_D57 181
- DDR\_A\_D58 <<>> DDR\_A\_D58 187
- DDR\_A\_D59 <<>> DDR\_A\_D59 189



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## JDIMMA H=5.2

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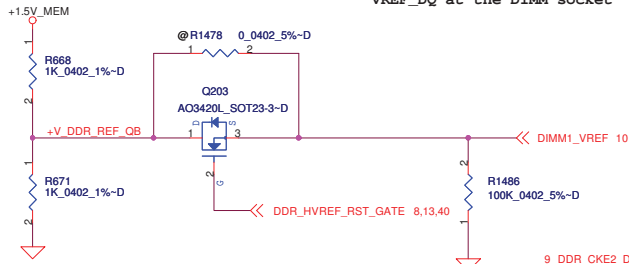


<b>Compal Electronics, Inc.</b>		
<b>DDRIII-SODIMM SLOT1</b>		
<b>LA-5573P</b>		
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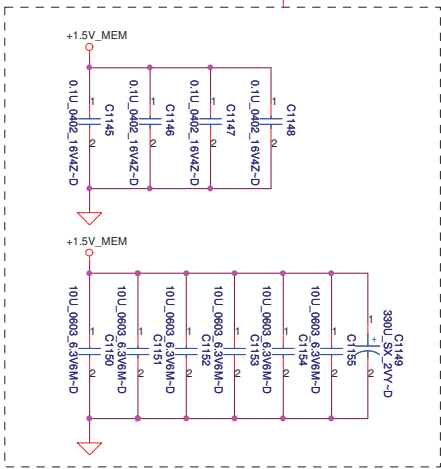
- 9 DDR\_B\_DQS#(0..7) <<>
- 9 DDR\_B\_D[0..63] <<>
- 9 DDR\_B\_DM[0..7] <<>
- 9 DDR\_B\_DQS(0..7) <<>
- 9 DDR\_B\_MA[0..15] <<>

Populate R88 for Intel DDR3 VREFDQ multiple methods M1

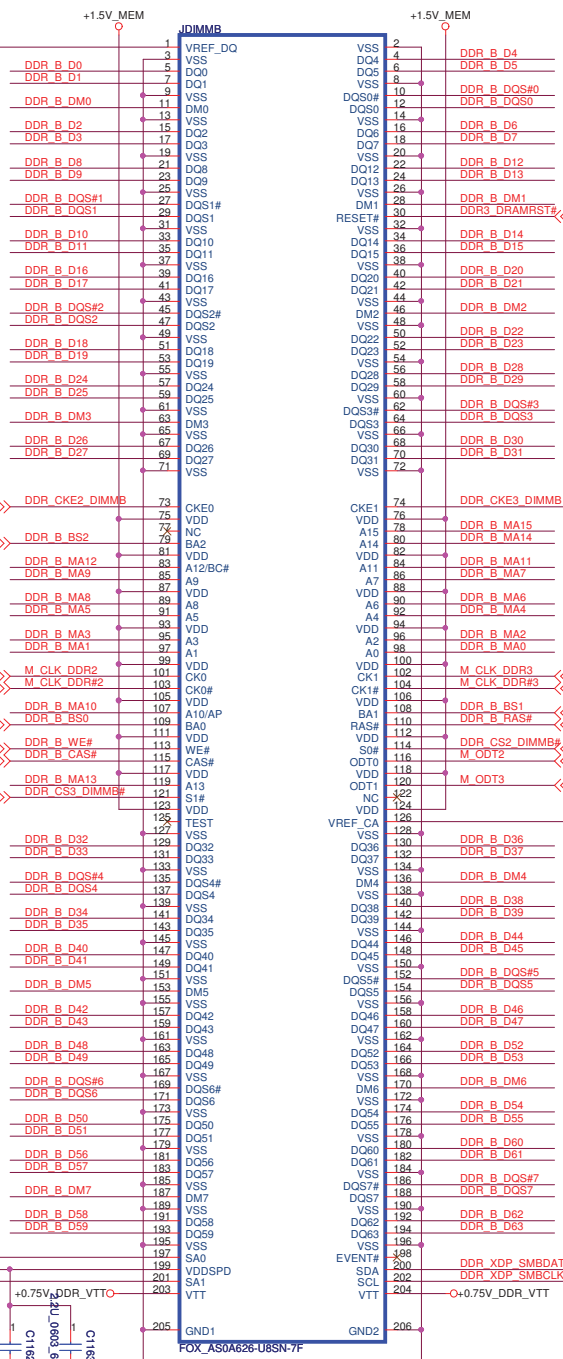
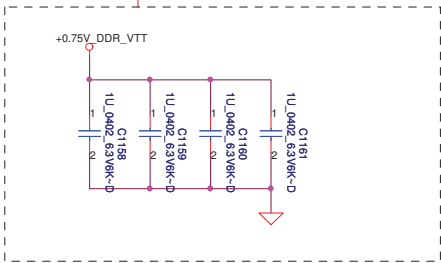
Note:  
Check voltage tolerance of VREF\_DQ at the DIMM socket



Layout Note:  
Place near JDIMMB



Layout Note:  
Place near JDIMMB.203, 204



# JDIMMB H=9.2

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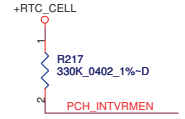
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<b>DDRIII-SODIMM SLOT2</b>		
<b>LA-5573P</b>		
File	Document Number	Rev
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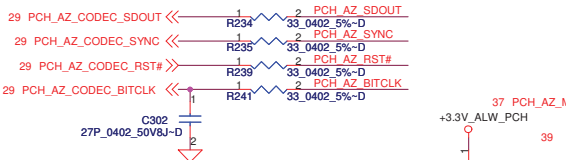
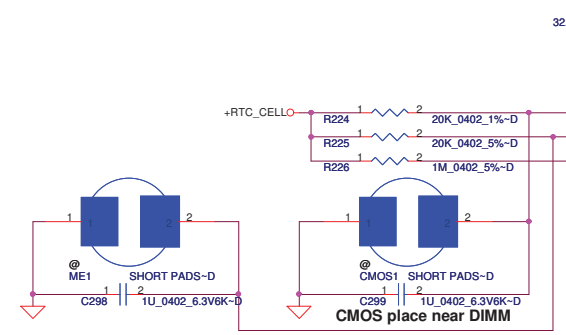
CMOS CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

ME CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

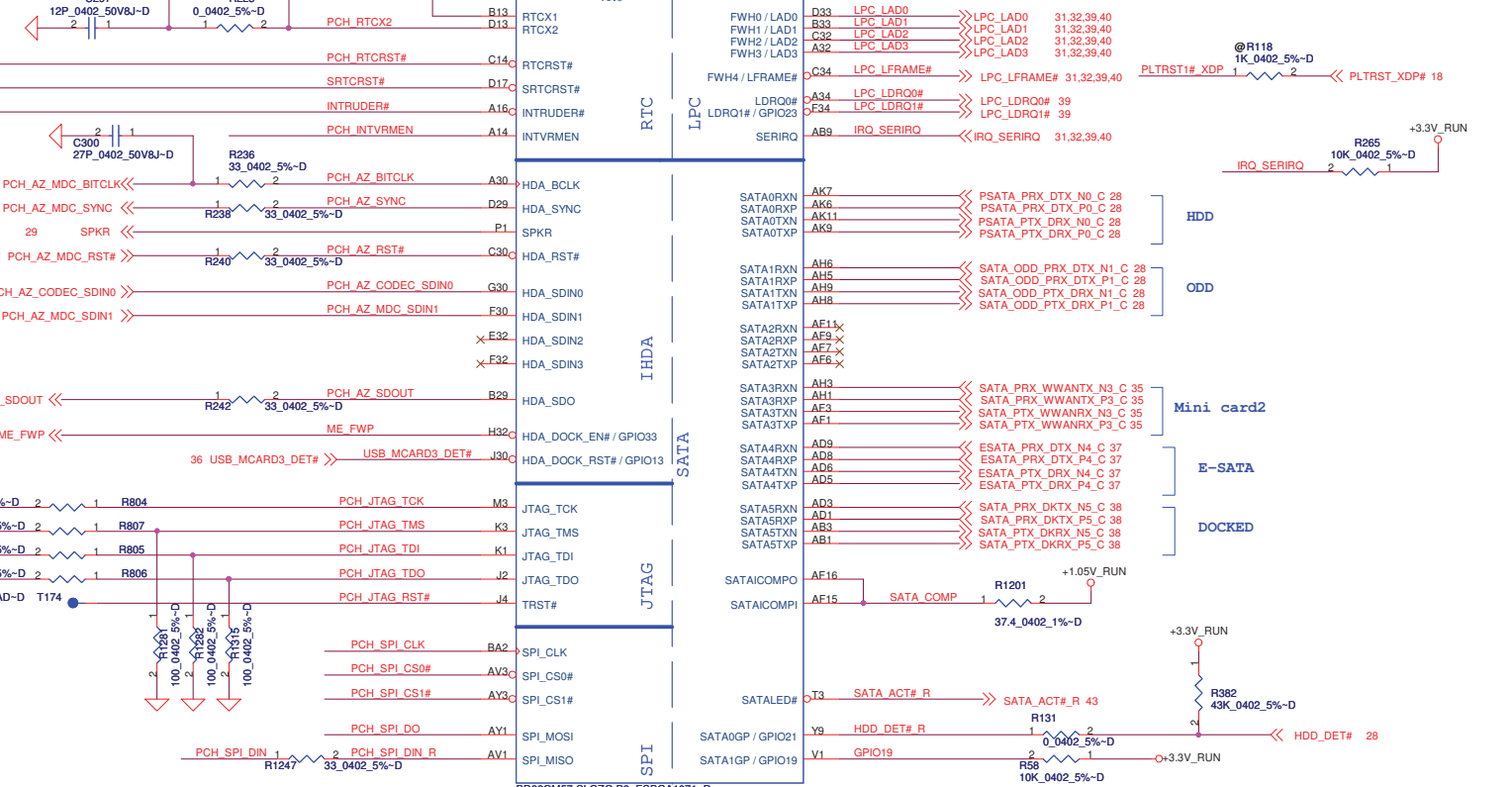
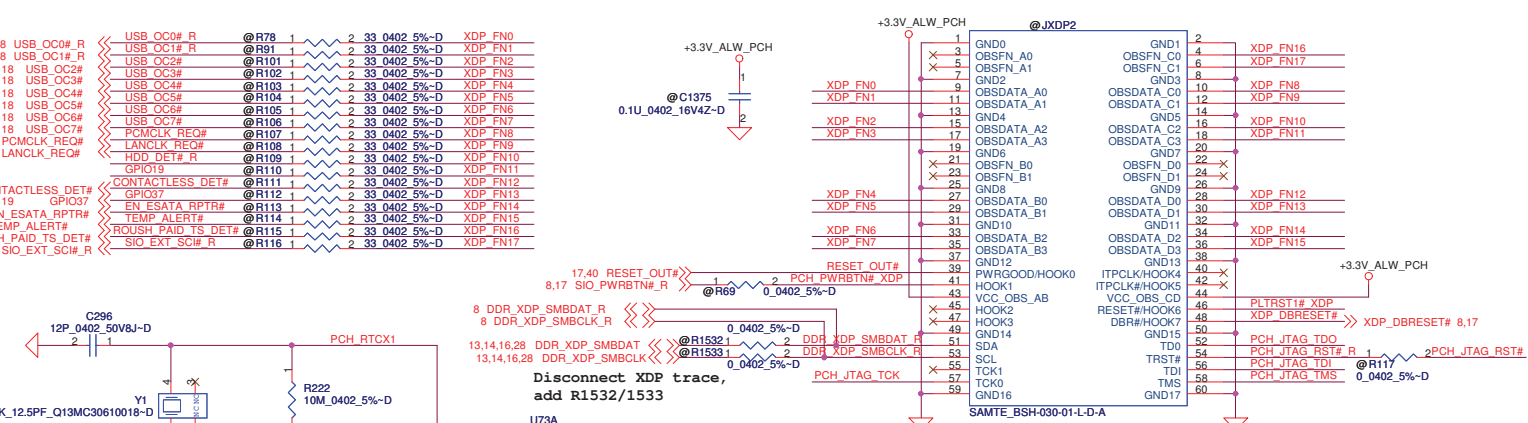
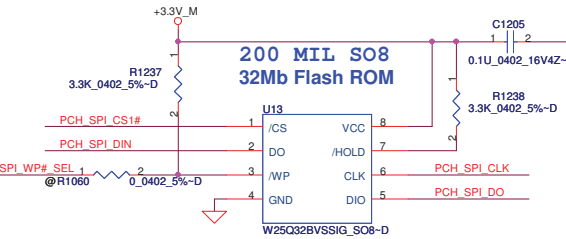
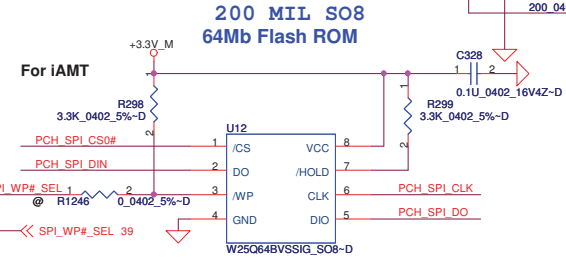


**INTRVREN - Integrated SUS**  
 1.1V VRM Enable  
 High - Enable Internal VRs

**On Die PLL VR is supplied by**  
 1.5V when sampled high, 1.8 V  
 when sampled low



Stuff R128, no stuff R123 when production



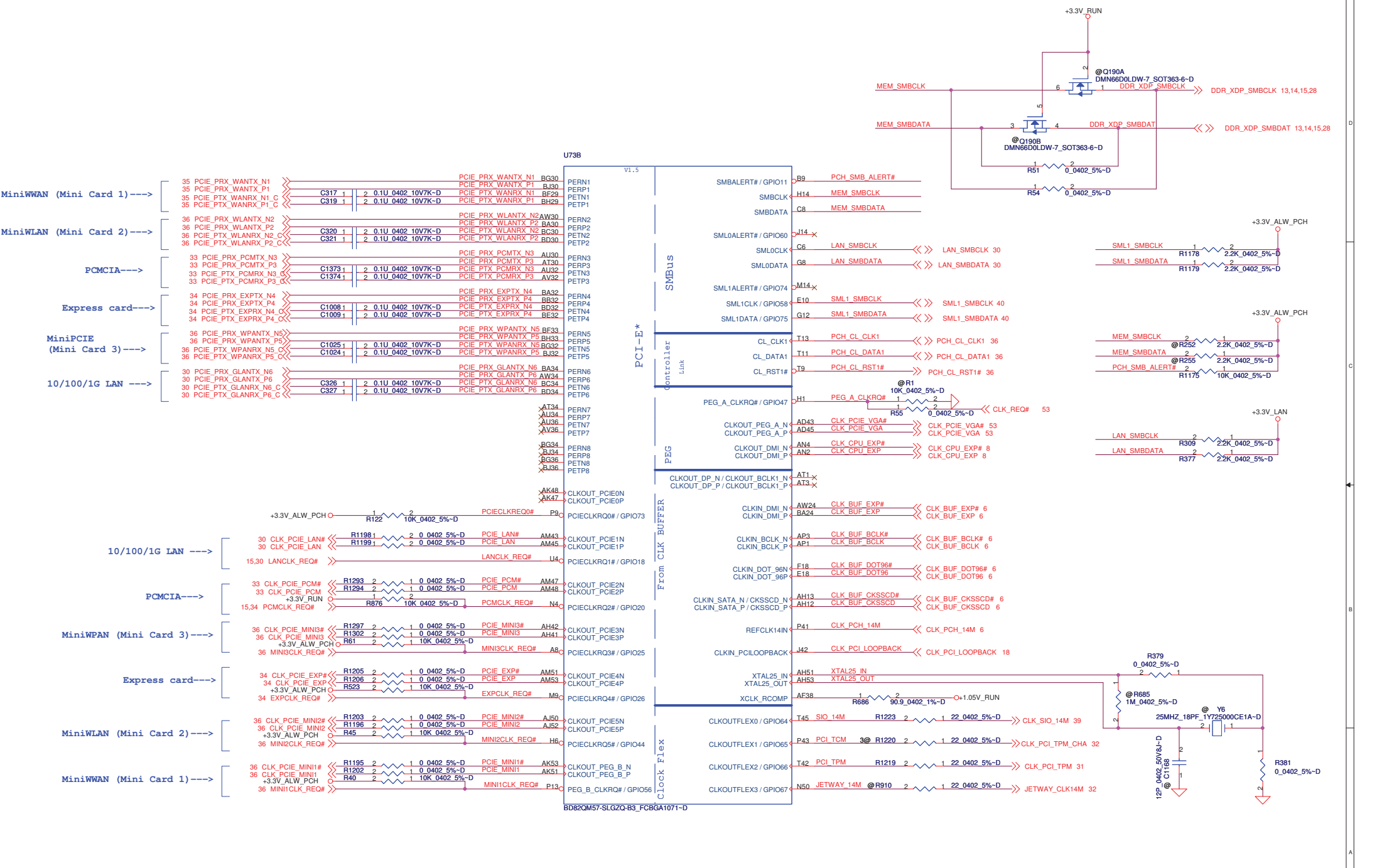
PCH Pin	Ref.	PCH JTAG Enable		PCH JTAG Disable		Production
		ES1	ES2	ES1	ES2	
TDO	R806	No Stuff	200 ohm	No Stuff	No Stuff	No Stuff
	R1315	No Stuff	100 ohm	No Stuff	No Stuff	No Stuff
TMS	R807	200 ohm	200 ohm	No Stuff	No Stuff	No Stuff
	R1281	100 ohm	100 ohm	No Stuff	No Stuff	No Stuff
TDI	R805	200 ohm	200 ohm	20K ohm	No Stuff	No Stuff
	R1282	100 ohm	100 ohm	10K ohm	No Stuff	No Stuff
TCK	R804	51 ohm	51 ohm	51 ohm	51 ohm	No Stuff
TRST#	R808	20K ohm	20K ohm	No Stuff	No Stuff	No Stuff
	R1316	10K ohm	10K ohm	No Stuff	No Stuff	No Stuff

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PCH (1/8)

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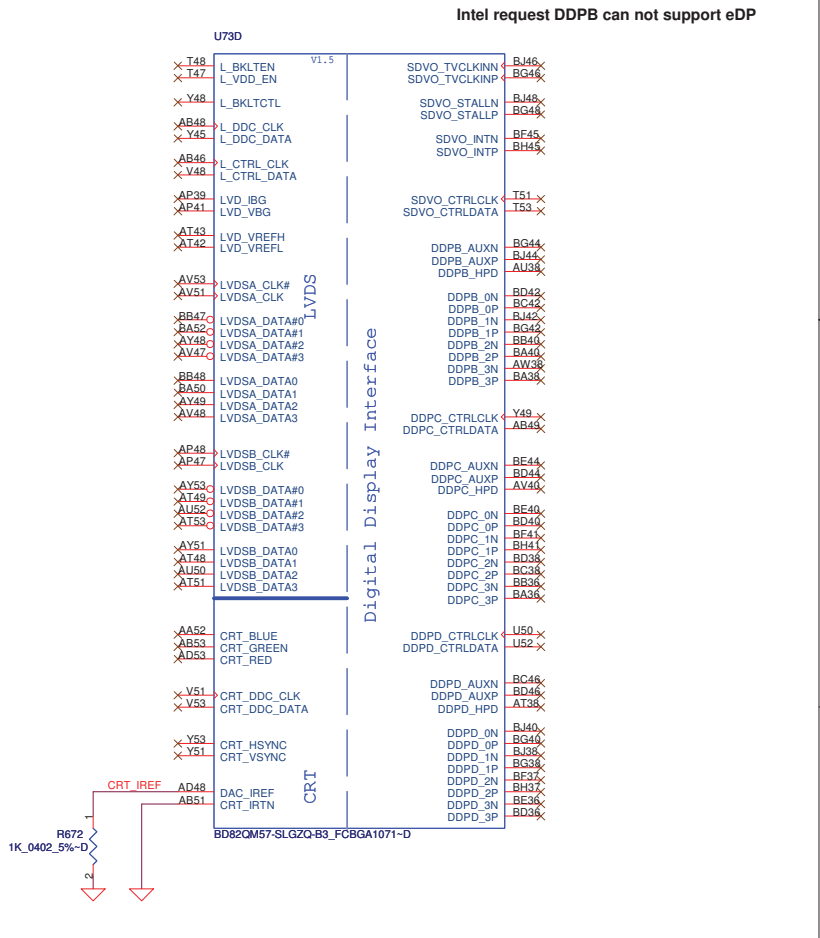
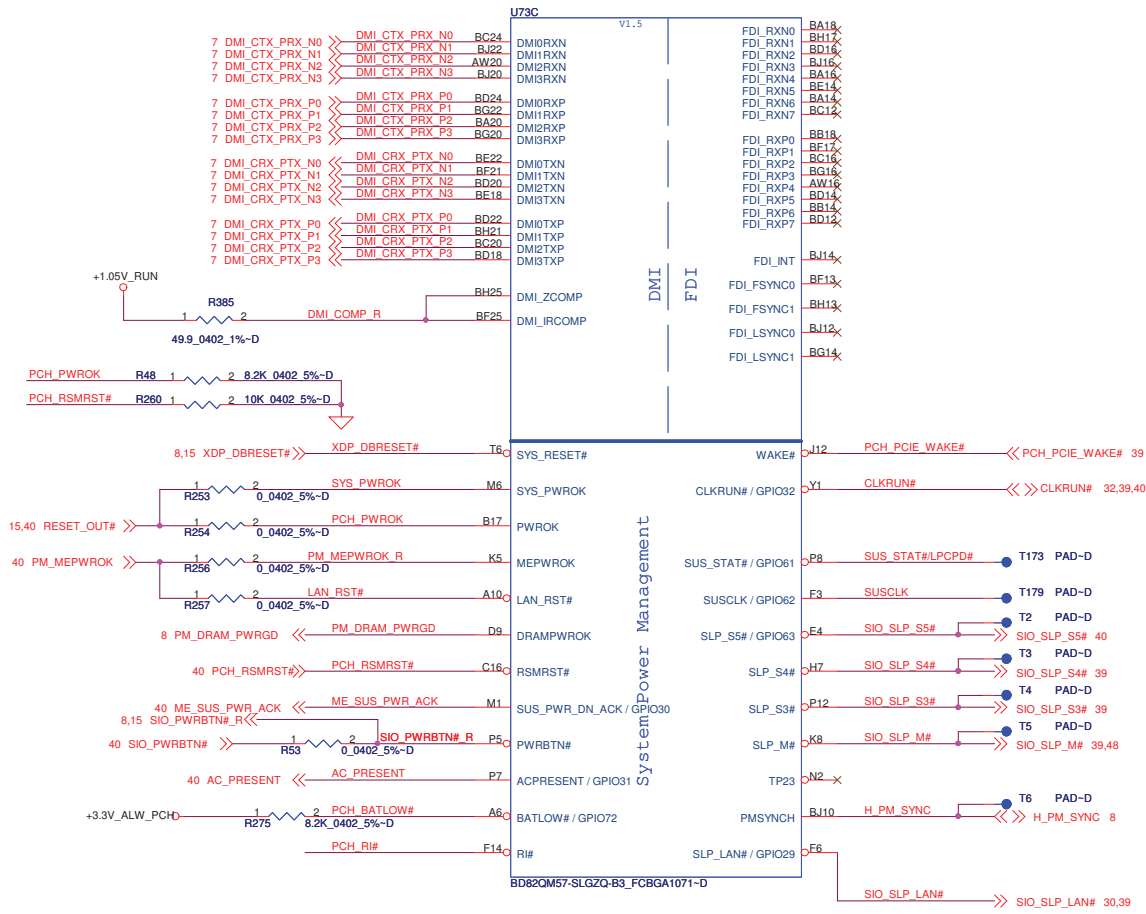
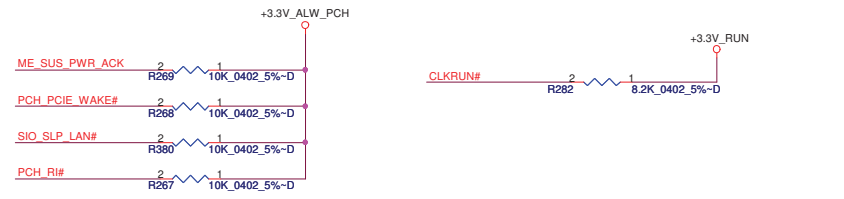
**PCH (2/8)**

Title \_\_\_\_\_


Size \_\_\_\_\_ Document Number **LA-5573P** Rev 0.1

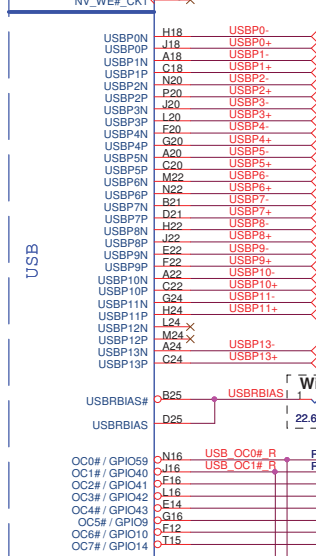
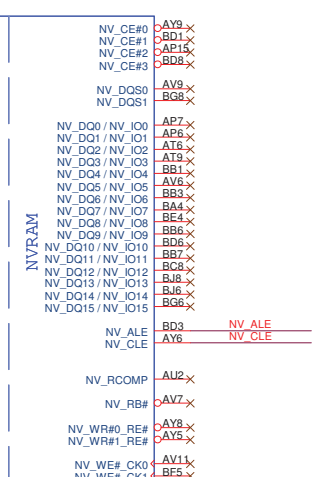
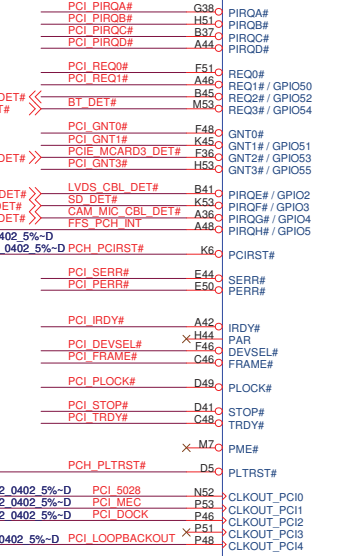
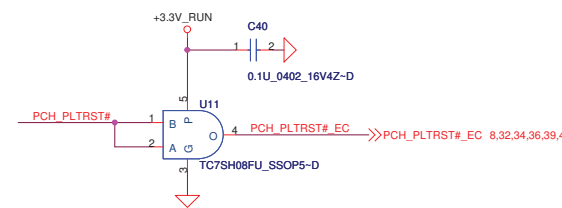
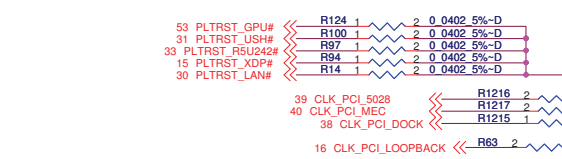
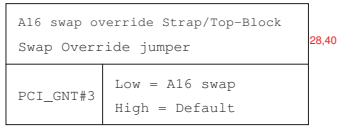
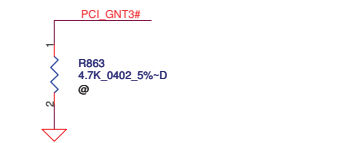
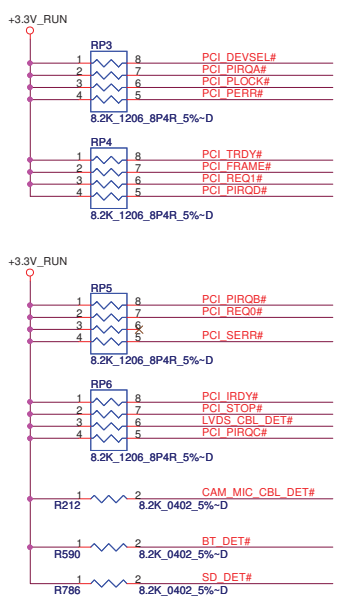
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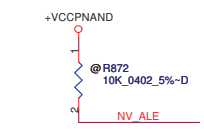


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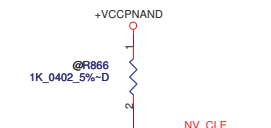
		<b>Compal Electronics, Inc.</b>	
		<b>PCH (3/8)</b>	
Size	Document Number	Rev	
	<b>LA-5573P</b>	0.1	
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PCH XDP ENABLE	Stuff: R78,R89,R101-R116
	No Stuff: R71,R77,RP1,RP2,R45,R40,R131,R58,R1242,R1243,R1244,R1245,R74,R130
PCH XDP DISABLE	Stuff: R71,R77,RP1,RP2,R45,R40,R131,R58,R1242,R1243,R1244,R1245,R74,R130
	No Stuff: R78,R89,R101-R116

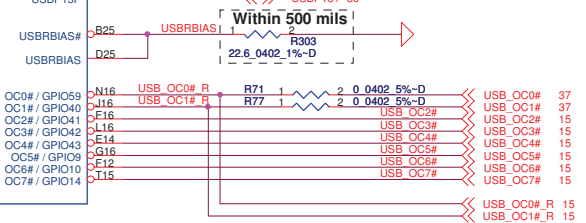
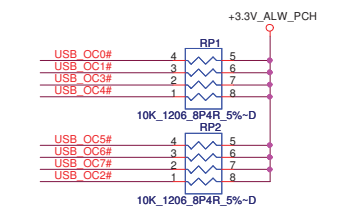


Danbury Technology Enabled	
NV_ALE	High = Enabled (Default) Low = Disabled

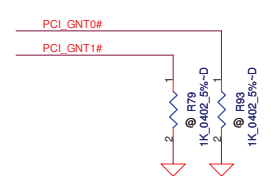


DMI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

- >Right Side Bottom
- >Right Side Top
- >Left Side Top
- >Left Side Bottom
- >WLAN
- >WWAN
- >Blue Tooth
- >BIO
- >DOCK
- >Express Card
- >Camera
- >PCIE/BKT



Boot BIOS Strap		
PCI_GNT#1	PCI_GNT#0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI



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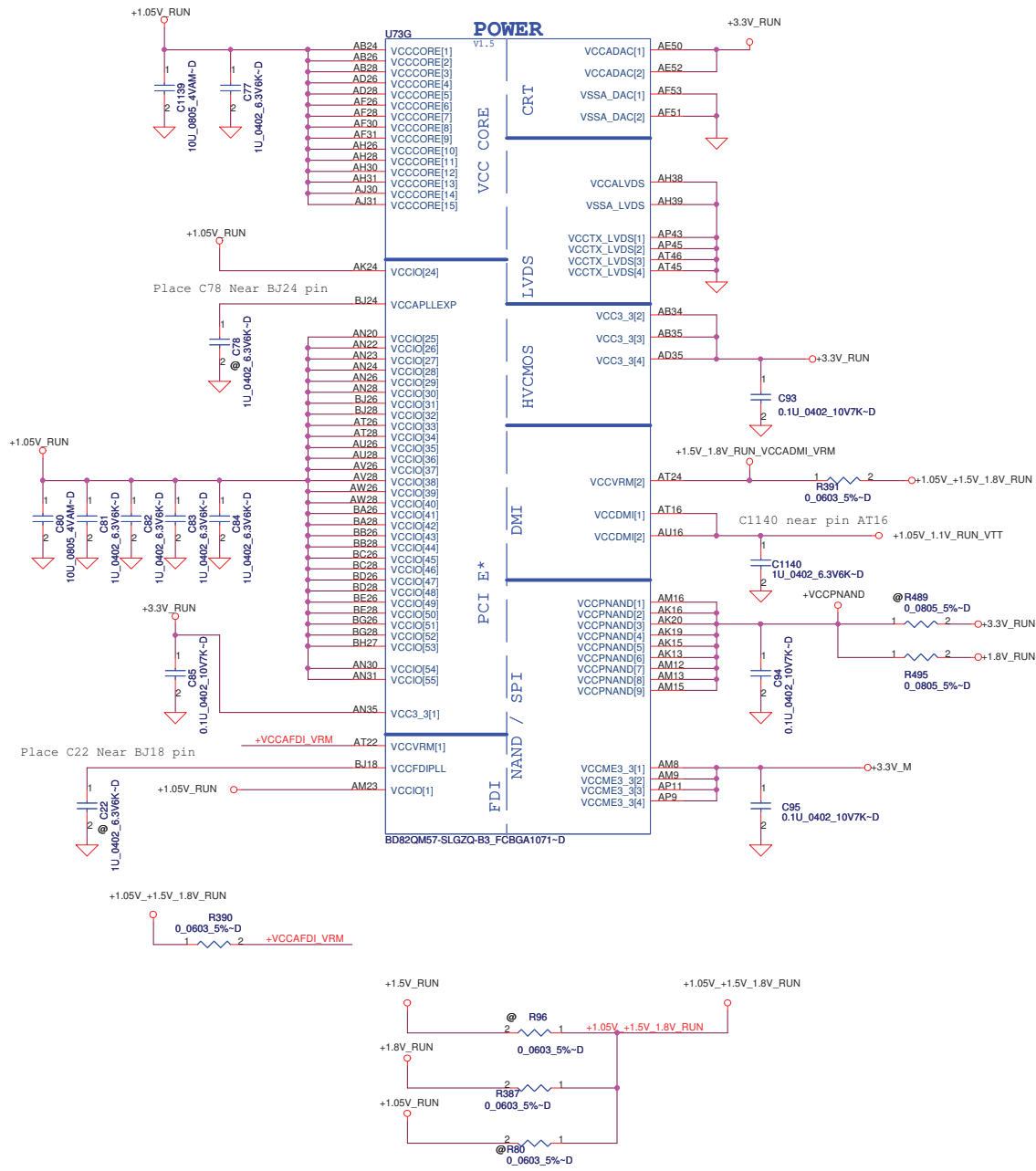
**PCH (4/8)**

Title: \_\_\_\_\_

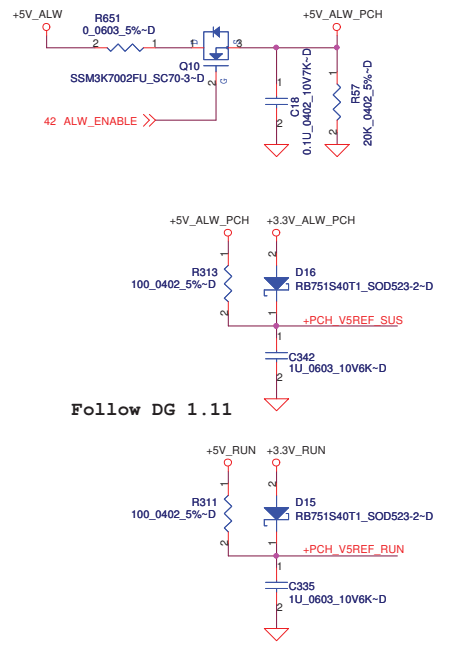
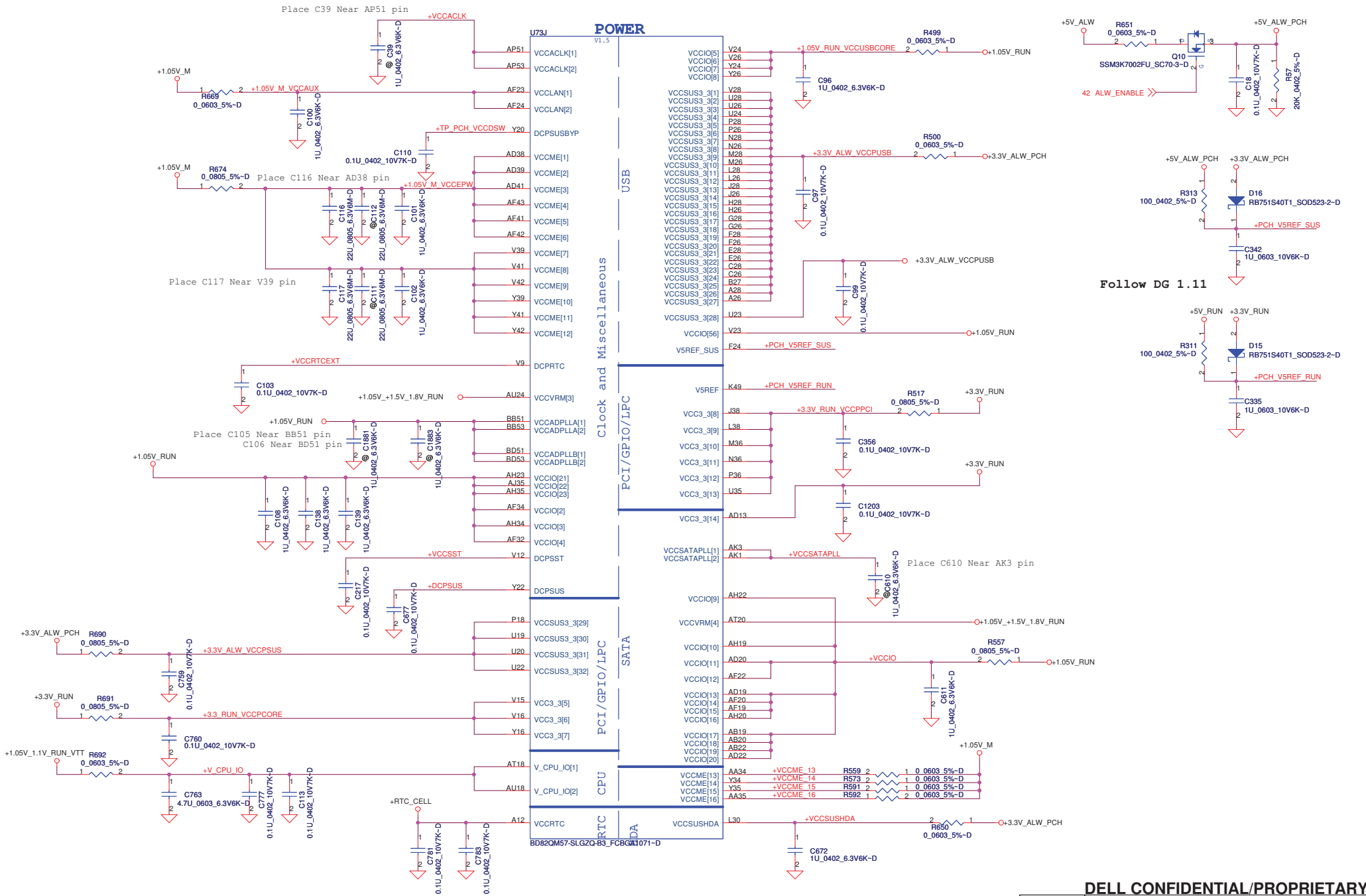
Size: \_\_\_\_\_ Document Number: **LA-5573P** Rev: 0.1

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PCH Power Rail Table		
Voltage Rail	Voltage	SO Iccmax Current (A)
V_CPU_IO	1.1/1.05	< 1 (mA)
V5REF	5	< 1 (mA)
V5REF_Sus	5	< 1 (mA)
Vcc3_3	3.3	0.357
VccAClk	1.1	0.052
VccADAC	3.3	0.069
VccADPLLA	1.1	0.068
VccADPLLB	1.1	0.069
Vccap11EXP	1.1	0.04
VccCore	1.1	1.432
VccDMI	1.1	0.058
VccDMI	1.1	0.061
VccFDIPLL	1.1	0.037
VccIO	1.1	3.062
VccLAN	1.1	0.32
VccME	1.1	1.849
VccME3_3	3.3	0.085
VccpNAND	1.8	0.156
VccRTC	3.3	2 (mA)
VccSATAPLL	1.1	0.031
VccSus3_3	3.3	0.163
VccSusHDA	3.3	0.006
VccVRM	1.8 / 1.5	0.196
VccALVDS	3.3	< 1 (mA)
VccTX_LVDS	1.8	0.059



**U73H** v1.5

AB16	VSS[0]	AK30
AA19	VSS[1]	AK31
AA20	VSS[2]	AK32
AA22	VSS[3]	AK34
AA19	VSS[4]	AK35
AA24	VSS[5]	AK38
AA26	VSS[6]	AK43
AA28	VSS[7]	AK46
AA30	VSS[8]	AK49
AA31	VSS[9]	AK5
AA32	VSS[10]	AK6
AB11	VSS[11]	AL2
AB15	VSS[12]	AL52
AB23	VSS[13]	AM11
AB30	VSS[14]	BB44
AB31	VSS[15]	AD24
AB32	VSS[16]	AM20
AB39	VSS[17]	AM22
AB43	VSS[18]	AM24
AB47	VSS[19]	AM26
AB5	VSS[20]	AM28
AB8	VSS[21]	AM30
AC2	VSS[22]	BA42
AC52	VSS[23]	AM31
AD11	VSS[24]	AM32
AD12	VSS[25]	AM34
AD16	VSS[26]	AM35
AD23	VSS[27]	AM39
AD30	VSS[28]	AM42
AD31	VSS[29]	AU20
AD32	VSS[30]	AM46
AD34	VSS[31]	AV22
AU22	VSS[32]	AM49
AD42	VSS[33]	AM7
AD46	VSS[34]	AA50
AD49	VSS[35]	BB10
AD7	VSS[36]	BB11
AE2	VSS[37]	AN52
AE4	VSS[38]	AN50
AF12	VSS[39]	AN52
Y13	VSS[40]	AP12
AH49	VSS[41]	AP23
AU4	VSS[42]	AP46
AF35	VSS[43]	AP49
AP13	VSS[44]	AP24
AN34	VSS[45]	AP2
AF45	VSS[46]	AR2
AF46	VSS[47]	AR2
AF49	VSS[48]	AR52
AF5	VSS[49]	AT11
AF9	VSS[50]	BA12
AG2	VSS[51]	AH48
AG52	VSS[52]	AT32
AH11	VSS[53]	AT36
AH15	VSS[54]	AT41
AH16	VSS[55]	AT47
AH24	VSS[56]	AT7
AH32	VSS[57]	AV12
AV18	VSS[58]	AV16
AH43	VSS[59]	AV20
AH7	VSS[60]	AV24
AJ19	VSS[61]	AV30
AJ2	VSS[62]	AV34
AJ20	VSS[63]	AV38
AJ22	VSS[64]	AV42
AJ23	VSS[65]	AV46
AJ26	VSS[66]	AV49
AJ28	VSS[67]	AV5
AJ32	VSS[68]	AV8
AJ34	VSS[69]	AW14
AT5	VSS[70]	AW18
AJ4	VSS[71]	AW2
AK12	VSS[72]	BF9
AM41	VSS[73]	AW32
AN19	VSS[74]	AW36
AK26	VSS[75]	AW40
AK22	VSS[76]	AW52
AK23	VSS[77]	AY11
AK28	VSS[78]	AY43
AK28	VSS[79]	AY47

BD82QM57-SLGZQ-B3\_FCBGA1071-D

**U73I** v1.5

AY7	VSS[159]	H49
B11	VSS[160]	H5
B15	VSS[161]	J24
B19	VSS[162]	K11
B23	VSS[163]	K43
B31	VSS[164]	K47
B35	VSS[165]	K7
B39	VSS[166]	L14
B43	VSS[167]	L18
B47	VSS[168]	L2
B7	VSS[169]	L22
BB2	VSS[170]	L32
BB12	VSS[171]	L36
BB16	VSS[172]	L40
BB20	VSS[173]	L52
BB24	VSS[174]	M12
BB30	VSS[175]	M16
BB34	VSS[176]	M20
BB38	VSS[177]	N38
BB42	VSS[178]	M34
BB49	VSS[179]	M38
BB5	VSS[180]	M42
BC10	VSS[181]	M46
BC14	VSS[182]	M49
BC18	VSS[183]	M5
BC2	VSS[184]	M8
BC22	VSS[185]	N24
BC32	VSS[186]	P11
BC36	VSS[187]	AD15
BC40	VSS[188]	P22
BC44	VSS[189]	P30
BC52	VSS[190]	P32
BD48	VSS[191]	P4
BD49	VSS[192]	P42
BD5	VSS[193]	P45
BD5	VSS[194]	P47
BE12	VSS[195]	R2
BE16	VSS[196]	R52
BE20	VSS[197]	T12
BE24	VSS[198]	T41
BE30	VSS[199]	T46
BE34	VSS[200]	T49
BE38	VSS[201]	T5
BE42	VSS[202]	T8
BE46	VSS[203]	U30
BE50	VSS[204]	U31
BE54	VSS[205]	U32
BE6	VSS[206]	U34
BE8	VSS[207]	P38
BE9	VSS[208]	V11
BE49	VSS[209]	P16
BF51	VSS[210]	V19
BG18	VSS[211]	V20
BP24	VSS[212]	V22
BG4	VSS[213]	V30
BG50	VSS[214]	V31
BH11	VSS[215]	V32
BH15	VSS[216]	V34
BH19	VSS[217]	V36
BH23	VSS[218]	V38
BH31	VSS[219]	V43
BH35	VSS[220]	V45
BH39	VSS[221]	V46
BH43	VSS[222]	V47
BH47	VSS[223]	V49
BH7	VSS[224]	V5
C12	VSS[225]	V7
C50	VSS[226]	V8
D51	VSS[227]	W2
E12	VSS[228]	WS2
E16	VSS[229]	Y11
E20	VSS[230]	Y12
E24	VSS[231]	Y15
E30	VSS[232]	Y19
E34	VSS[233]	Y23
E38	VSS[234]	Y28
E42	VSS[235]	Y30
E46	VSS[236]	Y31
E48	VSS[237]	Y32
E52	VSS[238]	Y38
F8	VSS[239]	Y43
F49	VSS[240]	Y46
F5	VSS[241]	Y49
G10	VSS[242]	Y6
G14	VSS[243]	Y8
G18	VSS[244]	Y8
G2	VSS[245]	P24
G22	VSS[246]	T43
G32	VSS[247]	AD51
G36	VSS[248]	AT8
G40	VSS[249]	AD47
G44	VSS[250]	Y47
G52	VSS[251]	AT12
AF39	VSS[252]	VSS[351]
H16	VSS[253]	VSS[352]
H20	VSS[254]	AM6
H30	VSS[255]	AT13
H34	VSS[256]	AM5
H38	VSS[257]	VSS[353]
H42	VSS[258]	VSS[354]
		VSS[355]
		VSS[356]
		AK39
		AV14
		VSS[366]

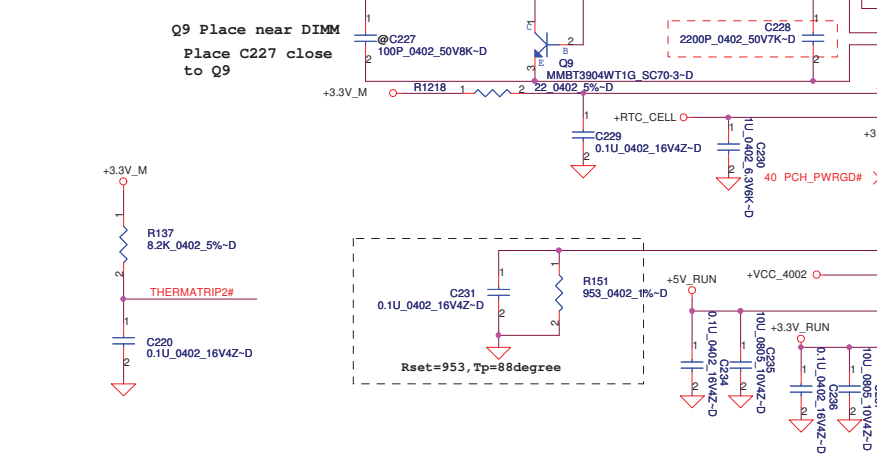
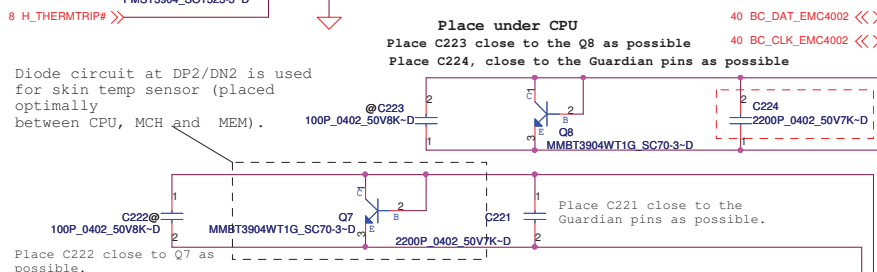
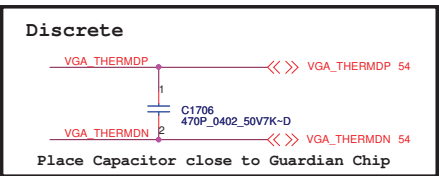
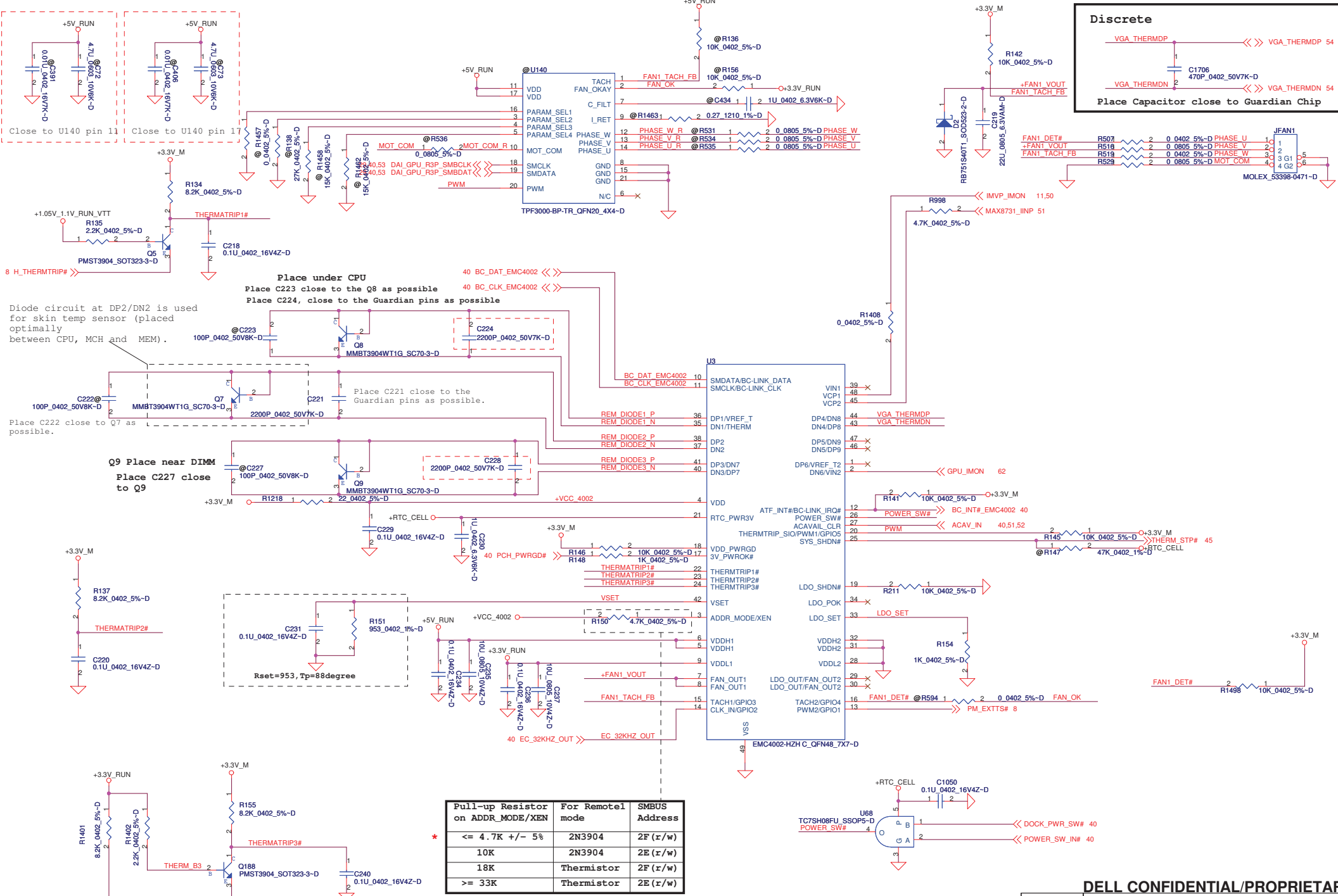
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PCH (8/8)		
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Pull-up Resistor on ADDR_MODE/XEN	For Remotel mode	SMBUS Address
<= 4.7K +/- 5%	2N3904	2F (x/w)
10K	2N3904	2E (x/w)
18K	Thermistor	2F (x/w)
>= 33K	Thermistor	2E (x/w)

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**FAN & Thermal Sensor**

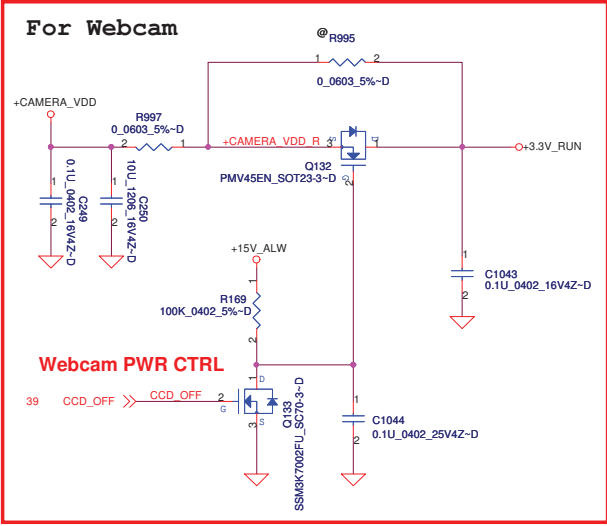
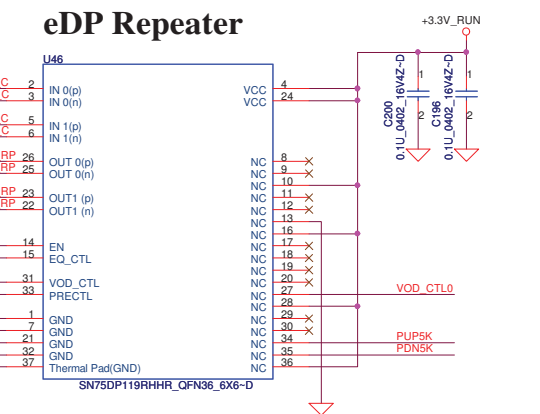
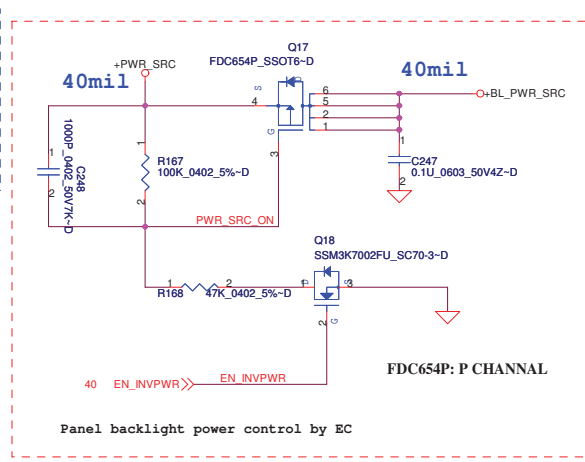
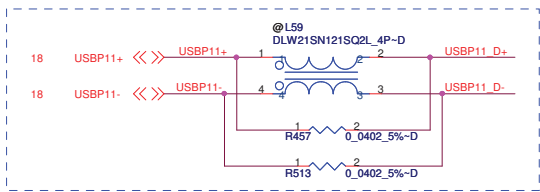
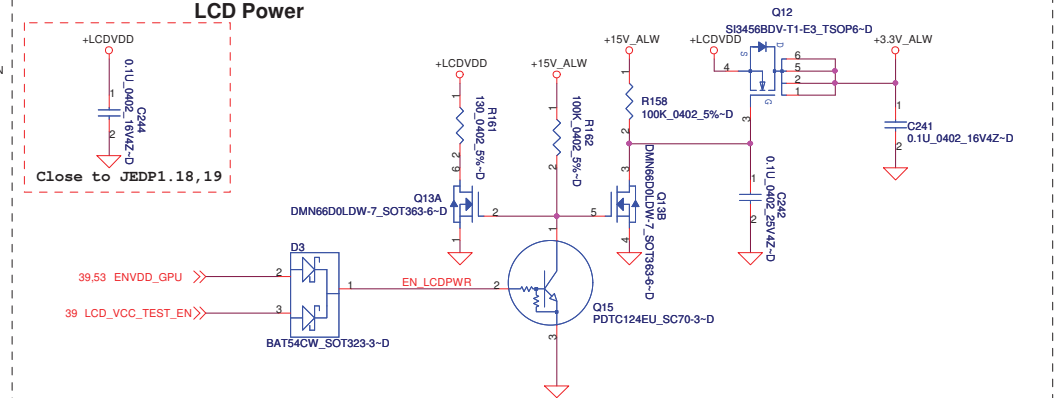
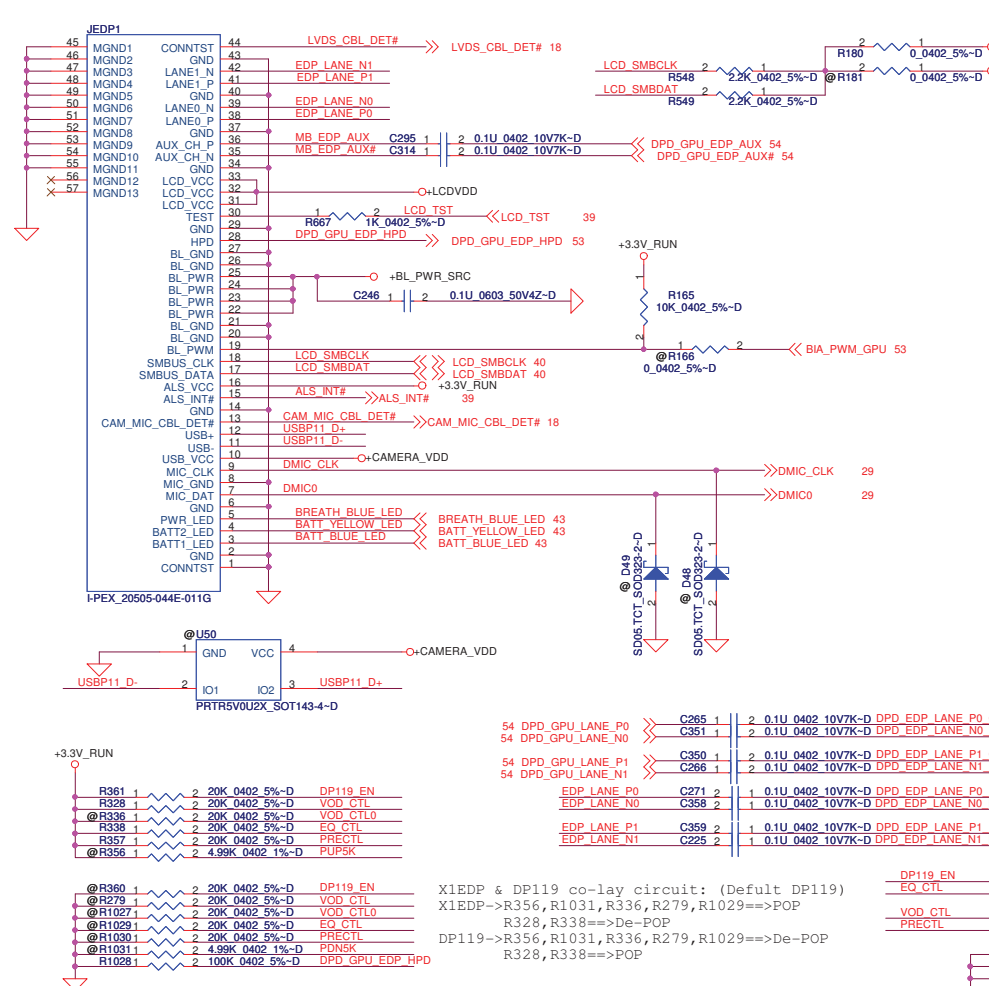
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Refer to SN75DP119RHHR rev. 0P35

VOD (mV)	PRE (dB)	PRECTL	VOD_CTL
300	2.5	0	0
	6	VCC/2	0
	8.5	1	0
400	0	0	VCC/2
	3.5	VCC/2	VCC/2
	5.5	1	VCC/2
600	0	0	1
	2	VCC/2	1
800	0	1	1

EQ gain (dB)	EQ_CTL
0	0
3	VCC/2
6	1

MODE	DP119_EN
PWR Down	0
OUT2 DIS	VCC/2
OUT1 OUT2 EN	1

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**eDP & CAM Conn**

Title: \_\_\_\_\_

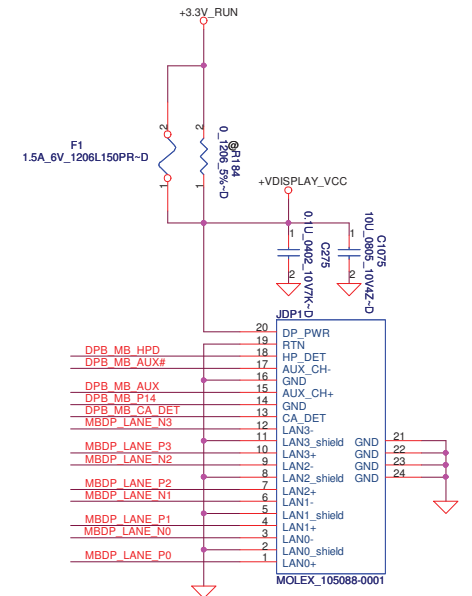
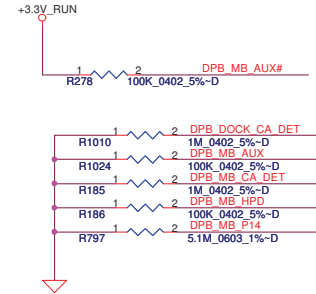
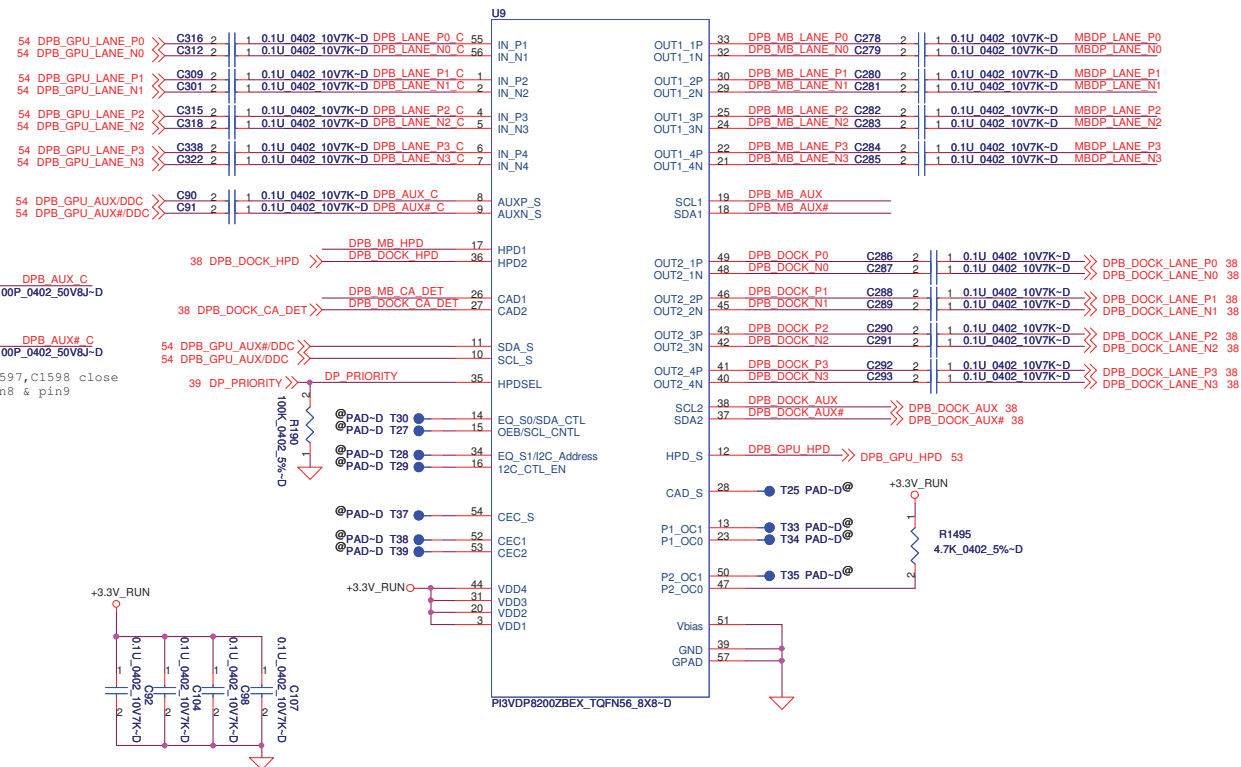
Size: \_\_\_\_\_ Document Number: **LA-5573P** Rev: 0.1

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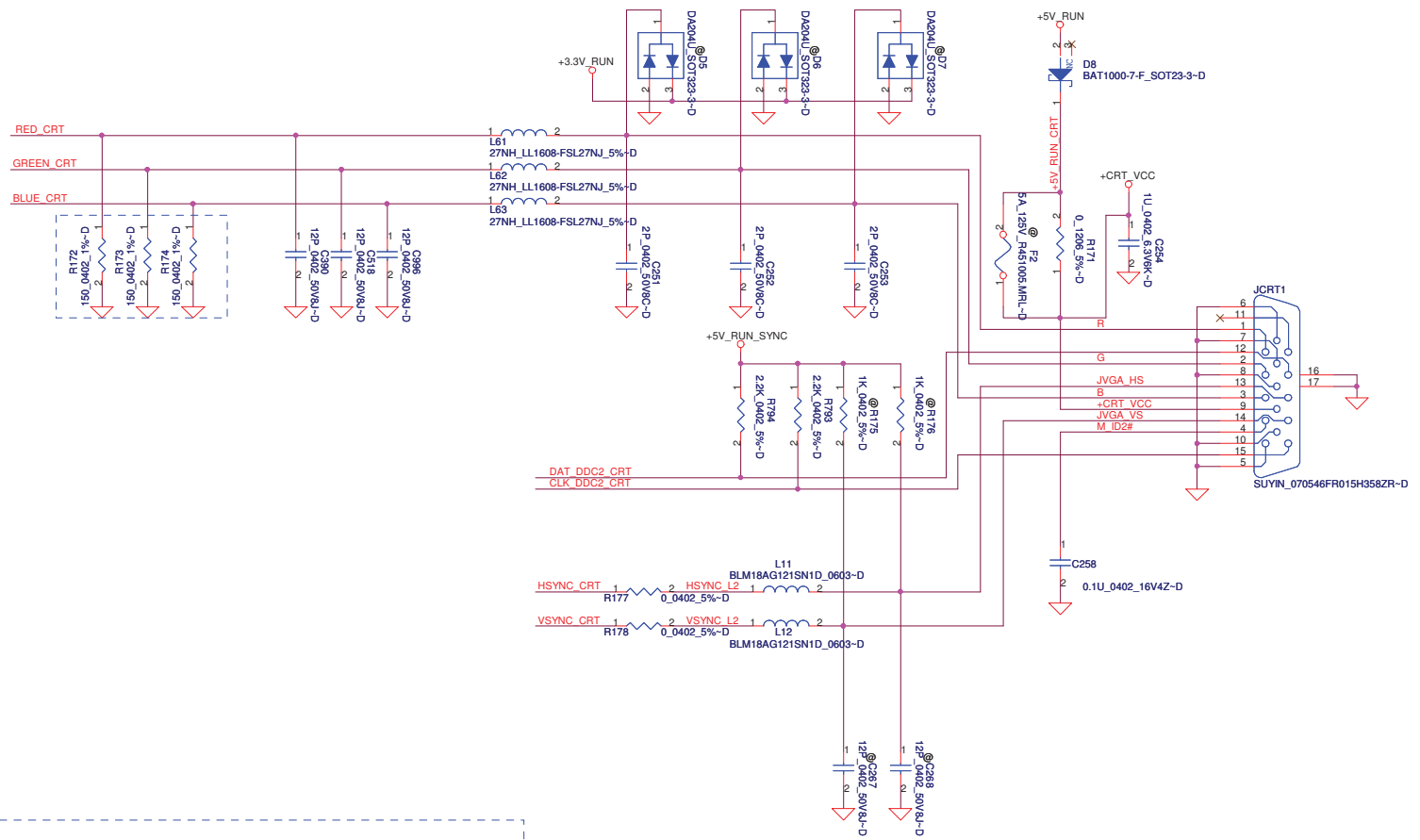
## DPB SW for MB & DOCK



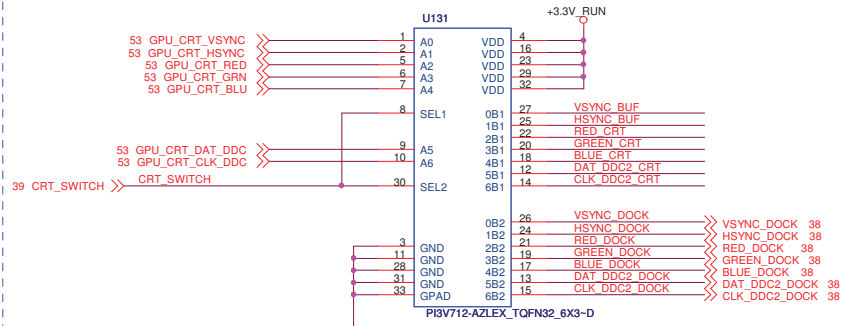
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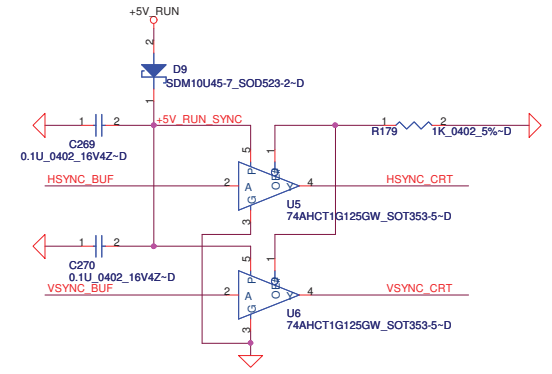
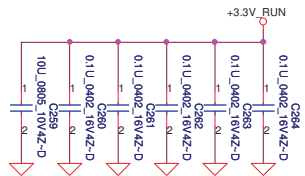
<b>Compal Electronics, Inc.</b>			
<b>Display port</b>			
Size	Document Number	Rev	
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### VGA SW for MB/DOCK



SEL1/SEL2	Chanel	Source
0	A=B1	MB
1	A=B2	APR/SPR



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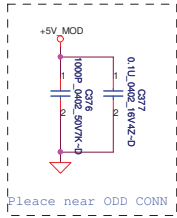
**Compal Electronics, Inc.**

**CRT/Video switch**

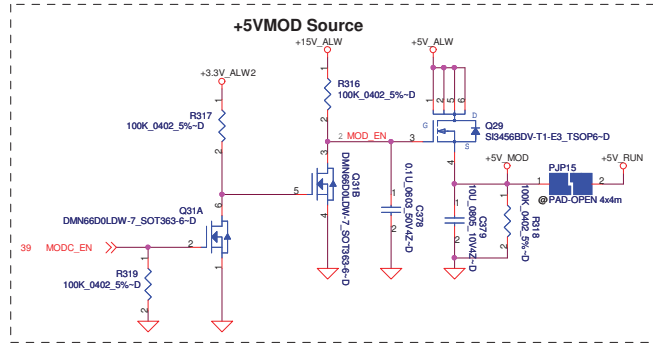
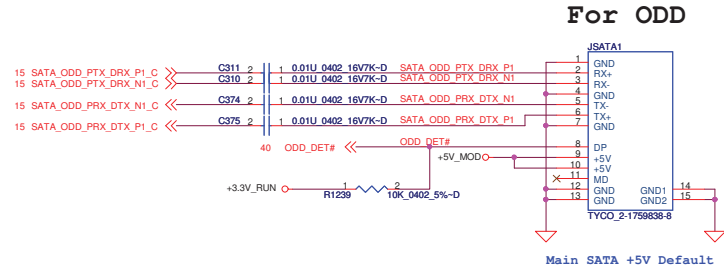
**LA-5573P**

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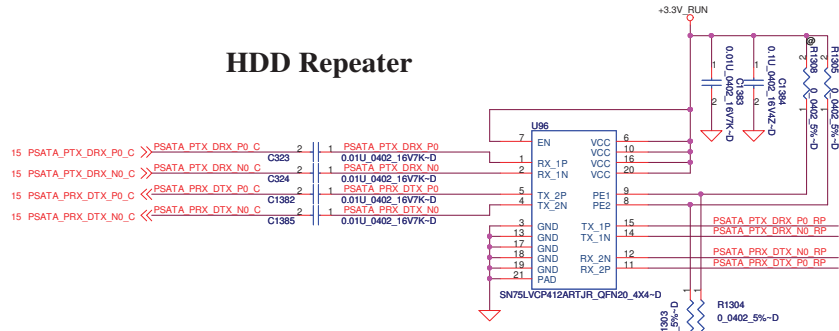
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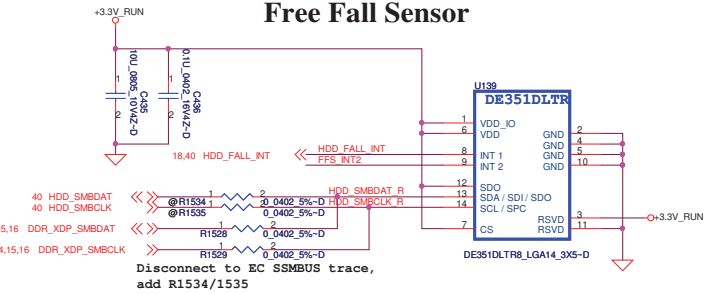
Please near ODD CONN



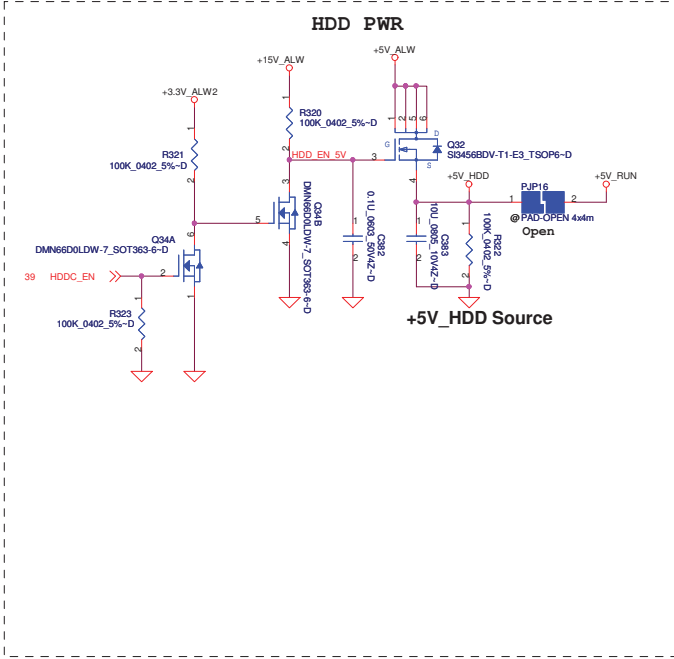
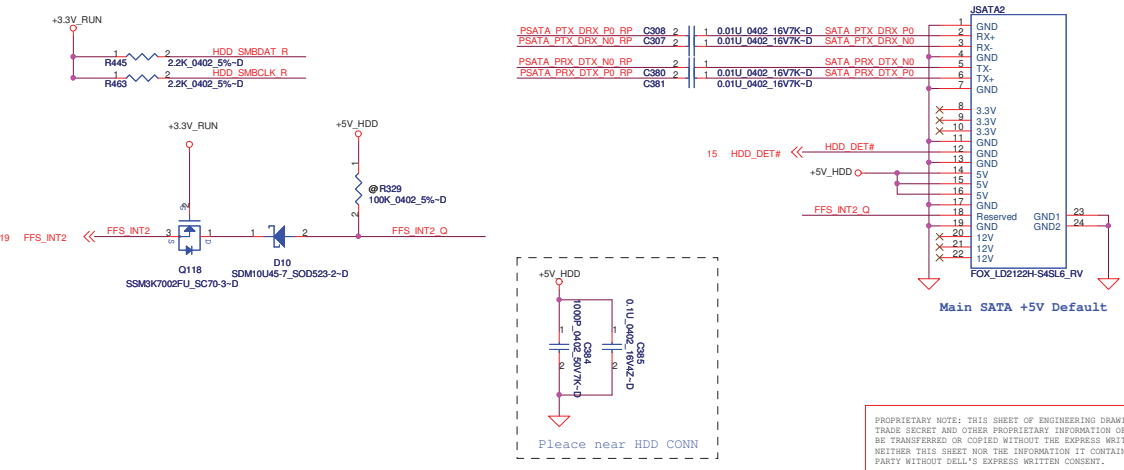
### HDD Repeater



### Free Fall Sensor



### For HDD Temp.



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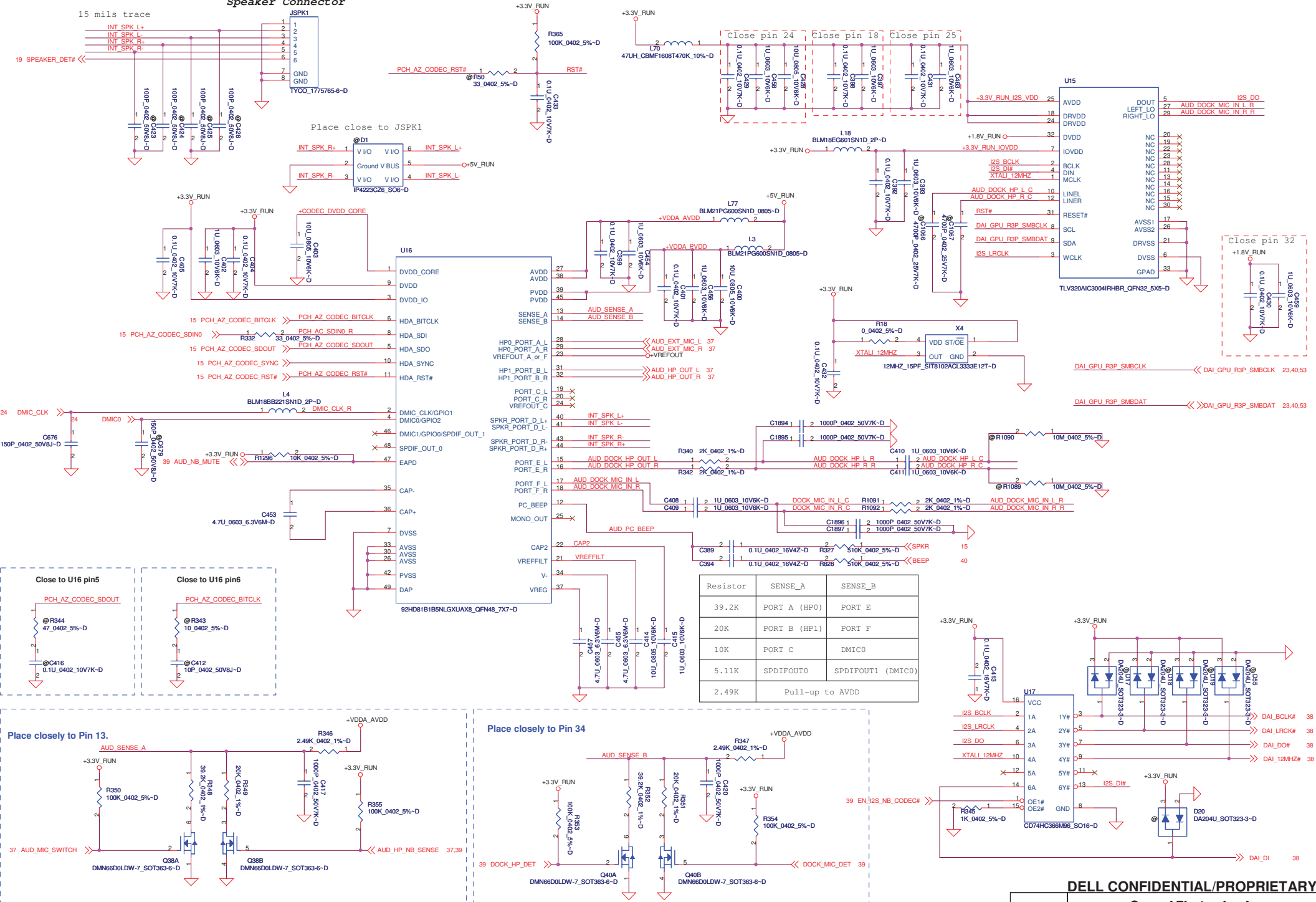
Compal Electronics, Inc.

File		ODD/HDD CONNECTOR	
Size	Document Number	LA-5573P	
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**Speaker Connector**



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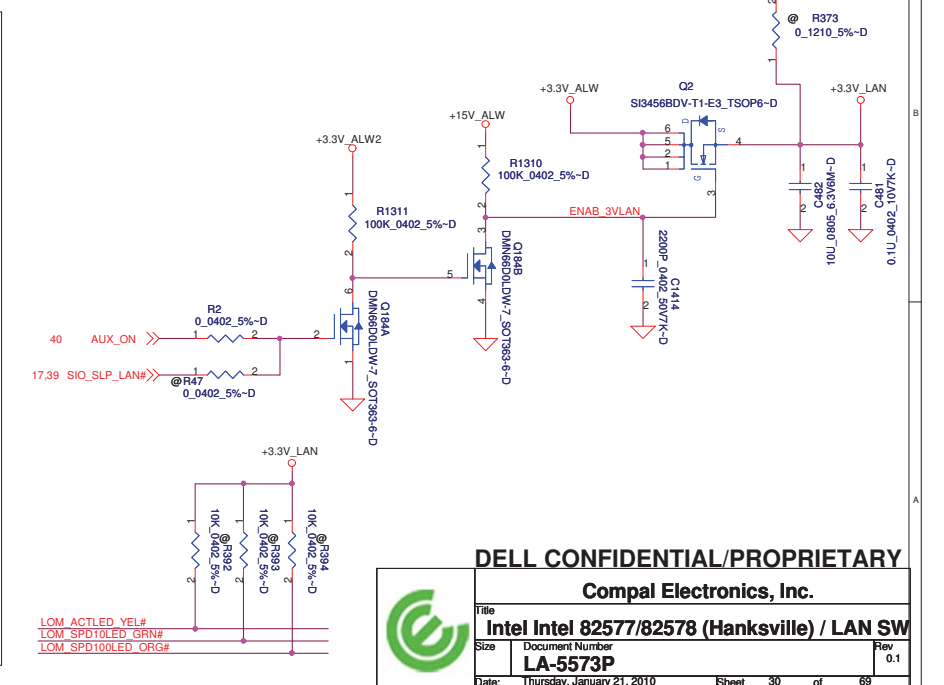
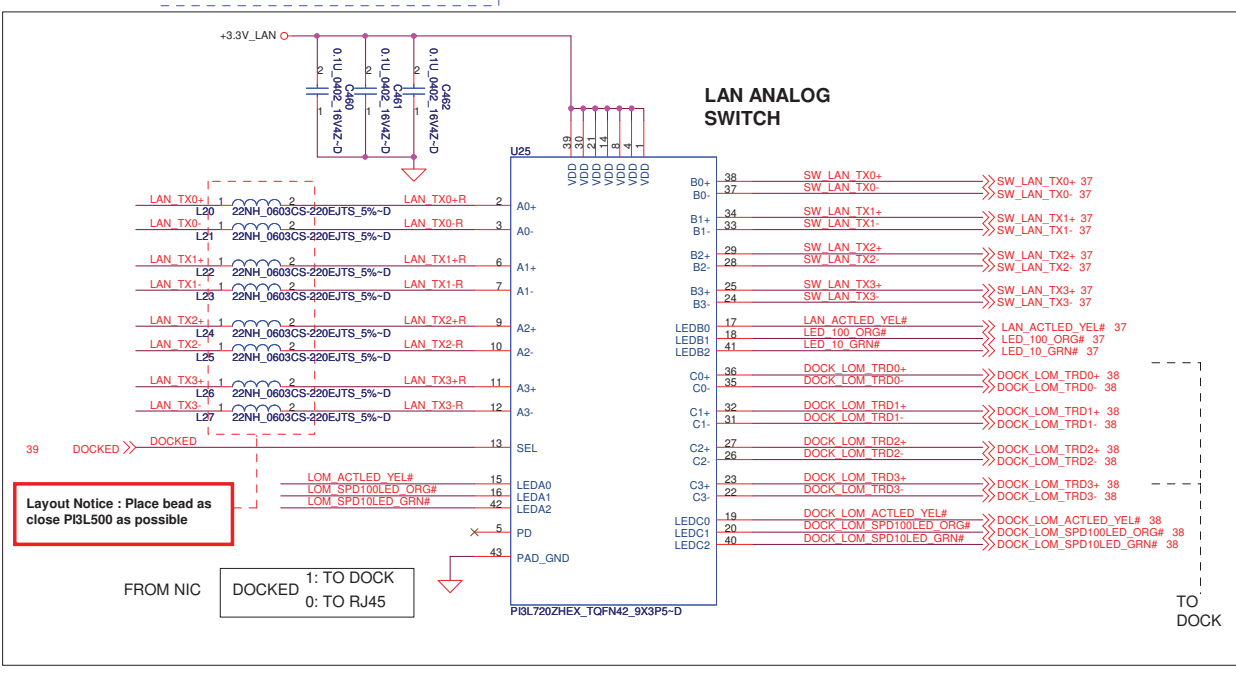
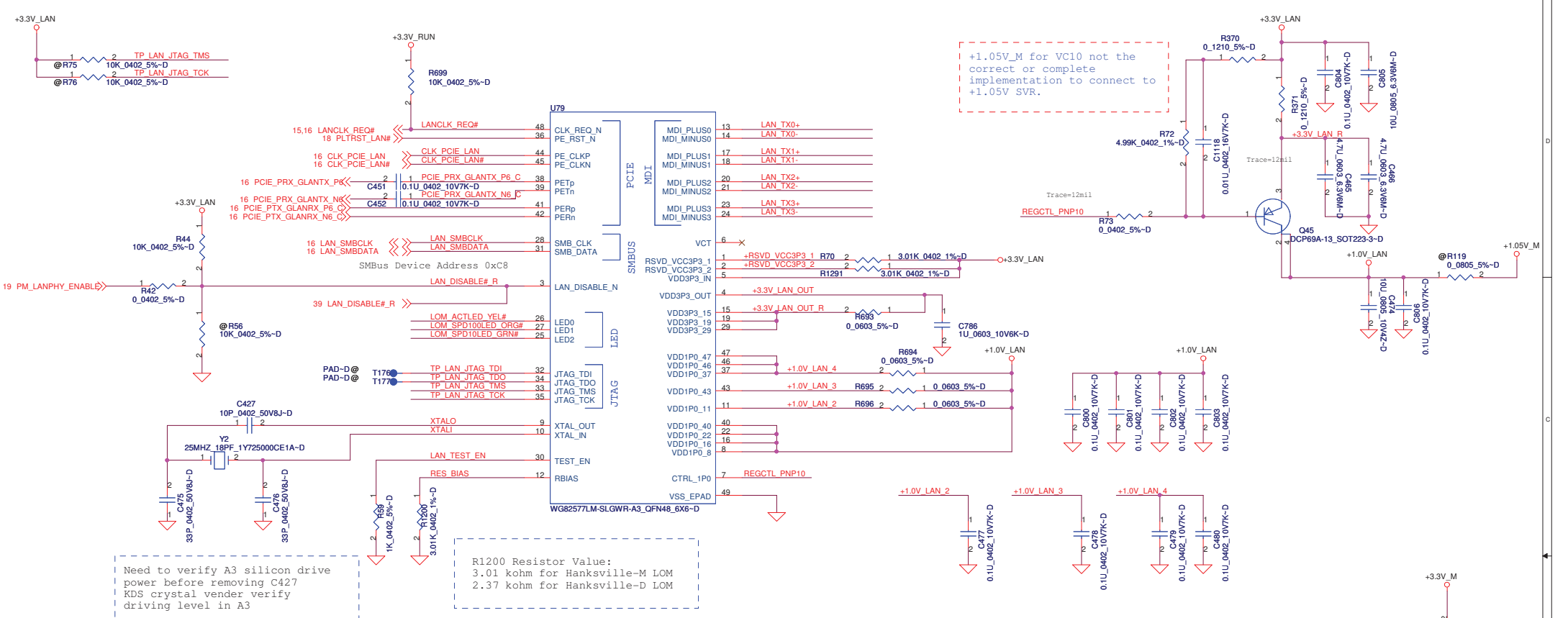
**Compal Electronics, Inc.**

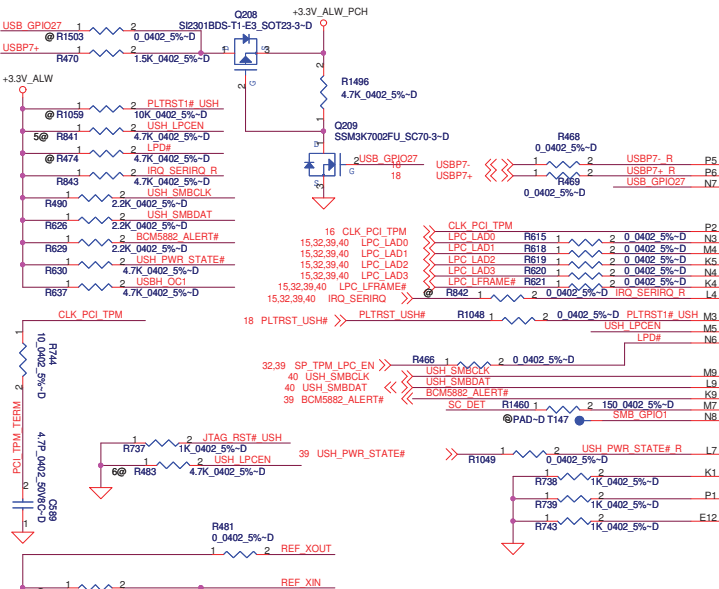
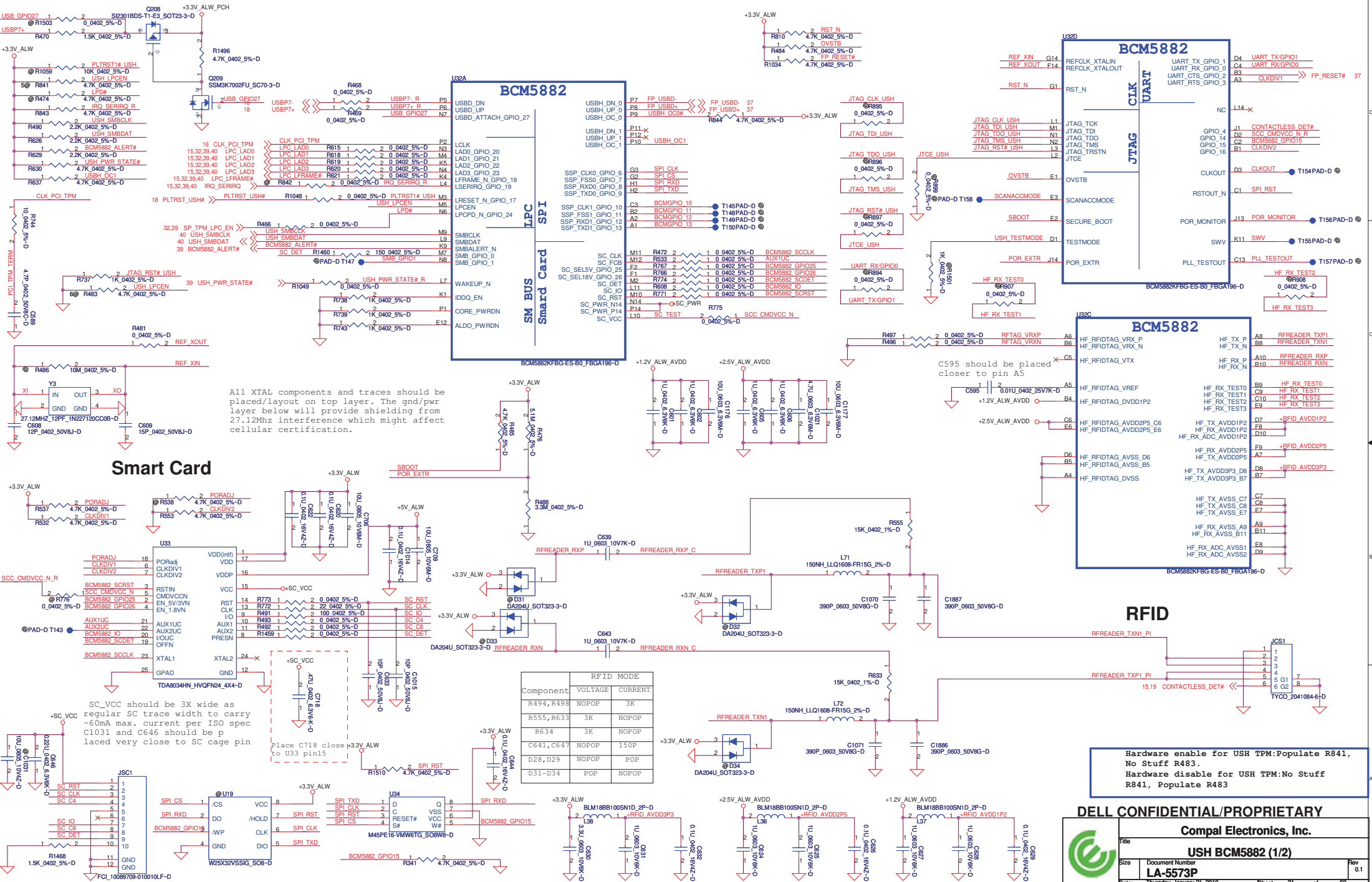
**Azalia (HD) Codec**

**LA-5573P**

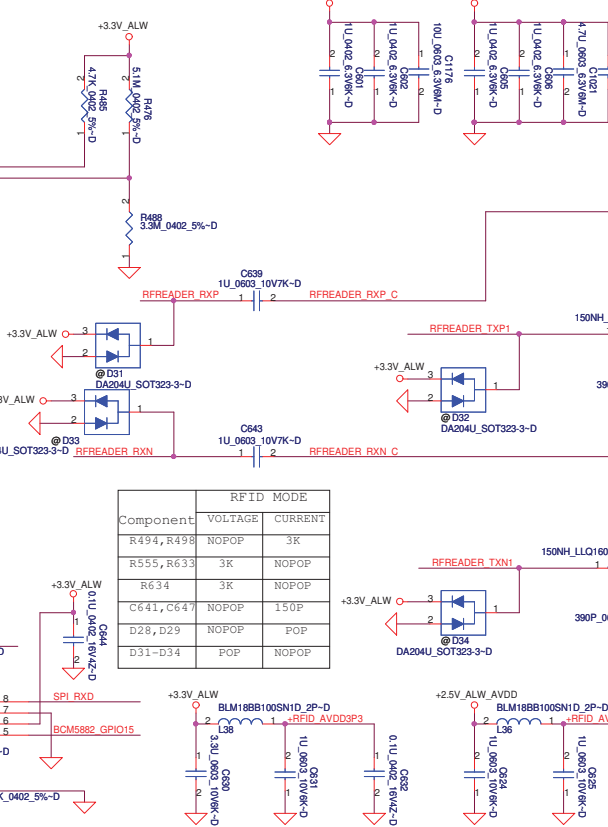
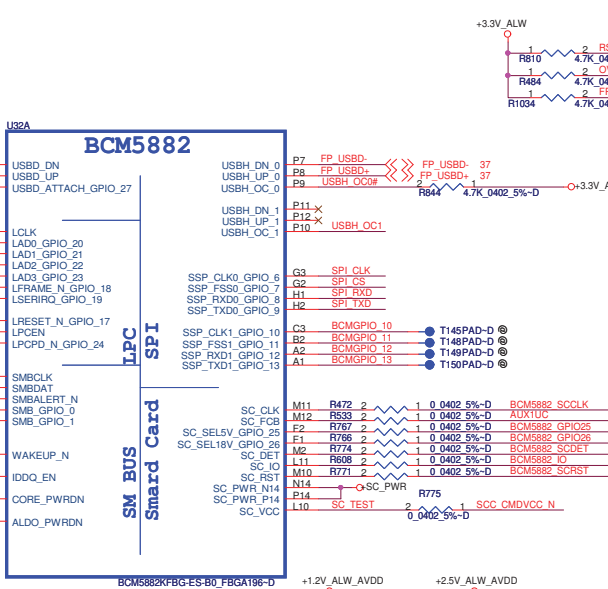
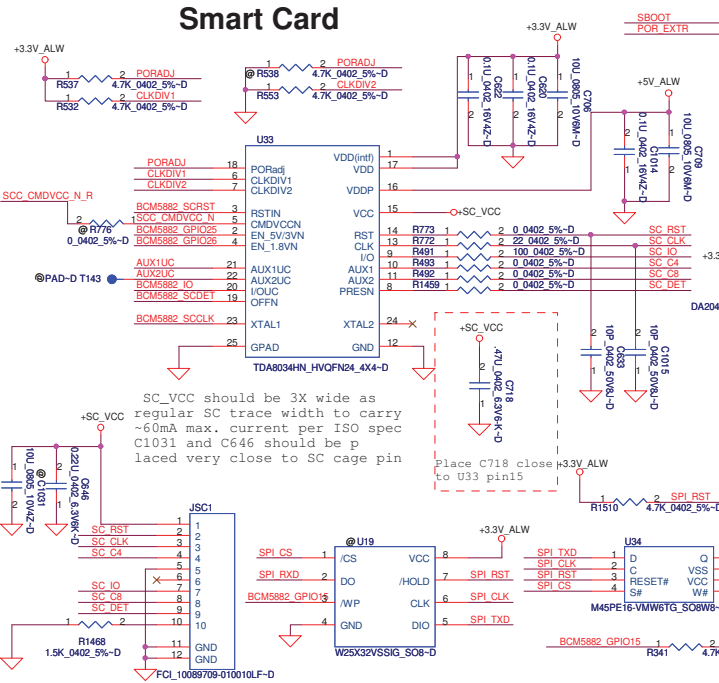
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 Date: Thursday, January 21, 2010 Sheet 29 of 69

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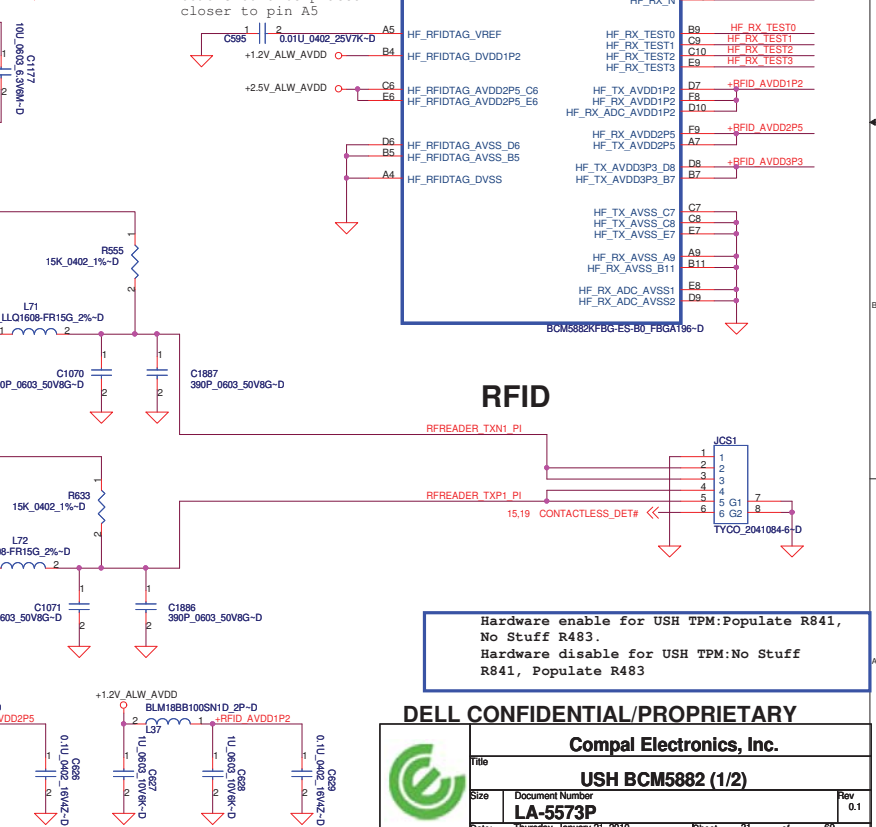
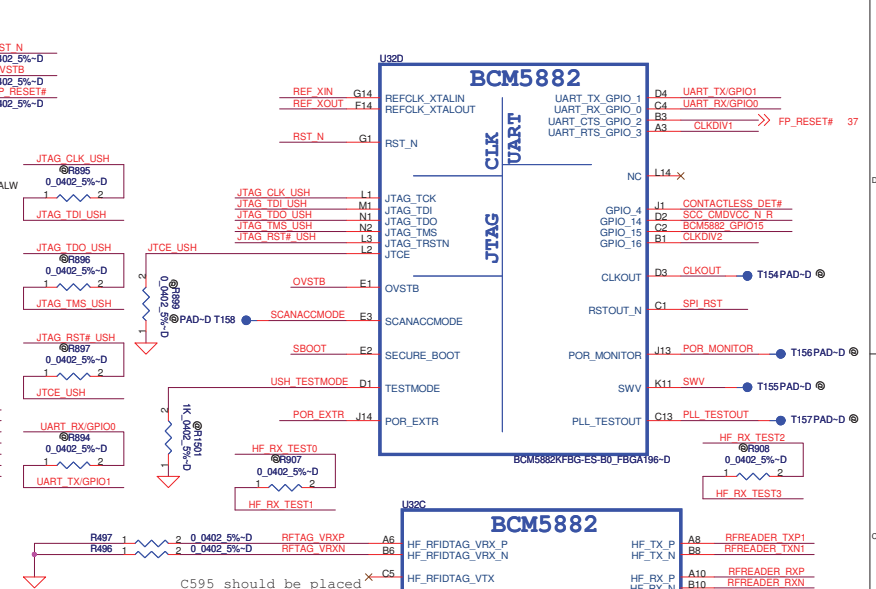




All XTAL components and traces should be placed/layout on top layer. The gnd/pwr layer below will provide shielding from 27.12Mhz interference which might affect cellular certification.



Component	VOLTAGE	CURRENT
R494, R498	NOPOP	3K
R555, R633	3K	NOPOP
R634	3K	NOPOP
C641, C647	NOPOP	150P
D28, D29	NOPOP	POP
D31-D34	POP	NOPOP



Hardware enable for USH TPM: Populate R841, No Stuff R483.  
Hardware disable for USH TPM: No Stuff R841, Populate R483

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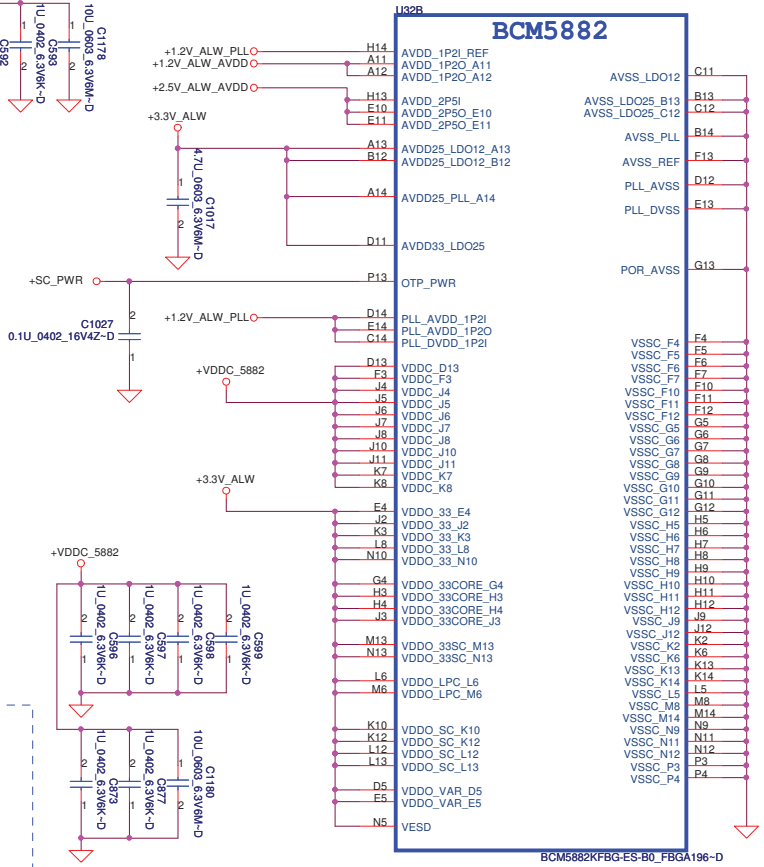
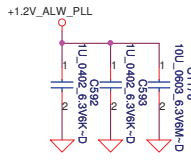
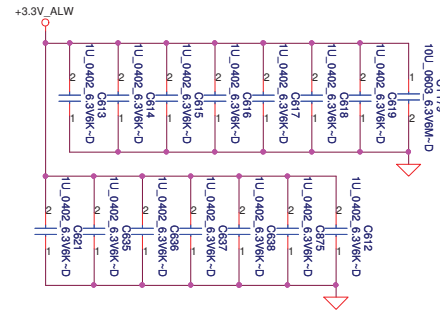
**Compal Electronics, Inc.**

**USH BCM5882 (1/2)**

File: \_\_\_\_\_  
 Size: \_\_\_\_\_ Document Number: **LA-5573P** Rev: 0.1  
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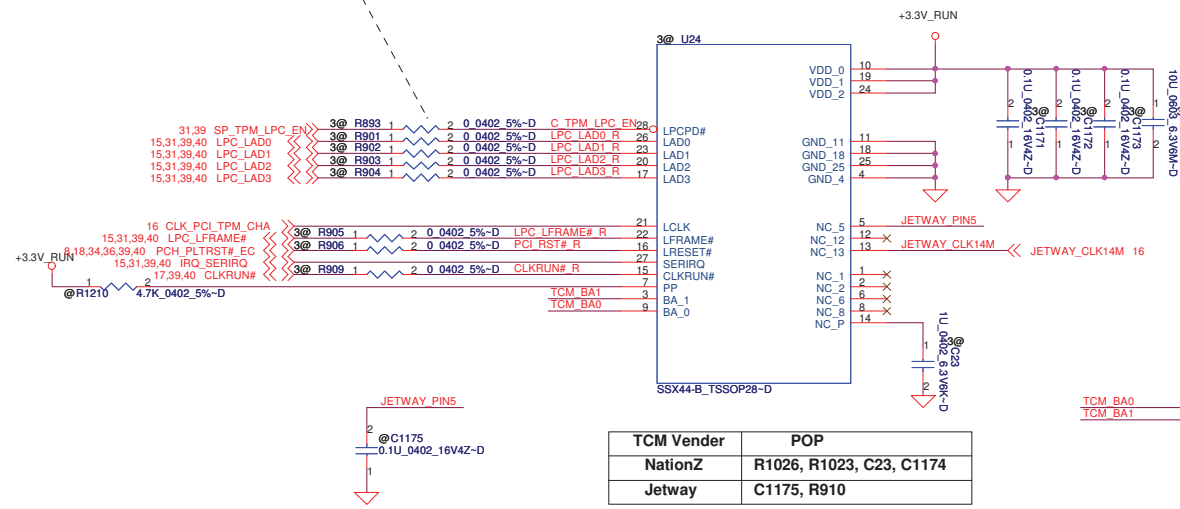


USH BCM5882 and China TCM Z8H172T Option				
PART/PIN	Ref Des	TCM Enable	TPM Enable	ALL TPM/TCM Disable
TCM circuit	All 3@	POP	@	@
USH_LPCEN	PU R841	@	POP	@
PD R483	POP	@	@	@
SIO 5028 ->SP_TPM_LPC_EN	PU R788	@	@	@
PCH GPIO39 ->TPM_ID1	PU R787	@	@	POP
PD R339	POP	POP	POP	@
PCH GPIO38 ->TPM_ID0	PU R273	POP	POP	@
PD R922	@	@	@	POP



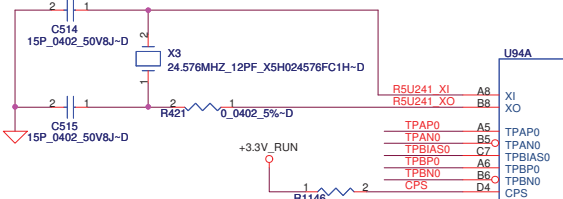
LOW: Power Down Mode  
High: Working Mode

China TCM: NationZ & Jetway co-lay

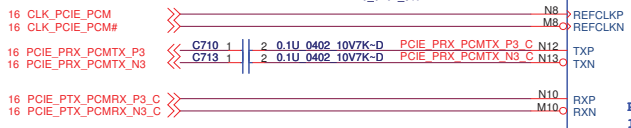




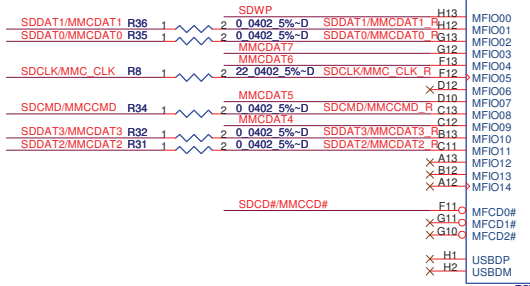
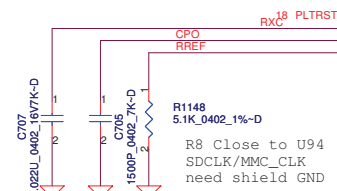
Crystal close to U94



C710, C713 as close as possible to U94



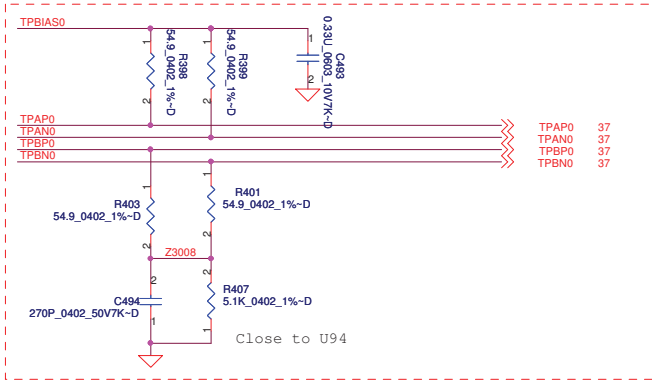
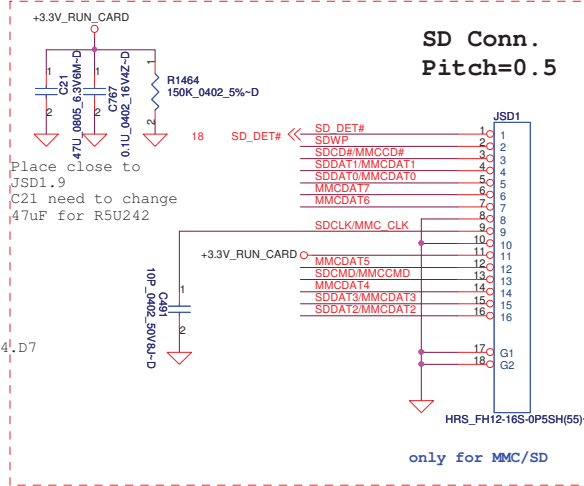
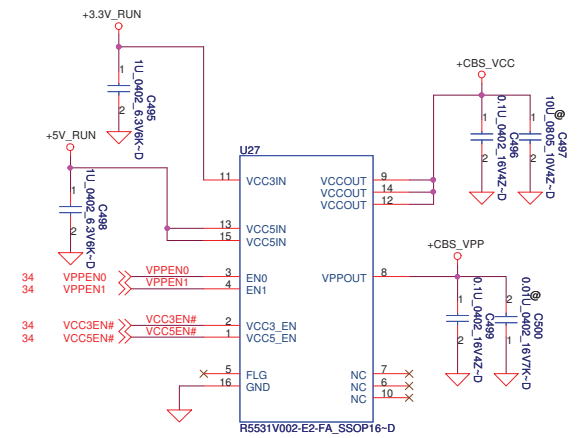
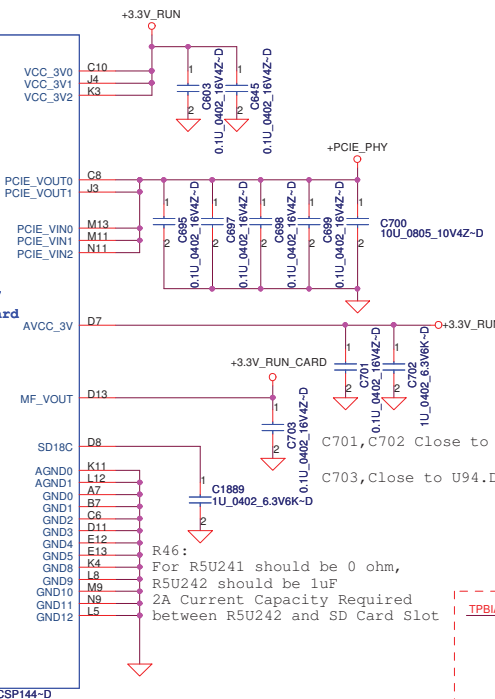
C707, C705, R1148 as close as possible to U94



MFIO Pin Assignment Table

MFIO	SD8	XD	MS8
00	WP	D7	BS
01	D1	D6	-
02	D0	D5	D1
03	D7	D4	-
04	D6	D3	D5
<b>05</b>	<b>CLK</b>	<b>D2</b>	<b>D0</b>
06	-	D1	-
07	D5	D0	D4
08	CMD	WP#	D2
09	D4	WE#	D6
10	D3	ALE	D3
11	D2	CLE	-
12	-	CE#	-
13	-	RE#	D7
<b>14</b>	-	R/B#	<b>CLK</b>

C645, Close to U94.C10  
 C603, Close to U94.J4/K3  
 C695, Close to U94.M13  
 C697, Close to U94.M11/N11  
 C698, Close to U94.J3  
 C699, Close to U94.C8

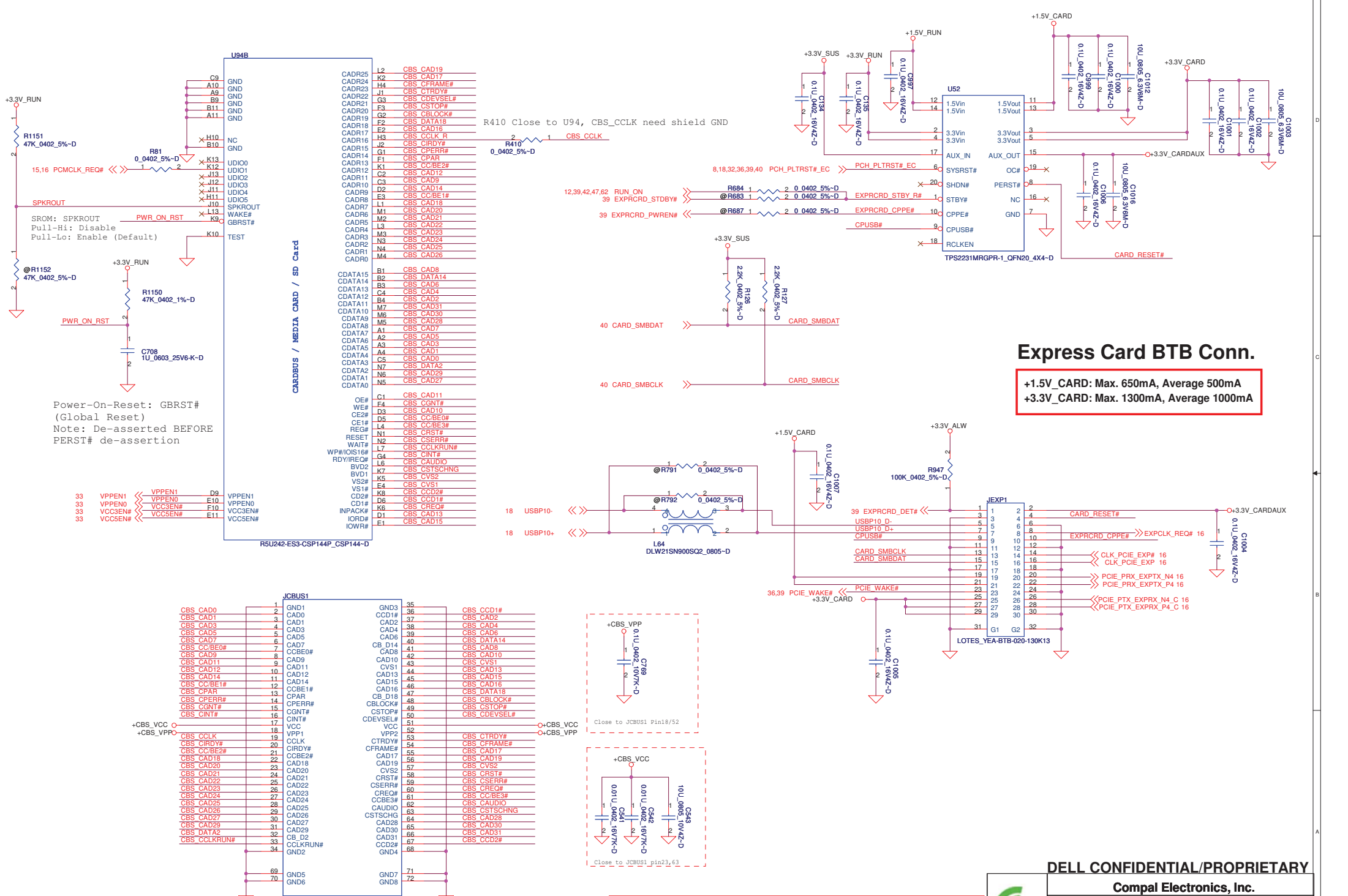


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 Size: Document Number LA-5573P  
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### Express Card BTB Conn.

**+1.5V\_CARD: Max. 650mA, Average 500mA**  
**+3.3V\_CARD: Max. 1300mA, Average 1000mA**



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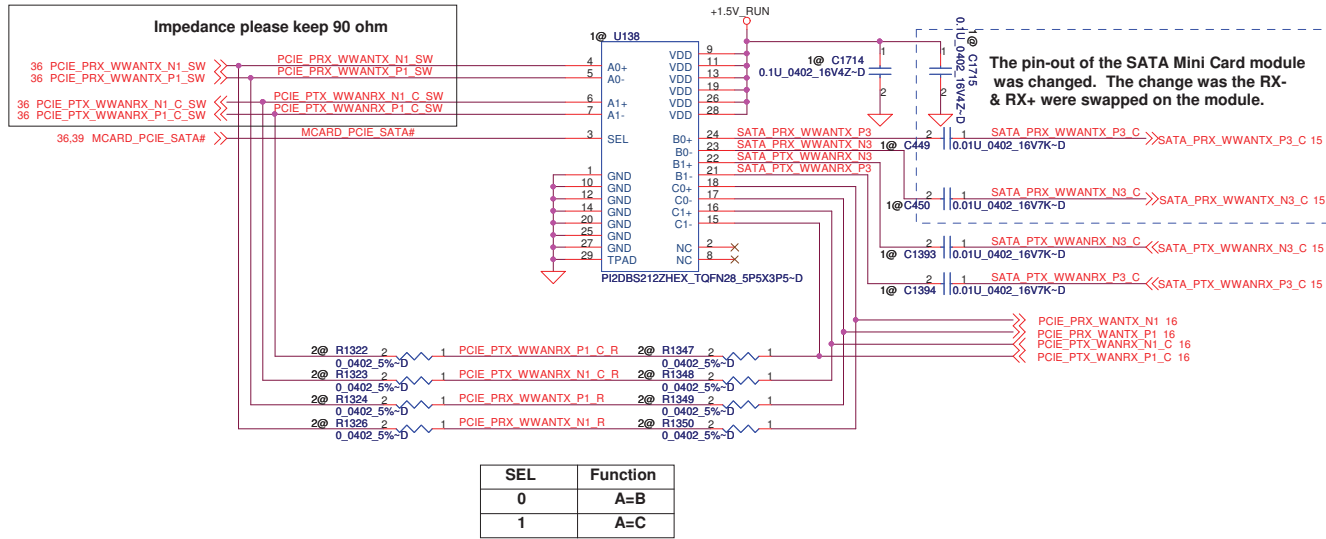
**Compal Electronics, Inc.**

Title			RSU242 (2/2)		
Size	Document Number	Rev			0.1
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# For Asics placement estimate

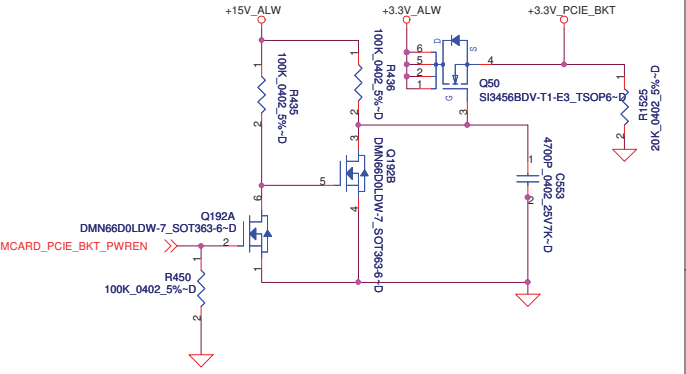
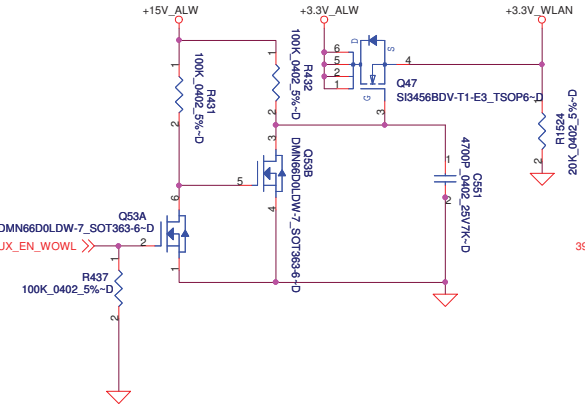
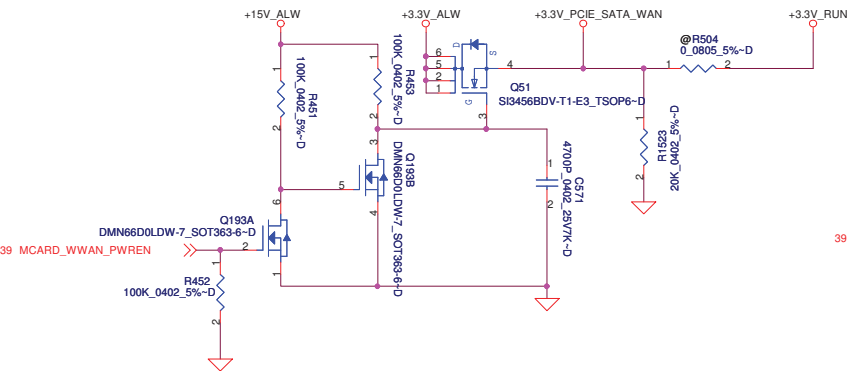
# PCIE/SATA SW for Mini card1



## Power Control for Mini card1

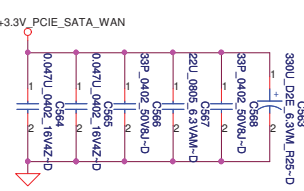
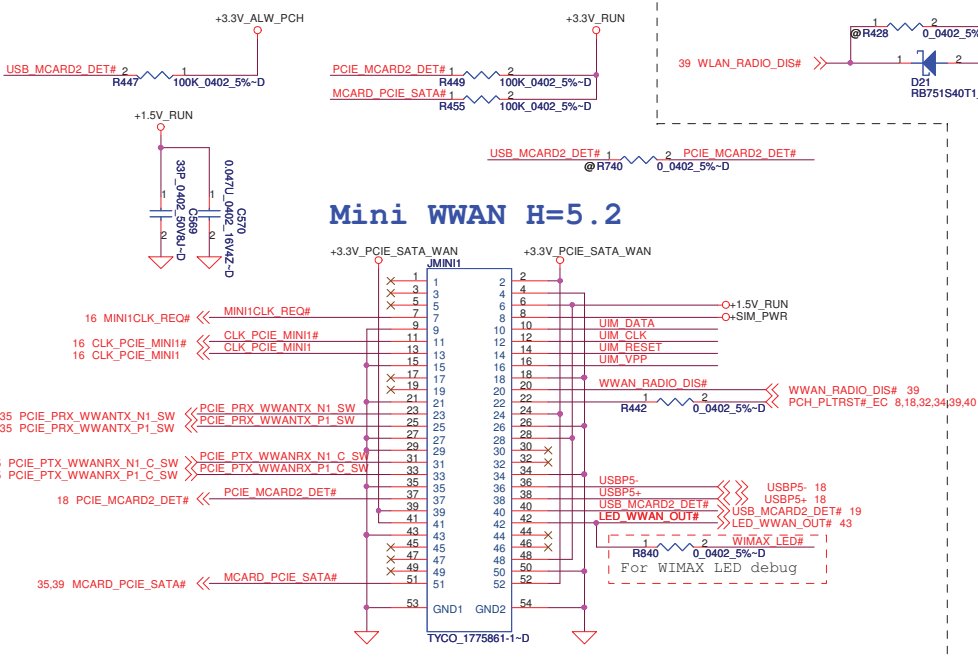
## Power Control for Mini card2

## Power Control for Mini card3

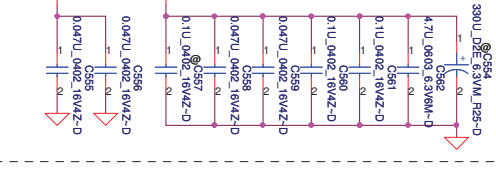
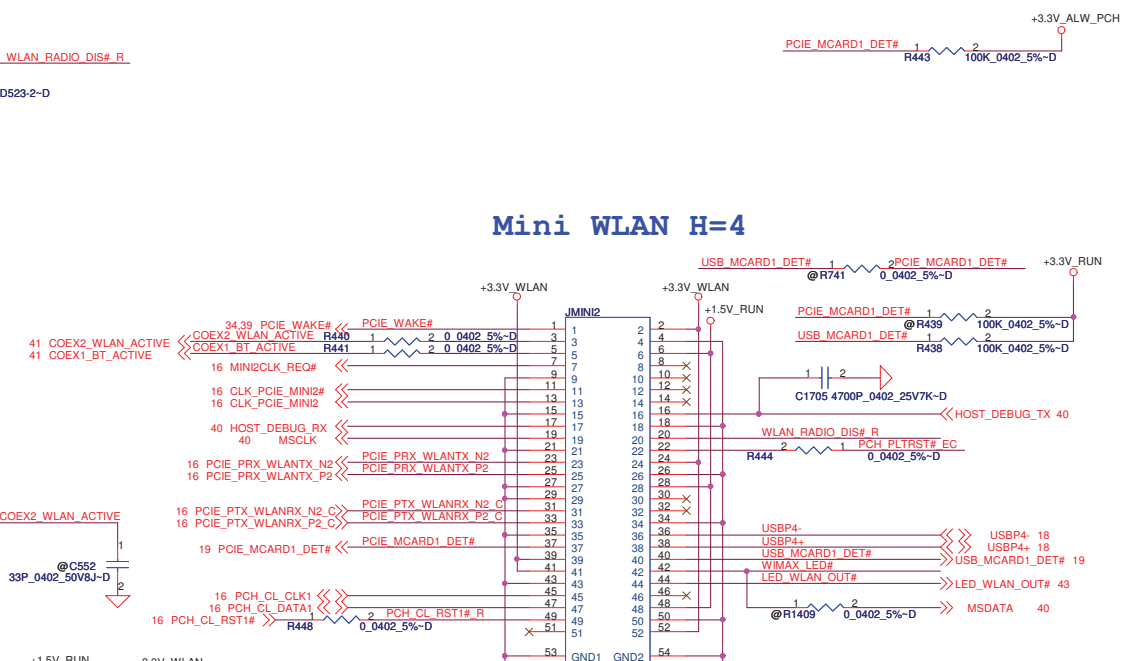


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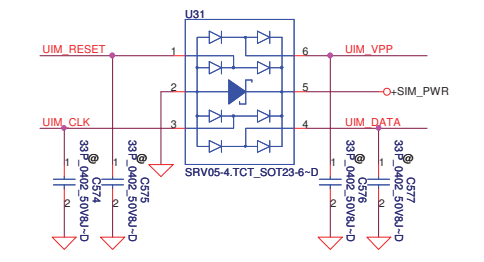
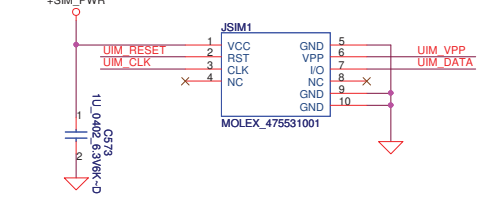




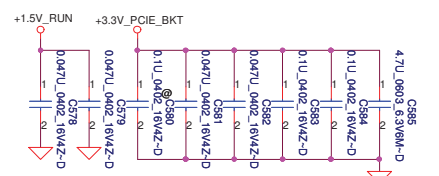
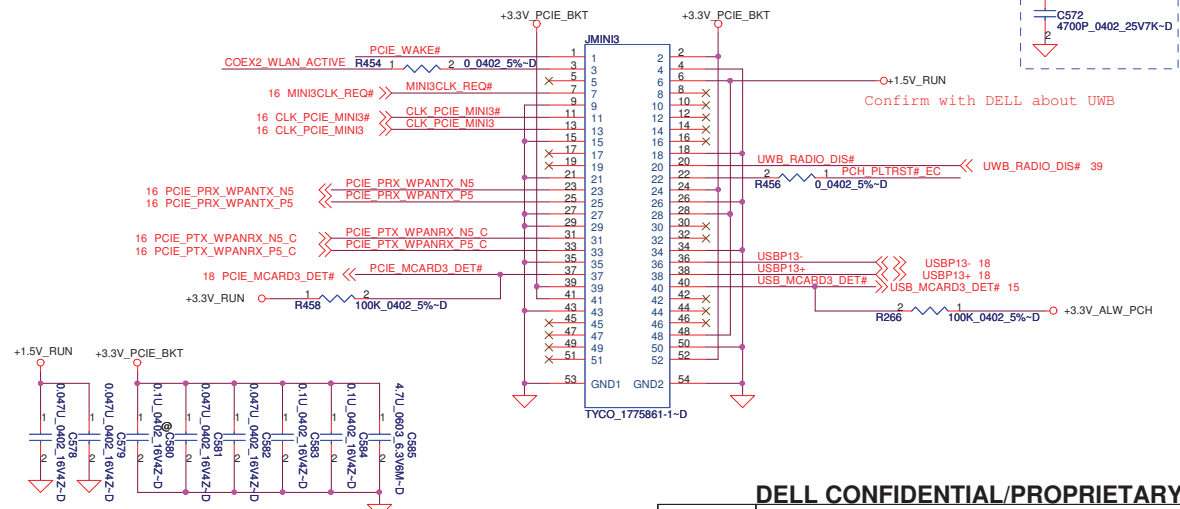
PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+~9%	1000	750	
+3.3Vaux	+~9%	330	250	250 (Wake enable) 5 (Not wake enable)
+1.5V	+~5%	500	375	NA



### SIM Card Push-Push



### PCIE/BKT Card H=4



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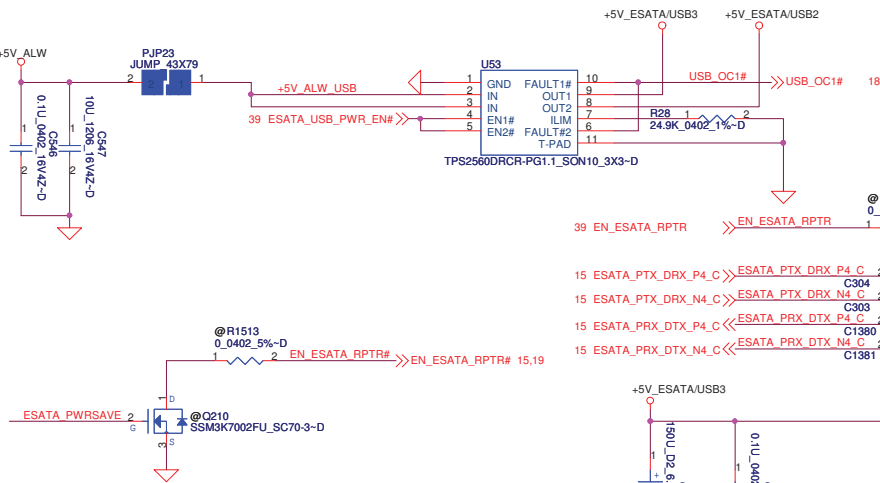
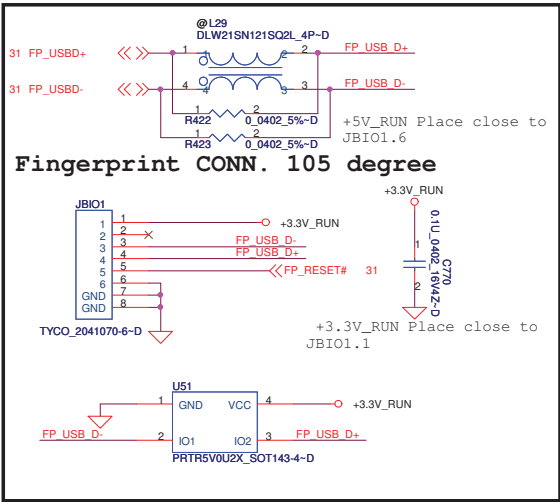
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**Mini Card**

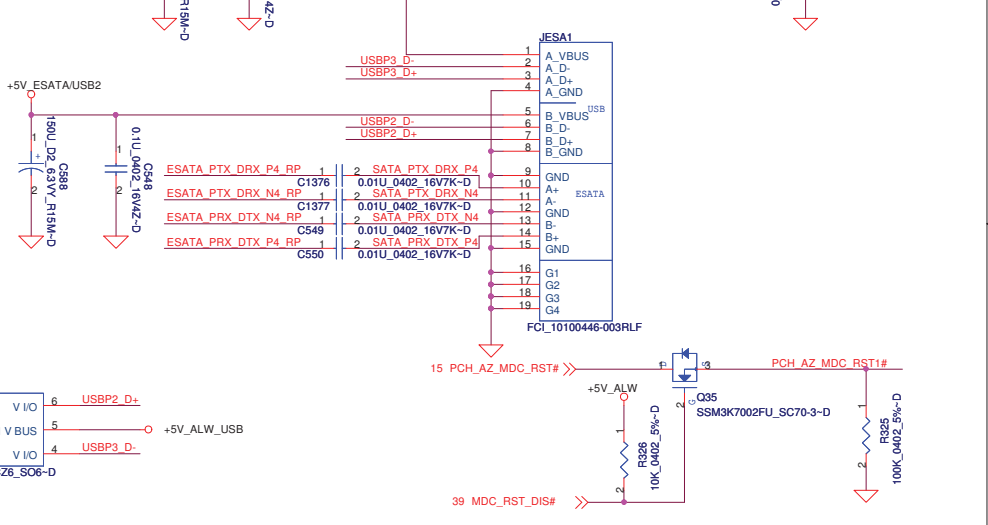
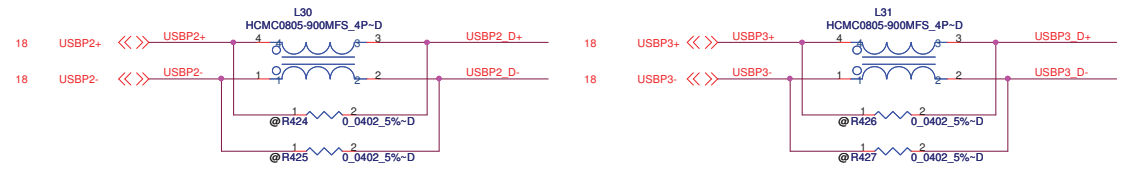
**LA-5573P**

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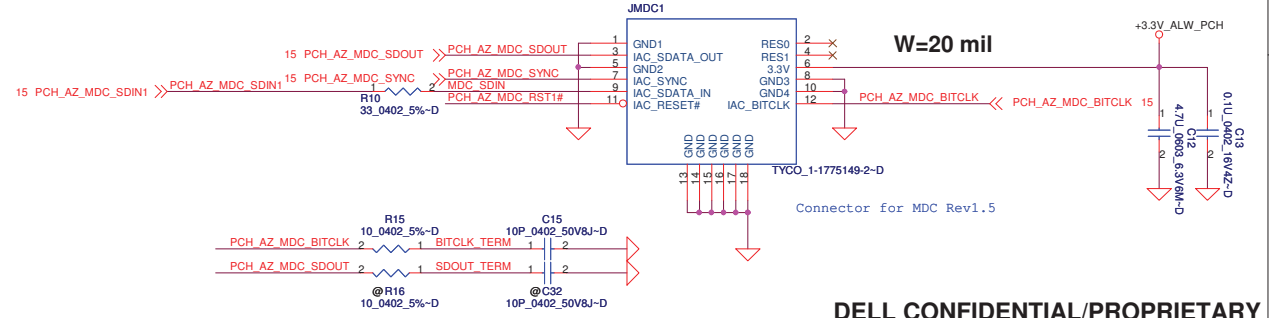
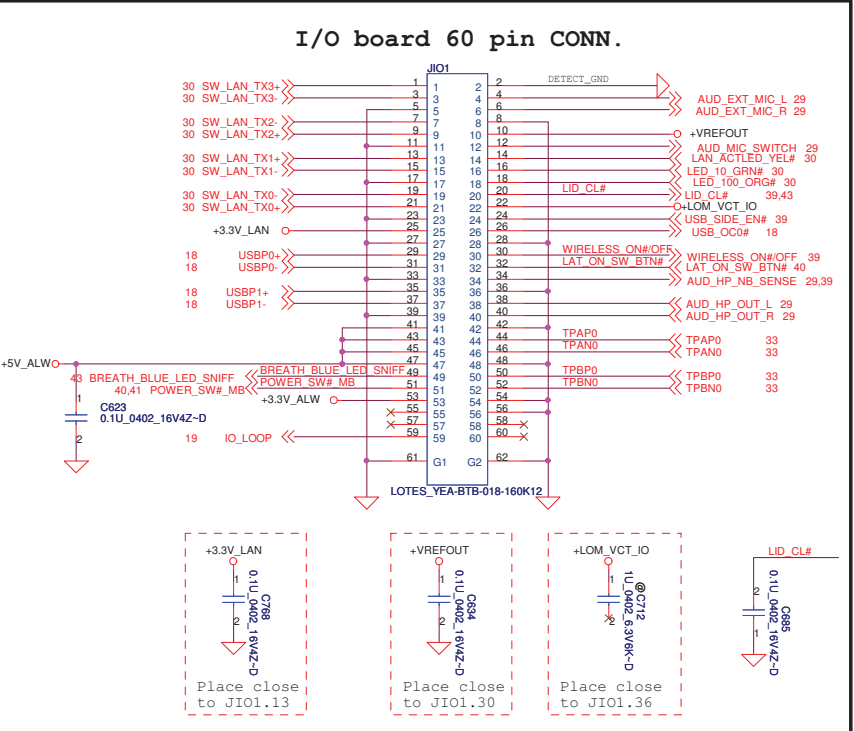
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### ESATA Repeater



### MDC CONN. H=5.5, Pitch=0.8



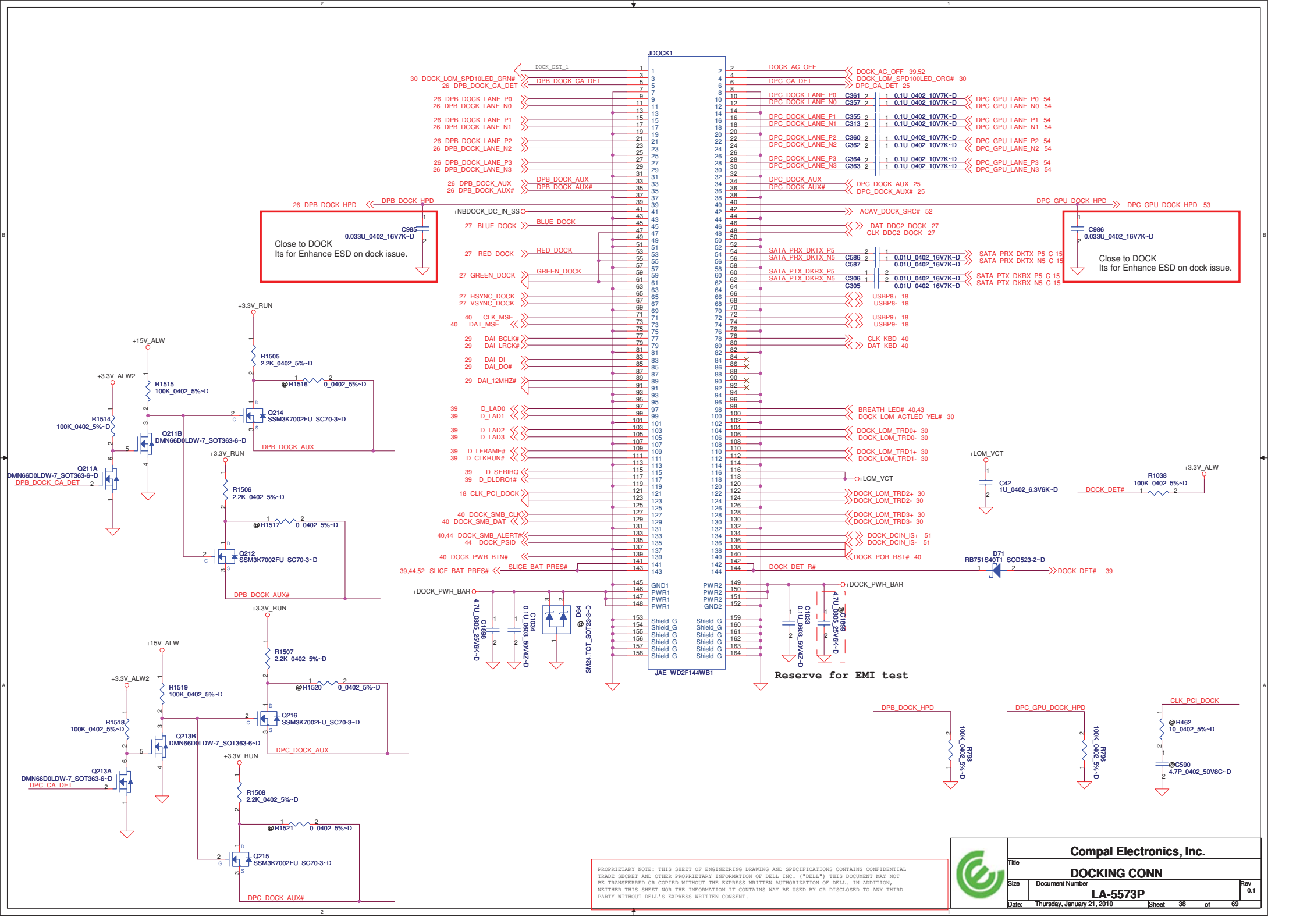
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## USB 2.0 PORT

Size Document Number  
**LA-5573P**  
 Date: Thursday, January 21, 2010 Sheet 37 of 69

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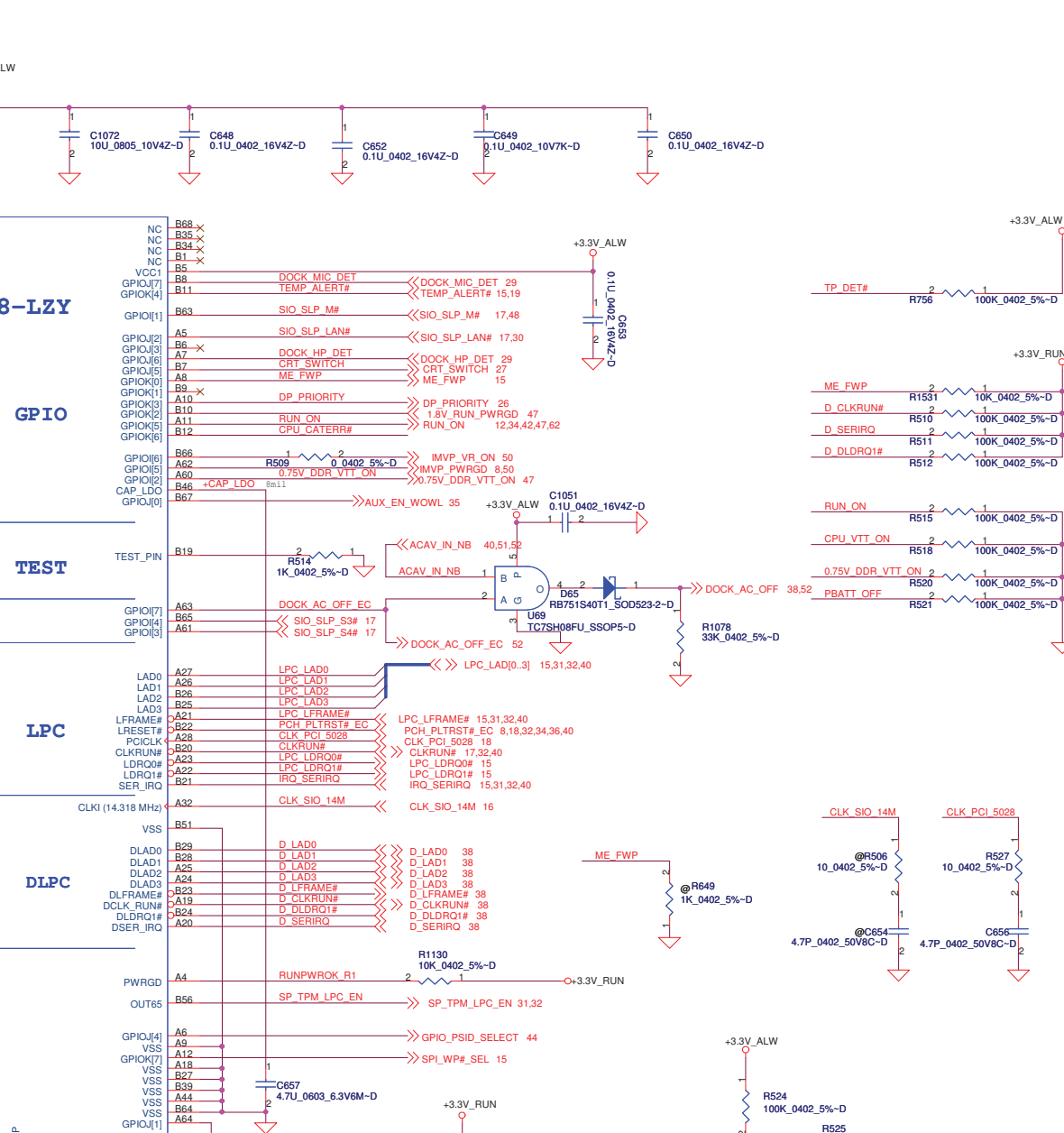
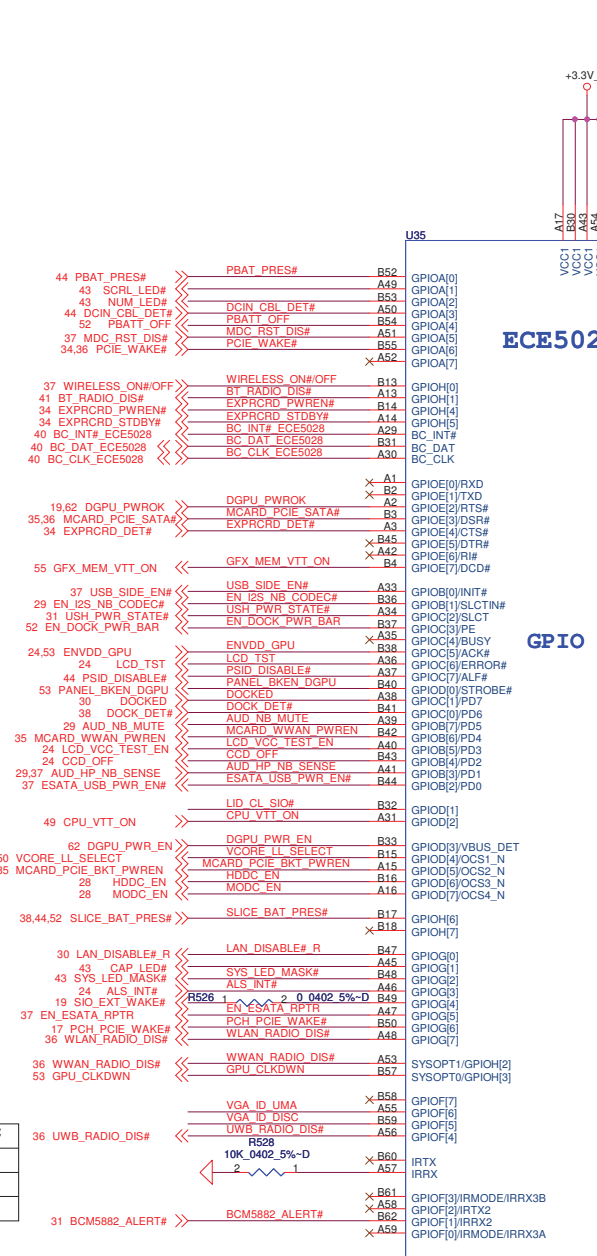
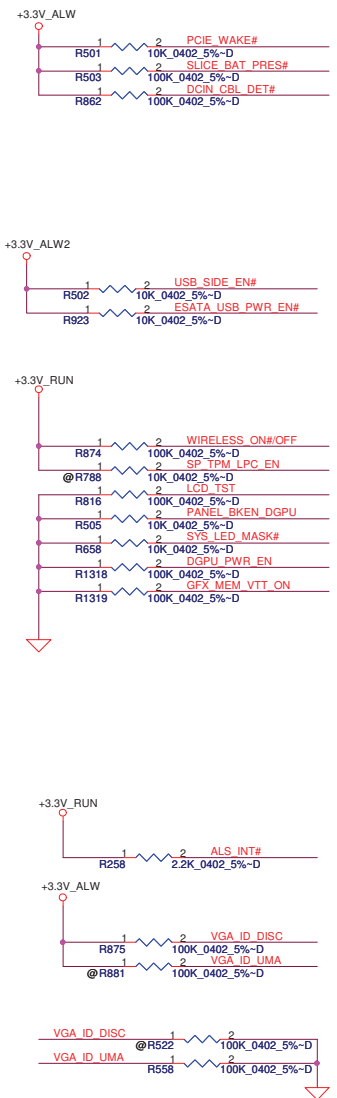
Close to DOCK  
Its for Enhance ESD on dock issue.

Close to DOCK  
Its for Enhance ESD on dock issue.

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<b>Compal Electronics, Inc.</b>			
<b>DOCKING CONN</b>			
<b>LA-5573P</b>			
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	VGA_ID_UMA	VGA_ID_DISC
Discrete	0	1
UMA	1	0
SG	1	1

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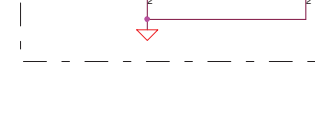
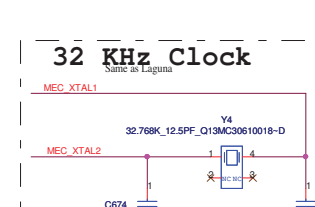
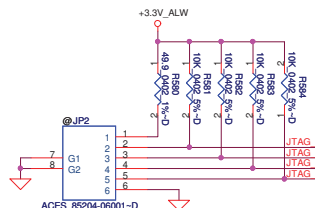
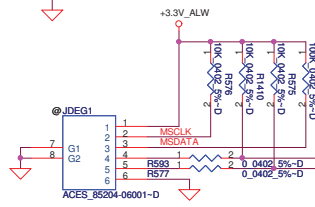
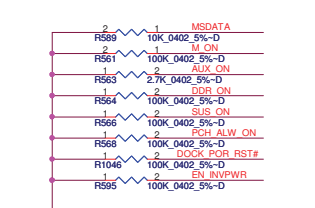
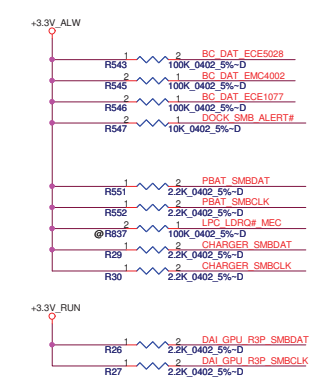
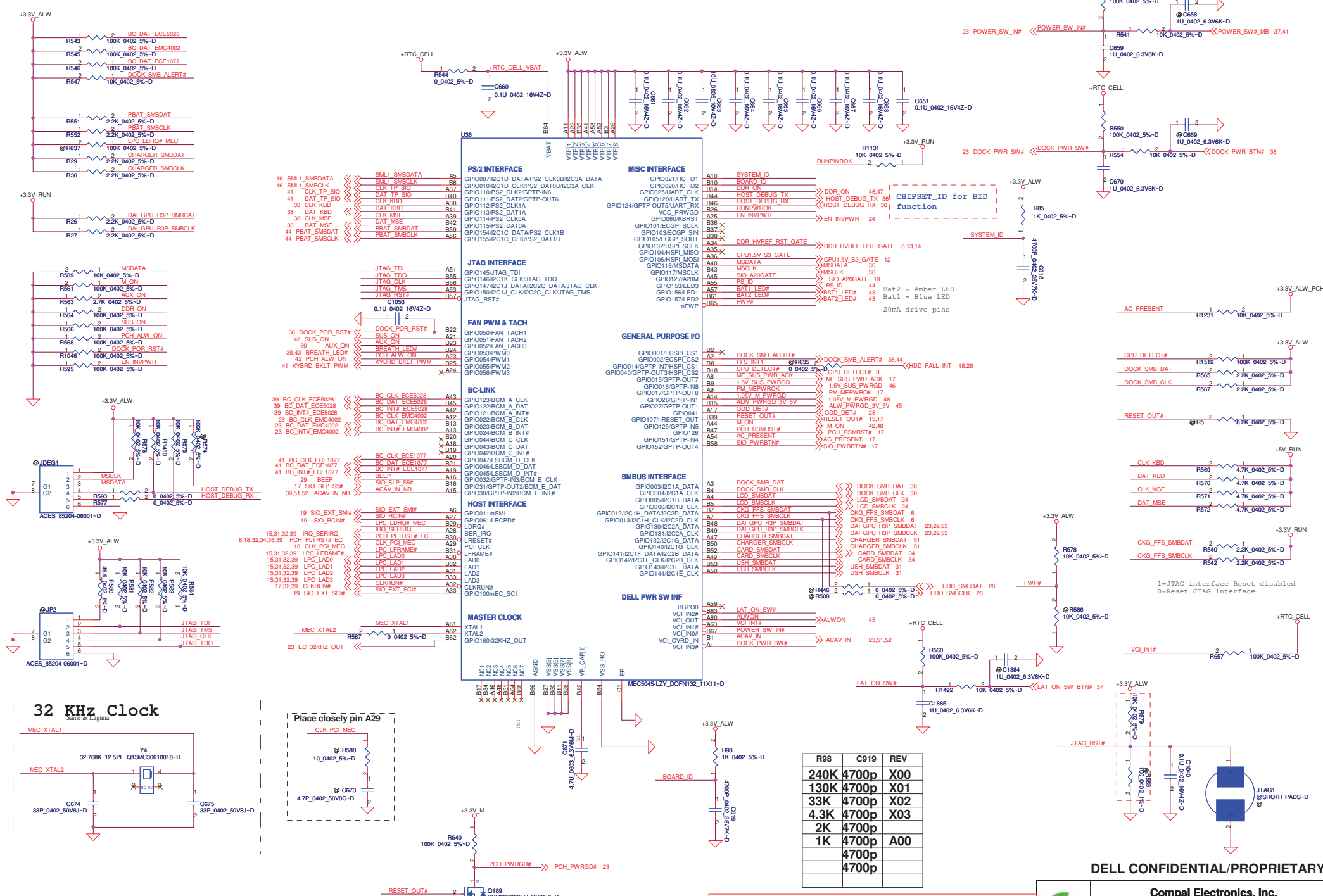
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**Compal Electronics, Inc.**

**ECE5028**

**LA-5573P**

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**PS/2 INTERFACE**

16 SML1_SMBDATA	SML1_SMBDATA	A5
16 SML1_SMBCLK	SML1_SMBCLK	B8
41 CLK_TP_SIO	CLK_TP_SIO	A37
41 DAT_TP_SIO	DAT_TP_SIO	B40
38 CLK_KBD	CLK_KBD	A39
38 DAT_KBD	DAT_KBD	B41
38 CLK_MSE	CLK_MSE	A39
38 DAT_MSE	DAT_MSE	B42
44 PBAT_SMBDAT	PBAT_SMBDAT	B59
44 PBAT_SMBCLK	PBAT_SMBCLK	A56

**JTAG INTERFACE**

1 JTAG_TDI	JTAG_TDI	A51
1 JTAG_TDO	JTAG_TDO	B55
1 JTAG_TMS	JTAG_TMS	B56
1 JTAG_RST#	JTAG_RST#	B57

**FAN PWM & TACH**

38 DOCK_POR_RST#	DOCK_POR_RST#	B22
42 SUS_ON	SUS_ON	A21
30 AUX_ON	AUX_ON	B23
38.43 BREATH_LED#	BREATH_LED#	B24
42 PCH_ALW_ON	PCH_ALW_ON	A23
41 KYBRD_BKLT_PWM	KYBRD_BKLT_PWM	B22

**BC-LINK**

39 BC_CLK_ECE5028	BC_CLK_ECE5028	A43
39 BC_DAT_ECE5028	BC_DAT_ECE5028	B45
39 BC_INT#_ECE5028	BC_INT#_ECE5028	A42
23 BC_CLK EMC4002	BC_CLK EMC4002	A12
23 BC_DAT EMC4002	BC_DAT EMC4002	B13
23 BC_INT#_EMC4002	BC_INT#_EMC4002	A13

**HOST INTERFACE**

19 SIO_EXT_SMI#	SIO_EXT_SMI#	A6
19 SIO_RCIN#	SIO_RCIN#	A27
19 IRO_SERRIO	IRO_SERRIO	B26
19 IRO_SERRIO_MEC	IRO_SERRIO_MEC	B26
19 PCH_PLTRST#_EC	PCH_PLTRST#_EC	B30
19 CLK_PCI_MEC	CLK_PCI_MEC	A20
19 LFRAME#	LFRAME#	B31
19 LPC_LAD0	LPC_LAD0	A30
19 LPC_LAD1	LPC_LAD1	A31
19 LPC_LAD2	LPC_LAD2	A32
19 LPC_LAD3	LPC_LAD3	A33
19 CLRUN#	CLRUN#	A34
19 SIO_EXT_SCI#	SIO_EXT_SCI#	A35

**MASTER CLOCK**

MEC_XTAL1	MEC_XTAL1	A61
MEC_XTAL2	MEC_XTAL2	A62
23 EC_32KHZ_OUT	EC_32KHZ_OUT	B62

**MISC INTERFACE**

GPIO021/RC_ID1	SYSTEM_ID	A10
GPIO020/RC_ID2	BOARD_ID	B10
GPIO025/UART_CLK	DDR_ON	46.47
GPIO110/PS2_CLK/GPTP-IN6	HOST_DEBUG_TX	36
GPIO111/PS2_DAT/GPTP-OUT6	HOST_DEBUG_RX	36
GPIO112/PS2_CLK1A	RUNPWROK	36
GPIO113/PS2_DAT1A	EN_INVPWR	24
GPIO114/PS2_CLK0A	DDR_HVREF_RST_GATE	8.13.14
GPIO115/PS2_DAT0A	CPU15V_S3_GATE	12
GPIO154/IC10_DATA/PF2_CLK1B	MISDATA	36
GPIO155/IC10_CLK/PF2_DAT1B	MISCLK	36
	SIO_A20GATE	19
	PS_ID	44
	BAT1_LED#	43
	BAT2_LED#	43
	nFWR#	20mA drive pins

**GENERAL PURPOSE I/O**

GPIO011/ECSP1_CS1	DOCK_SMB_ALERT#	38.44
GPIO002/ECSP1_CS2	CPU_DETECT#	8
GPIO014/GPTP-IN7/HSP1_CS1	ME_SUS_PWR_ACK	17
GPIO040/GPTP-OUT3/HSP1_CS2	ME_SUS_PWRACK	17
GPIO015/GPTP-OUT7	PM_WPWROK	17
GPIO016/GPTP-IN8	1.05V_M_PWROK	48
GPIO017/GPTP-OUT8	ALW_PWROK_3V_5V	45
GPIO026/GPTP-IN1	ODD_DET#	17
GPIO027/GPTP-OUT1	RESET_OUT#	15.17
GPIO107/HRESET_OUT	M_ON	42.48
GPIO125/GPTP-IN5	PCH_RSMRST#	17
GPIO128/GPTP-IN6	AC_PRESENT	17
GPIO151/GPTP-IN4	SIO_PWRBTN#	17
GPIO152/GPTP-OUT4		

**SMBUS INTERFACE**

GPIO031/IC21A_DATA	DOCK_SMB_DAT	38
GPIO032/IC21A_CLK	DOCK_SMB_CLK	38
GPIO005/IC21B_DATA	LCD_SMBDAT	24
GPIO006/IC21B_CLK	LCD_SMBCLK	24
GPIO130/IC22A_DATA	CKG_FFS_SMBDAT	6
GPIO131/IC22A_CLK	CKG_FFS_SMBCLK	6
GPIO132/IC22B_DATA	DAI_GPU_R3P_SMBDAT	23.29.53
GPIO133/IC22B_CLK	DAI_GPU_R3P_SMBCLK	23.29.53
GPIO141/IC21F_DATA/IC22B_DATA	CHARGER_SMBDAT	51
GPIO142/IC21F_CLK/IC22B_CLK	CHARGER_SMBCLK	51
GPIO143/IC21E_DATA	CARD_SMBDAT	34
GPIO144/IC21E_CLK	CARD_SMBCLK	34

**DELL PWR SW INF**

BGPO0	LAT_ON_SW#	45
VCI_IN#	ALWON	45
VCI_IN#	POWER_SW_IN#	45
VCI_IN#	ACAV_IN	23.51.52
VCI_IN#	DOCK_PWR_SW#	23.51.52

**DELL PWR SW INF**

NC1	VS22	B52
NC2	VS21	B51
NC3	VS20	B50
NC4	VS19	B49
NC5	VS18	B48
NC6	VS17	B47
NC7	VS16	B46
NC8	VS15	B45
NC9	VS14	B44
NC10	VS13	B43
NC11	VS12	B42
NC12	VS11	B41
NC13	VS10	B40
NC14	VS9	B39
NC15	VS8	B38
NC16	VS7	B37
NC17	VS6	B36
NC18	VS5	B35
NC19	VS4	B34
NC20	VS3	B33
NC21	VS2	B32
NC22	VS1	B31
NC23	VS0	B30

**SYSTEM ID**

A10	SYSTEM_ID	A10
B10	BOARD_ID	B10
B44	HOST_DEBUG_TX	36
B45	HOST_DEBUG_RX	36
B46	RUNPWROK	36
A25	EN_INVPWR	24
B36	DDR_HVREF_RST_GATE	8.13.14
A35	CPU15V_S3_GATE	12
A40	MISDATA	36
B43	MISCLK	36
A45	SIO_A20GATE	19
A52	PS_ID	44
B61	BAT1_LED#	43
B62	BAT2_LED#	43
B85	nFWR#	20mA drive pins

**GENERAL PURPOSE I/O**

B2	DOCK_SMB_ALERT#	38.44
B18	CPU_DETECT#	8
A8	ME_SUS_PWR_ACK	17
B9	ME_SUS_PWRACK	17
A9	PM_WPWROK	17
A14	1.05V_M_PWROK	48
A17	ALW_PWROK_3V_5V	45
B39	ODD_DET#	17
B39	RESET_OUT#	15.17
A44	M_ON	42.48
B47	PCH_RSMRST#	17
A54	AC_PRESENT	17
B58	SIO_PWRBTN#	17

**SMBUS INTERFACE**

A3	DOCK_SMB_DAT	38
B4	DOCK_SMB_CLK	38
A4	LCD_SMBDAT	24
B6	LCD_SMBCLK	24
B7	CKG_FFS_SMBDAT	6
A7	CKG_FFS_SMBCLK	6
B48	DAI_GPU_R3P_SMBDAT	23.29.53
B49	DAI_GPU_R3P_SMBCLK	23.29.53
A47	CHARGER_SMBDAT	51
B50	CHARGER_SMBCLK	51
B52	CARD_SMBDAT	34
A49	CARD_SMBCLK	34
B53	USH_SMBDAT	31
A50	USH_SMBCLK	31

**DELL PWR SW INF**

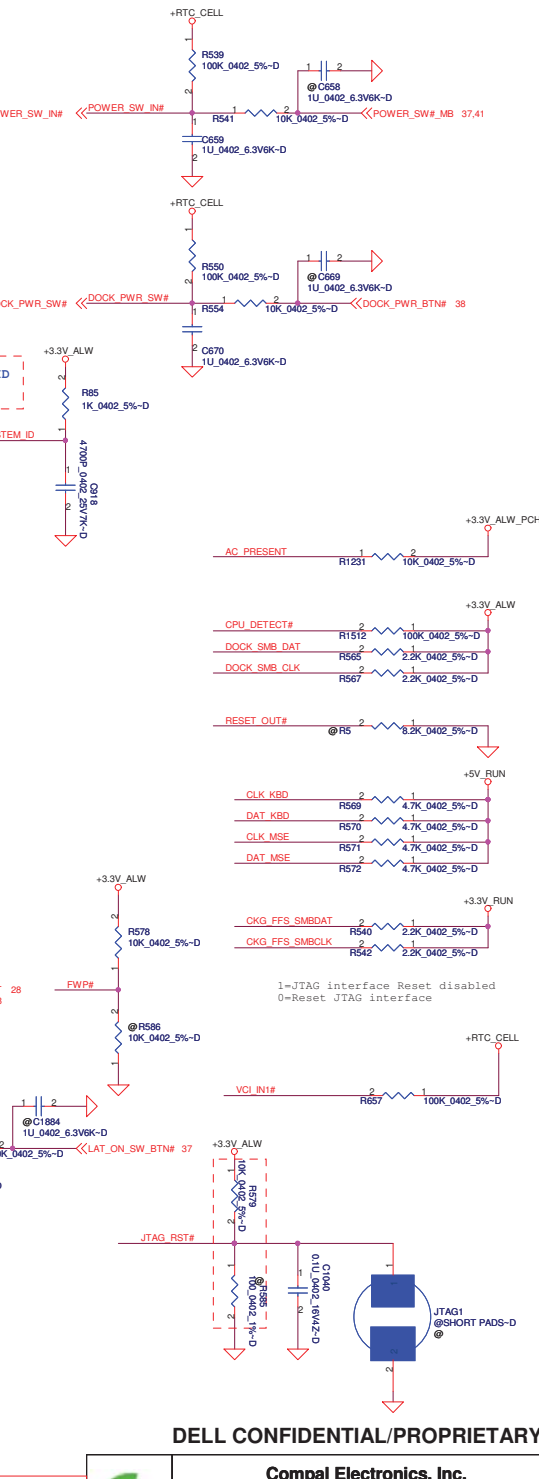
A59	LAT_ON_SW#	45
B63	ALWON	45
A63	POWER_SW_IN#	45
B67	ACAV_IN	23.51.52
A1	DOCK_PWR_SW#	23.51.52

**DELL PWR SW INF**

NC1	VS22	B52
NC2	VS21	B51
NC3	VS20	B50
NC4	VS19	B49
NC5	VS18	B48
NC6	VS17	B47
NC7	VS16	B46
NC8	VS15	B45
NC9	VS14	B44
NC10	VS13	B43
NC11	VS12	B42
NC12	VS11	B41
NC13	VS10	B40
NC14	VS9	B39
NC15	VS8	B38
NC16	VS7	B37
NC17	VS6	B36
NC18	VS5	B35
NC19	VS4	B34
NC20	VS3	B33
NC21	VS2	B32
NC22	VS1	B31
NC23	VS0	B30

**DELL PWR SW INF**

R98	C919	REV
240K	4700p	X00
130K	4700p	X01
33K	4700p	X02
4.3K	4700p	X03
2K	4700p	A00
1K	4700p	A00
4700p	4700p	
4700p	4700p	



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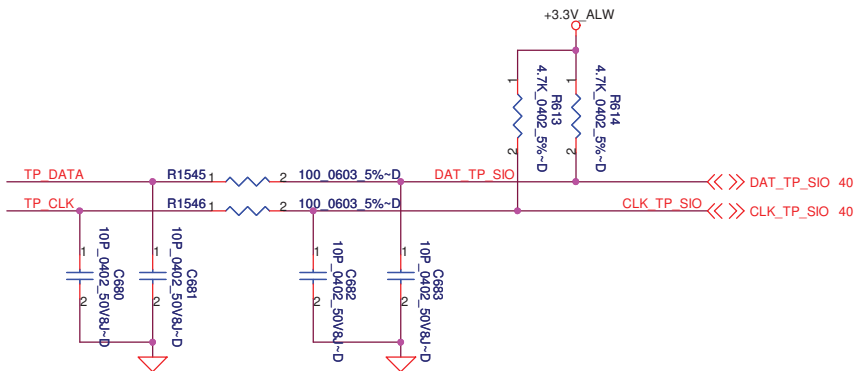
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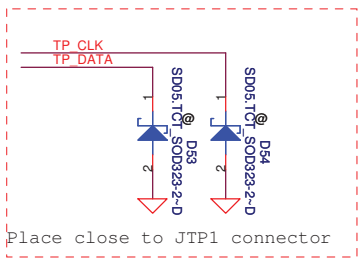
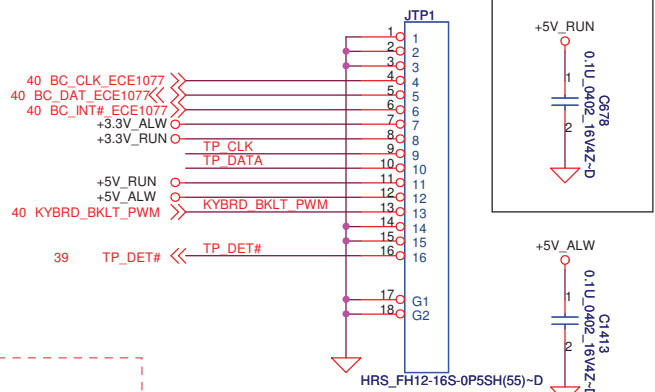
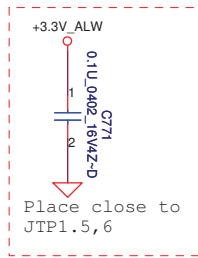
Date: Thursday, January 21, 2010 Sheet 40 of 69



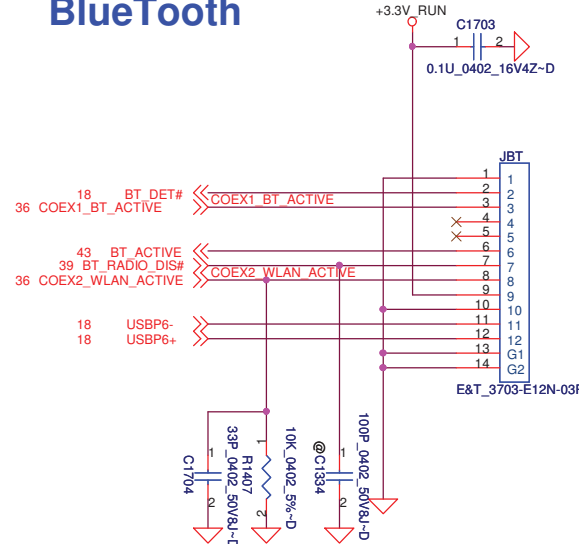
# Touch Pad



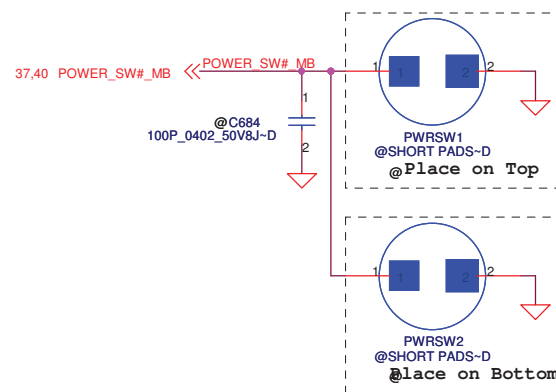
Touch Pad Conn. Pitch=0.5



# BlueTooth



# Power Switch for debug



@ FAN

Part Number	Description
DC28A000800	FAN SET DAQ20 DC5V AB7405HB-HB3 ADDA

@ Speak

Part Number	Description
PK230003Q0L	SPK PACK ZJX 2.0W 4 OHM FG

@SM CARD BODY

Part Number	Description
SP070007V0L	\$ SOCKET TYCO 1770551-1 10P H5.9 SMART

@PCMCIA BODY

Part Number	Description
DC000001Q0L	PCMCIA TYCO 1759096-1

@ MDC wire set cable

Part Number	Description
DC02000CS0L	H-CONN SET ZGX MB-MDC

@ T/P wire set cable

Part Number	Description
DC02000840L	H-CONN SET ZJX MB-B/T-TP-FP

@ LVDS cable

Part Number	Description
DC020003Y0L	H-CONN SET ZJX MB-LCD 14 WXGA+ (-1ch)

@ LVDS cable

Part Number	Description
DC02000870L	H-CONN SET ZJX MB-LCD 14 WXGA+ (-2ch)

@ RTC BATT

Part Number	Description
GC20323MX00	BATT CR2032 3V 220MAH MAXELL

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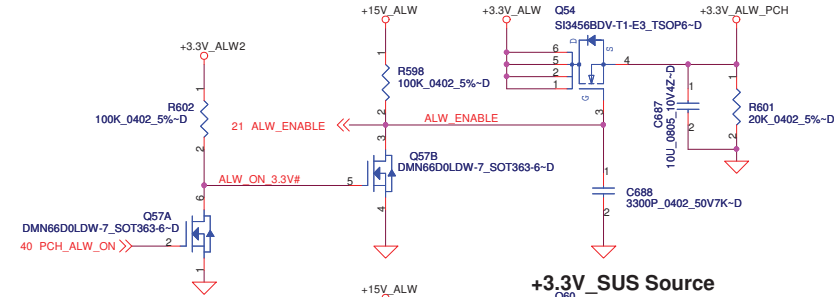


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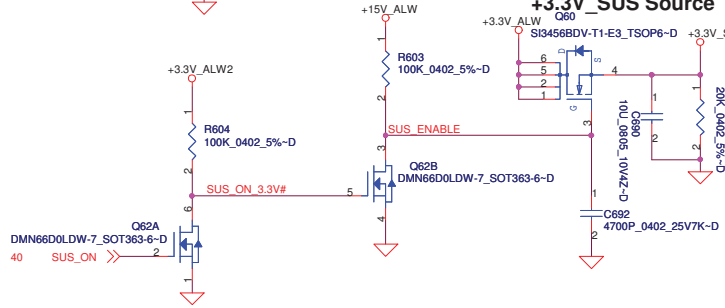
<b>Compal Electronics, Inc.</b>		
<b>Title</b> Touch PAD/Int KB/LID		
<b>Size</b>	<b>Document Number</b> LA-5573P	<b>Rev</b> 0.1
<b>Date:</b> Thursday, January 21, 2010	<b>Sheet</b> 41	<b>of</b> 69

# DC/DC Interface

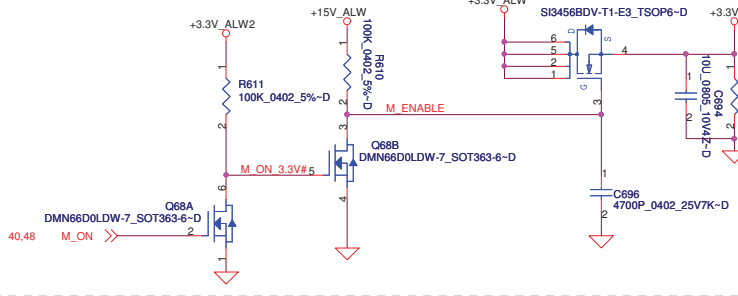
## +3.3V\_ALW\_PCH Source



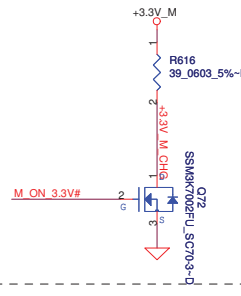
## +3.3V\_SUS Source



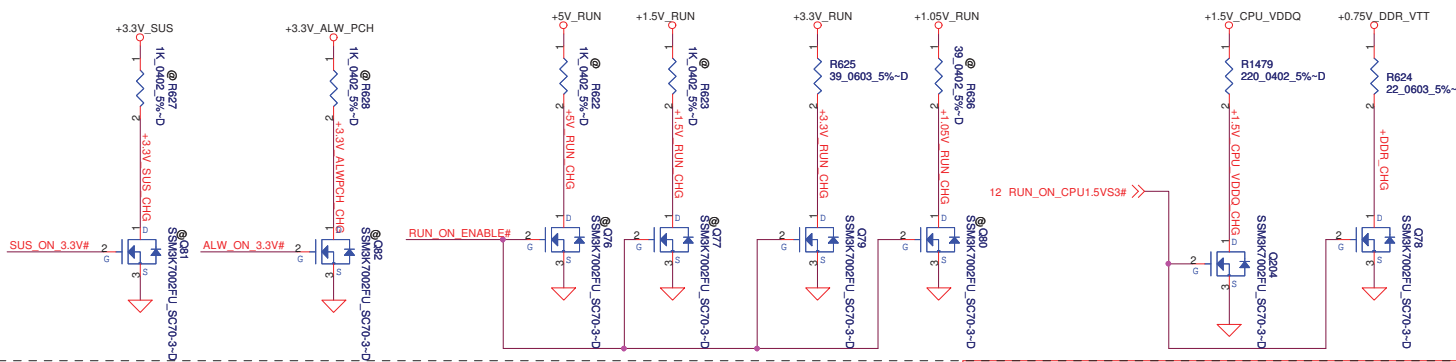
## +3.3VM Source



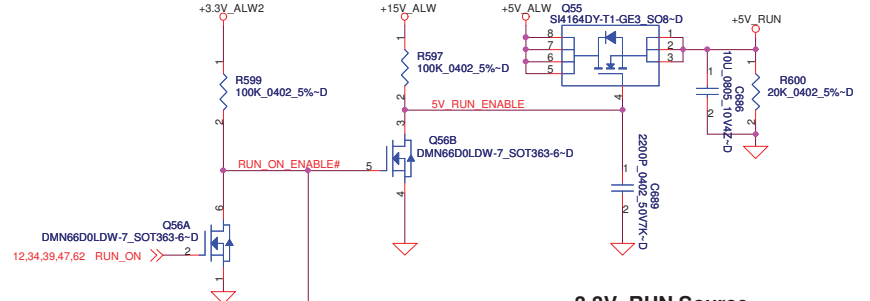
## Discharg Circuit



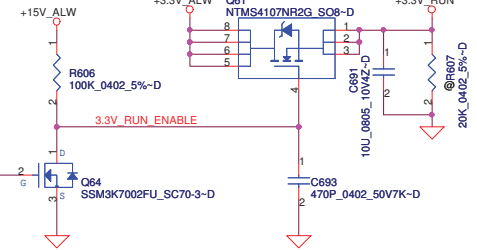
## Discharg Circuit



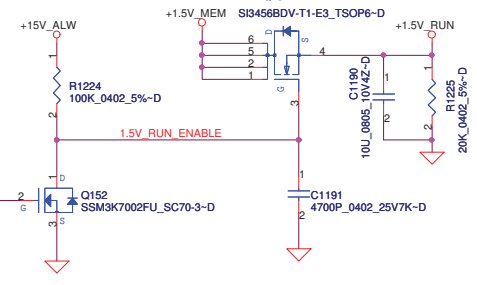
## +5VRUN Source



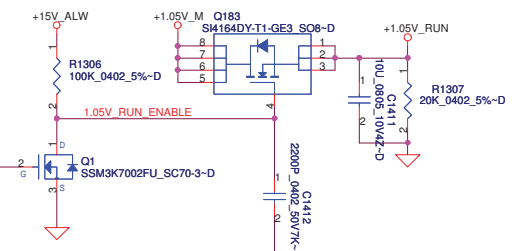
## +3.3V\_RUN Source



## +1.5V\_RUN Source



## +1.05V\_RUN Source



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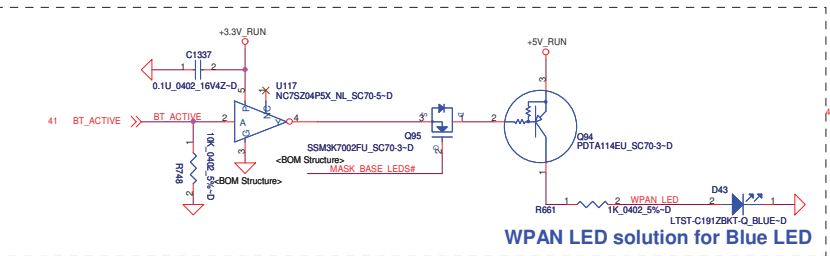
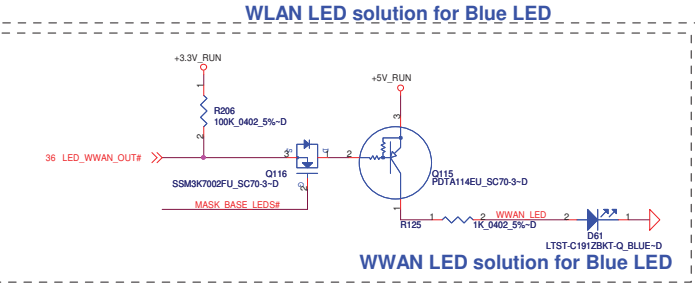
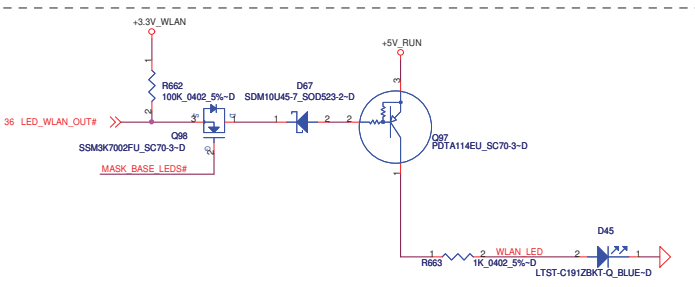
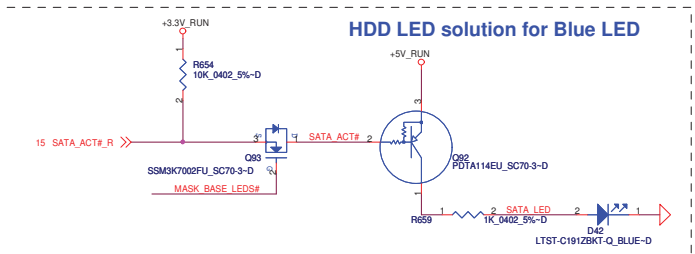
Compal Electronics, Inc.

POWER CONTROL

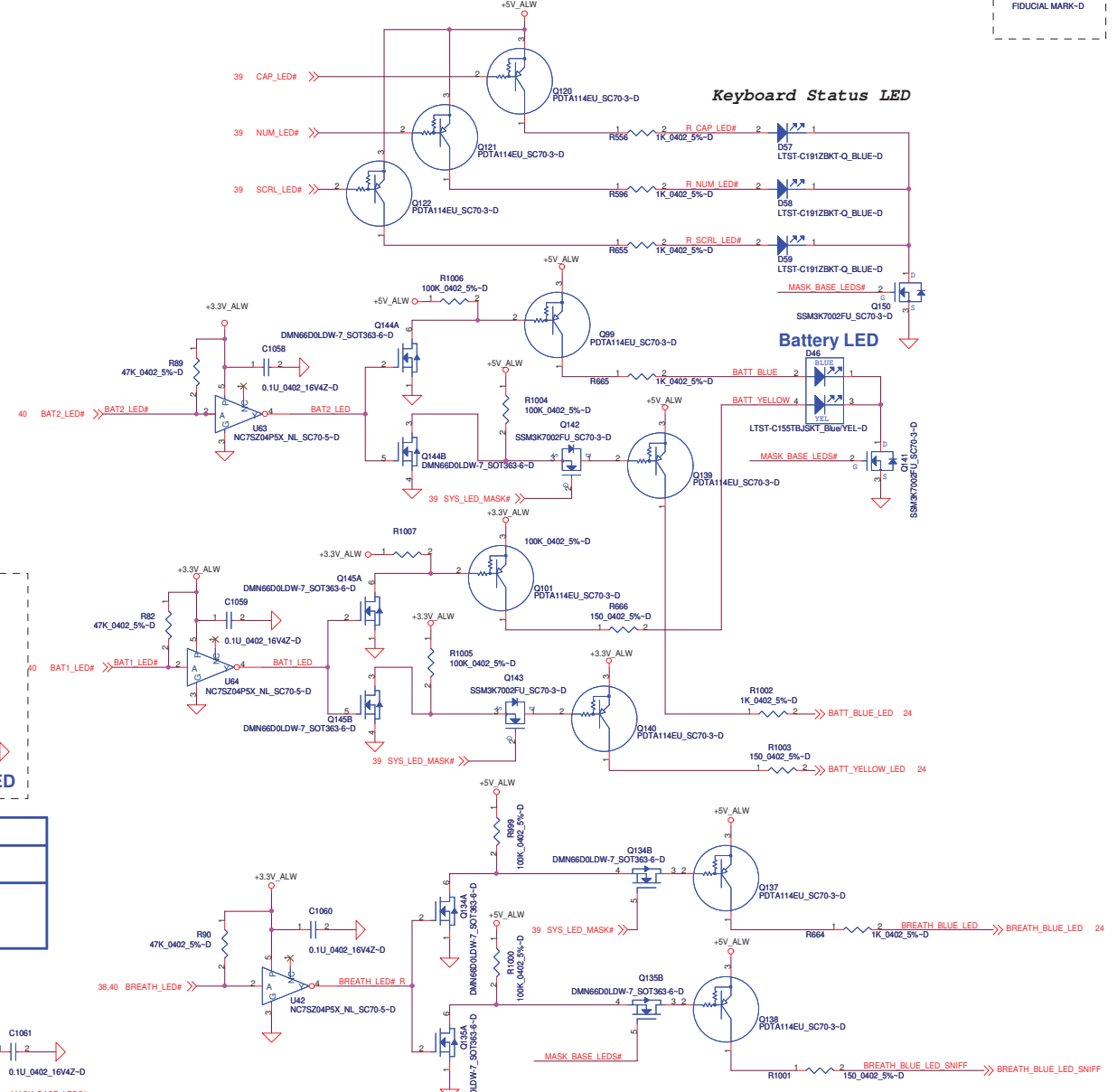
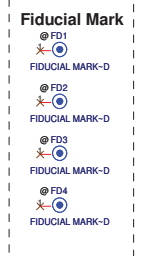
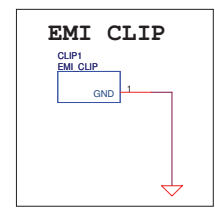
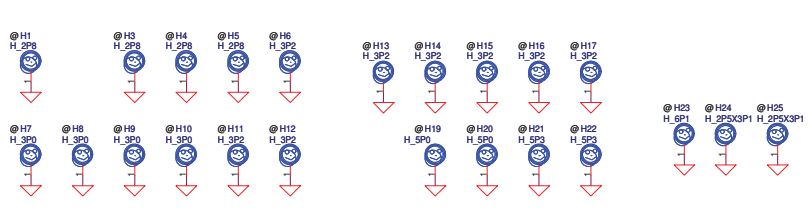
LA-5573P

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	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



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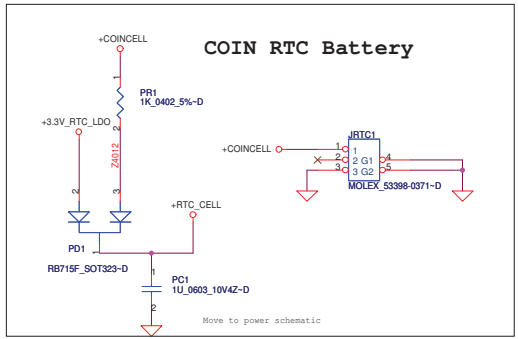
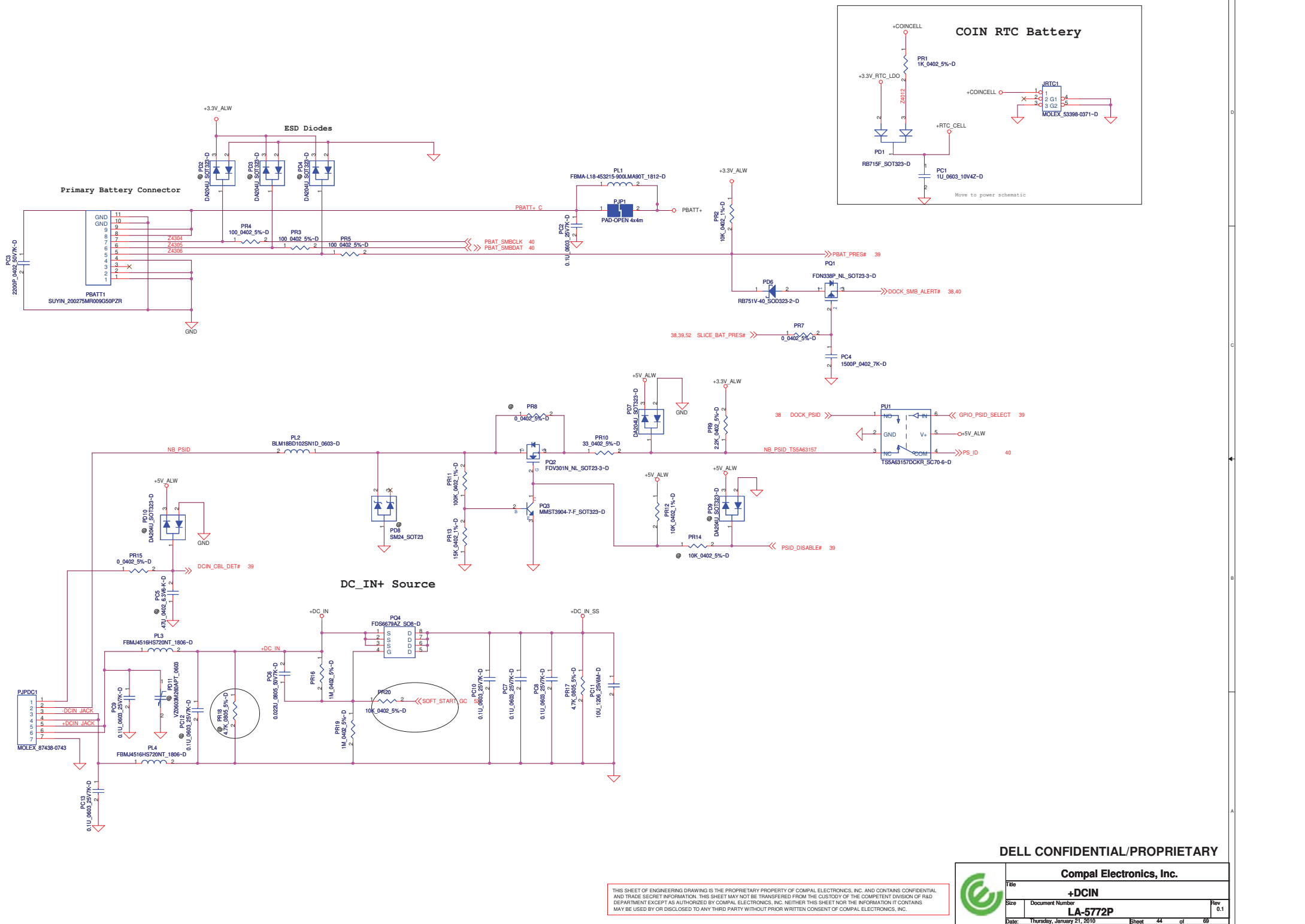
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**Compal Electronics, Inc.**

**PAD and Standoff**

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		<b>Compal Electronics, Inc.</b>	
		<b>+DCIN</b>	
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**+3.3V\_ALWP / +5V\_ALWP / +5V\_ALW2 / +15V\_ALWP / +3.3V\_RTC\_LDO**

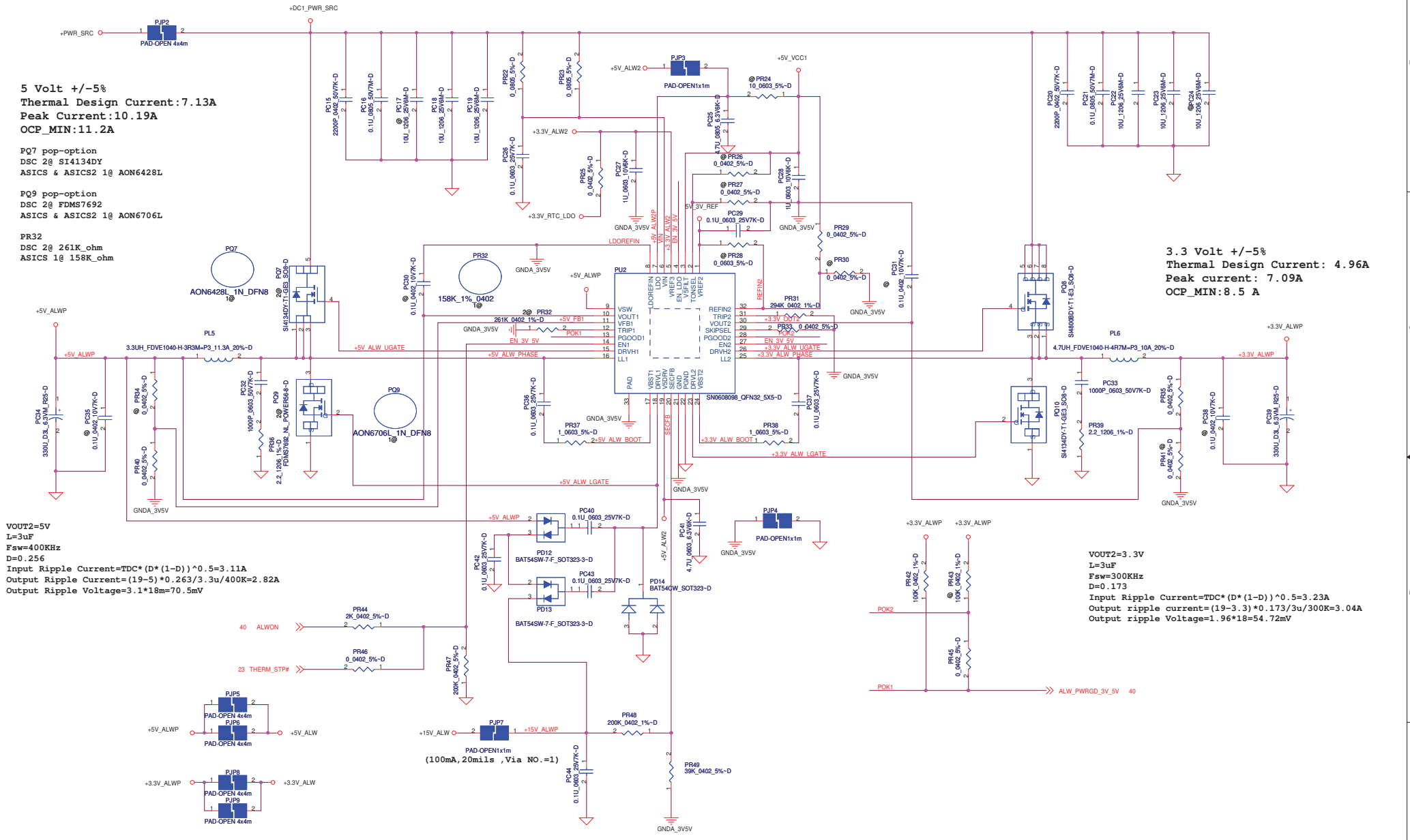
**5 Volt +/-5%**  
**Thermal Design Current: 7.13A**  
**Peak Current: 10.19A**  
**OCP\_MIN: 11.2A**

PQ7 pop-option  
 DSC 2@ SI4134DY  
 ASICS & ASICS2 1@ AON6428L

PQ9 pop-option  
 DSC 2@ FDMS7692  
 ASICS 1@ ASICS2 1@ AON6706L

PR32  
 DSC 2@ 261K\_ohm  
 ASICS 1@ 158K\_ohm

**3.3 Volt +/-5%**  
**Thermal Design Current: 4.96A**  
**Peak current: 7.09A**  
**OCP\_MIN: 8.5 A**



VOUT2=5V  
 L=3uF  
 Fsw=400KHz  
 D=0.256  
 Input Ripple Current=TDC\*(D\*(1-D))^0.5=3.11A  
 Output Ripple Current=(19-5)\*0.263/3.3u/400K=2.82A  
 Output Ripple Voltage=3.1\*18=70.5mV

VOUT2=3.3V  
 L=3uF  
 Fsw=300KHz  
 D=0.173  
 Input Ripple Current=TDC\*(D\*(1-D))^0.5=3.23A  
 Output ripple current=(19-3.3)\*0.173/3u/300K=3.04A  
 Output ripple Voltage=1.96\*18=54.72mV

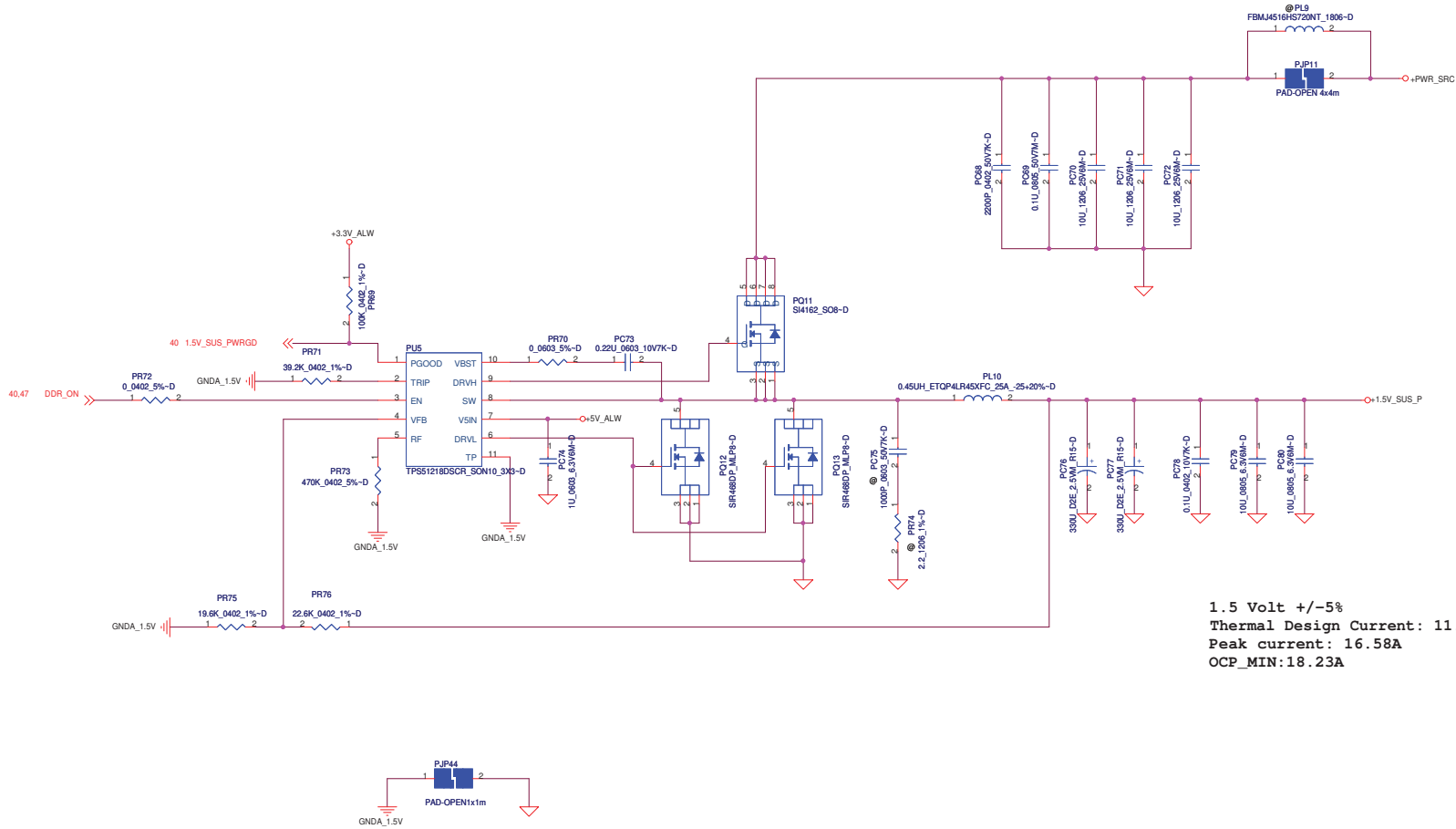
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**Compal Electronics, Inc.**

Title		DC/DC +3V/ +5V	
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1.5 Volt +/-5%  
 Thermal Design Current: 11.6A  
 Peak current: 16.58A  
 OCP\_MIN: 18.23A

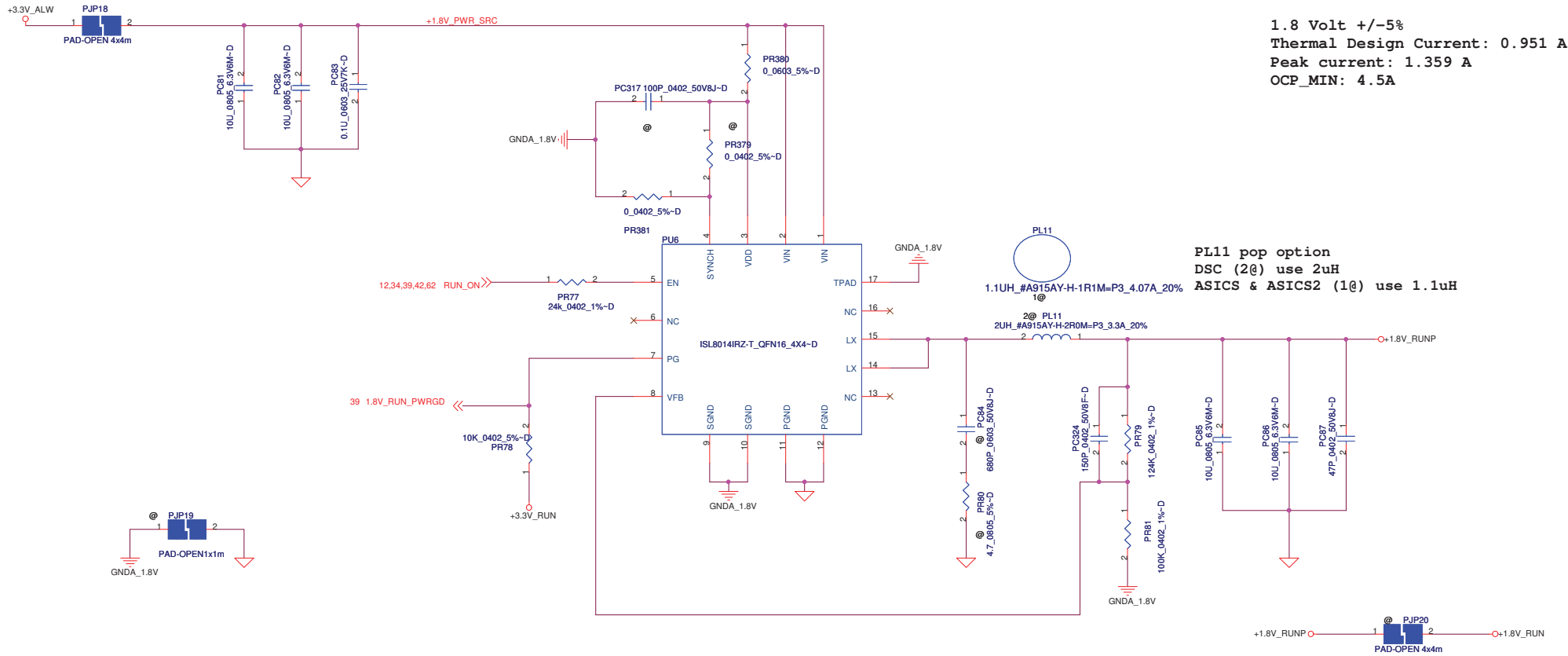
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Title		<b>+1.5V MEM</b>	
Size	Document Number	Rev	
	<b>LA-4151P</b>	<b>0.1</b>	
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### +1.8V\_RUNP

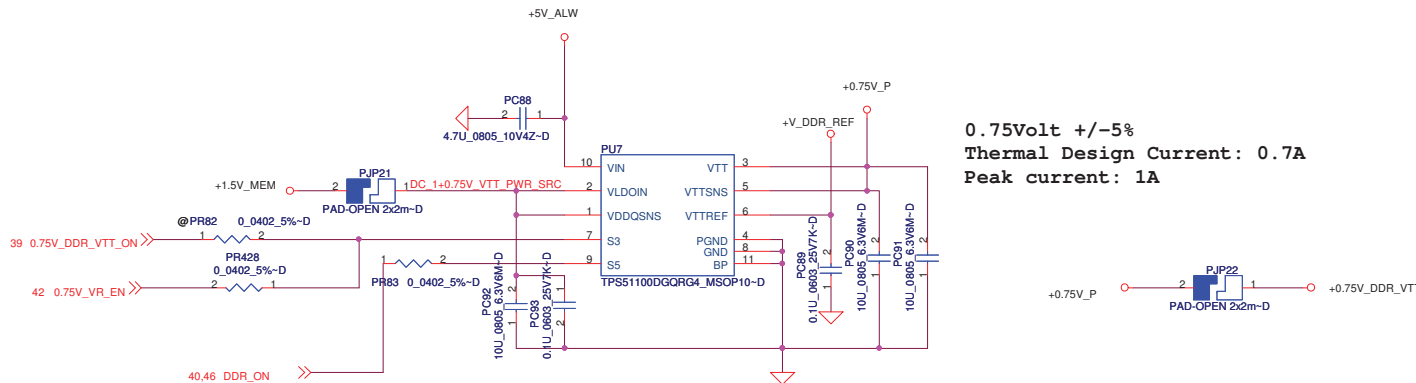


1.8 Volt +/-5%  
 Thermal Design Current: 0.951 A  
 Peak current: 1.359 A  
 OCP\_MIN: 4.5A

PL11 pop option  
 DSC (2@) use 2uH  
 ASICS & ASICS2 (1@) use 1.1uH

VOUT=1.8V  
 L=3.3uF  
 Fsw=290KHz  
 D=0.092  
 Input Ripple Current=TDC\*(D\*(1-D))^0.5=0.884A  
 Output Ripple Current=1.707A  
 Output Ripple Voltage=1.707\*15m=20.5mV

### +0.75V\_DDR\_VTT DDR3 Termination



0.75Volt +/-5%  
 Thermal Design Current: 0.7A  
 Peak current: 1A

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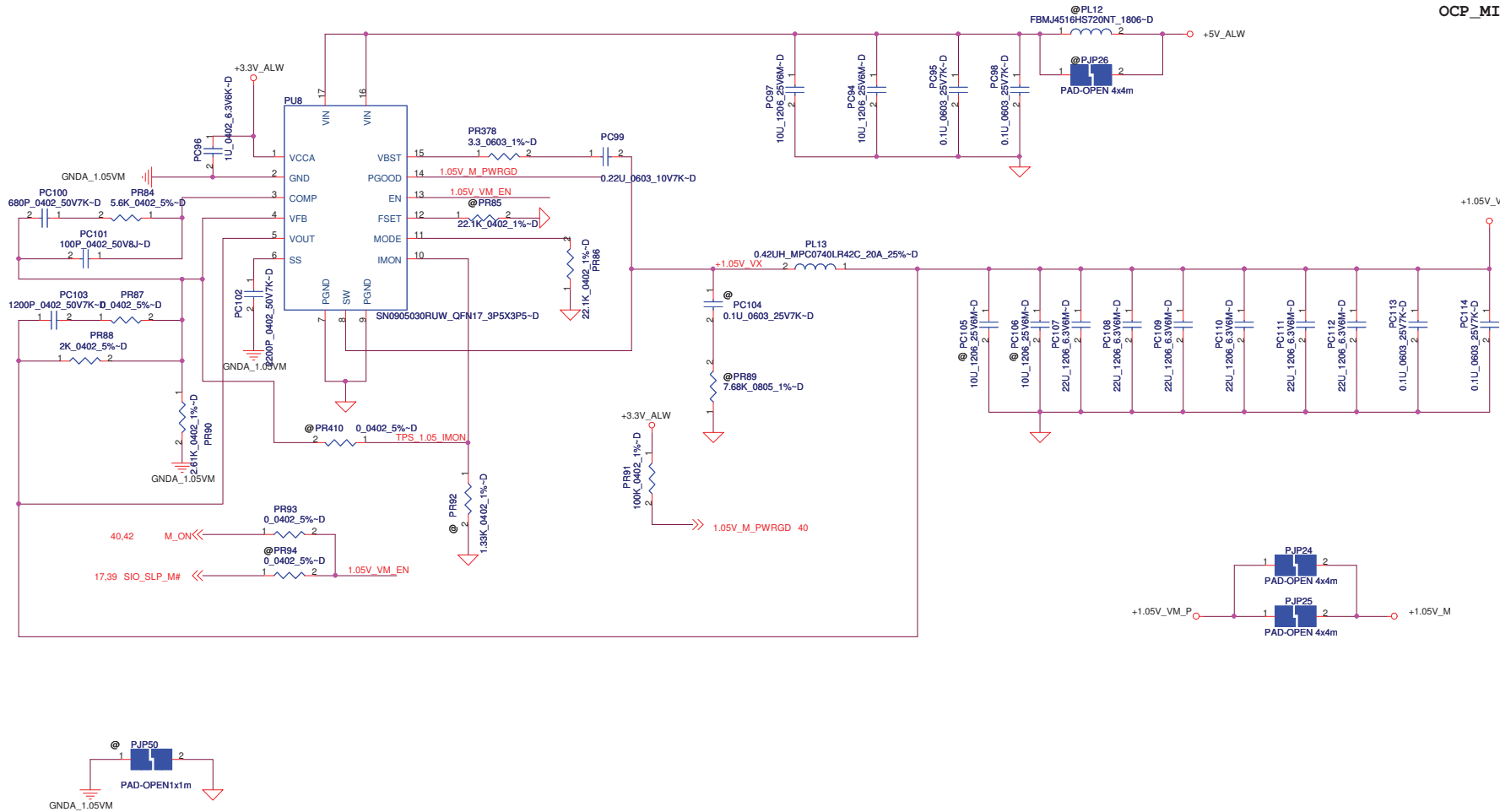
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+0.75V DDR VT/+1.8V RUN			
Size	Document Number	Rev	
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**+1.05V\_M\_P**

1.05 Volt +/-5%  
 Thermal Design Current: 7.6A  
 Peak current: 10.9A  
 OCP\_MIN: 11.9A



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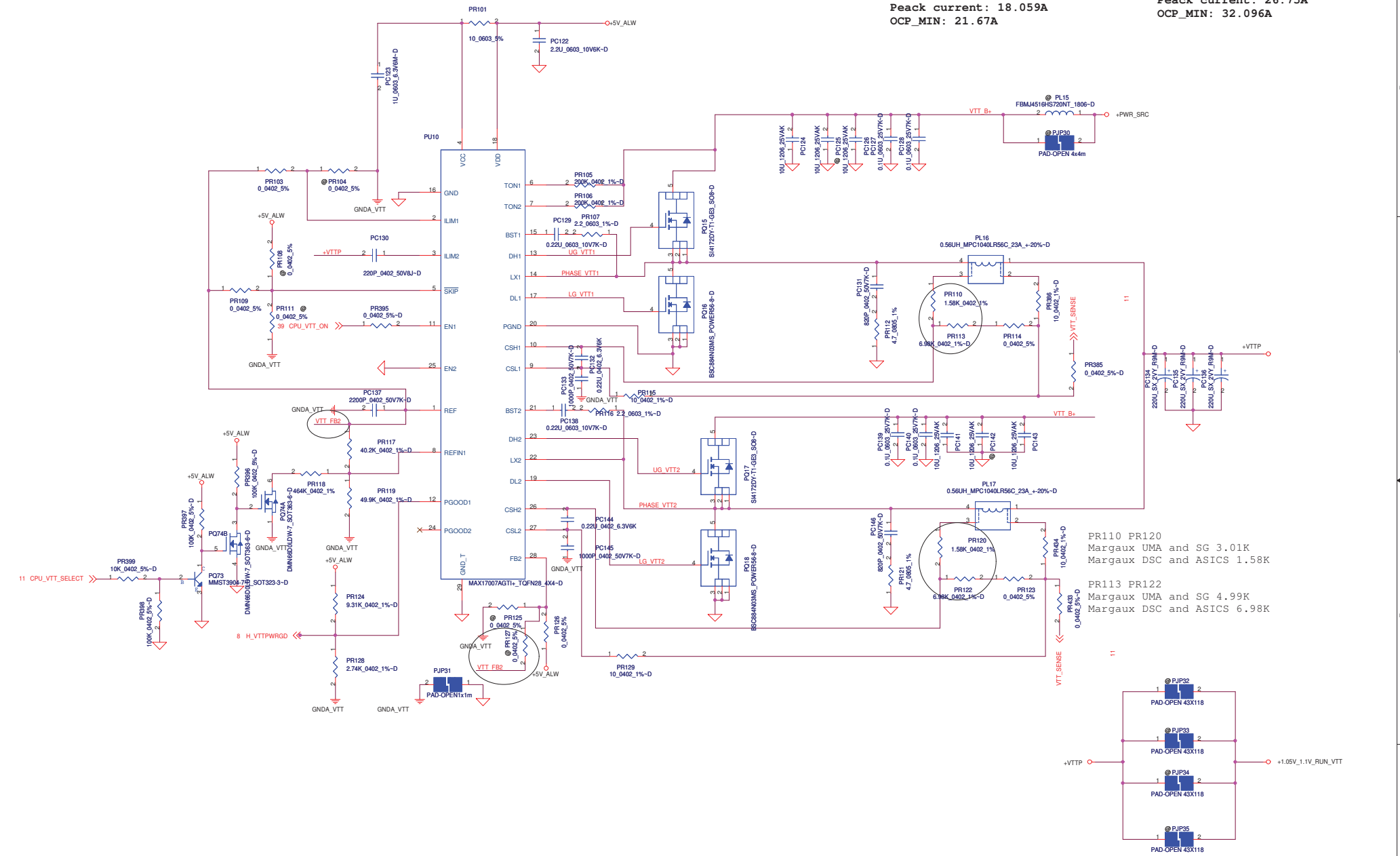
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1.1 Volt +/-5%  
 Thermal Design Current: 12.641A  
 Peak current: 18.059A  
 OCP\_MIN: 21.67A

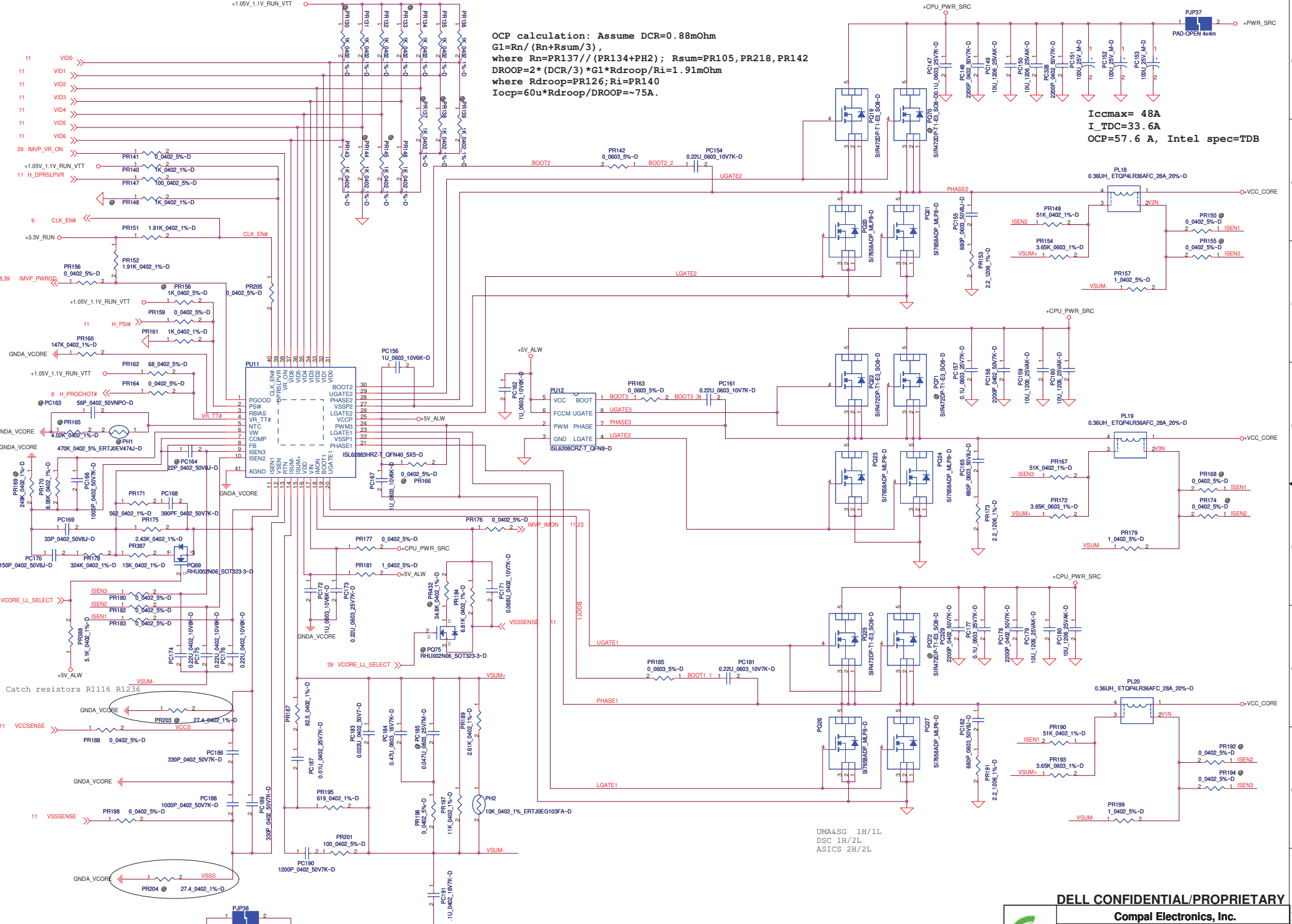
1.05 Volt +/-5%  
 Thermal Design Current: 18.72A  
 Peak current: 26.75A  
 OCP\_MIN: 32.096A



PR110 PR120  
 Margaux UMA and SG 3.01K  
 Margaux DSC and ASICs 1.58K

PR113 PR122  
 Margaux UMA and SG 4.99K  
 Margaux DSC and ASICs 6.98K

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OCP calculation: Assume DCR=0.88mOhm  
 $G1=Rn/(Rn+Rsum/3)$ ,  
 where  $Rn=PR137//((PR134+PH2)$ ;  $Rsum=PR105, PR218, PR142$   
 $DROOP=2*(DCR/3)*G1*Rdroop/Ri=1.91mOhm$   
 where  $Rdroop=PR126$ ;  $Ri=PR140$   
 $Iocp=60u*Rdroop/DROOP\sim 75A.$

**Iccmax= 48A**  
**I TDC=33.6A**  
**OCP=57.6 A, Intel spec=TDB**

Catch resistors R116 R1236

UMA&SG 1H/1L  
 DSC 1H/2L  
 ASICS 2H/2L

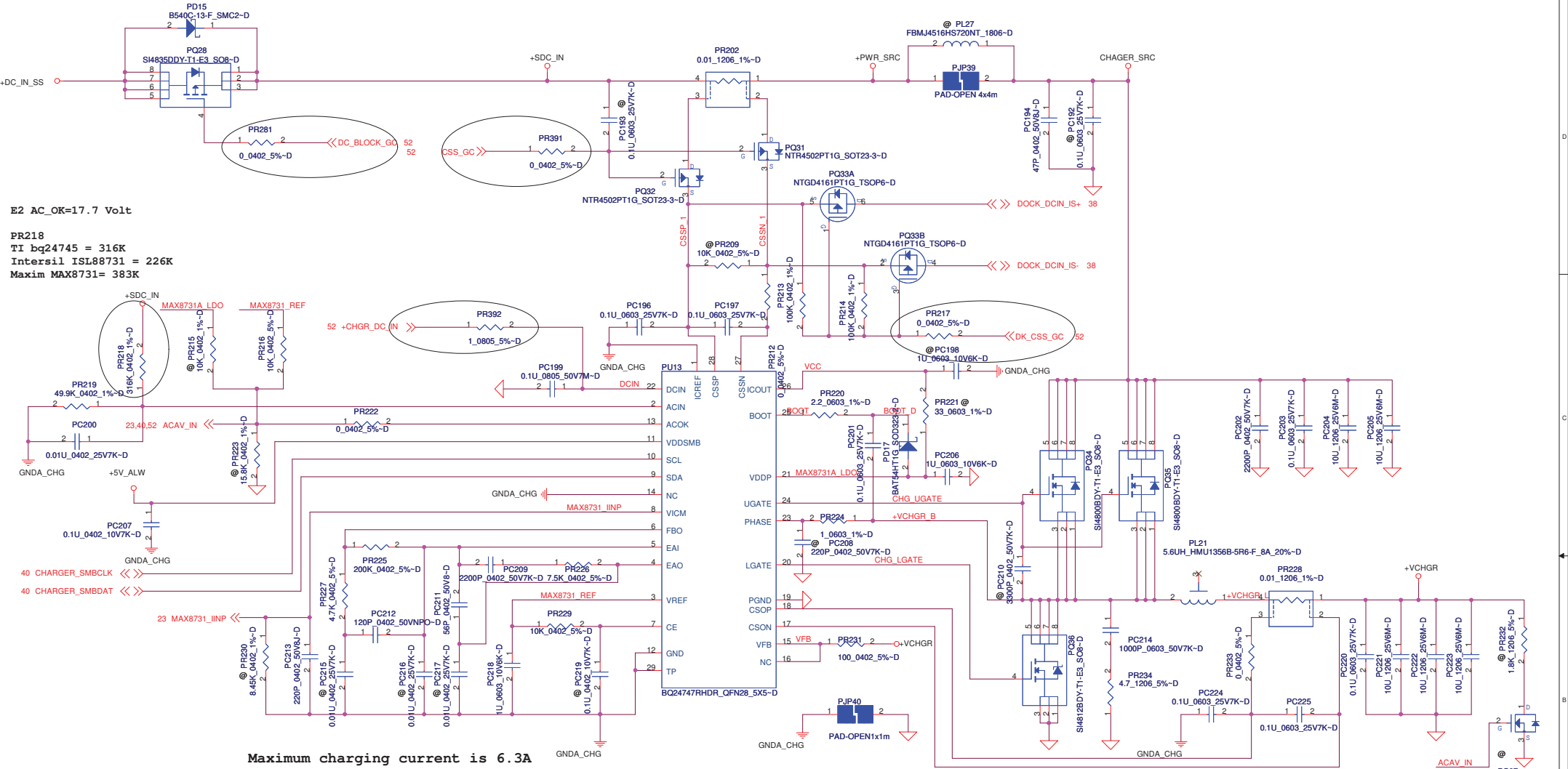
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Title		<b>+VCCORE</b>	
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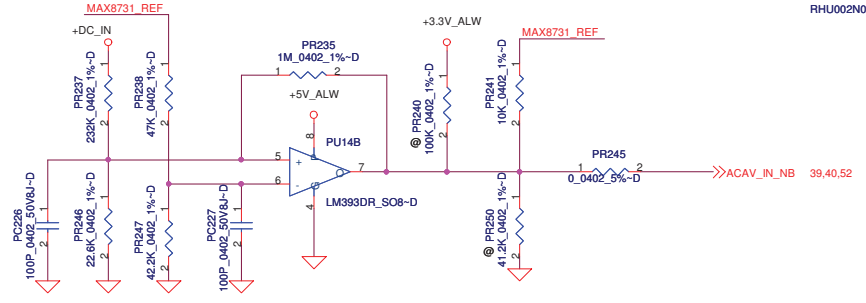
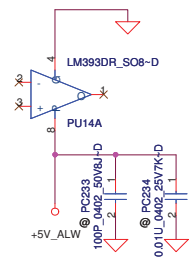


E2 AC\_OK=17.7 Volt  
 PR218  
 TI bq24745 = 316K  
 Intersil ISL88731 = 226K  
 Maxim MAX8731= 383K

40 CHARGER\_SMBCLK <<<  
 40 CHARGER\_SMBDAT <<<

23 MAX8731\_INP <<<

Maximum charging current is 6.3A



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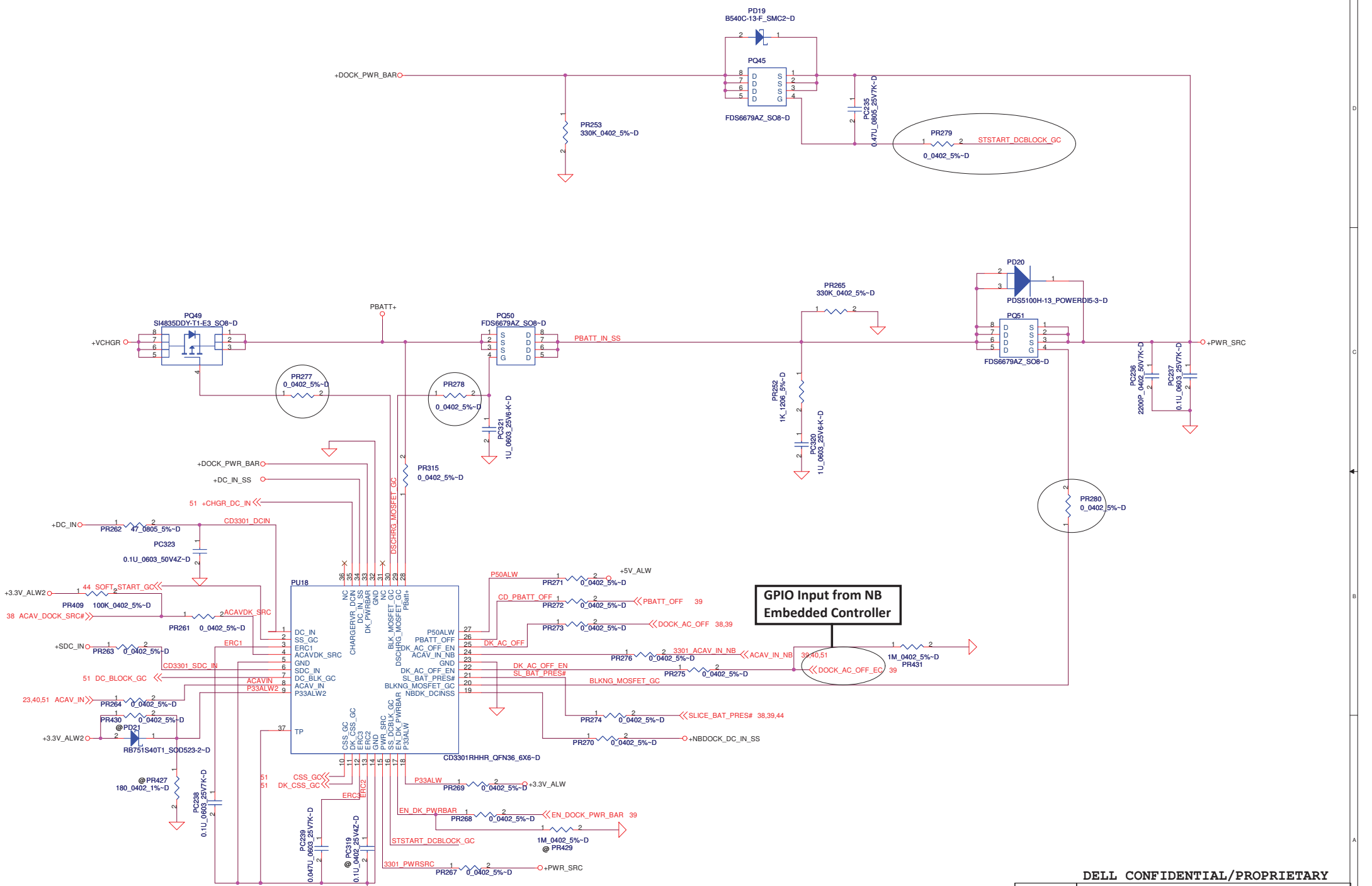
Compal Electronics, Inc.

Charger

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**GPIO Input from NB Embedded Controller**

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Title			
Selector			
LA-5772P			
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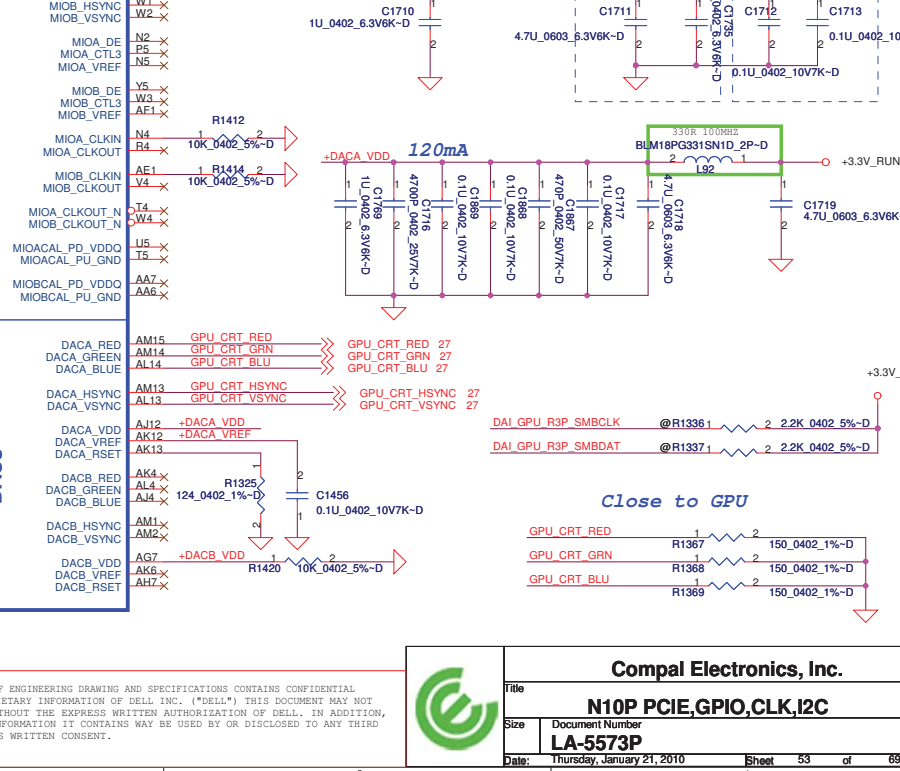
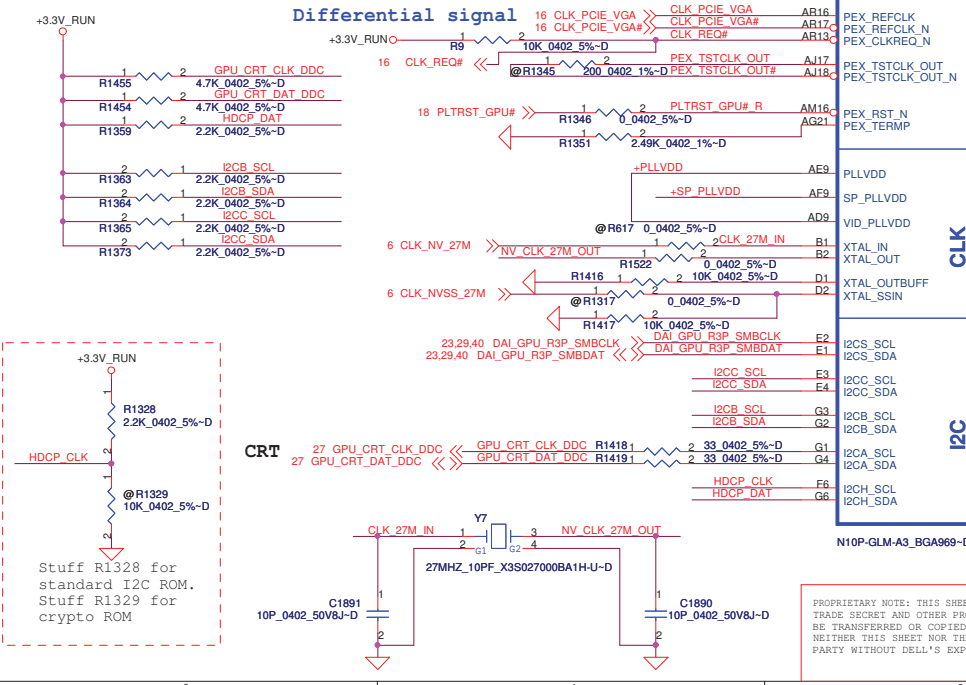
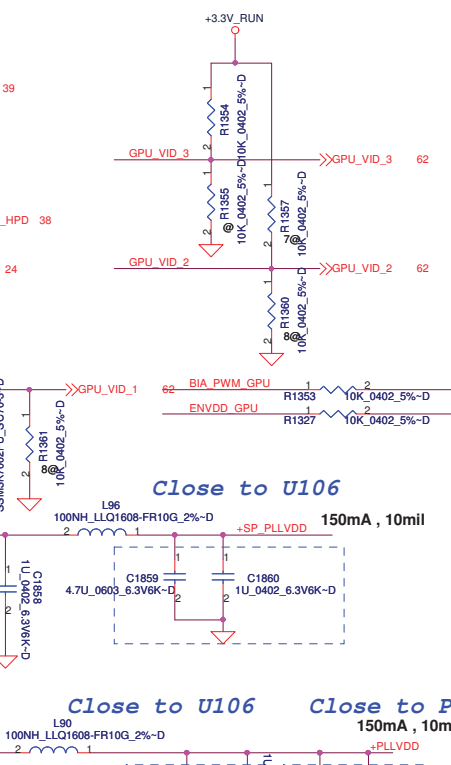
Table of pin configurations for PEG CTX and CRX signals, including PEG CTX GRX P0-15, PEG CRX GTX P0-15, and PEG CRX GTX N0-15. Includes component values like C1439 2, C1440 2, etc.

Table of pin configurations for PEG CTX GRX P0-15, PEG CRX GTX P0-15, and PEG CRX GTX N0-15. Includes component values like C1439 2, C1440 2, etc.

U106A Part 1 of 7

GPIO PCIE EXPRESS DVO CLK DACS

Table of pin configurations for GPIO, PCIE EXPRESS, DVO, CLK, and DACS signals. Includes signal names like GPU VID 1, GPU VID 2, GPU CLNDWN, etc.



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Table with company information: Compal Electronics, Inc., Title: N10P PCIe,GPIO,CLK,I2C, Size: Document Number LA-5573P, Date: Thursday, January 21, 2010, Sheet: 53 of 69, Rev: 3.0



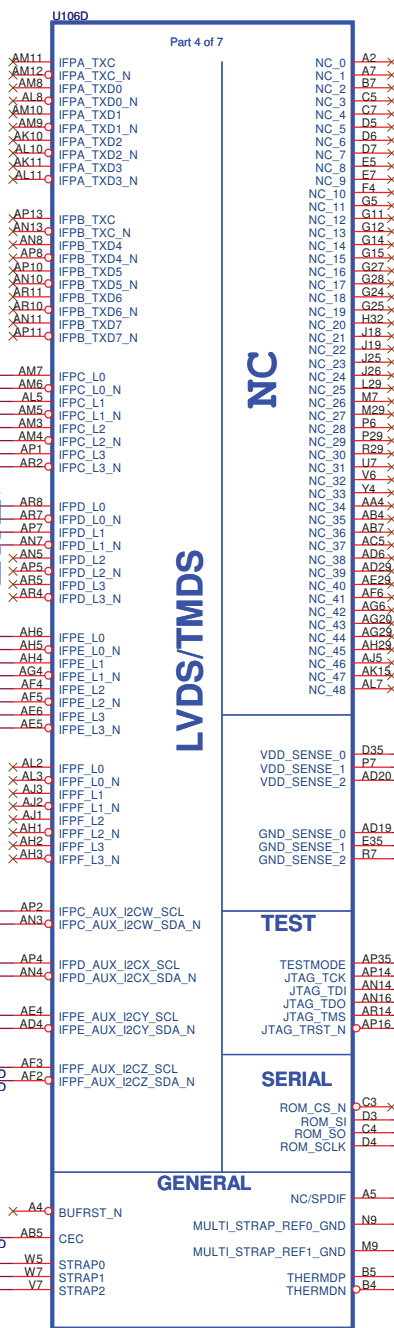
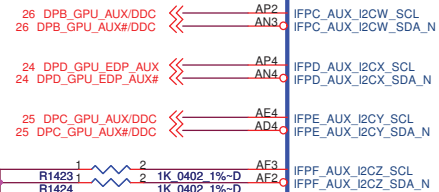
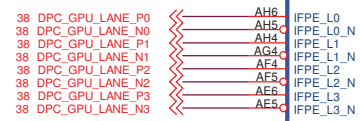
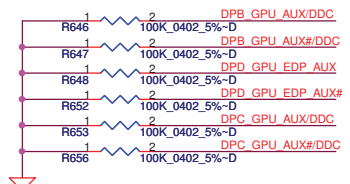
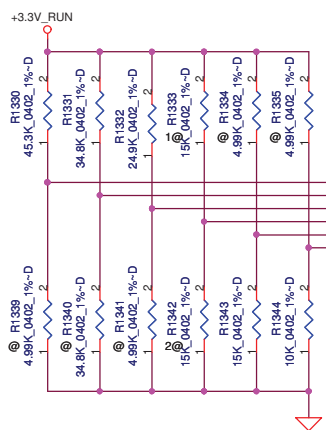
STRAP0	USER[3:0]
STRAP1	3GIO_PADCFG_LUT_ADR[3:0]
STRAP2	PCI_DEVID[3:0]

ROM_SCLK	PCIDEVID_EXT, SUB_VENDOR, SLOT_CLK, PEX_PLL_EN
ROM_SI	RAM_CFG[3:0]
ROM_SO	XCLK_417, FB_0_BAR_SIZE, ALT_ADOOR, VGA_DEVICE

	R1332	R1341	R1342	R1333	
Asics	10K	depop	15K	depop	N10P-GS
Margaux					

Resistor Values	PU/PD	Bit3-Bit0	
STRAP0	PU	1111	45K
STRAP1	PD	0110	35K
STRAP2	PU	1100	25K
ROM_SCLK	PD	0010	15K
ROM_SI	PD	0011	20K
ROM_SO	PD	0001	10K

For Samsung 64Mx16 DDR3 part stuff R1343=20K  
 For Hynix 64Mx16 DDR3 part stuff R1343=15K  
 Hynix H5TQ1G63BFR-12C SA00003240L



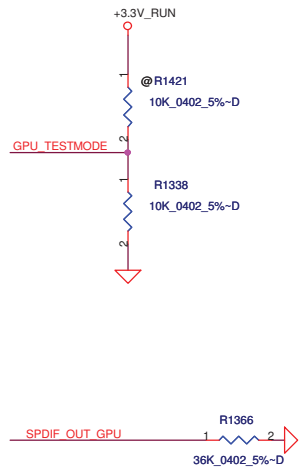
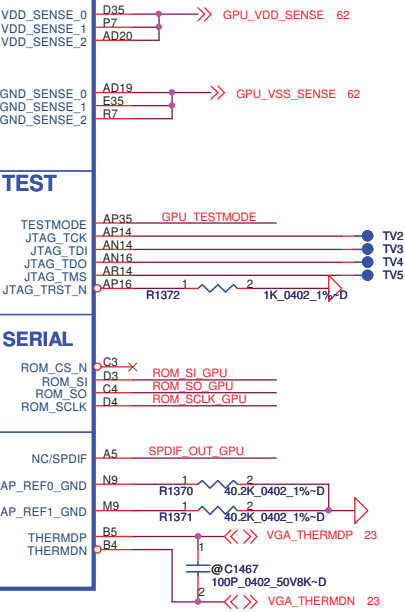
NC

LVDS/TMDS

TEST

SERIAL

GENERAL



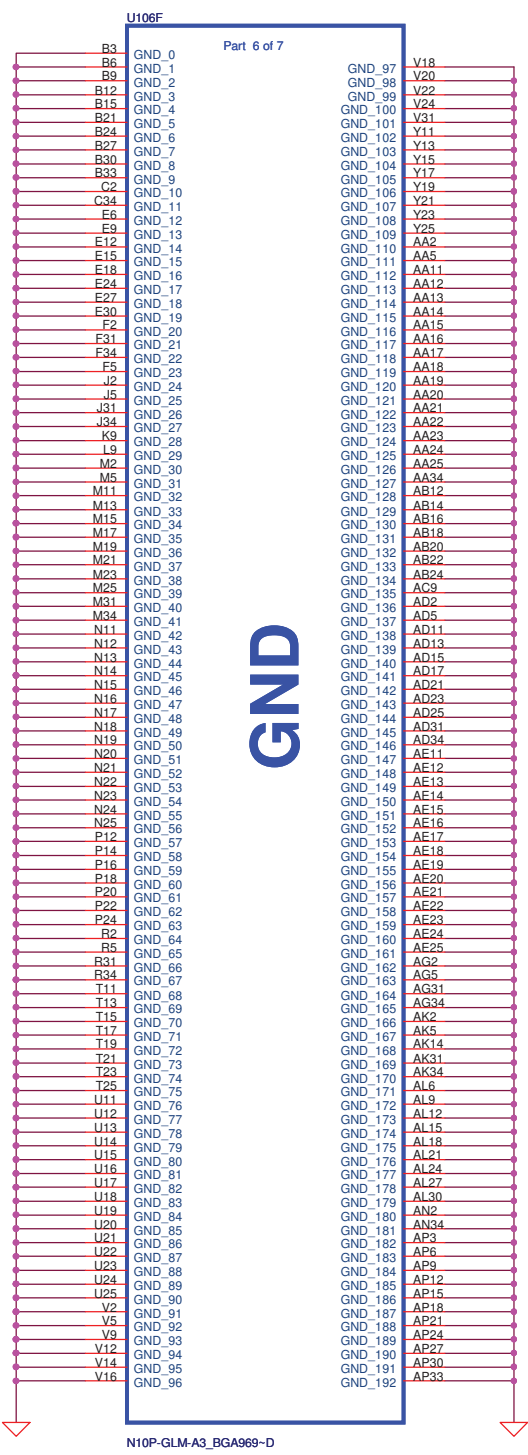
N10P-GLM-A3\_BGA969-D  
 Hynix H5TQ1G63BFR-12C SA00003240L

For Samsung 64Mx16 DDR3 part stuff R1343=20K  
 For Hynix 64Mx16 DDR3 part stuff R1343=15K

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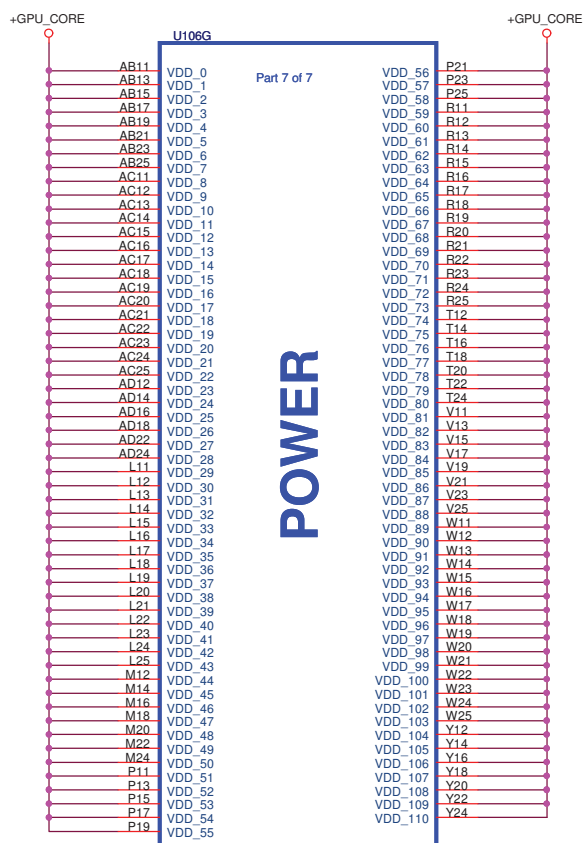


<b>Compal Electronics, Inc.</b>		
<b>N10P DP, STRAP</b>		
File	Document Number	Rev
	<b>LA-5573P</b>	<b>3.0</b>
Date:	Thursday, January 21, 2010	Sheet 54 of 69



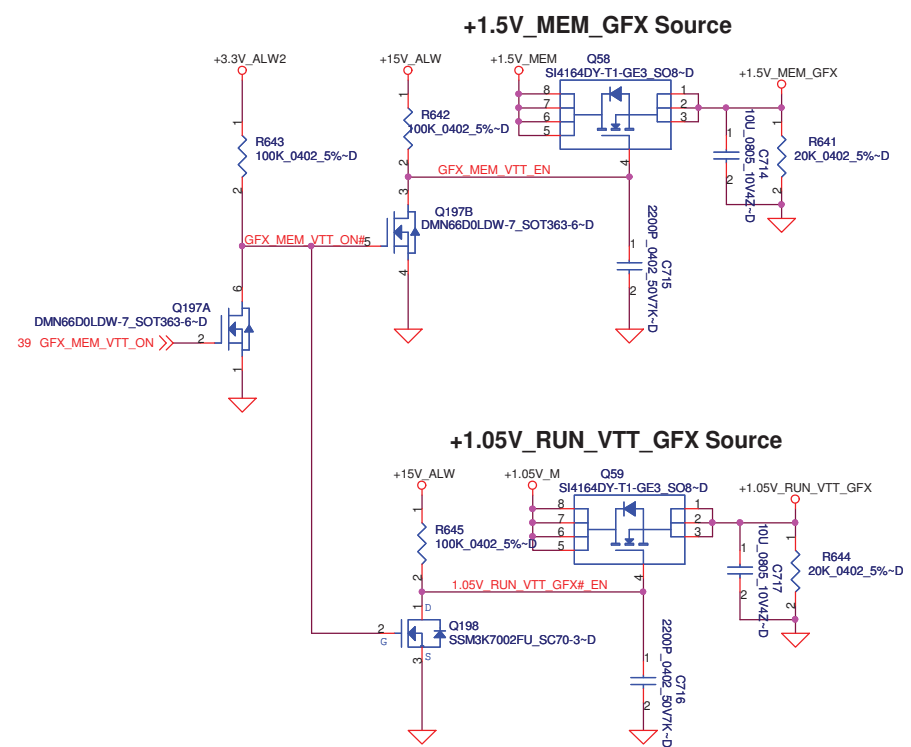
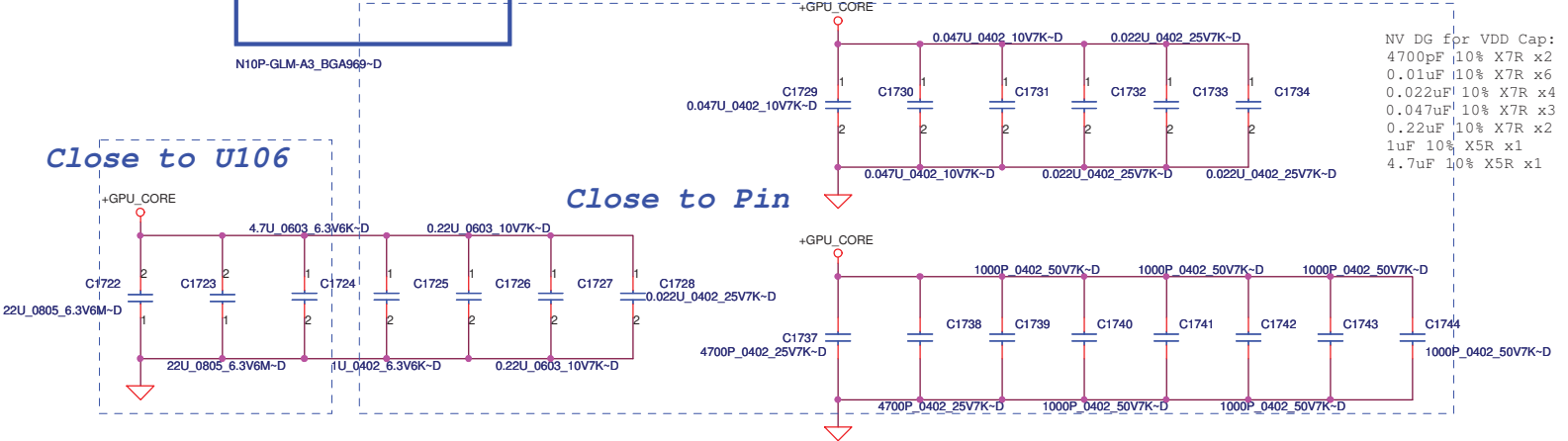
**GND**

N10P-GLM-A3\_BGA969-D



**POWER**

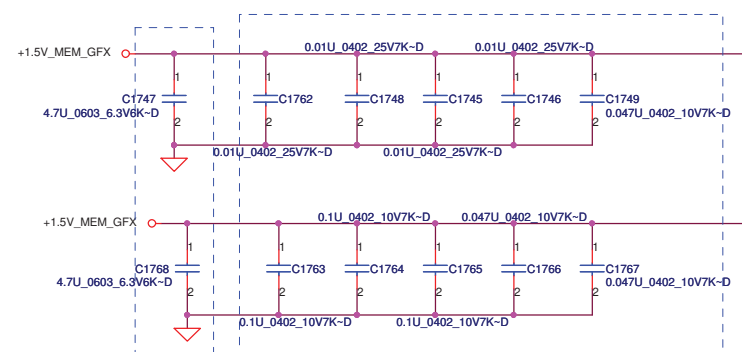
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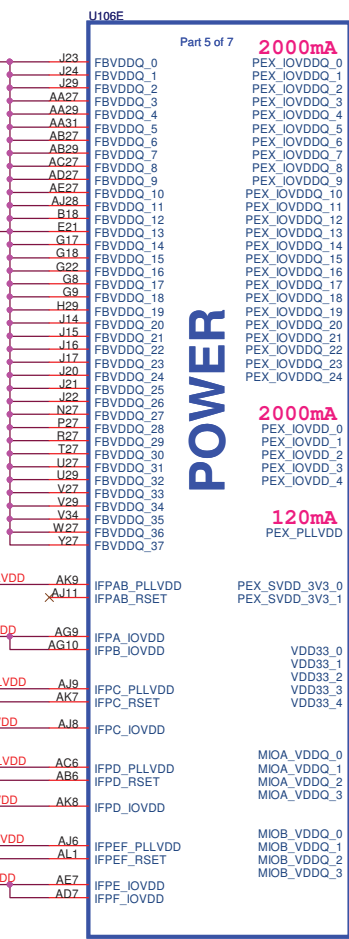
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<b>Compal Electronics, Inc.</b>			
Title			
<b>N10P GPU CORE, GND</b>			
Size	Document Number	Rev	
	<b>LA-5573P</b>	<b>3.0</b>	
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Close to U106      Close to Pin



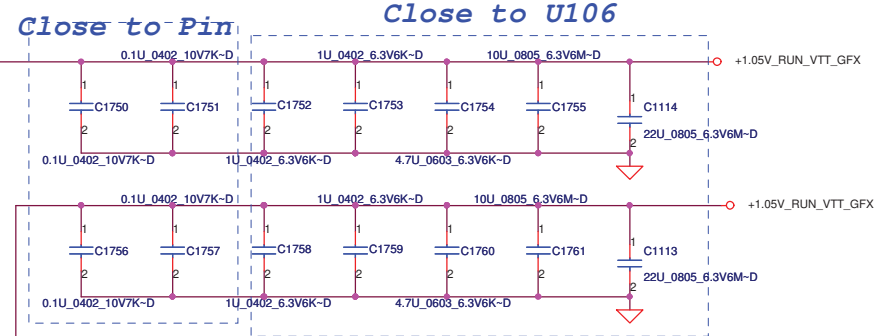
**POWER**

2000mA

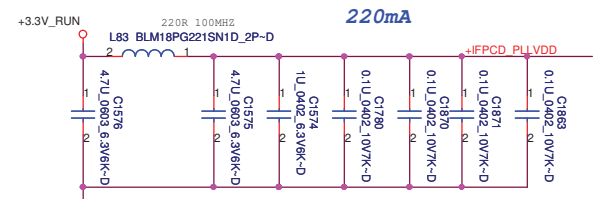
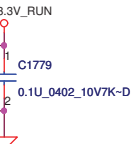
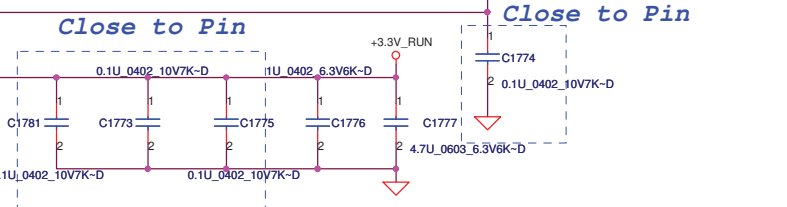
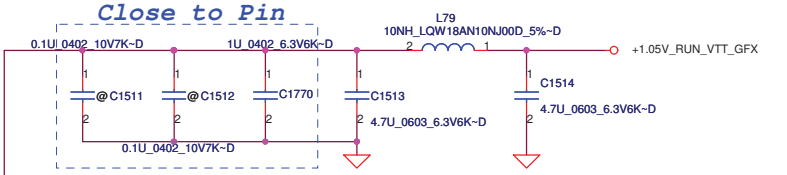
2000mA

120mA

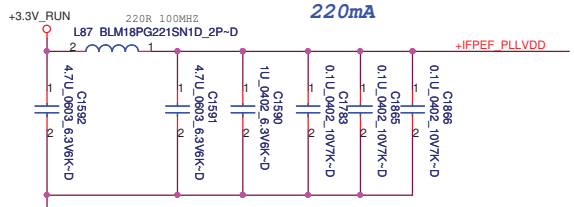
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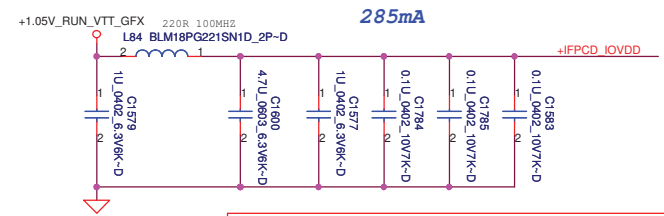
Close to Pin      Close to U106



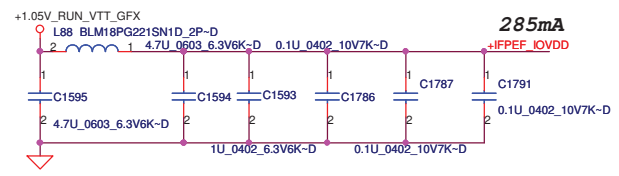
220mA



220mA



285mA



285mA

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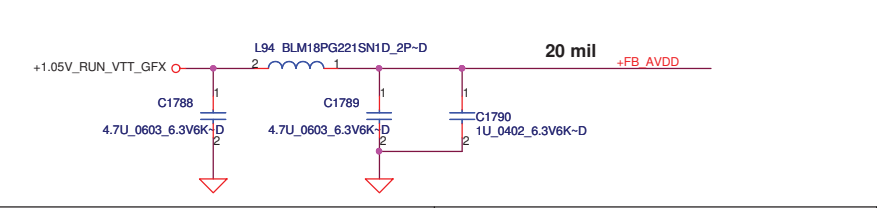
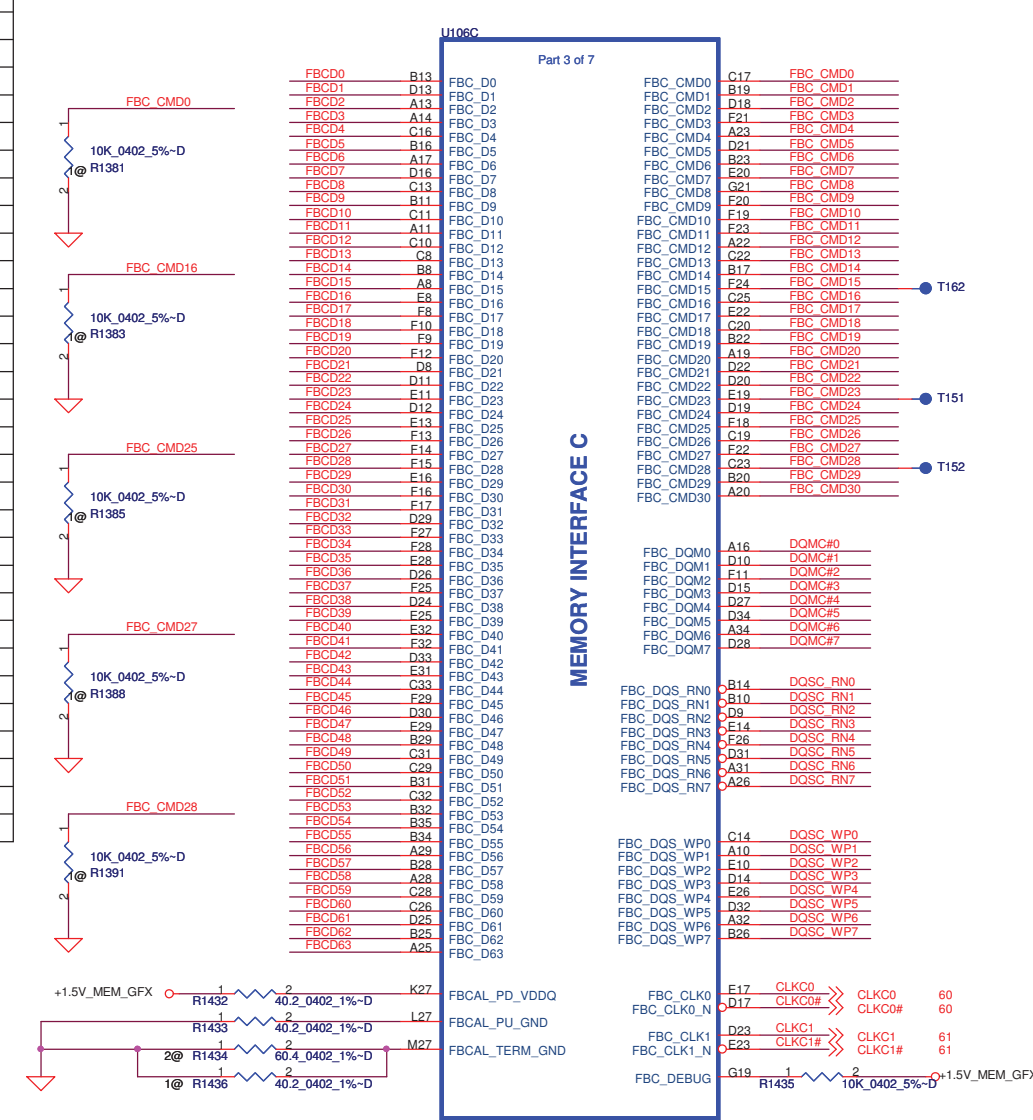
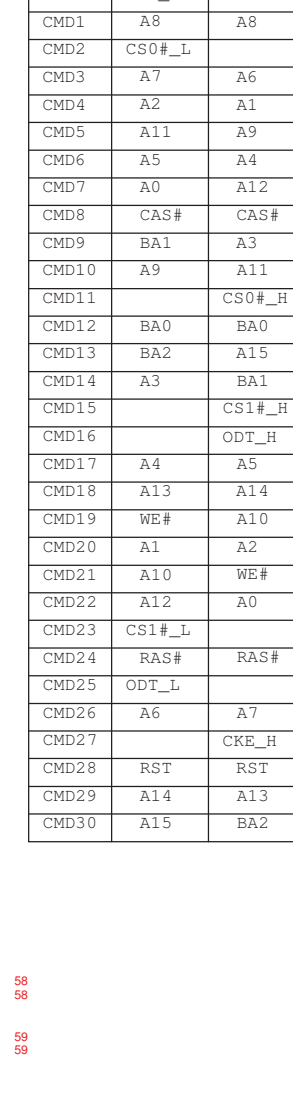
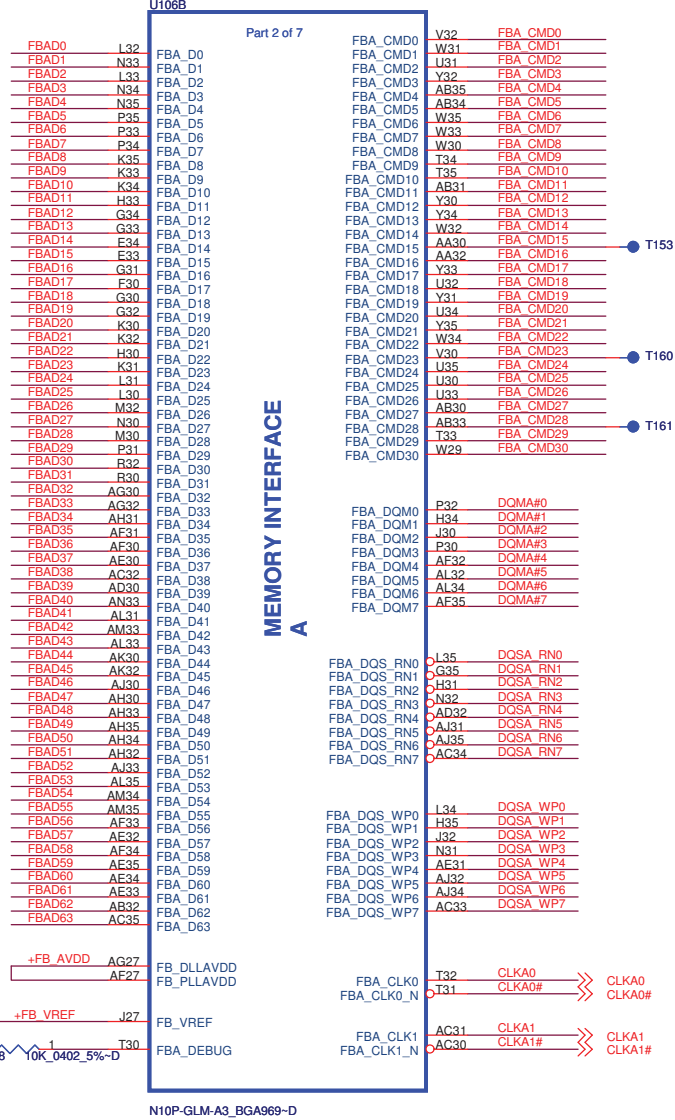
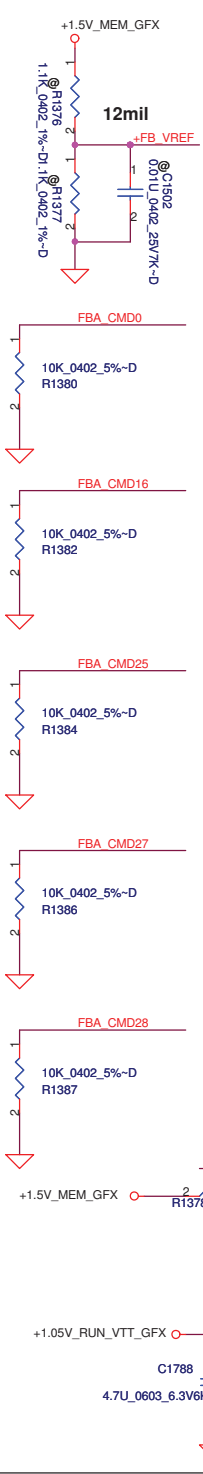
<b>Compal Electronics, Inc.</b>		
<b>Title</b>		
<b>N10P Power</b>		
<b>Size</b>	<b>Document Number</b>	<b>Rev</b>
	<b>LA-5573P</b>	<b>3.0</b>
<b>Date:</b>	<b>Thursday, January 21, 2010</b>	<b>Sheet 56 of 69</b>

# GPU CMD - Mirror Mode Mapping

		DATA Bus	
Address	0..31	32..63	
CMD0	CKE_L		
CMD1	A8	A8	
CMD2	CS0#_L		
CMD3	A7	A6	
CMD4	A2	A1	
CMD5	A11	A9	
CMD6	A5	A4	
CMD7	A0	A12	
CMD8	CAS#	CAS#	
CMD9	BA1	A3	
CMD10	A9	A11	
CMD11		CS0#_H	
CMD12	BA0	BA0	
CMD13	BA2	A15	
CMD14	A3	BA1	
CMD15		CS1#_H	
CMD16		ODT_H	
CMD17	A4	A5	
CMD18	A13	A14	
CMD19	WE#	A10	
CMD20	A1	A2	
CMD21	A10	WE#	
CMD22	A12	A0	
CMD23	CS1#_L		
CMD24	RAS#	RAS#	
CMD25	ODT_L		
CMD26	A6	A7	
CMD27		CKE_H	
CMD28	RST	RST	
CMD29	A14	A13	
CMD30	A15	BA2	

- FBAD[0..63] <<>> FBAD[0..63] 58,59
- FBA\_CMD[0..30] >>> FBA\_CMD[0..30] 58,59
- DQMA#[0..7] >>> DQMA#[0..7] 58,59
- DQSA\_RN[0..7] <<>> DQSA\_RN[0..7] 58,59
- DQSA\_WP[0..7] <<>> DQSA\_WP[0..7] 58,59

- FBAD[0..63] <<>> FBAD[0..63] 60,61
- FBC\_CMD[0..30] >>> FBC\_CMD[0..30] 60,61
- DQMC#[0..7] >>> DQMC#[0..7] 60,61
- DQSC\_RN[0..7] <<>> DQSC\_RN[0..7] 60,61
- DQSC\_WP[0..7] <<>> DQSC\_WP[0..7] 60,61



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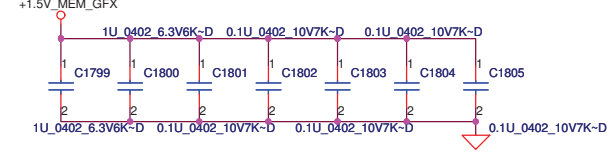
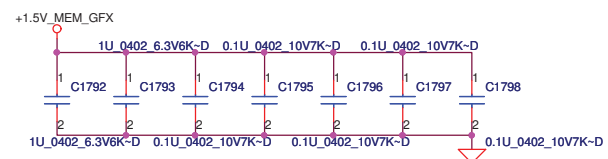
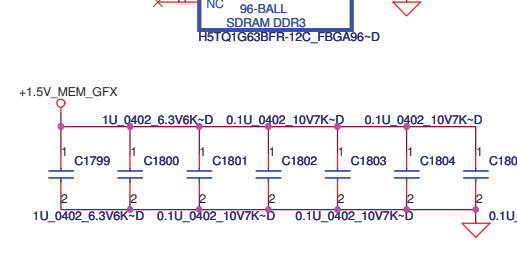
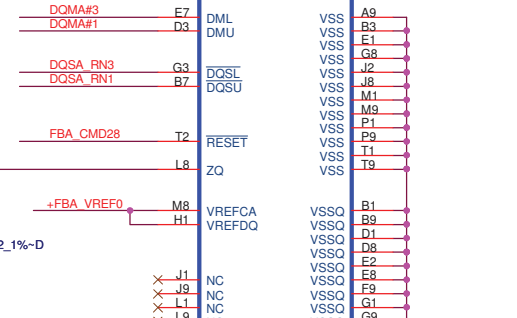
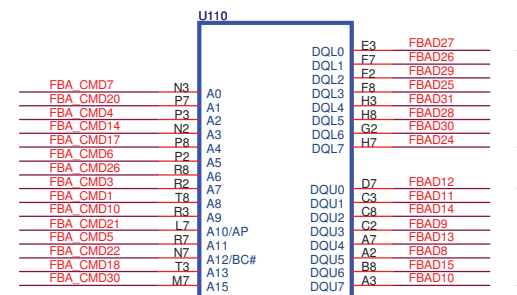
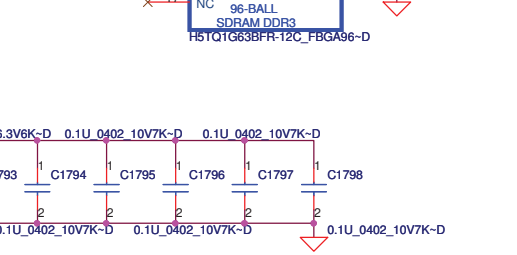
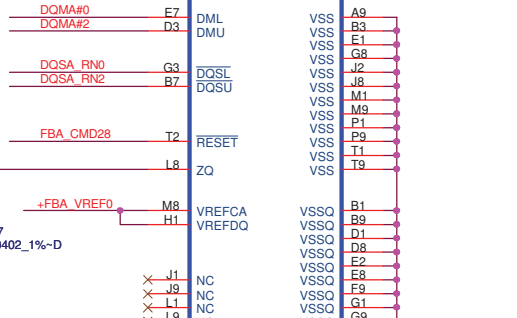
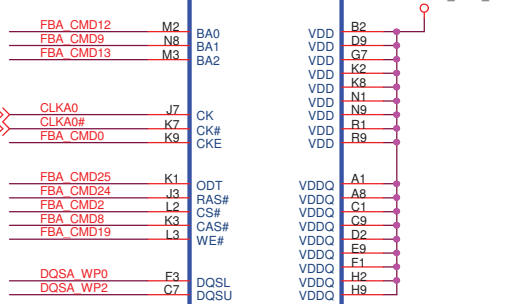
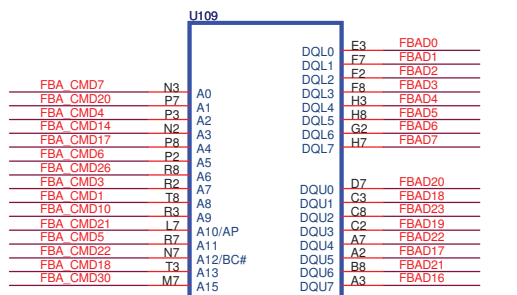
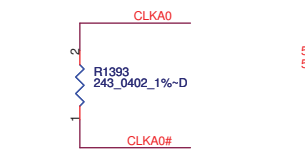
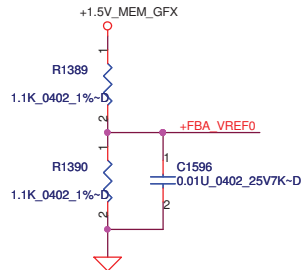
**N10P Memory**

**LA-5573P**

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# Memory Partition A - Lower 32 bits

FBA\_CMD[0..30] <<< FBA\_CMD[0..30] 57,59  
 FBAD[0..63] <<<> FBAD[0..63] 57,59  
 DQMA#[0..7] <<< DQMA#[0..7] 57,59  
 DQSA\_RN[0..7] <<<> DQSA\_RN[0..7] 57,59  
 DQSA\_WP[0..7] <<<> DQSA\_WP[0..7] 57,59



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**VRAM A Lower**

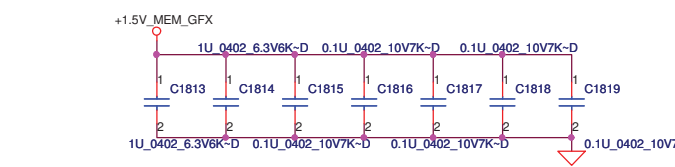
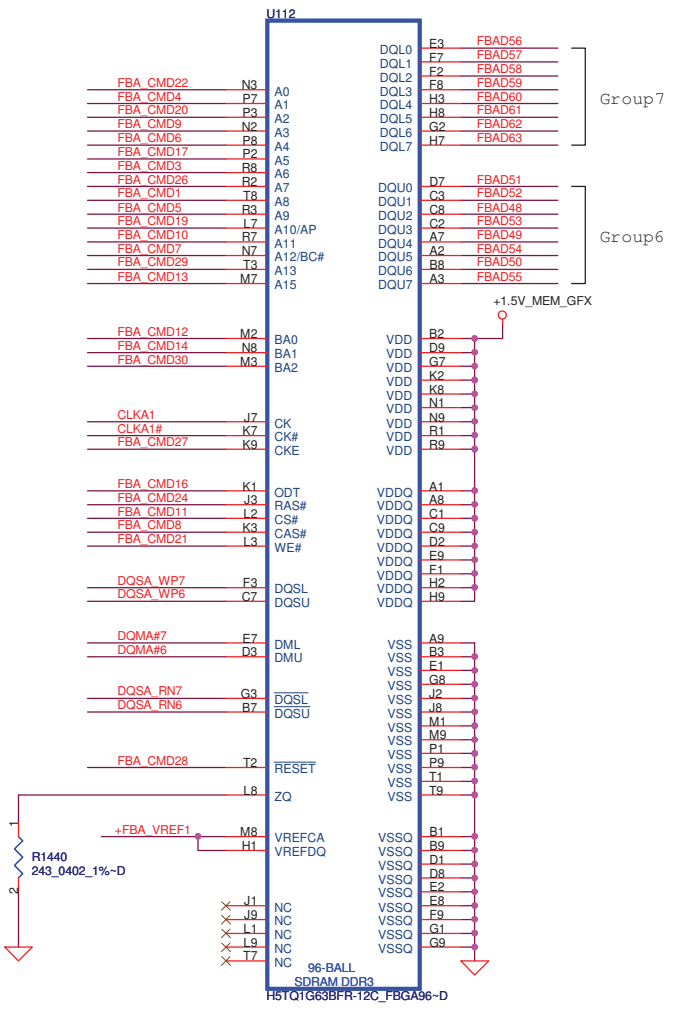
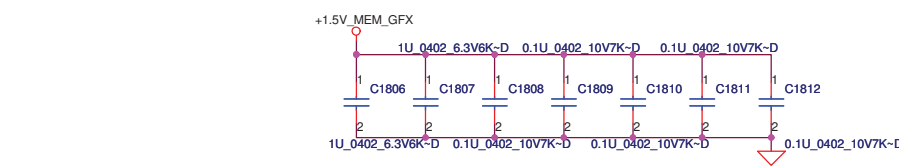
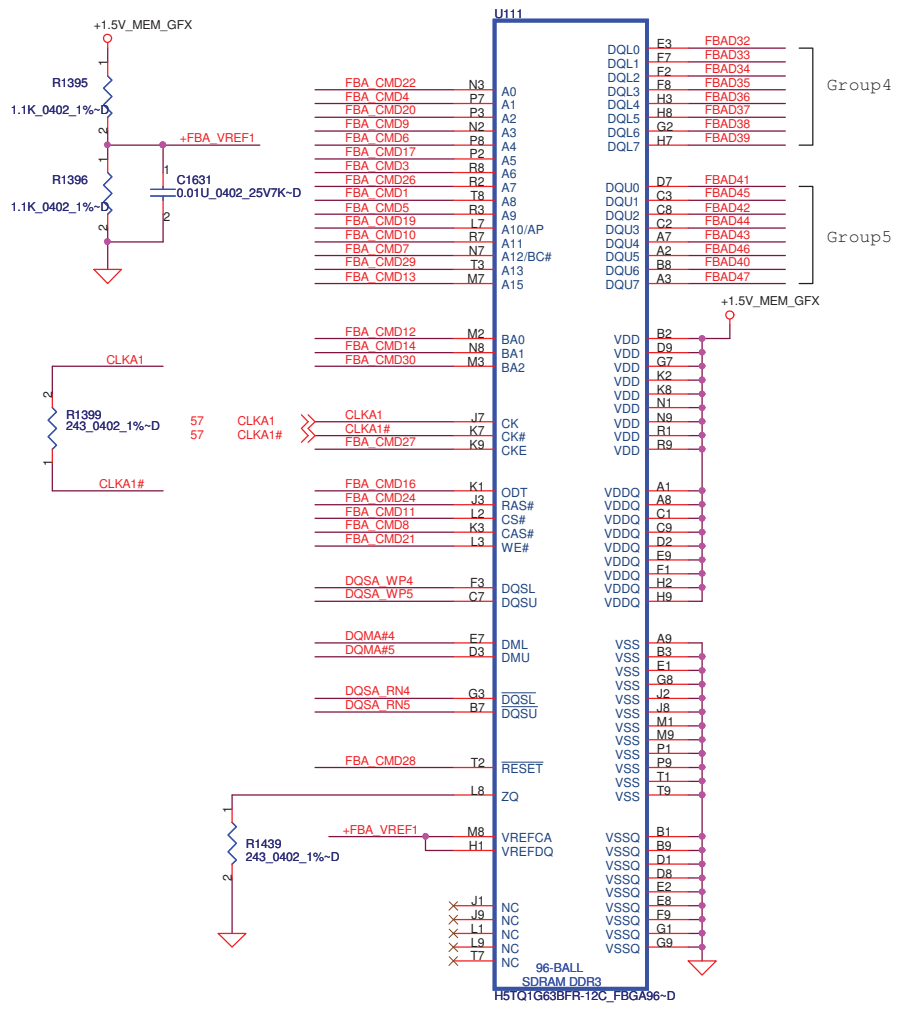
**LA-5573P**

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# Memory Partition A - Upper 32 bits

FBA\_CMD[0..30] <<< FBA\_CMD[0..30] 57,58  
 FBAD[0..63] >>> FBAD[0..63] 57,58  
 DQMA#[0..7] <<< DQMA#[0..7] 57,58  
 DQSA\_RN[0..7] >>> DQSA\_RN[0..7] 57,58  
 DQSA\_WP[0..7] >>> DQSA\_WP[0..7] 57,58



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**VRAM A Upper**

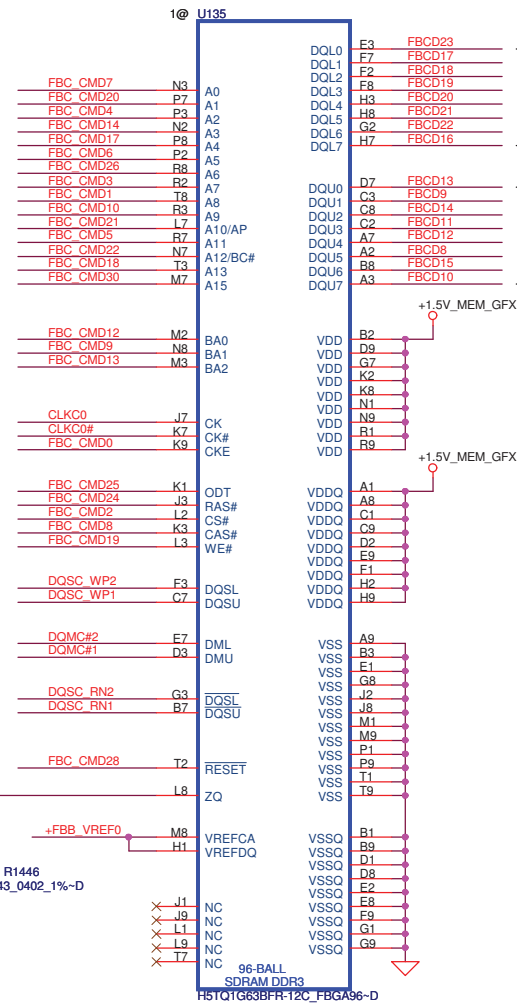
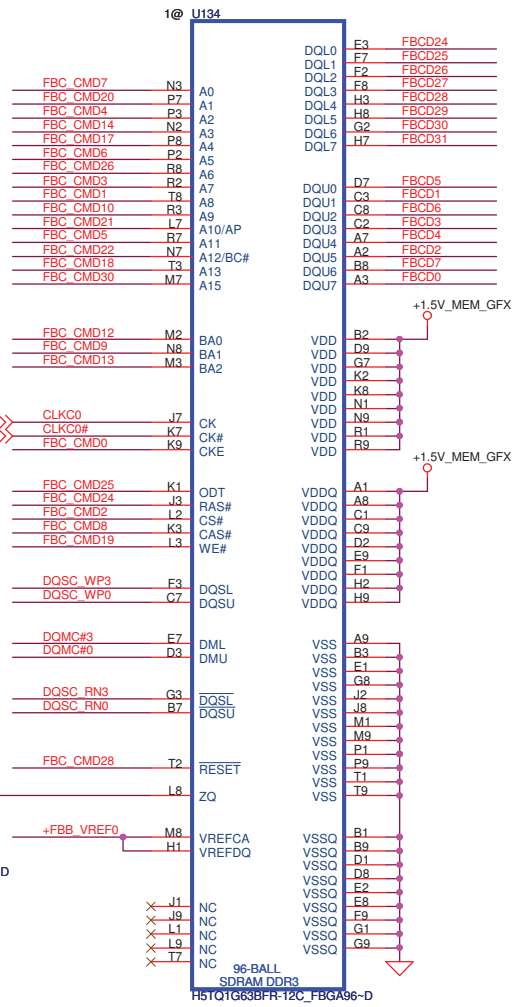
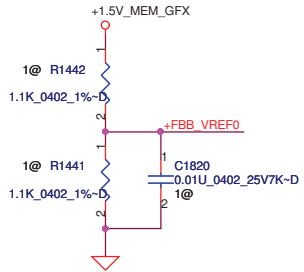
Document Number  
**LA-5573P**

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# Memory Partition C - Lower 32 bits

FB CD[0..63] <<>> FB CD[0..63] 57.61  
 FBC CMD[0..30] <<>> FBC\_CMD[0..30] 57.61  
 DQMC# [0..7] <<>> DQMC#[0..7] 57.61  
 DQSC RN[0..7] <<>> DQSC\_RN[0..7] 57.61  
 DQSC WP[0..7] <<>> DQSC\_WP[0..7] 57.61

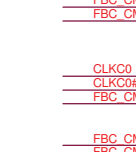


Group3  
Group0

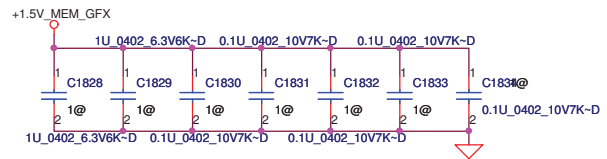
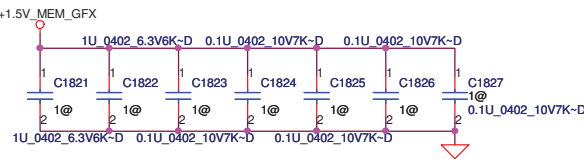
Group2  
Group1



57 CLKC0 <<>> CLKC0  
57 CLKC0# <<>> CLKC0#



57 CLKC0 <<>> CLKC0  
57 CLKC0# <<>> CLKC0#



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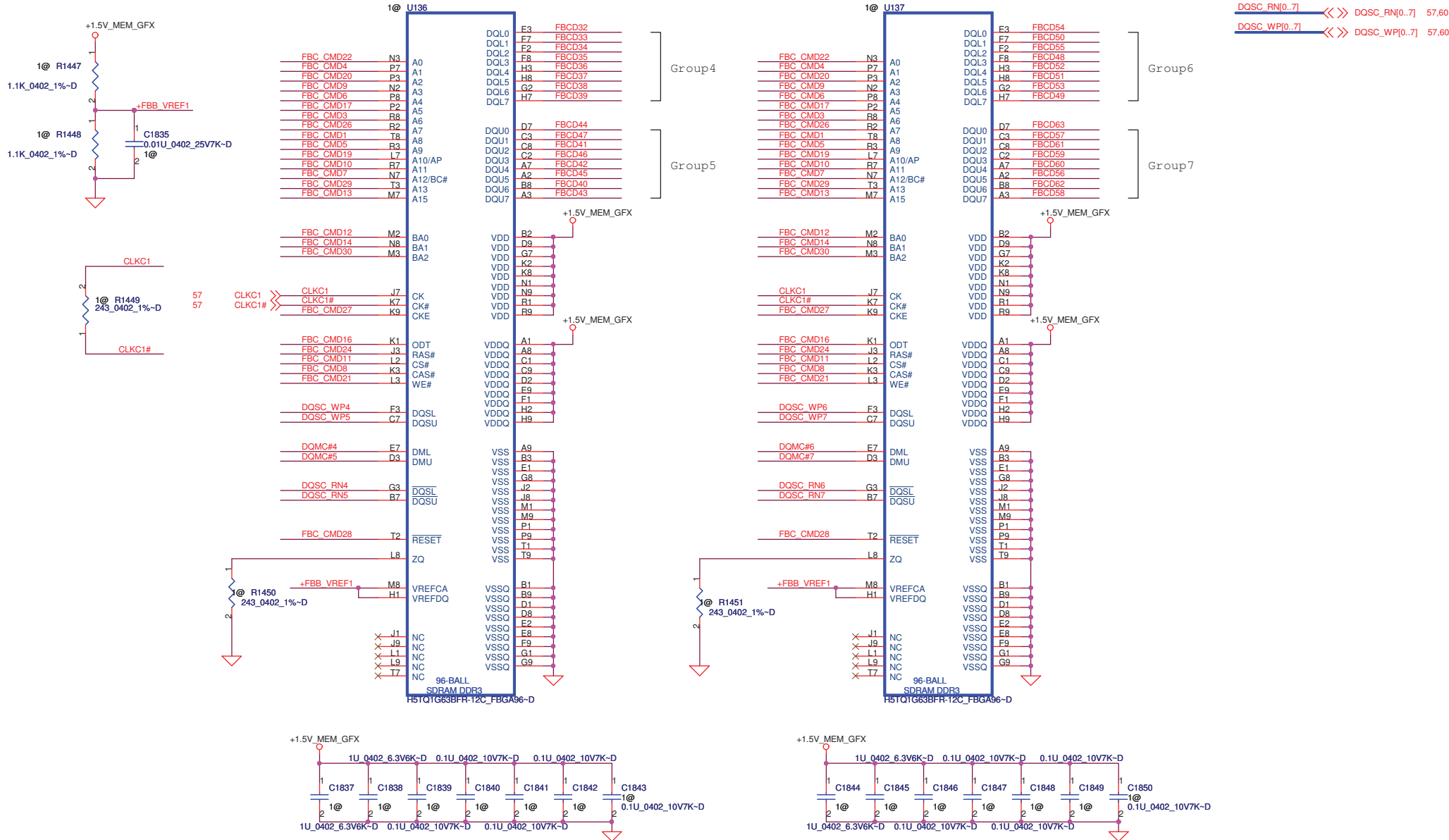
**VRAM C Lower**

**LA-5573P**


Title: \_\_\_\_\_  
 Size: \_\_\_\_\_ Document Number: \_\_\_\_\_  
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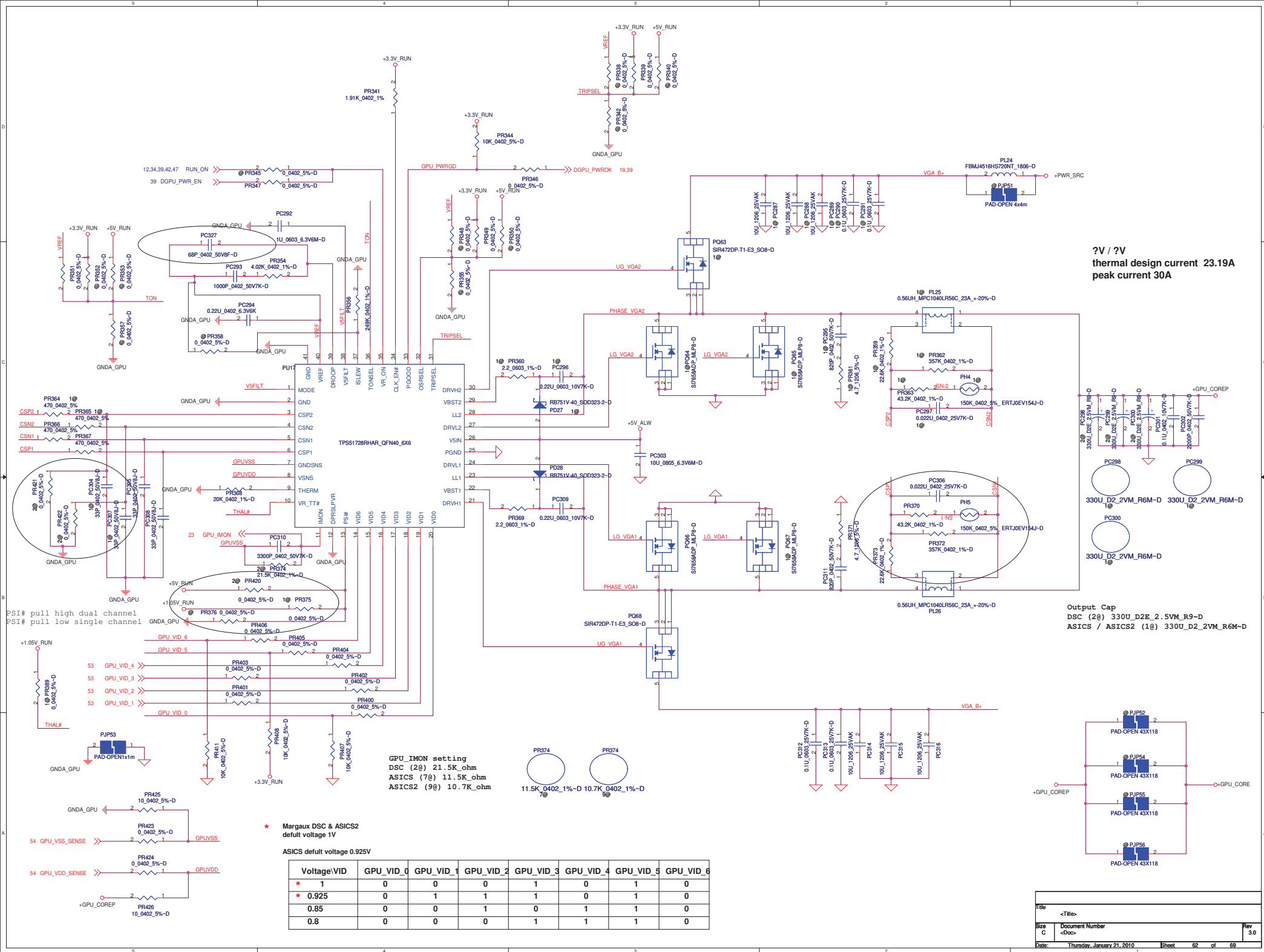
# Memory Partition C - Upper 32 bits

FB CD[0..63] <<> FB CD[0..63] 57,60  
 FBC\_CMD[0..30] <<> FBC\_CMD[0..30] 57,60  
 DOMC#[0..7] <<> DOMC#[0..7] 57,60  
 DQSC\_RN[0..7] <<> DQSC\_RN[0..7] 57,60  
 DQSC\_WP[0..7] <<> DQSC\_WP[0..7] 57,60

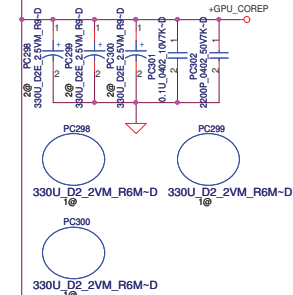


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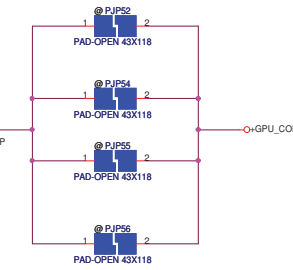
			<b>Compal Electronics, Inc.</b>		
			<b>VRAM C Upper</b>		
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?V / ?V  
 thermal design current 23.19A  
 peak current 30A



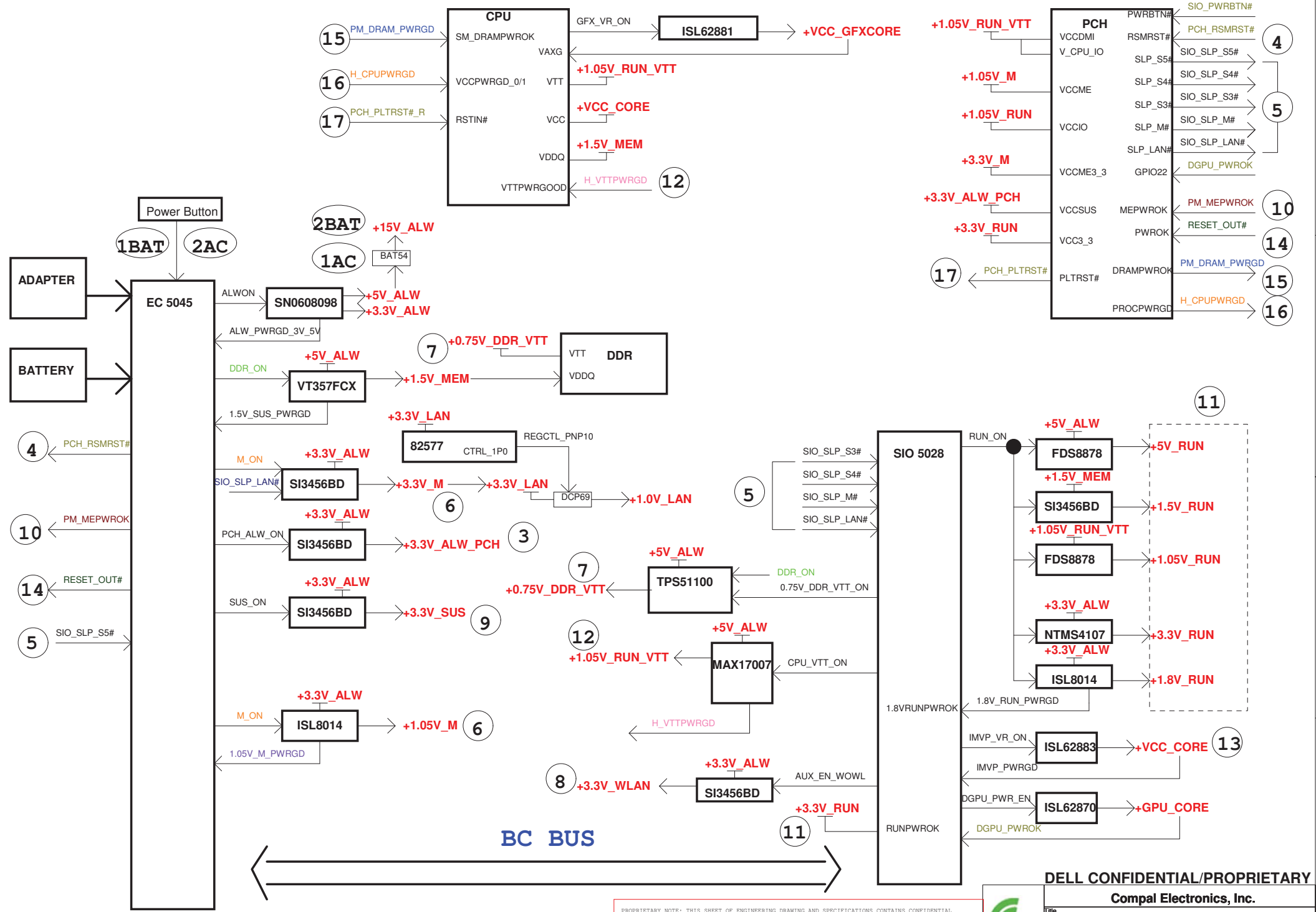
Output Cap  
 DSC (2@) 3300\_D2E\_2.5VM\_R9-D  
 ASICS / ASICS2 (1@) 3300\_D2\_2VM\_R6M-D



GPU\_IMON setting  
 DSC (2@) 21.5K\_ohm  
 ASICS (7@) 11.5K\_ohm  
 ASICS2 (9@) 10.7K\_ohm

\* Margaux DSC & ASICS2  
 default voltage 1V  
 ASICS default voltage 0.925V

Voltage/VID	GPU_VID_0	GPU_VID_1	GPU_VID_2	GPU_VID_3	GPU_VID_4	GPU_VID_5	GPU_VID_6
* 1	0	0	0	1	0	1	0
* 0.925	0	1	1	1	0	1	0
0.85	0	0	1	0	1	1	0
0.8	0	0	0	1	1	1	0



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<b>Power Sequence</b>		Rev 0.1
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# Version Change List ( P. I. R. List )

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	8, 12, 13, 14, 42	HW	6/30/2009	Intel	Intel S3 reduction circuit.	Add R1469, R1471-R1480, C1872-C1877, Q199-Q204, change R624 to 27 ohm, pop Q78, add net DDR_HVREF_RST_GATE from U36.B36, CPU1.5V_S3_GATE from U36.B37, change CPU VDDQ net name to +1.5V_CPU_VDDQ	X01
2	40	HW	6/30/2009	COMPAL	Board ID	R98 change to 130k ohm	X01
3	43	HW	6/30/2009	COMPAL	for derating concern	Change R1001 from 82 to 150 ohm	X00
4	8	HW	6/30/2009	Intel	Follow CRB by Intel request	R1286 needs to change to 0-ohm	X00
5	39, 40	HW	6/30/2009	COMPAL	MEMO implementation	de-pop R1319, R595	X00
6	8	HW	7/01/2009	Intel	Intel S3 reduction circuit.	Change R879 to 2k, R880 to 1.1k, add U141	X01
7	55	HW	7/01/2009	COMPAL	Rdson concern by ADC	Change Q55/Q58/Q59/Q183 to SI4164	X01
8	8, 42, 47	HW	7/02/2009	Intel	Intel S3 reduction circuit.	Add R1481-R1484, Q205, Q206, Q207, C1877, PR428, change R879 to 1.5k, R880 to 750 ohm, change net DDR_HVREF_RST_GATE to U36.A34, CPU1.5V_S3_GATE to U36.A36	X01
9	30	HW	7/03/2009	COMPAL	+3.3V_LAN enable control follow M09	De-pop R47	X01
10	12	HW	7/03/2009	DELL	Intel S3 reduction circuit.	De-pop R1473, separated +V_DDR_REF_Q for each SO-DIMM, The dividers should use 1% part replacement for 5% as well	X01
11	8, 12, 13, 14, 42	HW	7/08/2009	DELL Intel	Intel S3 reduction circuit.	Add C1879, PJP57, PJP58, R1485, R1486, change Q205 to PMST3904, Q200 to AO4728L, R624 to 22 ohm, connect RUN_ON_CPU1.5VS3# to Q78.2 Q204.2,	X01
12	8	HW	7/09/2009	COMPAL	Intel S3 reduction circuit.	Add R1487	X01
13	24	HW	7/14/2009	COMPAL	Nvidia BIA PWM implementation	POP R165, de-pop R166	X01
14	8, 15	HW	7/14/2009	COMPAL	Depop all related components where are located at 0 Z-hight area	Depop JXDP1, JXDP2, JDEG1, JP2 circuit	X02
15	24	HW	7/14/2009	DELL	ENVDD_PCH connection	Remove D91 and connect ENVDD_GPU to 5028.pin B38	X02
16	19	HW	7/14/2009	Intel	GPIO1,6,7 PU if not being used	Add R1489-R1491	X02
17	24	HW	7/14/2009	COMPAL	Camera need to be changed from 7 to 8 pin	Change JEDP1 pin definition	X02
18	37	HW	7/16/2009	COMPAL	JTP1, JBI01 power gnd pins redefined	Change JTP1, JBI01 pin definition	X02
19	37, 40	HW	7/16/2009	SMSC	LAT_ON_SW# needs to be added a luF cap	Add @C1884, C1885, R1492, change R560 to 100K, JIO.32 change to LAT_ON_SW_BTN#	X02
20	23	HW	7/16/2009	SMSC	R594 has to be a group with R3P circuit	De-pop R594 for M09 fan solution	X02
21	31	HW	7/17/2009	Braodcom	Found both PD R898 and PU R485 pop	depopulate R898 for normal operation	X02
22	40	HW	7/17/2009	COMPAL	Board ID	Change R98 to 62K ohm.	X02
23	31	HW	7/17/2009	Braodcom	RFID disable circuit remove	Remove R1062-R1065	X02
24	28, 37	HW	7/17/2009	TI	Please reserve 1 resistor and connect connector (Pin1 or 7) to MAX4951	Add R1493 & R1494 at pin 18 of U95 & U96 for power saving	X02
25	31	HW	7/17/2009	Braodcom	+SC_VCC Capacitor (C718) Value Change	Broadcom has recommended changing the value of C718 from .47uF to 220nF	X02
26	42	HW	7/17/2009	COMPAL	Backdrive EA Failure on Margaux/ASICS	Pop R625 and Q79	X02
27	24	HW	7/17/2009	DELL	eDP repeater change to SN75DP119.	update U46 circuit for eDP repeater	X02
28	23	HW	7/17/2009	COMPAL	R3P circuit by SMSC request	R536 depop for 3P FAN, R1457 change to 0 ohm, R138 change to 27K ohm	X02
29	21	HW	7/17/2009	Intel	The PLLs aren't used in a DIS system	De-pop C105 & C106	X02
30	33	HW	7/17/2009	TXC	EA result	C514, C515 have to change to 22pF	X02
31	36, 39	HW	7/22/2009	DELL	Reconnect the signal UWB_RADIO_DIS#	connect UWB_RADIO_DIS# from EC5028.A56 to MINI3.20	X02
32	23	HW	7/22/2009	DELL	Change FAN solution to M09	De-pop R3P circuit component & pop M09 solution	X02
33	42	HW	7/23/2009	COMPAL	de-rating result fail	Change Q61 from AO4456 to NTMS4107	X02
34	26	HW	7/23/2009	PERICOM	Pericom 8200 SW issue DVI can not work	Add R1495 to pull up U9 pin 23 (P1_OC0) of Pericom 8200 SW with a 4.7K ohm resistor to 3.3 RUN	X02
35	24	HW	7/23/2009	TI	eDP repeater DP119 vender review request	reserve pop option for X1EDP & DP119, change PU/PD to 20K.	X02
36	28	HW	7/23/2009	DELL	We will never disable the power to HDD redriver, go back connected in SSI	Remove R1493 & delete SATA_PWRSAVE	X02
37	18, 28, 40	HW	7/23/2009	DELL	There has been some confusion due to the net name showing active low	change net name HDD_FALL_INT1# to HDD_FALL_INT to show correct polarity	X02

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<b>EE PIR</b>			
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# Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
38	29	HW	7/24/2009	DELL	use the SiTimes part due to the cost savings	change X4 from TXC to SiTimes.	X02
39	31	HW	7/24/2009	Braodcom	connect pin-L10 of U32 to pin-5 of U33, and disconnect pin-D2 from pin-5 of U33	pop R775, de-pop R776	X02
40	33	HW	7/24/2009	COMPAL	fixed SD/MMC Clock overshoot and undershoot	Changing R8 dumping from 0-ohm to 10-ohm	X02
41	31	HW	7/24/2009	Braodcom	BCM5880 Leakage Issue on Margaux	Add Q208,Q209,R1496 circuit to fix.	X02
42	37, 39	HW	7/27/2009	DELL	ESATA repeater power saving	Add a 0 ohm jumper between EN pin and VDD, but no-pop it. Then connect the EN pin to 5028.A47 with a 0 ohm jumper that is popped.	X02
43	39	HW	7/27/2009	DELL	Sometimes VGA_ID_DISC and VGA_ID_UMA both read as low	Change R875 and R881 to +3.3V_ALW rail.	X02
44	23	HW	7/27/2009	SMSC	SMSC review feedback	The pull-up source of the R150 should be changed to +VCC_4002	X02
45	31	HW	7/27/2009	NXP	Better for decoupling noise	Change C1015 ,C633 to 10pf	X02
46	36	HW	7/27/2009	DELL	For PCH GPIOs rail.	PCIE_MCARD3_DET# & USB_MCARD1_DET# pull-ups (R458 & R438) need to change from +3.3V_ALW_PCH rail to +3.3V_RUN rail	X02
47	11	HW	7/27/2009	Intel	The VCC_Core de-coupling requirements for Clarksfield XE processor	C60-64, C66 change to 470uF/4mOhm, C44-C59 change to 22uF(0805)	X02
48	23, 40	HW	7/29/2009	SMSC	per SMSC 5045 AN 19.6, 4002 AN 16.11	R541, R554, R1492 should be 10K, R147 should be populate, Add R1498	X02
49	35	HW	7/29/2009	DELL	Braidwood has been removed from Ibex Peak platforms	De-pop JBW1 & R1453	X02
50	39	HW	7/29/2009	DELL	GPIO MAP update	change net name from RESERVED FOR ESATA to EN_ESATA_RPTR	X02
51	42	HW	7/29/2009	Compal	By Intel S3 timing concern	reserve R1500 & @R1499 0 ohm for Q206.2 from RUN_ON_CPU1.5VS3# & RUN_ON_ENABLE#	X02
52	37	HW	7/30/2009	Intel	Intel continues to recommend that all pre-production and production motherboards include common mode choke footprints to enable a stuffing option in case a choke is required to pass EMI testing	Add @L30, @L31, R424-R427	X02
53	31	HW	7/30/2009	Broadcom	Broadcom schematic review request	pop R537; Remove C647, C641,R634, R498, R898; Add @C1886 & @C1887; Remove L73, R631, C1026, R494, Short net RFREADER_TXN1_PI_R to RFREADER_RXP_C; Remove C642, C640, change R487, R496 to 0 ohm; Add @R1501; de-pop R496 & R497; JCS1 pin2 & pin3 and pin4 & pin5 should be short to carry higher current.	X02
54	31	HW	7/30/2009	Compal	Solve smart card cage vender reverse pin definition.	Reverse JSC1 pin definition	X02
55	31	HW	7/31/2009	Broadcom	Broadcom schematic review request	The pin1 of R497 and R496 should be connected to GND	X02
56	15, 40	HW	7/31/2009	KDS	KDS crystal EA result	change DIS C296 & C297 to 12pF, C674, C675 to 33pF	X02
57	8, 15	HW	7/31/2009	Intel	For XDP debug concern	Populate all the resistors and leave out the connector	X02
58	27	HW	8/03/2009	Compal	CRB EA result	C251-C253 to 4.7pF; L61-L63 to 10-Ohm Bead ; De-pop C996, C518, C390	X02
59	23	HW	8/03/2009	Compal	If populate R147 PU resistor for THERM_STP#, it will impact ALWON signal at MEC 5045	De-pop R147	X02
60	15, 40	HW	8/04/2009	KDS	KDS crystal EA result	change DIS C427 change to 200 ohm, C514, C515 back to 15P and change X3 from CL=16pF to CL=12pF	X02
61	8	HW	8/05/2009	DELL	fix the Intel S3 power up timing	change C1877 from 0.01uF to 0.22uF 0402 cap.	X02
62	28, 37	HW	8/06/2009	Compal	Per ESATA/SATA EA result	pop R1301, R1304, de-pop R1298, R1308	X02
63	28	HW	8/06/2009	Compal	ODD_DET# PU from +5V_MOD to +3.3V_RUN	connect R1239.1 to +3.3V_RUN & pop R1239	X02
64	42	HW	8/06/2009	SMSC	Watch dog timer may not be resetED when 4002 VDD_PWRGD is not completely at Logic Low	Pop R616 to 39 & pop Q72	X02
65	30	HW	8/10/2009	Intel	Remove the VCT trace	Remove @R562, @C41	X02
66	35	HW	8/10/2009	DELL	Braidwood Removal on RAM	Remove @JBW1, @C1851, @R1452, @R1453, @C1852, R1411	X02
67	31	HW	8/11/2009	Broadcom	Broadcom review request	Remove @R1061, Change C718 value to 470pF, change C646 value to 220pF. pin2 of R470 should have a 0ohm but de-pop resistor to USB_GPIO27 net.	X02

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
68	8	HW	8/11/2009	Intel	Intel review request	add @R1504 for DDR3_DRAMRST# CPU PD & add C1888 for PM_DRAMRST# to slow down gate of FET	X02
69	33	HW	8/11/2009	Richo	Change pop option for R5U242	Change C21 from 10U to 47U, change R46 to C1889 (1uF)	X02
70	38	HW	8/11/2009	Compal	For DVI DOCK issue	Add R1505-R1508	X02
71	21	HW	8/12/2009	Intel	Follow CRB rev 1.6 schematic	No stuff C111 and C112	X02
72	31	HW	8/12/2009	Broadcom	Per Broadcom request	pop R496 & R497 (0 ohm)	X02
73	31	HW	8/12/2009	Compal	Smart card EA result	change R772 to 47 Ohm for resolving SC_CLK Rise/Fail timing issue	X02
74	8	HW	8/12/2009	Intel	Follow Intel S3 white paper rev0.9	pop R1504 & change C1888 to 470pF	X02
75	37	HW	8/12/2009	DELL	add a pull-up to +3.3V_ALW for IO_LOOP	change R835.1 from +3.3V_ALW_PCH to +3.3V_ALW	X02
76	37	HW	8/12/2009	Compal	disconnect IO & DOCK VCT	rename IO VCT to +LOM_VCT_IO & reserve C712 pad for test.	X02
77	31	HW	8/13/2009	Broadcom	Per Broadcom request	need to have 4.7K pull-up to 3.3V_ALW for BCM5882 pin-C1 "RSTOUT_N"	X02
78	8	HW	8/13/2009	DELL	Avoid a glitch for DDR_HVREF_RST_GATE, please add a 1.1K 1% no-stuff pull-up to +1.5V_CPU_VDDQ rail on the PM_DRAM_PWRGD_R signal for a back-up option	change C1888 to 0.1u, add @R1511 for PM_DRAM_PWRGD_R	X02
79	8,45	HW	8/13/2009	DELL	CPU detection since the edge diode has been removed from M'09	Add R1512 for CPU_DETECT# and connect JCPU.AH24 to U36.B18	X02
80	37	HW	8/14/2009	DELL	Invert the EN_ESATA_RPTR signal and connect this to SATAGP4/GPIO16	Add @R1513 & @Q210, pop R1494 and de-pop R1497, change net name from GPIO16 to EN_ESATA_RPTR#	X02
81	33	HW	8/14/2009	Compal	Solve 1394 impedance issue	Change R399, R400, R401, R403 to 54.9 ohm.	X02
82	37	HW	8/14/2009	Compal	EMI solution	pop L30 & L31, de-pop R424-R427	X02
83	38	HW	8/17/2009	NV	Solve DIV issue	Add Q211-Q216, R1514-R1521 for SW DDC PU.	X02
84	11	HW	8/17/2009	Compal	PWR team request	de-pop C66, C64, change C60-C63 to 330uF, C44-C59 to 10uF, can meet Intel spec.	X02
85	55	HW	8/18/2009	NV	Reserve crystal for 27M.	add @R1522, @y7, @C1890, @C1891	X02
86	26	HW	8/19/2009	Pericom	8200 pin 8,9 add cpas to minimize noise	Add C1597 & C1598	X02
87	29	HW	8/19/2009	COMPAL	EMI solution	C676 to 150pF and R1295 to L4 (220 ohm), POP C1121-C1124, C1145-C1148	X02
88	33,34	HW	8/20/2009	COMPAL	EMI solution for SD CLOCK & EXP card USB	R8 change to 22 ohm, pop L64 & depop R791, R792	X02
89	11	HW	9/11/2009	DELL	To meet Intel spec	C60-C63, Margaux DIS-->330uF, Asics/Asics II-->470uF	X02
90	55	HW	9/11/2009	DELL	27M crystal for NV	add Y7, C1890, C1891, R1522, R1417, de-pop R617, R1317, R43, R39	X02
91	21	HW	9/11/2009	Intel	Intel request	de-pop C39, C610	X02
92	31	HW	9/11/2009	Broadcom	Broadcom review feedback	change C718 from 470p to .47u, C646 from 220p to .22u	X02
93	30	HW	9/11/2009	Intel	Follow Intel document request	change R1502 to C427 10pF, C475, C476 to 33pF	X02
94	35	HW	9/11/2009	Compal	Add PD 10k for Minicard PWR	Add R1523-R1525	X03
95	31	HW	10/23/2009	Compal	Smart card connector DFM issue	change JSC1 type (the same with Rothschild)	X03
96	54	HW	10/23/2009	NV	JTAG TRST#: Populate R1372 with 1K resistor.	Change R1372 to 1K and pop	X03
97	40	HW	10/23/2009	COMPAL	Board ID	Change R98 to 4.3K ohm.	X03
98	17	HW	10/23/2009	Intel	Intel schematic check list 2.0 request	R268 change from 1k ohm to 10k ohm, R672 change from 0.5% to 5%	X03
99	40	HW	10/23/2009	SMSC	SMSC review feed back	R561 and R1046 are too large it is recommend that no PU/PD be larger than 100K	X03
100	12,42	HW	10/23/2009	COMPAL	avoid double bleed off	+3.3V_M, +3.3V_RUN, +1.5V_CPU_VDDQ power plane discharge circuit have been pop, de-pop R612, R607, R1471.	X03
101	36	HW	10/23/2009	DELL	support WiMax LED status	Need to populate R840	X03
102	16,32	HW	10/25/2009	COMPAL	Change R910 placement	Please put R910 close to PCH not TCM chip	X03
103	41	HW	10/25/2009	COMPAL	Touch Pad PU need to move from 5V to 3V	R613, R614 change power rail from +5V_ALW to +3.3V_ALW	X03
104	31	HW	10/28/2009	Broadcom	For 5882-B0 request	L71, L72 68nH, 2%, 400mA; C1070, C1071 1500pF, 2%, 50V; C1886, C1887 150pF, 2%, 50V	X03
105	29	HW	10/28/2009	IDT	create a low pass filter with the pole set at 36kHz to filter out of band noise	de-pop C1066 & C1067, R1090, R1089 ; R340 & R342, R1091 & R1092 change to 2k, add C1894-C1897 1000pF.	X03
110	29	HW	10/28/2009	COMPAL	ME request for JSPK1 swap	JSPK1 Pin 2 and pin 4 swap, pin 3 and pin 5 swap	X03

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
111	8, 12, 13, 15, 16, 28	HW	10/29/2009	DELL	MEM SMBus design needs to change	Move Q190 connection, add R1528,R1529, add net name DDR_XDP_CLK/DAT	X03
112	31	HW	10/29/2009	DELL	smart card clock resistor	Change R772 from 47 ohm to 22 ohm	X03
113	37	HW	10/29/2009	COMPAL	EMI concern	pop R15 with 10 ohm and C15 with 10pF	X03
114	36	HW	10/29/2009	COMPAL	USB MCARD2_DET# change to +3.3V_ALW_PCH	R447 pull up should change to +3.3V_ALW_PCH	X03
115	40	HW	10/29/2009	COMPAL	avoid RESET_OUT# double PD	de-pop R5	X03
116	15	HW	11/02/2009	COMPAL	EMI, RF team concern	pop C300, C302	X03
117	24	HW	11/04/2009	COMPAL	LCD power sequencing issue	change R161 from 470 to 130 ohm .	X03
118	37	HW	11/05/2009	COMPAL	EMI concern	Change choke vender from Murata to Delta on L30,L31	X03
119	29	HW	11/05/2009	COMPAL	RF team concern	X4 change from Sitime to TXC	X03
120	15	HW	11/05/2009	COMPAL	RTC issue	Y1 & Y4 change from 30ppm to 10ppm.	X03
121	15	HW	11/05/2009	COMPAL	For flash ROM EOL issue	U13 change from W25X32 to W25Q32	X03
122	19	HW	11/09/2009	DELL	PCH driving the siganl low at GPIO15 initial	add R1530 2.2K PU resistor to +3.3V_ALW_PCH on the SIO_EXT_WAKE# signal.	X03
123	55	HW	11/10/2009	COMPAL	By power team request	Please pop 22u*2 at original reserved location C1722 and C1723.	X03
124	39	HW	11/10/2009	DELL	add a 10K 5% PU to +3.3V_RUN on ME_FWP	Add R1531	X03
125	24, 53	HW	11/11/2009	NV	By NV review request	pop R180, de-pop R181; change GPU booting voltage setting, GPU_VID1: @Q4, 7@R1374, 8@R1361, GPU_VID4:pop R1379, GPU VID2: 7@R1357, 8@R1360, GPU_VID3: pop R1354	X03
126	15, 28	HW	11/13/2009	COMPAL	To cut redundant trace for SMBUS	Add @R1532/R1533/R1534/R1535	X03
127	19	HW	11/17/2009	Intel	By Intel check list request	Add R1544 for PCH GPIO34	X03
128	41	HW	12/24/2009	Compal	To solve touch pad ESD issue	Change L41 and L42 to R1545 & R1546 with 100 ohm.	X03
129	29	HW	12/24/2009	Compal	RF noise issue concern	change Sitime 12MHz oscillator X4 to driver strength 1x	X03
130	15	HW	12/24/2009	Intel	Follow Intel check list rev2.0	Change R224 to tolerance from 5% to 1%	X03
131	36	HW	12/24/2009	DELL	Wimax LED abnormal operation.	de-pop R1409	X03
132	11	HW	12/24/2009	Compal	PWR team request	Change C60-C63, add C66 to 330uF for Ascis/AsicsII	X03
133	38	HW	12/24/2009	Compal	Simplo battery slice EMI issue	Add C1898 and C1899(Depop, reserve for EMI test)	A00
134	31	HW	12/24/2009	Braodcom	By Broadcom request	Change L71,L72 from 68nH to 150nH, C1070,C1071 from 1500pF to 390pF.C1887, C1888 from 150pF to 390pF.	A00
135	40	HW	12/30/2009	DELL	Board ID	Change R98 from 4.3K to 1K for A00	A00
136	33, 34	HW	12/30/2009	COMPAL	Change R5U242 to rev ES3	Change U94 from ES2 to ES3	A00
137	8, 15	HW	12/30/2009	Intel	De-pop XDP & JTAG resistor	de-pop C19,C20,R6,R7,R68,R19,R3,R1153,R1156,R1157,R66,R1241,R780-R785, R22,R24,R78,R91,R101-R116,C1375,R69,R118,R123,R804,R807,R805,R806,R1281, R1282,R1315	A00
138	28, 37	HW	01/15/2010	COMPAL	Change Esata repeater for power save	Change U95 U96 from 412 to 412A	A00
139	27	HW	01/15/2010	COMPAL	EMI concern	Change L61-L63 to 27nH, C251-C253 to 2P, pop C390, C518, C996	A00
140	11	HW	01/18/2010	COMPAL	No stuff MLCC caps to fix Acoustic noise	de-pop C46, C48, C50, C52	A00
141	15	HW	01/21/2010	COMPAL	For factory to do JTAG test	Pop R123, R804-R807, R1281, R1282, R1315	A00

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1	50	+VCORE_DSC	6/12	Dell	Adjust Vimon	ASICS and ASICS2 Change PR184 to 7.5K	
2	62	Graphic ASICS	6/19	TI	Adjust compensation	DSC Change PR370 to 43.2K, PR372 to 357K, PR373 to 22.6K, PC 306 to 0.022uF ASICS/ASICS2 Change PR370&PR363 to 43.2K, PR372&PR362 to 357K, PR373&PR359 to 22.6K, PC306&PC297 to 0.022uF	
3	62	Graphic ASICS	6/19	TI	Droop circuit add cap for filtering the noise	DSC, ASICS and ASICS2 Change PD26 to PC327 68pF	
4	62	Graphic ASICS	6/19	TI	Adjust to operate single phase	DSC PR364,PR365,PC304,PC307 unpop and add PR421&PR422 0_ohm to avoid PIN3,4 floating Add PR420 0_ohm connect +5V_RUN to control PSI# for Single phase	
5	62	Graphic ASICS	6/30	TI	add 0_ohm for cut power rail to debug	Add PR423 PR424 PR425 PR426	
6	62	Graphic ASICS	7/01	TI	CSS GC logic wrong issue	Add PR427 180_ohm to GND	
7	62	Graphic ASICS	7/2	ADC Guangyong 090612	Change PR374 and PC310 reference GND to GPUVSS	connect PR374 and PC310 pin1 to GPUVSS	
8	50	+VCORE	7/14	Dell / intersil	change Cisense GND to VSUM-	PC174 PC175 PC176 pin2 connect to VSUM-	
9	52	Selector	7/16	Compal	Add 1M_ohm pull down to fix ACAV_IN_NB oscillation when battery mode S5	Add PR429	
10	52	Selector	7/22	TI	new version CD3301 (PG2.1) dont need PD21	un-pop PD21 add PR430	
11	53	Selector	7/22	TI	DOCK_AC_OFF_EC floating issue	add PR431	
12	62	Graphic ASICS	8/3	TI	Pin38 V5FILT is output pin. don't need to connect to power rail.	Delete connection to +5V_RUN	
13	45 / 49 50 / 51	+5V/+3.3V +1.1VTT +Vcore charger	8/11	Compal / EMC	solve EMI issue	pop PC32 PC33 PR36 PR39 PL15 PC155 PC165 PC182 PR153 PR173 PR191 PL24 add PL27	
14	50	+VCORE	8/13	Intersil	Adjust Imon and Load line	PR195 change to 619, PR175 change to 2.43K, PR387 change to 15K PR184 change to 8.45K, add PR432 34.8K and PQ75 (PR432 and PQ75 un-pop Merle 0820) PC171 change to 0.068uF, PC183 add 0.022uF	
15	49	+1.1VTT	8/13	DELL	Improve ESD	PQ74 change SB57002528L to SB00000DH0L	
16	51	Charger	8/13	Dell / TI	change PU13 to BQ24747 to improve IC ESD to change strong	change PU13 from SA00001RK0L to SA00003KX0L	
17	48	+1.05V_VM_DSC	8/13	TI	change from TPS51318 to SN0905030	change PU8 to SN0905030	
18	45	+5V/+3.3V	8/17	TI/Compal	adjust OCP setting	Change PR31 from 243K to 294K, PR32 from 232K to 261K(DSC) 158K(ASICS)	
19	46	+1.5V_MEM_DSC	8/17	TI/Compal	adjust OCP setting	Change PR71 from 61.9K to 39.2K	
20	50	+VCORE	0820	Dell EMC	Add 2 2200pF caps. (jerry lin 0820)	Add PC328 PC329	

