

CHELSEA DJ2 UMA Schematics Document

AMD Danube CPU S1G4

RS880M + SB820M


2010-04-13

REV : X01

DY : Nopop Component
HDMI : Pop for HDMI function
GIGA : Pop for GIGA LAN
10/100 : Pop for 10/100 LAN

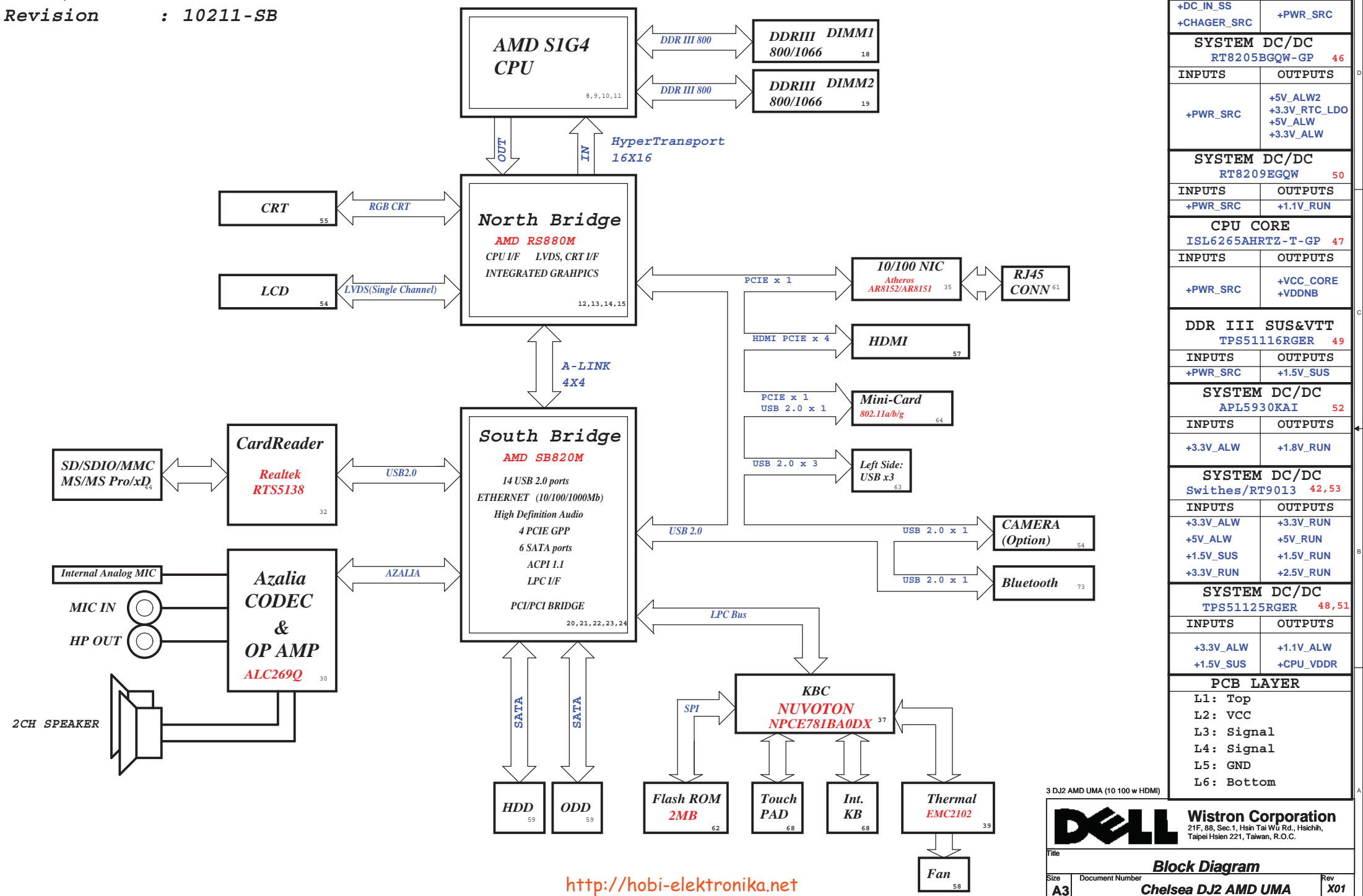
<http://hobi-elektronika.net>

3 DJ2 AMD UMA (10 100 w HDMI)

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title Cover Page		
Size Custom	Document Number Chelsea DJ2 AMD UMA	Rev X01
Date: Tuesday, April 13, 2010	Sheet 1 of 90	

Project code : 91.4EM01.001
 PCB P/N : 48.4EM18.0SA
 Revision : 10211-SB

Chelsea DJ2 AMD UMA Block Diagram



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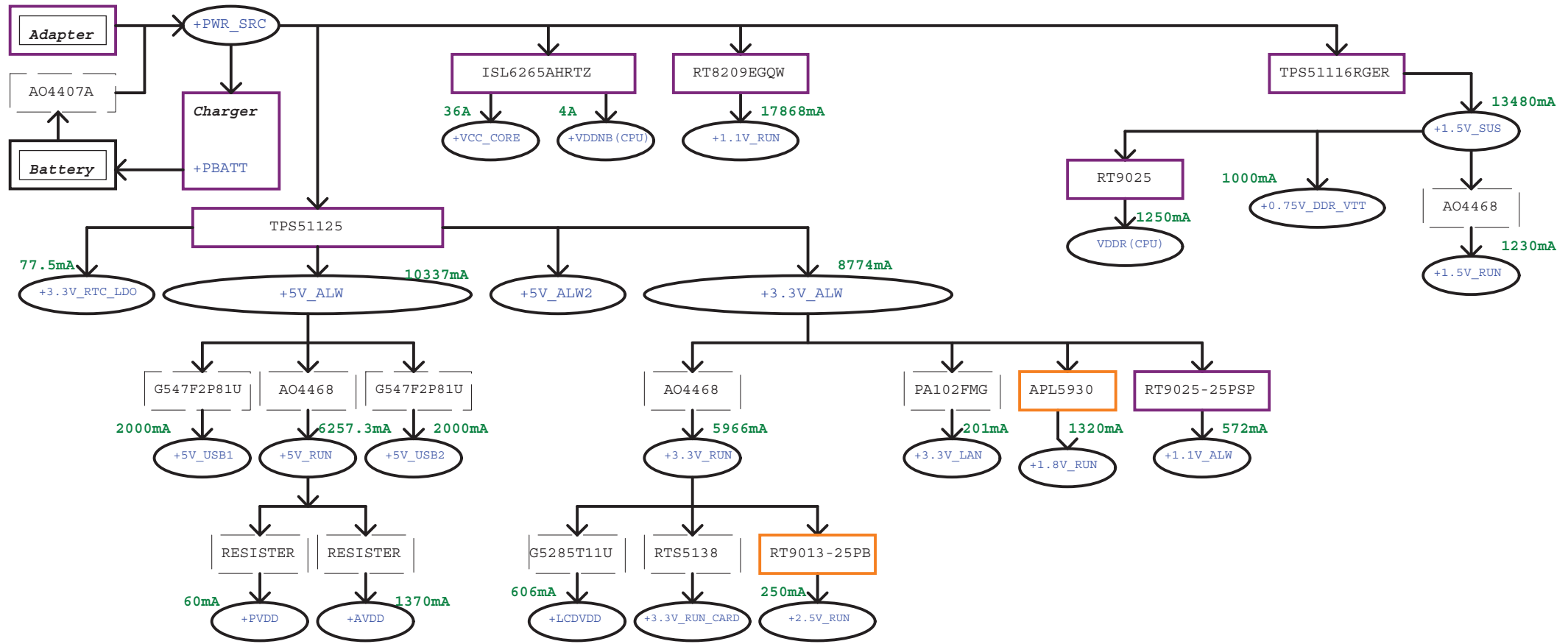
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Title: **Block Diagram**

Size: A3	Document Number: Chelsea DJ2 AMD UMA	Rev: X01
Date: Tuesday, April 13, 2010	Sheet 2 of 90	

Power Block Diagram

Power Shape



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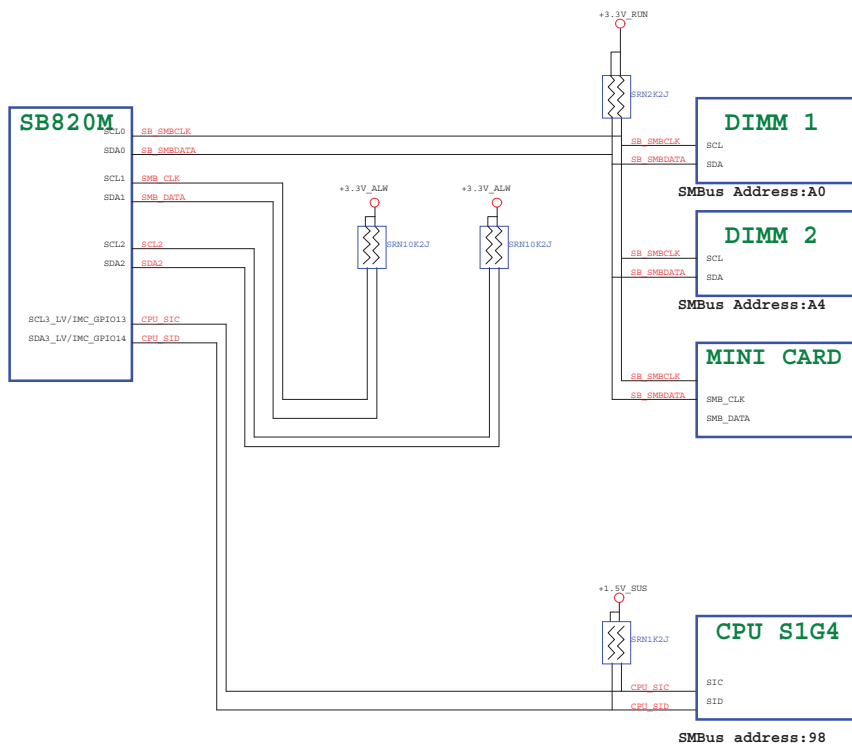
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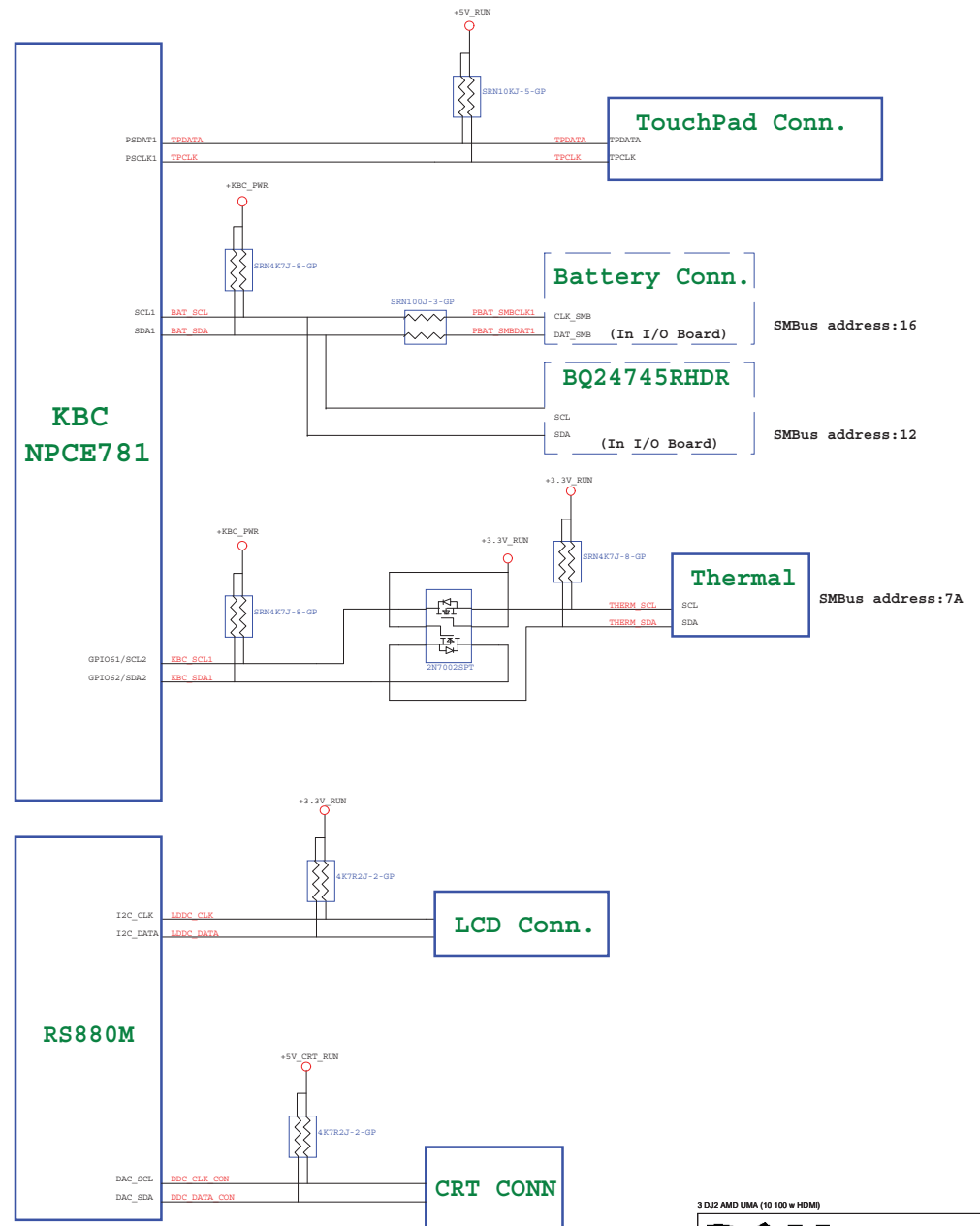
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Size: Custom	Document Number: Chelsea DJ2 AMD UMA	Rev: X01
Date: Tuesday, April 13, 2010	Sheet: 3 of	90

SB820M SMBus Block Diagram

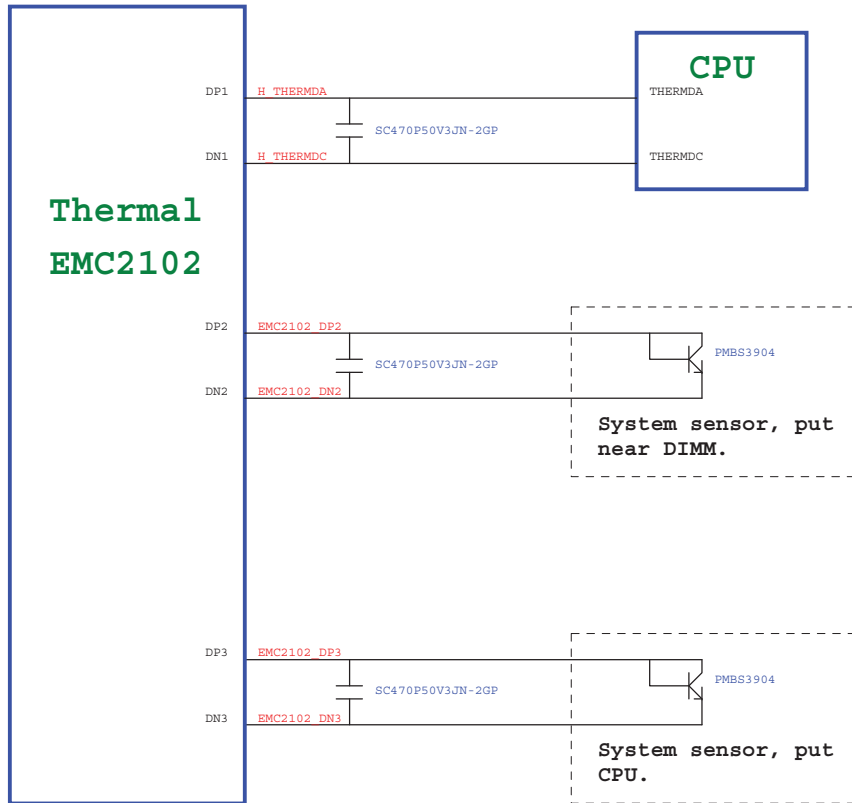


KBC SMBus Block Diagram

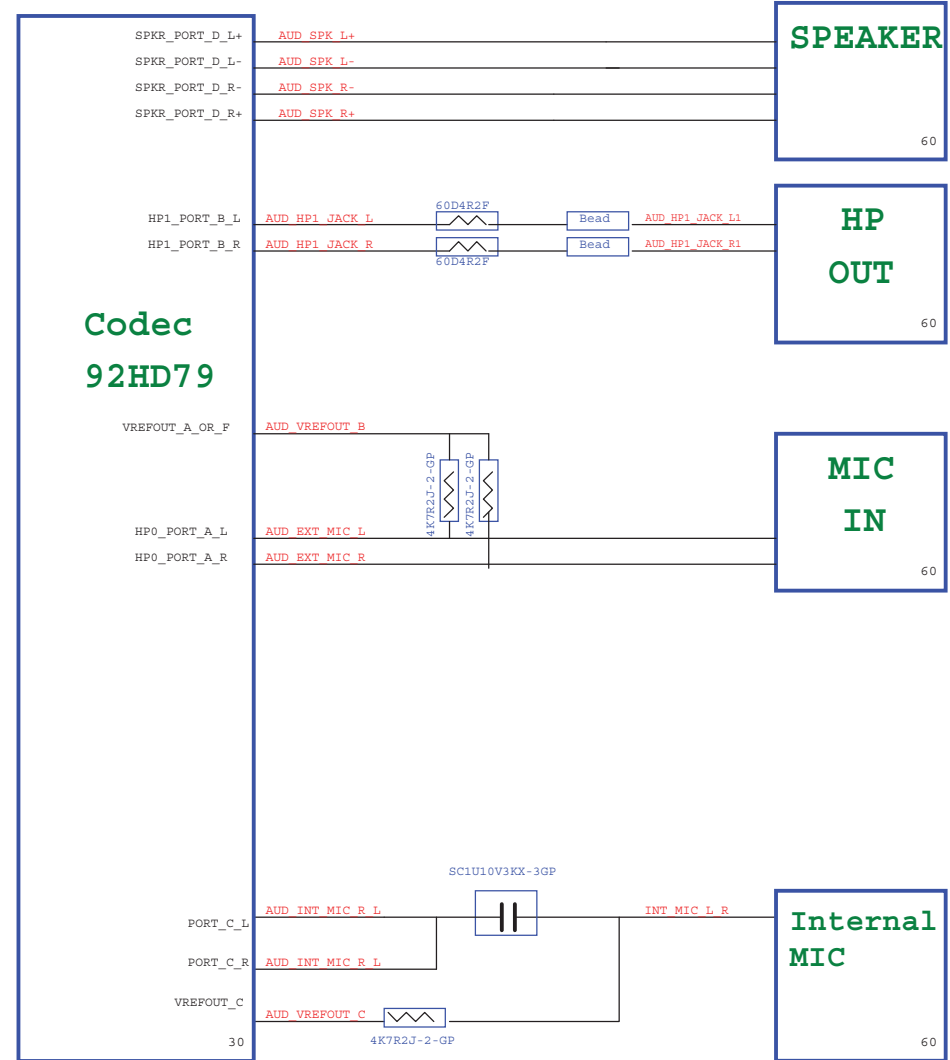


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Thermal Block Diagram



Audio Block Diagram



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		Title THERMAL/AUDIO BLOCK DIAGRAM	
Size	Document Number	Rev	
Custom	Chelsea DJ2 AMD UMA	X01	
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SB820M Strapping

Capture from 45484 Rev. 1.02 AMD SB8xx-Series Southbridge Design Guide

Name	Strap Name	Schematic Note
LPCCLK0	ECEnableStrap	Embedded Controller (EC) * 0 V - Disabled 3.3 V - Enabled
EC_PWM3 EC_PWM2	{ROMTYPE_1, ROMTYPE_0 }	ROM TYPE 3.3V ROMTYPE_1 0V ROMTYPE_0 SPI ROM 3.3V 3.3V Reserved 0V 0V Firmware Hub 0V 3.3V * LPC ROM (supports both LPC and PMC ROM types)
LPCCLK1	CLKGEN	Defines clock generator 0V - External clock mode: Use 100-MHz PCIe clock as reference clock and generate internal clocks only. * 3.3V- Integrated clock mode: Use 25-MHz crystal clock and generate both internal and external clocks
PCICLK1	BIF_GEN2_COMPLIANCE_Strap	Set PCIe to Gen II mode 0V- Force PCIe interface at Gen I mode * 3.3V- PCIe interface is at Gen II mode Not Applicable to SB820M but provision for pull-down is required.
PCICLK2	BootFailTmrEn	Watchdog function * 0V- Disable the boot fail timer function 3.3V- Enable the boot fail timer function
PCICLK3	DefaultStrapMode	Default Debug Straps * 0V- Disable Debug Straps. 3.3V- Select external Debug Straps
PCICLK4	CPUClkSel	CPU/NB HT Clock Selection 0V- Reserved. * 3.3V- Required setting for integrated clock mode. This strap is not used if the strap CLKGEN is configured for external clock generator mode.
AZ_SDOUT	CoreSpeedMode	Slow down core clock for low power platform. * 0V- Performance mode 3.3V- Low Power mode

NB880M Strapping

Capture from 46113 rs880m ds nda 1.03

Name	Strap Function	Schematic Note
DAC_VSYNC	STRAP_DEBUG_BUS_GPIO_ENABLE#	Enables debug bus access through memory I/O pads and GPIOs. 0: Enable * 1: Disable
DAC_HSYNC	SIDE_PORT_EN#	Indicates if memory side-port is available or not 0: Available * 1: Not available
SUS_STAT#	LOAD_EEPROM_STRAPS#	Selects loading of strap values from EEPROM. 0: I2C master can load strap values from EEPROM if connected, or use default values if EEPROM is not connected. Please refer to RS880M's reference schematics for system level implementation details. * 1: Use default values

USB Table

USB	
Pair	Device
0	USB1
1	USB3
2	USB2
3	USB1 (I/O Board, 17")
4	WLAN
5	Reserve
6	Reserve
7	Reserve
8	Reserve
9	Reserve
10	CARD READER
11	CAMERA
12	BLUETOOTH
13	Reserve

PCIE Routing

LANE0	MiniCard WLAN
LANE1	LAN

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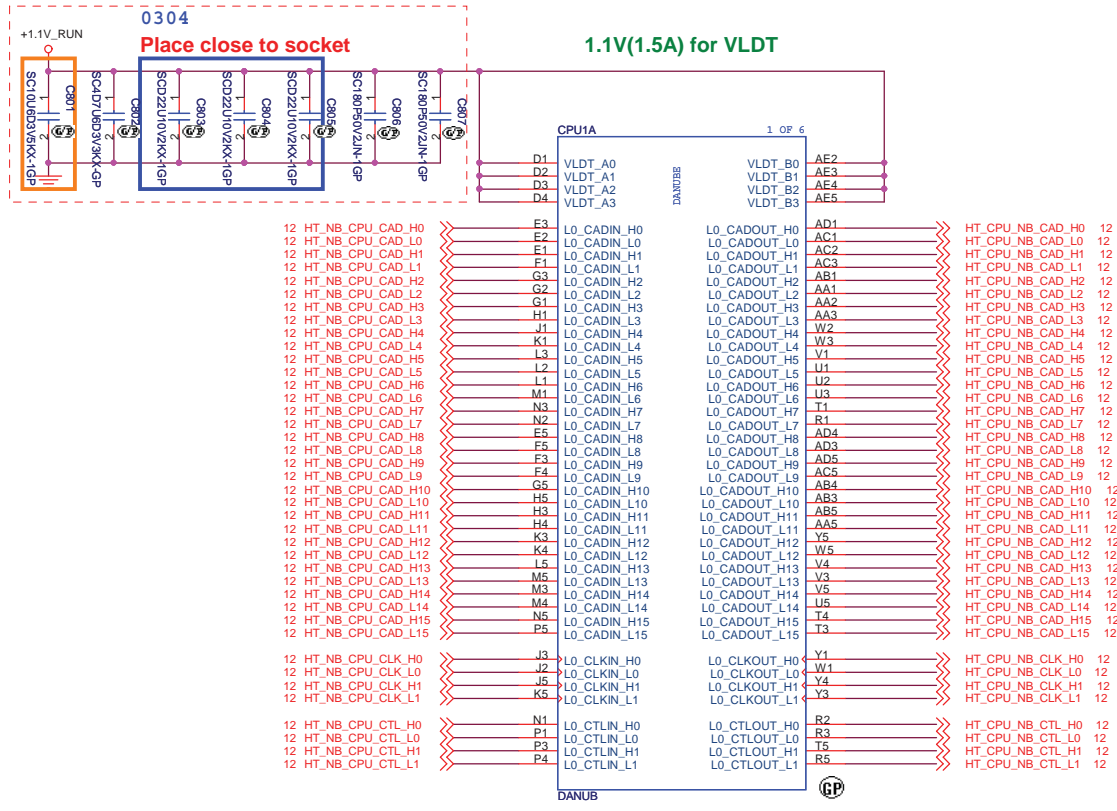
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3 DJ2 AMD UMA (10 100 w HDMI)

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Title Clock Generator ICS9LPRS480		
Size Custom	Document Number Chelsea DJ2 AMD UMA	Rev X01
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SSID = CPU



12 HT_NB_CPU_CAD_H0	E3	L0_CADIN_H0	L0_CADOUT_H0	AD1	HT_CPU_NB_CAD_H0	12
12 HT_NB_CPU_CAD_L0	E2	L0_CADIN_L0	L0_CADOUT_L0	AC1	HT_CPU_NB_CAD_L0	12
12 HT_NB_CPU_CAD_H1	F1	L0_CADIN_H1	L0_CADOUT_H1	AC2	HT_CPU_NB_CAD_H1	12
12 HT_NB_CPU_CAD_L1	G3	L0_CADIN_L1	L0_CADOUT_L1	AC3	HT_CPU_NB_CAD_L1	12
12 HT_NB_CPU_CAD_H2	G2	L0_CADIN_H2	L0_CADOUT_H2	AA1	HT_CPU_NB_CAD_H2	12
12 HT_NB_CPU_CAD_L2	G1	L0_CADIN_L2	L0_CADOUT_L2	AA2	HT_CPU_NB_CAD_L2	12
12 HT_NB_CPU_CAD_H3	H1	L0_CADIN_H3	L0_CADOUT_H3	AA3	HT_CPU_NB_CAD_H3	12
12 HT_NB_CPU_CAD_L3	J1	L0_CADIN_L3	L0_CADOUT_L3	W2	HT_CPU_NB_CAD_L3	12
12 HT_NB_CPU_CAD_H4	K1	L0_CADIN_H4	L0_CADOUT_H4	W3	HT_CPU_NB_CAD_H4	12
12 HT_NB_CPU_CAD_L4	L3	L0_CADIN_L4	L0_CADOUT_L4	V1	HT_CPU_NB_CAD_L4	12
12 HT_NB_CPU_CAD_H5	L2	L0_CADIN_H5	L0_CADOUT_H5	U1	HT_CPU_NB_CAD_H5	12
12 HT_NB_CPU_CAD_L5	L1	L0_CADIN_L5	L0_CADOUT_L5	U2	HT_CPU_NB_CAD_L5	12
12 HT_NB_CPU_CAD_H6	M1	L0_CADIN_H6	L0_CADOUT_H6	U3	HT_CPU_NB_CAD_H6	12
12 HT_NB_CPU_CAD_L6	N2	L0_CADIN_L6	L0_CADOUT_L6	T1	HT_CPU_NB_CAD_L6	12
12 HT_NB_CPU_CAD_H7	N1	L0_CADIN_H7	L0_CADOUT_H7	R1	HT_CPU_NB_CAD_H7	12
12 HT_NB_CPU_CAD_L7	E5	L0_CADIN_L7	L0_CADOUT_L7	AD4	HT_CPU_NB_CAD_L7	12
12 HT_NB_CPU_CAD_H8	F5	L0_CADIN_H8	L0_CADOUT_H8	AD3	HT_CPU_NB_CAD_H8	12
12 HT_NB_CPU_CAD_L8	F3	L0_CADIN_L8	L0_CADOUT_L8	AD5	HT_CPU_NB_CAD_L8	12
12 HT_NB_CPU_CAD_H9	F4	L0_CADIN_H9	L0_CADOUT_H9	AC5	HT_CPU_NB_CAD_H9	12
12 HT_NB_CPU_CAD_L9	G5	L0_CADIN_L9	L0_CADOUT_L9	AB4	HT_CPU_NB_CAD_L9	12
12 HT_NB_CPU_CAD_H10	H5	L0_CADIN_H10	L0_CADOUT_H10	AB3	HT_CPU_NB_CAD_H10	12
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12 HT_NB_CPU_CAD_L11	K3	L0_CADIN_L11	L0_CADOUT_L11	Y5	HT_CPU_NB_CAD_L11	12
12 HT_NB_CPU_CAD_H12	K4	L0_CADIN_H12	L0_CADOUT_H12	W5	HT_CPU_NB_CAD_H12	12
12 HT_NB_CPU_CAD_L12	L5	L0_CADIN_L12	L0_CADOUT_L12	V4	HT_CPU_NB_CAD_L12	12
12 HT_NB_CPU_CAD_H13	M5	L0_CADIN_H13	L0_CADOUT_H13	V3	HT_CPU_NB_CAD_H13	12
12 HT_NB_CPU_CAD_L13	M3	L0_CADIN_L13	L0_CADOUT_L13	V5	HT_CPU_NB_CAD_L13	12
12 HT_NB_CPU_CAD_H14	M4	L0_CADIN_H14	L0_CADOUT_H14	U5	HT_CPU_NB_CAD_H14	12
12 HT_NB_CPU_CAD_L14	N5	L0_CADIN_L14	L0_CADOUT_L14	T4	HT_CPU_NB_CAD_L14	12
12 HT_NB_CPU_CAD_H15	P5	L0_CADIN_H15	L0_CADOUT_H15	T3	HT_CPU_NB_CAD_H15	12
12 HT_NB_CPU_CAD_L15		L0_CADIN_L15	L0_CADOUT_L15		HT_CPU_NB_CAD_L15	12
12 HT_NB_CPU_CLK_H0	J3	L0_CLKIN_H0	L0_CLKOUT_H0	Y1	HT_CPU_NB_CLK_H0	12
12 HT_NB_CPU_CLK_L0	J2	L0_CLKIN_L0	L0_CLKOUT_L0	W1	HT_CPU_NB_CLK_L0	12
12 HT_NB_CPU_CLK_H1	J5	L0_CLKIN_H1	L0_CLKOUT_H1	Y4	HT_CPU_NB_CLK_H1	12
12 HT_NB_CPU_CLK_L1	K5	L0_CLKIN_L1	L0_CLKOUT_L1	Y3	HT_CPU_NB_CLK_L1	12
12 HT_NB_CPU_CTL_H0	N1	L0_CTLIN_H0	L0_CTLOUT_H0	R2	HT_CPU_NB_CTL_H0	12
12 HT_NB_CPU_CTL_L0	P1	L0_CTLIN_L0	L0_CTLOUT_L0	R3	HT_CPU_NB_CTL_L0	12
12 HT_NB_CPU_CTL_H1	P3	L0_CTLIN_H1	L0_CTLOUT_H1	T5	HT_CPU_NB_CTL_H1	12
12 HT_NB_CPU_CTL_L1	P4	L0_CTLIN_L1	L0_CTLOUT_L1	R5	HT_CPU_NB_CTL_L1	12

SKT-BGA638H176

1'nd 62.10055.111
2'nd 62.10055.181

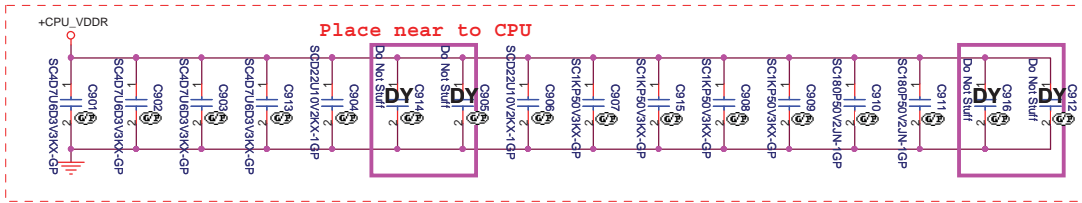
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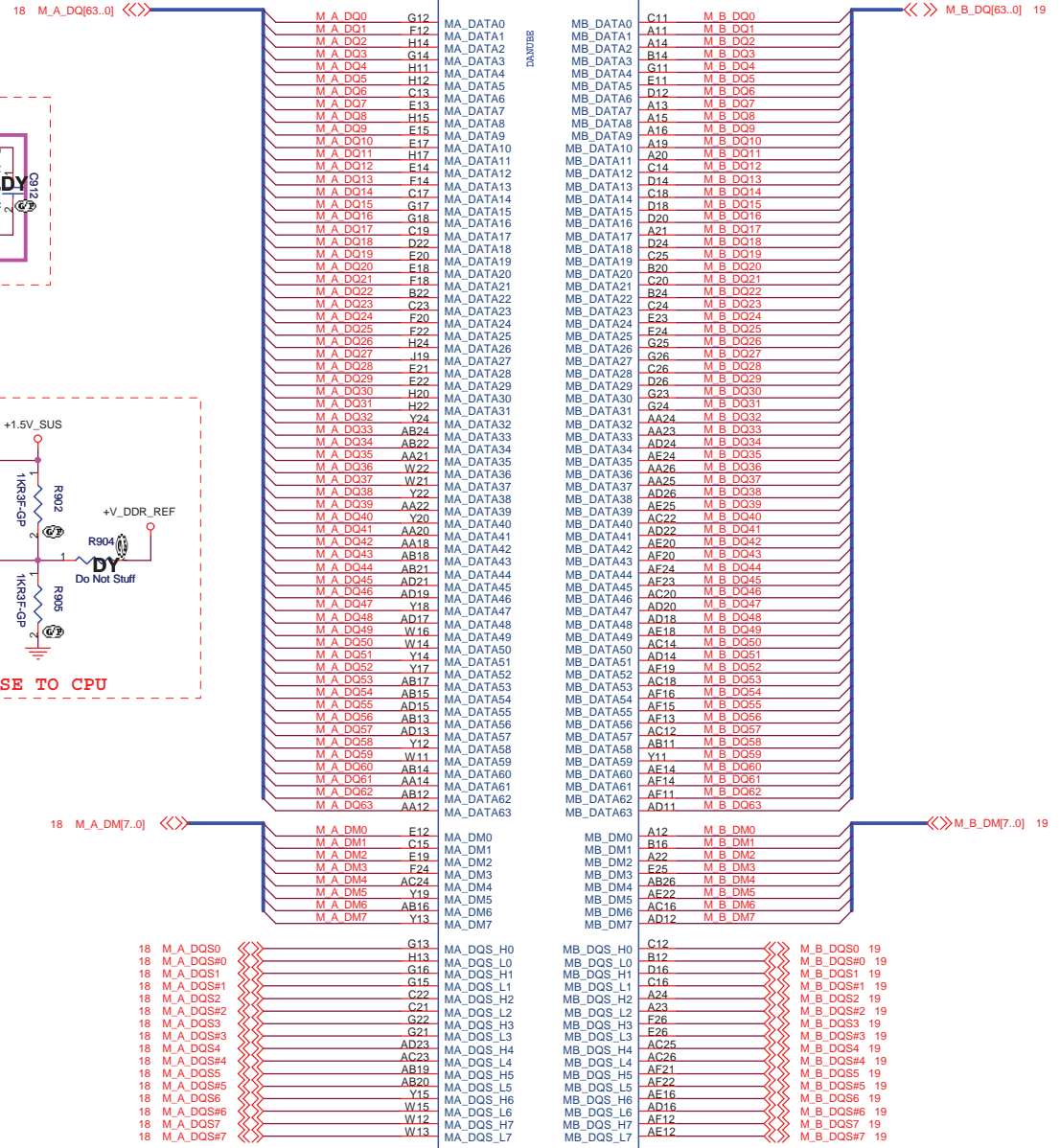
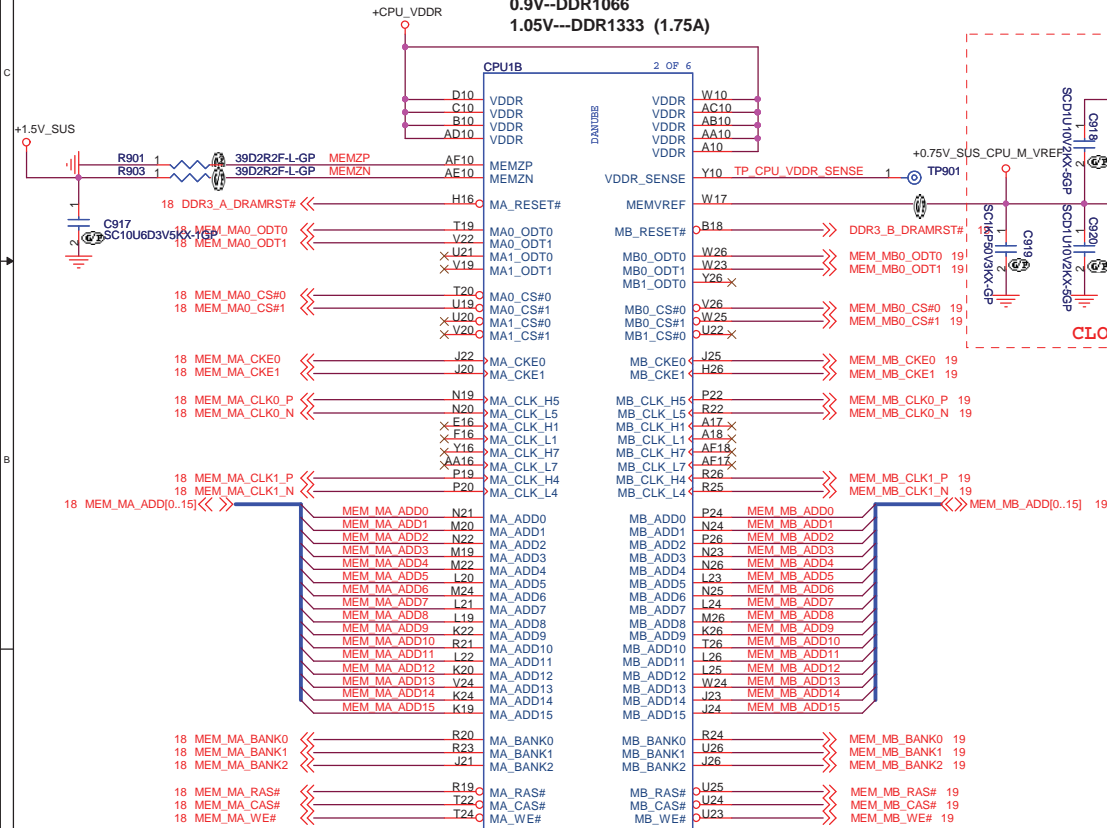
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Size	Document Number	Rev	
Custom	Chelsea DJ2 AMD UMA		X01
Date:	Tuesday, April 13, 2010	Sheet	8 of 90

SSID = CPU

4.70UF*4
0.22UF*4
1000PF*4
180PF*4



0.9V(1.25A) for VDDR
1.05V---DDR1066
1.05V---DDR1333 (1.75A)



DANUB
3 DJ2 AMD UMA (10 100 w HDM)

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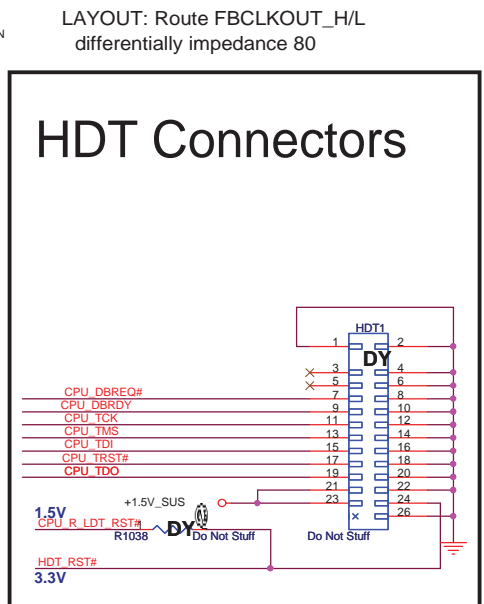
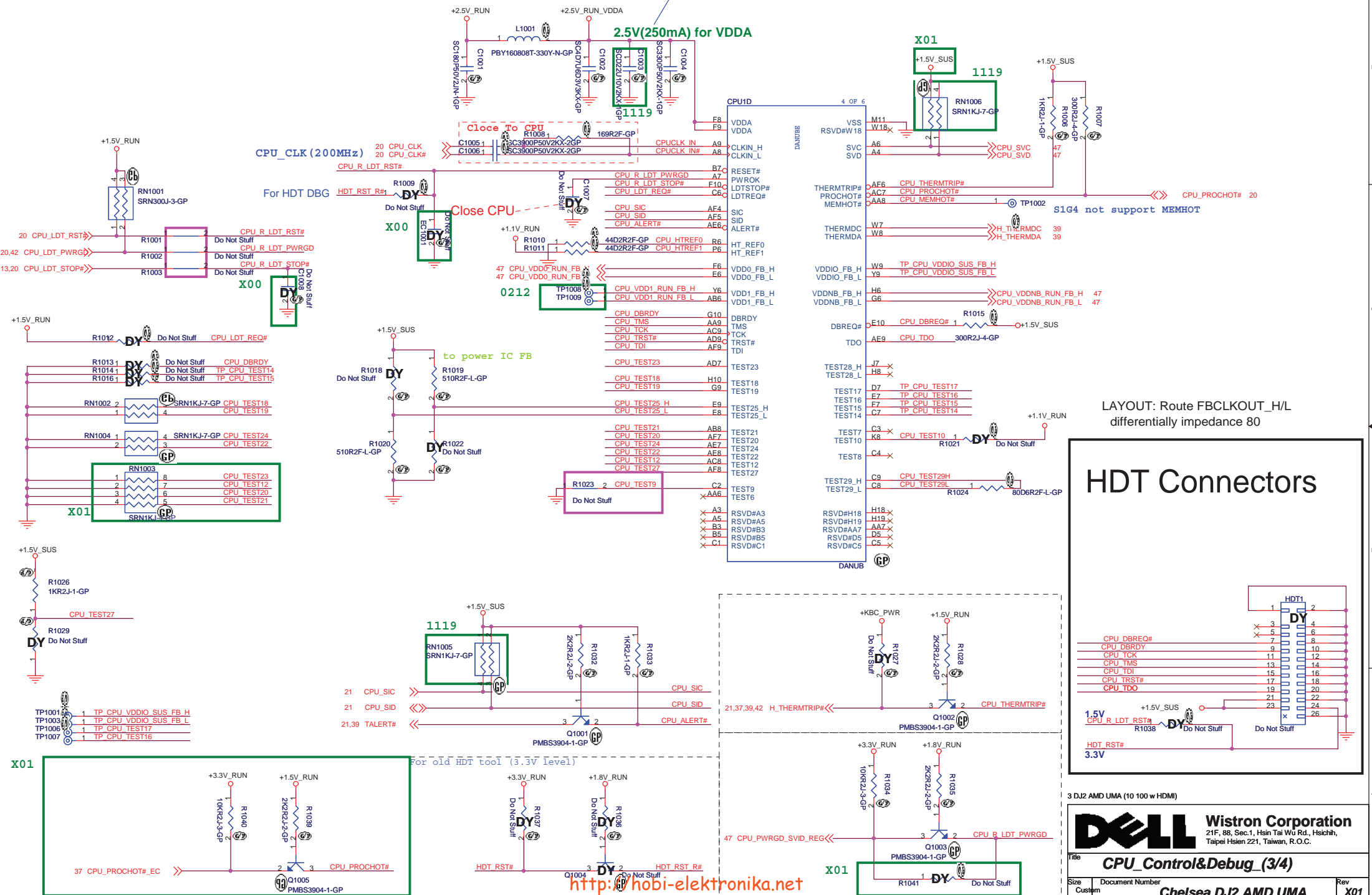
File: **CPU DDR(2/4)**

Size	Document Number	Rev
Custom	Chelsea DJ2 AMD UMA	X01

Date: Tuesday, April 13, 2010 Sheet 9 of 90

SSID = CPU

LAYOUT: ROUTE VDDA TRACE APPROX.
50mils WIDE (USE 2X25 mil TRACES TO
EXIT BALL FIELD) AND 500 mils LONG.



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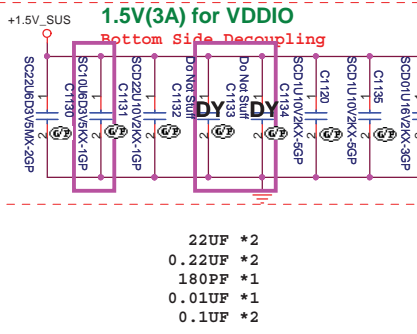
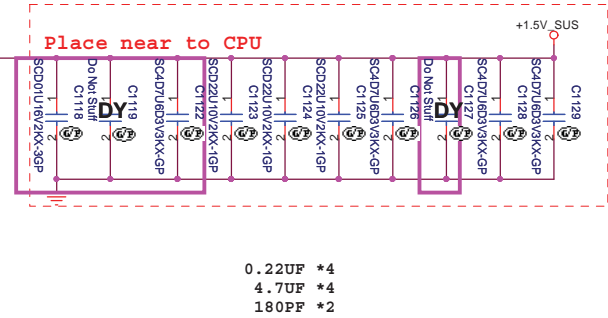
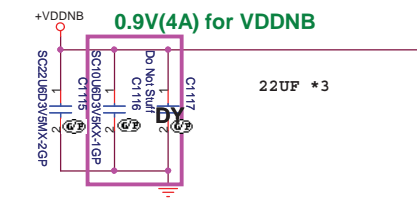
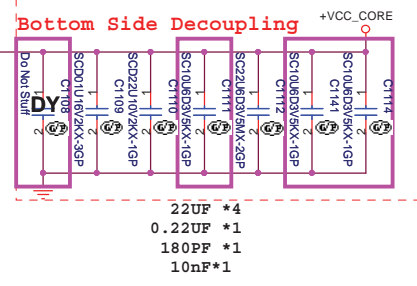
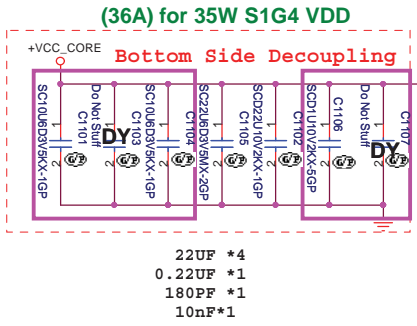
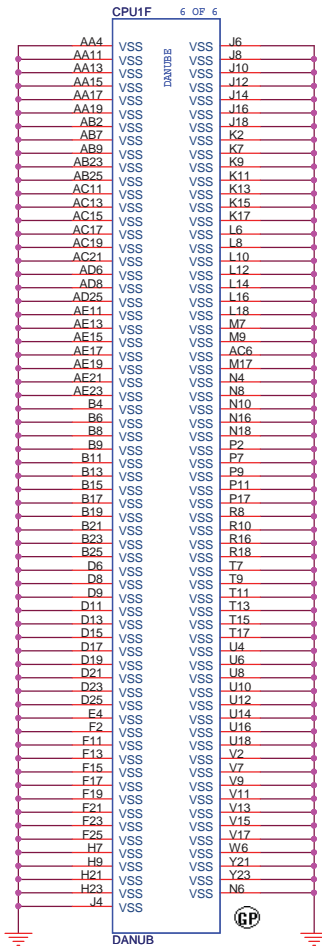
Title: **CPU_Control&Debug (3/4)**

Size: Custom	Document Number: Chelsea DJ2 AMD UMA	Rev: X01
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SSID = CPU



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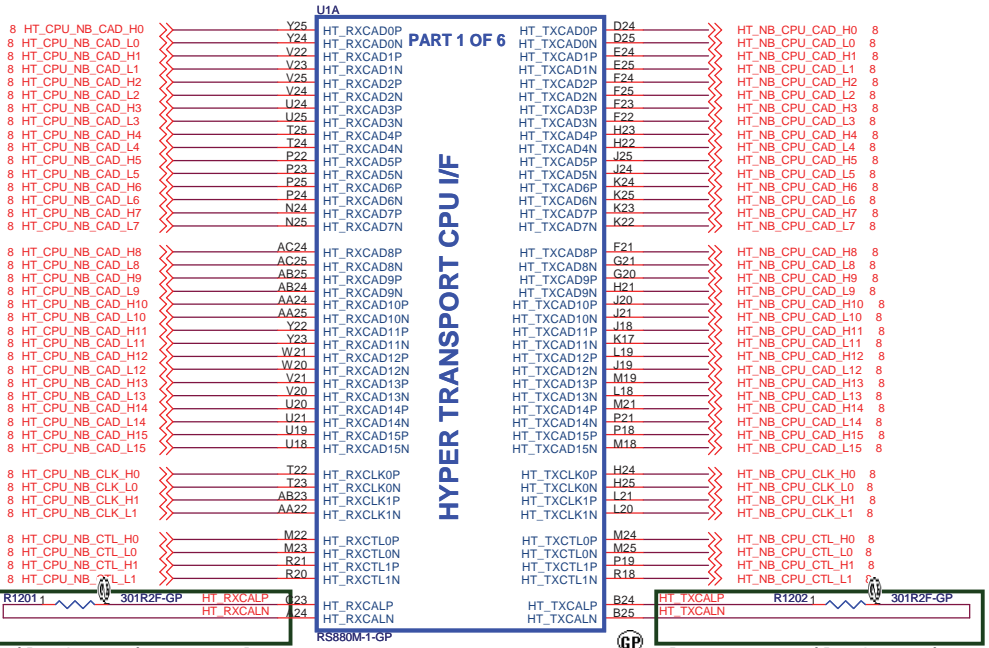
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Size A3	Document Number Chelsea DJ2 AMD UMA	Rev X01
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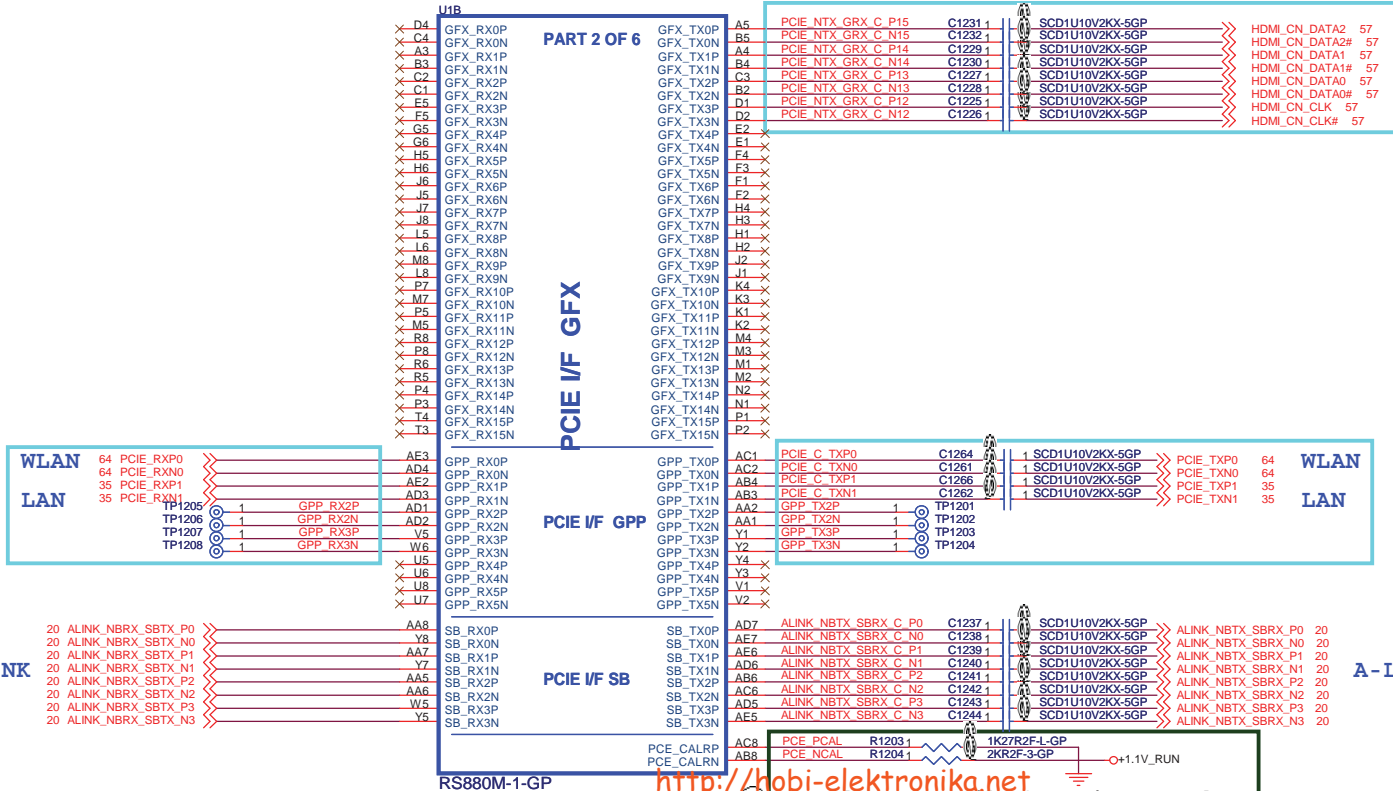
SSID = N.B

RS880M : 71.RS880.M05



Place < 1000mils from pin C23 and A24

Place < 1000mils from pin B25 and B24



Place < 100mils from pin AC8 and AB8

HDMI

A-LINK

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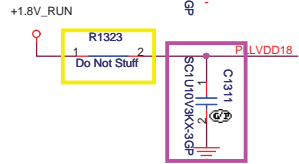


Title		AMD-RS880M HT LINK&PCIe(1/4)	
Size	Document Number	Rev	
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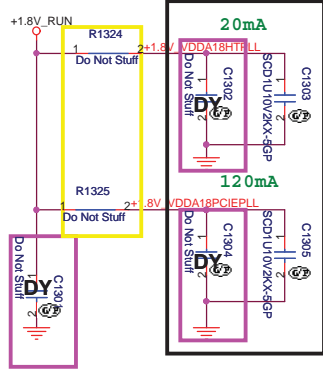
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SSID = N.B

RS880M : 71.RS880.M05

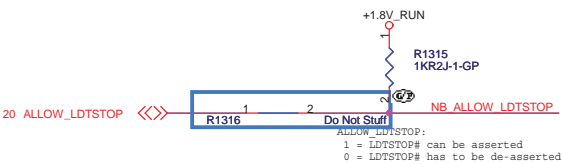
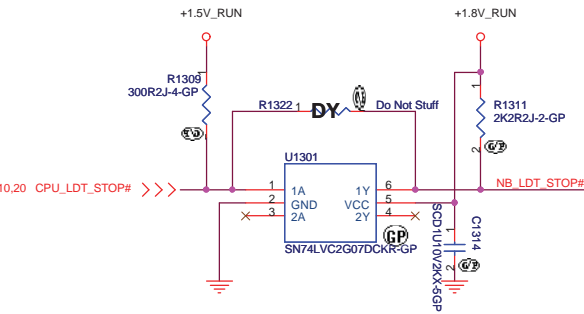


Layout Note
Trace at least 15 mil

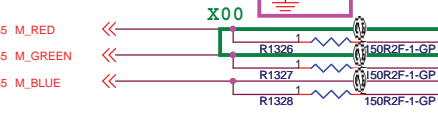
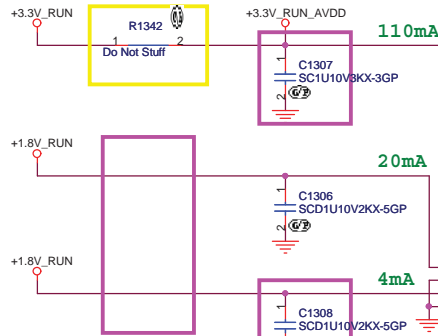


20mA

120mA

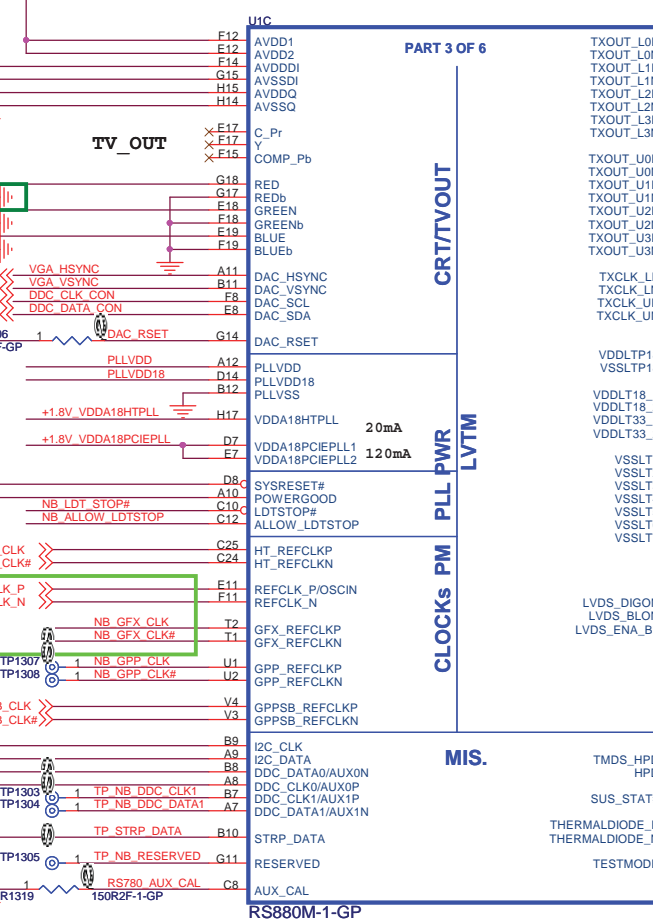
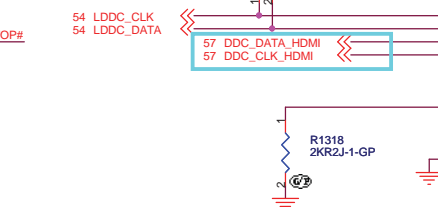
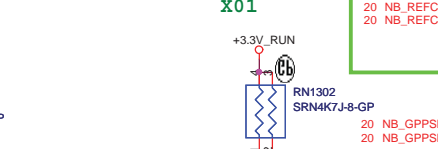
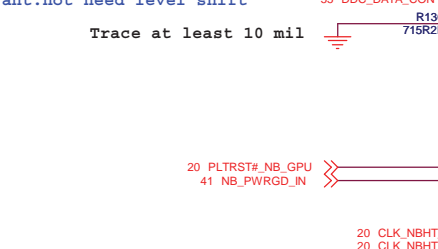


ALLOW_LDTSTOP:
1 = LDTSTOP# can be asserted
0 = LDTSTOP# has to be de-asserted



UMA: DAC_CLK and DATA with 5V-tolerant, not need level shift

Trace at least 10 mil

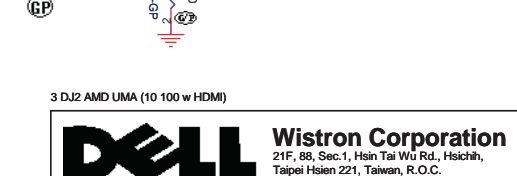
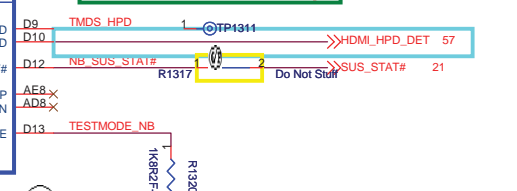
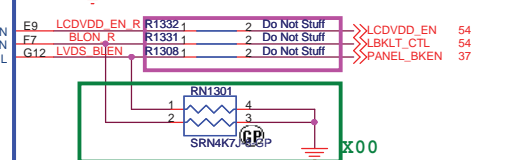
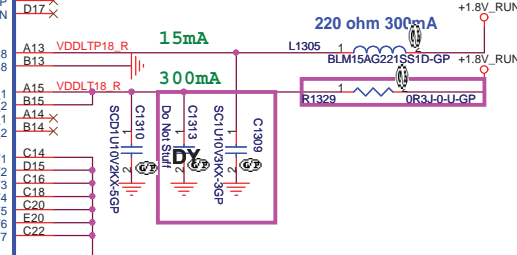


STRAP_DEBUG_BUS_GPIO_ENABLE# (RS880M use VGA_VSYNC)
Enables debug bus access through memory I/O pads and GPIOs.
*1 : Disable
0 : Enable

SIDE_PORT_EN# (RS880M use VGA_HSYNC)
*1 = Memory Side port Not available
0 = Memory Side port available

LOAD_EEPROM_STRAPS#(RS880M use SUS_STAT#)
Selects Loading of STRAPS From EEPROM
*1 : use Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

*DEFAULT



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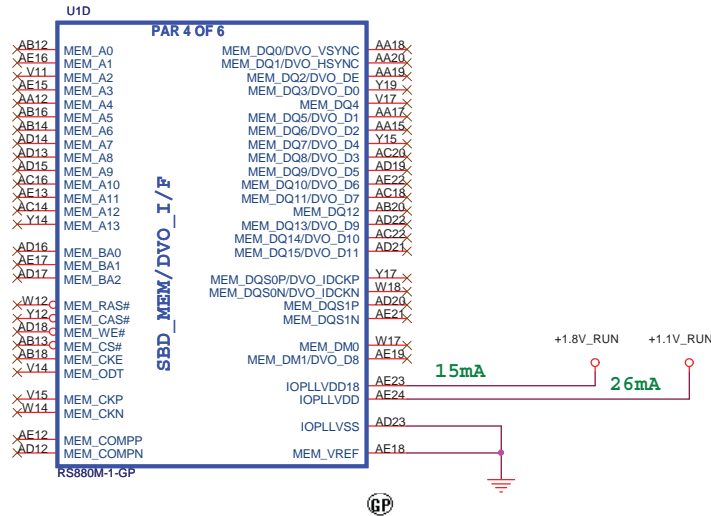
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Size	Document Number	Rev
Custom	Chelsea DJ2 AMD UMA	X01

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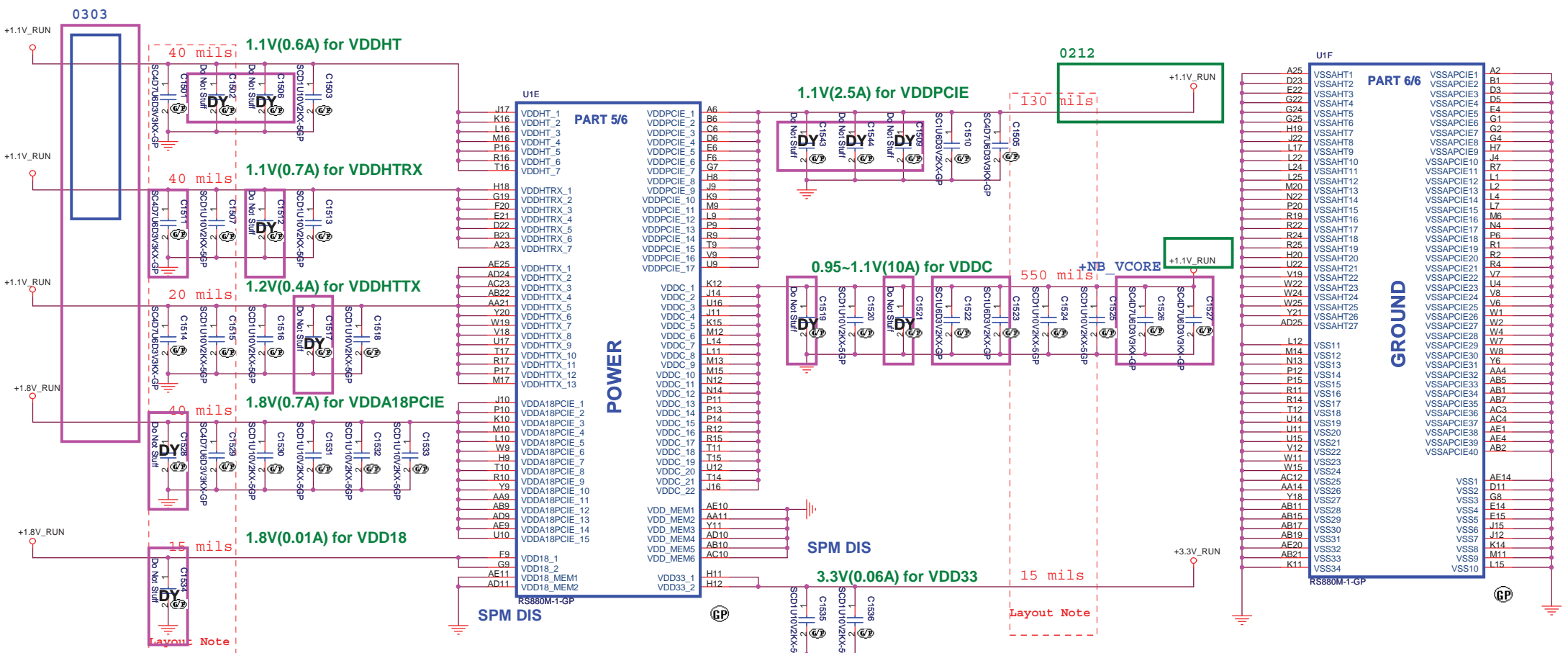
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SSID = N.B



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Title AMD-RS880M_SidePort_(3/4)			
Size A3	Document Number Chelsea DJ2 AMD UMA		Rev X01
Date: Tuesday, April 13, 2010	Sheet 14		of 90

SSID = N.B



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3 DJ2 AMD UMA (10 100 w HDMI)

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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **AMD-RS880M_PWR&GD_(4/4)**

Size: A3 Document Number: **Chelsea DJ2 AMD UMA** Rev: **X01**

Date: Tuesday, April 13, 2010 Sheet 15 of 90

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3 DJ2 AMD UMA (10 100 w HDMI)



Title		
Reserved		
Size	Document Number	Rev
A3	Chelsea DJ2 AMD UMA	X01
Date:	Tuesday, April 13, 2010	Sheet 16 of 90

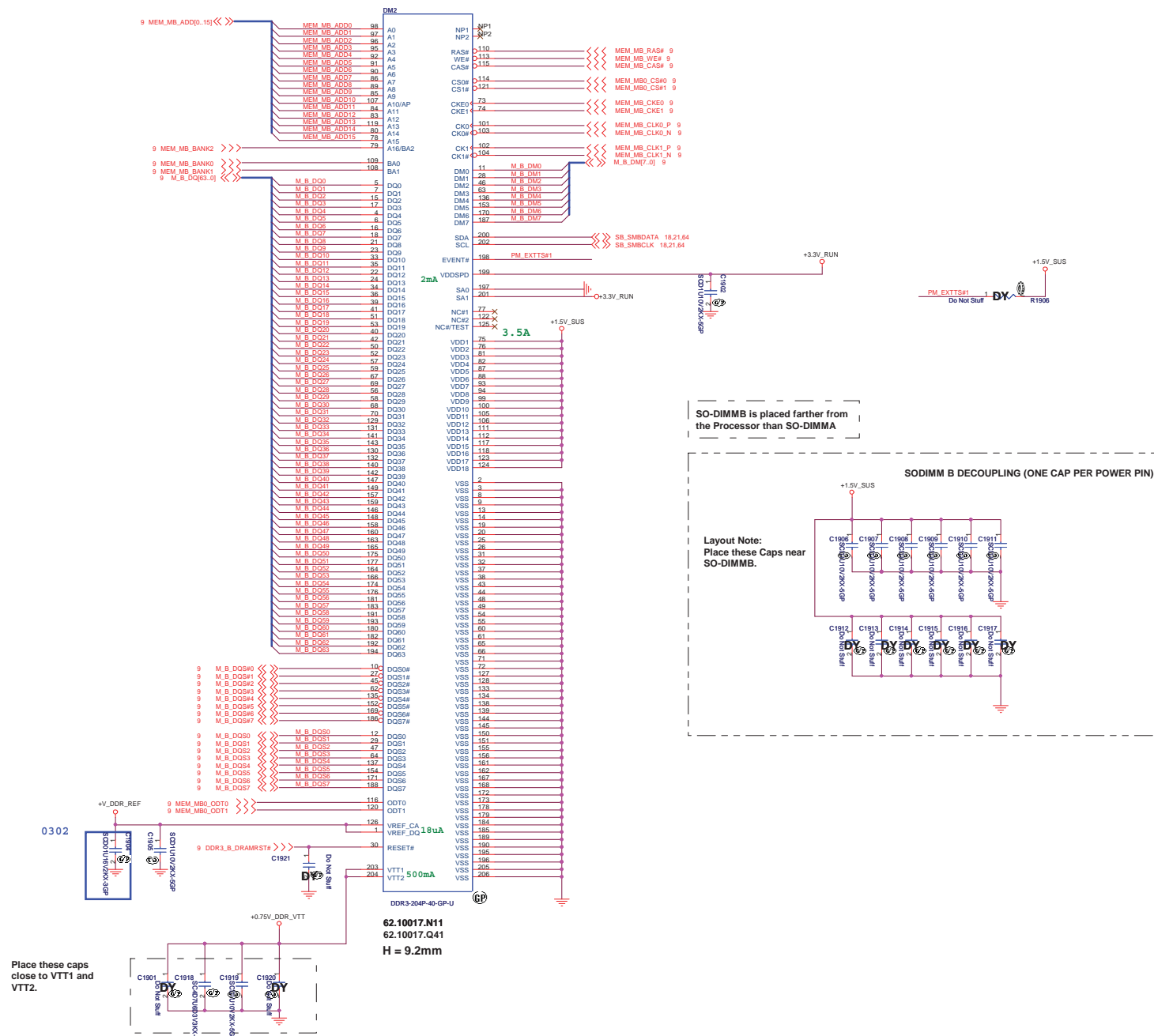
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<http://hobi-elektronika.net>

3 DJ2 AMD UMA (10 100 w HDMI)



Title		
Reserved		
Size A3	Document Number Chelsea DJ2 AMD UMA	Rev X01
Date: Tuesday, April 13, 2010	Sheet 17 of 90	



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3 DJ2 AMD UMA (10 100 w HDMI)

DELL Wistron Corporation
21F, 8th, Sec. 1, Hsin Tai Wu Rd., Hsichia, Taipei Hsien 221, Taiwan, R.O.C.

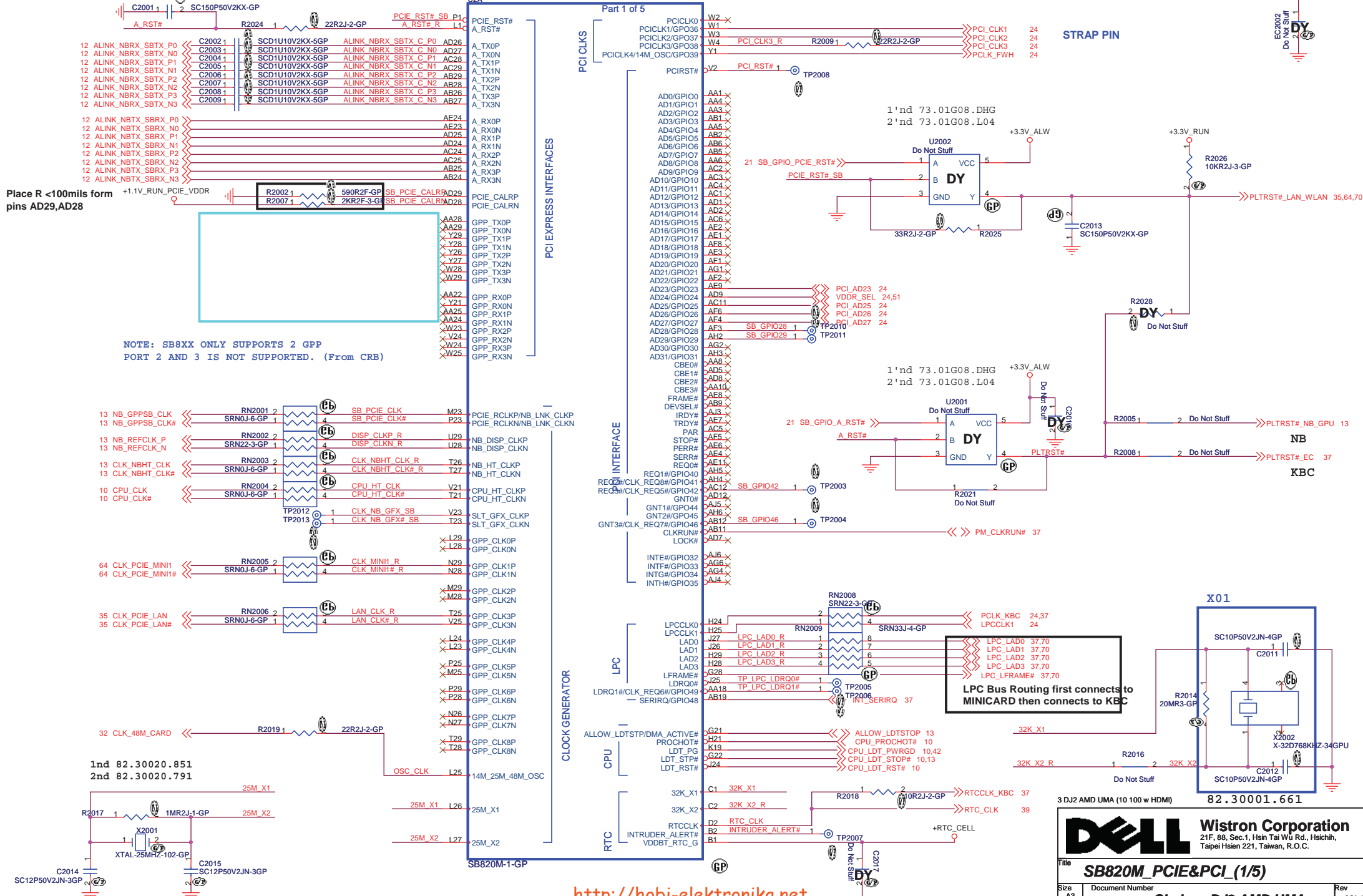
Title: **DDR3-SODIMM2**

Size: Document Number: **Chelsea DJ2 AMD UMA** Rev: **X01**

Date: Tuesday, April 13, 2010 Sheet: 19 of 90

SSID = S.B

SB700 A12 : 71.SB820M02



Place R <100mils form pins AD29,AD28

NOTE: SB8XX ONLY SUPPORTS 2 GPP PORT 2 AND 3 IS NOT SUPPORTED. (From CRB)

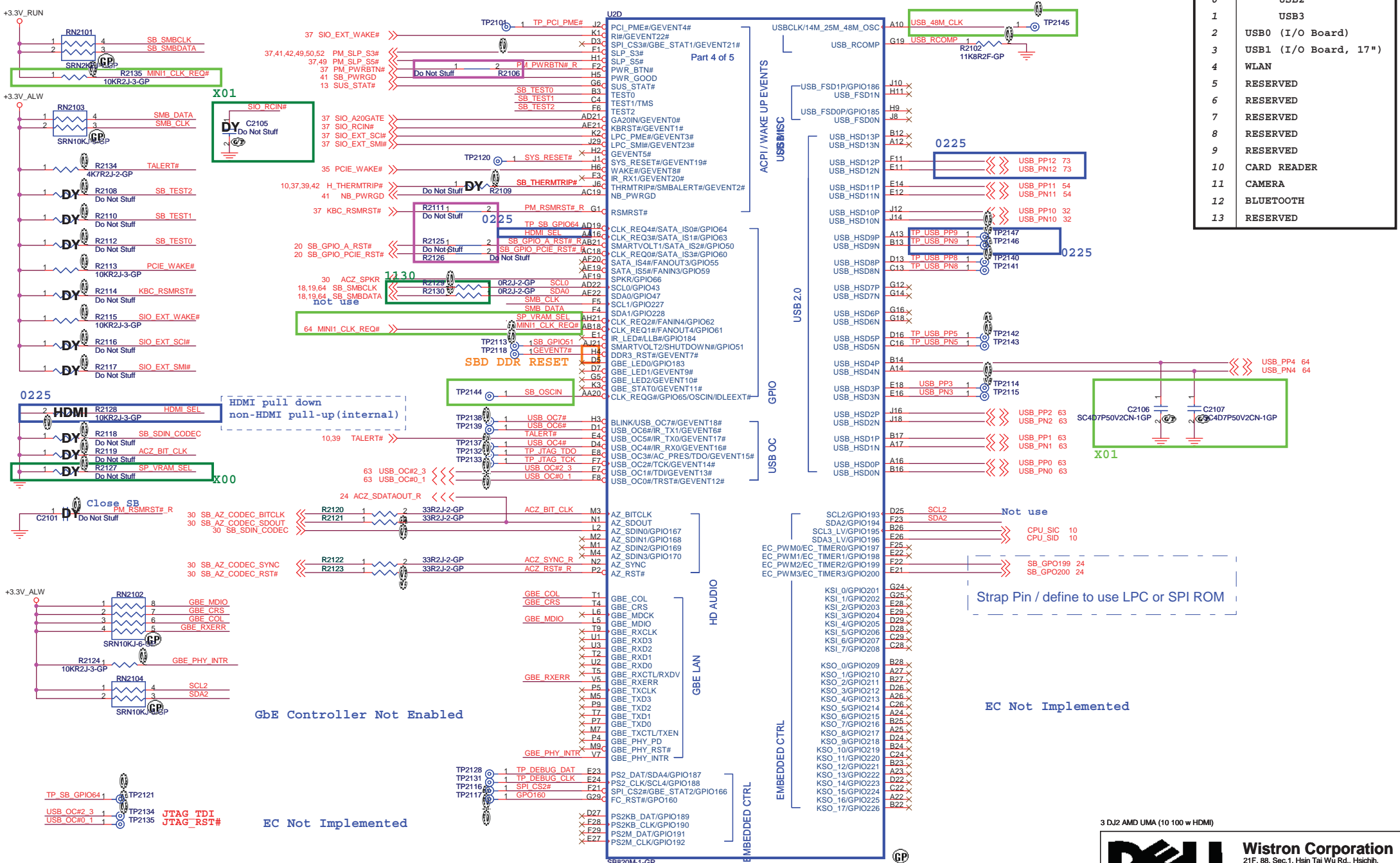
LPC Bus Routing first connects to MINICARD then connects to KBC

http://hobi-elektronika.net



SSID = S.B

USB	
Pair	Device
0	USB2
1	USB3
2	USB0 (I/O Board)
3	USB1 (I/O Board, 17")
4	WLAN
5	RESERVED
6	RESERVED
7	RESERVED
8	RESERVED
9	RESERVED
10	CARD READER
11	CAMERA
12	BLUETOOTH
13	RESERVED



3 DJ2 AMD UMA (10 100 w HDMI)



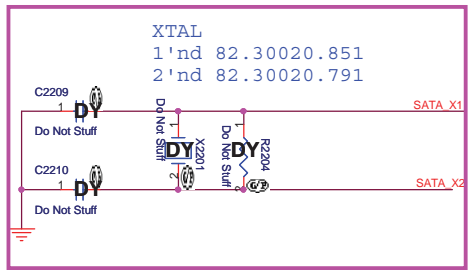
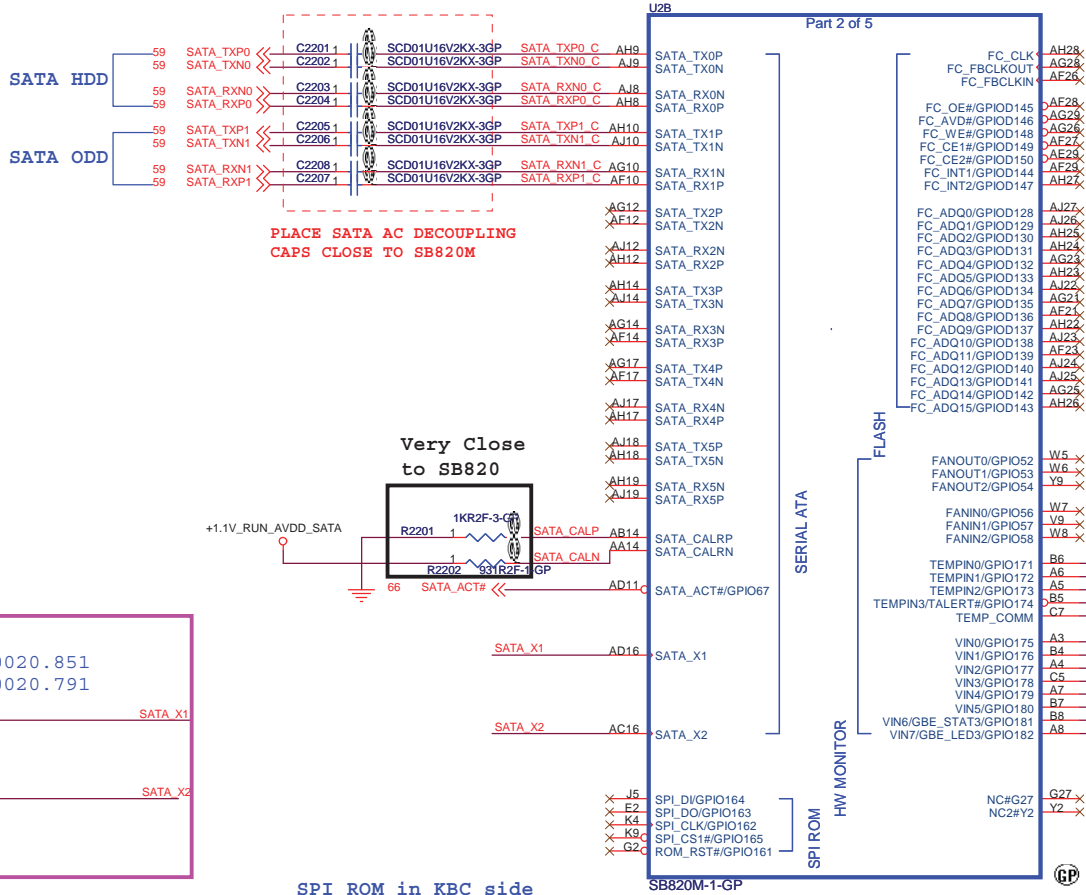
Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsihnh,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **SB820M_USB&GPIO (2/5)**

Size Custom	Document Number	Rev
	Chelsea DJ2 AMD UMA	X01

Date: Wednesday, April 14, 2010 Sheet 21 of 90

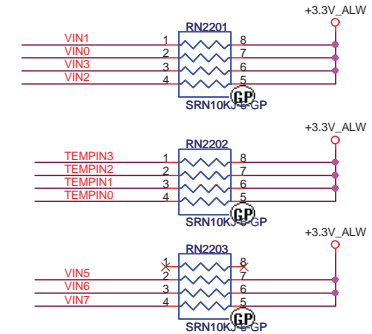
<http://hobi-elektronika.net>



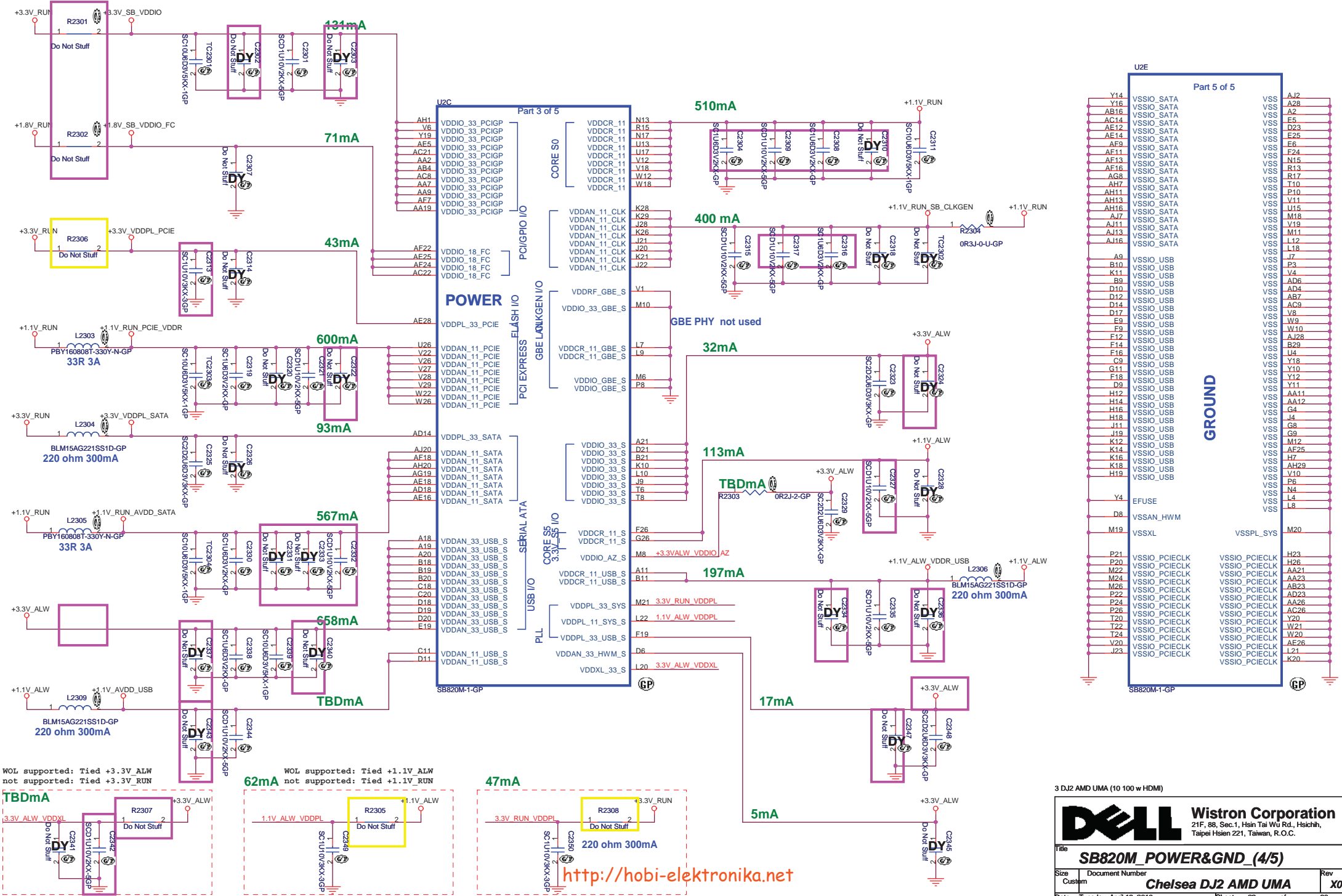
GPIOD[150:128] are open drain GPIO pins where as GPO160 is an open drain GPO pin. These pins are not programmed to GPIO mode by default.

If use as GPIO, need to pull up to 1.8V_RUN

suggest not use HW monitor



SSID = S.B



WOL supported: Tied +3.3V_ALW
not supported: Tied +3.3V_RUN

WOL supported: Tied +1.1V_ALW
not supported: Tied +1.1V_RUN

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3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

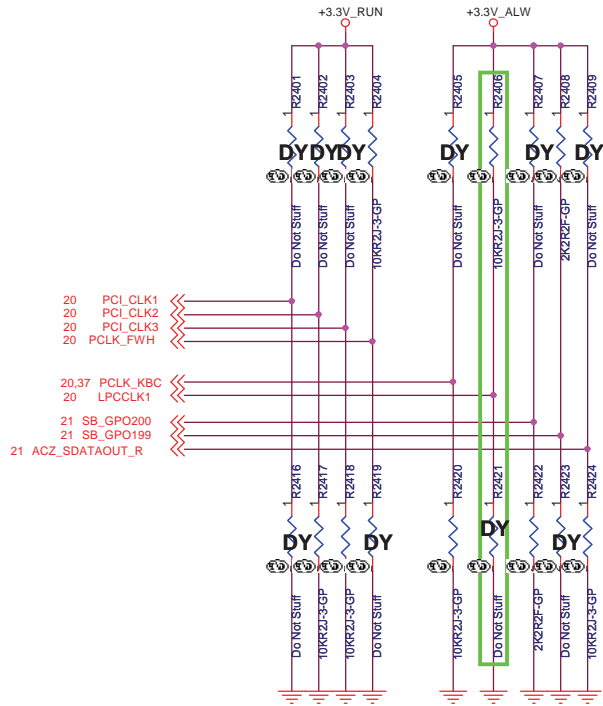
Title: **SB820M_POWER&GND_(4/5)**

Size	Document Number	Rev
Custom	Chelsea DJ2 AMD UMA	X01

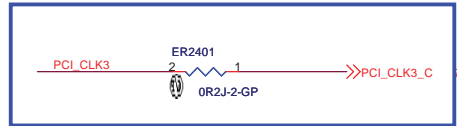
Date: Tuesday, April 13, 2010 Sheet 23 of 90

SSID = S.B

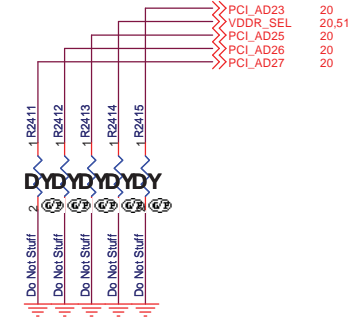
REQUIRED STRAPS



0309



DEBUG STRAPS



REQUIRED SYSTEM STRAPS

USE this pin to determine INT/EXT CLK

	AZ_SDOUT#	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCLK_FWH (PCI_CLK4)	PCLK_KBC (LPCCLK0)	LPCCLK1	SB_GPO200 , SB_GPO199 ROM TYPE:
PULL HIGH	LOW POWER MODE	Allow PCIE GEN2 DEFAULT	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	non_Fusion CLOCK mode DEFAULT	ENABLE EC	DEFAULT CLKGEN ENABLED (Use Internal)	H, H = Reserved H, L = SPI ROM
PULL LOW	PERFORMANCE MODE DEFAULT	Force PCIE GEN1	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External)	L, H = LPC ROM DEFAULT L, L = FWH ROM

Not Applicable to SB820M
but provision for pull-down is required.

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL (DEFAULT)	Disable ILA AUTORUN (DEFAULT)	USE FC PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Disable PCI MEM BOOT (DEFAULT)
PULL LOW	BYPASS PCI PLL	Enable ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	Enable PCI MEM BOOT

Note: SB820 has 15K internal PU FOR PCI_AD[27:23]

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3 DJ2 AMD UMA (10 100 w HDMI)

DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **SB820M_STRAPPING_(5/5)**


Size A3 Document Number **Chelsea DJ2 AMD UMA** Rev **X01**

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3 DJ2 AMD UMA (10 100 w HDMI)

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
CPU (VCC CORE)		
Size	Document Number	Rev
	Chelsea DJ2 AMD UMA	X01
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3 DJ2 AMD UMA (10 100 w HDMI)

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
CPU (VCC_GFXCORE)		
Size	Document Number	Rev
	Chelsea DJ2 AMD UMA	X01
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3 DJ2 AMD UMA (10 100 w HDMI)

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		CPU (VSS)
Size	Document Number	Rev
	Chelsea DJ2 AMD UMA	X01
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3 DJ2 AMD UMA (10 100 w HDMI)




Title		
Reserved		
Size A3	Document Number Chelsea DJ2 AMD UMA	Rev X01
Date: Tuesday, April 13, 2010	Sheet 28	of 90

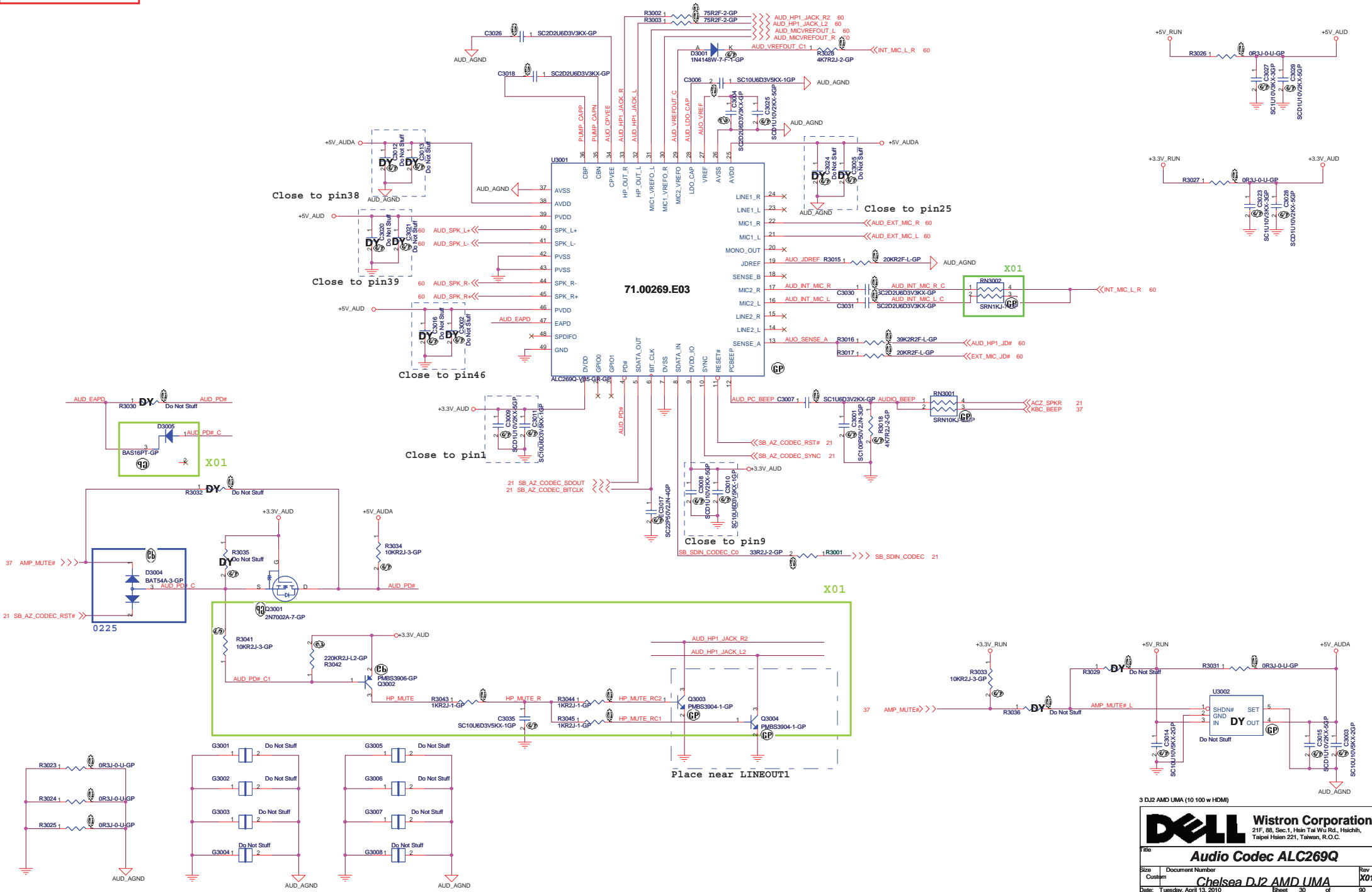
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3 DJ2 AMD UMA (10 100 w HDMI)

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
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SSID = AUDIO



3 DJ2 AMD UMA (10 100 w HDMI)



Title		Audio Codec ALC269Q	Rev	X01
Size	Document Number			
Customer	Chelsa D.J2 AMD UMA			
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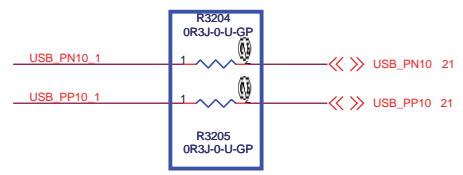
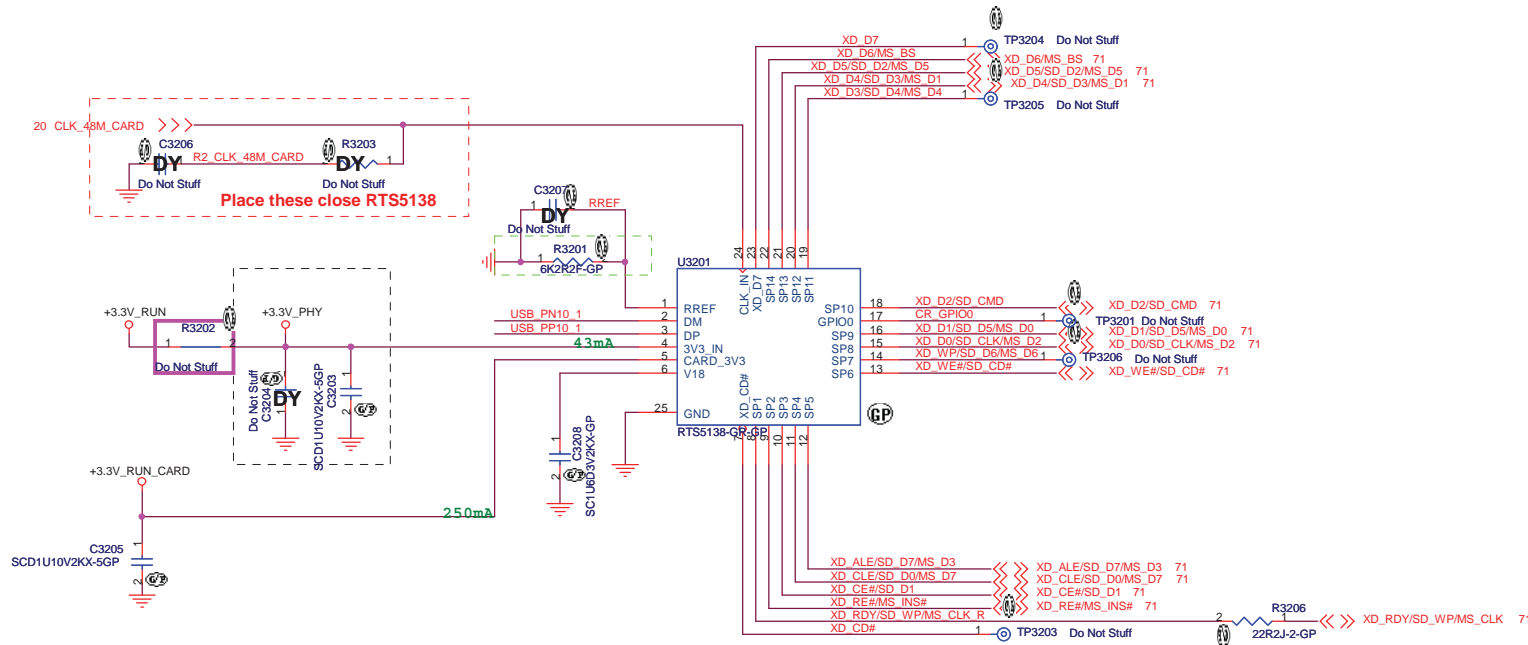
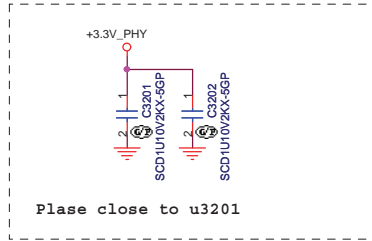
<http://hobi-elektronika.net>

3 DJ2 AMD UMA (10 100 w HDMI)



Title		
Reserved		
Size	Document Number	Rev
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SSID = SDIO



Place R3204 and R3205 together

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3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
Card Reader-RTS5138		
Size	Document Number	Rev
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3 DJ2 AMD UMA (10 100 w HDMI)




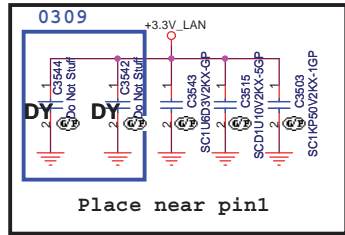
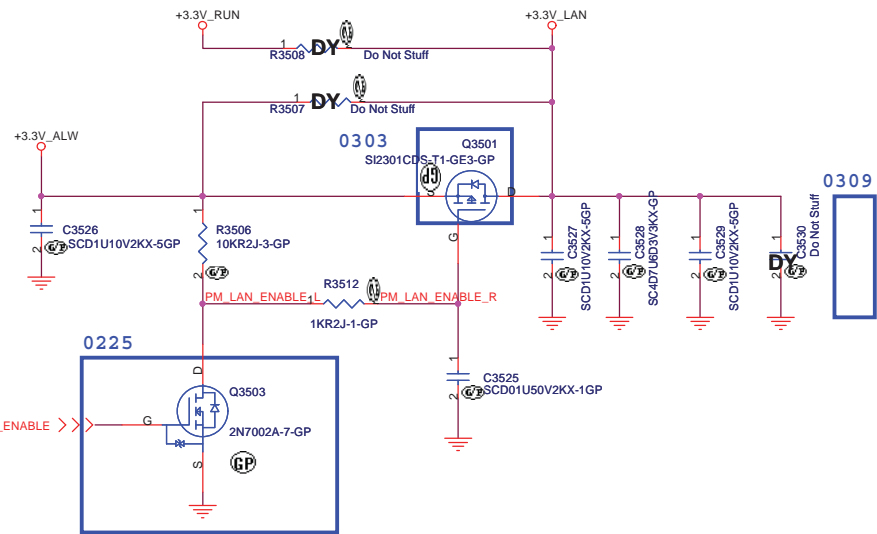
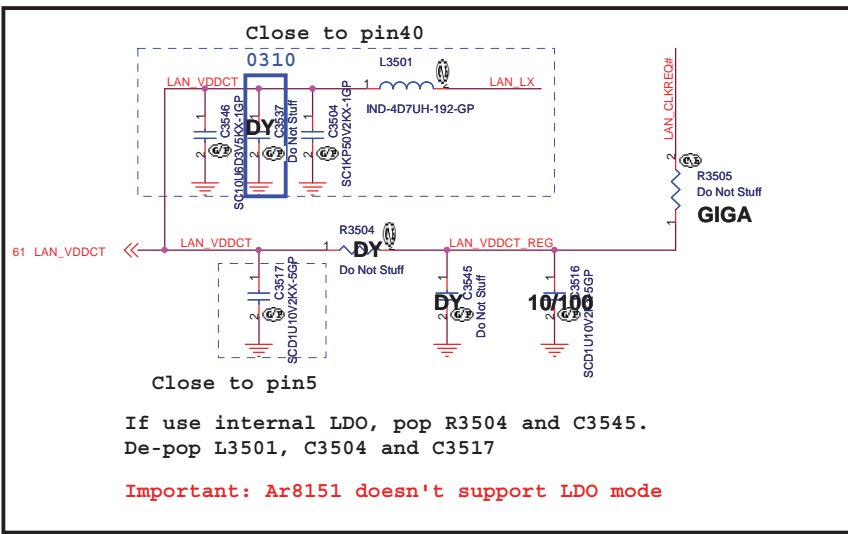
Title		
Reserved		
Size	Document Number	Rev
A3	Chelsea DJ2 AMD UMA	X01
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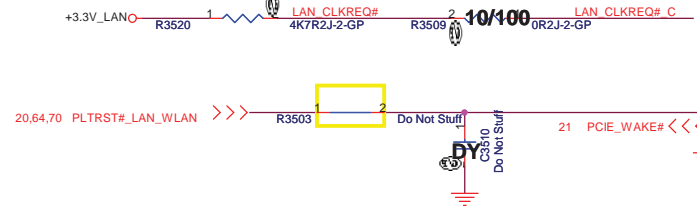
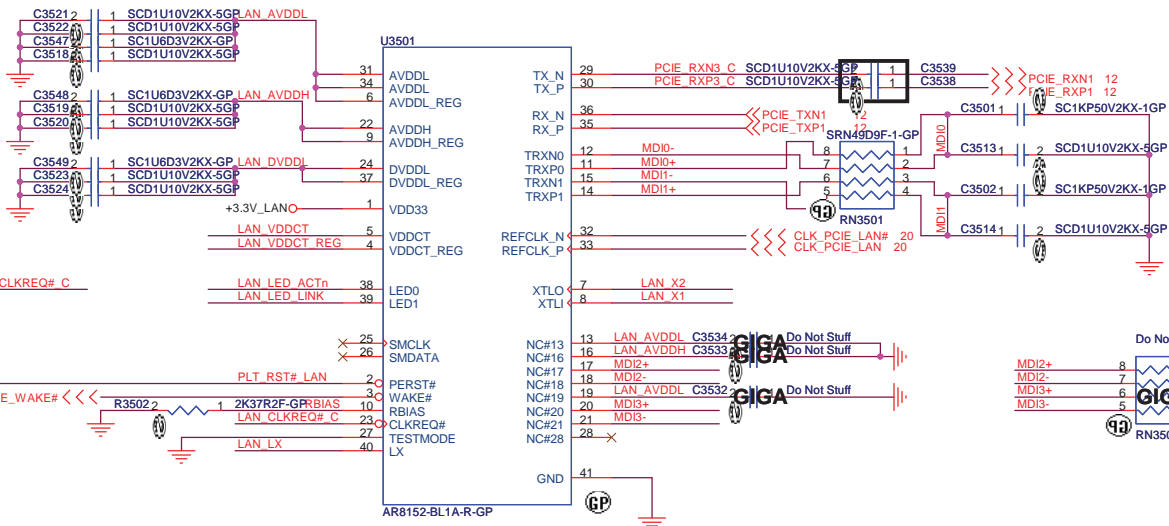
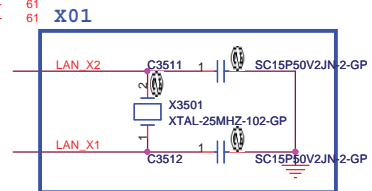
<http://hobi-elektronika.net>

3 DJ2 AMD UMA (10 100 w HDMI)

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
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A3	Chelsea DJ2 AMD UMA	X01	
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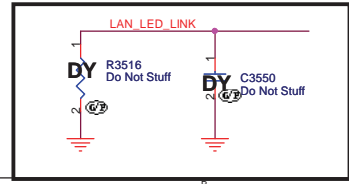
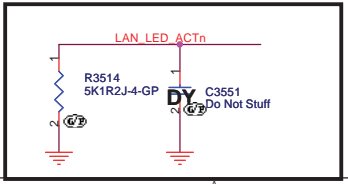


Pin6 is the AVDDL LDO output, 1uF+0.1uF (C3547 and C3518) close to Pin6; C3522, C3521 close to Pin31, Pin34 respectively.
Pin9 is the AVDDH LDO output, 1uF+0.1uF (C3548 and C3519) close to Pin9; C3520 close to Pin22.
Pin37 is the DVDDL LDO output, 1uF+0.1uF (C3549 and C3523) close to Pin37; C3524 close to Pin24.



If overclocking, de-pop R3514 and C3551

If use LDO mode, pop R3516 and C3550



GIGA LAN use 71.08151.003

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3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **AR8152/AR8151**

Size A3	Document Number	Rev
	Chelsea DJ2 AMD UMA	X01

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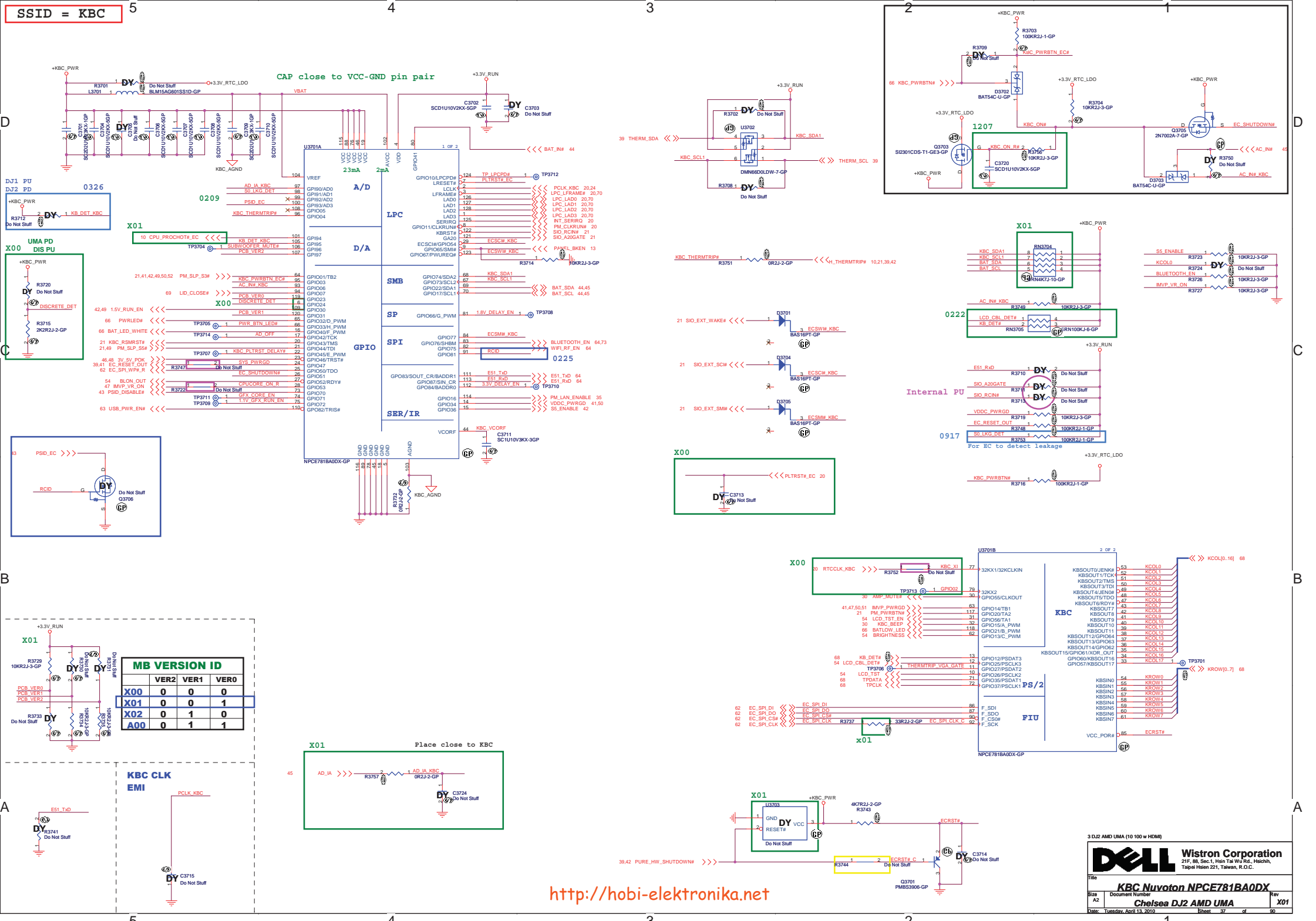
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3 DJ2 AMD UMA (10 100 w HDMI)



Title		
Reserved		
Size	Document Number	Rev
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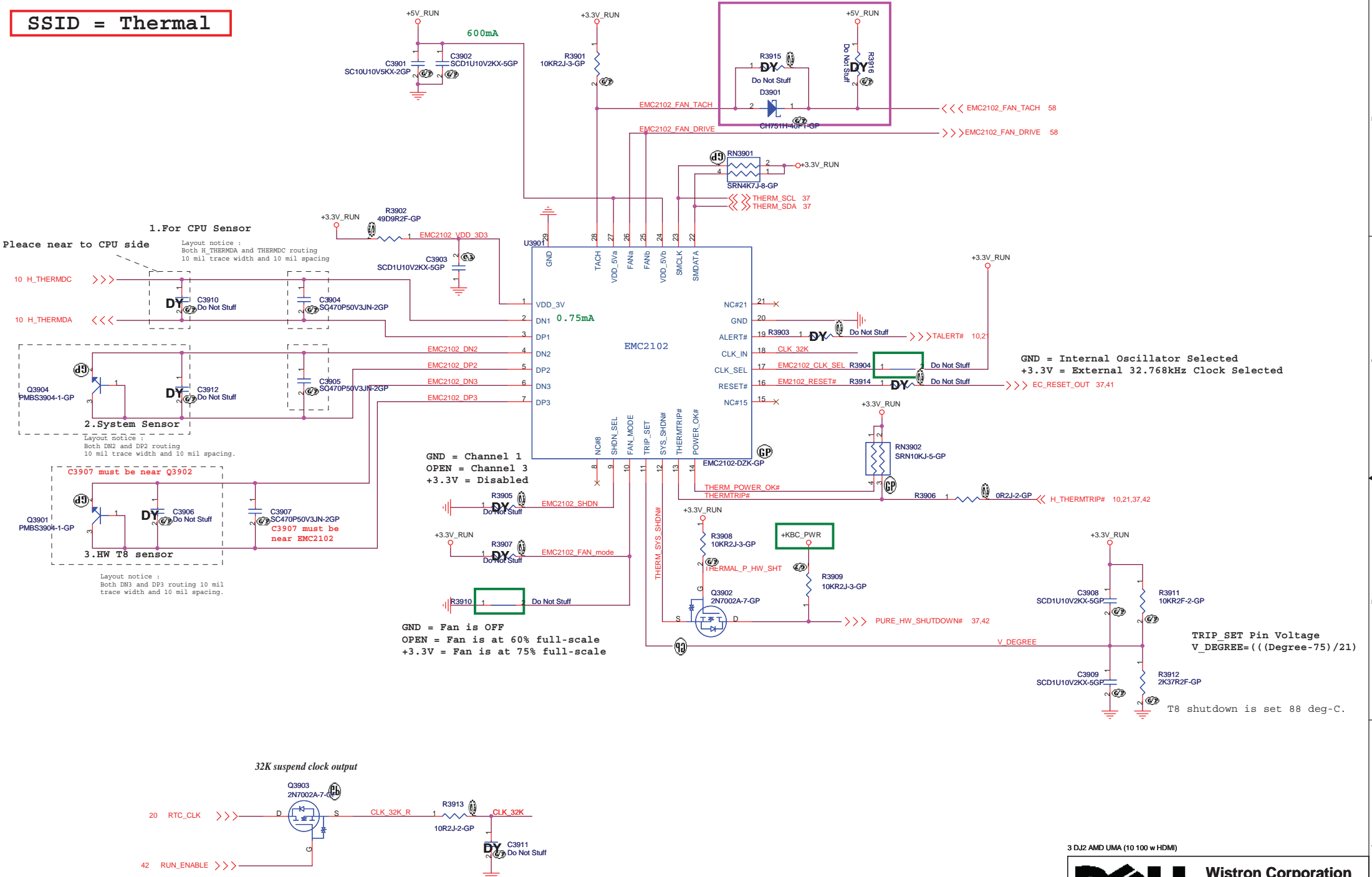
<http://hobi-elektronika.net>

3 DJ2 AMD UMA (10 100 w HDMI)



Title		
Reserved		
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SSID = Thermal



10 H_THERMDC >>>
 10 H_THERMDA <<<

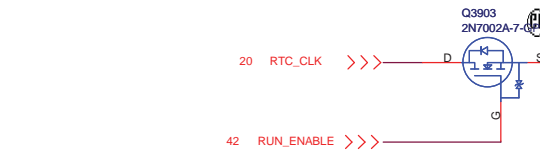
2. System Sensor
 Layout notice :
 Both DN2 and DP2 routing
 10 mil trace width and 10 mil spacing.

3. HW T8 sensor
 Layout notice :
 Both DN3 and DP3 routing 10 mil
 trace width and 10 mil spacing.

C3907 must be near Q3902

C3907 must be near EMC2102

32K suspend clock output



GND = Channel 1
 OPEN = Channel 3
 +3.3V = Disabled

R3905
 Do Not Stuff

+3.3V_RUN
 R3907
 Do Not Stuff

R3910
 Do Not Stuff

GND = Fan is OFF
 OPEN = Fan is at 60% full-scale
 +3.3V = Fan is at 75% full-scale

GND = Internal Oscillator Selected
 +3.3V = External 32.768kHz Clock Selected

TRIP_SET Pin Voltage
 $V_DEGREE = ((Degree - 75) / 21)$

T8 shutdown is set 88 deg-C.

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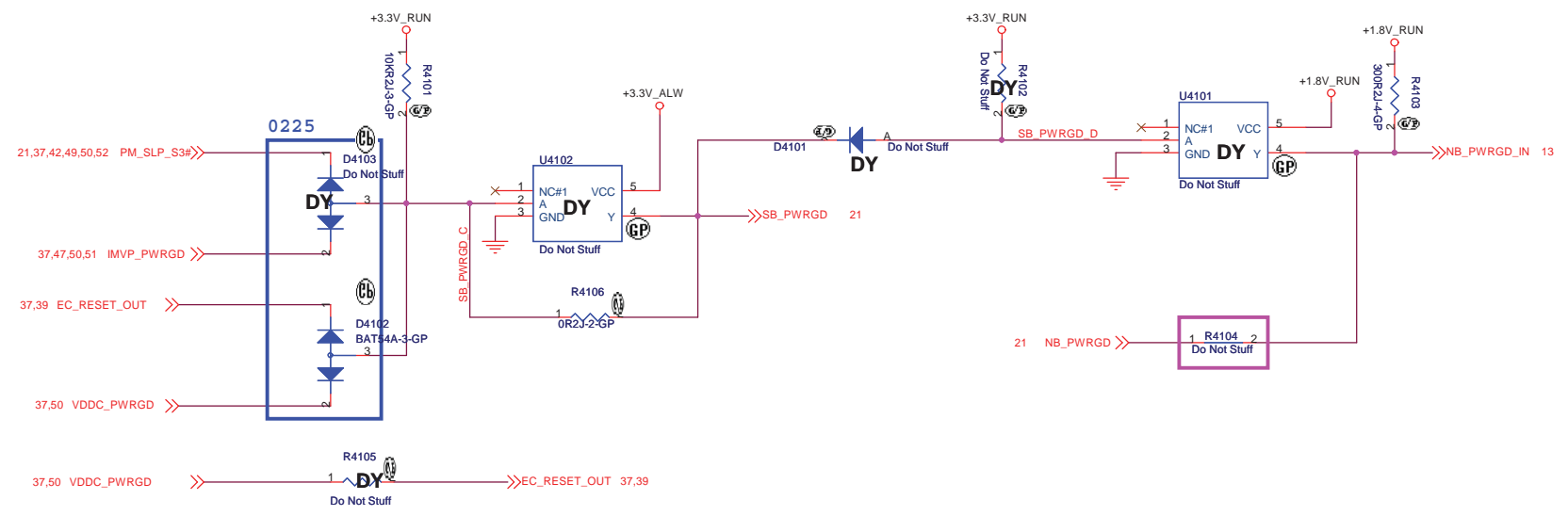
<http://hobi-elektronika.net>

3 DJ2 AMD UMA (10 100 w HDMI)



Title		
Reserved		
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SSID = Reset.Suspend



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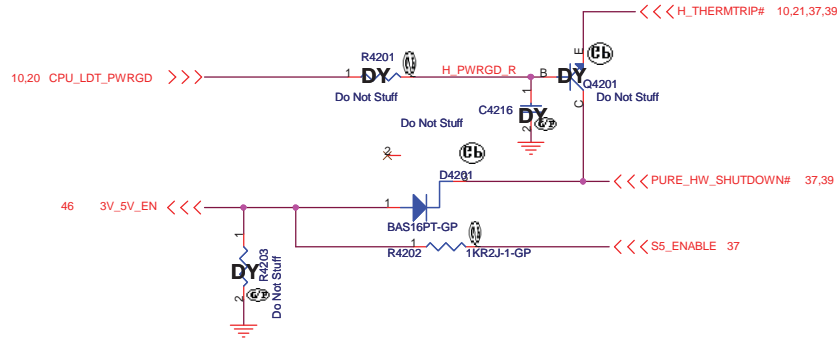
3 DJ2 AMD UMA (10 100 w HDMI)

DELL Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

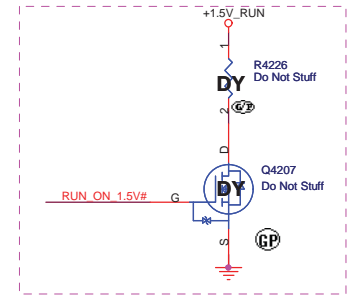
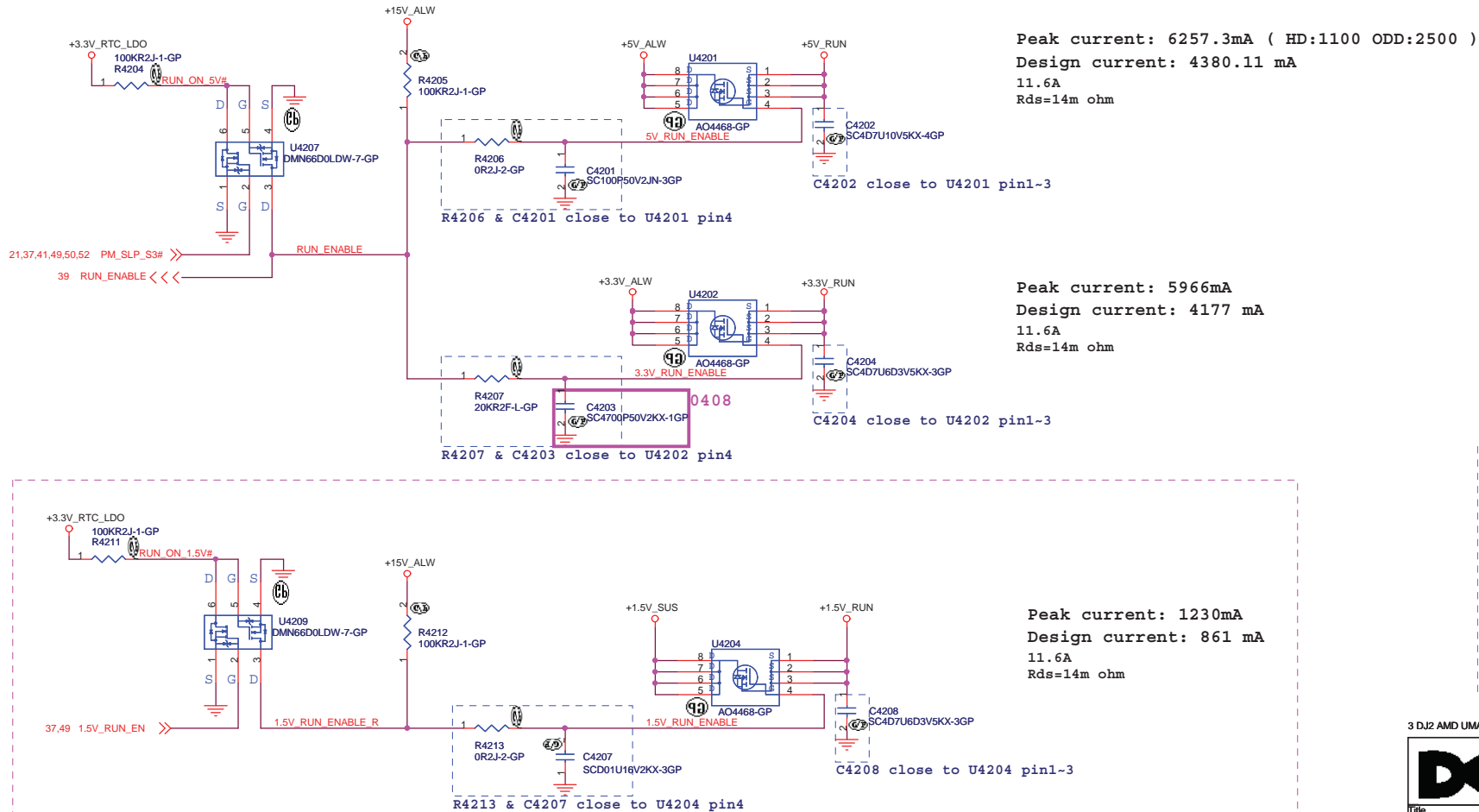
Title **Power On Logic**

Size A3	Document Number Chelsea DJ2 AMD UMA	Rev X01
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SSID = Reset.Suspend



Run Power

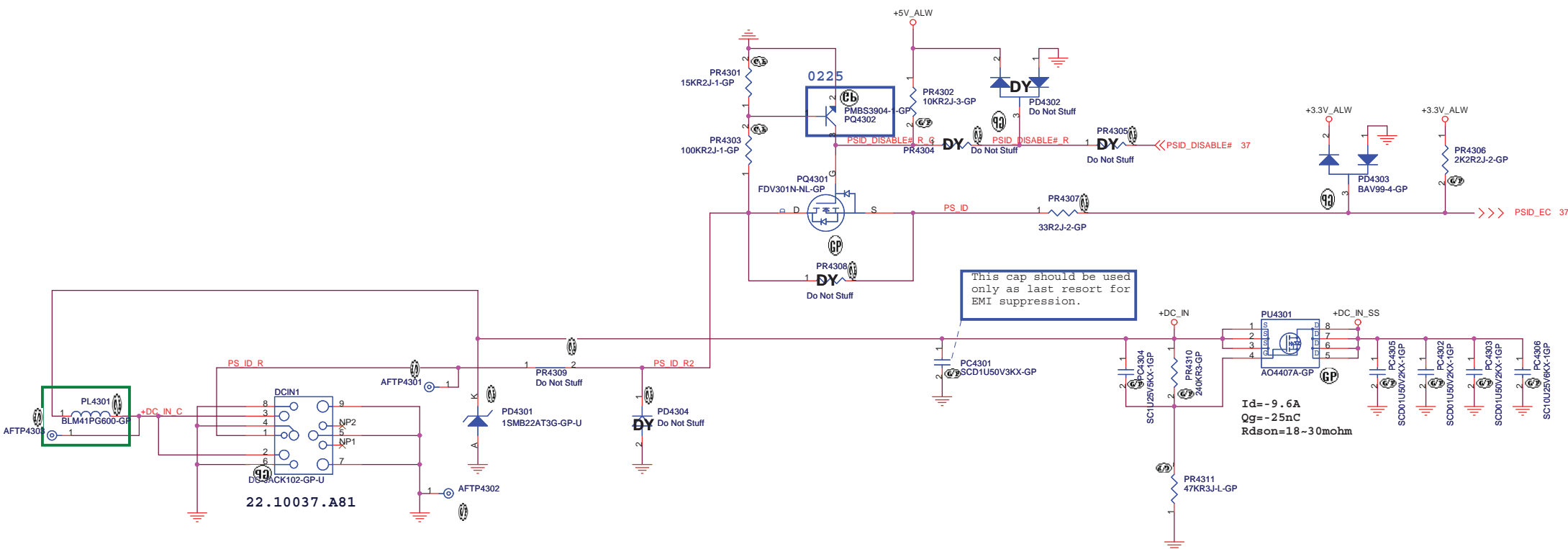


3 DJ2 AMD UMA (10 100 w HDMI)

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
			Title: Power Plane Enable		
Size: Custom	Document Number: Chelsea DJ2 AMD UMA			Date: Tuesday, April 13, 2010	
Sheet: 42 of 90			http://hobi-elektronika.net		

SSID = PWR.Support

DCIN CONN



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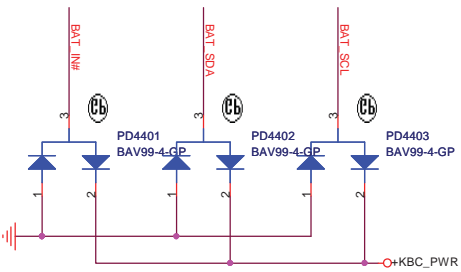
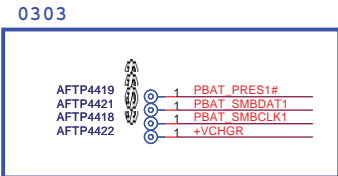
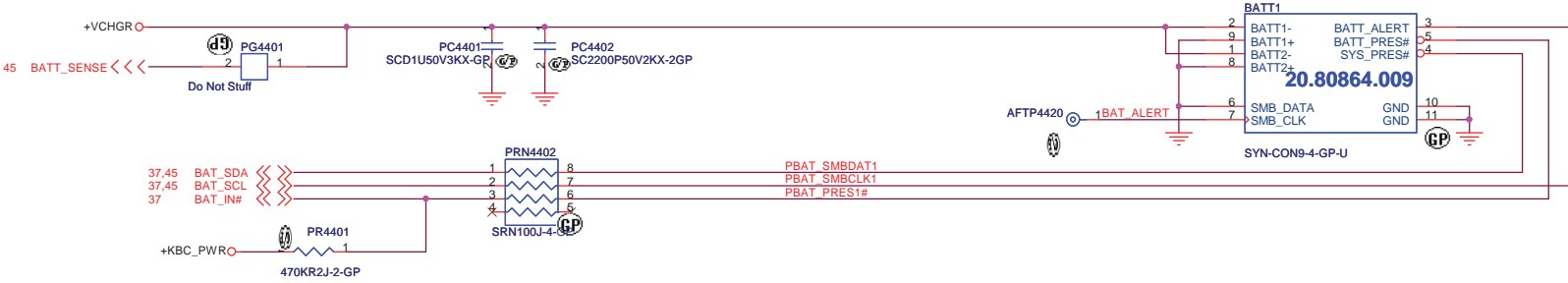
3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **DCIN**

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Batt Connector



3 DJ2 AMD UMA (10 100 w HDMI)

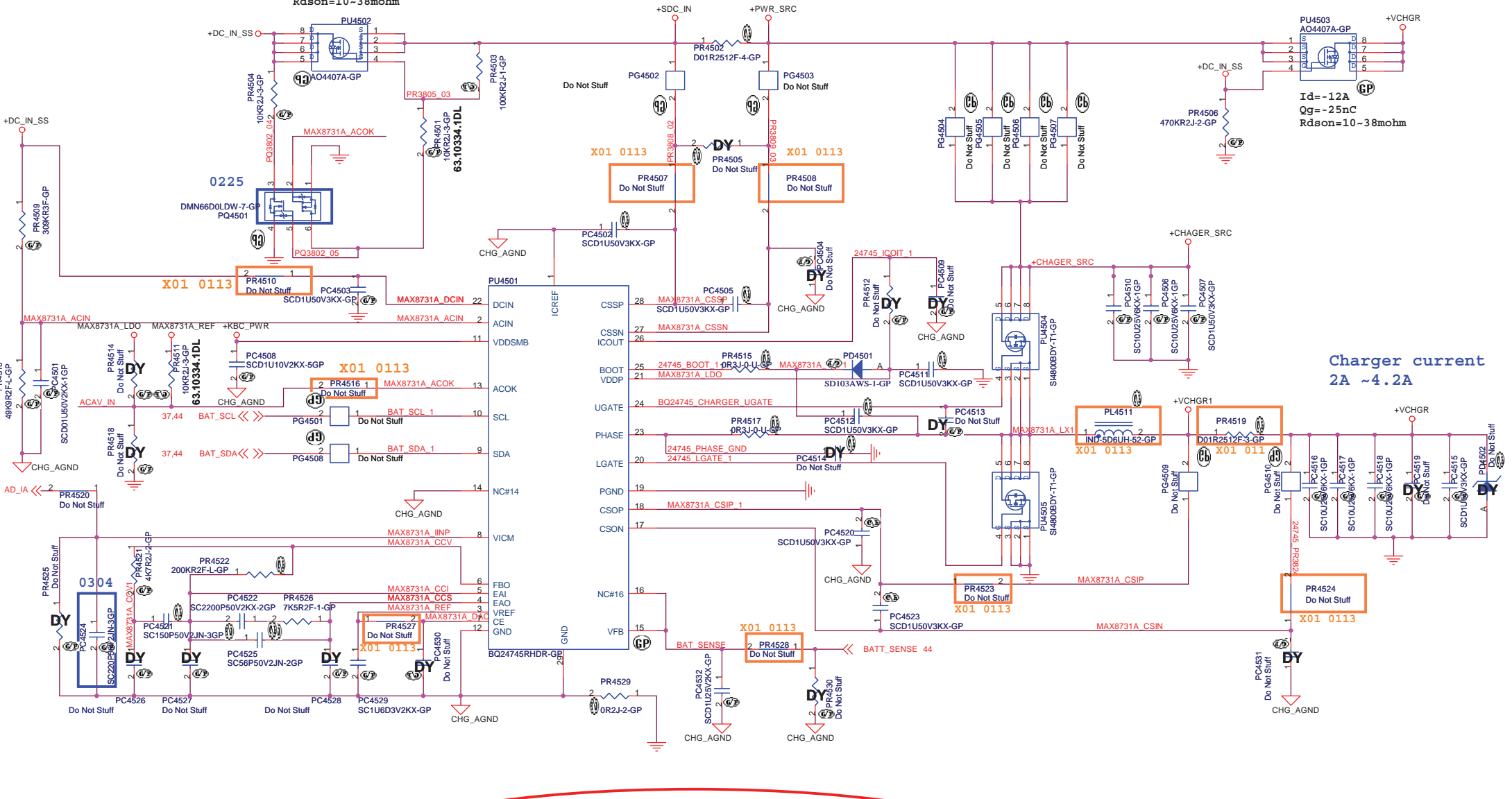
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **BATT CONN**

Size: A3	Document Number: Chelsea DJ2 AMD UMA	Rev: X01
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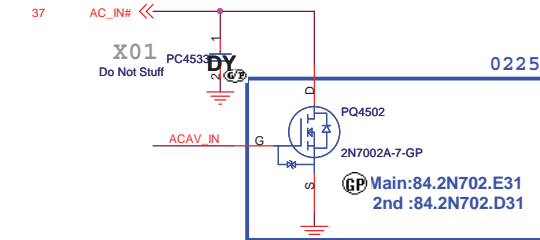
SSID = Charger

Id=-12A
Qg=-25nC
Rdson=10~38mohm



Charger current
2A ~4.2A

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
 Inductor: 5.8UH SIL104R-5R8A-R DCR:24mohm Isat =7Arms Delta / 68.5R850.101
 O/P cap: 10U 25V K1206 X5R/ 78.10622.52L
 H/S: SI4800BDY/ 23mOhm/30mohm@4.5Vgs/ 84.04800.D37
 L/S: SI4800BDY/ 23mOhm/30mohm@4.5Vgs/ 84.04800.D37



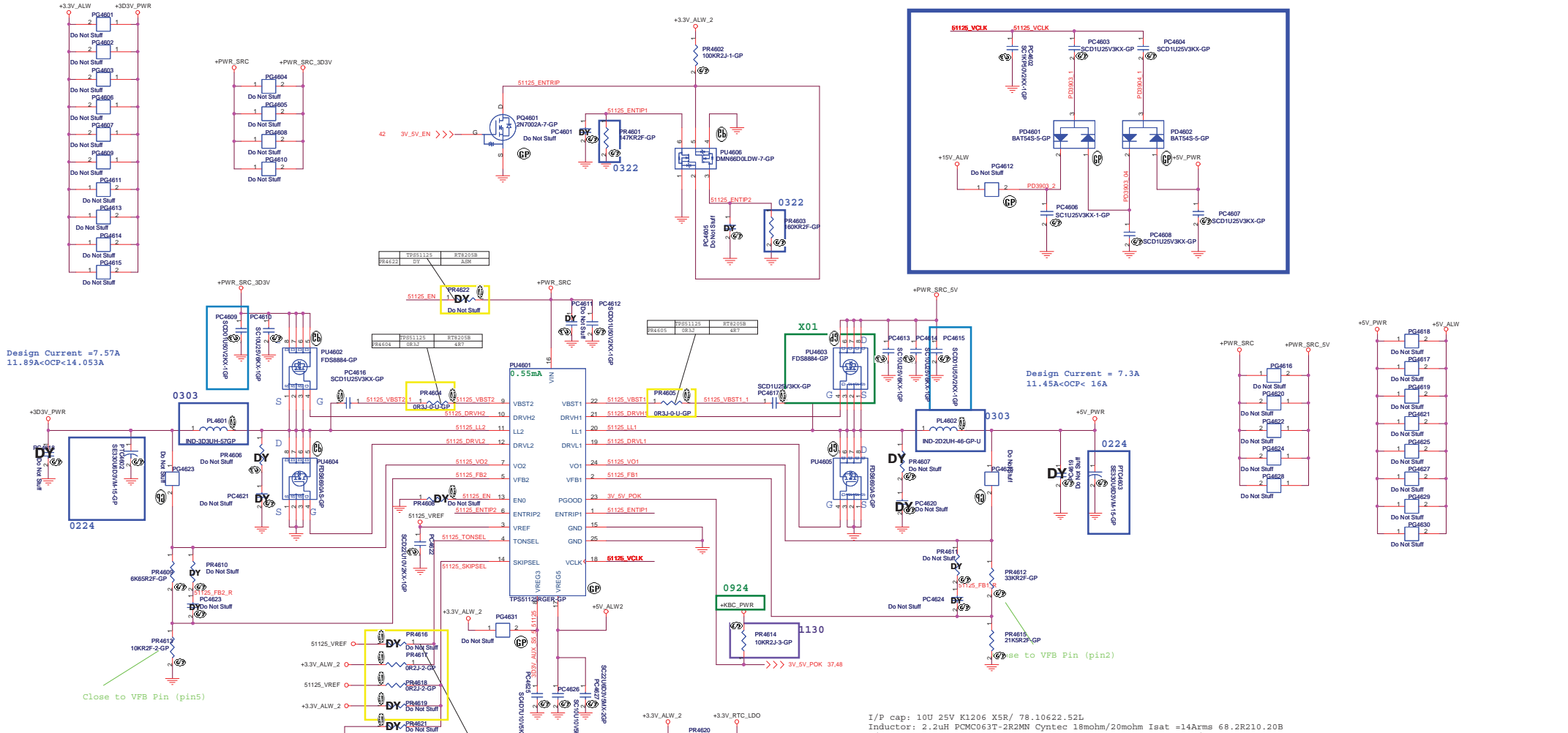
<http://hobi-elektronika.net>

3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **CHARGER BQ24745**

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Design Current = 7.57A
11.89A<OCP<14.053A

Design Current = 7.3A
11.45A<OCP< 16A

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
 Inductor: 3.3UH PCMC063T-3R3MN Cynotec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
 O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
 O/P cap: 100U 6.3V TEPSLB20J107M(45) 8R 45mOhm 1.374Arms NEC_TOKIN/77.C1071.081
 H/S: FDS8884 23mohm/30mOhm@4.5Vgs/ 84.08884.037
 L/S: FDS6690AS 12mohm/15mOhm@4.5Vgs/ 84.06690.E37

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
 Inductor: 2.2uH PCMC063T-2R2MN Cynotec 18mohm/20mohm Isat =14Arms 68.2R210.20B
 O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
 O/P cap: 100U 6.3V TEPSLB20J107M(45) 8R 45mOhm 1.374Arms NEC_TOKIN/77.C1071.081
 H/S: FDS8884 23mohm/30mOhm@4.5Vgs/ 84.08884.037
 L/S: FDS6690AS 12mohm/15mOhm@4.5Vgs/ 84.06690.E37

RT8205B(74.08205.A73):

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

RT8205B(74.08205.B73):

TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3	365kHz	460kHz
VREG5	365kHz	460kHz

TP5S1125

74.51125.073	
RT8205BQGW	74.08205.B73

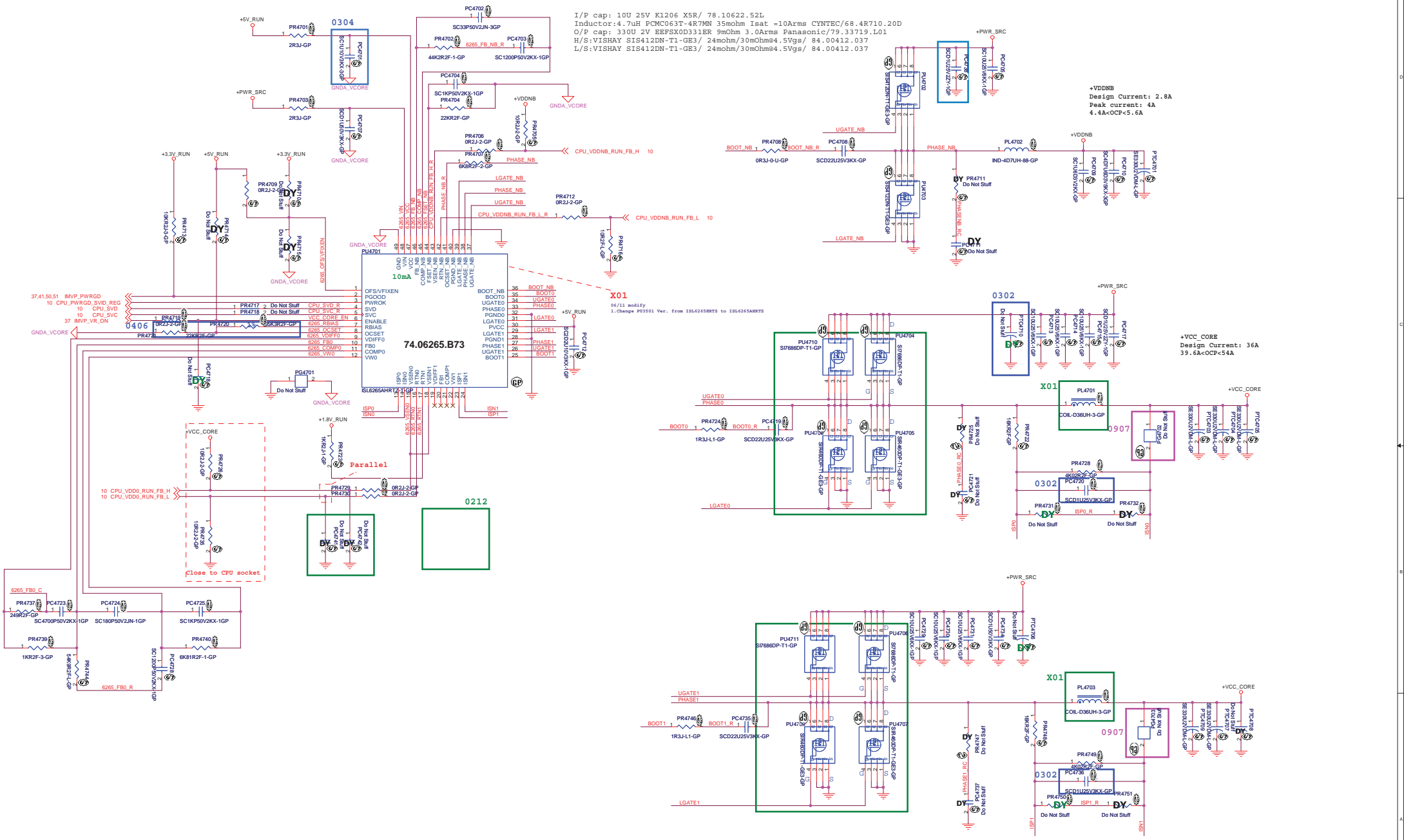
SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

EN0	Open	820k to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

<http://hobi-elektronika.net>

ISL6265HRTZ-T for +VCC_CORE&+VDDNB

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
 Inductor: 4.7uH PCMC063T-4R7MN 35mohm Isat =10Arms CYNTEC/68.4R710.20D
 O/P cap: 330U 2V EEF5X0D331ER 9mOhm 3.0Arms Panasonic/79.33719.L01
 H/S: VISHAY SI5412DN-T1-GE3/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037
 L/S: VISHAY SI5412DN-T1-GE3/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037

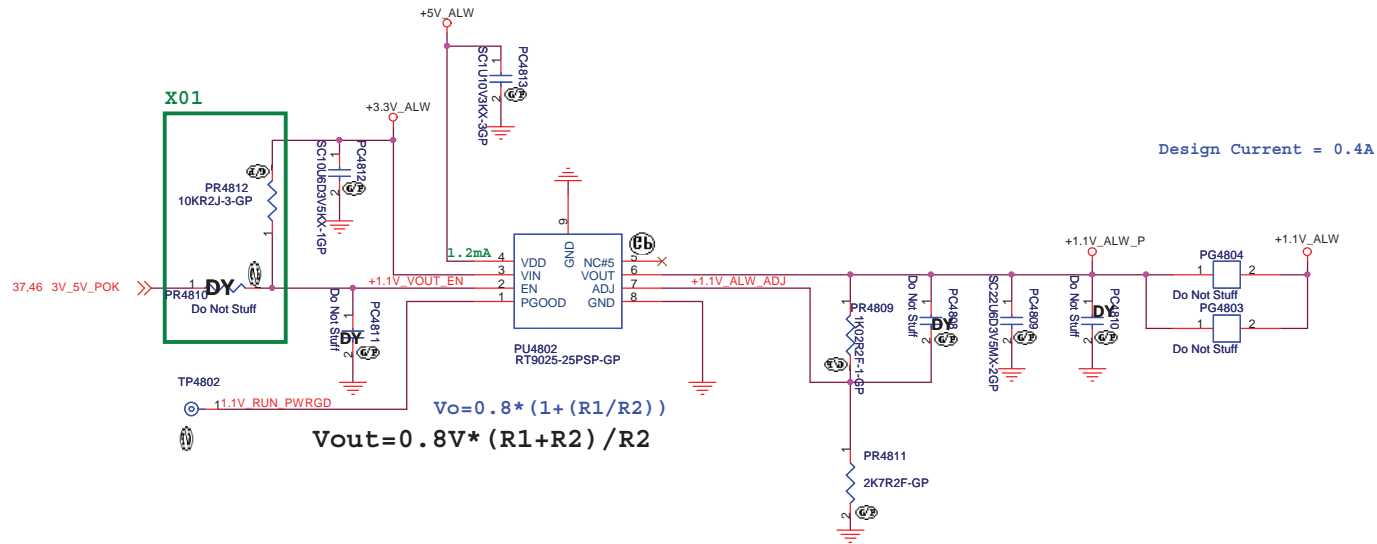


+VDDNB
 Design Current: 2.8A
 Peak current: 4A
 4.4A@CC<5.6A

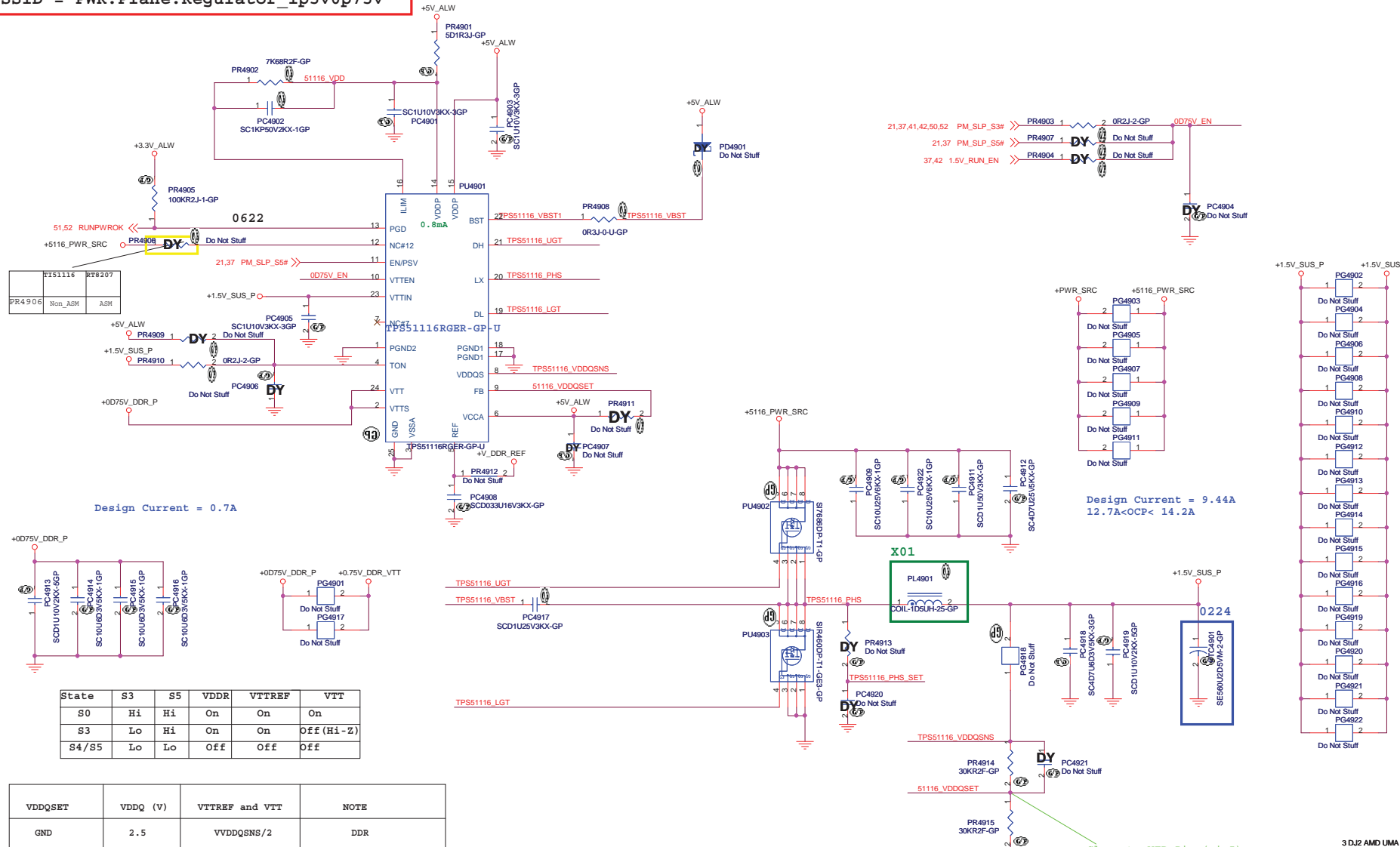
+VCC_CORE
 Design Current: 36A
 39.6A@CC<54A

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
 Inductor: 0.36uH PCMC104T-R36MN1R05J CYNTEC DCR 1.05 (+5%~-5%)mohm
 Isat =60Arms 68.R3610.20C
 O/P cap: 330U 2V EEF5X0D331ER 9mOhm 3.0Arms Panasonic/79.33719.L01
 H/S: SiS406DN/ POWERPAK-8/ 11.5mOhm/14.5mOhm @4.5Vgs/ 84.00406.037
 L/S: SiS402DN/ POWERPAK-8/ 6.4mOhm/8mohm@4.5Vgs/ 84.00402.037

RT9025 for +1.1V_ALW



SSID = PWR.Plane.Regulator_1p5v0p75v



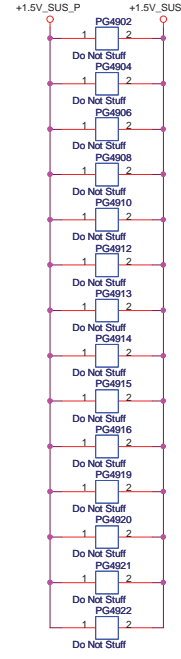
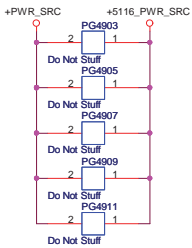
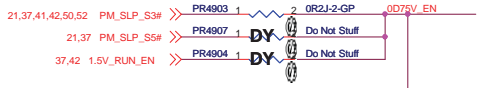
Design Current = 0.7A

Design Current = 9.44A
12.7A < OCP < 14.2A

State	S3	S5	VDDR	VTREF	VIT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (H1-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTREF and VIT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
 Inductor: 1.5UHPMCMC104T-1R5MN DCR:3.8/4.2mohm Isat =33Arms Cyntec/ 68.1R510.10J
 O/P cap: 220U 2V EEFXC0D221R 15mOhm 2.7Arms PANASONIC/ 79.22719.20L
 H/S: PDS8880 9.6mohm/12mOhm@4.5Vgs/ 84.08880.037
 L/S: PDS6676AS 5.9mOhm/7.25mOhm@4.5Vgs/ 84.06676.A37



Close to VFB Pin (pin5)

3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
 21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS5116RGER +1.5V SUS**

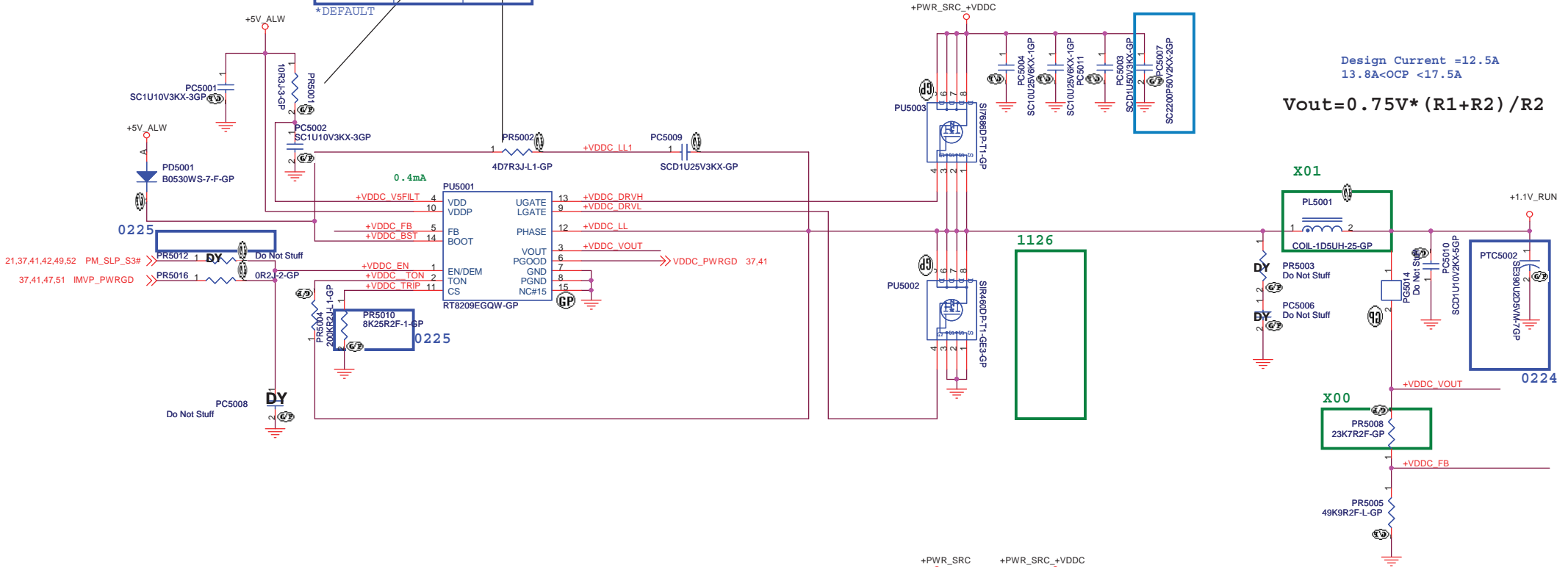
Size: Custom Document Number
 Customer: **Chelsea DJ2 AMD UMA** Rev: X01

Date: Tuesday, April 13, 2010 Sheet 49 of 90

SSID = PWR.Plane.Regulator_VDDC

PWM TYPE	PR5001	PR5002
*RT8209E	10 ohm	4.7 ohm
TPS51117	300 ohm	0 ohm

*DEFAULT

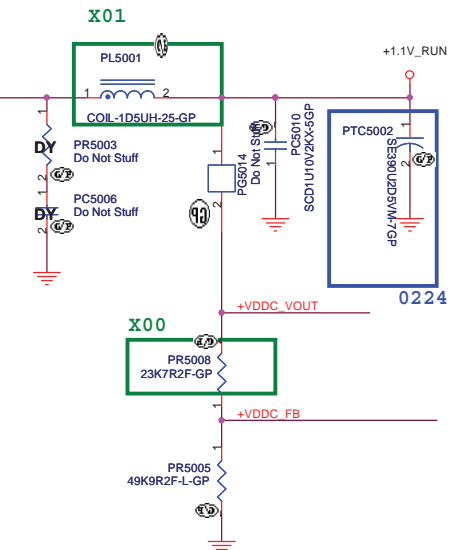
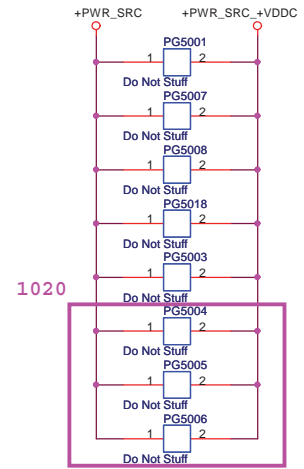


Design Current =12.5A
13.8A<OCP <17.5A

$$V_{out} = 0.75V * (R1 + R2) / R2$$

21,37,41,42,49,52 PM_SLP_S3#
37,41,47,51 IMVP_PWRGD

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UHPCMC104T-1R5MN DCR:3.8/4.2mohm Isat =33Arms Cyntec/ 68.1R510.10
O/P cap: 330U 2.5V PSLV0E337M(15) 15mOhm 2.886Arms NEC_TOKIN/ 77.C3371.10L
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037



3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

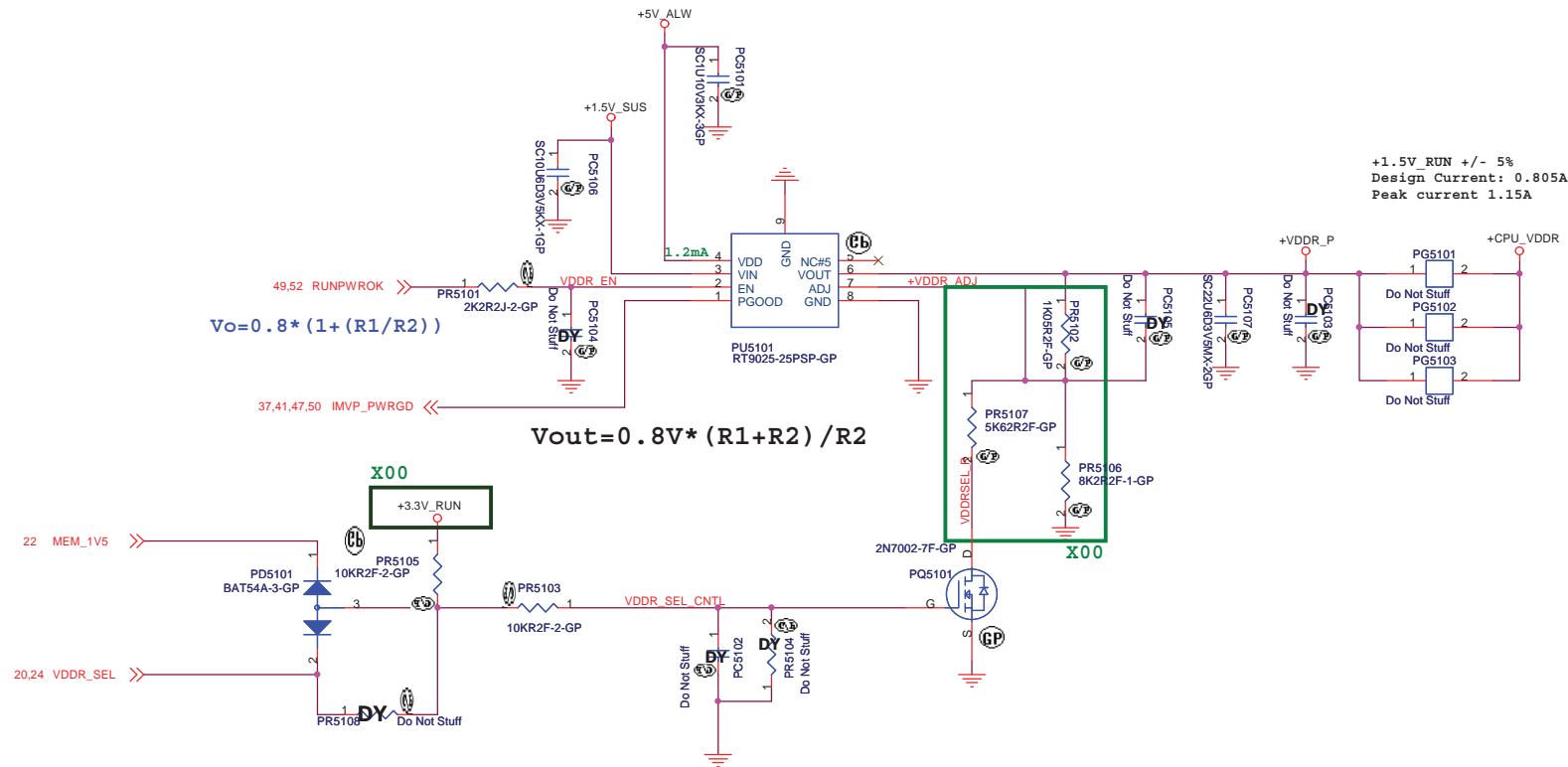
Title: **RT8209 +1.1V RUN**

Size A3 Document Number **Chelsea DJ2 AMD UMA** Rev **X01**

Date: Tuesday, April 13, 2010 Sheet 50 of 90

SSID = PWR.Plane.Regulator_VDDR

RT9025 for +VDDR



VDDR_SEL	+CPU_VDDR
H	1.05V
L	0.9V

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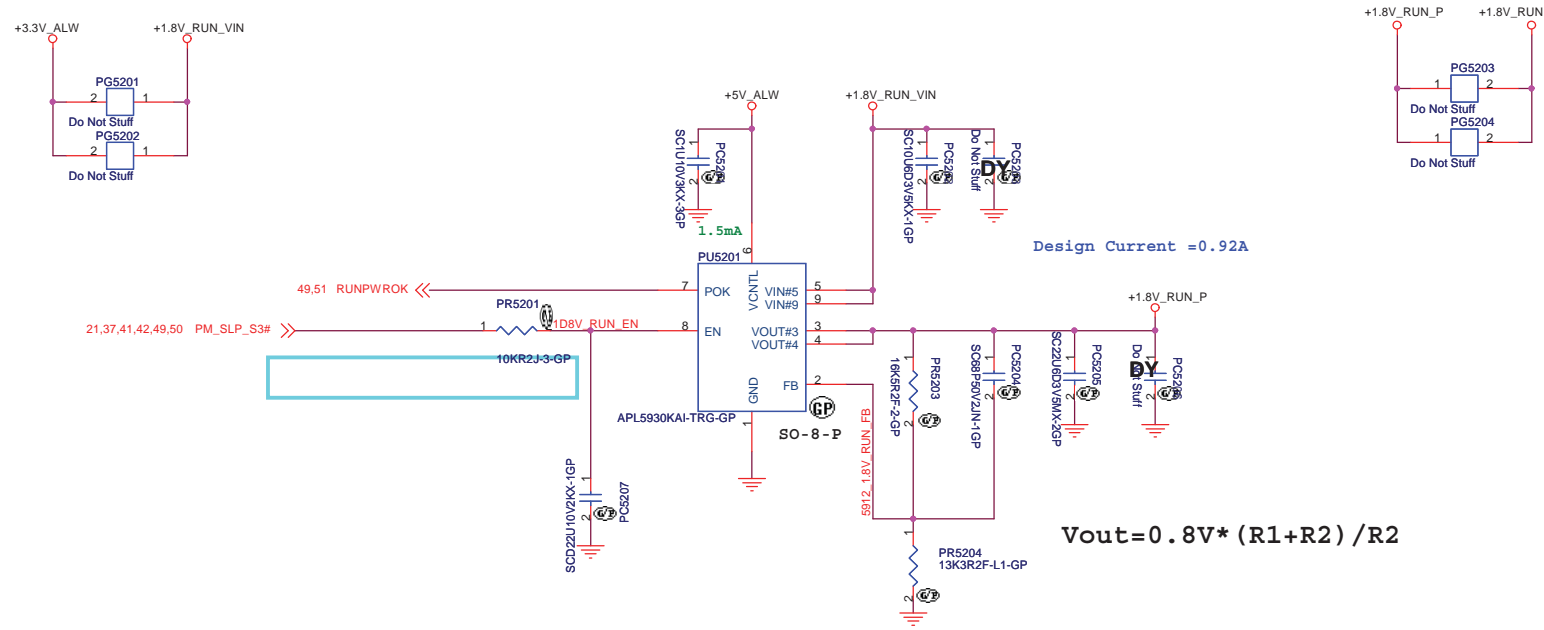
3 DJ2 AMD UMA (10 100 w HDMI)

DELL Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title RT9025 +VDDR		
Size A3	Document Number Chelsea DJ2 AMD UMA	Rev X01
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SSID = PWR.Plane.Regulator_1p8v

APL5930 for +1.8V_RUN



<http://hobi-elektronika.net>

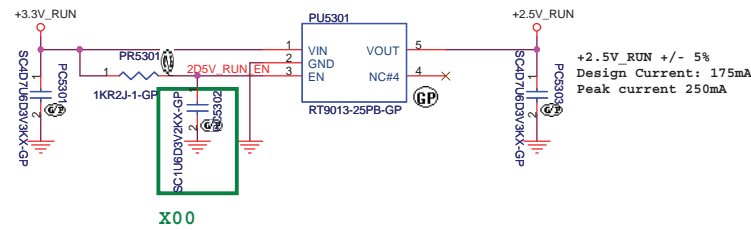
3 DJ2 AMD UMA (10 100 w HDMI)



Title		
APL5930 +1.8V RUN		
Size	Document Number	Rev
A3	Chelsea DJ2 AMD UMA	X01
Date:	Tuesday, April 13, 2010	Sheet 52 of 90

SSID = PWR.Plane.Regulator_2p5v

RT9013-25PB for +2.5V_RUN



<http://hobi-elektronika.net>

3 DJ2 AMD UMA (10 100 w HDMI)

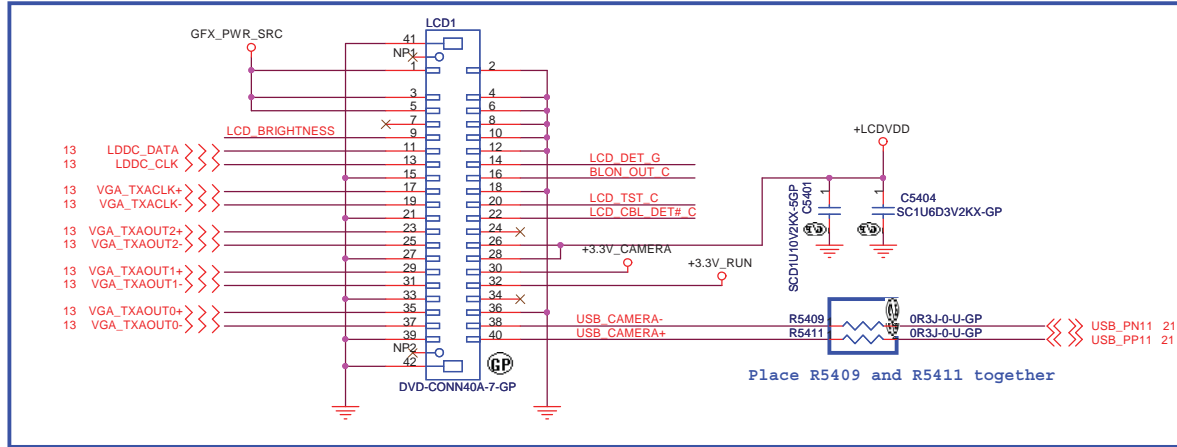


Title VREG : +CPU_VDDR&+2.5V_RUN		
Size Custom	Document Number Chelsea DJ2 AMD UMA	Rev X01
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SSID = VIDEO

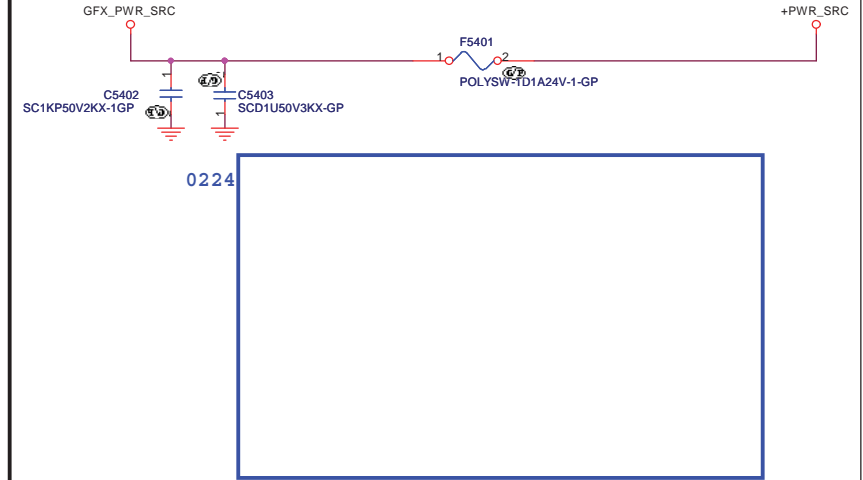
LVDS CONNECTOR

0225



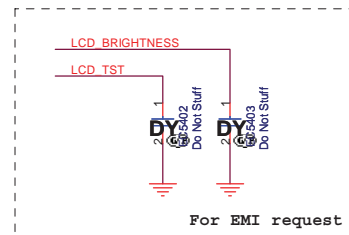
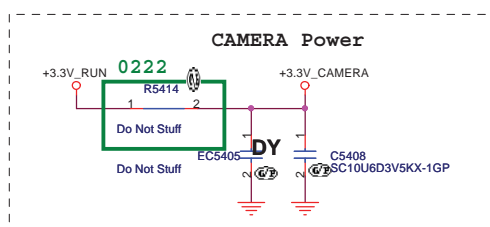
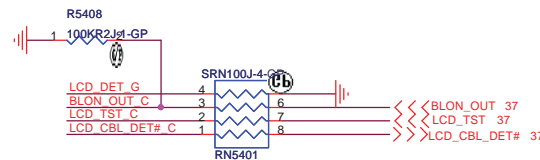
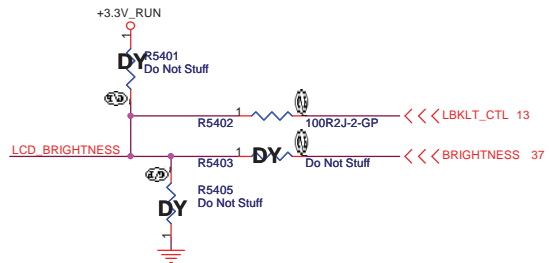
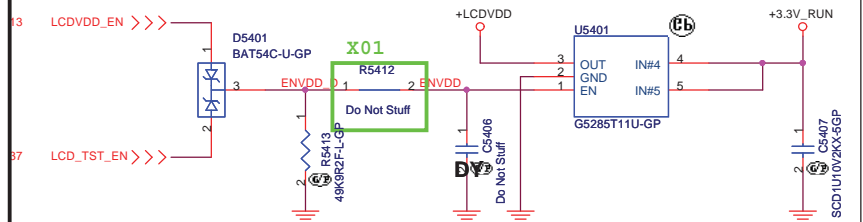
SSID = Inverter

INVERTER POWER



SSID = VIDEO

LCD POWER



3 DJ2 AMD UMA (10 100 w HDMI)



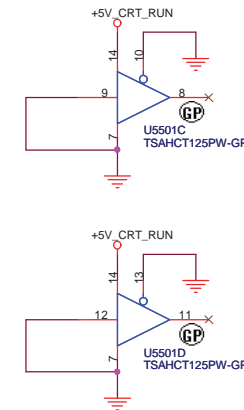
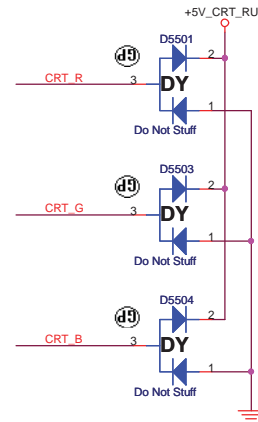
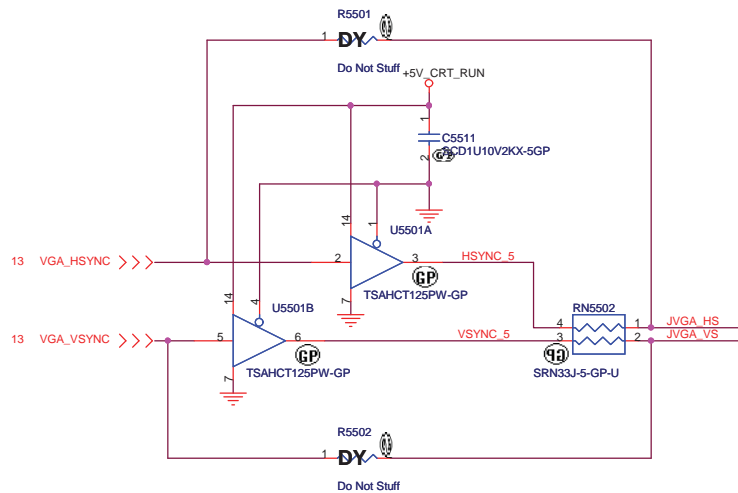
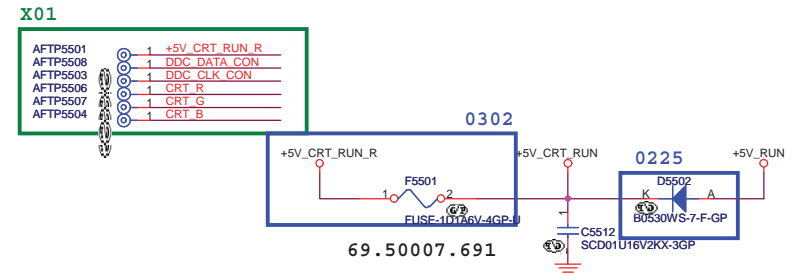
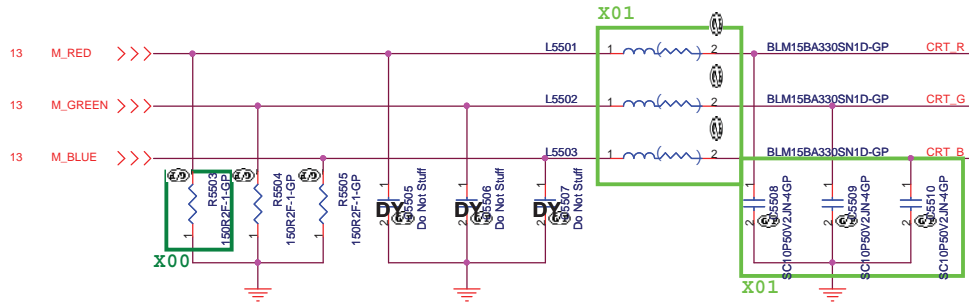
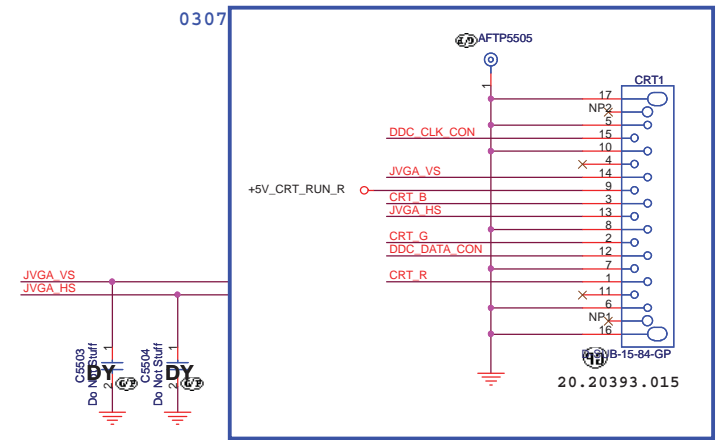
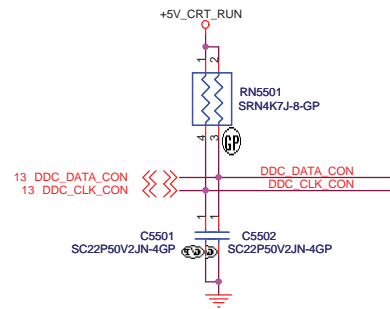
Title LCD/Inverter Connector		
Size A3	Document Number Chelsea DJ2 AMD UMA	Rev X01
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SSID = VIDEO

Layout Note:

- *Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
- * RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.



<http://hobi-elektronika.net>


3 DJ2 AMD UMA (10 100 w HDMI)

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
			Title: CRT Connector		
Size	Document Number	Sheet		Rev	
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(Blanking)

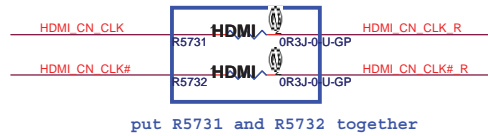
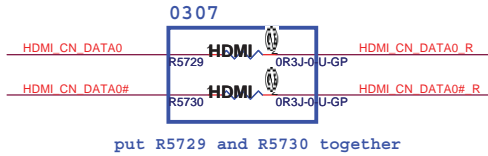
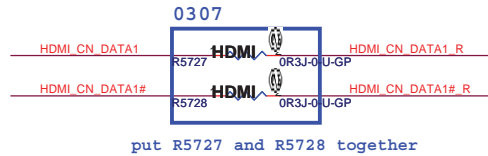
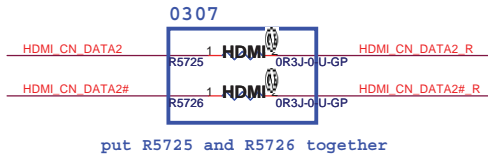
<http://hobi-elektronika.net>

3 DJ2 AMD UMA (10 100 w HDMI)

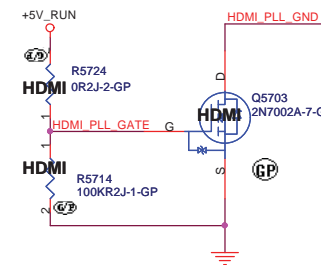
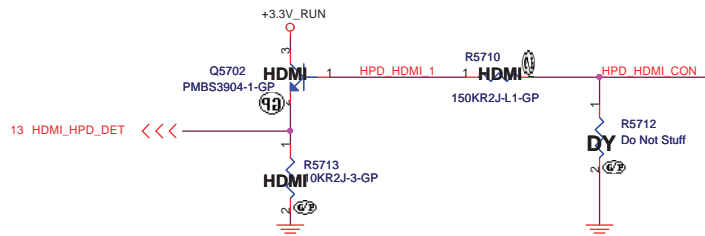
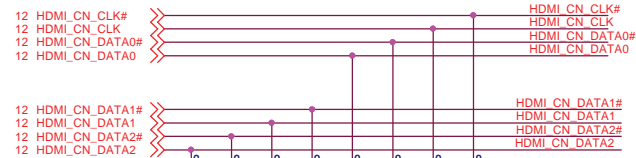
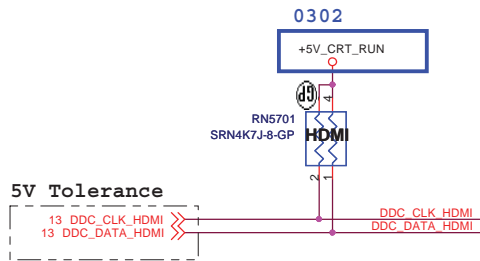
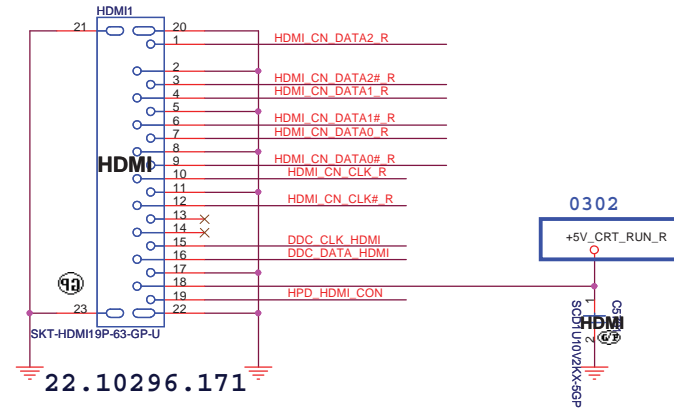
		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
Size A3	Document Number Chelsea DJ2 AMD UMA	Rev X01
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SSID = VIDEO

HDMI CONNECTOR



HDMI CONN



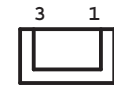
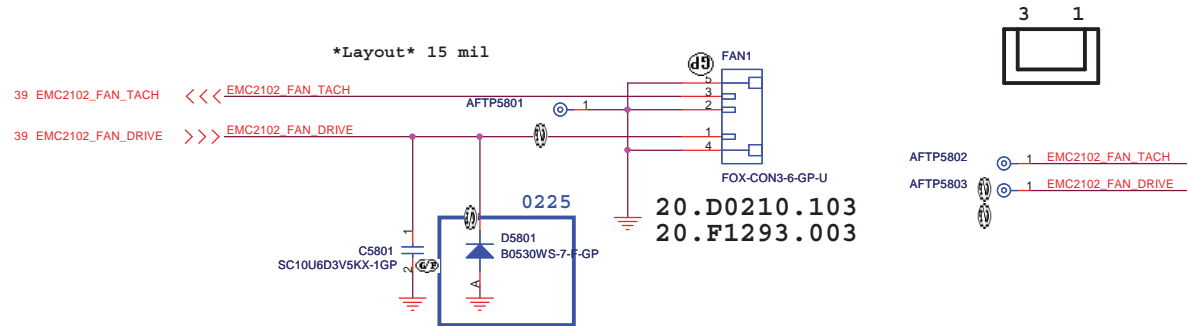
<http://hobi-elektronika.net>

3 DJ2 AMD UMA (10 100 w HDMI)

DELL		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
HDMI Level Shifter/Connector			
Size	Document Number	Rev	
A3	Chelsea DJ2 AMD UMA	X01	
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SSID = Thermal

Fan Connector



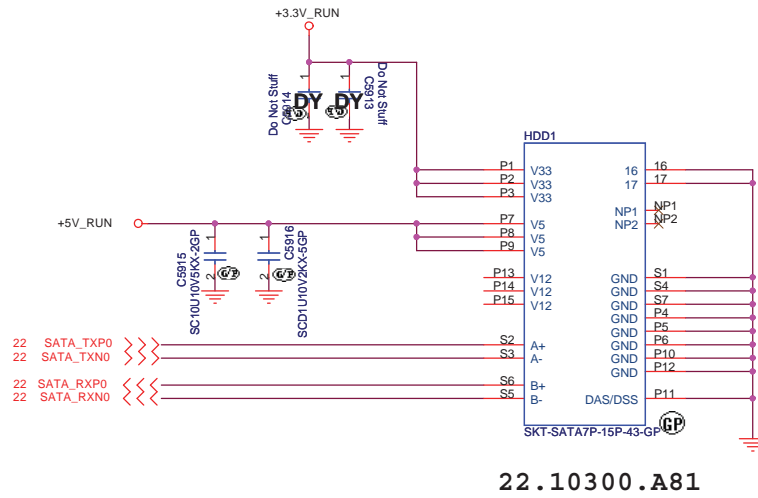
<http://hobi-elektronika.net>

3 DJ2 AMD UMA (10 100 w HDMI)

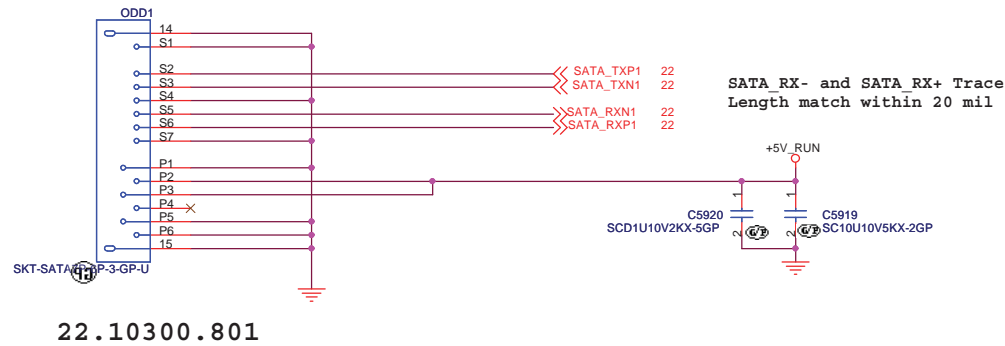


Title ITP/Fan Connector		
Size A3	Document Number Chelsea DJ2 AMD UMA	Rev X01
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SATA HDD Connector



ODD Connector

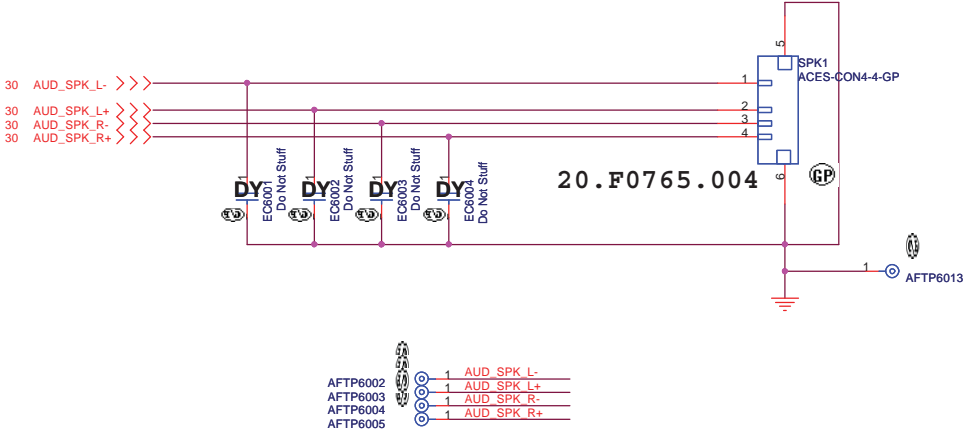


<http://hobi-elektronika.net>

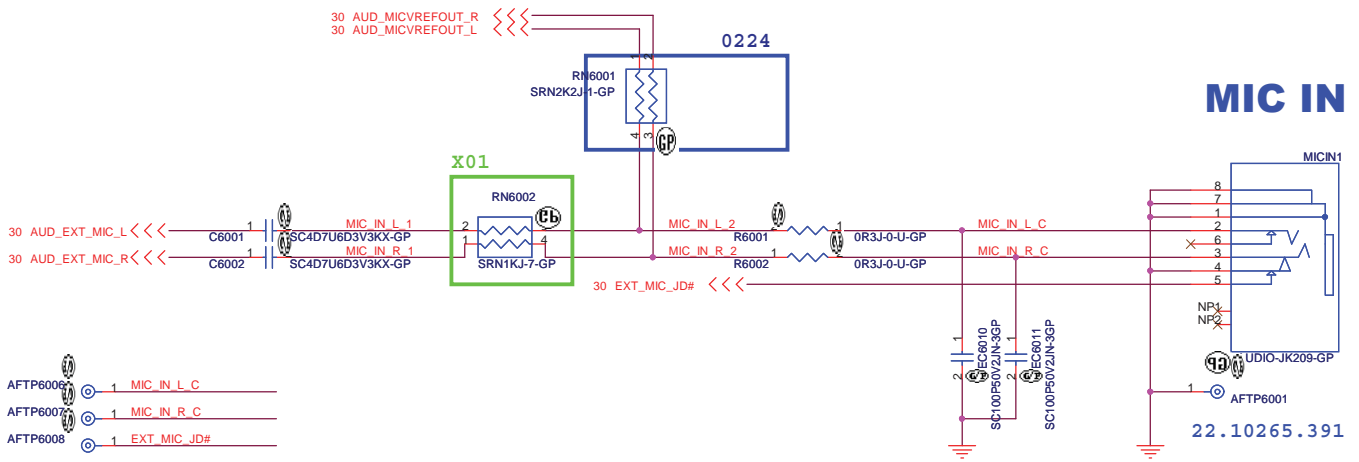
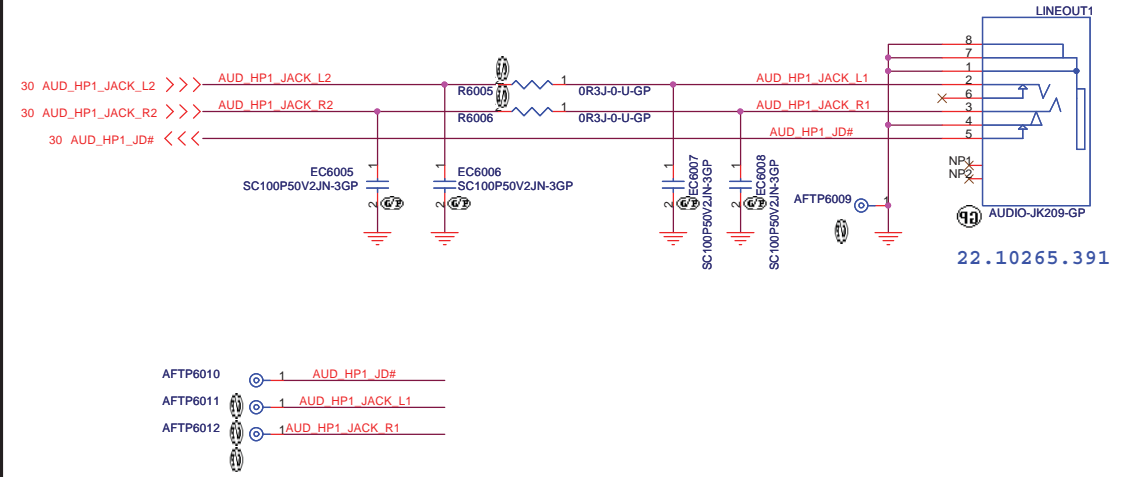
3 DJ2 AMD UMA (10 100 w HDMI)

SSID = AUDIO

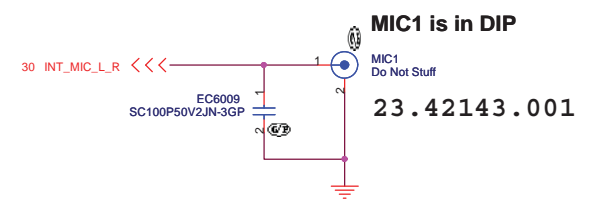
Speaker Connector



LINE1 OUT



Internal Microphone



<http://hobi-elektronika.net>

3 DJ2 AMD UMA (10 100 w HDMI)

DELL Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

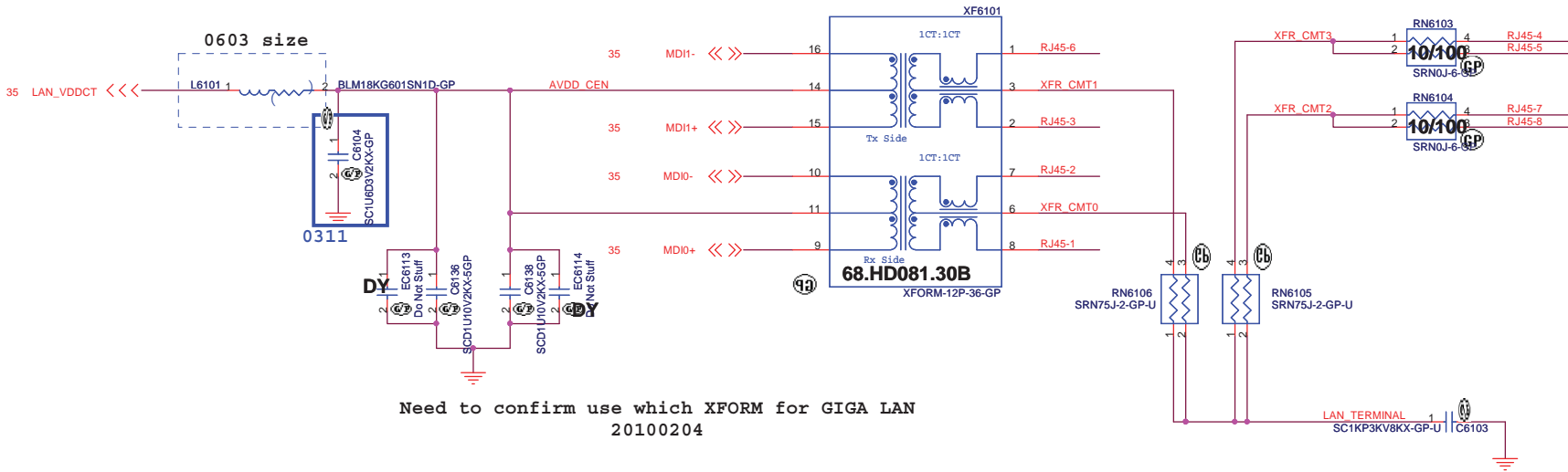
Title
Audio Jack

Size A3	Document Number Chelsea DJ2 AMD UMA	Rev X01
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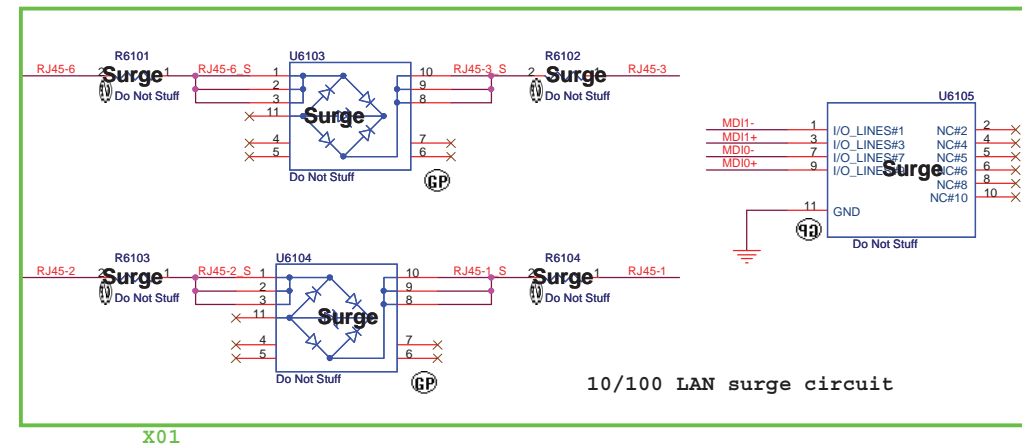
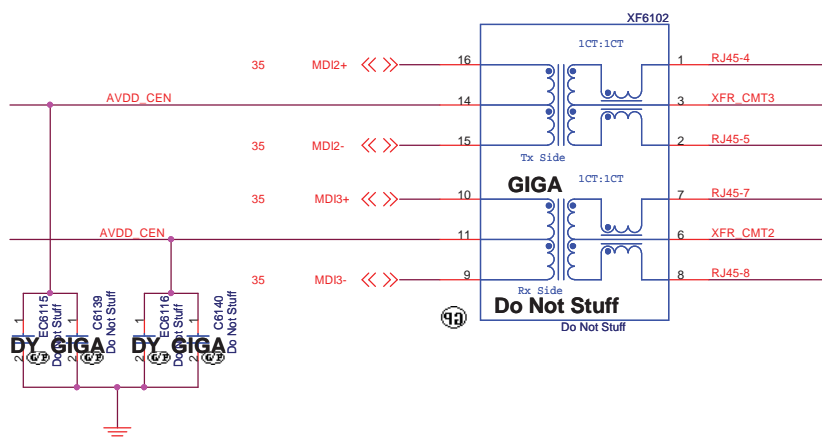
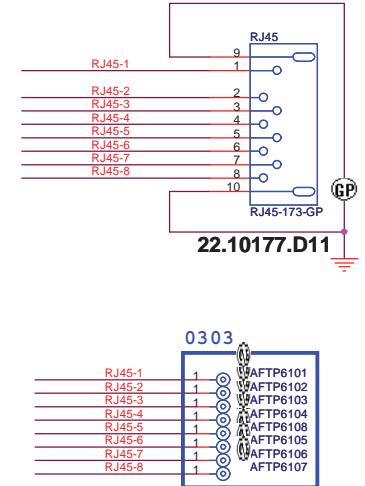
2009-10-1 Change MDI1+(XF601.16) to MDI1+(XF601.15)
 Change MDI1-(XF601.15) to MDI1-(XF601.16)
 Change MDI0+(XF601.10) to MDI0+(XF601.9)
 Change MDI0-(XF601.9) to MDI0-(XF601.10)
 Change RJ45-3(XF601.1) to RJ45-3(XF601.2)
 Change RJ45-6(XF601.2) to RJ45-6(XF601.1)
 Change RJ45-1(XF601.7) to RJ45-1(XF601.8)
 Change RJ45-2(XF601.8) to RJ45-2(XF601.7)

1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

10/100M Lan Transformer



RJ45 Connector



<http://hobi-elektronika.net>

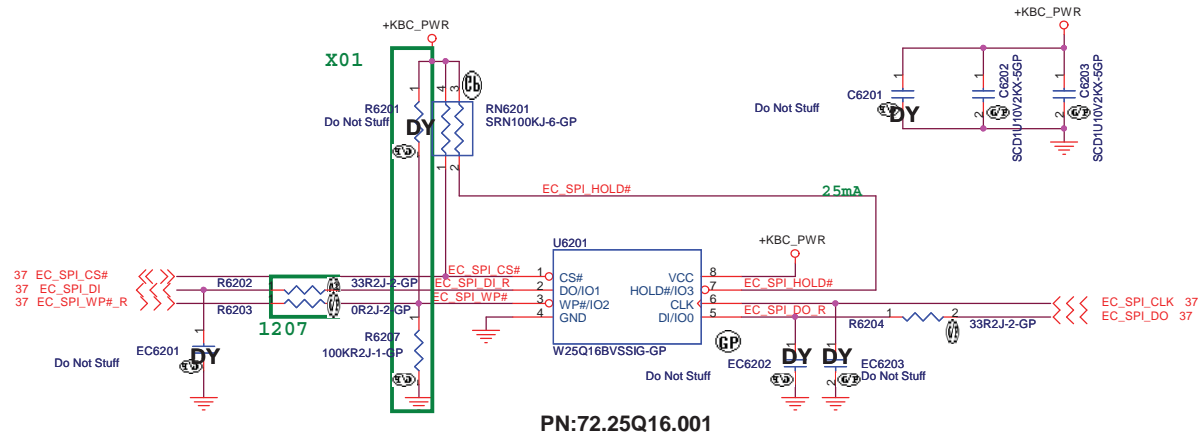
3 DJ2 AMD UMA (10 100 w HDMI)

DELL Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

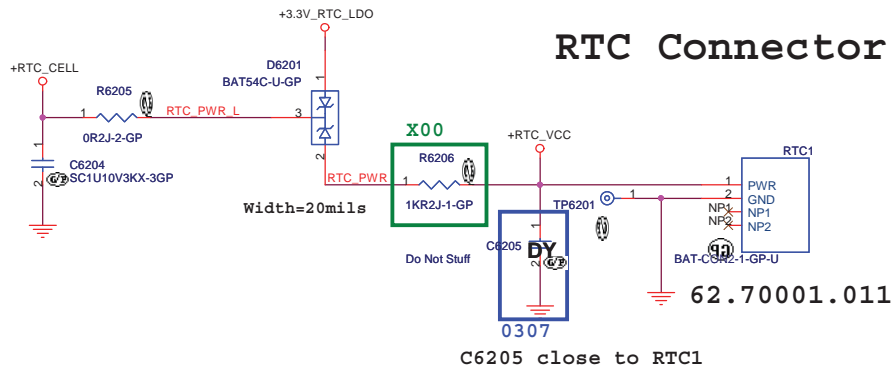
Title			XFORM/RJ45		
Size	Document Number	Rev			
A3		Chelsea DJ2 AMD UMA			X01
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SSID = Flash.ROM

SPI FLASH ROM (16M bits) for KBC



SSID = RBATT



<http://hobi-elektronika.net>

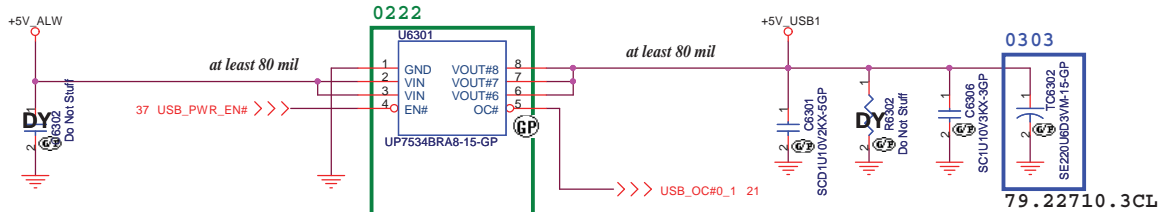
3 DJ2 AMD UMA (10 100 w HDMI)

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

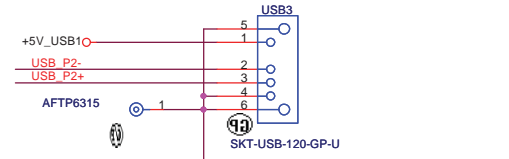
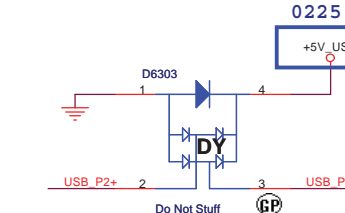
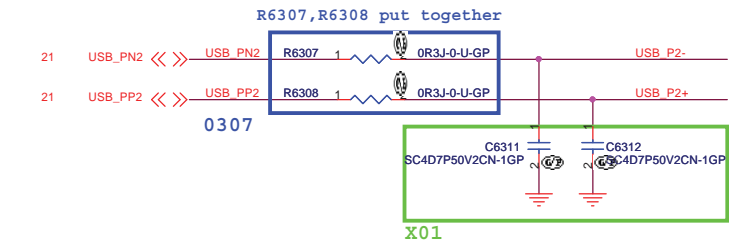
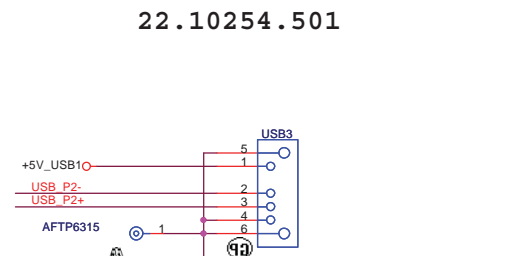
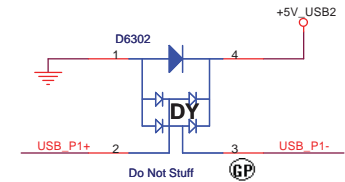
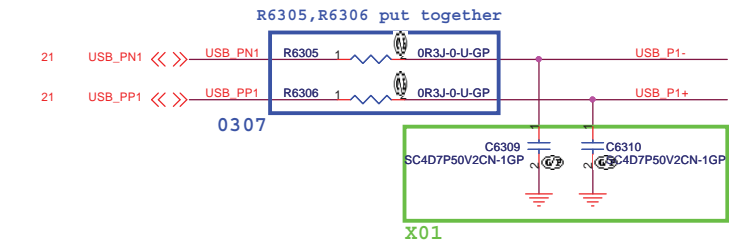
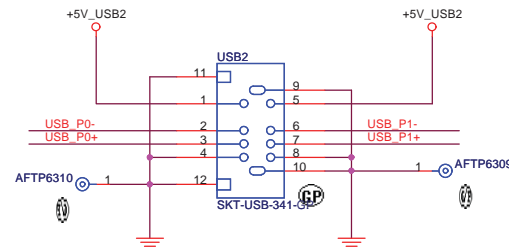
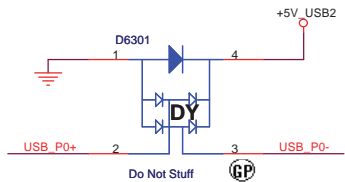
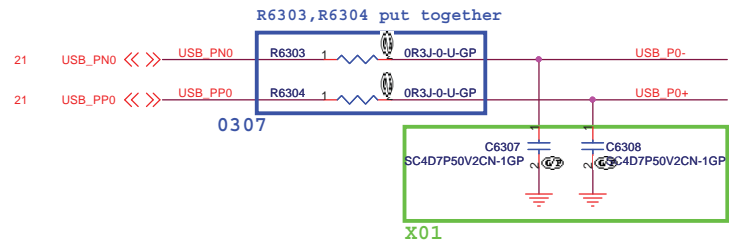
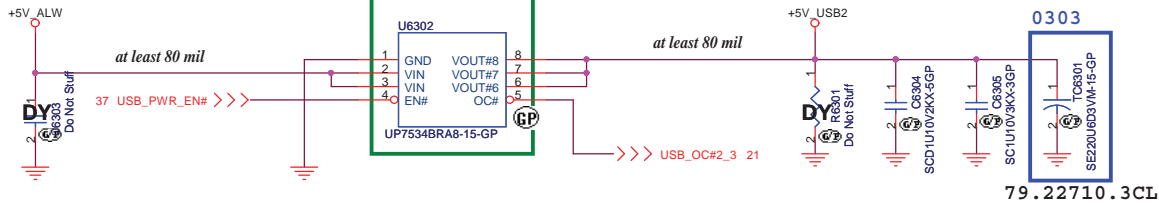
Title		
Flash/RTC		
Size	Document Number	Rev
A3	Chelsea DJ2 AMD UMA	X01
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SSID = USB

USB Power



Right USB Power



AFTP6311	1	+5V_USB1
AFTP6304	1	+5V_USB2
AFTP6302	1	USB_P0-
AFTP6301	1	USB_P0+
AFTP6306	1	USB_P1-
AFTP6305	1	USB_P1+
AFTP6313	1	USB_P2+
AFTP6312	1	USB_P2-

3 DJ2 AMD UMA (10 100 w HDMI)

DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB**

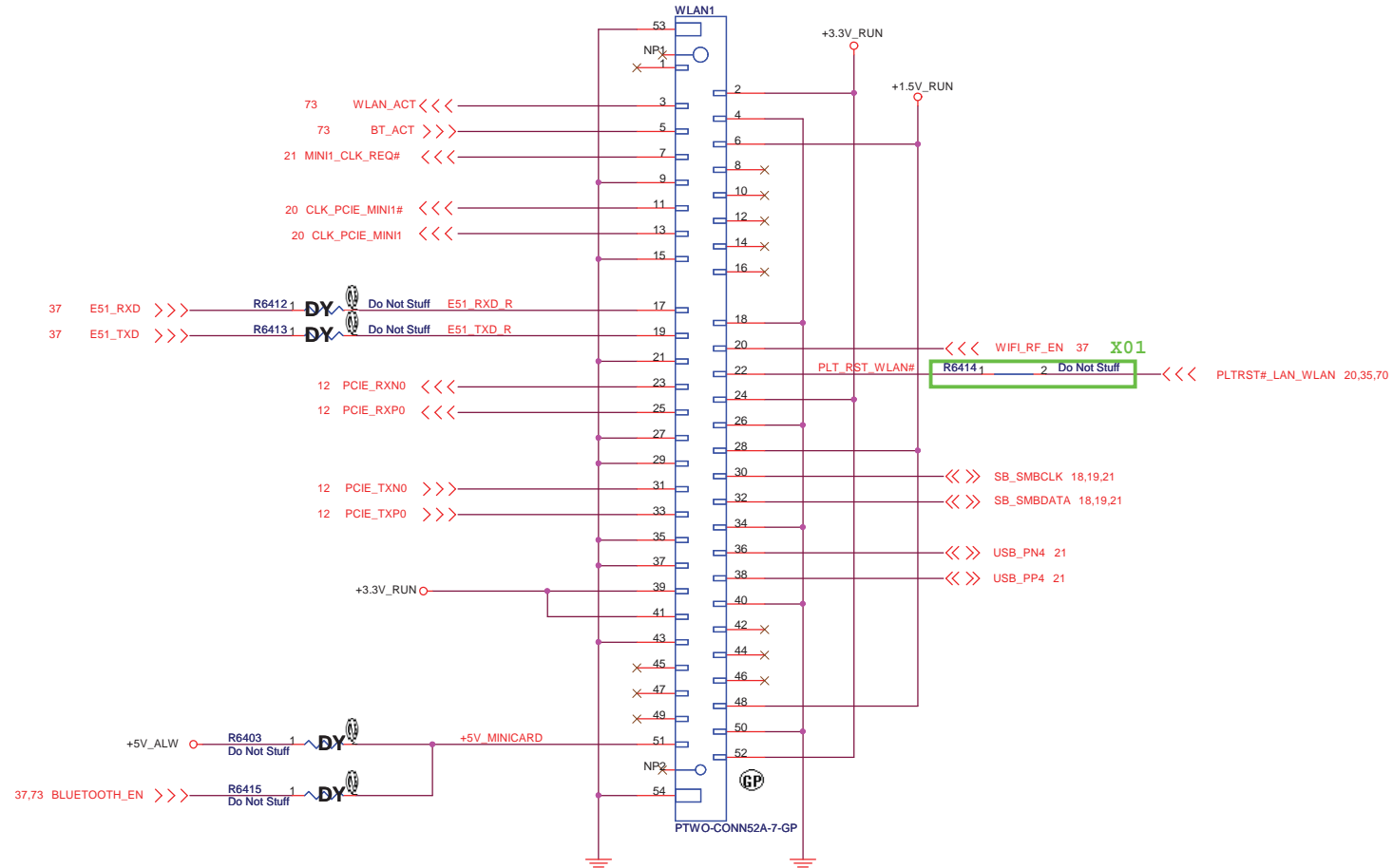
Size: Document Number: **Chelsea DJ2 AMD UMA** Rev: **X01**

Date: Wednesday, April 14, 2010 Sheet 63 of 90

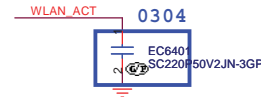
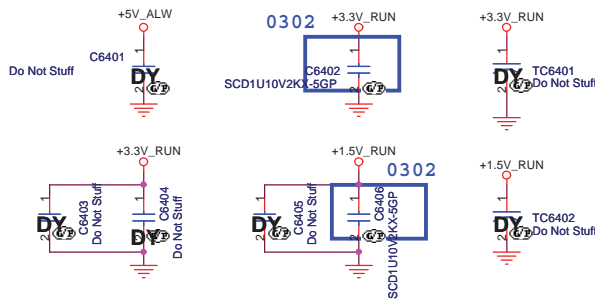
<http://hobi-elektronika.net>

SSID = Wireless

Mini Card Connector(802.11a/b/g)



20.F1516.052
62.10043.771



<http://hobi-elektronika.net>

3 DJ2 AMD UMA (10 100 w HDMI)



Title			MINICARD		
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A3		Chelsea DJ2 AMD UMA			X01
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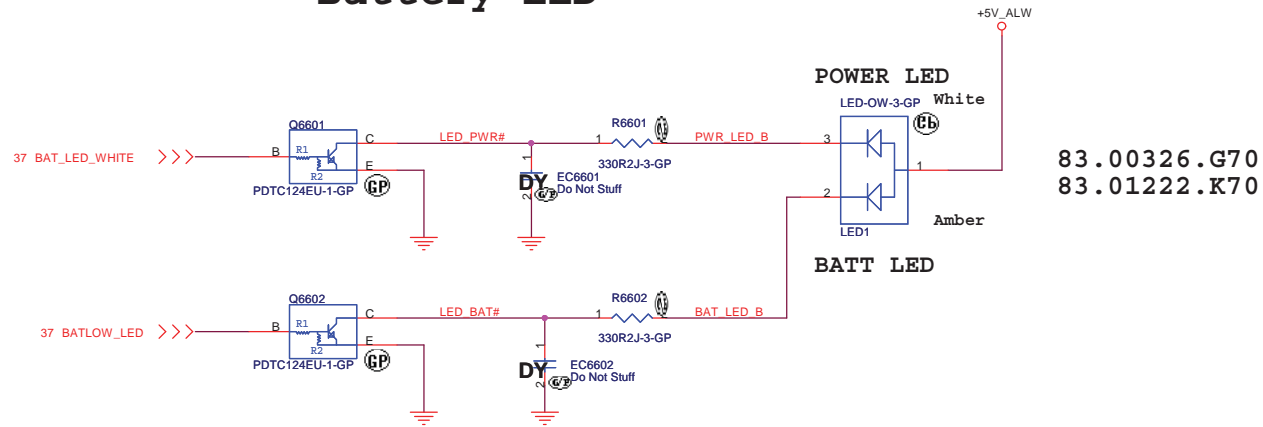
3 DJ2 AMD UMA (10 100 w HDMI)



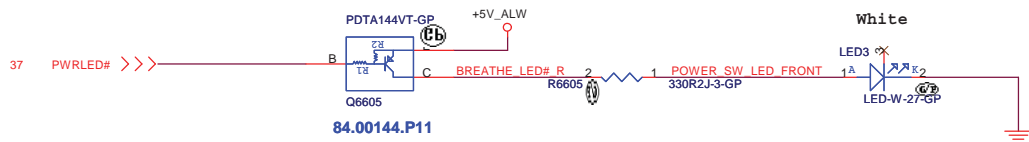
Title		
Reserved		
Size A3	Document Number Chelsea DJ2 AMD UMA	Rev X01
Date: Tuesday, April 13, 2010	Sheet 65 of 90	1

SSID = User.Interface

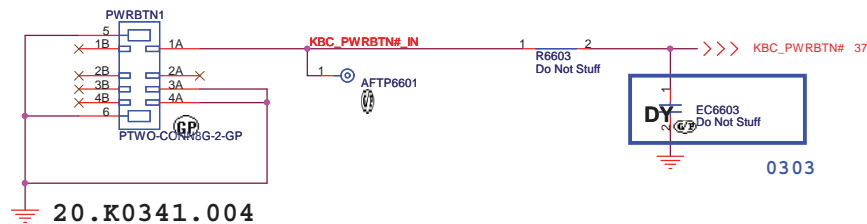
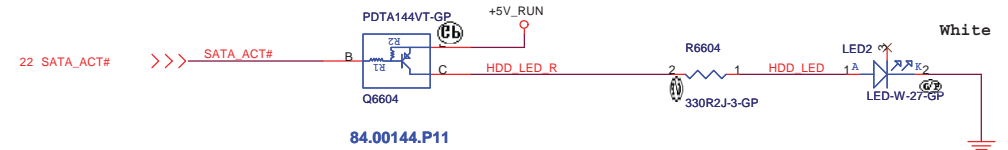
Battery LED



BREATHE PWR LED (Front)



HDD LED



3 DJ2 AMD UMA (10 100 w HDMI)



Title LED/PWRBTN		
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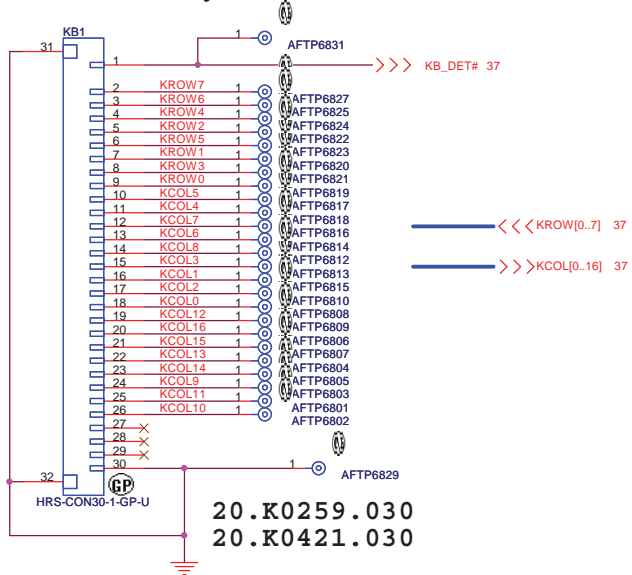
3 DJ2 AMD UMA (10 100 w HDMI)



Title		
Reserved		
Size A3	Document Number Chelsea DJ2 AMD UMA	Rev X01
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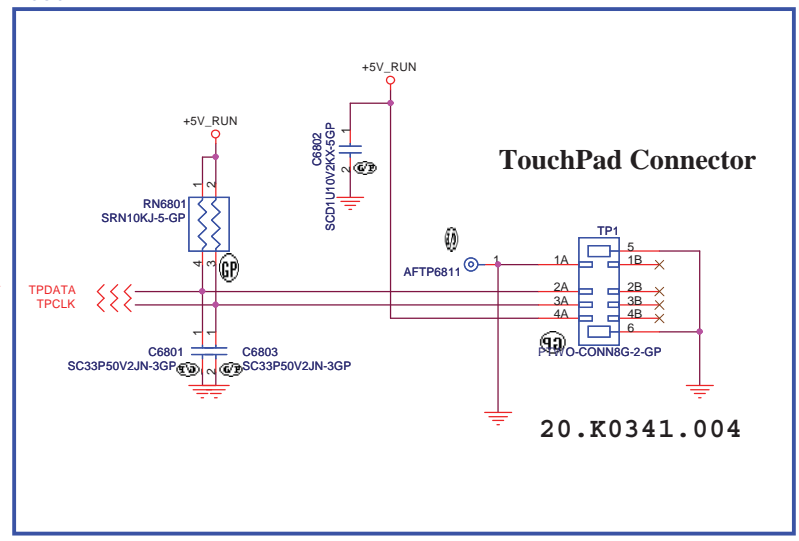
SSID = KBC

Internal Keyboard Connector

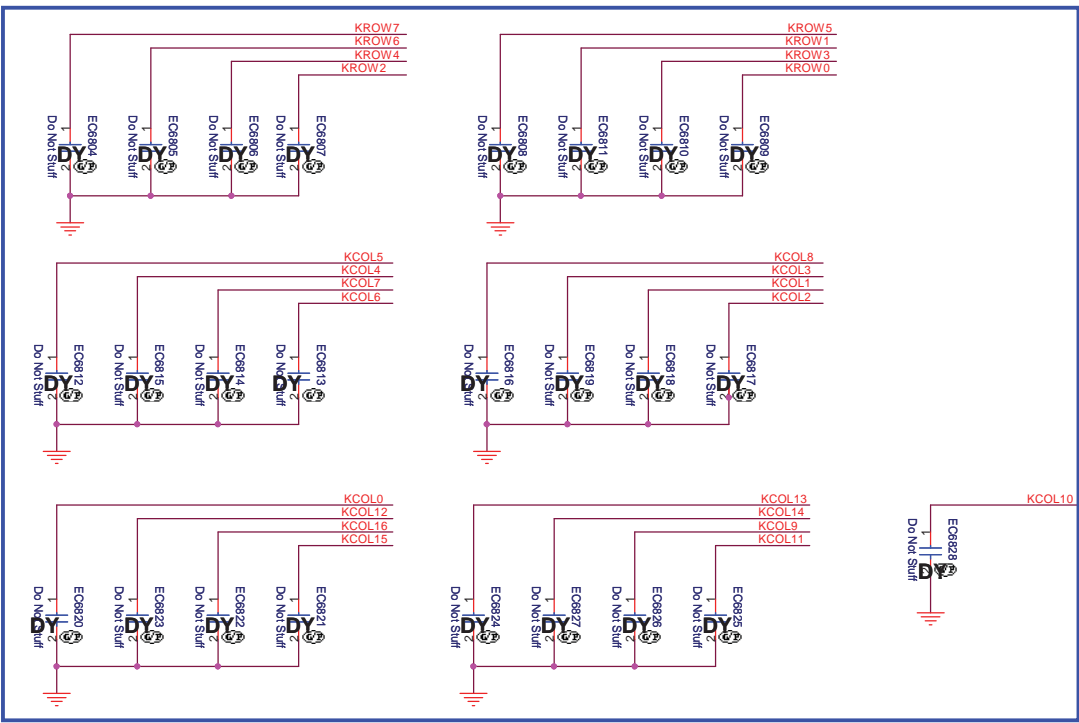


SSID = Touch.Pad

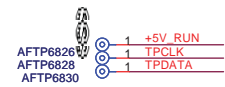
0302



0304



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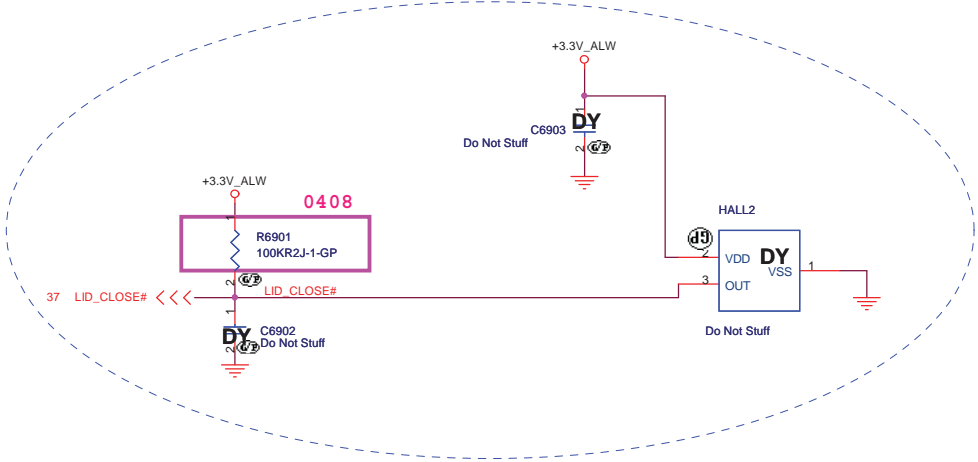
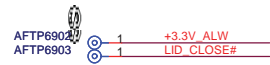
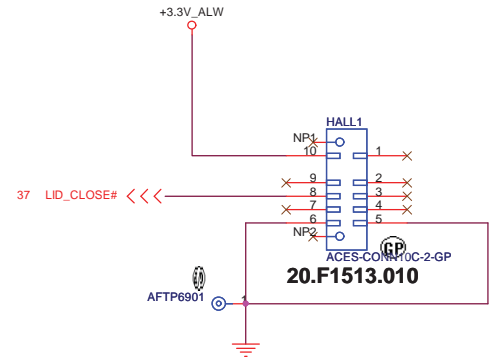
3 DJ2 AMD UMA (10 100 w HDMI)

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Key Board/Touch Pad**

Size A3	Document Number Chelsea DJ2 AMD UMA	Rev X01
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SSID = User. Interface



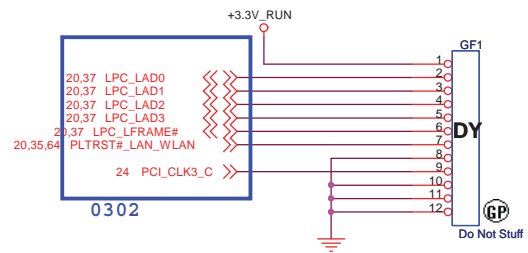
<http://hobi-elektronika.net>

3 DJ2 AMD UMA (10 100 w HDMI)

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Hall Sensor**

Size: A3	Document Number: Chelsea DJ2 AMD UMA	Rev: X01
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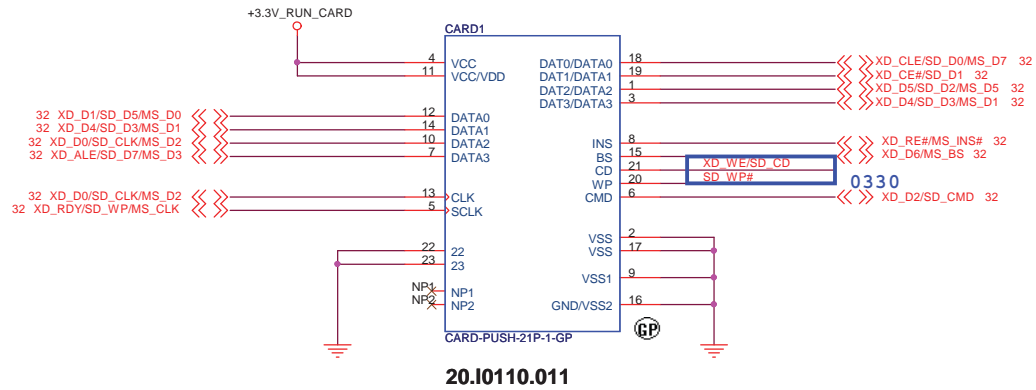
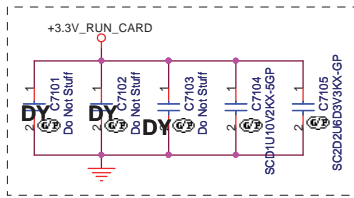
<http://hobi-elektronika.net>

3 DJ2 AMD UMA (10 100 w HDMI)

DELL		Wistron Corporation	
		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
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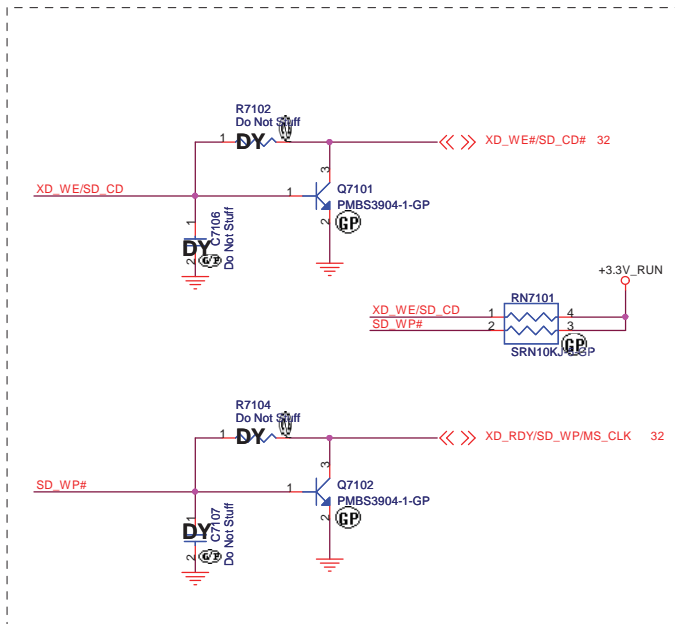
SSID = SDIO

SD/XD/MS Card Reader



20.I0110.011

For reverse card connector 0330



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3 DJ2 AMD UMA (10 100 w HDMI)



Title CARD Reader Connector		
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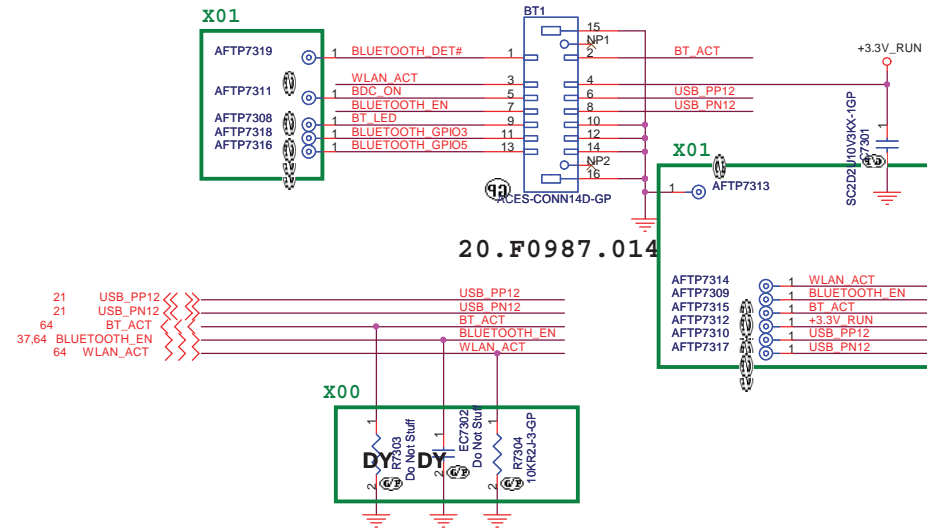
3 DJ2 AMD UMA (10 100 w HDMI)



Title		
RESERVED		
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SSID = User.Interface

Bluetooth Module conn.



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3 DJ2 AMD UMA (10 100 w HDMI)



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Bluetooth		
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3 DJ2 AMD UMA (10 100 w HDMI)



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3 DJ2 AMD UMA (10 100 w HDMI)



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IO Board Connector		
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Reserved		
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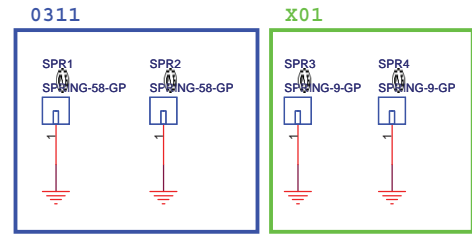
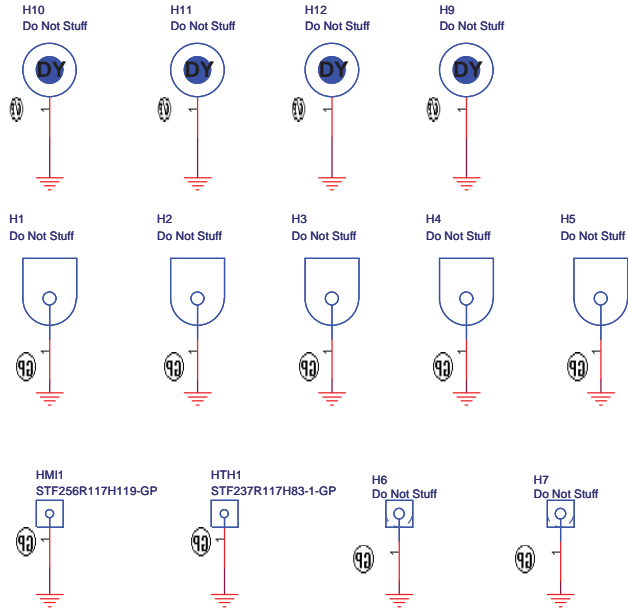
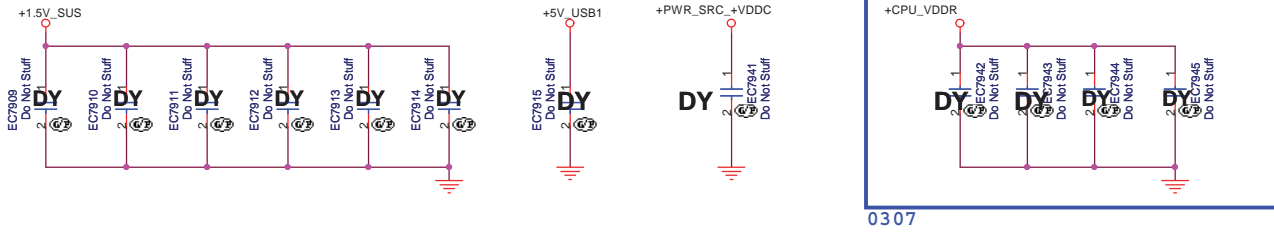
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3 DJ2 AMD UMA (10 100 w HDMI)



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EMI Request



3 DJ2 AMD UMA (10 100 w HDMI)

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: **UNUSED PARTS/EMI Capacitors**

Size: A3	Document Number: Chelsea DJ2 AMD UMA	Rev: X01
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3 DJ2 AMD UMA (10 100 w HDMI)

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
VGA PCIE(1/4)		
Size	Document Number	Rev
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3 DJ2 AMD UMA (10 100 w HDMI)

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		VGA LVDS/TV/CRT(2/4)	
Size	Document Number	Rev	
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Title		VGA POWER/GND(3/4)	
Size	Document Number	Rev	
A3	Chelsea DJ2 AMD UMA	X01	
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3 DJ2 AMD UMA (10 100 w HDMI)

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
VGA MEMORY/STRAPS(4/4)			
Size	Document Number	Rev	
A3	Chelsea DJ2 AMD UMA	X01	
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3 DJ2 AMD UMA (10 100 w HDMI)

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
GPU-VRAM (1/2)		
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Title		
GPU-VRAM (2/2)		
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3 DJ2 AMD UMA (10 100 w HDMI)

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
TPS51117 +VCC GFXCORE		
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3 DJ2 AMD UMA (10 100 w HDMI)

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
APL5930 +1.1V RUN		
Size	Document Number	Rev
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3 DJ2 AMD UMA (10 100 w HDMI)

DELL **Wistron Corporation**
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **Reserved**


Size A3 Document Number **Chelsea DJ2 AMD UMA** Rev **X01**

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DATE	VERSION	ITEM	PAGE	Modify List	Issue Description	OWNER
		1	37	pop R3729 , depop R3733	MB version	EE
		2	37	DY R3712	compare DJ1 and DJ2 (for battery)	EE
		3	71	add R7101-R7104; C7106-C7107; Q7101-Q7102	For reversal cardreader connector	EE
		4	69	pop R6901	For lid_close# PU when Hall sensor BD not connect	EE
		5	70	depop GF1	non-pop debug port	EE
		6	42	C4203 from 100pF to 4.7nF	For sequence	EE
		7	61	reserve U6103, U5104, U6105	For LAN Surge	EE
		8	47	PR4720 change to 95.3Kohm(64.95325.6DL). PR4721 change to 22Kohm(64.22025.6DL).	For CPU_CORE OCP	EE
		9	20	RN2006 from 0R to 10R	For CLK_LAN slew rate fail	EE
		10	55	C5508-C5510 from 8.2pF to 10pF L5501-L5503 change to 33 ohm bead	For EMI request	EMI
		11	79	add SPR3 and SPR4	For EMI request	EMI
		12	63 21	add C6307-C6312 ; C2106-C2107 4.7pF	Fine tune USB signal	EE

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3 DJ2 AMD UMA (10 100 w HDMI)




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Title: **Change History**

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DATE	VERSION	ITEM	PAGE	Modify List	Issue Description	OWNER

3 DJ2 AMD UMA (10 100 w HDMI)

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Change History			
Size	Document Number		Rev
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