

FM9 XXXX Intel Discrete GFX

VER : 1A

PWA:

PWB:

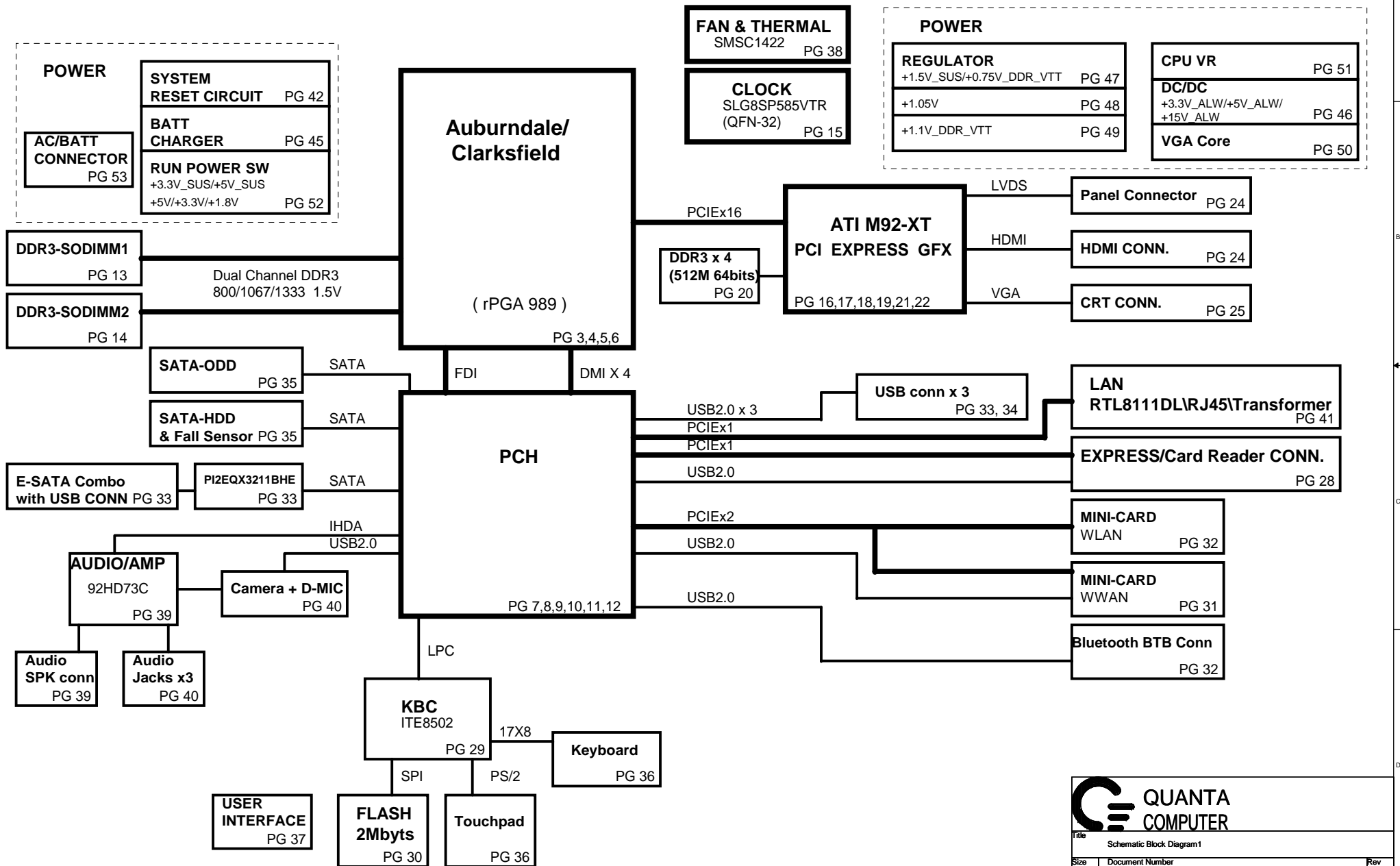








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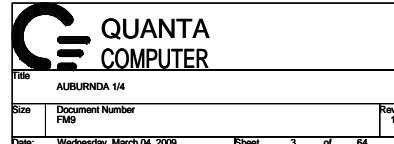
Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	24,30,45,46,47,48,49,50,51	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	08,11,29,30	RTC		S0~S5
+3.3V_ALW	+3.3V	08,29,30,35,36,37,42,44,45,46,47,52,53	8051 POWER	ALWON	S0~S5
+5V_ALW2	+5V	37,46,53	LARGE POWER	RUN_ON	S0~S5
+3.3V_LAN	+3.3V	41	LAN POWER	AUX_ON	
+5V_SUS	+5V	11,33,34,35,37,51,52	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	7,09,10,11,13,14,19,24,26,28,29,37,41,42,44,48,49,50,51,52	SLP_S5# CTRLD POWER	SUS_ON	
+1.5V_SUS	+1.8V	03,05,13,14,47,50,52	SODIMM POWER	SUS_ON	
+0.75V_DDR_VTT	+0.9V	13,14,47,52	SODIMM POWER	RUN_ON	
+5V_RUN	+5V	11,18,24,25,35,36,38,39,40,52	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,7,8,9,10,11,13,14,15,17,24,25,26,28,29,30,31,32,33,35,37,38,39,40,41,42,46,51,52,59	SLP_S3# CTRLD POWER	RUN_ON	
+1.8V_RUN	+1.8V	05,11,26,44,52	SDVO POWER	RUN_ON	
+1.5V_RUN	+1.5V	11,18,19,20,28,31,32,52	CALISTOGA/ICH9 POWER	RUN_ON	
+1.8V_RUN_GFX	+1.25V	17,18,21,22,44,52	VGA POWER	RUN_ON	
+VCC_GFX_CORE	+0.9V~+1.2V	18,21,50	VGA POWER	RUN_ON	
+1.05V_PCH	+1.05V	08,09,11,15,48	CPU/CALISTOGA/ICH8 POWER	1.05V_RUN_ON	
+VCC_CORE	+0.7V~+1.77V	05,51	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	26	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	36	Module Power	MODC_EN	
+5V_HDD	+5V	36	HDD Power	HDDC_EN	
+1.1V_VTT	+1.1V	03,05,10,11,49,59			
+1.1V_GFX_PCIE	+1.1V	18,50			

GND PLANE	PAGE	DESCRIPTION
 GND_CHG	46	
 GND_1.05V	47	
 GND_VGA	50	
 GND_SIGNAL	51	
 AGND_DC/DC	52	
 GND	ALL	

AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)

SC(V1.0),P17:
SKTOCC#
Can be left No Connect
or tied to GND



AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

U34C

M A DQ0 A10 SA_DQ[0]
M A DQ1 C10 SA_DQ[1]
M A DQ2 C7 SA_DQ[2]
M A DQ3 A7 SA_DQ[3]
M A DQ4 B10 SA_DQ[4]
M A DQ5 D10 SA_DQ[5]
M A DQ6 E10 SA_DQ[6]
M A DQ7 A8 SA_DQ[7]
M A DQ8 D8 SA_DQ[8]
M A DQ9 F10 SA_DQ[9]
M A DQ10 E6 SA_DQ[10]
M A DQ11 F7 SA_DQ[11]
M A DQ12 E9 SA_DQ[12]
M A DQ13 B7 SA_DQ[13]
M A DQ14 F7 SA_DQ[14]
M A DQ15 C6 SA_DQ[15]
M A DQ16 H10 SA_DQ[16]
M A DQ17 G8 SA_DQ[17]
M A DQ18 K7 SA_DQ[18]
M A DQ19 J8 SA_DQ[19]
M A DQ20 G7 SA_DQ[20]
M A DQ21 G10 SA_DQ[21]
M A DQ22 J7 SA_DQ[22]
M A DQ23 J10 SA_DQ[23]
M A DQ24 L7 SA_DQ[24]
M A DQ25 M8 SA_DQ[25]
M A DQ26 M8 SA_DQ[26]
M A DQ27 L9 SA_DQ[27]
M A DQ28 L6 SA_DQ[28]
M A DQ29 K8 SA_DQ[29]
M A DQ30 N8 SA_DQ[30]
M A DQ31 P9 SA_DQ[31]
M A DQ32 AH5 SA_DQ[32]
M A DQ33 AF5 SA_DQ[33]
M A DQ34 AK6 SA_DQ[34]
M A DQ35 AK7 SA_DQ[35]
M A DQ36 A6 SA_DQ[36]
M A DQ37 AG5 SA_DQ[37]
M A DQ38 AJ7 SA_DQ[38]
M A DQ39 AJ6 SA_DQ[39]
M A DQ40 AJ10 SA_DQ[40]
M A DQ41 AJ8 SA_DQ[41]
M A DQ42 AK10 SA_DQ[42]
M A DQ43 AK12 SA_DQ[43]
M A DQ44 AK8 SA_DQ[44]
M A DQ45 AL7 SA_DQ[45]
M A DQ46 AK11 SA_DQ[46]
M A DQ47 AL8 SA_DQ[47]
M A DQ48 AM6 SA_DQ[48]
M A DQ49 AM10 SA_DQ[49]
M A DQ50 AR11 SA_DQ[50]
M A DQ51 AL11 SA_DQ[51]
M A DQ52 AM9 SA_DQ[52]
M A DQ53 AN9 SA_DQ[53]
M A DQ54 AT11 SA_DQ[54]
M A DQ55 AP12 SA_DQ[55]
M A DQ56 AM12 SA_DQ[56]
M A DQ57 AN12 SA_DQ[57]
M A DQ58 AM13 SA_DQ[58]
M A DQ59 AT14 SA_DQ[59]
M A DQ60 AT12 SA_DQ[60]
M A DQ61 AL13 SA_DQ[61]
M A DQ62 AR14 SA_DQ[62]
M A DQ63 AP14 SA_DQ[63]

DDR SYSTEM MEMORY A

Clarksfield/Auburndale

Channel A DQ[15,32,48,54], DM[5]
Requires minimum 12mils spacing
with all other signals, including data signals.

SA_CLK[0] AA6 M_A_CLK0 13
SA_CLK[0] AA7 M_A_CLK0# 13
SA_CKE[0] P7 M_A_CKE0 13

SA_CLK[1] Y6 M_A_CLK1 13
SA_CLK[1] Y5 M_A_CLK1# 13
SA_CKE[1] P6 M_A_CKE1 13

SA_CS#[0] AE2 M_A_CS0# 13
SA_CS#[1] AE8 M_A_CS1# 13

SA_ODT[0] AD8 M_A_ODT0 13
SA_ODT[1] AF9 M_A_ODT1 13

SA_DM[0] B9 M_A_DM0 M_A_DM[7:0] 13
SA_DM[1] D7 M_A_DM1
SA_DM[2] H7 M_A_DM2
SA_DM[3] M7 M_A_DM3
SA_DM[4] AG6 M_A_DM4
SA_DM[5] AM7 M_A_DM5
SA_DM[6] AN10 M_A_DM6
SA_DM[7] AN13 M_A_DM7

SA_DQS#[0] C9 M_A_DQS#0 M_A_DQS[7:0] 13
SA_DQS#[1] F8 M_A_DQS#1
SA_DQS#[2] J8 M_A_DQS#2
SA_DQS#[3] N9 M_A_DQS#3
SA_DQS#[4] AH7 M_A_DQS#4
SA_DQS#[5] AK9 M_A_DQS#5
SA_DQS#[6] AP11 M_A_DQS#6
SA_DQS#[7] AT13 M_A_DQS#7

SA_DQS[0] C8 M_A_DQS0 M_A_DQS[7:0] 13
SA_DQS[1] F9 M_A_DQS1
SA_DQS[2] H9 M_A_DQS2
SA_DQS[3] M9 M_A_DQS3
SA_DQS[4] AH8 M_A_DQS4
SA_DQS[5] AK10 M_A_DQS5
SA_DQS[6] AN11 M_A_DQS6
SA_DQS[7] AR13 M_A_DQS7

SA_MA[0] Y3 M_A_A0 M_A_A[15:0] 13
SA_MA[1] W1 M_A_A1
SA_MA[2] AA8 M_A_A2
SA_MA[3] AA3 M_A_A3
SA_MA[4] V1 M_A_A4
SA_MA[5] AA9 M_A_A5
SA_MA[6] T1 M_A_A6
SA_MA[7] Y9 M_A_A7
SA_MA[8] U6 M_A_A8
SA_MA[9] U6 M_A_A9
SA_MA[10] AD4 M_A_A10
SA_MA[11] T2 M_A_A11
SA_MA[12] U8 M_A_A12
SA_MA[13] T3 M_A_A13
SA_MA[14] T3 M_A_A14
SA_MA[15] V9 M_A_A15

13 M_A_BS0 AC3 SA_BS[0]
13 M_A_BS1 AB2 SA_BS[1]
13 M_A_BS2 U7 SA_BS[2]

13 M_A_CAS# AE1 SA_CAS#
13 M_A_RAS# AB3 SA_RAS#
13 M_A_WE# AE8 SA_WE#

U34D

M B DQ0 B5 SB_DQ[0]
M B DQ1 A5 SB_DQ[1]
M B DQ2 C3 SB_DQ[2]
M B DQ3 B3 SB_DQ[3]
M B DQ4 E4 SB_DQ[4]
M B DQ5 A6 SB_DQ[5]
M B DQ6 A4 SB_DQ[6]
M B DQ7 C4 SB_DQ[7]
M B DQ8 D1 SB_DQ[8]
M B DQ9 D2 SB_DQ[9]
M B DQ10 F2 SB_DQ[10]
M B DQ11 F1 SB_DQ[11]
M B DQ12 C2 SB_DQ[12]
M B DQ13 F5 SB_DQ[13]
M B DQ14 F3 SB_DQ[14]
M B DQ15 G4 SB_DQ[15]
M B DQ16 H6 SB_DQ[16]
M B DQ17 G2 SB_DQ[17]
M B DQ18 J6 SB_DQ[18]
M B DQ19 J3 SB_DQ[19]
M B DQ20 G1 SB_DQ[20]
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M B DQ27 M1 SB_DQ[27]
M B DQ28 K5 SB_DQ[28]
M B DQ29 K4 SB_DQ[29]
M B DQ30 M4 SB_DQ[30]
M B DQ31 N5 SB_DQ[31]
M B DQ32 AE3 SB_DQ[32]
M B DQ33 AE1 SB_DQ[33]
M B DQ34 AJ3 SB_DQ[34]
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M B DQ50 AT4 SB_DQ[50]
M B DQ51 AN6 SB_DQ[51]
M B DQ52 AN4 SB_DQ[52]
M B DQ53 AN3 SB_DQ[53]
M B DQ54 AT5 SB_DQ[54]
M B DQ55 AT6 SB_DQ[55]
M B DQ56 AN7 SB_DQ[56]
M B DQ57 AP6 SB_DQ[57]
M B DQ58 AP8 SB_DQ[58]
M B DQ59 AT9 SB_DQ[59]
M B DQ60 AT7 SB_DQ[60]
M B DQ61 AP9 SB_DQ[61]
M B DQ62 AR10 SB_DQ[62]
M B DQ63 AR10 SB_DQ[63]

DDR SYSTEM MEMORY - B

Clarksfield/Auburndale

Channel B DQ[16,18,36,42,56,57,60,61,62]
Requires minimum 12mils spacing
with all other signals, including data signals.

SB_CLK[0] W8 M_B_CLK0 14
SB_CLK[0] W9 M_B_CLK0# 14
SB_CKE[0] M3 M_B_CKE0 14

SB_CLK[1] V7 M_B_CLK1 14
SB_CLK[1] V6 M_B_CLK1# 14
SB_CKE[1] M2 M_B_CKE1 14

SB_CS#[0] AB8 M_B_CS0# 14
SB_CS#[1] AD6 M_B_CS1# 14

SB_ODT[0] AC7 M_B_ODT0 14
SB_ODT[1] AD1 M_B_ODT1 14

SB_DM[0] D4 M_B_DM0 M_B_DM[7:0] 14
SB_DM[1] E1 M_B_DM1
SB_DM[2] H3 M_B_DM2
SB_DM[3] K1 M_B_DM3
SB_DM[4] AH1 M_B_DM4
SB_DM[5] AL2 M_B_DM5
SB_DM[6] AR4 M_B_DM6
SB_DM[7] AT8 M_B_DM7

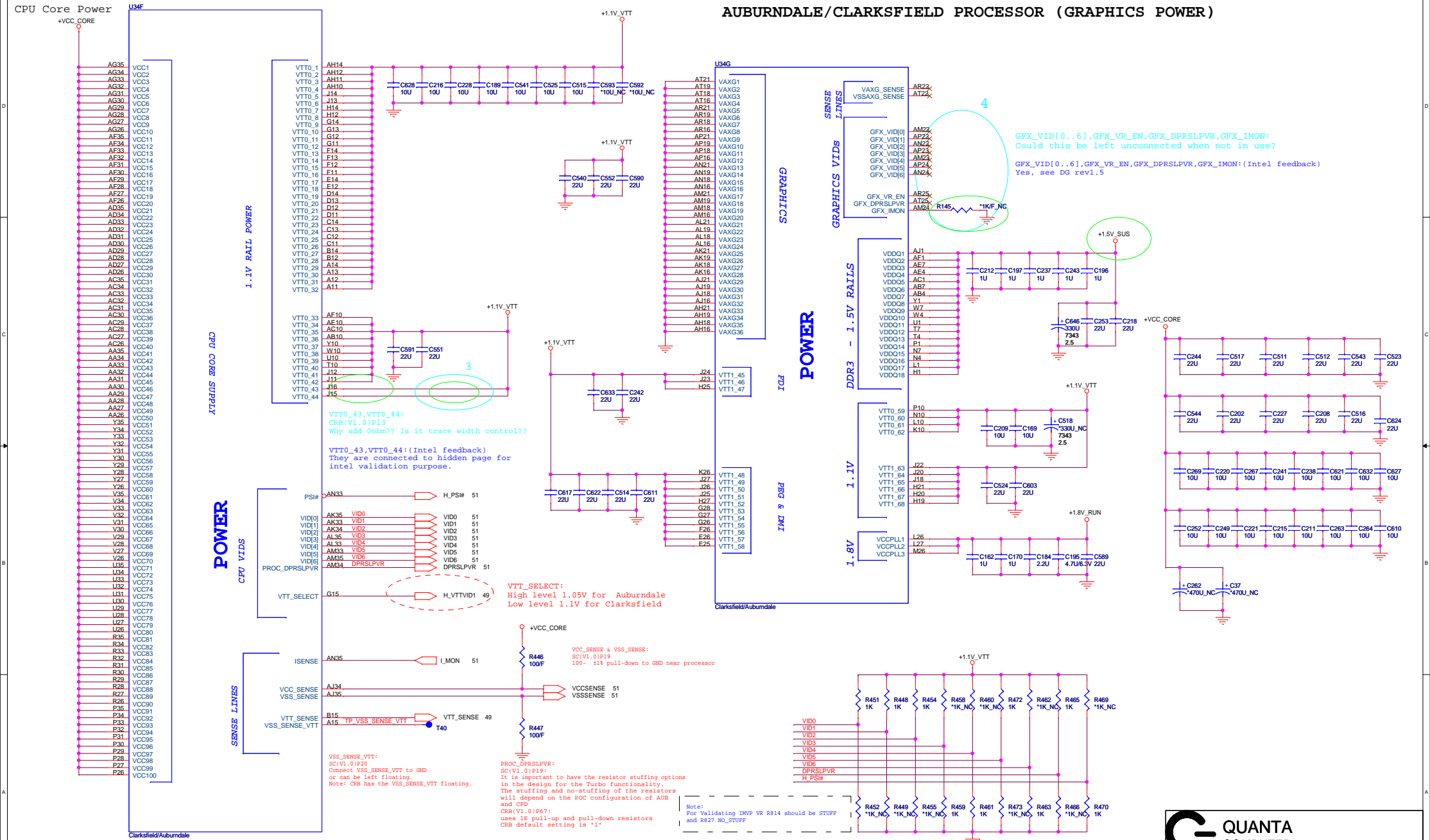
SB_DQS#[0] D5 M_B_DQS#0 M_B_DQS[7:0] 14
SB_DQS#[1] E4 M_B_DQS#1
SB_DQS#[2] L4 M_B_DQS#2
SB_DQS#[3] L4 M_B_DQS#3
SB_DQS#[4] AH2 M_B_DQS#4
SB_DQS#[5] AL4 M_B_DQS#5
SB_DQS#[6] AR5 M_B_DQS#6
SB_DQS#[7] AR8 M_B_DQS#7

SB_DQS[0] C5 M_B_DQS0 M_B_DQS[7:0] 14
SB_DQS[1] E3 M_B_DQS1
SB_DQS[2] H4 M_B_DQS2
SB_DQS[3] M5 M_B_DQS3
SB_DQS[4] AG2 M_B_DQS4
SB_DQS[5] AL5 M_B_DQS5
SB_DQS[6] AP5 M_B_DQS6
SB_DQS[7] AR7 M_B_DQS7

SB_MA[0] U5 M_B_A0 M_B_A[15:0] 14
SB_MA[1] V2 M_B_A1
SB_MA[2] T5 M_B_A2
SB_MA[3] V3 M_B_A3
SB_MA[4] R1 M_B_A4
SB_MA[5] T8 M_B_A5
SB_MA[6] R2 M_B_A6
SB_MA[7] R6 M_B_A7
SB_MA[8] R4 M_B_A8
SB_MA[9] R5 M_B_A9
SB_MA[10] AB5 M_B_A10
SB_MA[11] P3 M_B_A11
SB_MA[12] R3 M_B_A12
SB_MA[13] AF7 M_B_A13
SB_MA[14] P5 M_B_A14
SB_MA[15] N1 M_B_A15

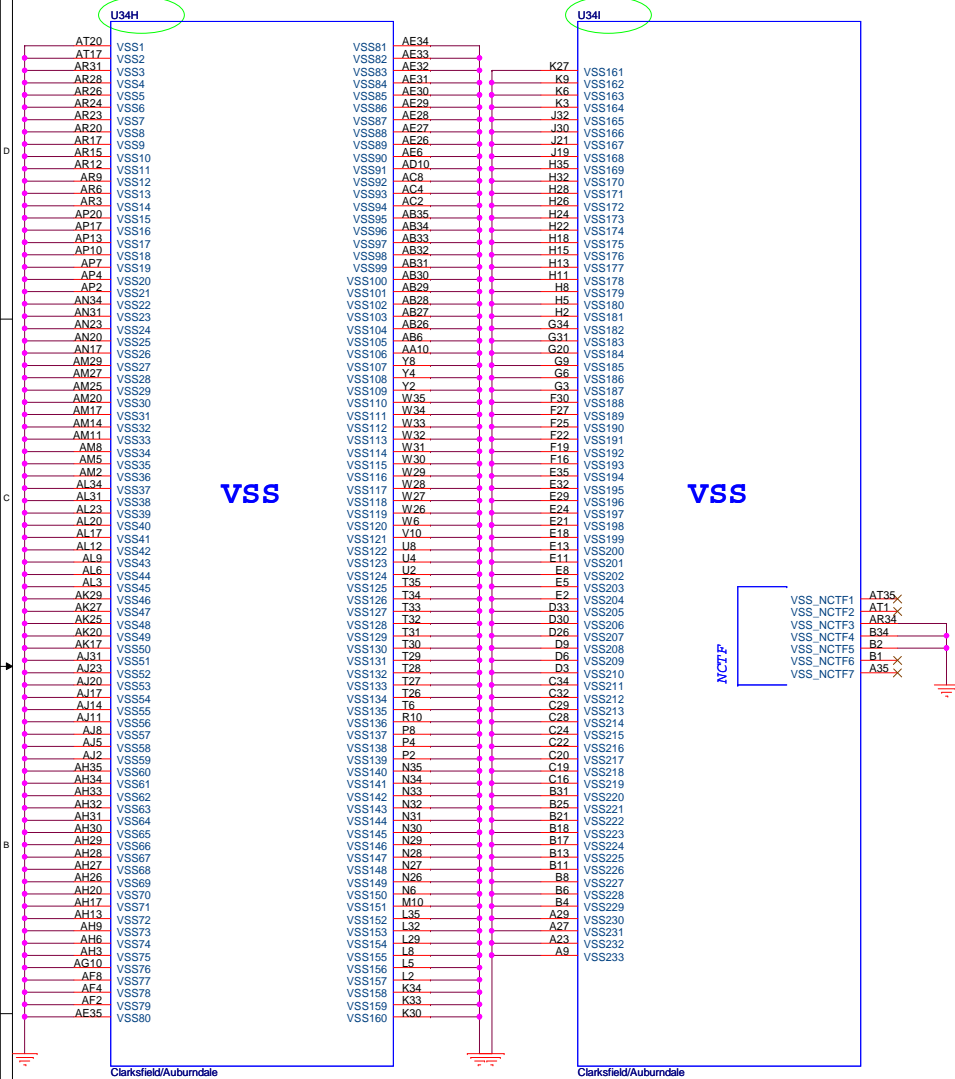


AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)

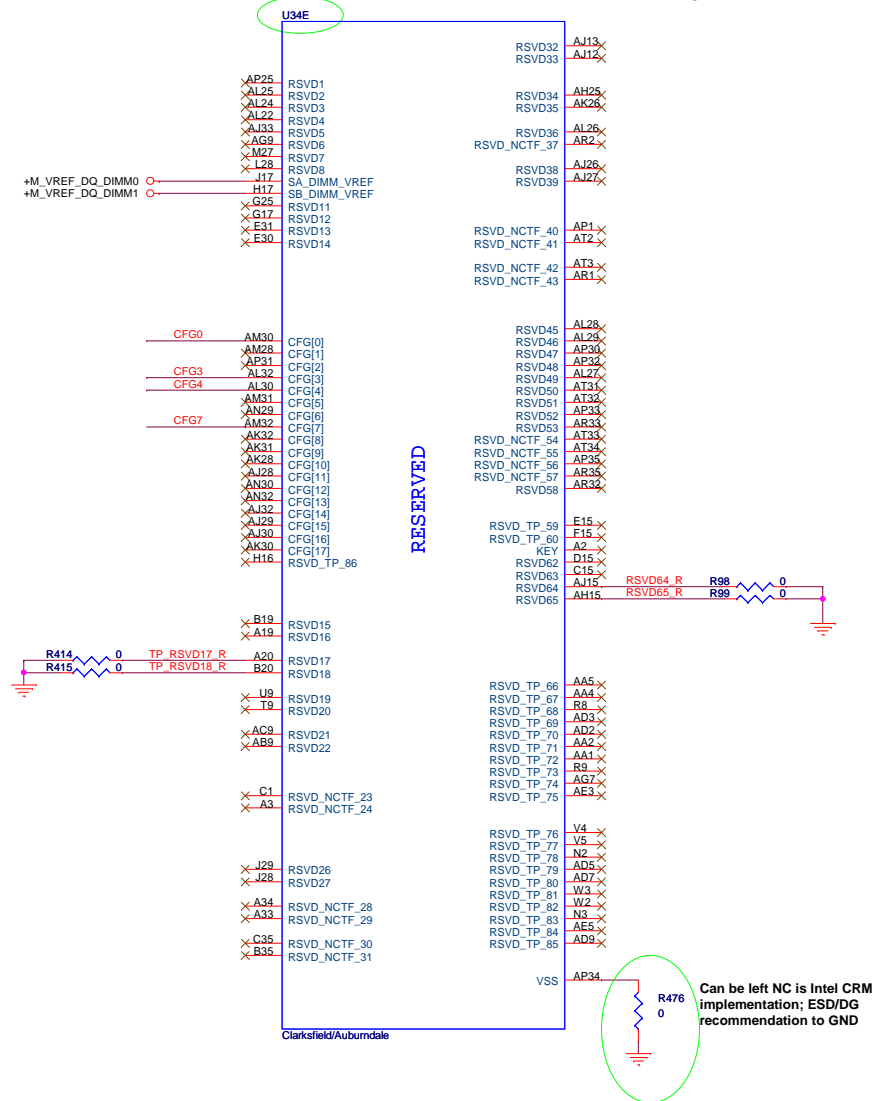


AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)

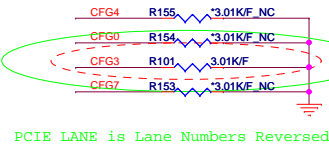
AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR (RESERVED, CFG)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.



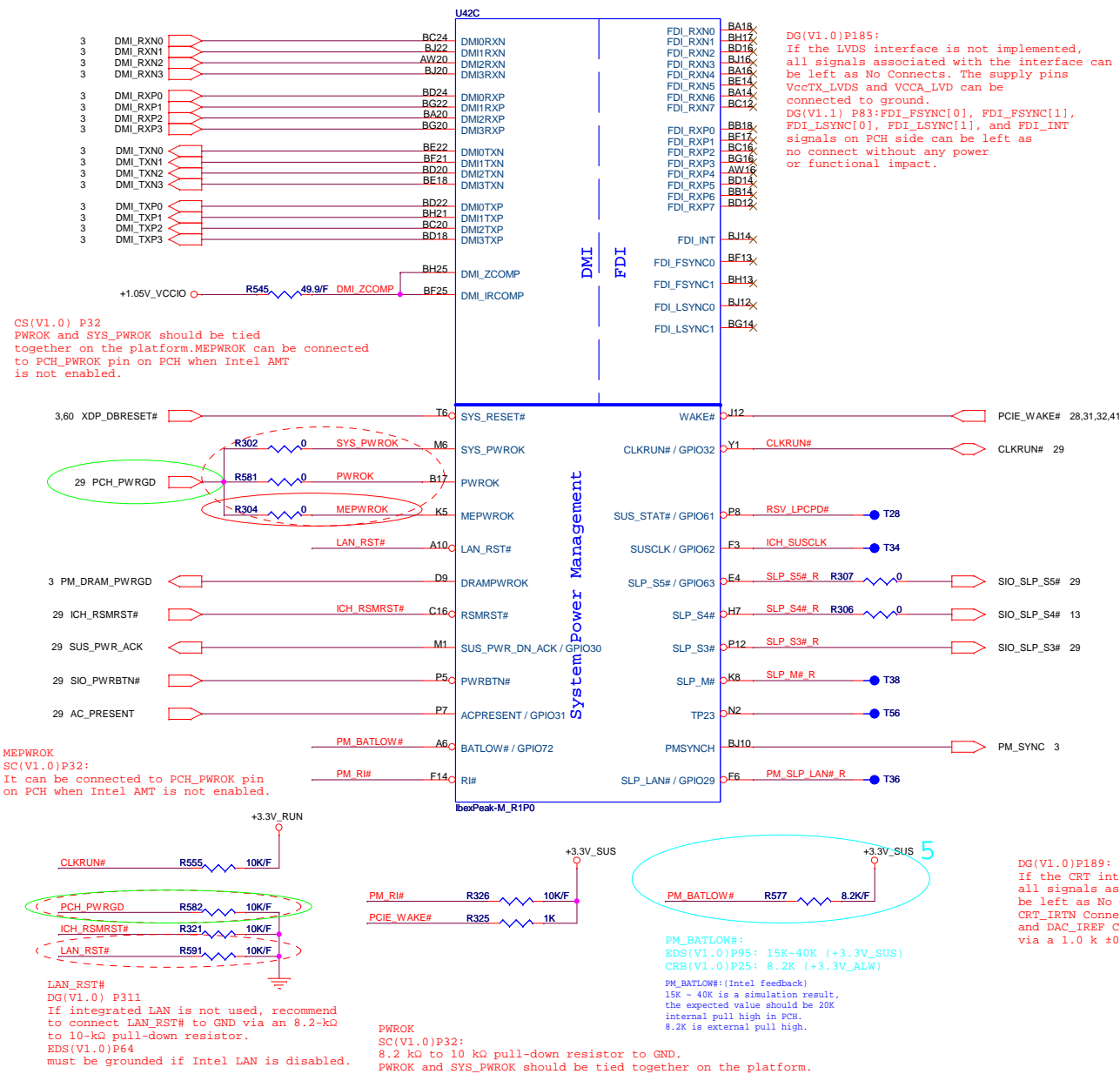
PCIE LANE is Lane Numbers Reversed

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

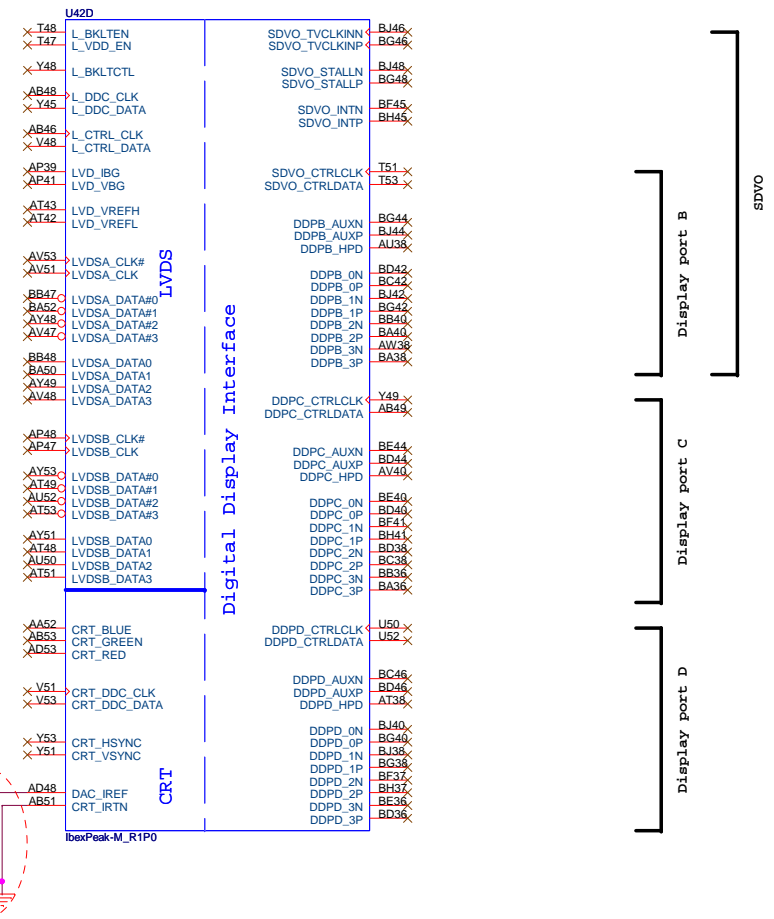


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IBEX PEAK-M (DMI,FDI,GPIO)



IBEX PEAK-M (LVDS,DDI)



DG(V1.0)P189:
If the CRT interface is not implemented,
all signals associated with the interface can
be left as No Connects. The pins
CRT_IRTN Connect this signals to GND
and DAC_IREF Connect to GND
via a 1.0 k $\pm 0.5\%$ pull-down resistor



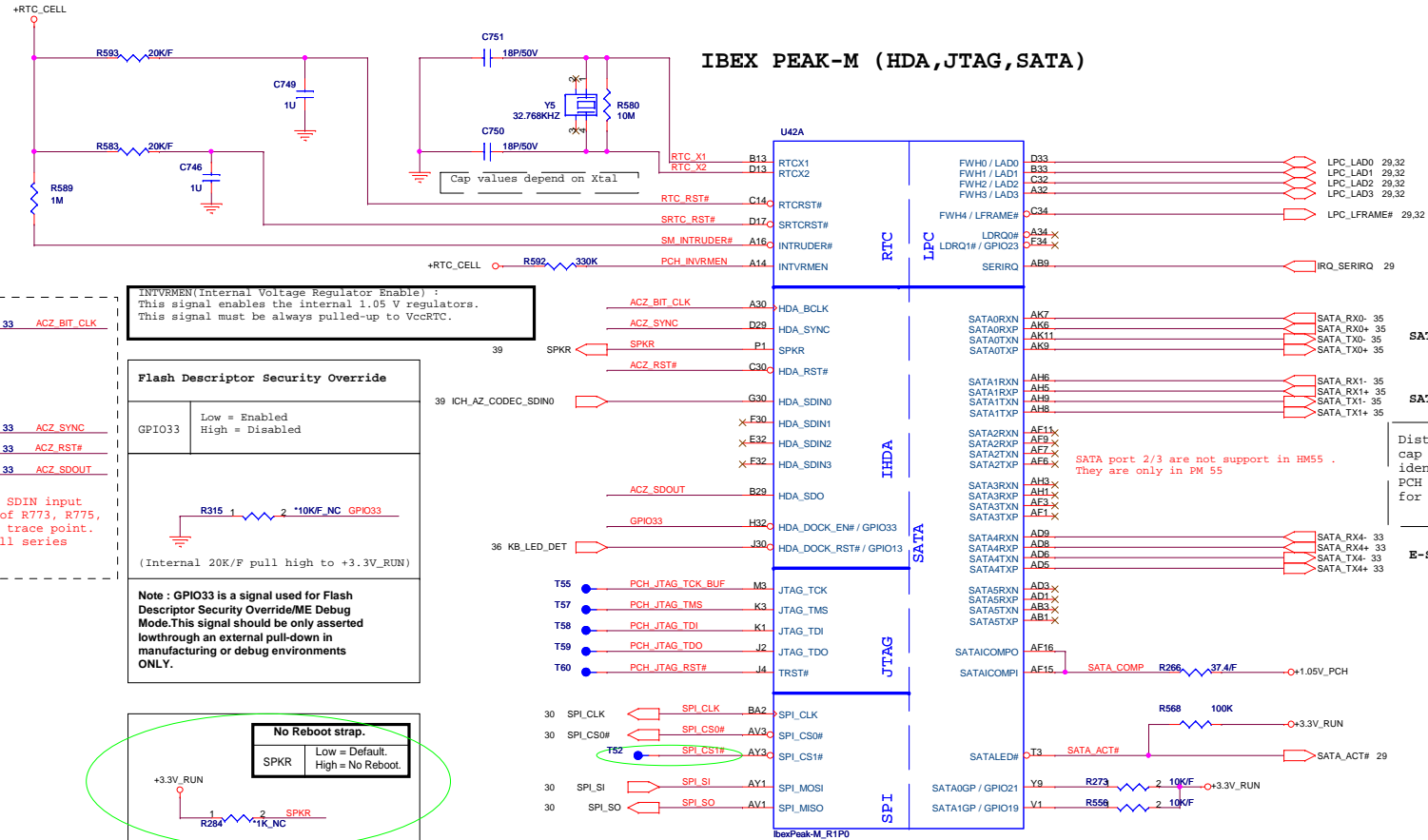
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IBEX PEAK-M (HDA,JTAG,SATA)



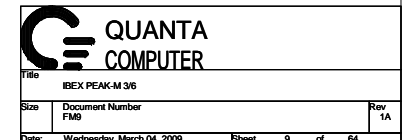
IBEX PEAK-M 1/6

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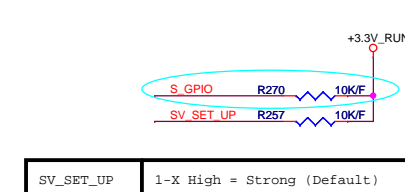
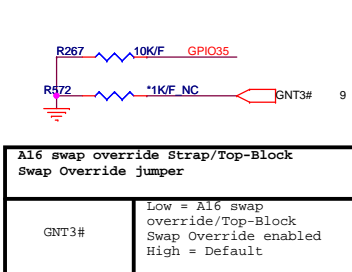
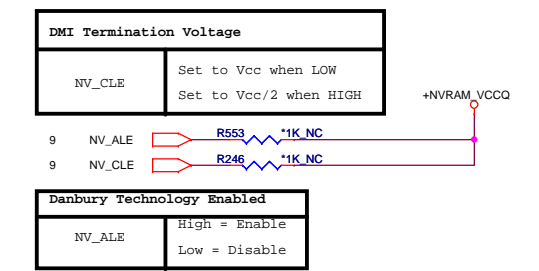
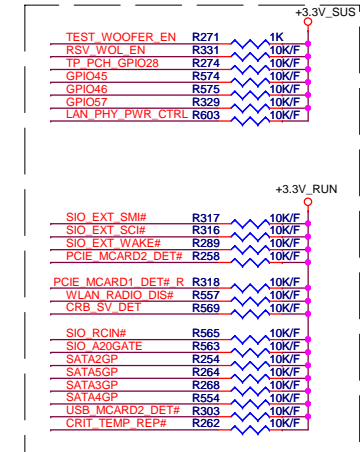
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IBEX PEAK-M (PCI-E, SMBUS, CLK)

U42B



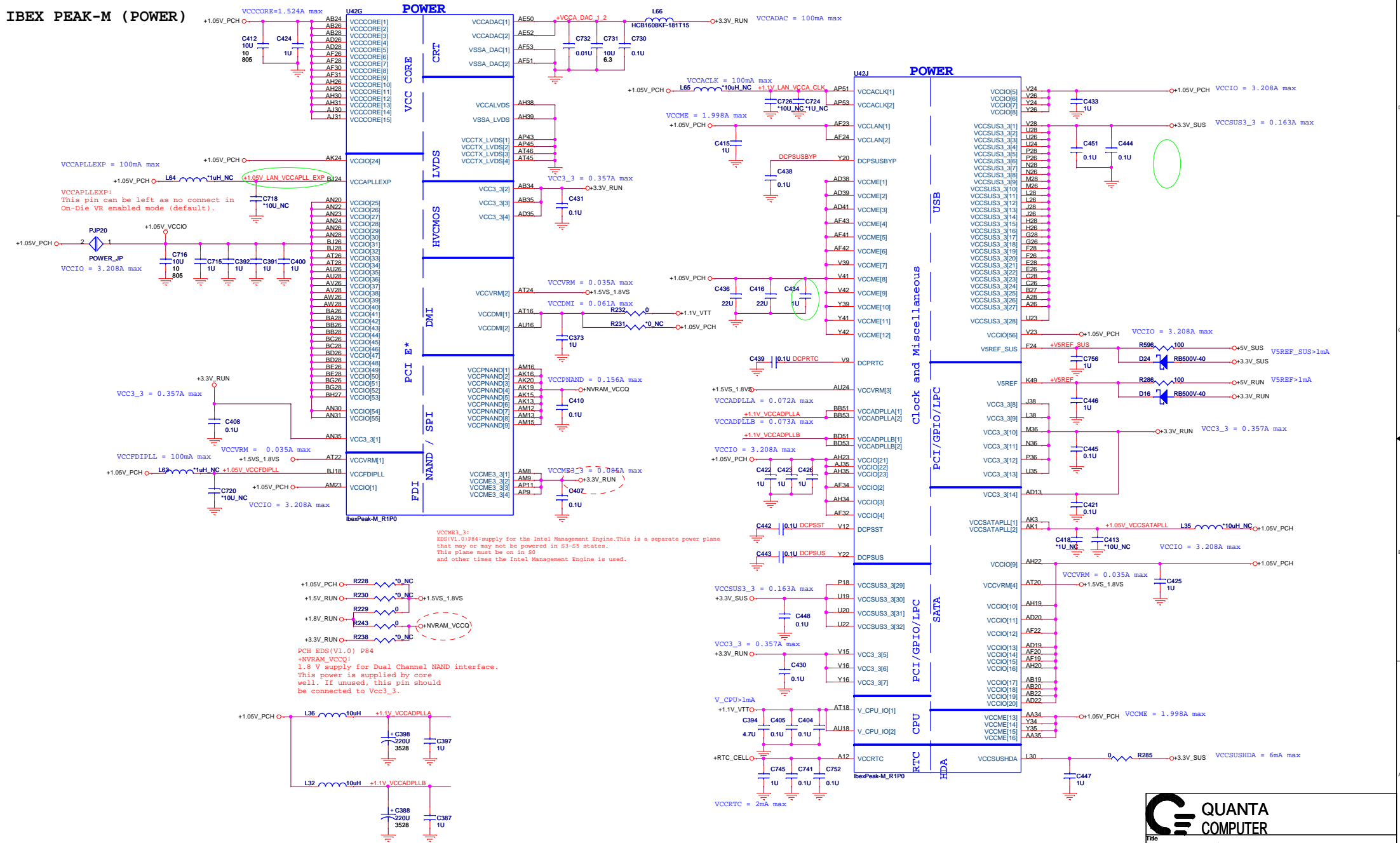
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



BMBUS#:
If not used, require a weak pull-up (8.2- 10 kΩ) to Vcc3.3.
CRB(V1.0)P28: it has 1K PU and 100 ohm on this net for validation purpose.

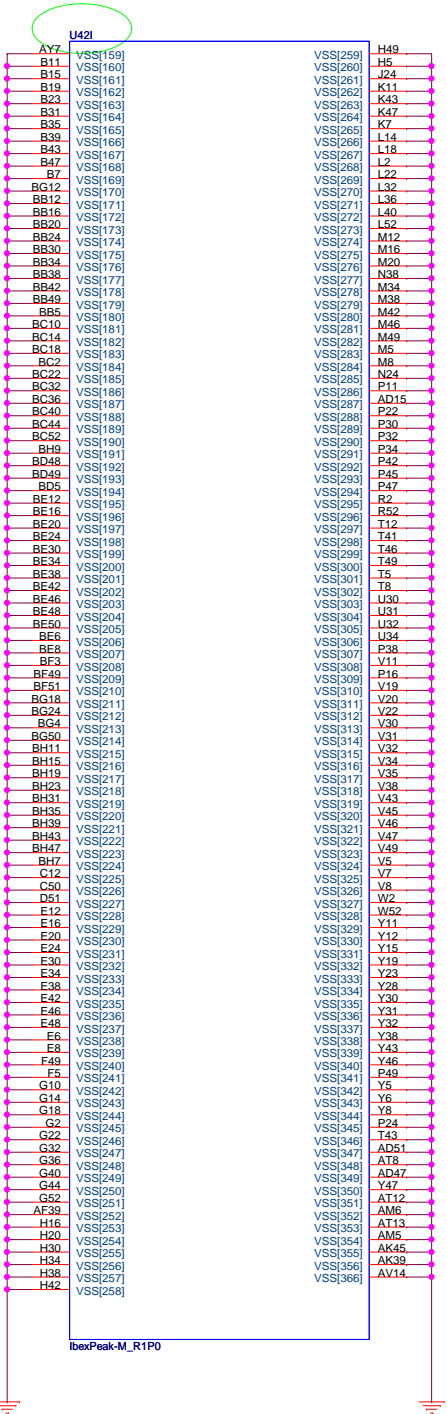
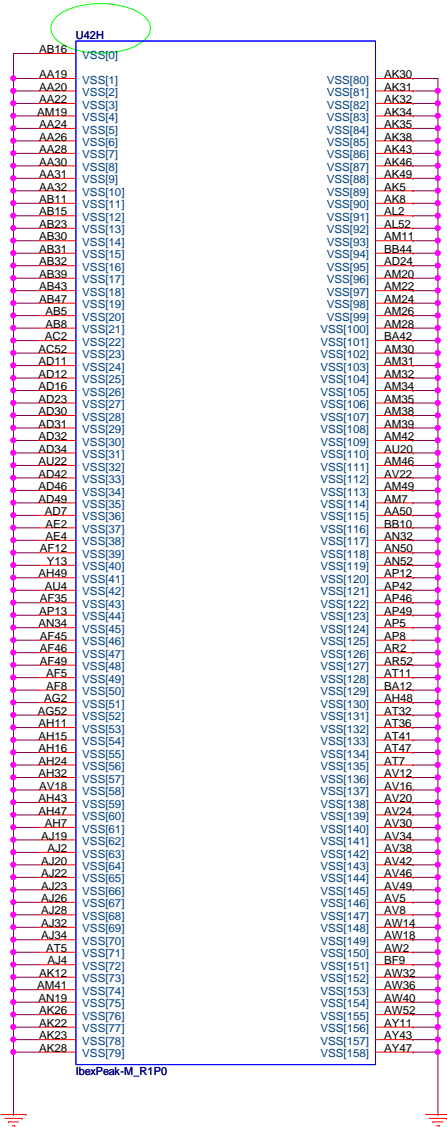
BMBUS#:(Intel feedback)
Follow CRB checklist, 1K is for intel BIOS validation purpose.

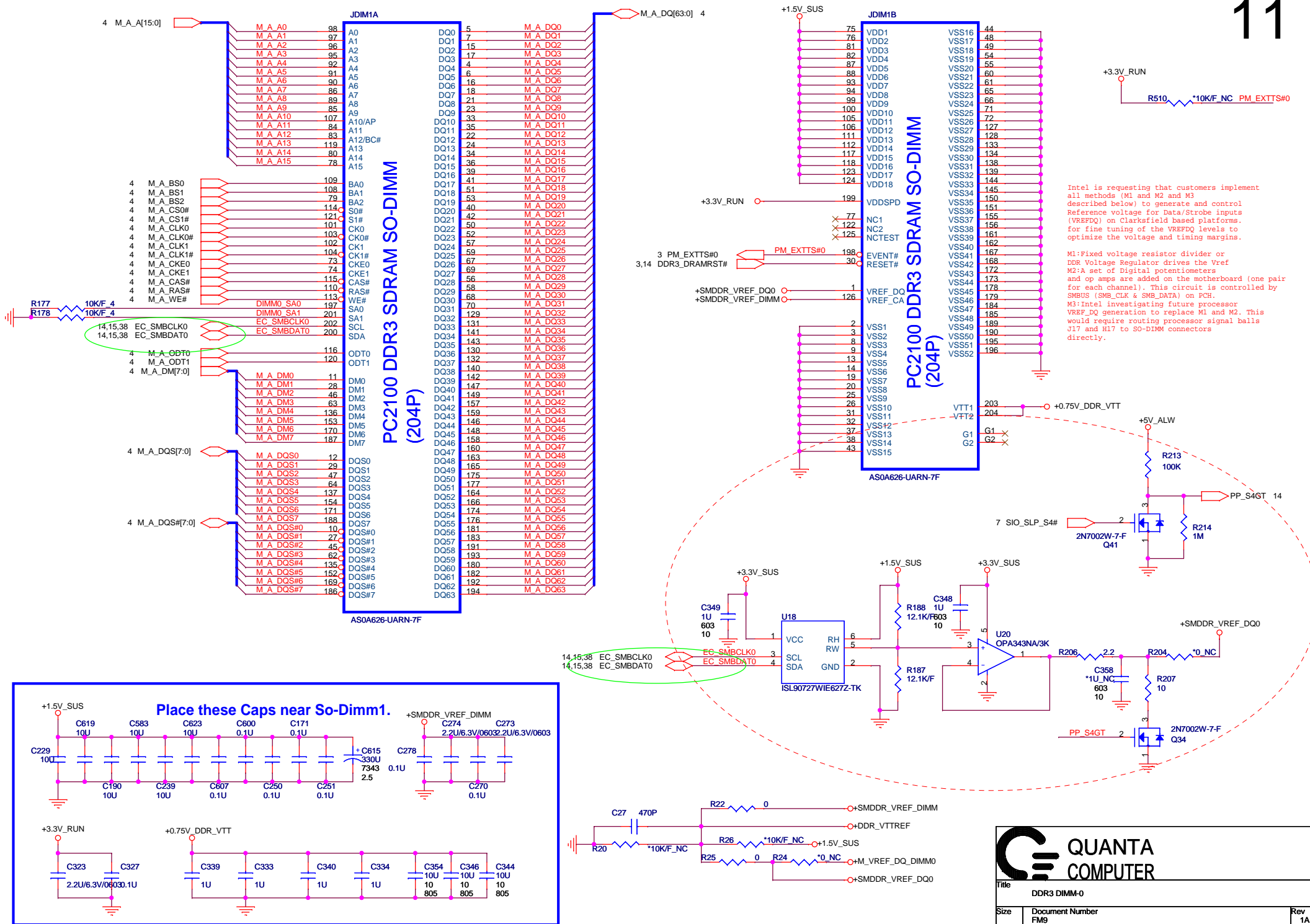
IBEX PEAK-M (POWER)

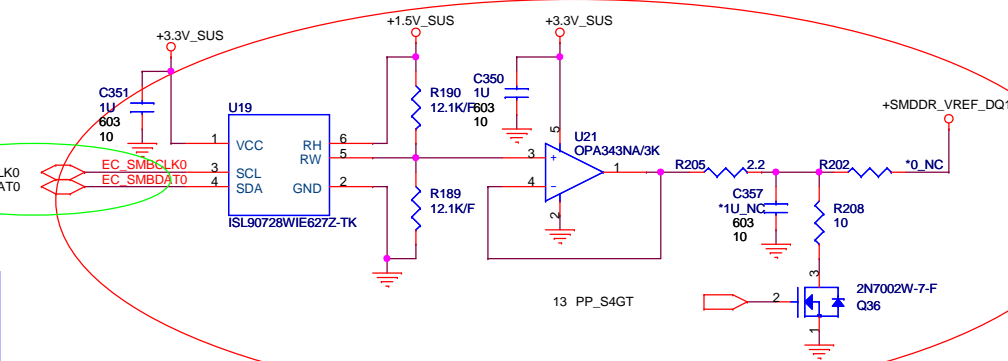
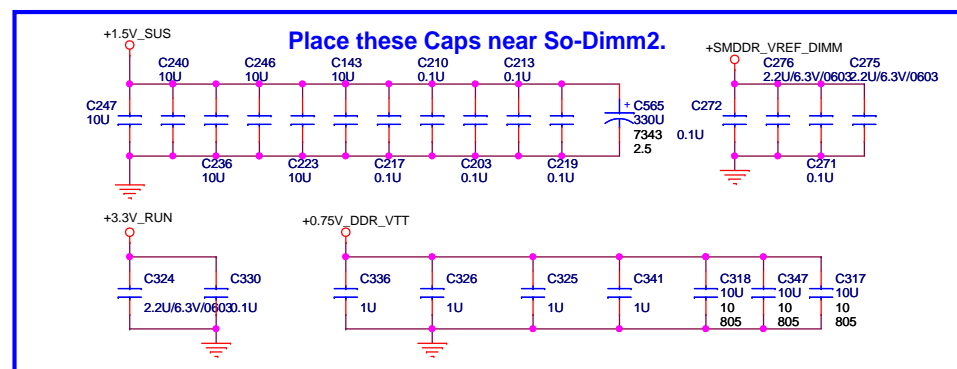
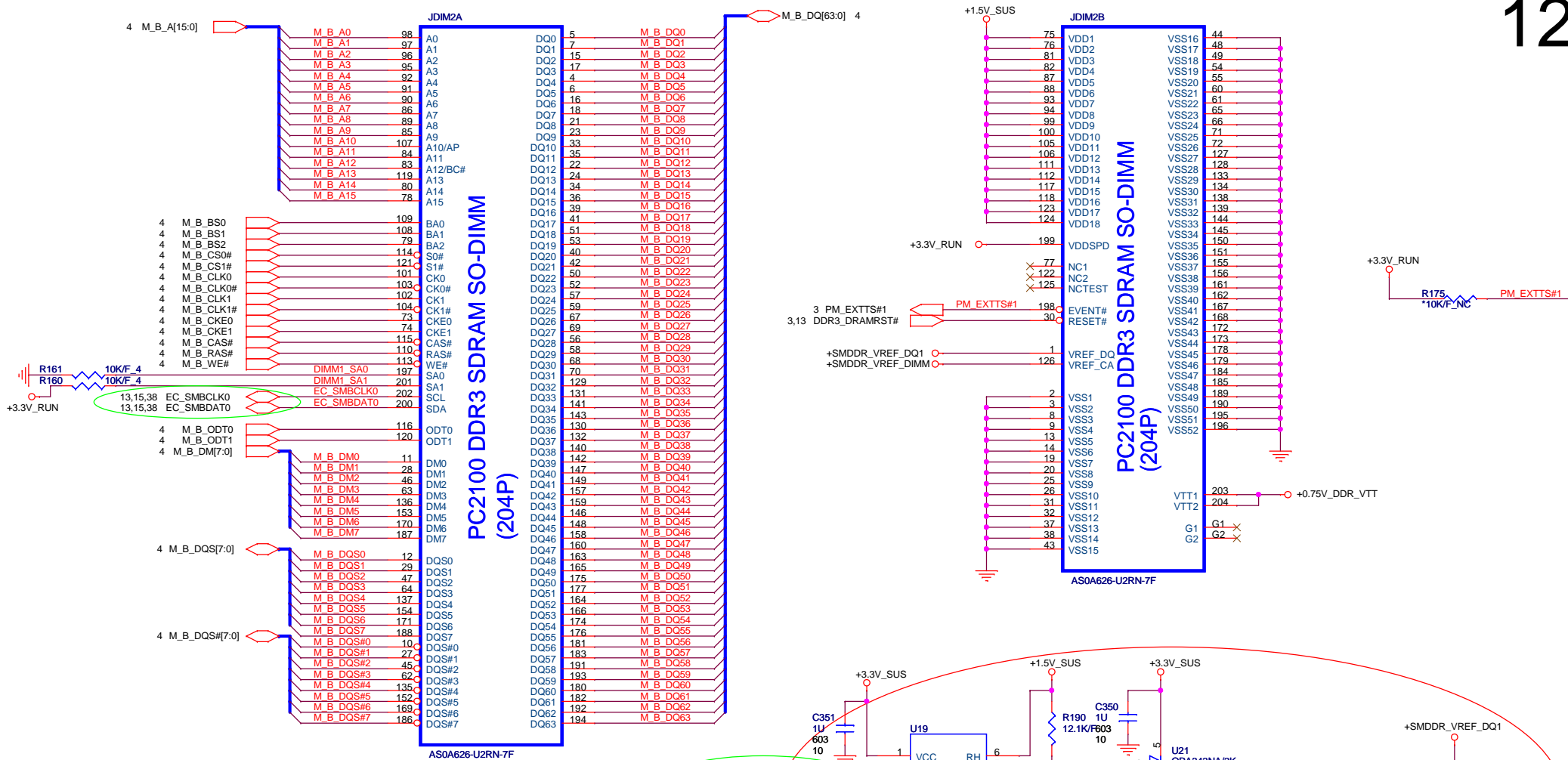


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IBEX PEAK-M 5/6			
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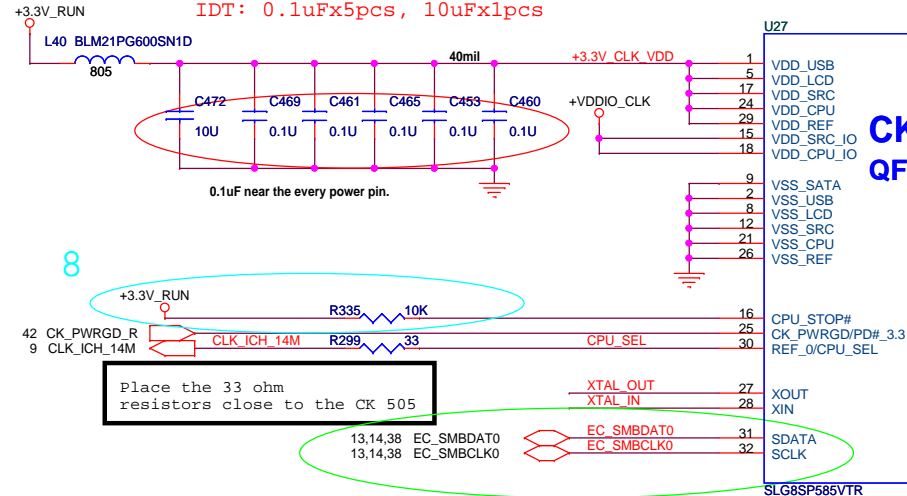
IBEX PEAK-M (GND)



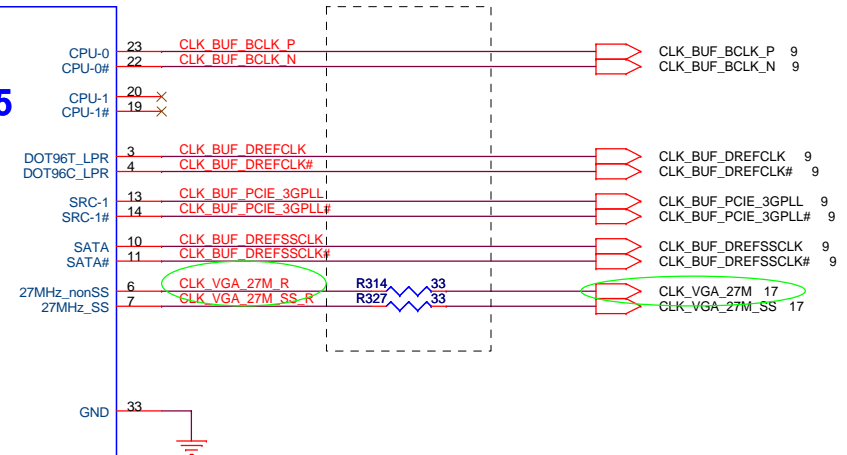




Realtek: 0.1uF x 6 pcs, 22uF x 1 pcs
IDT: 0.1uF x 5 pcs, 10uF x 1 pcs

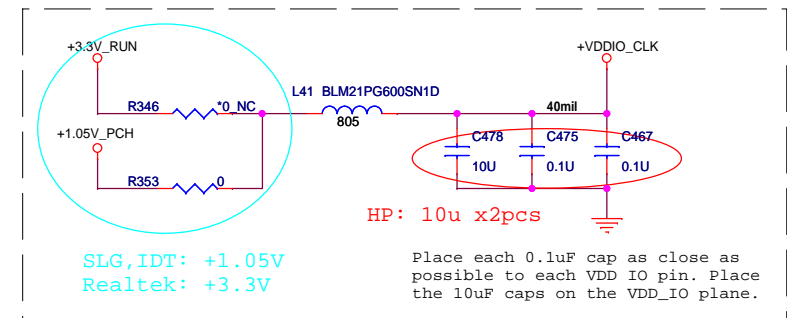
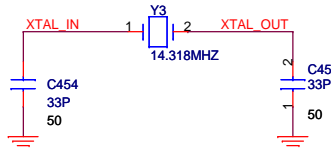


Place within 0.5" of CLKGEN



Realtek: 0.1uF x 3 pcs, 22uF x 1 pcs
IDT: 0.1uF x 2 pcs, 10uF x 1 pcs

Add capacitor pads for improving WWAN.



HP: 10u x 2 pcs

SLG, IDT: +1.05V
Realtek: +3.3V

+VDDIO_CLK:
SLG date sheet (V0.2) P15: Min 1.05V, Max 3.465V.
Realtek date sheet (V1.2) P11: Min 1.05V, Max 3.3V.
IDT date sheet (V0.7) P10: Min 0.9975V, Max 3.465V.

PIN	30	CPU_0	CPU_1
0 (default)		133MHz	133MHz
1 (0.7V-1.5V)		100MHz	100MHz

CPU_SEL:
SLG date sheet (V0.2) P15:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
Realtek date sheet (V1.2) P11:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
IDT date sheet (V0.7) P10:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.

3 PCIE_MTX_GRX_P0..15]
3 PCIE_MTX_GRX_N0..15]

PCIE_MTX_GRX_P0 AF30
PCIE_MTX_GRX_N0 AE31
PCIE_MTX_GRX_P1 AE29
PCIE_MTX_GRX_N1 AD28
PCIE_MTX_GRX_P2 AD30
PCIE_MTX_GRX_N2 AC31
PCIE_MTX_GRX_P3 AC29
PCIE_MTX_GRX_N3 AB28
PCIE_MTX_GRX_P4 AB30
PCIE_MTX_GRX_N4 AA31
PCIE_MTX_GRX_P5 AA29
PCIE_MTX_GRX_N5 Y28
PCIE_MTX_GRX_P6 Y30
PCIE_MTX_GRX_N6 W31
PCIE_MTX_GRX_P7 W28
PCIE_MTX_GRX_N7 V28
PCIE_MTX_GRX_P8 V30
PCIE_MTX_GRX_N8 U31
PCIE_MTX_GRX_P9 U29
PCIE_MTX_GRX_N9 T28
PCIE_MTX_GRX_P10 T30
PCIE_MTX_GRX_N10 R31
PCIE_MTX_GRX_P11 R29
PCIE_MTX_GRX_N11 P28
PCIE_MTX_GRX_P12 P30
PCIE_MTX_GRX_N12 N31
PCIE_MTX_GRX_P13 N29
PCIE_MTX_GRX_N13 M28
PCIE_MTX_GRX_P14 M30
PCIE_MTX_GRX_N14 L31
PCIE_MTX_GRX_P15 L29
PCIE_MTX_GRX_N15 K30

U32A

PART 1 OF 10

PCI-EXPRESS INTERFACE

PCIE_REFCLKP AK30
PCIE_REFCLKN AK32
PERSTB A27
M92-S2M92-XT

PCIE_TX0P AH30
PCIE_TX0N AG31
PCIE_TX1P AG29
PCIE_TX1N AF28
PCIE_TX2P AF27
PCIE_TX2N AF26
PCIE_TX3P AD27
PCIE_TX3N AD26
PCIE_TX4P AC25
PCIE_TX4N AB25
PCIE_TX5P Y23
PCIE_TX5N Y24
PCIE_TX6P AB27
PCIE_TX6N AB26
PCIE_TX7P Y27
PCIE_TX7N Y26
PCIE_TX8P W24
PCIE_TX8N W23
PCIE_TX9P V27
PCIE_TX9N U26
PCIE_TX10P U24
PCIE_TX10N U23
PCIE_TX11P T26
PCIE_TX11N T27
PCIE_TX12P T24
PCIE_TX12N T23
PCIE_TX13P P27
PCIE_TX13N P26
PCIE_TX14P P24
PCIE_TX14N P23
PCIE_TX15P M27
PCIE_TX15N N26

M92-S2 XT AJ072800T04 100-CG1675(216-0728004)
M92-S2 AJ072800T03 100-CG1643(216-0728003)

3 PCIE_MRX_GTX_P0..15]
3 PCIE_MRX_GTX_N0..15]

PCIE_MRX_GTX_P0 0.1U 2 1 C87 16 PCIE_MRX_GTX_C_P0
PCIE_MRX_GTX_P1 0.1U 2 1 C94 16 PCIE_MRX_GTX_C_P1
PCIE_MRX_GTX_P2 0.1U 2 1 C92 16 PCIE_MRX_GTX_C_P2
PCIE_MRX_GTX_P3 0.1U 2 1 C88 16 PCIE_MRX_GTX_C_P3
PCIE_MRX_GTX_P4 0.1U 2 1 C100 16 PCIE_MRX_GTX_C_P4
PCIE_MRX_GTX_P5 0.1U 2 1 C103 16 PCIE_MRX_GTX_C_P5
PCIE_MRX_GTX_P6 0.1U 2 1 C108 16 PCIE_MRX_GTX_C_P6
PCIE_MRX_GTX_P7 0.1U 2 1 C115 16 PCIE_MRX_GTX_C_P7
PCIE_MRX_GTX_P8 0.1U 2 1 C131 16 PCIE_MRX_GTX_C_P8
PCIE_MRX_GTX_P9 0.1U 2 1 C148 16 PCIE_MRX_GTX_C_P9
PCIE_MRX_GTX_P10 0.1U 2 1 C136 16 PCIE_MRX_GTX_C_P10
PCIE_MRX_GTX_P11 0.1U 2 1 C167 16 PCIE_MRX_GTX_C_P11
PCIE_MRX_GTX_P12 0.1U 2 1 C140 16 PCIE_MRX_GTX_C_P12
PCIE_MRX_GTX_P13 0.1U 2 1 C180 16 PCIE_MRX_GTX_C_P13
PCIE_MRX_GTX_P14 0.1U 2 1 C150 16 PCIE_MRX_GTX_C_P14
PCIE_MRX_GTX_P15 0.1U 2 1 C168 16 PCIE_MRX_GTX_C_P15
PCIE_MRX_GTX_N0 0.1U 2 1 C90 16 PCIE_MRX_GTX_C_N0
PCIE_MRX_GTX_N1 0.1U 2 1 C96 16 PCIE_MRX_GTX_C_N1
PCIE_MRX_GTX_N2 0.1U 2 1 C95 16 PCIE_MRX_GTX_C_N2
PCIE_MRX_GTX_N3 0.1U 2 1 C91 16 PCIE_MRX_GTX_C_N3
PCIE_MRX_GTX_N4 0.1U 2 1 C105 16 PCIE_MRX_GTX_C_N4
PCIE_MRX_GTX_N5 0.1U 2 1 C107 16 PCIE_MRX_GTX_C_N5
PCIE_MRX_GTX_N6 0.1U 2 1 C114 16 PCIE_MRX_GTX_C_N6
PCIE_MRX_GTX_N7 0.1U 2 1 C128 16 PCIE_MRX_GTX_C_N7
PCIE_MRX_GTX_N8 0.1U 2 1 C118 16 PCIE_MRX_GTX_C_N8
PCIE_MRX_GTX_N9 0.1U 2 1 C159 16 PCIE_MRX_GTX_C_N9
PCIE_MRX_GTX_N10 0.1U 2 1 C142 16 PCIE_MRX_GTX_C_N10
PCIE_MRX_GTX_N11 0.1U 2 1 C181 16 PCIE_MRX_GTX_C_N11
PCIE_MRX_GTX_N12 0.1U 2 1 C147 16 PCIE_MRX_GTX_C_N12
PCIE_MRX_GTX_N13 0.1U 2 1 C166 16 PCIE_MRX_GTX_C_N13
PCIE_MRX_GTX_N14 0.1U 2 1 C160 16 PCIE_MRX_GTX_C_N14
PCIE_MRX_GTX_N15 0.1U 2 1 C182 16 PCIE_MRX_GTX_C_N15

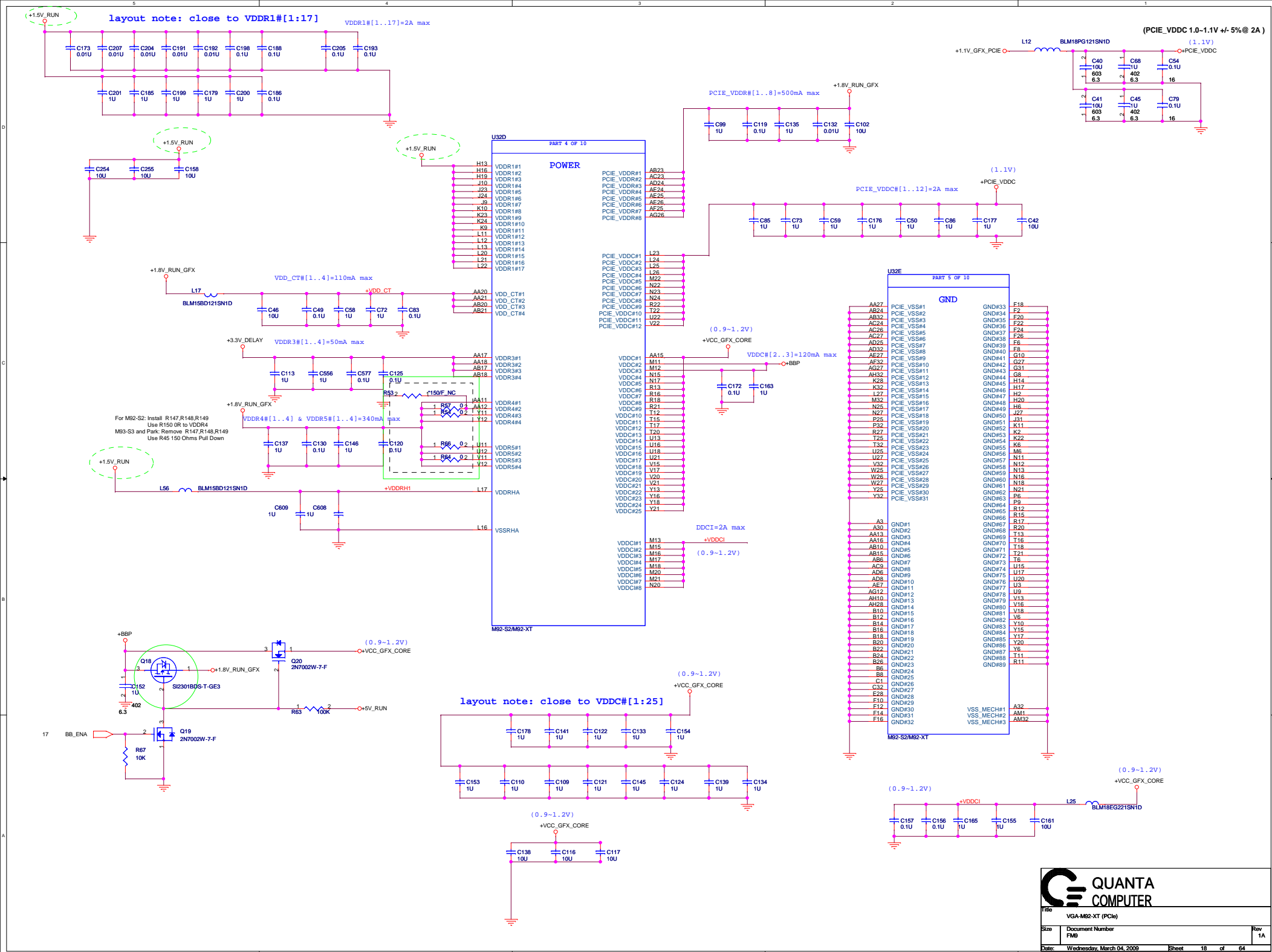
100 MHz (+/-300 ppm) input frequency, 0-0.7 V single-ended swing.
clock must be provided less than 400ns
after CLKREQ# is asserted

9 CLK_PCIE_VGA AK30
9 CLK_PCIE_VGA# AK32

9,9,26,28,29,31,32,41 PLTRST# A27



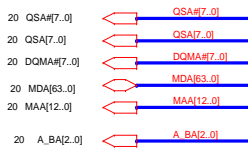
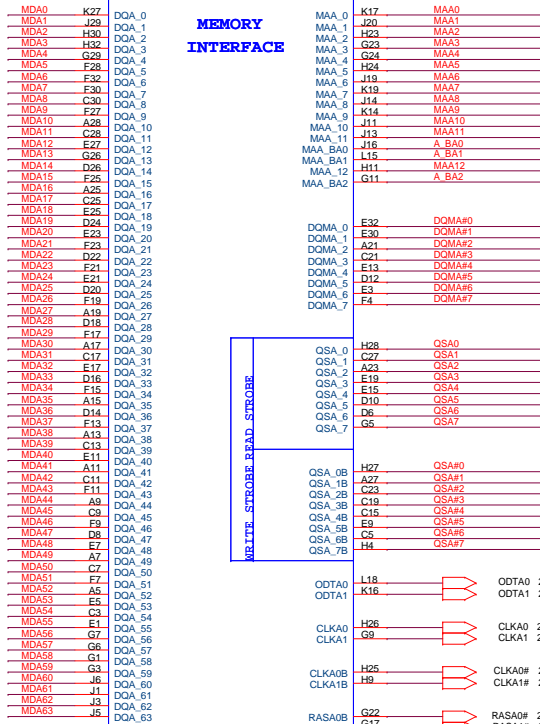
QUANTA COMPUTER logo and title block containing document information: Title (VGA-M92-XT (PCIe)), Size (Document Number FM9), Date (Wednesday, March 04, 2009), Sheet (16 of 64), and Revision (1A).



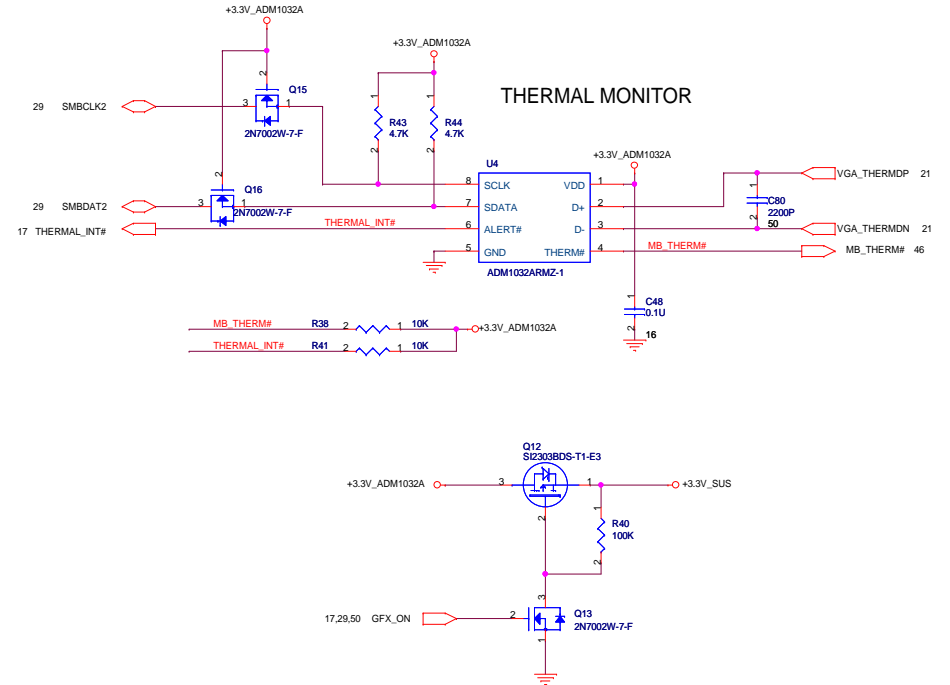
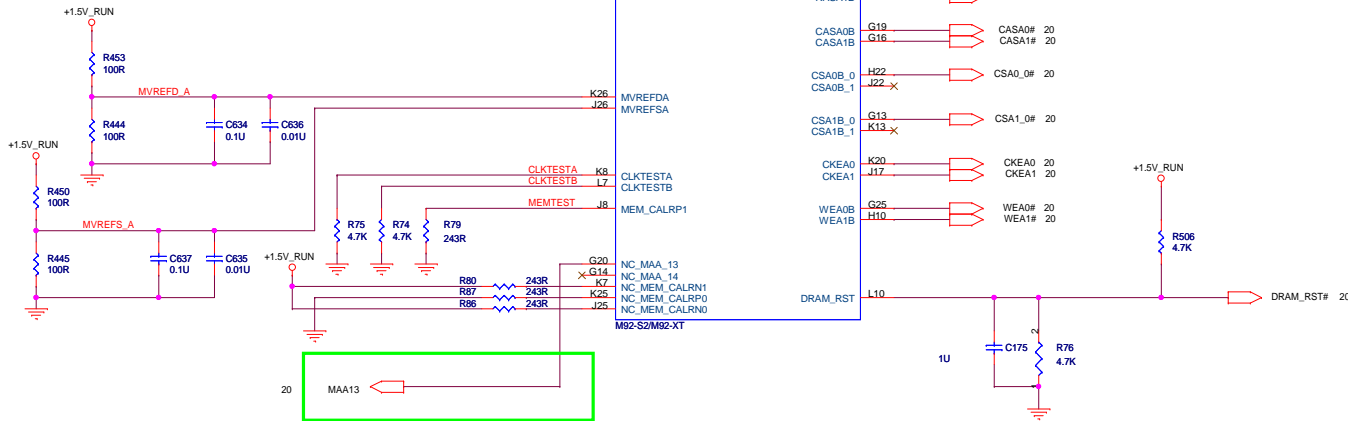
MEMORY INTERFACE

U32C

MEMORY INTERFACE

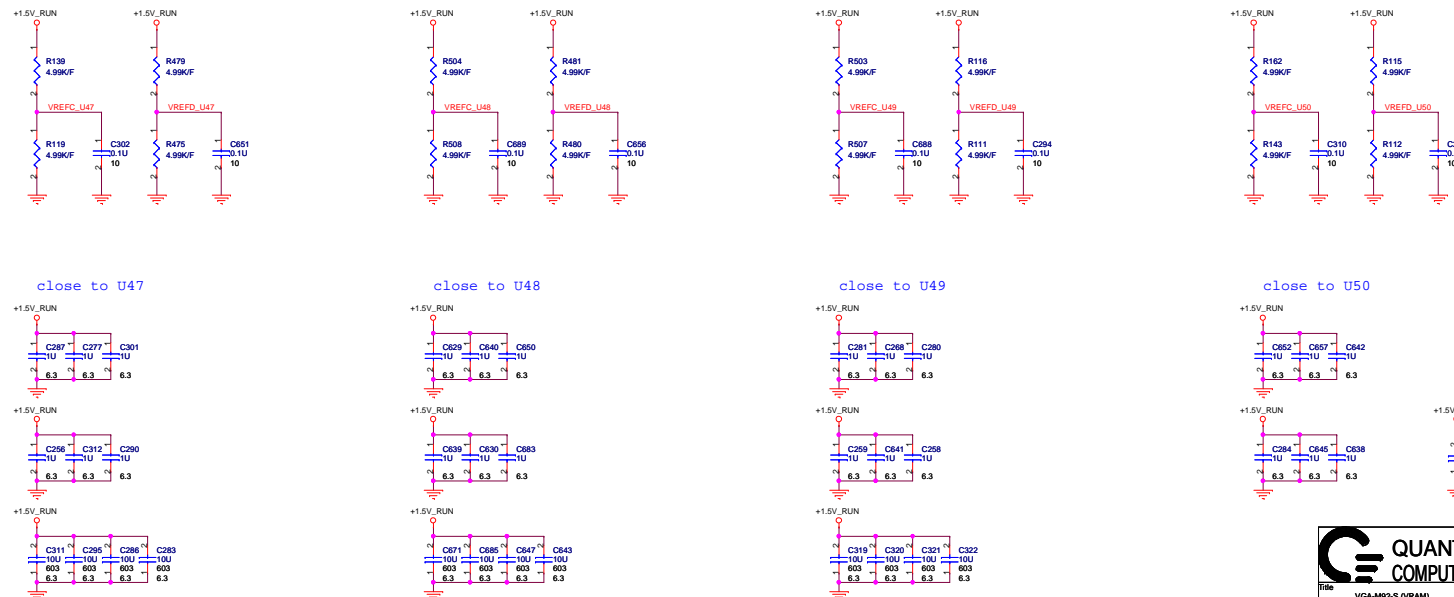
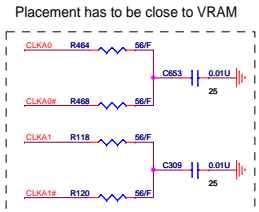
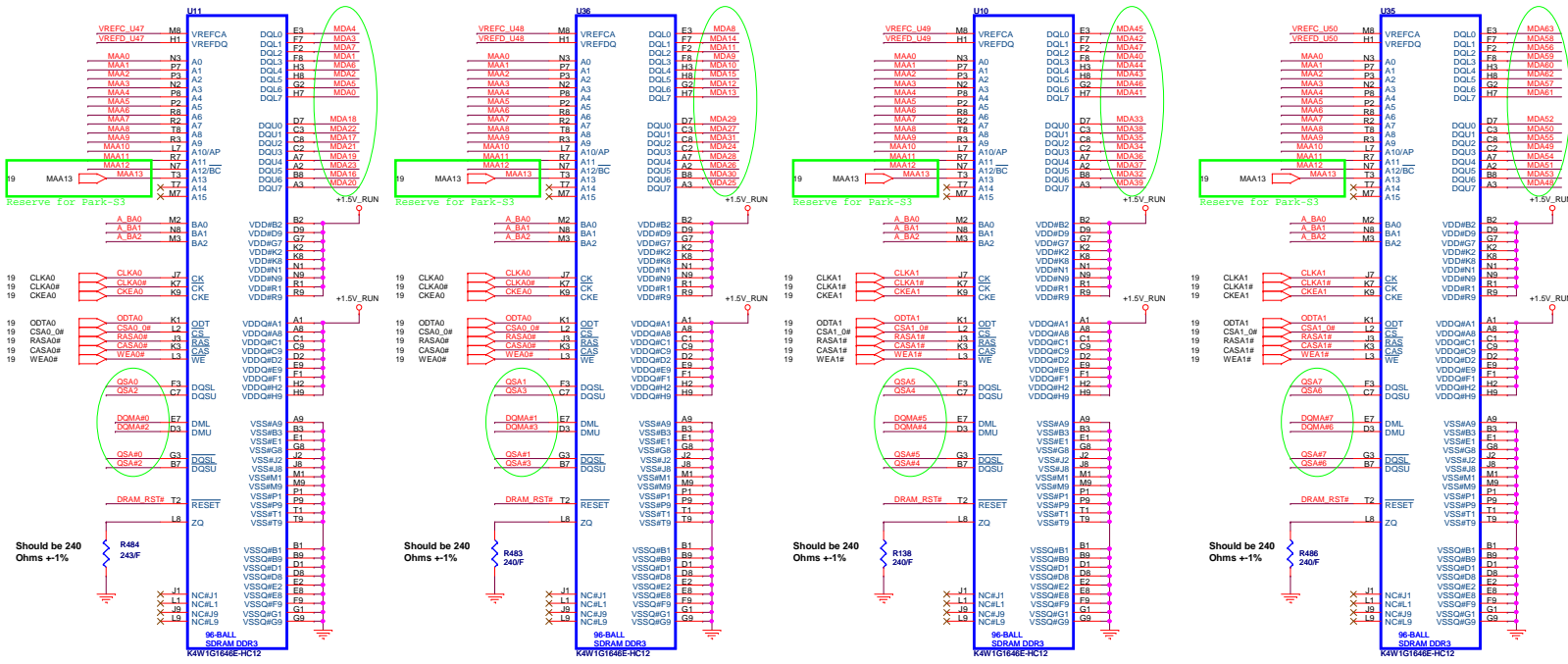


DIVIDER RESISTORS	DDR3
MVREF TO 1.5V	100R
MVREF TO GND	100R

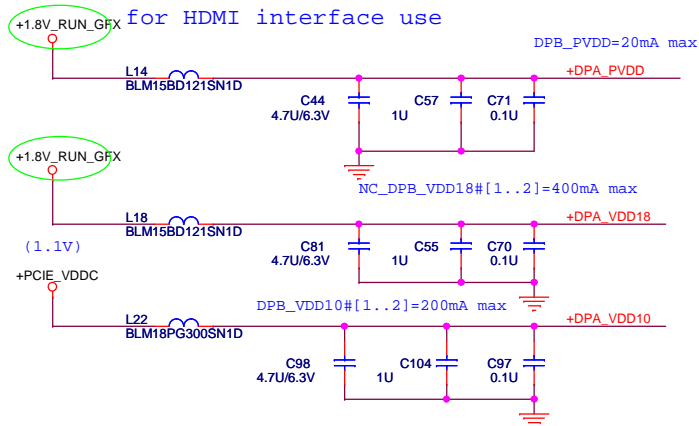
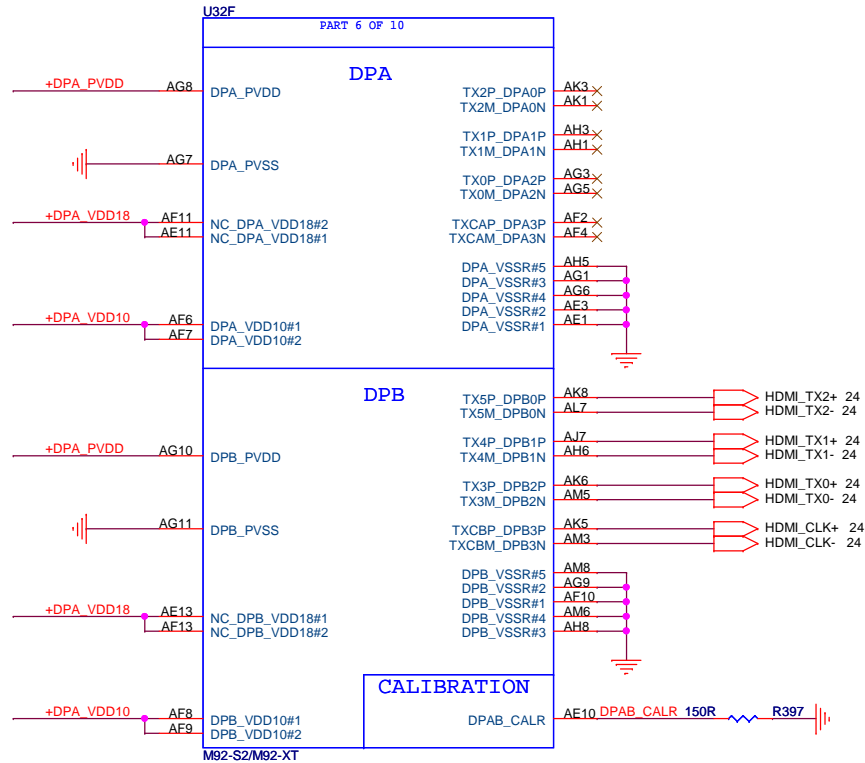


19 MDA[63..0] MDA[63..0]
 19 MAA[12..0] MAA[12..0]
 19 QSA[7..0] QSA[7..0]
 19 QSA[7..0] QSA[7..0]
 19 QDMA[47..0] QDMA[47..0]
 19 DRAM_RST# DRAM_RST#
 19 A_BA[2..0] A_BA[2..0]

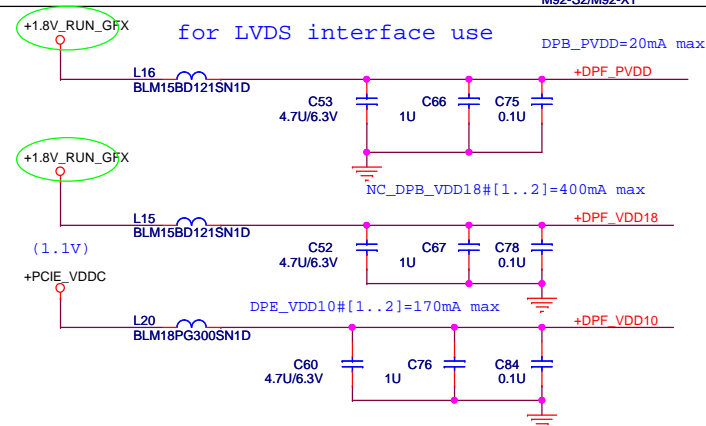
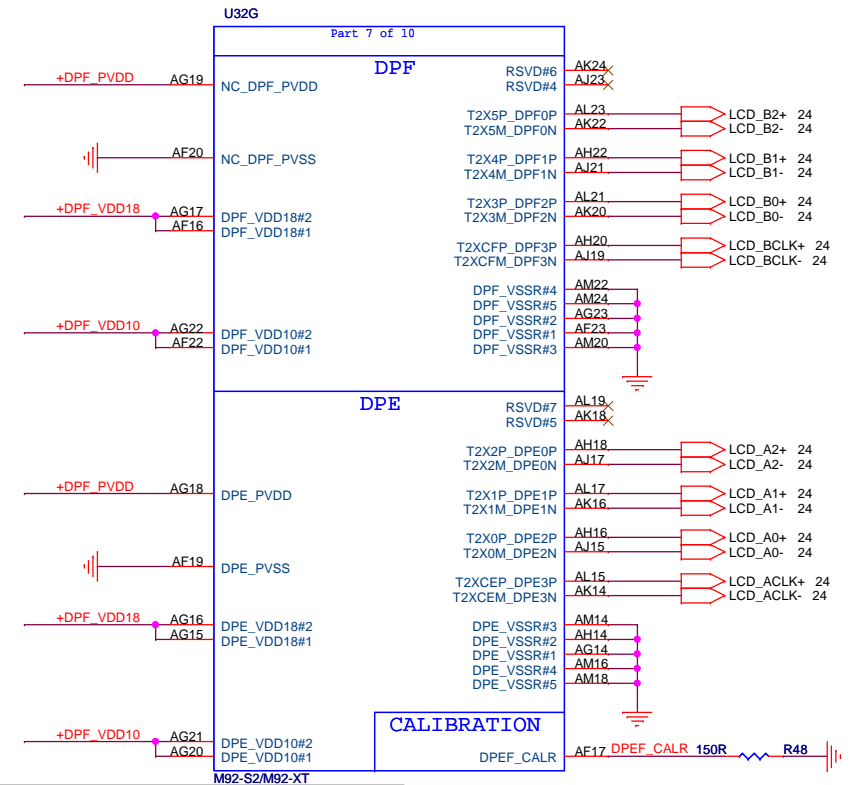
DDR3



TMDP(HDMI) INTERFACE



LVDS INTERFACE



Title			VGA-M92-XT (PCIe)
Size	Document Number	Rev	
	FM9	1A	
Date:	Wednesday, March 04, 2009	Sheet	22 of 64



Title

VGA-M82-S (PCIe)

Size

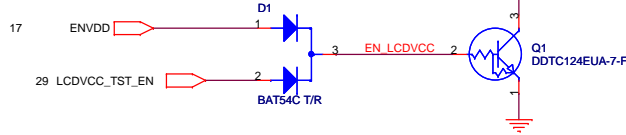
Document Number FM9

Rev	1A
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Date: Wednesday, March 04, 2009

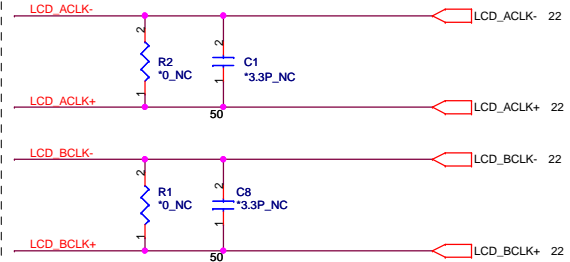
Sheet	23	of	64
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Support the new imbedded diagnostics.

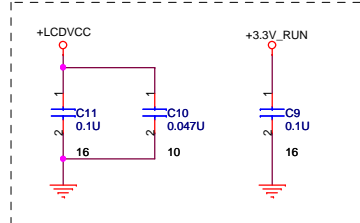
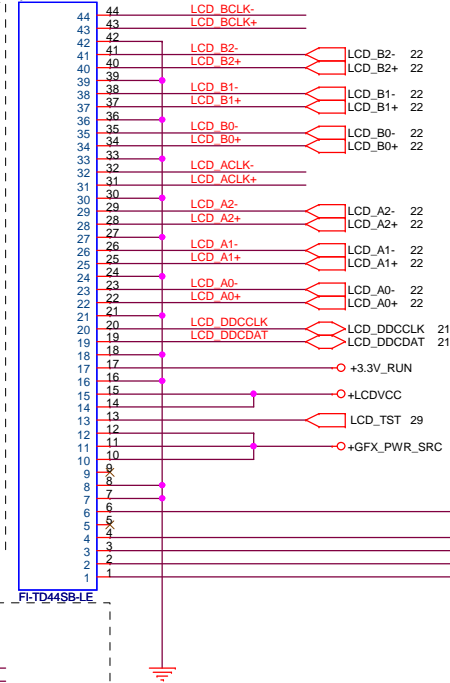


Shunt capacitors on LVDS for improving WWAN.

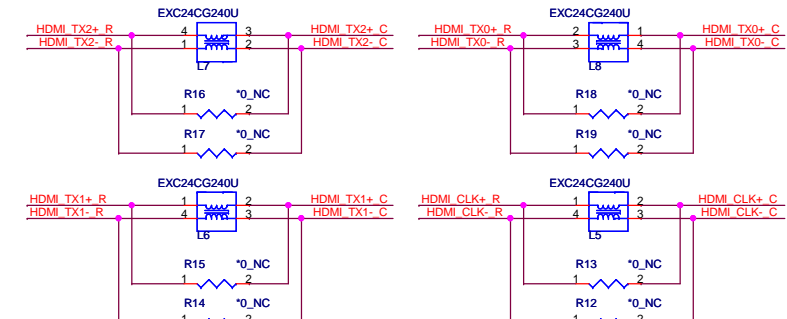
LCD B0-	C13	1	2	*3.3P NC	50	LCD B0+
LCD B1-	C5	1	2	*3.3P NC	50	LCD B1+
LCD B2-	C4	1	2	*3.3P NC	50	LCD B2+
LCD A0-	C3	1	2	*3.3P NC	50	LCD A0+
LCD A1-	C7	1	2	*3.3P NC	50	LCD A1+
LCD A2-	C2	1	2	*3.3P NC	50	LCD A2+



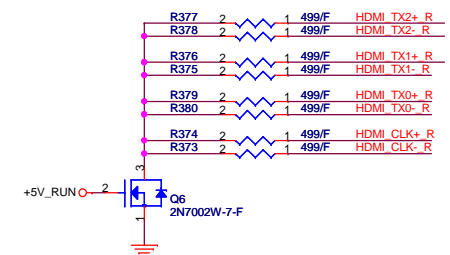
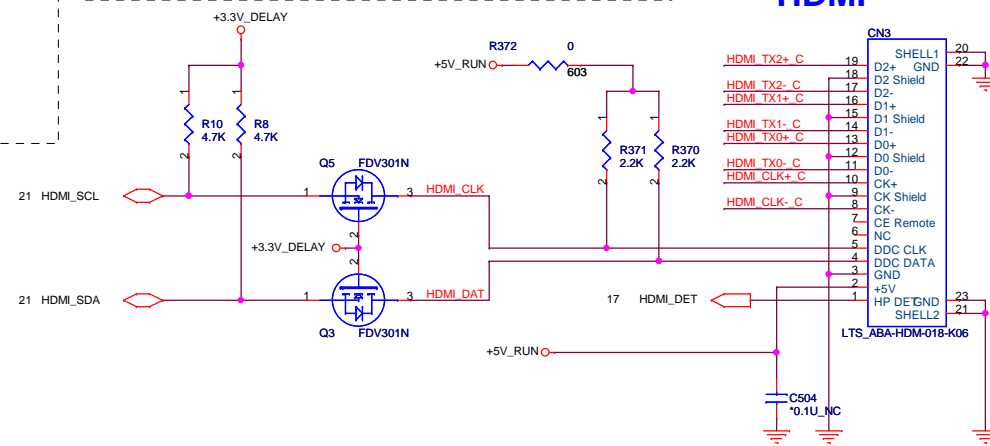
FL-TD4S8LE



Address : A9H --Contrast
AAH --Backlight



HDMI

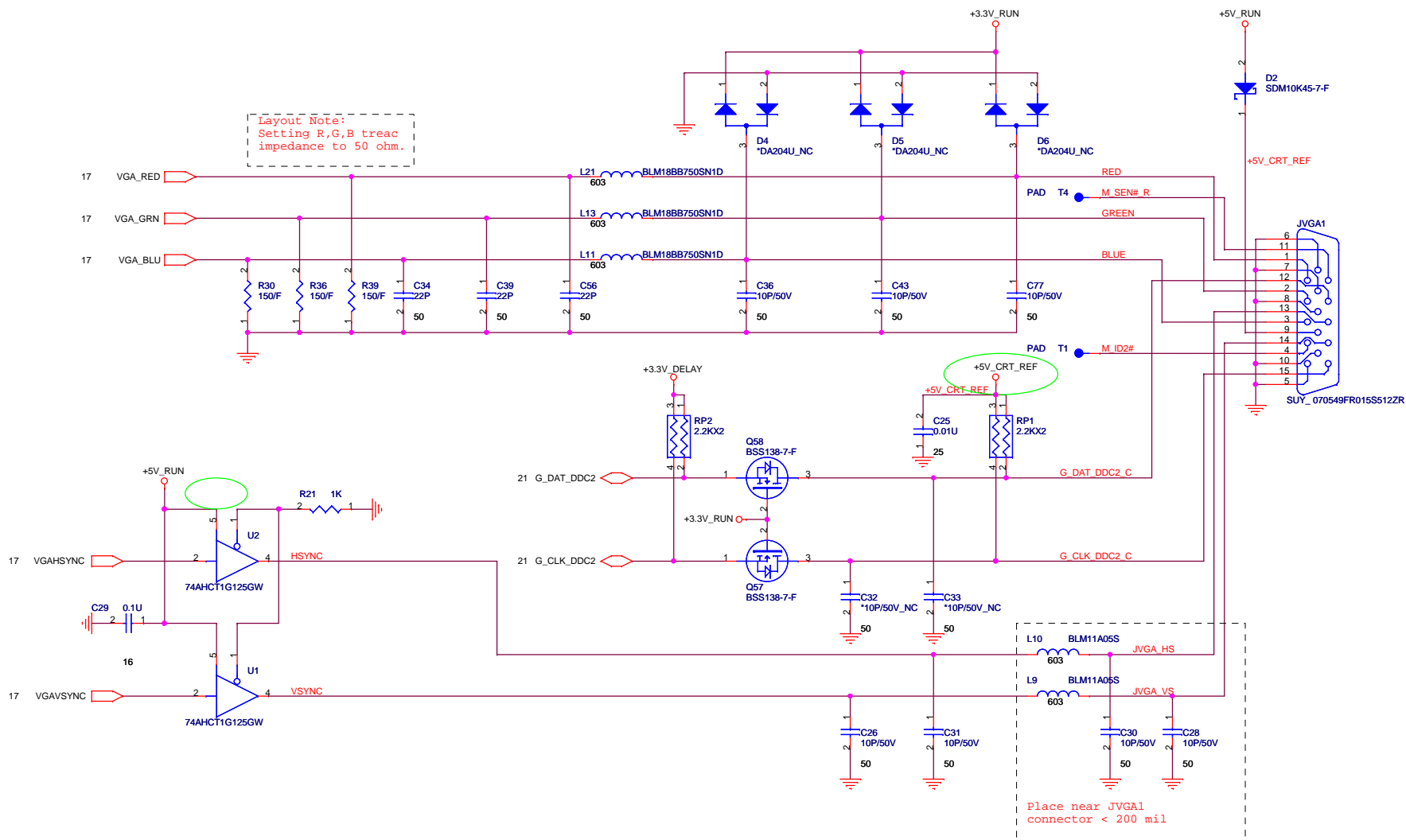


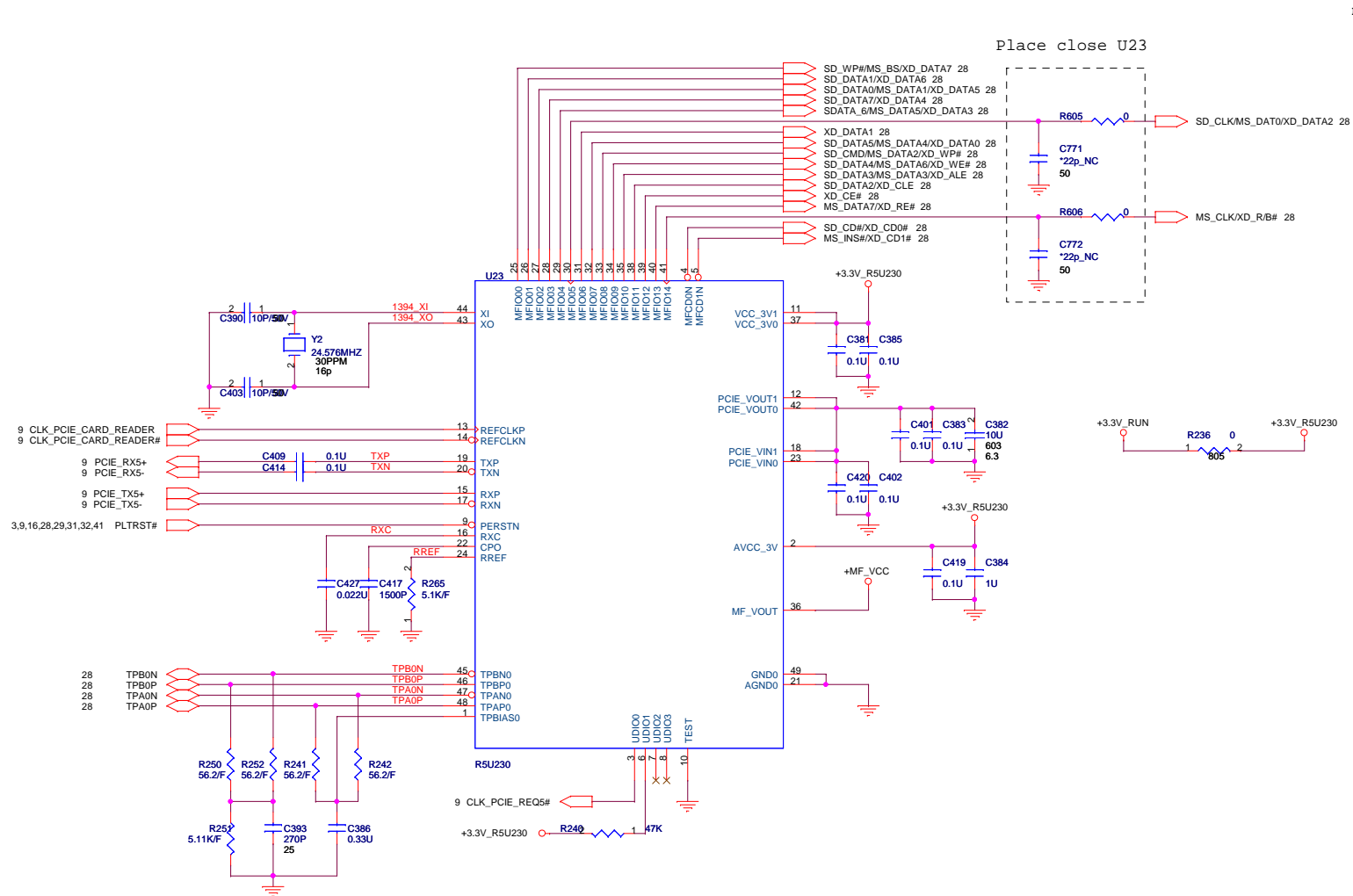
QUANTA COMPUTER

Title: LCD CONN & CK-SSCD


Size: Document Number FM9 Rev 1A

Date: Wednesday, March 04, 2009 Sheet 24 of 64





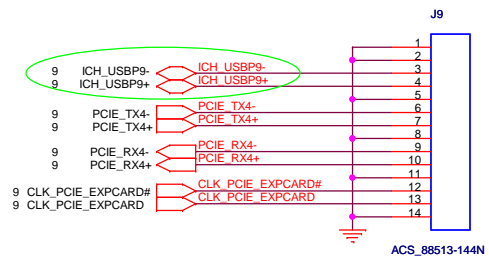
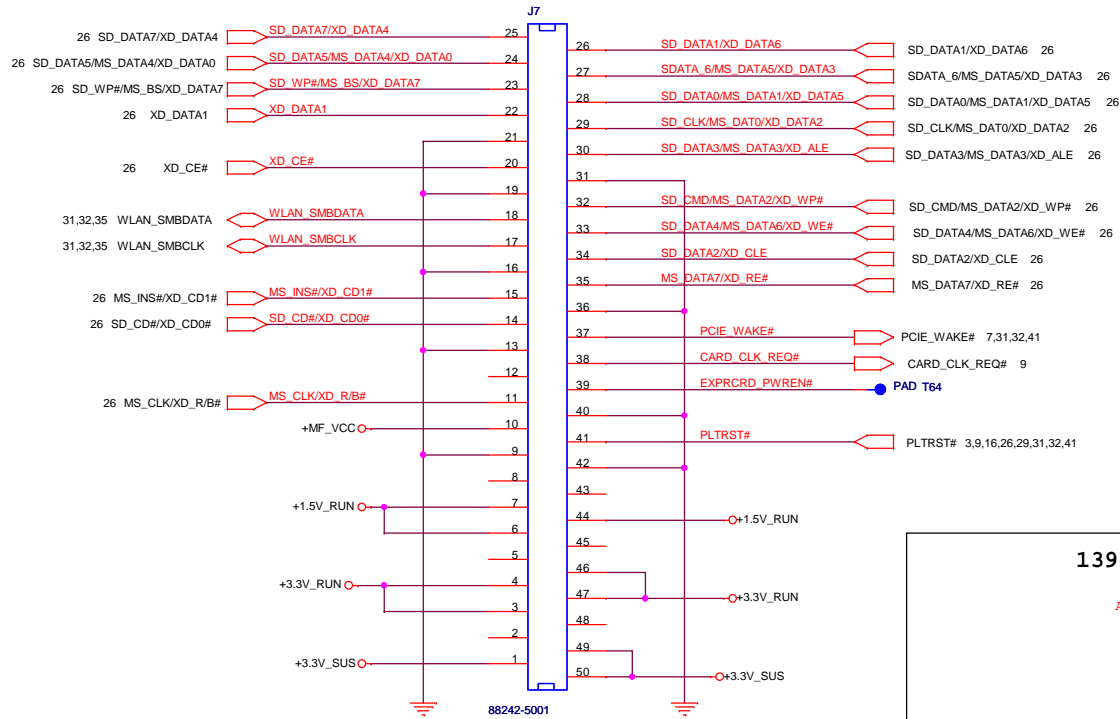
	A	B	C	D	E
1					
2					
3					
4					



QUANTA
COMPUTER

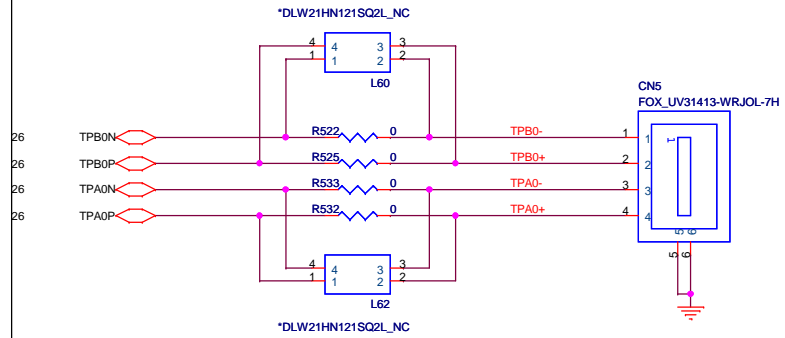
Title IEEE 1394		
Size FM9	Document Number	Rev 1A
Date: Wednesday, March 04, 2009		
Sheet 27 of 64		

Express Card/CARD READER



1394 CONNECTOR

AS CLOSE AS POSSIBLE TO 1394 CONNECTOR.



```
*TPA0P/TPA0N,TPB0P/TPB0N pair trace : As close as possible.
*TPA0P/TPA0N,TPB0P/TPB0N pair trace : Same length electrically.
```



Title	ExpressCard/SmartCard
-------	-----------------------

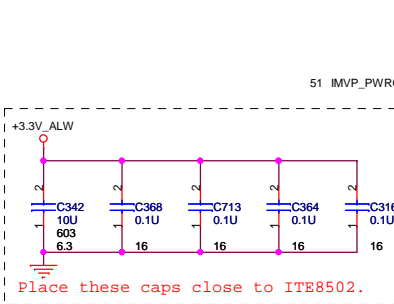
Size	Docu FM9
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Document Number

Rev
1A

Date: Wednesday, March 04, 2009

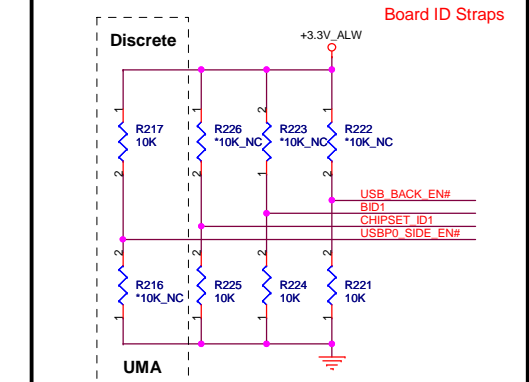
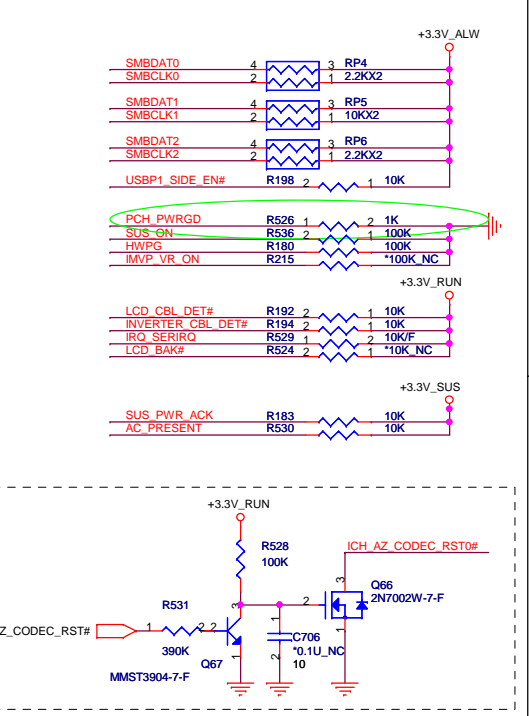
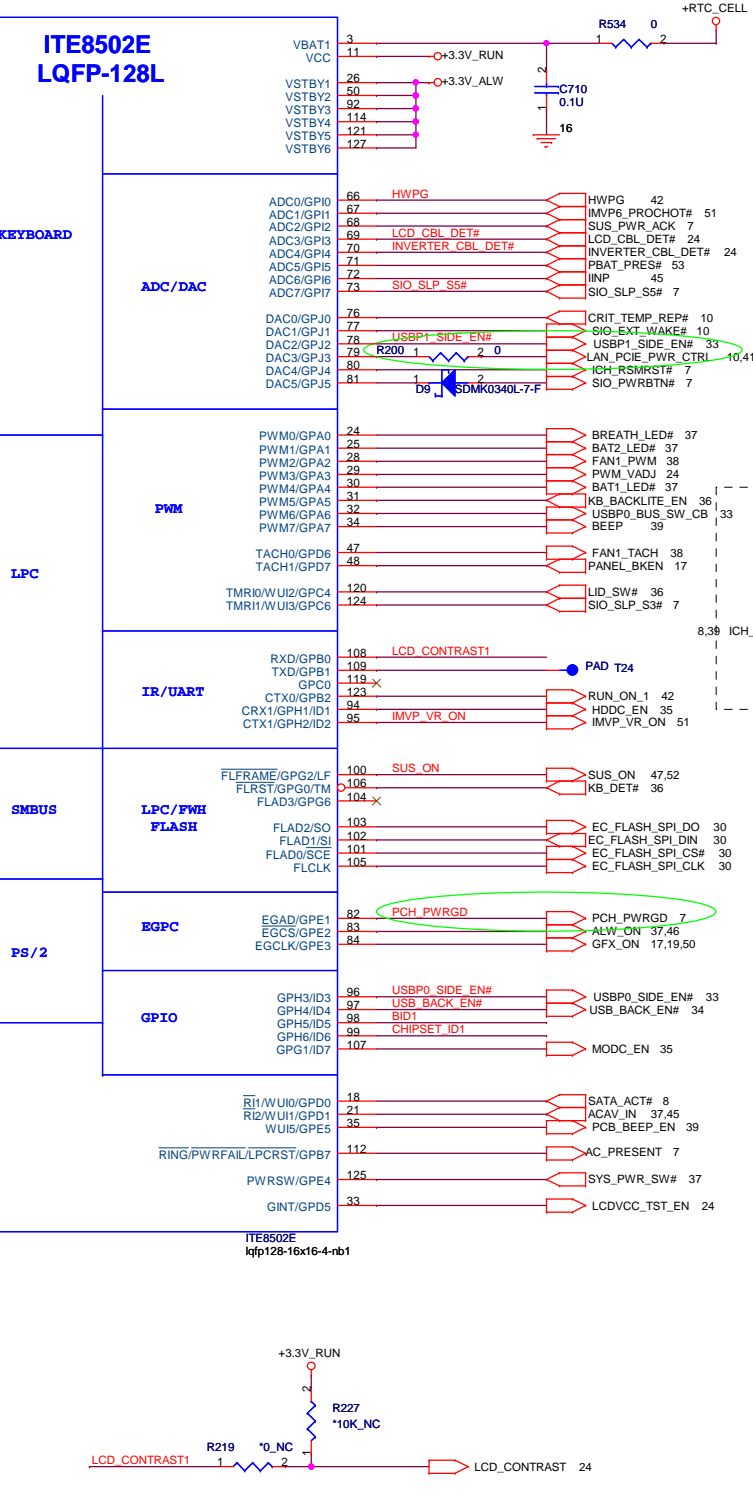
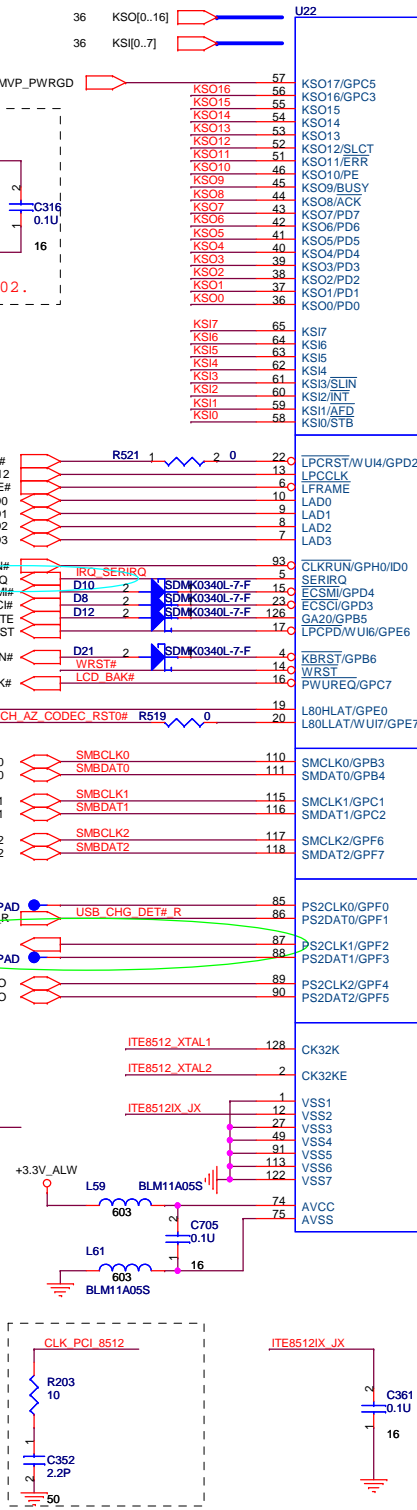
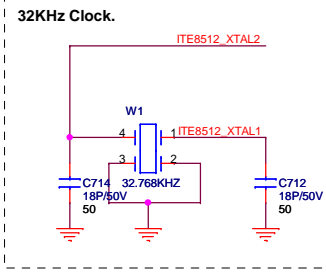
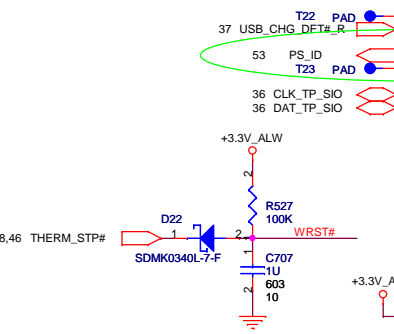
Sheet 28 of 64



Charge and BAT

CLK, LCD and Thermal

G_Thermal and Media button



VGA_IDENTIFY

BID0

CHIPSET ID1	BID1	USB BACK_EN#	FM9B(UMA)	FM9(Ds)
0	0	0	SSI (X00)	SSI (X00)
0	0	1	PT (X01)	PT (X01)
0	1	0	ST (X02)	ST (X02)
0	1	1	QT (A00)	QT (A00)
1	0	0	(A01)	(A01)
1	0	1		

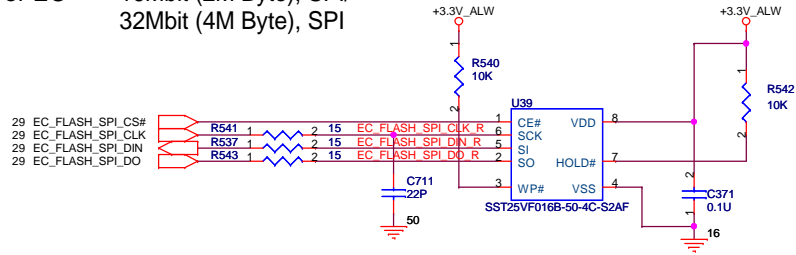
QUANTA COMPUTER

Ultra I/O Controller ECE5028

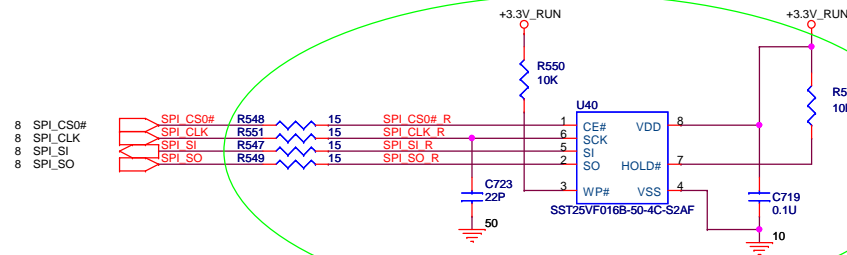
Size: Document Number FM9 Rev 1A

Date: Wednesday, March 04, 2009 Sheet 29 of 64

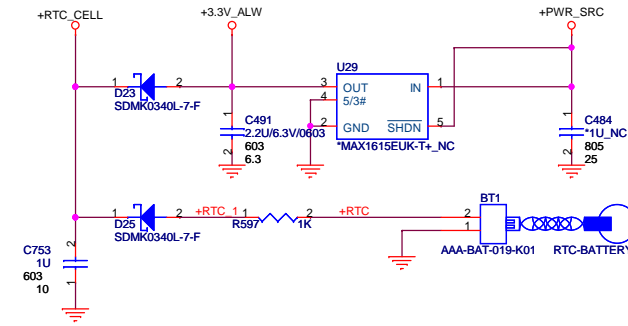
For EC 16Mbit (2M Byte), SPI/
32Mbit (4M Byte), SPI



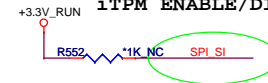
For PCH 16Mbit (2M Byte), SPI/
32Mbit (4M Byte), SPI



RTC BATTERY



iTPM ENABLE/DISABLE



TPM Function	R712
Enable	Mount
Disable	NC (Default)



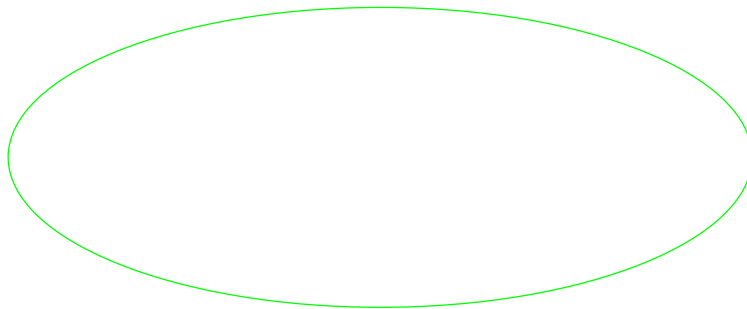
Title Ultra I/O Controller ECE5028

Size Document Number FM9

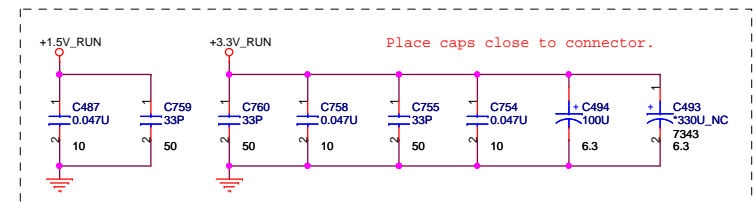
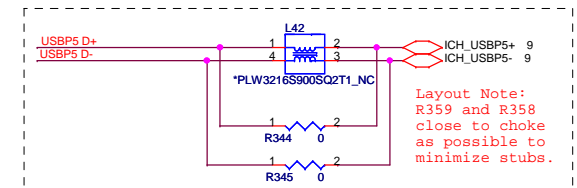
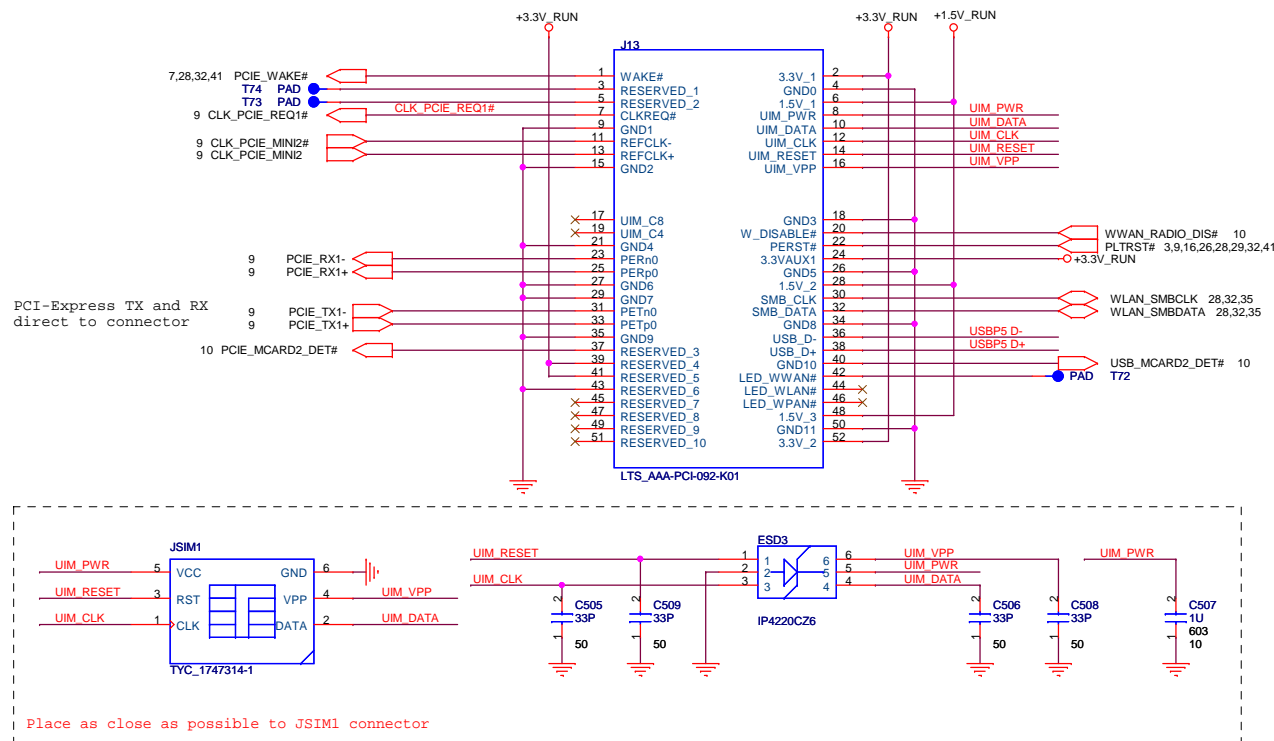
Rev 1A

Date: Wednesday, March 04, 2009

Sheet 30 of 64

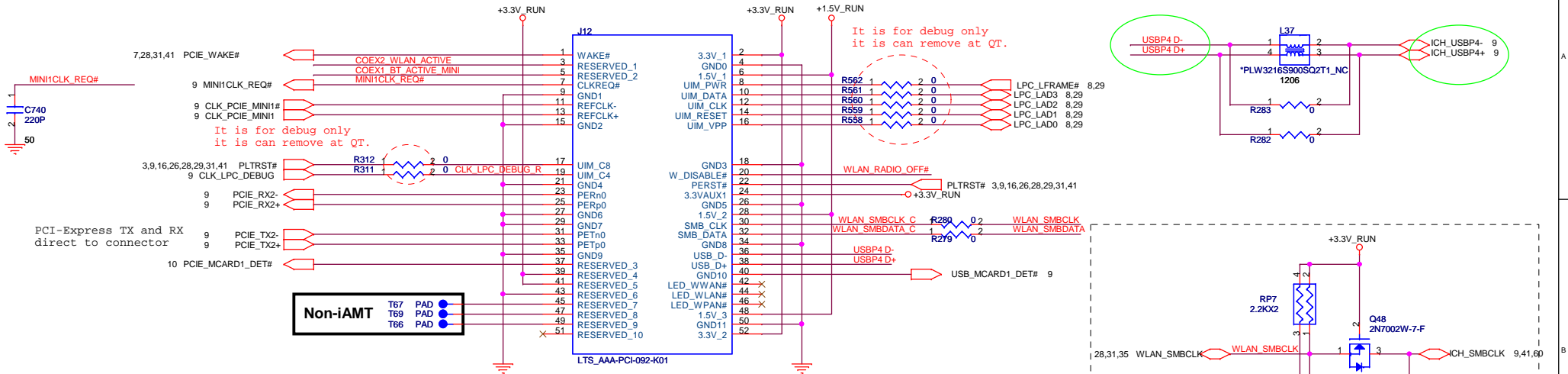


MiniCard WWAN connector

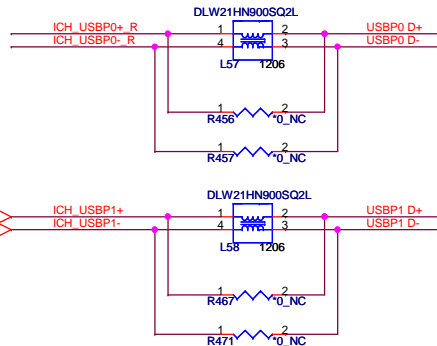


Title: MINI-PCI		
Size: FMS	Document Number: FMS	Rev: 1A
Date: Wednesday, March 04, 2009	Sheet: 31	of: 64

MiniCard WLAN connector

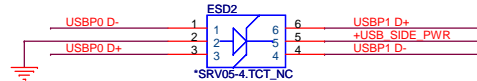


External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently



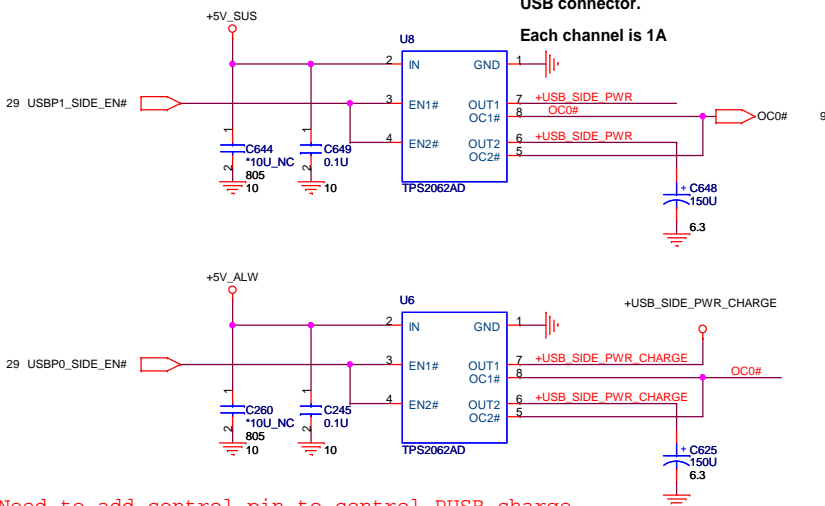
Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

Place ESD diodes as close as USB connector.



Place one 150uF cap by each USB connector.

Each channel is 1A

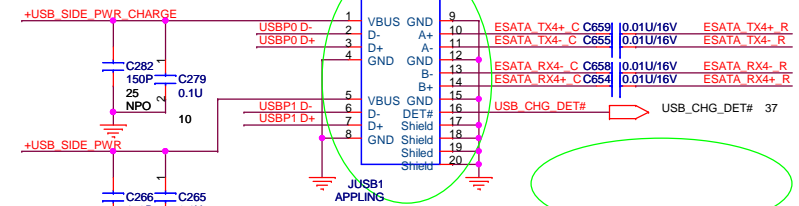


Need to add control pin to control PUSB charge

Support USBP1 charge function.
JUSB1 need to add USB_CHG_DET# pin wire to EC GPIO to detect USB device.

Side External USBX2

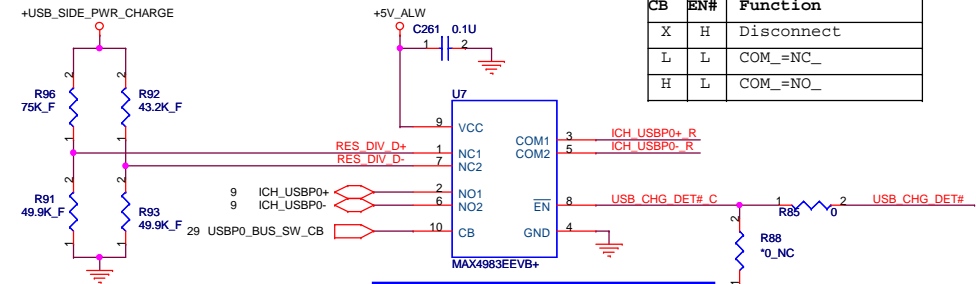
PN is old, Because New Part can't ready before SST build.



Please put those on the same side of MB PCB

USBx2 & ESATA COMBO & PWR CHARGE

USB BUS SW



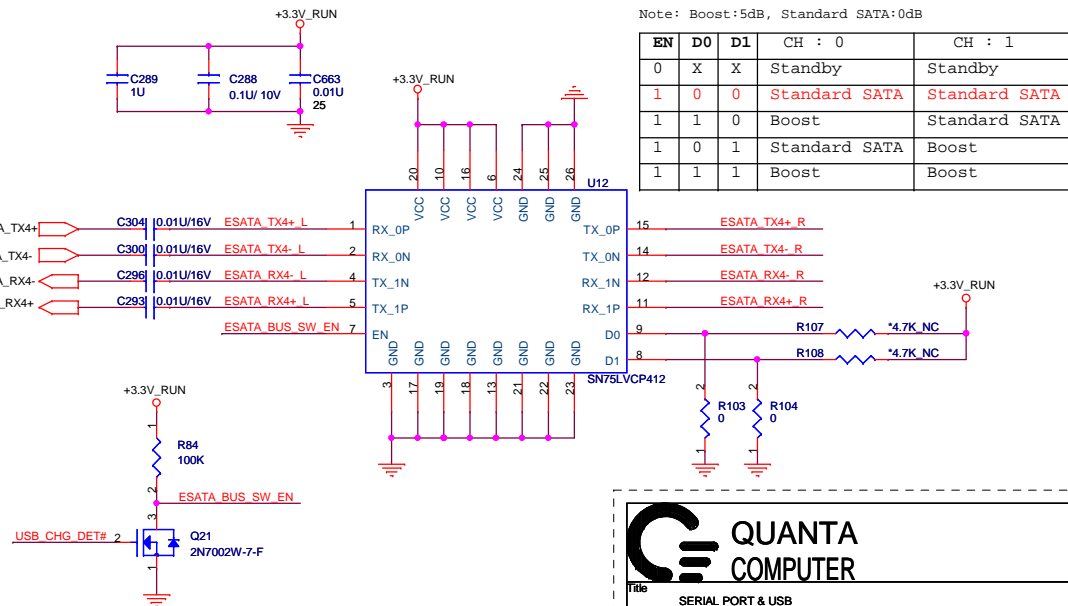
(5V)-43.2K-(D-)-49.9K-GND (about 2.68V)
(5V)-75.0K-(D+)-49.9K-GND (about 2.00V)

CB	EN#	Function
X	H	Disconnect
L	L	COM_=NC_
H	L	COM_=NO_

E-SATA Re-driver

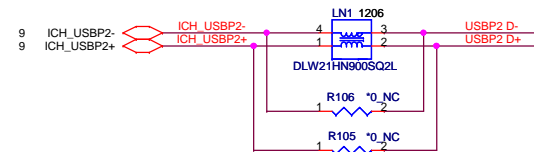
Please put those on the same side of MB PCB

Note: Boost:5dB, Standard SATA:0dB



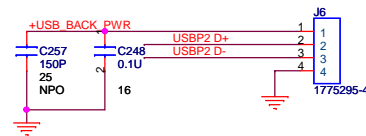
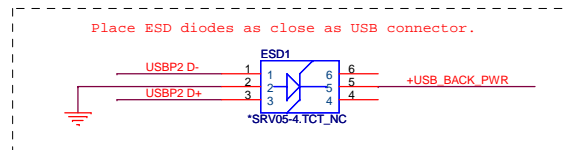
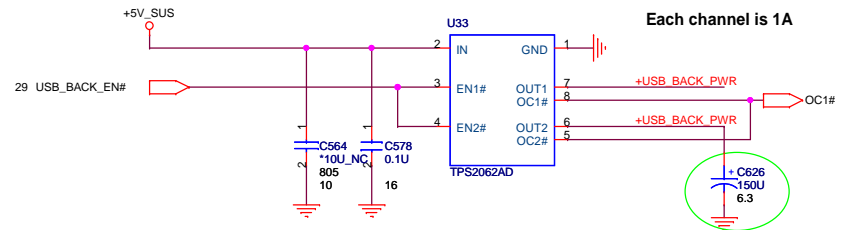
EN	D0	D1	CH : 0	CH : 1
0	X	X	Standby	Standby
1	0	0	Standard SATA	Standard SATA
1	1	0	Boost	Standard SATA
1	0	1	Standard SATA	Boost
1	1	1	Boost	Boost



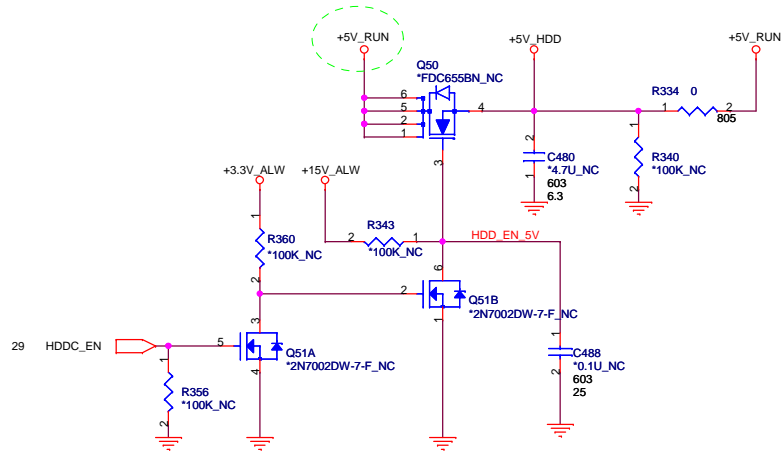
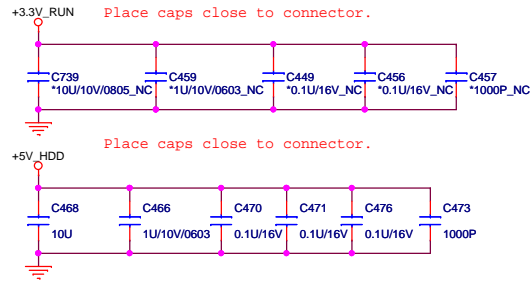
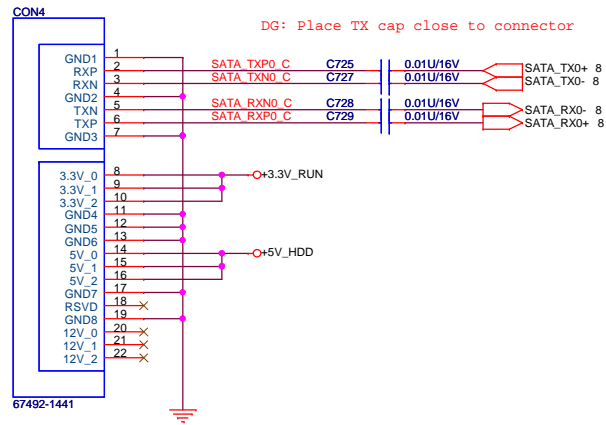


Place one 150uF cap by each USB connector.

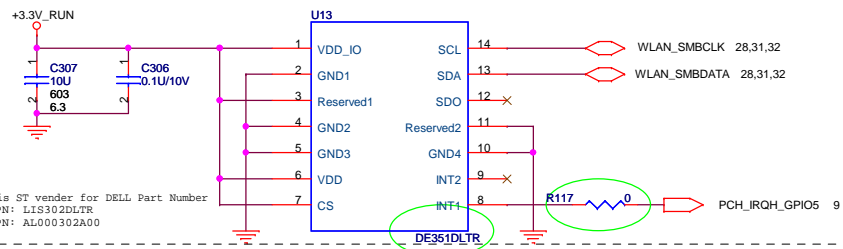
Each channel is 1A



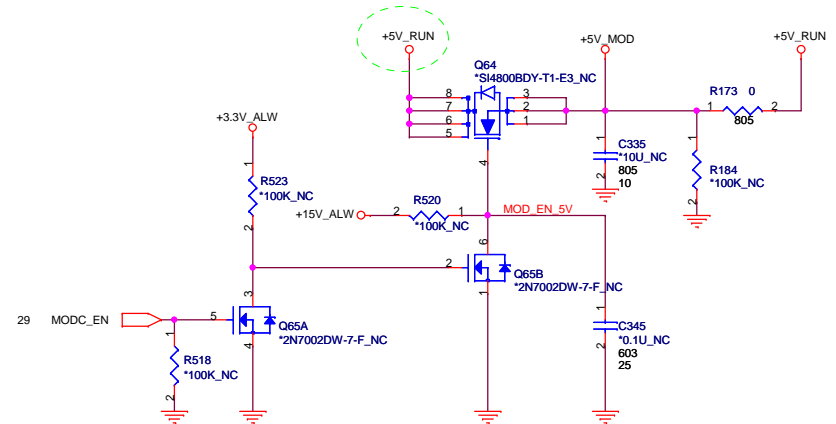
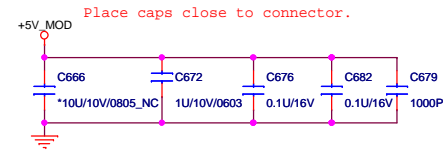
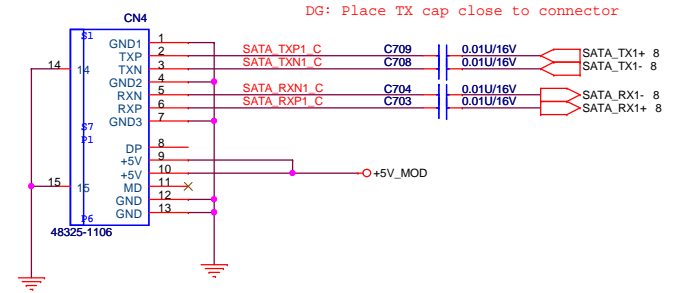
SATA Connector.



3-axis Fall Sensor (HDD data protector)



ODD Connector

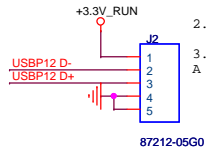


Title			SATA (HDD&CD_ROM)
Size	Document Number	Rev	
	FMR	1A	
Date:	Wednesday, March 04, 2009	Sheet	35 of 64

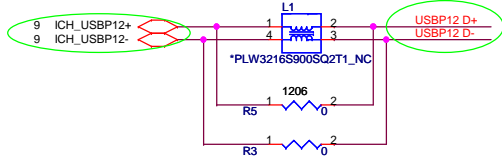
Date: Wednesday, March 04, 2009 Sheet 36 of 64

Touch Screen Module

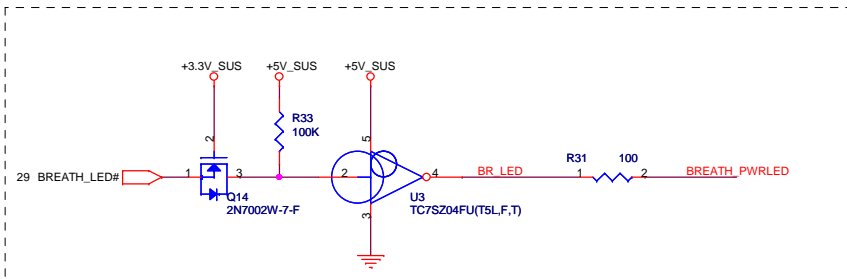
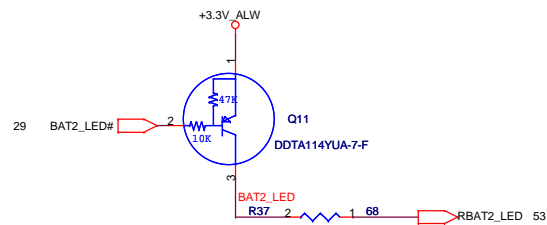
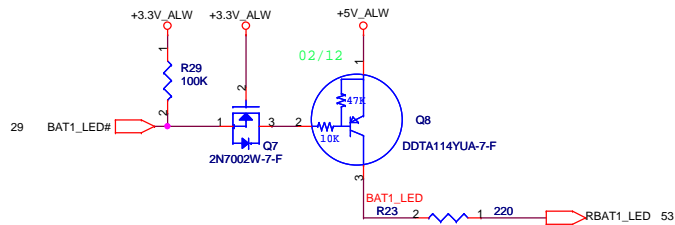
- Note:
1. VBUS IND:VBUS indication should be supplied to single the DuoSense to connect According to the USB 2.0 specification. A GND voltage from the host should indicate a connection.
 2. Maximum cable resistance on VCC, GND should be 150m ohm.
 3. FPC cable should support 12MHz USB singles. A tri-state should indicate no connection.



Need check the connector footprint and symbol.



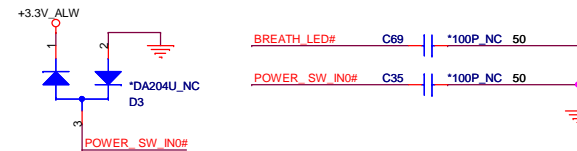
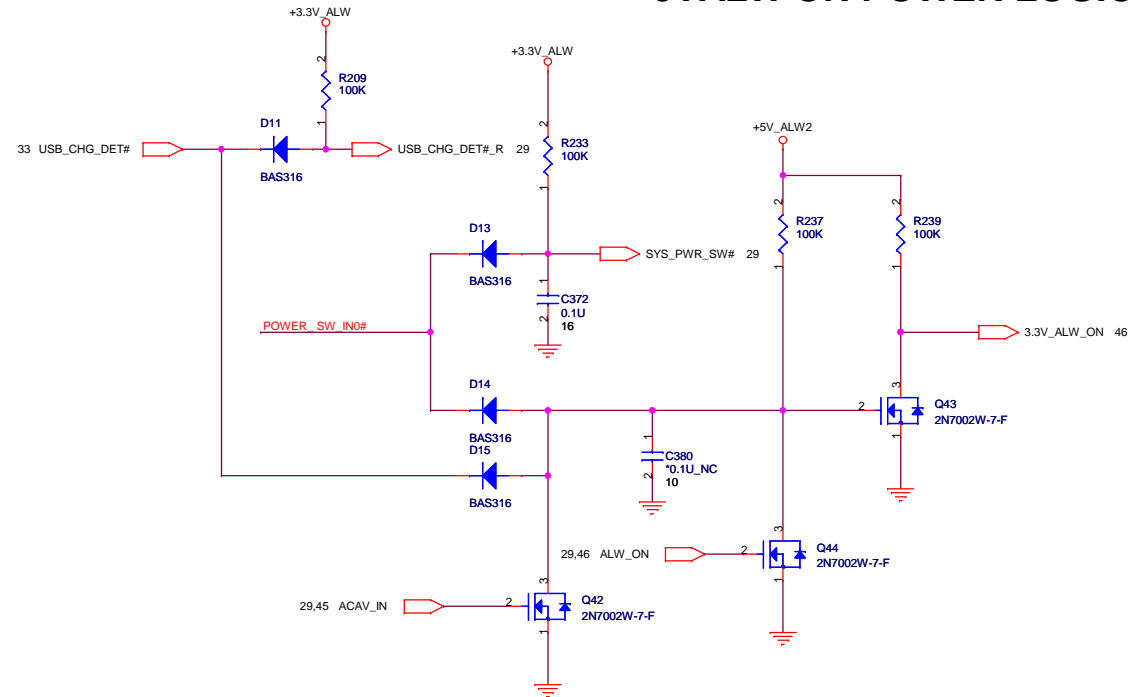
Battery status.

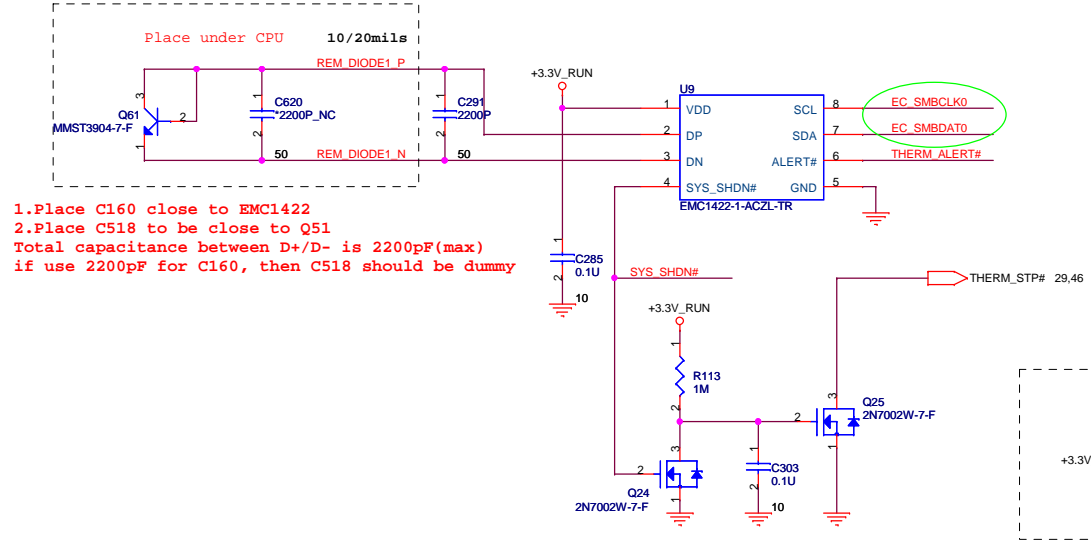
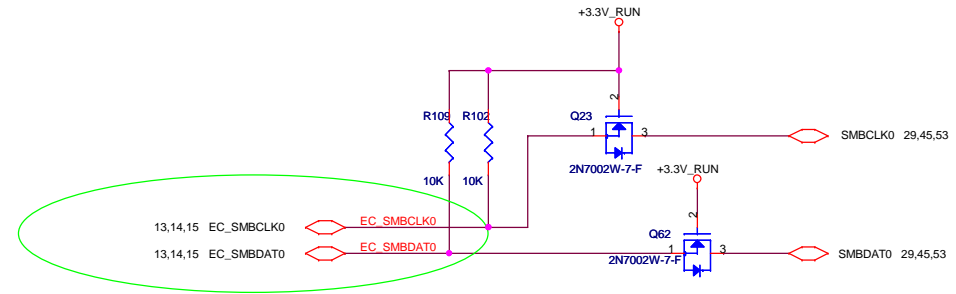
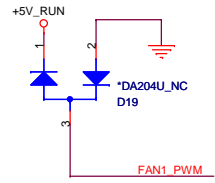
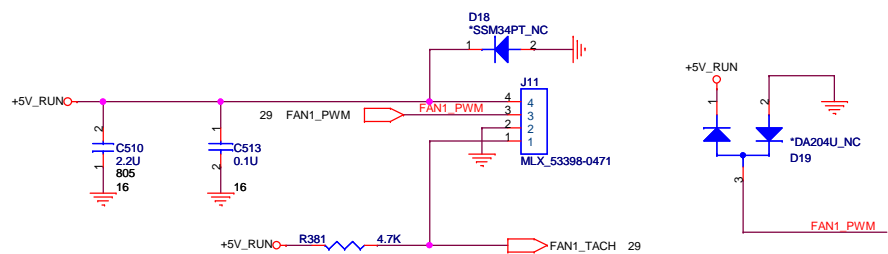


Power button Cable

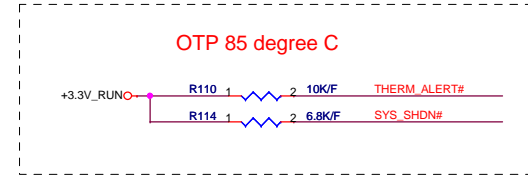


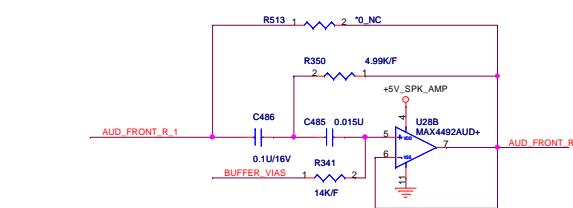
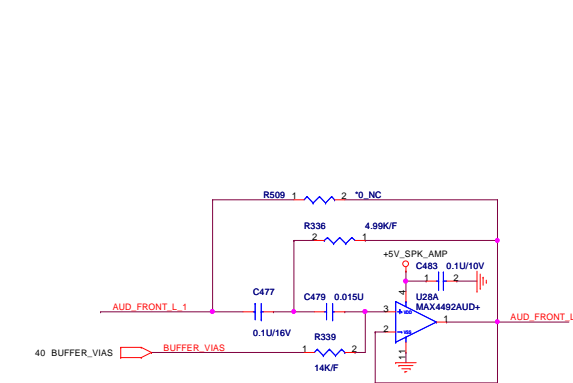
3VALW ON POWER LOGIC



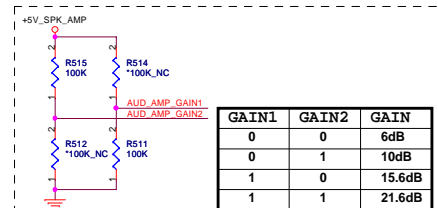
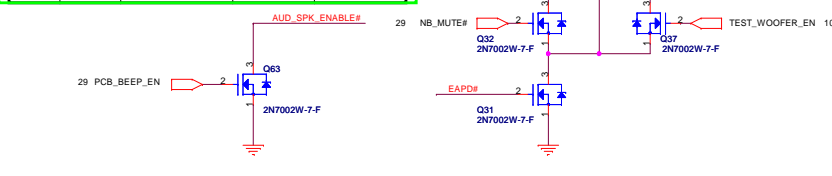


1.Place C160 close to EMC1422
 2.Place C518 to be close to Q51
 Total capacitance between D+/D- is 2200pF(max)
 if use 2200pF for C160, then C518 should be dummy

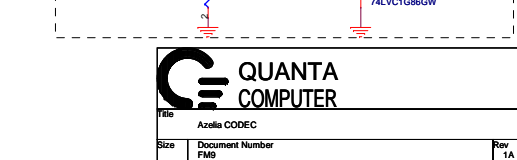
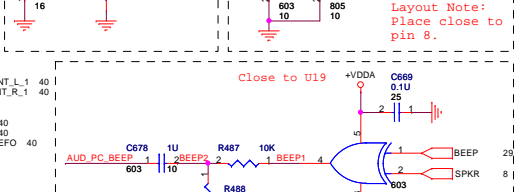
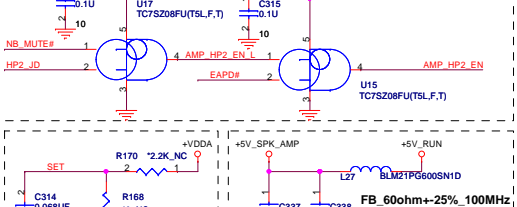
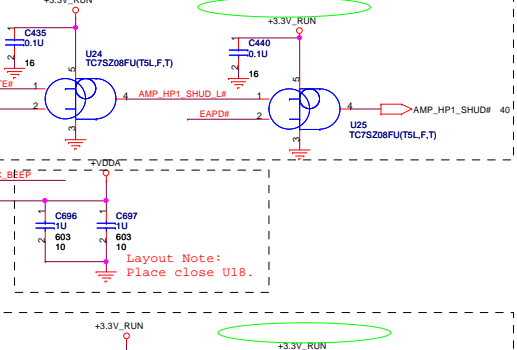
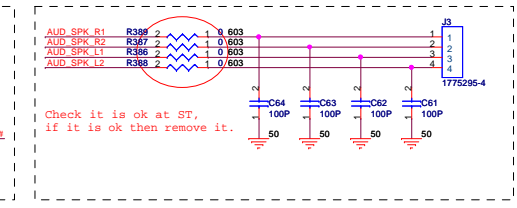
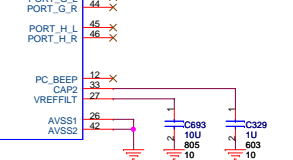
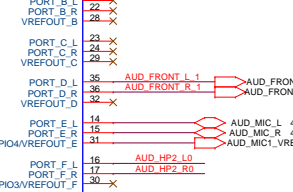
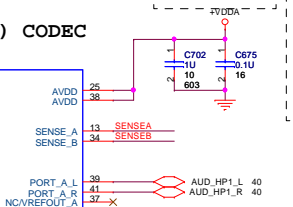
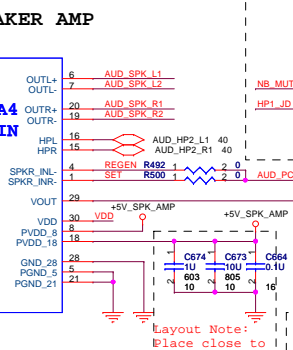
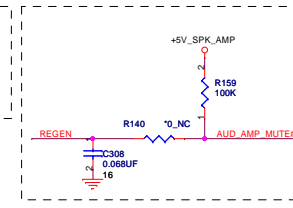
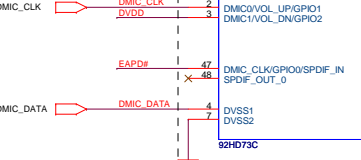
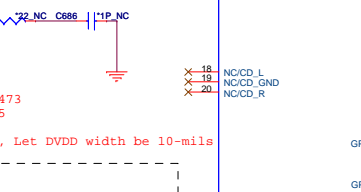
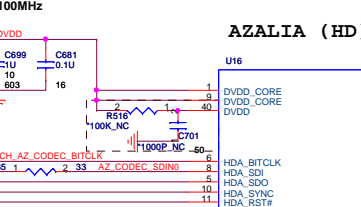
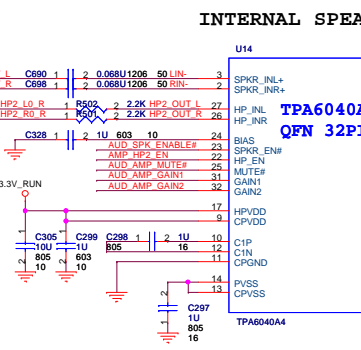
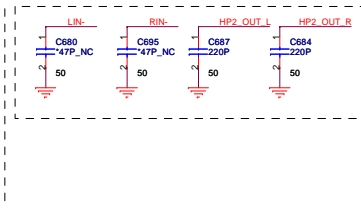
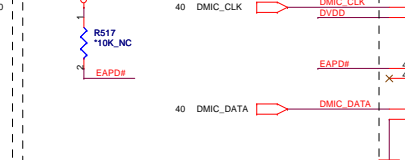
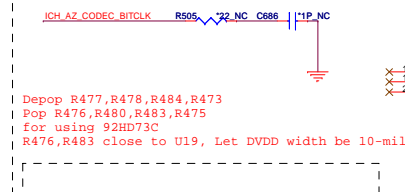
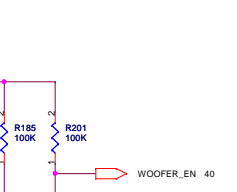
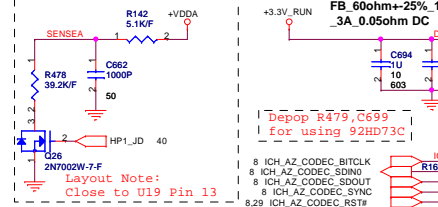
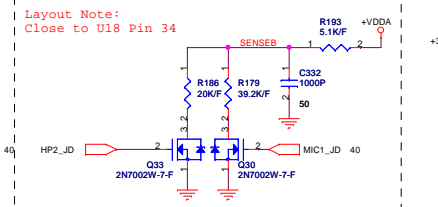
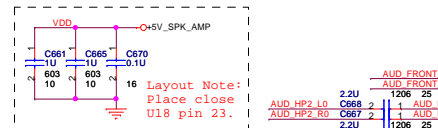




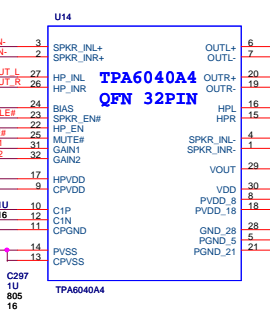
EAPD#	NB_MUTE#	TEST_WOOFER_EN	AUD_SPK_ENABLE#	SUB_MUTE#
0	0	0	H	L
0	0	1	H	L
0	1	0	H	L
0	1	1	H	L
1	0	0	H	L
1	0	1	H (Disable SPK)	H (Test Woofer)
1	1	0	L (Test SPK)	L (Disable Woofer)
1	1	1	L	H



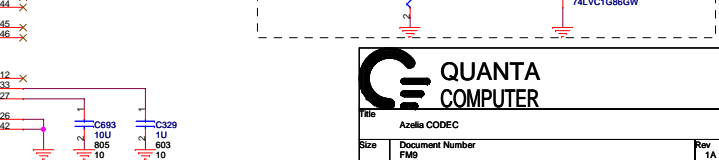
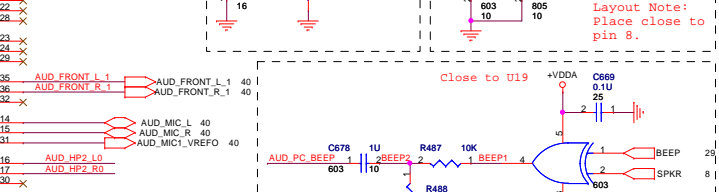
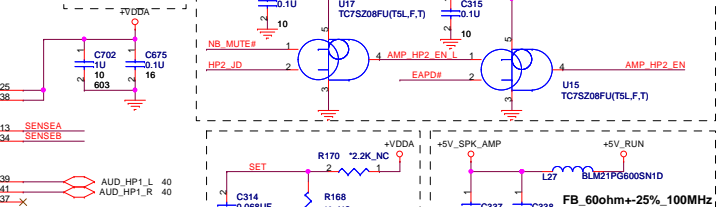
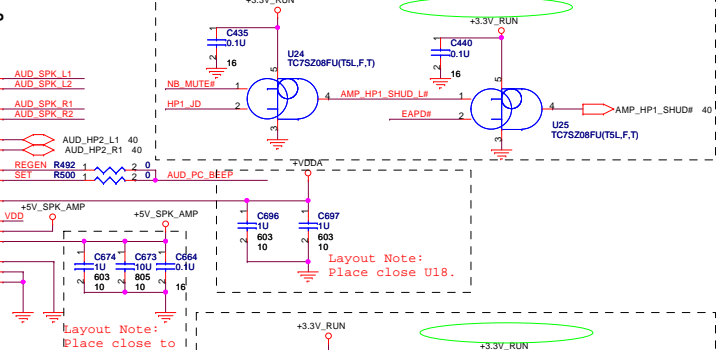
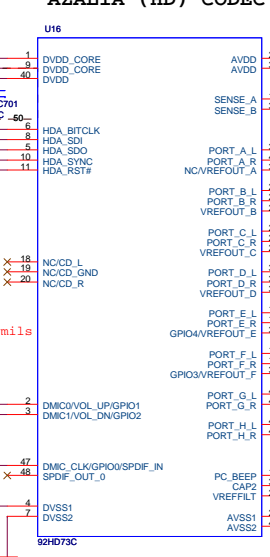
GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



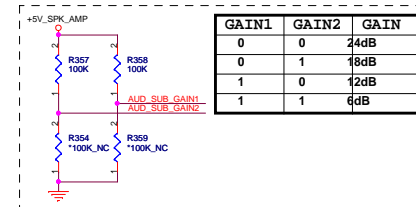
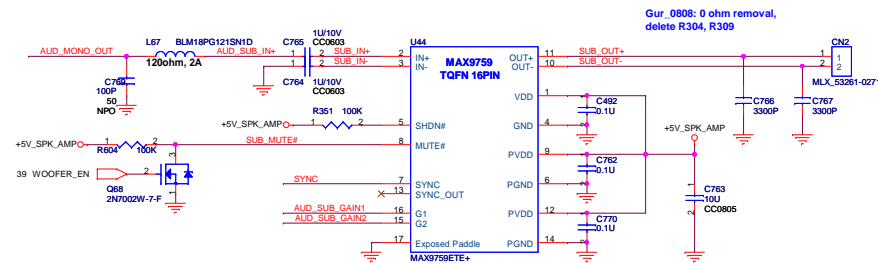
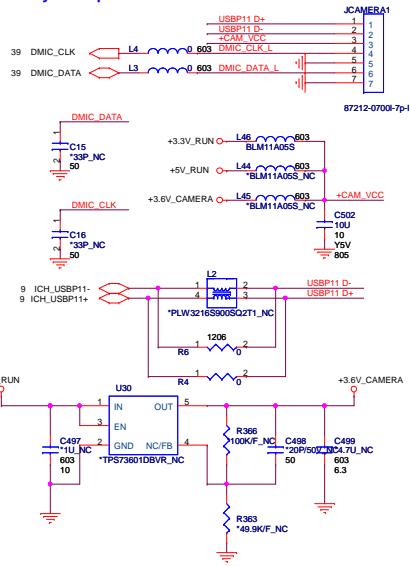
INTERNAL SPEAKER AMP



AZALIA (HD) CODEC

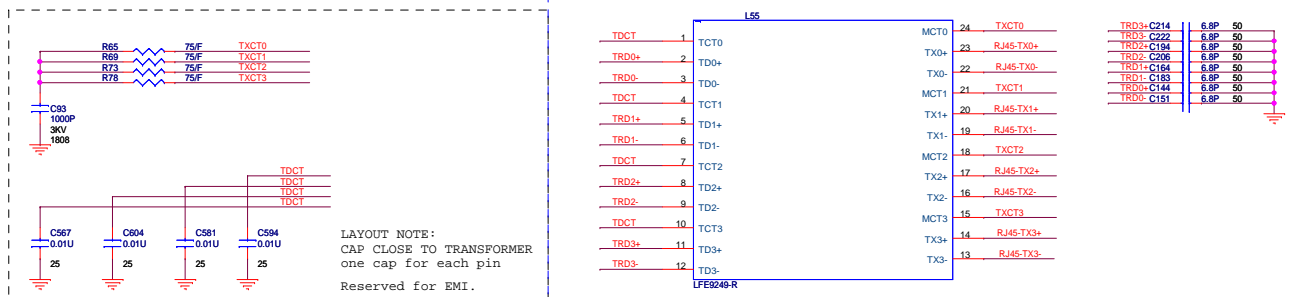
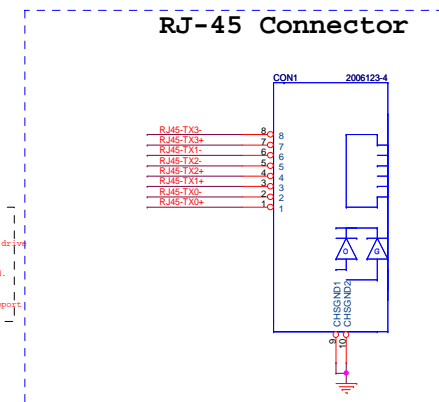
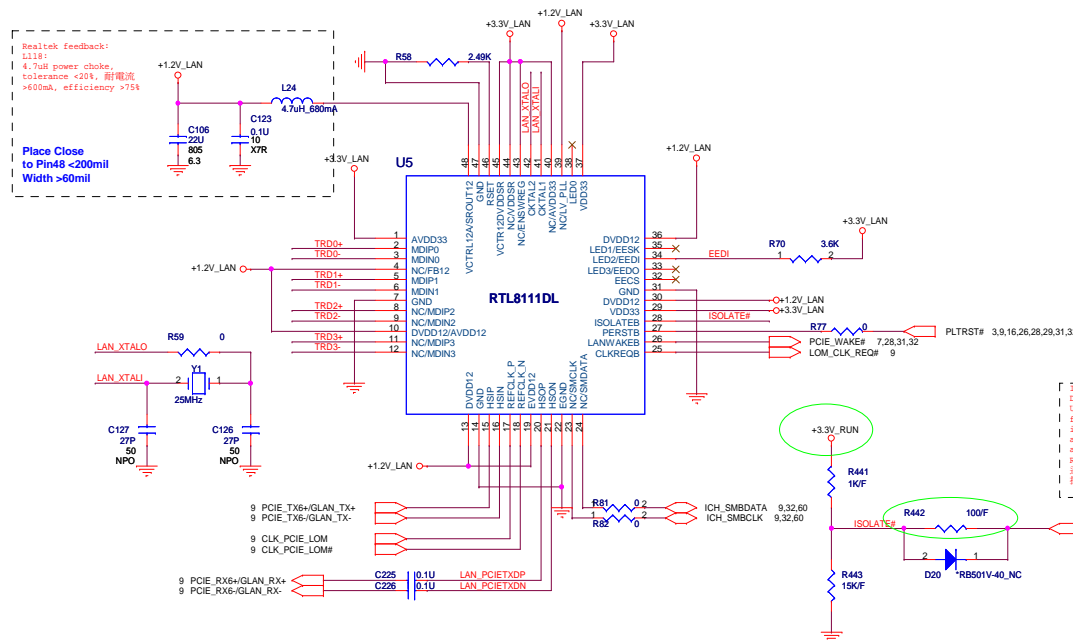
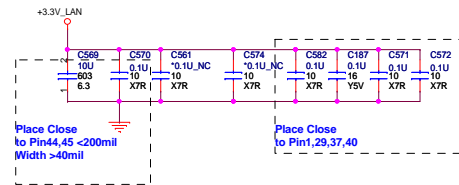
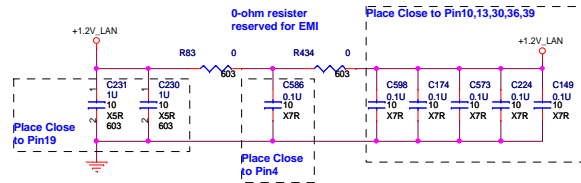


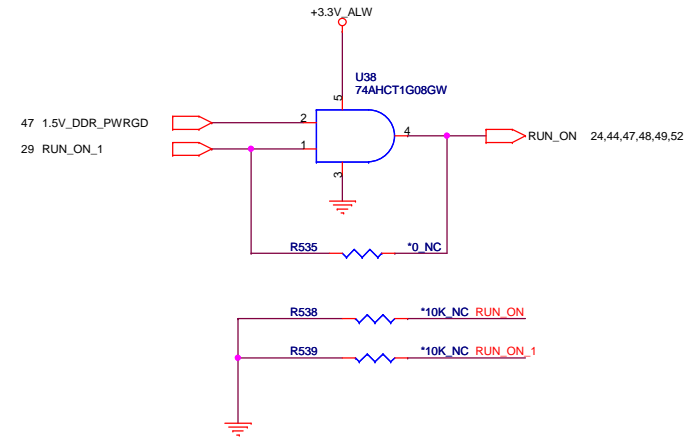
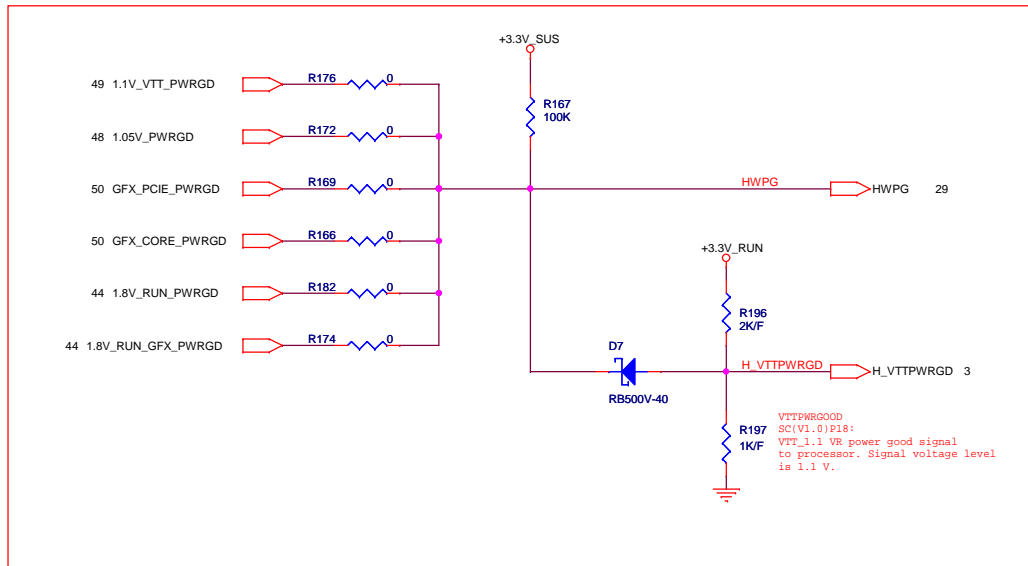
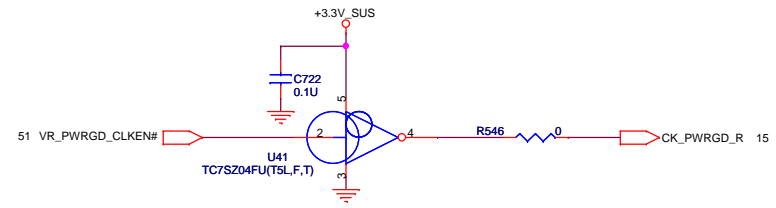
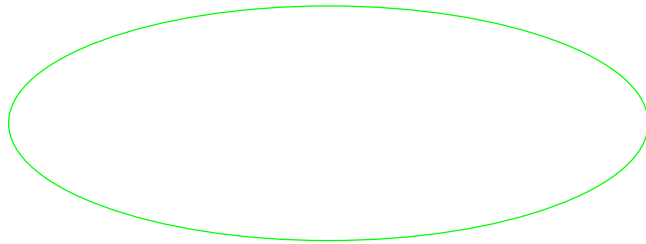
Array Microphone & Camera




GAIN1	GAIN2	GAIN
0	0	24dB
0	1	18dB
1	0	12dB
1	1	6dB

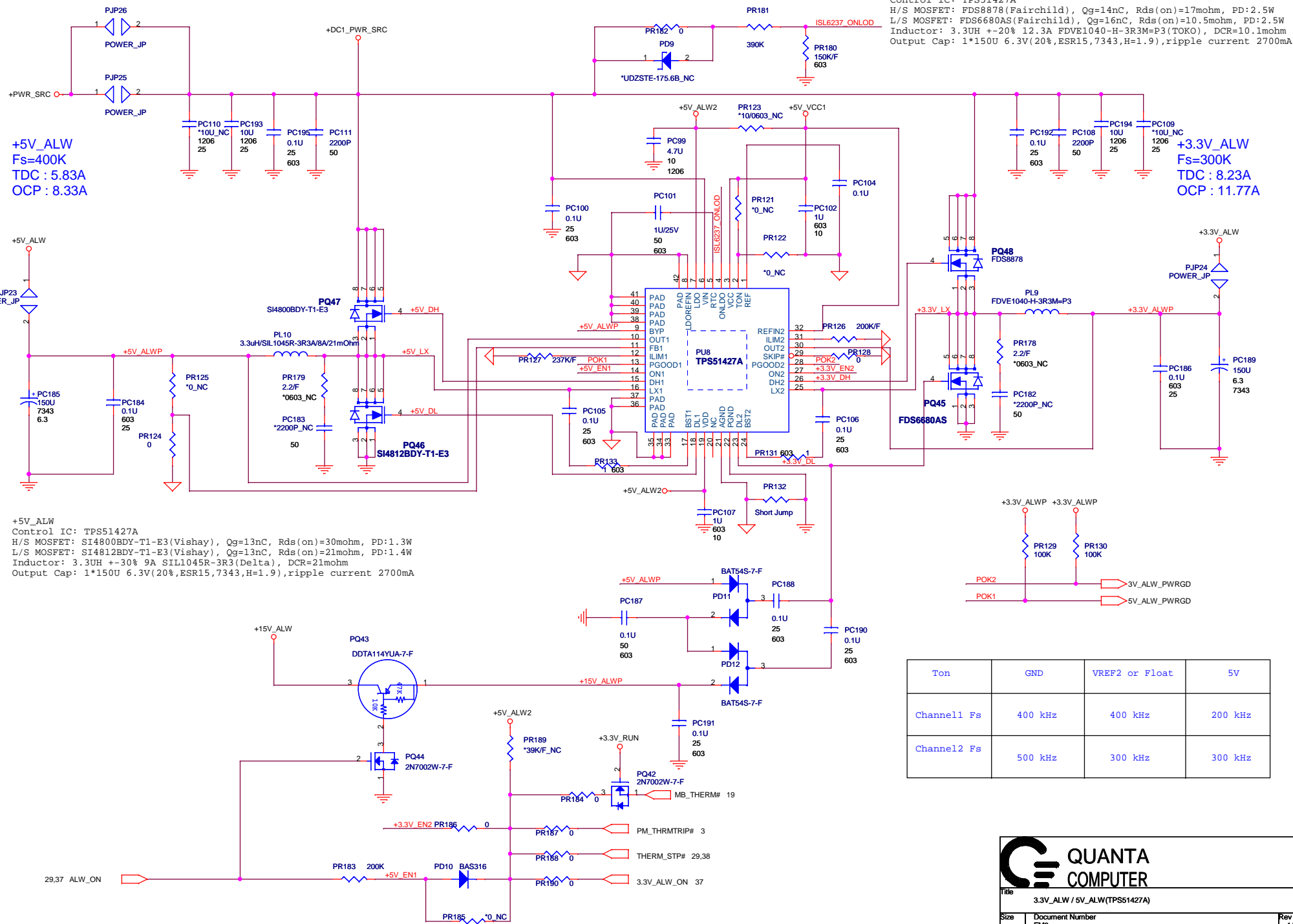






	1	2	3	4	5
A					
B					
C					
D					
	1	2	3	4	5

 <div> QUANTA COMPUTER </div>		
Title Battery Selector		
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Ton	GND	VREF2 or Float	5V
Channel1 Fs	400 kHz	400 kHz	200 kHz
Channel2 Fs	500 kHz	300 kHz	300 kHz



Title: 3.3V_ALW / 5V_ALW(TPS51427A)

Size: FMS

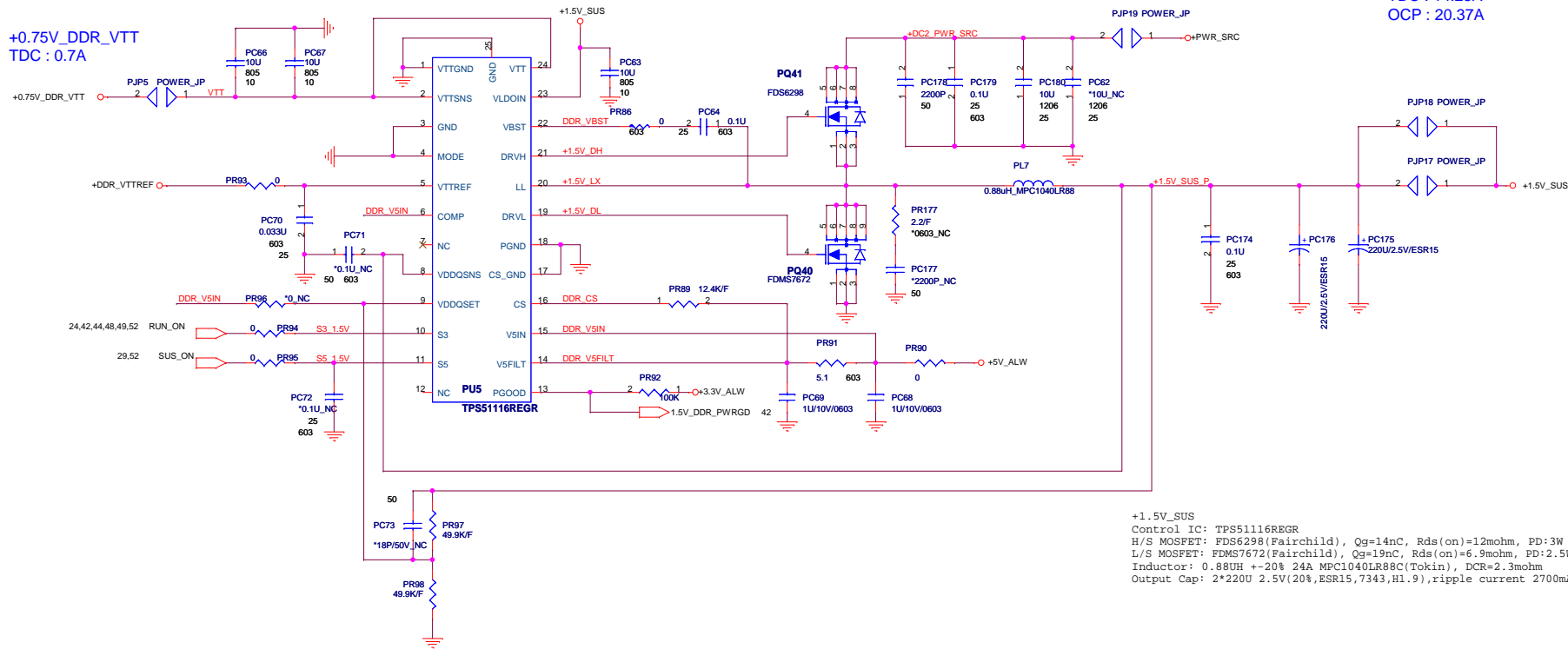
Document Number

Rev 1A

Date: Wednesday, March 04, 2009

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+0.75V_DDR_VTT
TDC : 0.7A



VDDQ and VTT discharge control

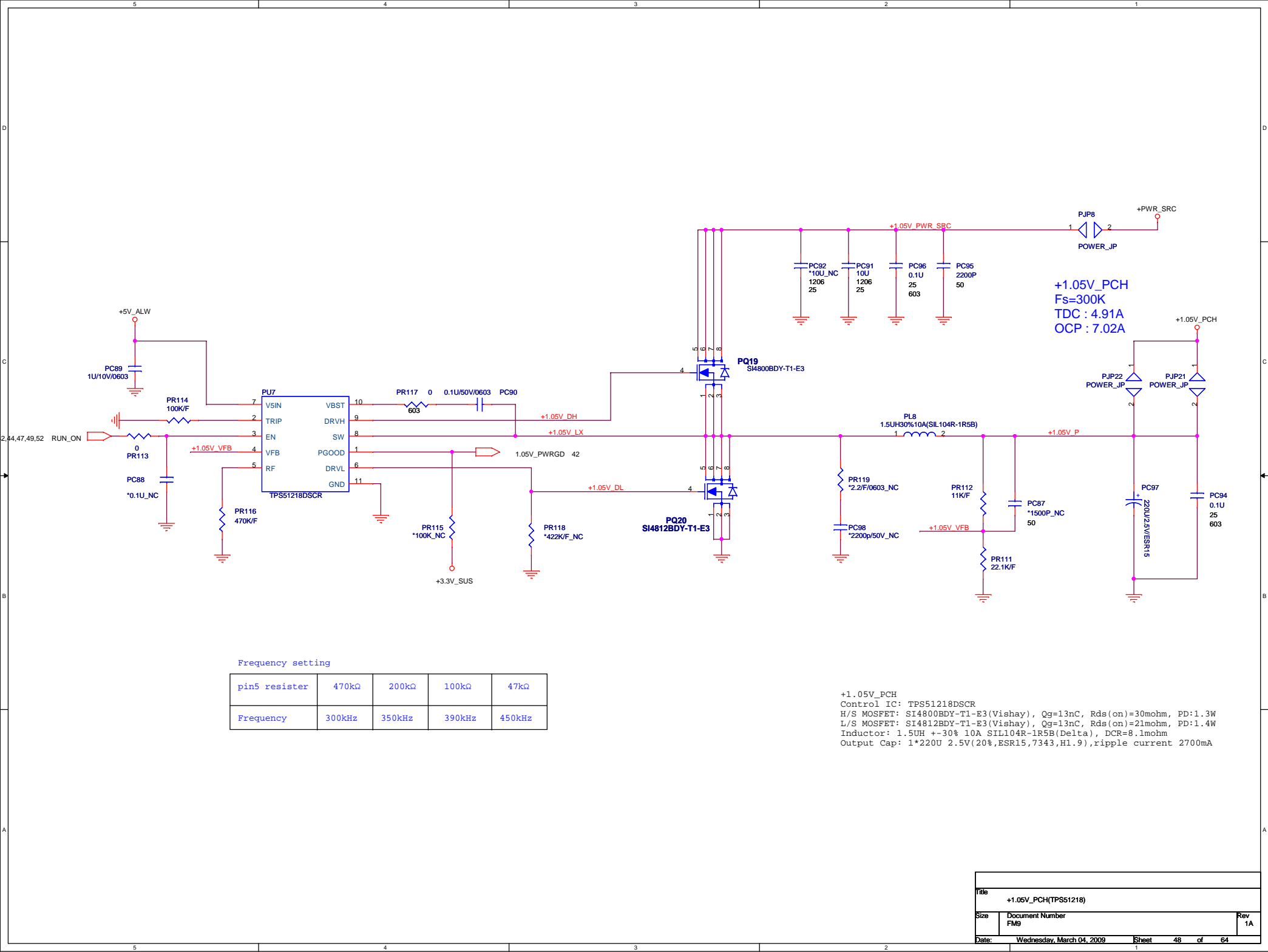
MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

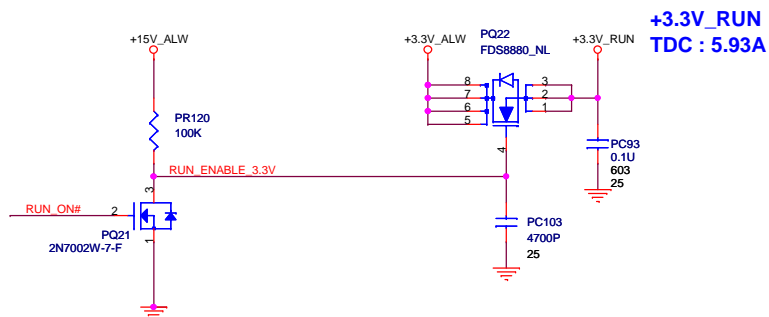
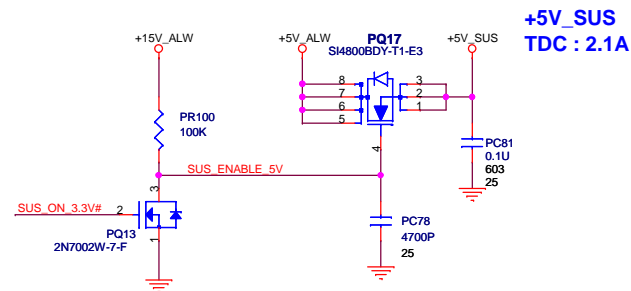
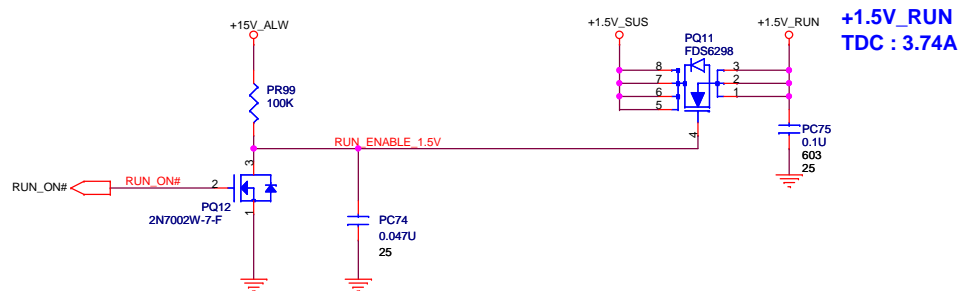
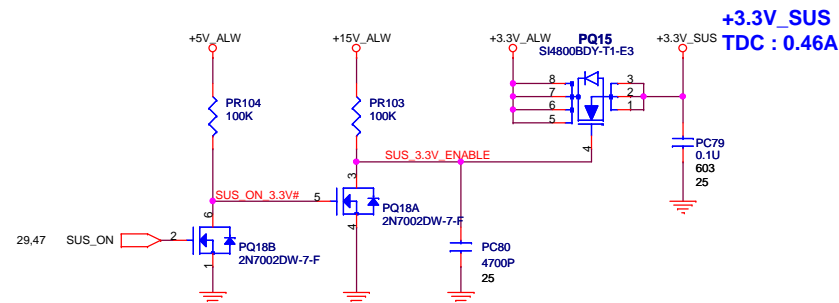
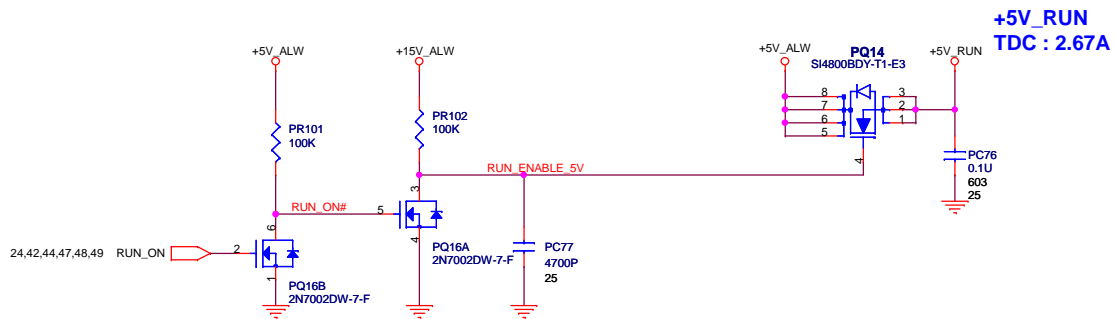
VDDQ output voltage selection

VDDQSET	VDDQ(V)	VTTREF and VTT	NOTE
GND	2.5V	VDDQSNS/2	DDR
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

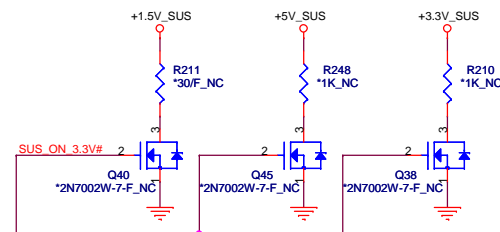
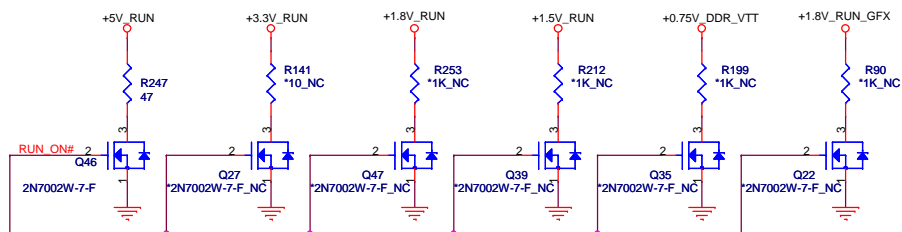
Outputs Management by S3, S5 control

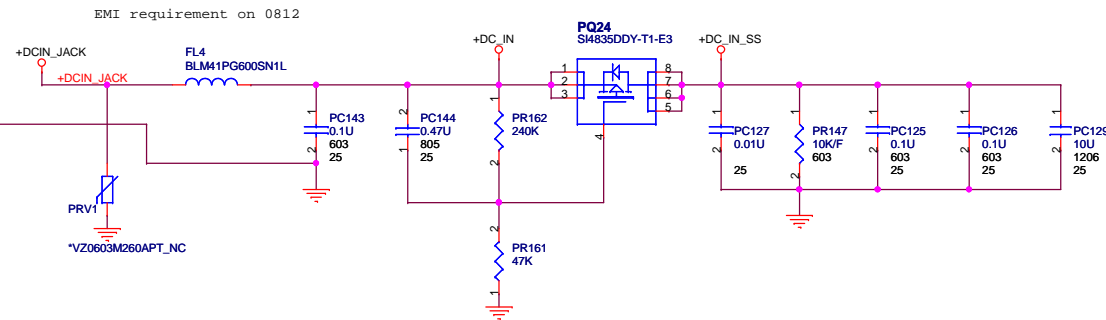
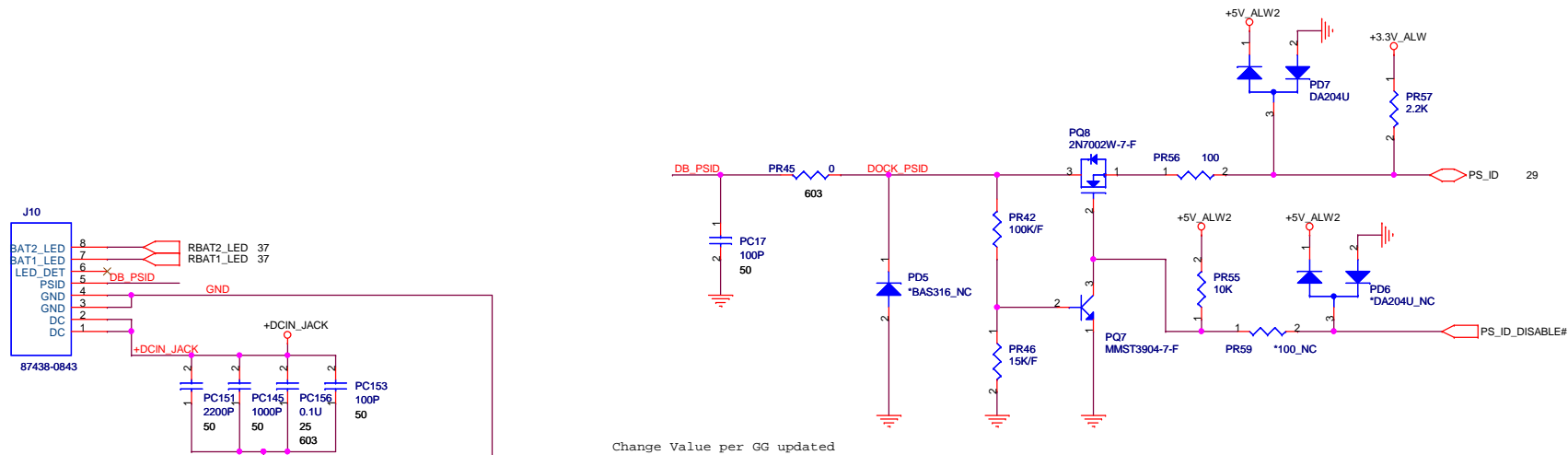
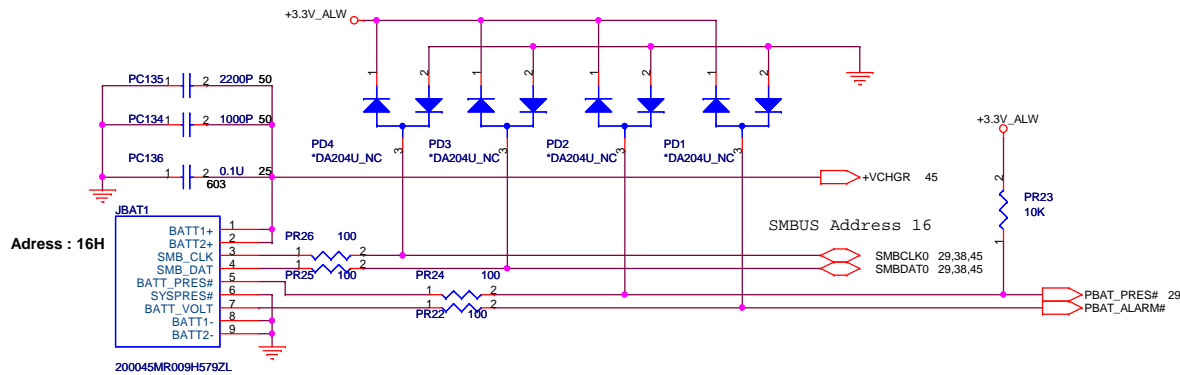
State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)





Reserve discharge path





Title
DCIN,BATT CONNECTOR

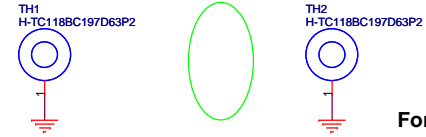
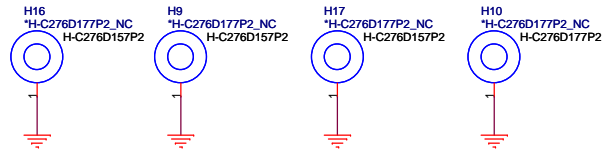
Size
Document Number
FM9

Rev
1A

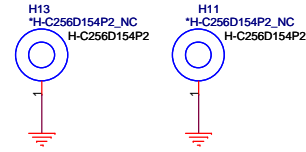
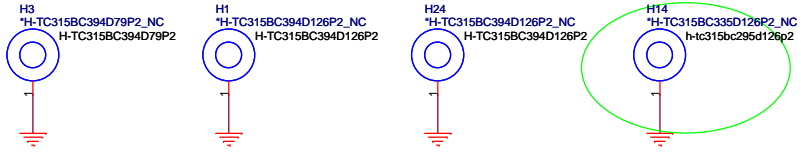
Date: Wednesday, March 04, 2009

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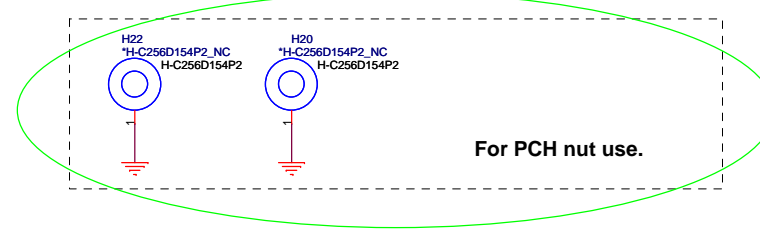
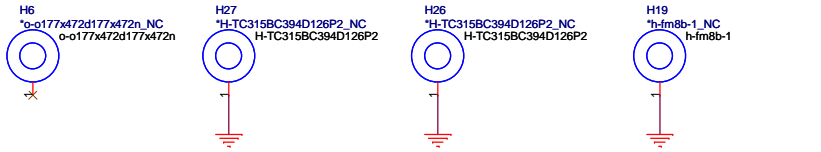
FOR CPU use



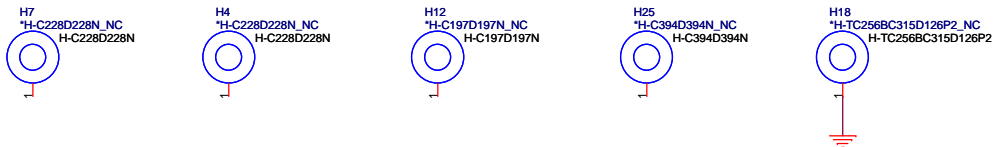
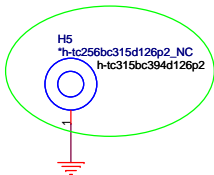
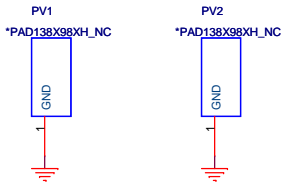
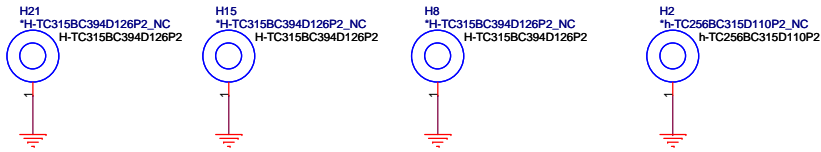
For MiniCard nut use.
on 31' header



For GPU nut use.




For PCH nut use.



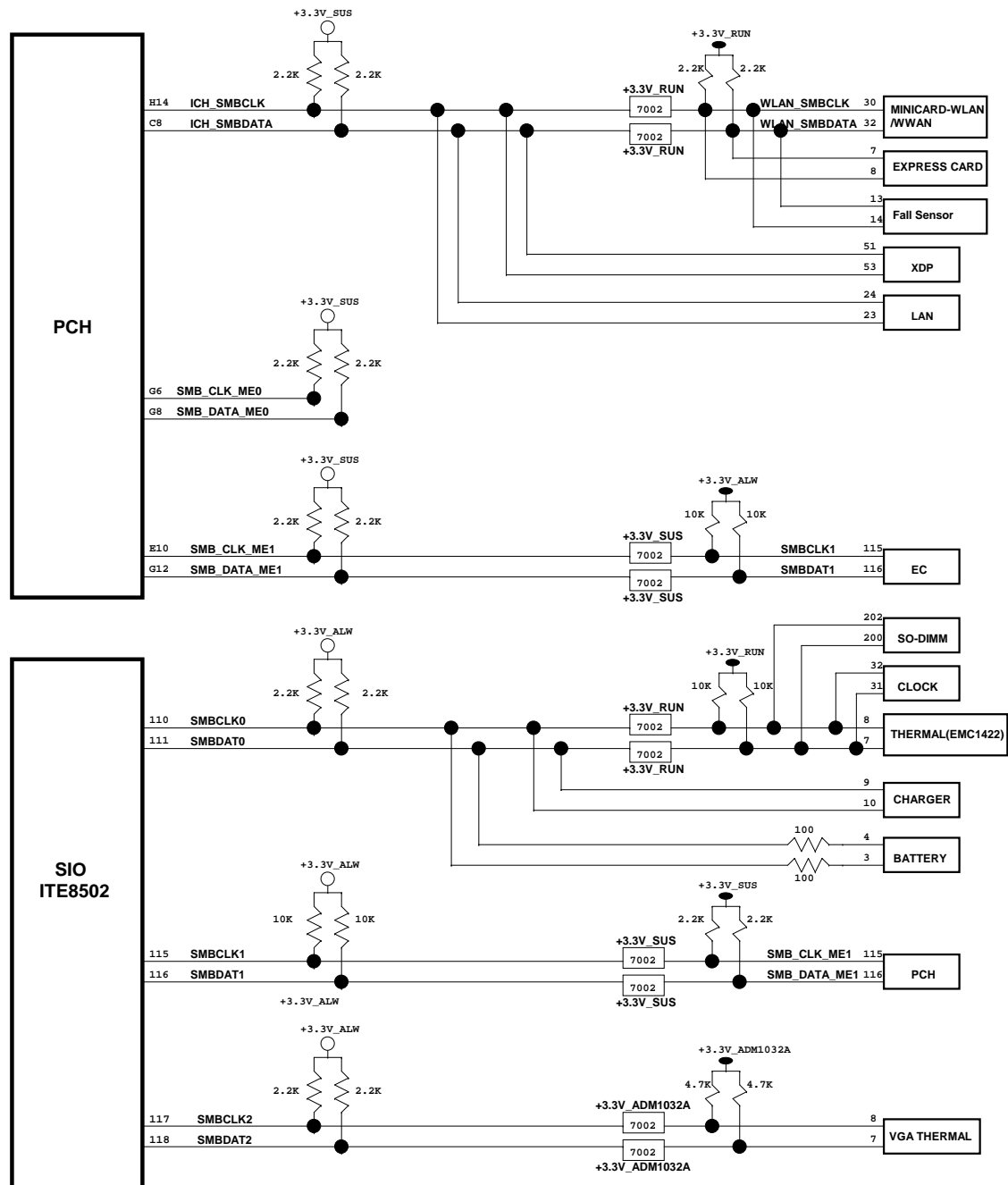
Title SCREW PAD		
Size FM9	Document Number FM9	Rev 1A
Date: Wednesday, March 04, 2009	Sheet 54	of 64

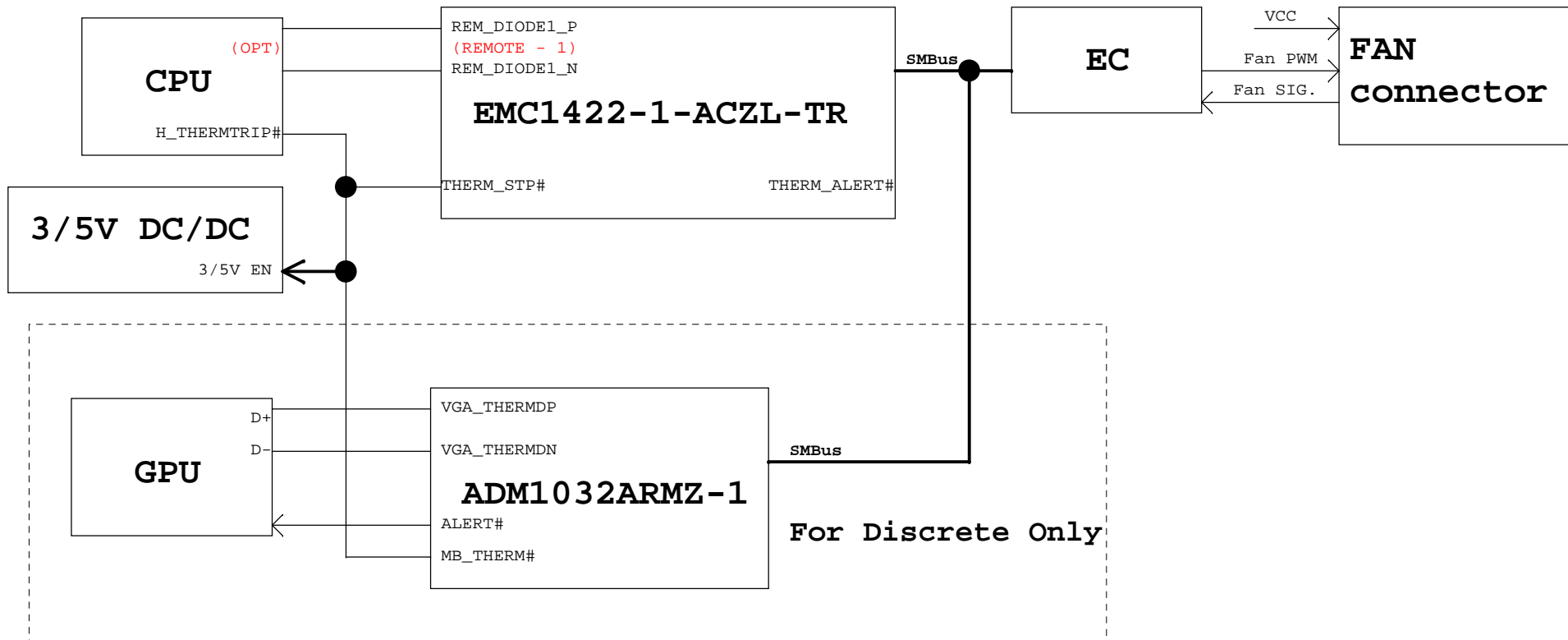
Reserved for EMI.

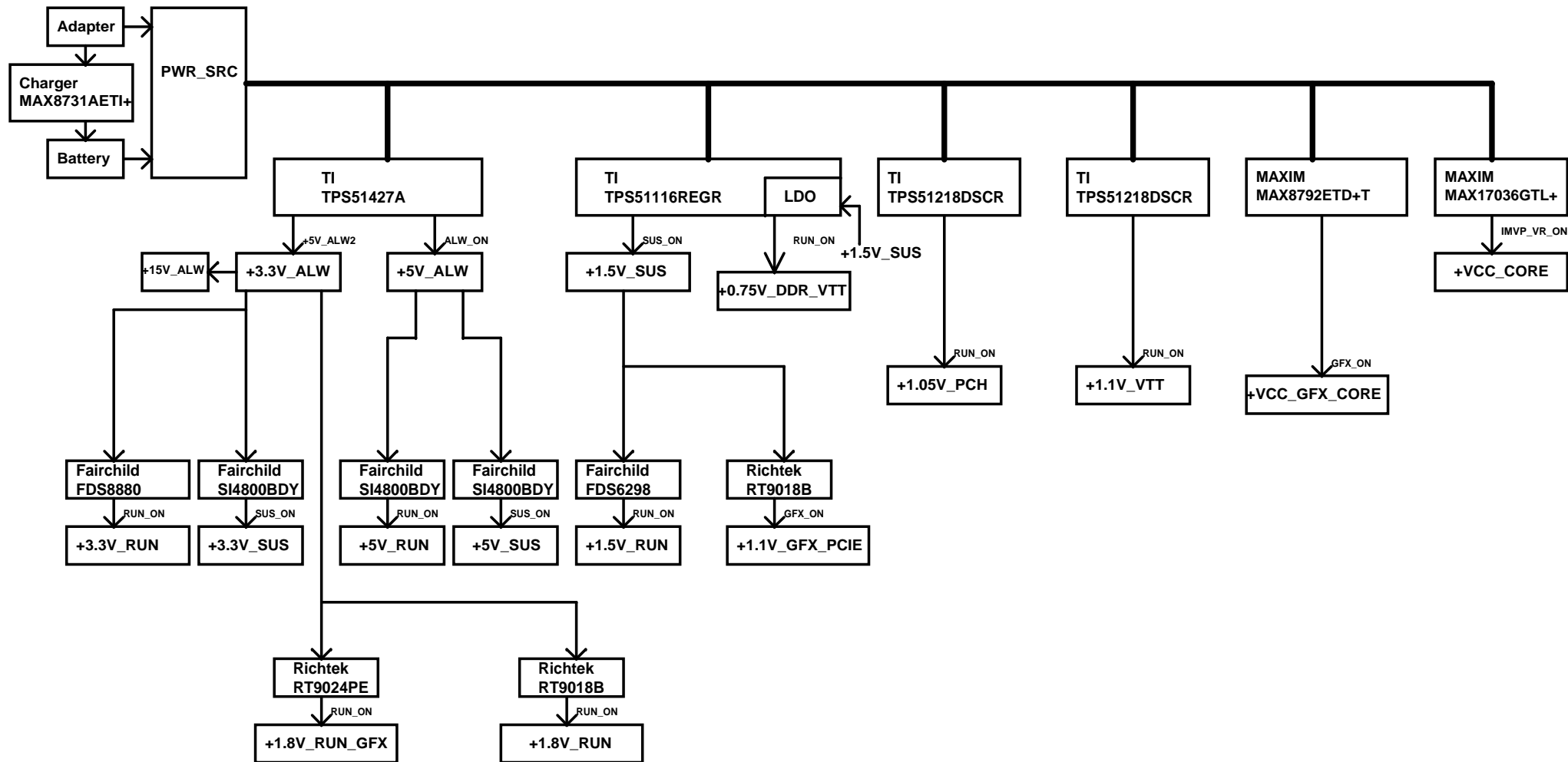


QUANTA
COMPUTER

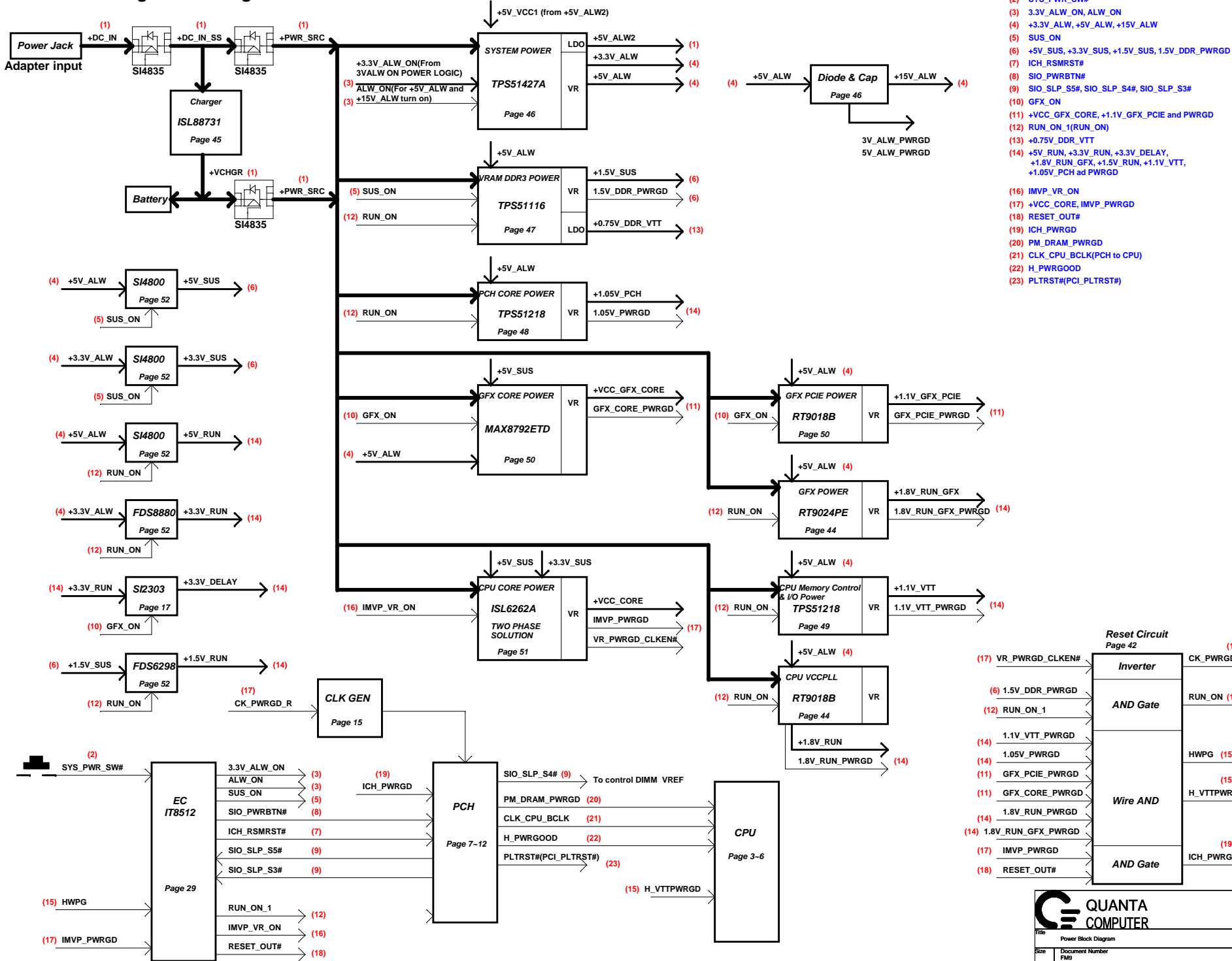
Title		
EMI CAP		
Size	Document Number	Rev
FM9		1A
Date:	Wednesday, March 04, 2009	Sheet 55 of 64







FM9 Power Design Block Diagram 2009/02/25



- (1) AC : DC_IN -> DC_IN_SS -> +PWR_SRC
- (2) Bat : +VCHGR -> +PWR_SRC, +5V_ALW2,
- (3) SYS_PWR_SW#
- (4) 3.3V_ALW_ON, ALW_ON
- (5) +3.3V_ALW, +5V_ALW, +15V_ALW
- (6) SUS_ON
- (7) +5V_SUS, +3.3V_SUS, +1.5V_SUS, 1.5V_DDR_PWRGD
- (8) ICH_RSMRST#
- (9) SIO_PWRBTN#
- (10) SIO_SLP_S5#, SIO_SLP_S4#, SIO_SLP_S3#
- (11) GFX_ON
- (12) +VCC_GFX_CORE, +1.1V_GFX_PCIE and PWRGD
- (13) RUN_ON_1(RUN_ON)
- (14) +0.75V_DDR_VTT
- (15) +5V_RUN, +3.3V_RUN, +3.3V_DELAY,
- (16) +1.8V_RUN_GFX, +1.5V_RUN, +1.1V_VTT,
- (17) +1.05V_PCH and PWRGD
- (18) IMVP_VR_ON
- (19) +VCC_CORE, IMVP_PWRGD
- (20) RESET_OUT#
- (21) ICH_PWRGD
- (22) PM_DRAM_PWRGD
- (23) CLK_CPU_BCLK(PCH to CPU)
- (24) H_PWRGOOD
- (25) PLTRST#(PCI_PLTRST#)

