


Thurman Discrete VGA nVidia G86 Schematics Document

uFCPGA Mobile Merom

Intel Crestline-PM + ICH8M

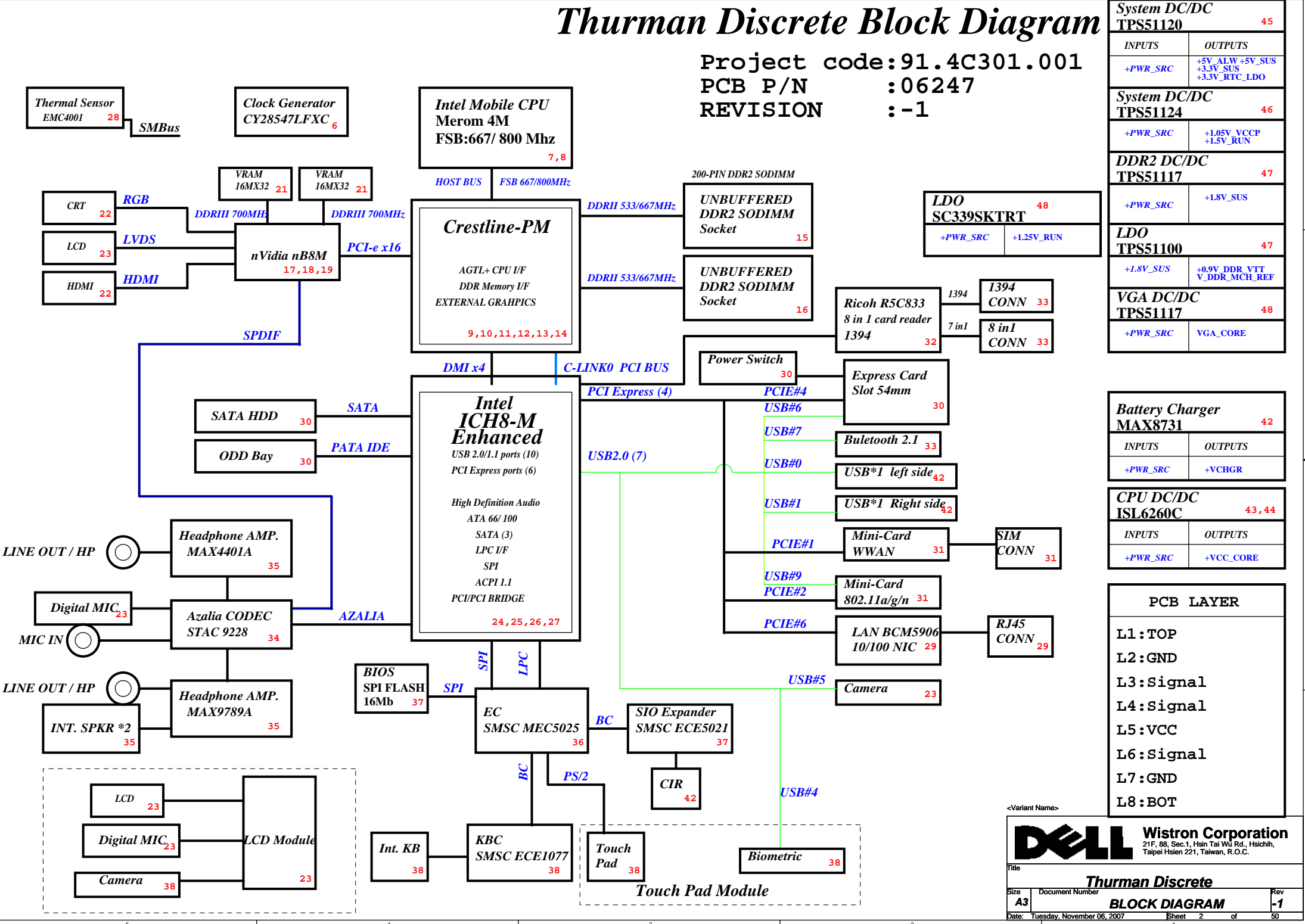
2007-11-06

REV : -1(DELL:A00)

<Variant Name>			
		Wistron Corporation <small>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>	
Title Thurman Discrete			
Size A3	Document Number COVER PAGE	Date: Tuesday, November 06, 2007	Rev -1
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Thurman Discrete Block Diagram

Project code: 91.4C301.001
 PCB P/N : 06247
 REVISION : -1



System DC/DC TPS51120		45
INPUTS	OUTPUTS	
+PWR_SRC	+5V_ALW +5V_SUS +3.3V_SUS +3.3V_RTC_LDO	
System DC/DC TPS51124		46
+PWR_SRC	+1.05V_VCCP +1.5V_RUN	
DDR2 DC/DC TPS51117		47
+PWR_SRC	+1.8V_SUS	
LDO TPS51100		47
+PWR_SRC	+1.25V_RUN	
+1.8V_SUS	+0.9V_DDR_VTT V_DDR_MCH_REF	
VGA DC/DC TPS51117		48
+PWR_SRC	VGA_CORE	

Battery Charger MAX8731		42
INPUTS	OUTPUTS	
+PWR_SRC	+VCHGR	

CPU DC/DC ISL6260C		43, 44
INPUTS	OUTPUTS	
+PWR_SRC	+VCC_CORE	

PCB LAYER	
L1: TOP	
L2: GND	
L3: Signal	
L4: Signal	
L5: VCC	
L6: Signal	
L7: GND	
L8: BOT	

<Variant Name>

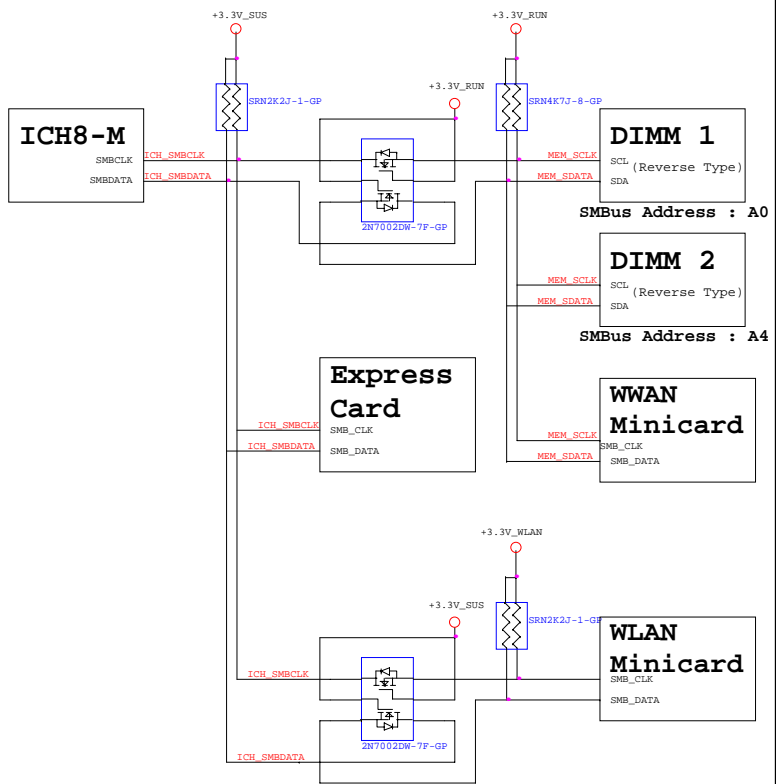
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Title: **Thurman Discrete**

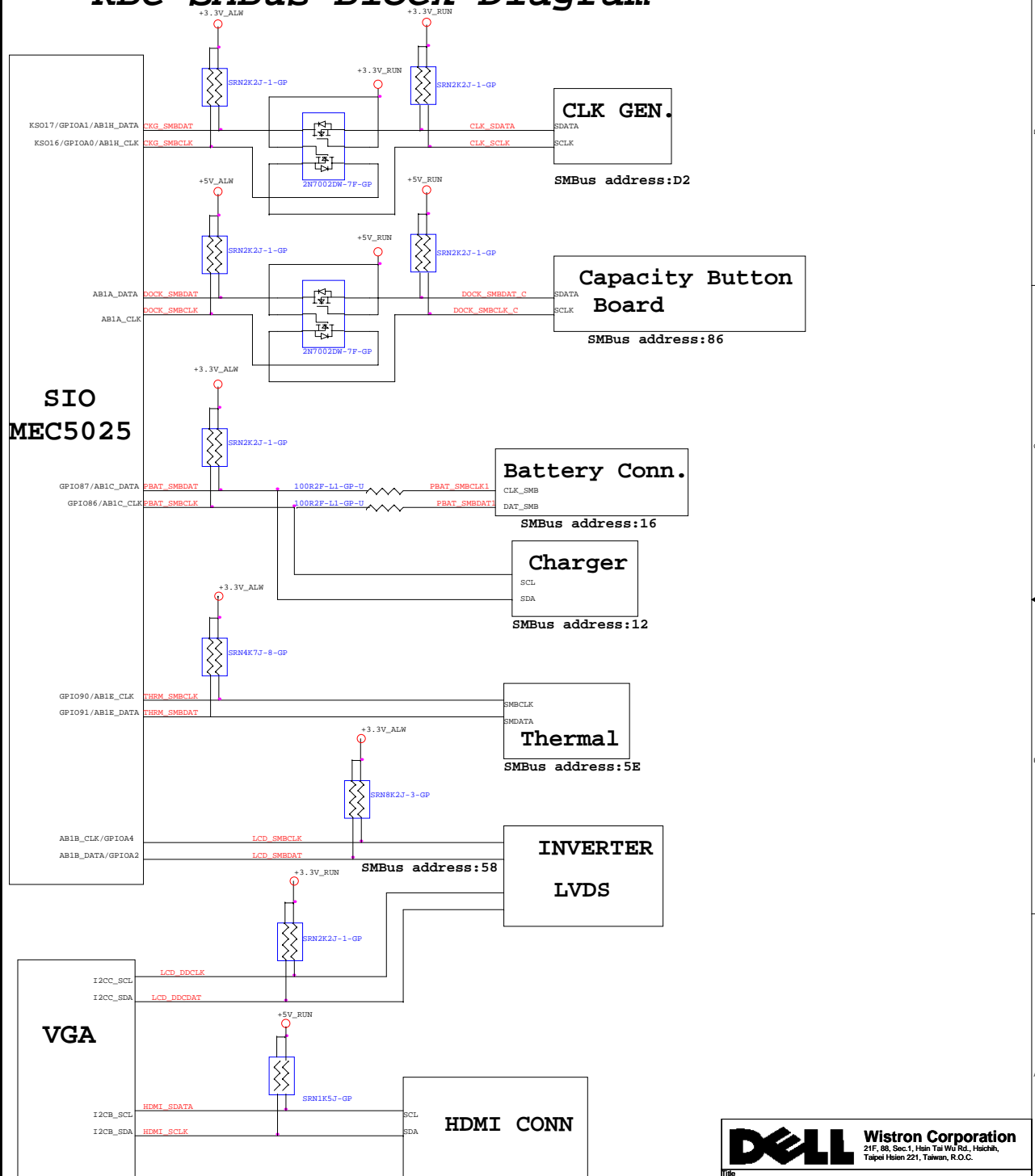
Size: **A3** Document Number: **BLOCK DIAGRAM** Rev: **-1**

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ICH8 SMBus Block Diagram



KBC SMBus Block Diagram



CLOCK GEN CY28547

27M_SS/LCD96_100M SELECTION TABLE

BYTE 10
 BYTE 15
 IO_VOUT[2,1,0]

bits S1	Bit4 S0	Spread Spectrum S1(10)
0	0	-0.5%(Default)
0	1	-1.0%
1	0	-1.5%
1	1	-2.0%

Bit2 IO_VOUT2	Bit1 IO_VOUT1	Bit0 IO_VOUT0	IO_VOUT[2,1,0]
0	0	0	0.3V
0	0	1	0.4V
0	1	0	0.5V
0	1	1	0.6V
1	0	0	0.7V
1	0	1	0.8V(Default)
1	1	0	0.9V
1	1	1	1.0V

PIN34 FCTSEL1	0 UMA	1 DISC.
PIN43	DOT96T	27M_NonSpread
PIN44	DOT96C	27M_Spread
PIN47	LCD100/96T	SRCT_0
PIN48	LCD100/96C	SRCC_0

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M

INTEL CRESTLINE STRAP PIN

* is Default setting

CFG Strap	Low	High
CFG 5	DMI X 2	DMI X 4 *
CFG 6	Moby Dick	Calistoga *
CFG 7	DT/Transportable CPU	Mobile CPU *
CFG 9	Reserved Lane	Normal Operation *
CFG 10	Reserved	Mobility *
CFG 11	Calistoga *	Reserved
CFG 16 FSB Dynamic ODT	Disabled	Enabled *
CFG 18 VCC Select	1.05V *	1.5V
CFG 19 DMI Lane Reserved	Normal Operation*	Reserved Lane
CFG 20 PCIE/SDVO Select	Only PCIE or SDVO is operation *	PCIE and SDVO are operation simu
SDVO_CTRLDATA	No SDVO Device present *	SDVO Device present

	CFG[13:12]
LL	Reserved
LH	XOR Mode Enabled
HL	All Z Mode Enabled
HH	Normal Operation*

PCIE Routing ICH USB TABLE

LANE1	MiniCard WWAN
LANE2	MiniCard WLAN
LANE3	No use
LANE4	Express Card
LANE5	No use
LANE6	10/100 LOM

USB0	USB1
USB1	USB2
USB2	
USB3	
USB4	Biometric
USB5	Camera
USB6	Express Card
USB7	BT
USB8	
USB9	MINI Card WWAN

PCI ROUTING

	IDSEL	INT	REQ	GNT
1394/MediaCard	AD17	C D	1	1

INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUIT	XOR Chain Entrance/PCIE Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIE Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCL1_5 VRM Enable/Disable.Always sampled.	Enables integrated VccSus1_05,VccSus1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIE LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overridden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

ICH_RSVDtp3	AZ DOUT ICH	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation(default)
1	1	Set PCIE port cofig bit1

A16 swap override strap		
PCI_GNT#3	low = A16 swap override enable	high = default

BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPT
1	0	DCT
1	1	LPC(Default)

integrated VccSus1_05,VccSus1_5,VccCL1_5		
SM_INTVRMEN	High=Enable	Low=Disable

integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable

DEFAULE HIGH

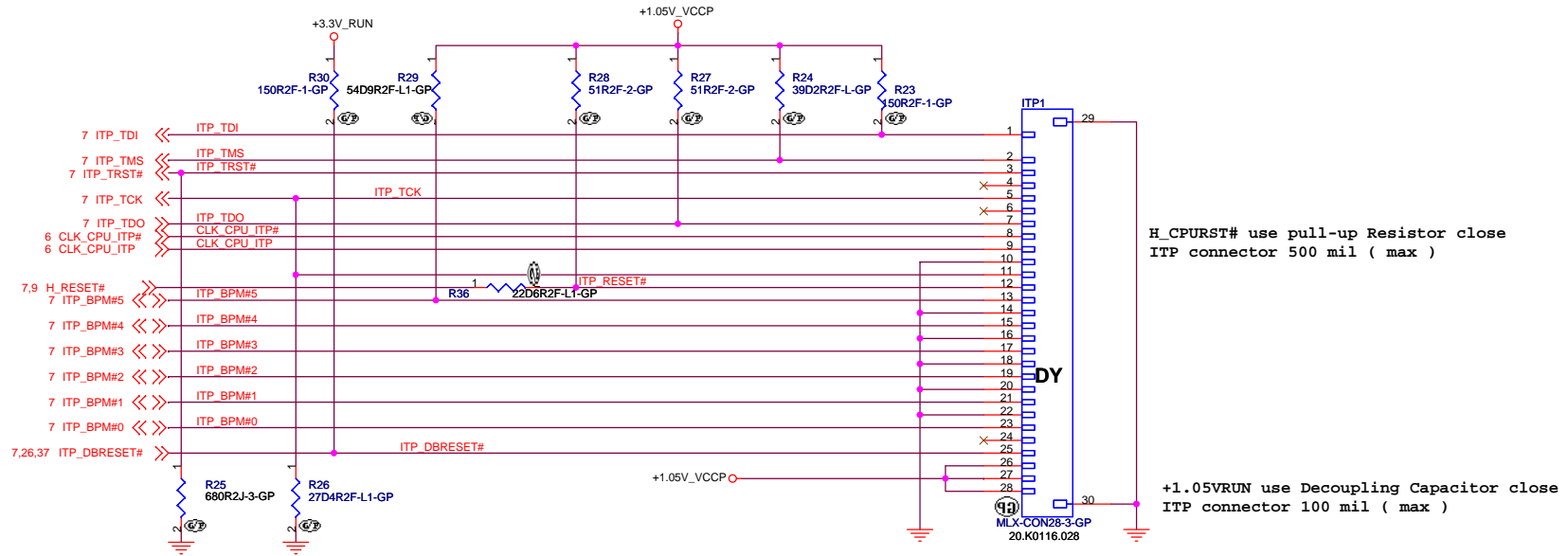
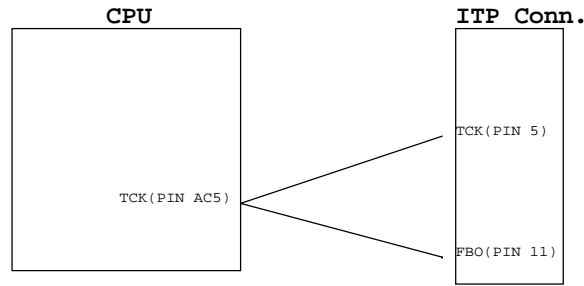
No Reboot Strap	
SPKR	LOW = Defaulte
	High=No Reboot

8.2K PULL HIGH

INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

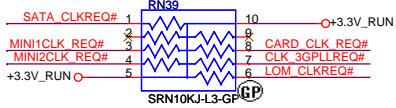
SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUIT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOST	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	TBD

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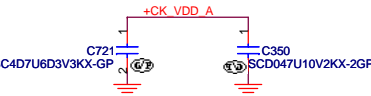


ITP Debug Conn.

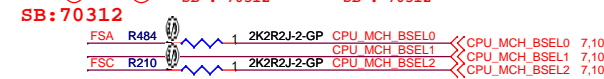
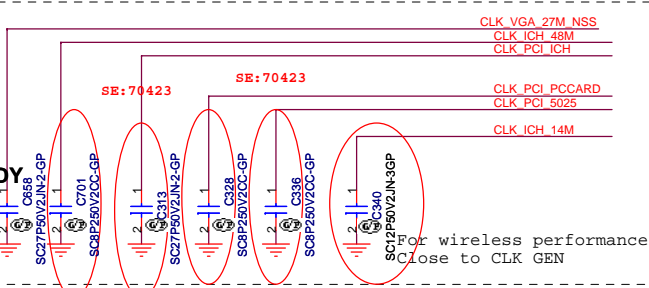
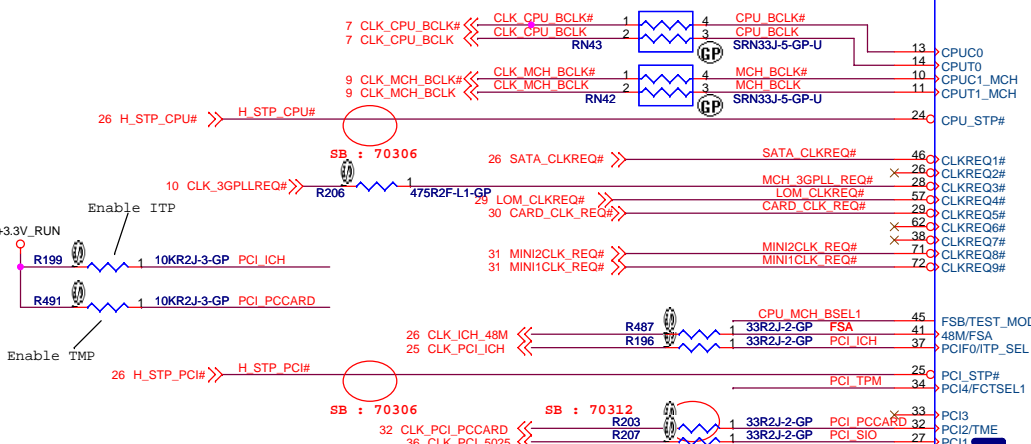
CLKREQ PULL HIGH



60ohm 100MHz
3000mA 0.05ohm DC



**Pull low to Decide
VTT_PWRGO Low active**



SEL2	SEL1	SEL0	CPU	FSB
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M

PIN34	FCTSEL1	0 UMA	1 DISC.
PIN43	DOT96T	27M_NonSpread	
PIN44	DOT96C	27M_Spread	
PIN47	LCD100/96T	SRCT_0	
PIN48	LCD100/96C	SRCC_0	

CLK_VGA_27M_NSS OPTION		
	G72	NB8M
R198	147 ohm 64.14705.6DL	33 ohm
R448	84.5 ohm	no-stuff
clk. Voltage	1.2V	3.3 V

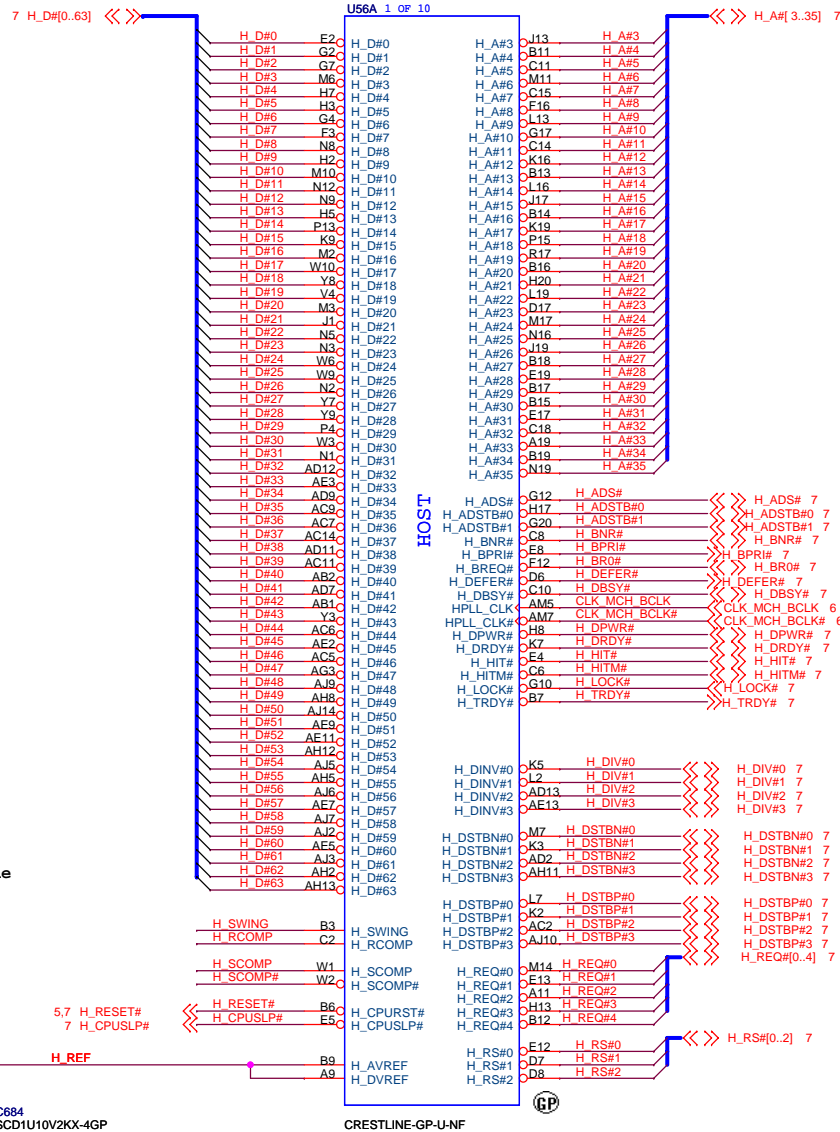
PIN9	PIN39
PGMODE	DISCRIPTION
0	VTT_PWRGD#/PD
1	CKPWRGD/PD# (DEFAULT)

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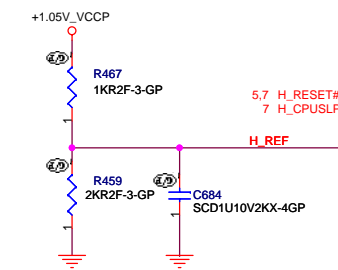
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Size A3 Document Number **CLK_GEN CY28547** Rev -1

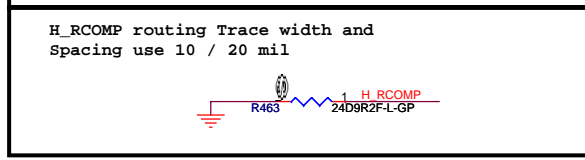
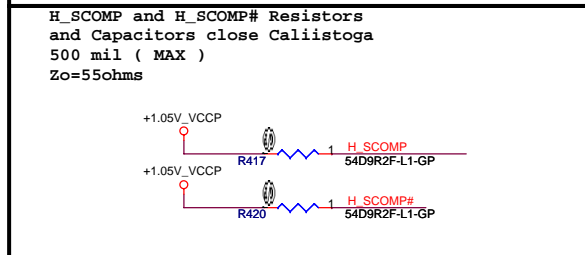
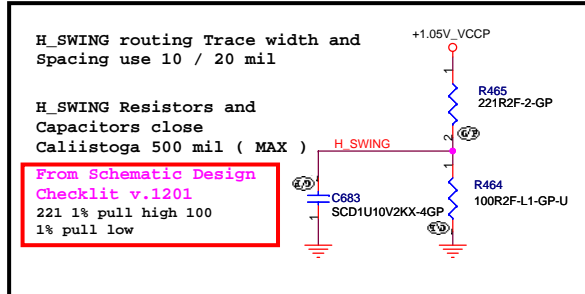
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H_REF Decoupling Crestline close Crestline 100 mil



Change to 71.CREB.T.M03



<Variant Name>

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Size: **A3** Document Number: **GMCH-FSB LIBC (1/6)** Rev: **-1**

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15 DDR_A_D[0..63] <<>> DDR_A_D[0..63]

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DDR A D0	AR43	SA_DQ0
DDR A D1	AW44	SA_DQ1
DDR A D2	BA45	SA_DQ2
DDR A D3	AY46	SA_DQ3
DDR A D4	AR41	SA_DQ4
DDR A D5	AR45	SA_DQ5
DDR A D6	AT42	SA_DQ6
DDR A D7	AW47	SA_DQ7
DDR A D8	BA45	SA_DQ8
DDR A D9	BF48	SA_DQ9
DDR A D10	BG47	SA_DQ10
DDR A D11	BJ45	SA_DQ11
DDR A D12	BB47	SA_DQ12
DDR A D13	BG50	SA_DQ13
DDR A D14	BH49	SA_DQ14
DDR A D15	BE45	SA_DQ15
DDR A D16	AW43	SA_DQ16
DDR A D17	BE44	SA_DQ17
DDR A D18	BG42	SA_DQ18
DDR A D19	BE40	SA_DQ19
DDR A D20	BE44	SA_DQ20
DDR A D21	BH45	SA_DQ21
DDR A D22	BG40	SA_DQ22
DDR A D23	BF40	SA_DQ23
DDR A D24	AR40	SA_DQ24
DDR A D25	AW40	SA_DQ25
DDR A D26	AT39	SA_DQ26
DDR A D27	AW36	SA_DQ27
DDR A D28	AW41	SA_DQ28
DDR A D29	AY41	SA_DQ29
DDR A D30	AV38	SA_DQ30
DDR A D31	AT38	SA_DQ31
DDR A D32	AV13	SA_DQ32
DDR A D33	AT13	SA_DQ33
DDR A D34	AW11	SA_DQ34
DDR A D35	AV11	SA_DQ35
DDR A D36	AU15	SA_DQ36
DDR A D37	AT11	SA_DQ37
DDR A D38	BA13	SA_DQ38
DDR A D39	BA11	SA_DQ39
DDR A D40	BE10	SA_DQ40
DDR A D41	BD10	SA_DQ41
DDR A D42	BD8	SA_DQ42
DDR A D43	AY9	SA_DQ43
DDR A D44	BG10	SA_DQ44
DDR A D45	AW9	SA_DQ45
DDR A D46	BD7	SA_DQ46
DDR A D47	BB9	SA_DQ47
DDR A D48	BB5	SA_DQ48
DDR A D49	AY7	SA_DQ49
DDR A D50	AT5	SA_DQ50
DDR A D51	AT7	SA_DQ51
DDR A D52	AY6	SA_DQ52
DDR A D53	BB7	SA_DQ53
DDR A D54	AR5	SA_DQ54
DDR A D55	AR8	SA_DQ55
DDR A D56	AR9	SA_DQ56
DDR A D57	AN3	SA_DQ57
DDR A D58	AM8	SA_DQ58
DDR A D59	AN10	SA_DQ59
DDR A D60	AT9	SA_DQ60
DDR A D61	AN9	SA_DQ61
DDR A D62	AM9	SA_DQ62
DDR A D63	AN11	SA_DQ63

DDR SYSTEM MEMORY A

SA_BS0	SA_BS1	SA_BS2	SA_CAS#	SA_DM0	SA_DM1	SA_DM2	SA_DM3	SA_DM4	SA_DM5	SA_DM6	SA_DM7	SA_DQS0	SA_DQS1	SA_DQS2	SA_DQS3	SA_DQS4	SA_DQS5	SA_DQS6	SA_DQS7	SA_DQS#0	SA_DQS#1	SA_DQS#2	SA_DQS#3	SA_DQS#4	SA_DQS#5	SA_DQS#6	SA_DQS#7	SA_MA0	SA_MA1	SA_MA2	SA_MA3	SA_MA4	SA_MA5	SA_MA6	SA_MA7	SA_MA8	SA_MA9	SA_MA10	SA_MA11	SA_MA12	SA_MA13	SA_MA14	SA_RAS#	SA_RCVEN#	SA_WE#
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BB19	DDR A BS0	DDR A BS[0..2]	BL17	DDR A CAS#	AT45	DDR A DM0	BD44	DDR A DM1	BD42	DDR A DM2	AW38	DDR A DM3	AW13	DDR A DM4	BG8	DDR A DM5	AY5	DDR A DM6	AN6	DDR A DM7	AT46	DDR A DQS0	BE48	DDR A DQS1	BB43	DDR A DQS2	BC37	DDR A DQS3	BB16	DDR A DQS4	BH6	DDR A DQS5	BB2	DDR A DQS6	AP3	DDR A DQS7	AT47	DDR A DQS#0	BD47	DDR A DQS#1	BC41	DDR A DQS#2	BA37	DDR A DQS#3	BA16	DDR A DQS#4	BH7	DDR A DQS#5	BC1	DDR A DQS#6	AP2	DDR A DQS#7	B119	DDR A MA0	BD20	DDR A MA1	BK27	DDR A MA2	BH28	DDR A MA3	BL24	DDR A MA4	BK28	DDR A MA5	BJ27	DDR A MA6	BJ25	DDR A MA7	BL28	DDR A MA8	BA28	DDR A MA9	BC19	DDR A MA10	BE28	DDR A MA11	BG30	DDR A MA12	BJ16	DDR A MA13	BJ29	DDR A MA14	BE18	DDR A RAS#	AY20	M_A_RCVEN#	TP6	BA19	DDR A WE#
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CRESTLINE-GP-U-NF



16 DDR_B_D[0..63] <<>> DDR_B_D[0..63]

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DDR B D0	AP49	SB_DQ0
DDR B D1	AR51	SB_DQ1
DDR B D2	AW50	SB_DQ2
DDR B D3	AW51	SB_DQ3
DDR B D4	AN51	SB_DQ4
DDR B D5	AN50	SB_DQ5
DDR B D6	AV50	SB_DQ6
DDR B D7	AV49	SB_DQ7
DDR B D8	BA50	SB_DQ8
DDR B D9	BB50	SB_DQ9
DDR B D10	BA49	SB_DQ10
DDR B D11	BE50	SB_DQ11
DDR B D12	BA51	SB_DQ12
DDR B D13	AY49	SB_DQ13
DDR B D14	BE50	SB_DQ14
DDR B D15	BE49	SB_DQ15
DDR B D16	BJ50	SB_DQ16
DDR B D17	BJ44	SB_DQ17
DDR B D18	BJ43	SB_DQ18
DDR B D19	BL43	SB_DQ19
DDR B D20	BK47	SB_DQ20
DDR B D21	BK49	SB_DQ21
DDR B D22	BK43	SB_DQ22
DDR B D23	BK42	SB_DQ23
DDR B D24	BJ41	SB_DQ24
DDR B D25	BL41	SB_DQ25
DDR B D26	BJ37	SB_DQ26
DDR B D27	BJ36	SB_DQ27
DDR B D28	BK41	SB_DQ28
DDR B D29	BJ40	SB_DQ29
DDR B D30	BL35	SB_DQ30
DDR B D31	BK37	SB_DQ31
DDR B D32	BK13	SB_DQ32
DDR B D33	BE11	SB_DQ33
DDR B D34	BK11	SB_DQ34
DDR B D35	BC11	SB_DQ35
DDR B D36	BC13	SB_DQ36
DDR B D37	BE12	SB_DQ37
DDR B D38	BC12	SB_DQ38
DDR B D39	BG12	SB_DQ39
DDR B D40	BJ10	SB_DQ40
DDR B D41	BL9	SB_DQ41
DDR B D42	BK5	SB_DQ42
DDR B D43	BL5	SB_DQ43
DDR B D44	BK9	SB_DQ44
DDR B D45	BK10	SB_DQ45
DDR B D46	BJ8	SB_DQ46
DDR B D47	BJ6	SB_DQ47
DDR B D48	BF4	SB_DQ48
DDR B D49	BH5	SB_DQ49
DDR B D50	BG1	SB_DQ50
DDR B D51	BC2	SB_DQ51
DDR B D52	BK3	SB_DQ52
DDR B D53	BE4	SB_DQ53
DDR B D54	BD3	SB_DQ54
DDR B D55	BJ2	SB_DQ55
DDR B D56	BA3	SB_DQ56
DDR B D57	BB3	SB_DQ57
DDR B D58	AR1	SB_DQ58
DDR B D59	AT3	SB_DQ59
DDR B D60	AY2	SB_DQ60
DDR B D61	AY3	SB_DQ61
DDR B D62	AU2	SB_DQ62
DDR B D63	AT2	SB_DQ63

DDR SYSTEM MEMORY B

CRESTLINE-GP-U-NF



16 DDR_B_BS[0..2] <<>> DDR_B_BS[0..2]

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SB_BS0	SB_BS1	SB_BS2	SB_CAS#	SB_DM0	SB_DM1	SB_DM2	SB_DM3	SB_DM4	SB_DM5	SB_DM6	SB_DM7	SB_DQS0	SB_DQS1	SB_DQS2	SB_DQS3	SB_DQS4	SB_DQS5	SB_DQS6	SB_DQS7	SB_DQS#0	SB_DQS#1	SB_DQS#2	SB_DQS#3	SB_DQS#4	SB_DQS#5	SB_DQS#6	SB_DQS#7	SB_MA0	SB_MA1	SB_MA2	SB_MA3	SB_MA4	SB_MA5	SB_MA6	SB_MA7	SB_MA8	SB_MA9	SB_MA10	SB_MA11	SB_MA12	SB_MA13	SB_MA14	SB_RAS#	SB_RCVEN#	SB_WE#
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AY17	DDR B BS0	DDR_B_BS[0..2]	BE17	DDR B CAS#	AR50	DDR B DM0	BD49	DDR B DM1	BK45	DDR B DM2	BL39	DDR B DM3	BH12	DDR B DM4	BJ7	DDR B DM5	BF3	DDR B DM6	AW2	DDR B DM7	AT50	DDR B DQS0	BD50	DDR B DQS1	BK46	DDR B DQS2	BK39	DDR B DQS3	BJ12	DDR B DQS4	BL7	DDR B DQS5	BE2	DDR B DQS6	AV2	DDR B DQS7	AU50	DDR B DQS#0	BC50	DDR B DQS#1	BL45	DDR B DQS#2	BK38	DDR B DQS#3	BK12	DDR B DQS#4	BK7	DDR B DQS#5	BF2	DDR B DQS#6	AV3	DDR B DQS#7	BC18	DDR B MA0	BG28	DDR B MA1	BG25	DDR B MA2	AW17	DDR B MA3	BF25	DDR B MA4	BE25	DDR B MA5	BA29	DDR B MA6	BC28	DDR B MA7	AY28	DDR B MA8	BD37	DDR B MA9	BG17	DDR B MA10	BE37	DDR B MA11	BA39	DDR B MA12	BC13	DDR B MA13	BE24	DDR B MA14	AV16	DDR B RAS#	AY18	M_B_RCVEN#	TP5	BC17	DDR B WE#
------	-----------	----------------	------	------------	------	-----------	------	-----------	------	-----------	------	-----------	------	-----------	-----	-----------	-----	-----------	-----	-----------	------	------------	------	------------	------	------------	------	------------	------	------------	-----	------------	-----	------------	-----	------------	------	-------------	------	-------------	------	-------------	------	-------------	------	-------------	-----	-------------	-----	-------------	-----	-------------	------	-----------	------	-----------	------	-----------	------	-----------	------	-----------	------	-----------	------	-----------	------	-----------	------	-----------	------	-----------	------	------------	------	------------	------	------------	------	------------	------	------------	------	------------	------	------------	-----	------	-----------

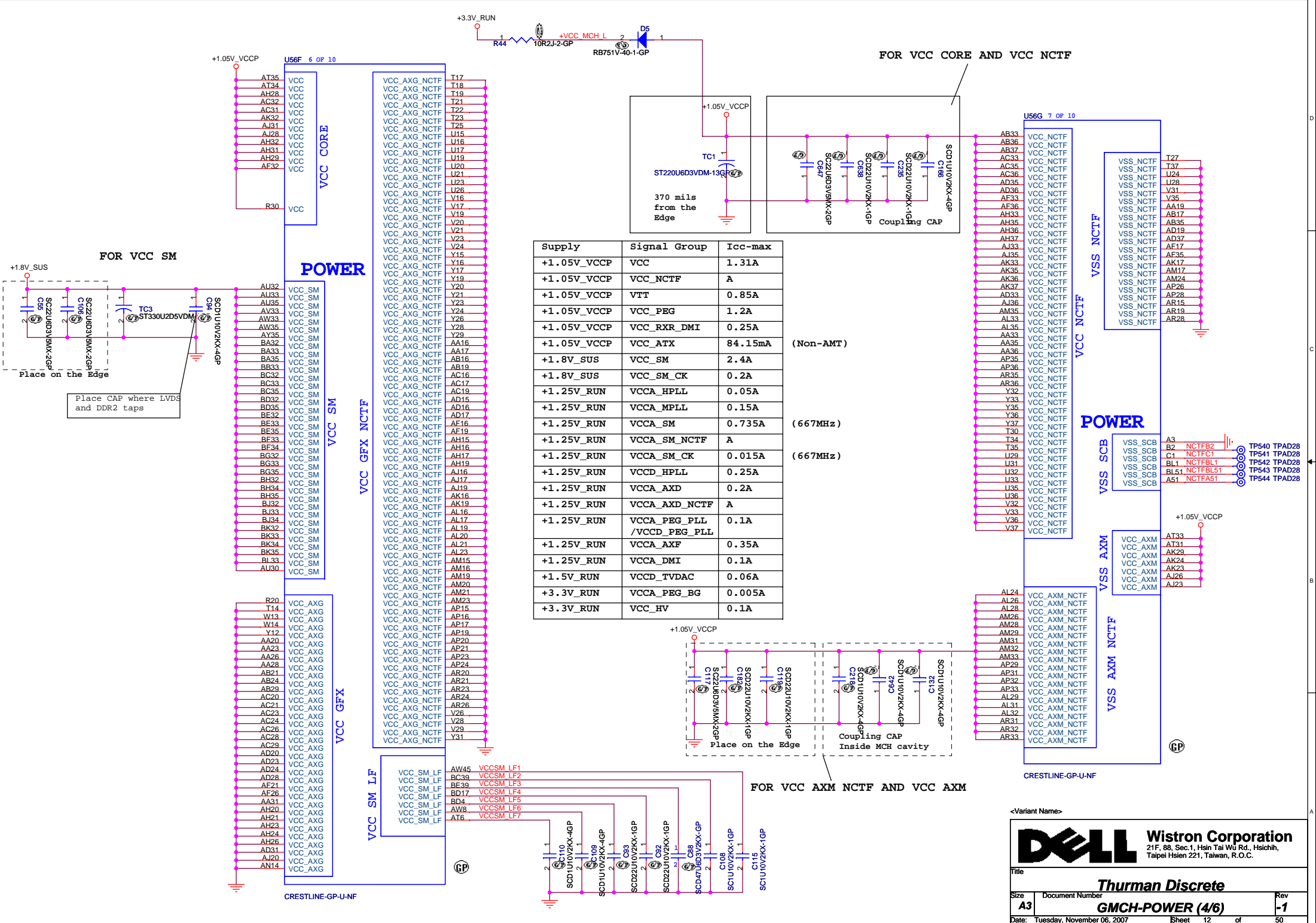
CRESTLINE-GP-U-NF

<-Variant Name>

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Title: **Thurman Discrete**

Size: A3	Document Number: GMCH-DDR (3/6)	Rev: -1
Date: Tuesday, November 06, 2007	Sheet: 11	of: 50



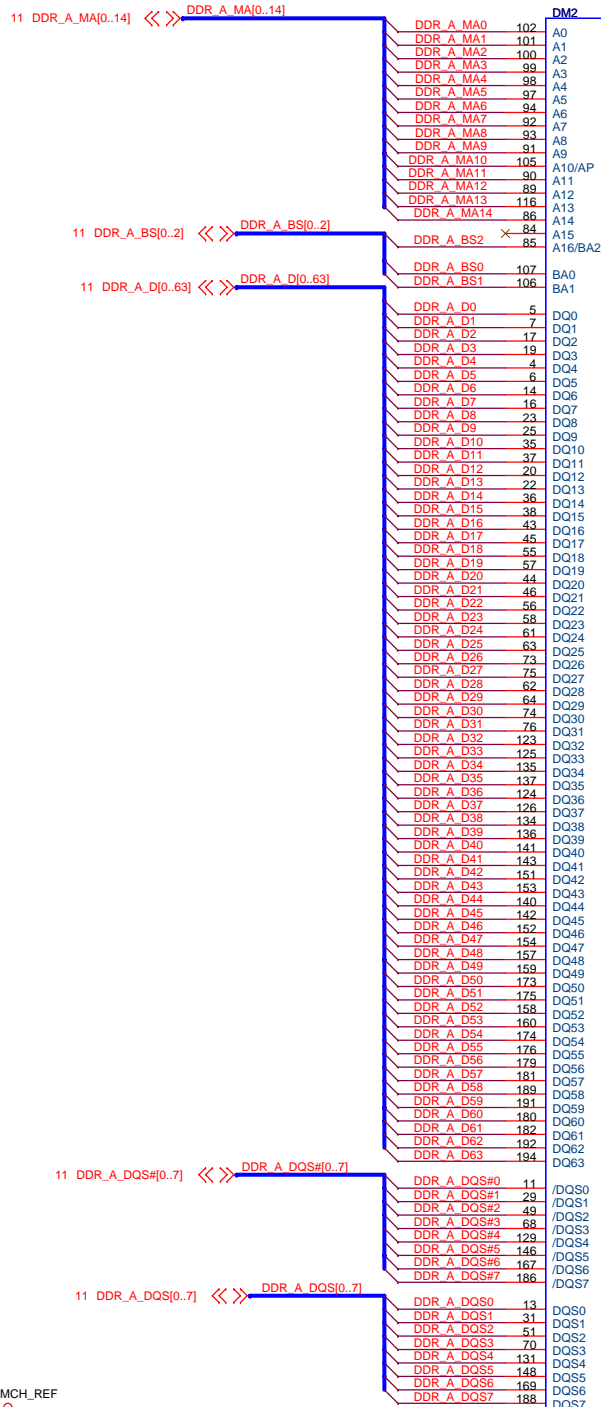
Supply	Signal Group	Icc-max	
+1.05V_VCCP	VCC	1.31A	
+1.05V_VCCP	VCC_NCTF	A	
+1.05V_VCCP	VTT	0.85A	
+1.05V_VCCP	VCC_PEG	1.2A	
+1.05V_VCCP	VCC_RXR_DMI	0.25A	
+1.05V_VCCP	VCC_ATX	84.15mA	(Non-AMT)
+1.8V_SUS	VCC_SM	2.4A	
+1.8V_SUS	VCC_SM_CK	0.2A	
+1.25V_RUN	VCCA_HPLL	0.05A	
+1.25V_RUN	VCCA_MPLL	0.15A	
+1.25V_RUN	VCCA_SM	0.735A	(667MHz)
+1.25V_RUN	VCCA_SM_NCTF	A	
+1.25V_RUN	VCCA_SM_CK	0.015A	(667MHz)
+1.25V_RUN	VCCD_HPLL	0.25A	
+1.25V_RUN	VCCA_AXD	0.2A	
+1.25V_RUN	VCCA_AXD_NCTF	A	
+1.25V_RUN	VCCA_PEG_PLL	0.1A	
+1.25V_RUN	VCCA_PEG_PLL /VCCD_PEG_PLL		
+1.25V_RUN	VCCA_AXF	0.35A	
+1.25V_RUN	VCCA_DMI	0.1A	
+1.5V_RUN	VCCD_TVDAC	0.06A	
+3.3V_RUN	VCCA_PEG_BG	0.005A	
+3.3V_RUN	VCC_HV	0.1A	

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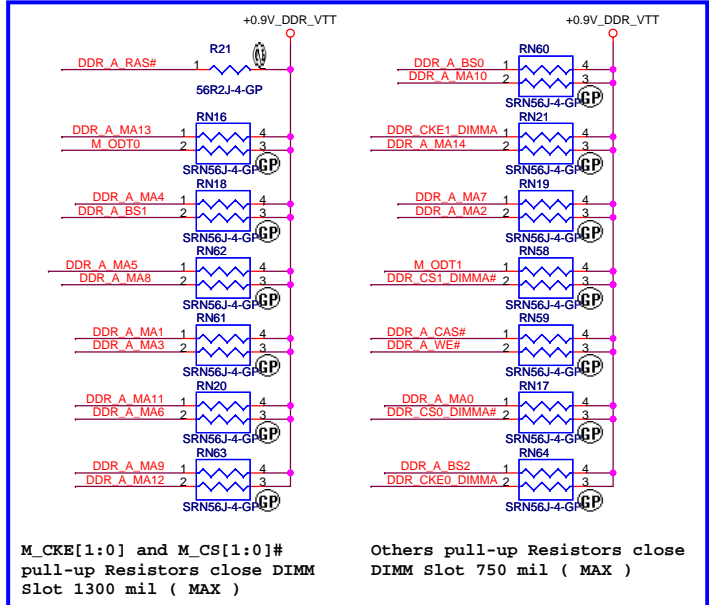
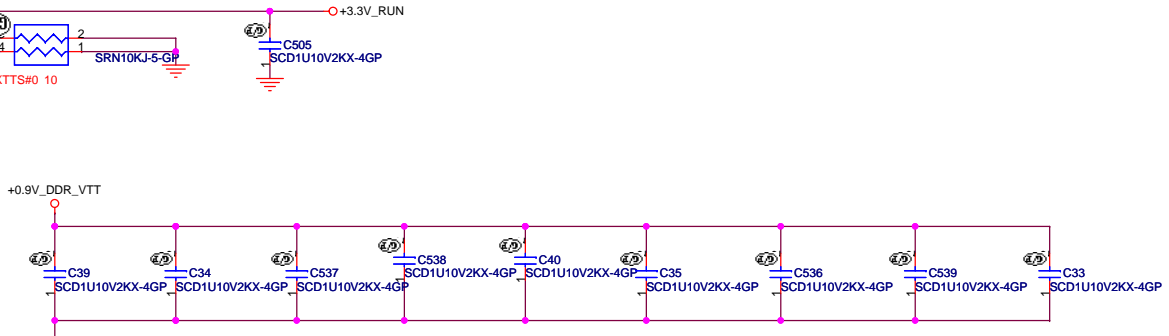
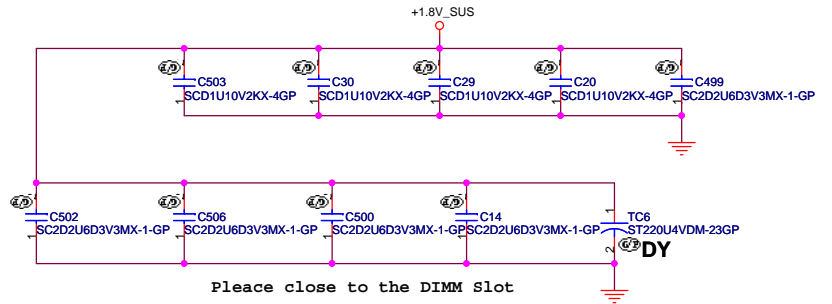
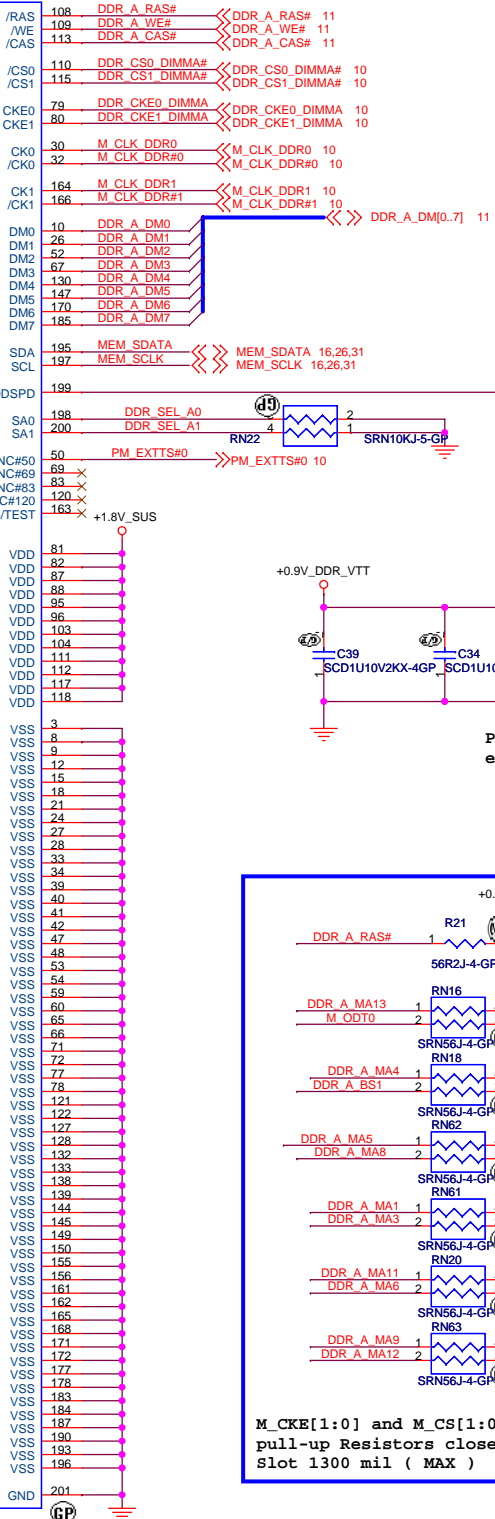
Thurman Discrete
GMCH-POWER (4/6)

Size **A3** Document Number **GMCH-POWER (4/6)** Rev **-1**

Date: Tuesday, November 06, 2007 Sheet 12 of 50



REVERSE TYPE High 5.2 mm



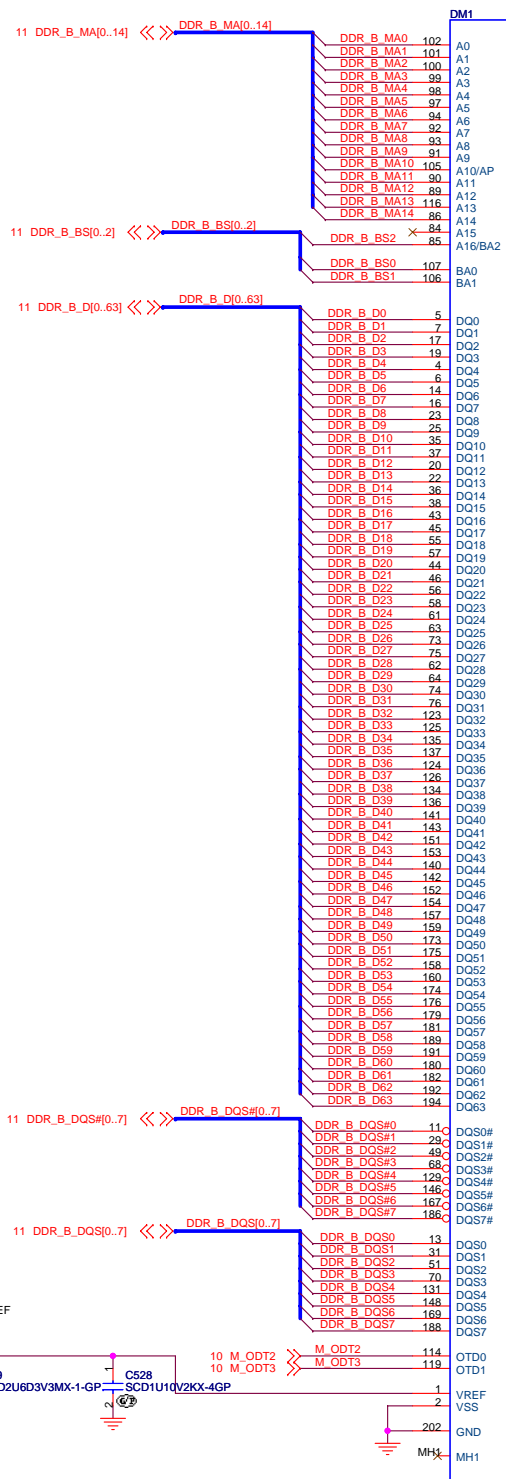
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

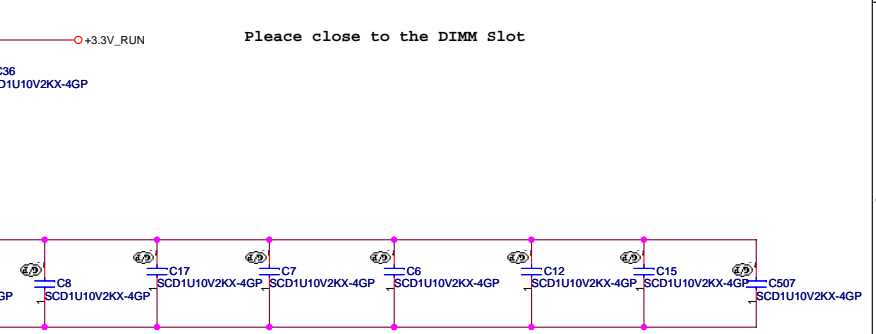
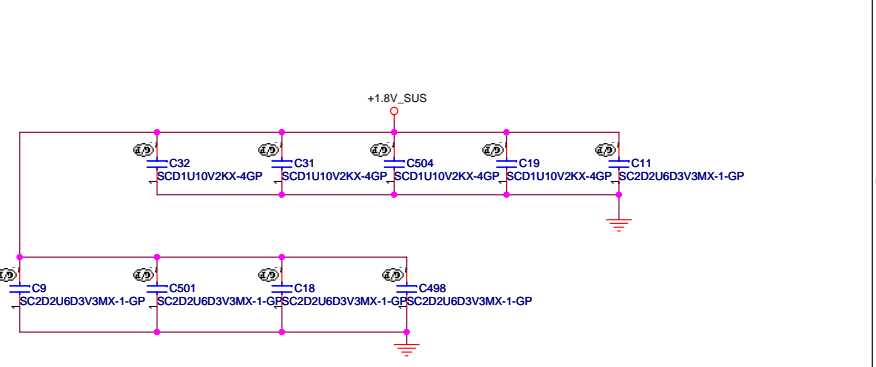
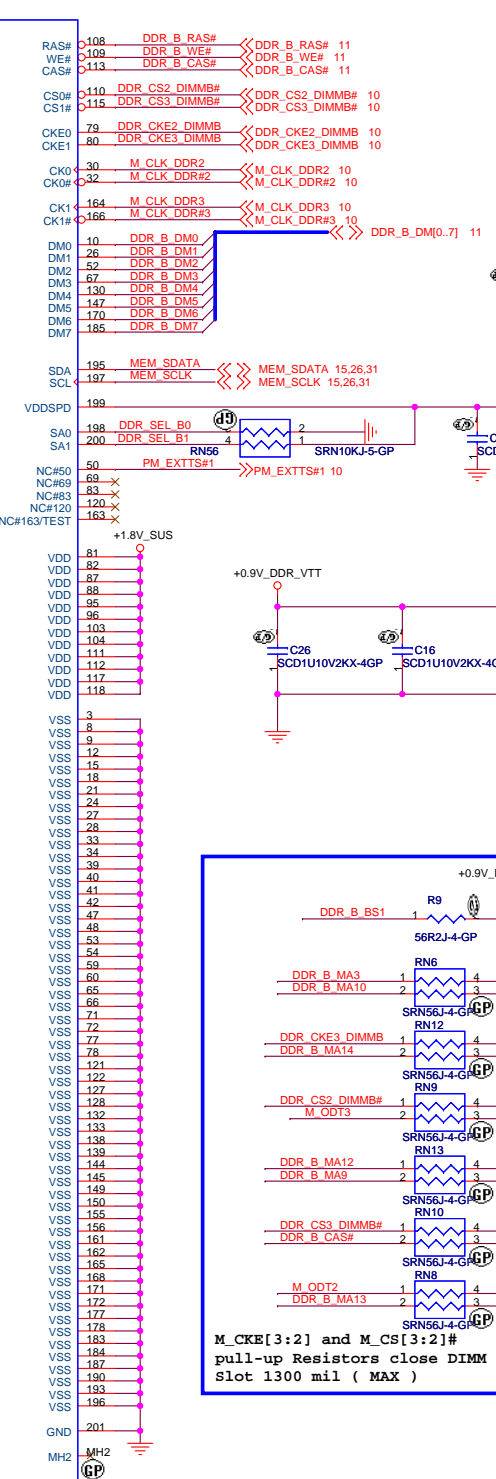
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Size: **A3** Document Number: **DDR2-SODIMM1** Rev: **-1**

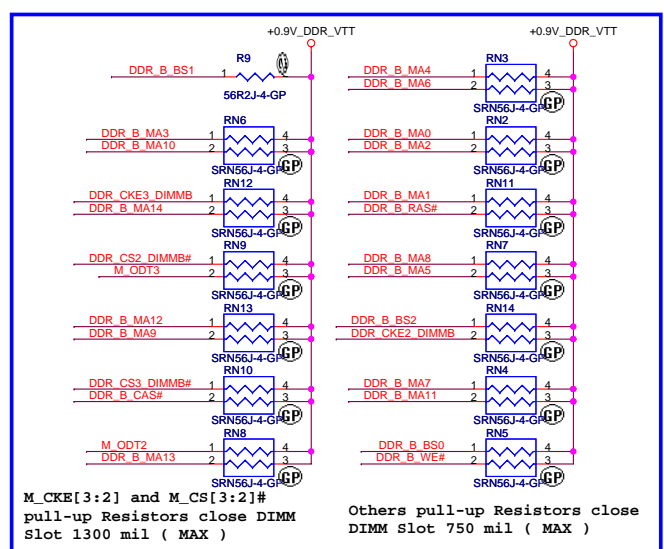
Date: Tuesday, November 06, 2007 Page 15 of 50



REVERSE TYPE High 9.2 mm



Please use One Capacitor close to every Two pull-up Resistors



M_CKE[3:2] and M_CS[3:2]# pull-up Resistors close DIMM Slot 1300 mil (MAX)
Others pull-up Resistors close DIMM slot 750 mil (MAX)

-Variant Name-

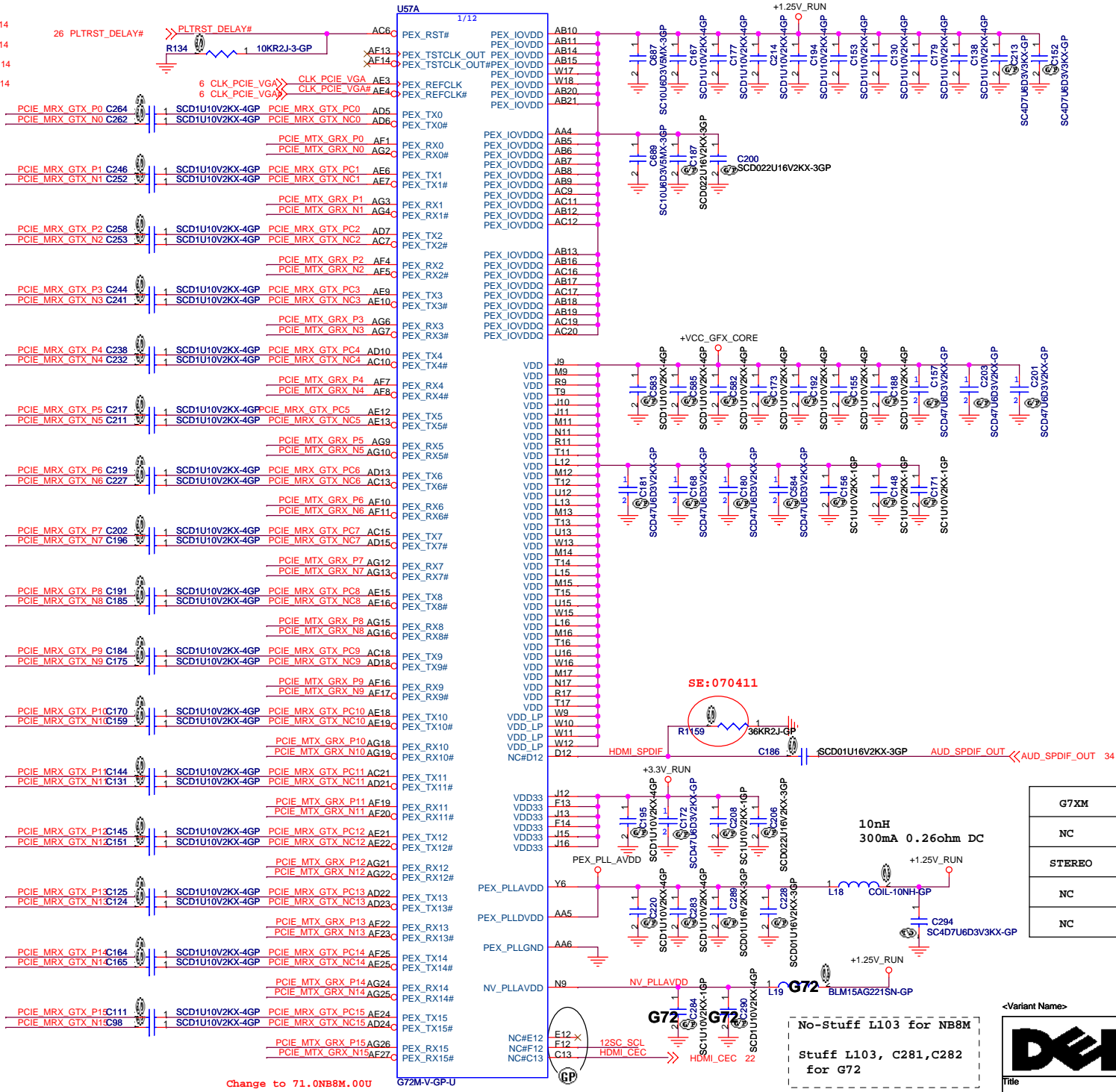
DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Thurman Discrete**

Size: Custom Document Number: **DDR2-SODIMM2** Rev: **-1**

Date: Tuesday, November 06, 2007 Sheet 16 of 50

PCIE_MRX_GTX_N0_15] >> PCIE_MRX_GTX_N0_15] 14
 PCIE_MRX_GTX_P0_15] >> PCIE_MRX_GTX_P0_15] 14
 PCIE_MTX_GRX_N0_15] << PCIE_MTX_GRX_N0_15] 14
 PCIE_MTX_GRX_P0_15] << PCIE_MTX_GRX_P0_15] 14



PCIE_MRX_GTX_P0 C264	1	SCD1U10V2KX-4GP	PCIE_MRX_GTX_P0	AD5	PEX_TX0
PCIE_MRX_GTX_N0 C262	1	SCD1U10V2KX-4GP	PCIE_MRX_GTX_N0	AD6	PEX_TX0#
PCIE_MRX_GTX_P1 C246	1	SCD1U10V2KX-4GP	PCIE_MRX_GTX_P1	AE6	PEX_TX1
PCIE_MRX_GTX_N1 C252	1	SCD1U10V2KX-4GP	PCIE_MRX_GTX_N1	AE7	PEX_TX1#
PCIE_MRX_GTX_P2 C258	1	SCD1U10V2KX-4GP	PCIE_MRX_GTX_P2	AD7	PEX_TX2
PCIE_MRX_GTX_N2 C253	1	SCD1U10V2KX-4GP	PCIE_MRX_GTX_N2	AG7	PEX_TX2#
PCIE_MRX_GTX_P3 C244	1	SCD1U10V2KX-4GP	PCIE_MRX_GTX_P3	AE9	PEX_TX3
PCIE_MRX_GTX_N3 C241	1	SCD1U10V2KX-4GP	PCIE_MRX_GTX_N3	AE10	PEX_TX3#
PCIE_MRX_GTX_P4 C238	1	SCD1U10V2KX-4GP	PCIE_MRX_GTX_P4	AD10	PEX_TX4
PCIE_MRX_GTX_N4 C232	1	SCD1U10V2KX-4GP	PCIE_MRX_GTX_N4	AC10	PEX_TX4#
PCIE_MRX_GTX_P5 C217	1	SCD1U10V2KX-4GP	PCIE_MRX_GTX_P5	AE12	PEX_TX5
PCIE_MRX_GTX_N5 C211	1	SCD1U10V2KX-4GP	PCIE_MRX_GTX_N5	AE13	PEX_TX5#
PCIE_MRX_GTX_P6 C219	1	SCD1U10V2KX-4GP	PCIE_MRX_GTX_P6	AD13	PEX_TX6
PCIE_MRX_GTX_N6 C227	1	SCD1U10V2KX-4GP	PCIE_MRX_GTX_N6	AC13	PEX_TX6#
PCIE_MRX_GTX_P7 C202	1	SCD1U10V2KX-4GP	PCIE_MRX_GTX_P7	AC15	PEX_TX7
PCIE_MRX_GTX_N7 C196	1	SCD1U10V2KX-4GP	PCIE_MRX_GTX_N7	AD15	PEX_TX7#
PCIE_MRX_GTX_P8 C191	1	SCD1U10V2KX-4GP	PCIE_MRX_GTX_P8	AE15	PEX_TX8
PCIE_MRX_GTX_N8 C185	1	SCD1U10V2KX-4GP	PCIE_MRX_GTX_N8	AE16	PEX_TX8#
PCIE_MRX_GTX_P9 C184	1	SCD1U10V2KX-4GP	PCIE_MRX_GTX_P9	AC18	PEX_TX9
PCIE_MRX_GTX_N9 C175	1	SCD1U10V2KX-4GP	PCIE_MRX_GTX_N9	AD18	PEX_TX9#
PCIE_MRX_GTX_P10 C170	1	SCD1U10V2KX-4GP	PCIE_MRX_GTX_P10	AC18	PEX_RX9
PCIE_MRX_GTX_N10 C159	1	SCD1U10V2KX-4GP	PCIE_MRX_GTX_N10	AD19	PEX_RX9#
PCIE_MRX_GTX_P11 C144	1	SCD1U10V2KX-4GP	PCIE_MRX_GTX_P11	AC21	PEX_TX11
PCIE_MRX_GTX_N11 C131	1	SCD1U10V2KX-4GP	PCIE_MRX_GTX_N11	AD21	PEX_TX11#
PCIE_MRX_GTX_P12 C145	1	SCD1U10V2KX-4GP	PCIE_MRX_GTX_P12	AE21	PEX_TX12
PCIE_MRX_GTX_N12 C151	1	SCD1U10V2KX-4GP	PCIE_MRX_GTX_N12	AE22	PEX_TX12#
PCIE_MRX_GTX_P13 C125	1	SCD1U10V2KX-4GP	PCIE_MRX_GTX_P13	AD22	PEX_TX13
PCIE_MRX_GTX_N13 C124	1	SCD1U10V2KX-4GP	PCIE_MRX_GTX_N13	AD23	PEX_TX13#
PCIE_MRX_GTX_P14 C164	1	SCD1U10V2KX-4GP	PCIE_MRX_GTX_P14	AE25	PEX_TX14
PCIE_MRX_GTX_N14 C165	1	SCD1U10V2KX-4GP	PCIE_MRX_GTX_N14	AE25	PEX_TX14#
PCIE_MRX_GTX_P15 C111	1	SCD1U10V2KX-4GP	PCIE_MRX_GTX_P15	AE24	PEX_TX15
PCIE_MRX_GTX_N15 C98	1	SCD1U10V2KX-4GP	PCIE_MRX_GTX_N15	AD24	PEX_TX15#
			PCIE_MTX_GRX_P15	AG26	PEX_RX15
			PCIE_MTX_GRX_N15	AF27	PEX_RX15#

Change to 71.0NB8M.00U

	G7XM	G8XM	G3-64 BALL
NC	I2SC_SCL		F12
STEREO	DACB_CS		F7 (Pag 17)
NC	GPI013		C13
NC	GPI014		E12

Variant Name:

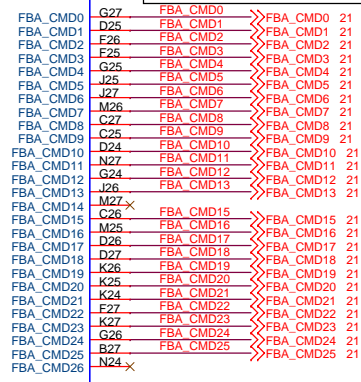
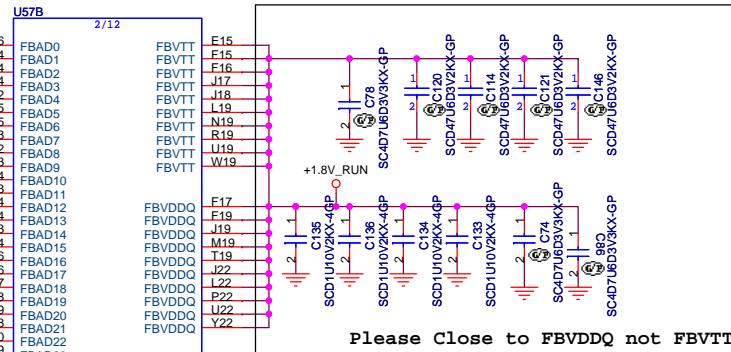
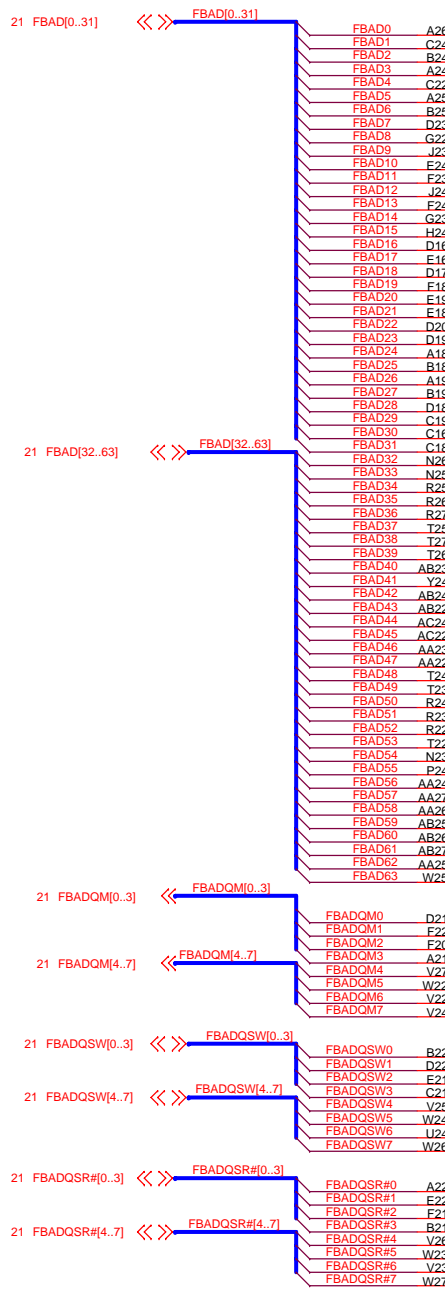
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File: **Thurman Discrete**

Size: A3 Document Number: **VGA-PCIE (1/4)** Rev: **-1**

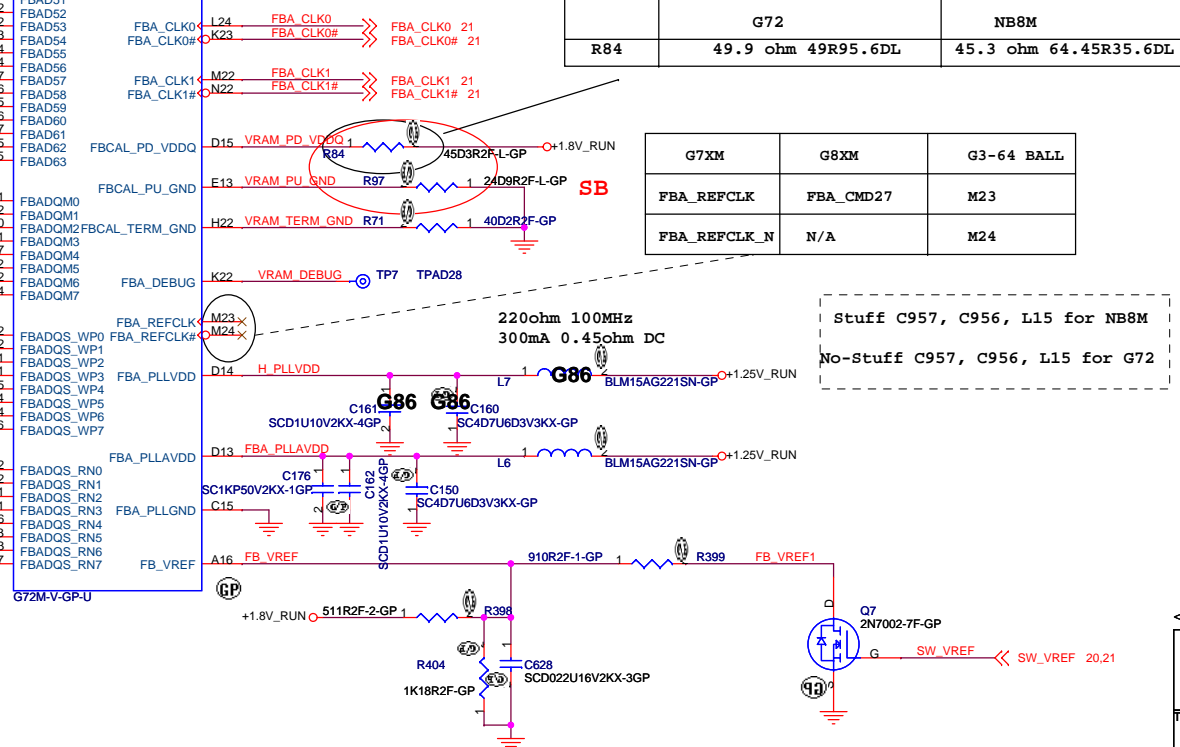
Date: Tuesday, November 06, 2007 Sheet 17 of 50

No-Stuff L103 for NB8M
 Stuff L103, C281, C282 for G72



FBCAL_PD_VDDQ OPTION		
	G72	NB8M
R84	49.9 ohm 49R95.6DL	45.3 ohm 64.45R35.6DL

	G7XM	G8XM	G3-64 BALL
FBA_REFCLK		FBA_CMD27	M23
FBA_REFCLK_N	N/A		M24

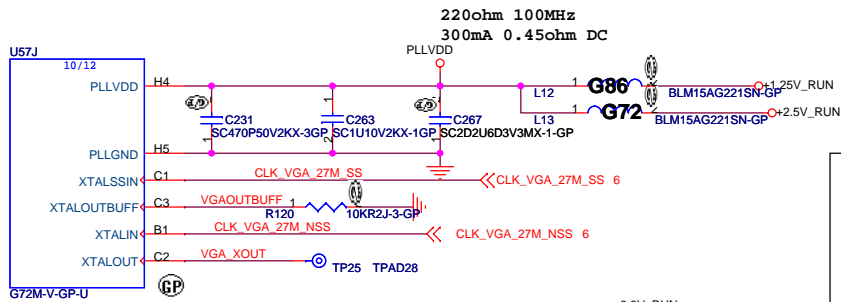


<Variant Name>

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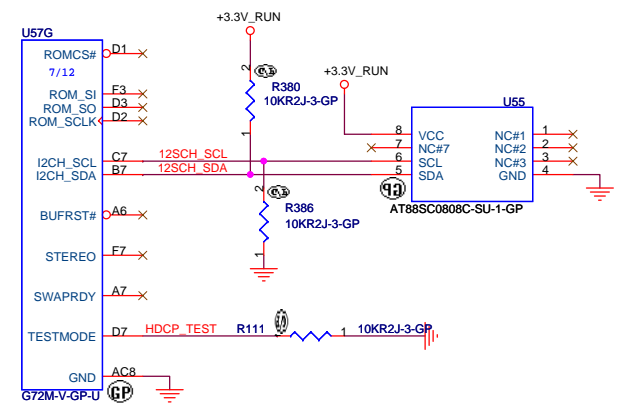
Title: **Thurman Discrete**

Size A3	Document Number	Rev
	VGA-VRAM(2/4)	-1
Date: Tuesday, November 06, 2007	Sheet 18 of	50

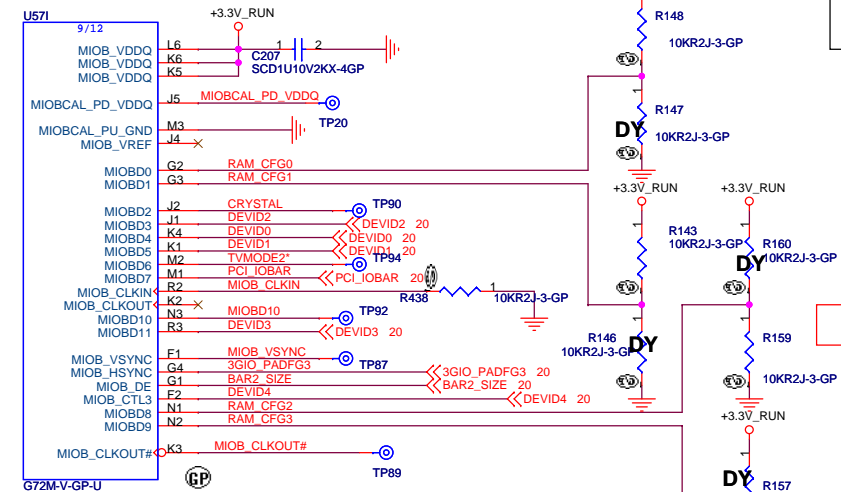


Stuff L100 for G72
Stuff L11 for NB8M

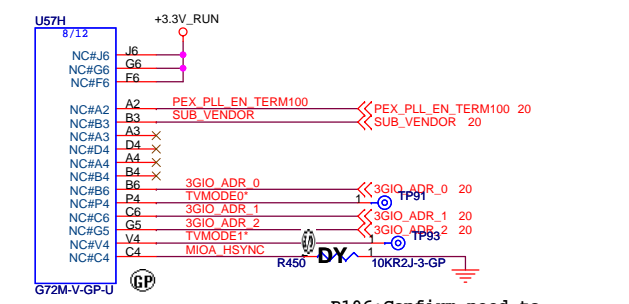
MIOBD0	Infineon 8MX32 DDR3 1.8V	0101
MIOBD1	HyNix 8MX32 DDR3 1.8V	0111
MIOBD8	Samsung 8MX32 DDR3 1.8V	0110
MIOBD9	Infineon 16MX32 DDR3 1.8V	0001
	HyNix 16MX32 DDR3 1.8V	0010
	Samsung 16MX32 DDR3 1.8V	0011



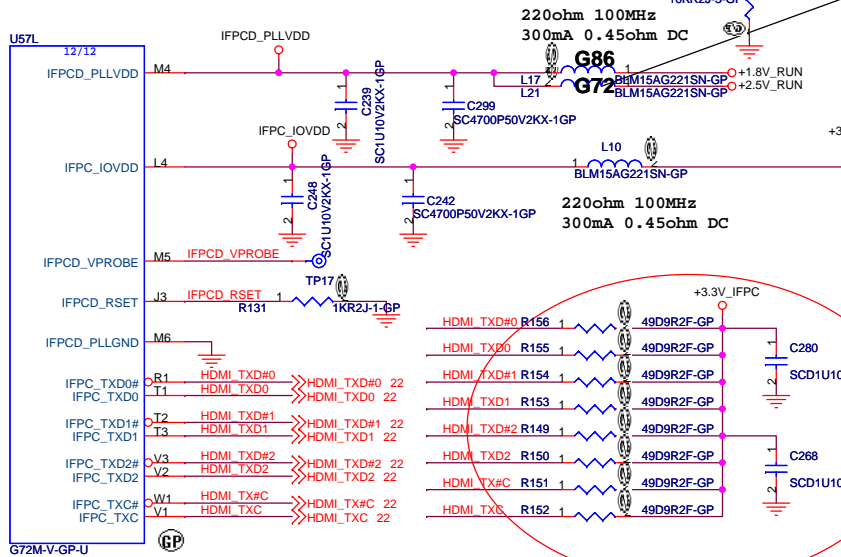
	DEVID3	DEVID2	DEVID1	DEVID0
G72GLM	1	1	0	0
G72M	1	0	0	0
G72MV	0	1	1	1
G86M	0	1	1	1



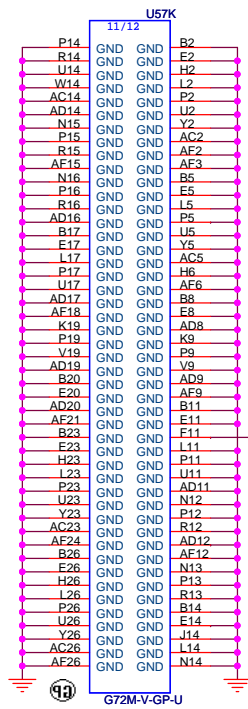
Stuff L101 for G72
Stuff L53 for NB8M



R106: Confirm need to
no stuff not for G72
and G86.

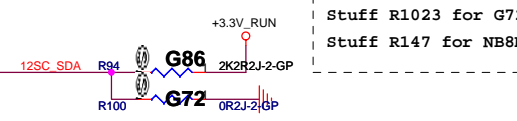


Stuff L101 for G72
Stuff L53 for NB8M



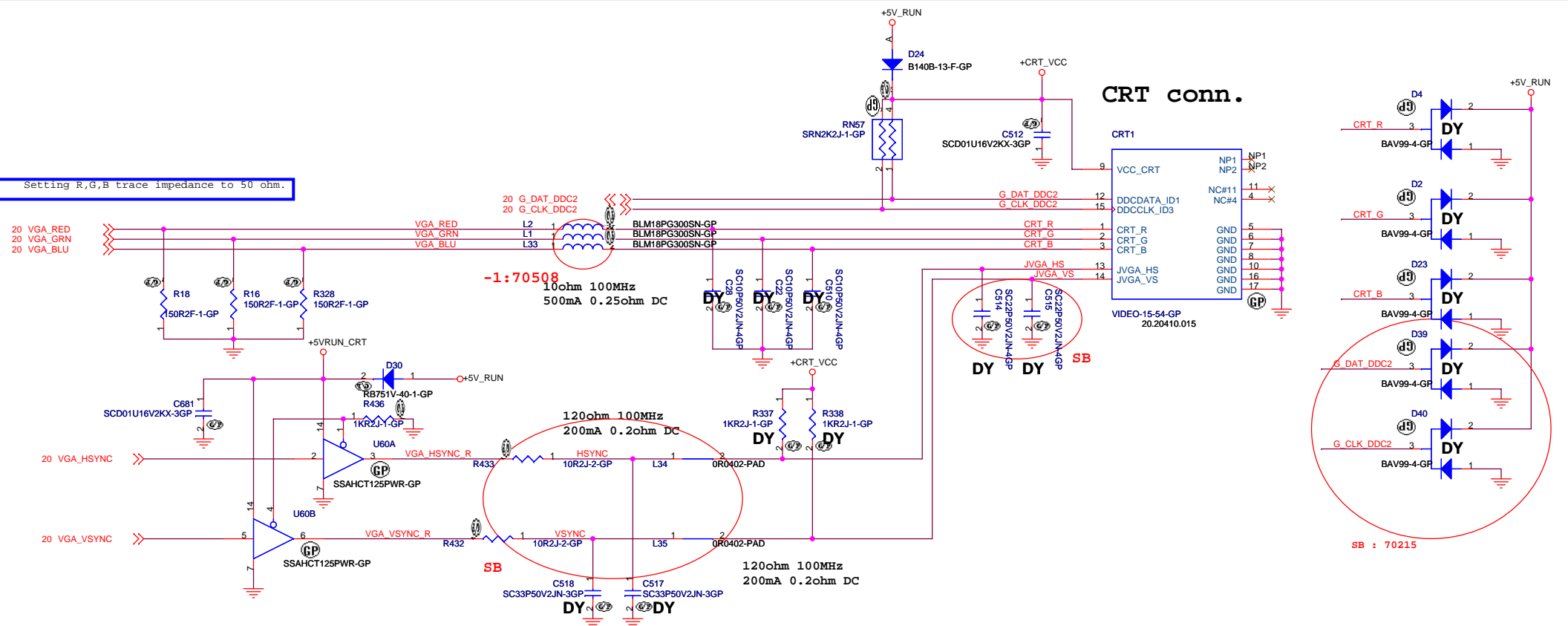
G7XM	G8XM	G3-64 ball
	12SC_SDA	F11

Stuff R1023 for G72
Stuff R147 for NB8M

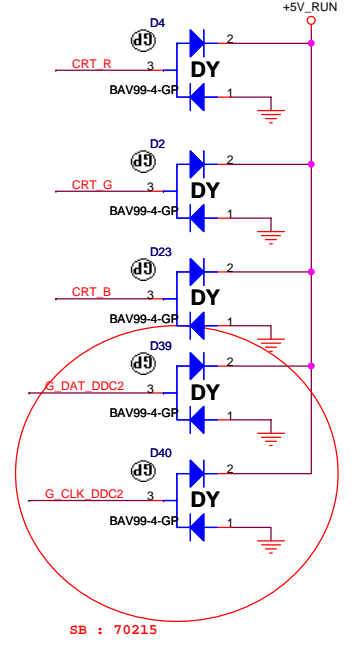


SB: 70 316

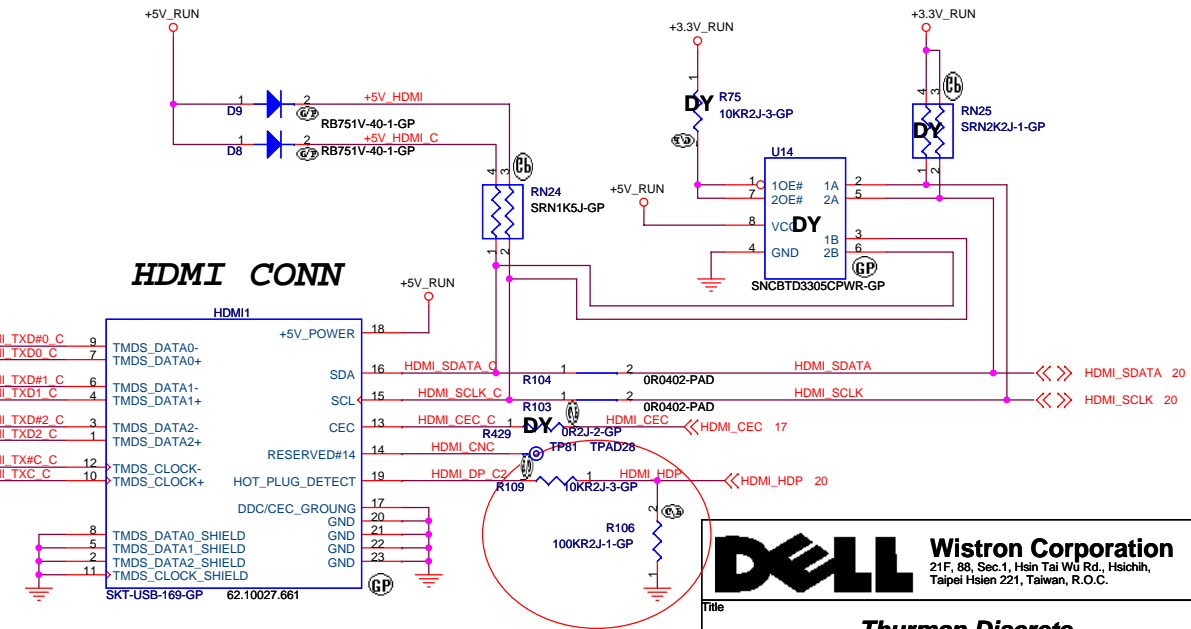
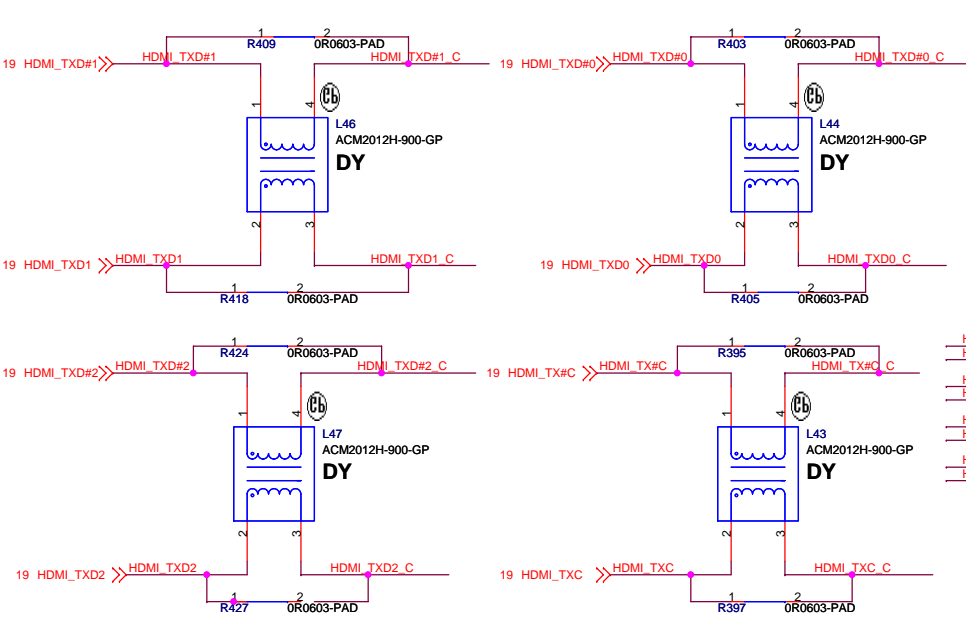
Setting R,G,B trace impedance to 50 ohm.



CRT conn.



SB : 70215

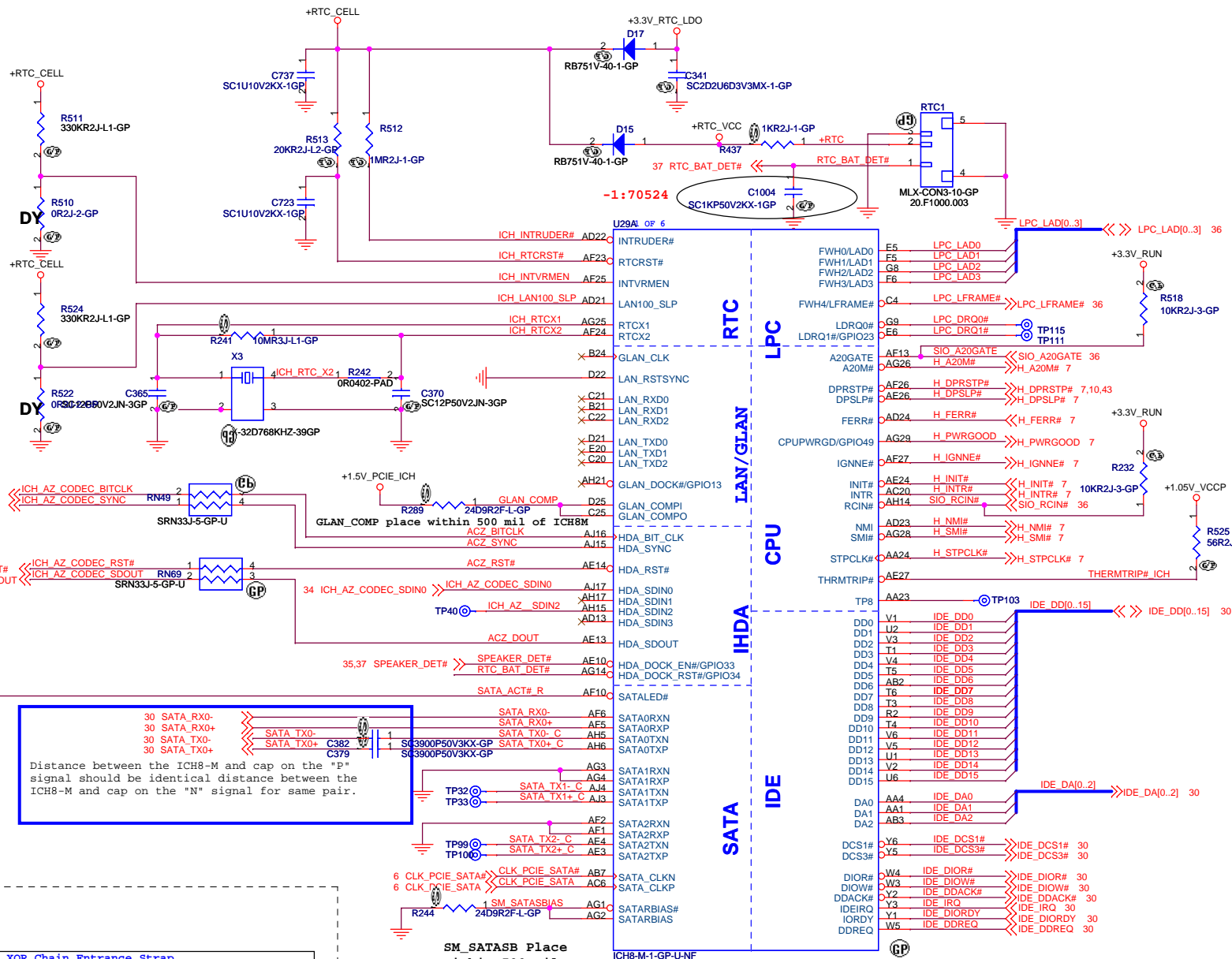


HDMI CONN

SE: 70412

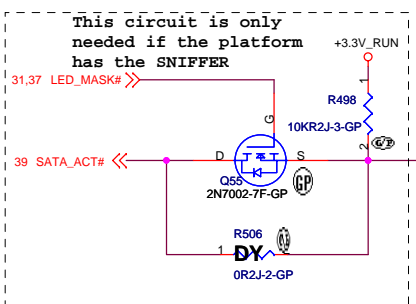


RTC circuitry

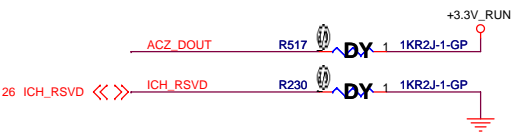


ICH8-Strap PIN

integrated VccSus1_05,VccSus1_5,VccCl1_5		
ICH_INTVRMEN	High=Enable	Low=Disable
integrated VccLan1_05VccCl1_05		
ICH_LAN100_SLP	High=Enable	Low=Disable



ICH8-Strap PIN



XOR Chain Entrance Strap

ICH_RSVD	ACZ_DOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation(default)
1	1	Set PCIE port cofig bit1

SM_SATASB Place within 500 mil of ICH8-M

Change to 71.0IC8M.M08

<Variant Name>



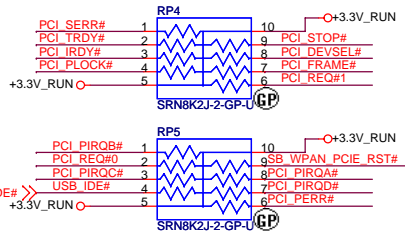
ICH8-Strap PIN

BOOT BIOS Strap		
PCI_GNT#0 (R166)	SPI_CS#1 (R167)	BOOT BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC

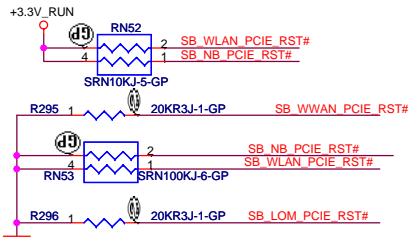
Al6 swap override strap	
PCI_GNT#3 (R168)	low = Al6 swap override enable high = default



PCI I/F PULL HIGH

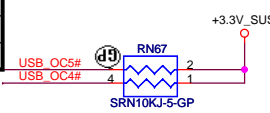


BIOS should not enable the internal GPIO pull up

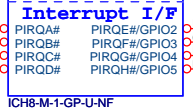
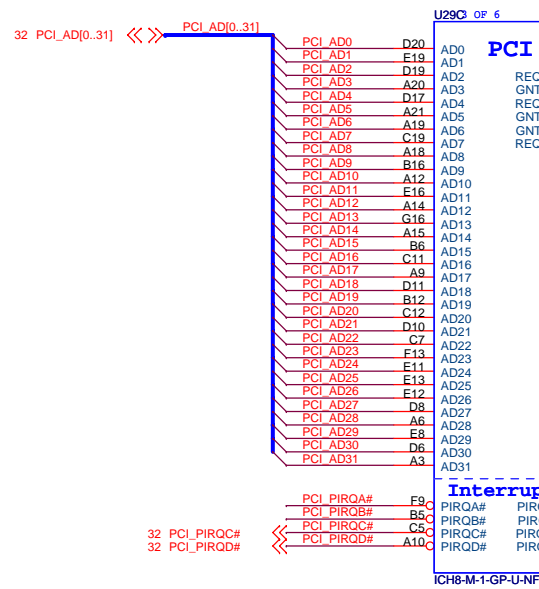


PCIE Interface Routing

LANE1	MiniCard WWAN
LANE2	MiniCard WLAN
LANE3	No use
LANE4	Express Card
LANE5	No use
LANE6	LAN

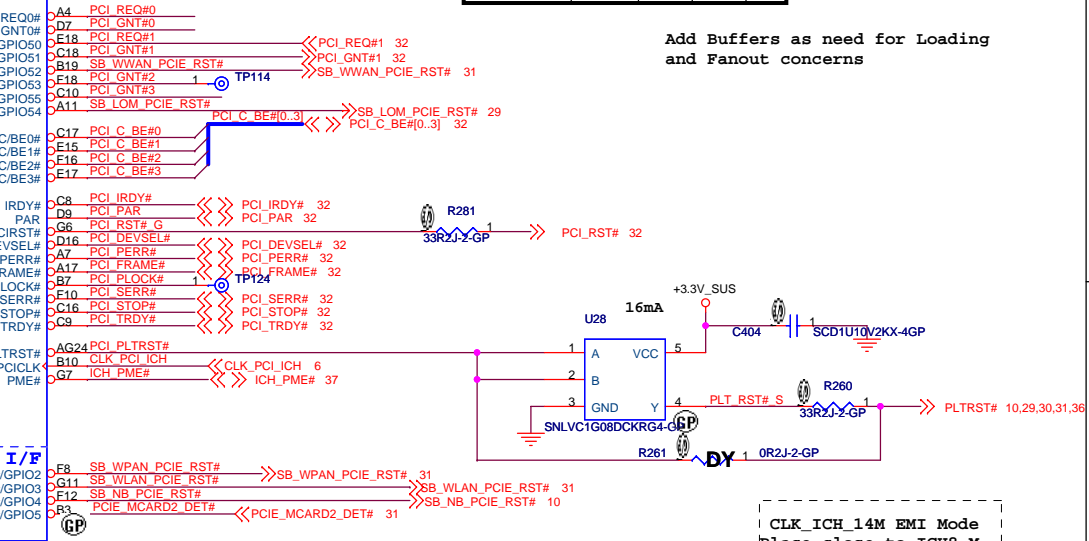


Layout Note:
Place R235, R237 and R234 within 500 mils from ICH.

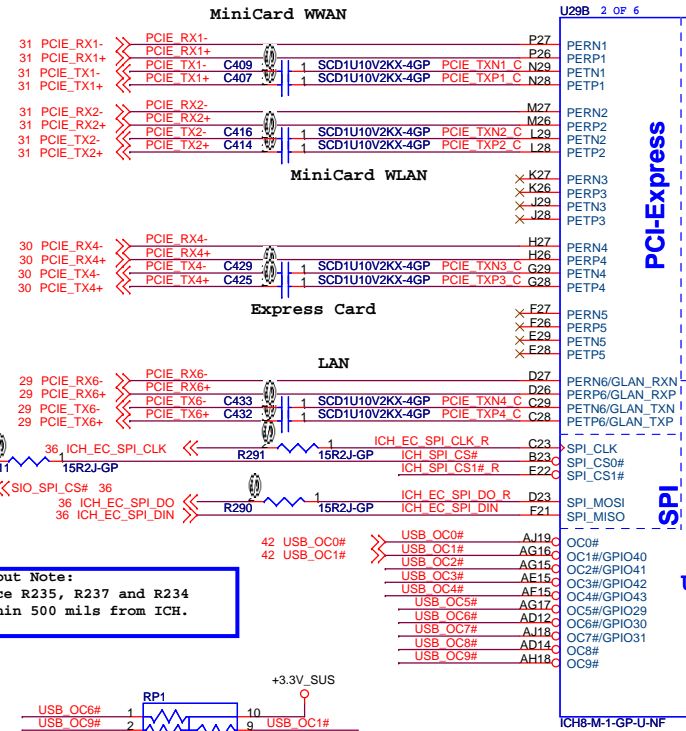
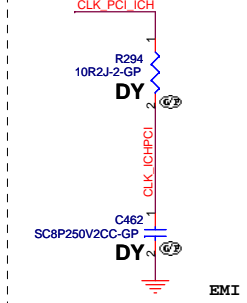


PCI Interface Routing				
IDSEL	INT	REQ	GNT	
AD17	C	1	1	

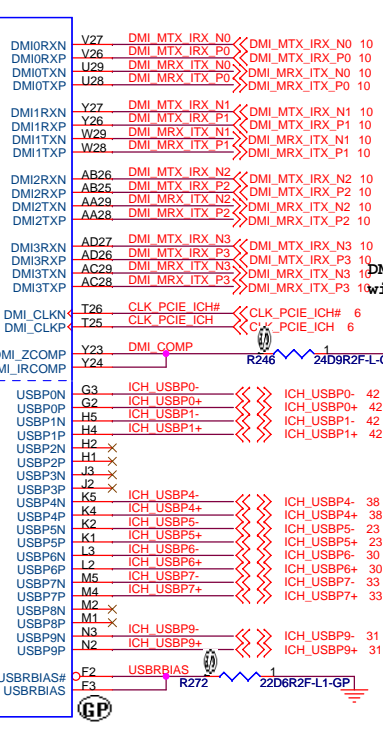
Add Buffers as need for Loading and Fanout concerns



CLK_ICH_14M EMI Mode
Place close to ICH8-M



PCI-Express Direct Media Interface

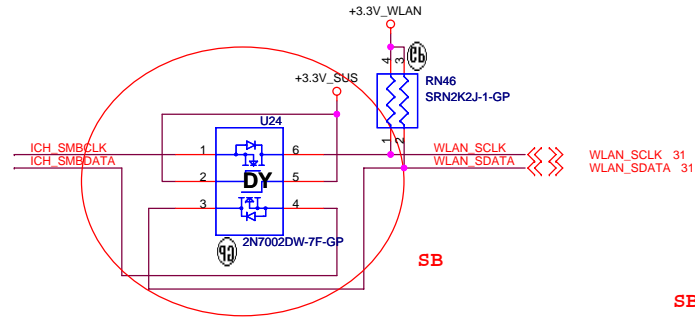
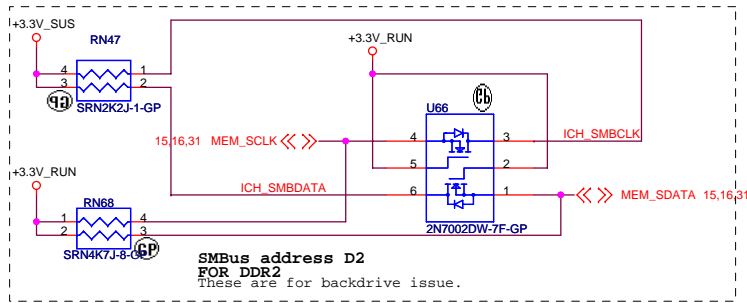


USB0	USB1
USB1	USB2
USB2	
USB3	
USB4	Biometric
USB5	Camera
USB6	Express Card
USB7	BT
USB8	
USB9	MINI Card WWAN

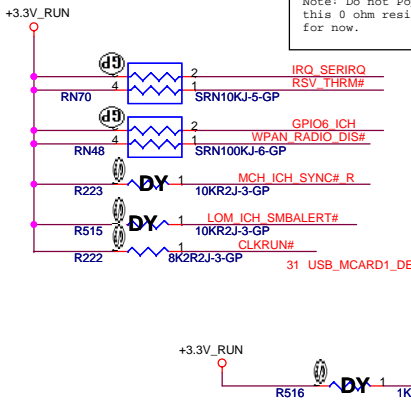
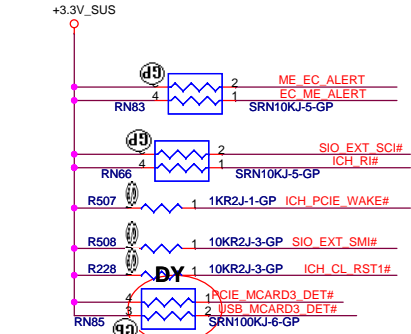
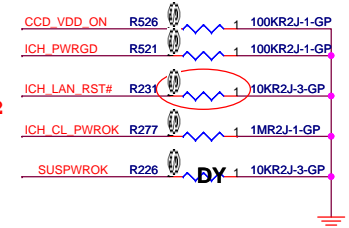
<Variant Name>



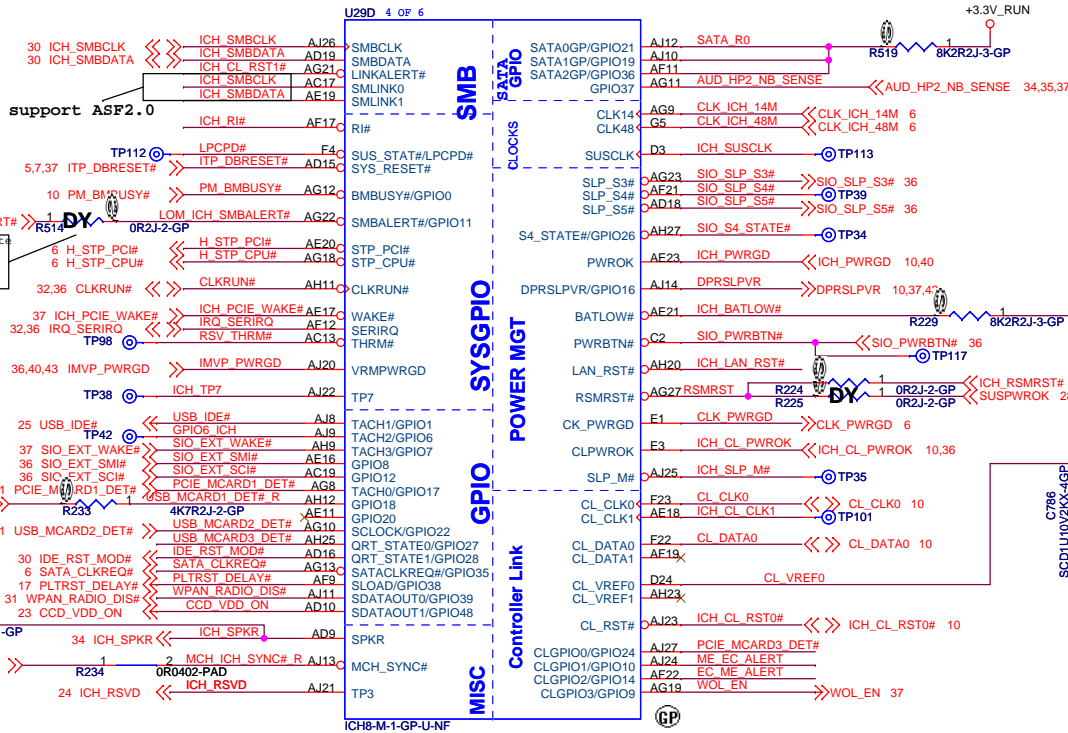
USBRBIAS close to ICH8M 500 mils and Trace impedance should be 60 ohm +/- 15%



SB: 70302

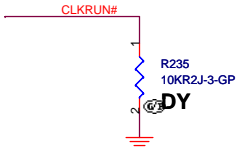


Note: Do not Populate this 0 ohm resistor for now.

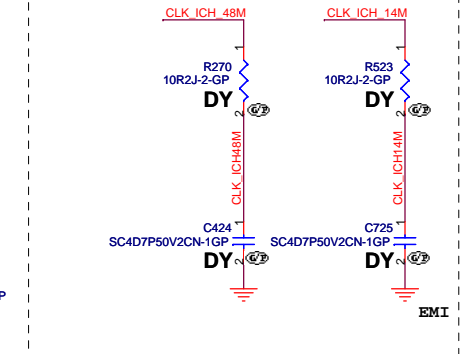


ICH8-Strap PIN

No Reboot Strap	
ICH_SPKR	LOW = Default
	High=No Reboot



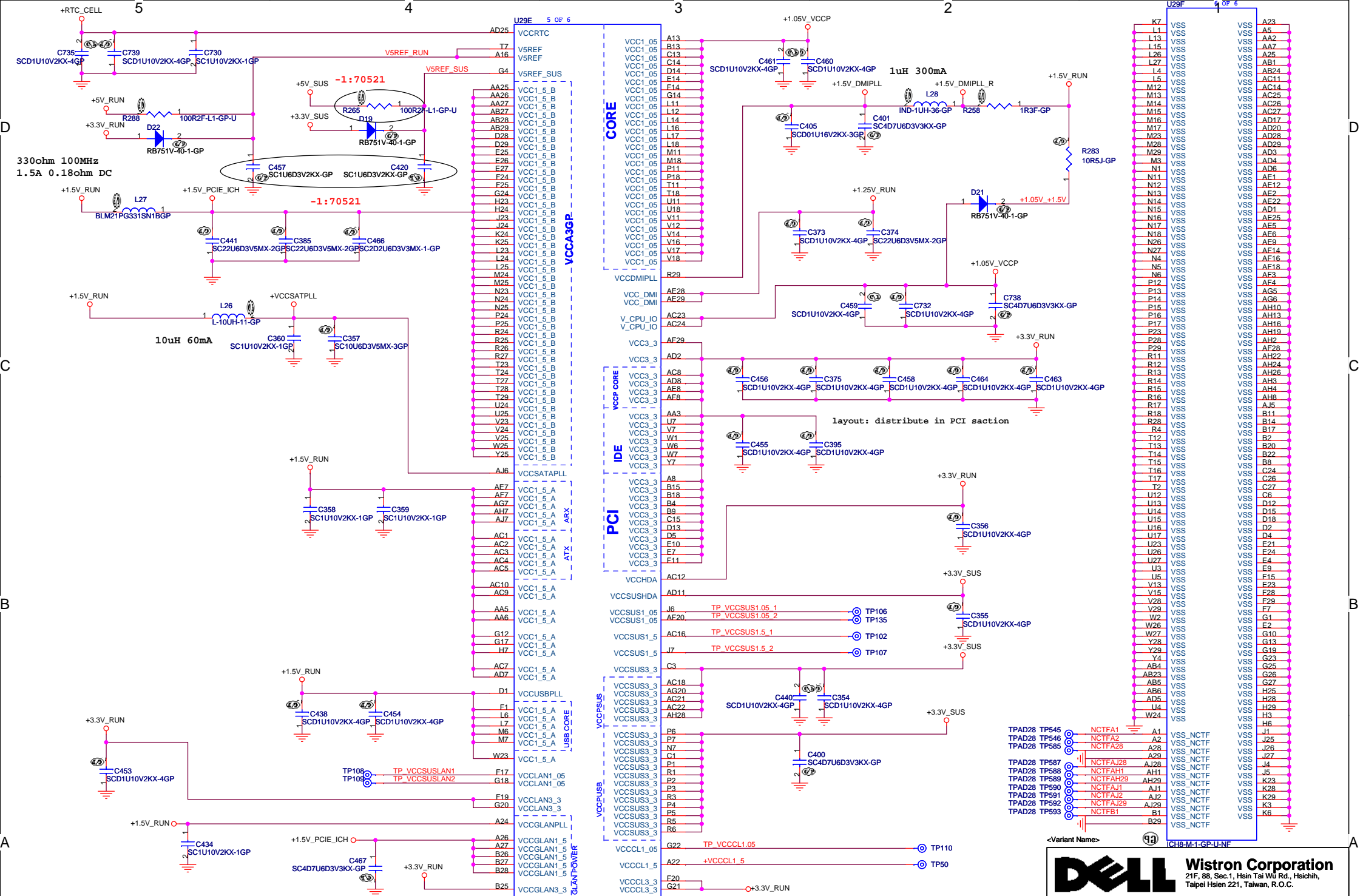
CLK_ICH_48M and CLK_ICH_14M EMI Mode
Place close to ICH8-M




<Variant Name>



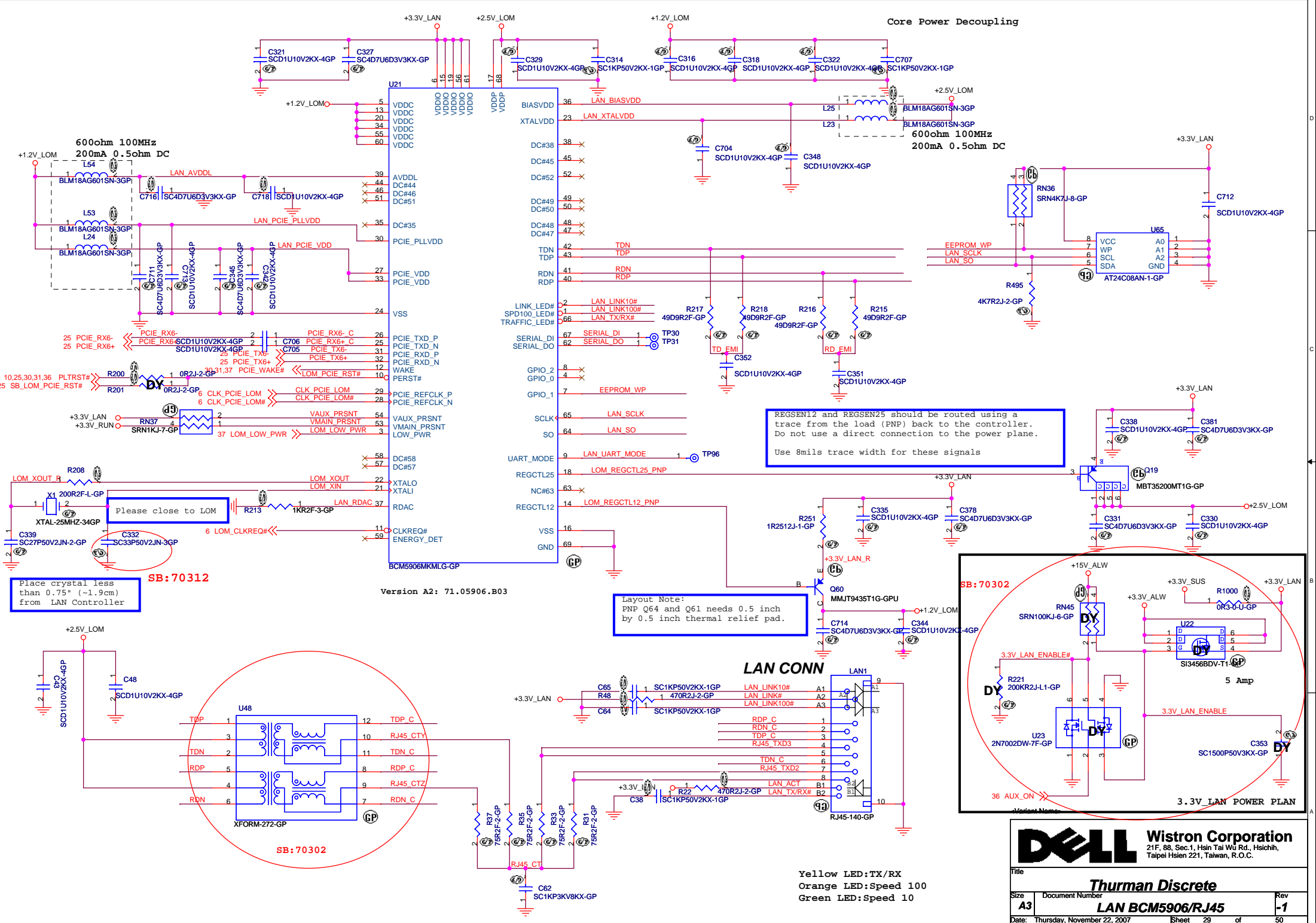
Title			Thurman Discrete		
Size	Document Number		Rev		
A3	ICH8M-CL/PM/GPIO (3/4)		-1		
Date:	Tuesday, November 06, 2007	Sheet	26	of	50




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 Taipei Hsien 221, Taiwan, R.O.C.

Thurman Discrete
ICH8M-POWER (4/4)

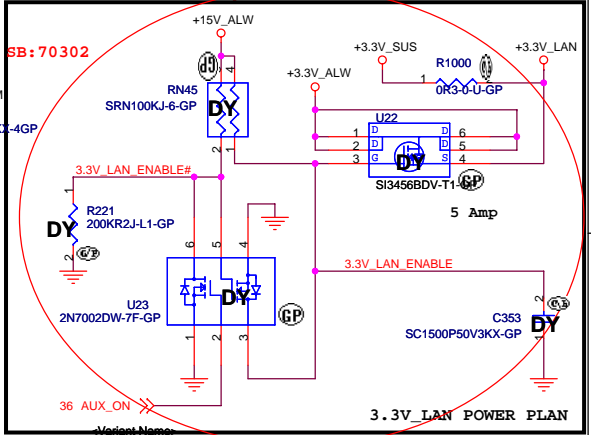
Title: _____
 Size: **A3** Document Number: _____
 Date: **Tuesday, November 06, 2007** Sheet **27** of **50**



REGSEN12 and REGSEN25 should be routed using a trace from the load (PNP) back to the controller. Do not use a direct connection to the power plane.
Use 8mils trace width for these signals

Layout Note:
PNP Q64 and Q61 needs 0.5 inch by 0.5 inch thermal relief pad.

Place crystal less than 0.75" (~1.9cm) from LAN Controller



LAN CONN

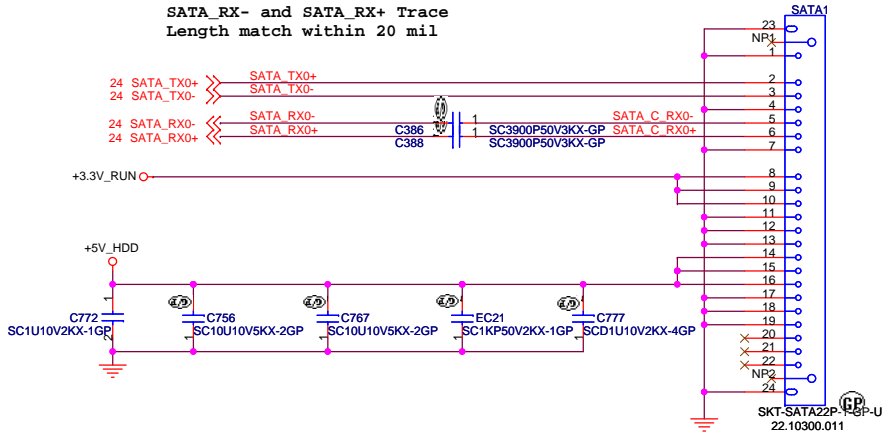
Yellow LED:TX/RX
Orange LED:Speed 100
Green LED:Speed 10



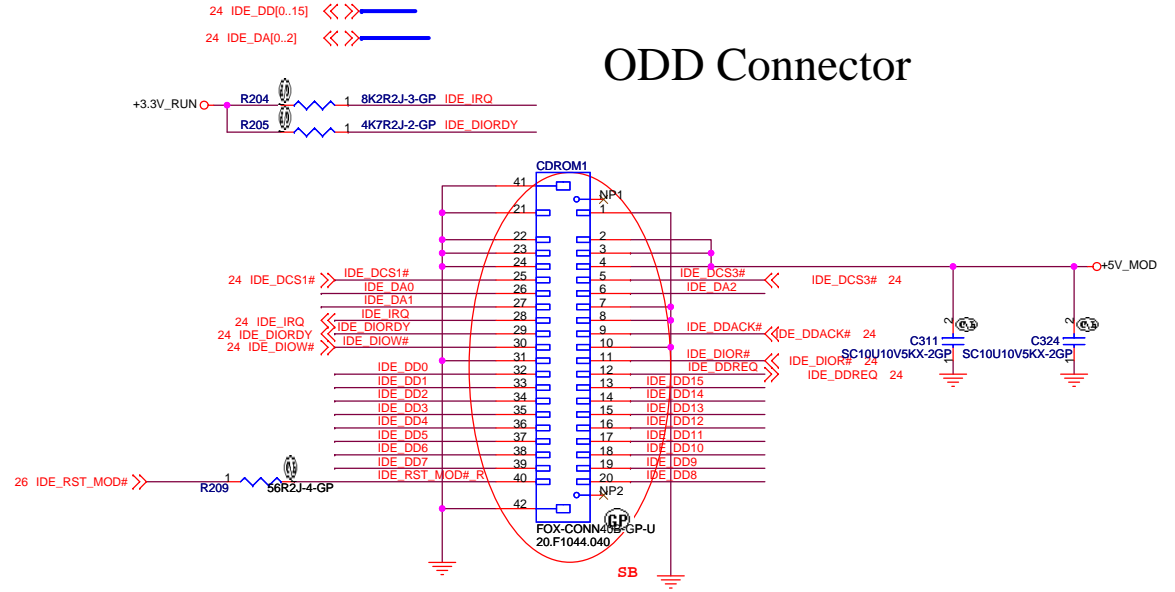
SSID = IDE & SATA

SATA HDD Connector

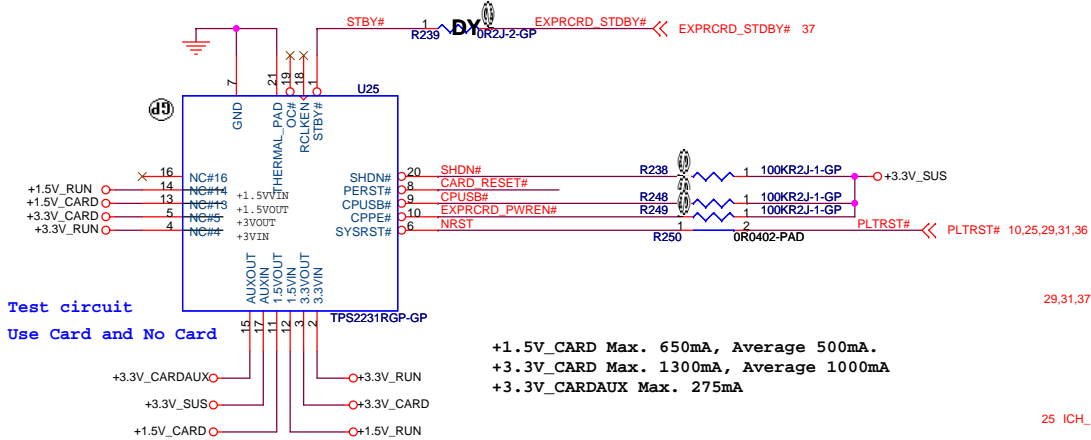
SATA_RX- and SATA_RX+ Trace
Length match within 20 mil



ODD Connector

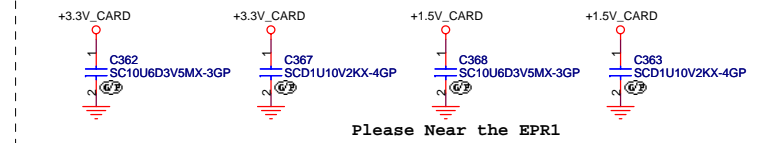
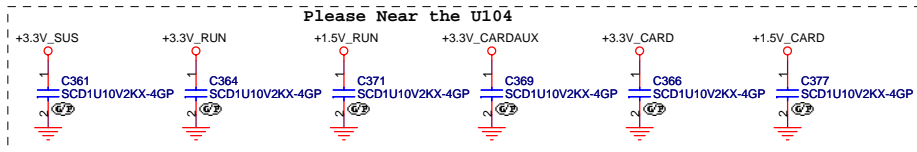


Express Card

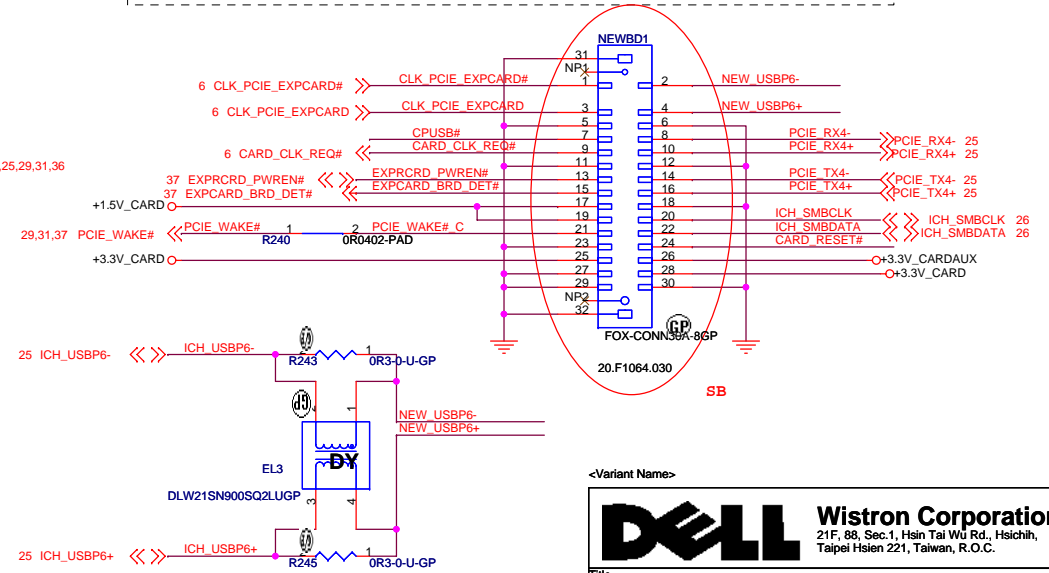


Test circuit
Use Card and No Card

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA



Please Near the EPR1

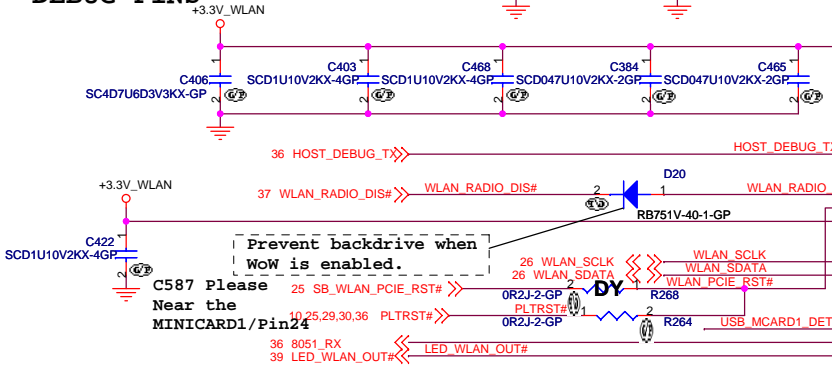


<Variant Name>

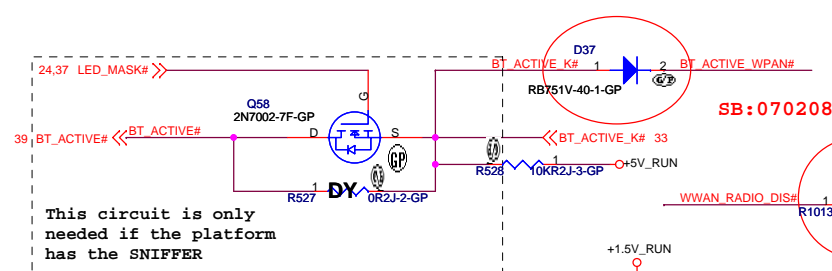
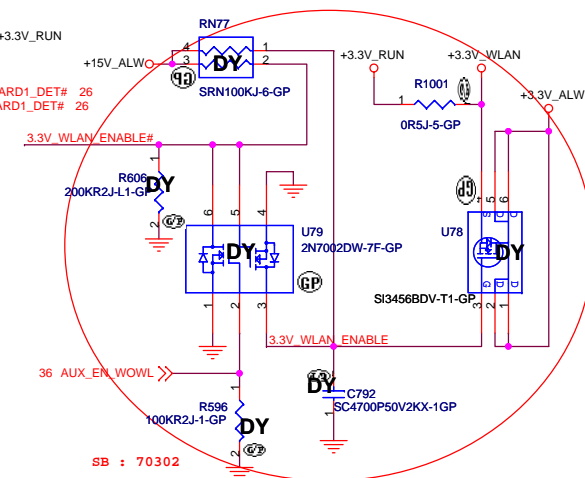
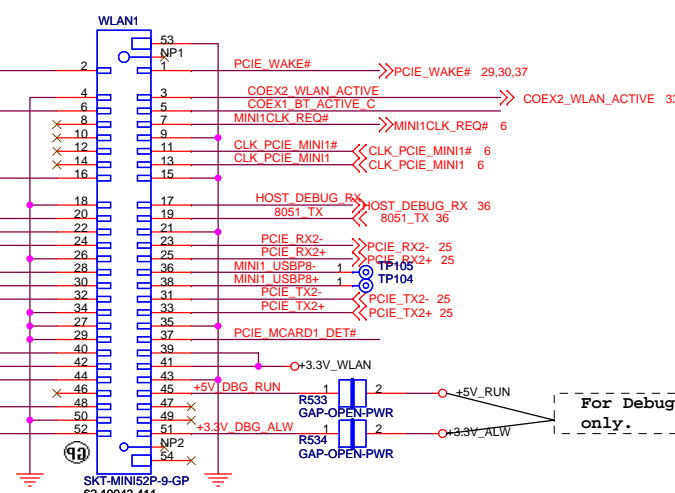
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Taipei Hsien 221, Taiwan, R.O.C.

JMINI Pin	Debug Pin Name	EC Pin
16	HOST_DEBUG_TX	70
17	HOST_DEBUG_RX	71
19	8051_TX	82
42	8051_RX	81

DEBUG PINS



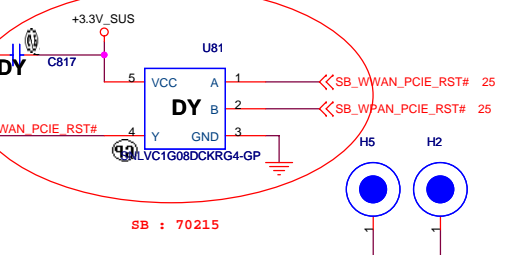
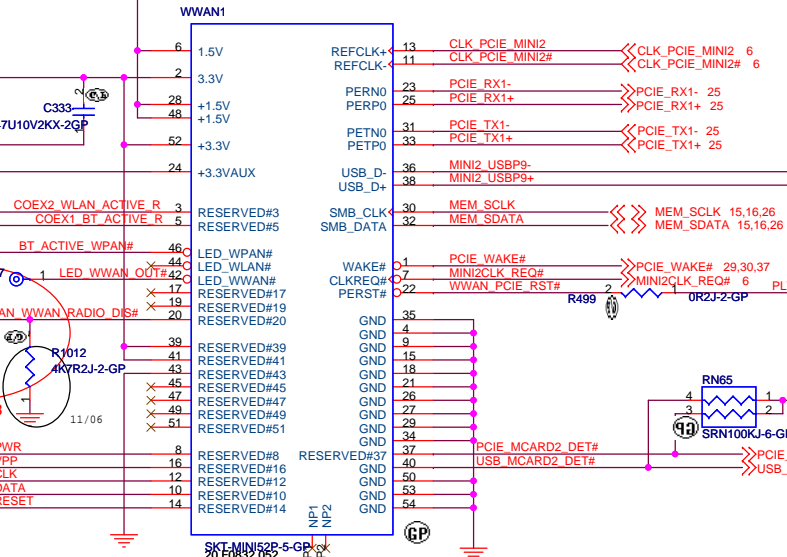
MiniCard WLAN connector



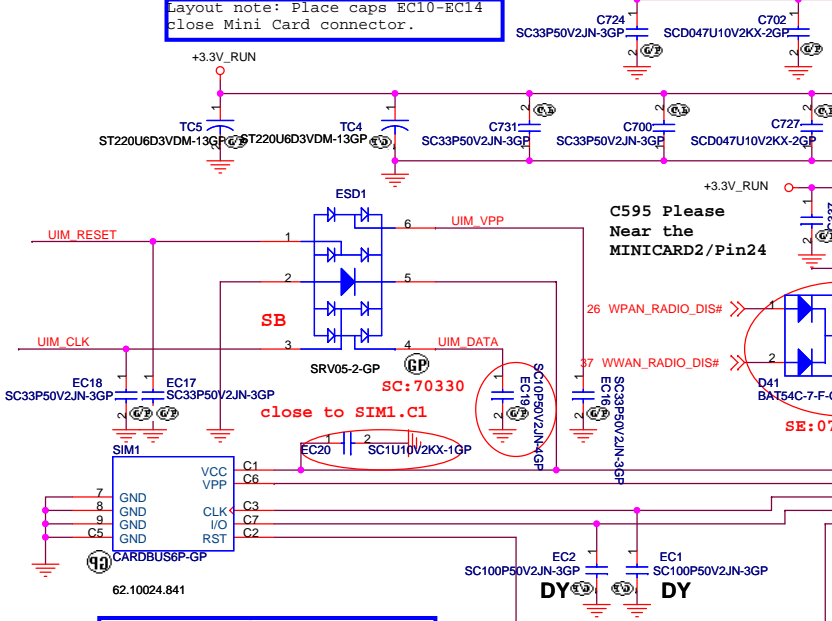
SB:070208

SE:070412

MiniCard WWAN connector



SB : 70215



SC:70330

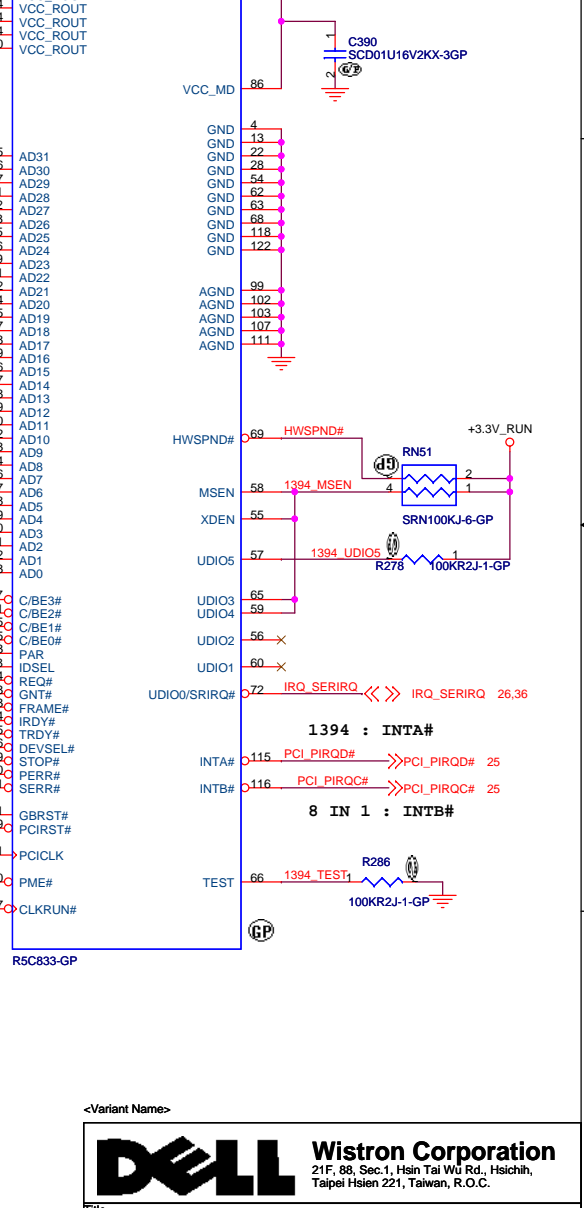
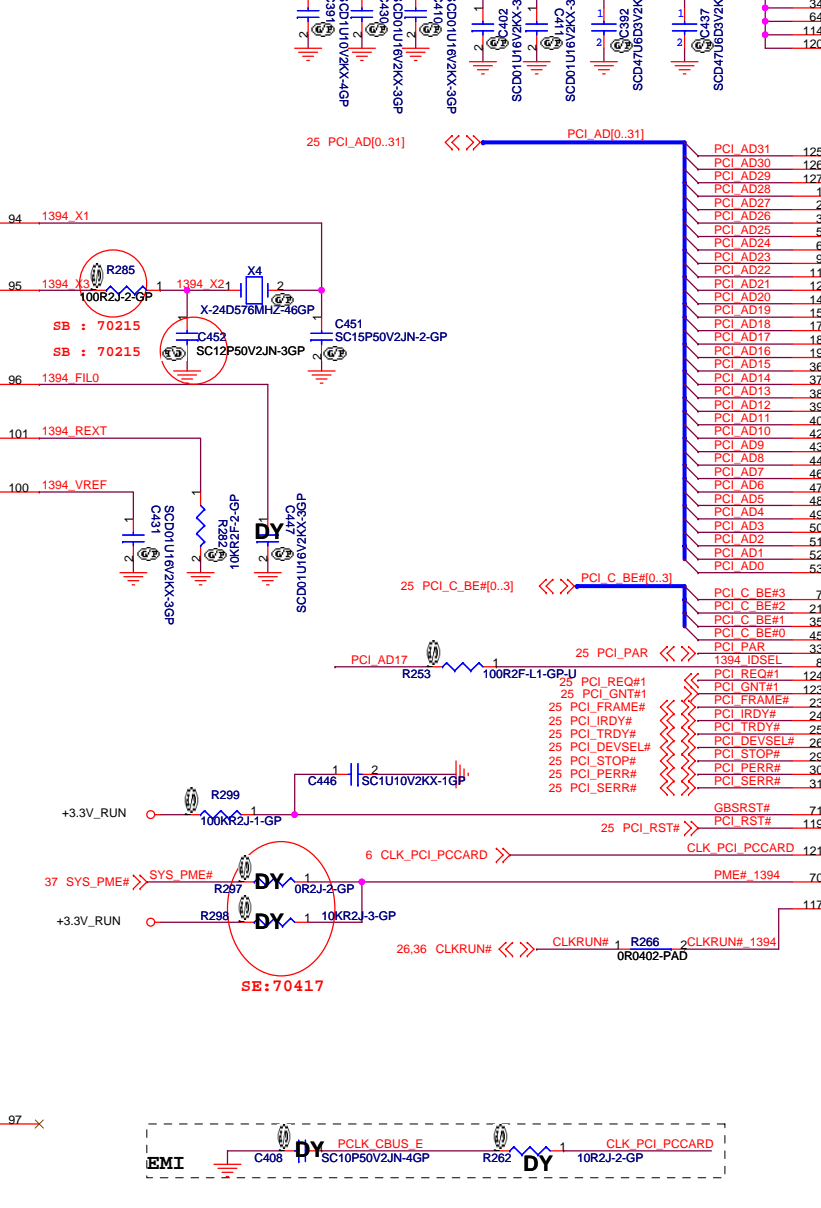
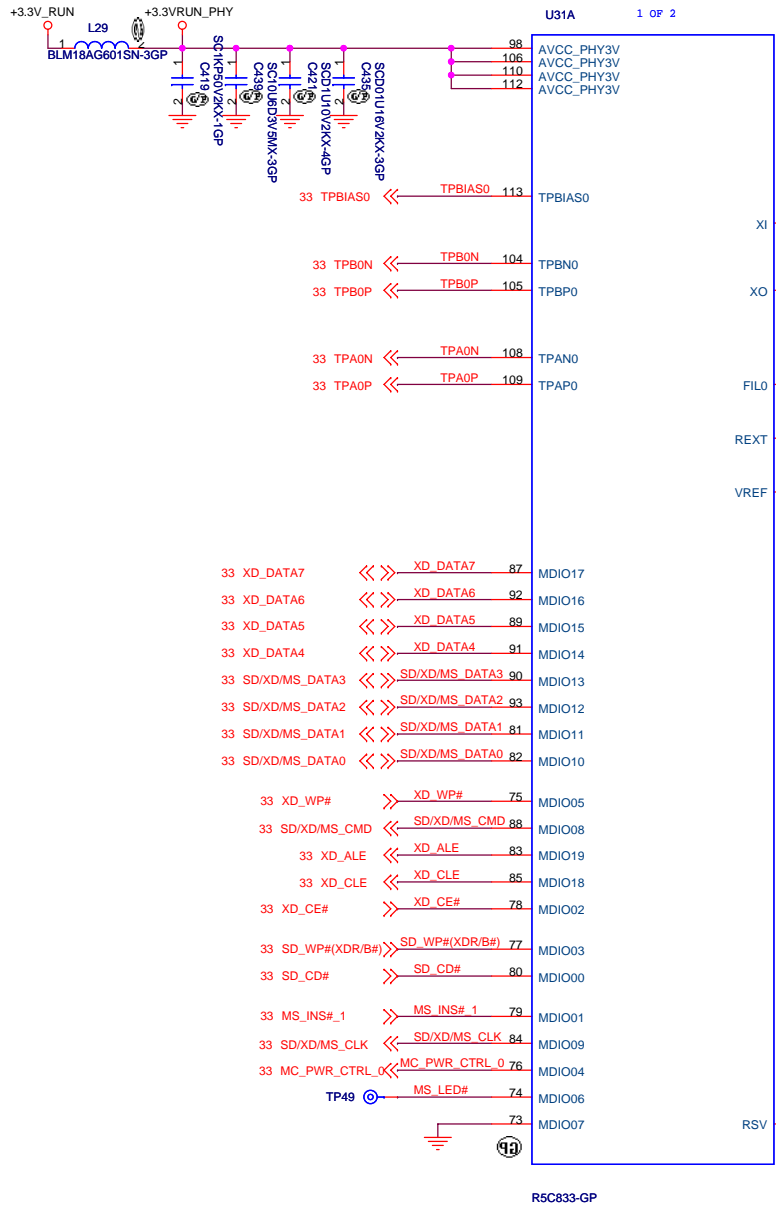
SE:070408

Layout note: Place caps EC87, EC88 close SIM Card connector.



SSID = 1394

600ohm 100MHz
200mA 0.5ohm DC



<-Variant Name>

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Title

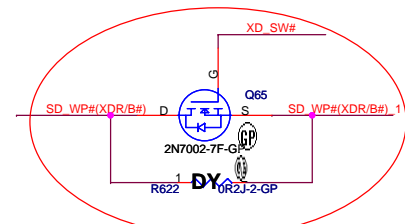
Thurman Discrete

Size **A3** Document Number **1394 R5C833** Rev **-1**

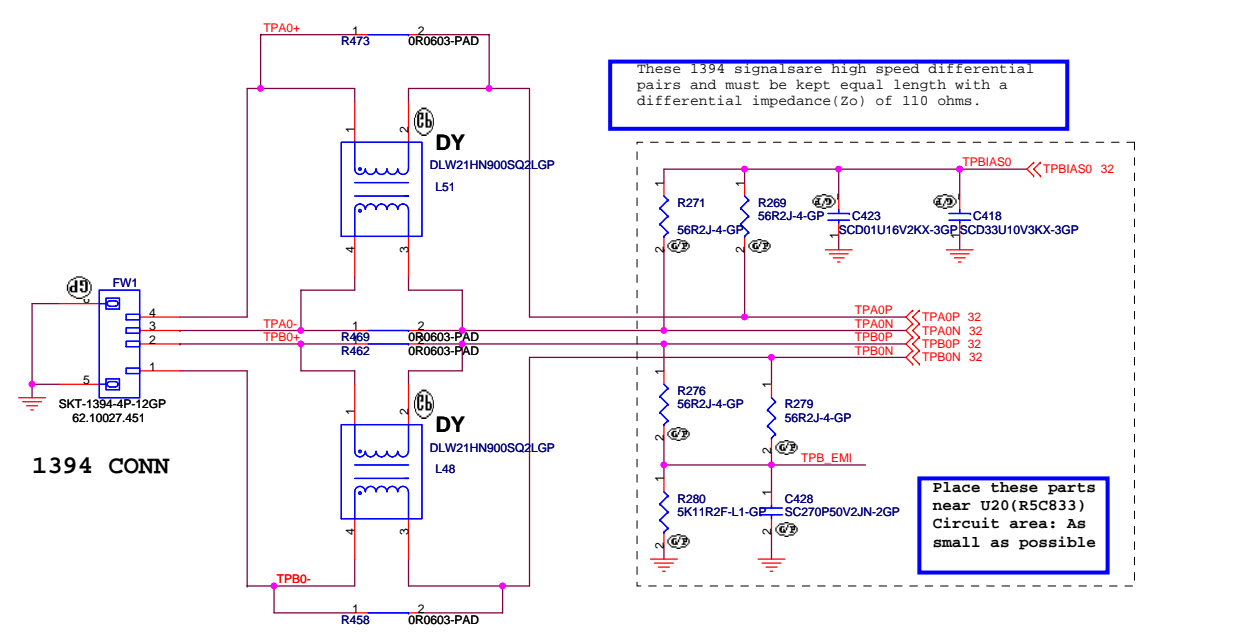
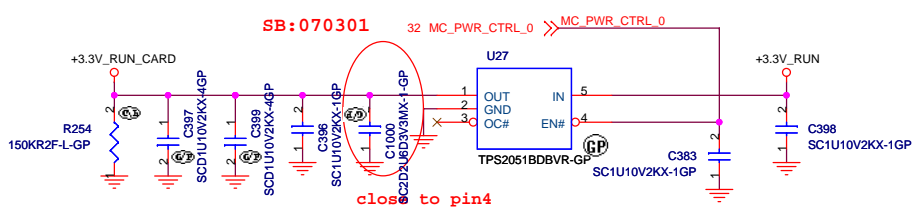
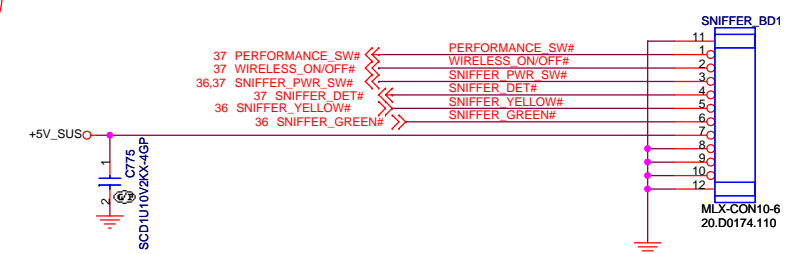
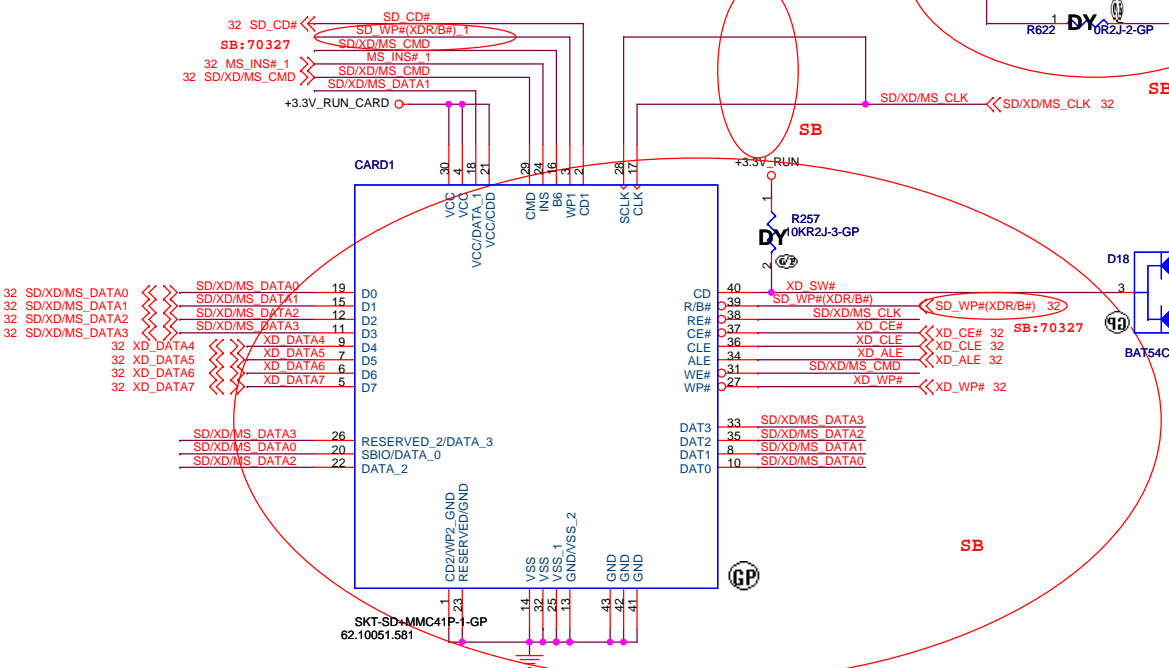
Date: Tuesday, November 06, 2007 Sheet 32 of 50

SSID = 1394

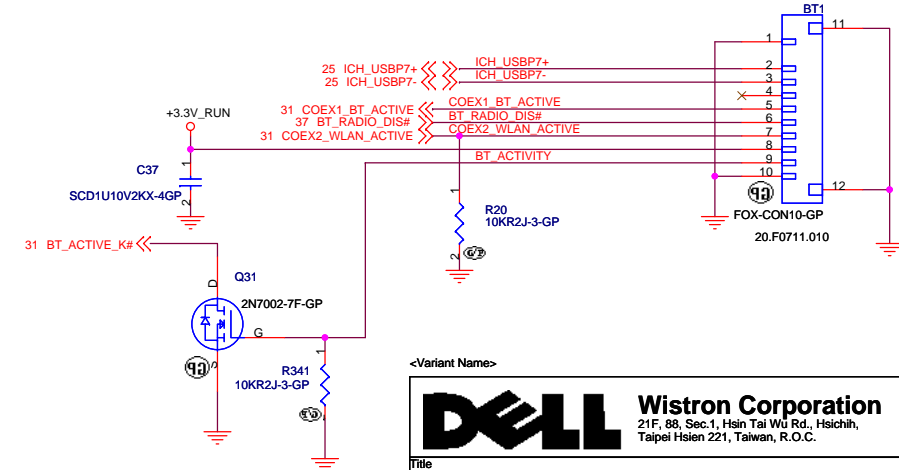
Card Reader CONN



SNIFFER BOARD CONN



Bluetooth Module conn.



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 Taipei Hsien 221, Taiwan, R.O.C.

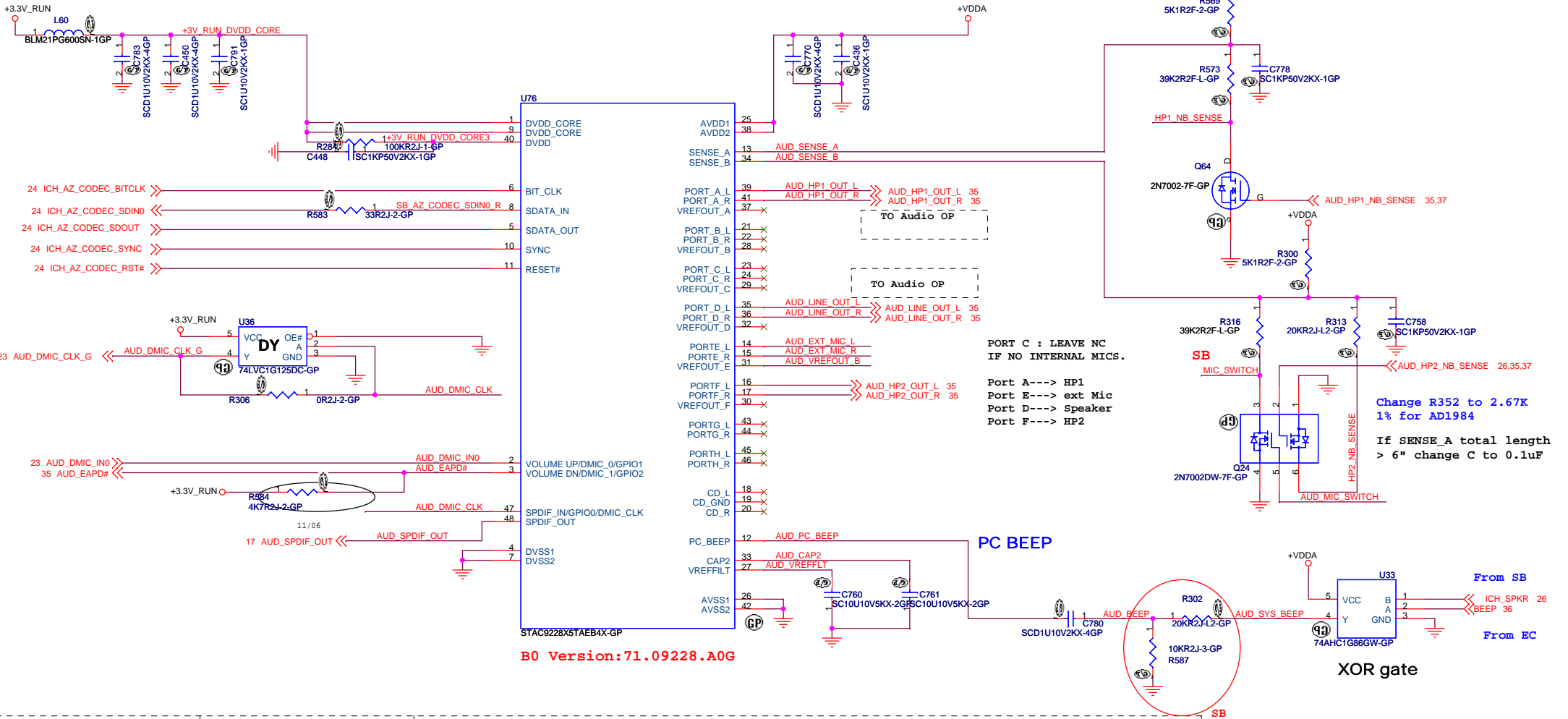
Thurman Discrete

8in1 /1394/SNIFFER BD CON/BT

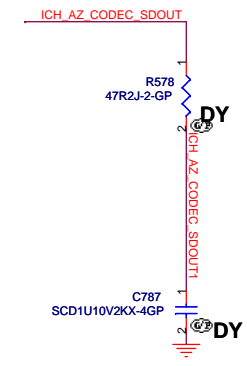
Rev -1

Date: Tuesday, November 06, 2007 Sheet 33 of 50

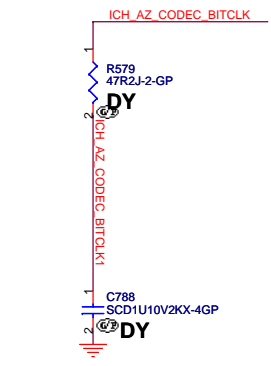
60ohm 100MHz
3000mA 0.05ohm DC



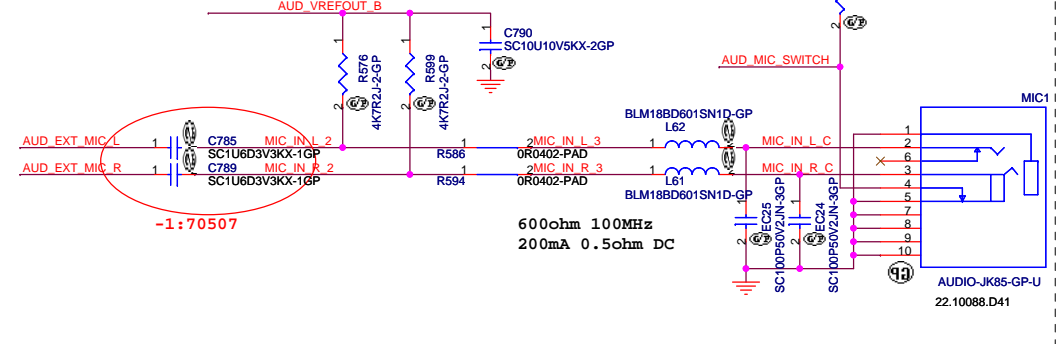
Azalia I/F EMI



Azalia I/F EMI



MIC IN



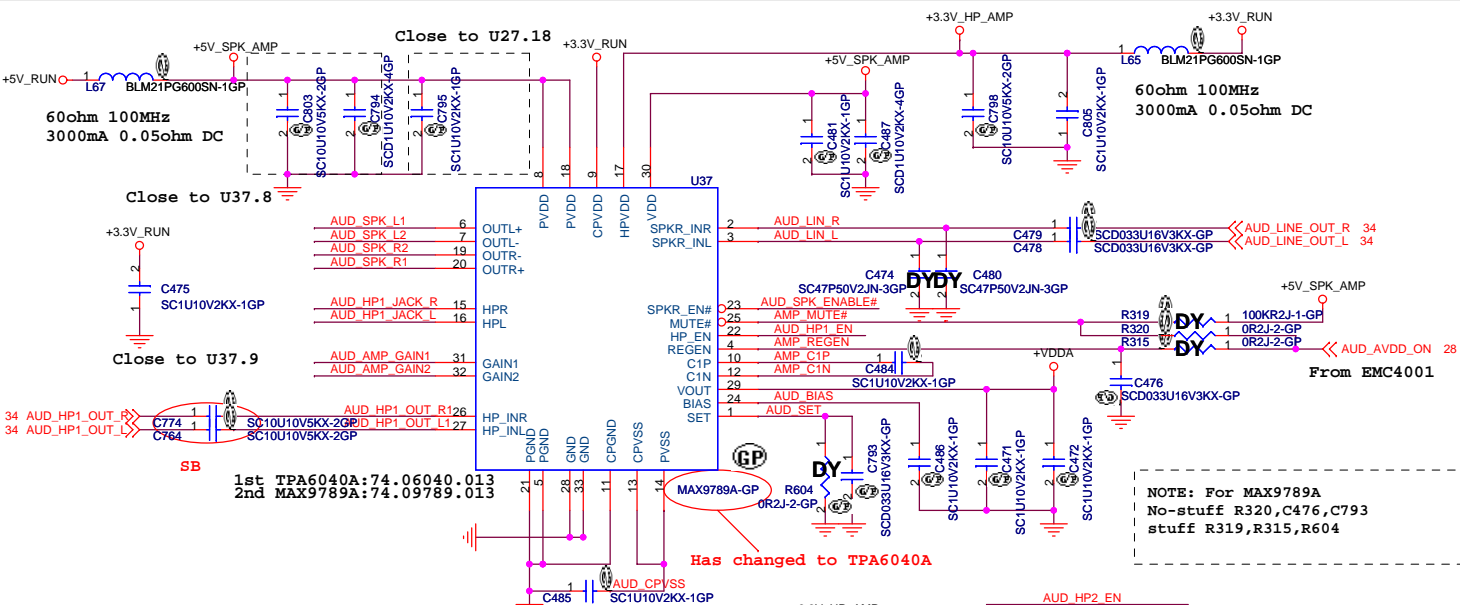
<Variant Name>

DELL Wistron Corporation
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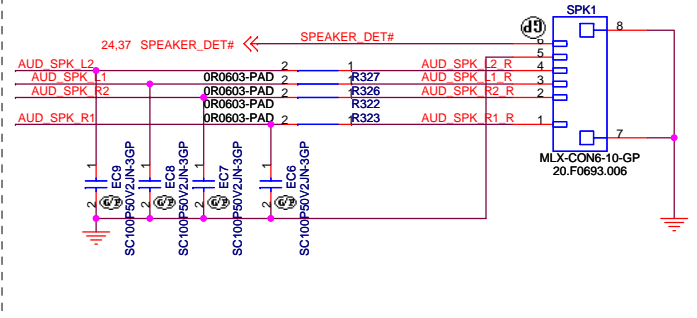
Title
Thurman Discrete

Size **A3** Document Number
CODEC STAC9228 Rev
-1

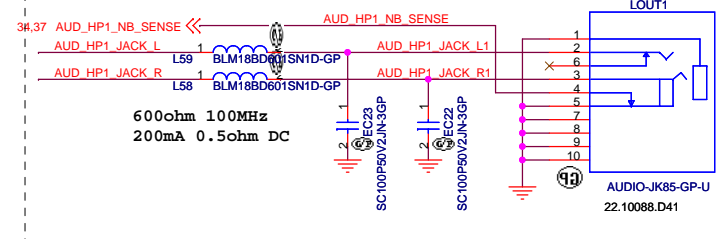
Date: Thursday, November 22, 2007 Sheet 34 of 50



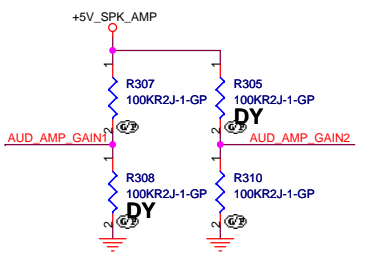
Speaker



LINE1 OUT

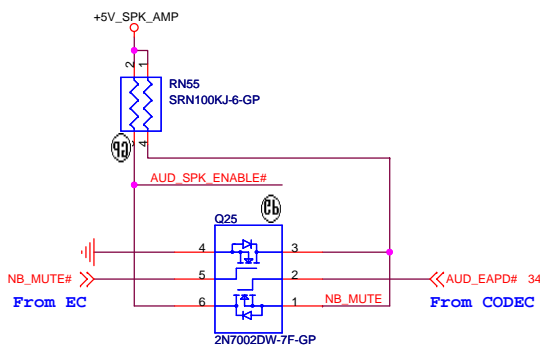


GAIN SETTING

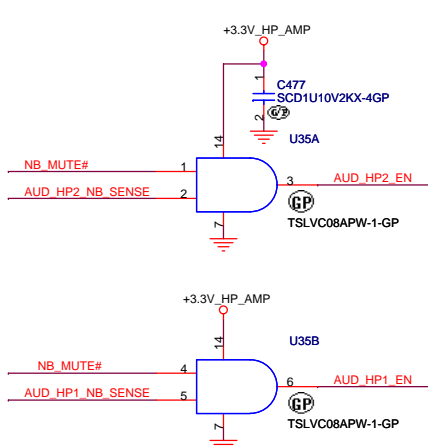


GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

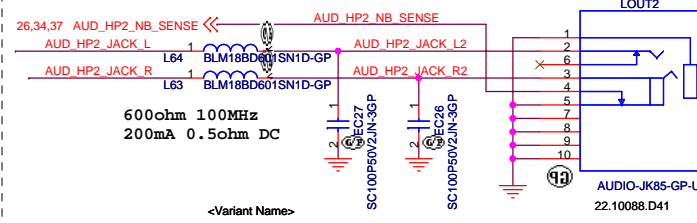
Signal inverter for speaker shutdown



AND Gate for HP Mute Function



LINE2 OUT



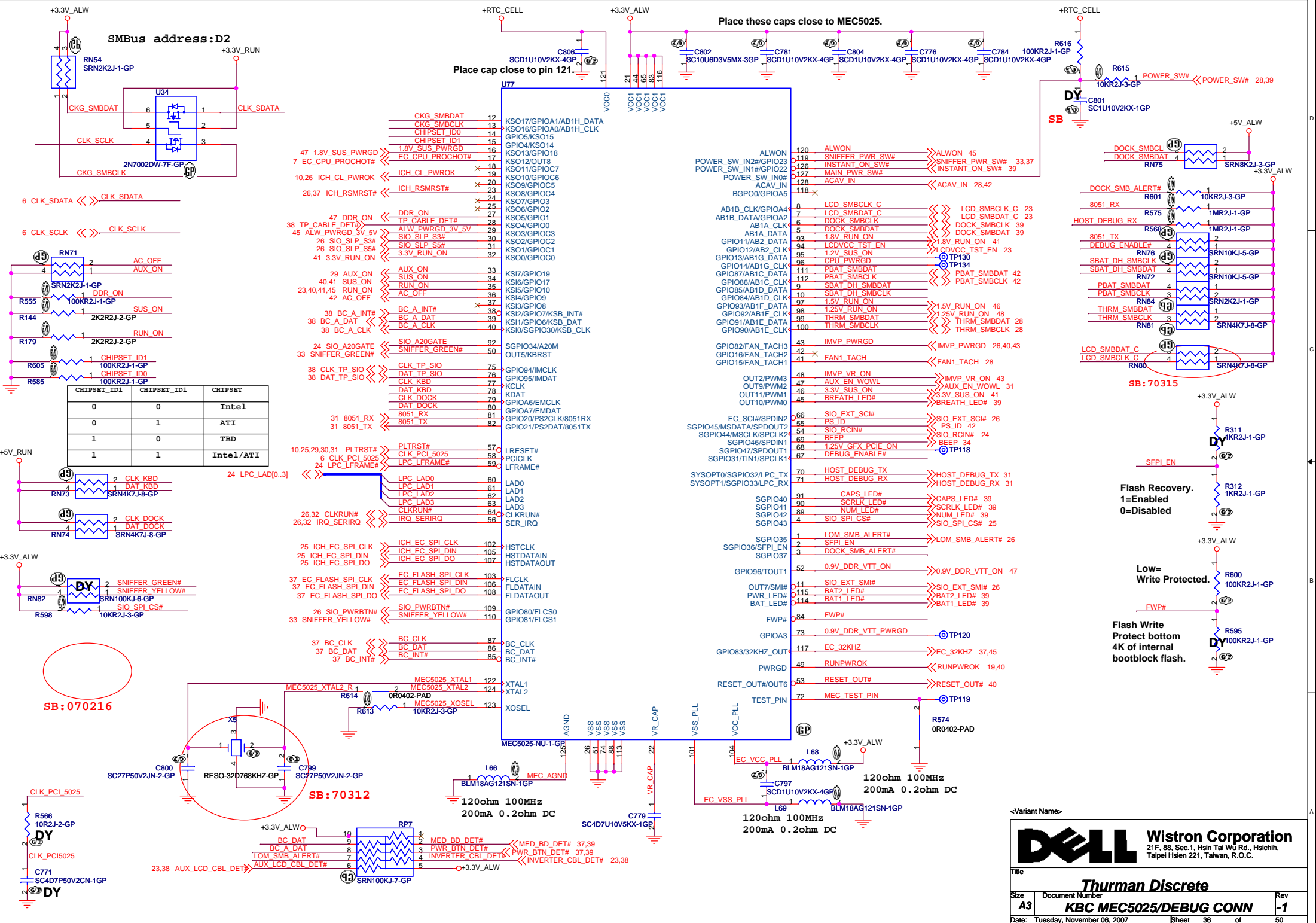
<-Variant Name>

Wistron Corporation
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Title: **Thurman Discrete**

Size: **A3** Document Number: **AUDIO AMP** Rev: **-1**

Date: Tuesday, November 06, 2007 Sheet 35 of 50



Place cap close to pin 121.

Place these caps close to MEC5025.

47 1.8V_SUS_PWRGD	1.8V SUS_PWRGD	16	GPI04/KS014
7 EC_CPU_PROCHOT#	EC_CPU_PROCHOT#	17	KS013/GPIO18
10,26 ICH_CL_PWROK	ICH_CL_PWROK	18	KS011/GPIOC7
	ICH_RSMRST#	19	KS010/GPIOC6
26,37 ICH_RSMRST#	ICH_RSMRST#	20	KS09/GPIOC5
	DDR_ON	21	KS08/GPIOC4
	TP_CABLE_DET#	22	KS07/GPIO3
	TP_CABLE_DET#	23	KS06/GPIO2
	ALW_PWRGD_3V_5V	24	KS05/GPIO1
	ALW_PWRGD_3V_5V	25	KS04/GPIO0
	SIO_SLP_S3#	26	KS03/GPIOC3
	SIO_SLP_S5#	27	KS02/GPIOC2
	3.3V_RUN_ON	28	KS01/GPIOC1
	3.3V_RUN_ON	29	KS00/GPIOC0
	AUX_ON	30	KS17/GPIO19
	SUS_ON	31	KS16/GPIO17
	RUN_ON	32	KS15/GPIO10
	AC_OFF	33	KS14/GPIO9
	AC_OFF	34	KS13/GPIO8
	BC_A_INT#	35	KS12/GPIO7/KSB_INT#
	BC_A_DAT	36	KS11/GPIO6/KSB_DAT
	BC_A_CLK	37	KS10/GPIO30/KSB_CLK
	SIO_A20GATE	38	SGPIO34/A20M
	SNIFFER_GREEN#	39	OUT5/KBRST
	CLK_TP_SIO	40	GPI04/IMCLK
	DAT_TP_SIO	41	GPI05/IMDAT
	DAT_KBD	42	KCLK
	CLK_DOCK	43	KDAT
	DAT_DOCK	44	GPI06/EMCLK
	8051_RX	45	GPI07/EMDAT
	8051_TX	46	GPI020/PS2CLK/8051RX
	8051_TX	47	GPI021/PS2DAT/8051TX
	PLTRST#	48	LRESSET#
	CLK_PCI_5025	49	PCICLK
	LPC_LFRAME#	50	LPC_LFRAME#
	LPC_LAD0	51	LAD0
	LPC_LAD1	52	LAD1
	LPC_LAD2	53	LAD2
	LPC_LAD3	54	LAD3
	CLKRUN#	55	CLKRUN#
	IRQ_SERIRQ	56	IRQ_SERIRQ
	ICH_EC_SPI_CLK	57	HSTCLK
	ICH_EC_SPI_DIN	58	HSTDATIN
	ICH_EC_SPI_DO	59	HSTDATOUT
	EC_FLASH_SPI_CLK	60	EC_FLASH_SPI_CLK
	EC_FLASH_SPI_DIN	61	EC_FLASH_SPI_DIN
	EC_FLASH_SPI_DO	62	EC_FLASH_SPI_DO
	SIO_PWRBTN#	63	GPI080/FLCS0
	SNIFFER_YELLOW#	64	GPI081/FLCS1
	BC_CLK	65	BC_CLK
	BC_DAT	66	BC_DAT
	BC_INT#	67	BC_INT#
	MED_BD_DET#	68	MED_BD_DET#
	PWR_BTN_DET#	69	PWR_BTN_DET#
	INVERTER_CBL_DET#	70	INVERTER_CBL_DET#
	AUX_LCD_CBL_DET#	71	AUX_LCD_CBL_DET#

CHIPSET_ID1	CHIPSET_ID1	CHIPSET
0	0	Intel
0	1	ATI
1	0	TBD
1	1	Intel/ATI

Flash Recovery.
1=Enabled
0=Disabled

Low=
Write Protected.

Flash Write
Protect bottom
4K of internal
bootblock flash.

Variant Name:

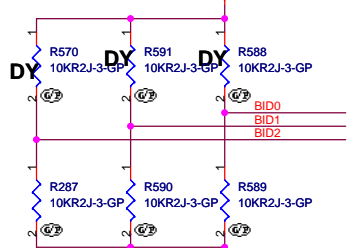
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Thurman Discrete**

Size: **A3** Document Number: **KBC MEC5025/DEBUG CONN** Rev: **-1**

Date: Tuesday, November 06, 2007 Sheet 36 of 50

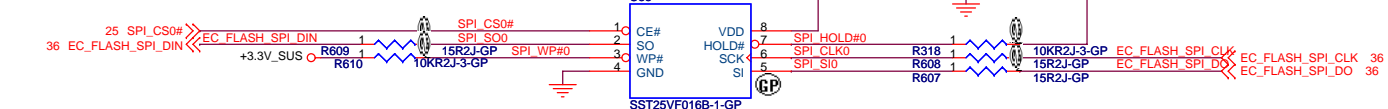
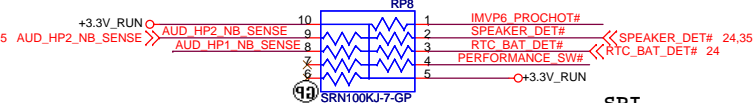
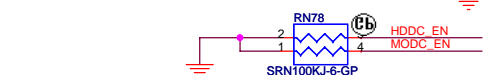
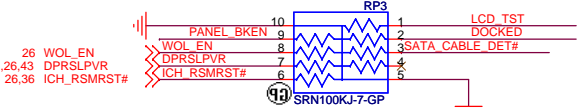
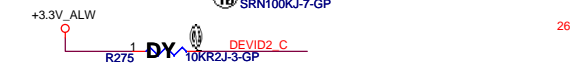
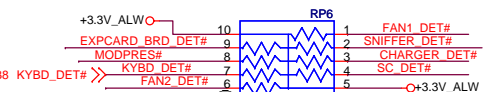
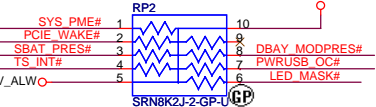
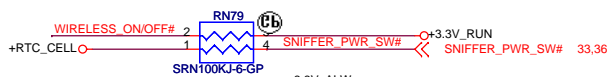
Board ID Straps



BID1	BID0	Board Rev.
0	0	ENG1 (M00)
0	1	ENG2 (X00)
1	0	ENG3 (X01)
1	1	ENG4 (X02)
0	0	RAMP (A00)

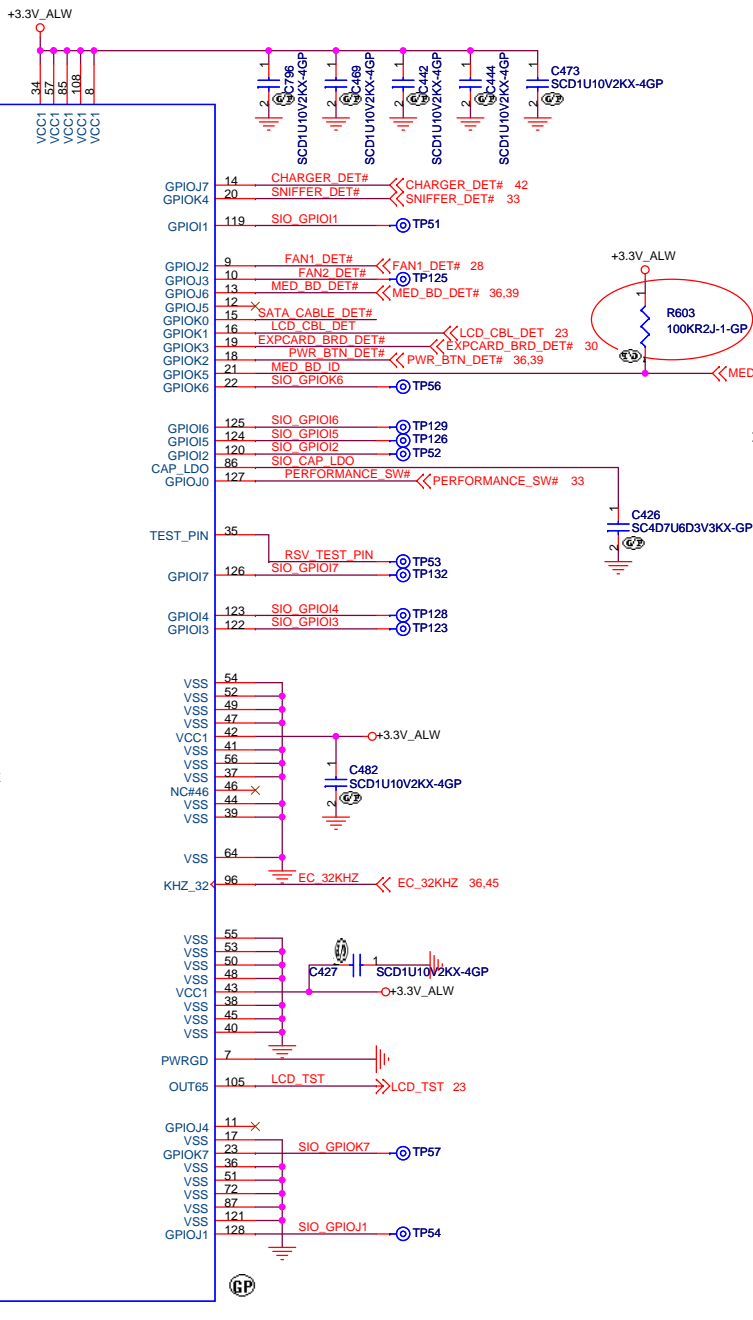
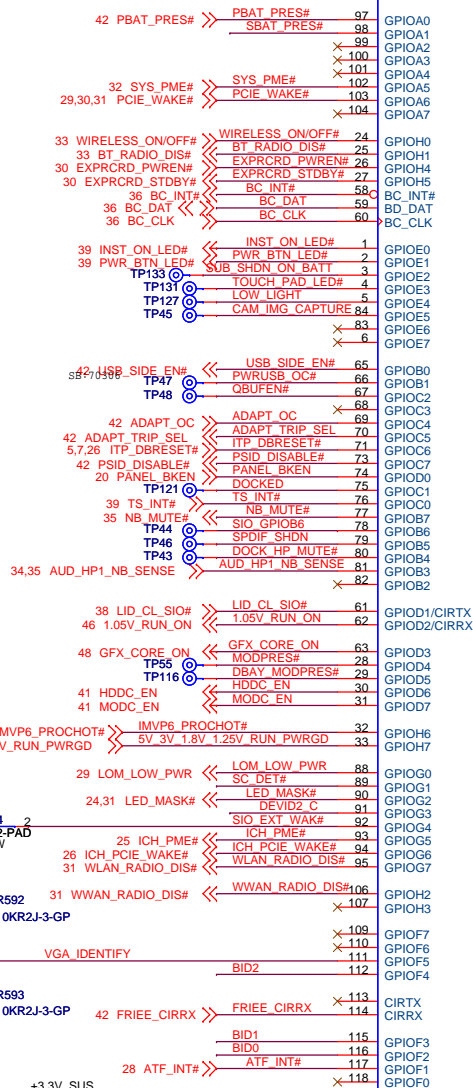
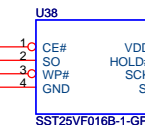
BID2:
 0: Intel CPU + Intel Chipset
 1: Intel CPU + ATI Chipset

SB:70306



VGA IDENTITY
 1= Discrete GFX
 0=UMA

SPI

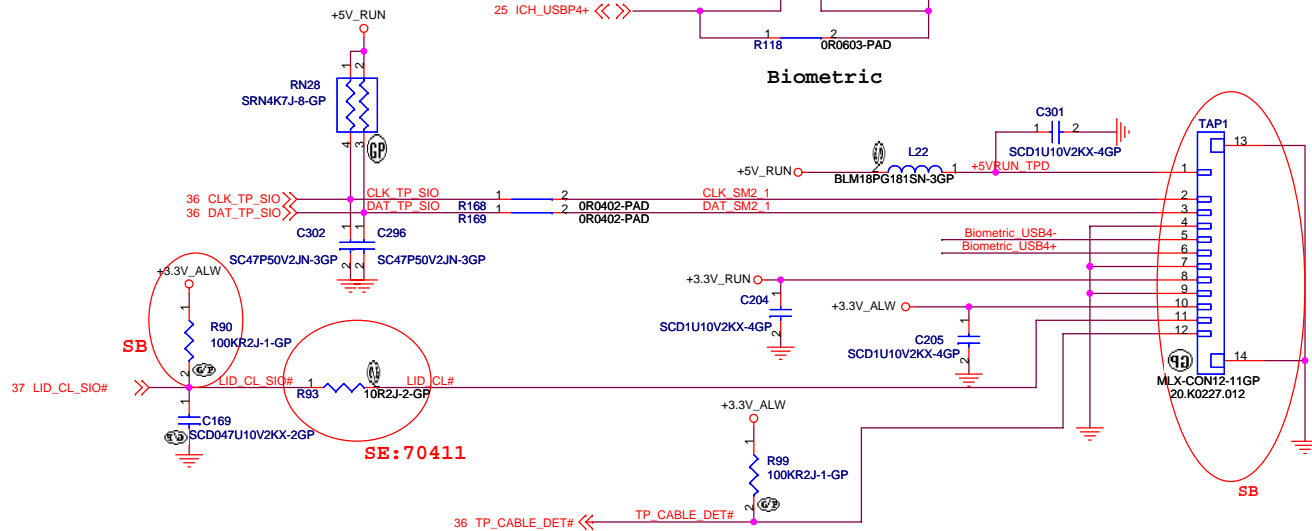
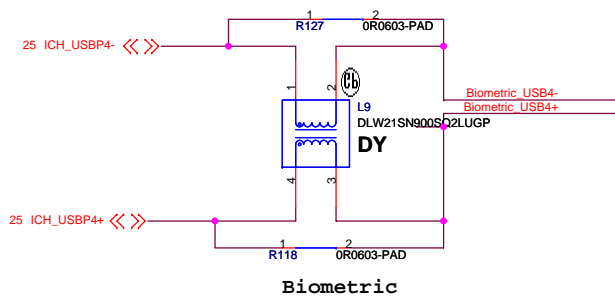
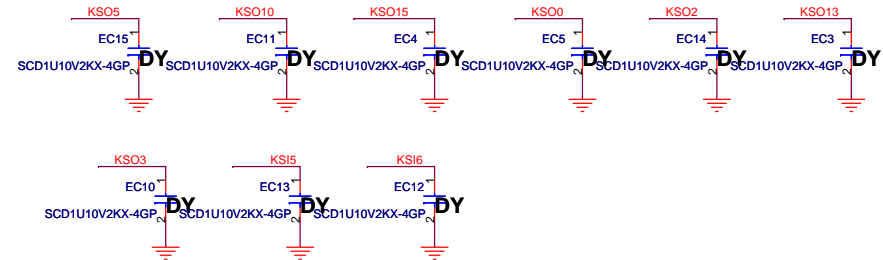
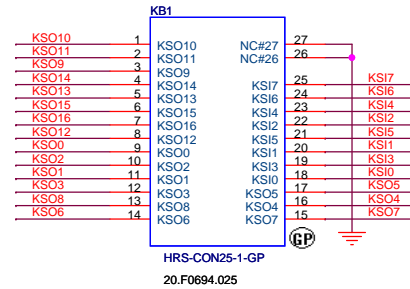
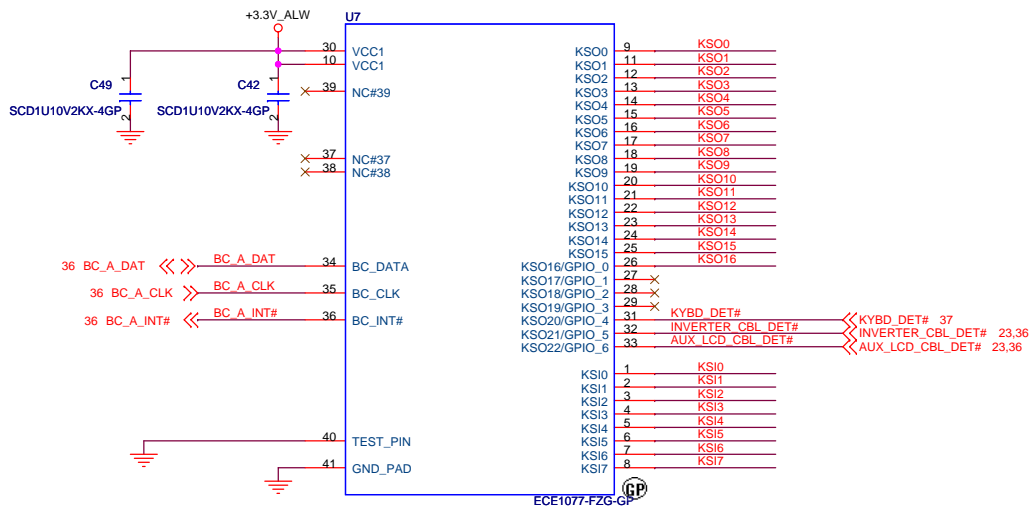


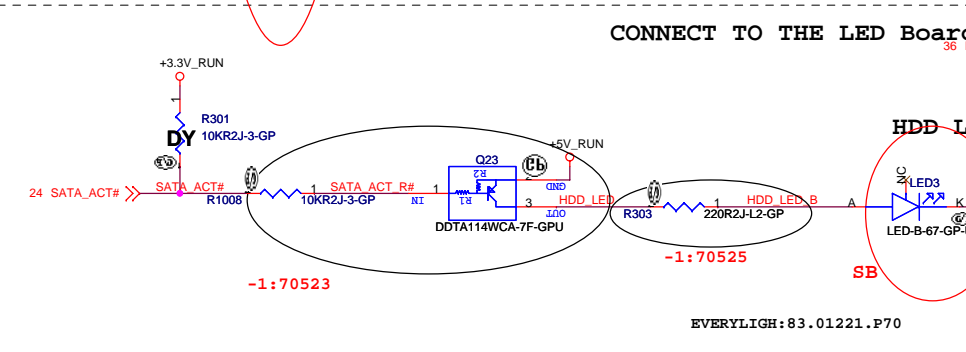
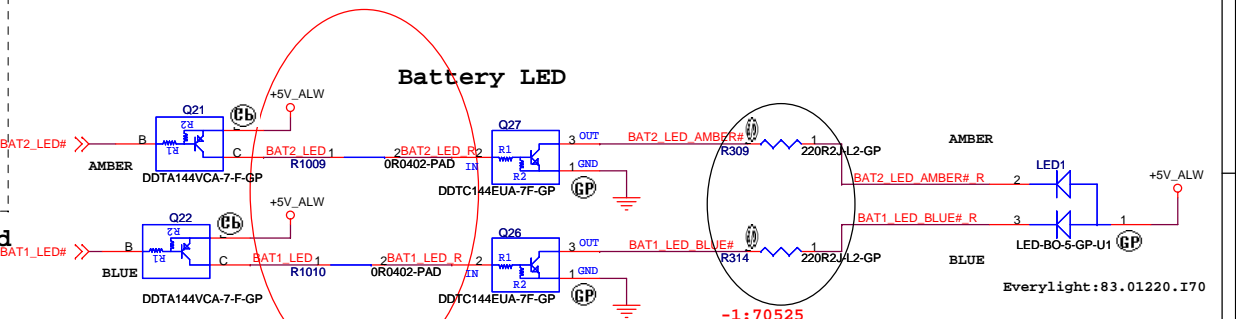
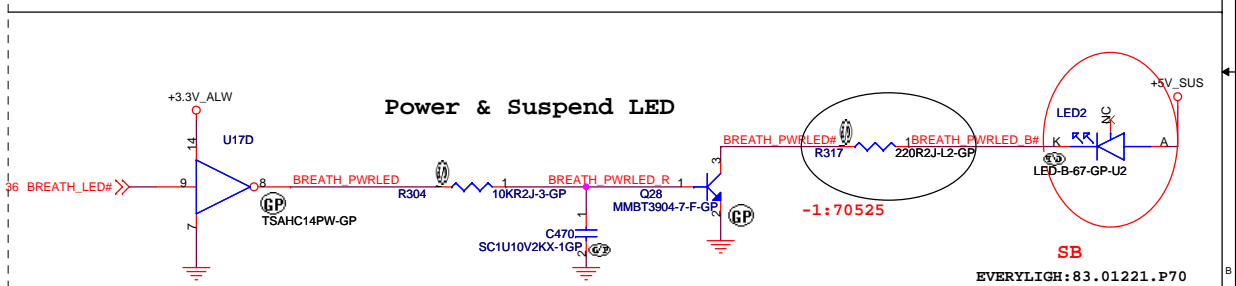
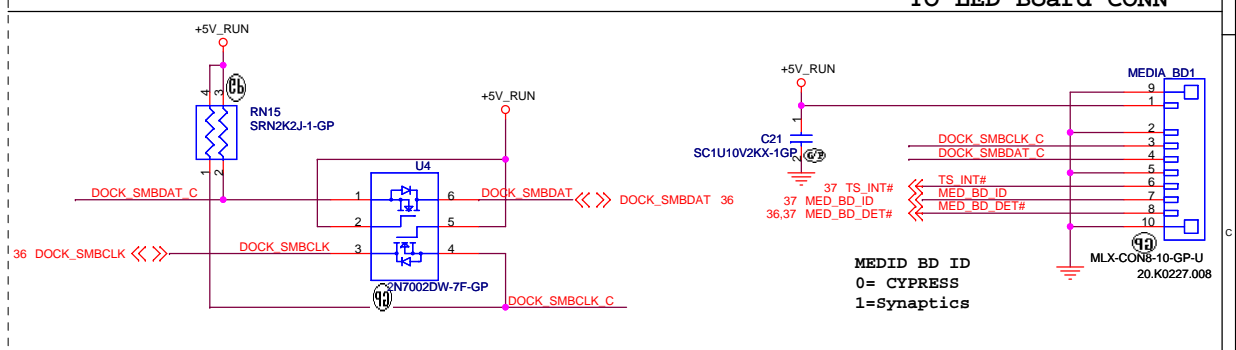
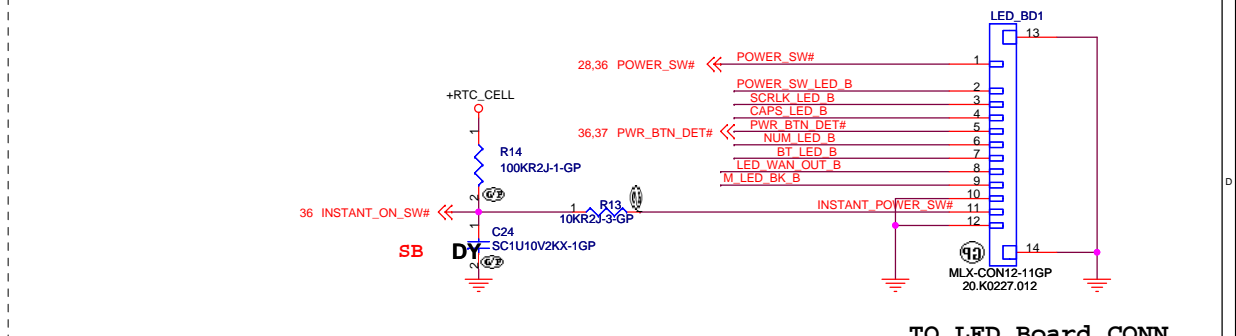
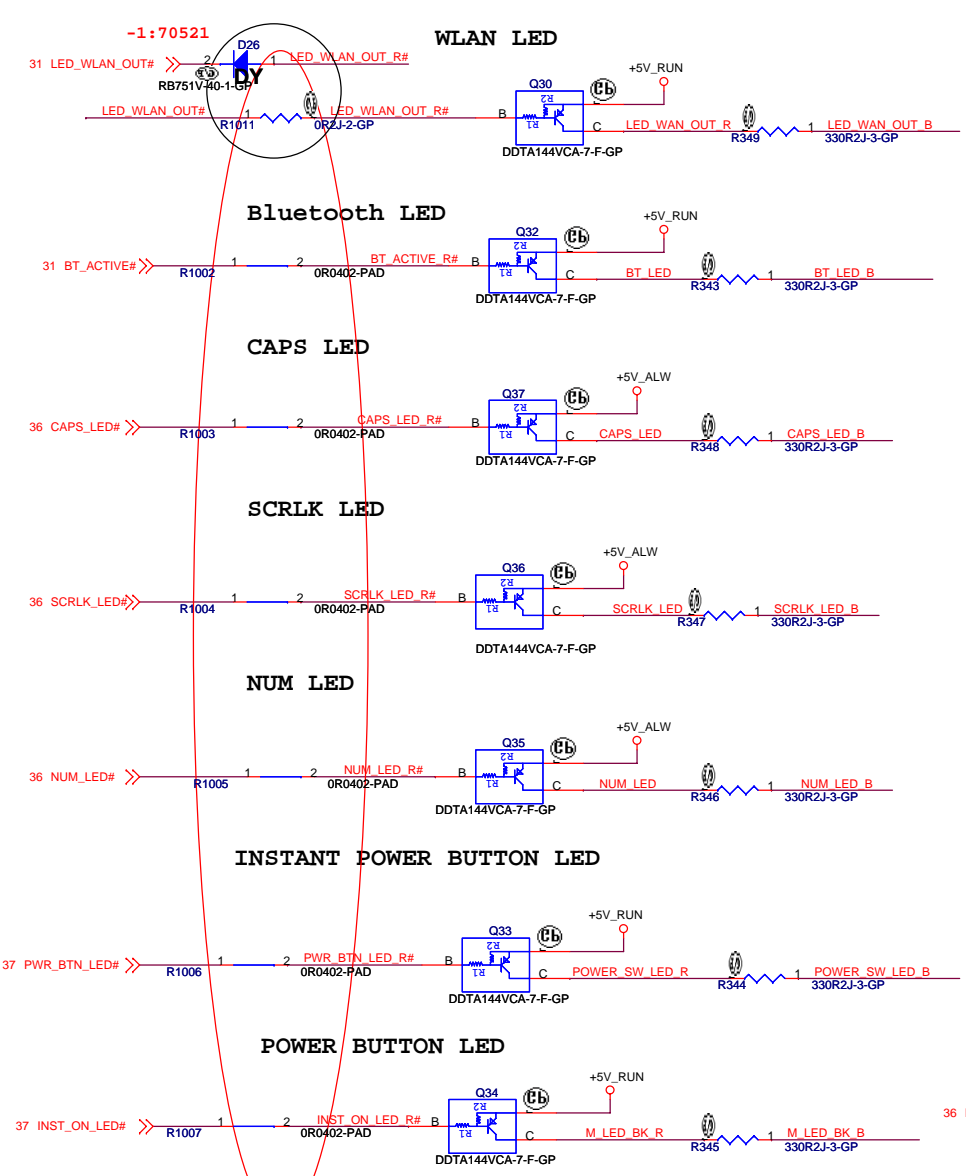
MEDID BD ID
 0= CYPRESS
 1=Synaptics

<Variant Name>



File	Thurman Discrete	
Size	Document Number	Rev
A3	SIO ECE5011/SPI ROM	-1
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LED Placement

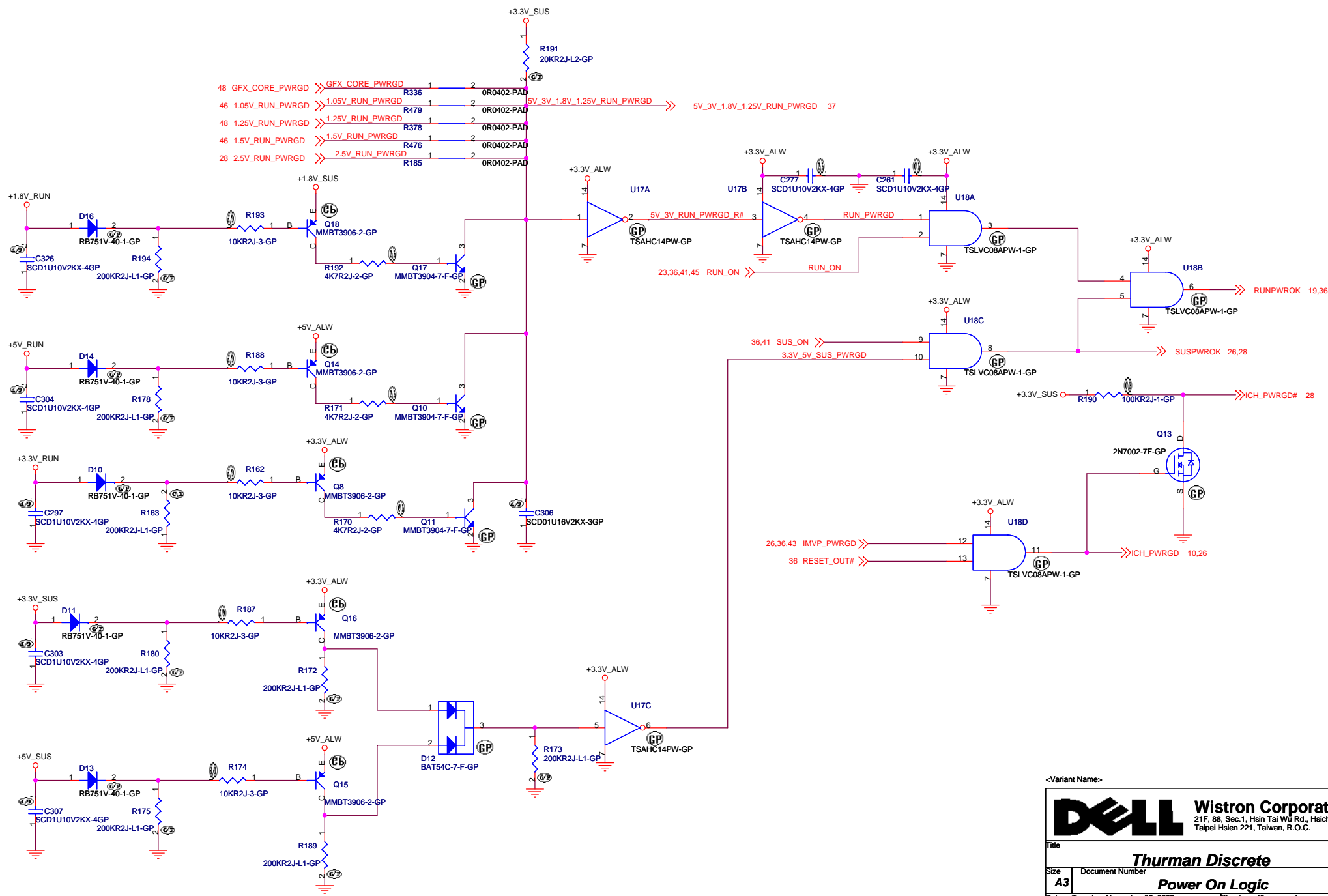
POWER LED1	HDD LED2	BATTERY LED3
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File: **Thurman Discrete**

Size: **A3** Document Number: **LED BD/Capacity Button BD** Rev: **-1**

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<Variant Name>

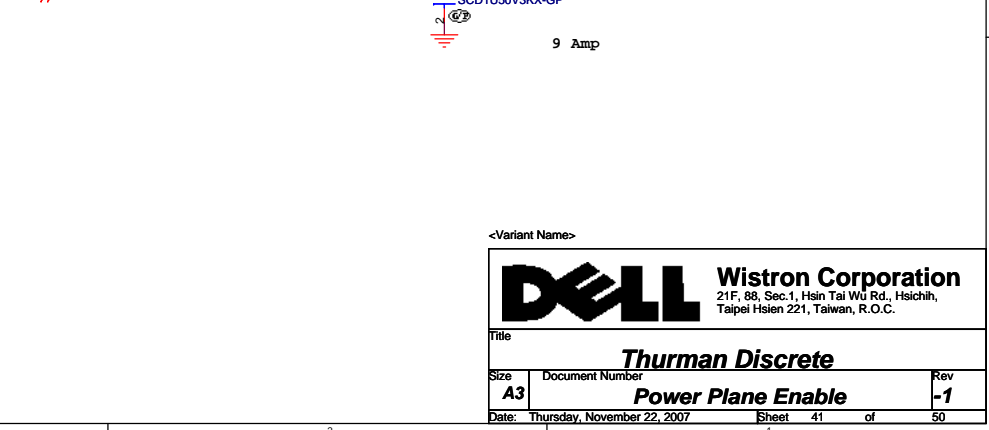
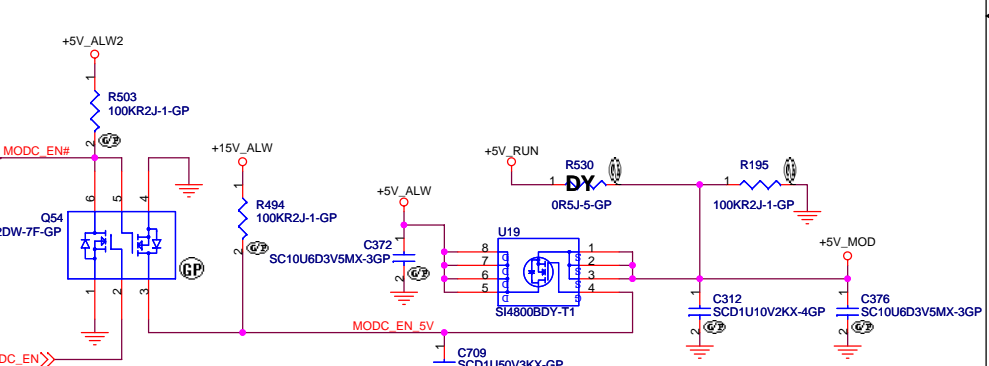
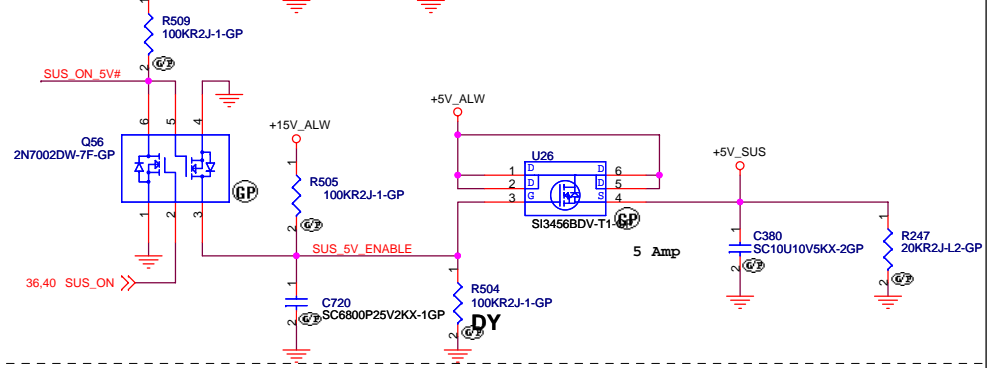
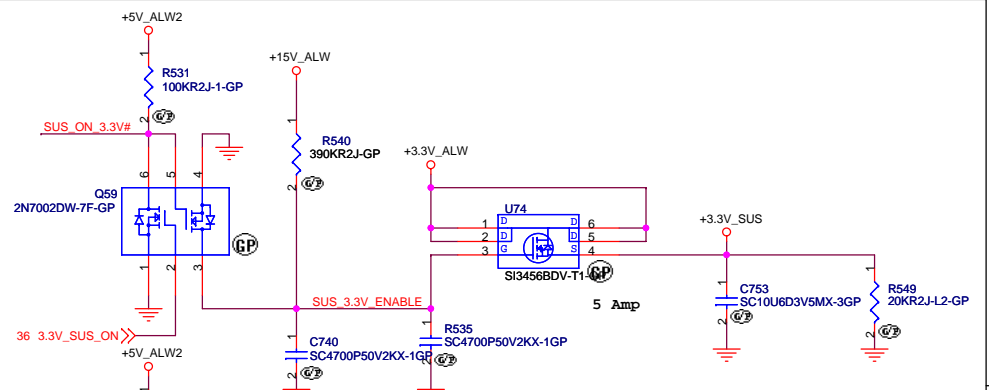
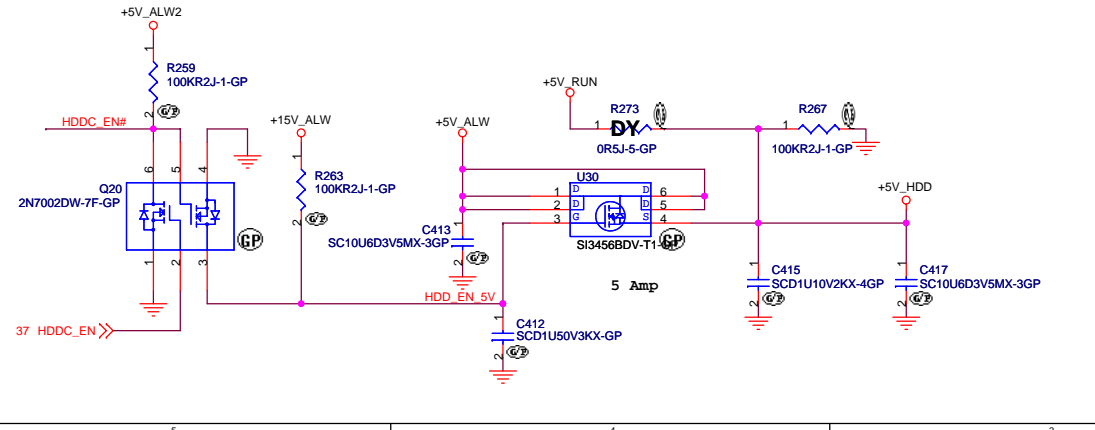
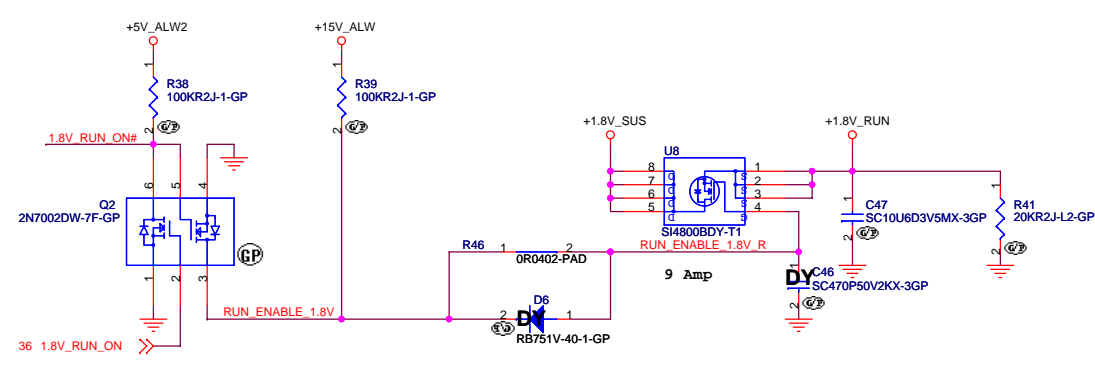
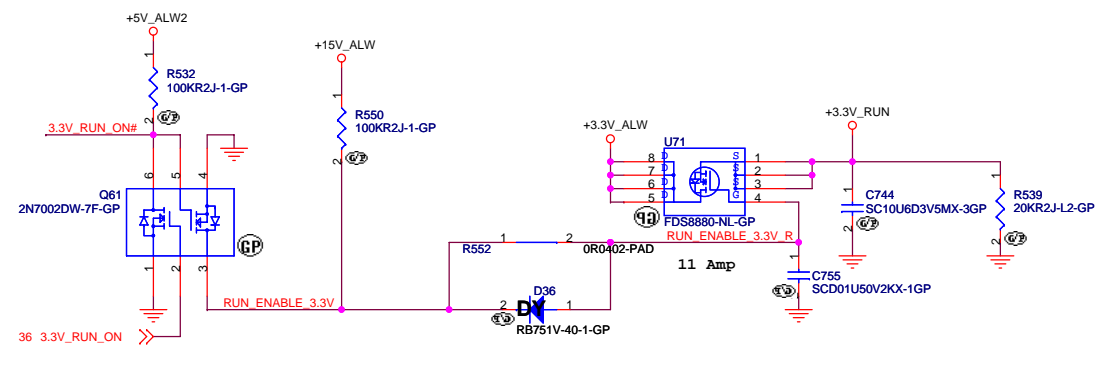
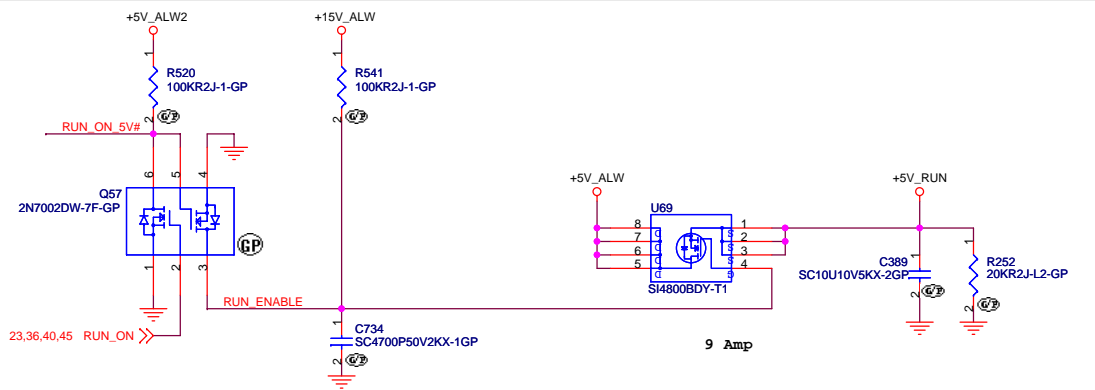
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Title

Thurman Discrete

Size	Document Number	Rev
A3	Power On Logic	-1

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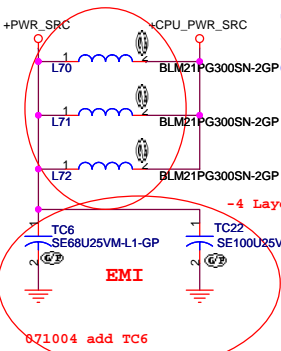
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Title: **Thurman Discrete**

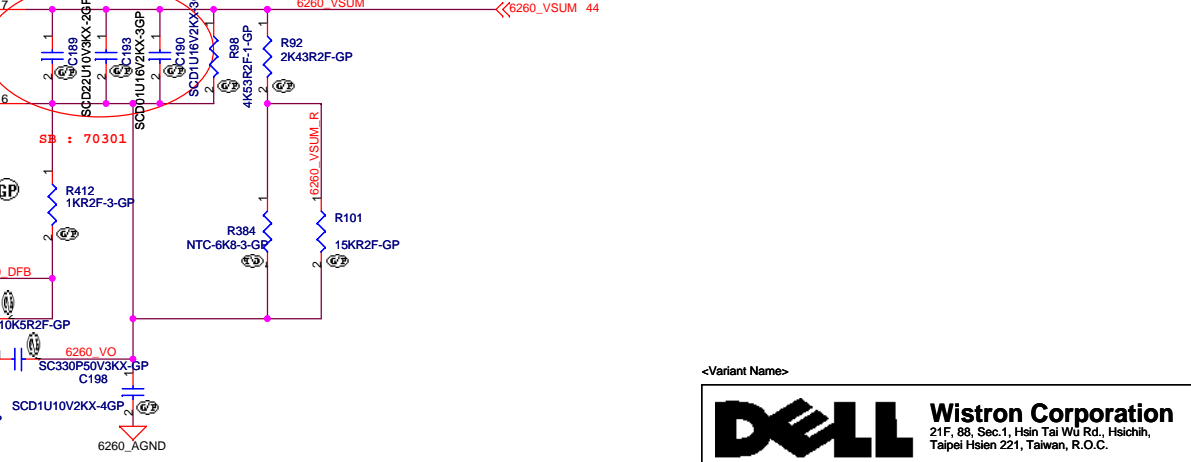
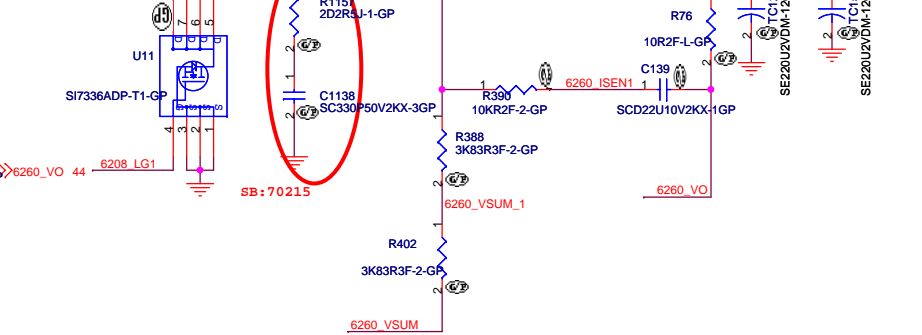
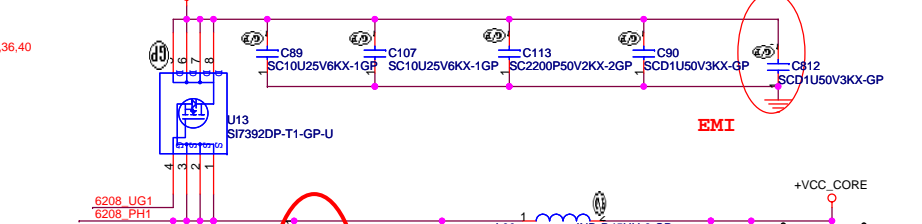
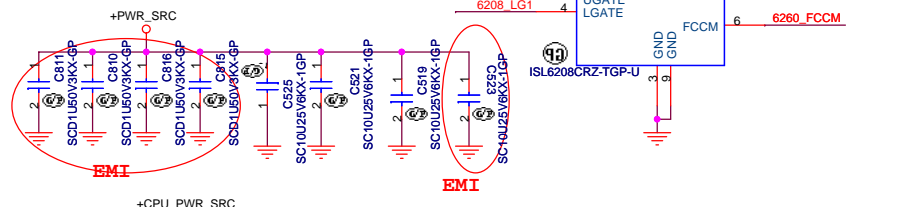
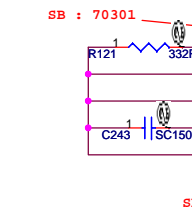
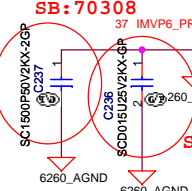
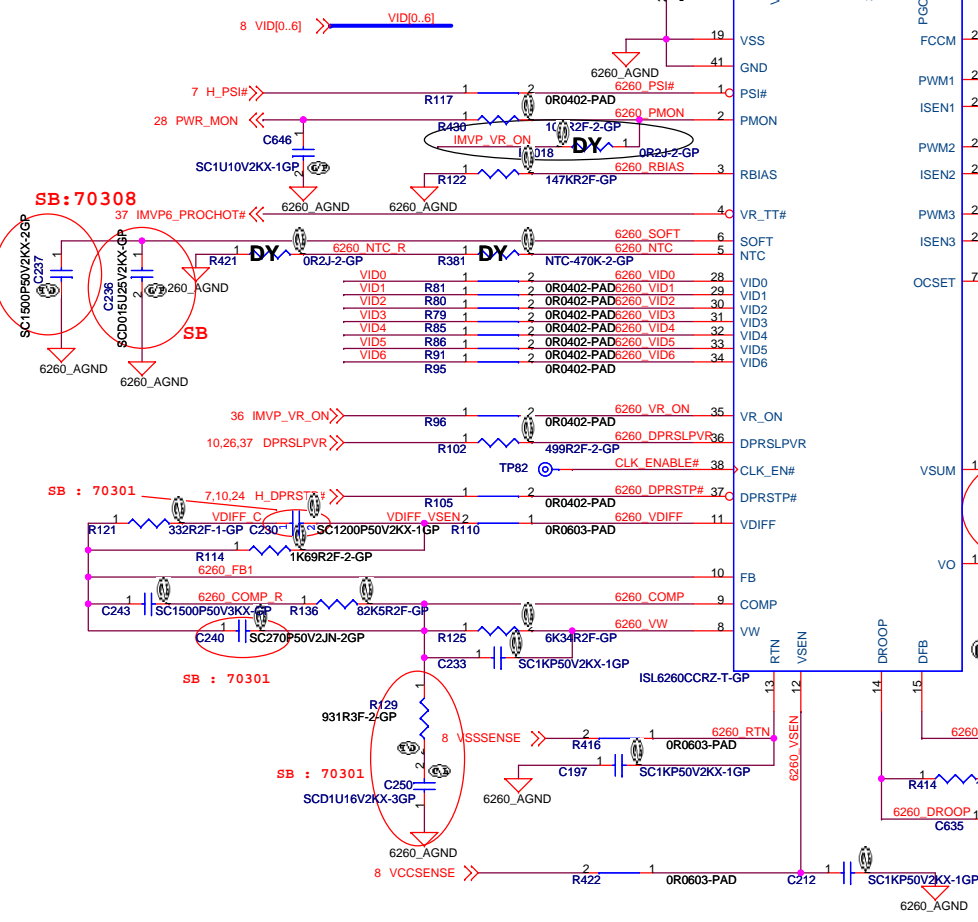
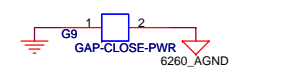
Size: **A3** Document Number: **Power Plane Enable** Rev: **-1**

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Thermal Design = 35.2A
 Peak Current [Ipeak] = 44A
 OCP design = 1.2 * Ipeak

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
 Inductor: 0.45UH ETQP4LR45XFC/ 68.R4510.10A
 O/P cap: 330U 2V EFSX0D331XE/ 79.33719.20L
 H/S: SI7392DP/ POWERPAK-8/ 16.5mOhm/ 4.5Vgs/ 84.07392.A37
 L/S: SI7336ADP/ POWERPAK-8/ 4mOhm/ 4.5Vgs/ 84.07336.B37



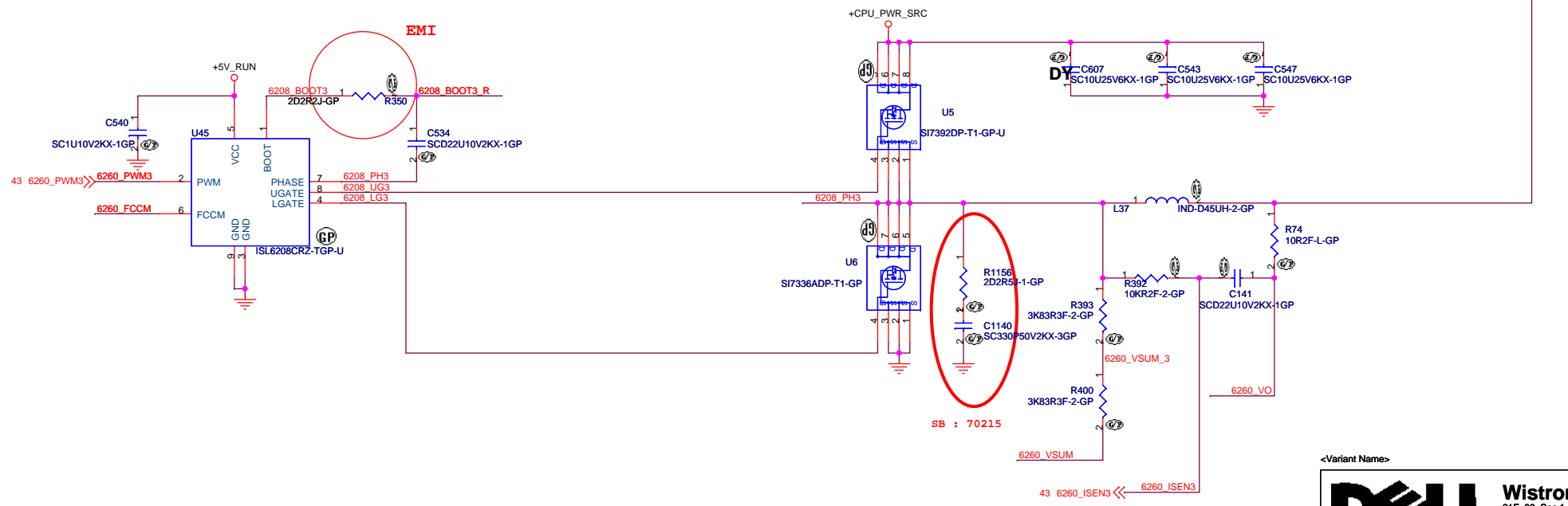
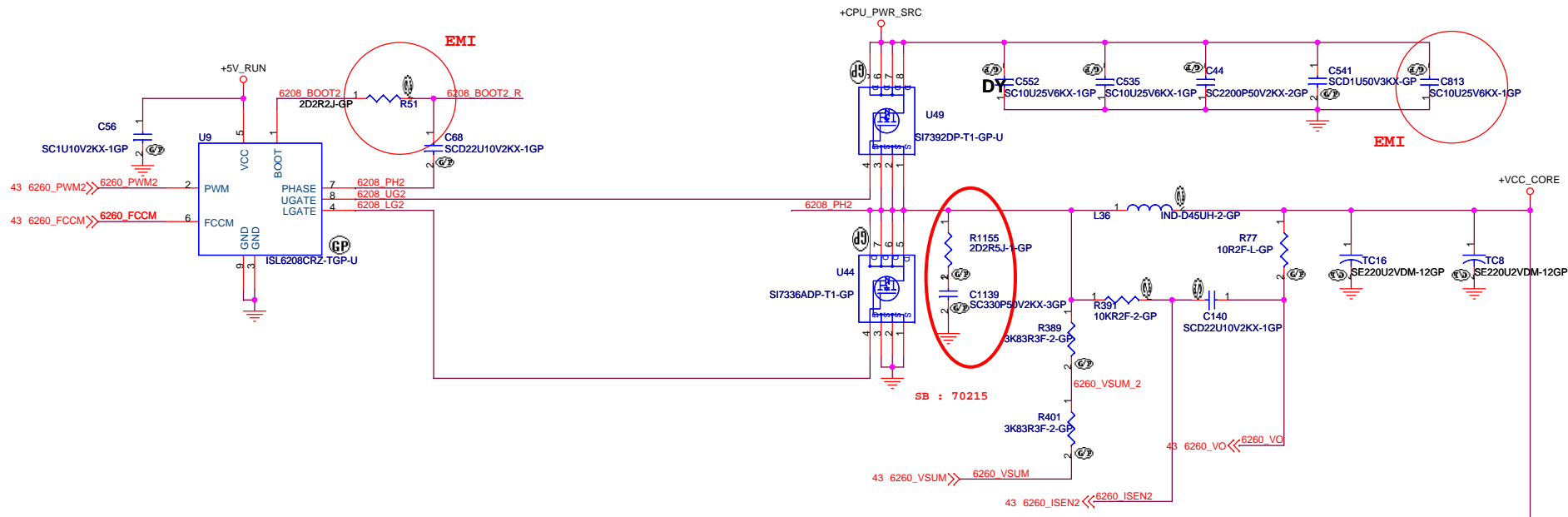
<Variant Name>

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Title: **Thurman Discrete**

Size: **A3** Document Number: **CPU Core-01** Rev: **-1**

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<Variant Name>

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 Taipei Hsien 221, Taiwan, R.O.C.

Title

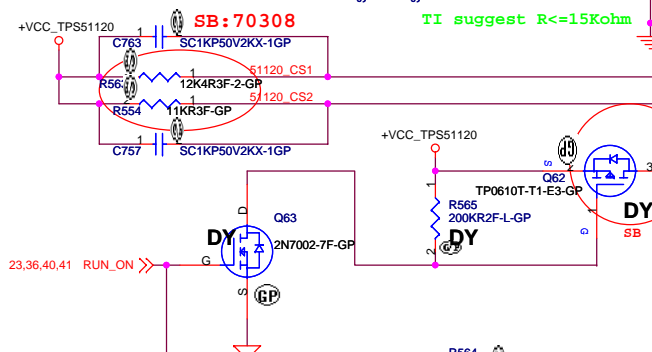
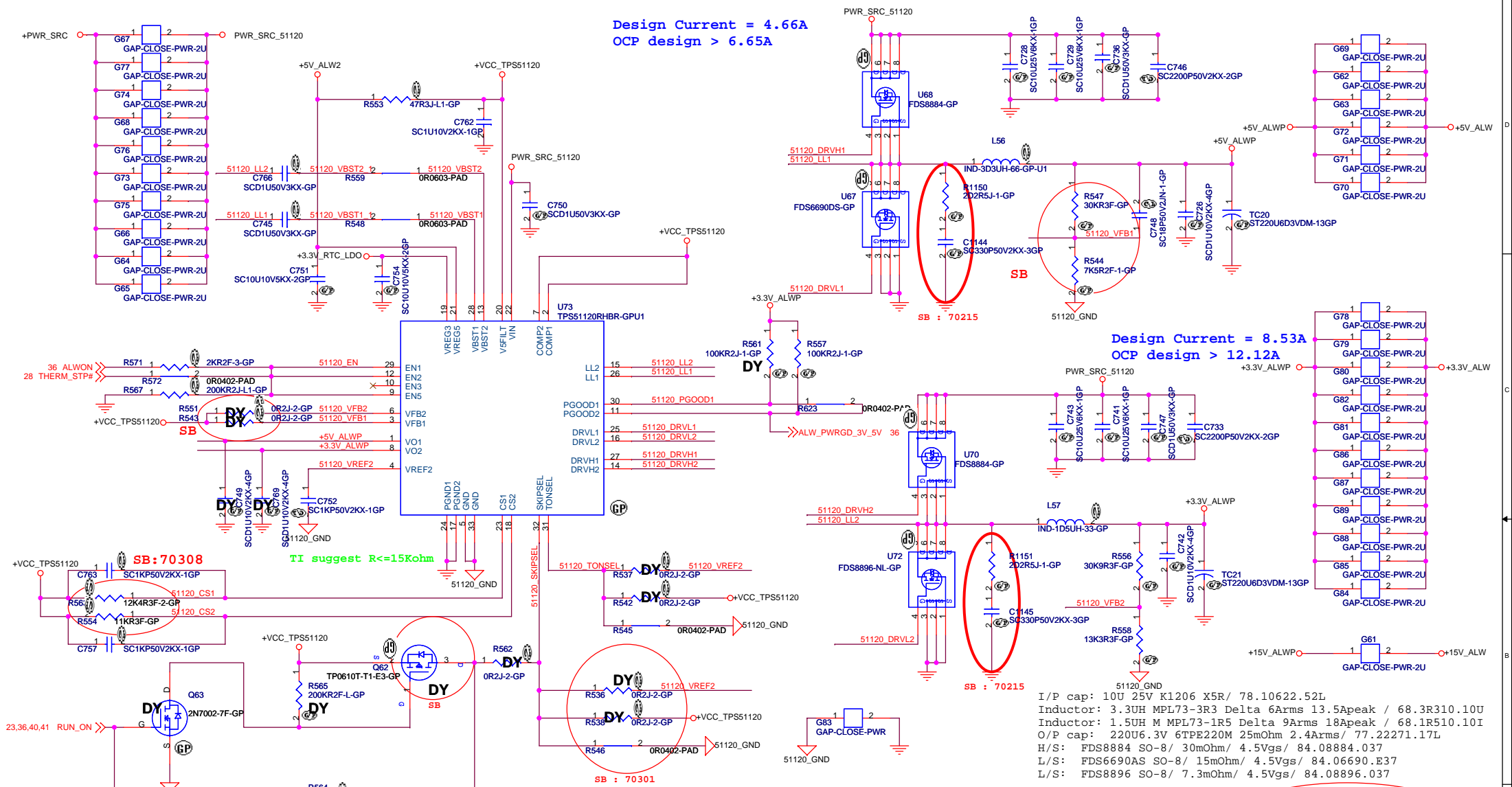
Thurman Discrete

Size	Document Number	Rev
A3	CPU Core-02	-1

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Design Current = 4.66A
OCP design > 6.65A

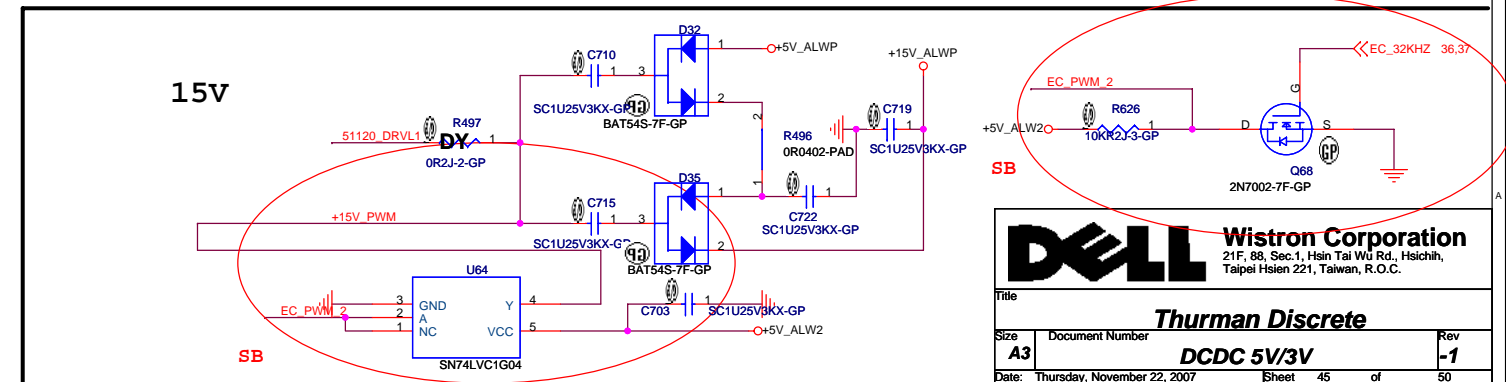
Design Current = 8.53A
OCP design > 12.12A



$V_{out} = 1V * (R1 + R2) / R2$

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
 Inductor: 3.3UH MPL73-3R3 Delta 6Arms 13.5Apeak / 68.3R310.10U
 Inductor: 1.5UH M MPL73-1R5 Delta 9Arms 18Apeak / 68.1R510.10I
 O/P cap: 220U6.3V 6TPE220M 25mOhm 2.4Arms/ 77.22271.17L
 H/S: FDS8884 SO-8/ 30mOhm/ 4.5Vgs/ 84.08884.037
 L/S: FDS6690AS SO-8/ 15mOhm/ 4.5Vgs/ 84.06690.E37
 L/S: FDS8896 SO-8/ 7.3mOhm/ 4.5Vgs/ 84.08896.037

	GND	VREF2	PLX01	V5FIL2
SKIPSEL	AUTOSKIP	AUTOSKIP / FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 580k/CH2	280k/CH1 430k/CH2	220k/CH1 330k/CH2	180k/CH1 2870k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1,EN2	Switcher OFF	not use	Switcher ON	Switcher ON
EN3,EN5	LDO OFF	not use	LDO ON	VR203 ON

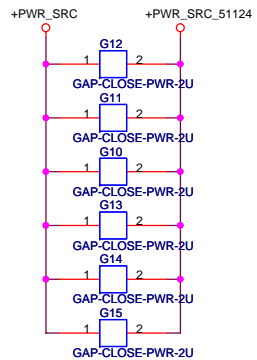


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Title: **Thurman Discrete**

Size: **A3** Document Number: **DCDC 5V/3V** Rev: **-1**

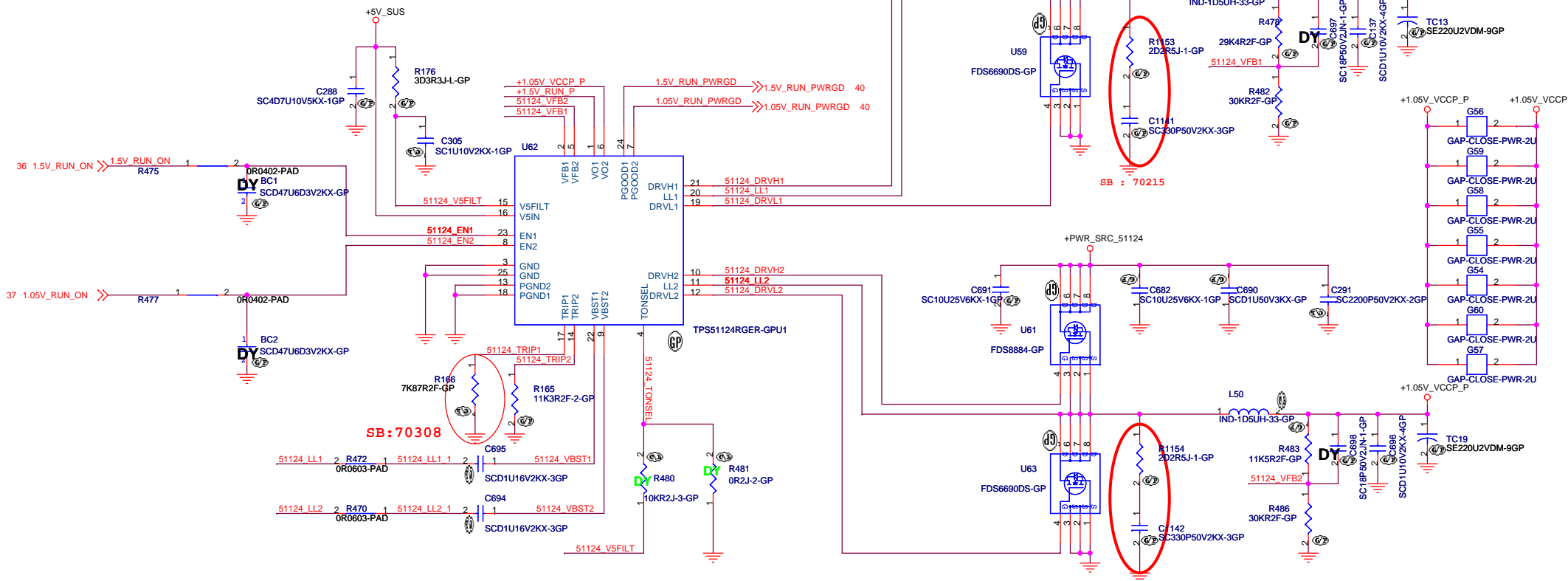
Date: Thursday, November 22, 2007 Sheet 45 of 50



$V_{trip}(mV) = R_{trip}(Kohm) * 10(\mu A)$
 $I_{ocp} = (V_{trip}/R_{dson}) + ((1/(2*L*f)) * ((V_{in}-V_{out}) * V_{out})/V_{in})$

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
 Inductor: 1.5UH M MPL73-1R5 Delta 9Arms 18Apeak / 68.1R510.10I
 O/P cap: 220U 2V EEF5X0D221ER 9mOhm 3Arms Panasonic/ 79.22719.2PL
 H/S: FDS8884 SO-8/ 30mOhm/ 4.5Vgs/ 84.08884.037
 L/S: FDS6690AS SO-8/ 15mOhm/ 4.5Vgs/ 84.06690.E37

Design Current = 6.0A
 OCP design > 6.8A
 Included 1.25V LDO(3.02A)



SB: 70308

SB: 70215

SB: 70215

Design Current= 5.9A
 OCP design > 7.3A

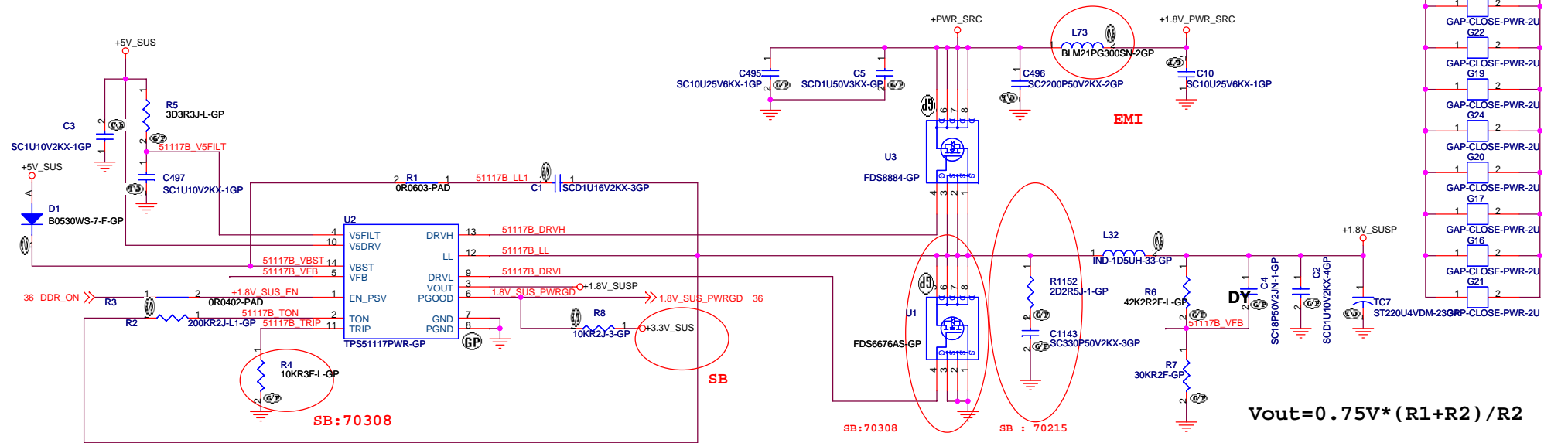
	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

$V_{out} = 0.758V * (R1+R2)/R2$ --> PWM mode
 $V_{out} = 0.764V * (R1+R2)/R2$ --> Skip Mode

<Variant Name>

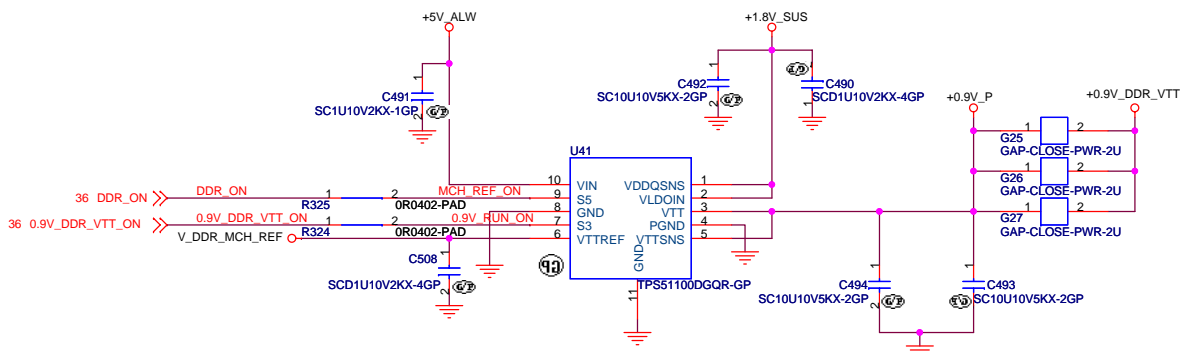
 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title Thurman Discrete		
Size A3	Document Number DCDC 1.5V/1.05V	Rev -1
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Design Current = 8.64A
 OCP design = 12.34A



$$V_{out} = 0.75V * (R1 + R2) / R2$$

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
 Inductor: 1.5UH M MPL73-1R5 Delta 9Arms 18Apeak / 68.1R510.10I
 O/P cap: 220U 4V 4TPE220MF 15mOhm 3.1Arms/ 77.22271.161
 H/S & L/S: FDS8884 SO-8/ 30mOhm/ 4.5Vgs/ 84.08884.037
 L/S: FDS8896 SO-8/ 7.3mOhm/ 4.5Vgs/ 84.08896.037
 Ton = 200KOhm --> 330KHz



<Variant Name>

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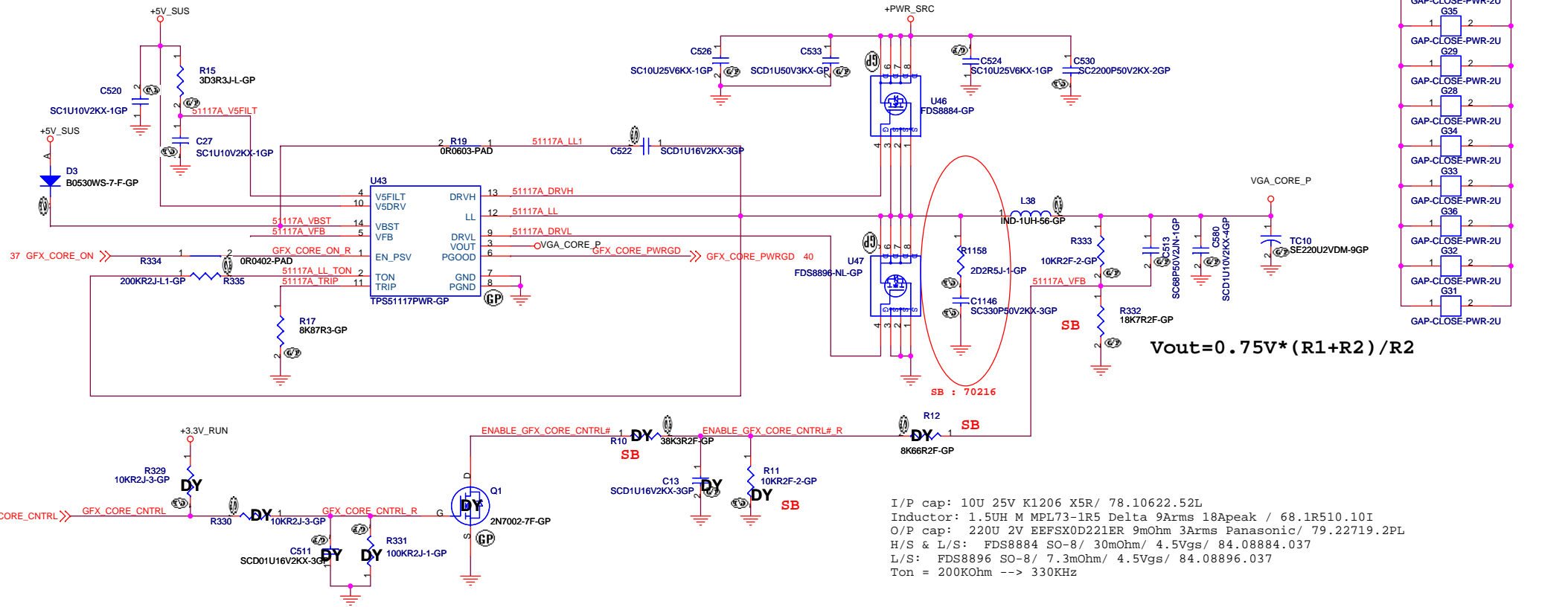
Title

Thurman Discrete

Size	Document Number	Rev
A3	DCDC 1.8V/0.9V	-1

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Design Current = 11A
 OCP design = 15A
 VGA_CORE = 1.0V

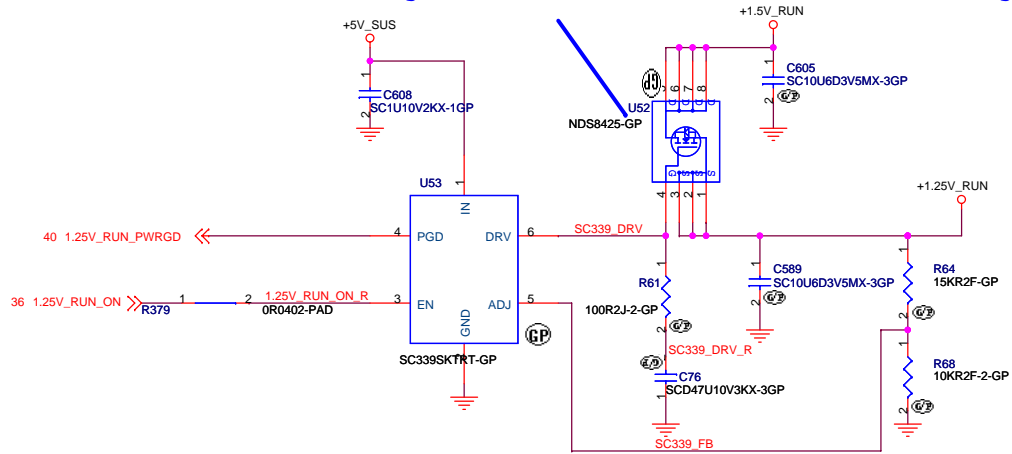


$$V_{out} = 0.75V * (R1 + R2) / R2$$


I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
 Inductor: 1.5UH M MPL73-1R5 Delta 9Arms 18Apeak / 68.1R510.10I
 O/P cap: 220U 2V EEF5X0D221ER 9mOhm 3Arms Panasonic/ 79.22719.2PL
 H/S & L/S: FDS8884 SO-8/ 30mOhm/ 4.5Vgs/ 84.08884.037
 L/S: FDS8896 SO-8/ 7.3mOhm/ 4.5Vgs/ 84.08896.037
 Ton = 200KOhm --> 330KHz

Will change to NDS8425. 28mOhm/@2.7V

Design Current = 3.0A



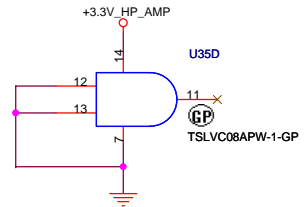
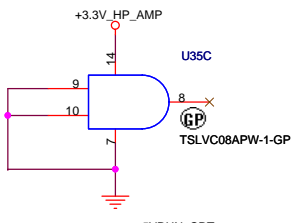
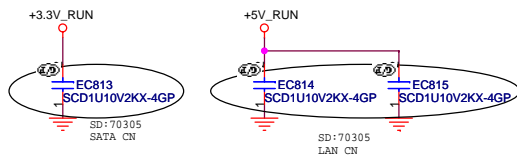
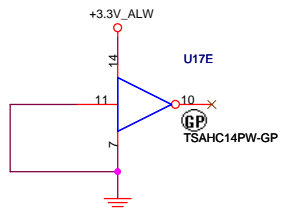
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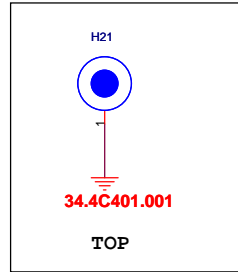
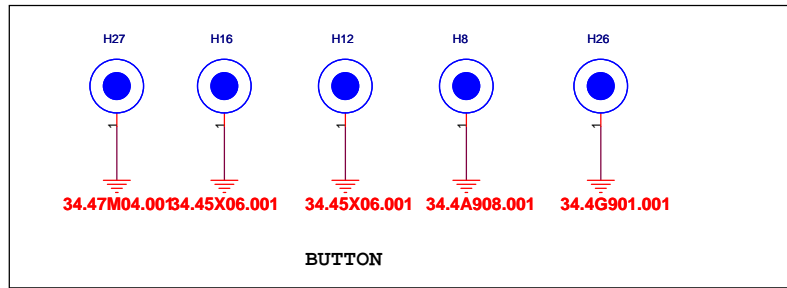
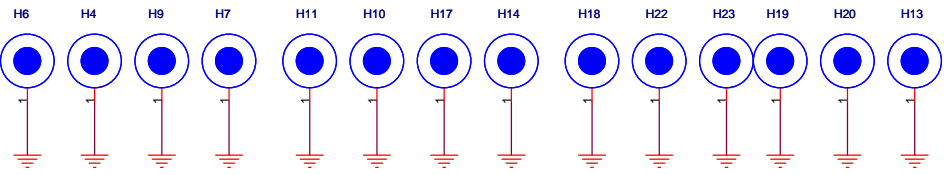
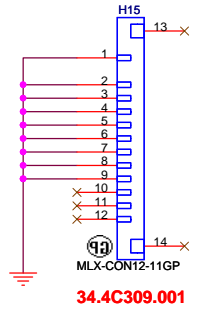
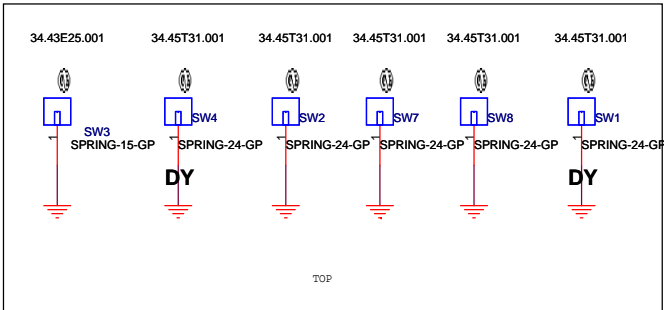
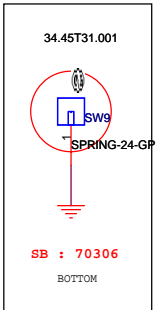
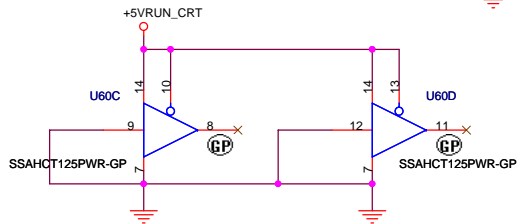
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Title: **Thurman Discrete**

Size: A3	Document Number: DCDC VGA_Core/1.25V	Rev: -1
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SW3 - 34.43E25.001
 SW9 - 34.49Q02.001
 SW5 - 34.34T31.001 (Only for UMA)
 others=34.45T31.001



<Variant Name>

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Title: **Thurman Discrete**

Size: A3	Document Number: EMI&MISC	Rev: -1
Date: Thursday, November 22, 2007	Sheet 49 of 50	

