

# Compal confidential

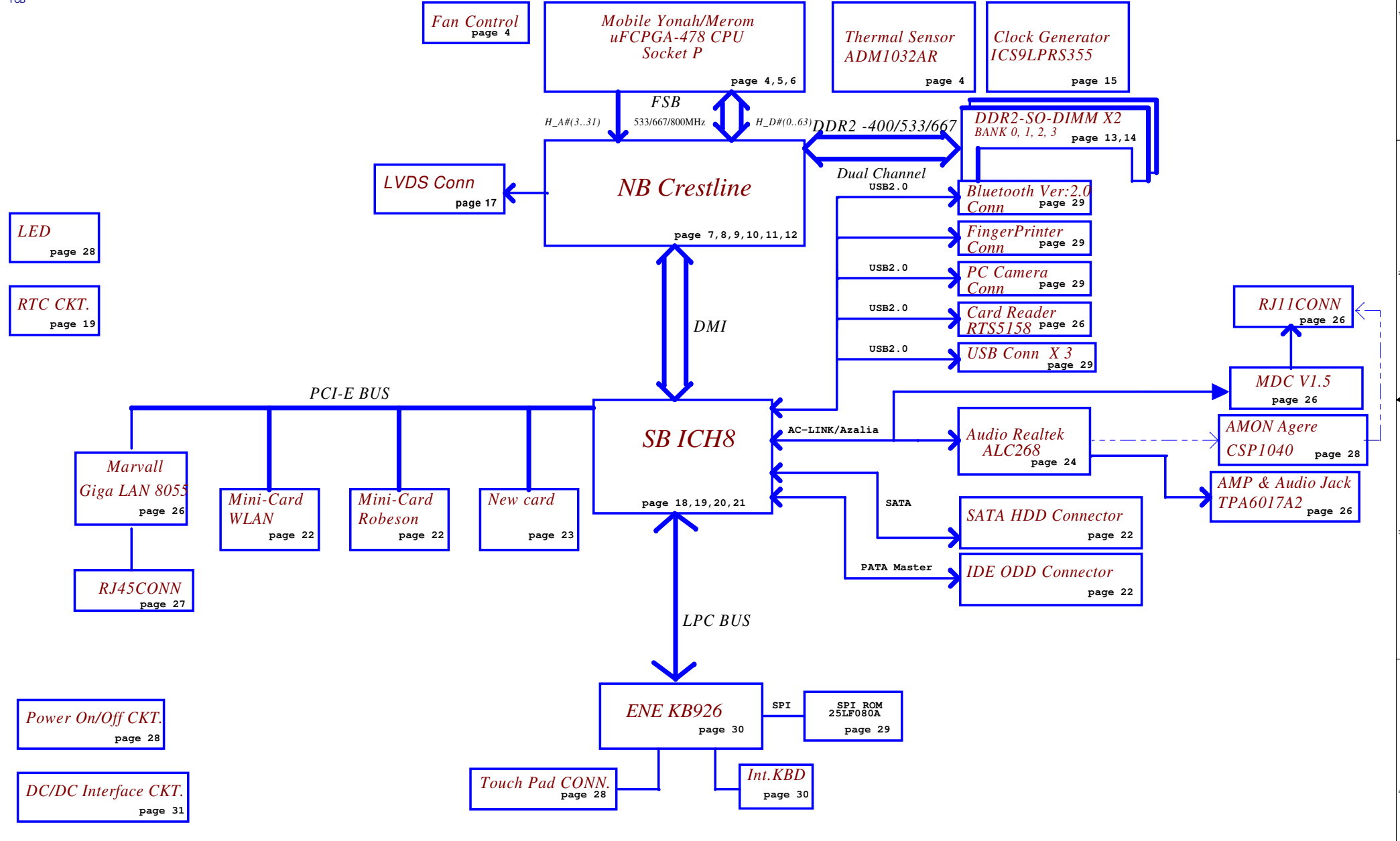
## Schematics Document

### Mobile Merom uFCPGA with Satna Rosa Platform

2007-07-24  
REV: 0.3

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# Supra 1.0 (Merom +Crestline+ICH8) 12"



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Compal Electronics, Inc.  
Block Diagram

## Voltage Rails

power plane State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +1.25VS +0.9V +VCCP +CPU_CORE
S0	○	○	○	○
S1	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

### Symbol Note :

 : means Digital Ground

 : means Analog Ground

@ : means just reserve , no build

DEBUG@ : means just reserve for debug.

## I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

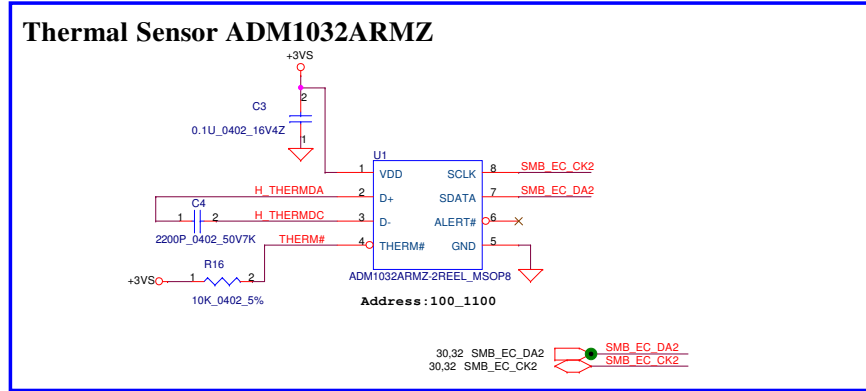
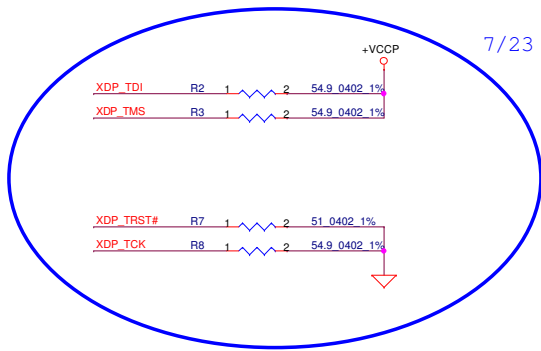
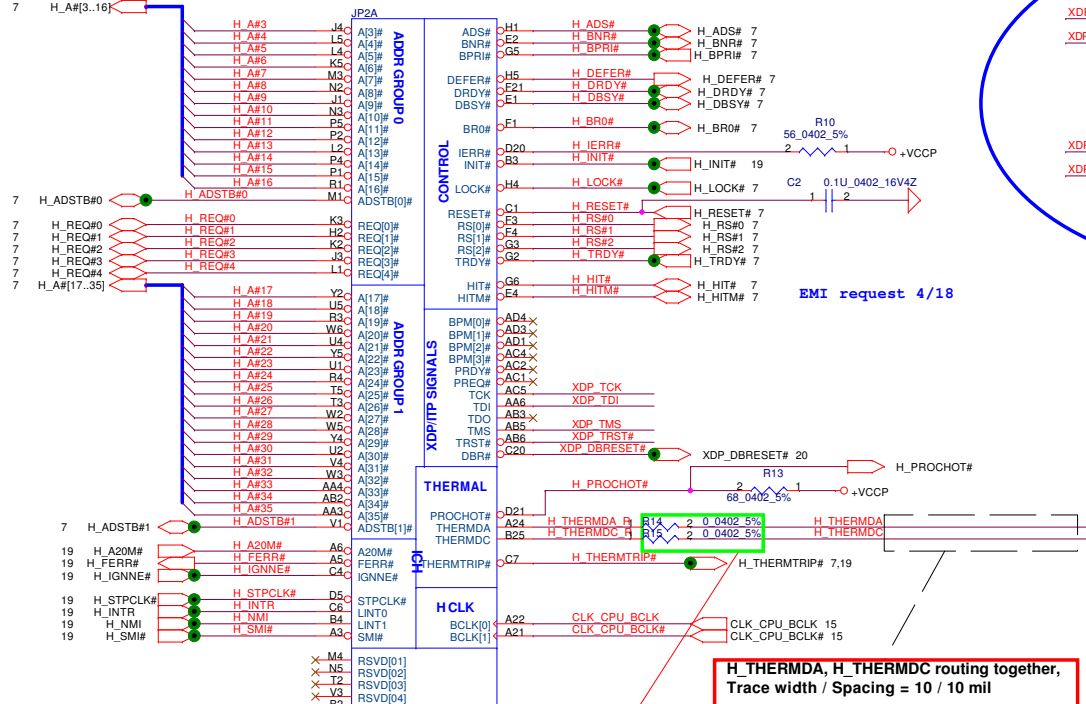
SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU) ADM1032	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CLK1 SMB_EC_DAT1	KB925	✗	✓	✓	✗	✗	✗	✗	✗
SMB_EC_CLK2 SMB_EC_DAT2	KB925	✗	✗	✗	✓	✗	✗	✗	✗
SMB_CLK_CLK1 SMB_CLK_DAT1	ICH8	✗	✗	✗	✗	✓	✓	✓	✗
LCD_CLK LCD_DAT	Crestline	✗	✗	✗	✗	✗	✗	✗	✓

**BOM: 43XXXXXX**

**Jump-Short: PJP?**

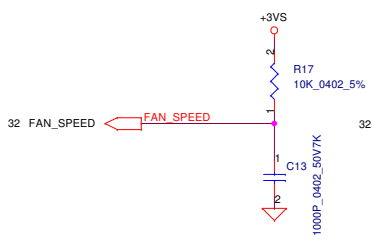
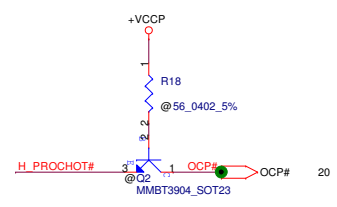
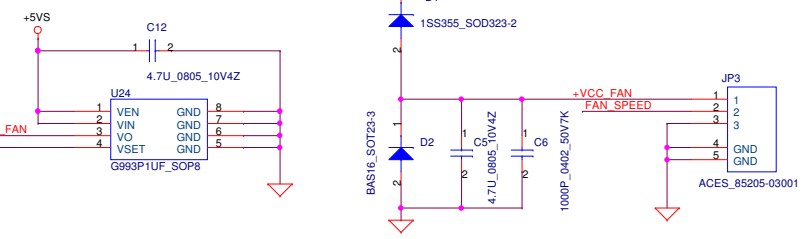
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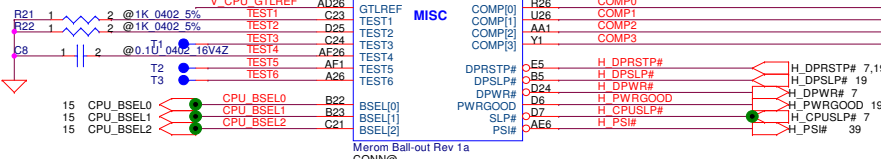
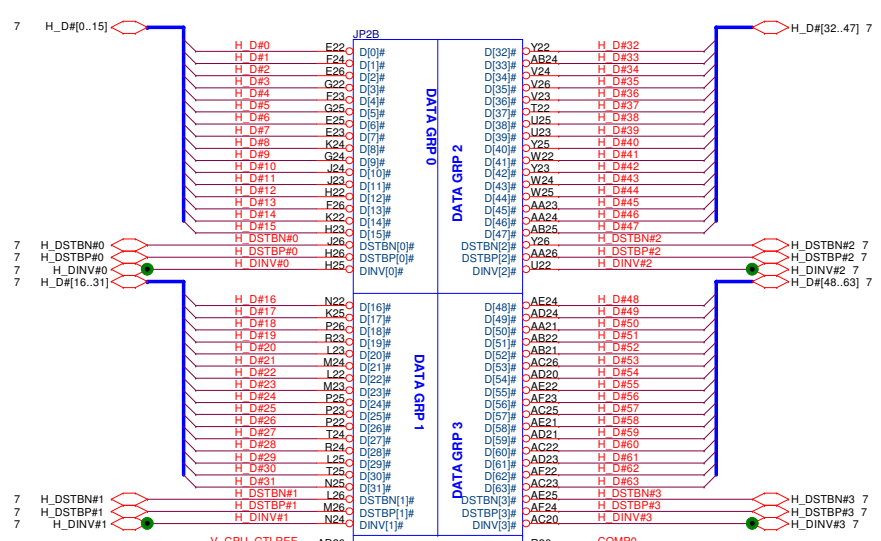
**H\_THERMDA, H\_THERMDC routing together, Trace width / Spacing = 10 / 10 mil**

For Merom, R14 and R15 are 0ohm  
For Penryn, R14 and R15 are 100ohm.

### Voltage Fan Control circuit

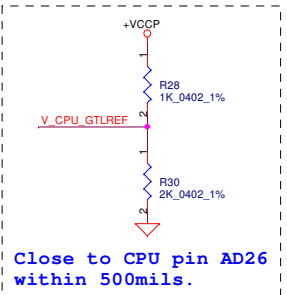


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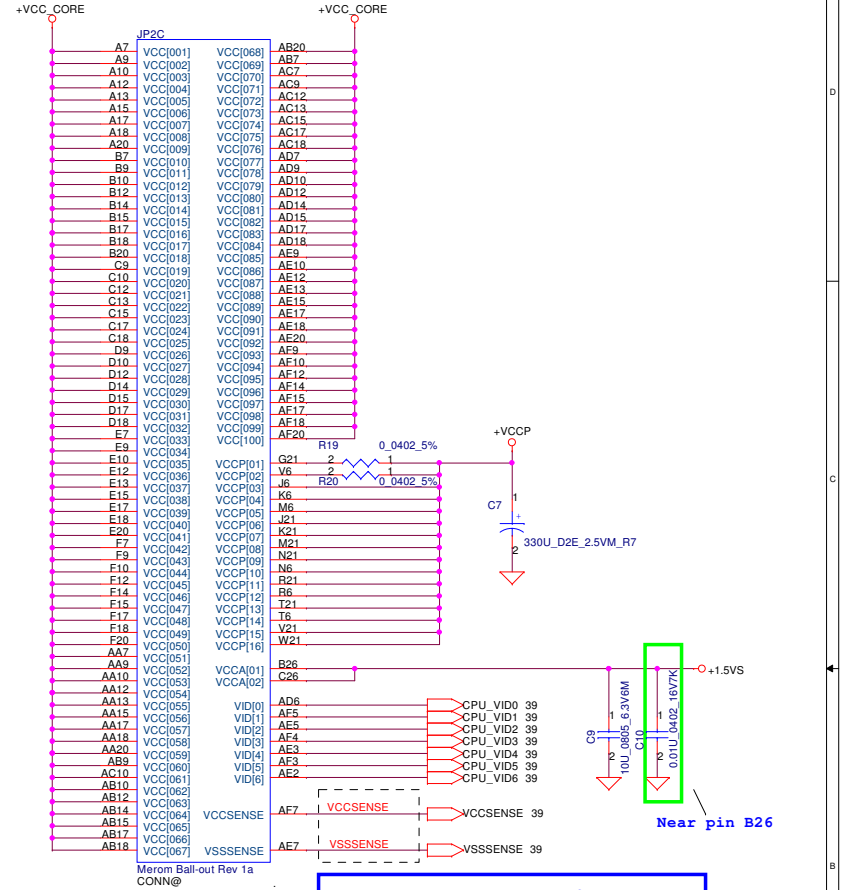
layout note: Route TEST3 & TEST5 trace to ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

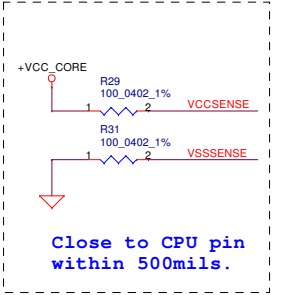


Close to CPU pin AD26 within 500mils.

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



Length match within 25 mils. The trace width/space/other is 20/7/25.

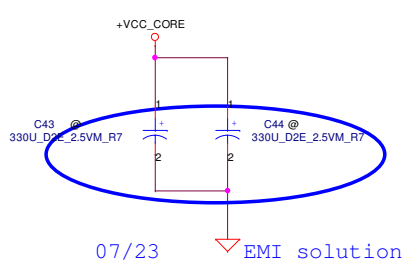


Close to CPU pin within 500mils.

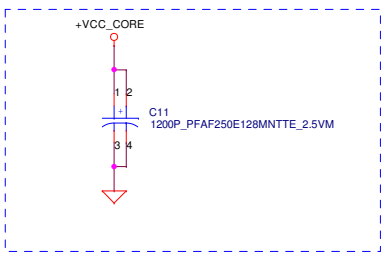
JP2D		
A4	VSS[001]	P6
A8	VSS[002]	P21
A11	VSS[003]	P24
A14	VSS[004]	R2
A16	VSS[005]	R5
A19	VSS[006]	R22
A22	VSS[007]	R25
AF2	VSS[008]	T1
AF2	VSS[008]	T1
B6	VSS[009]	T4
B8	VSS[010]	T23
B11	VSS[011]	T26
B12	VSS[012]	U3
B16	VSS[013]	U6
B19	VSS[014]	U21
B21	VSS[015]	U24
B24	VSS[016]	V2
C5	VSS[017]	V5
C8	VSS[018]	V22
C11	VSS[019]	V25
C14	VSS[020]	W1
C16	VSS[021]	W4
C19	VSS[022]	W23
C2	VSS[023]	W26
C22	VSS[024]	Y3
C25	VSS[025]	Y6
D1	VSS[026]	Y21
D4	VSS[027]	Y24
D8	VSS[028]	AA2
D11	VSS[029]	AA5
D13	VSS[030]	AA11
D16	VSS[031]	AA12
D19	VSS[032]	AA14
D22	VSS[033]	AA16
D26	VSS[034]	AA19
E3	VSS[035]	AA22
E6	VSS[036]	AA25
E8	VSS[037]	AB1
E11	VSS[038]	AB4
E14	VSS[039]	AB8
E16	VSS[040]	AB11
E19	VSS[041]	AB13
E21	VSS[042]	AB16
E24	VSS[043]	AB19
F5	VSS[044]	AB23
F8	VSS[045]	AB26
F11	VSS[046]	AC3
F13	VSS[047]	AC6
F16	VSS[048]	AC8
F19	VSS[049]	AC11
F2	VSS[050]	AC14
F22	VSS[051]	AC16
F25	VSS[052]	AC19
G4	VSS[053]	AC21
G1	VSS[054]	AC24
G23	VSS[055]	AD2
G26	VSS[056]	AD5
H3	VSS[057]	AD8
H6	VSS[058]	AD11
H21	VSS[059]	AD13
H24	VSS[060]	AD16
J2	VSS[061]	AD19
J5	VSS[062]	AD22
J22	VSS[063]	AD25
J25	VSS[064]	AE1
K1	VSS[065]	AE4
K4	VSS[066]	AE8
K23	VSS[067]	AE11
K26	VSS[068]	AE14
L3	VSS[069]	AE16
L6	VSS[070]	AE19
L21	VSS[071]	AE23
L24	VSS[072]	AE26
M2	VSS[073]	A2
M5	VSS[074]	AF6
M22	VSS[075]	AF8
M25	VSS[076]	AF11
N1	VSS[077]	AF13
N4	VSS[078]	AF16
N22	VSS[079]	AF19
N26	VSS[080]	AF21
P3	VSS[081]	A25
		AF25

Merom Ball-out Rev 1a

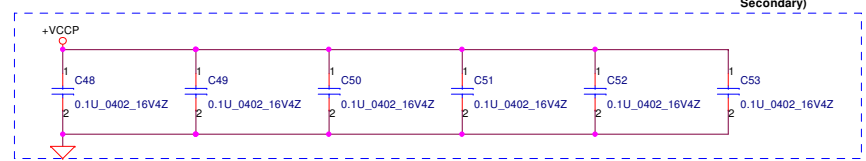
Near CPU CORE regulator



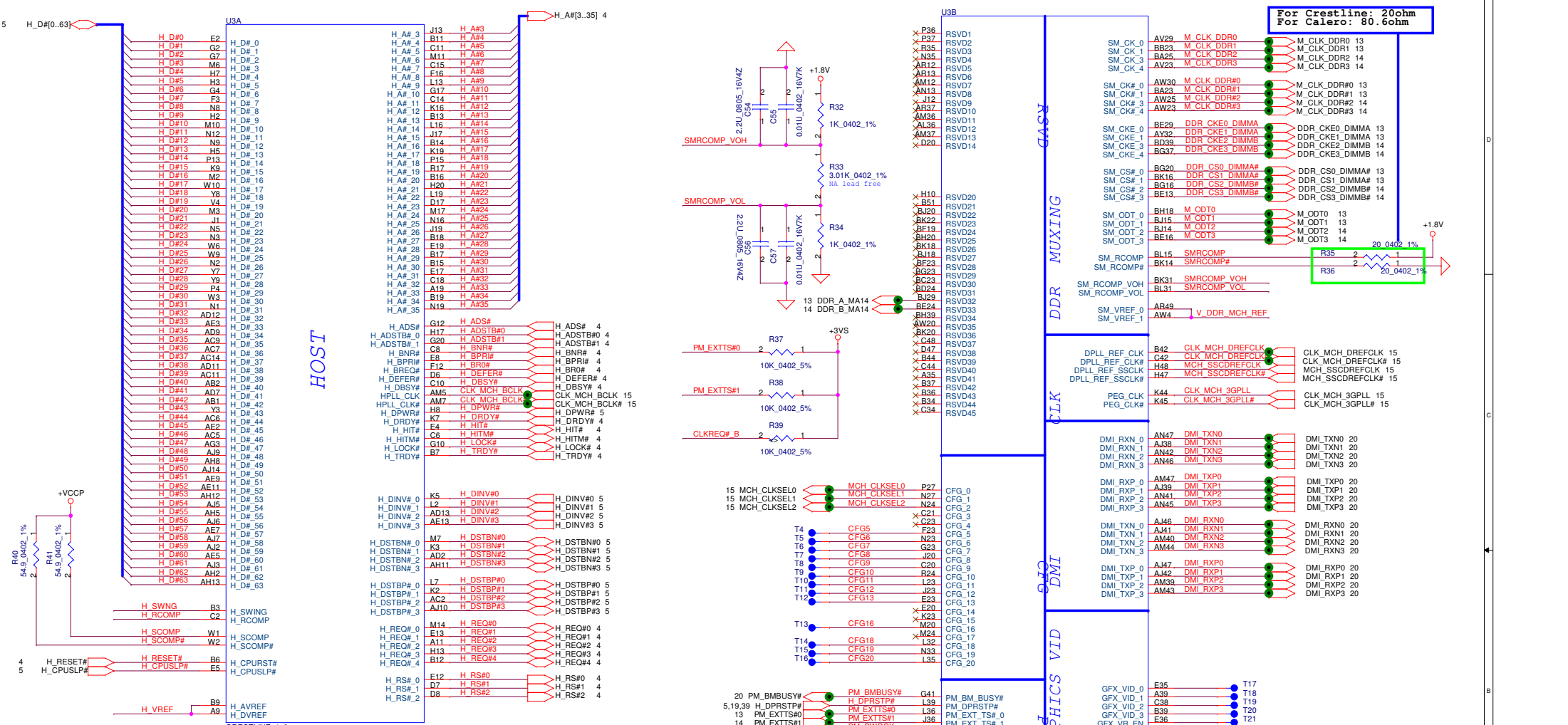
Proadlizer



Place these inside socket cavity on L8 (North side Secondary)



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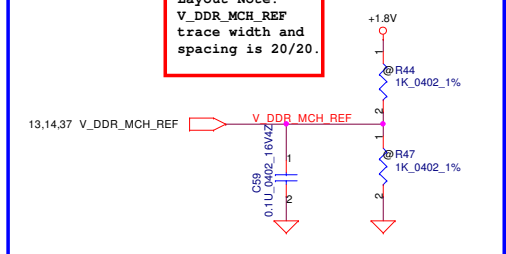
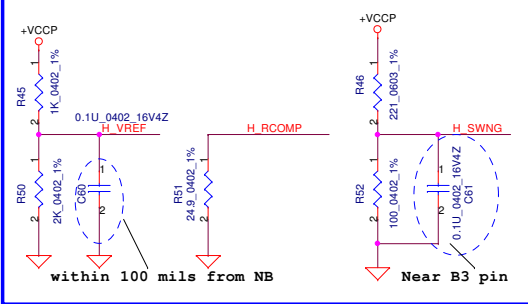


For Crestline: 20ohm  
For Calero: 80.6ohm

**layout note:**  
Route H\_SCOMP and H\_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces

**Layout Note:**  
H\_RCOMP / H\_VREF / H\_SWNG  
trace width and spacing is 10/20

**Layout Note:**  
V\_DDR\_MCH\_REF  
trace width and spacing is 20/20.

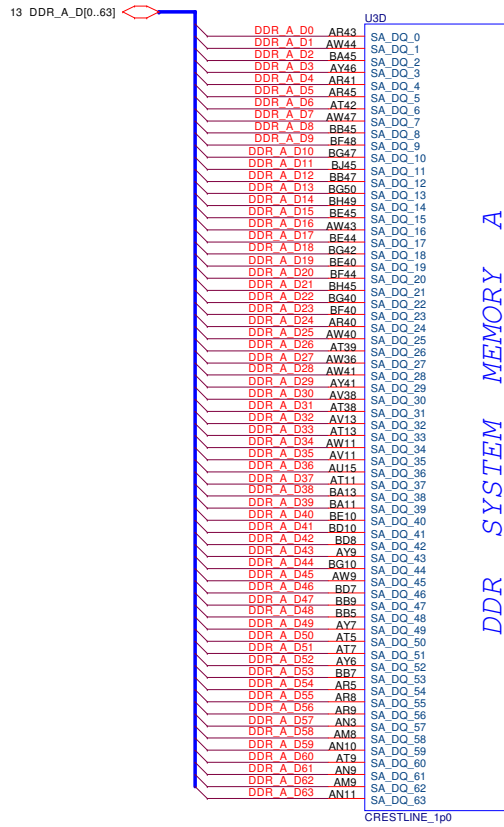


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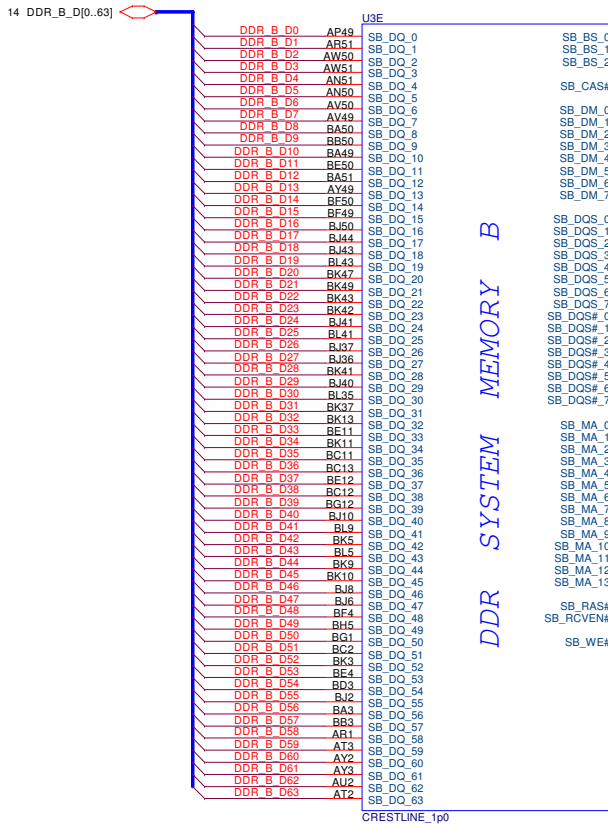
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DDR SYSTEM MEMORY A

CRESTLINE\_1p0



DDR SYSTEM MEMORY B

CRESTLINE\_1p0

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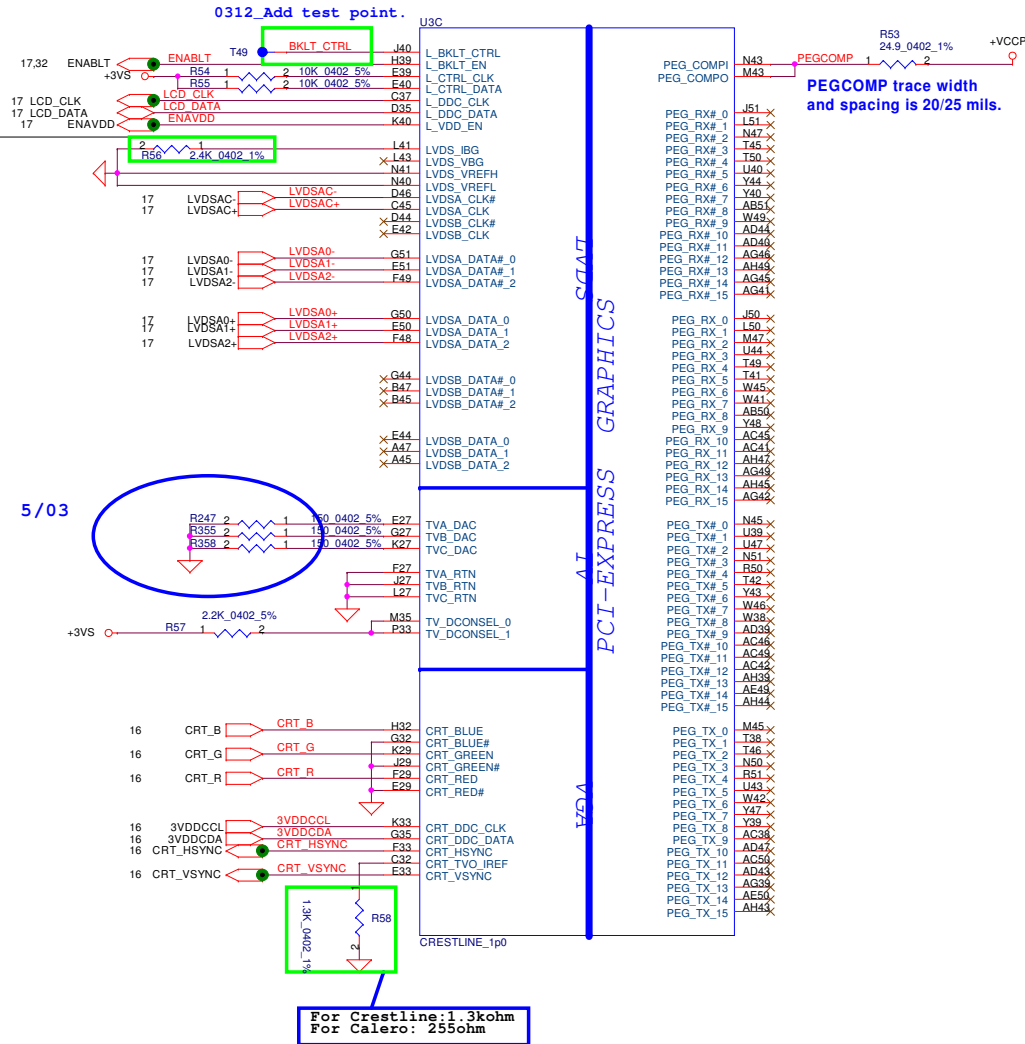


## Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu.

CFG[17:3] have internal pull up  
CFG[19:18] have internal pull down

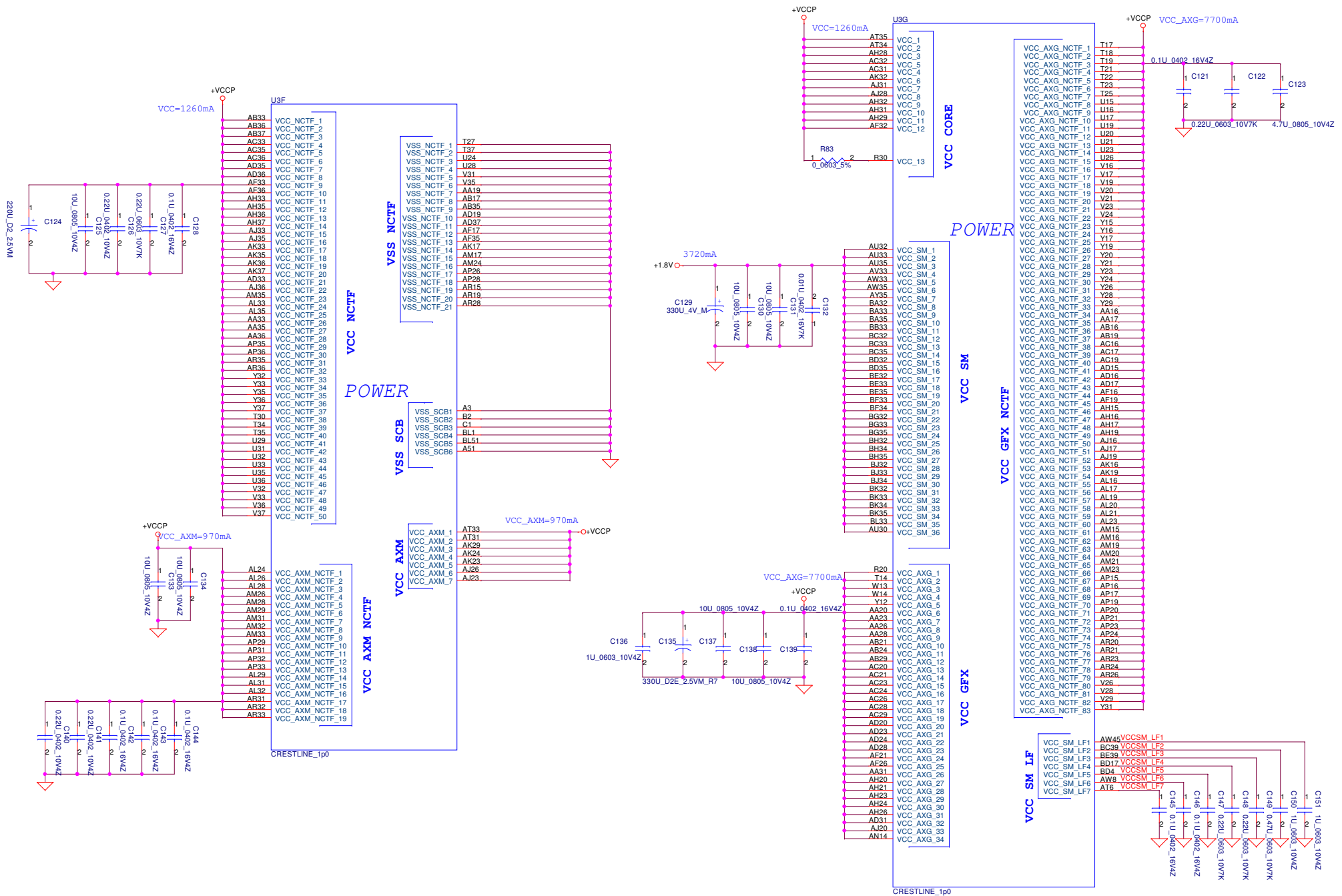
For Crestline: 2.4kohm  
For Calero: 1.5kohm



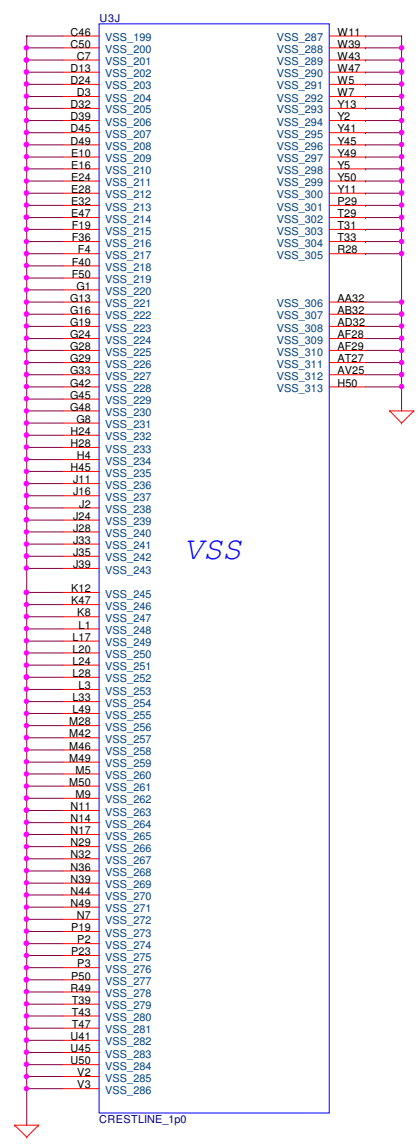
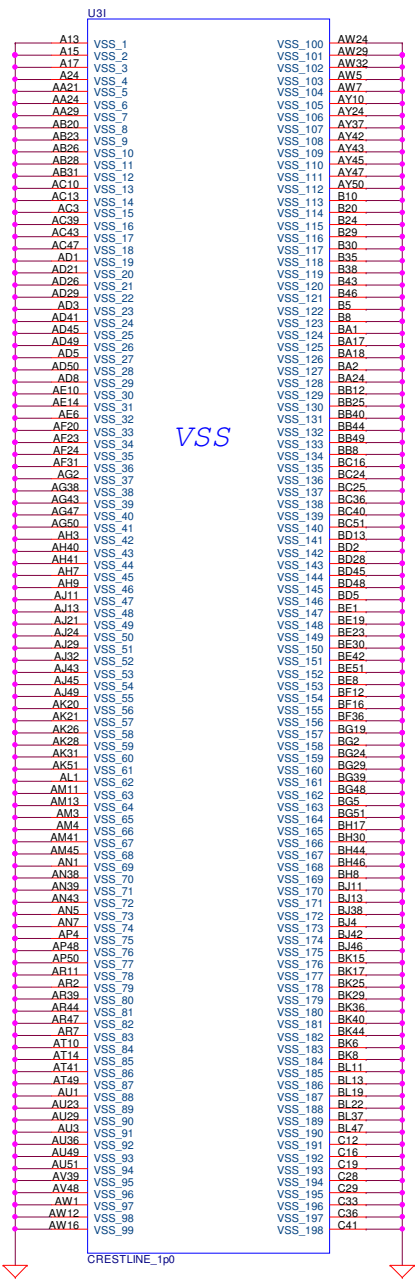
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<b>CRESTLINE((3/6)-VGA/LVDS/TV</b>		
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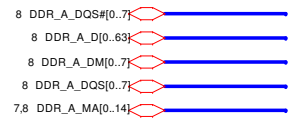




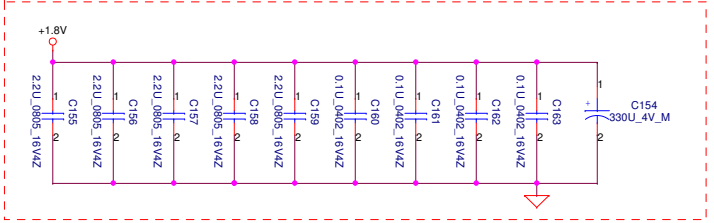
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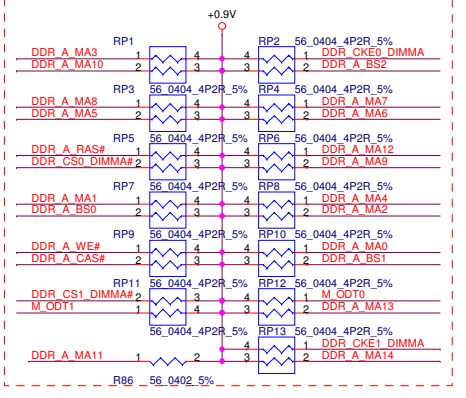
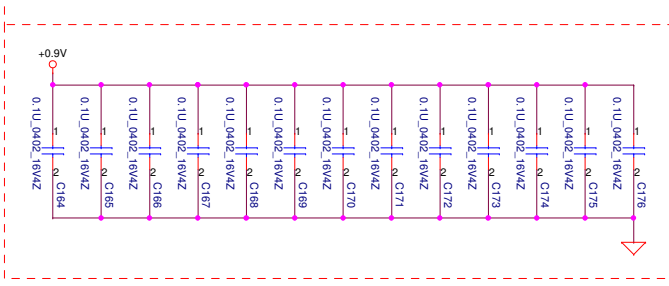
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**Layout Note:**  
Place near JP34



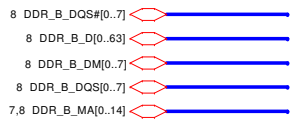
**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9VS



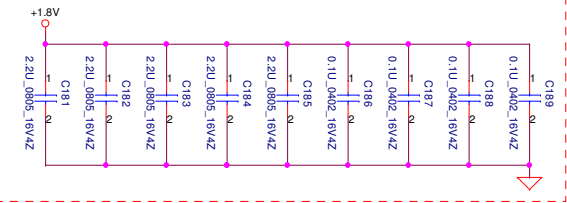
**Layout Note:**  
Place these resistor closely JP34, all trace length Max=1.5"



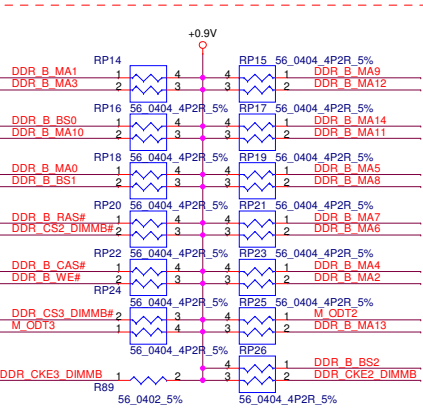
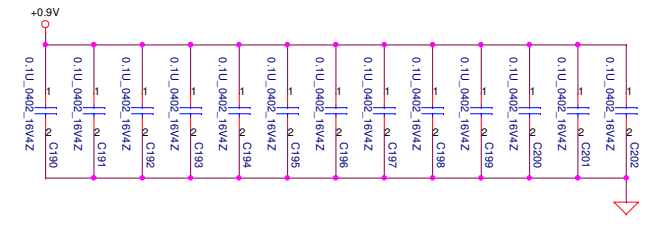
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				<b>DDR2-SODIMM SLOT1</b>
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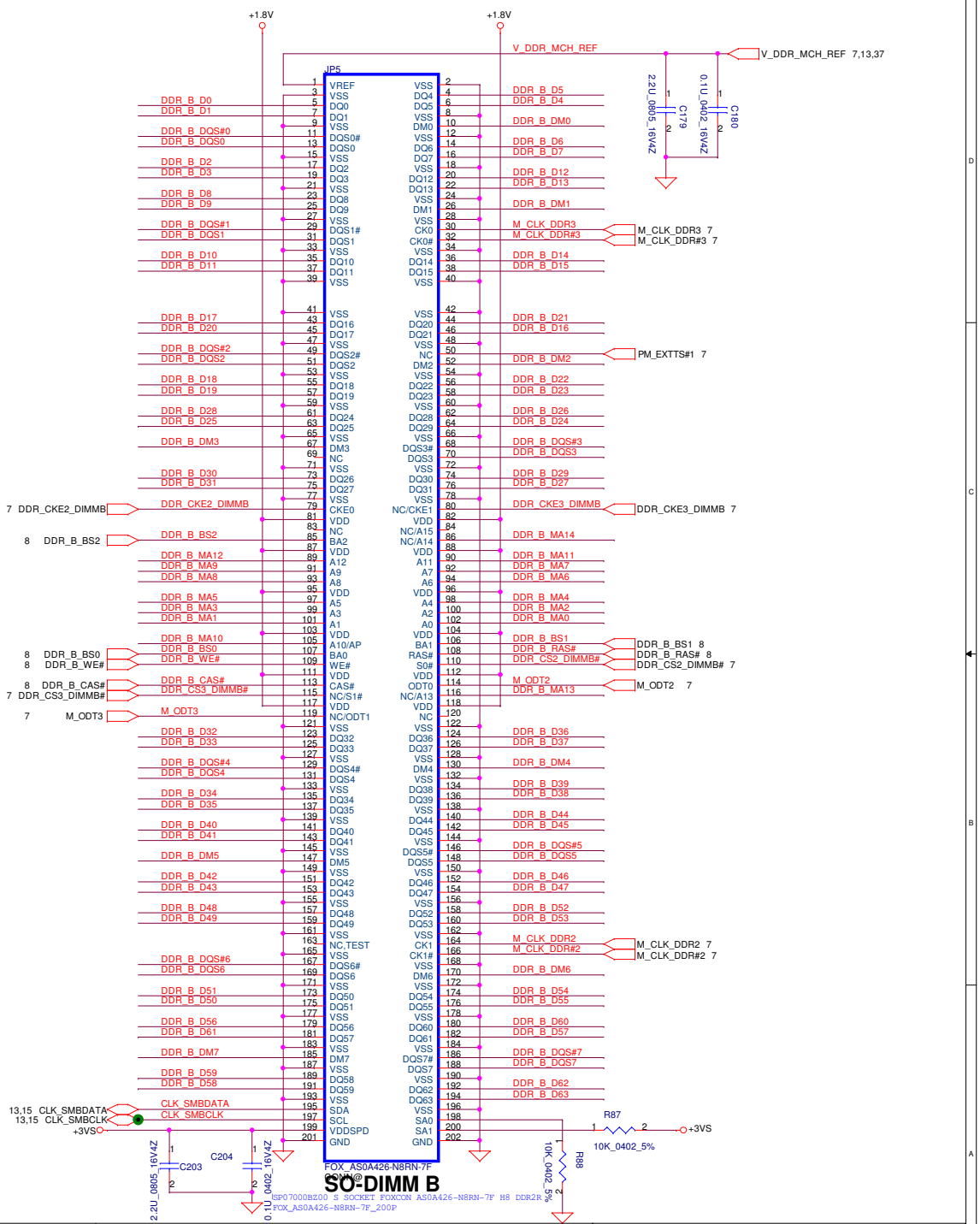
**Layout Note:**  
Place near JP10



**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9VS



**Layout Note:**  
Place these resistor closely JP10, all trace length Max=1.5"

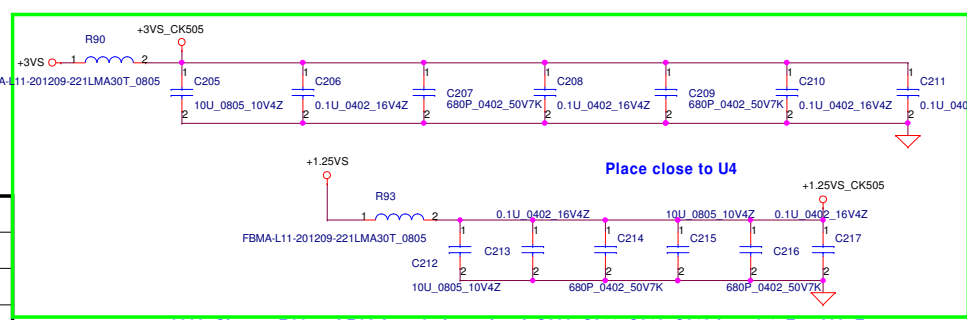


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Issued Date	2006/02/13	Deciphered Date	2006/03/10	Compal Electronics, Inc.	
				DDRII-SODIMM SLOT2	
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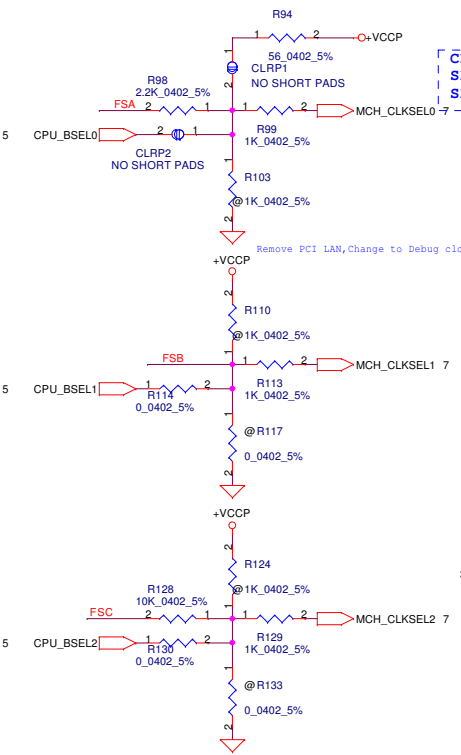
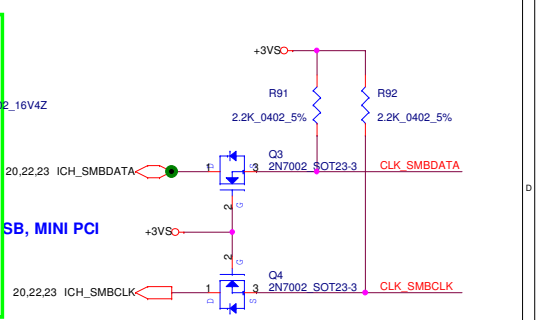
FSLC	FSLB	FSLA	CPU	SRC	PCI
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz
0	0	1	133	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3

**FSB Frequency Set:**

CPU Driven	Stuff	R1107	R1135	R1083
*(Default)	No Stuff	R1074	R1086	R1098
	Stuff	R1074	R1086	R1098
667MHz	No Stuff	R1083	R1107	R1128
	Stuff	R1083	R1107	R1128
800MHz	No Stuff	R1083	R1086	R1098
	Stuff	R1083	R1086	R1098



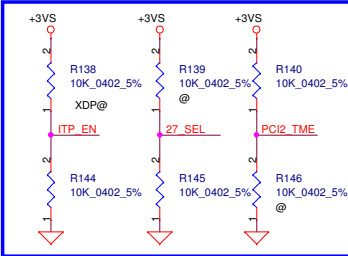
0308\_Change R89 and R92 form 0 ohm to bead, C209, C211, C216, C218 from 0.1uF to 680pF.



CLRP4, CLRP5 for 667/800 FSB select  
SHORT CLRP5, NO SHORT CLRP4 -- CPU option  
SHORT CLRP4, NO SHORT CLRP5 -- FSB 667

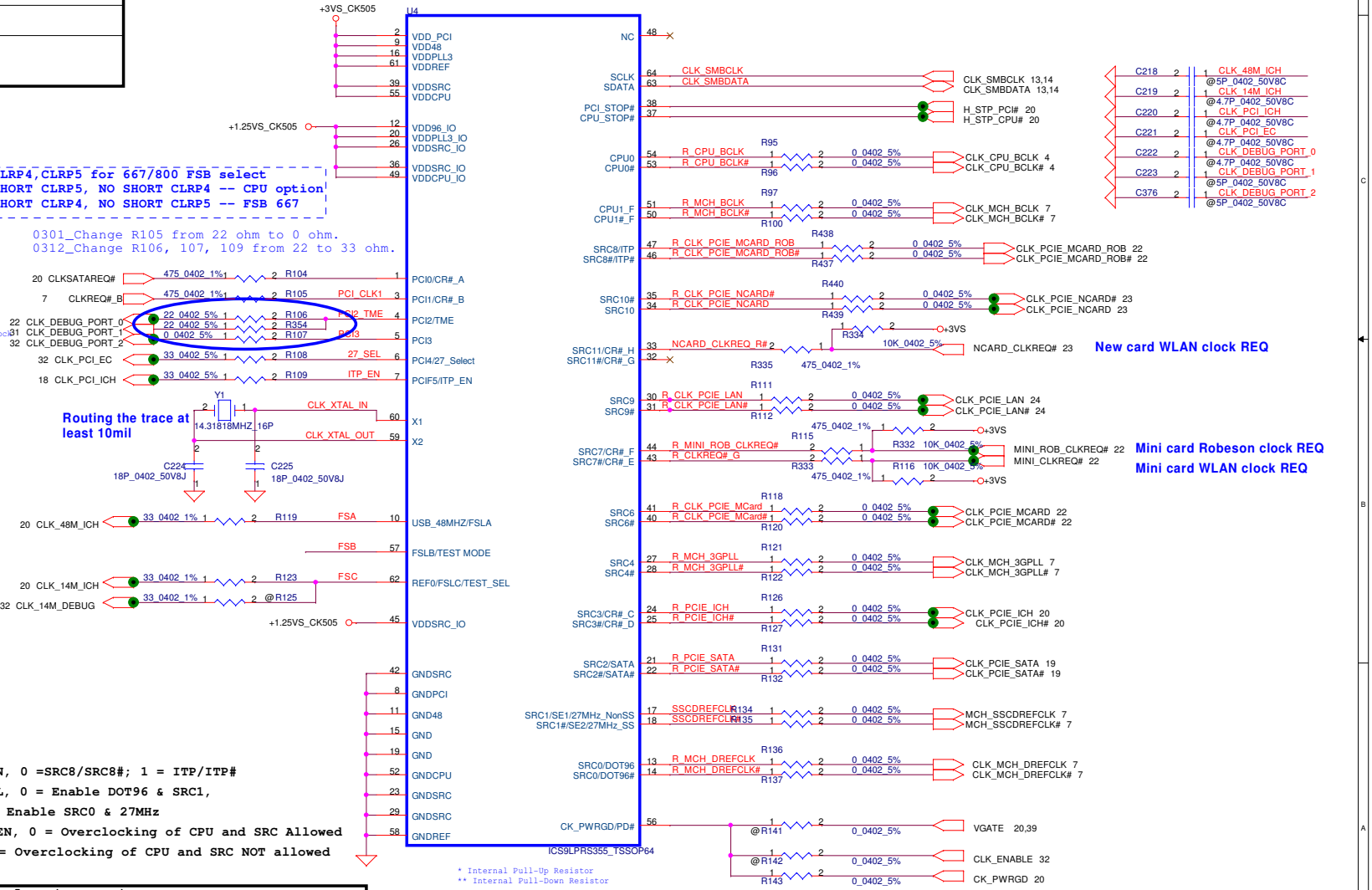
0301\_Change R105 from 22 ohm to 0 ohm.  
0312\_Change R106, 107, 109 from 22 to 33 ohm.

Routing the trace at least 10mil



For ITP\_EN, 0 = SRC8/SRC8#; 1 = ITP/ITP#  
For 27\_SEL, 0 = Enable DOT96 & SRC1,  
1 = Enable SRC0 & 27MHz  
For PCI2\_EN, 0 = Overclocking of CPU and SRC Allowed  
1 = Overclocking of CPU and SRC NOT allowed

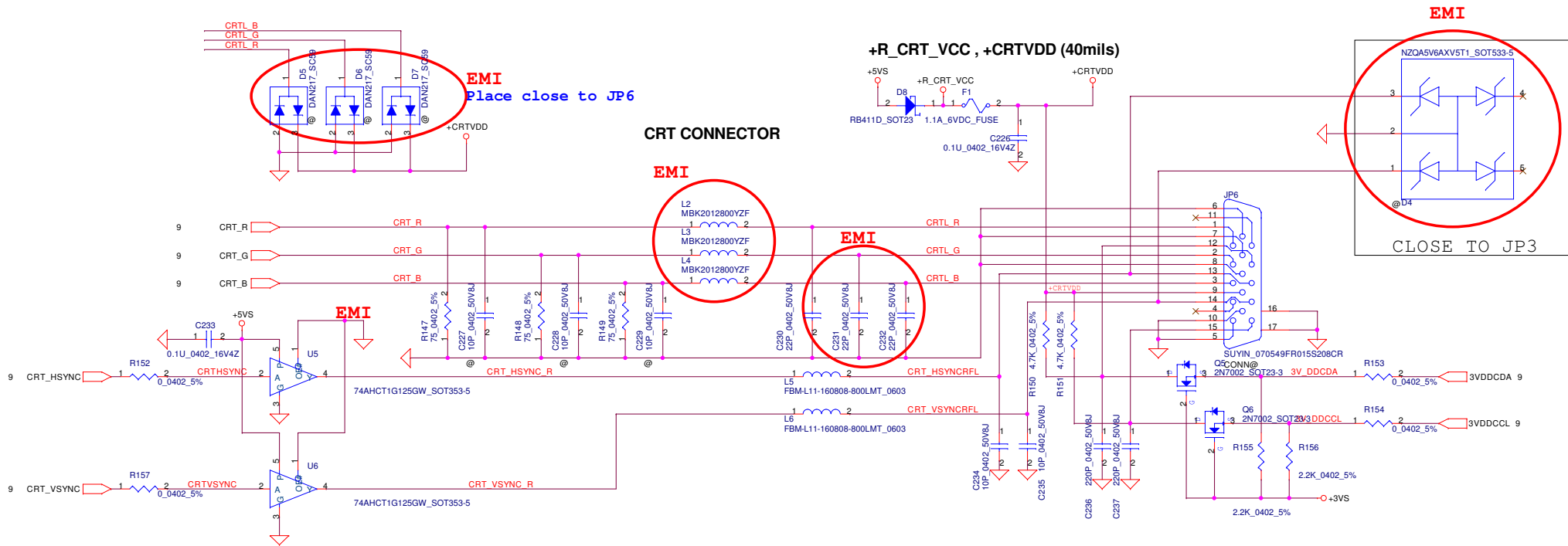
For Layout request:  
1. Change MINI\_CLKREQ# from pin 32 to pin 43.  
2. Change CLK\_PCIE\_MCARD from SRC9 to SRC6.



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Title		Rev	
Clock generator		0.3	
Size	Document Number	LA-3821P	
Date	Tuesday, July 31, 2007	Sheet	15 of 43

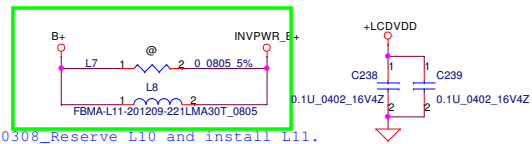


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Issued Date	2006/02/13	Deciphered Date	2006/07/26
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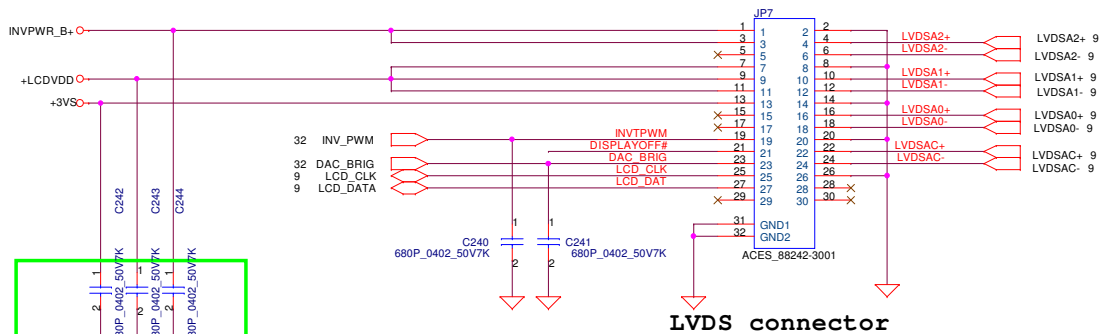
Title			<b>Compal Electronics, Inc.</b>	
Size			<b>CRT &amp; TVout Connector</b>	
Document Number			LA-3821P	
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# LVDS CONN

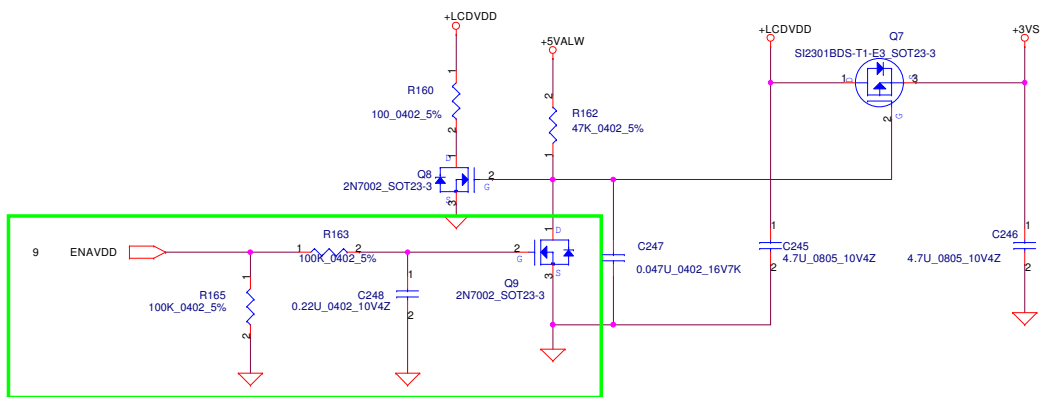
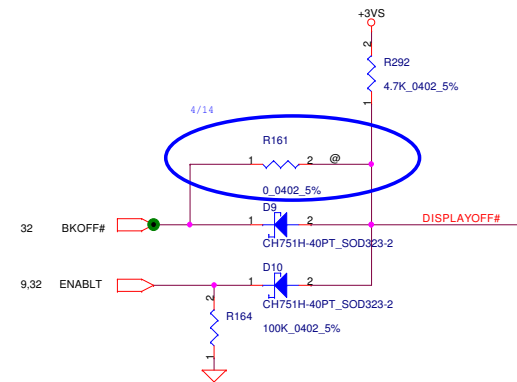
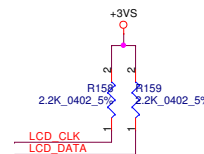


0308\_Reserve L10 and install L11.



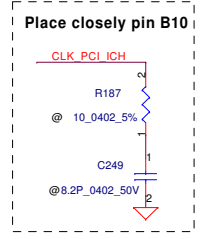
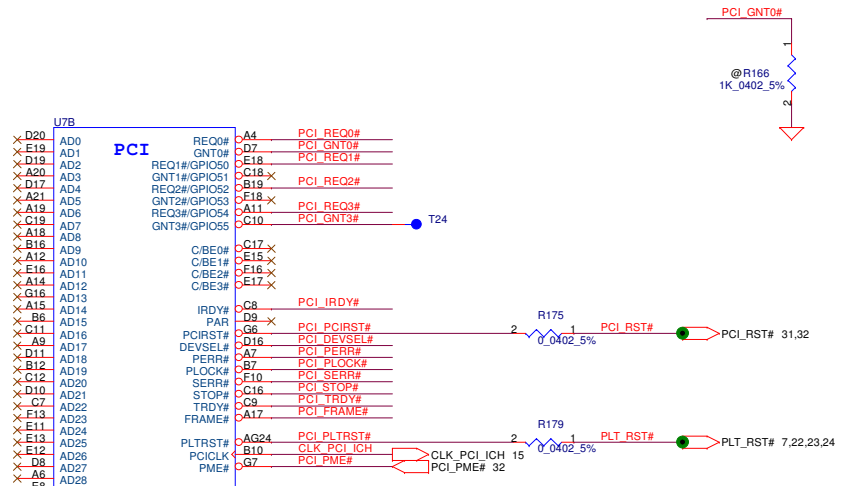
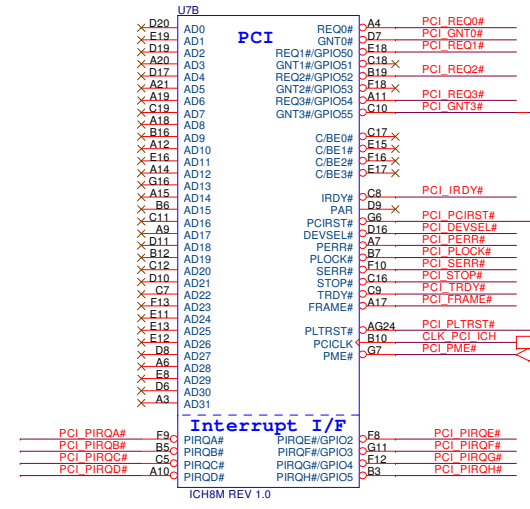
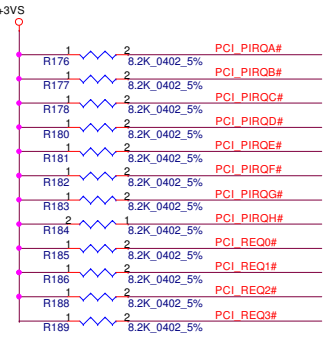
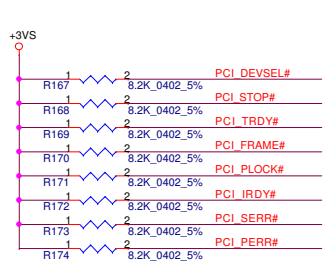
LVDS connector

0308\_Install all cap for EMI request.



Avoid Panel display garbage after power on.

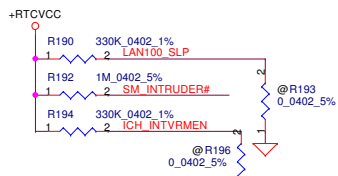
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Issued Date	2006/02/13	Deciphered Date	2006/07/26	Compal Electronics, Inc.		
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Size	Document Number	Rev		Date		
	LA-3821P	0.3		Tuesday, July 31, 2007		
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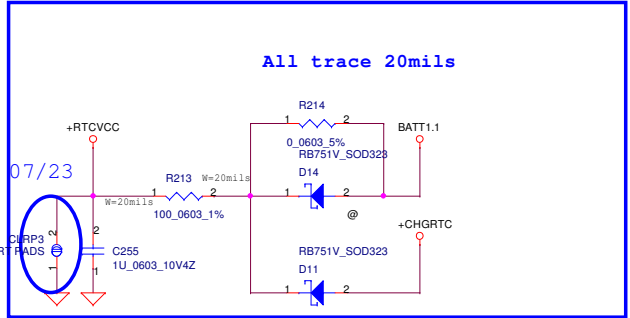
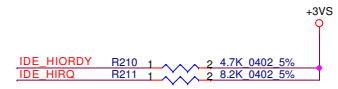
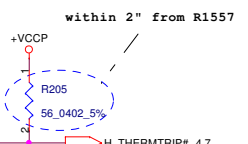
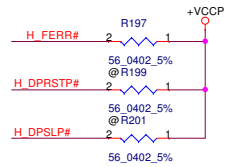
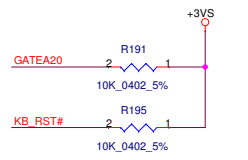
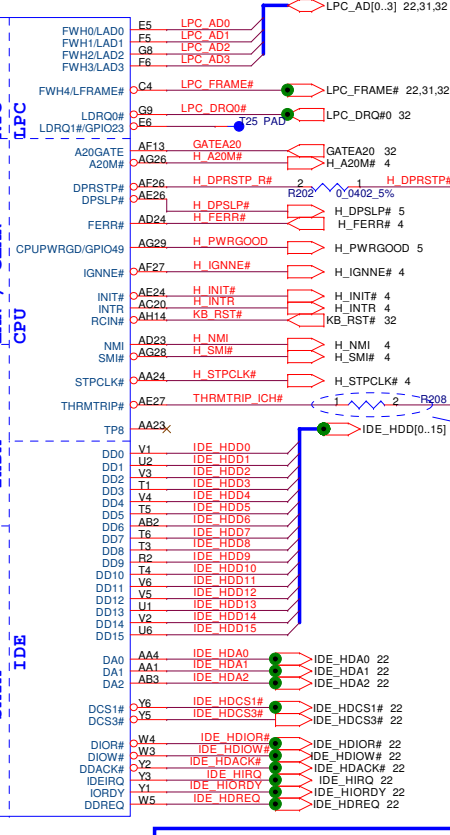
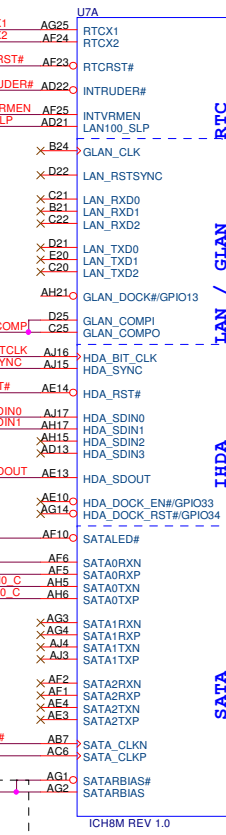
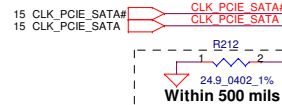
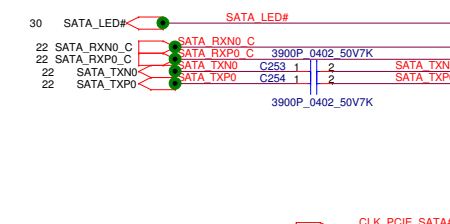
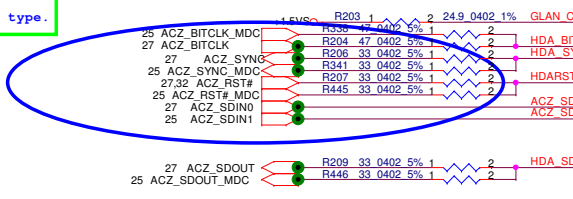
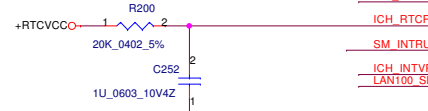
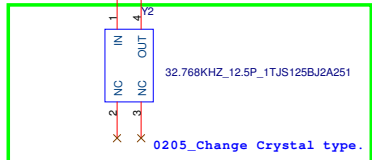
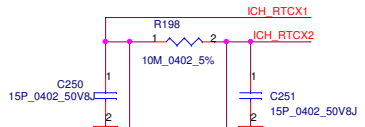
Boot BIOS Strap		
PCI_GNT0#	SPL_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *

A16 swap override Strap	
PCI_GNT3#	*Low= A16 swap override Enable High= Default



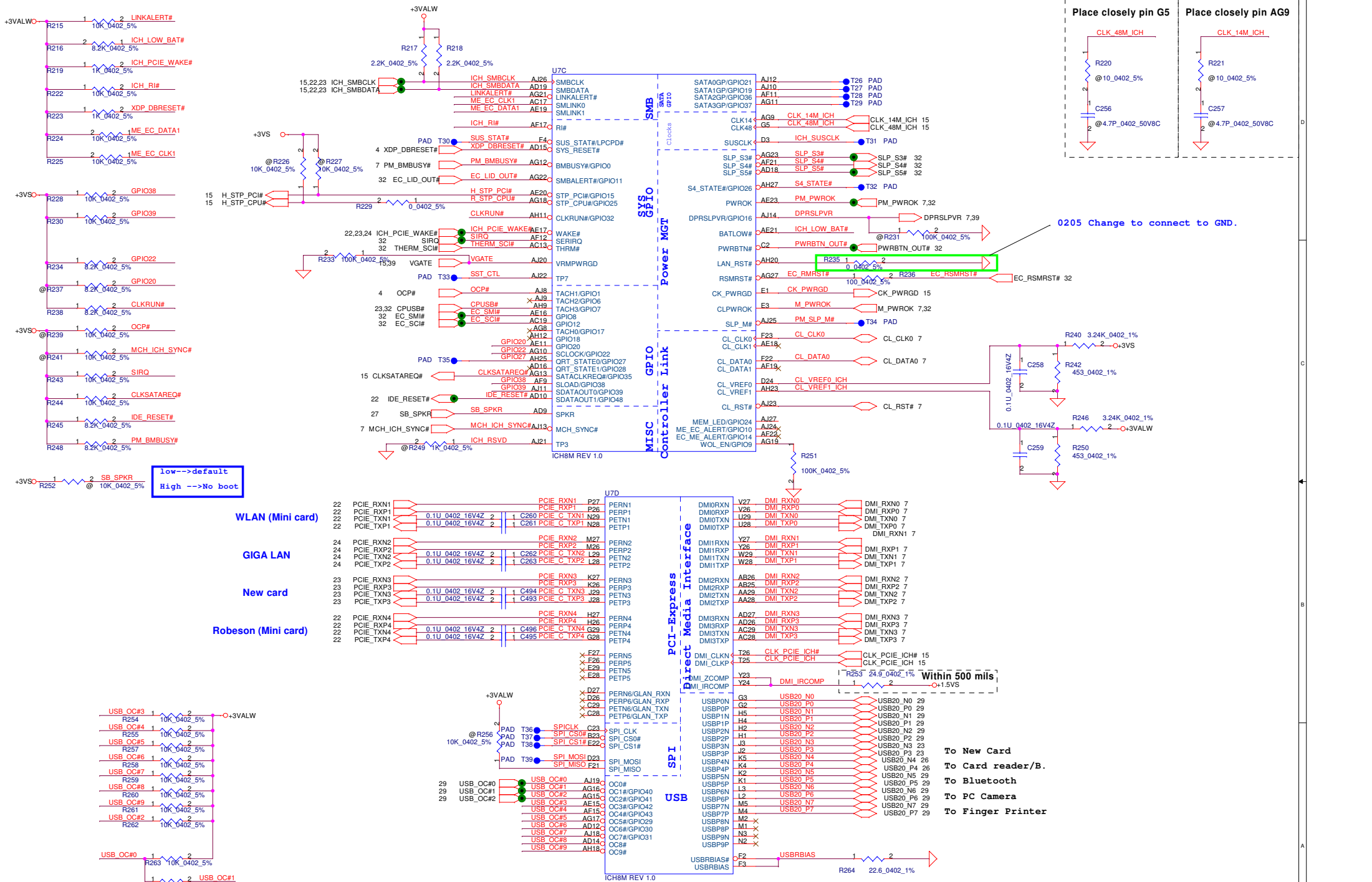
ICH8M Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)
ICH8M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)	
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)



0420\_Change RTC battery to power part

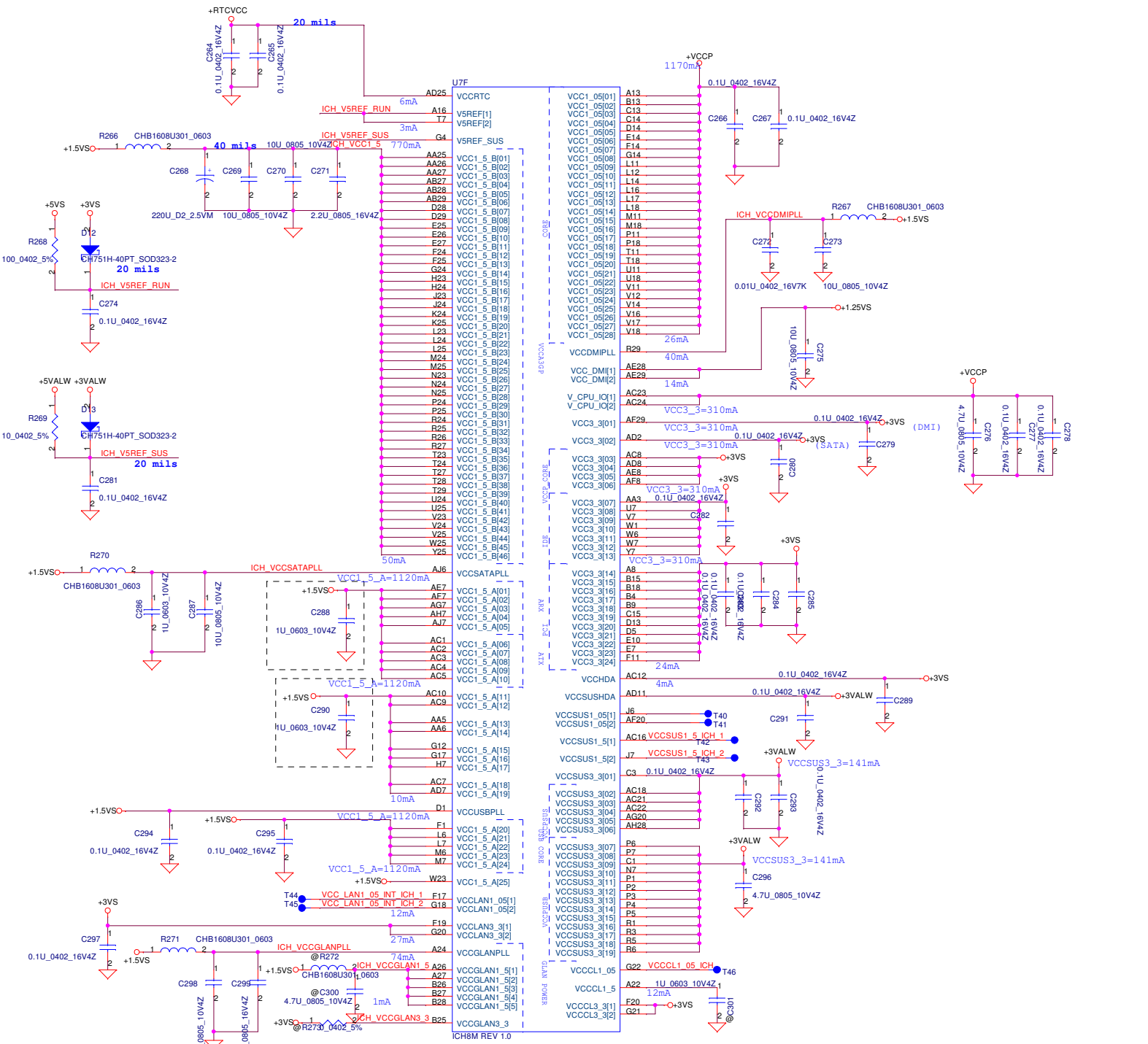
All trace 20mils

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<b>Compal Electronics, Inc.</b>		
<b>ICH8(3/4) PM,USB,GPIO</b>		
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UTE

A23	VSS1001	VSS1099	K7
A5	VSS1002	VSS1100	L1
AA2	VSS1003	VSS1101	L13
AA7	VSS1004	VSS1102	L15
AB5	VSS1005	VSS1103	L26
AB1	VSS1006	VSS1104	L27
AB24	VSS1007	VSS1105	L4
AC11	VSS1008	VSS1106	L5
AC14	VSS1009	VSS1107	L13
AC25	VSS1010	VSS1108	L14
AC26	VSS1011	VSS1109	L14
AC27	VSS1012	VSS1110	L15
AD17	VSS1013	VSS1111	L17
AD20	VSS1014	VSS1112	M23
AD28	VSS1015	VSS1113	M2
AD29	VSS1016	VSS1114	M28
AD3	VSS1017	VSS1115	M29
AD4	VSS1018	VSS1116	M3
AD6	VSS1019	VSS1117	N1
AE1	VSS1020	VSS1118	N11
AE12	VSS1021	VSS1119	N12
AE2	VSS1022	VSS1120	N13
AE22	VSS1023	VSS1121	N14
AE3	VSS1024	VSS1122	N15
AE5	VSS1025	VSS1123	N16
AE6	VSS1026	VSS1124	N16
AE9	VSS1027	VSS1125	N17
AF14	VSS1028	VSS1126	N18
AF16	VSS1029	VSS1127	N26
AF18	VSS1030	VSS1128	N27
AF3	VSS1031	VSS1129	N5
AF4	VSS1032	VSS1130	N6
AG5	VSS1033	VSS1131	P12
AG6	VSS1034	VSS1132	P13
AH10	VSS1035	VSS1133	P14
AH3	VSS1036	VSS1134	P15
AH3	VSS1037	VSS1135	P16
AH16	VSS1038	VSS1136	P17
AH19	VSS1039	VSS1137	P23
AH2	VSS1040	VSS1138	P28
AF28	VSS1041	VSS1139	P29
AH22	VSS1042	VSS1140	R11
AH24	VSS1043	VSS1141	R12
AH26	VSS1044	VSS1142	R13
AH3	VSS1045	VSS1143	R14
AH4	VSS1046	VSS1144	R15
AH8	VSS1047	VSS1145	R16
AJ5	VSS1048	VSS1146	R17
B11	VSS1049	VSS1147	R18
B14	VSS1050	VSS1148	R28
B17	VSS1051	VSS1149	T12
B20	VSS1052	VSS1150	T15
B22	VSS1053	VSS1151	T13
B2	VSS1054	VSS1152	T14
C24	VSS1055	VSS1153	T16
C26	VSS1056	VSS1154	T16
C27	VSS1057	VSS1155	T17
C6	VSS1058	VSS1156	T2
D12	VSS1059	VSS1157	U13
D15	VSS1060	VSS1158	U14
D18	VSS1061	VSS1159	U15
D4	VSS1062	VSS1160	U16
D2	VSS1063	VSS1161	U17
E21	VSS1064	VSS1162	U23
E24	VSS1065	VSS1163	U26
E4	VSS1066	VSS1164	U27
E9	VSS1067	VSS1165	U2
F15	VSS1068	VSS1166	U5
E23	VSS1069	VSS1167	U13
F28	VSS1070	VSS1168	U15
F29	VSS1071	VSS1169	U28
F7	VSS1072	VSS1170	V29
G1	VSS1073	VSS1171	W2
E2	VSS1074	VSS1172	W26
G10	VSS1075	VSS1173	W27
G13	VSS1076	VSS1174	Y28
G19	VSS1077	VSS1175	Y29
G23	VSS1078	VSS1176	Y4
G25	VSS1079	VSS1177	Y4
G26	VSS1080	VSS1178	Y23
G27	VSS1081	VSS1179	Y28
H5	VSS1082	VSS1180	Y29
H25	VSS1083	VSS1181	Y4
H29	VSS1084	VSS1182	Y23
H3	VSS1085	VSS1183	Y28
H6	VSS1086	VSS1184	Y29
J1	VSS1087	VSS1185	Y4
J25	VSS1088	VSS1186	Y23
J26	VSS1089	VSS1187	Y28
J27	VSS1090	VSS1188	Y29
J4	VSS1091	VSS1189	Y4
J5	VSS1092	VSS1190	Y23
K23	VSS1093	VSS1191	Y28
K28	VSS1094	VSS1192	Y29
K29	VSS1095	VSS1193	Y4
K3	VSS1096	VSS1194	Y23
K6	VSS1097	VSS1195	Y28
	VSS1098	VSS1196	Y29
	VSS_NCTF[01]	VSS_NCTF[01]	A1
	VSS_NCTF[02]	VSS_NCTF[02]	A2
	VSS_NCTF[03]	VSS_NCTF[03]	A28
	VSS_NCTF[04]	VSS_NCTF[04]	A29
	VSS_NCTF[05]	VSS_NCTF[05]	AH1
	VSS_NCTF[06]	VSS_NCTF[06]	AH29
	VSS_NCTF[07]	VSS_NCTF[07]	AJ1
	VSS_NCTF[08]	VSS_NCTF[08]	AJ2
	VSS_NCTF[09]	VSS_NCTF[09]	AJ28
	VSS_NCTF[10]	VSS_NCTF[10]	AJ29
	VSS_NCTF[11]	VSS_NCTF[11]	B1
	VSS_NCTF[12]	VSS_NCTF[12]	B29

ICH8M REV 1.0

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Deciphered Date	2006/03/10

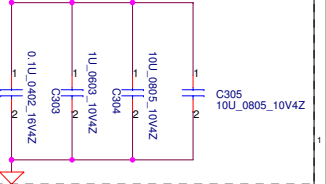
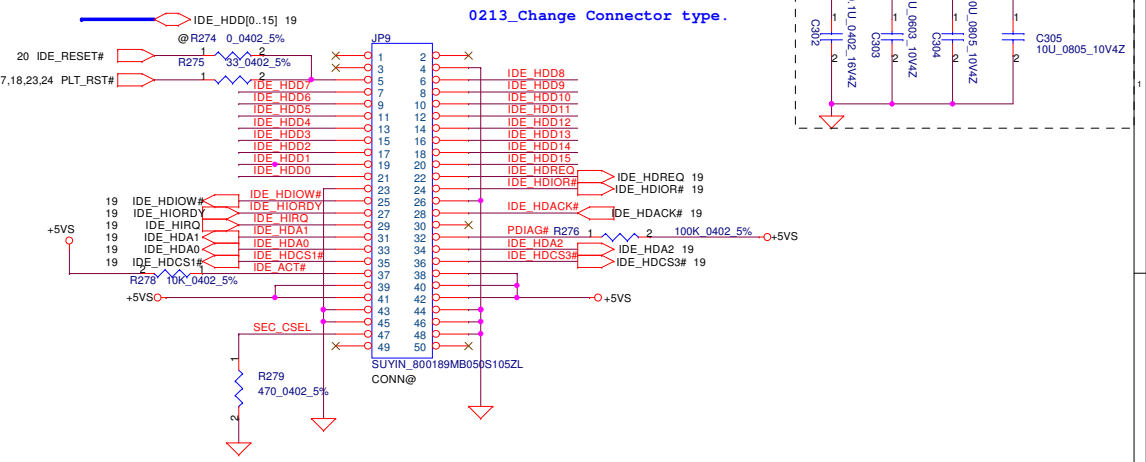
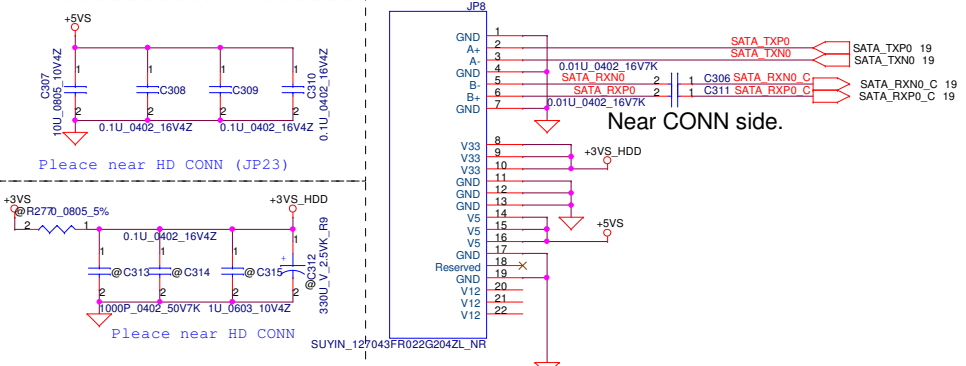
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ICH8(4/4) POWER&GND		
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# HDD Connector

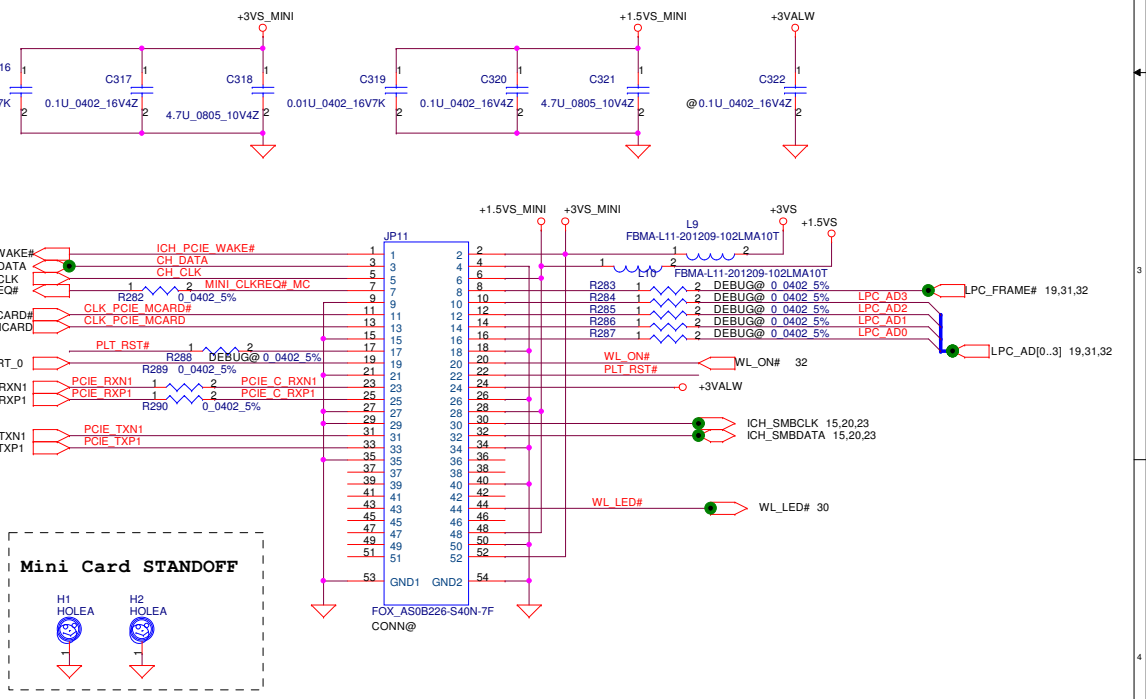
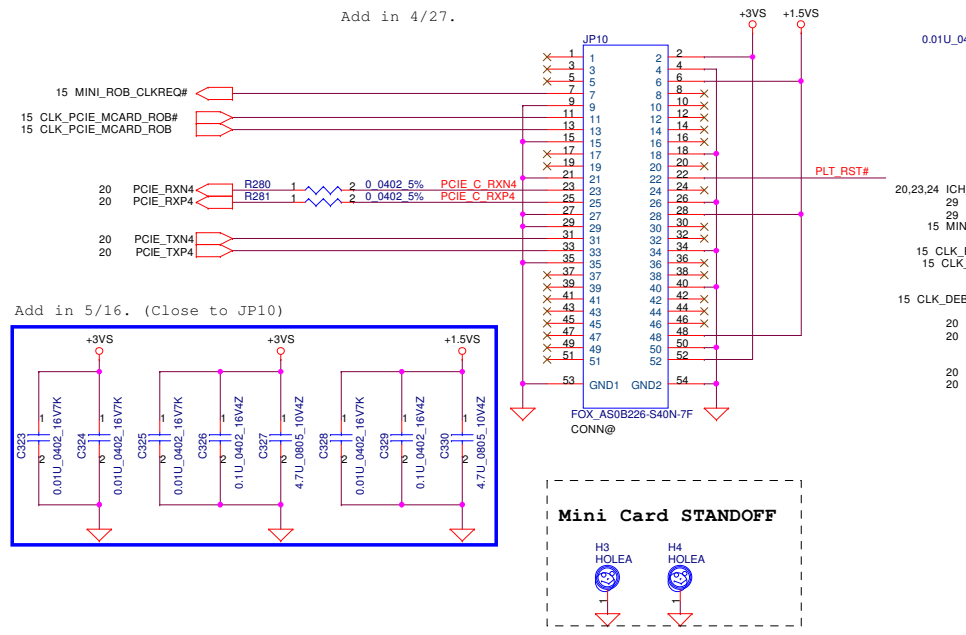
# CD-ROM Connector

Place caps. near ODD CONN.

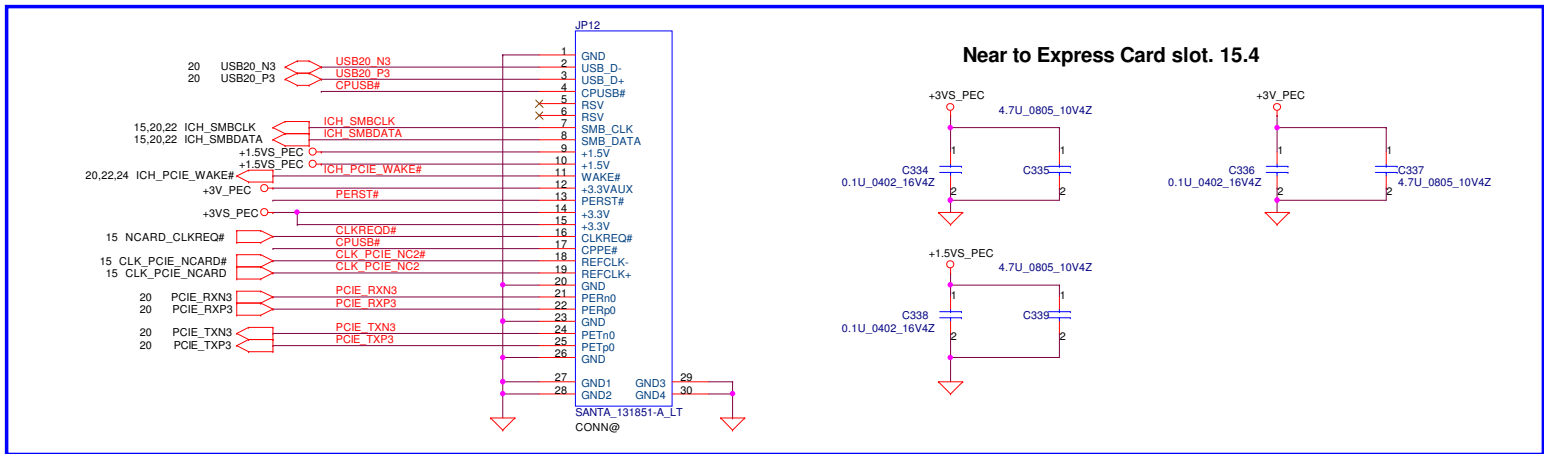
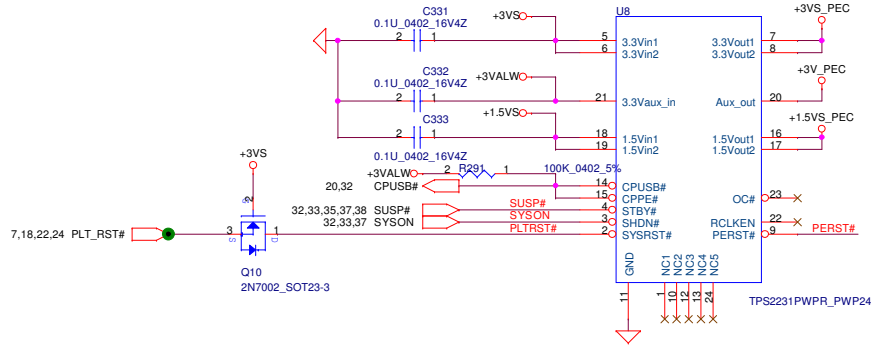


# Mini-Express Card---WLAN

# NAND mini Card(Robson support)

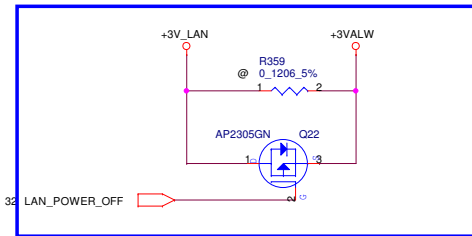
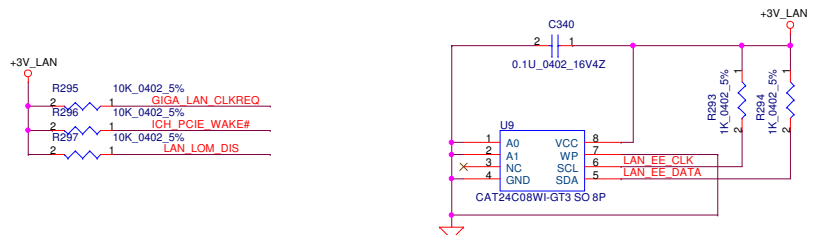


### Express Card Power Switch

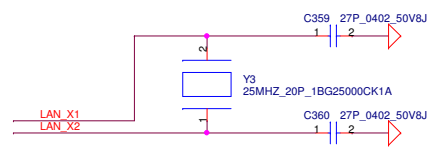
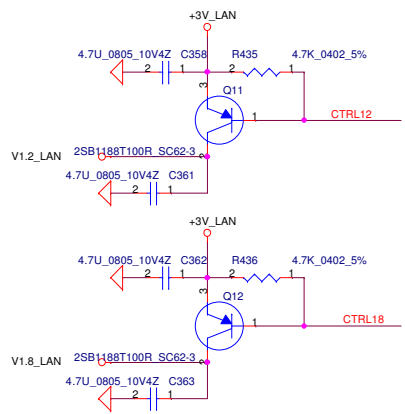
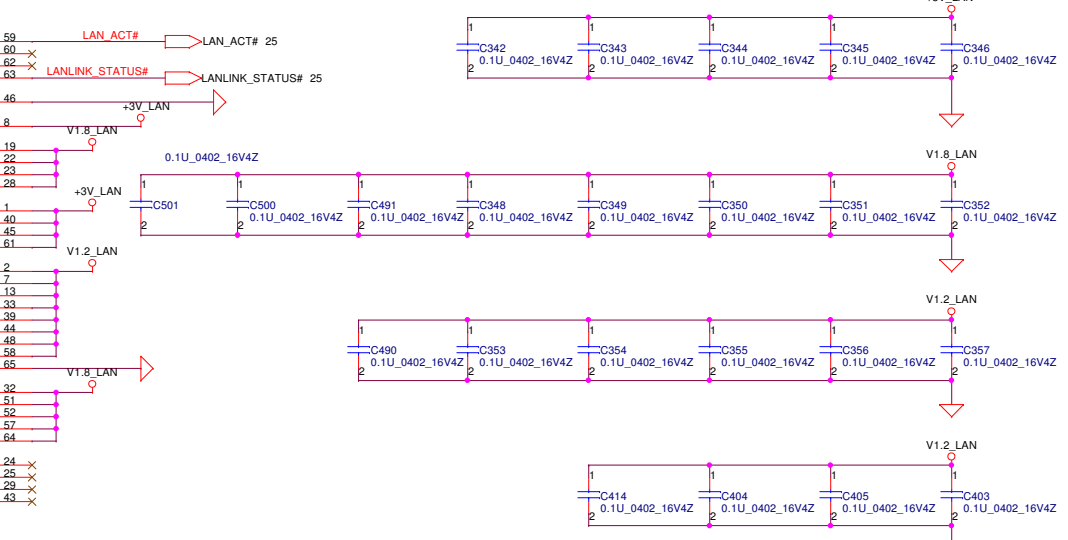
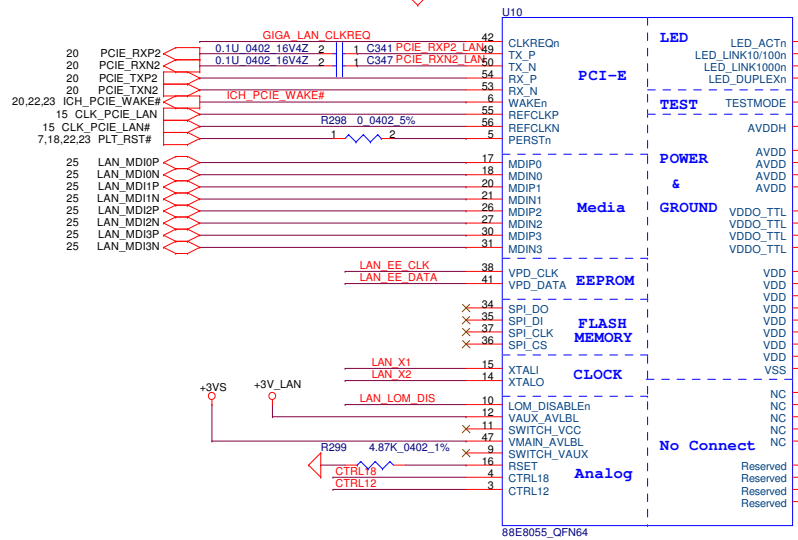


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Issued Date	2005/03/10	Deciphered Date	2006/03/10
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<b>Express Card</b>		
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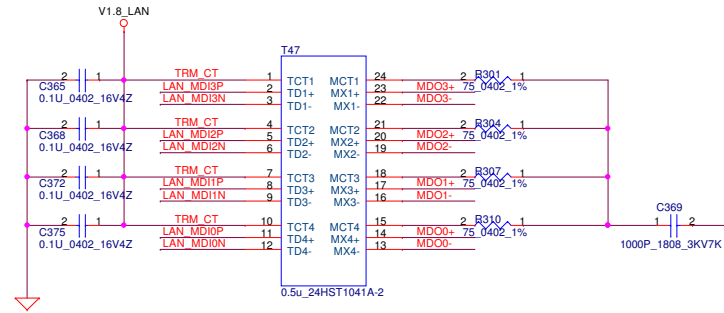
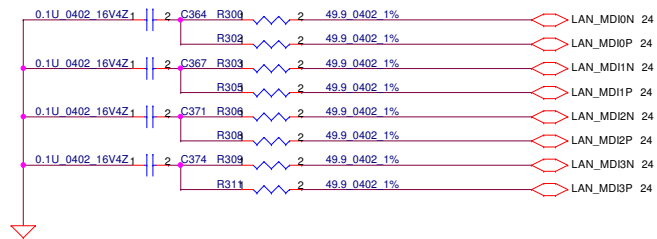


Turn off power when S3. 06/14

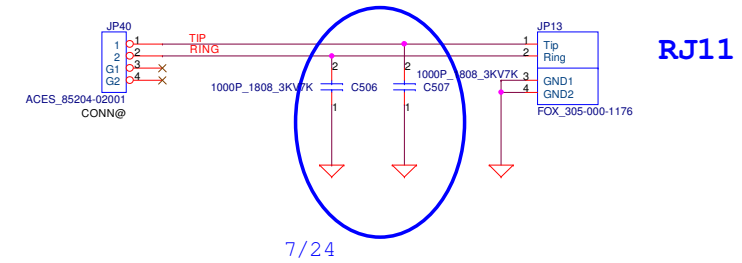
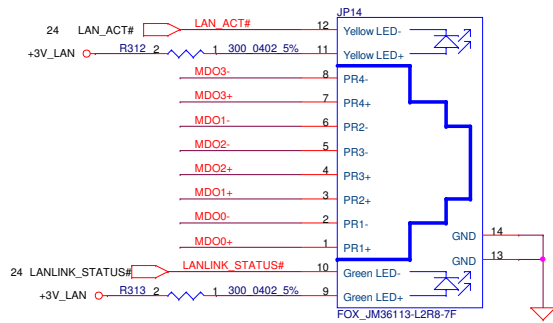


Security Classification	Compal Secret Data			Title		
Issued Date	2006/02/13	Deciphered Date	2007/08/29	LAN-8100CL		
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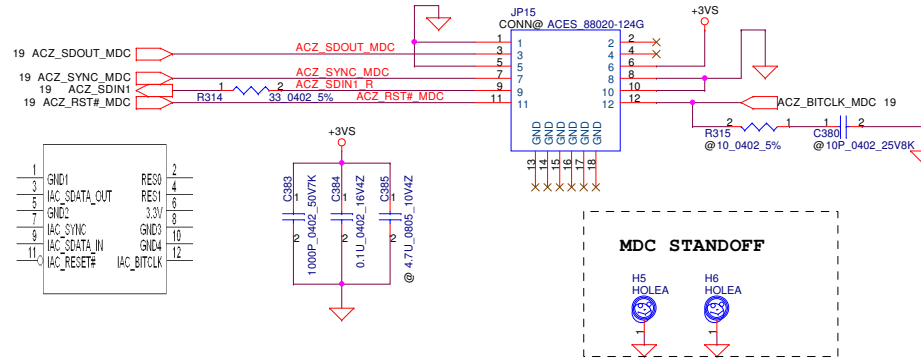


Note: MDO[3..0]+/- signals should route to JP13 first then to JP30.



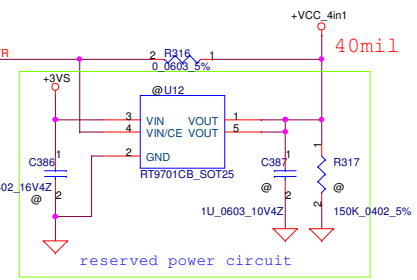
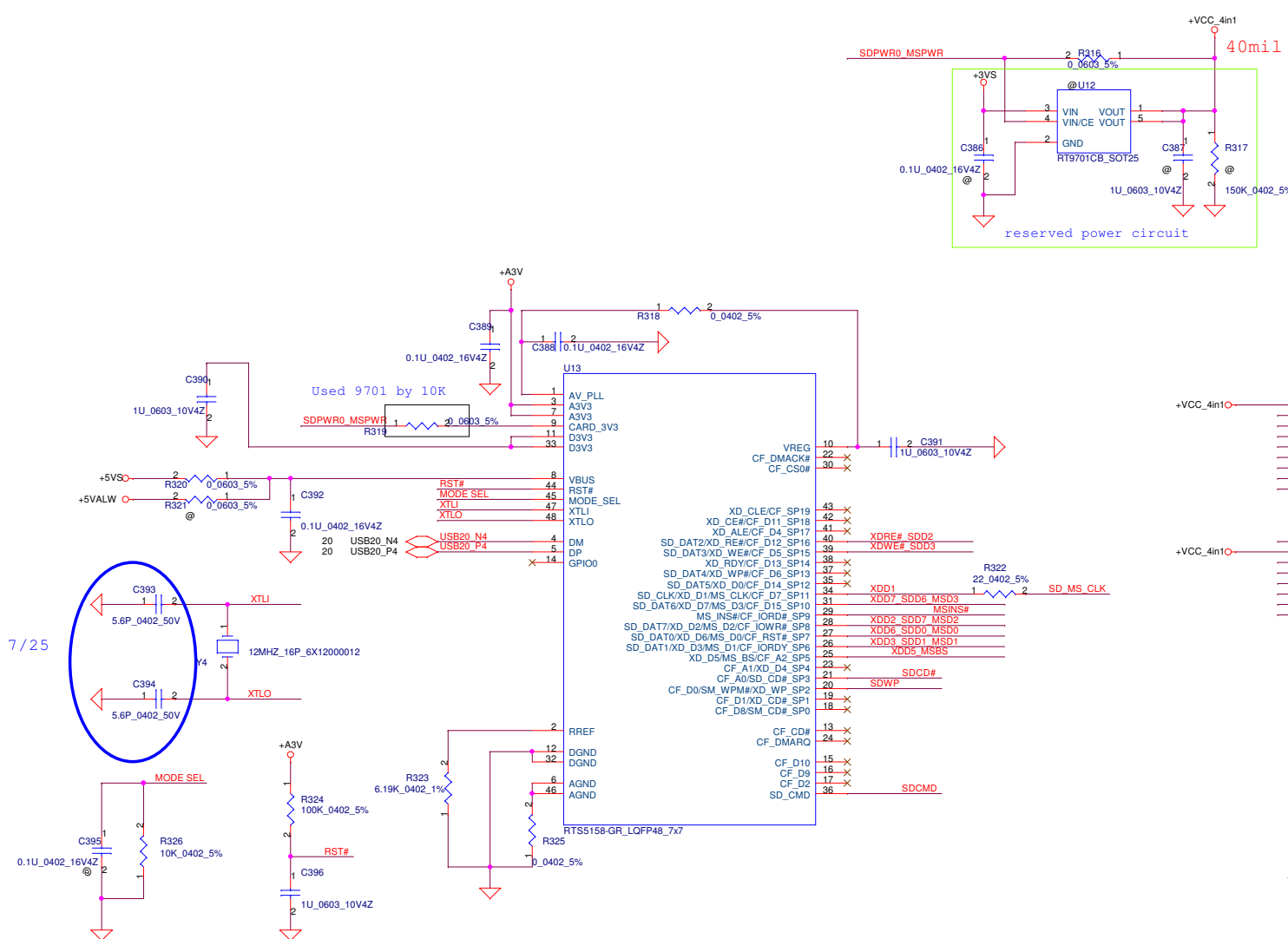
### MDC 1.5 Conn.

Change type 4/25

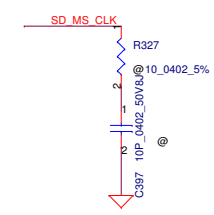
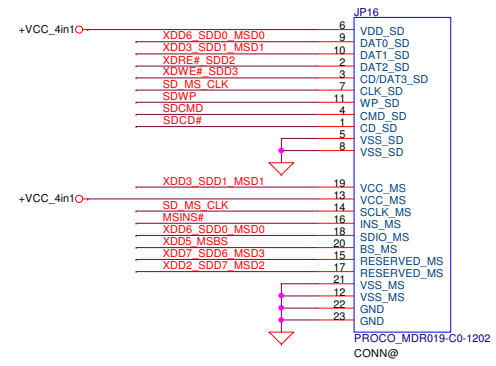


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Issued Date	2006/02/13	Deciphered Date	2006/07/26	Compal Electronics, Inc.		
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				Size	Document Number	Rev
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7/25

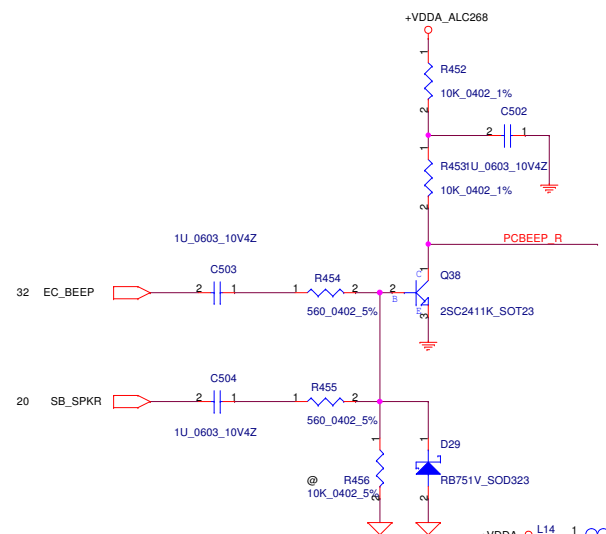


### 3 in 1 Card Reader

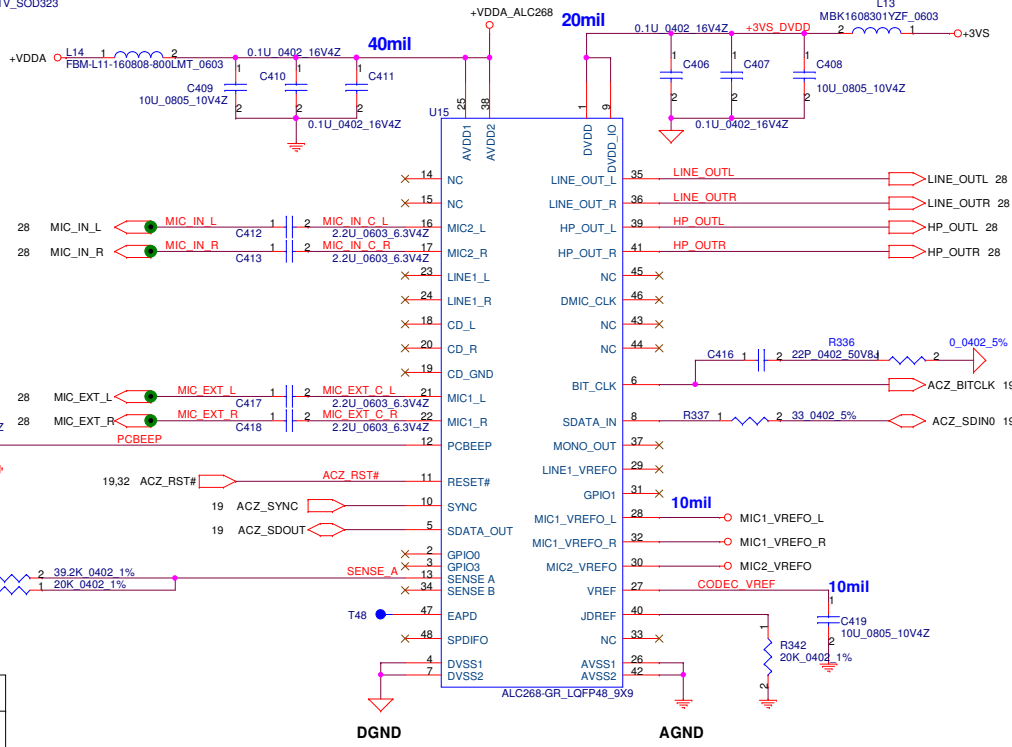


Compal Electronics, Inc.			
Title			
Card reader board			
Size	Document Number	Rev	
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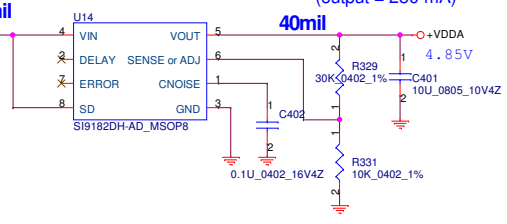
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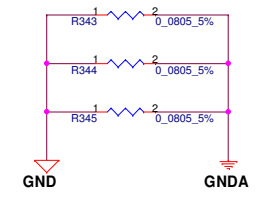
### HD Audio Codec



28.7K for Module Design (VDDA = 4.702)  
(output = 250 mA)



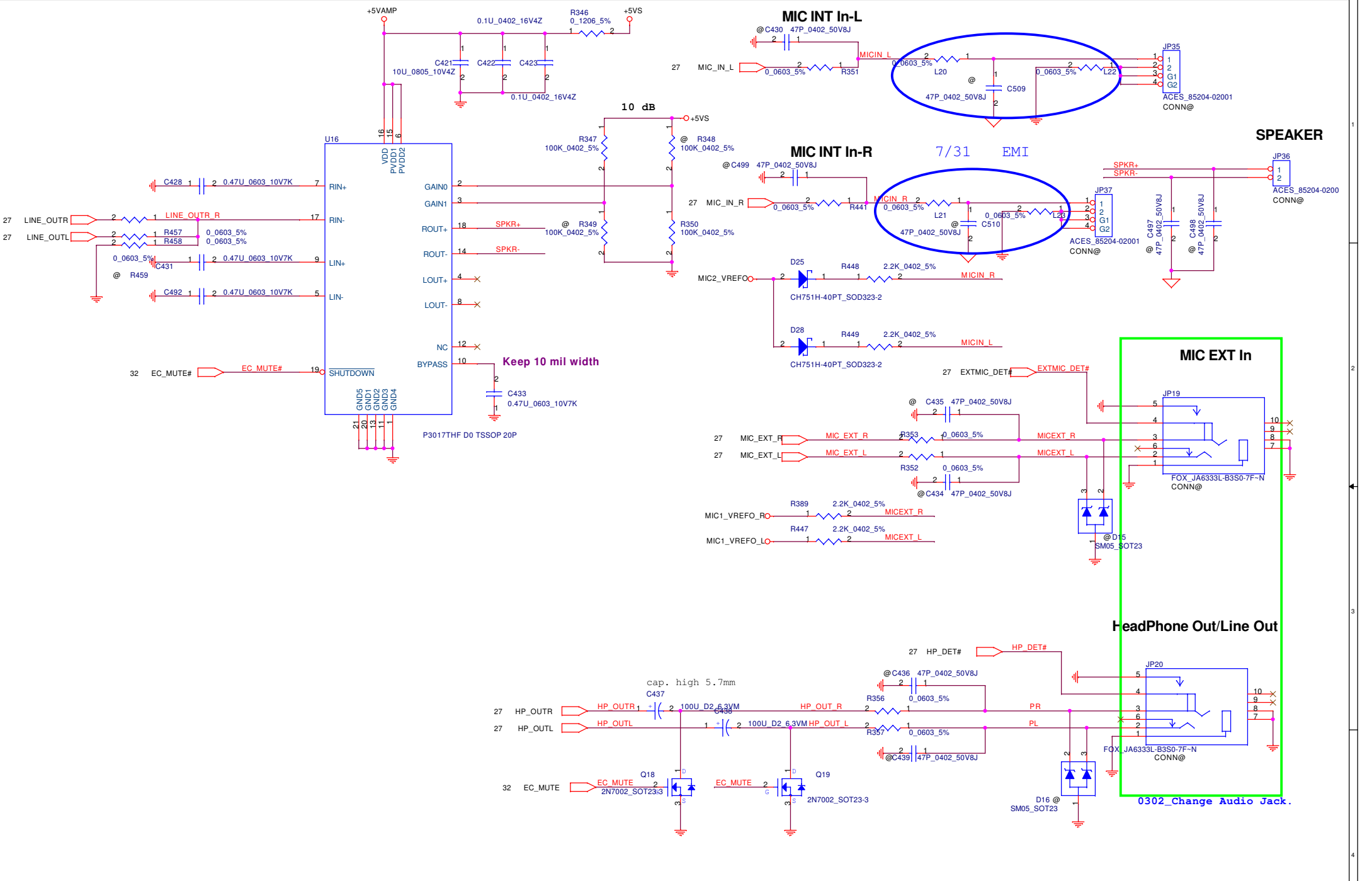
Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)



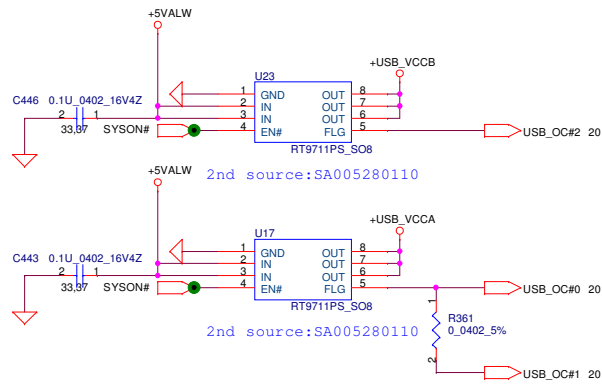
Security Classification	Compal Secret Data	
Issued Date	2006/08/18	Deciphered Date
		2007/8/18

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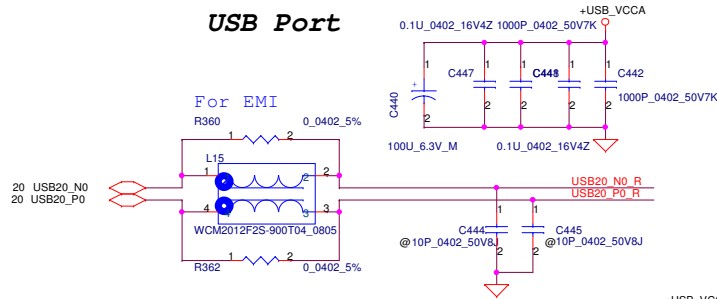
Compal Electronics, Inc.		
Title HD Audio Codec ALC268		
Size B	Document Number LA-3821P	Rev 0.3
Date: Tuesday, July 31, 2007	Sheet 27	of 43



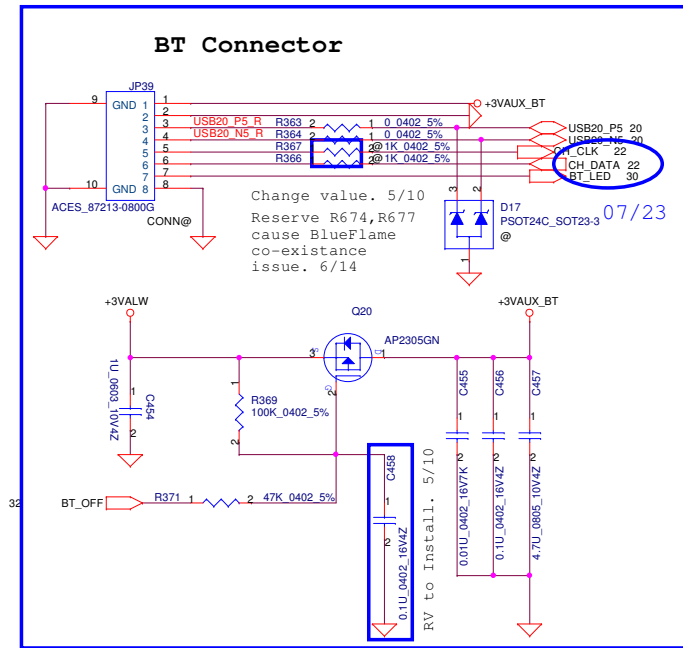
Security Classification		Compal Secret Data		Title	
Issued Date	2006/02/13	Deciphered Date	2007/08/29	Compal Electronics, Inc.	
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Size	Document Number			Rev	0.3
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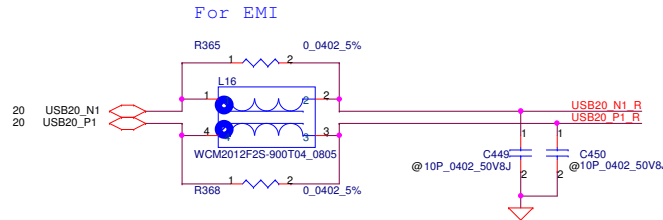
### USB Port



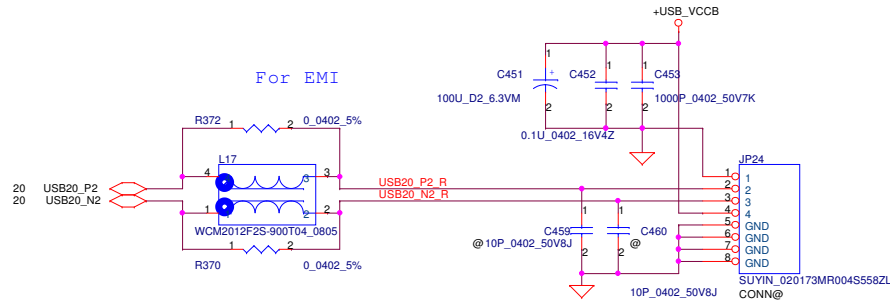
### BT Connector



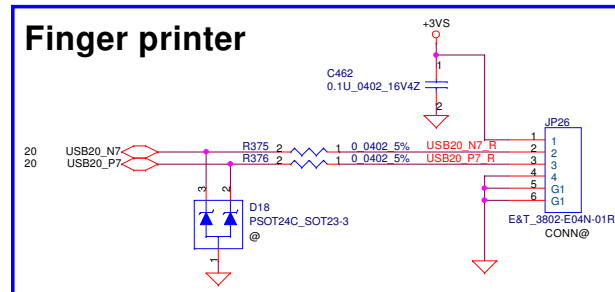
### For EMI



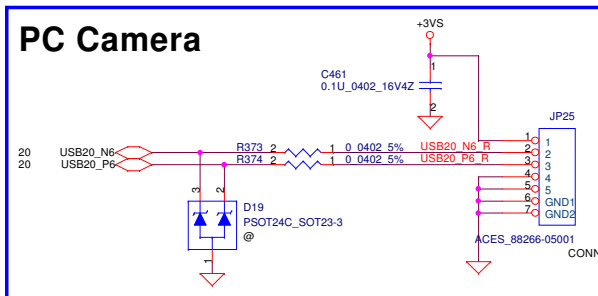
### For EMI



### Finger printer

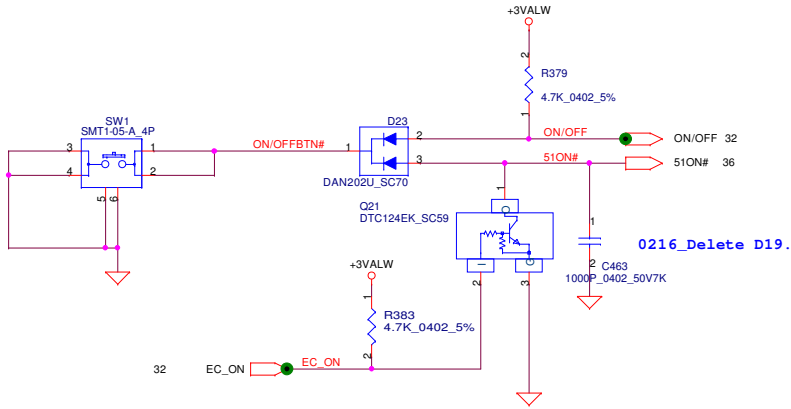


### PC Camera

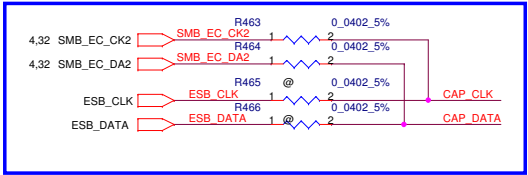


Security Classification	Compal Secret Data		Title	<b>Compal Electronics, Inc.</b>	
Issued Date	2006/02/13	Deciphered Date	2006/07/26	<b>USB CONN.</b>	
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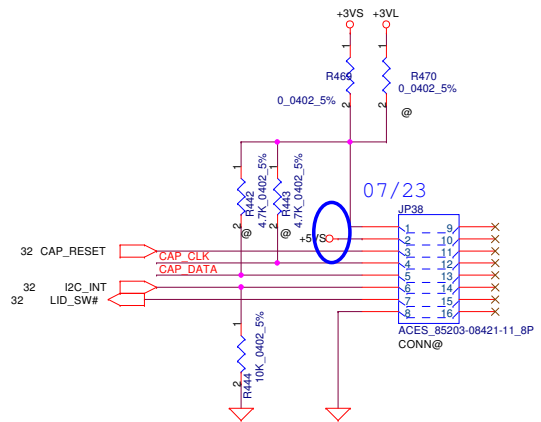
# Power ON/OFF



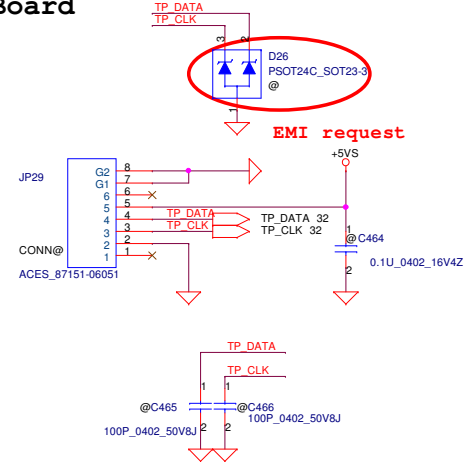
0216\_Delete D19.



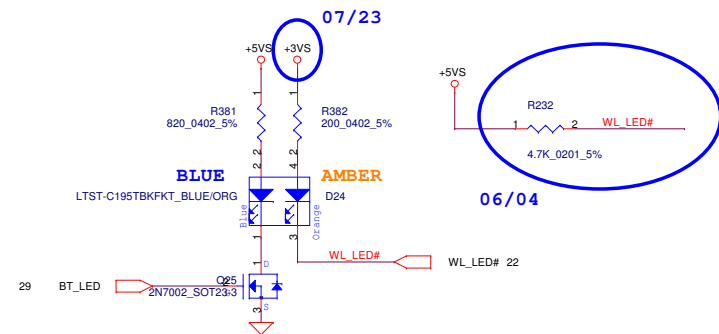
06/15 Change pin define for try ENE cap bottom



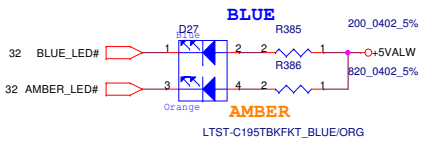
# T/P Board



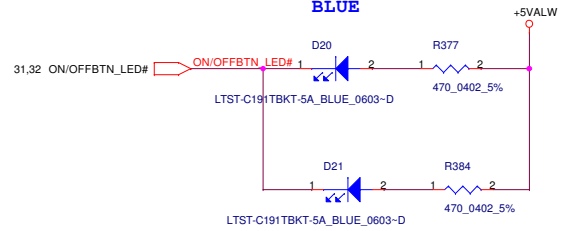
# Wireless ON Amber Bluetooth ON Blue



# Battery Charge LED(Left 2)



# POWER LED1

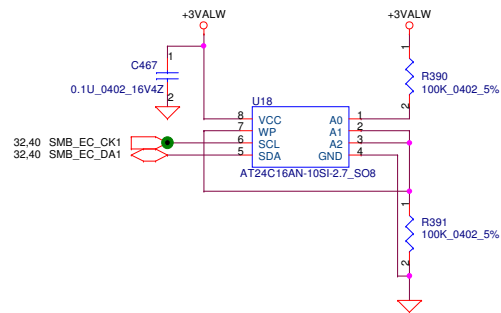


# HDD LED(Left 3)

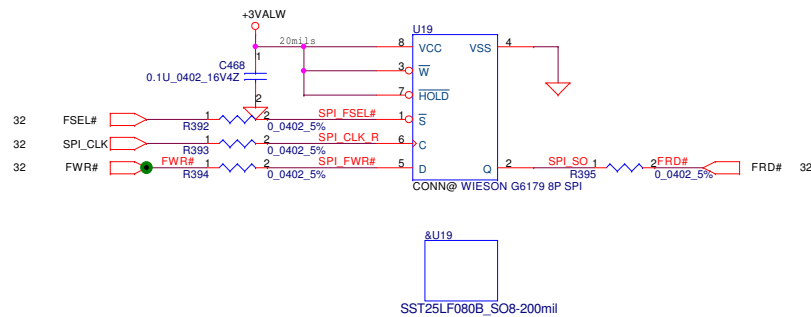


# POWER LED2

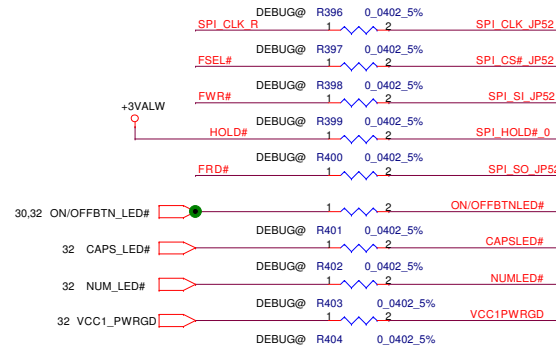
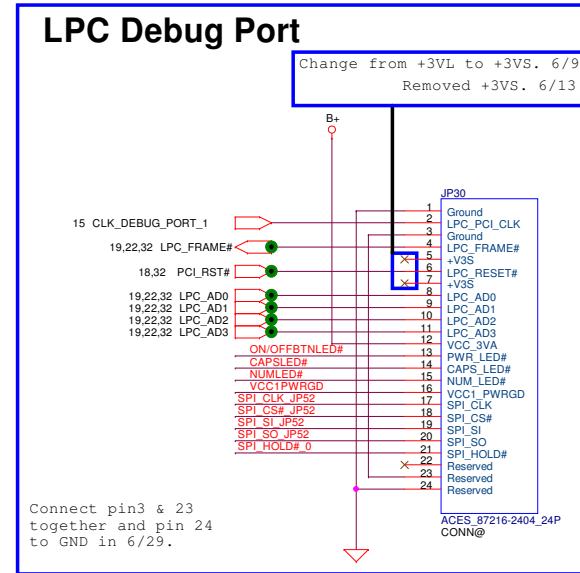
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/02/13	Deciphered Date	2006/07/26	Title
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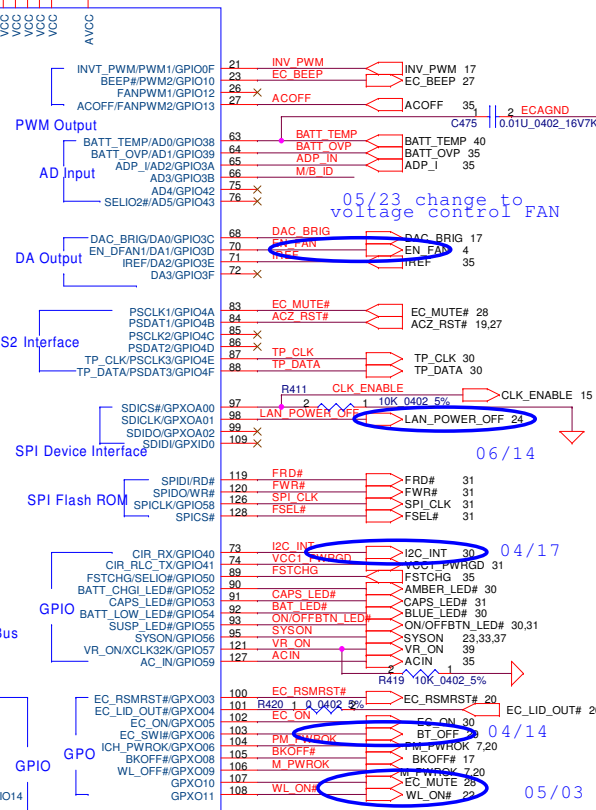
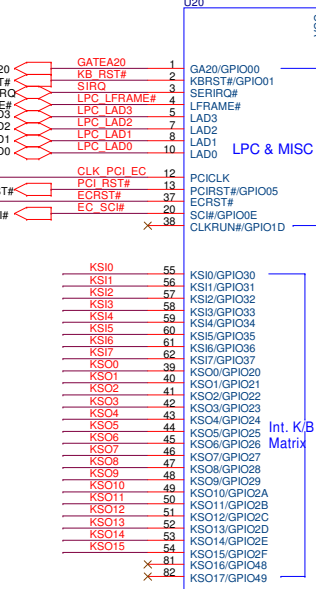
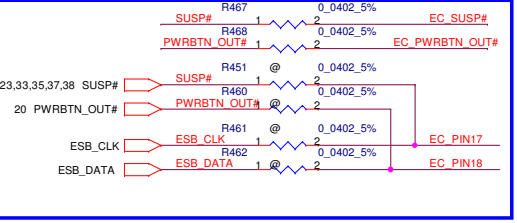
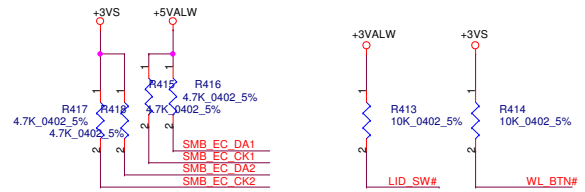
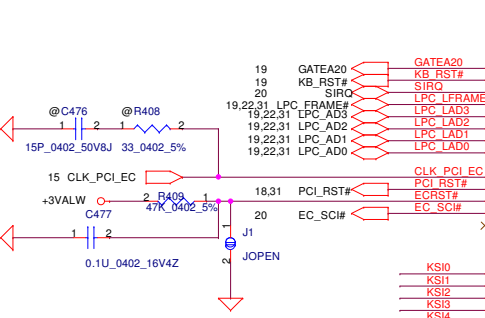
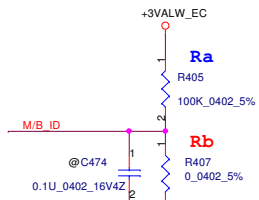
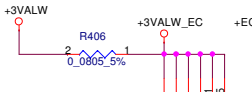
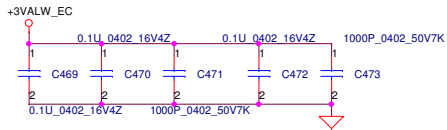
**SPI ROM**



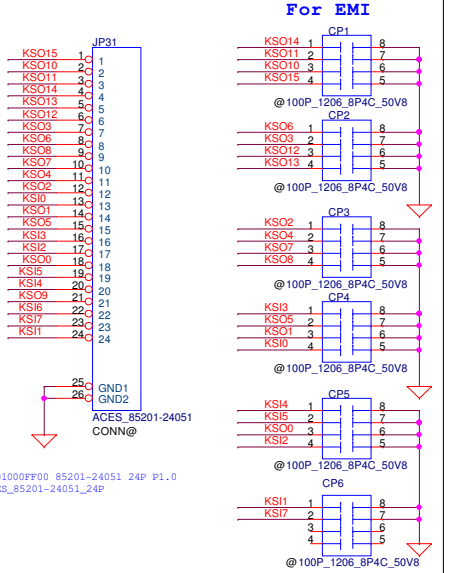
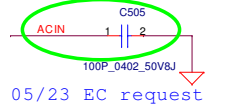
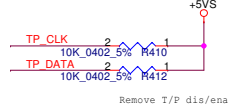
**B-Test remove SPI ROM socket**



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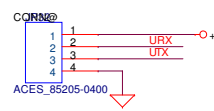
VCC	3.3V+/-5%			
Ra	100K+/-5%			
Board ID	Rb	V <sub>NO_RST</sub> min	V <sub>NO_RST</sub> typ	V <sub>NO_RST</sub> max
0	0	0V	0V	0V
1	8.2K+/-5%	0.216V	0.250V	0.289V
2	18K+/-5%	0.436V	0.503V	0.538V
3	33K+/-5%	0.712V	0.819V	0.875V
4	56K+/-5%	1.036V	1.185V	1.264V
5	100K+/-5%	1.453V	1.650V	1.759V
6	200K+/-5%	1.935V	2.200V	2.341V
7	NC	2.500V	3.300V	3.300V



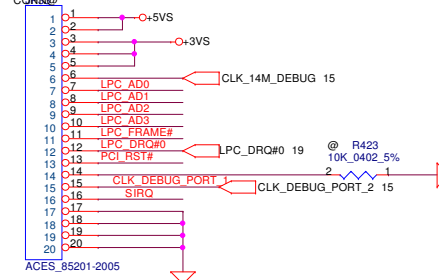
06/15 Change pin define for try ENE cap bottom

05/23 change to voltage control FAN

### EC DEBUG port



### FOR LPC SIO DEBUG PORT

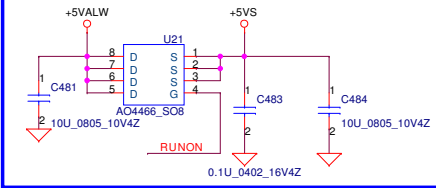


Security Classification	Compal Secret Data	
Issued Date	2006/02/13	Deciphered Date
		2006/07/26
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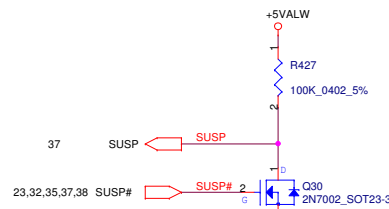
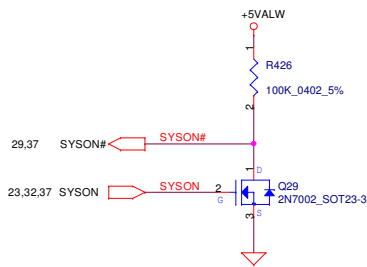
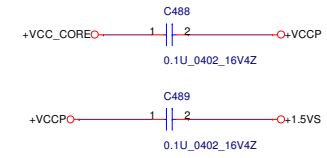
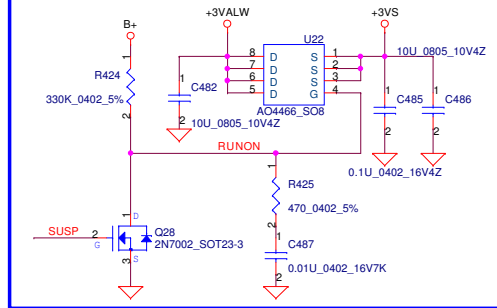
Compal Electronics, Inc.		
EC KB926/KB conn		
Title	Size	Rev
Document Number	LA-3821P	0.3
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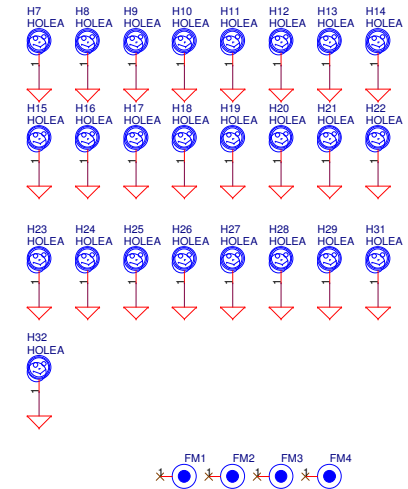
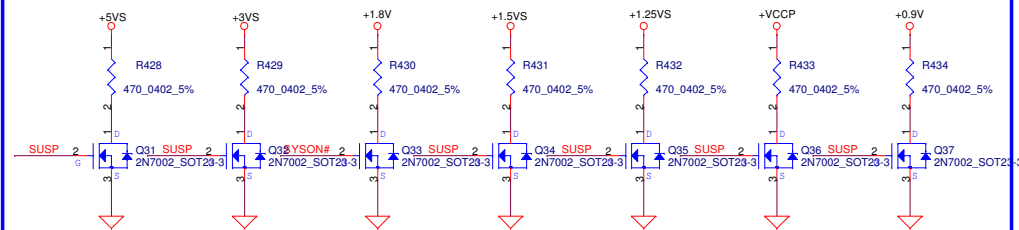
### +5VALW to +5VS Transfer



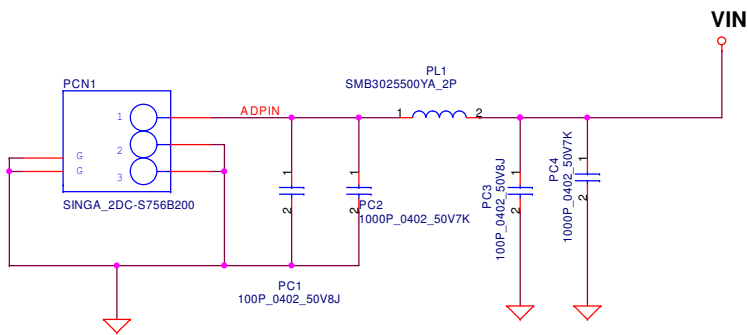
### +3VALW to +3VS Transfer



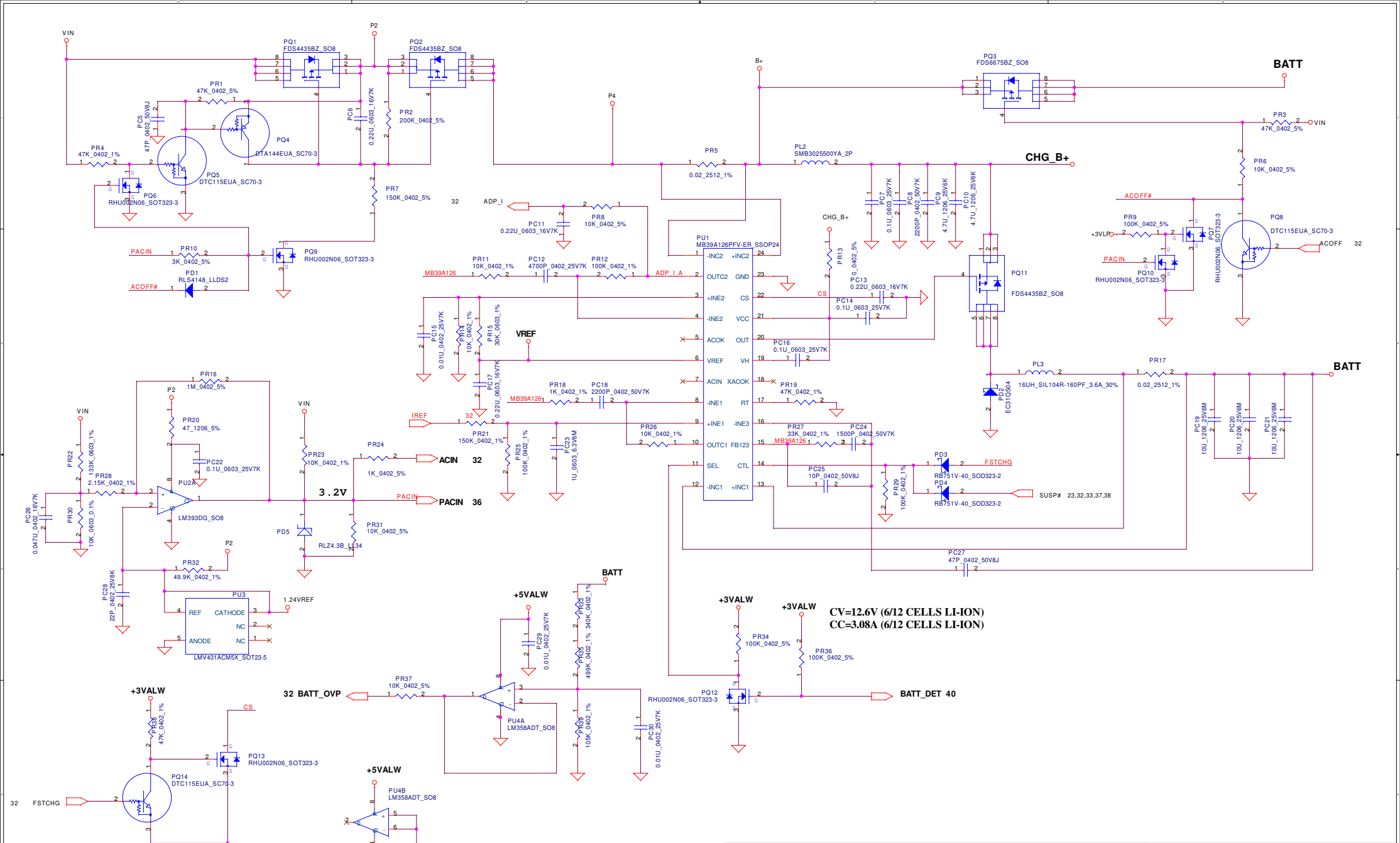
### Discharge circuit



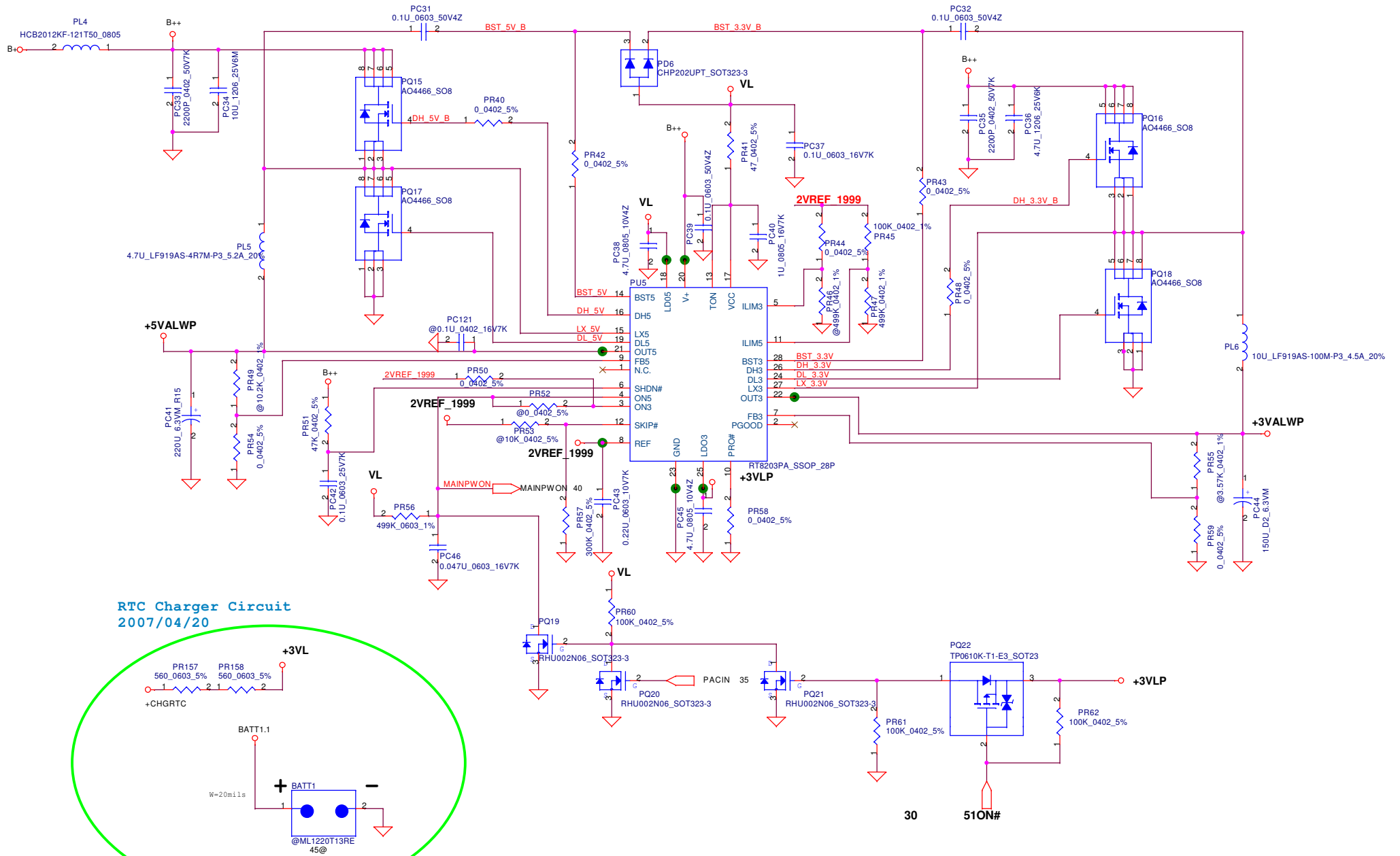
Security Classification	Compal Secret Data			Title	
Issued Date	2006/02/13	Deciphered Date	2006/07/26	DC/DC Interface	
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Issued Date	<Issued_Date>	Deciphered Date	<Deciphered_Date>	<b>DC CONN</b>
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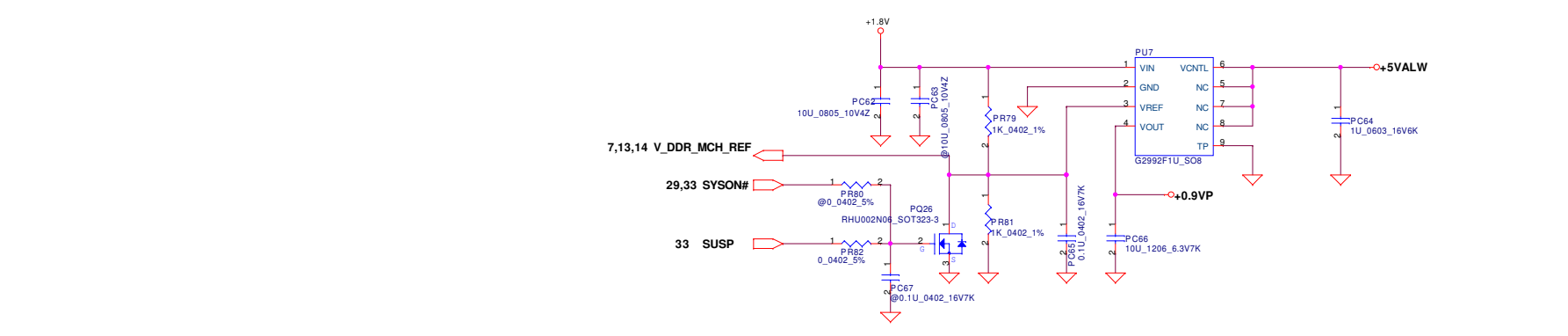
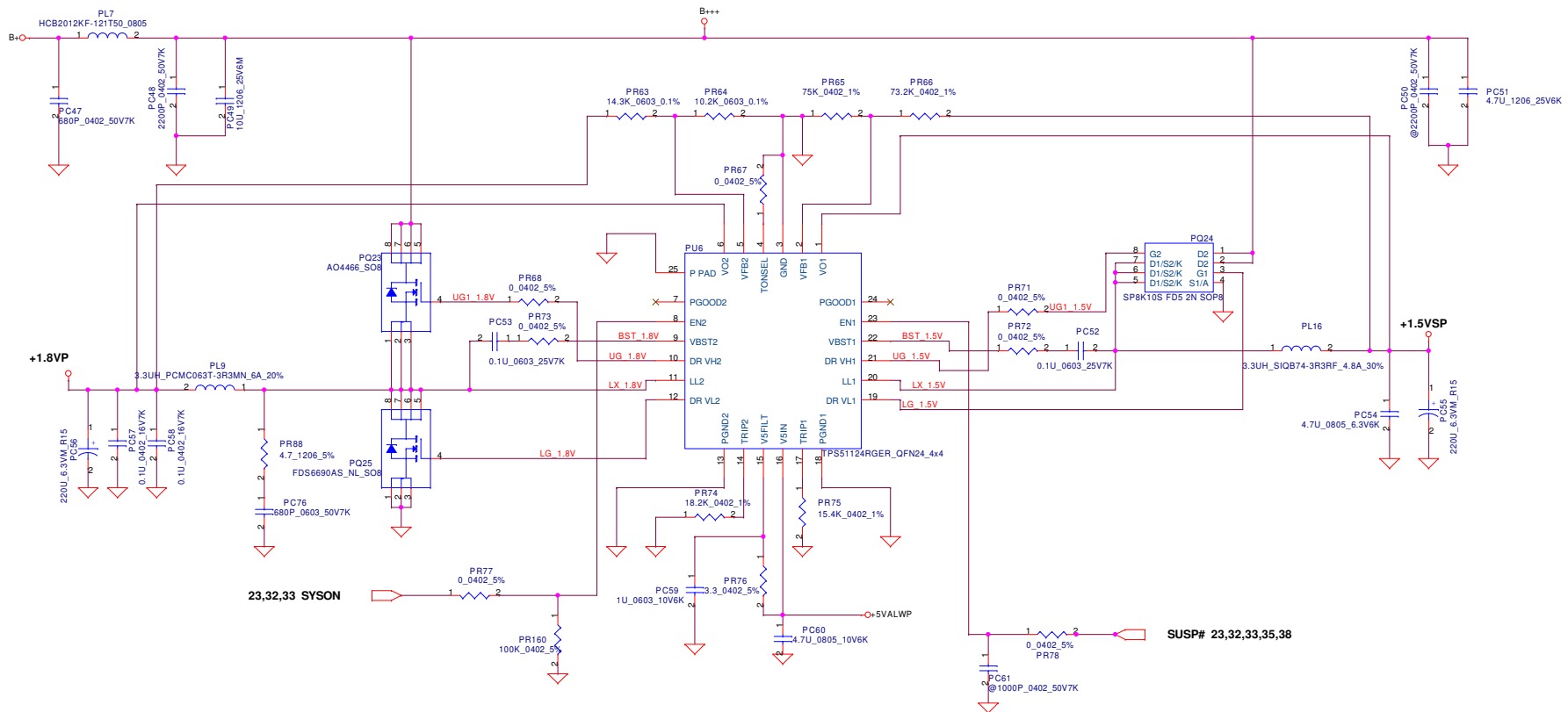


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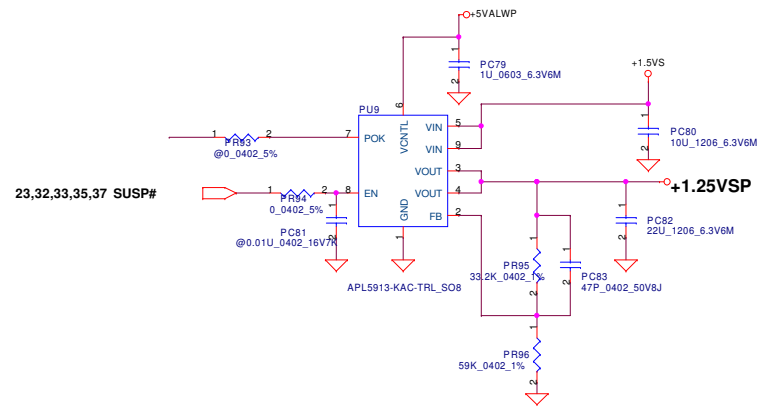
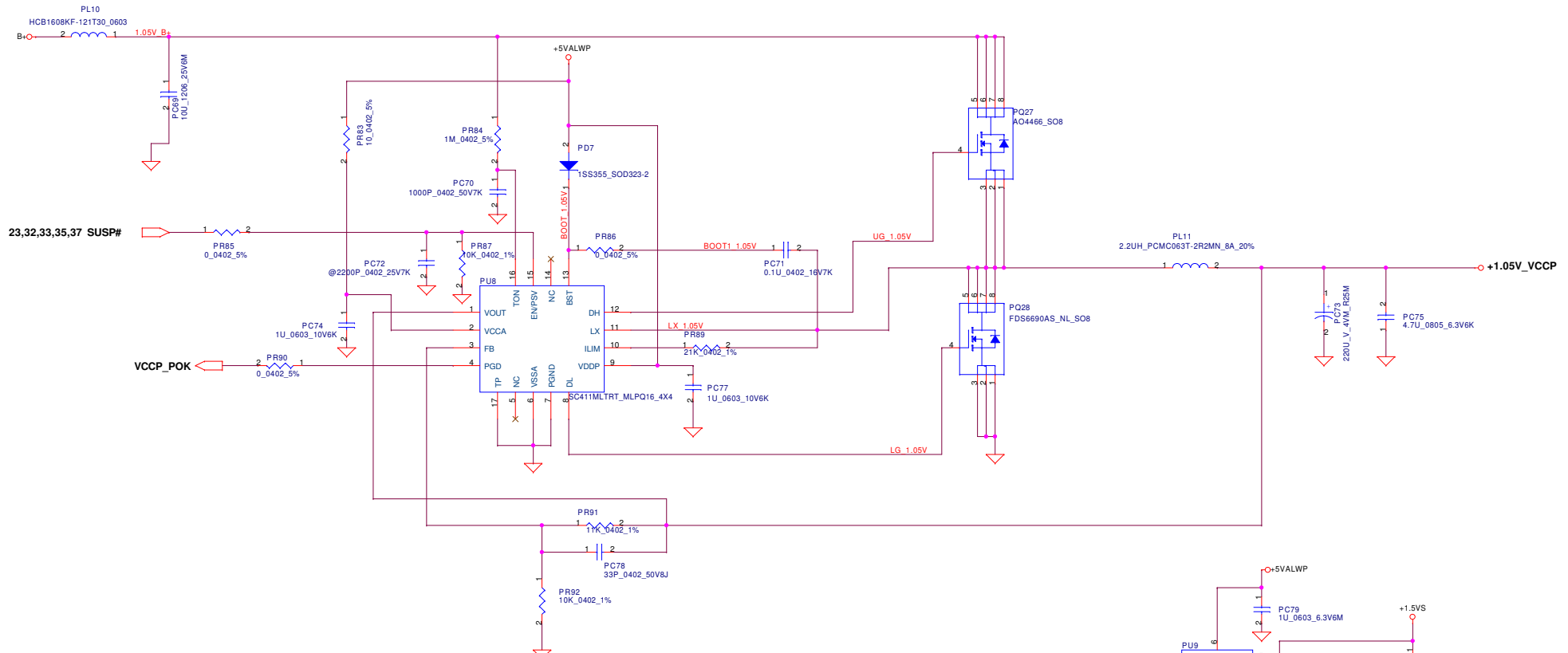


RTC Charger Circuit  
2007/04/20

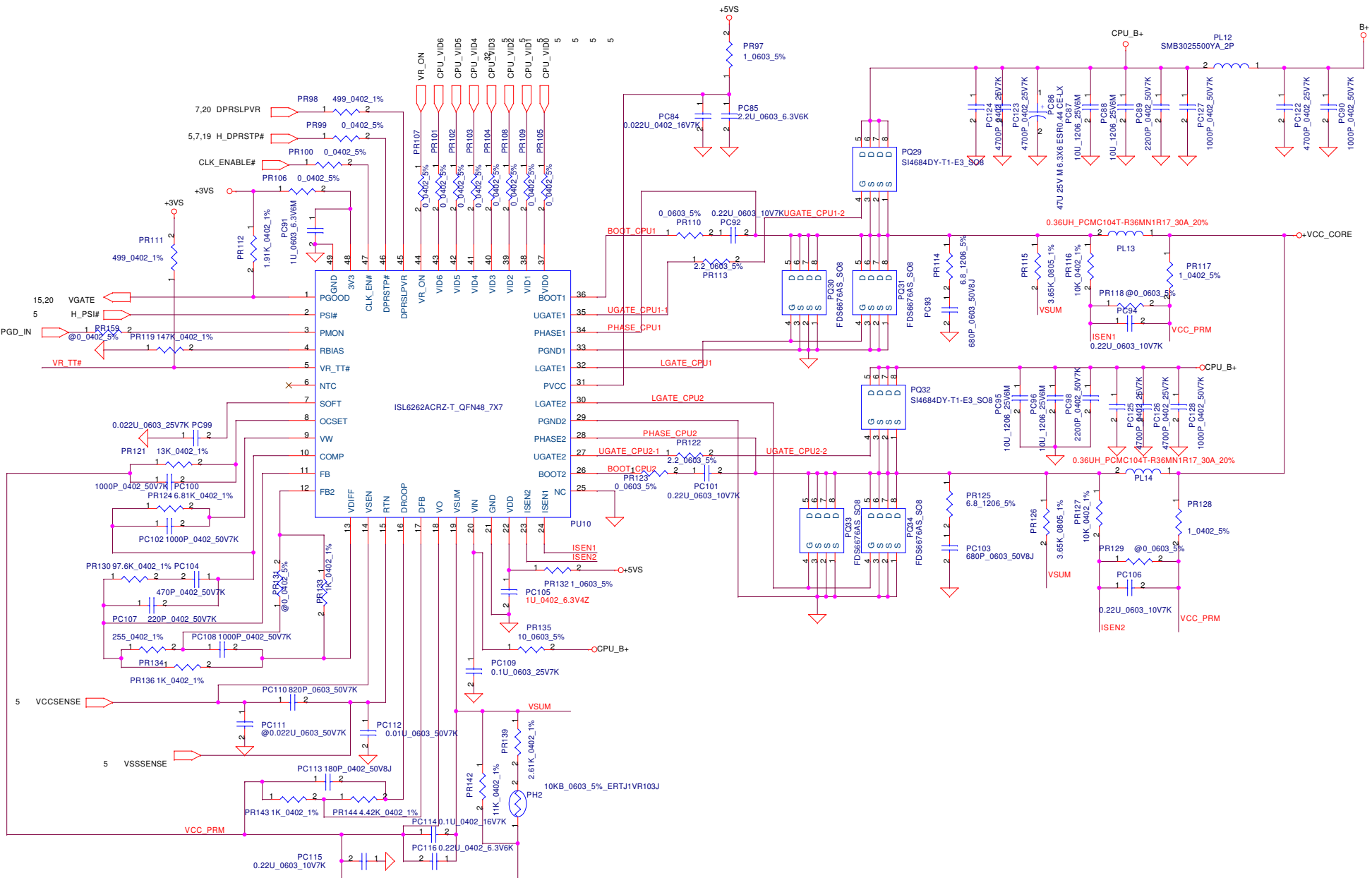
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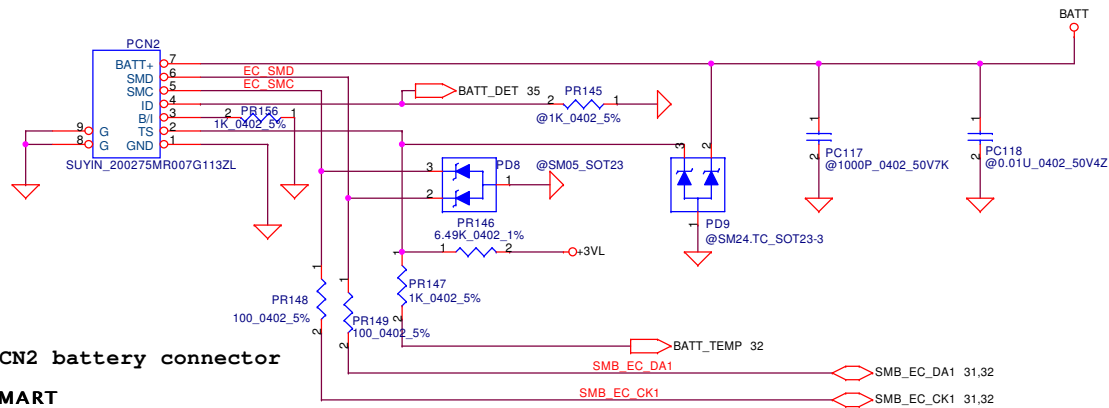
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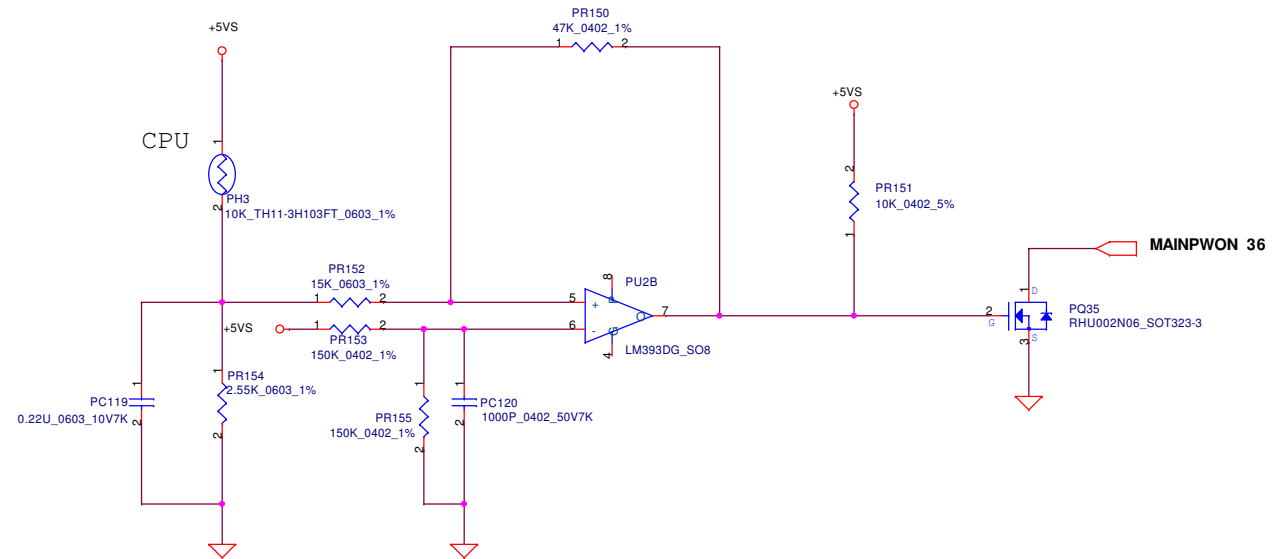
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PCN2 battery connector

- SMART Battery:**  
**7.BATT+**  
**6.SMD**  
**5.SMC**  
**4.ID**  
**3.B/I**  
**2.TS**  
**1.GND**

**PH3 under CPU bottom side :**  
 CPU thermal protection at 90 +/-3 degree C  
 Recovery at 47 +/-3 degree C



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Item	Reason for change	PG#	Modify List	Date	Phase
1	RT8203 crosstalk issue	37	add PC121 and 0.1uF	2007/05/24	SI
2	PU6 pin8 add a resistor to GND	38	add PR160 100K_ohm	2007/05/24	SI
3	remove PL15	36	remove PL15	2007/06/12	SI
4	EMI request	39	add PC122, PC123, PC124, PC125, PC126, PC127, PC128	2007/07/23	PV
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					

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Version change list (P.I.R. List)

Power section

Item	Reason for change	PG#	Modify List	Date	Phase
1	EC team request	32	ACIN add 100P (C505) to GND	2007/05/30	SI
2	Change Board ID	32	R407 from 0 Ohm to 8.2K,R405 install 100K	2007/05/30	SI
3	USB power switch fail	29	U23 & U17 change pin 4 from SLP_S5# to SYSON#	2007/05/30	SI
4	FAN use voltage control	4	del U2,Q1;add U24,C13 for 3 pin FAN	2007/05/30	SI
5	USB JP24 fail	29	Change pin define	2007/05/30	SI
6	Speaker output fail	28	Add R457,R458,R459 for Line_out	2007/05/30	SI
7	MS Pro fail	26	Add MS_D1,MS_D2,MS_D3 net	2007/06/06	SI
8	WLAN LED fail when disable WLAN	30	Add R232 pull high +5VS	2007/06/06	SI
9	+3VALW leakage	30	Del R387	2007/06/06	SI
10	Capacitor board fail	32	Add net CAP_RESET for Capacitor board reset	2007/06/06	SI
11	XDP fail	15	XDP clock share in robeson card	2007/06/06	SI
12	LAN power consumption is too large when S3	24	Add Q22	2007/06/14	SI
13	RJ11' cap is duplicate MDC module.	25	Delete C378,C379	2007/06/14	SI
14	Reverse some resistor for tring ENE cap board	30 32	Add R460~R468,R451	2007/06/14	SI
15	+LCDVDD over current when diplay.	17	Change R163 from 47K to 100K Change C248 from 0.1U to 0.22U	2007/06/21	SI
16	LAN fail	24	Change JP14 pin define	2007/06/06	SI
17	WLAN LED (Amber led) issue	30	WLAN LED need change from +5VS to +3VS	2007/07/23	PV
18	030 project Bluetooth module issue	29	Swap pin5 & pin7	2007/07/23	PV
19	change Cap board LED supply voltage	30	from +3VS to +5VS	2007/07/23	PV
20	CMOS timing can't reset	19	SHORT PAD (CLRP3) connect between +RTCVCC and GND	2007/07/23	PV
20	EMI issue (CPU core)	5	add C43 & C44 (330U)	2007/07/23	PV
21	EMI/ESD issue (XDO connector)	4	delete XDP connector	2007/07/23	PV
22	EMI/ESD issue (RJ11 connector)	25	add 1000P at RJ11 RING & TIP	2007/07/23	PV

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