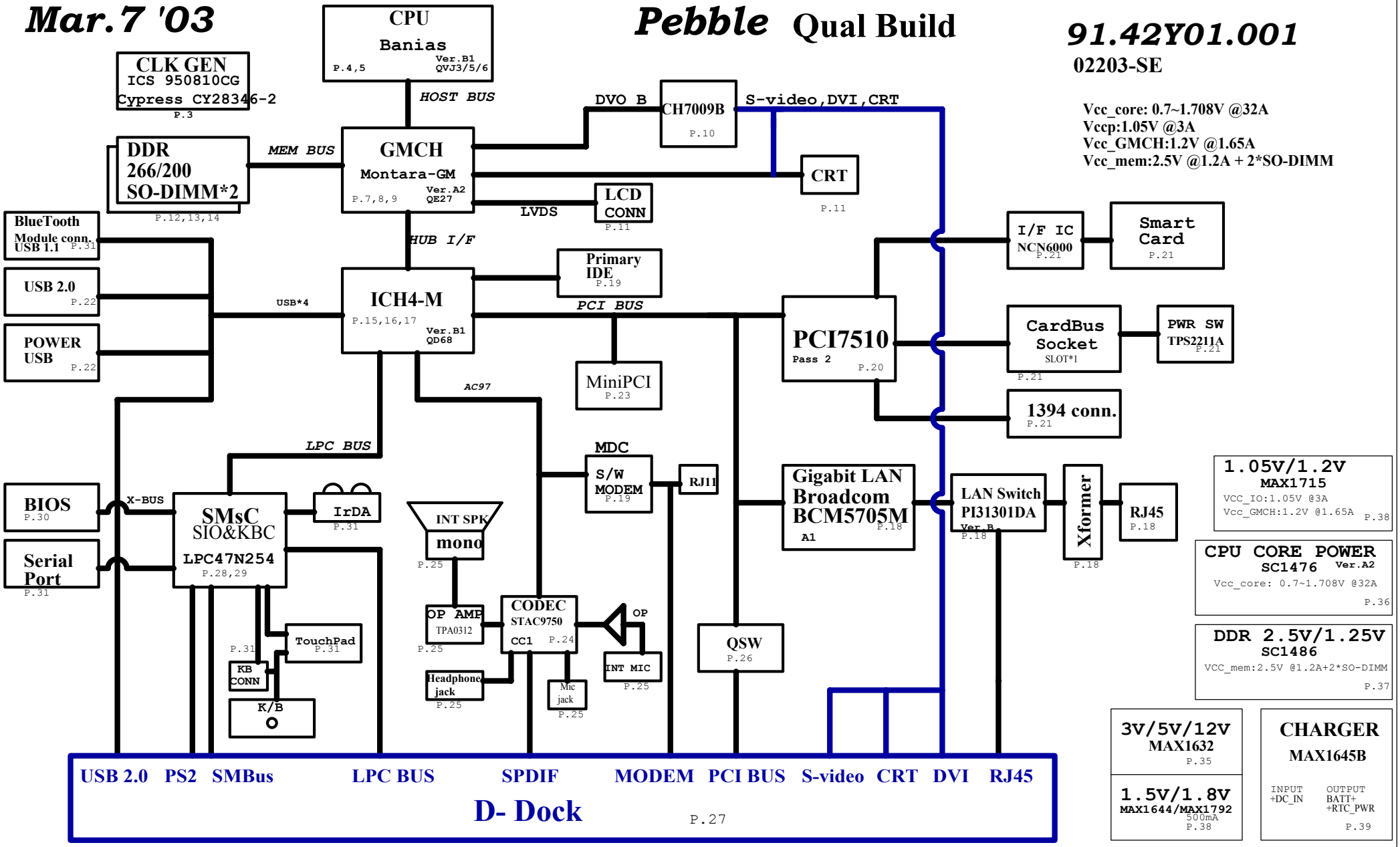
Mar.7 '03

Pebble Qual Build

91.42Y01.001

02203-SE

Vcc_core: 0.7~1.708V @32A
Vccp:1.05V @3A
Vcc_GMCH:1.2V @1.65A
Vcc_mem:2.5V @1.2A + 2*SO-DIMM



1.05V/1.2V
MAX1715
VCC_IO:1.05V @3A
Vcc_GMCH:1.2V @1.65A
P.38

CPU CORE POWER
SC1476 Ver.A2
Vcc_core: 0.7~1.708V @32A
P.36

DDR 2.5V/1.25V
SC1486
VCC_mem:2.5V @1.2A+2*SO-DIMM
P.37

3V/5V/12V
MAX1632
P.35

1.5V/1.8V
MAX1644/MAX1792
500mA
P.38

CHARGER
MAX1645B
INPUT +DC_IN
OUTPUT BATT+ +RTC_PWR
P.39

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM
Size: Custom | Document Number: PEBBLE--02203 | Rev: SE
Date: Thursday, March 13, 2003 | Sheet 1 of 40

CG_* : CPU GTL+
CC_* : CPU CMOS
M_* : MEMORY BUS
G_* : AGP BUS
P_* : PCI BUS
HL_* : HUB LINK I/F
LPC_* : LPC I/F
ICH_AC_* : AC'97 LINK I/F
IDE_* : IDE BUS

PCI TABLE

DEVICE	IDSEL	IRQ	REQ# / GNT#	DREQ/DGNT
PCMCIA PCI7510	AD17	PIRQD# PIRQC#	REQB# / GNTB#	REQ#1 / GNT#1
LAN Broadcom BCM5705M	AD16	PIRQC#		REQ4# / GNT4#
MINIPCI SLOT	AD19	PIRQB# PIRQD#		REQ3# / GNT3#
D-DOCK	AD24	PIRQB#		REQ0# / GNT0#

Montania to Montania+ changes

1.Changed VR resistor to generate 1.35V for MGM+ core(R529,R530)

2.Changed R112 from 27.4 to 37.4 Ohm (changes HLZCOMP for MGM+)

3.Put R612,R613,R614 1K ohm

4.Need Changed PSWING,HLVREF for MGM+ if use MGM core
(For Pebble don't need change because we use +1.5VRUN)

5.Layour meet DDR333 require
(For Pebble already done)

+DC_IN — +DC_IN 27,37,39
DOCK_DC_IN — DOCK_DC_IN 27
PWR_SRC — PWR_SRC 11,22,27,33,35,36,37,38,39
DOCK_PWR_SRC — DOCK_PWR_SRC 27
VCC_IO — VCC_IO 4,5,6,7,9,16,17,33,38
VCC_CORE — VCC_CORE 5,33,36
+1.5VRUN — +1.5VRUN 4,7,8,9,10,11,15,17,33
+1.8VRUN — +1.8VRUN 4,33,38
+1.2VRUN — +1.2VRUN 7,9,38

+3VRUN — +3VRUN 3,4,6,8,9,10,11,12,15,16,17,18,19,23,24,26,28,29,31,32,33,34,36,38,40
+3VSUS — +3VSUS 6,11,15,16,17,18,19,20,21,23,25,27,31,33,34,37,38,40
+3VALW — +3VALW 16,25,27,28,29,30,34,40
+3.3VRTC — +3.3VRTC 16,28,34,37
+5VRUN — +5VRUN 6,8,10,11,17,19,23,26,29,31,32,33,34,36,37,40

+5VSUS — +5VSUS 6,11,17,21,22,24,25,31,32,33,34,35,37,38,40
+5VALW — +5VALW 11,27,28,32,33,34,39
+5V_QDOCK — +5V_QDOCK 26
+3VAUX_LAN — +3VAUX_LAN 18,23,33
+1.2VAUX_LAN — +1.2VAUX_LAN 18
+2.5VAUX_LAN — +2.5VAUX_LAN 18,27
BATT+ — BATT+ 39
+5VHDD — +5VHDD 19,33

LCDVDD — LCDVDD 11

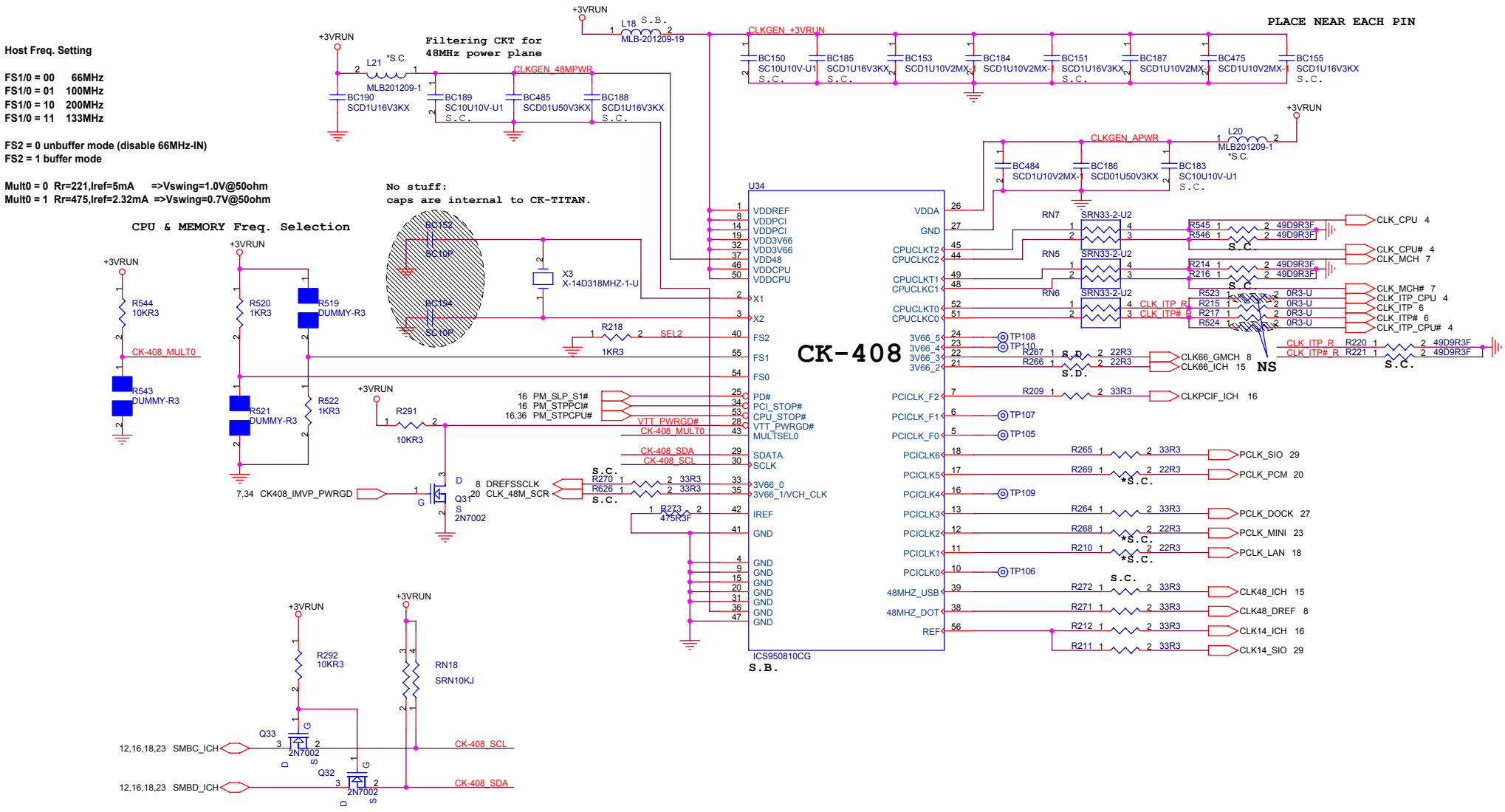
AC97_5V — AC97_5V 19
AC97_3V — AC97_3V 19
CRT_VCC — CRT_VCC 11
CBS_VCC — CBS_VCC 20,21
CBS_VPP — CBS_VPP 21
CBS_VCCF — CBS_VCCF 21
+1.25VRUN — +1.25VRUN 13,14,33,37
+2.5VSUS — +2.5VSUS 6,7,9,12,14,33,37
ICH_VBIAS — ICH_VBIAS 16
VCC_RTC — VCC_RTC 16
+RTCSRC — +RTCSRC 37
+RTC_PWR — +RTC_PWR 34,35,37,39,40

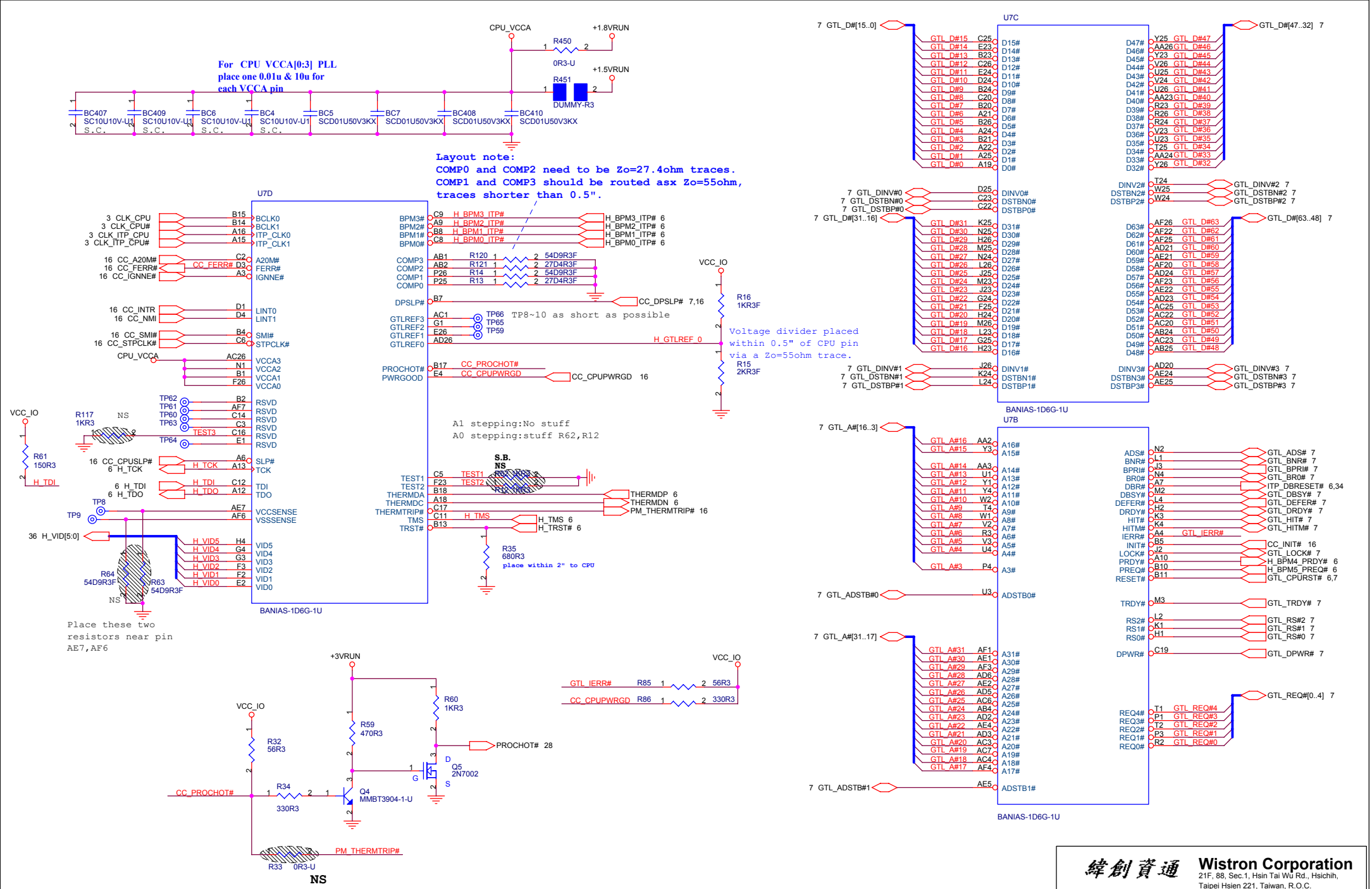
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Table of Content***

Size	Document Number	Rev
A3	**PEBBLE--02203**	SD

Date: Monday, February 24, 2003 Sheet 2 of 40


Host Freq. Setting
FS1/0 = 00 66MHz
FS1/0 = 01 100MHz
FS1/0 = 10 200MHz
FS1/0 = 11 133MHz
FS2 = 0 unbuffer mode (disable 66MHz-IN)
FS2 = 1 buffer mode
Mult0 = 0 Rr=221,Iref=5mA =>Vswing=1.0V@50ohm
Mult0 = 1 Rr=475,Iref=2.32mA =>Vswing=0.7V@50ohm
CPU & MEMORY Freq. Selection
Filtering CKT for 48MHz power plane
No stuff:
caps are internal to CK-TITAN.
PLACE NEAR EACH PIN
CK-408
ICS950810CG
S.B.
+3VRUN
CLKGEN_+3VRUN
CLKGEN_48MPWR
CLKGEN_APWR
CK-408_MULT0
CK-408_SCL
CK-408_SDA
SMBC_ICH
SMBD_ICH
CK408_IMVP_PWRGD
PM_SLP_S1#
PM_STPPCI#
PM_STPCPU#
VTT_PWRGD#
CLK_48M_SCR
DREFSSCLK
SEL2
CLK_ITP_R
CLK_ITP#_R
CLK_CPU
CLK_CPU#
CLK_MCH
CLK_MCH#
CLK_ITP_CPU
CLK_ITP
CLK_ITP#
CLK_ITP_CPU#
CLK66_GMCH
CLK66_ICH
CLKPCIF_ICH
PCLK_SIO
PCLK_PCM
PCLK_DOCK
PCLK_MINI
PCLK_LAN
CLK48_ICH
CLK48_DREF
CLK14_ICH
CLK14_SIO
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Clock GEN.
PEBBLE--02203
Size A3
Rev SD
Date: Thursday, March 13, 2003
Sheet 3 of 40



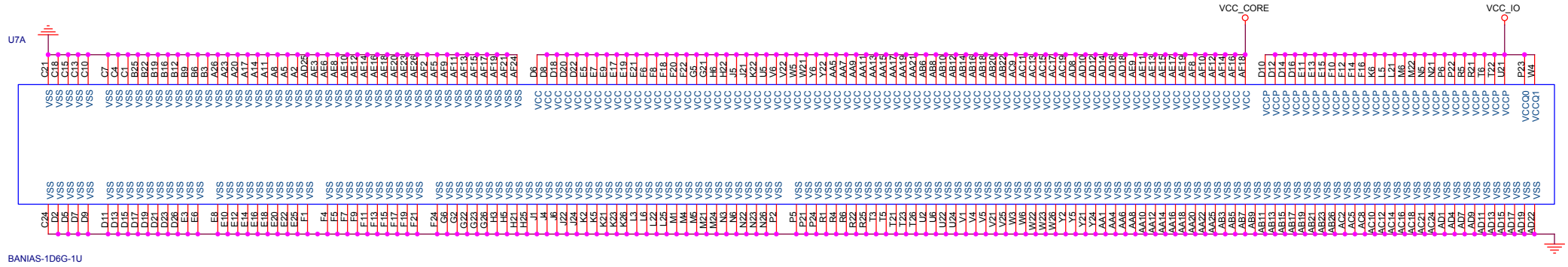
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Banias CPU (1 of 2)**

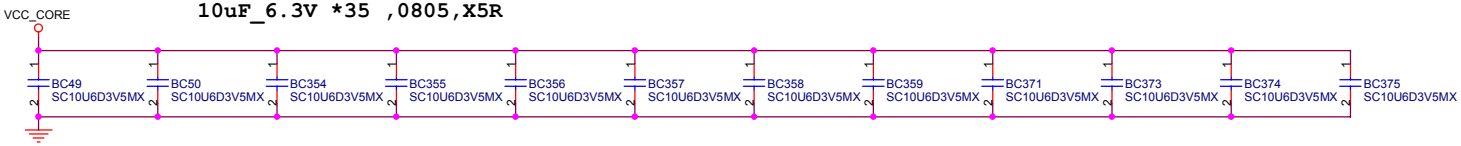
Size	Document Number	Rev
A3	PEBBLE--02203	SD

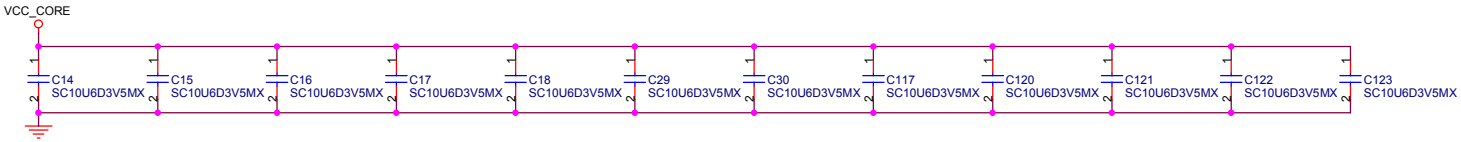
Date: Thursday, March 13, 2003 Sheet 4 of 40

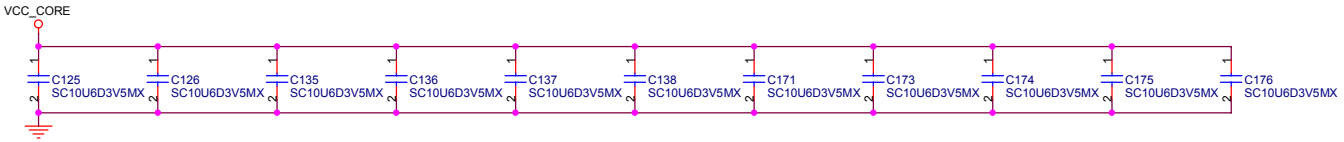
Ref 10598 EMTS
P69 need place
Decoupling
near between
VCCQ ???



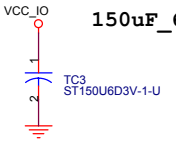
10uF_6.3V *35 ,0805,X5R



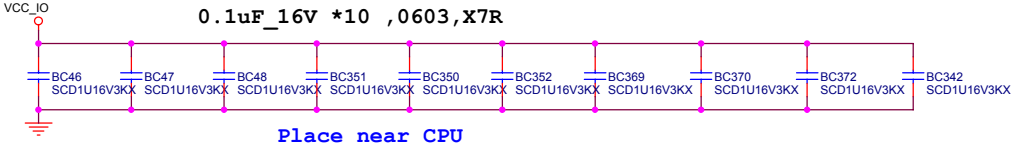




150uF_6.3V *1



0.1uF_16V *10 ,0603,X7R



Place near CPU

Banias CPU part number

B9.00016.001	IC CPU BANIAS1.7G UFCBGA
B9.00017.001	IC CPU BANIAS1.6G UFCBGA
B9.00018.001	IC CPU BANIAS1.5G UFCBGA
B9.00019.001	IC CPU BANIAS1.4G UFCBGA
B9.00020.001	IC CPU BANIAS1.3G UFCBGA

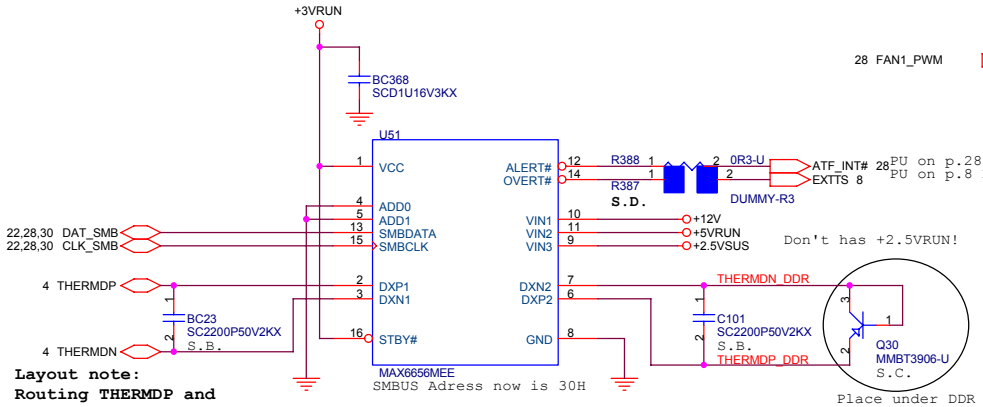
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Banias CPU (2 of 2)*

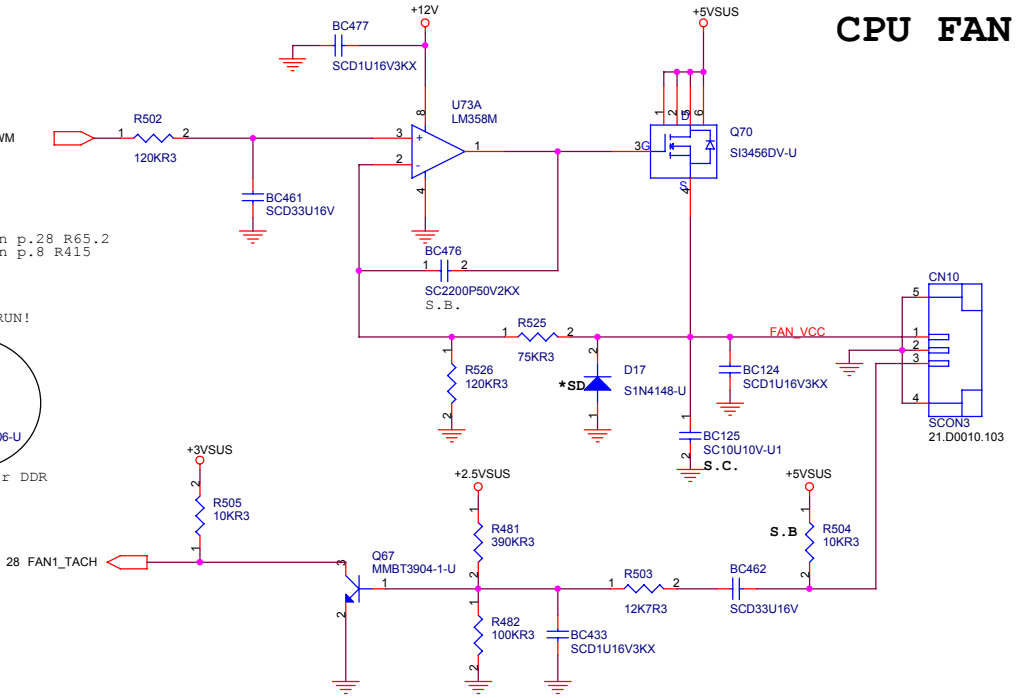
Size: A3 | Document Number: PEBBLE--02203 | Rev: SD

Date: Thursday, March 13, 2003 | Sheet 5 of 40

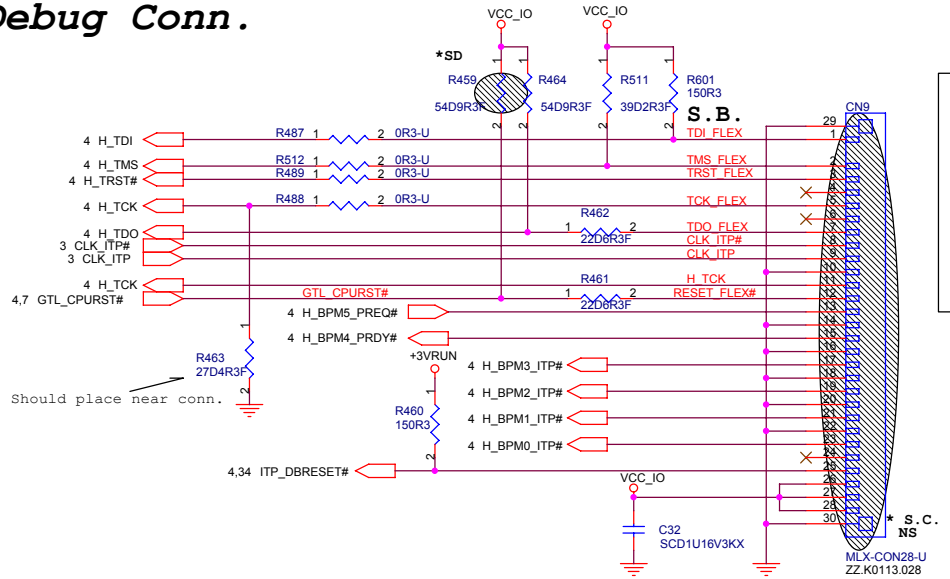
THERMAL SENSOR MAX6656

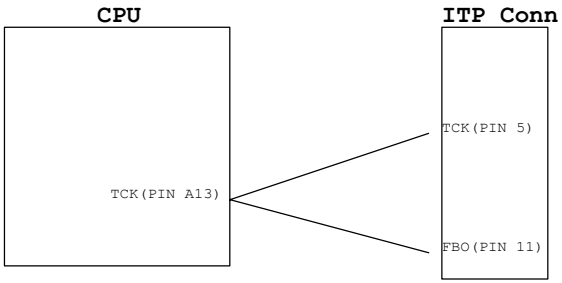


CPU FAN



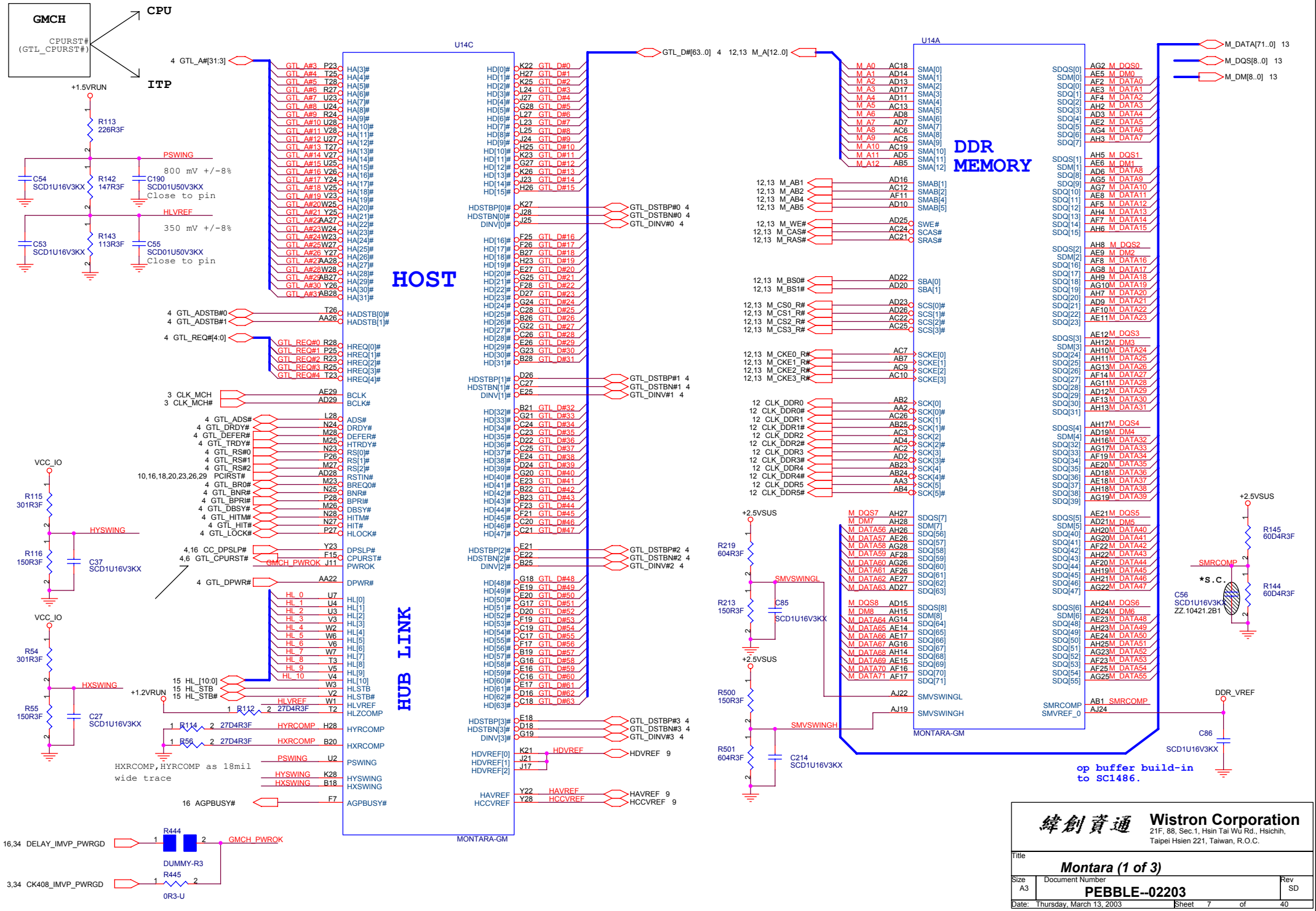
ITP Debug Conn.





緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***MAX6656,Fan Control***	
Size A3	Document Number **PEBBLE--02203**	Rev SD
Date: Thursday, March 13, 2003	Sheet 6 of 40	

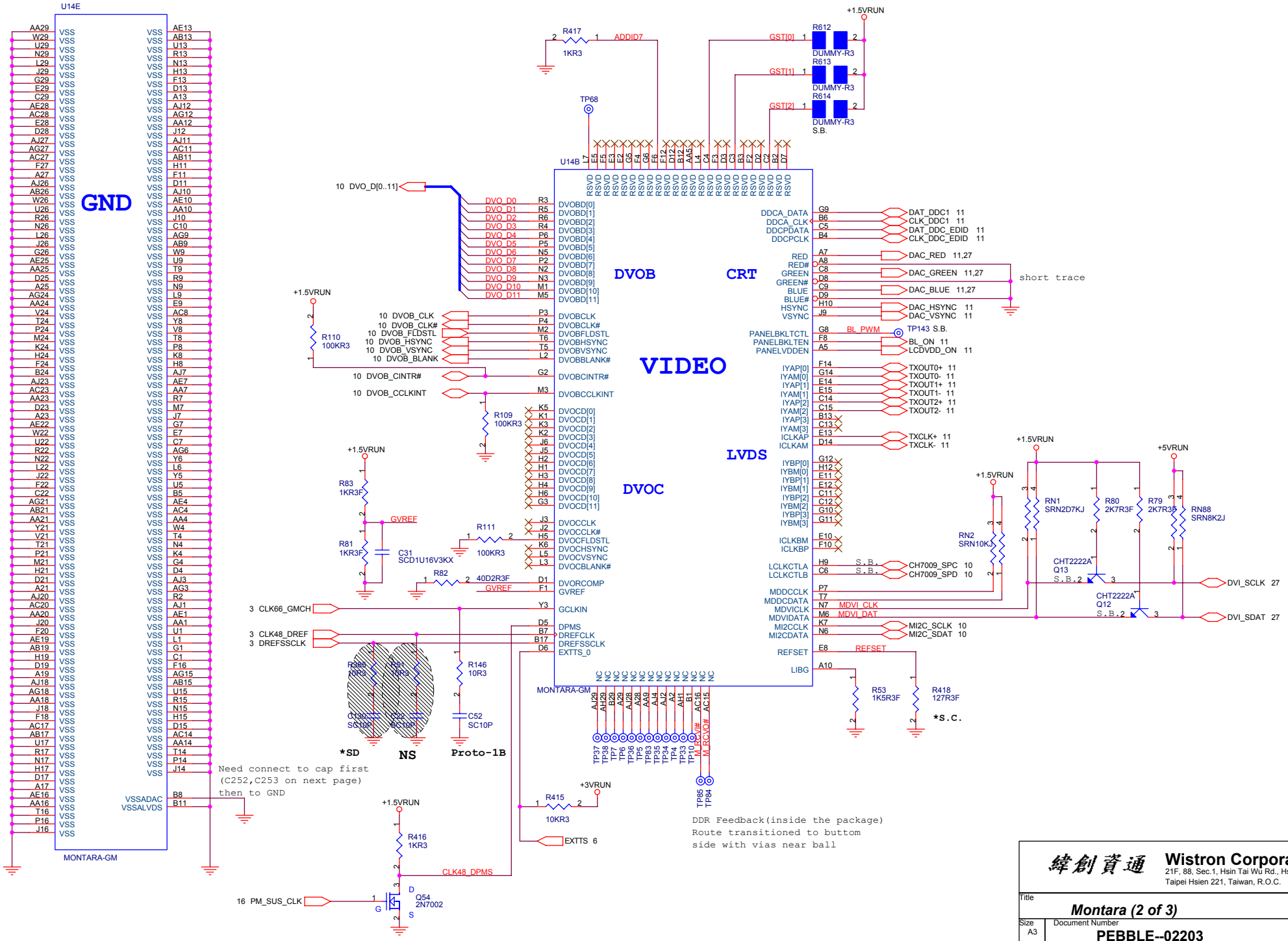


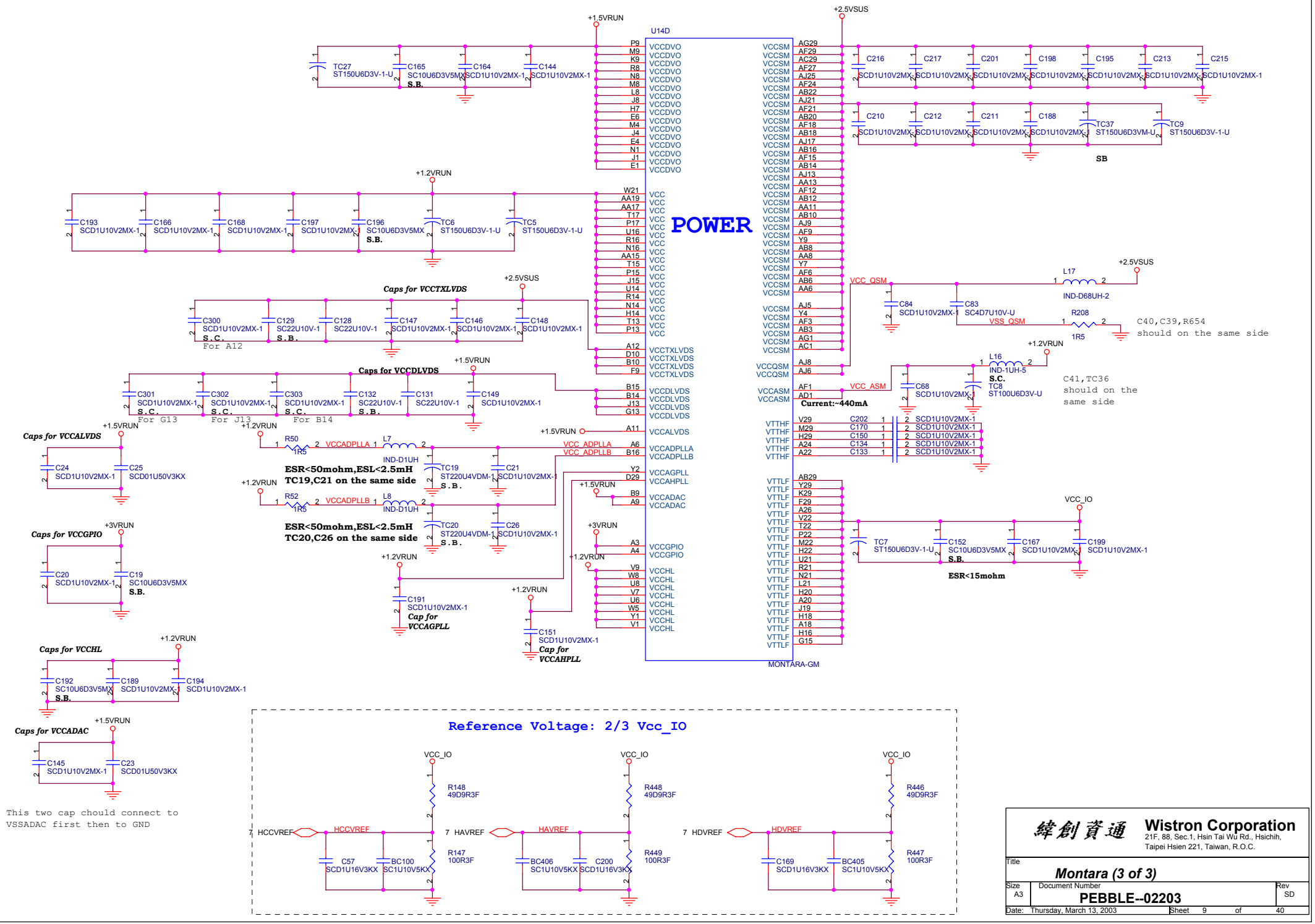
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

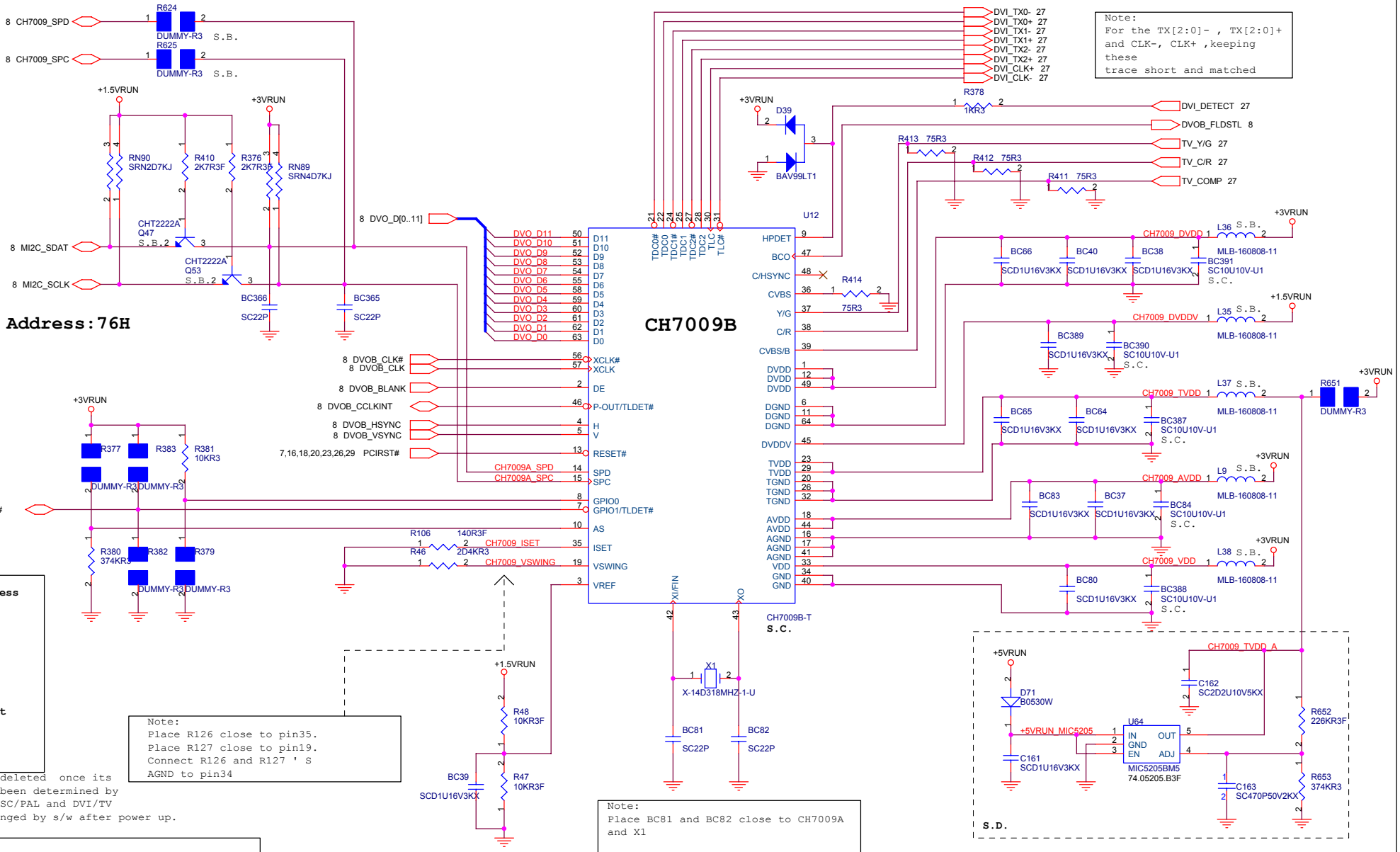
Title: *Montara (1 of 3)*

Size: A3 | Document Number: PEBBLE--02203 | Rev: SD

Date: Thursday, March 13, 2003 | Sheet 7 of 40


U14E
GND
MONTARA-GM
VSSADAC
VSSALVDS
U14B
VIDEO
DVOB
DVOC
CRT
LVDS
MONTARA-GM
10 DVO_D[0..11]
DVO_D0
DVO_D1
DVO_D2
DVO_D3
DVO_D4
DVO_D5
DVO_D6
DVO_D7
DVO_D8
DVO_D9
DVO_D10
DVO_D11
10 DVOB_CLK
10 DVOB_CLK#
10 DVOB_FLDSTL
10 DVOB_HSYNC
10 DVOB_VSYNC
10 DVOB_BLANK
10 DVOB_CINTR#
10 DVOB_CCLKINT
DDCA_DATA
DDCA_CLK
DDCPDATA
DDCPCLK
DAT_DDC1 11
CLK_DDC1 11
DAT_DDC_EDID 11
CLK_DDC_EDID 11
RED
RED#
GREEN
GREEN#
BLUE
BLUE#
HSYNC
VSYNC
DAC_RED 11,27
DAC_GREEN 11,27
DAC_BLUE 11,27
DAC_HSYNC 11
DAC_VSYNC 11
short trace
PANELBKLTCTL
PANELBKLTEN
PANELVDDEN
BL_PWM
TP143 S.B.
BL_ON 11
LCDVDD_ON 11
IYAP[0]
IYAM[0]
IYAP[1]
IYAM[1]
IYAP[2]
IYAM[2]
IYAP[3]
IYAM[3]
ICLKAP
ICLKAM
TXOUT0+ 11
TXOUT0- 11
TXOUT1+ 11
TXOUT1- 11
TXOUT2+ 11
TXOUT2- 11
TXCLK+ 11
TXCLK- 11
IYBP[0]
IYBM[0]
IYBP[1]
IYBM[1]
IYBP[2]
IYBM[2]
IYBP[3]
IYBM[3]
ICLKBM
ICLKBP
LCLKCTLA
LCLKCTLB
CH7009_SPC 10
CH7009_SPD 10
MDDCCLK
MDDCDATA
MDVICLK
MDVIDATA
MDVI_CLK
MDVI_DAT
MI2CCLK
MI2CDATA
MI2C_SCLK 10
MI2C_SDAT 10
REFSET
LIBG
3 CLK66_GMCH
3 CLK48_DREF
3 DREFSSCLK
GCLKIN
DPMS
DREFCLK
DREFSSCLK
EXTTS_0
EXTTS 6
16 PM_SUS_CLK
CLK48_DPMS
Q54 2N7002
DVI_SCLK 27
DVI_SDAT 27
Need connect to cap first
(C252,C253 on next page)
then to GND
*SD
NS
Proto-1B
*S.C.
DDR Feedback(inside the package)
Route transitioned to buttom
side with vias near ball
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Montara (2 of 3)
Size A3
Document Number PEBBLE--02203
Rev SD
Date: Thursday, March 13, 2003
Sheet 8 of 40


U14D
POWER
MONTARA-GM
+1.5VRUN
+2.5VSUS
+1.2VRUN
+3VRUN
+2.5VSUS
Caps for VCCTXLVDS
Caps for VCCDLVDS
Caps for VCCALVDS
Caps for VCCGPIO
Caps for VCCHL
Caps for VCCADAC
ESR<50mohm,ESL<2.5mH
TC19,C21 on the same side
ESR<50mohm,ESL<2.5mH
TC20,C26 on the same side
Cap for VCCAGPLL
Cap for VCCAHPLL
Current:~440mA
ESR<15mohm
SB
C40,C39,R654
should on the same side
C41,TC36
should on the
same side
This two cap chould connect to
VSSADAC first then to GND
Reference Voltage: 2/3 Vcc_IO
HCCVREF
HAVREF
HDVREF
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Montara (3 of 3)
PEBBLE--02203
Thursday, March 13, 2003
Sheet 9 of 40



緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

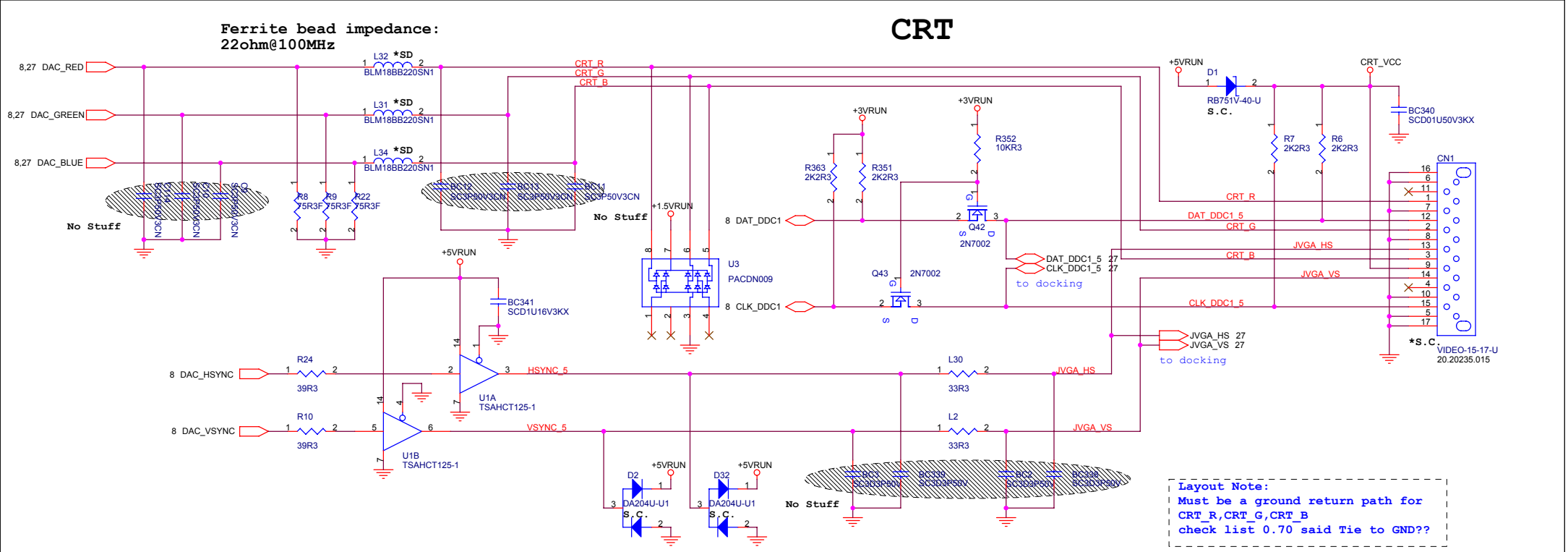
Title: **S-VIDEO/DVI**

Size	Document Number	Rev
A3	PEBBLE--02203	SD

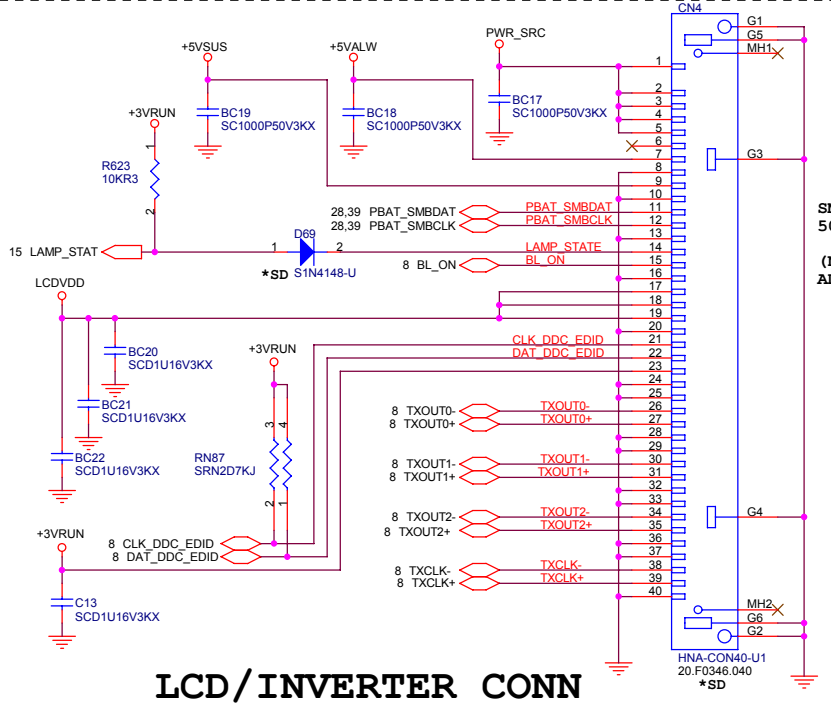
Date: Thursday, March 13, 2003 Sheet 10 of 40

CRT

Ferrite bead impedance:
22ohm@100MHz

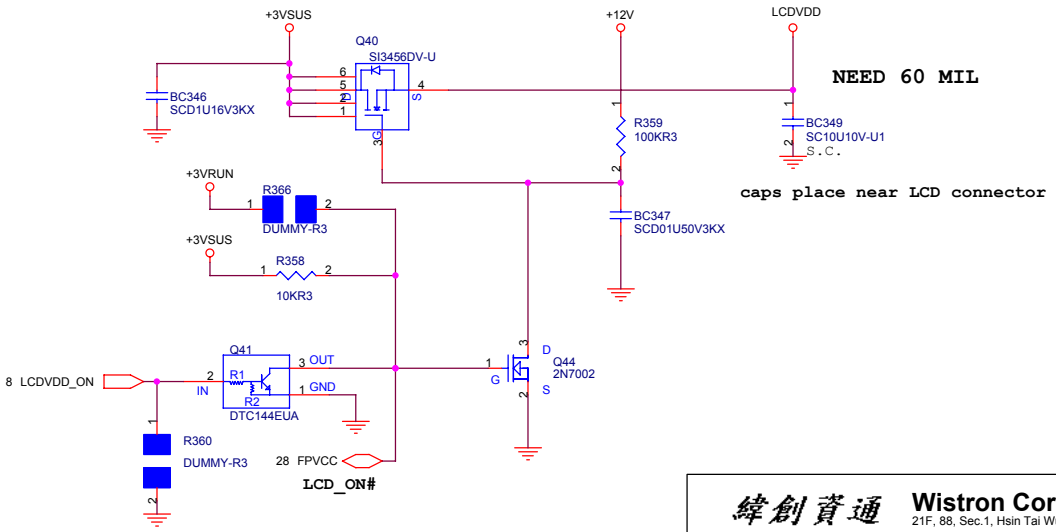


Layout Note:
Must be a ground return path for CRT_R,CRT_G,CRT_B
check list 0.70 said Tie to GND??



SMB ADDRESS 50h

(New) SMB ADDRESS 58h

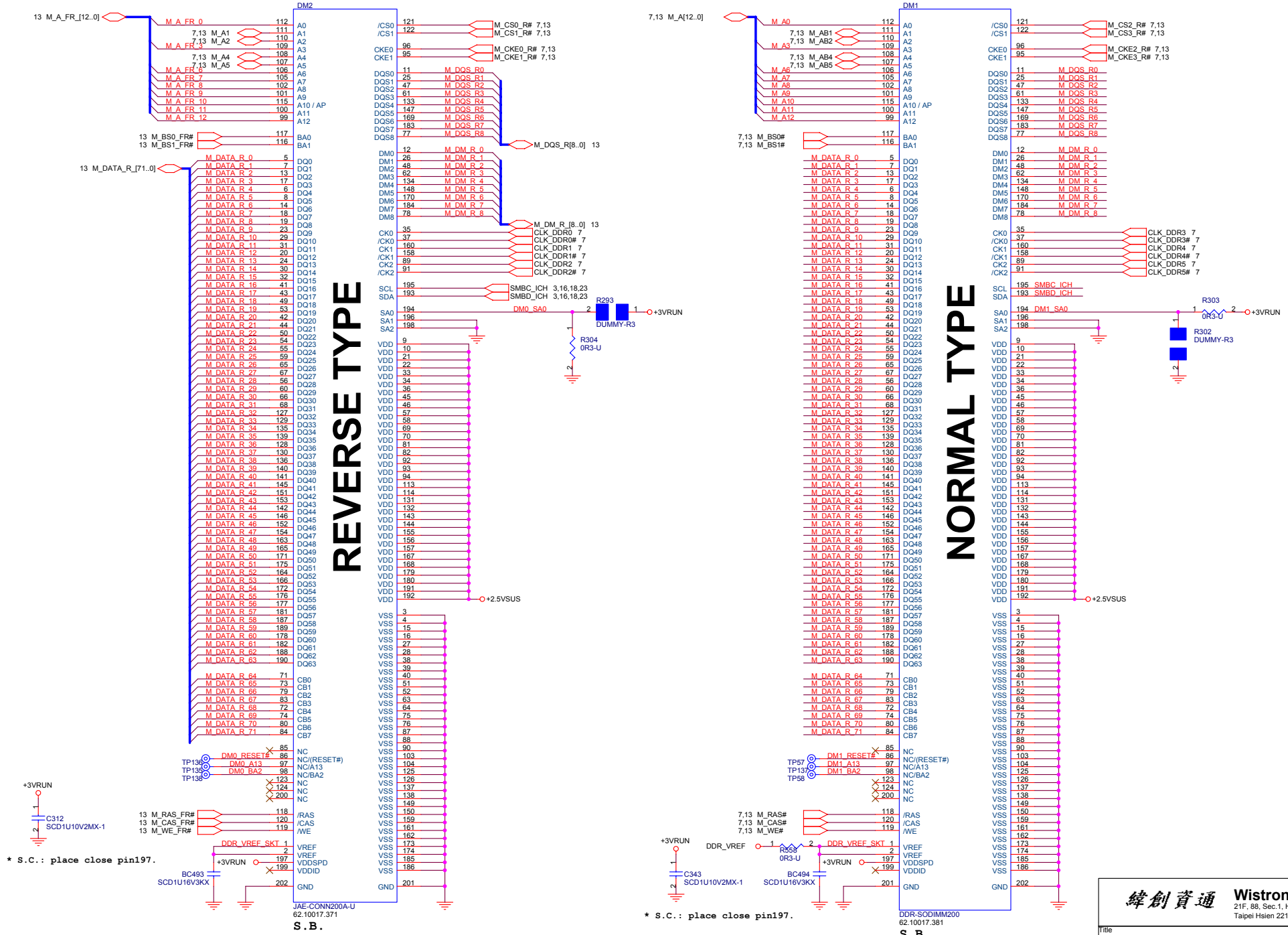


DIFFERENTIAL GND MUST LAY AROUND SIGNAL AND CAN'T USE THE SAME PATH WITH PWR GND

LCD/INVERTER CONN

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

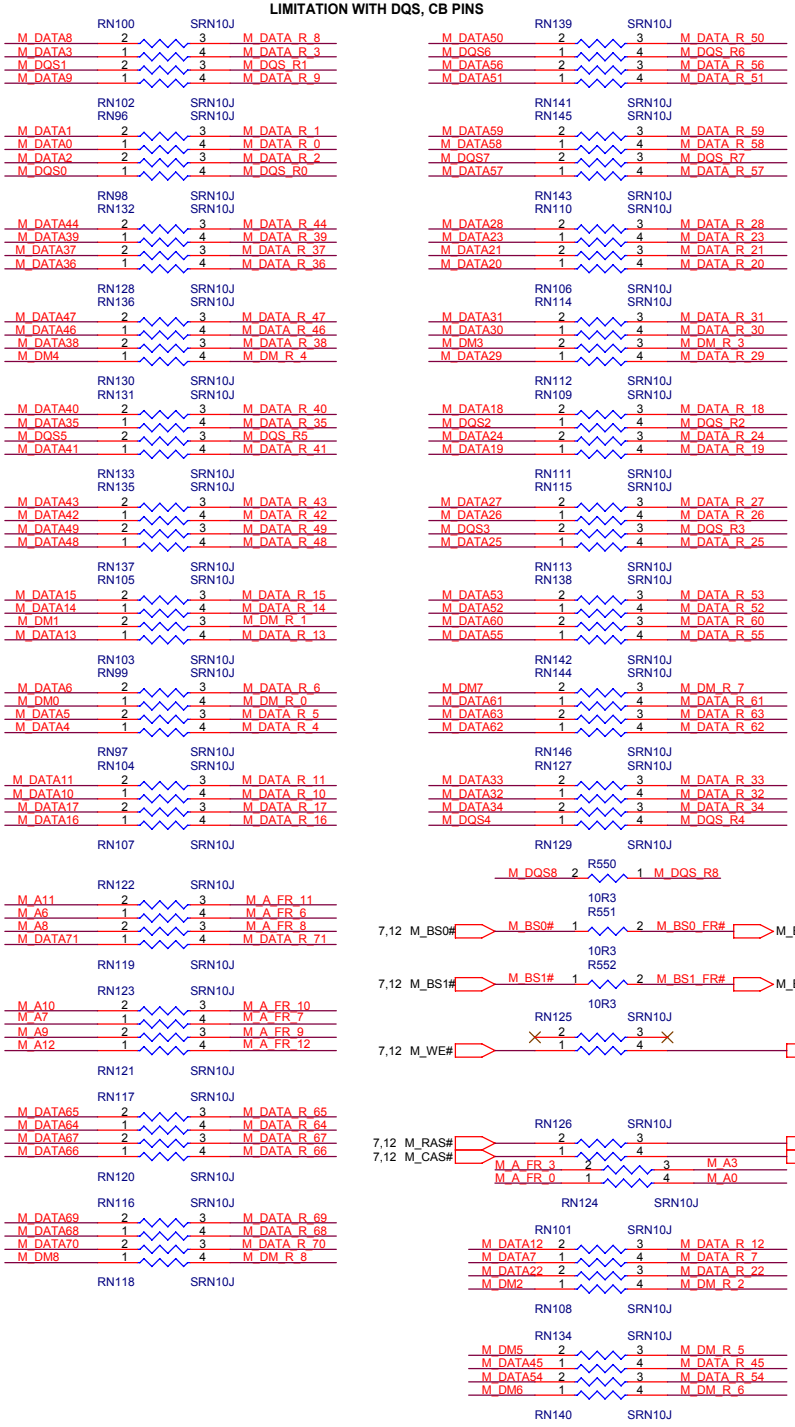
Title	LCD_INVERTER & CRT CONN.	
Size A3	Document Number PEBBLE--02203	Rev SD
Date: Thursday, March 13, 2003	Sheet 11 of 40	



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***DDR Socket***	
Size: Custom	Document Number: **PEBBLE--02203**	Rev: SD
Date: Thursday, March 13, 2003	Sheet 12 of 40	

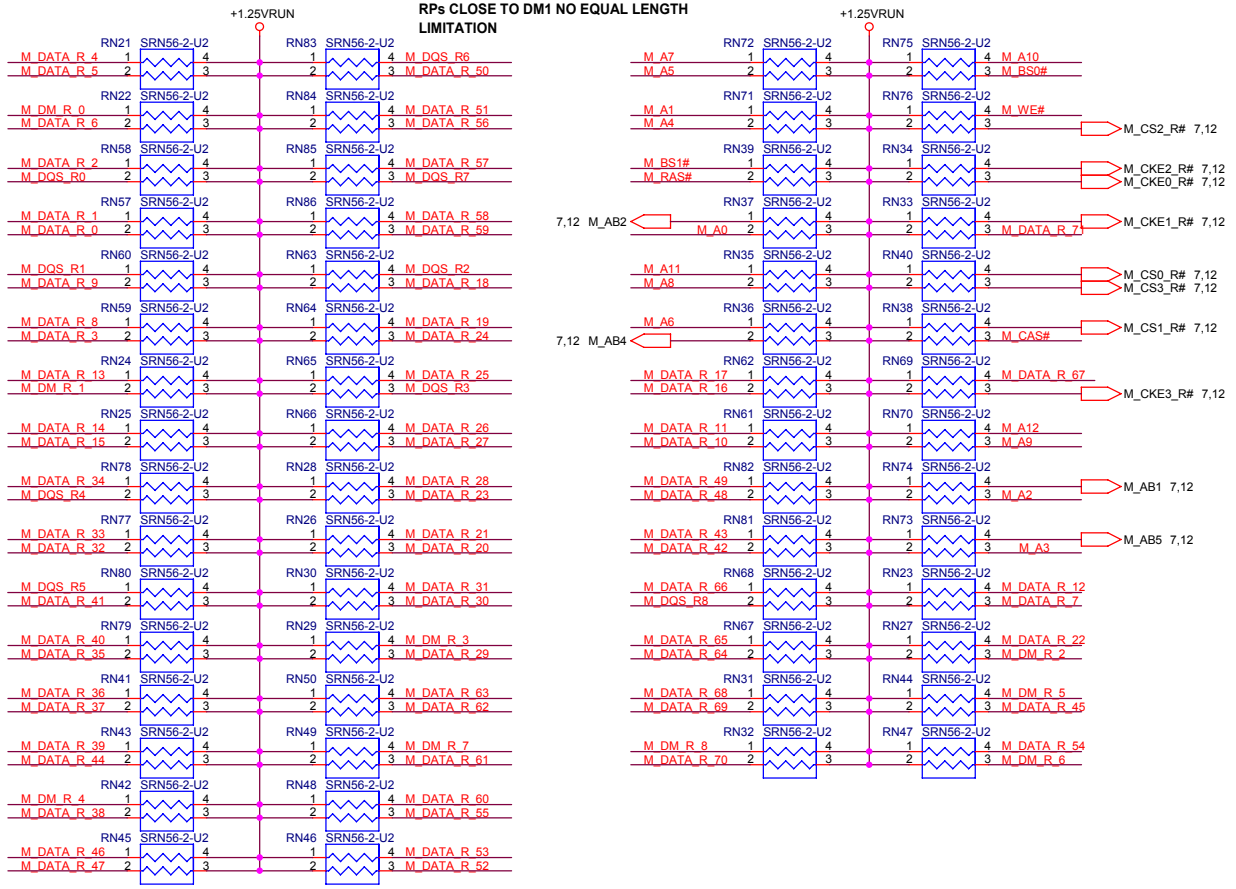
SERIES DAMPING

PLACE RNs CLOSE TO DM0, < 0.75"
STRICT EQUAL LENGTH
LIMITATION WITH DQS, CB PINS



PARALLEL TERMINATION

PULL HIGH STUBS < 0.8", Command <0.25",PLACE
RPs CLOSE TO DM1 NO EQUAL LENGTH
LIMITATION



Control signals use Topology 2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR Serial/Terminator Resistor***

Size	Document Number	Rev
A3	**PEBBLE--02203**	SD

Date: Thursday, March 13, 2003 Sheet 13 of 40

PLACE ONE 0.1 and ONE 0.01 CAP CLOSE TO EVERY 4
PULL-UP TERMINATION RESISTORS, CRB-P13
DATA(64)+ADD(13)+DQS(9)+CB(8)+CMD(13)=107
0.1UF 0402 X7R 59X

+1.25VRUN

BC227 SCD01U16V2KX
BC229 SCD01U16V2KX
BC231 SCD01U16V2KX
BC233 SCD01U16V2KX
BC235 SCD01U16V2KX
BC237 SCD01U16V2KX
BC239 SCD01U16V2KX
BC241 SCD01U16V2KX
BC243 SCD01U16V2KX
BC245 SCD01U16V2KX
BC247 SCD01U16V2KX
BC249 SCD01U16V2KX

BC251 SCD01U16V2KX
BC299 SCD01U16V2KX
BC301 SCD01U16V2KX
BC303 SCD01U16V2KX
BC305 SCD01U16V2KX
BC307 SCD01U16V2KX
BC309 SCD01U16V2KX
BC311 SCD01U16V2KX
BC313 SCD01U16V2KX
BC315 SCD01U16V2KX
BC317 SCD01U16V2KX
BC319 SCD01U16V2KX

BC321 SCD01U16V2KX
BC323 SCD01U16V2KX
BC325 SCD01U16V2KX
BC327 SCD01U16V2KX
BC329 SCD01U16V2KX
BC331 SCD01U16V2KX
BC226 SCD1U10V2MX-1
BC228 SCD1U10V2MX-1
BC230 SCD1U10V2MX-1
BC232 SCD1U10V2MX-1
BC234 SCD1U10V2MX-1

BC236 SCD1U10V2MX-1
BC238 SCD1U10V2MX-1
BC240 SCD1U10V2MX-1
BC242 SCD1U10V2MX-1
BC244 SCD1U10V2MX-1
BC246 SCD1U10V2MX-1
BC248 SCD1U10V2MX-1
BC250 SCD1U10V2MX-1
BC300 SCD1U10V2MX-1
BC302 SCD1U10V2MX-1
BC304 SCD1U10V2MX-1
BC306 SCD1U10V2MX-1

BC308 SCD1U10V2MX-1
BC310 SCD1U10V2MX-1
BC312 SCD1U10V2MX-1
BC314 SCD1U10V2MX-1
BC316 SCD1U10V2MX-1
BC318 SCD1U10V2MX-1
BC320 SCD1U10V2MX-1
BC322 SCD1U10V2MX-1
BC324 SCD1U10V2MX-1
BC326 SCD1U10V2MX-1
BC328 SCD1U10V2MX-1
BC330 SCD1U10V2MX-1

PLACE CAPS BETWEEN AND NEAR DDR SKTS
PLACE EACH 0.1UF CAP CLOSE TO POWER PIN

+2.5VSUS

BC495 SCD1U10V2MX-1
BC496 SCD1U10V2MX-1
BC497 SCD1U10V2MX-1
BC498 SCD1U10V2MX-1
BC499 SCD1U10V2MX-1
BC500 SCD1U10V2MX-1
BC501 SCD1U10V2MX-1
BC502 SCD1U10V2MX-1

BC276 SCD1U10V2MX-1
BC277 SCD1U10V2MX-1
BC278 SCD1U10V2MX-1
BC279 SCD1U10V2MX-1
BC280 SCD1U10V2MX-1
BC281 SCD1U10V2MX-1
BC282 SCD1U10V2MX-1
BC283 SCD1U10V2MX-1

BC284 SCD1U10V2MX-1
C242 SCD1U10V2MX-1
C243 SCD1U10V2MX-1
C244 SCD1U10V2MX-1
C245 SCD1U10V2MX-1
C246 SCD1U10V2MX-1
C247 SCD1U10V2MX-1
C248 SCD1U10V2MX-1

S.C.

C313 SCD1U10V2MX-1
C314 SCD1U10V2MX-1
C318 SCD1U10V2MX-1
C319 SCD1U10V2MX-1
C321 SCD1U10V2MX-1

C254 SCD1U10V2MX-1
C255 SCD1U10V2MX-1
C256 SCD1U10V2MX-1
C257 SCD1U10V2MX-1
C258 SCD1U10V2MX-1
C259 SCD1U10V2MX-1
C286 SCD1U10V2MX-1

S.B

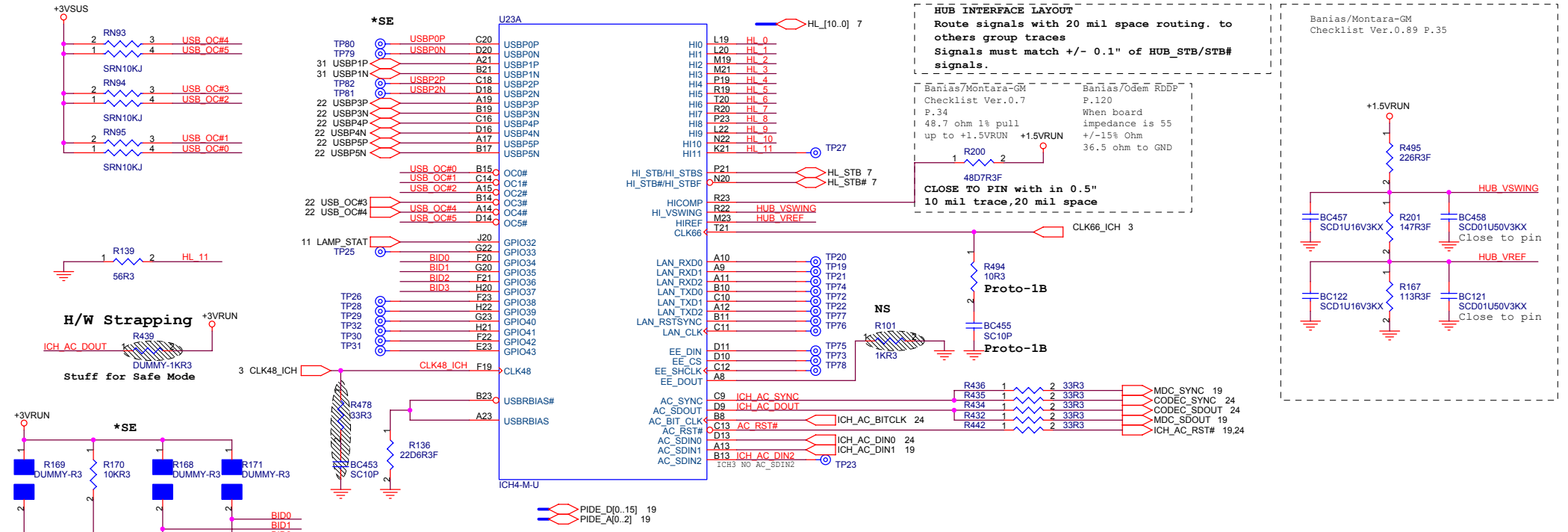
BC213 SC10U10V-U1
TC10 ST150U6D3V-1-U
TC45 ST150U6D3V-1-U
S.C.

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR Decoupling CPA***

Size	Document Number	Rev
A3	PEBBLE--02203	SD

Date: Thursday, March 13, 2003 Sheet 14 of 40



ICH4 Integrated Pull-up and Pull-down Resistors

ICH4 EDS 10429 4.2

EE_DIN, EE_DOUT, PME#, PWRBTN# GNT[B:A]#/GNT[5]#/GPIO[17:16], LAD[3:0]#/FWH[3:0]#, LDRQ[1:0],	ICH4 internal 20K pull-ups
LAN_RXD[2:0]	ICH4 internal 10K pull-ups
AC_BITCLK, AC_RST#, AC_SDIN[2:0], AC_SDOUT, AC_SYNC, DPRSLPVR, SPKR	ICH4 internal 20K pull-downs
USB[5:0][P,N]	ICH4 internal 15K pull-downs
PDD[7]/SDD[7], PDDREQ / SDDREQ	ICH4 internal 11.5K pull-downs
LANCLK	ICH4 internal 100K pull-downs

ICH4 IDE Integrated Series Termination Resistors

PDD[15:0],SDD[15:0],PDIOW#,SDIOW#, PDIOR#,PDIOW#,PDREQ,SDREQ, PDDACK#, SDDACK#, PIORDY,SIORDY, PDA[2:0],SDA[2:0], PDCS1#,SDCS1#, PDCS3#,SDCS3#,IRQ14,IRQ15,	approximately 33 ohm

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH4-M (1 of 3)

Size: A3 | Document Number: PEBBLE--02203 | Rev: SE

Date: Thursday, March 13, 2003 | Sheet 15 of 40

PCI/Interrupt I/F Pullups

RP2 SRP8K2-1: P_REQ#0, P_TRDY#, P_FRAME#, P_SERR# → P_PLOCK#, P_DEVSEL#, P_PERR#, P_IRDY#
RP3 SRP8K2-1: P_STOP#, P_REQ#2 → PIRQB#, PIRQA#, P_REQ#1, GPIO7
RP1 SRP8K2-1: SERIRQ, PCIRST#, PIRQD#, PIRQC# → P_REQ#3, P_REQB#, P_REQ#4, P_REQA#
RN92 SRN8K2J: ICH_GPIO2, ICH_GPIO3
RN91 SRN8K2J: ICH_GPIO4, ICH_GPIO5
RN4 SRN10KJ: SYS_RESET#, BATLOW#

REQ4:Broadcom LAN
REQ3:Mini PCI
REQ2:USB 2.0(No on Pebble)
REQ1:Card Bus
REQ0:Docking
REQB:PCI4515 ???

P_AD[31..0] 18,20,23,26
P_C/BE#[3..0] 18,20,23,26

U23D (ICH4-M-U): PIRQA#, PIRQB#, PIRQC#, PIRQD#, PIRQE#/GPIO2, PIRQF#/GPIO3, PIRQG#/GPIO4, PIRQH#/GPIO5; REQ4#, REQ3#, REQ2#, REQ1#, REQ0#, REQB#/REQ5#/GPIO1, REQA#/GPIO0; GNT4#, GNT3#, GNT2#, GNT1#, GNT0#, GNTB#/GNT5#/GPIO17, GNTA#/GPIO16; FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, PAR, PERR#, PLOCK#, SERR#, PME#, PCIRST#, PCICLK; AD31–AD0, C/BE3#–C/BE0#

R493 10R3, BC443 SC10P

BIOS NOTE:
BIOS should disable PM_STPCPU# on CK_Titan.
(Use H_DPSLP# instead)

U23B (ICH4-M-U): APICCLK, APICD0, APICD1; STPCLK#, A20M#, CPUSLP#, CPUPWRGD, INTR, NMI, SMI#, IGNEE#, A20GATE, RCIN#, FERR#, INIT#; SERIRQ; LFRAME#/FWH4, LDRQ0#, LDRQ1#; LAD0/FWH0, LAD1/FWH1, LAD2/FWH2, LAD3/FWH3; SUSCLK; INTRUDER#, RTCRST#, PWROK, RSMRST#, VCCRTC, VBIAS, RTCX1, RTCX2; DPRSLPVR, DPSLP#; AGPBUSY#/GPIO6, GPIO7, GPIO8; GPIO12, GPIO13; STP_PCI#/GPIO18, SLP_S1#/GPIO19, STP_CPU#/GPIO20, C3_STAT#/GPIO21, CPUPERF#/GPIO22, SSMUXSEL/GPIO23, CLKRUN#/GPIO24, GPIO25, GPIO27, GPIO28; SLP_S3#, SLP_S4#, SLP_S5#, RI#; PWRBTN#, SYS_RESET#, LAN_RST#, BATLOW#/TP0, SUS_STAT#/LPCPD#, VGATE/VRMPWRGD, THRMTRIP#, THRM#; SMLINK0, SMLINK1, SMBDATA, SMBCLK, SMBALERT#/GPIO11; SPKR; CLK14

TP104, R497 10KR3, R496 10KR3, R255 56R3, R254 56R3, R514 100KR3, R176 0R3-U

CLK termination close to ICH4

R138 33R3, BC99 SC10P

RTC Circuitry

VCC_RTC, +3VALW, +3.3VRTC
D54 RB751V-40-U S.C., R536 1KR3
BC481 SC1U10V5KX
LAYOUT: MAKE PAD ACCESSABLE
RTCRST#, R537 180KR3, D53 RB751V-40-U S.C.
GP8 GAP-OPEN, BC480 SCD1U16V3KX
RTCRST# delay 18~25ms
BC181 SCD047U25V3KX
ICH_VBIAS
R252 10MR3, R251 10MR3
RTCX1, RTCX2
BC179 SC3P50V3CN, BC180 SC3P50V3CN
X5 XTAL-32D768K-4P 82.30001.031

R539 0R3-U, PM_SLP_S1# → PM_SLP_S1# 3
U75 NC7S208 (VCC, GND)
PM_SLP_S1# G, PM_SLP_S3#
BC483 SCD01U16V3KX

R533 DUMMY-R3, SUSPWROK
R534 10KR3, R515 56R3, R516 56R3
VCC_IO
If ICH-4 LAN not used,10K ohm PD or connect directly to ----RSMRST#(SUSPWROK) But in Bon conncet to PWROK(DELAY_IMVP_PWRGD)
PM_THERMTRIP# 4
28,31 COM_RI0#
20 CBS_RI#
RN3 SRN10KJ, ICH_RI#
NO STUFF

RN10 SRN4D7KJ: SMBD_ICH, SMBC_ICH
SMB_ALERT#, R531 10KR3

R535 100KR3 DELAY_IMVP_PWRGD
R532 100KR3 SUSPWROK
LPC_LDRQ1# TP89
R197 8K2R3 THRM#
R250 10KR3 P_CLKRUN#
R196 10KR3 AGPBUSY#
R198 DUMMY-R3 ICH_PME#
TP70 P_GNT#4, TP24 P_GNT#0, TP71 P_GNTA#, TP69 P_GNTB#

Should go high no sooner than 10mS after both +3VRUN and +1.8VRUN have reach their nominal voltage

Should go high no sooner than 10mS after both +3VSUS and +1.8VSUS have reach their nominal voltage

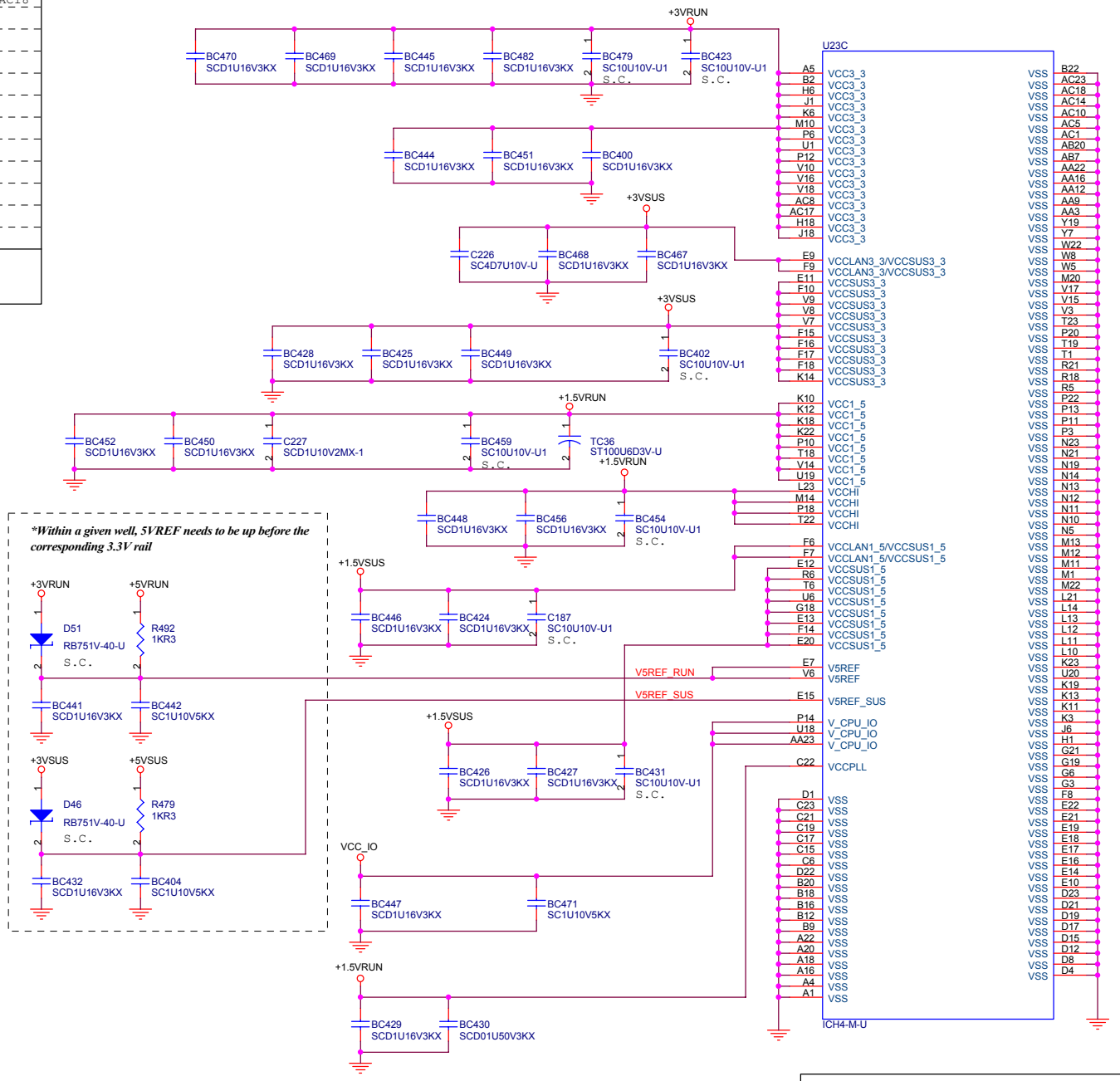
H/W Strapping
R477 DUMMY-1KR3 P_GNTA#
Stuff for A16 Swap Override

H/W Strapping
R137 DUMMY-1KR3 ICH_SPKR, +3VRUN
Stuff for No Reboot

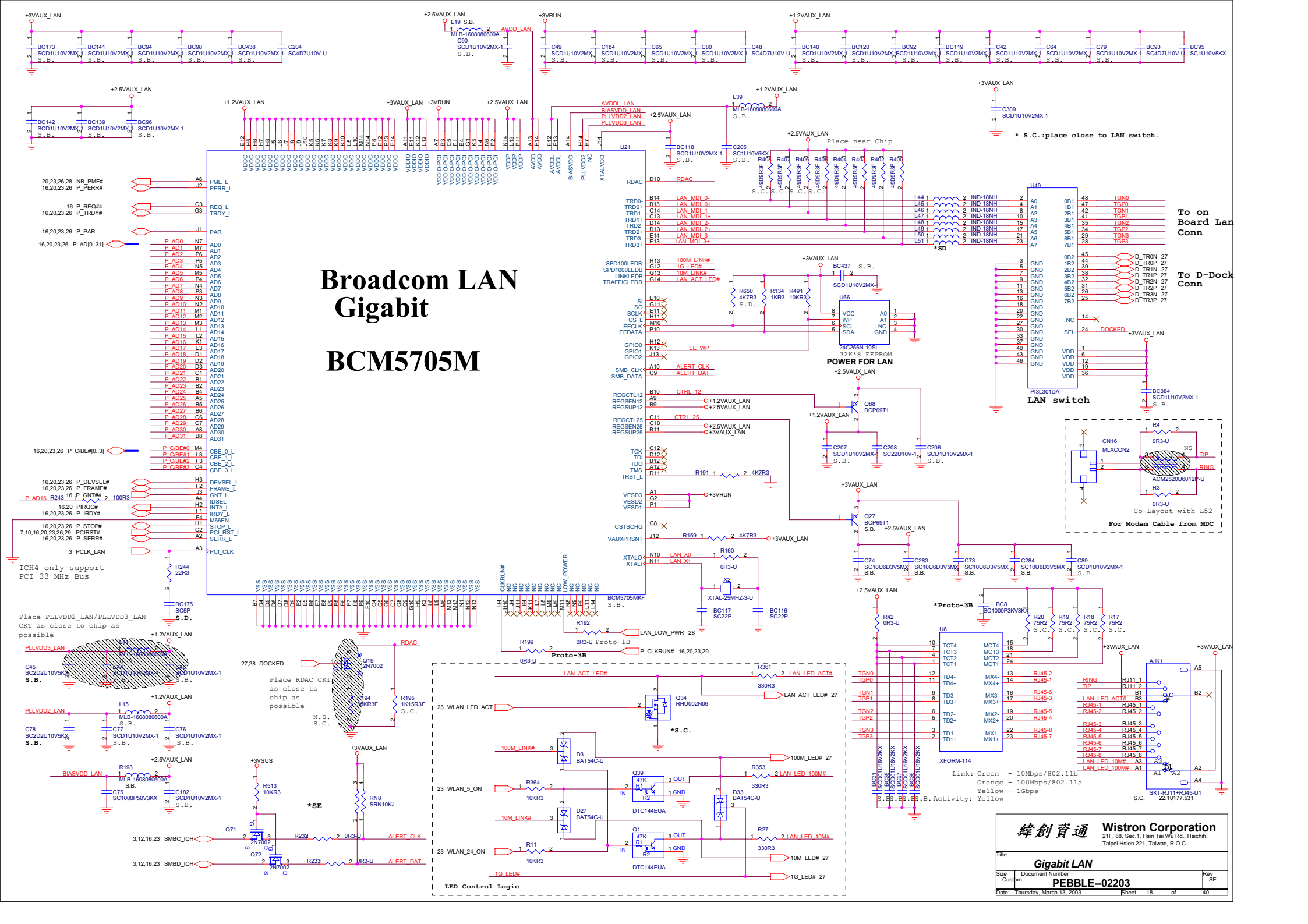
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH4-M (2 of 3)
Size: Custom | Document Number: PEBBLE--02203 | Rev: SD
Date: Thursday, March 13, 2003 | Sheet 16 of 40

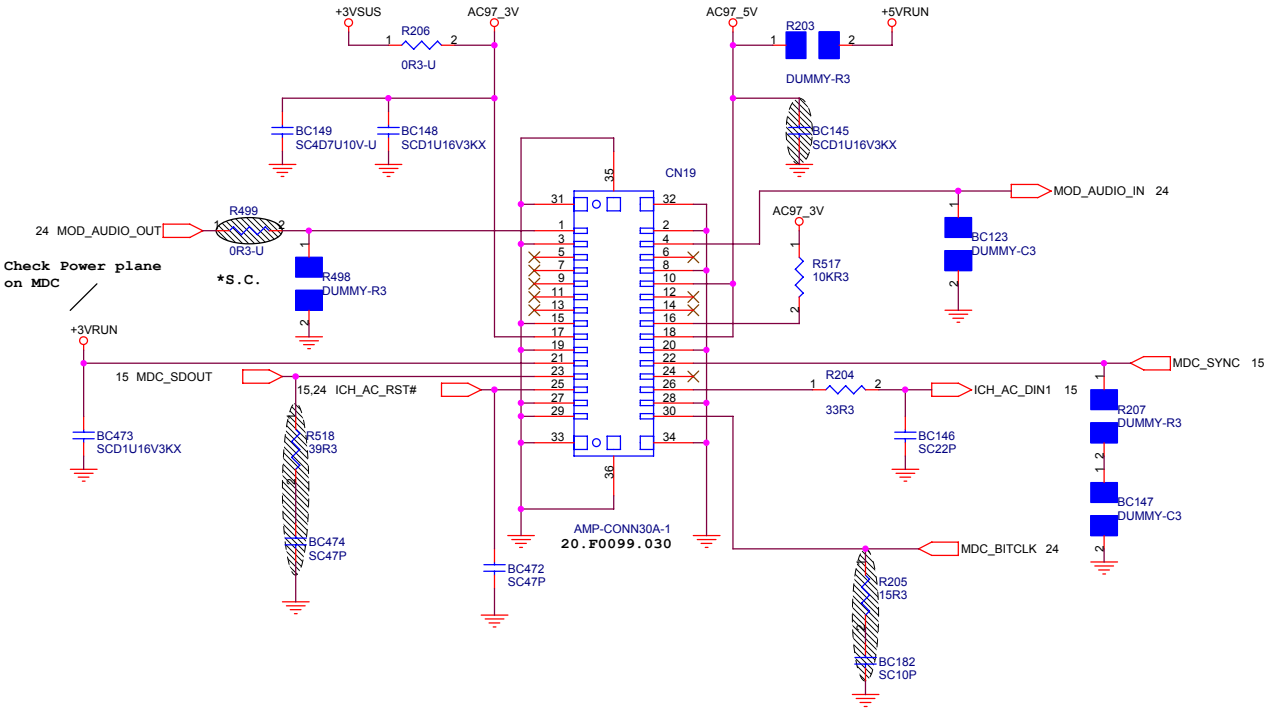
		Near Balls
3.3VRUN	22uF*2,0.1uF*9	0.1uF*6	A1,A4,H1,T1,AC10,AC18
1.5VRUN	100uF*1,22uF*1,0.1uF*4	0.1uF*2	K23,C23
3.3VSUS	22uF*1,0.1uF*4	0.1uF*2	A22,AC5
1.5VSUS	10uF*1,0.1uF*3	0.1uF*2	A16,AC1
1.8VRUN	22uF*1,0.1uF*2	0.1uF*2	T23,N23
VCC_IO	1uF*1,0.1uF*2	0.1uF*1	AA23
3.3VLAN	22uF*1,4.7uF*1,0.1uF*2	0.1uF*2	E9,F9
1.5VLAN	22uF*1,0.1uF*2	0.1uF*2	F6,F7
VCCPLL	0.1uF*1,0.01uF*1	0.1uF*1	C22
VCC5REF		0.1uF*1	E7
VCC5REFSUS		0.1uF*1	A16
VCCRTC		0.1uF*1	AB5
	Intel ERB Ver.0.5 p17	Intel MGM Checklist Ver.0.7 p41



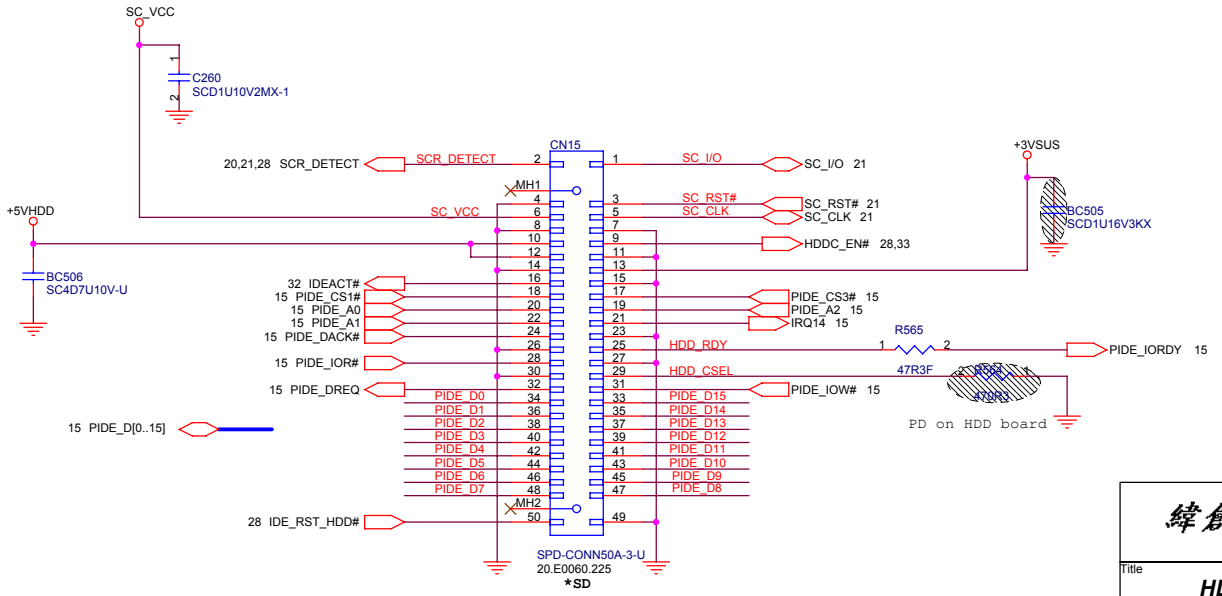
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***ICH4-M (3 of 3)***	
Size A3	Document Number **PEBBLE--02203**	Rev SD
Date: Thursday, March 13, 2003	Sheet 17 of 40	


Broadcom LAN
Gigabit
BCM5705M
ICH4 only support
PCI 33 MHz Bus
POWER FOR LAN
LAN switch
To on
Board Lan
Conn
To D-Dock
Conn
Place near Chip
Place PLLVDD2_LAN/PLLVDD3_LAN
CKT as close to chip as
possible
Place RDAC CKT
as close to
chip as
possible
*SE
*SD
*Proto-3B
Proto-3B
LED Control Logic
Co-Layout with L52
For Modem Cable from MDC
* S.C.:place close to LAN switch.
Link: Green - 10Mbps/802.11b
Orange - 100Mbps/802.11a
Yellow - 1Gbps
Activity: Yellow
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Gigabit LAN
PEBBLE--02203
Date: Thursday, March 13, 2003
Sheet 18 of 40

Modem Connector

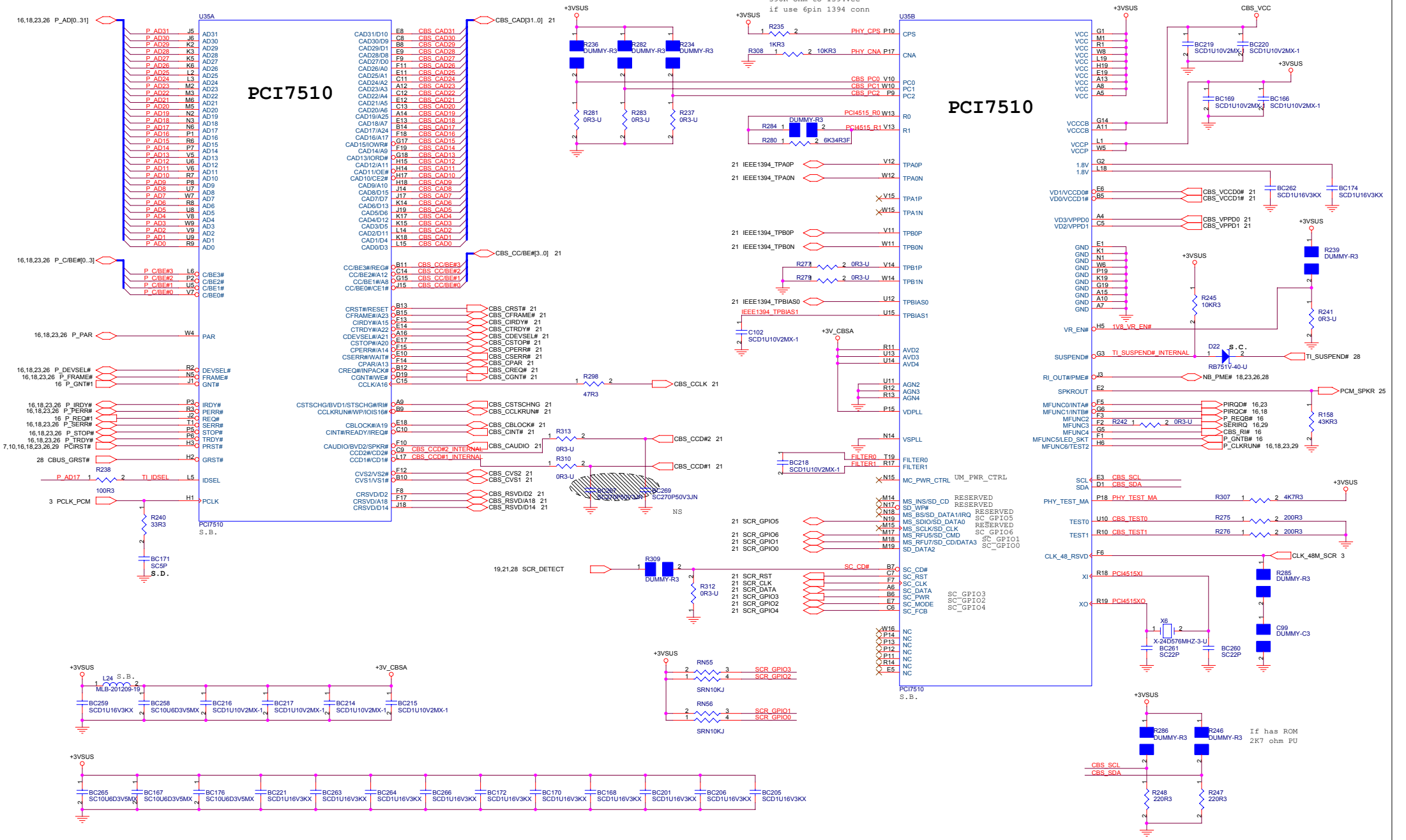


HDD & SMART CARD CONNECTOR



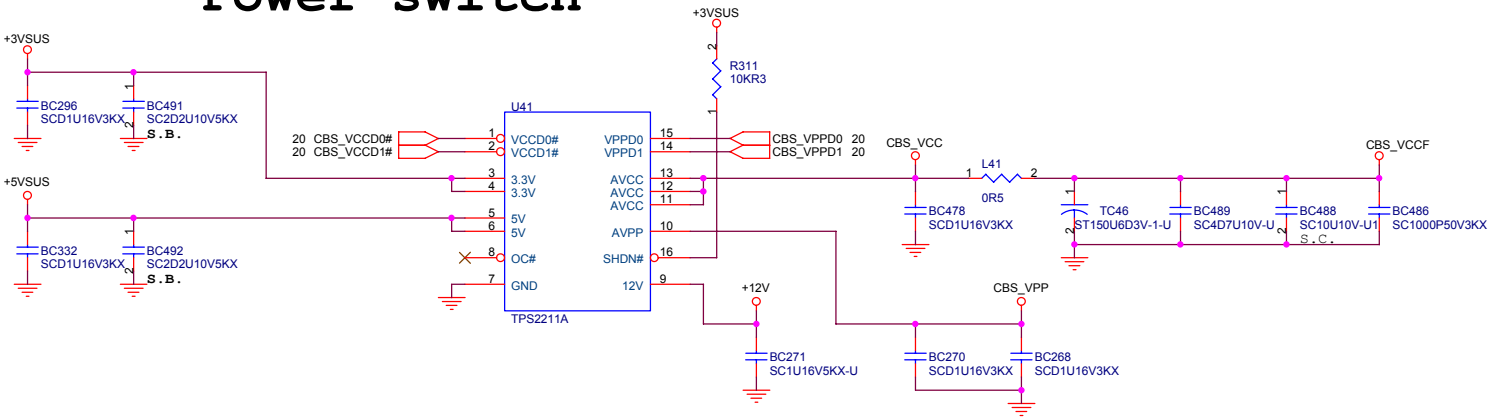
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***HDD & MDC CONN.***	
Size A3	Document Number **PEBBLE--02203**	Rev SD
Date: Thursday, March 13, 2003	Sheet 19 of 40	

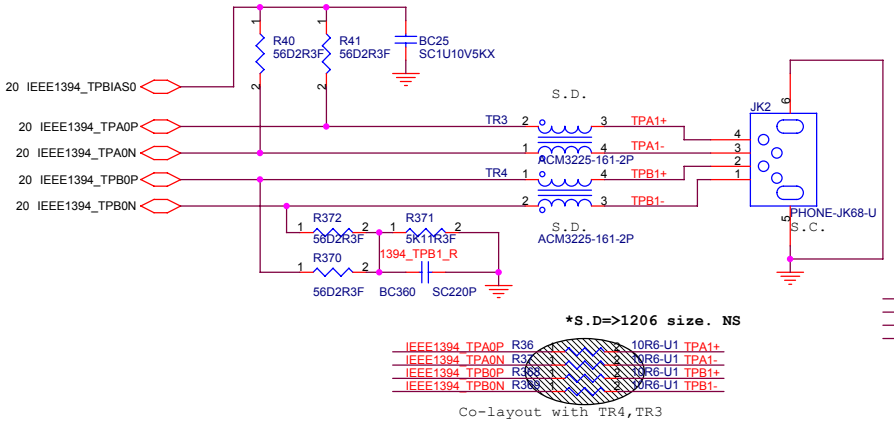


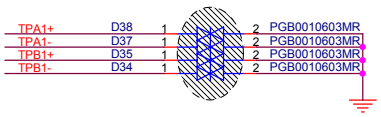
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CARDBUS CONTROLLER***	
Size: Custom	Document Number: **PEBBLE--02203**	Rev: SD
Date: Thursday, March 13, 2003	Sheet 20 of 40	

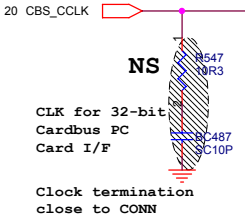
Power switch

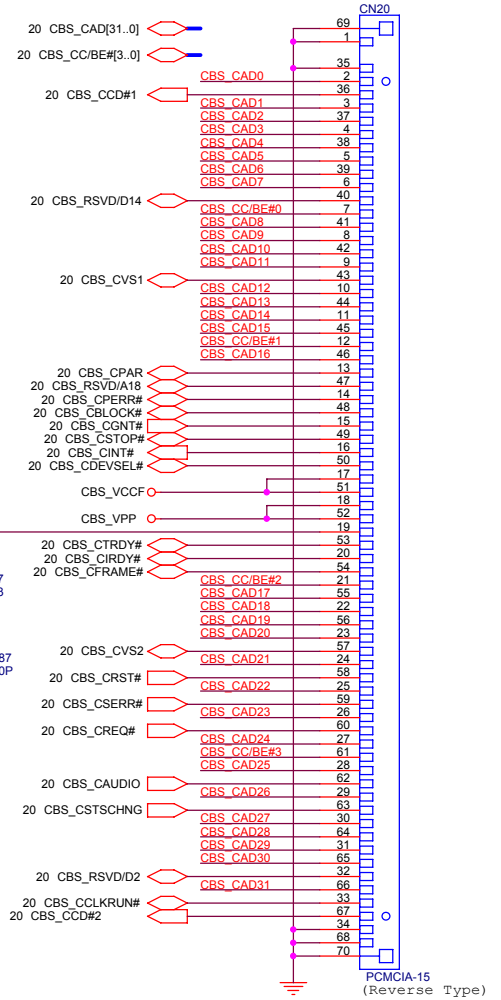


1394 conn.

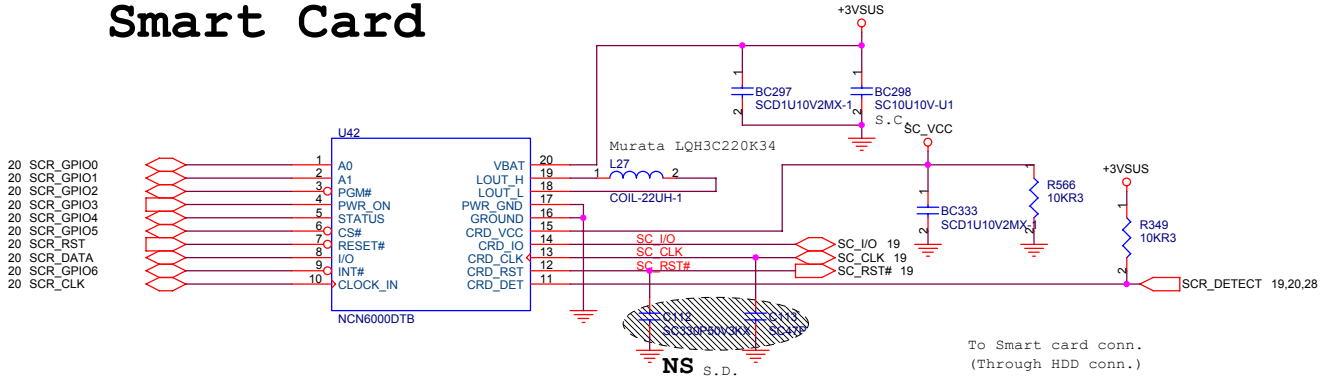


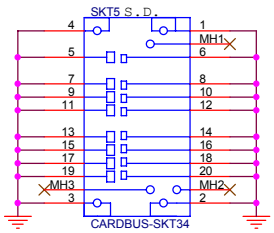






Smart Card





緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

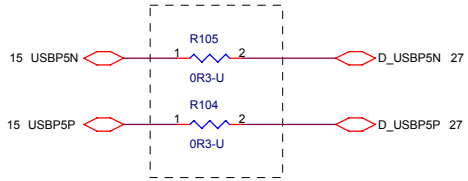
Title: ***CARDBUS CONNECTOR & POWER SWITCH***

Size	Document Number	Rev
A3	**PEBBLE--02203**	SD

Date: Thursday, March 13, 2003 Sheet 21 of 40

USB4

TO D DOCK

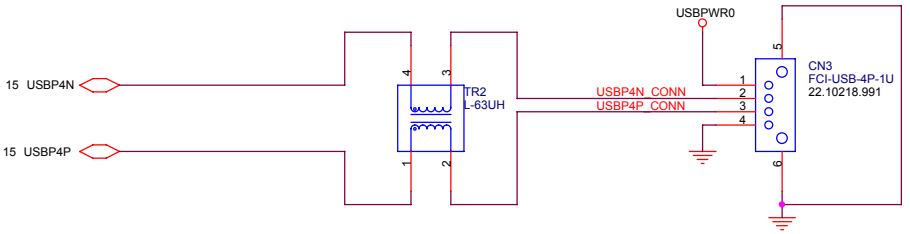


ICH4 provides an output driver impedance of 45 Ohm
and integrates 15K Ohm Pull-down R

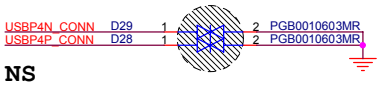
*SE

USB Port#	Destination
0	
1	BlueTooth
2	
3	Power USB
4	Rear
5	D-Dock

USB Common mode choke
MURATA PLW3216S900SQ2

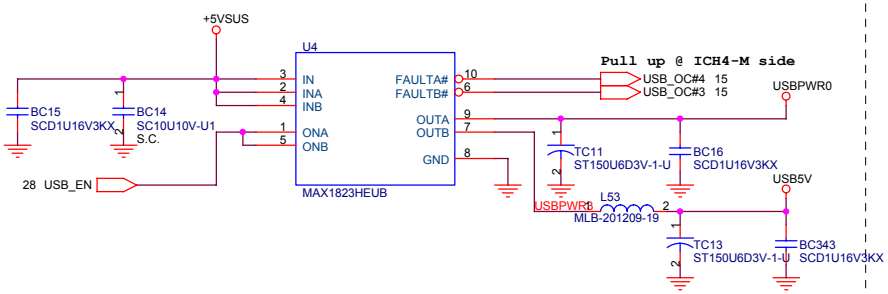


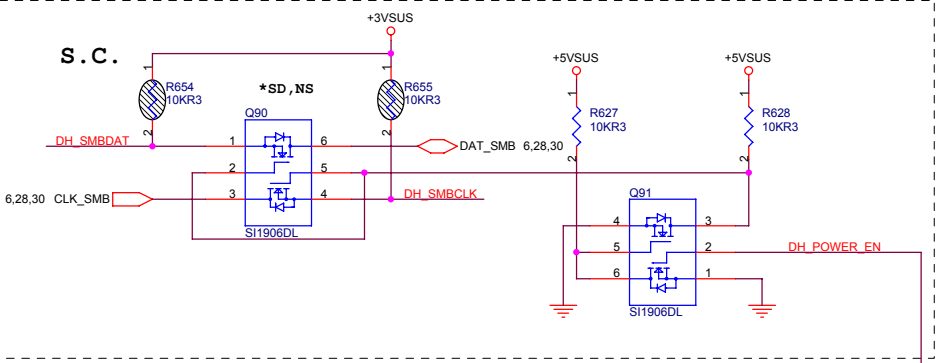
USB Common mode choke
MURATA PLW3216S900SQ2



NS
ESD suppressor
Place near
CN9&10

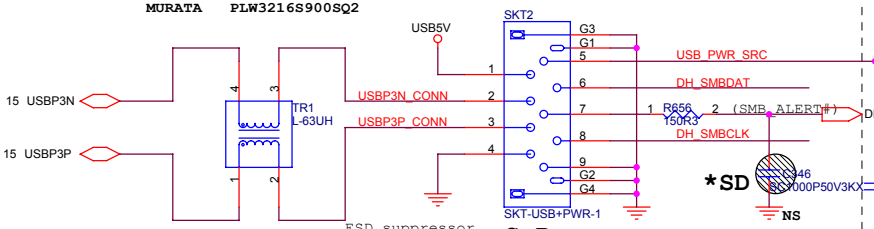
Dual USB switch for USB0/Power USB





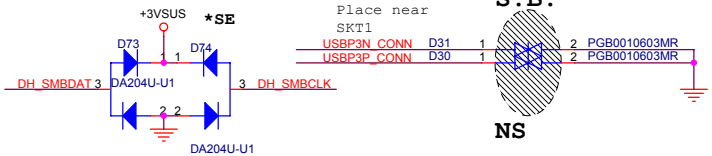
POWER USB

USB Common mode choke
MURATA PLW3216S900SQ2

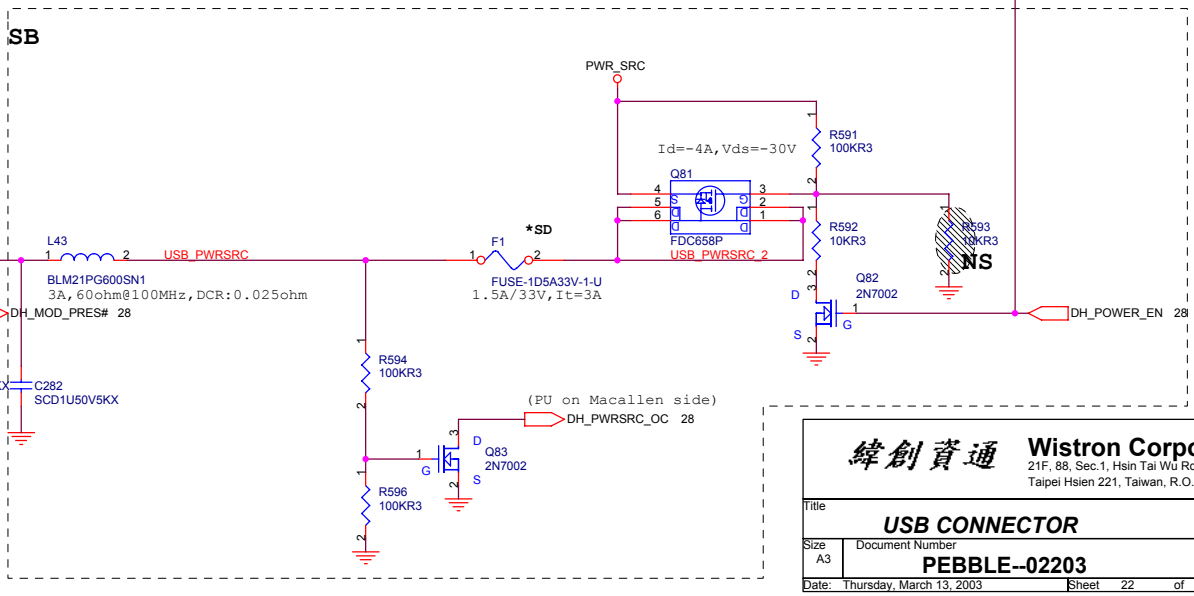


ESD suppressor
Place near
SKT1

S.B.



SB



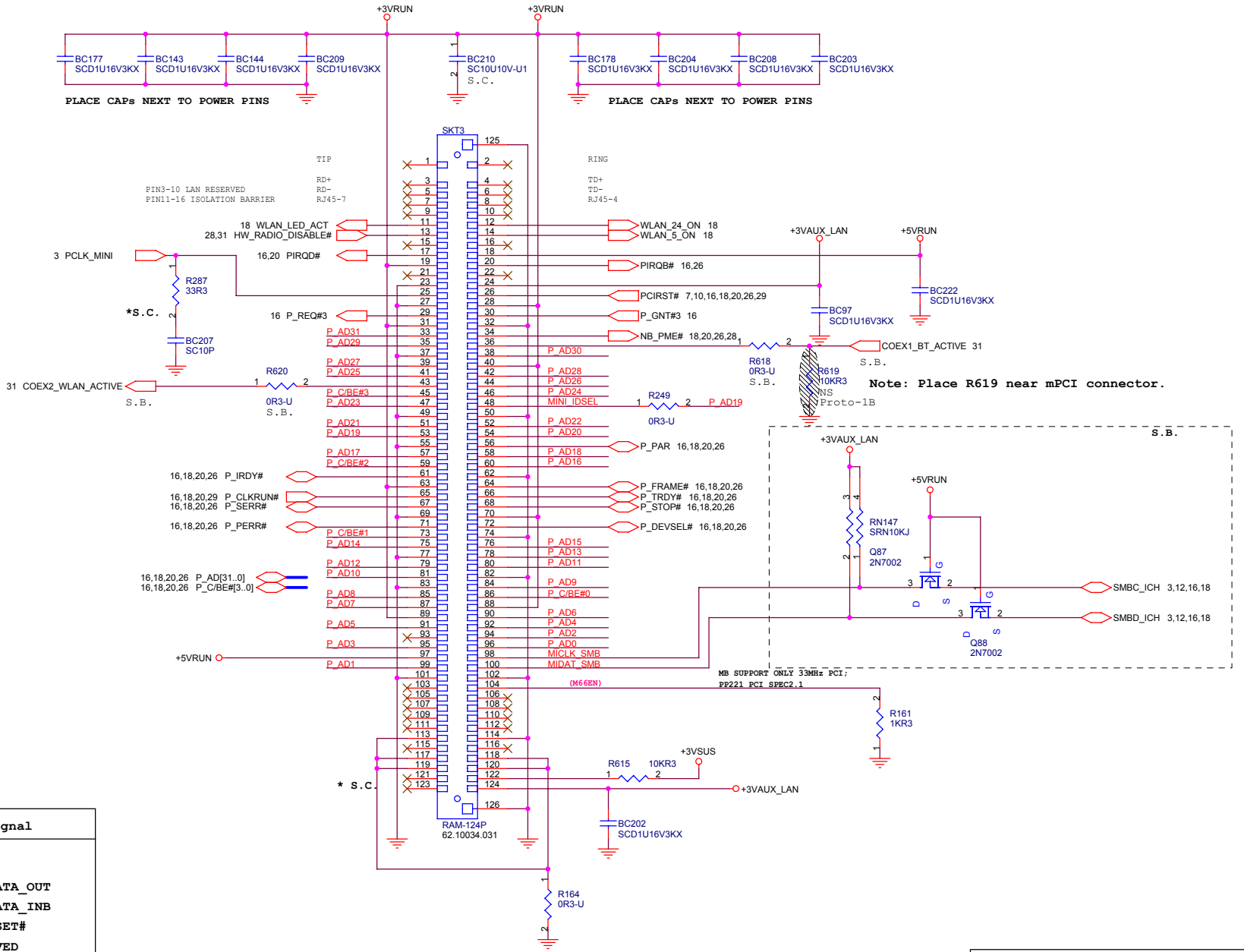
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB CONNECTOR

Size	Document Number	Rev
A3	PEBBLE--02203	SE

Date: Thursday, March 13, 2003 Sheet 22 of 40

MINIPCI SLOT



MINIPCI SPEC.

Pin#	Signal	Pin#	Signal
101	GND	102	GND
103	AC_SYNC	104	M66EN
105	AC_SDATA_INA	106	AC_SDATA_OUT
107	AC_BIT_CLK	108	AC_SDATA_INB
109	AC_PRIMARY#	110	AC_RESET#
111	MOD_AUDIO_MON	112	RESERVED
113	AUDIO_GND	114	GND
115	SYS_AUDIO_OUT	116	SYS_AUDIO_IN
117	SYS_AUDIO_OUT_GND	118	SYS_AUDIO_IN_GND
119	AUDIO_GND	120	AUDIO_GND
121		122	MPCIACT#
123	VCC5A	124	3.3VAUX

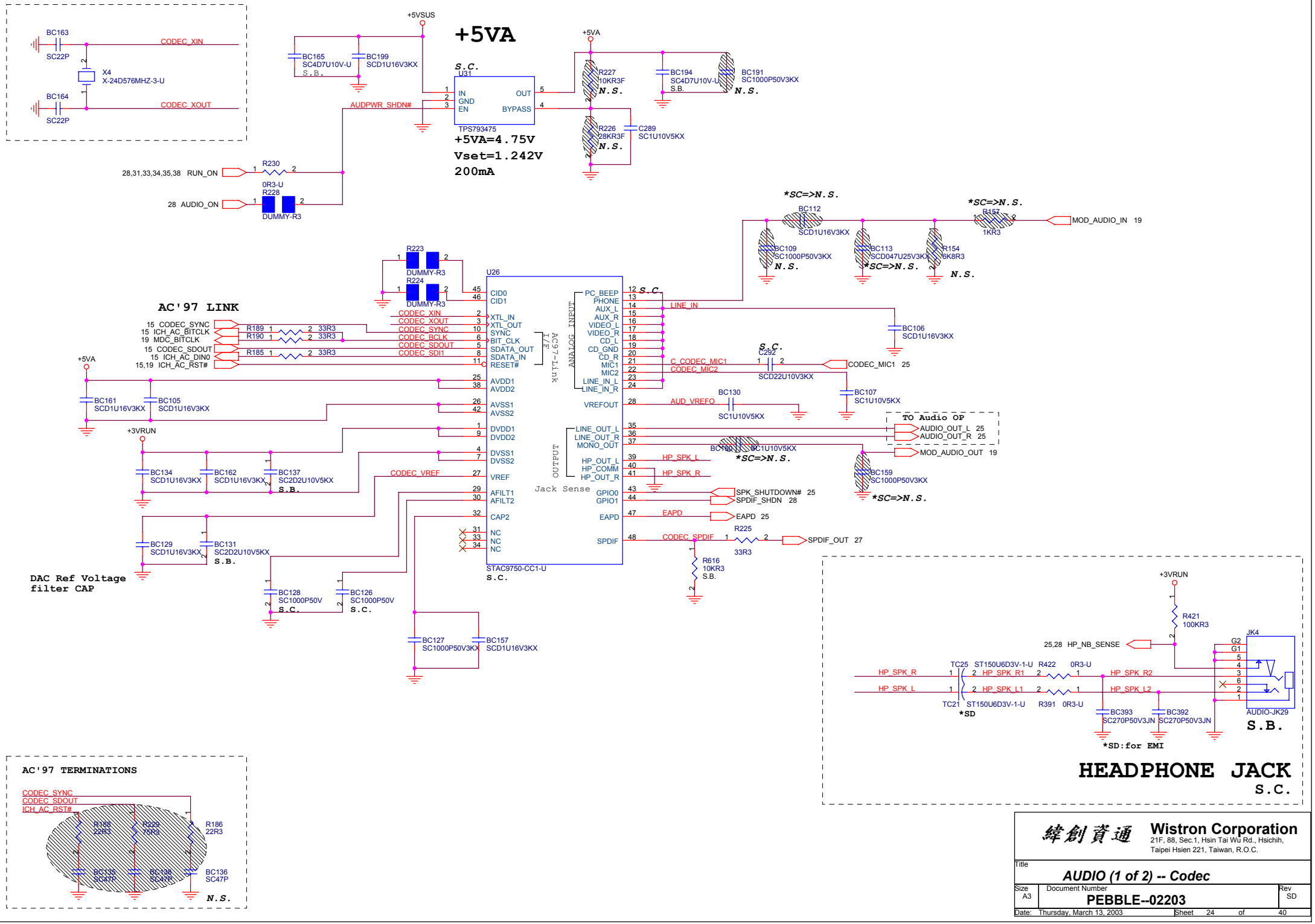
POWER REQUIREMENT TOTAL = 2W
+5VRUN = 100 mA
+3VAUX = 375 mAMPMAX

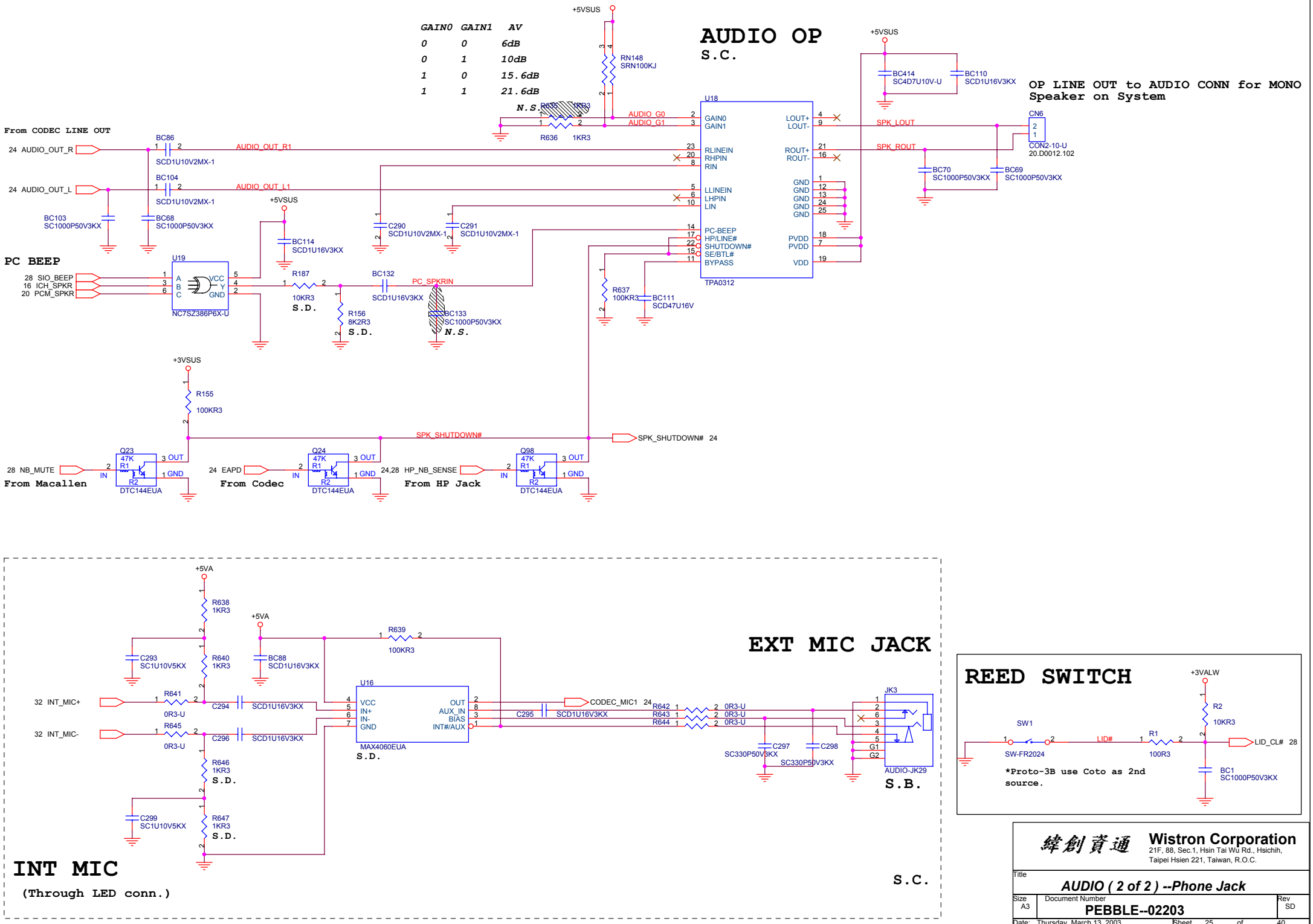
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Mini-PCI CONNECTOR

Size: A3 | Document Number: PEBBLE--02203 | Rev: SD

Date: Thursday, March 13, 2003 | Sheet 23 of 40


+5VA
S.C.
+5VA=4.75V
Vset=1.242V
200mA
TPS793475
AC'97 LINK
STAC9750-CC1-U
S.C.
Jack Sense
DAC Ref Voltage filter CAP
TO Audio OP
HEADPHONE JACK
S.C.
AC'97 TERMINATIONS
N.S.
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
AUDIO (1 of 2) -- Codec
PEBBLE--02203
Thursday, March 13, 2003

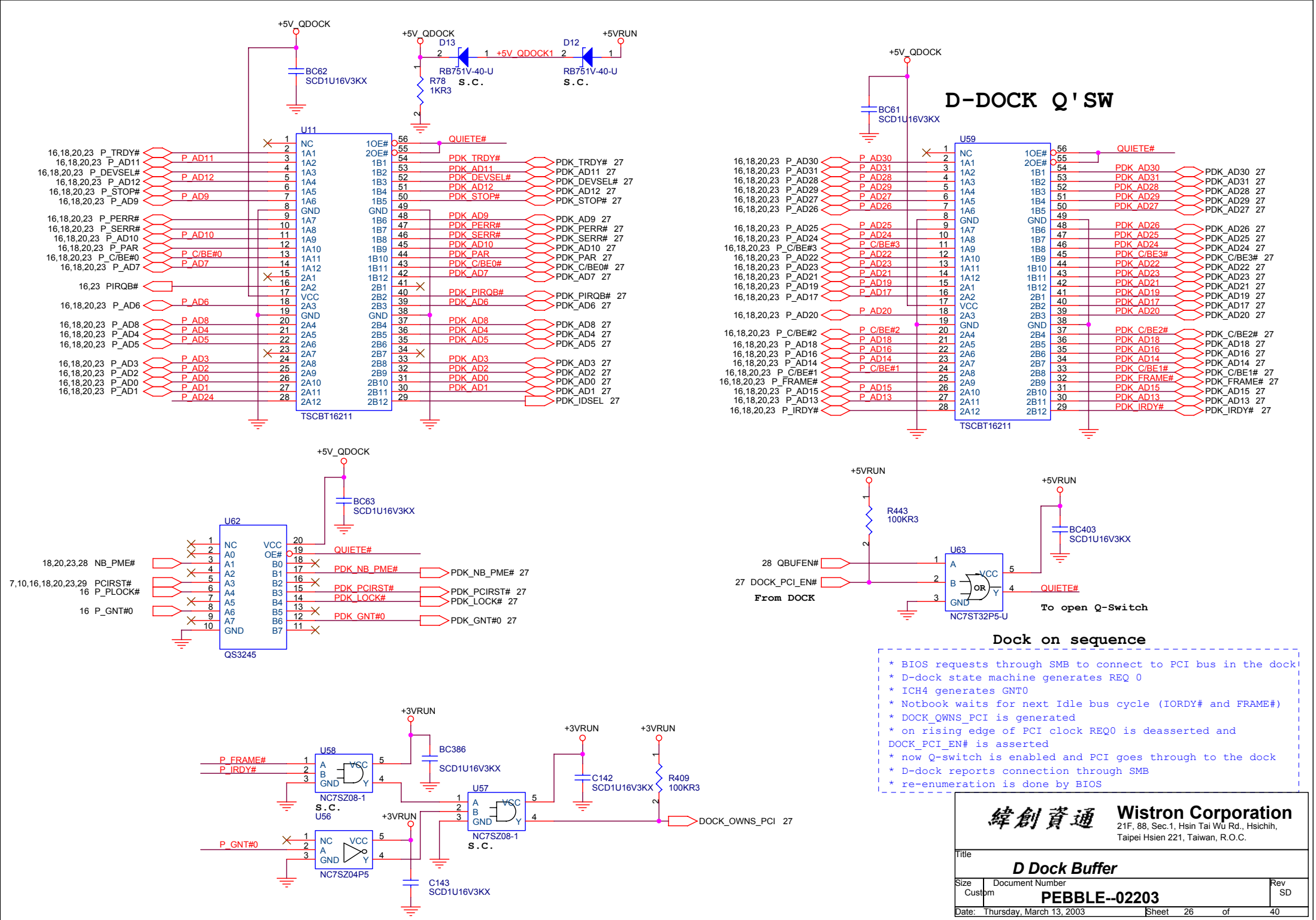


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO (2 of 2) --Phone Jack

Size: A3 | Document Number: PEBBLE--02203 | Rev: SD

Date: Thursday, March 13, 2003 | Sheet 25 of 40

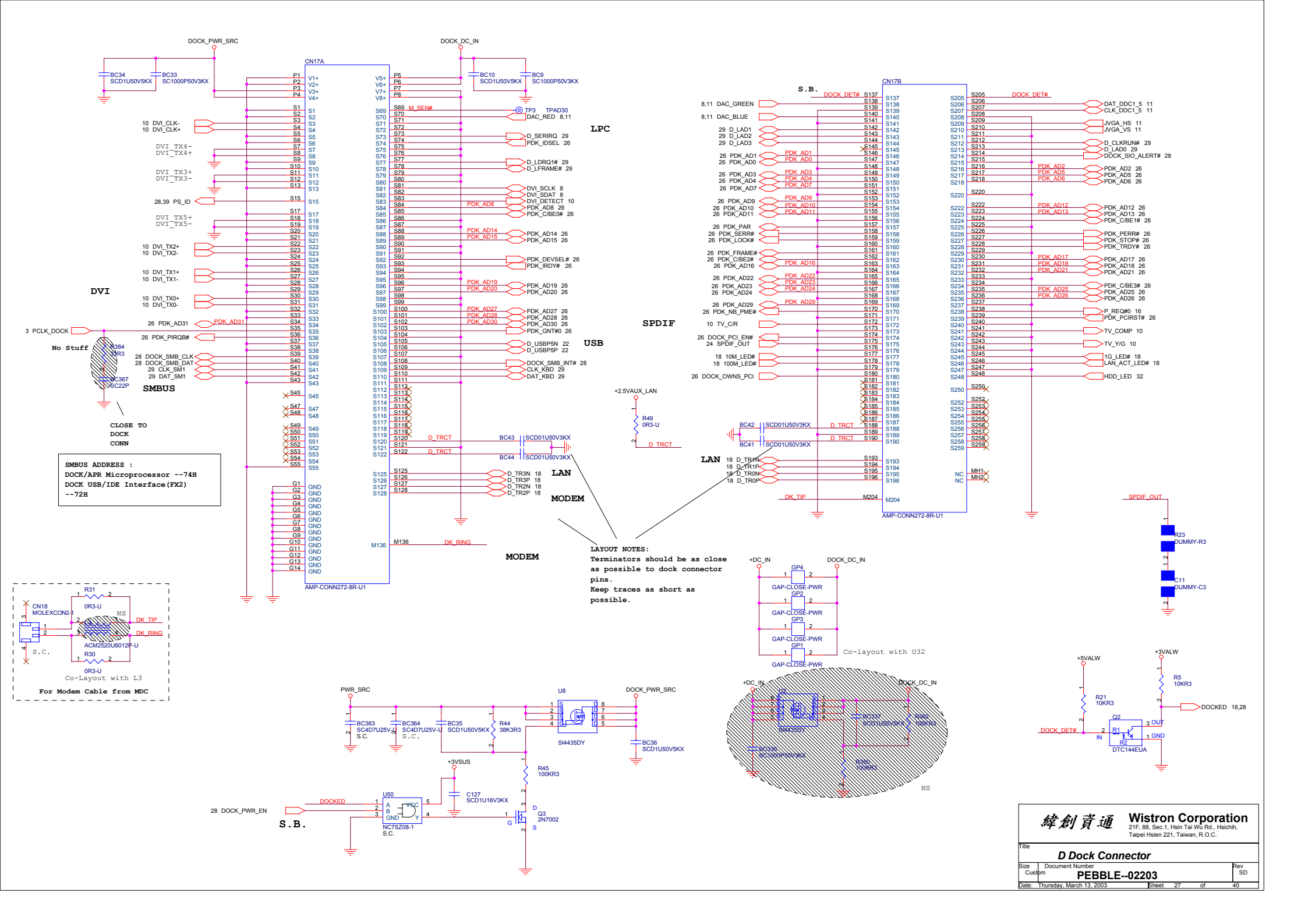


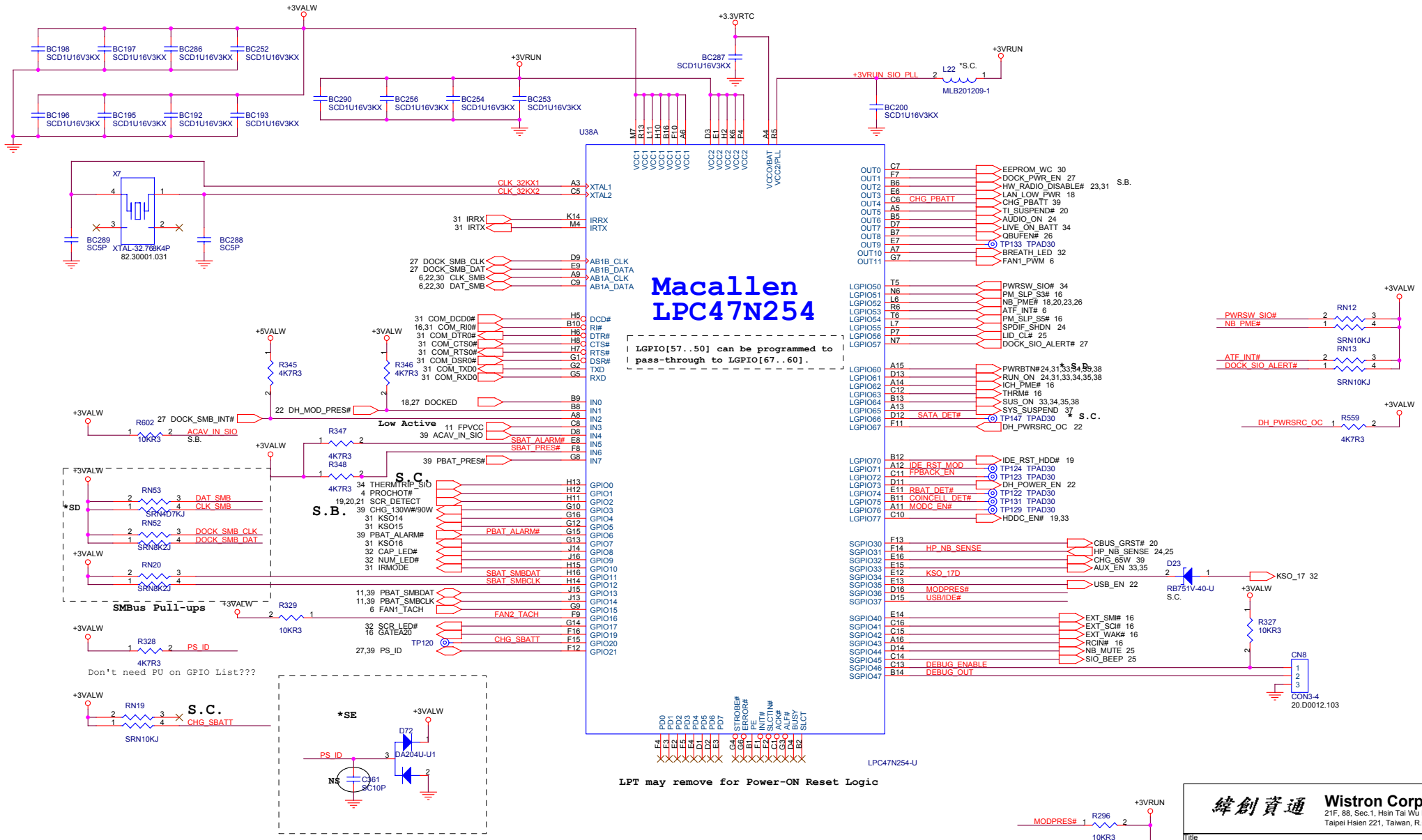
Dock on sequence

* BIOS requests through SMB to connect to PCI bus in the dock
* D-dock state machine generates REQ 0
* ICH4 generates GNT0
* Notbook waits for next Idle bus cycle (IORDY# and FRAME#)
* DOCK_QWNS_PCI is generated
* on rising edge of PCI clock REQ0 is deasserted and DOCK_PCI_EN# is asserted
* now Q-switch is enabled and PCI goes through to the dock
* D-dock reports connection through SMB
* re-enumeration is done by BIOS

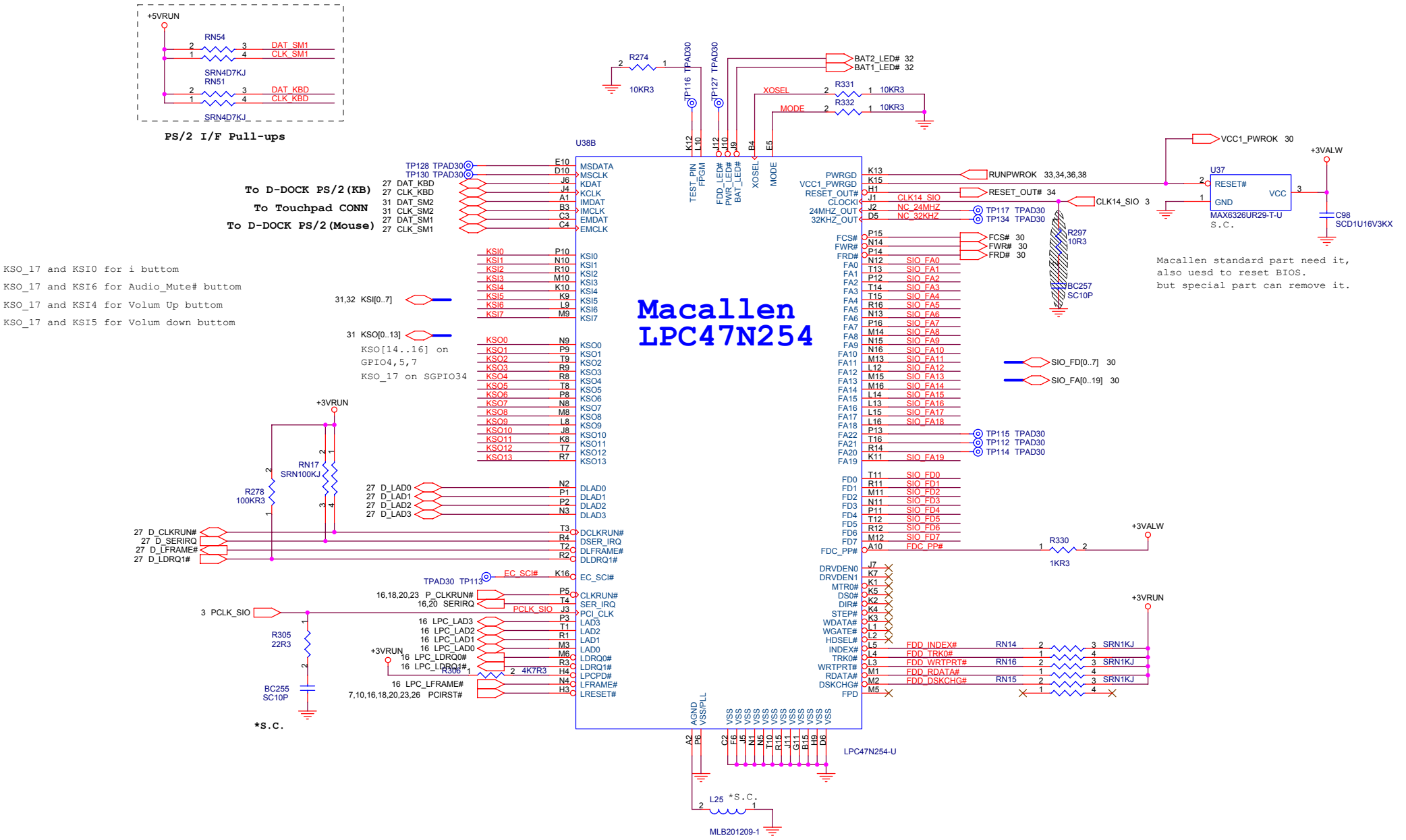
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *D Dock Buffer*			
Size: Custom	Document Number: PEBBLE--02203		Rev: SD
Date: Thursday, March 13, 2003	Sheet 26	of	40


DOCK_PWR_SRC
DOCK_DC_IN
CN17A
AMP-CONN272-8R-U1
DVI
SMBUS
No Stuff
CLOSE TO DOCK CONN
SMBUS ADDRESS :
DOCK/APR Microprocessor --74H
DOCK USB/IDE Interface(FX2)
--72H
LPC
SPDIF
USB
LAN
MODEM
MODEM
S.B.
CN17B
AMP-CONN272-8R-U1
LAYOUT NOTES:
Terminators should be as close as possible to dock connector pins.
Keep traces as short as possible.
Co-layout with U32
Co-Layout with L3
For Modem Cable from MDC
S.B.
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
D Dock Connector
PEBBLE--02203
Thursday, March 13, 2003
Sheet 27 of 40



Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: Macallen (1 of 2)	
Size: Custom	Document Number: PEBBLE--02203
Rev: SE	
Date: Thursday, March 13, 2003	Sheet 28 of 40



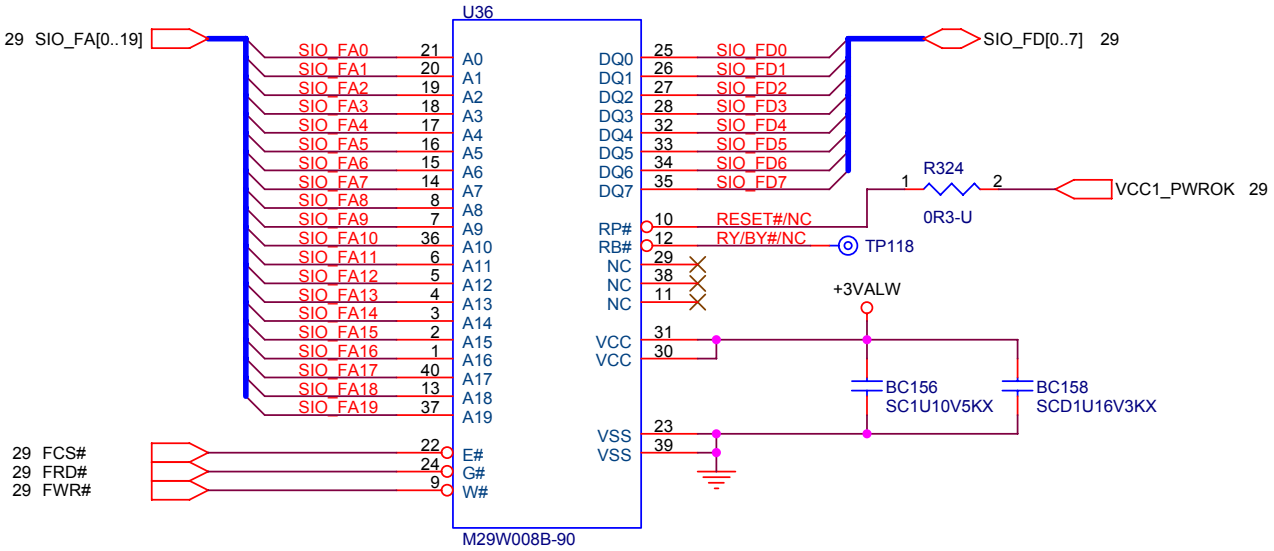
緯創資通	**Wistron Corporation**
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
	Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Macallen (2 of 2)***

Size	Document Number	Rev
A3	**PEBBLE--02203**	SD

Date: Thursday, March 13, 2003 Sheet 29 of 40

8Mbit(1M Byte),No PLCC type

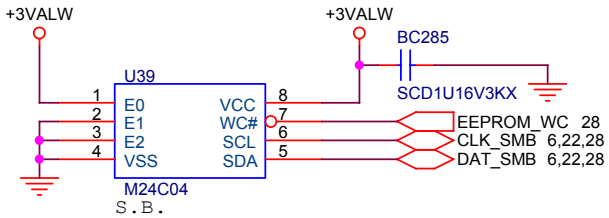


ST: M29W008AB-90 "72.29008.C09"

MXIC: 29LV008BTC-90 "72.29008.B09"

SMBus address A2

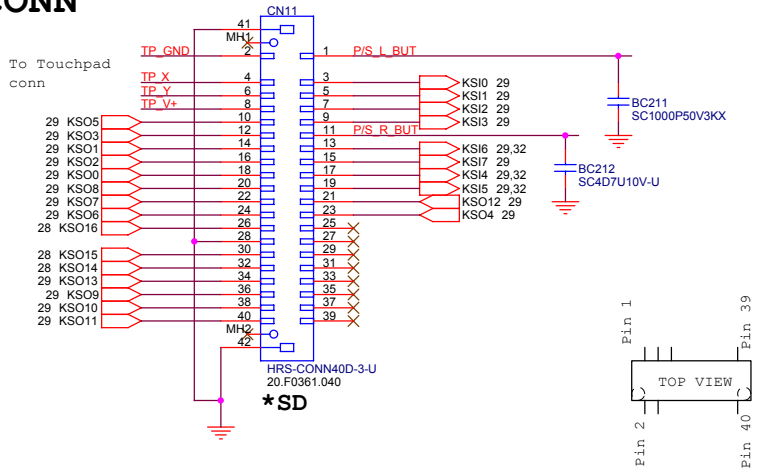
User Password



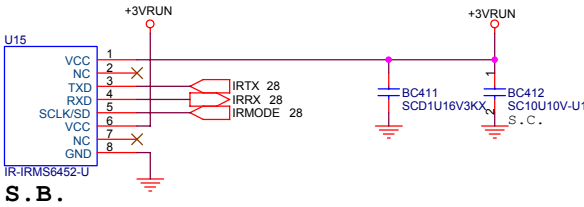
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	BIOS	
Size A4	Document Number PEBBLE--02203	Rev SD
Date: Thursday, March 13, 2003	Sheet 30 of 40	

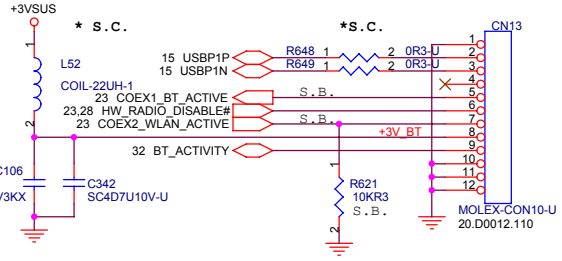
KB CONN



FIR

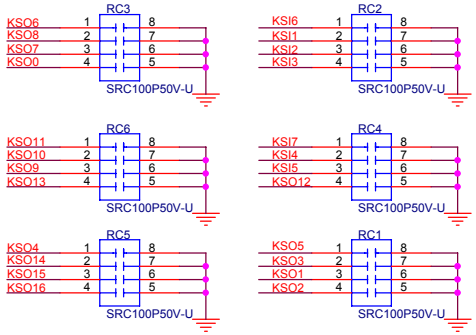


Bluetooth Module conn.

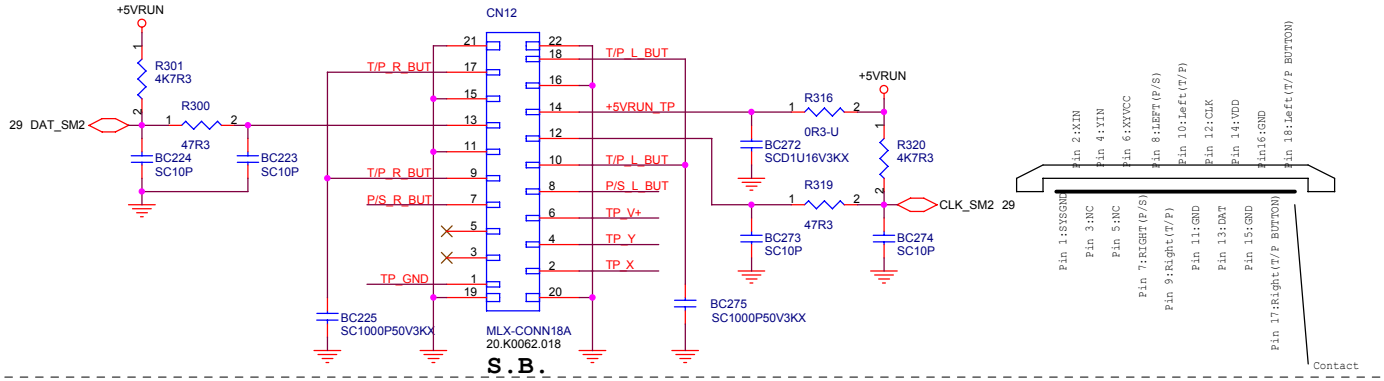


Note:Place R621 near CN13.

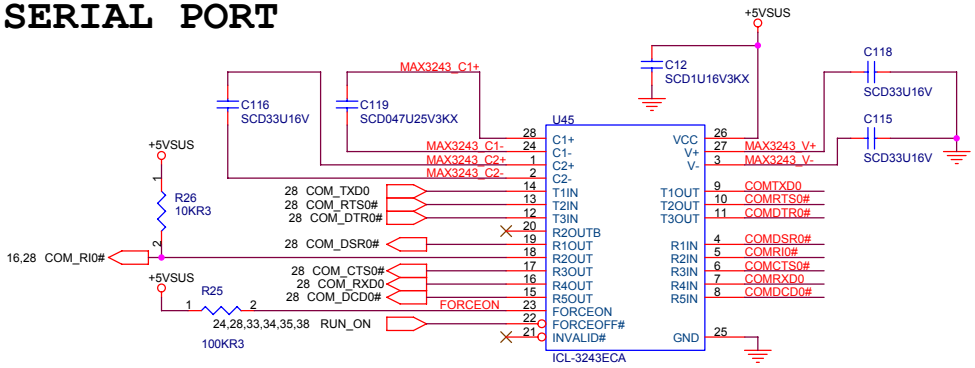
*SD:for EMI

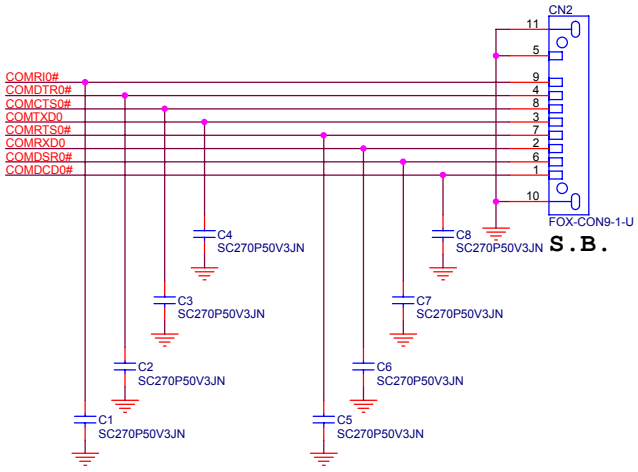


TOUCHPAD CONN



SERIAL PORT

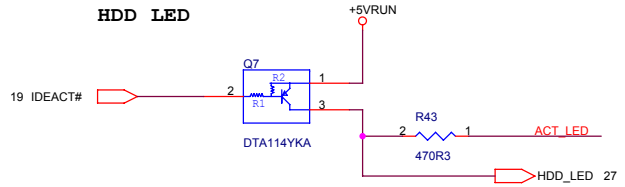




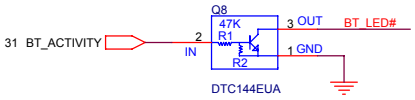
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	T/P,KB Connector & IrDA		
Size A3	Document Number PEBBLE--02203		Rev SD
Date: Thursday, March 13, 2003	Sheet 31	of	40

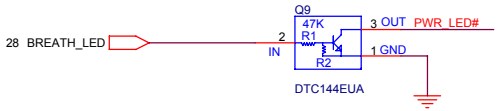
HDD LED



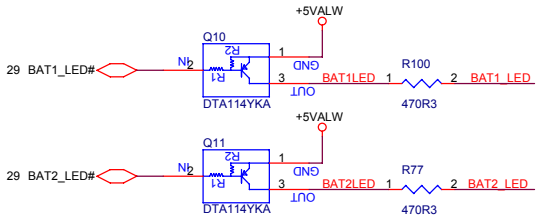
BLUETOOTH LED



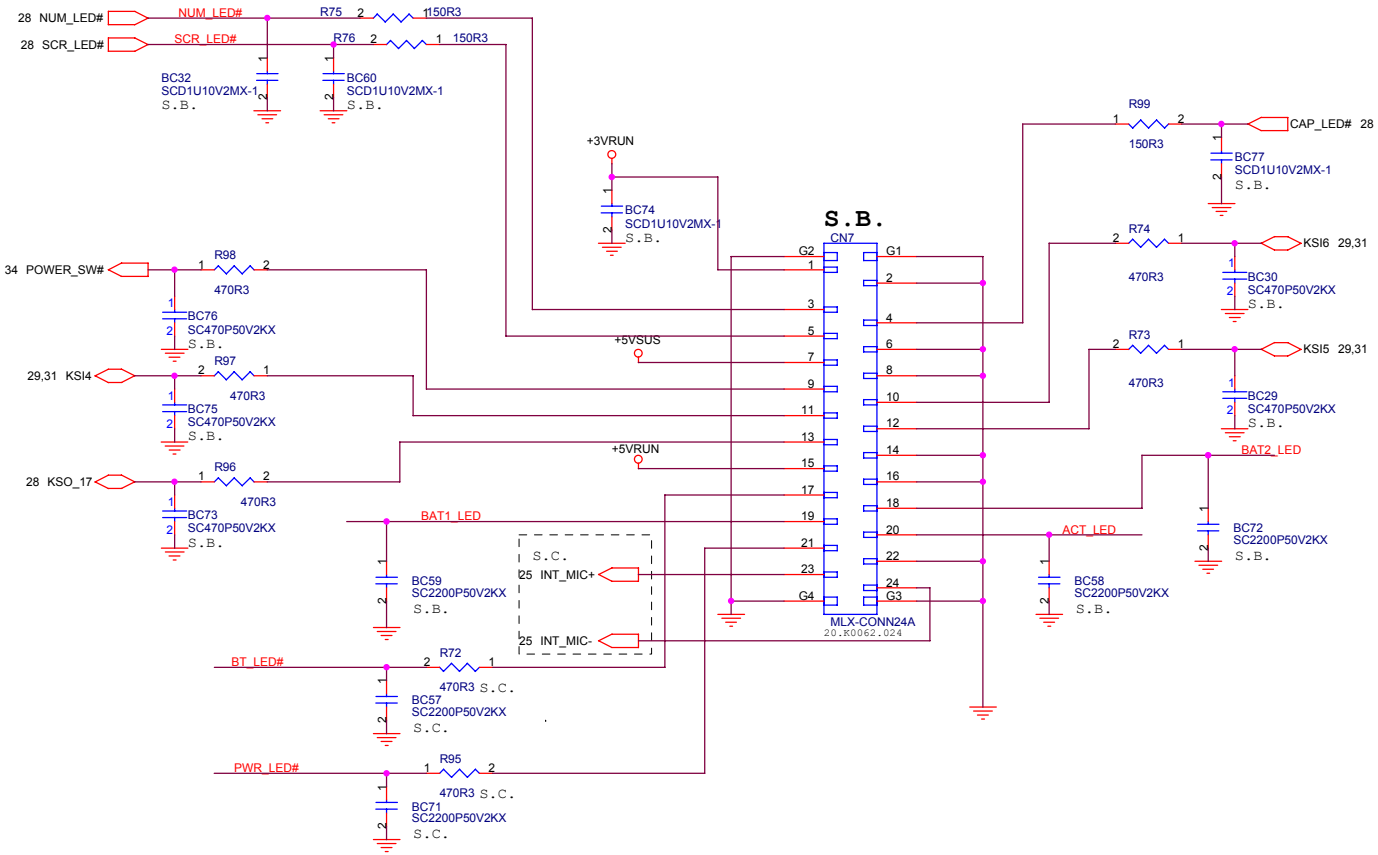
POWER LED

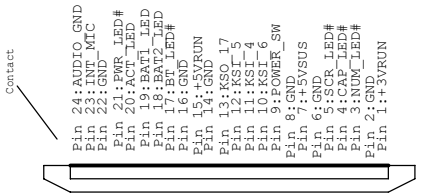


BATTERY LED

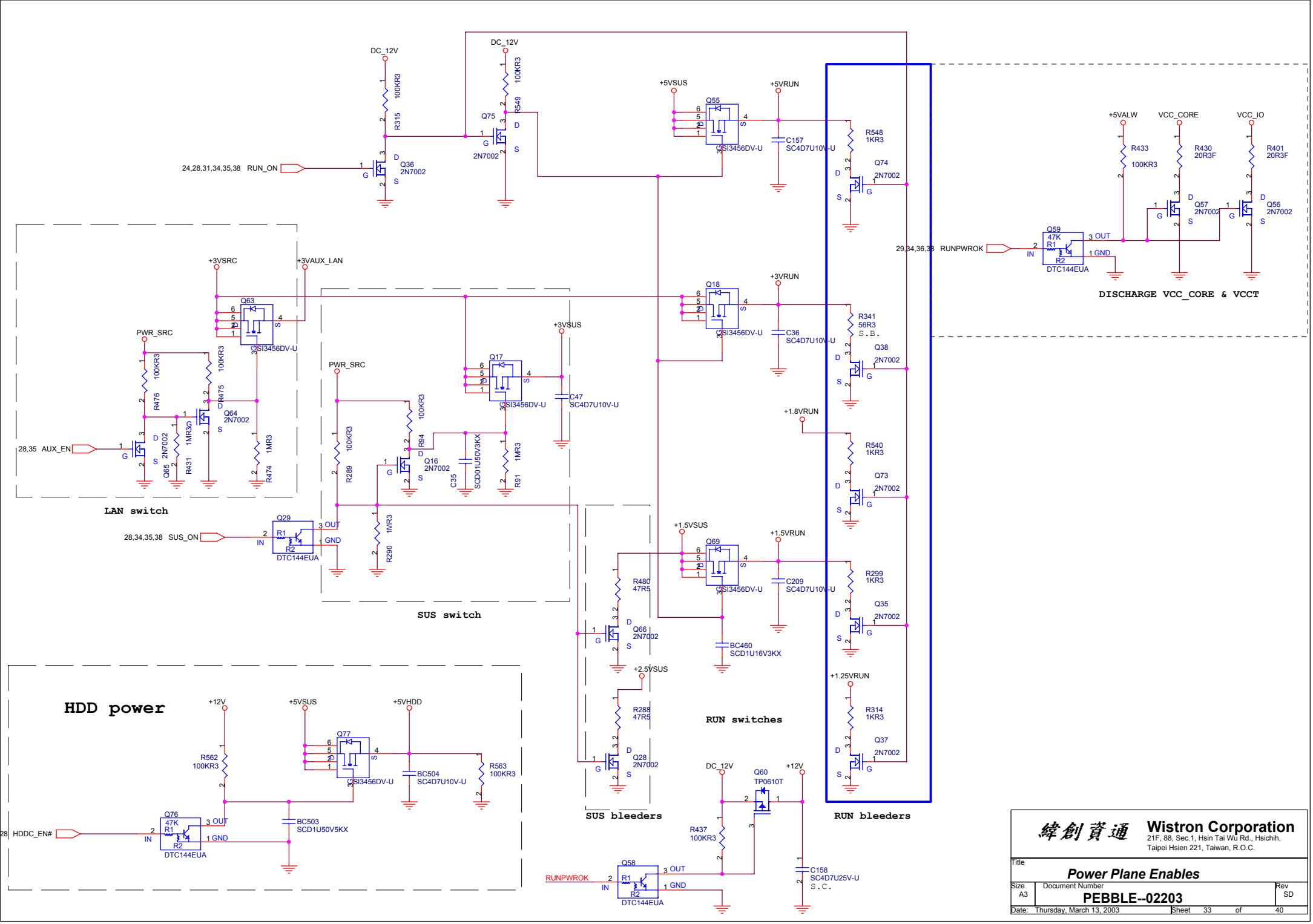


LED & BUTTON BD CONN

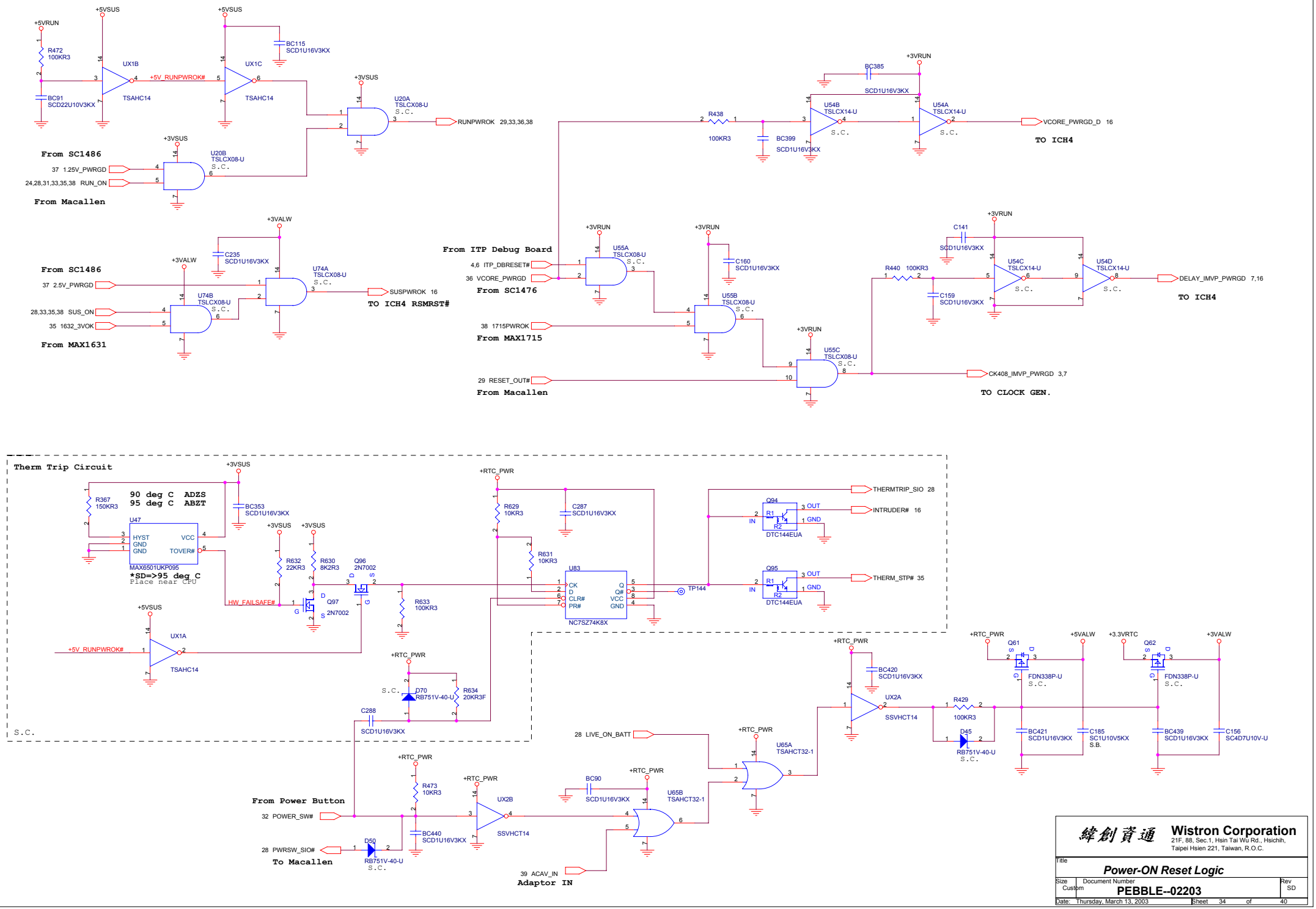




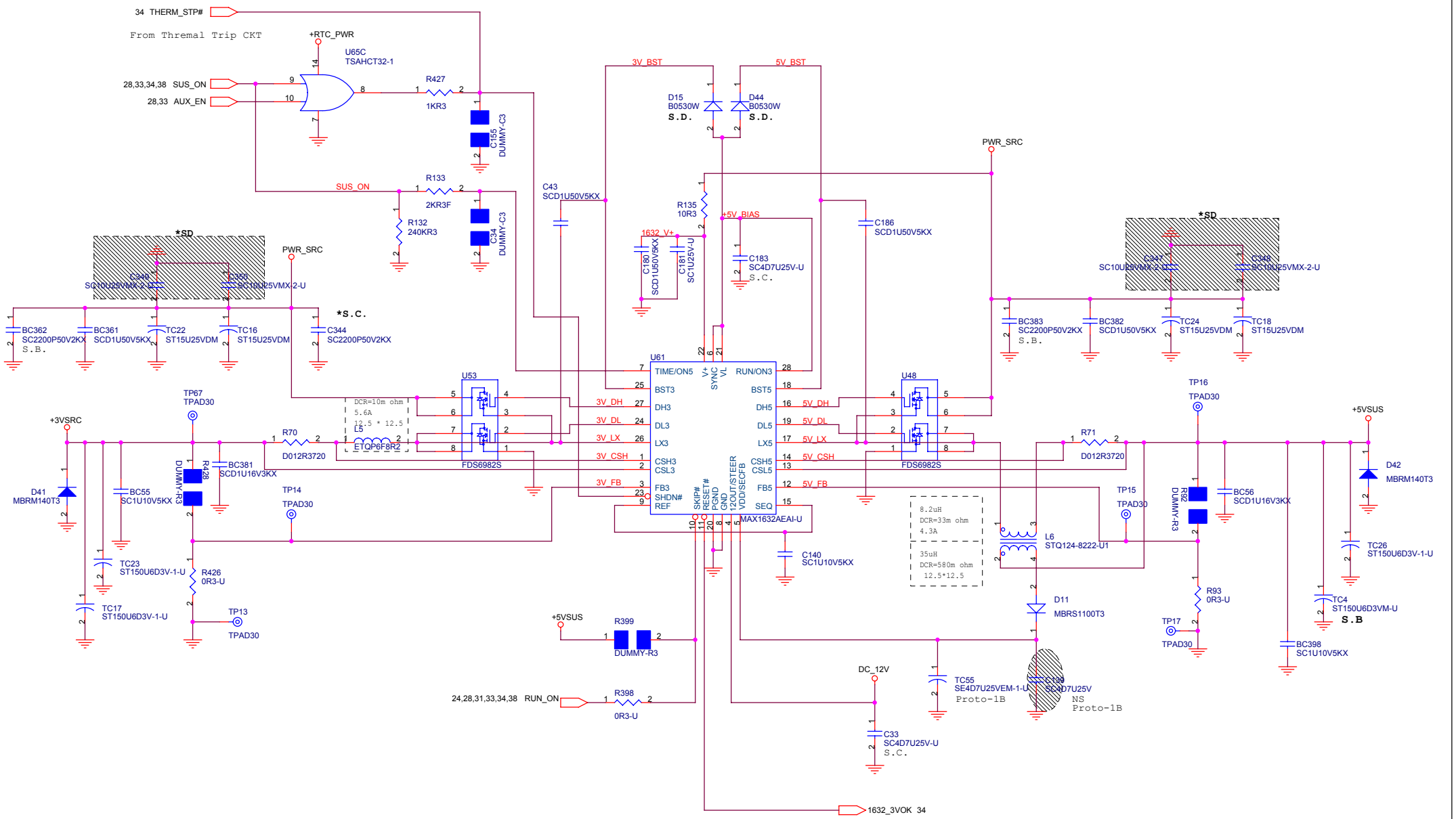
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***LED Button FPC Connector***	
Size A3	Document Number **PEBBLE--02203**	Rev SD
Date: Thursday, March 13, 2003	Sheet 32 of 40	



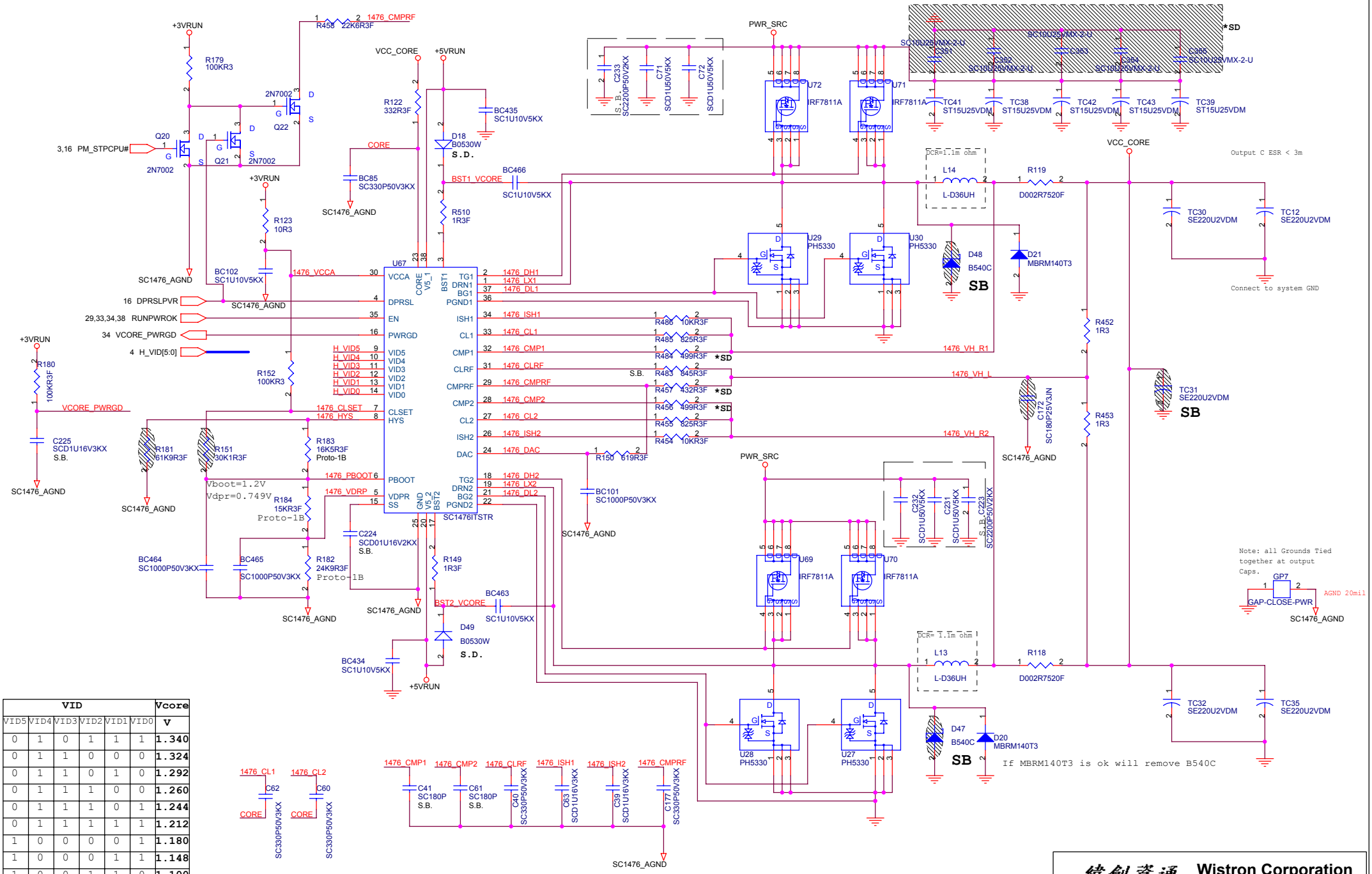
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Power Plane Enables***	
Size A3	Document Number **PEBBLE--02203**	Rev SD
Date: Thursday, March 13, 2003	Sheet 33 of 40	



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Power-ON Reset Logic***	
Size: Custom	Document Number: **PEBBLE--02203**	Rev: SD
Date: Thursday, March 13, 2003	Sheet 34 of 40	



Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	DC/DC 3V/5V/12V
Size A3	Document Number PEBBLE--02203 Rev SD
Date: Thursday, March 13, 2003	Sheet 35 of 40



VID						Vcore
VID5	VID4	VID3	VID2	VID1	VID0	V
0	1	0	1	1	1	1.340
0	1	1	0	0	0	1.324
0	1	1	0	1	0	1.292
0	1	1	1	0	0	1.260
0	1	1	1	0	1	1.244
0	1	1	1	1	1	1.212
1	0	0	0	0	1	1.180
1	0	0	0	1	1	1.148
1	0	0	1	1	0	1.100
1	0	1	0	0	1	1.052
1	0	1	0	1	1	1.020
1	0	1	1	1	0	0.972
1	1	0	0	0	0	0.940

10 mil Trace list for layout

PIN4
PIN5
PIN7
PIN25
PIN30

20 mil Trace list for layout

The +5VRUN(PIN38 and PIN20)
BST1_VCORE
BST2_VCORE

100 mil Trace list for layout

1476_DH1
1476_LX1
1476_DL1
1476_DH2
1476_LX2
1476_DL2

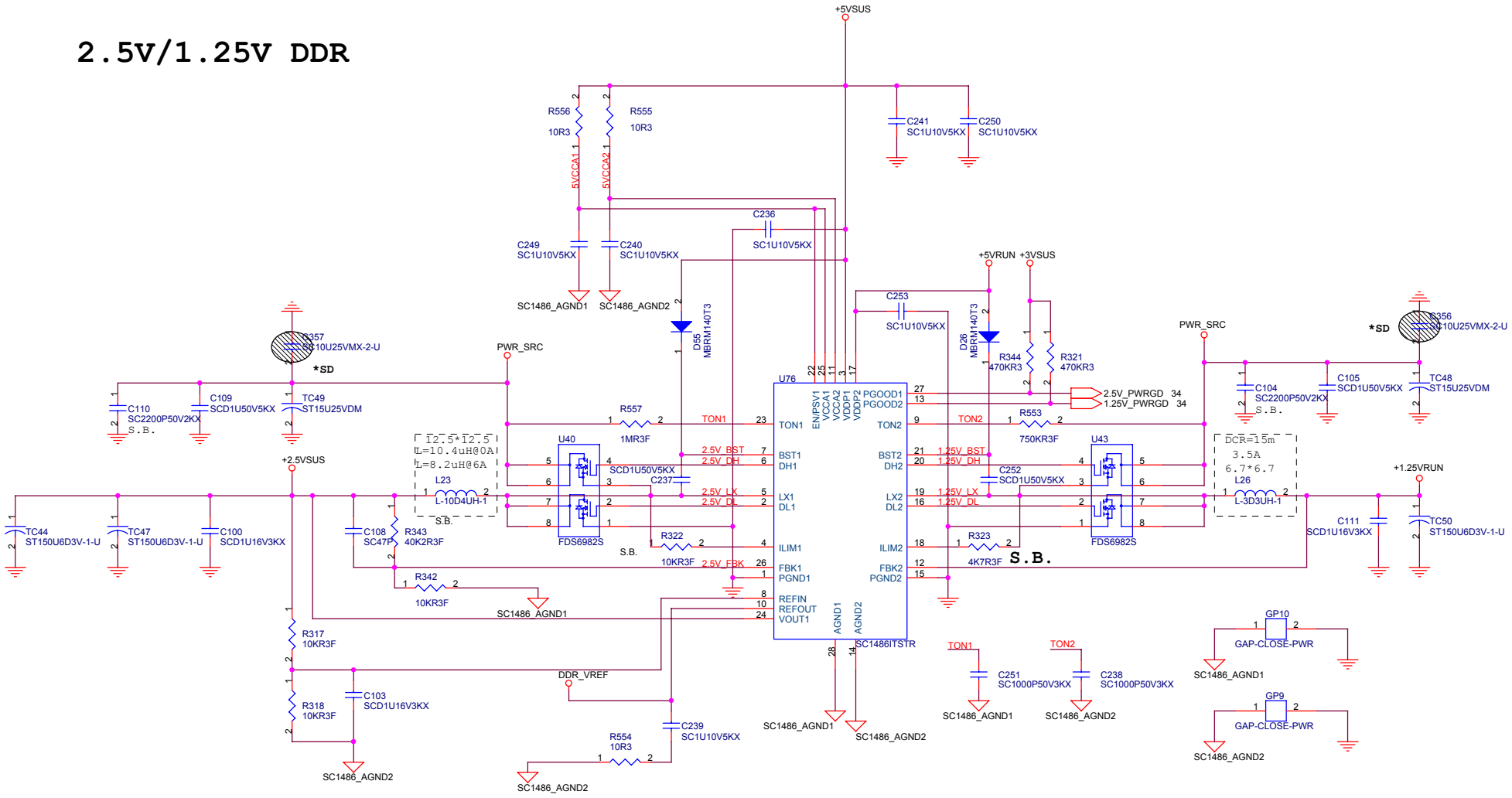
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

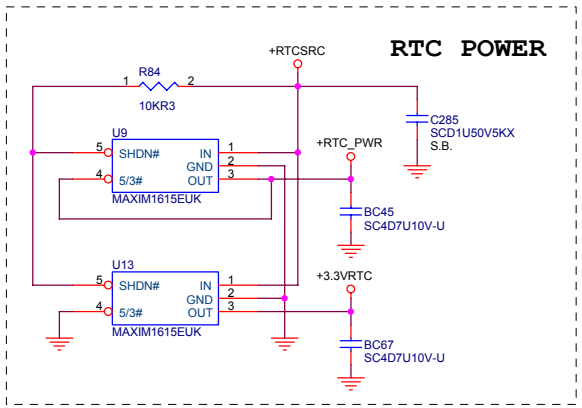
Title: ***CPU_CORE--IMVP4***

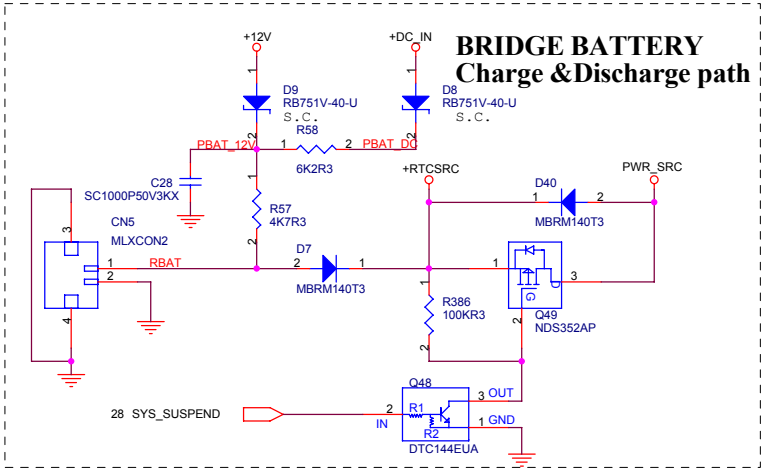
Size: A3 | Document Number: **PEBBLE--02203** | Rev: SD

Date: Thursday, March 13, 2003 | Sheet 36 of 40

2.5V/1.25V DDR







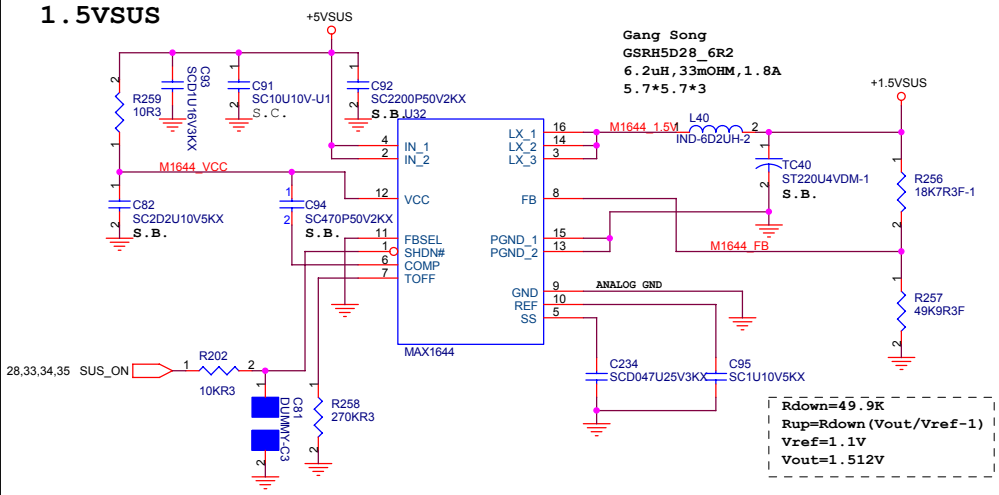
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *DDR 2.5V & 1.25V*

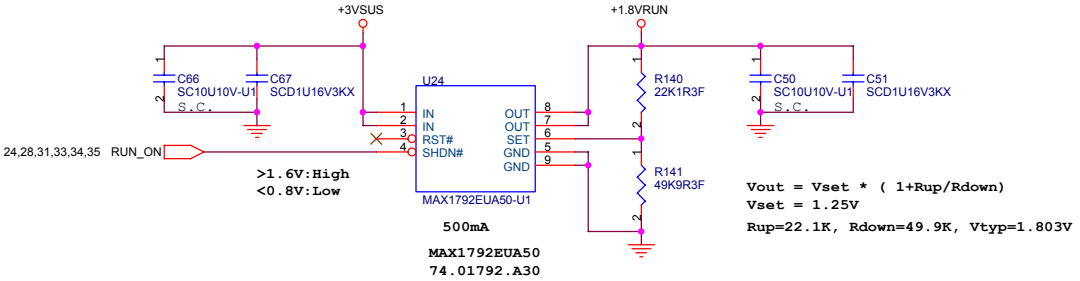
Size A3 | Document Number: **PEBBLE--02203** | Rev SD

Date: Thursday, March 13, 2003 | Sheet 37 of 40

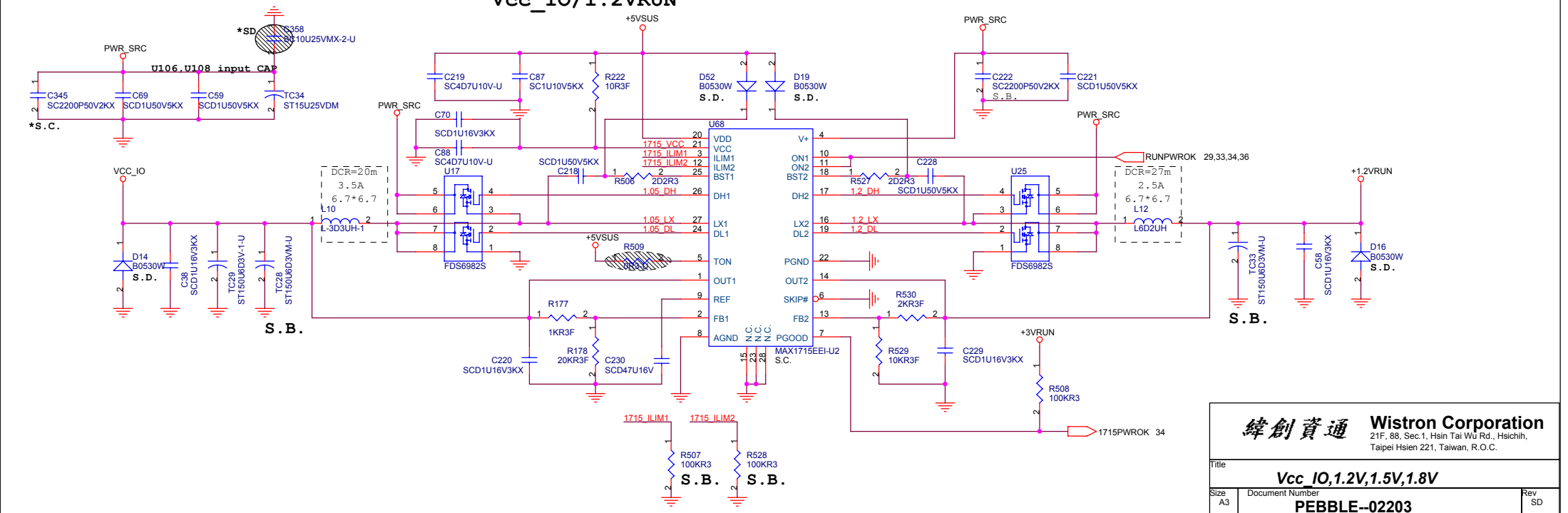
1.5VSUS



1.8VRUN



Vcc_IO/1.2VRUN

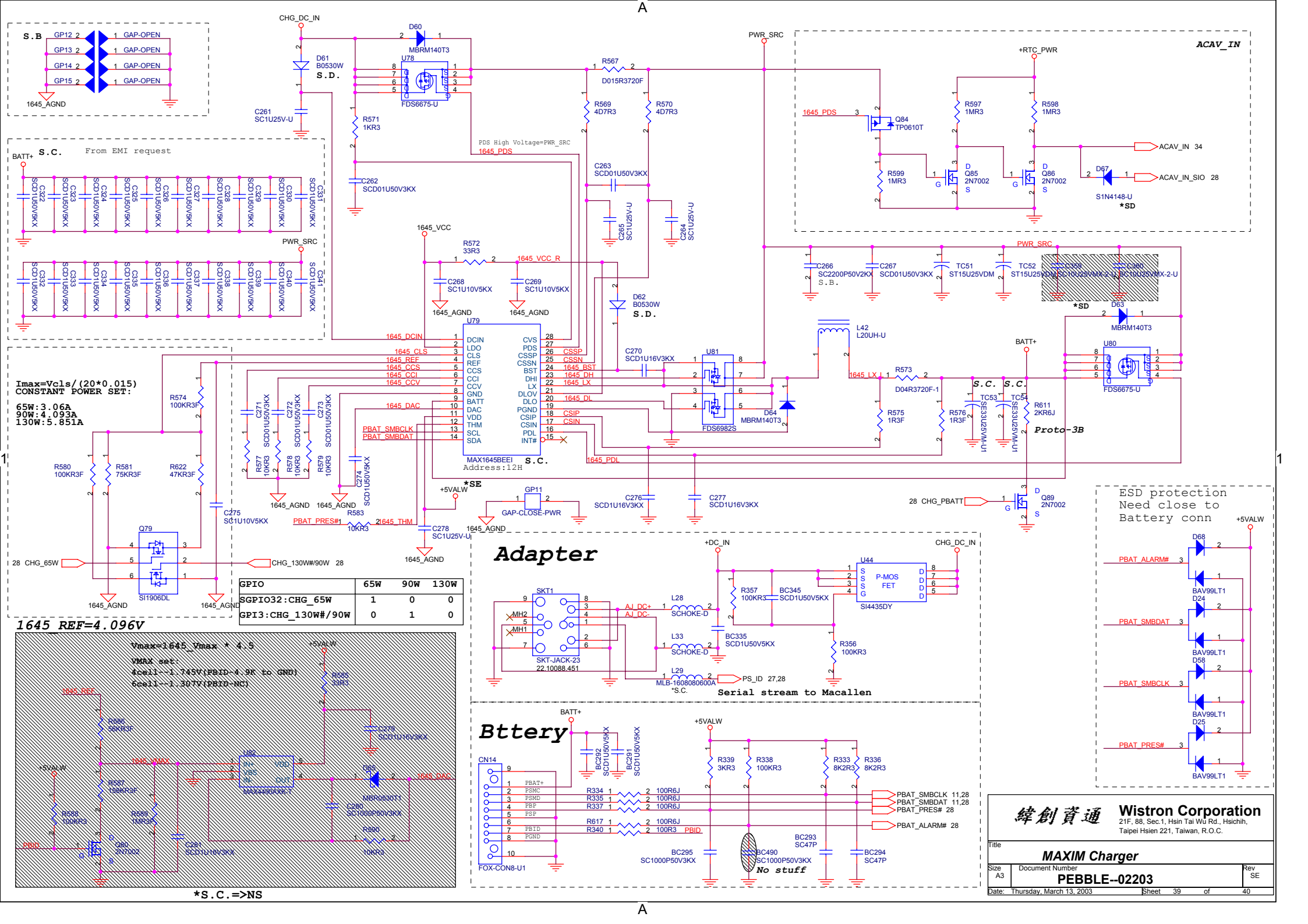


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Vcc_IO,1.2V,1.5V,1.8V*

Size A3 | Document Number: **PEBBLE--02203** | Rev SD

Date: Thursday, March 13, 2003 | Sheet 38 of 40


S.B
GP12
GP13
GP14
GP15
GAP-OPEN
1645_AGND
S.C.
From EMI request
BATT+
PWR_SRC
CHG_DC_IN
D60
MBRM140T3
D61
B0530W
S.D.
C261
SC1U25V-U
U78
FDS6675-U
R571
1KR3
C262
SCD01U50V3KX
R567
D015R3720F
R569
4D7R3
R570
4D7R3
C263
SCD01U50V3KX
C265
SC1U25V-U
C264
SC1U25V-U
PDS High Voltage=PWR_SRC
1645_PDS
ACAV_IN
+RTC_PWR
1645_PDS
Q84
TP0610T
R597
1MR3
R598
1MR3
R599
1MR3
Q85
2N7002
Q86
2N7002
D67
S1N4148-U
*SD
ACAV_IN 34
ACAV_IN_SIO 28
1645_VCC
R572
33R3
1645_VCC_R
C268
SC1U10V5KX
C269
SC1U10V5KX
D62
B0530W
S.D.
U79
MAX1645BEEI
Address:12H
S.C.
1645_DCIN
1645_CLS
1645_REF
1645_CCS
1645_CCI
1645_CCV
1645_DAC
PBAT_SMBCLK
PBAT_SMBDAT
1645_PDL
C270
SCD1U16V3KX
U81
FDS6982S
L42
L20UH-U
D64
MBRM140T3
1645_LX_1
R573
D04R3720F-1
R575
1R3F
R576
1R3F
TC53
SE33U25VM-U1
TC54
SE33U25VM-U1
R611
2KR6J
Proto-3B
C266
SC2200P50V2KX
S.B.
C267
SCD01U50V3KX
TC51
ST15U25VDM
TC52
ST15U25VDM
C359
SC10U25VMX-2-U
C360
SC10U25VMX-2-U
D63
MBRM140T3
U80
FDS6675-U
Imax=Vcls/(20*0.015)
CONSTANT POWER SET:
65W:3.06A
90W:4.093A
130W:5.851A
R574
100KR3F
R580
100KR3F
R581
75KR3F
R622
47KR3F
C275
SC1U10V5KX
Q79
SI1906DL
28 CHG_65W
CHG_130W#/90W 28
C271
SCD01U50V3KX
C272
SCD01U50V3KX
C273
SCD01U50V3KX
R577
10KR3
R578
10KR3
R579
10KR3
C274
SCD01U50V5KX
R583
10KR3
PBAT_PRES#1
1645_THM
C278
SC1U25V-U
+5VALW
*SE
GP11
GAP-CLOSE-PWR
C276
SCD1U16V3KX
C277
SCD1U16V3KX
28 CHG_PBATT
Q89
2N7002
ESD protection
Need close to
Battery conn
D68
BAV99LT1
D24
BAV99LT1
D58
BAV99LT1
D25
BAV99LT1
PBAT_ALARM#
PBAT_SMBDAT
PBAT_SMBCLK
PBAT_PRES#
Adapter
+DC_IN
CHG_DC_IN
SKT1
SKT-JACK-23
22.10088.451
AJ_DC+
AJ_DC-
L28
SCHOKE-D
L33
SCHOKE-D
L29
MLB-1608080600A
*S.C.
R357
100KR3
BC345
SCD1U50V5KX
BC335
SCD1U50V5KX
R356
100KR3
U44
P-MOS
FET
SI4435DY
PS_ID 27,28
Serial stream to Macallen
Bttery
BATT+
CN14
FOX-CON8-U1
BC292
SCD1U50V5KX
BC291
SCD1U50V5KX
R339
3KR3
R338
100KR3
R333
8K2R3
R336
8K2R3
R334
R335
R337
R617
R340
100R6J
100R3
PBID
PBAT_SMBCLK 11,28
PBAT_SMBDAT 11,28
PBAT_PRES# 28
PBAT_ALARM# 28
BC295
SC1000P50V3KX
BC490
SC1000P50V3KX
No stuff
BC293
SC47P
BC294
SC47P
1645 REF=4.096V
Vmax=1645_Vmax * 4.5
VMAX set:
4cell--1.745V(PBID-4.9K to GND)
6cell--1.307V(PBID-NC)
R585
33R3
C279
SCD1U16V3KX
U82
MAX4380AAX+T
R587
100KF9F
R588
100KR3
R589
1MR3F
Q80
2N7002
C281
SCD1U16V3KX
D65
MBR0530T1
C280
SC1000P50V3KX
R590
10KR3
1645_DAC
*S.C.=>NS
GPIO
65W
90W
130W
SGPIO32:CHG_65W
1
0
0
GPI3:CHG_130W#/90W
0
1
0
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
MAXIM Charger
Size
A3
Document Number
PEBBLE--02203
Rev
SE
Date: Thursday, March 13, 2003
Sheet 39 of 40

Impedance measurement coupon

Trace length >= 4 inches

Trace width / Spacing = 5 / 5 mil-----45 ohm

L1: R510 — R511

L10: R512 — R513

Trace width / Spacing = 4 / 5 mil----55 ohm

L3: R514 — R515

L4: R516 — R517

L7: R518 — R519

L8: R520 — R521

USB Diff. pair Twidth/Tspacing = 4/5 mil-----90 ohm

L8: R522 — R523; R524 — R525

Diff. pair for LVDS, LAN
Twidth/Tspacing = 4/8 mil-----100 ohm

L3: R526 — R527; R528 — R529

L8: R530 — R531; R532 — R533

1394 Diff. pair Twidth/Tspacing = 4/10 mil----110 ohm

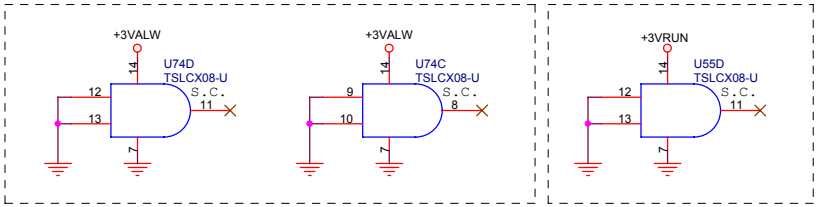
L8: R534 — R535; R536 — R537

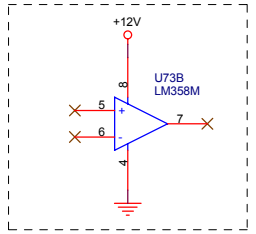
Host CLK signal Trace Twidth/Tspacing = 4/8 mil----100ohm

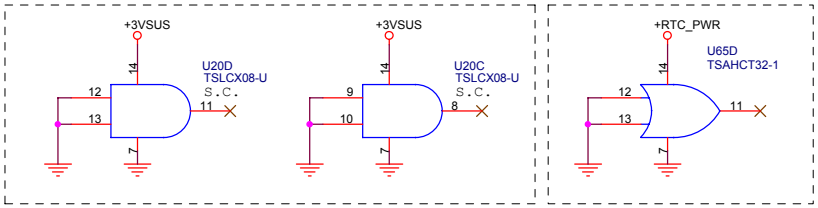
L4: R538 — R539; R540 — R541

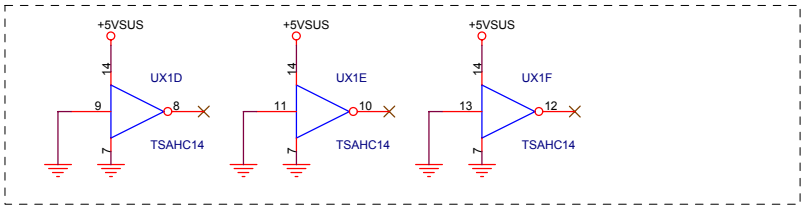
DDR CLK signal Trace Twidth/Tspacing = 7/4 mil----70ohm

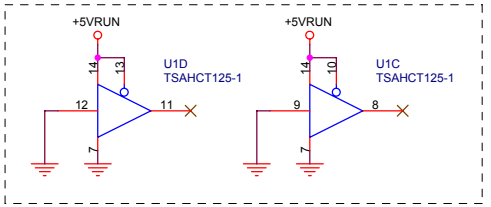
L8: R542 — R543; R544 — R545

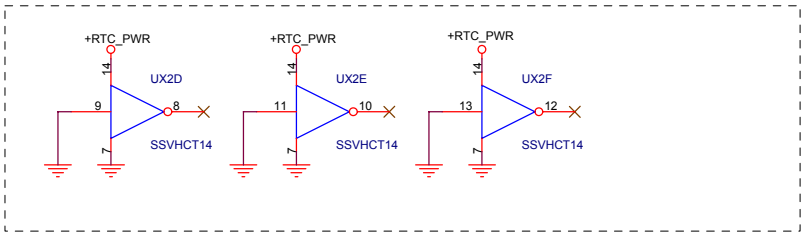


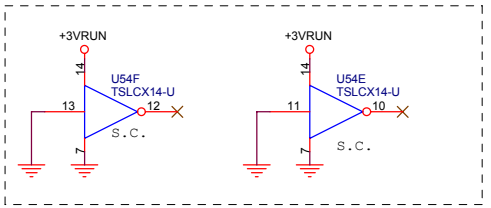


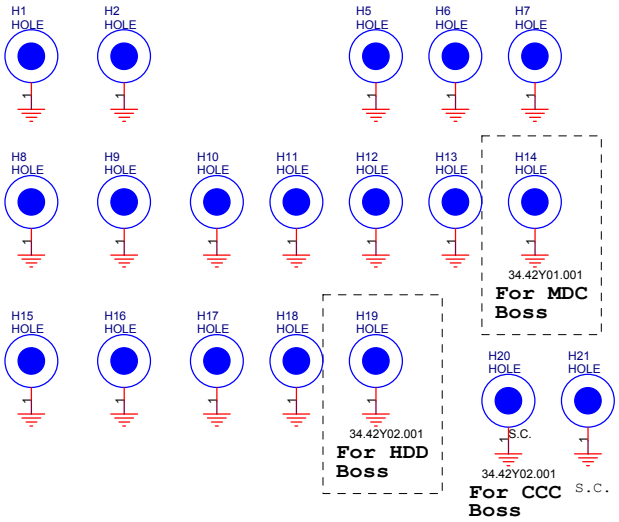


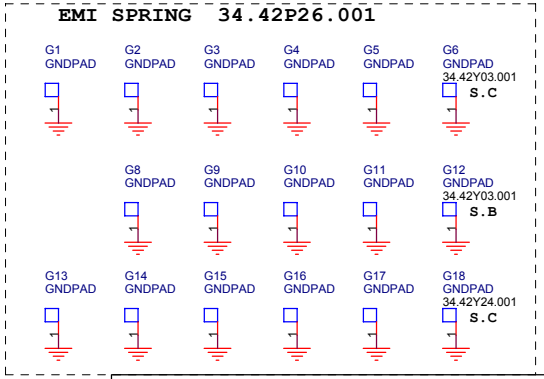












緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Holes & GND PADS***

Size: A3 | Document Number: **PEBBLE--02203** | Rev: SD

Date: Thursday, March 13, 2003 | Sheet 40 of 40