

Key-West / Kinney Block Diagram

Project code: 91.4D901.001
 PCB P/N : 48.4D901.021
 REVISION : 05209-2

CLK GEN³
 ICS954226AG

SB

4,5
Mobile CPU
 Celeron/Dothan

6,7,8,9,10
Alviso
 GML

15,16,17,18
ICH6-M

DDRII*2^{11,12}
 400MHz

LVDS → **LCD**¹³

RGB CRT → **CRT**¹⁴

Mini-PCI²⁵
 802.11a/b/g

RJ45
 CONN²²

10/100 BCM4401²¹

RJ11
 CONN²²

MODEM
 MDC 1.5 Card²⁶

SB

AZALIA

LINE OUT²⁴

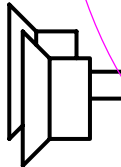
OP AMP
 MAX4411²⁴

MIC IN²⁴

AZALIA CODEC
 STAC9200²³

OP AMP
 TPA6017²⁴

SB



2CH SPEAKER

Host BUS
 400MHz

DMI I/F
 100MHz

PCI BUS

USB 2.0

USB x 3²⁶

P IDE

MASTER

HDD²⁰

SLAVE

DVD/
 CD-RW²⁰

PCI EXPRESS / USB 2.0

PCI EXPRESS
 CARD²⁰

LPC Bus

Power
 Switch²⁰
 TPS2231

KBC²⁷
 H8S/RE144AV

SC

FlashRom²⁹
 4Mb
 (S12kB)

Touch
 Pad²⁸

Int.
 KB²⁸

SMBus

Thermal Sensor
 & Fan¹⁹
 ENC 6N300

SB

SYSTEM DC/DC MAX8734A ³³	
INPUTS	OUTPUTS
DCBATOUT	5V_S3 3V_S3

SYSTEM DC/DC TPS5130 ^{34,35}	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D2V_S0 1D8V_S3

MAXIM CHARGER MAX1909 ³¹	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 4.0A 5V 100mA

CPU DC/DC MAX1907 ³²	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 27A

PCB LAYER	
L1:	Signal 1
L2:	GND
L3:	Signal 2
L4:	Signal 3
L5:	VCC
L6:	Signal 4

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Title: **Block Diagram**

Size: A3 Document Number: **Key-West / Kinney** Rev: -2

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ICH6-M Integrated Pull-up and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

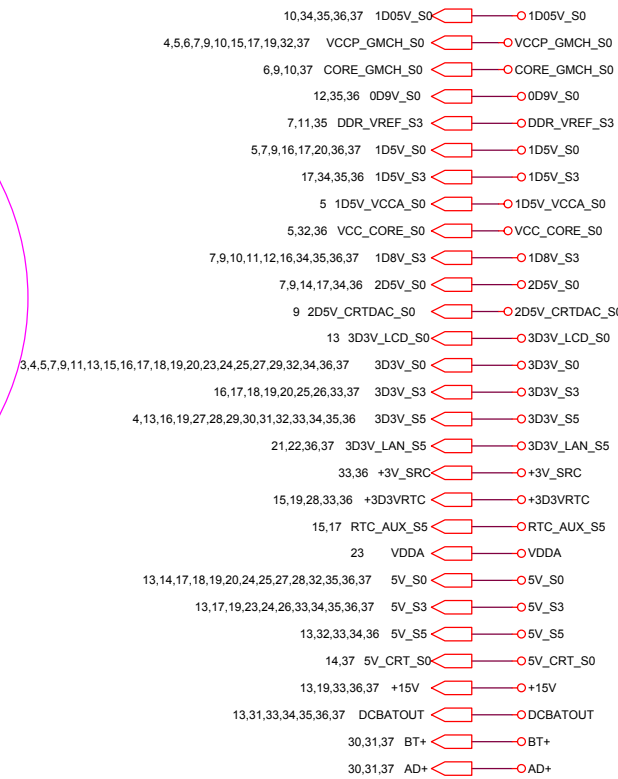
ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, EE_CS, GNT[5]/GPO[17], GNT[6]/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVR, SPKR	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

ICH6-M IDE Integrated Series Termination Resistors

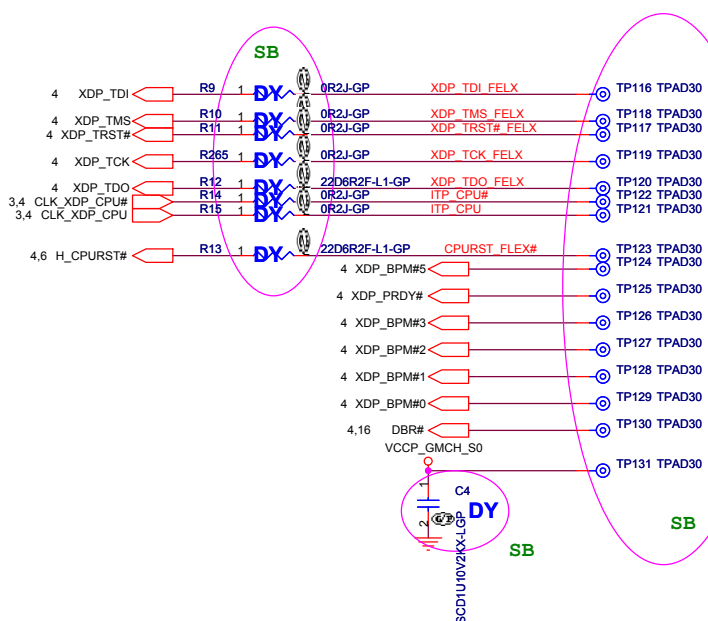
DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

Key-West / Kinney difference

	Key-West	Kenny
	non-Wake on LAN from S5	Wake on LAN from S5
R595	Stuff 1K ohm 0402	Dummy
R132, R573	Stuff 0 ohm 0805	Dummy
R360	Dummy	Stuff 1K ohm 0402
R131	Dummy	Stuff 10K ohm 0402
R368	Dummy	Stuff 100K ohm 0402
R367	Dummy	Stuff 200K ohm 0402
U56	Dummy	Stuff NC7SZ32M5X_NL
C172	Dummy	Stuff 0.01u 16V 0402
C174	Dummy	Stuff 10u 6.3V 0805
C308	Dummy	Stuff 0.047u 25V 0603
Q14	Dummy	Stuff DDTC144EUA-7-F
Q15	Dummy	Stuff FDN338P_NL
U58	Dummy	Stuff SI3456BDV-T1-E3
Q39	Dummy	Stuff 2N7002



-1



Device	SMBus addr.
Clock Gen.	D2
DDR Module 1	A0
DDR Module 2	A4
LCD	58
Guardian	5E
Battery	16
EEPROM	A2

USB Port	Key West Define
USBP[0]	USB1 Up connector
USBP[1]	New card used
USBP[2]	USB1 Down connector
USBP[3]	NC
USBP[4]	USB2 connector
USBP[5]	NC
USBP[6]	NC
USBP[7]	NC

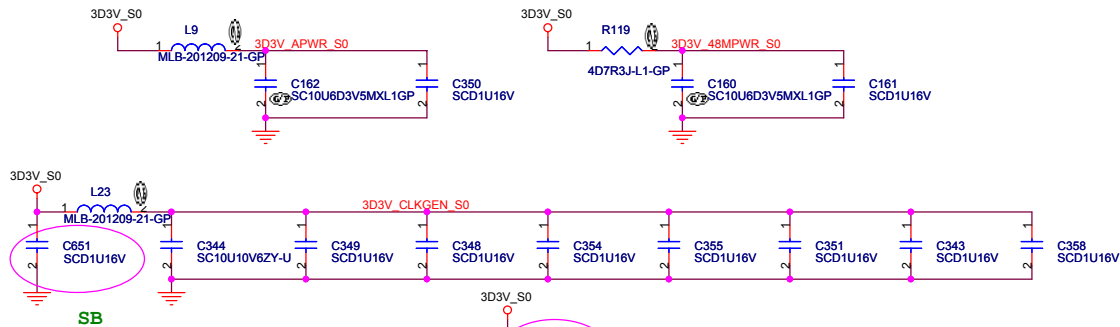
PCIE Port	Key West Define
PE[1]	NC
PE[2]	NC
PE[3]	NC
PE[4]	New card used

PCI RESOURCE TABLE

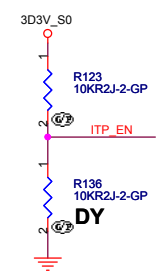
DEVICE	IDSEL	PCI IRQ	REQ#/GNT#
Mini-PCI	AD19	P_INTB# / P_INTD#	REQ3#/GNT3#
LAN	AD16	P_INTC#	REQ4#/GNT4#

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Title: **ITP**
 Size: A3 Document Number: **Key-West / Kinney** Rev: **-2**
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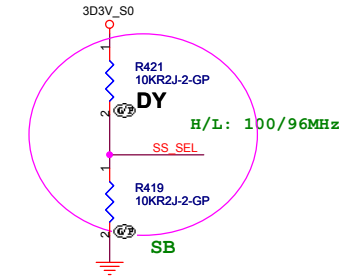
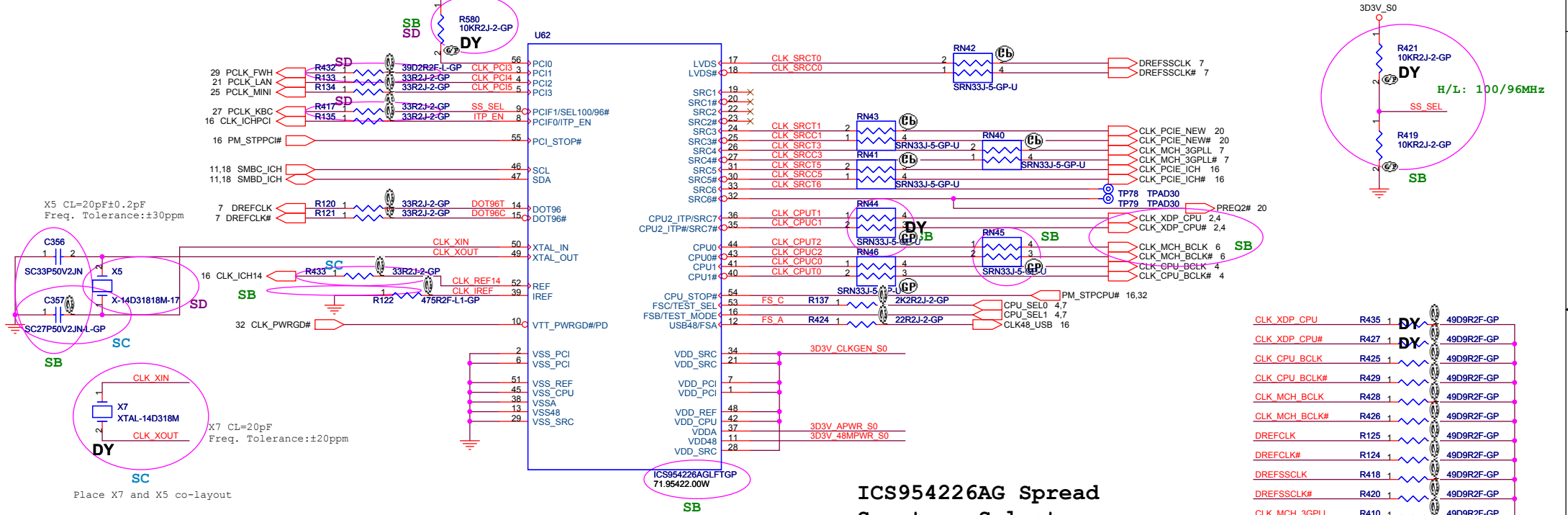


4.5,7,9,11,13,15,16,17,18,19,20,23,24,25,27,29,32,34,36,37 3D3V_S0

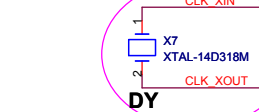
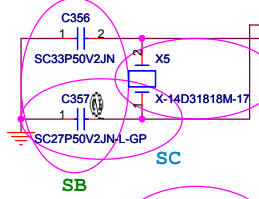


Dummy R123(up side),Mounting R136(down side)
--SRC7 on

Mounting R136(up side),Dummy R123(down side)
--CPU2_ITP on



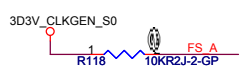
X5 CL=20pF±0.2pF
Freq. Tolerance:±30ppm



X7 CL=20pF
Freq. Tolerance:±20ppm

Place X7 and X5 co-layout

NEAR CLKGEN

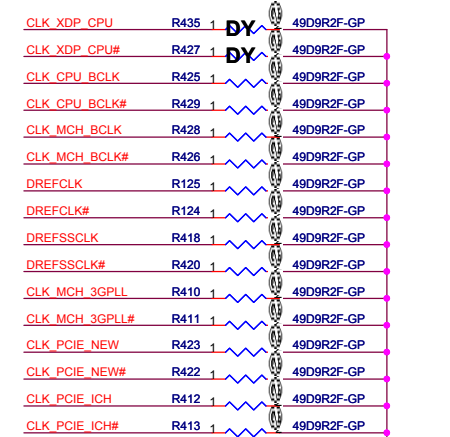


1st source: 71.95422.00W (ICS954226AGLFTGP)
2nd source: 71.00140.00W (IDTCV140PAG-GP)
3rd source: 71.28442.00W (CY28442ZXC-2T-GP)

FS_C	FS_B	FS_A	CPU
0	0	0	266M
0	0	1	133M
0	1	0	200M
0	1	1	166M
1	0	0	333M
1	0	1	100M
1	1	0	400M
1	1	1	Reserved

ICS954226AG Spread Spectrum Select

S3	S2	S1	S0	Spread Amount%
0	0	0	0	-0.8
0	0	0	1	-1.0
0	0	1	0	-1.25
0	0	1	1	-1.5
0	1	0	0	-1.75
0	1	0	1	-2.0
0	1	1	0	-2.5
0	1	1	1	-3.0
1	0	0	0	+/-0.3
1	0	0	1	+/-0.4
1	0	1	0	+/-0.5
1	0	1	1	+/-0.6
1	1	0	0	+/-0.8
1	1	0	1	+/-1.0
1	1	1	0	+/-1.25
1	1	1	1	+/-1.5



<Variant Name>

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Title: **Clock Generator (ICS954226AG)**

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6 H_A#[31..3]

VCCP_GMCH_S0
2,5,6,7,9,10,15,17,19,32,37 VCCP_GMCH_S0

1st source: 62.10079.001
2nd source: 62.10053.341

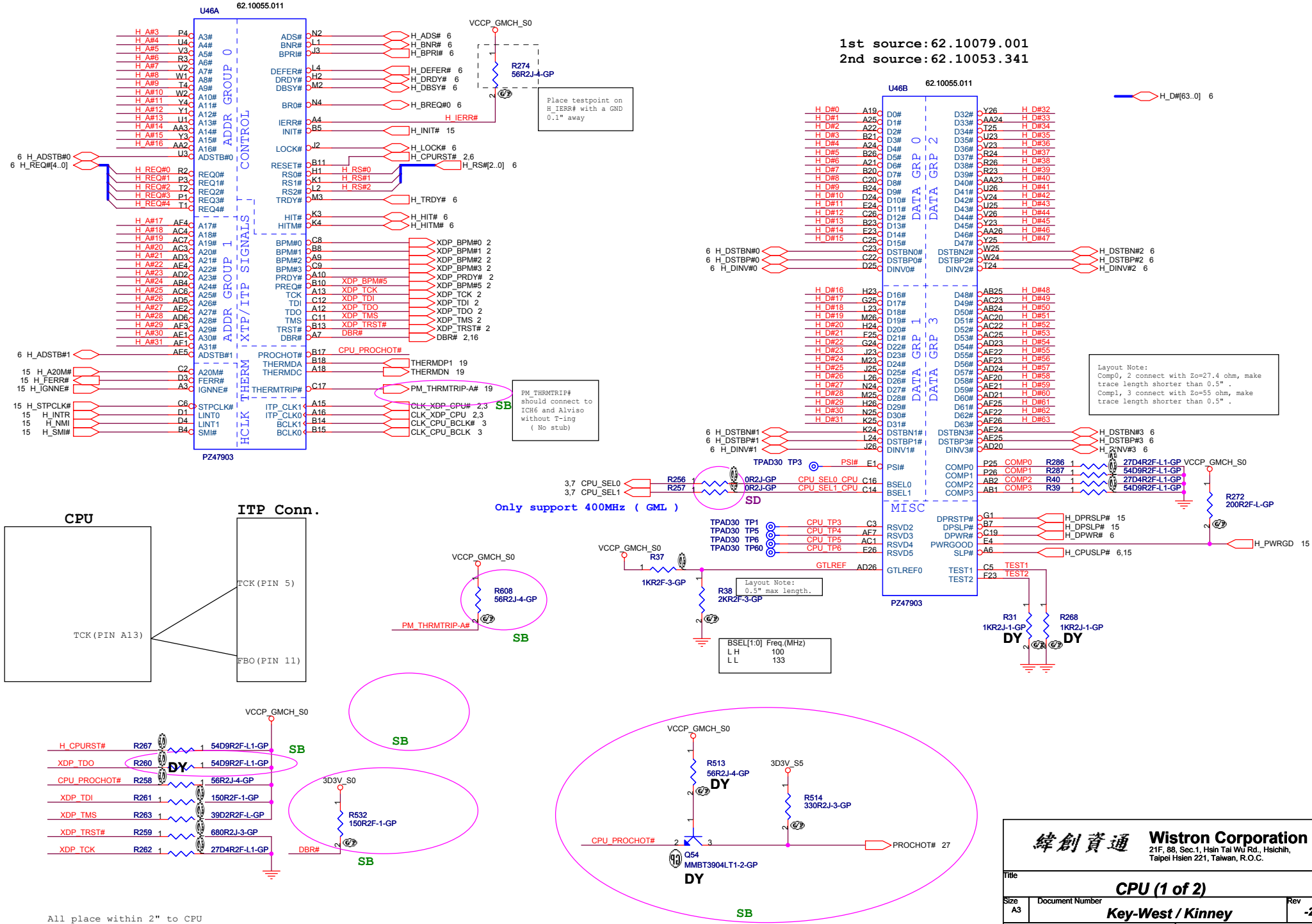
Place testpoint on H_IERR# with a GND 0.1" away

Layout Note:
Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5".
Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5".

Only support 400MHz (GML)

Layout Note:
0.5" max length.

BSEL[1:0] Freq.(MHz)	
LH	100
LL	133



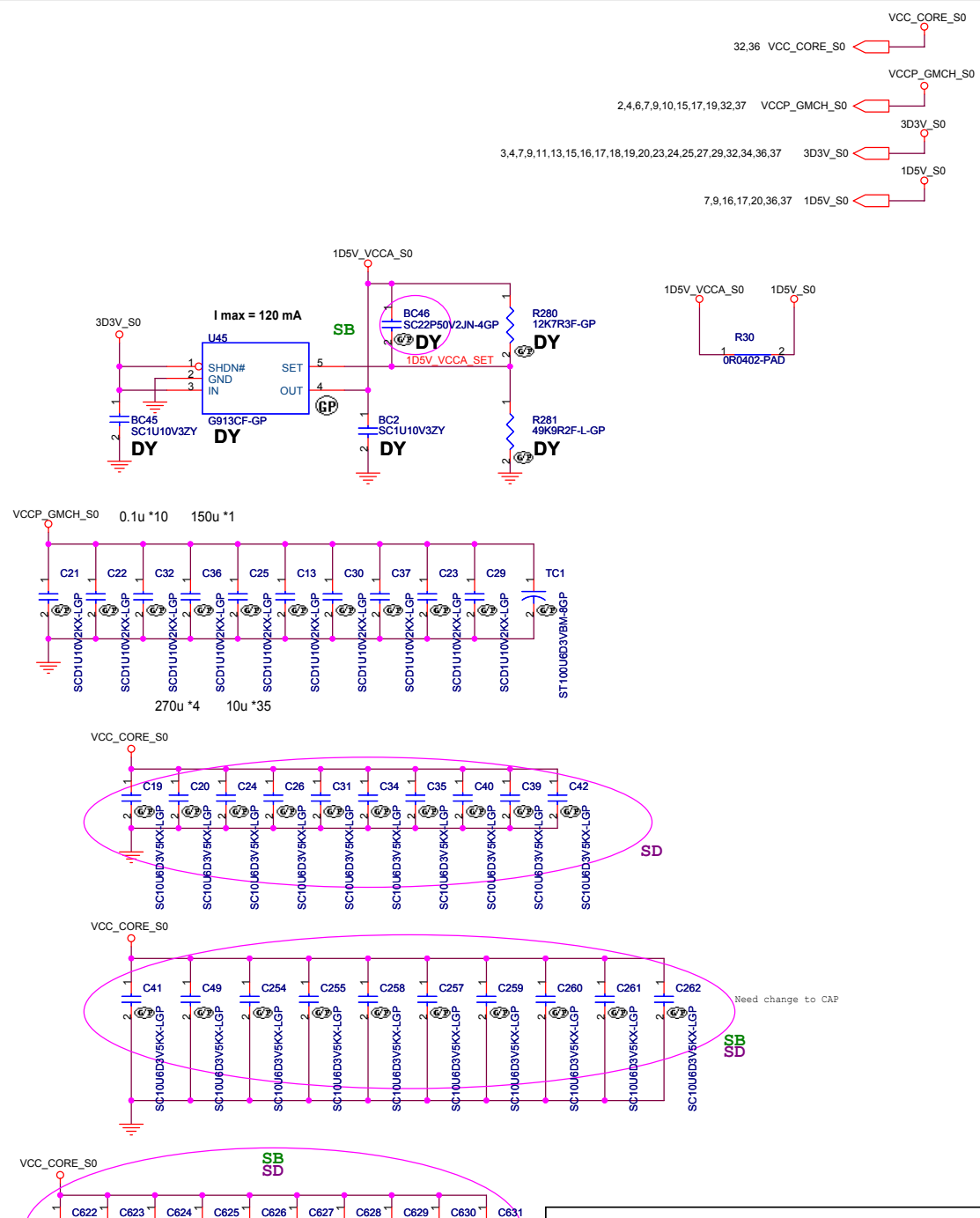
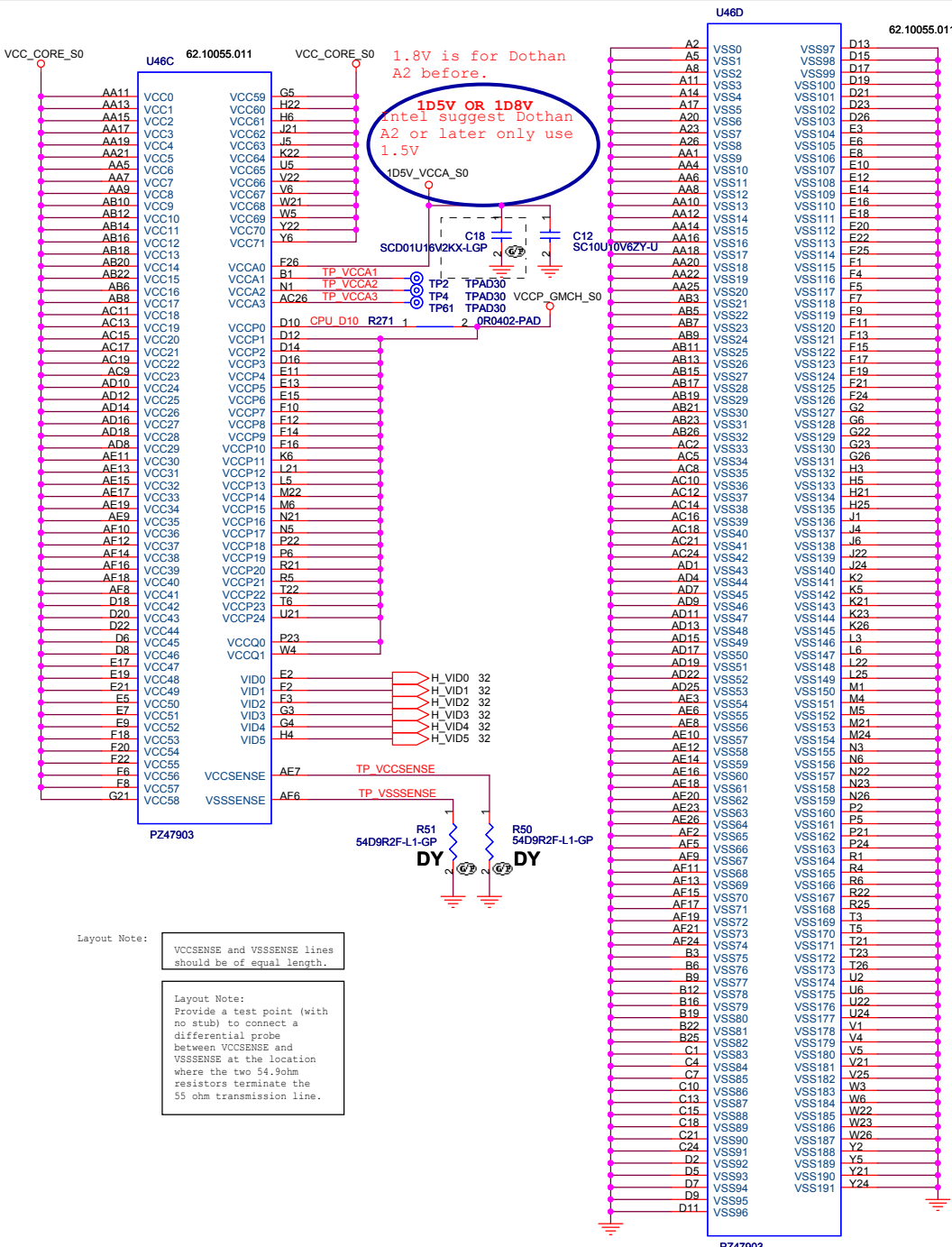
All place within 2" to CPU

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Title: **CPU (1 of 2)**

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Layout Note:
VCCSENSE and VSSSENSE lines should be of equal length.

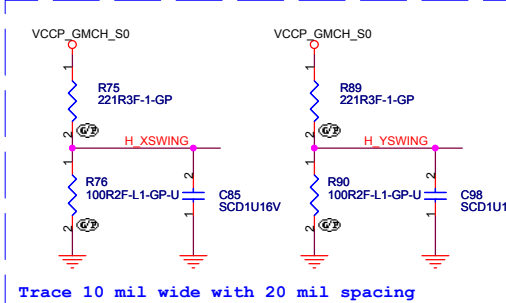
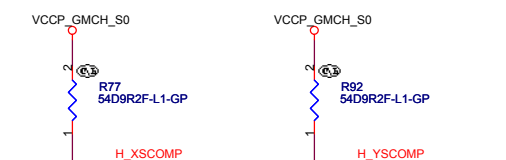
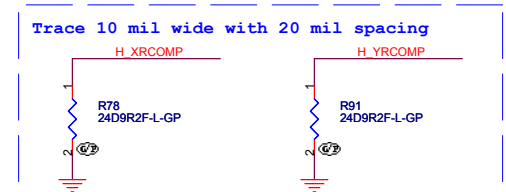
Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.

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CPU (2 of 2)

Key-West / Kinney

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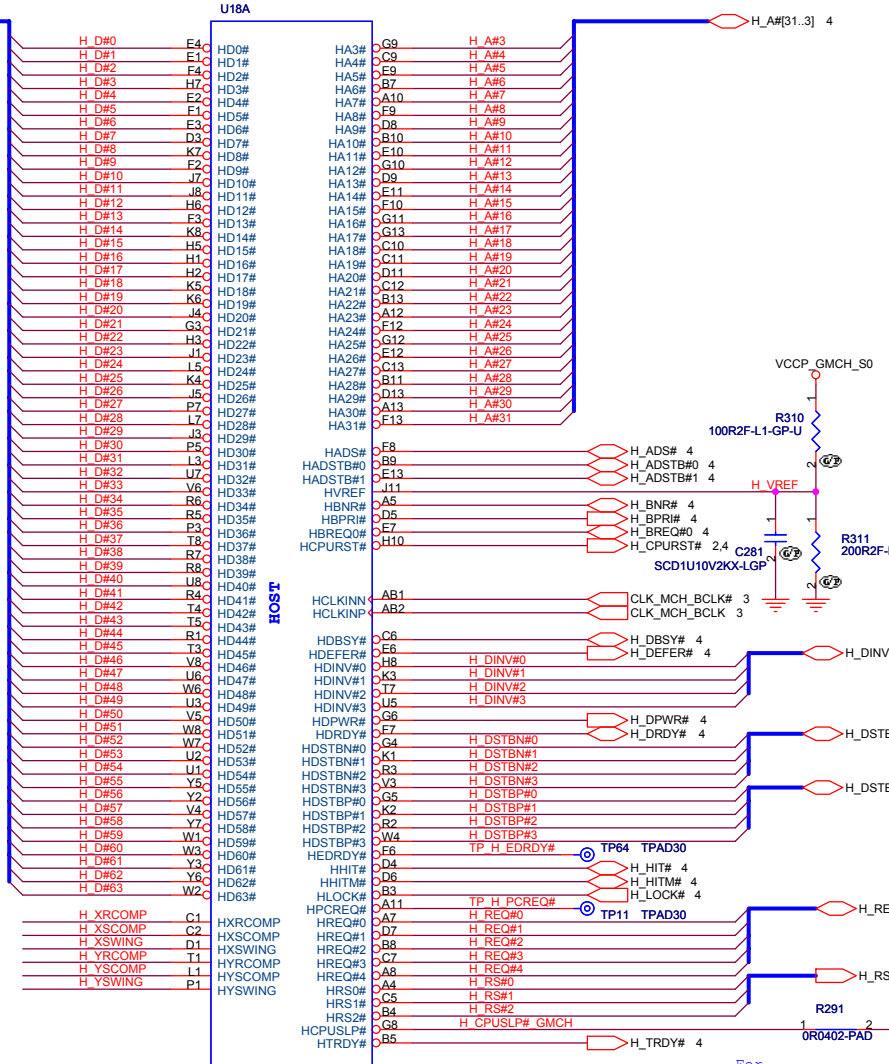


Alviso Strapping Signals and Configuration

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REF. NO. 15577 page 183

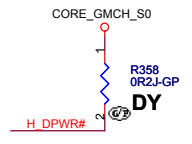
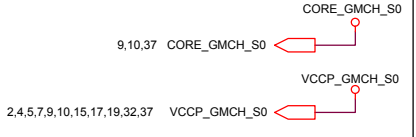
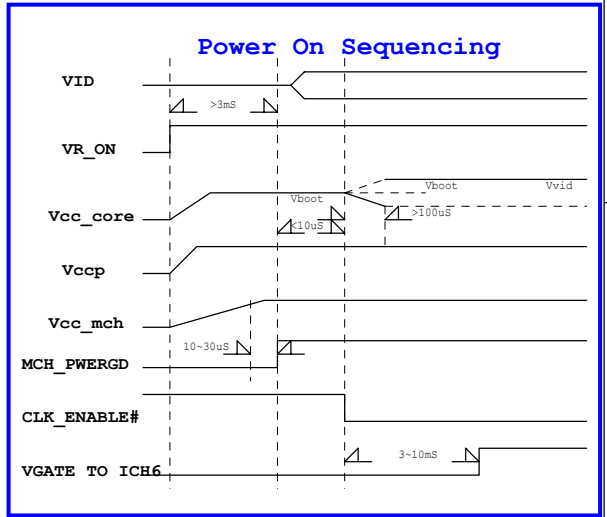
Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 101 = FSB400 others = Reversed
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	Reserved	0 = DDR2 (Default) 1 = DDR1
CFG7	CPU Strap	0 = Reserved 1 = Dothan (Default)
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reserve Lanes 1 = Normal (Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG17	Reserved	
CFG18	GMCH core VCC Select	0 = 1.05V (Default) 1 = 1.5V
CFG19	CPU VTT Select	0 = 1.05V (Default) 1 = 1.2V
CFG20	Reserved	
SDVOCRTL_DATA	SDVO Present	0 = No SDVO device present (Default) 1 = SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORK In signal.



71.0GMCH.0J1
910GML (LF C1) : 71.0GMCH.M28
915GM (LF C1) : 71.0GMCH.M27

For Banias/Celeron-M: R291=DUMMY
For Dothan A: R291=DUMMY
For Dothan B: R291=0R



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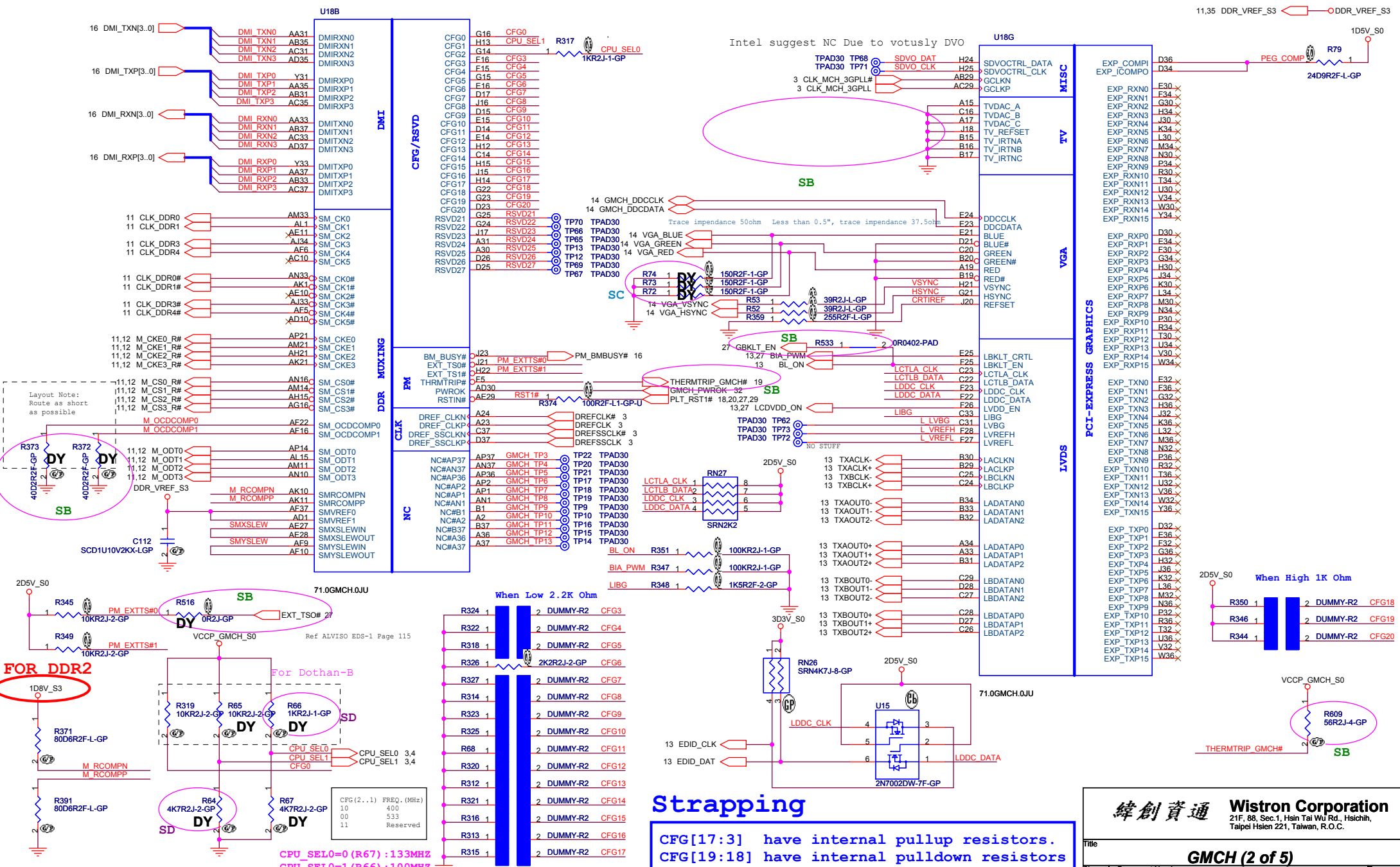
Title: **GMCH (1 of 5)**

Size: A3 Document Number: Key-West / Kinney Rev: -2

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3,4,5,9,11,13,15,16,17,18,19,20,23,24,25,27,29,32,34,36,37 3D3V_S0
 9,14,17,34,36 2D5V_S0
 9,10,11,12,16,34,35,36,37 1D8V_S3
 5,9,16,17,20,36,37 1D5V_S0
 2,4,5,6,9,10,15,17,19,32,37 VCCP_GMCH_S0
 11,35 DDR_VREF_S3

Alviso will provide SDVO_CTRLCLK and CTRLDATA pulldowns on-die



Strapping

CFG[17:3] have internal pullup resistors.
 CFG[19:18] have internal pulldown resistors

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Title: **GMCH (2 of 5)**

Size: A3 Document Number: Key-West / Kinney Rev: -2

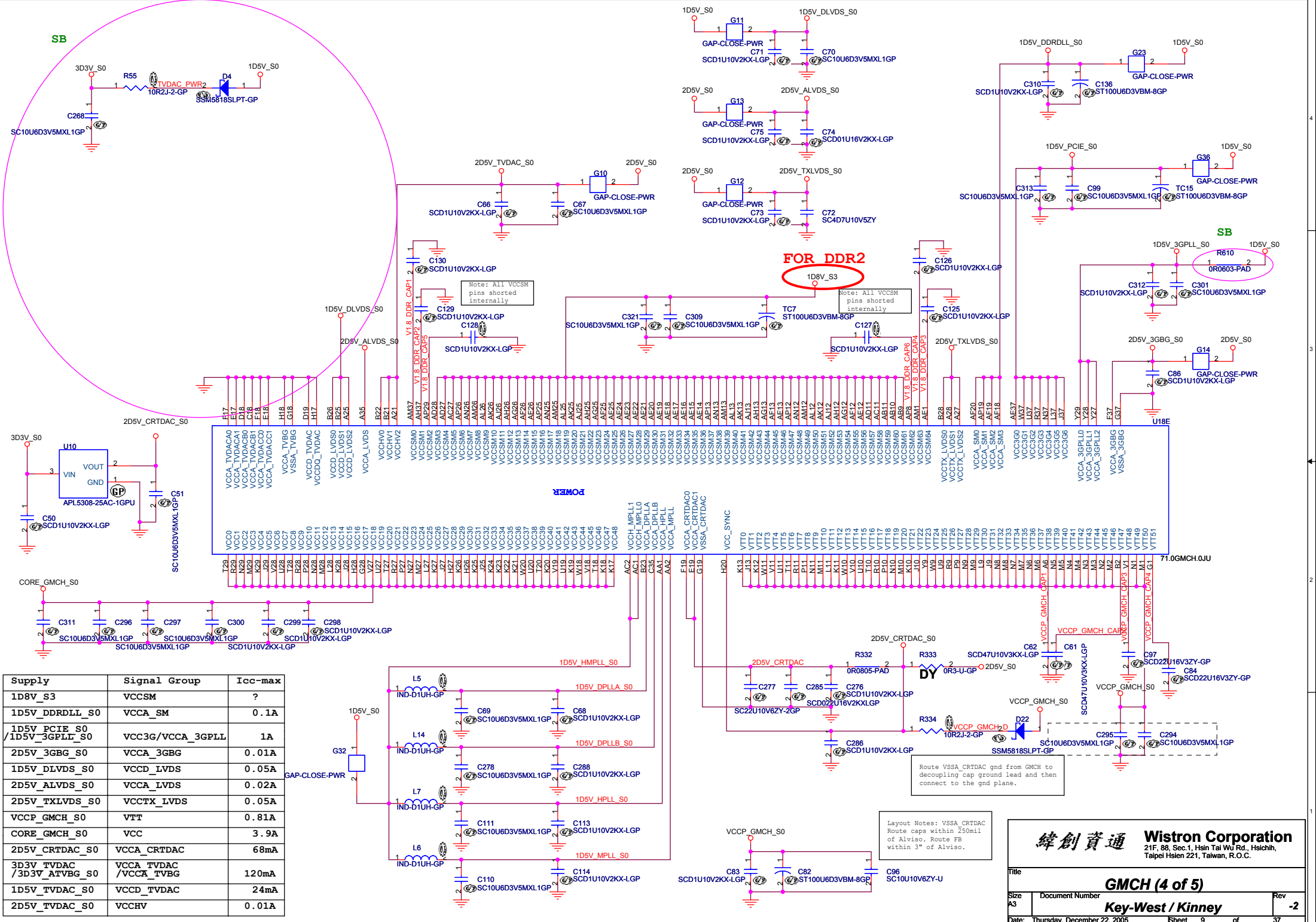
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SUPPORT DDRII 400



71.0GMCH.0JU

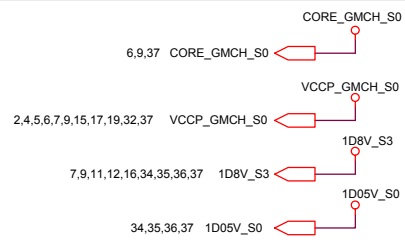
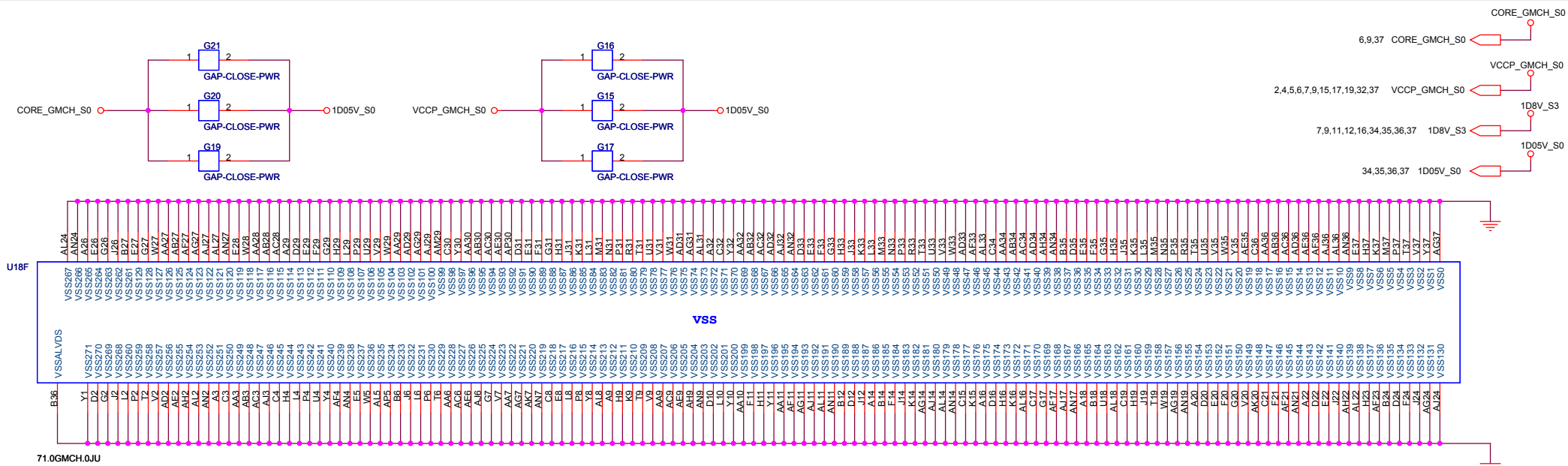
71.0GMCH.0JU



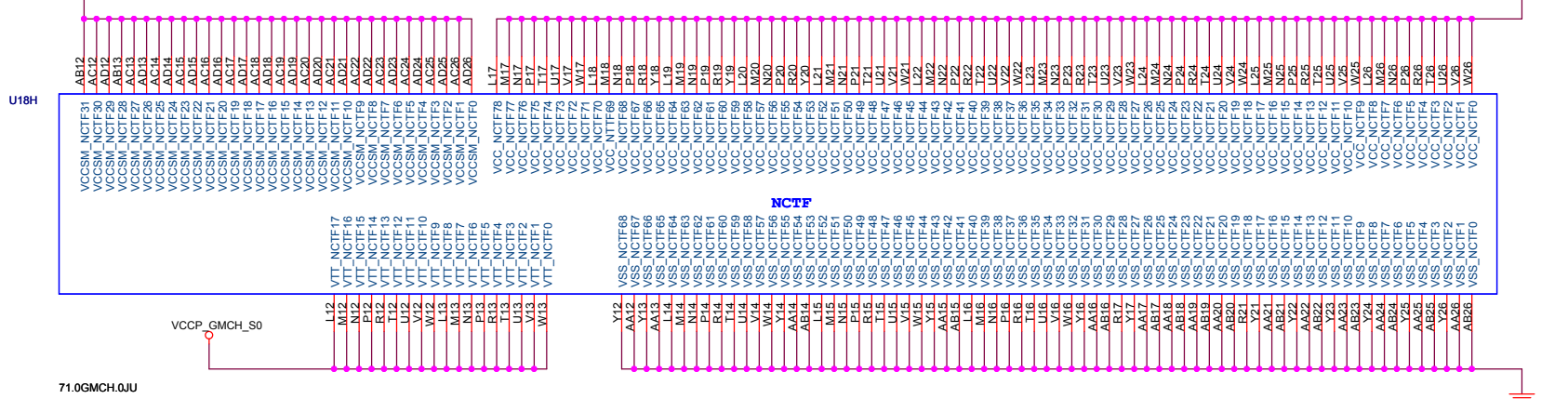
Supply	Signal Group	Icc-max
1D8V_S3	VCCSM	?
1D5V_DDRDLL_S0	VCCA_SM	0.1A
1D5V_PCIE_S0 /1D5V_3GPLL_S0	VCC3G/VCCA_3GPLL	1A
2D5V_3GBG_S0	VCCA_3GBG	0.01A
1D5V_DLVDS_S0	VCCD_LVDS	0.05A
2D5V_ALVDS_S0	VCCA_LVDS	0.02A
2D5V_TXLVDS_S0	VCCTX_LVDS	0.05A
VCCP_GMCH_S0	VTT	0.81A
CORE_GMCH_S0	VCC	3.9A
2D5V_CRTDAC_S0	VCCA_CRTDAC	68mA
3D3V_TVDAC	VCCA_TVDAC	
/3D3V_ATVBS_S0	VCCA_TVBS	120mA
1D5V_TVDAC_S0	VCCD_TVDAC	24mA
2D5V_TVDAC_S0	VCCHV	0.01A

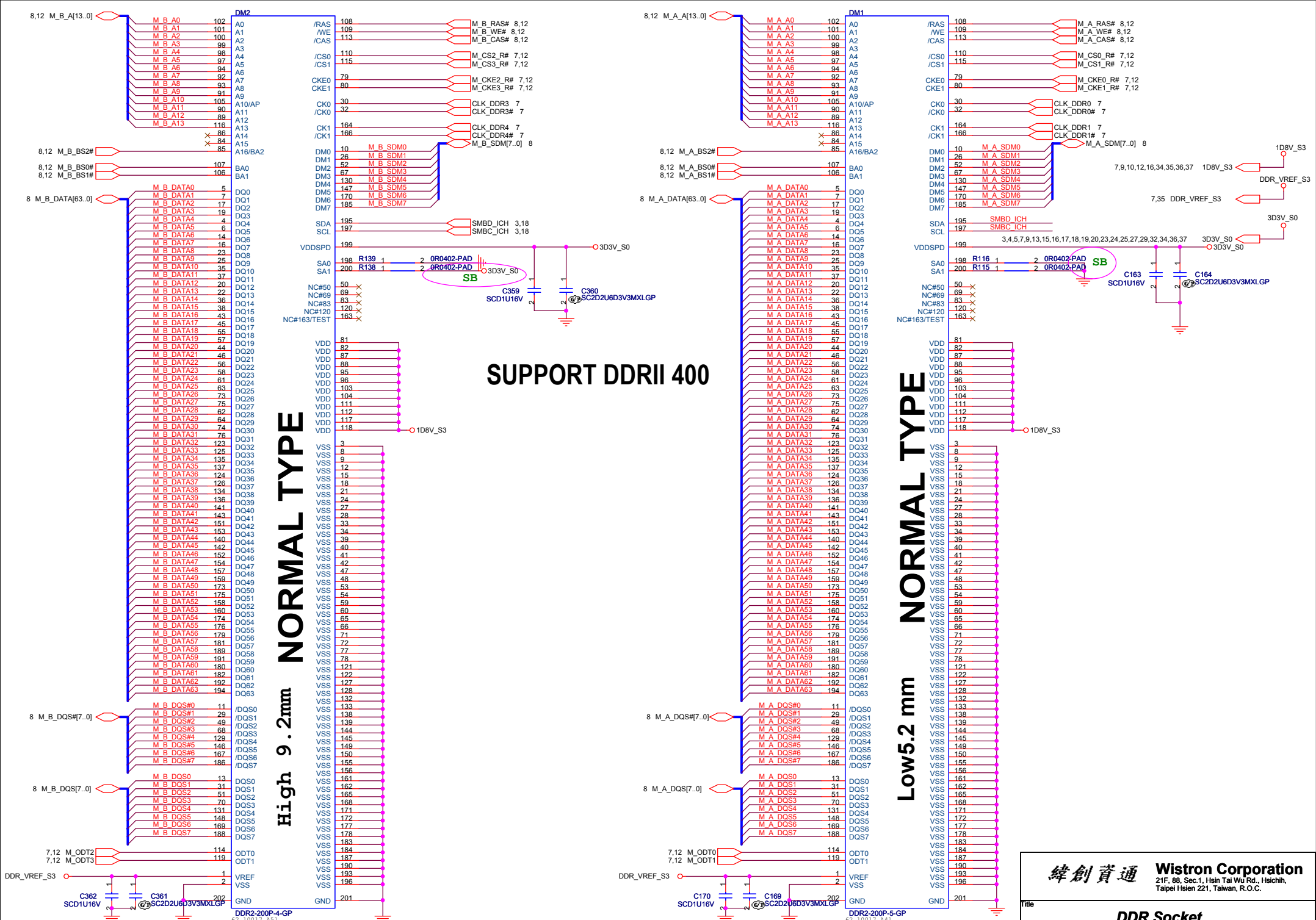
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GMCH (4 of 5)
 Title
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FOR DDR2





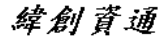
SUPPORT DDRII 400

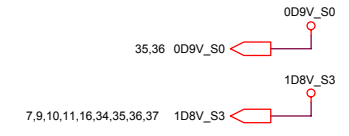
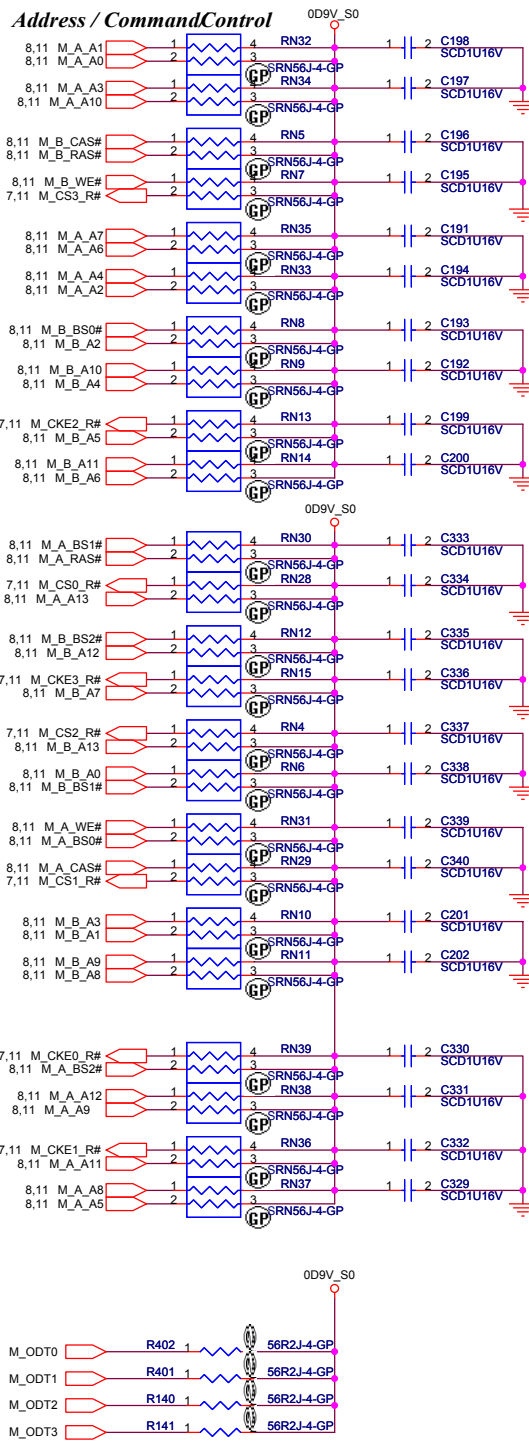
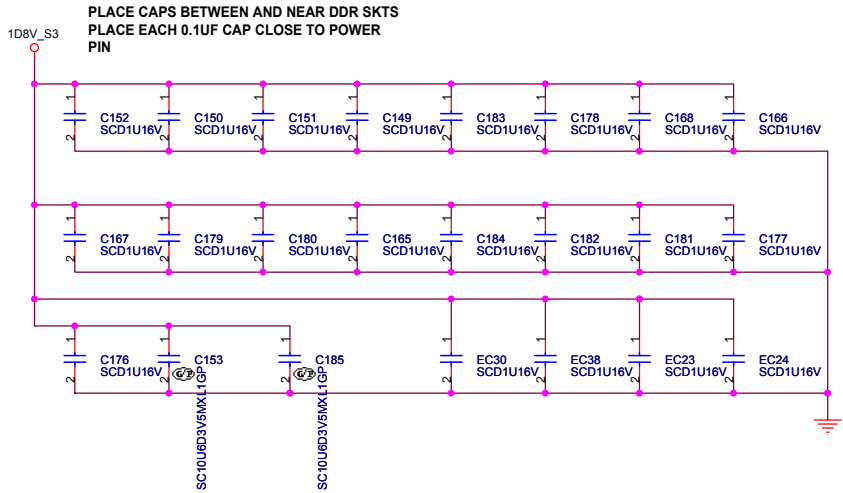
High 9.2mm NORMAL TYPE

Low5.2 mm NORMAL TYPE

Hi 9.2mm 1st source:62.10017.A51
2nd source:62.10017.A61

1st source:62.10017.A41
2nd source:62.10017.B01

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DDR Socket		
Size Custom	Document Number	Rev -2
Key-West / Kinney		
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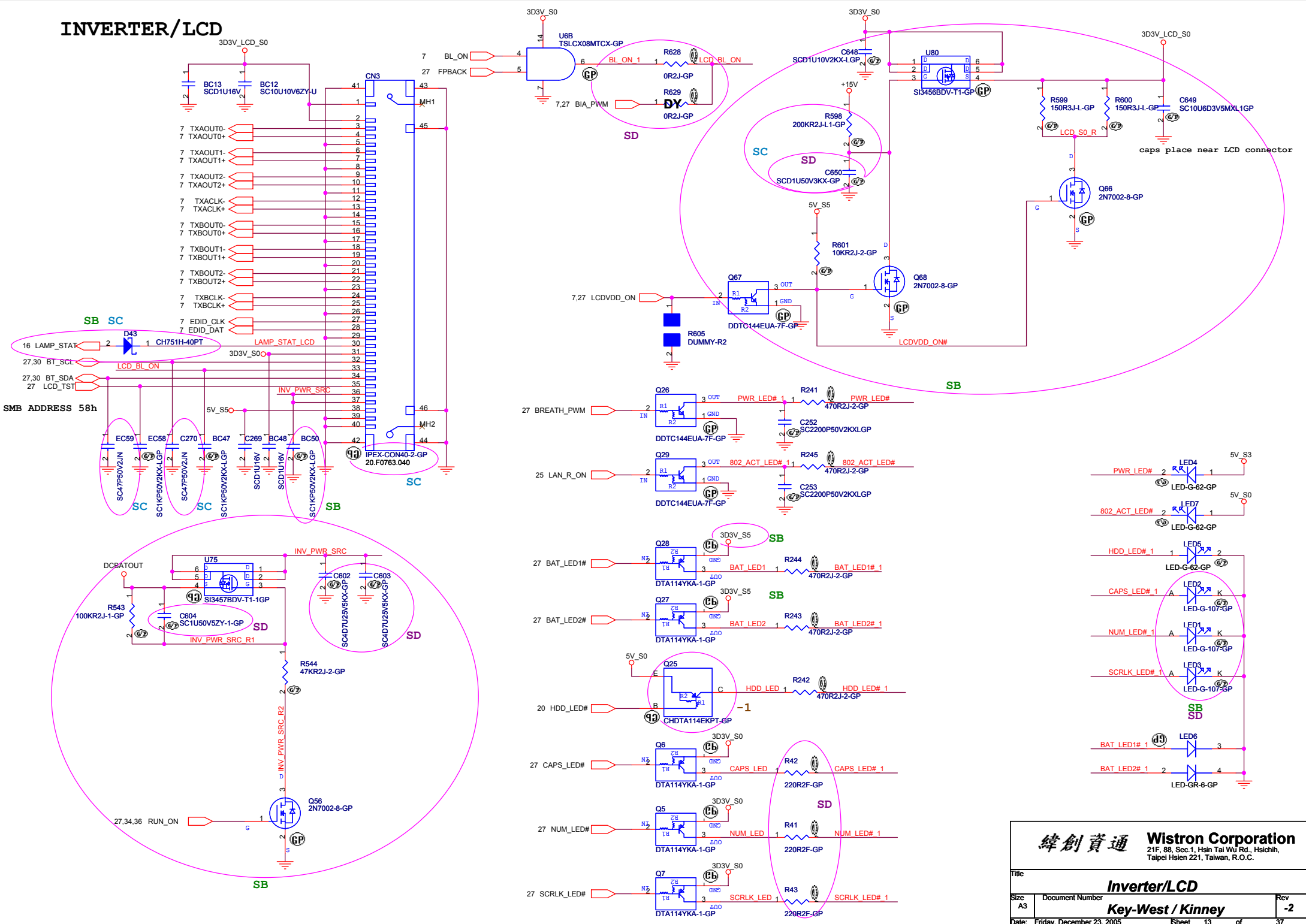


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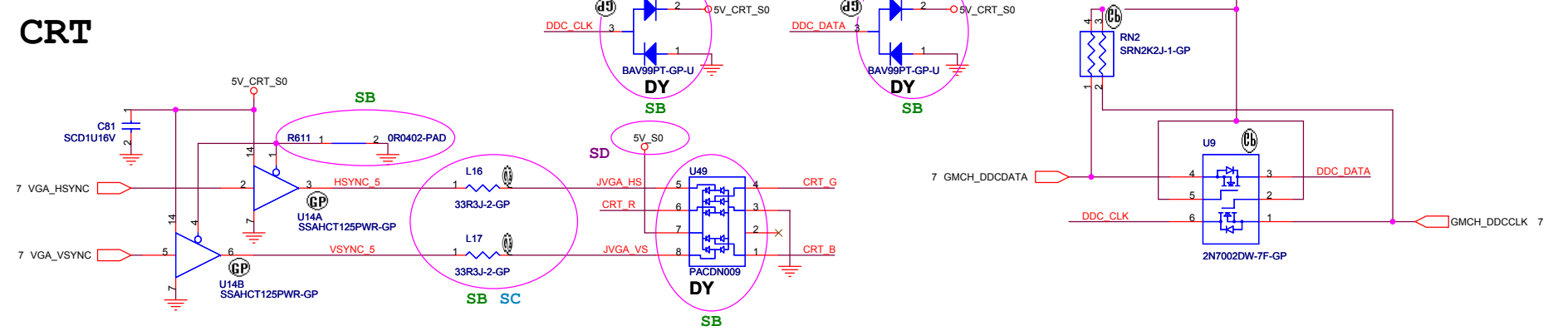
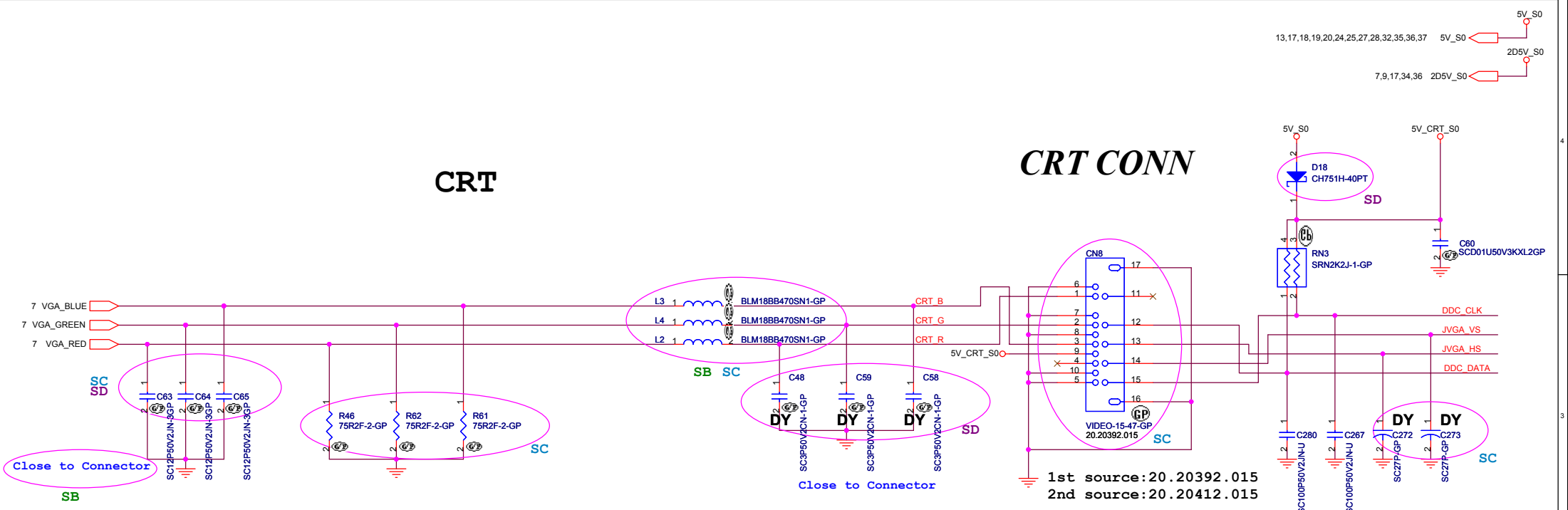
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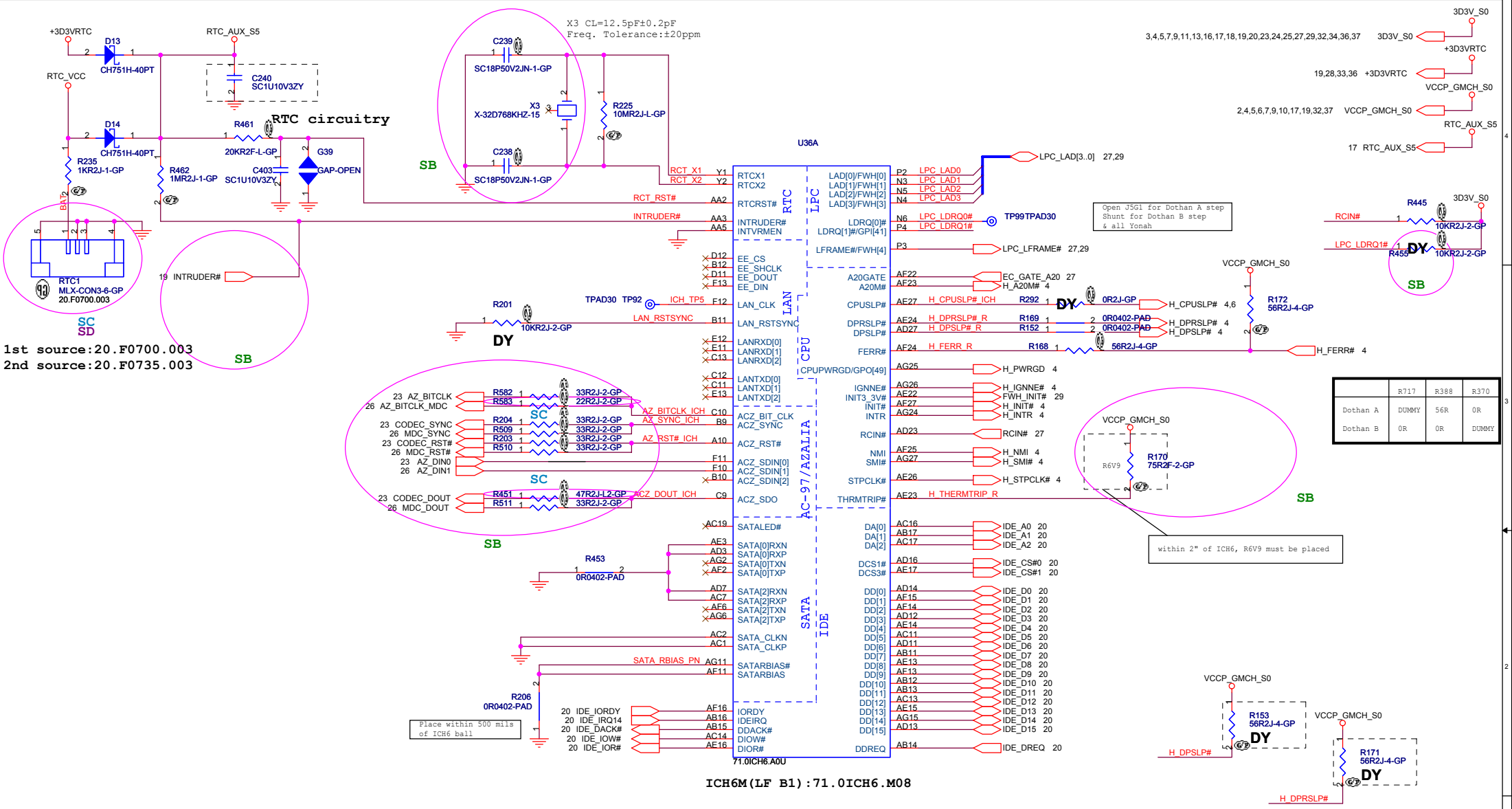
Size	Document Number	Rev
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INVERTER/LCD



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Title	
Inverter/LCD	
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Rev -2	





1st source: 20.F0700.003
 2nd source: 20.F0735.003

	R171	R388	R370
Dothan A	DUMMY	56R	0R
Dothan B	0R	0R	DUMMY

Place within 500 mils of ICH6 ball

Open J5G1 for Dothan A step
 Shunt for Dothan B step
 & all Yonah

within 2" of ICH6, R6V9 must be placed

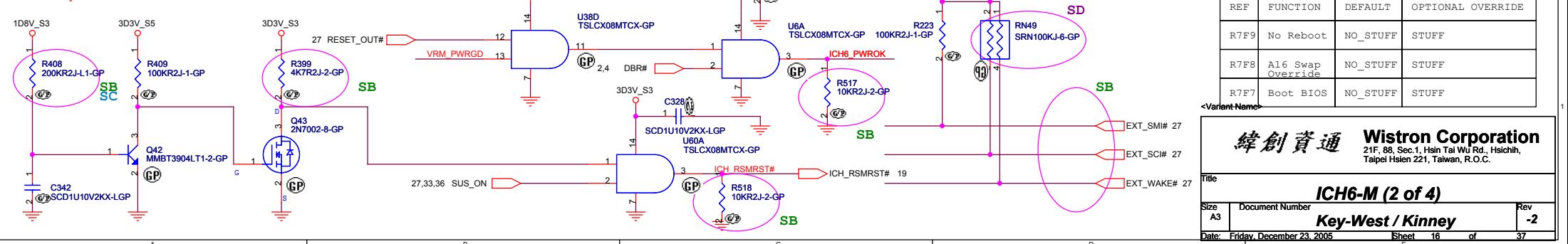
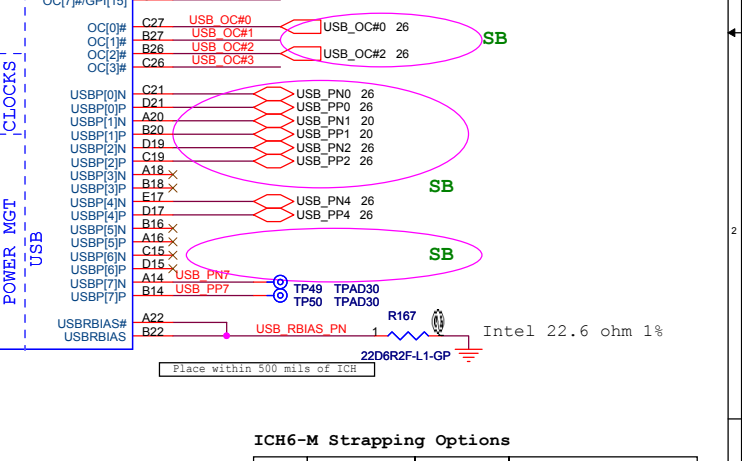
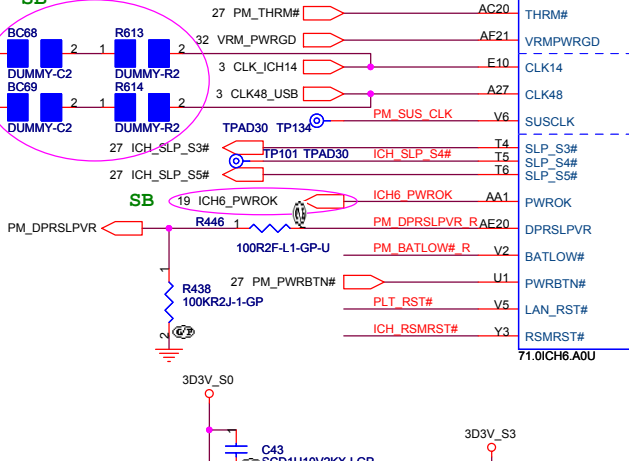
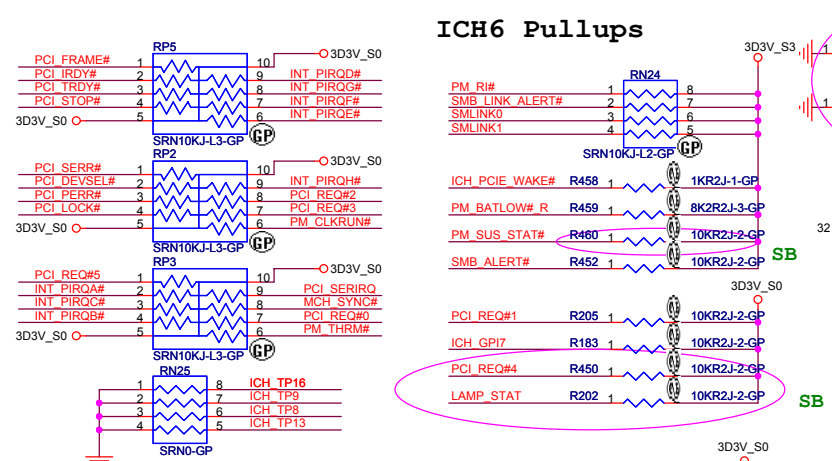
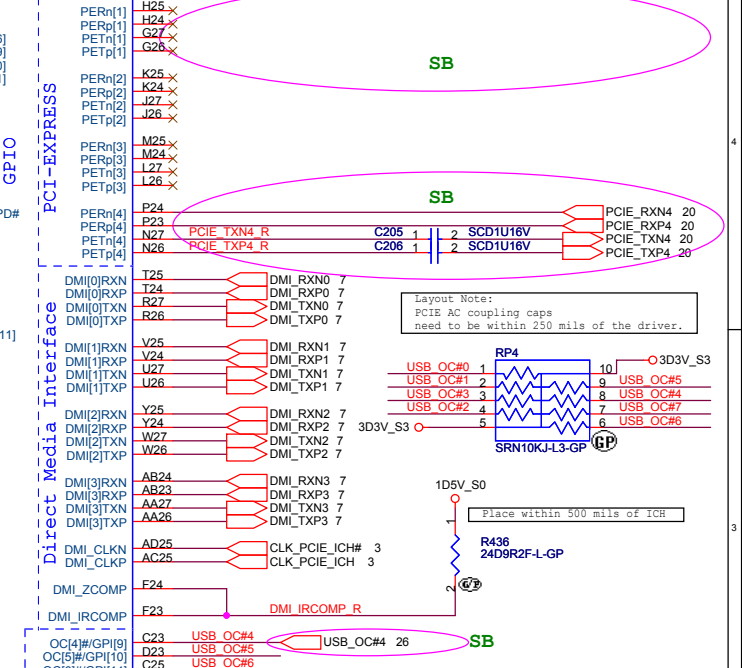
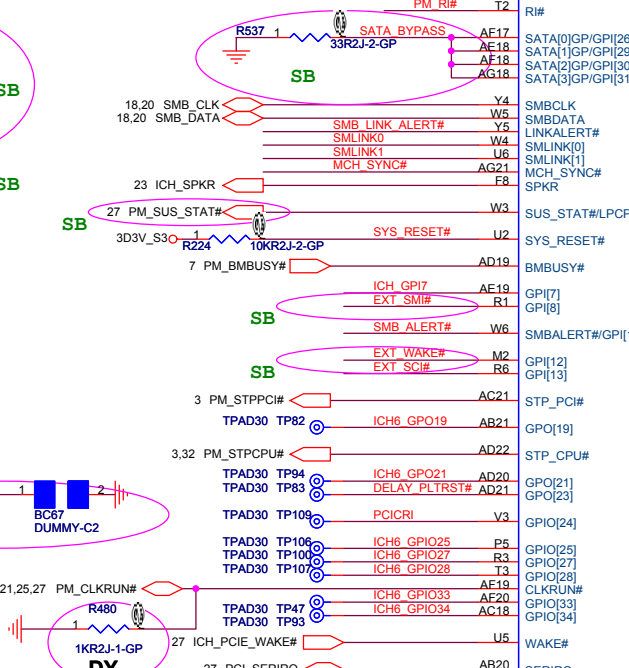
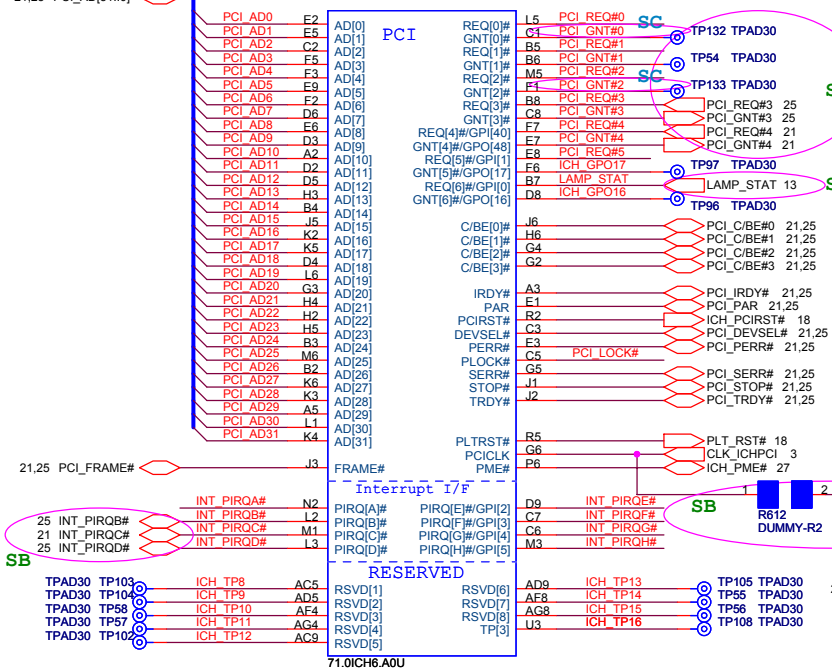
ICH6M (LF B1) : 71.0 ICH6.M08

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 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **ICH6-M (1 of 4)**

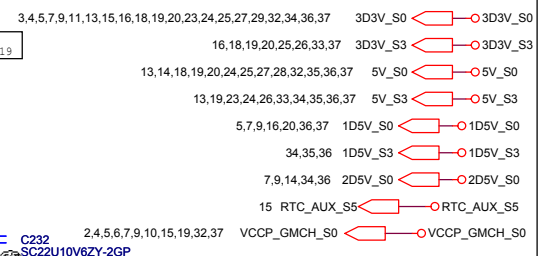
Size: A3 Document Number: **Key-West / Kinney** Rev: **-2**

Date: Friday, December 23, 2005 Sheet 15 of 37

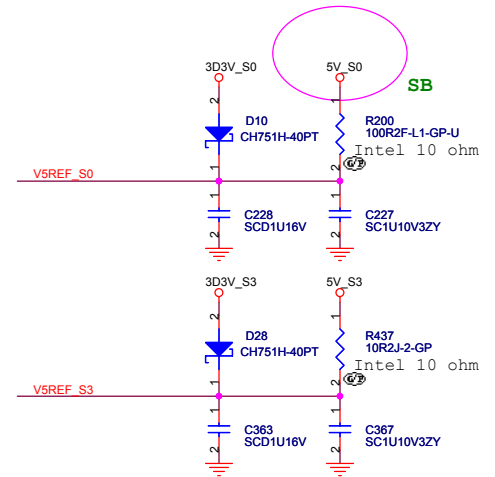


Layout Note:
Place above caps within
100 mils of ICH near F27, P27, AG27

Layout Note:
Place near pin AA19



*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail



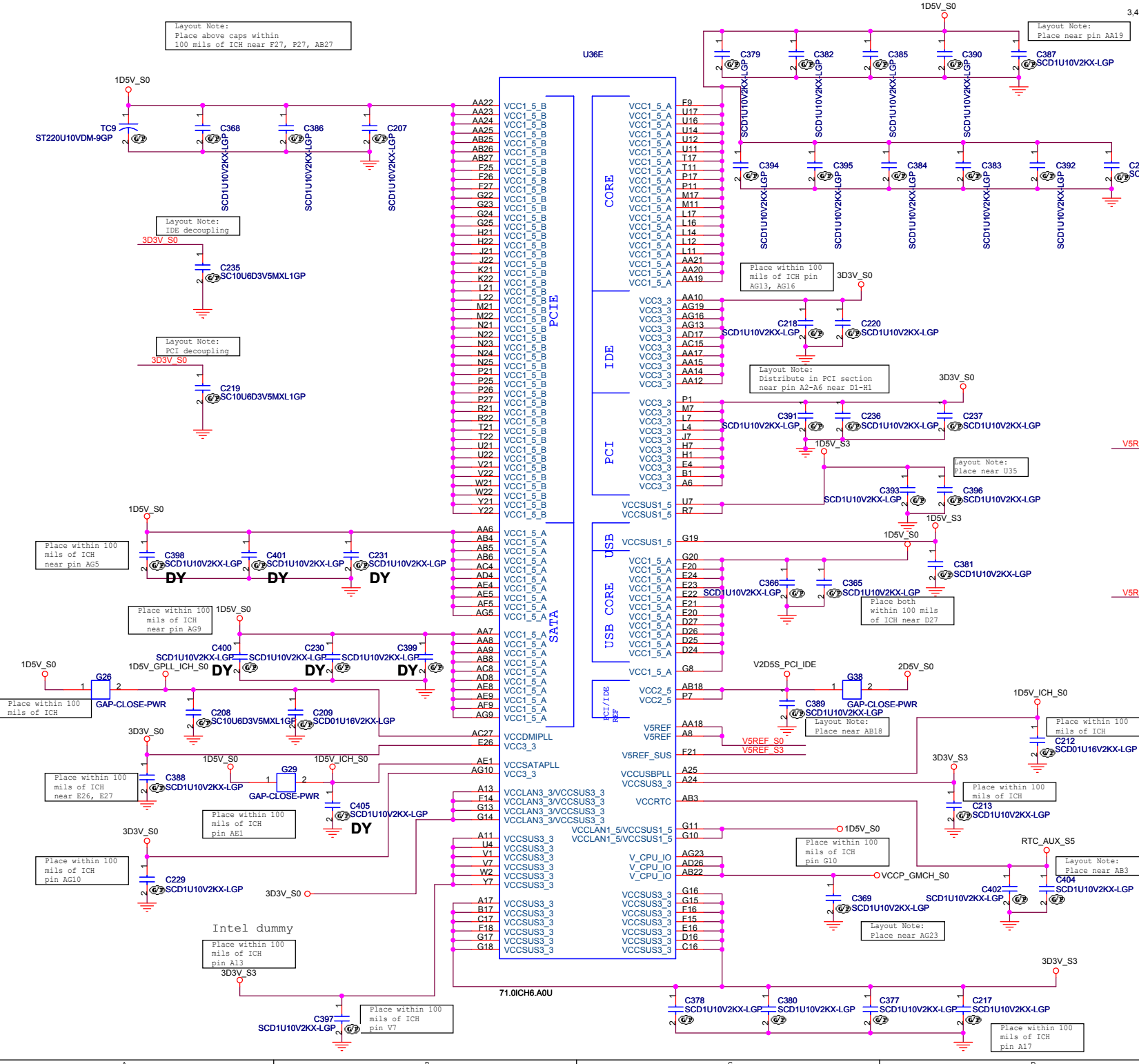
Supply	Signal Group	Icc-max
V5REF_S0	V5REF	0.001A
V5REF_S3	V5REF_SUS	0.01A
3D3V_S0	VCC3_3	0.19A
3D3V_S3	VCCSUS3_3 / VCCLAN3_3	0.39A
2D5V_S0	VCC2_5	0.01A
1D5V_S0	VCC1_5	2.95A
1D5V_S3	VCCSUS1_5 / VCCLANT_5	0.27A
VCCP_GMCH_S0	V_CPU_IO	0.014A
RTC_AUX_S5	VCCRTC	5uA

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Title: **ICH6-M (3 of 4)**

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Date: Friday, December 23, 2005 Sheet 17 of 37



Layout Note:
IDE decoupling

Layout Note:
PCI decoupling

Place within 100 mils of ICH pin AG13, AG16

Layout Note:
Distribute in PCI section near pin A2-A6 near D1-H1

Layout Note:
Place near U35

Place both within 100 mils of ICH near D27

Layout Note:
Place near AB18

Place within 100 mils of ICH

Place within 100 mils of ICH

Place within 100 mils of ICH pin G10

Layout Note:
Place near AB3

Layout Note:
Place near AG23

Place within 100 mils of ICH pin A17

Place within 100 mils of ICH near pin AG5

Place within 100 mils of ICH near pin AG9

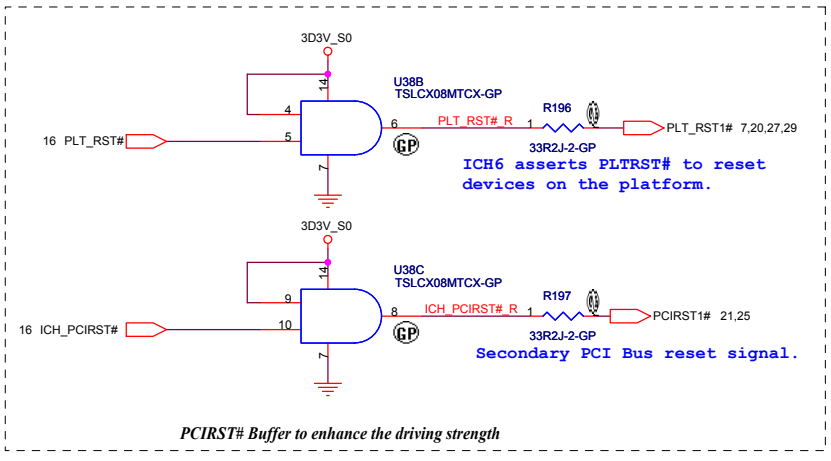
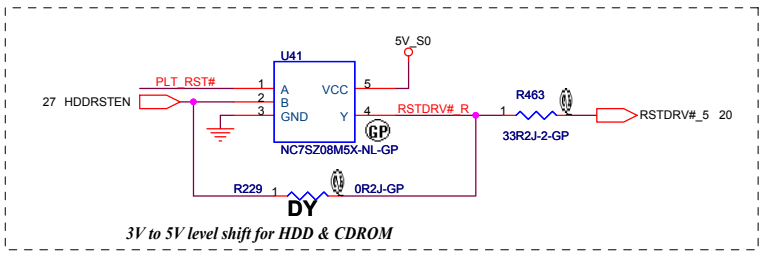
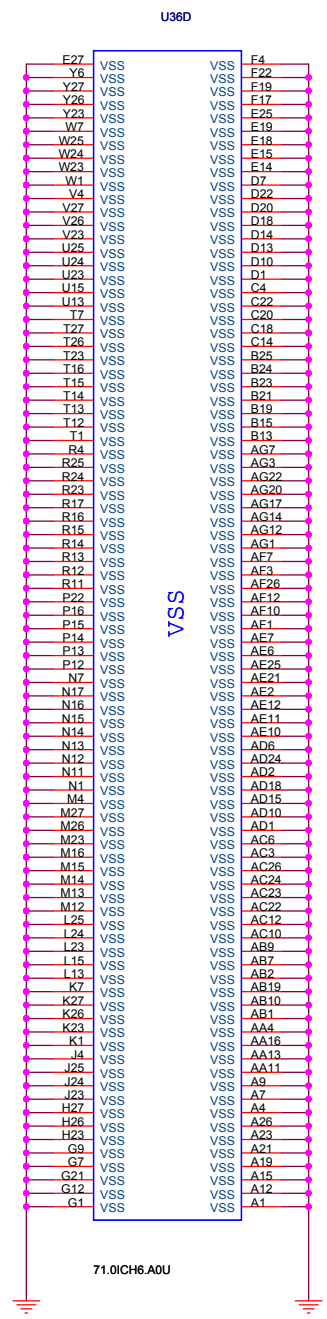
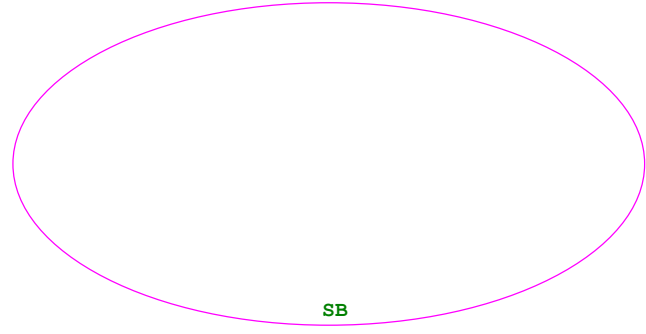
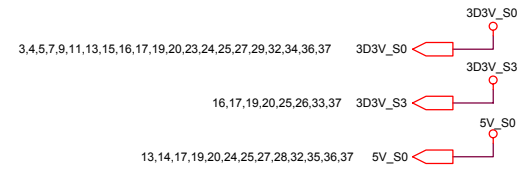
Place within 100 mils of ICH

Place within 100 mils of ICH near E26, E27

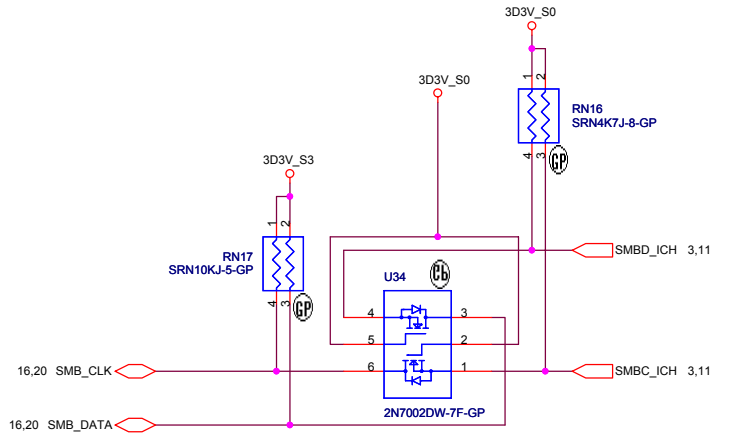
Place within 100 mils of ICH pin AG10

Intel dummy
Place within 100 mils of ICH pin A13

Place within 100 mils of ICH pin V7

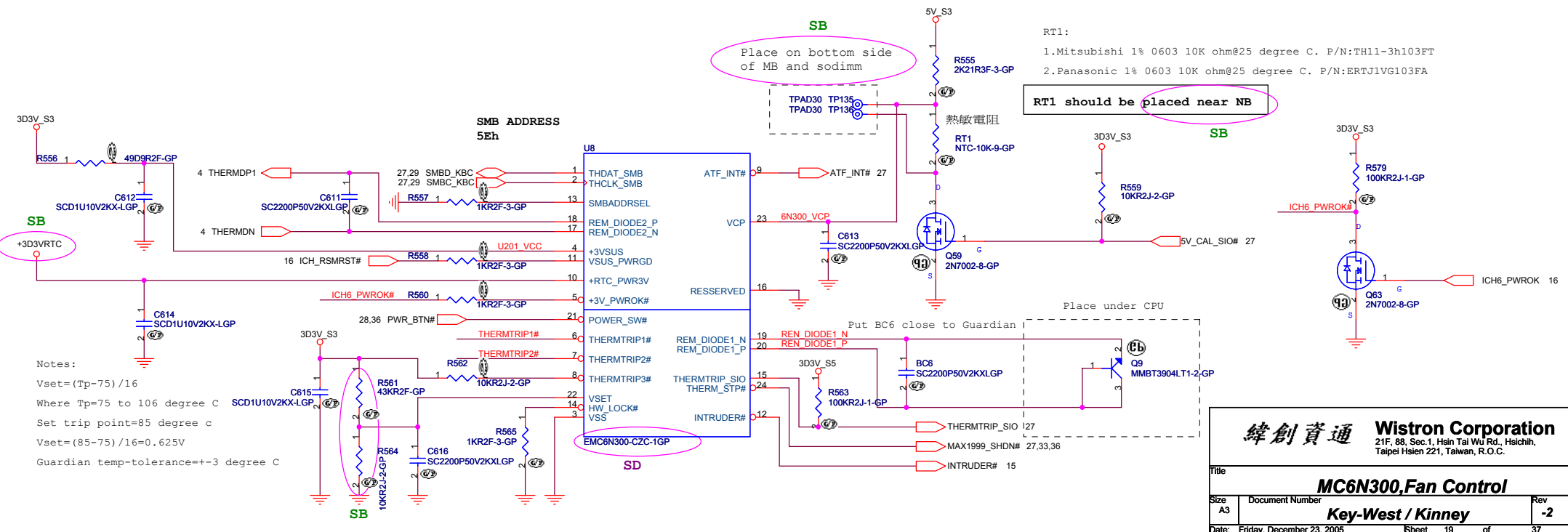
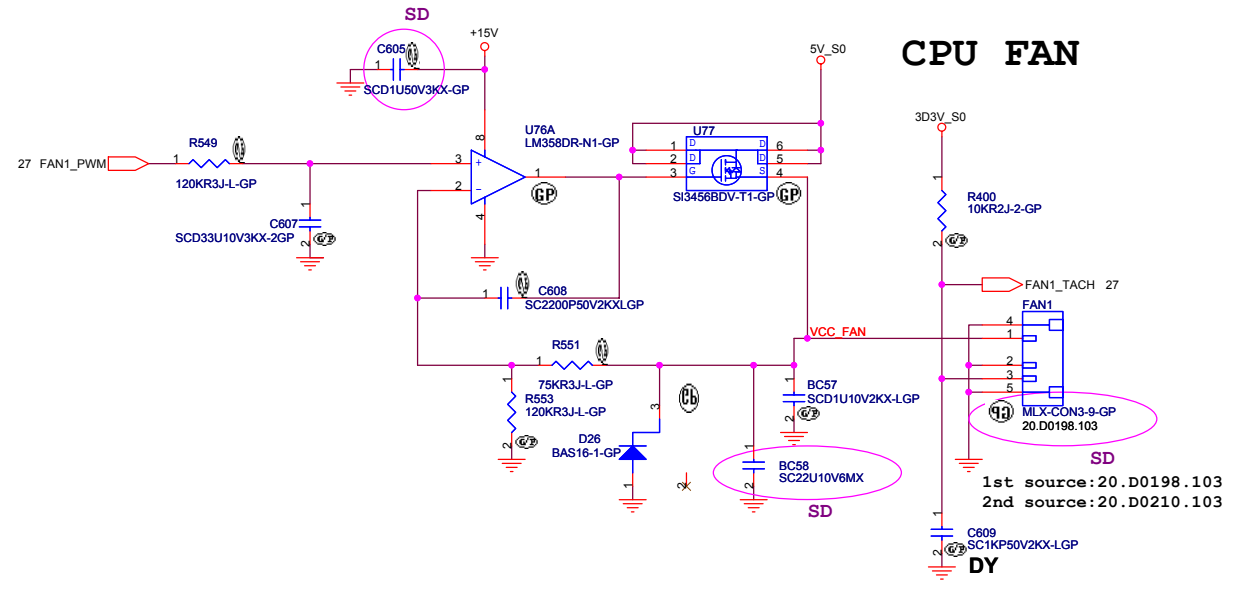
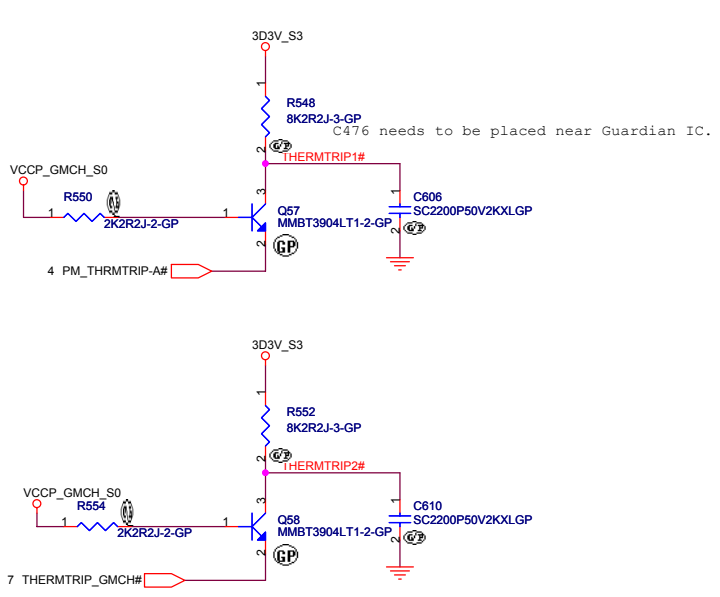


SMBUS (ICH6 ---> SODIMM, CLKGEN)



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Title: **ICH6-M (4 of 4)**
 Size: A3 Document Number: **Key-West / Kinney** Rev: **-2**
 Date: Friday, December 23, 2005 Sheet 18 of 37



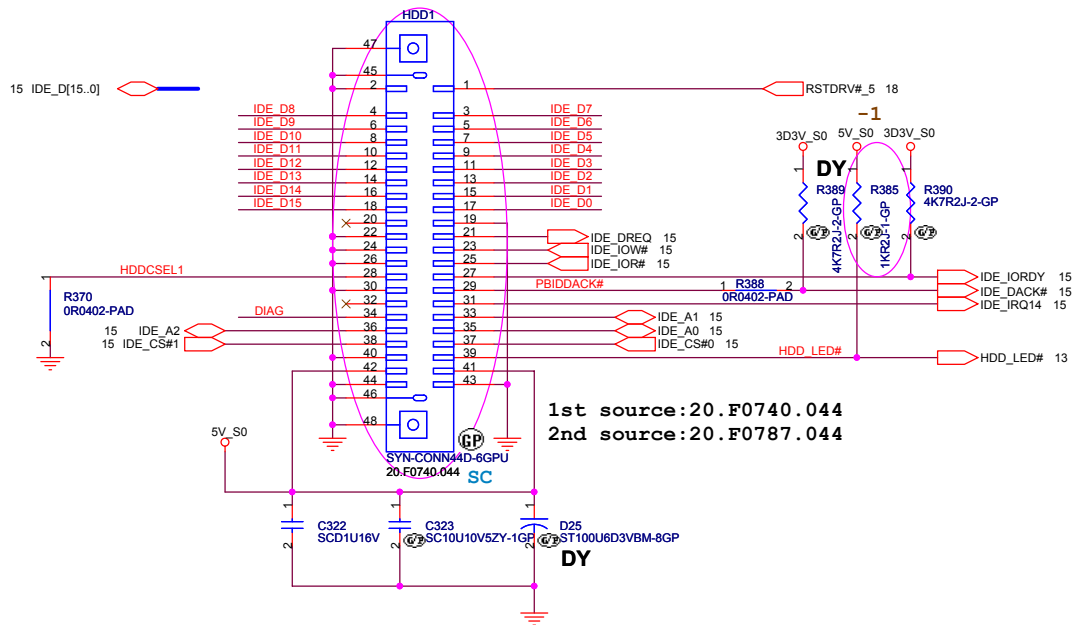
緯創資通 **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **MC6N300, Fan Control**

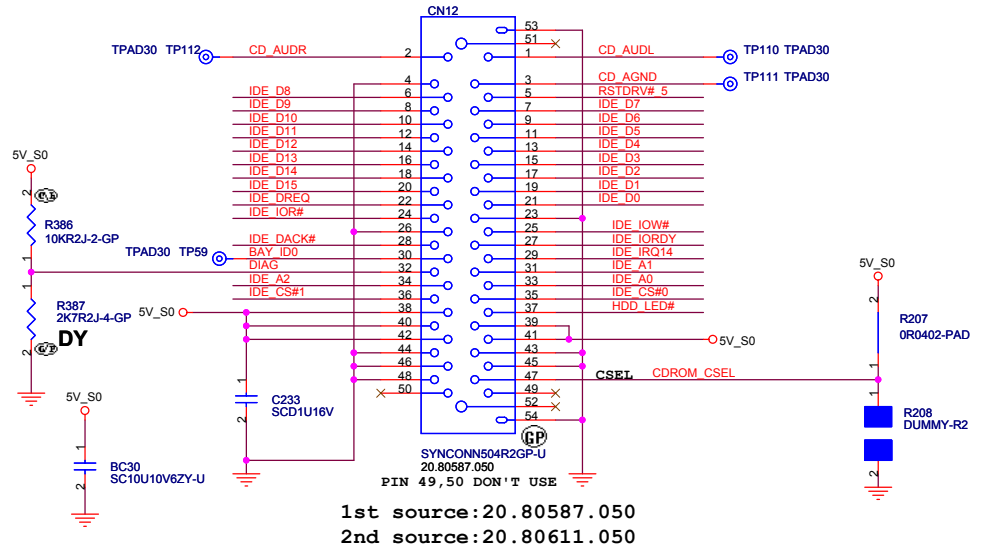
Size A3	Document Number	Rev -2
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Date: Friday, December 23, 2005 Sheet 19 of 37

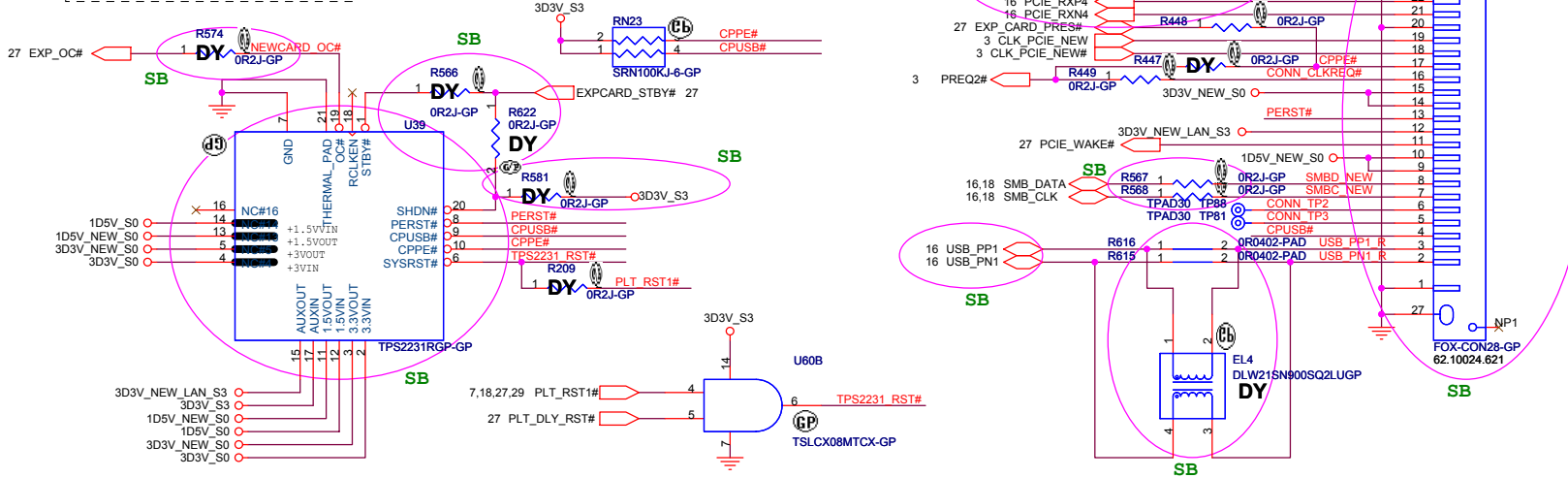
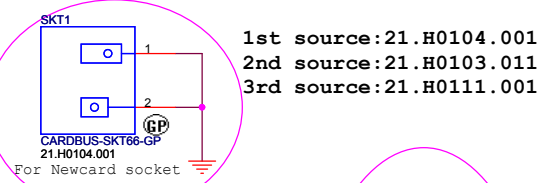
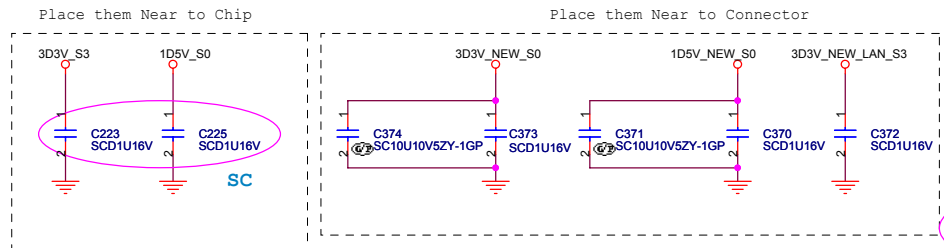
HDD Connector



CDROM



NEWCARD Connector



SMBUS (ICH6--NEWCARD, LAN)

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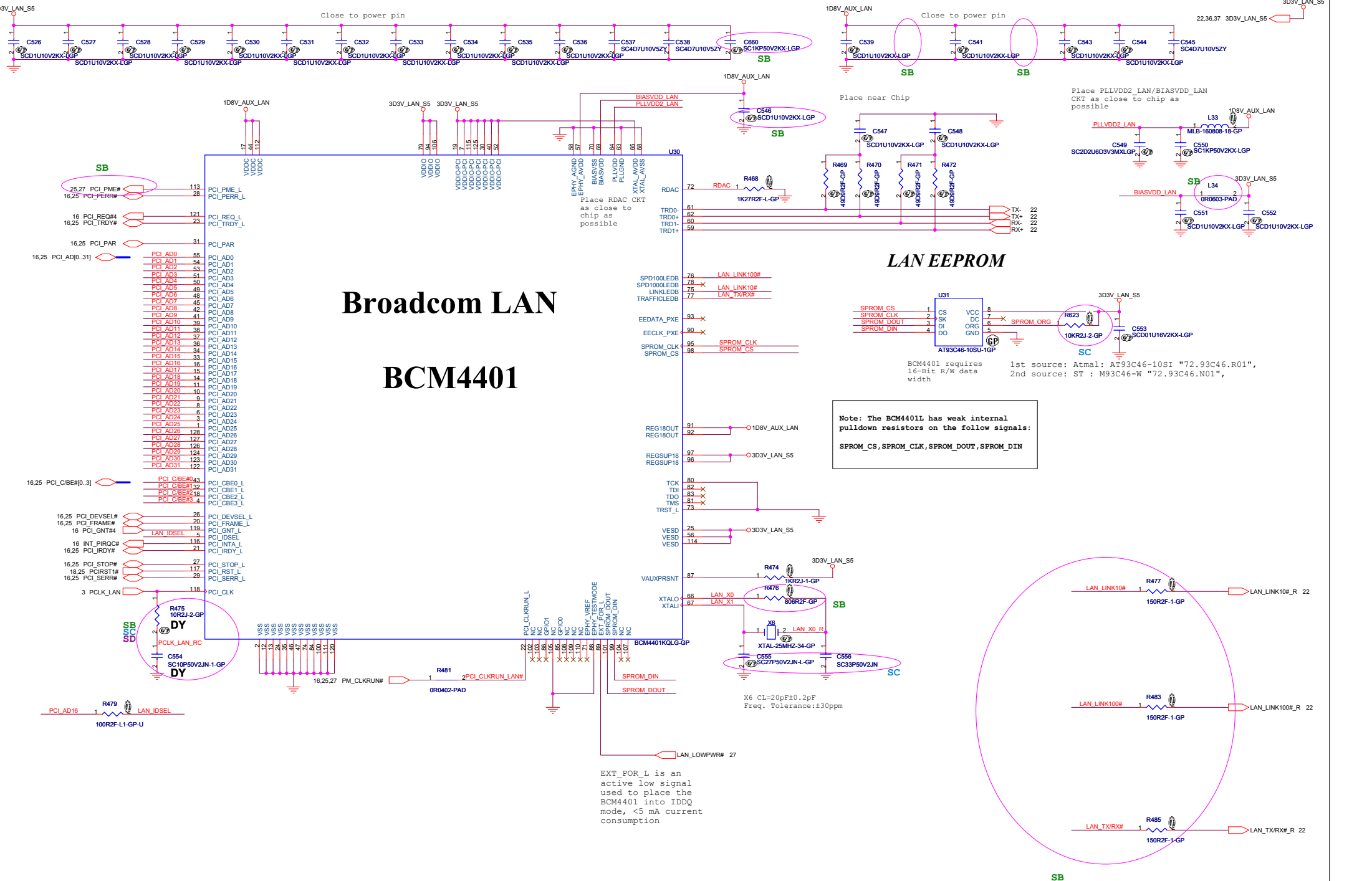
Title: **HDD / CDROM / NEW CARD**

Size: A3 Document Number: **Key-West / Kinney** Rev: -2

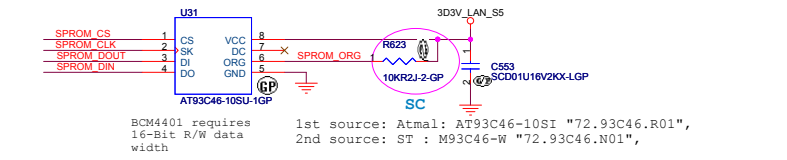
Date: Friday, December 23, 2005 Sheet: 20 of 37

Broadcom LAN

BCM4401



LAN EEPROM



BCM4401 requires 1st source: Atmel: AT93C46-10SI "72.93C46.R01", 16-Bit R/W data width
2nd source: ST : M93C46-W "72.93C46.N01",

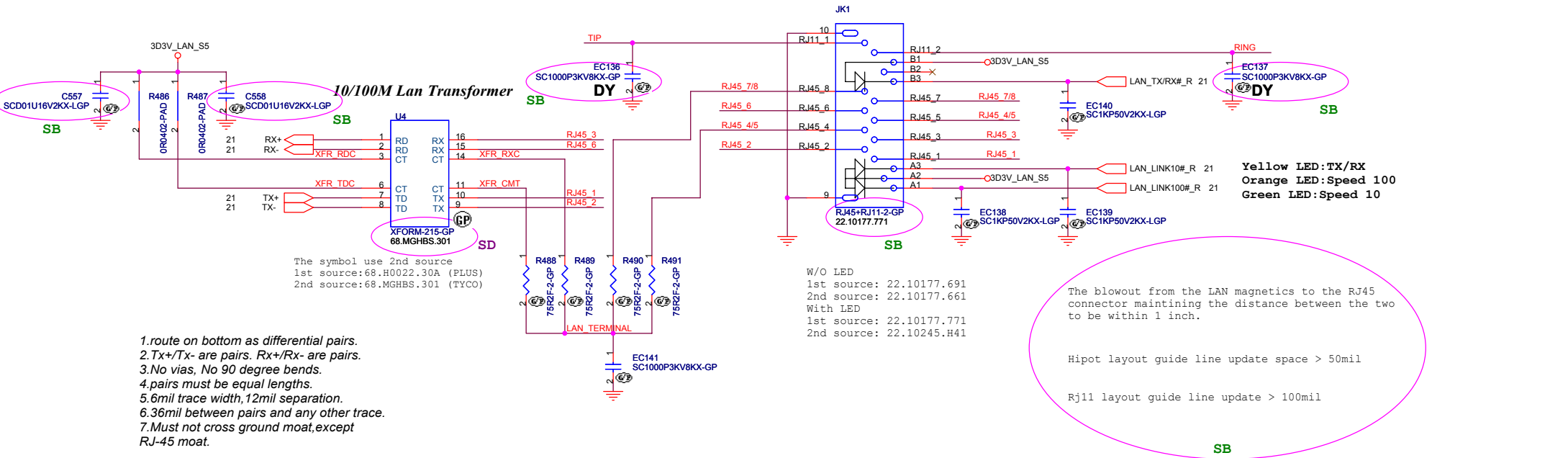
Note: The BCM4401L has weak internal pulldown resistors on the follow signals:
SPROM_CS, SPROM_CLK, SPROM_DOUT, SPROM_DIN

EXT_POR_L is an active low signal used to place the BCM4401 into IDDQ mode, <5 mA current consumption

Change LAN solution

LAN/MODEM CONN

21.36.37 3D3V_LAN_S5



The symbol use 2nd source
 1st source: 68.H0022.30A (PLUS)
 2nd source: 68.MGHBS.301 (TYCO)

1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

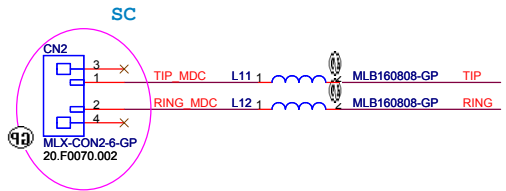
W/O LED
 1st source: 22.10177.691
 2nd source: 22.10177.661
 With LED
 1st source: 22.10177.771
 2nd source: 22.10245.H41

The blowout from the LAN magnetics to the RJ45 connector maintaining the distance between the two to be within 1 inch.

Hipot layout guide line update space > 50mil

Rj11 layout guide line update > 100mil

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6



Change LAN solution

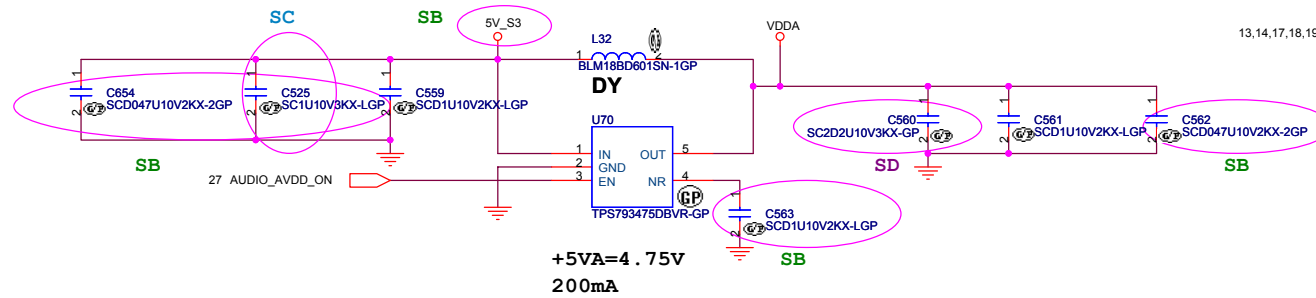
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
LAN Connector	
Size A3	Document Number
Key-West / Kinney	
Date: Friday, December 23, 2005	Sheet 22 of 37

+5VA

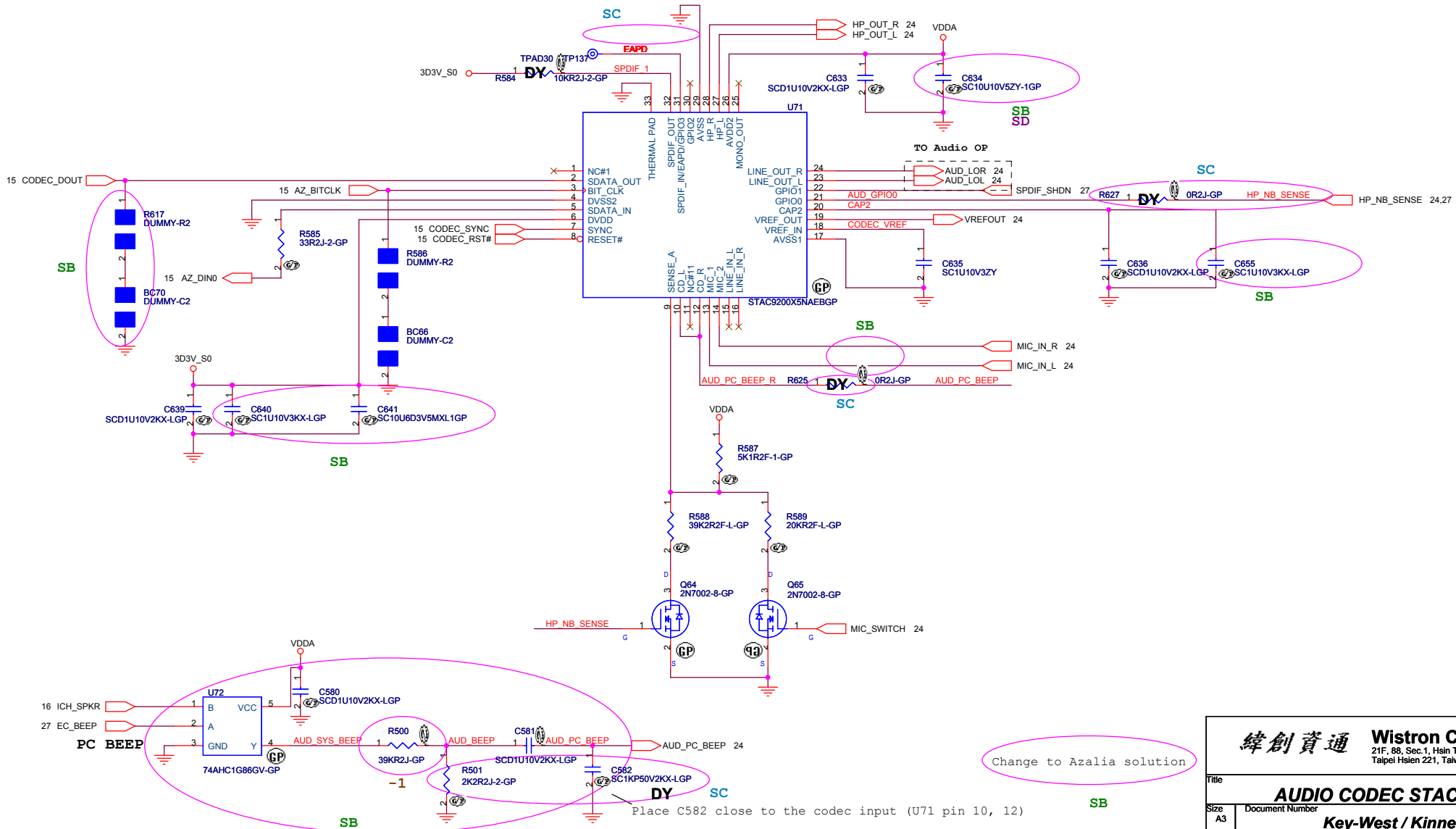
3,4,5,7,9,11,13,15,16,17,18,19,20,24,25,27,29,32,34,36,37 3D3V_S0

5V_S0

13,14,17,18,19,20,24,25,27,28,32,35,36,37 5V_S0



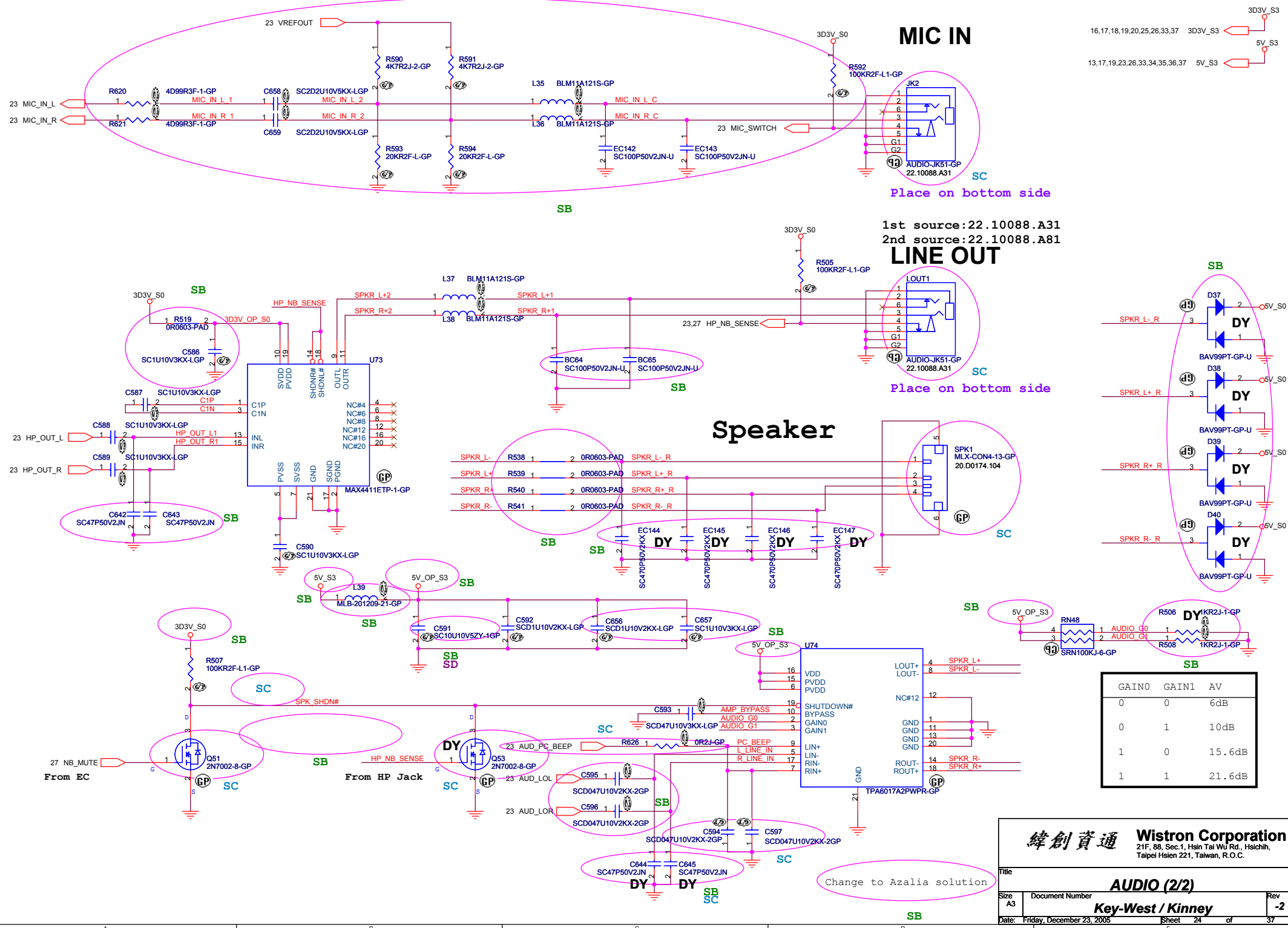
+5VA=4.75V
200mA



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Title: **AUDIO CODEC STAC9200**

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Key-West / Kinney		
Date: Friday, December 23, 2005	Sheet 23	of 37



MIC IN

Place on bottom side

1st source: 22.10088.A31
2nd source: 22.10088.A81

LINE OUT

Place on bottom side

Speaker

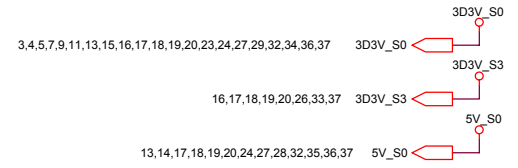
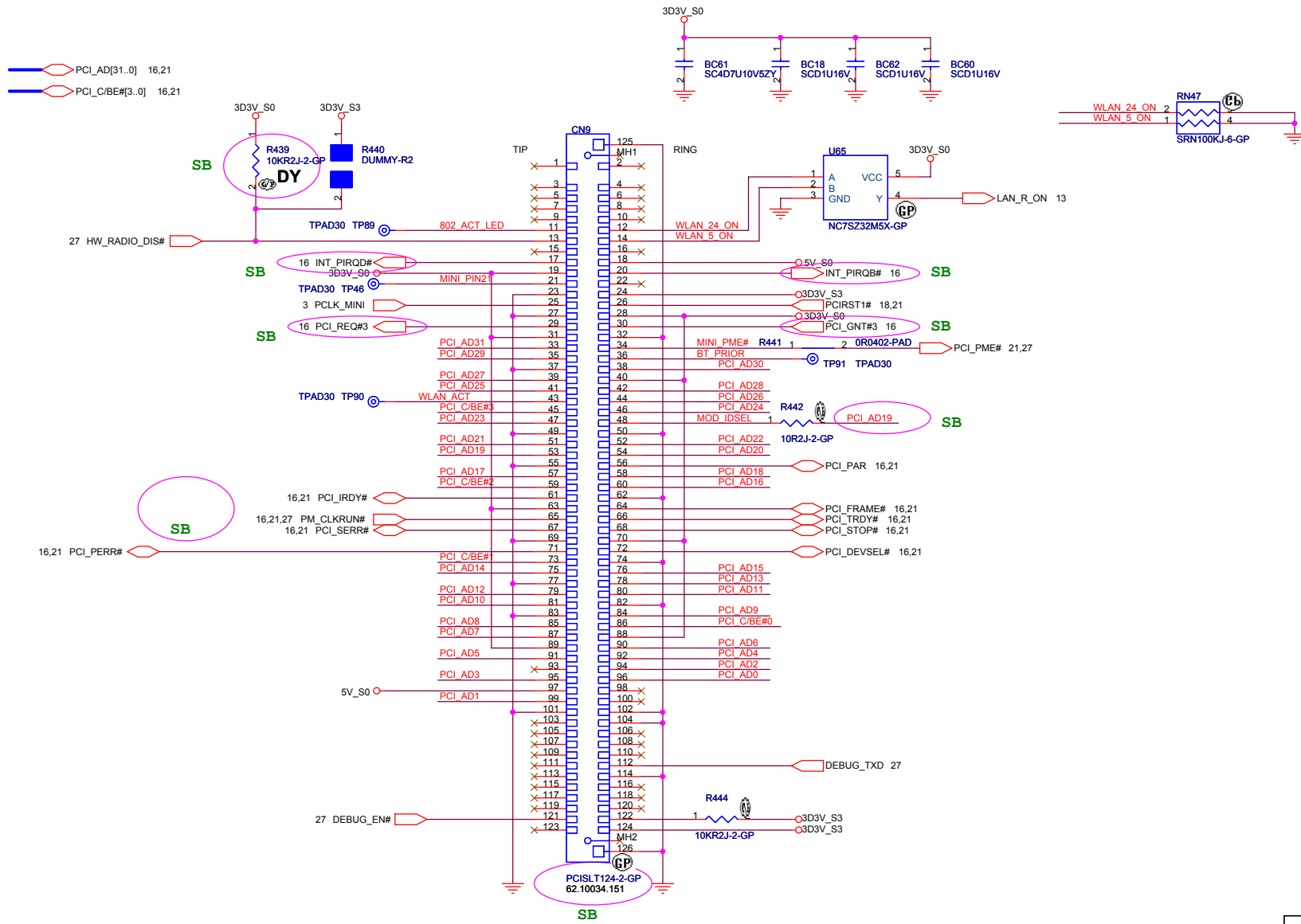
GAIN0	GAIN1	AV
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

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Title		
AUDIO (2/2)		
Size A3	Document Number	Rev
	Key-West / Kinney	-2
Date: Friday, December 23, 2005	Sheet 24	of 37

Change to Azalia solution

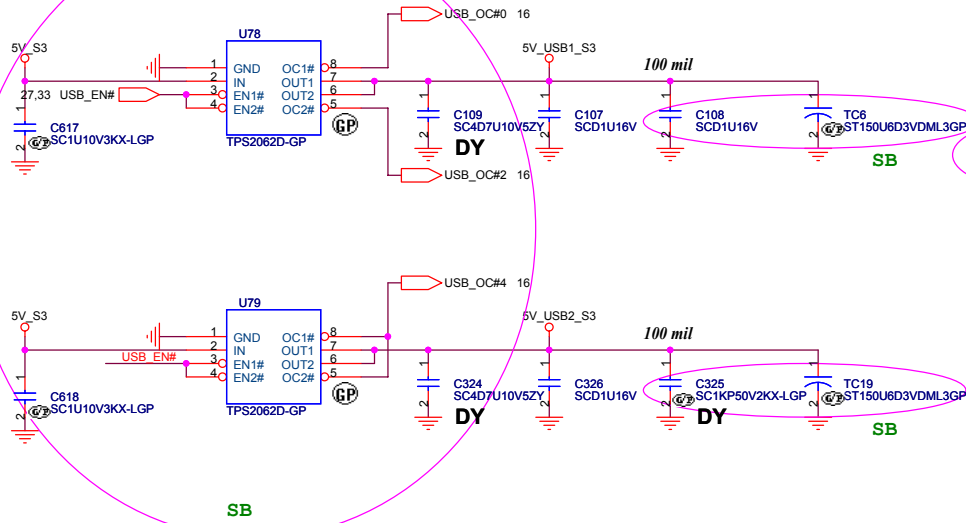
MINI-PCI



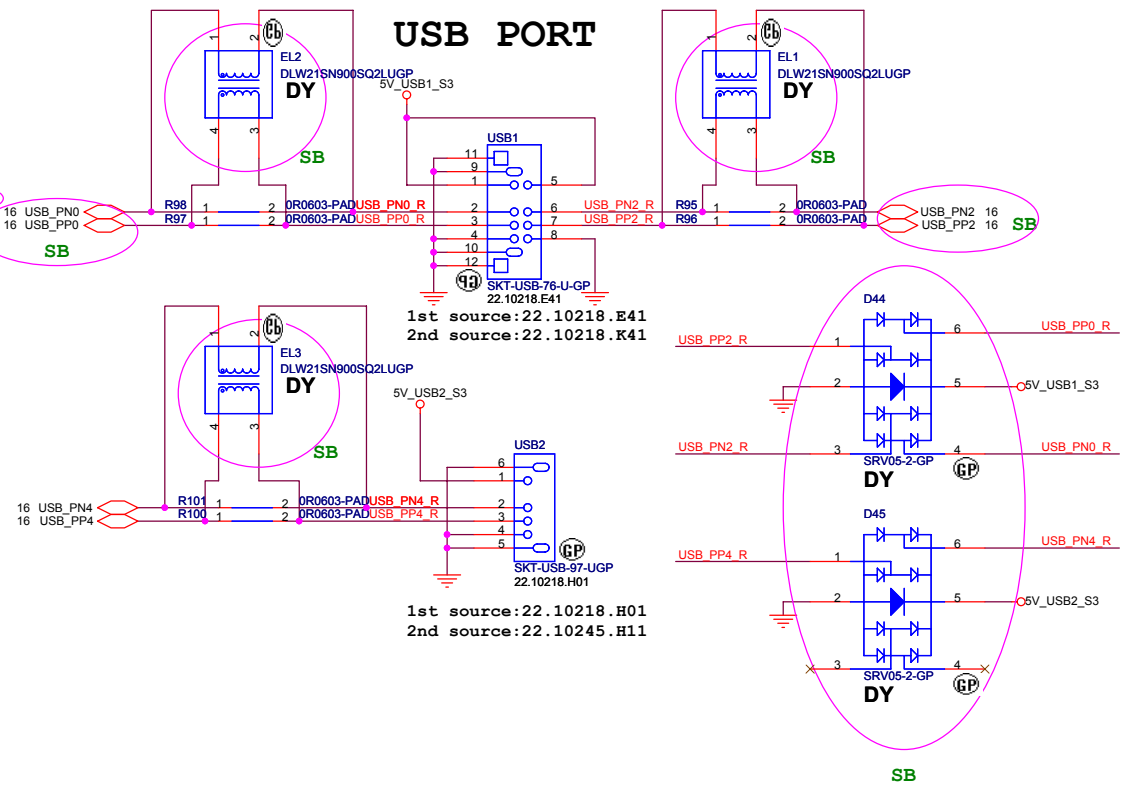
1st source: 62.10034.151
2nd source: 62.10043.151

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
MINI-PCI	
Title Size A3 Date: Friday, December 23, 2005	Document Number Key-West / Kinney Sheet 25 of 37
Rev -2	

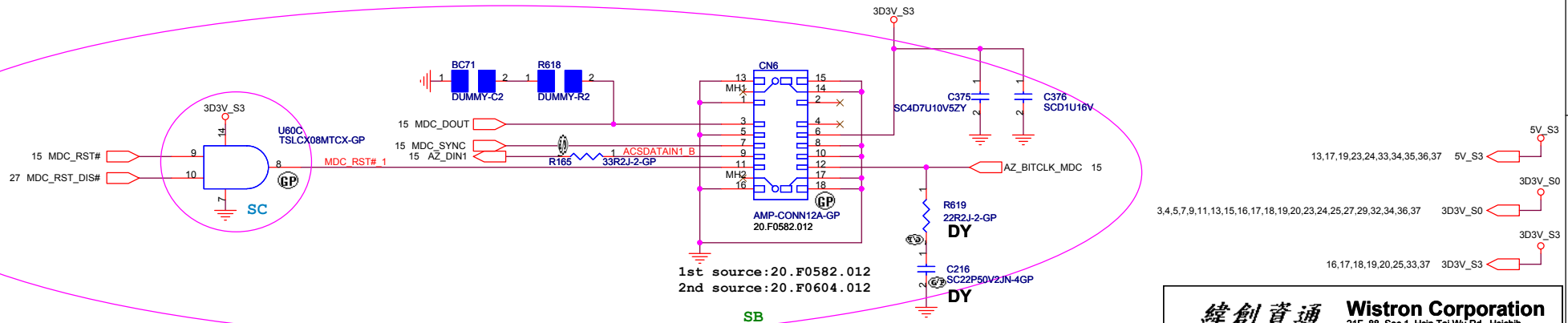
USB POWER



USB PORT



MDC Connector

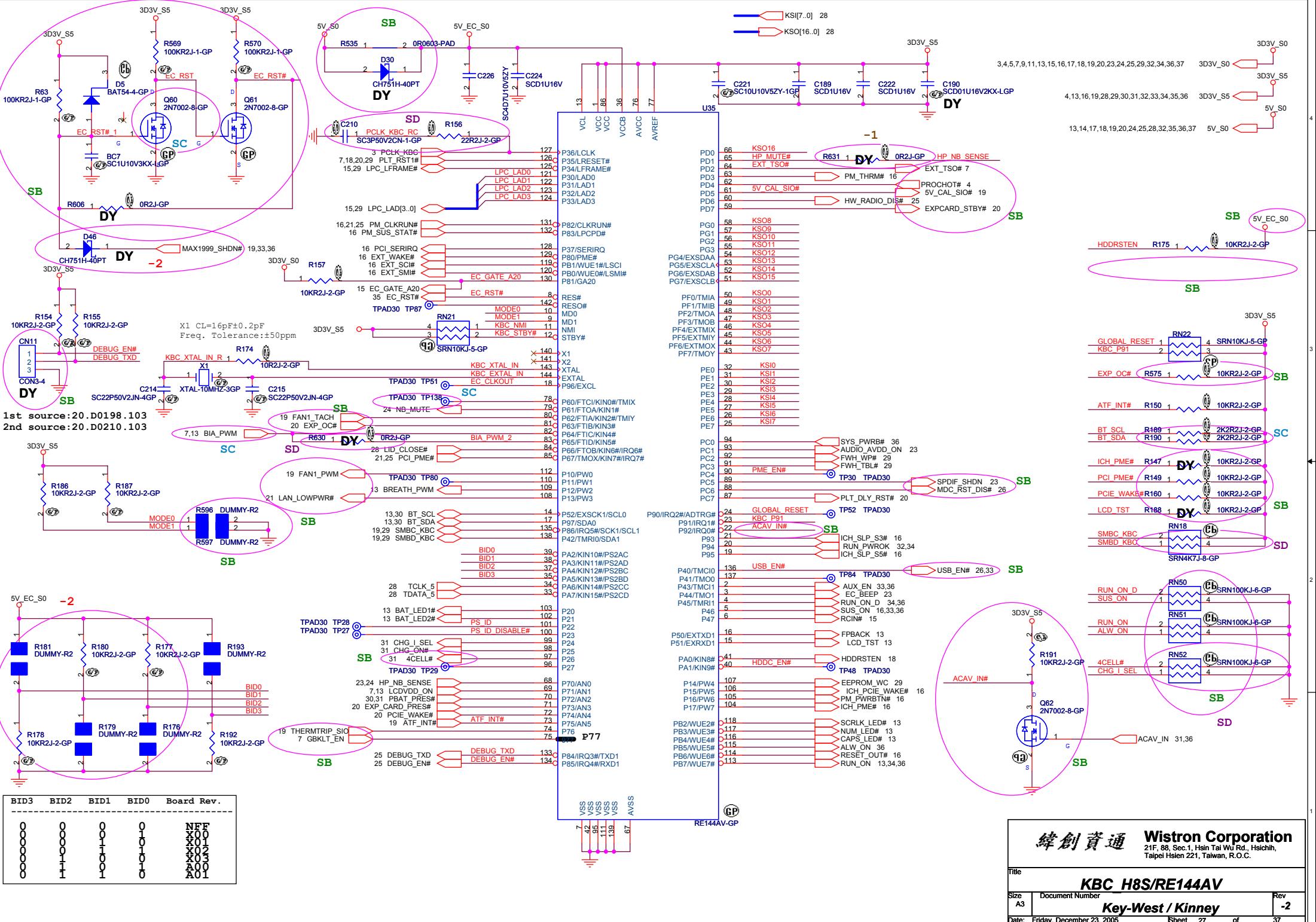


緯創資通 Wistron Corporation
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Title: **USB / MDC CONN.**

Size: A3, Document Number: Key-West / Kinney, Rev: -2

Date: Friday, December 23, 2005, Sheet 26 of 37



1st source:20.D0198.103
 2nd source:20.D0210.103

BID3	BID2	BID1	BID0	Board Rev.
0	0	0	0	NFF
0	0	0	0	X01
0	0	0	0	X02
0	0	0	0	X03
0	0	0	0	X04
0	0	0	0	A01

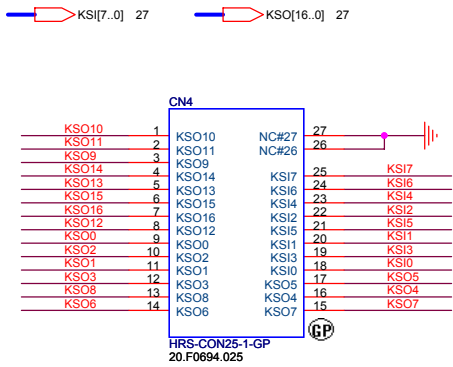
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **KBC H8S/RE144AV**

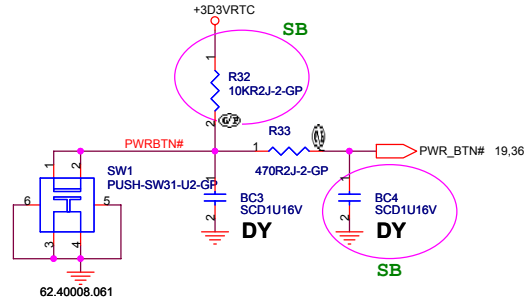
Size: A3 Document Number: **Key-West / Kinney** Rev: **-2**

Date: Friday, December 23, 2005 Sheet 27 of 37

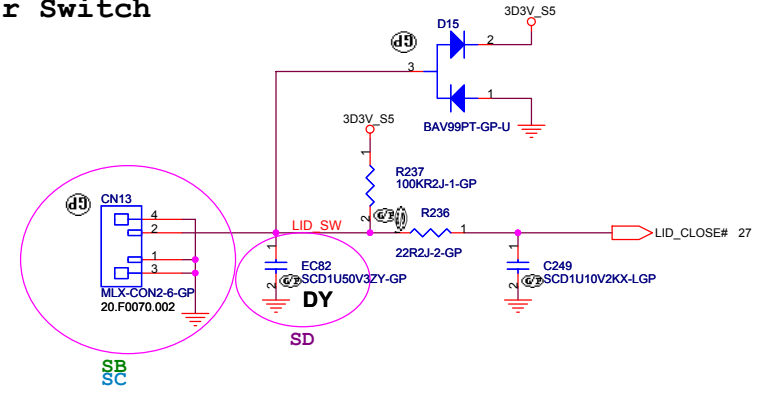
INTERNAL KEYBOARD CONNECTOR



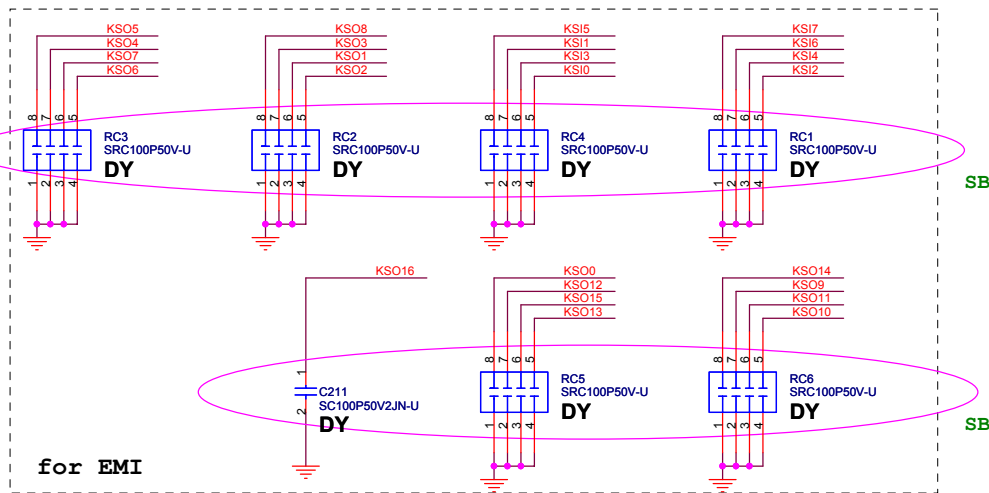
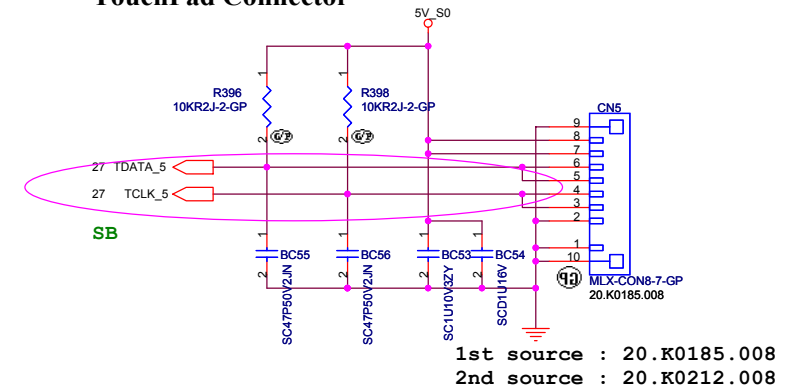
POWER BUTTON



Cover Switch

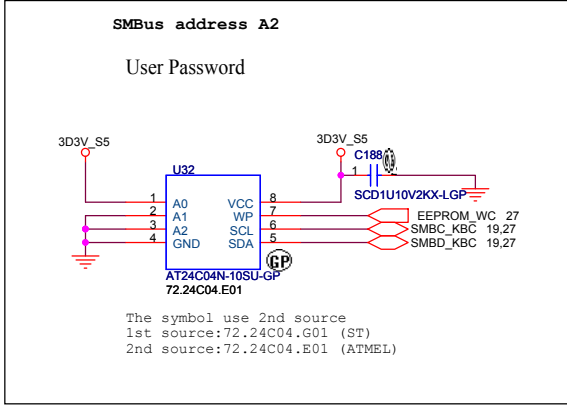
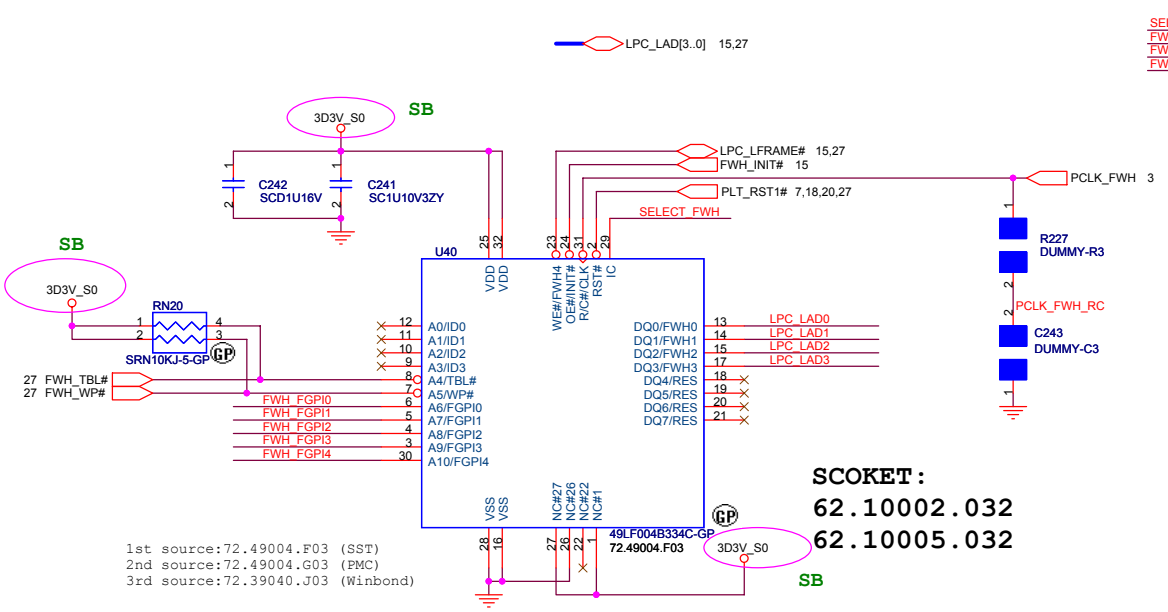


TouchPad Connector



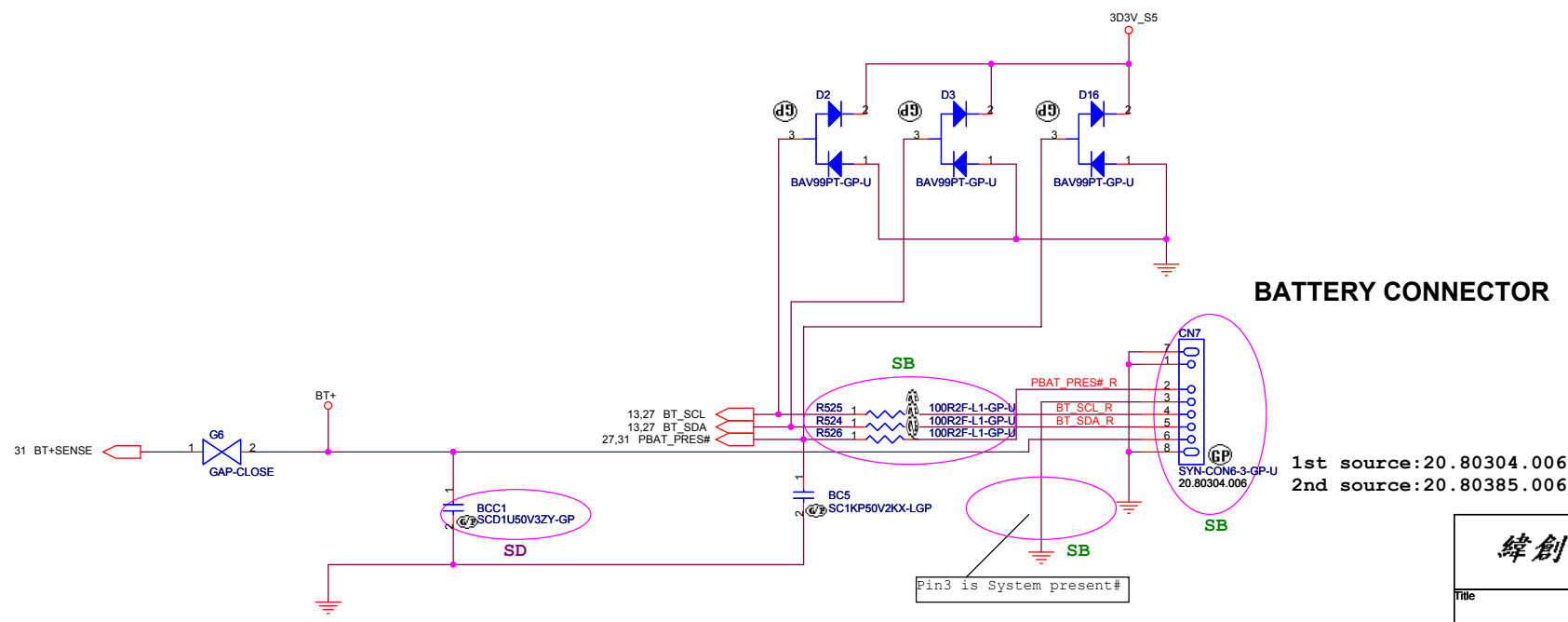
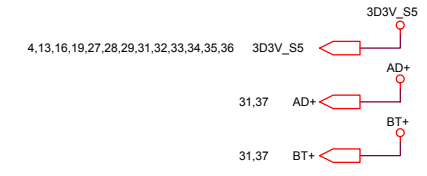
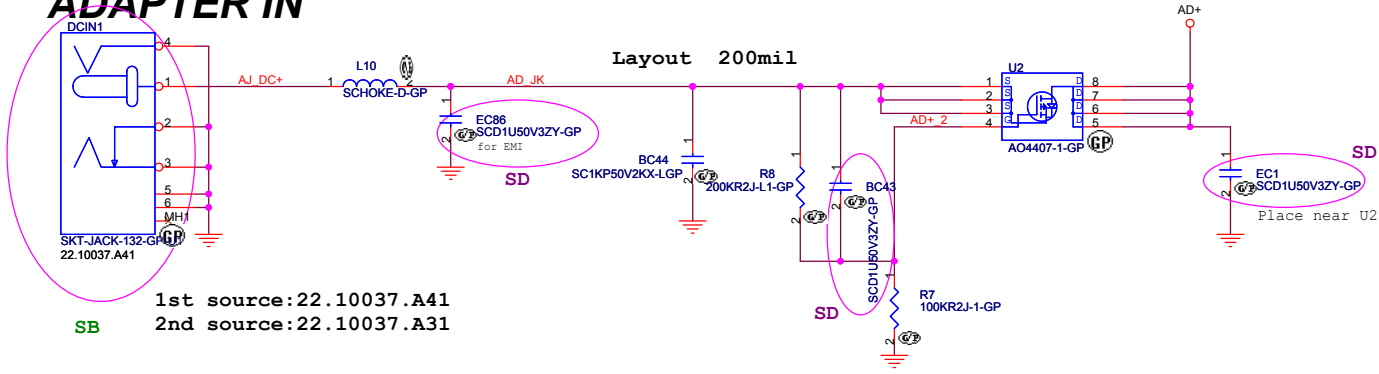
512KB Flash

Unused FGPI pins must not be float



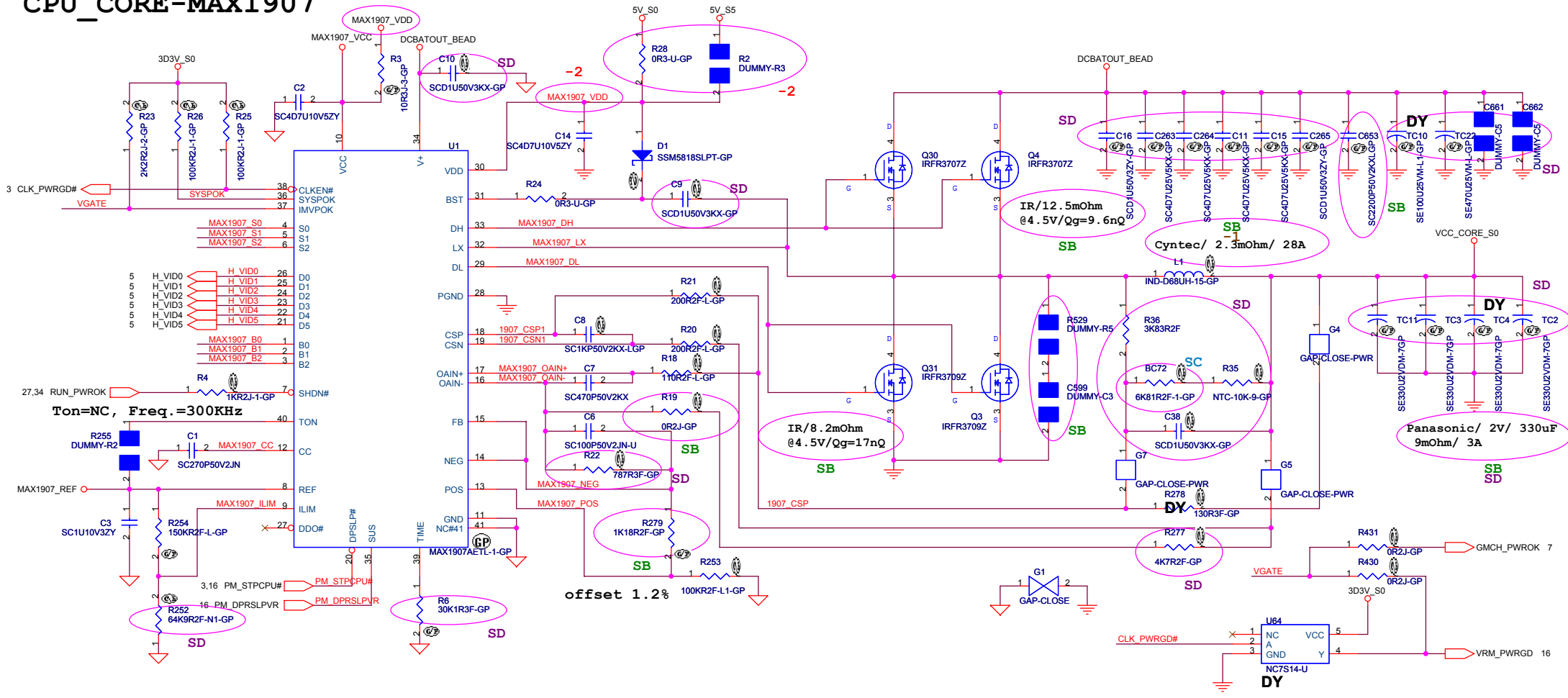
Adaptor in to generate DCBATOUT

ADAPTER IN



Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: Adaptor/ Battery conn.	
Size: A3	Document Number: Key-West / Kinney
Date: Friday, December 23, 2005	Sheet 30 of 37
Rev: -2	

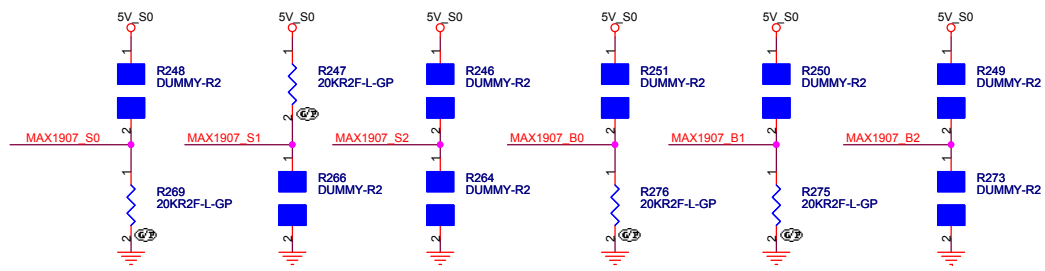
CPU_CORE-MAX1907



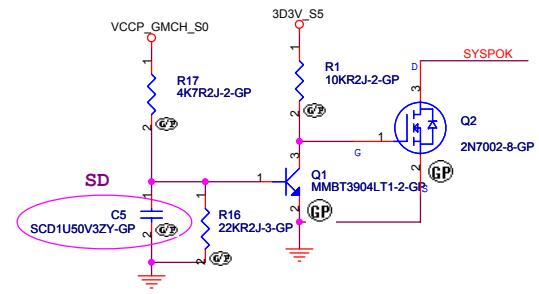
OCP=30A, Vally current = 27.5A,
 Vilim=550mV(55mVp-p*10)

Deeper Sleep Voltage : 0.748V
 , S0=L, S1=H, S2=Open,

Boot-up Voltage : 1.2V
 , B0=L, B1=L, B2=Open



VID						Vcore
VID5	VID4	VID3	VID2	VID1	VID0	v
0	1	0	1	1	1	1.340
0	1	1	0	0	0	1.324
0	1	1	0	1	0	1.292
0	1	1	1	0	0	1.260
0	1	1	1	0	1	1.244
0	1	1	1	1	1	1.212
1	0	0	0	0	1	1.180
1	0	0	0	1	1	1.148
1	0	0	1	1	0	1.100
1	0	1	0	0	1	1.052
1	0	1	0	1	1	1.020
1	0	1	1	1	0	0.972
1	1	0	0	0	0	0.940



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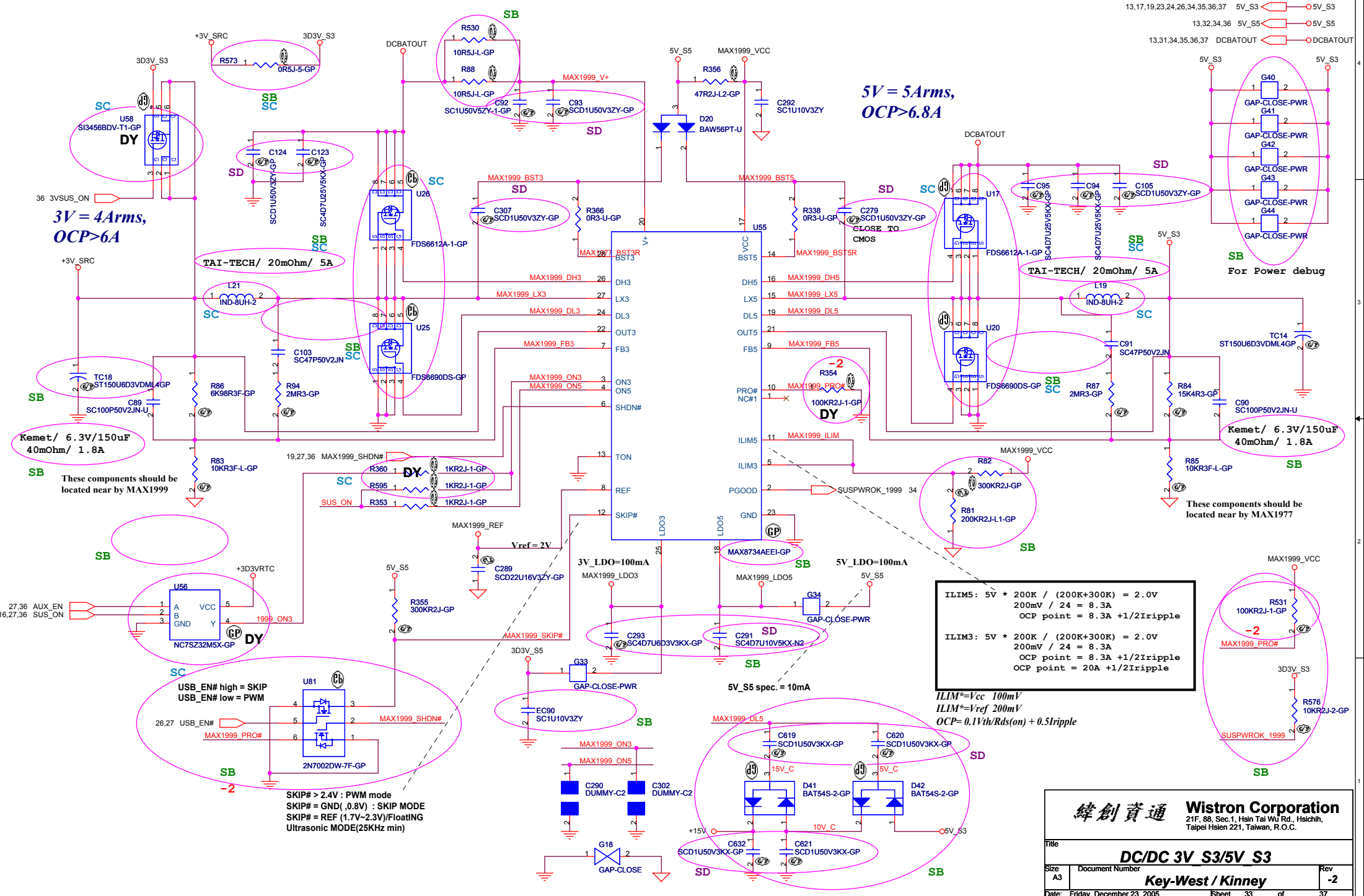
Title: **IMVP IV-CPU POWER-MAX1907**

Size: A3 Document Number: **Key-West / Kinney** Rev: -2

Date: Friday, December 23, 2005 Sheet: 32 of 37

SYSTEM DC/DC 3D3V_S3 / 5V_S3

- 16,17,18,19,20,25,26,37 3D3V_S3
- 4,13,16,19,27,28,29,30,31,32,34,35,36 3D3V_S5
- 13,17,19,23,24,26,34,35,36,37 5V_S3
- 13,32,34,36 5V_S5
- 13,31,34,35,36,37 DCBATOUT



$ILIM5: 5V * 200K / (200K+300K) = 2.0V$
 $200mV / 24 = 8.3A$
 $OCP \text{ point} = 8.3A + 1/2 I_{ripple}$
 $ILIM3: 5V * 200K / (200K+300K) = 2.0V$
 $200mV / 24 = 8.3A$
 $OCP \text{ point} = 8.3A + 1/2 I_{ripple}$
 $OCP \text{ point} = 20A + 1/2 I_{ripple}$

$ILIM^* = V_{cc} / 100mV$
 $ILIM^* = V_{ref} / 200mV$
 $OCP = 0.1V_{th} / R_{ds(on)} + 0.5I_{ripple}$

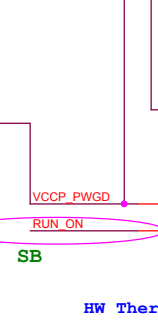
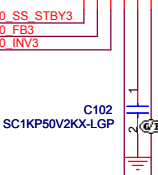
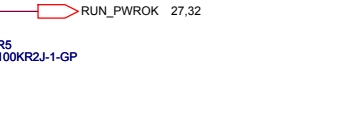
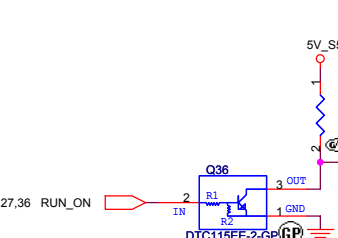
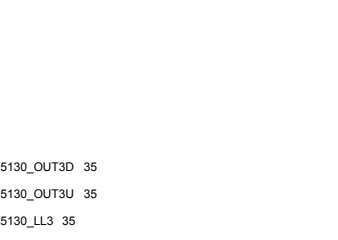
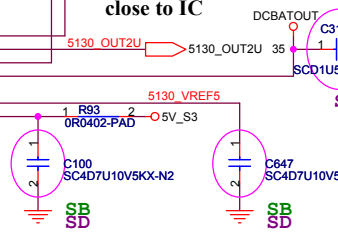
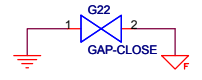
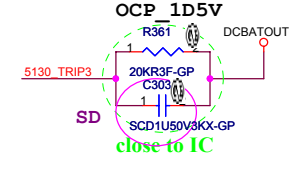
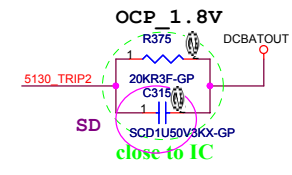
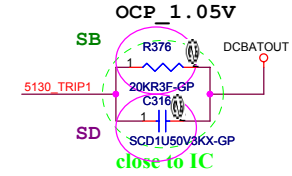
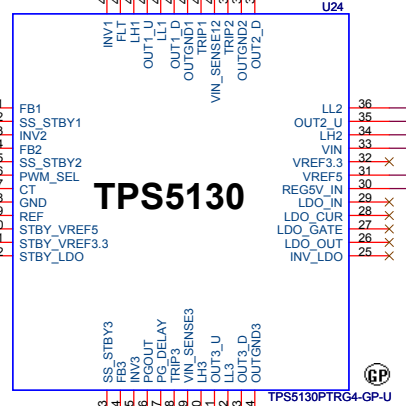
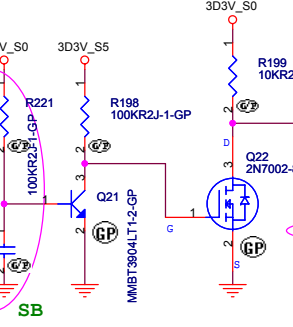
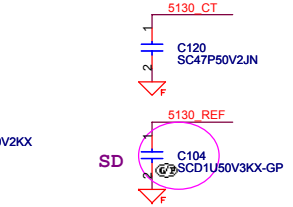
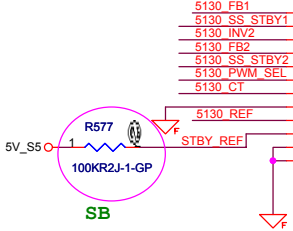
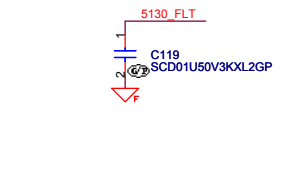
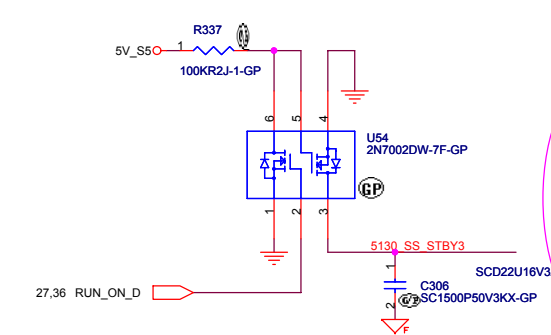
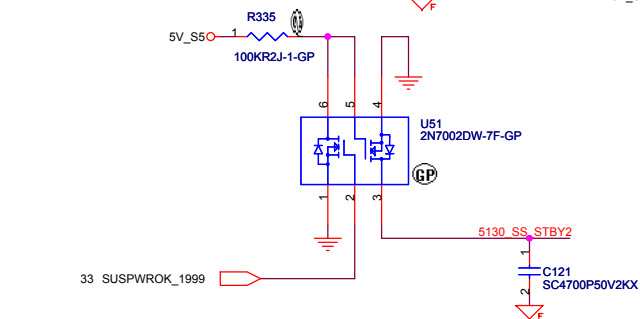
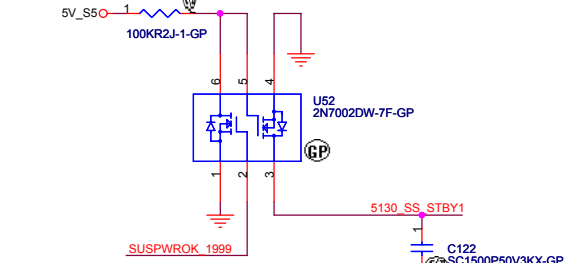
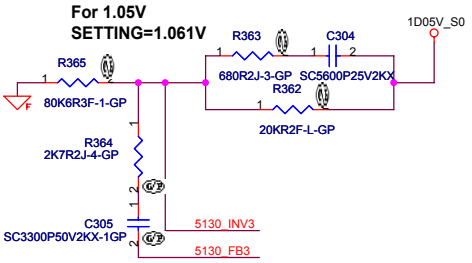
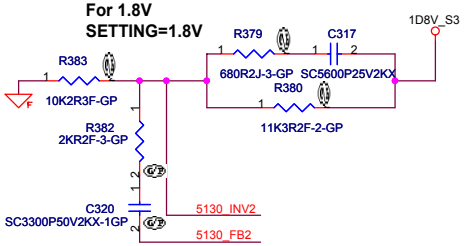
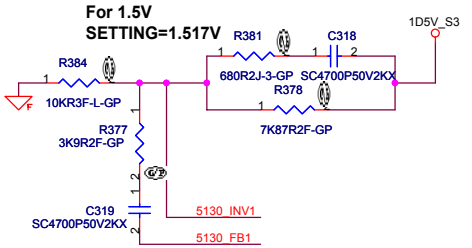
SKIP# > 2.4V : PWM mode
 SKIP# = GND(,0.8V) : SKIP MODE
 SKIP# = REF (1.7V-2.3V)/Floating
 Ultrasonic MODE(25KHz min)

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Title: **DC/DC 3V S3/5V S3**
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TI TPS5130 for 1.5V, 1.8V, 1.05V.

(1D5V=>CH1 , 1D8V=>CH2 , 1D05V =>CH3)

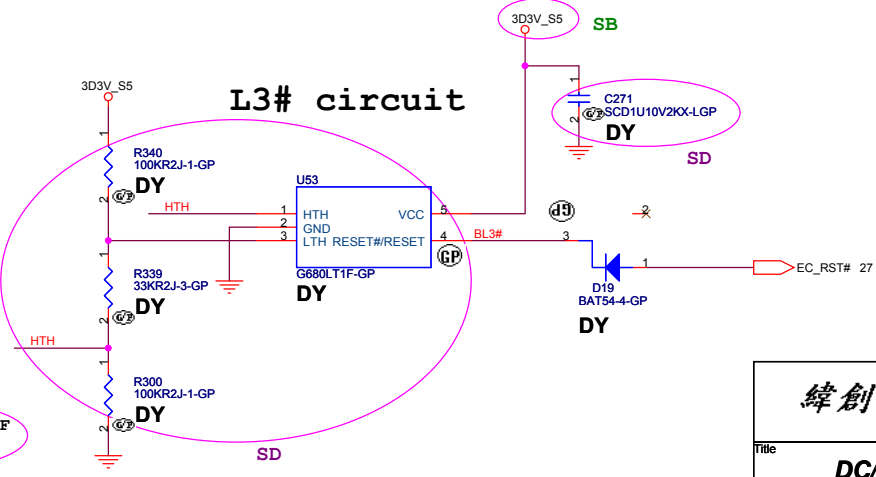
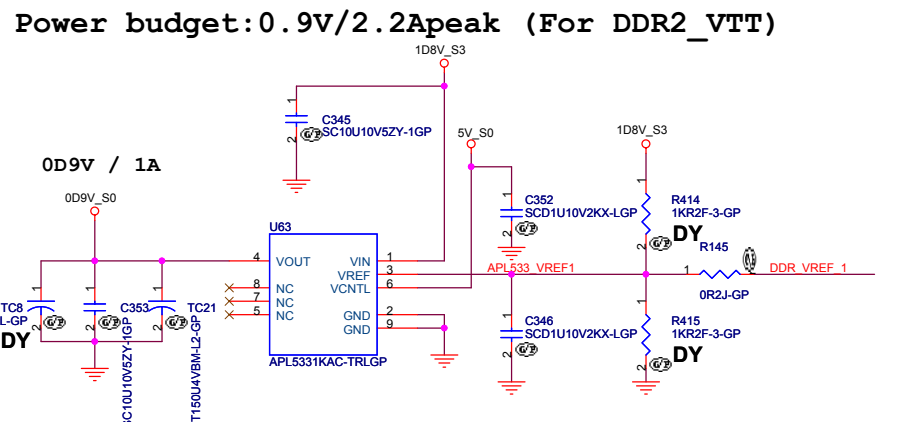
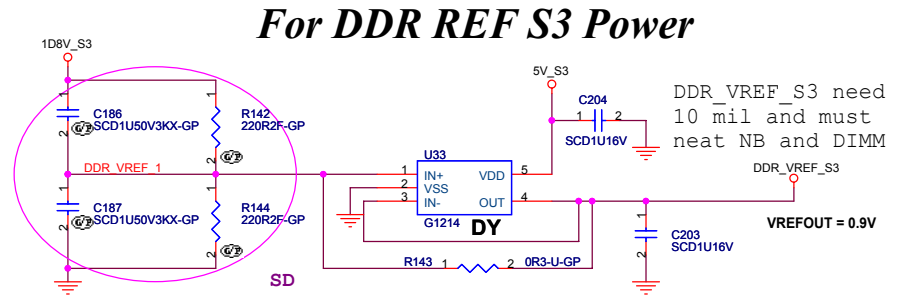
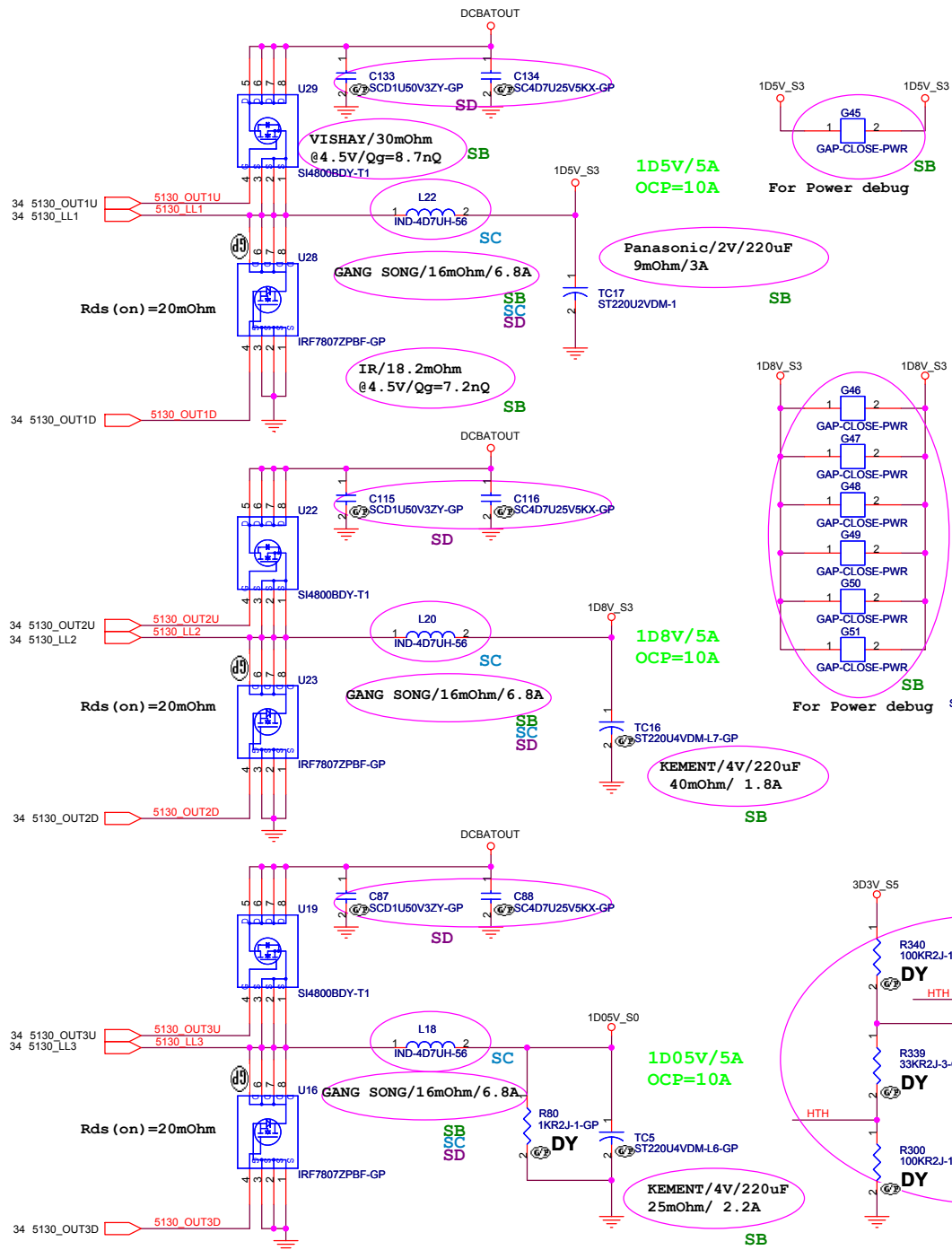


HW Thermal Throttling

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Title: DC/DC 1D8V/1D5V/1D05V			
Size: A3	Document Number:	Rev: -2	
Key-West / Kinney			
Date: Friday, December 23, 2005	Sheet: 34	of 37	

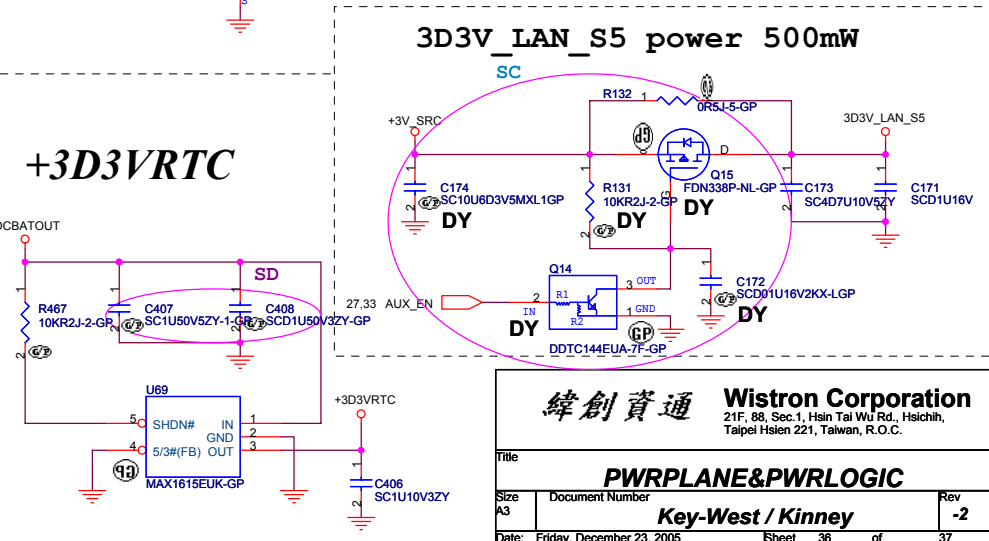
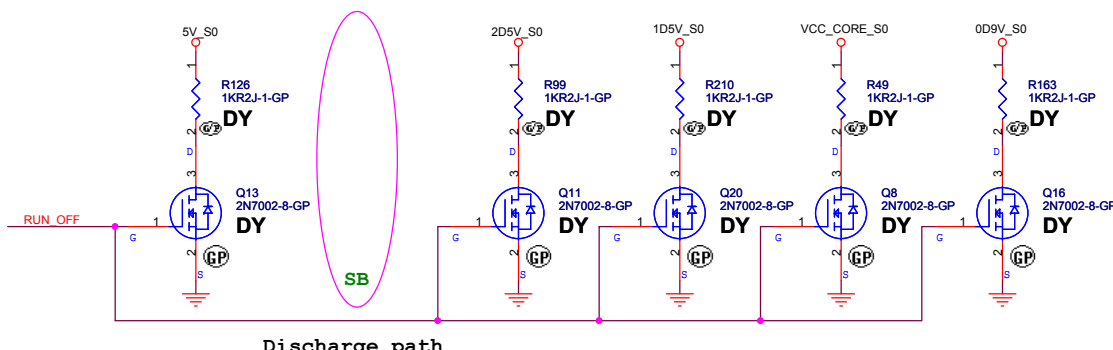
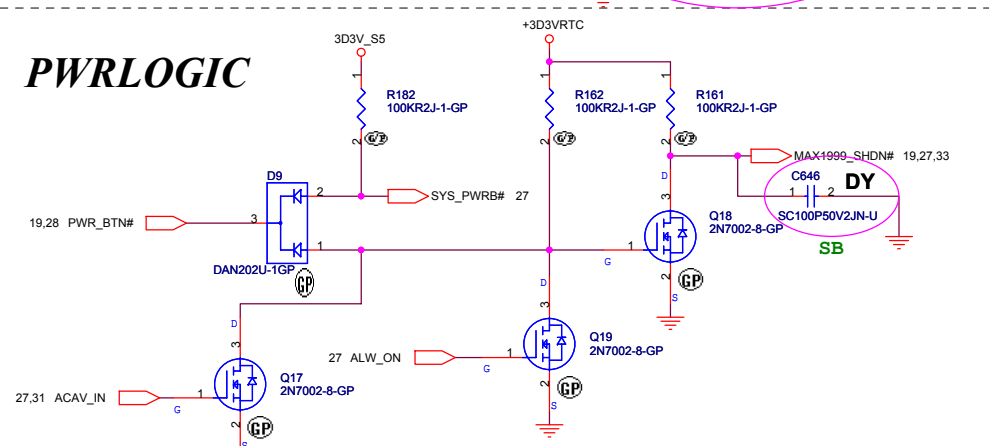
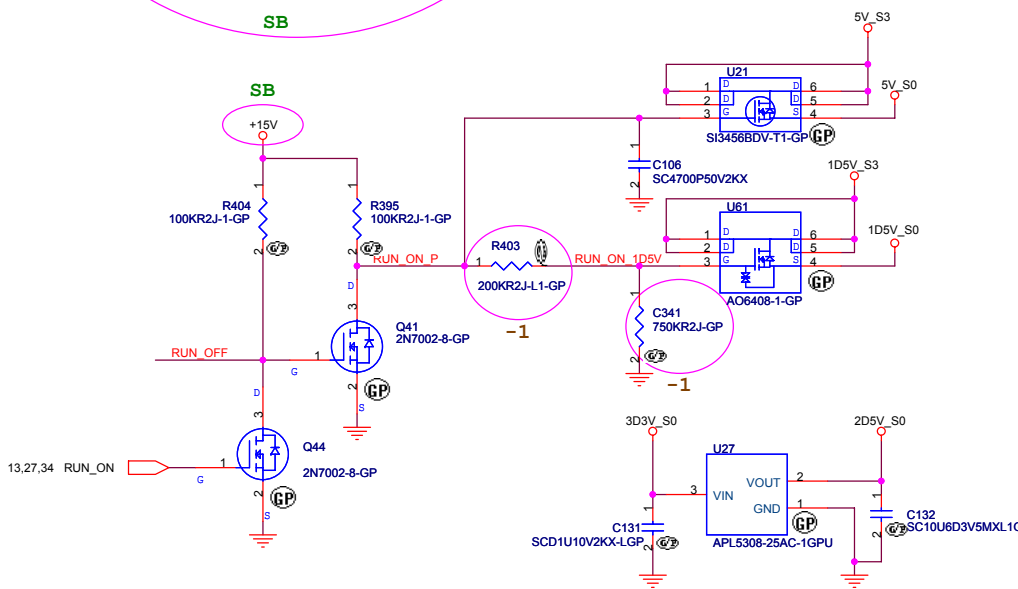
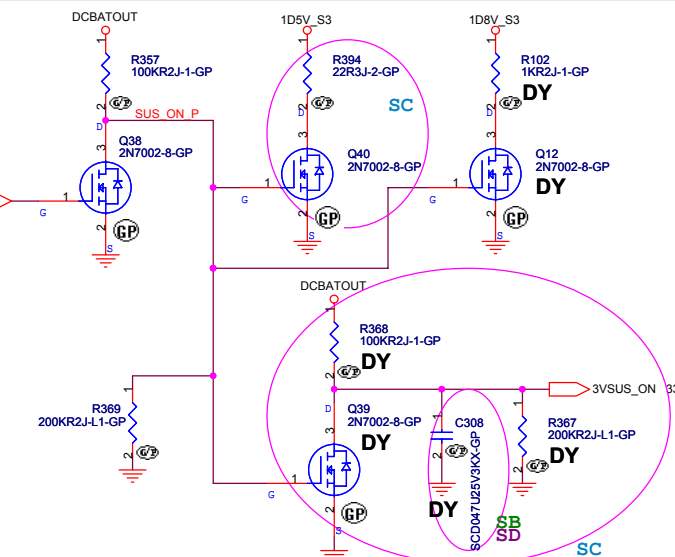
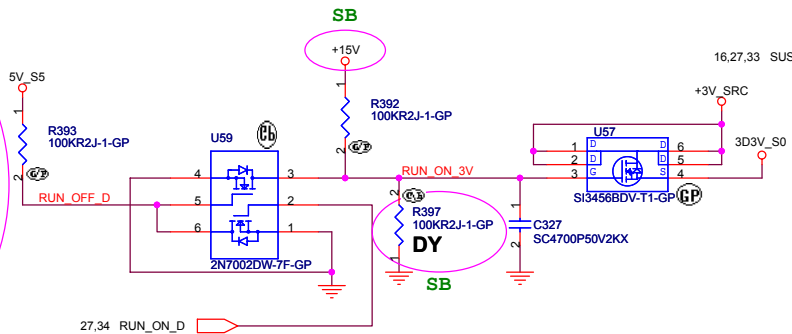
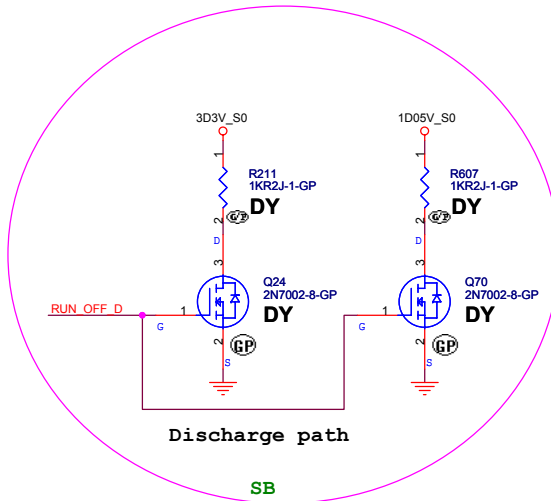
TI TPS5130 for 1.5V, 1.8V, 1.05V

(1D5V=>CH1 , 1D8V=>CH2 , 1D05V =>CH3)



- 13,31,33,34,36,37 DCBATOUT
- 13,32,33,34,36 5V_S5
- 10,34,36,37 1D05V_S0
- 7,9,10,11,12,16,34,36,37 1D8V_S3
- 13,14,17,18,19,20,24,25,27,28,32,36,37 5V_S0
- 12,36 0D9V_S0
- 17,34,36 1D5V_S3

Run Power



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Title: **PWRPLANE&PWRLOGIC**

Size: A3 Document Number: **Key-West / Kinney** Rev: **-2**

Date: Friday, December 23, 2005 Sheet: 36 of 37

