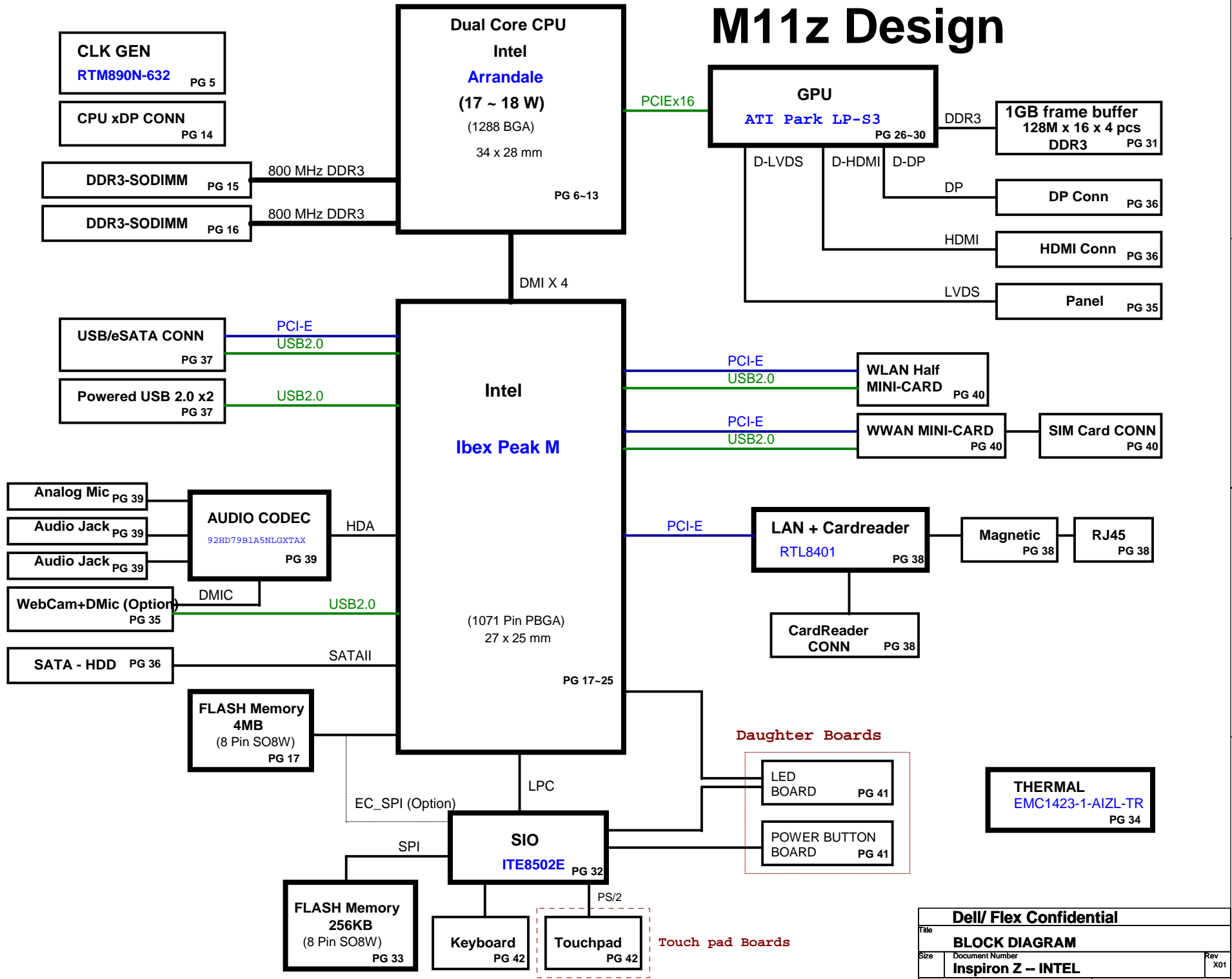


M11z Design

POWER

- AC/BATT CONNECTOR PG 44
- BATT CHARGER BQ24745 PG 45
- +5V_ALW +3.3V_ALW_17020 TPS51125 PG 46
- +V1.8S RT8015B PG 47
- +V1.5 TPS51218 +0.75V_DDR_VTT TPS51100 PG 48
- +V1.05S TPS51218 PG 49
- CPU CORE +CPU_VCORE MAX17028 PG 50
- VGA CORE +VGA_CORE TPS51218 PG 51
- SUS/ RUN POWER SW +V5 / +V5S / +V1.5S +3.3V_ALW / +V3.3A_PCH / +V3.3 / +V3.3S PG 42



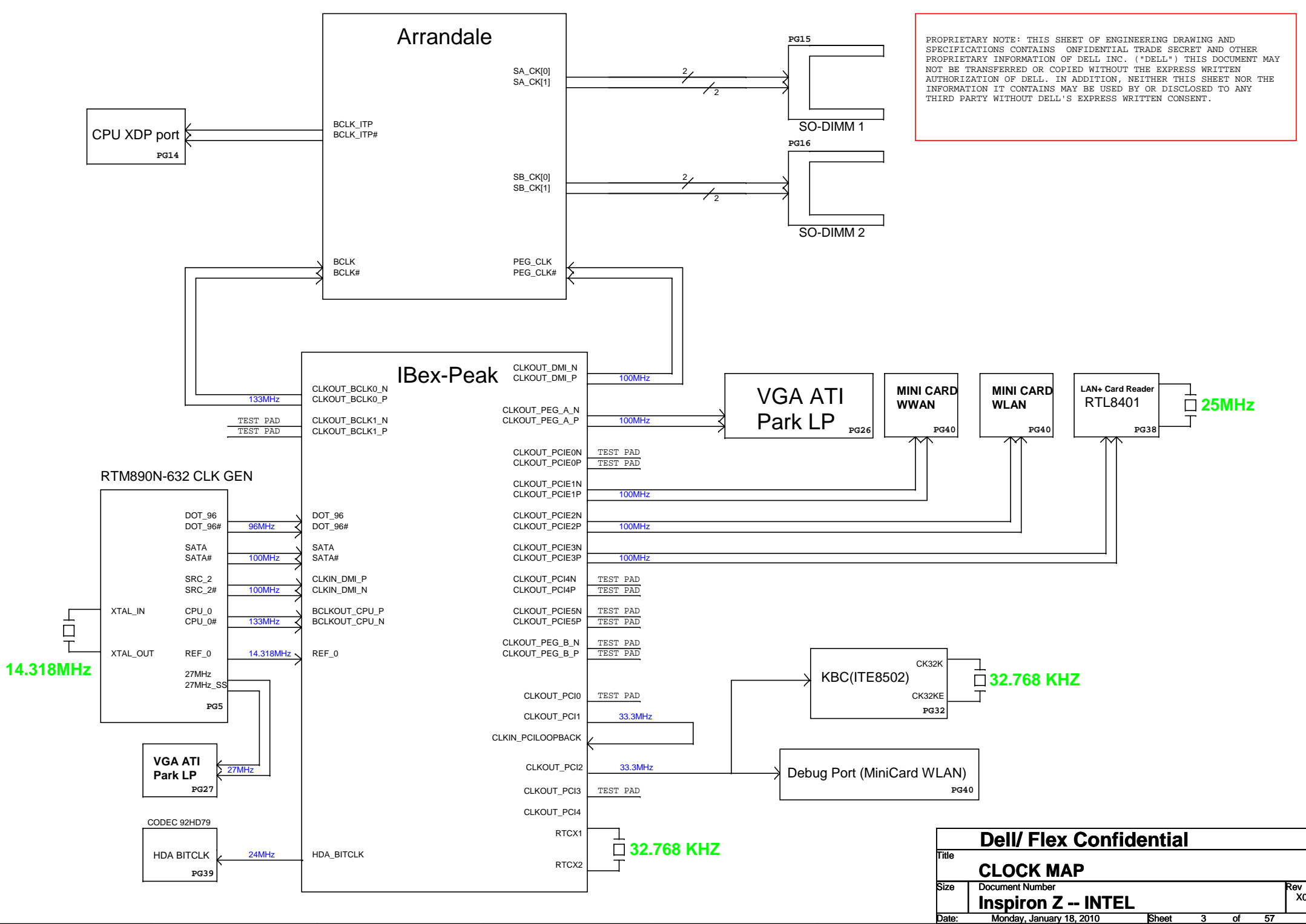
Page#	INDEX Description	Page#	INDEX Description
1	BLOCK DIAGRAM	45	PWR - CHARGER_BQ24745
2	Front Page	46	PWR - 5V/3V_MAX17020ETJ+
3	CLOCK MAP	47	PWR - +V1.8S_RT8015B
4	POWER SEQUENCING	48	PWR - +V1.5 / +0.75VS
5	CLOCK GEN (RTM890N-632)	49	PWR - +V1.05S_TPS51218
6-13	CPU Arrandale	50	PWR - CPU VCORE_MAX17028
14	XDP_PROCESSOR	51	PWR - +VGA_CORE/+V1S_VGA
15-16	DDRIII SO-DIMM(204P)	52	SCREW / PAD
17-25	PCH	53	Power Block Diagram
26-30	VGA ATI Park LP	54	PCI Reset Map
31	VRAM 128Mx16	55	KBC Power Up Sequence
32	KBC - ITE8502E	56	SMBus Map
33	RTC BAT/ EC_ROM		
34	THRM_EMC1423-1		
35	LVDS / WEBCAM		
36	HDMI / DP		
37	HDD / USB / eSATA		
38	LAN/ Media_RTL8401		
39	AUDIO_92HD75B2X5NLGXYB		
40	WLAN / WWAN		
41	BT / KB / TP / LED / SW		
42	RUN POWER_SW		
43	PWRGD / RESET CIRCUIT		
44	PWR - DCIN_BAT		

Power States								
Power Rail	Control Signal	S0	S3	S4	S5	G3	S4/ M-off	S5/ M-off
+RTC_CELL	RTC	V	V	V	V	V		
+PWR_SRC	N/A	V	V	V	V			
+15V_ALW	5V_ALW_ON	V	V	V	V			
+5V_ALW	+5V_EN1/5V_ALW_ON	V	V	V	V			
+V5_LDO	+PWR_SRC	V	V	V	V			
+V3.3A	+3.3V_EN2/5V_ALW_ON	V	V	V	V			
+V3.3A_PCH	3VA_PCH_ON	V	V	V	V			
+V5	SUS_ON#	V	V					
+USB_RIGHT_PWR	USB_EN0#	V	V					
+USB_LEFT_PWR	USB_EN1#	V	V					
+V3.3	SUS_ON#	V	V					
+V1.5	SUS_ON	V	V					
+V1.5_DDR	SUS_ON#	V	V					
+V5S	RUN_ON	V						
+V3.3S	RUN_ON#	V						
+LCDVCC	LCD_DIGON_GFX	V						
+V1.8S	RUN_ON	V						
+V1.5S_VGA	RUN_ON#	V						
+V1.5S	RUN_ON#	V						
+V1.05S_VTT	RUN_ON	V						
+V1.05S	RUN_ON	V						
+V1S_VGA	RUN_ON	V						
+CPU_VCORE	IMVP_VR_ON	V						
+VGA_CORE	RUN_ON	V						
+0.75V_DDR_VTT	RUN_ON	V						

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL"). THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Dell/ Flex Confidential			
Title	PAGE INDEX/ PWR STATUS		
Size	Document Number	Rev	
	Inspiron Z – INTEL	X01	
Date:	Monday, January 18, 2010	Sheet	2 of 57

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.



Dell/ Flex Confidential			
Title CLOCK MAP			
Size	Document Number		Rev X01
Date: Monday, January 18, 2010			Sheet 3 of 57

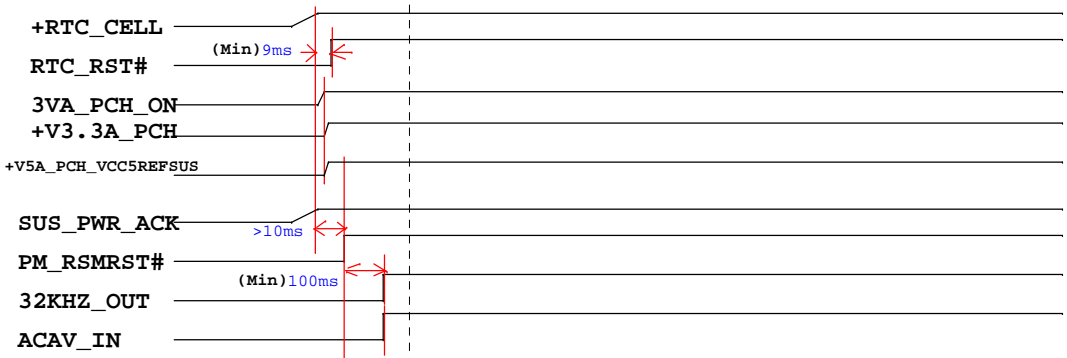
14.318MHz

25MHz

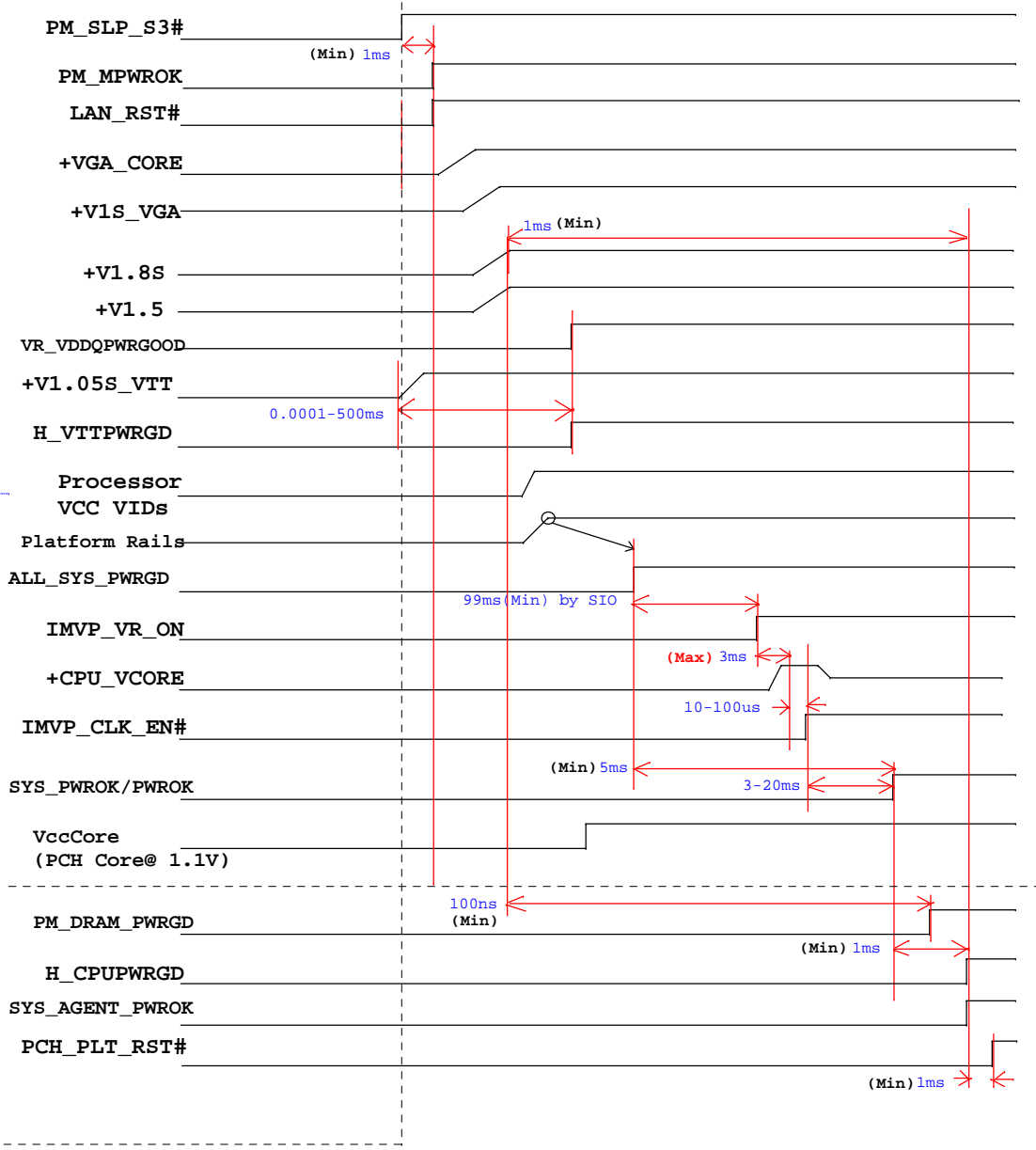
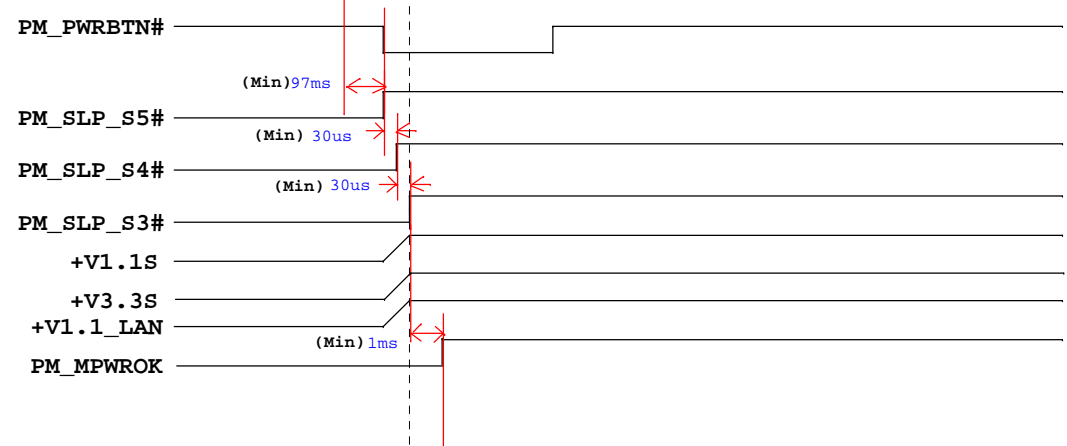
32.768 KHz

32.768 KHz

G3 to S5



S5 to S0



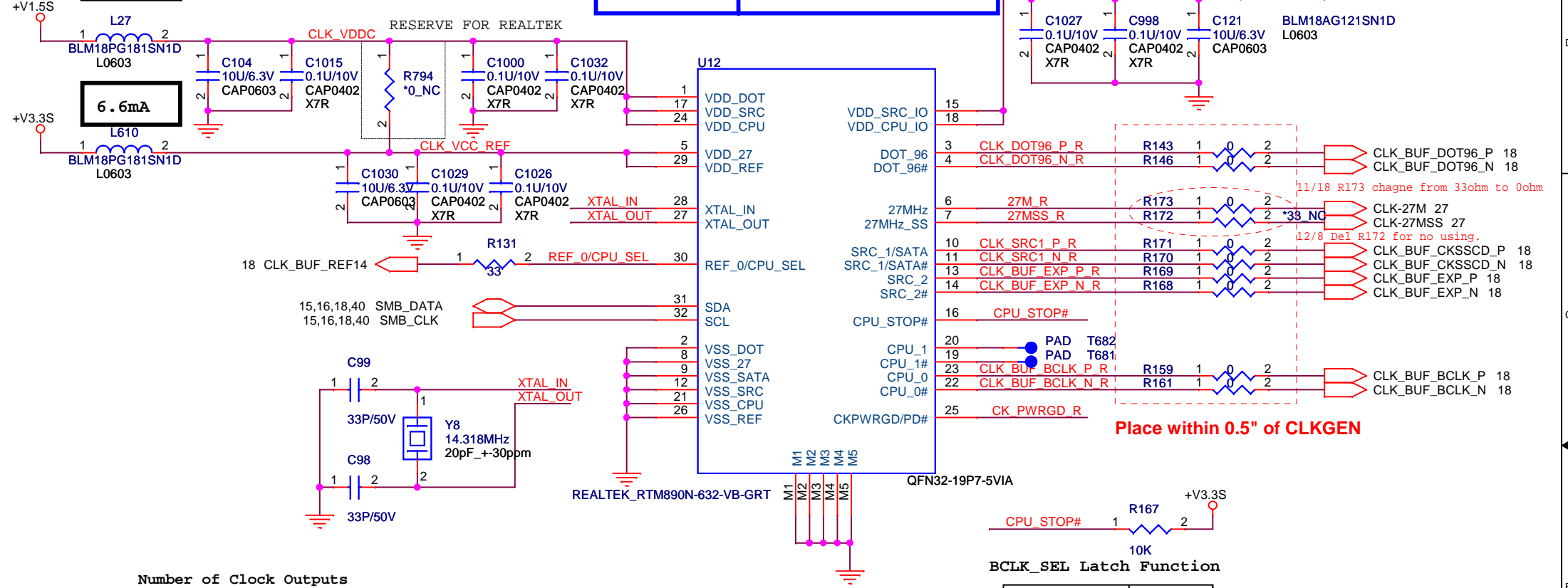
**CLK_VCC: 40mil width
0.1uF near the every power pin.**

Clock Gen	PN
REALTEK (VB)	DELH-12D00J0000010G
IDT	DELH-12D00J0000011G

19.8mA

26.3mA

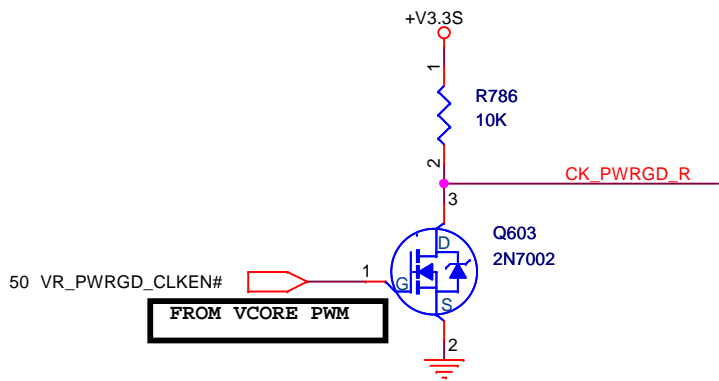
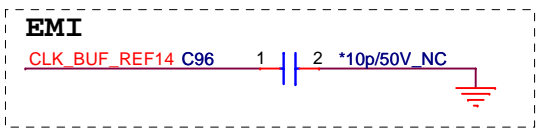
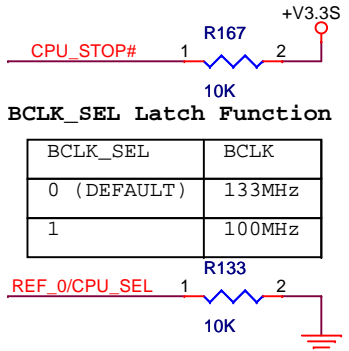
6.6mA



Place within 0.5" of CLKGEN

Number of Clock Outputs

Output	Number
BCLK (133MHz)	2
SRC (100MHz)	1
SRC/SATA(100MHz)	1
REF (14.318MHz)	1
DOT (96MHz)	1
27MHz	1
27MHz SS	1



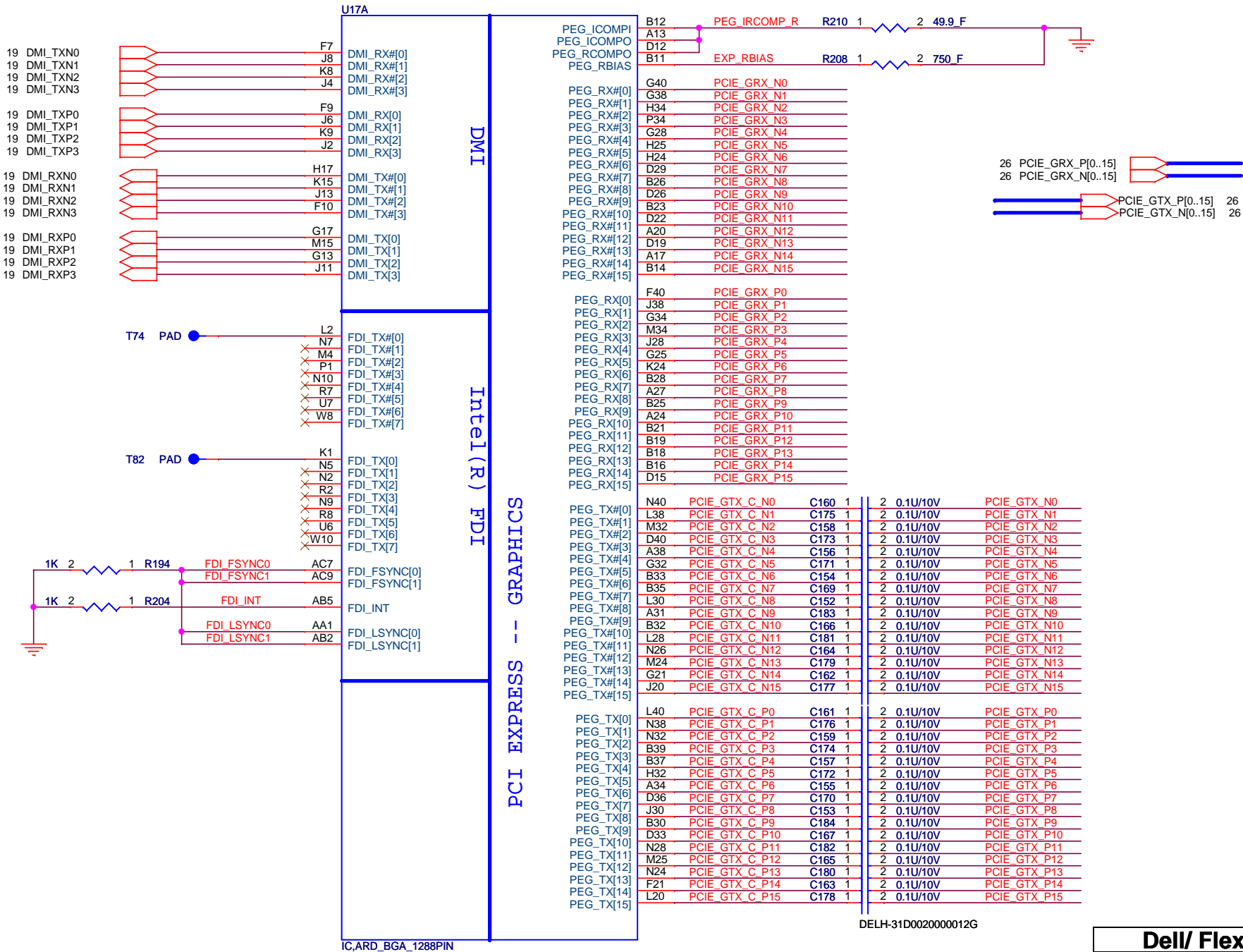
Dell/ Flex Confidential

Title: **CLOCK_GEN_RTM890N-632-GRT**

Size: Document Number **Inspiron Z -- INTEL** Rev X01

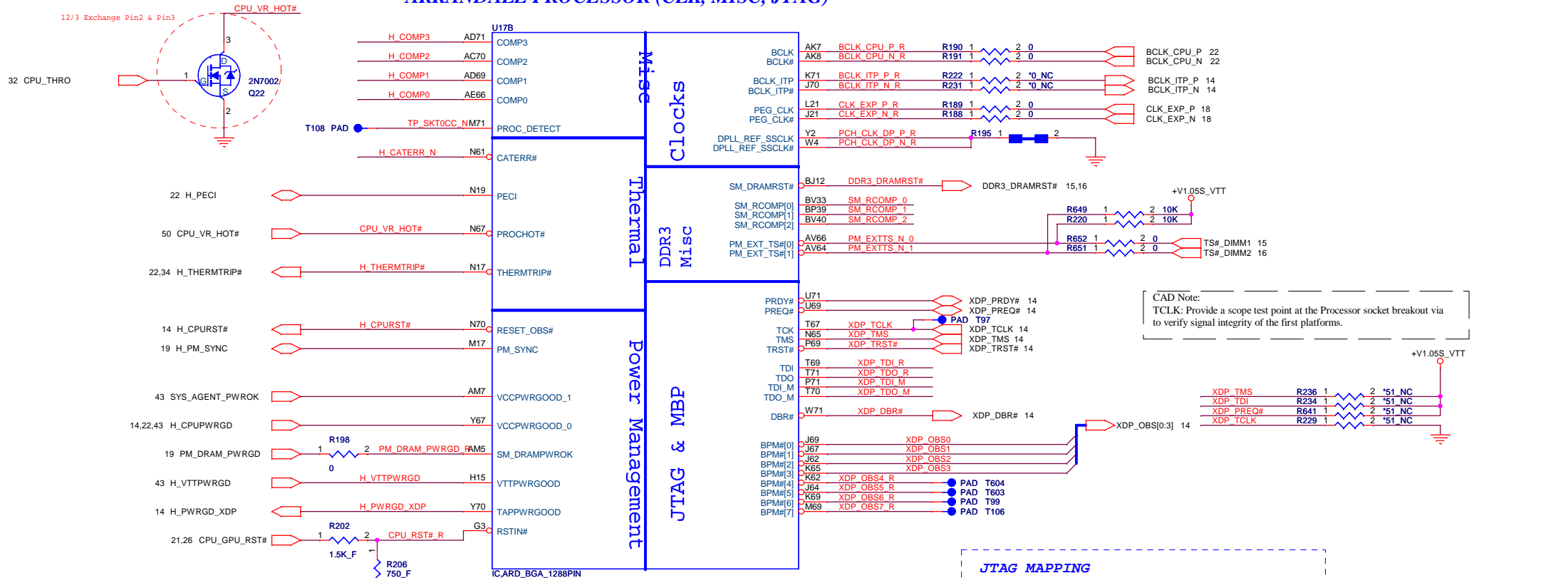
Date: Monday, January 18, 2010 Sheet 5 of 57

ARRANDALE PROCESSOR (DMI, PEG, FDI)

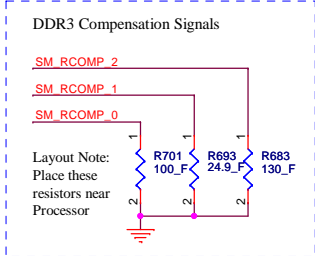
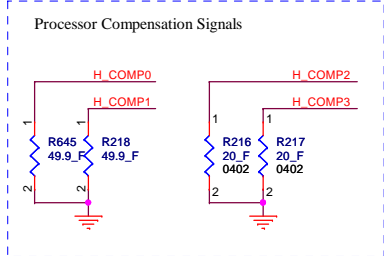
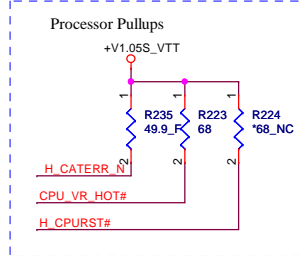
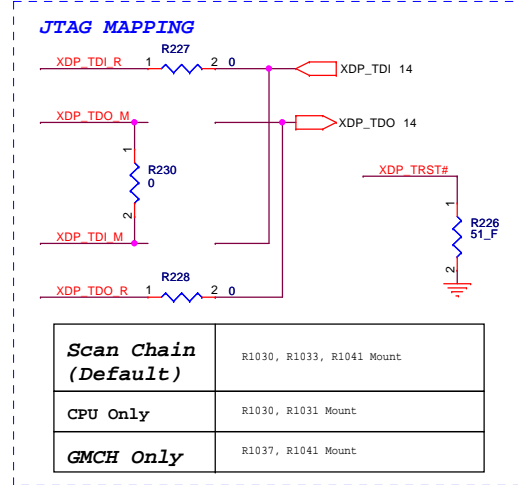
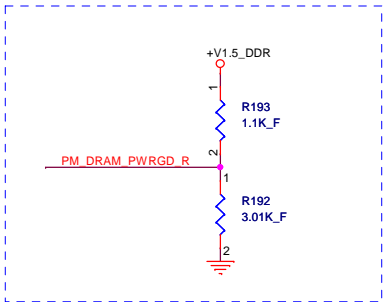


Dell/ Flex Confidential		
Title CPU_DMI/ PEG/ FDI		
Size	Document Number Inspection Z -- INTEL	Rev X01
Date:	Monday, January 18, 2010	Sheet 6 of 57

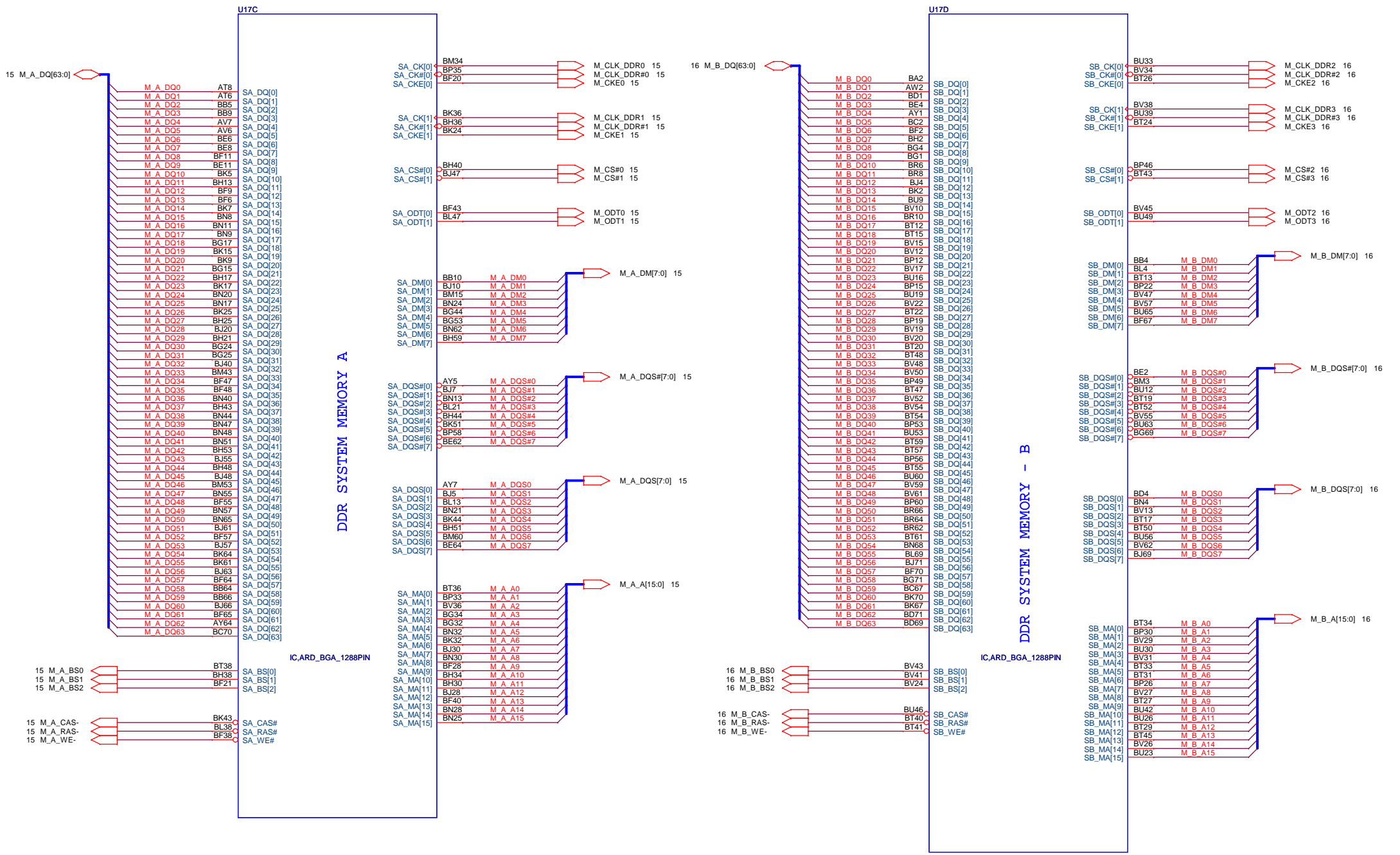
ARRANDALE PROCESSOR (CLK, MISC, JTAG)



CAD Note:
TCLK: Provide a scope test point at the Processor socket breakout via to verify signal integrity of the first platforms.



ARRANDALE PROCESSOR (DDR3)

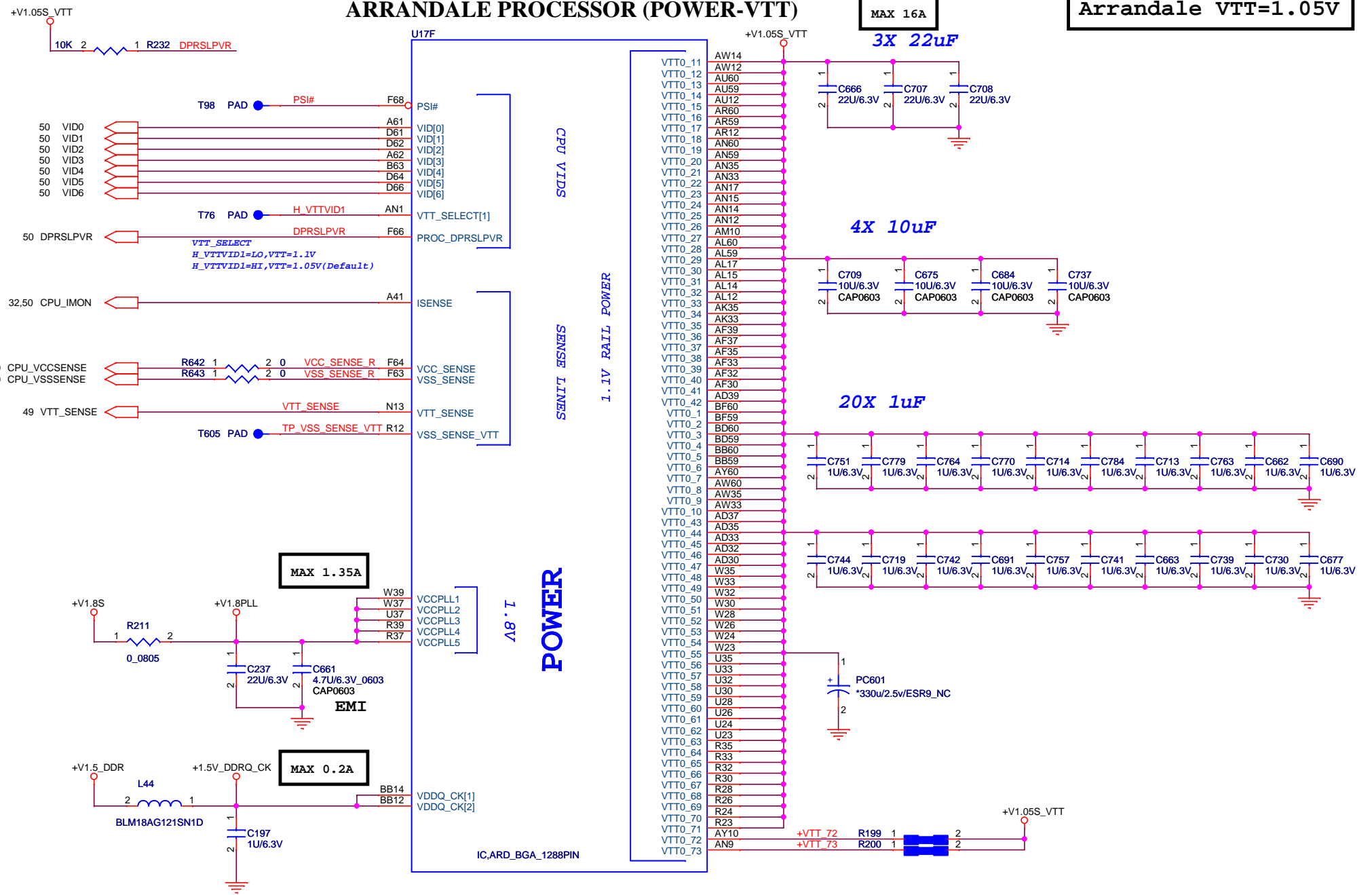


BGA1288-34X28

ARRANDALE PROCESSOR (POWER-VTT)

Arrandale VTT=1.05V

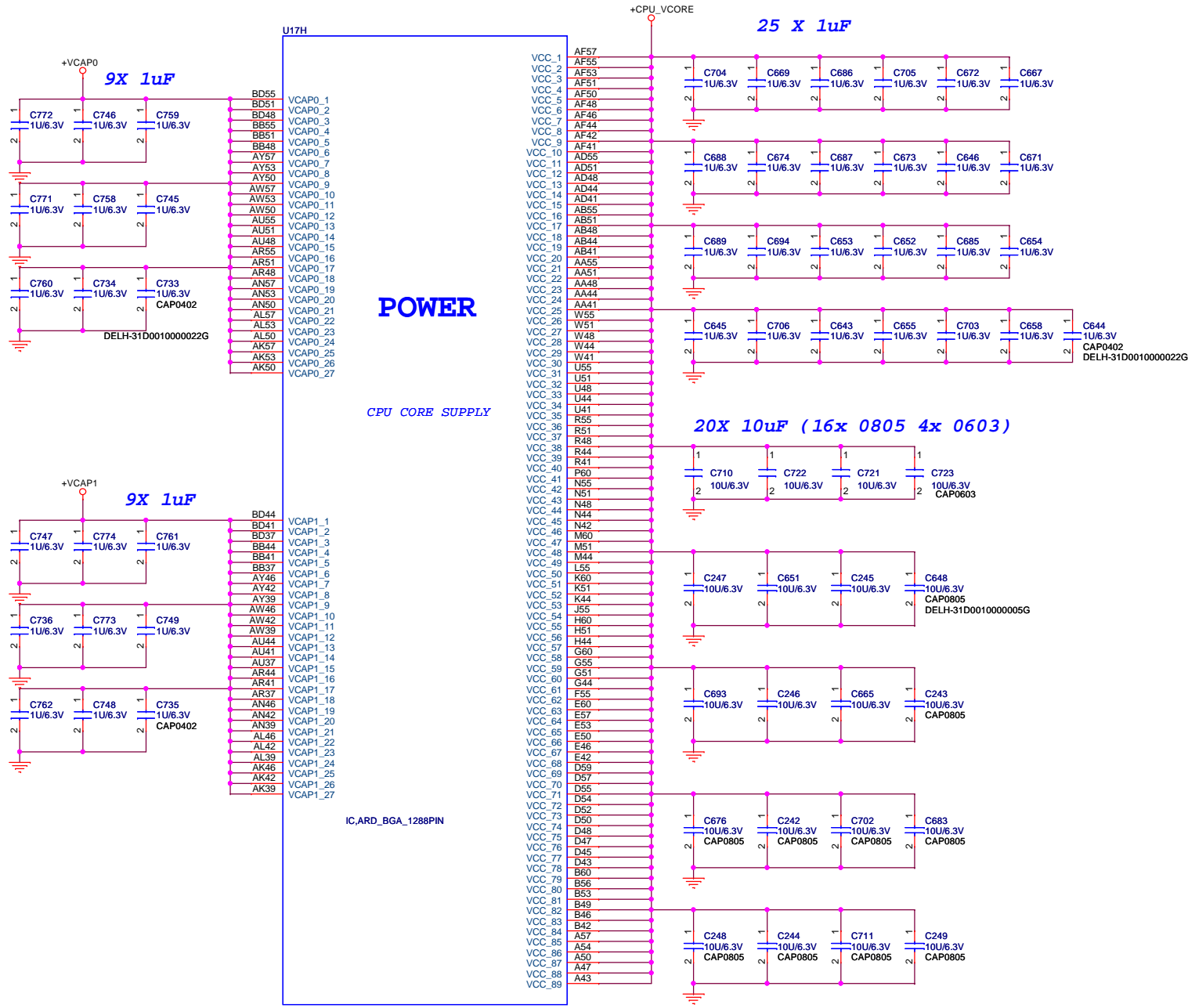
MAX 16A



Dell/ Flex Confidential		
Title CPU POWER_CORE		
Size	Document Number Inspiron Z -- INTEL	Rev X01
Date:	Monday, January 18, 2010	Sheet 9 of 57

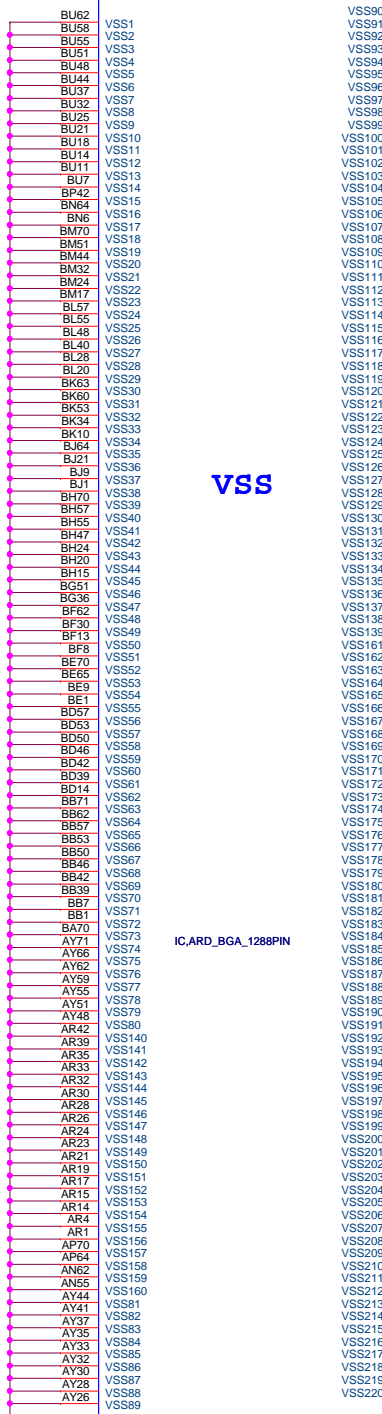
ARRANDALE PROCESSOR (POWER-CORE)

MAX 27A



ARRANDALE / CLARKSFIELD PROCESSOR (GND)

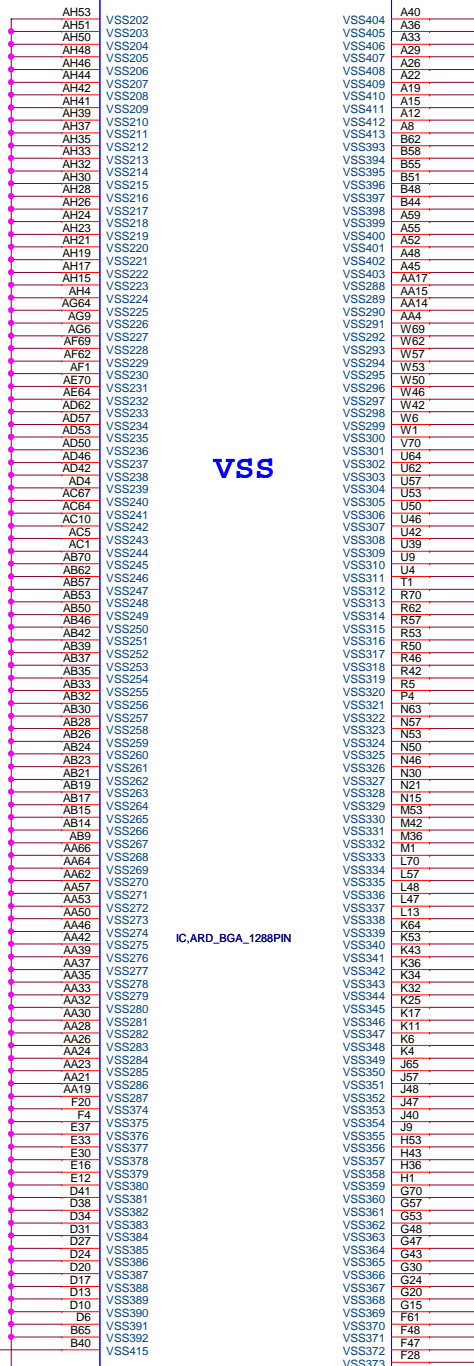
U171



VSS

IC_ARD_BGA_1288PIN

U17J

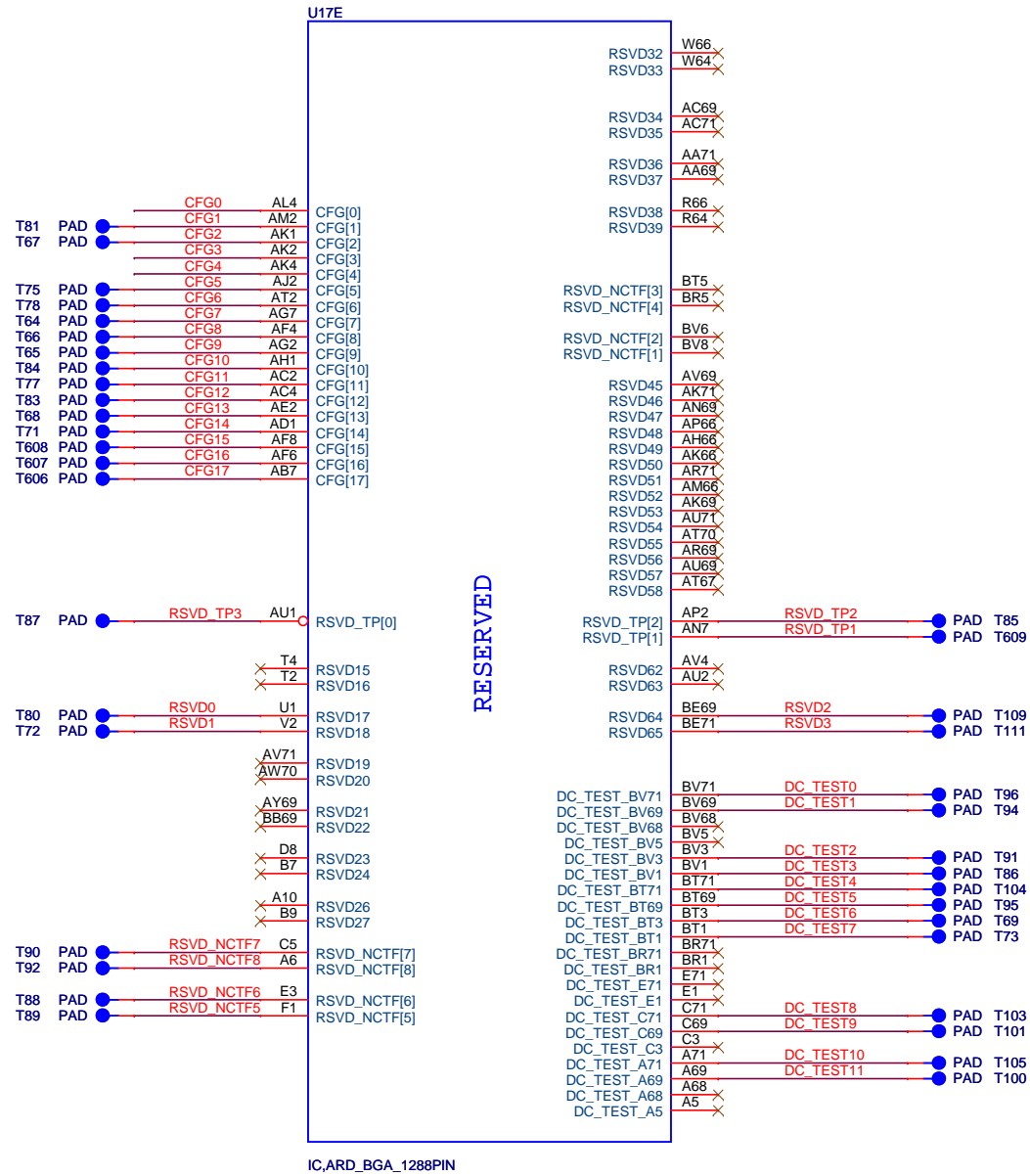


VSS

IC_ARD_BGA_1288PIN

R604

ARRANDALE /CLARKSFIELD PROCESSOR(RESERVED, CFG)



IC,ARD_BGA_1288PIN

CFG Straps for PROCESSOR

PCI-Express Configuration Select

CFG0	1:Single PEG(Default) 0:Bifurcation enabled
------	--

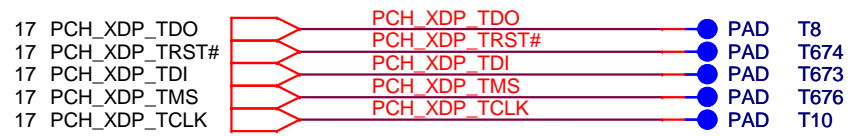
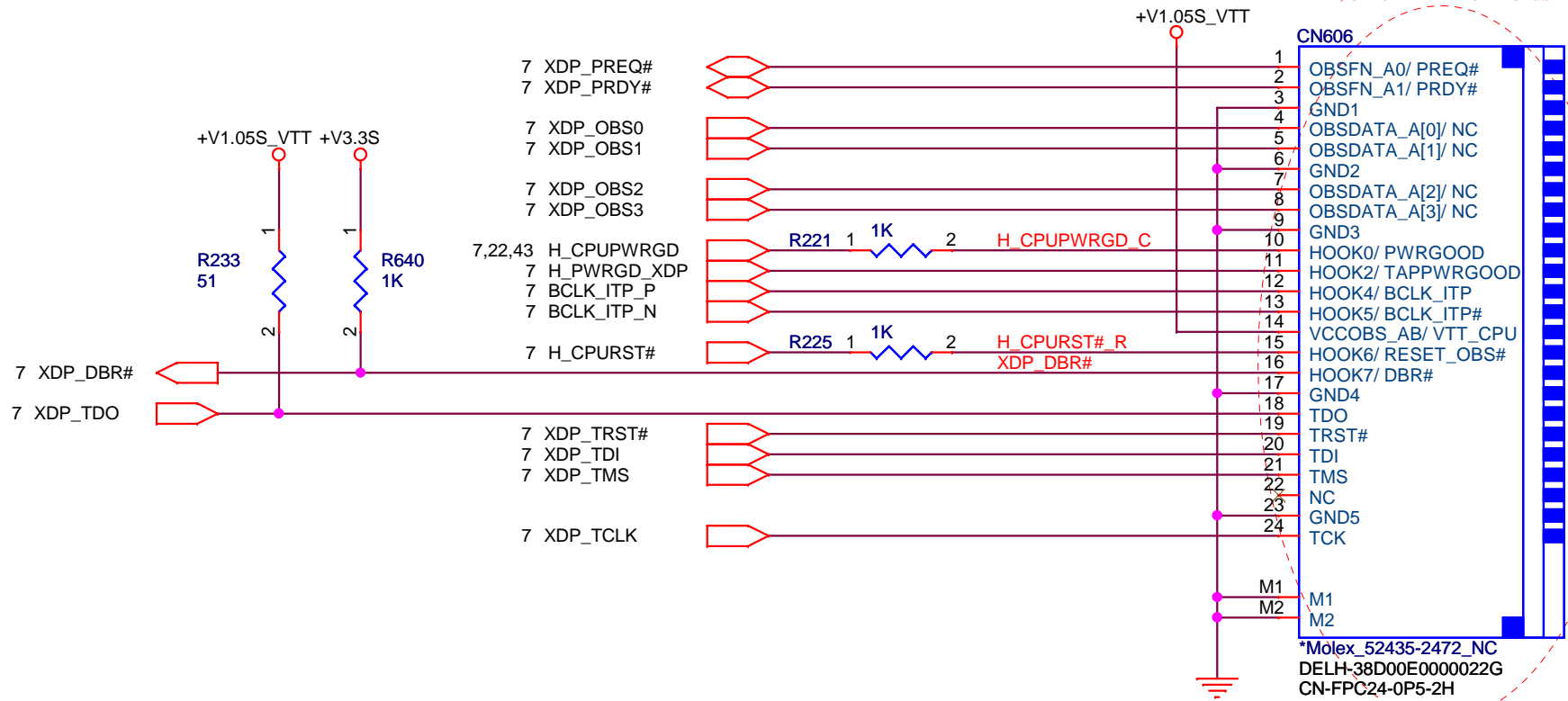
CFG3 - PCI-Express Static Lane Reversal

CFG3	1 :Normal Operation(Default) 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...
------	---

CFG4 - Display Port Presence

CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port (Default) 0:Enabled; An external Display Port device is connected to the Embedded Display Port
------	--

12/8 Del R172 for no using.

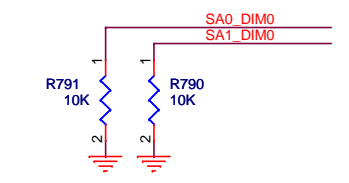
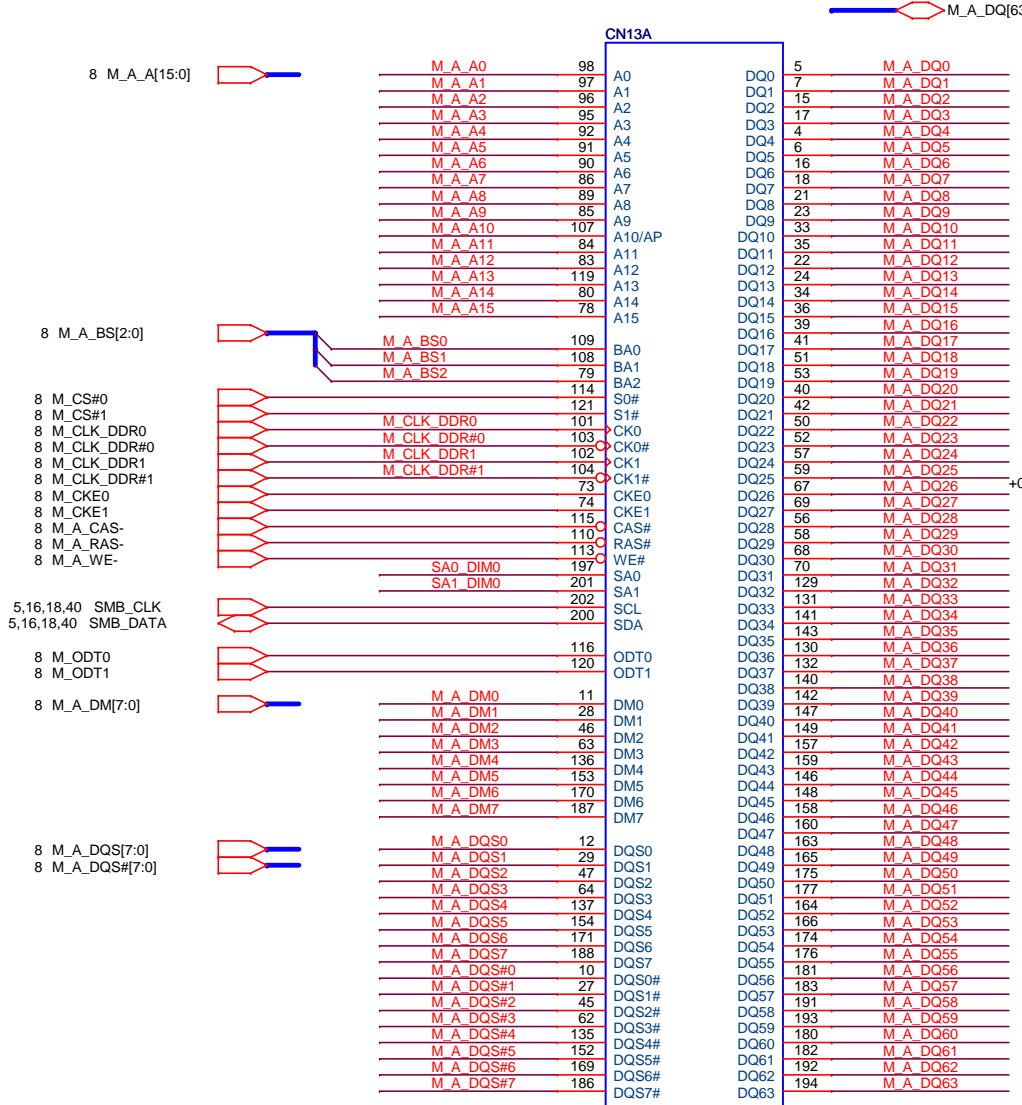


Dell/ Flex Confidential

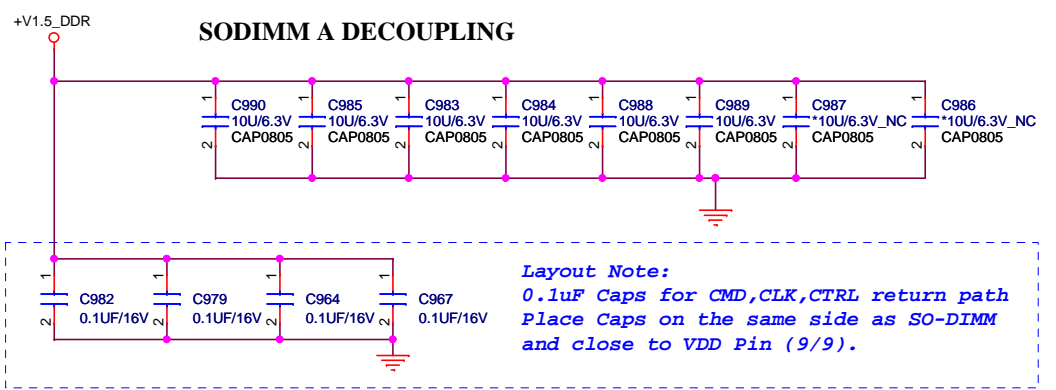
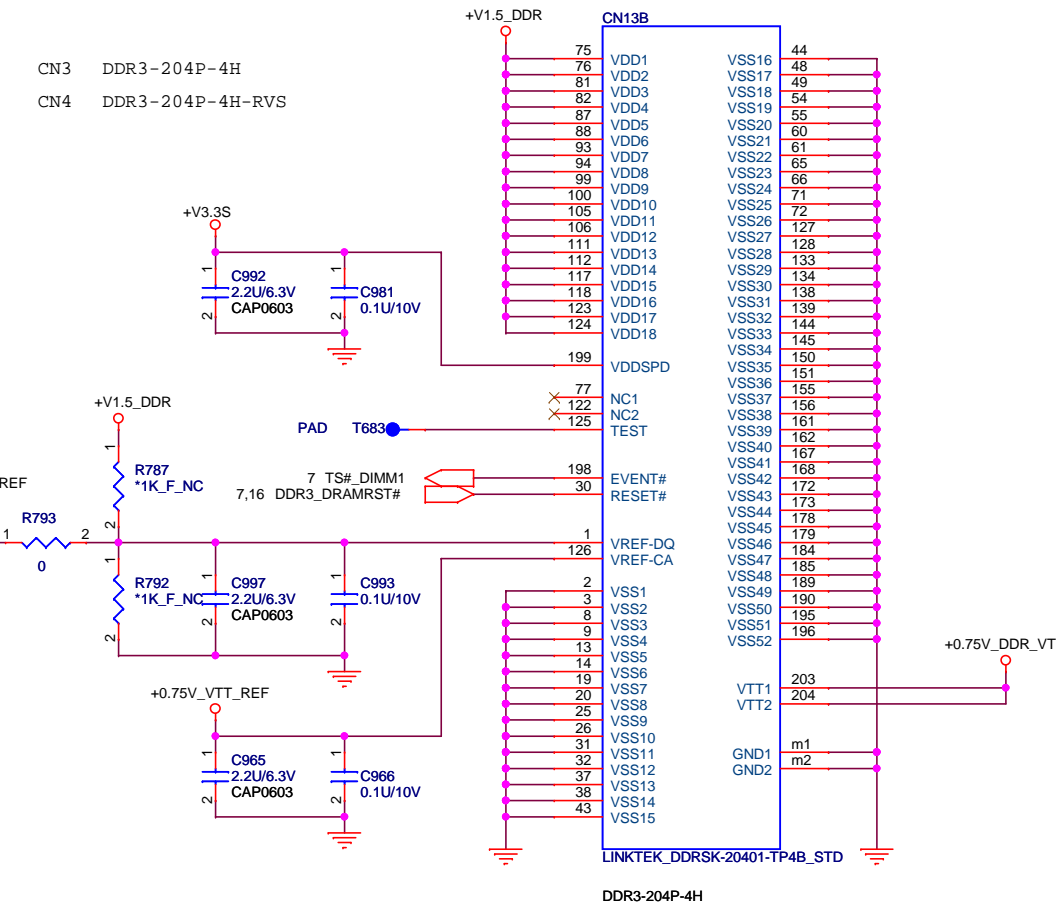
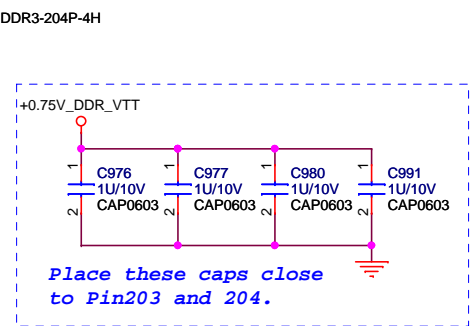
Title **XDP_PROCESSOR/ PCH**

Size	Document Number	Rev
	Inspiron Z -- INTEL	X01

Date: Monday, January 18, 2010 Sheet 14 of 57



SO-DIMM Address		
SA0_DIM0 = 0, SA1_DIM0 = 0	SPD	0xA0
	TS	0x30
SA0_DIM0 = 1, SA1_DIM0 = 0	SPD	0xA2
	TS	0x32



8 M_B_A[15:0]

M_B_A0 98
 M_B_A1 97
 M_B_A2 96
 M_B_A3 95
 M_B_A4 92
 M_B_A5 91
 M_B_A6 90
 M_B_A7 86
 M_B_A8 89
 M_B_A9 85
 M_B_A10 107
 M_B_A11 84
 M_B_A12 83
 M_B_A13 119
 M_B_A14 80
 M_B_A15 78

8 M_B_BS[2:0]

M_B_BS0 109
 M_B_BS1 108
 M_B_BS2 79

8 M_CS#2
 8 M_CS#3
 8 M_CLK_DDR2
 8 M_CLK_DDR#2
 8 M_CLK_DDR3
 8 M_CLK_DDR#3
 8 M_CKE2
 8 M_CKE3
 8 M_B_CAS-
 8 M_B_RAS-
 8 M_B_WE-

M_B_BS0 109
 M_B_BS1 108
 M_B_BS2 79
 M_CLK_DDR2 114
 M_CLK_DDR#2 121
 M_CLK_DDR3 101
 M_CLK_DDR#3 103
 M_CLK_DDR3 102
 M_CLK_DDR#3 104
 CK1# 73
 CKE0 74
 CKE1 115
 CAS# 110
 RAS# 113
 WE# 197
 SA0_DIM1 201
 SA1_DIM1 202

5,15,18,40 SMB_CLK
 5,15,18,40 SMB_DATA

SA0_DIM1 201
 SA1_DIM1 202

8 M_ODT2
8 M_ODT3

ODT0 116
 ODT1 120

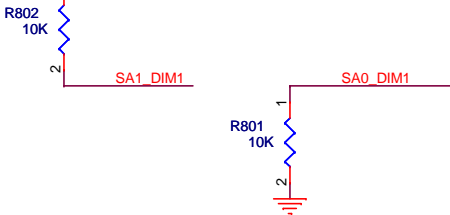
8 M_B_DM[7:0]

M_B_DM0 11
 M_B_DM1 28
 M_B_DM2 46
 M_B_DM3 63
 M_B_DM4 136
 M_B_DM5 153
 M_B_DM6 170
 M_B_DM7 187

8 M_B_DQS[7:0]
8 M_B_DQS#[7:0]

M_B_DQS0 12
 M_B_DQS1 29
 M_B_DQS2 47
 M_B_DQS3 64
 M_B_DQS4 137
 M_B_DQS5 154
 M_B_DQS6 171
 M_B_DQS7 188
 M_B_DQS#0 10
 M_B_DQS#1 27
 M_B_DQS#2 45
 M_B_DQS#3 62
 M_B_DQS#4 135
 M_B_DQS#5 152
 M_B_DQS#6 169
 M_B_DQS#7 186

+V3.3S



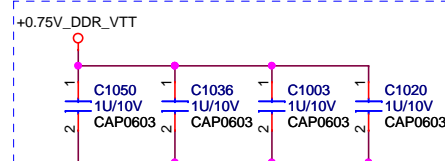
SO-DIMM Address	
SPD	0xA4
TS	0x34

CN14A
 A0
 A1
 A2
 A3
 A4
 A5
 A6
 A7
 A8
 A9
 A10/AP
 A11
 A12
 A13
 A14
 A15

DQ0 5
 DQ1 7
 DQ2 15
 DQ3 17
 DQ4 4
 DQ5 6
 DQ6 16
 DQ7 21
 DQ8 18
 DQ9 23
 DQ10 33
 DQ11 35
 DQ12 22
 DQ13 24
 DQ14 34
 DQ15 36
 DQ16 39
 DQ17 41
 DQ18 51
 DQ19 53
 DQ20 40
 DQ21 42
 DQ22 50
 DQ23 52
 DQ24 57
 DQ25 59
 DQ26 67
 DQ27 69
 DQ28 56
 DQ29 58
 DQ30 68
 DQ31 70
 DQ32 129
 DQ33 131
 DQ34 141
 DQ35 143
 DQ36 130
 DQ37 132
 DQ38 140
 DQ39 142
 DQ40 147
 DQ41 149
 DQ42 157
 DQ43 159
 DQ44 146
 DQ45 148
 DQ46 158
 DQ47 160
 DQ48 163
 DQ49 165
 DQ50 175
 DQ51 177
 DQ52 166
 DQ53 174
 DQ54 176
 DQ55 181
 DQ56 183
 DQ57 191
 DQ58 193
 DQ59 180
 DQ60 182
 DQ61 192
 DQ62 194
 DQ63 194

LINKTEK_DDRRK-20401-TP4B

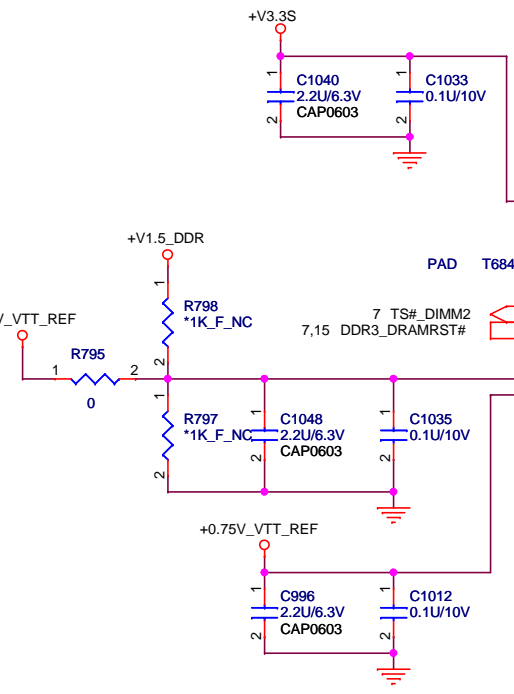
DDR3-204P-4H-RVS



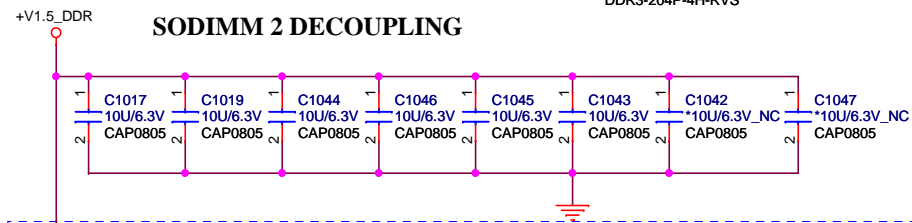
Place these caps close
 to Pin203 and 204.

M_B_DQ[63:0] 8

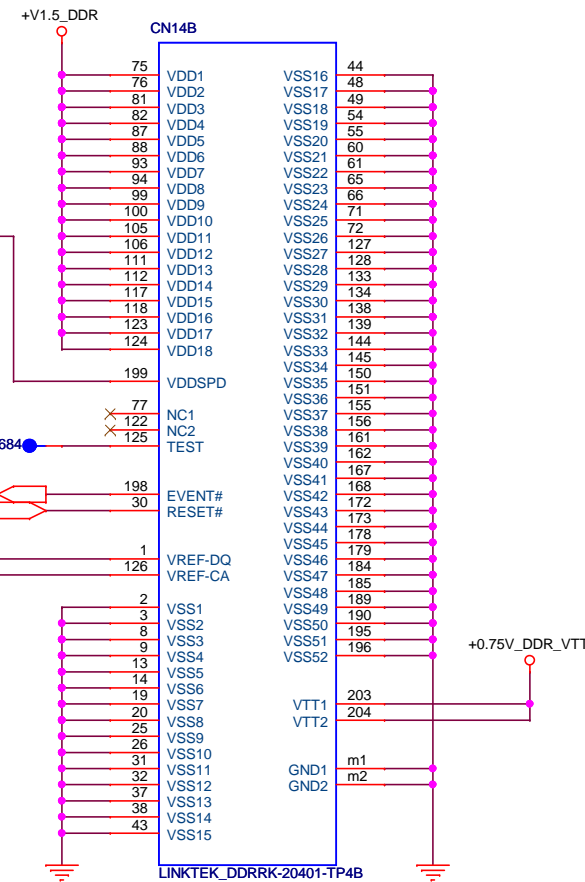
CN13 DDR3-204P-4H
 CN14 DDR3-204P-4H-RVS



SODIMM 2 DECOUPLING



Layout Note:
 0.1uF Caps for CMD,CLK,CTRL return path
 Place Caps on the same side as SO-DIMM
 and close to VDD Pin (9/9).



DDR3-204P-4H-RVS

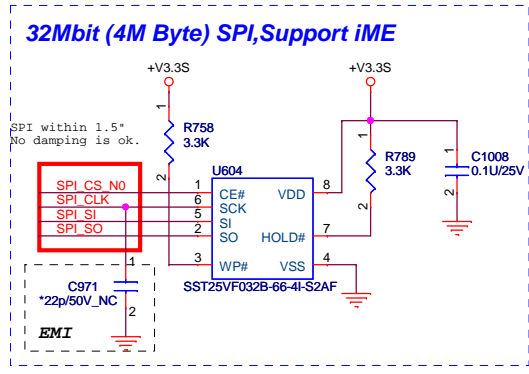
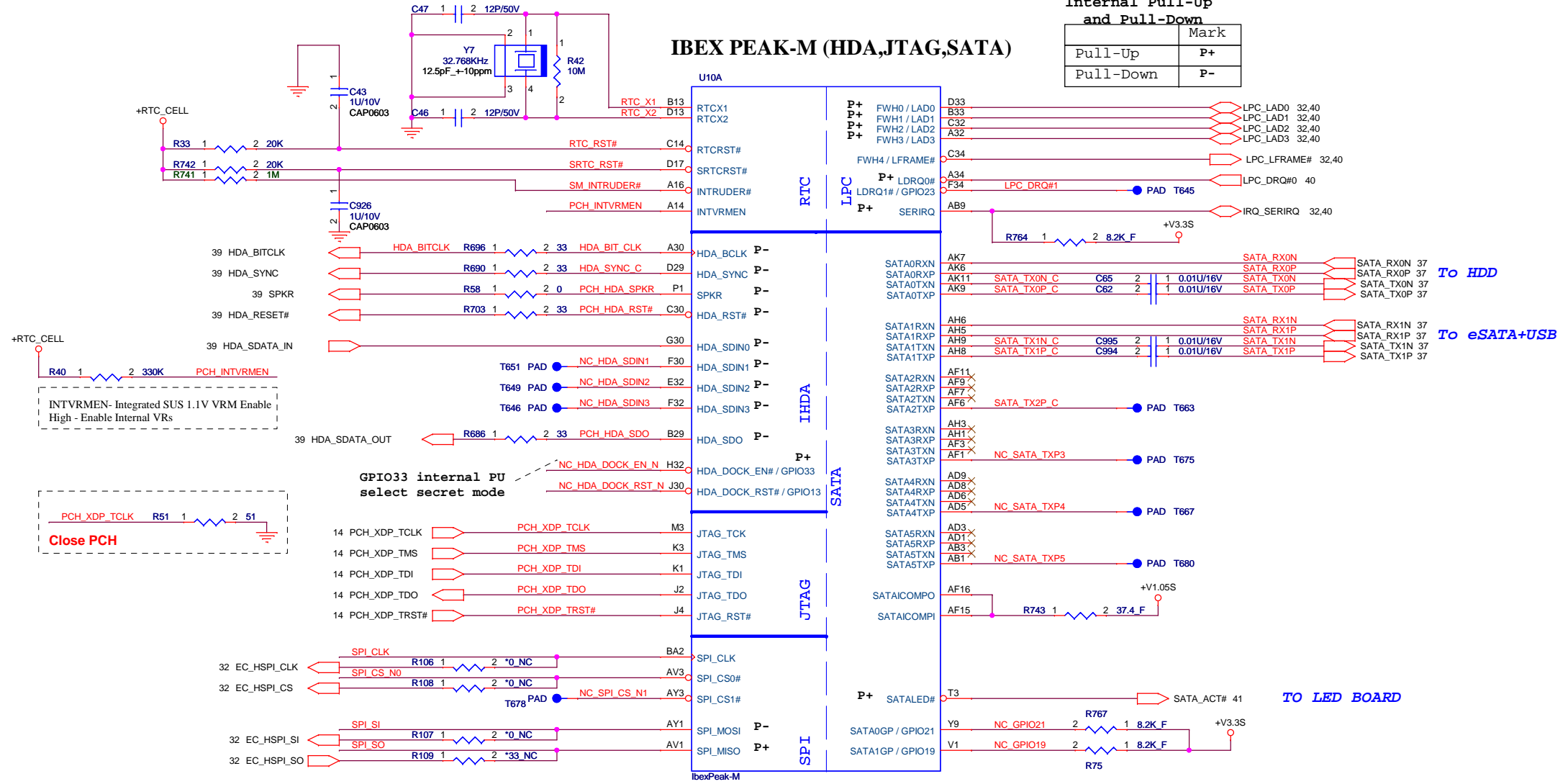
LINKTEK_DDRRK-20401-TP4B

Dell/ Flex Confidential		
Title	DDR3 SO-DIMM2_204P_RVS	
Size	Document Number	Rev X01
Date:	Monday, January 18, 2010	Sheet 16 of 57

IBEX PEAK-M (HDA,JTAG,SATA)

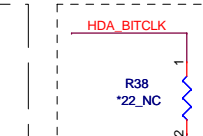
Internal Pull-Up and Pull-Down

Pull-Up	Mark
Pull-Up	P+
Pull-Down	P-



NO REBOOT STRAP		
HDA_SPKR	NA	Low=Default
	MOUNTED	High=No Reboot

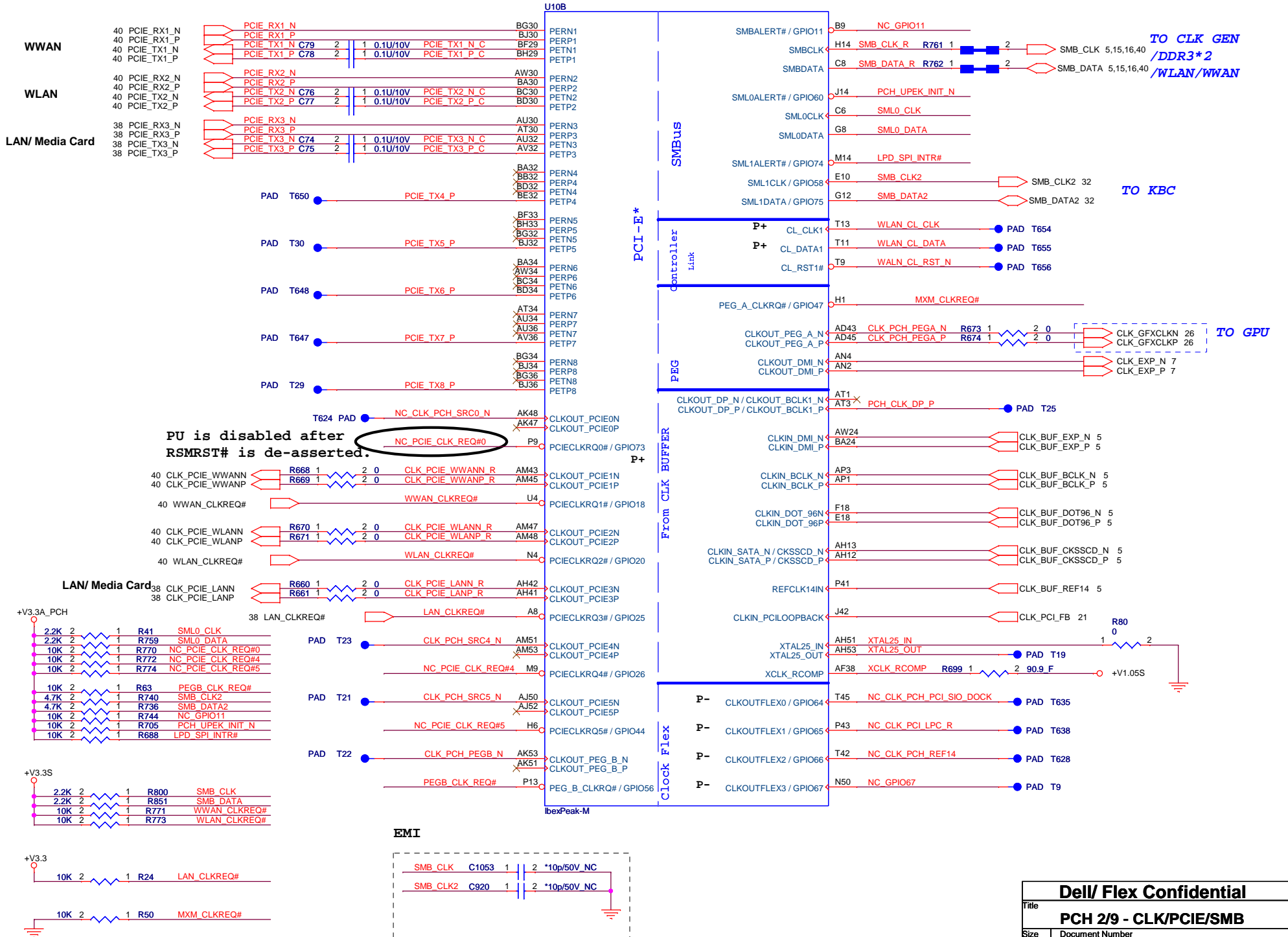
iTPM ENABLE/DISABLE		
SPI_SI	NA	Low=Disable(Default)
	MOUNTED	High=Enable



Flash Descriptor Security

High	Flash Descriptor will be in effect (default)
Low	Descriptor Security will be overridden

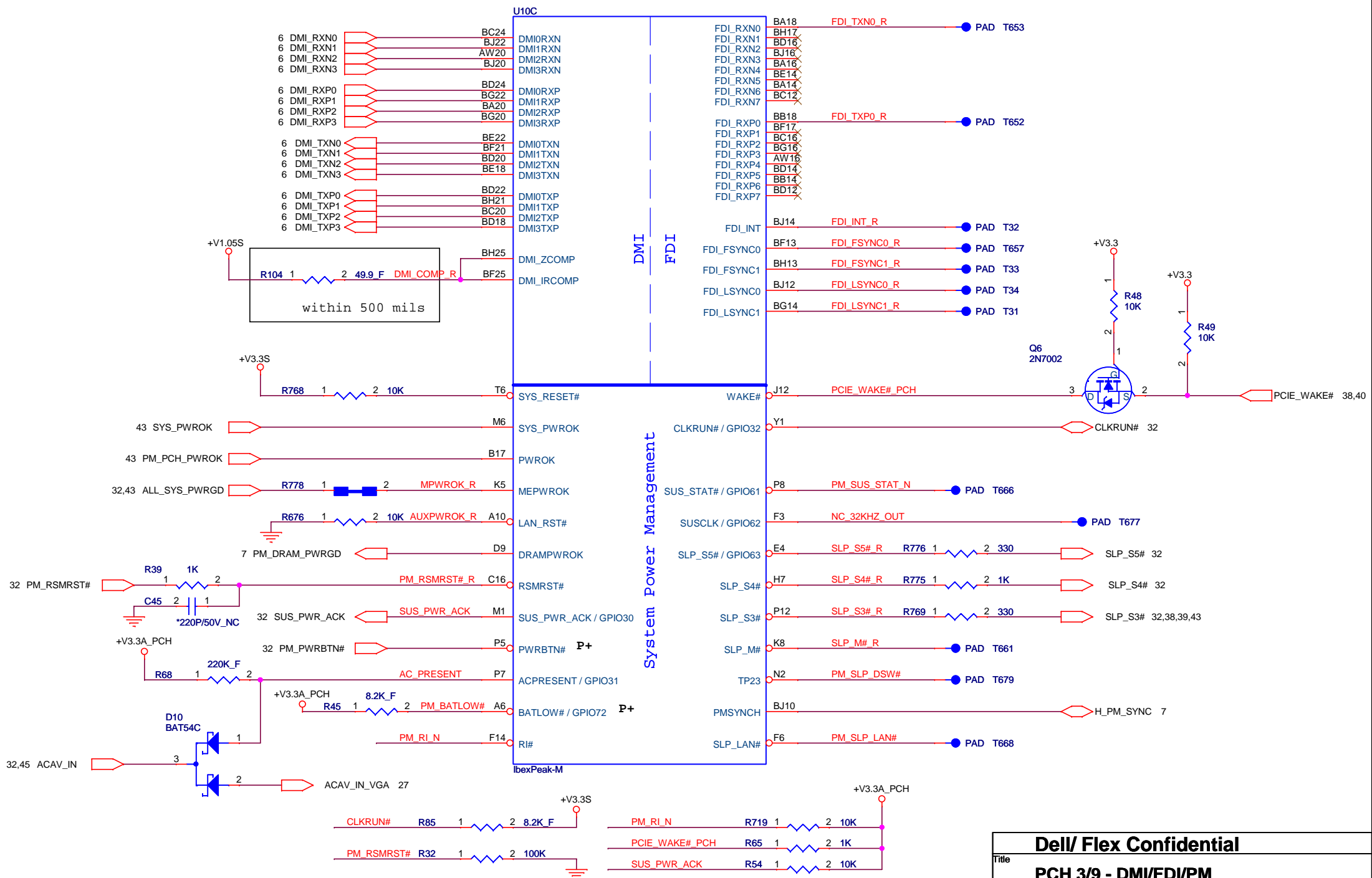
IBEX PEAK-M (PCI-E,SMBUS,CLK)



PU is disabled after RSMRST# is de-asserted.

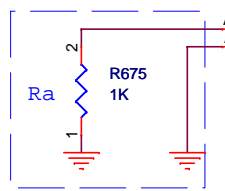
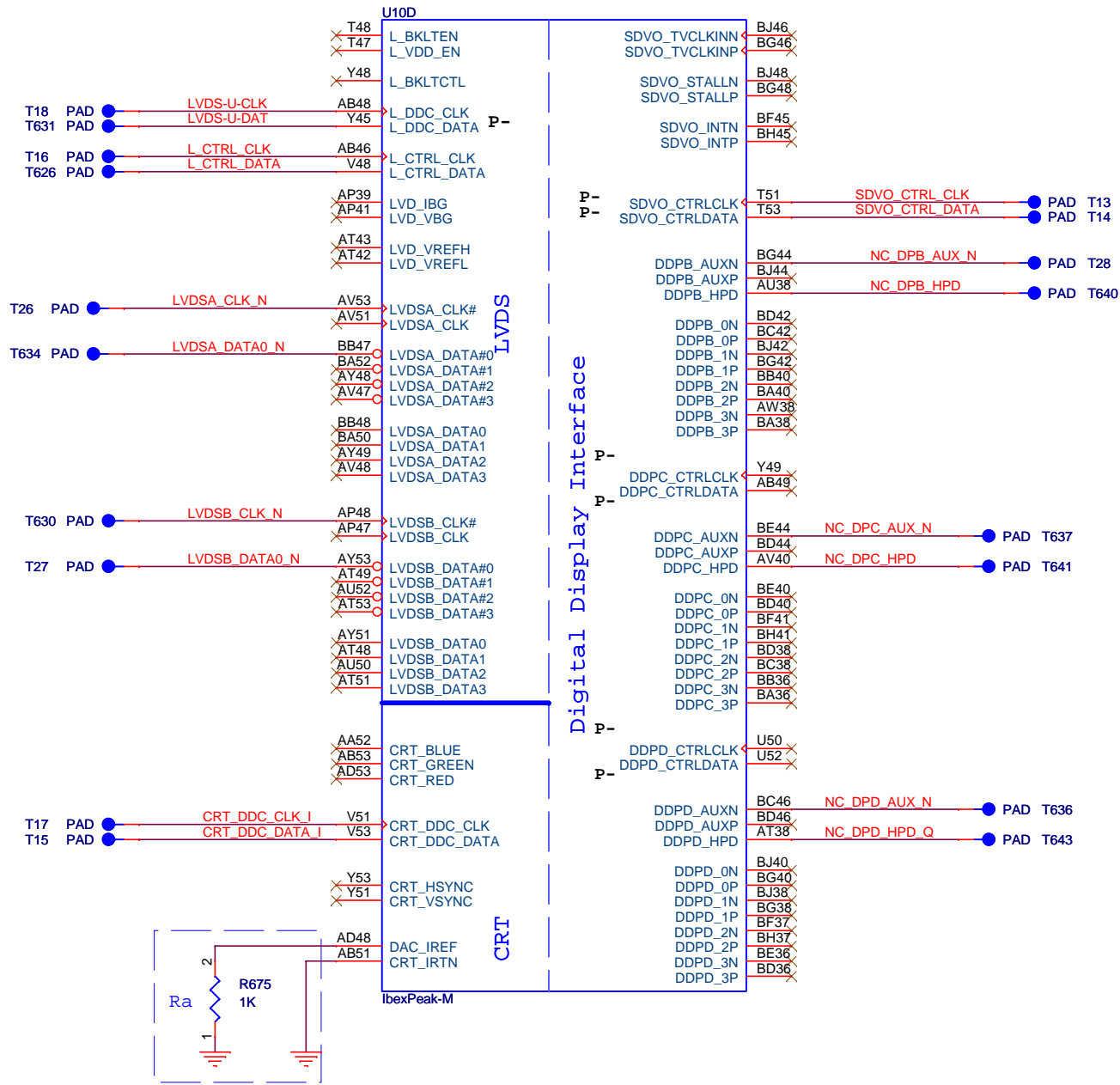
NC_PCIE_CLK_REQ#0

IBEX PEAK-M (DMI,FDI,GPIO)



Dell/ Flex Confidential		
PCH 3/9 - DMI/FDI/PM		
Size	Document Number	Rev
	Inspiron Z -- INTEL	X01
Date:	Monday, January 18, 2010	Sheet 19 of 57

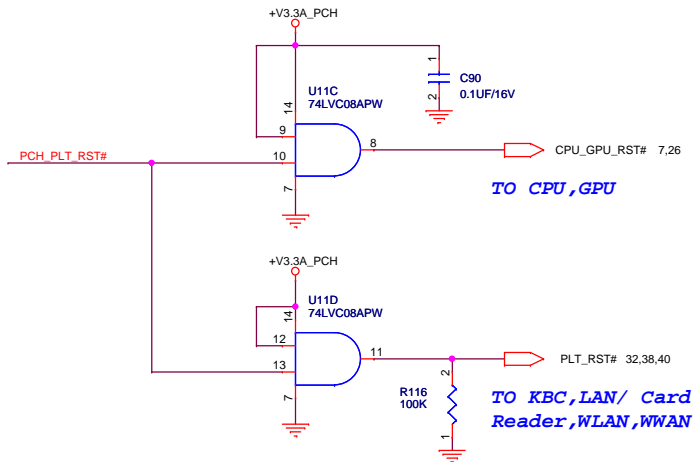
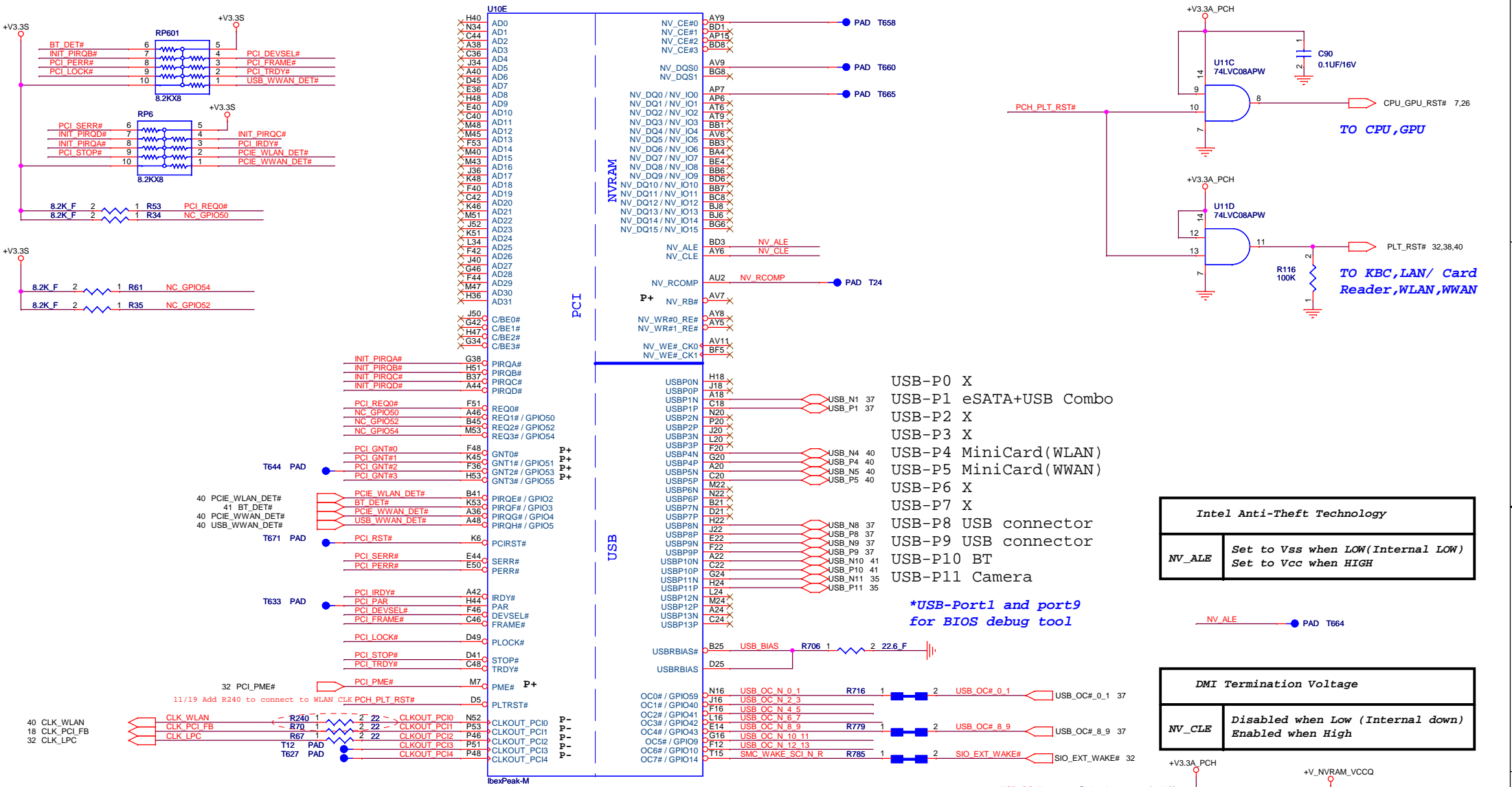
IBEX PEAK-M (LVDS,DDI)



Internal VGA disable
keep Ra to GND and IRTN
keep connect to GND

Dell/ Flex Confidential		
Title PCH 4/9 - CRT/DP/LVDS		
Size	Document Number Inspiron Z -- INTEL	Rev X01
Date:	Monday, January 18, 2010	Sheet 20 of 57

IBEX PEAK-M (PCI,USB,INTEL(R) TURBO MEMORY)



- USB-P0 X
- USB-P1 eSATA+USB Combo
- USB-P2 X
- USB-P3 X
- USB-P4 MiniCard(WLAN)
- USB-P5 MiniCard(WWAN)
- USB-P6 X
- USB-P7 X
- USB-P8 USB connector
- USB-P9 USB connector
- USB-P10 BT
- USB-P11 Camera

**USB-Port1 and port9 for BIOS debug tool*

Intel Anti-Theft Technology	
NV_ALE	Set to Vss when LOW (Internal LOW) Set to Vcc when HIGH

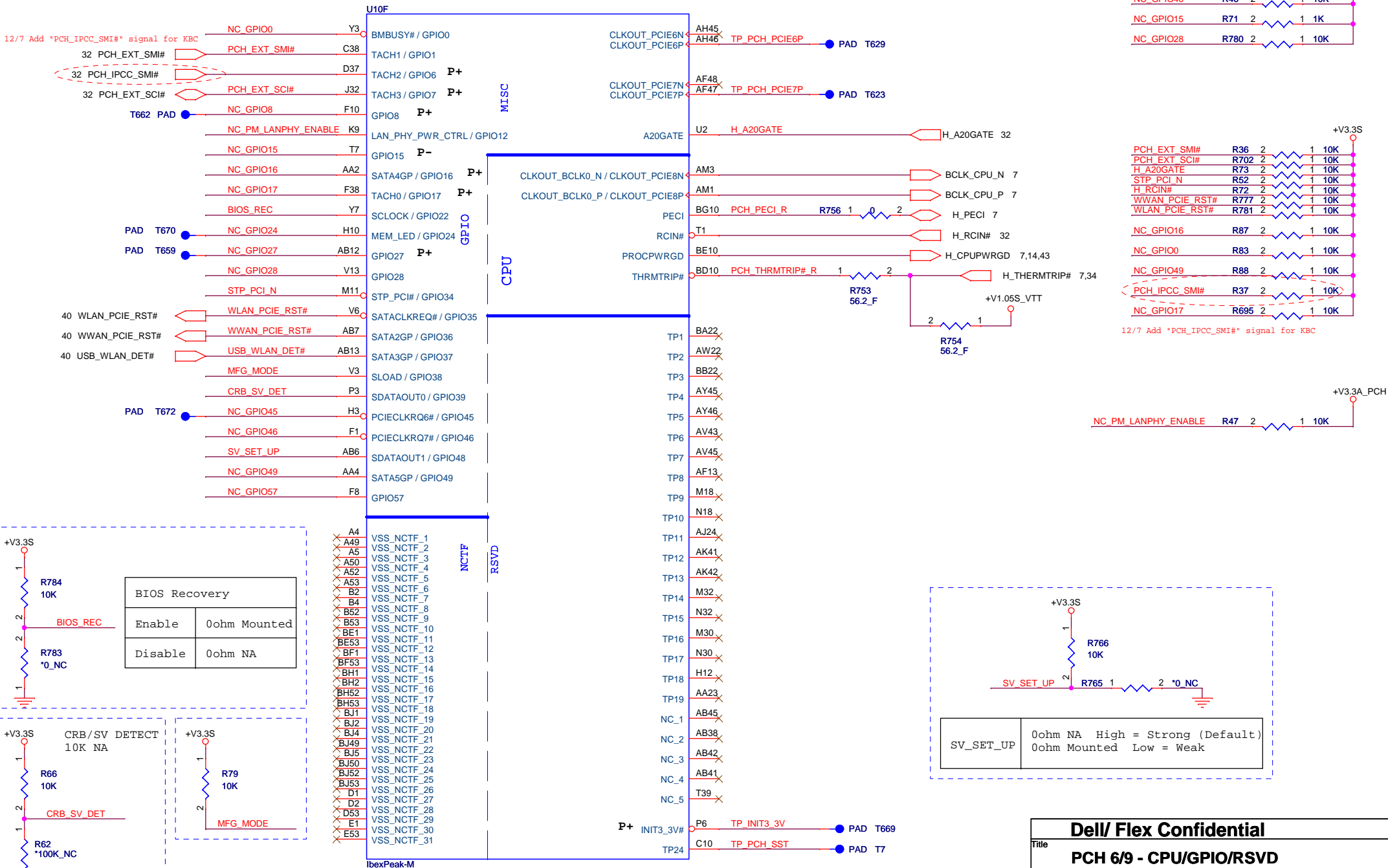
DMI Termination Voltage	
NV_CLE	Disabled when Low (Internal down) Enabled when High

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT_N3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

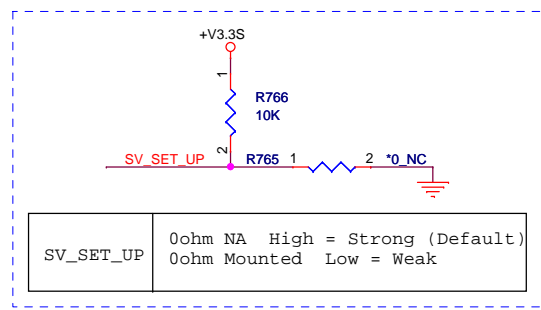
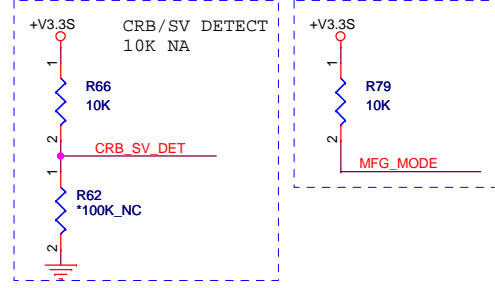
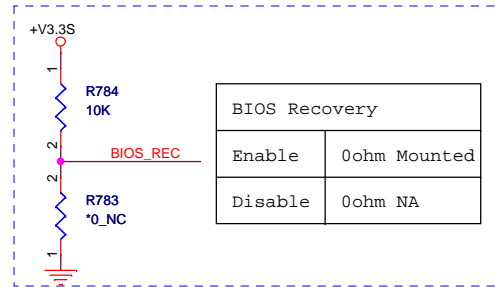
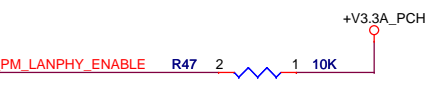
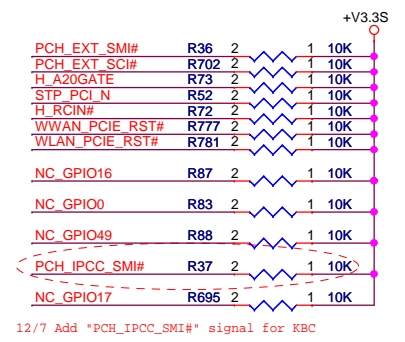
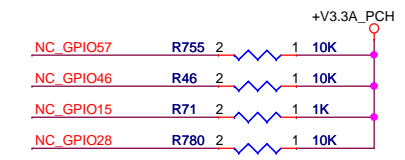
Boot BIOS Strap(internal pull up 20k)		
PCI_GNT_N0	PCI_GNT_N1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI -> NOW

Dell/ Flex Confidential		
PCH 5/9 - PCI/USB/NVRAM		
Size	Document Number	Rev X01
Date:	Monday, January 18, 2010	Sheet 21 of 57

IBEX PEAK-M(GPIO,VSS_NCTF,RSVD)



12/7 Add "PCH_IPCC_SMI#" signal for KBC



IBEX PEAK-M(POWER)

POWER

USB

Clock and Miscellaneous

PCI/GPIO/LPC

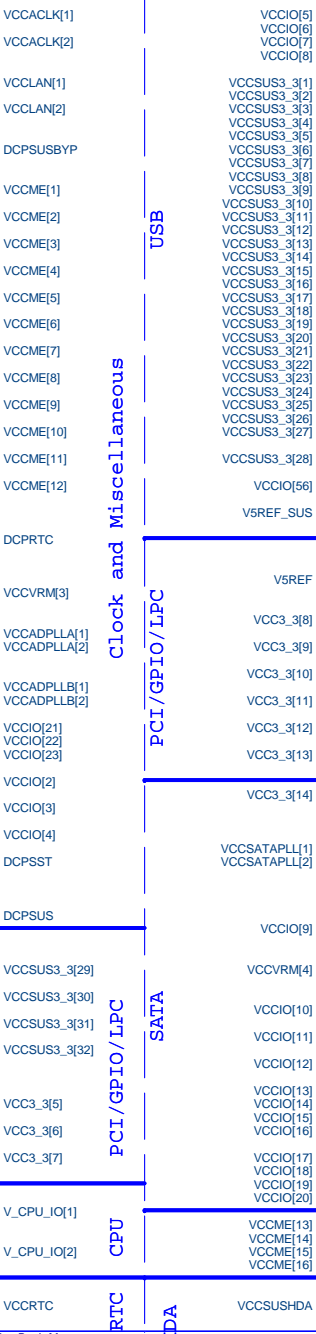
SATA

PCI/GPIO/LPC

CPU

RTC

HDA



320mA

VCCME Total
3062mA

Please note that all IbeX Peak-M rails with netnames +V1.1S and +V1.1M rails are actually +V1.05S and +V1.05M rails

1UF*2 pcs for 2 blocks

Internal VRM supply

68mA
69mA

VCCIO Total
3062mA

VCCSUS3_3 Total
163mA

<1mA

<1mA

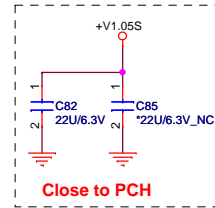
VCC3_3 Total
357mA

31mA

<1mA

2mA

6mA

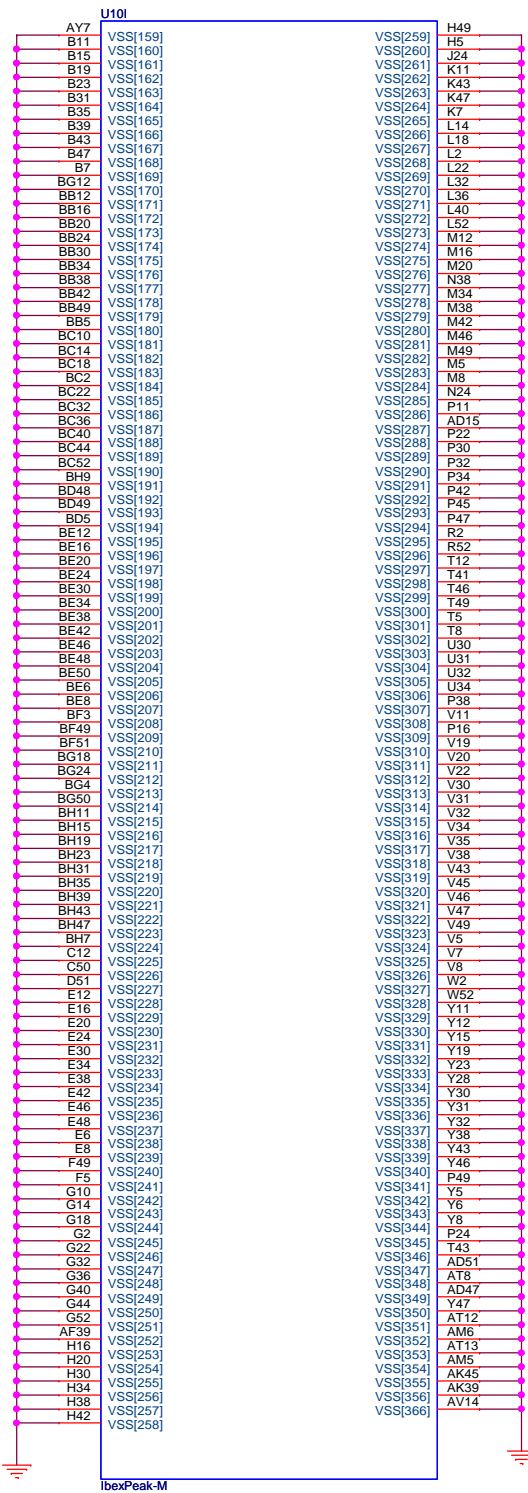
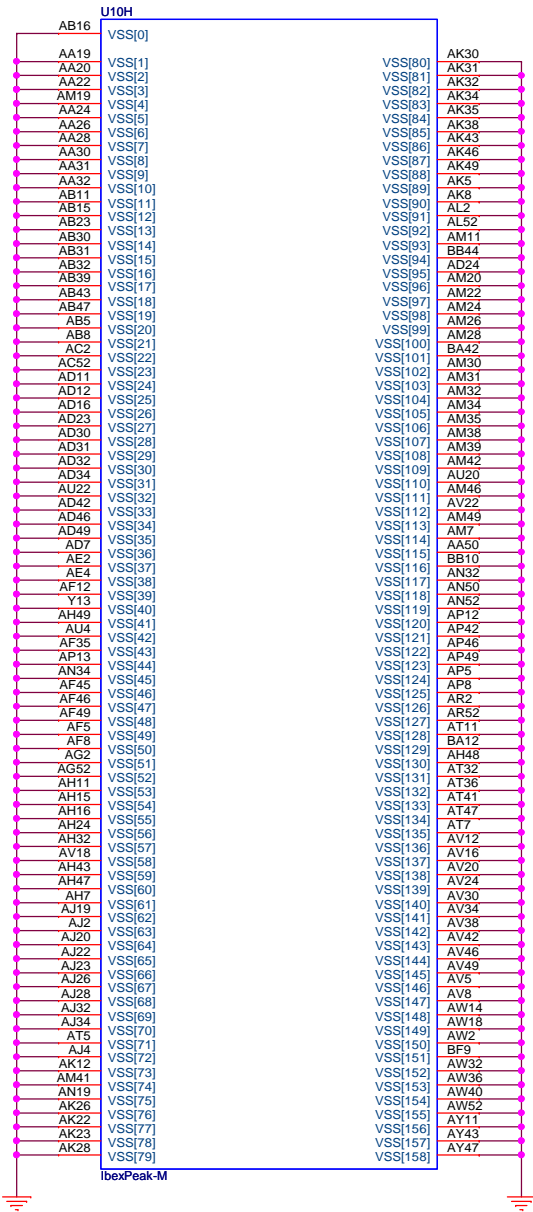


+5V_ALW has off during S4/S5 battery mode.

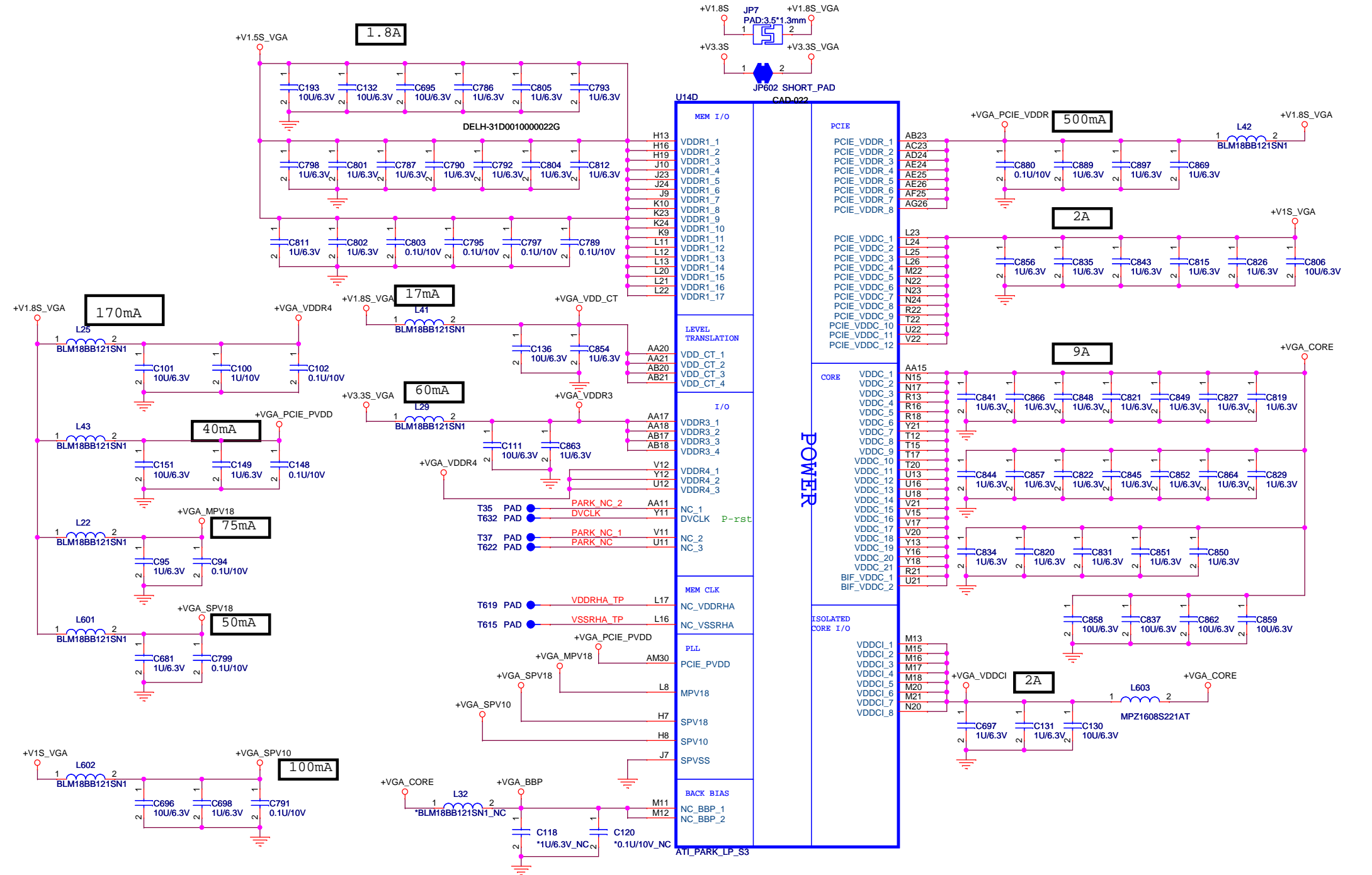


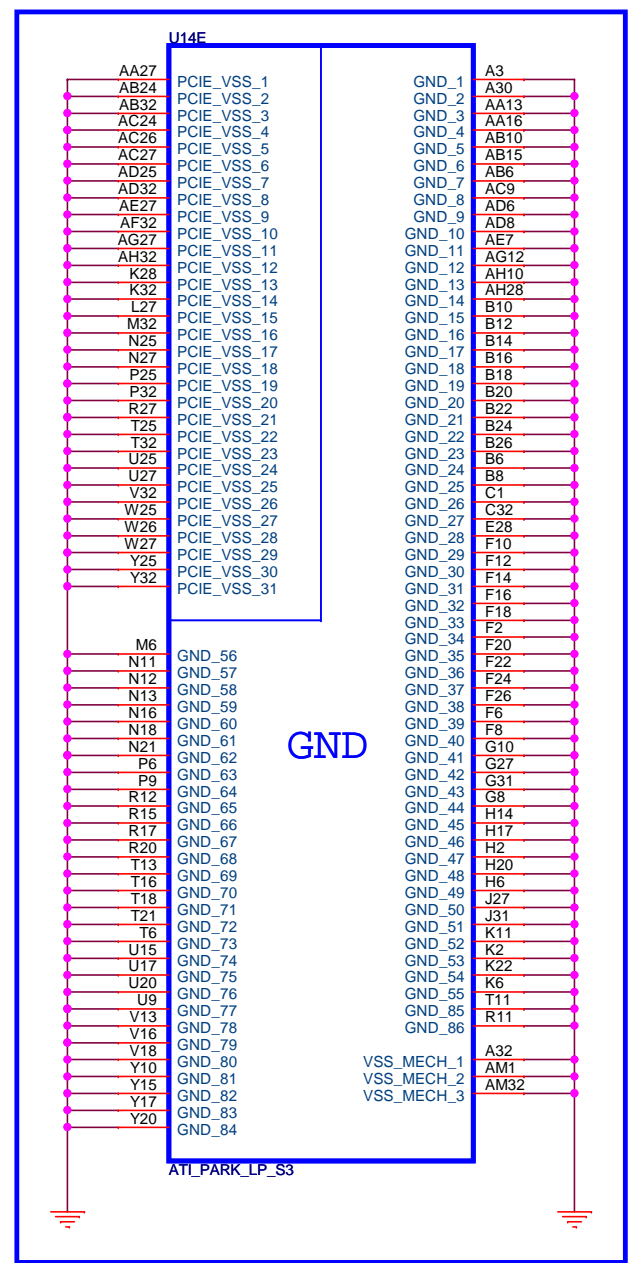
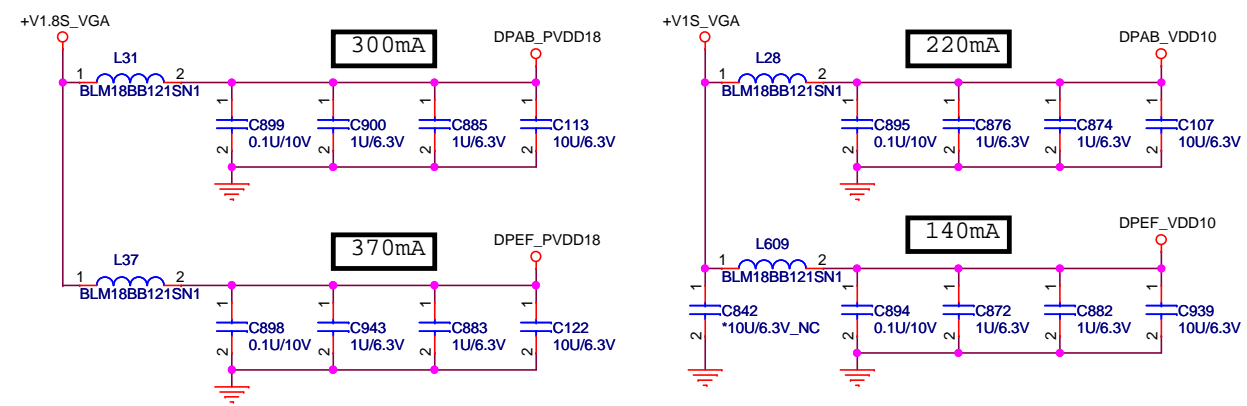
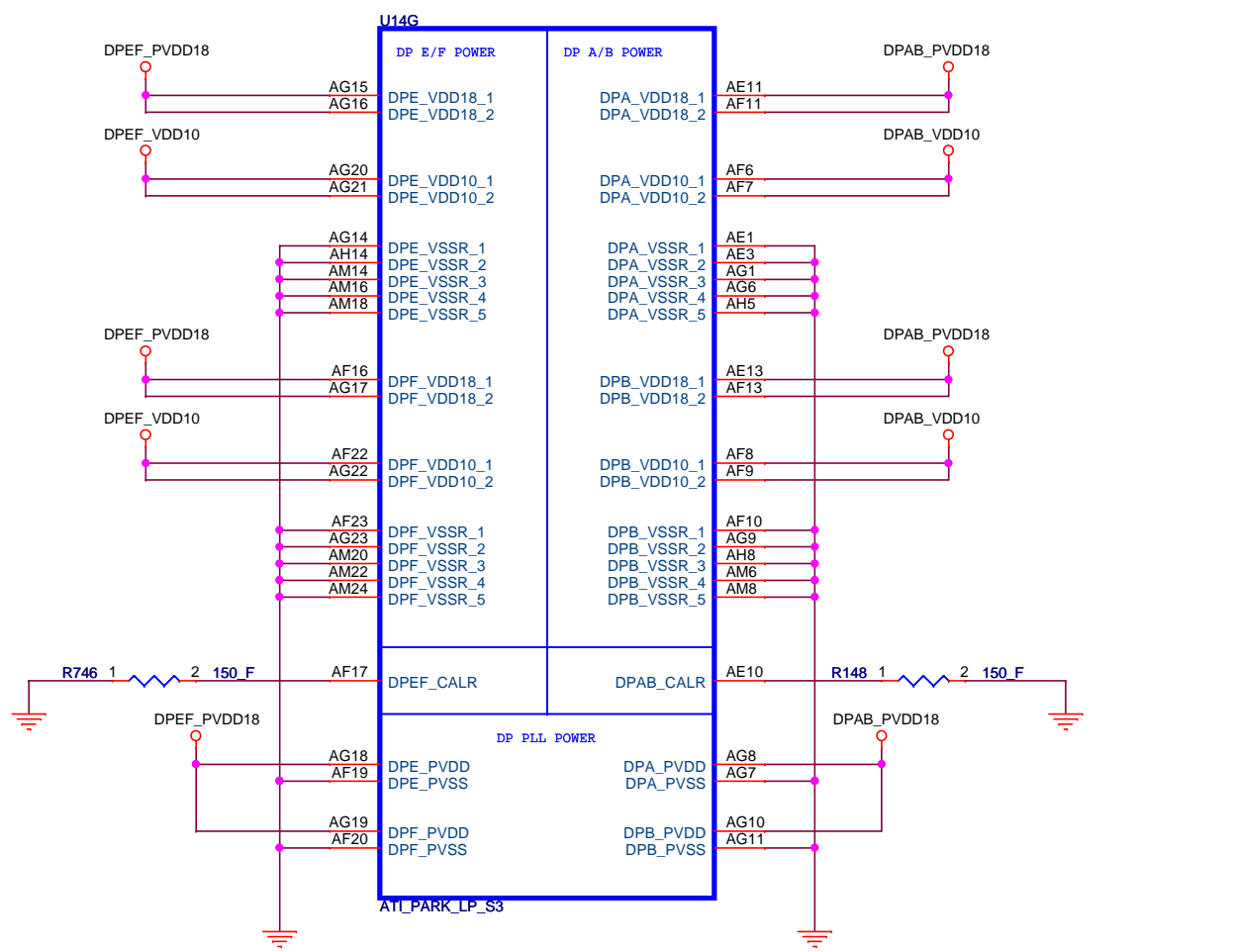
Dell/ Flex Confidential		
Title PCH 8/9 - POWER_2		
Size	Document Number Inspiron Z -- INTEL	Rev X01
Date:	Monday, January 18, 2010	Sheet 24 of 57

IBEX PEAK-M (GND)

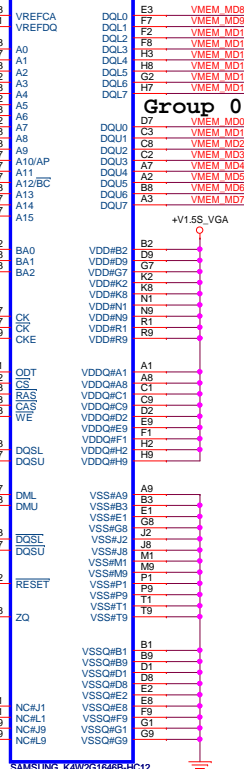


Dell/ Flex Confidential		
Title		
PCH 9/9 - GND		
Size	Document Number	Rev X01
Inspiron Z -- INTEL		
Date:	Monday, January 18, 2010	Sheet 25 of 57

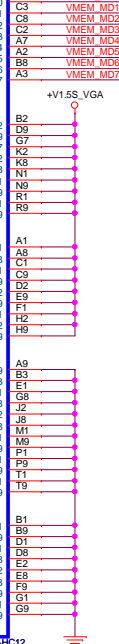




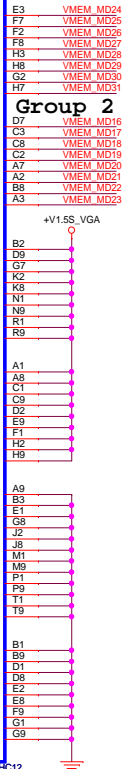
U15 Group 1



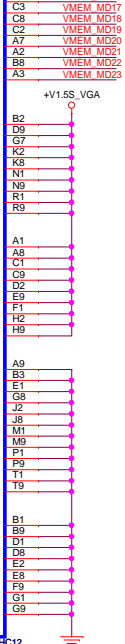
Group 0



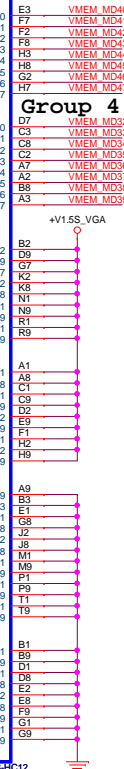
U601 Group 3



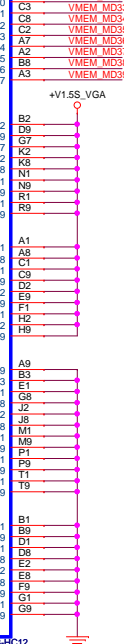
Group 2



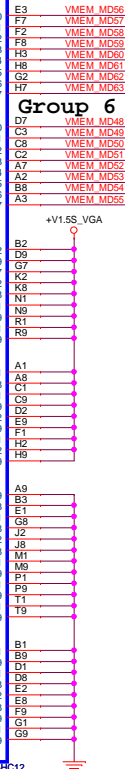
U13 Group 5



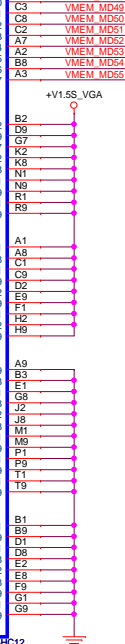
Group 4



U602 Group 7



Group 6

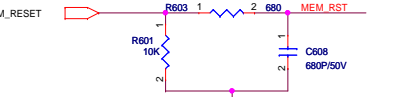
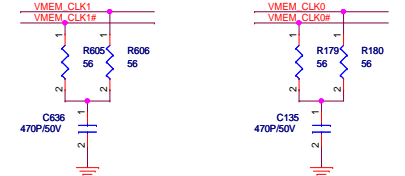
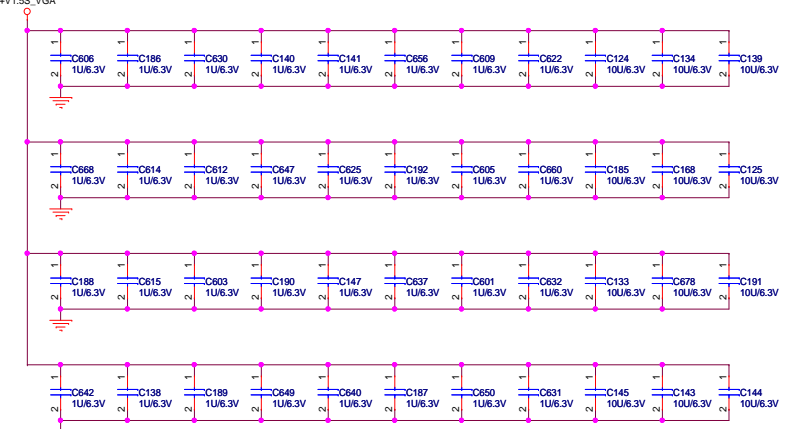
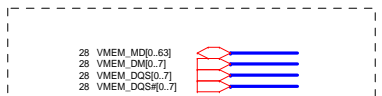
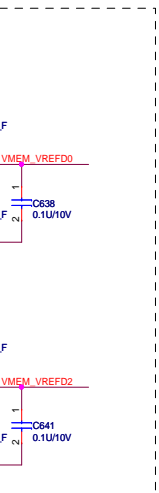


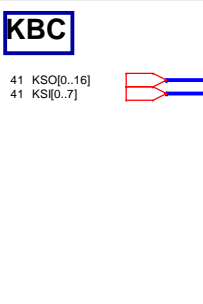
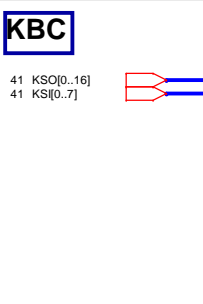
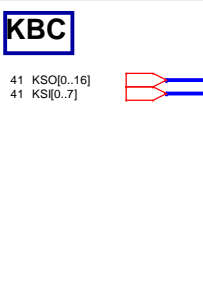
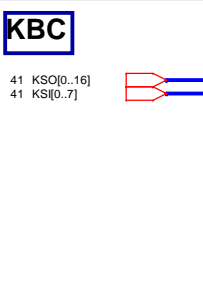
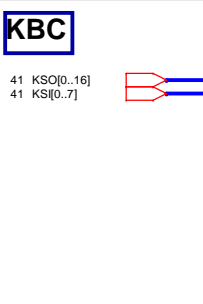
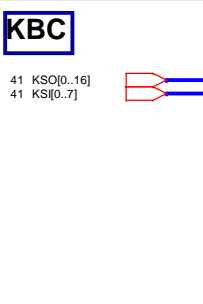
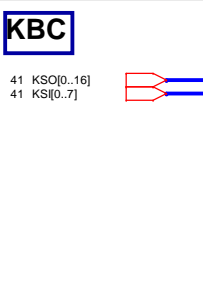
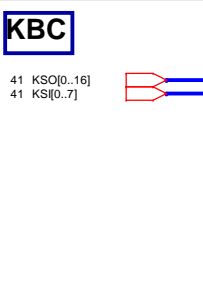
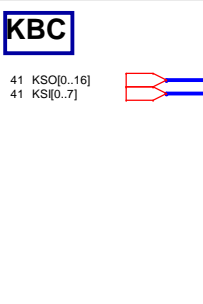
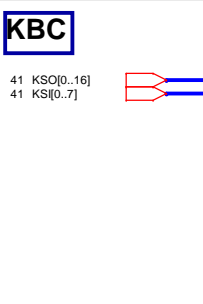
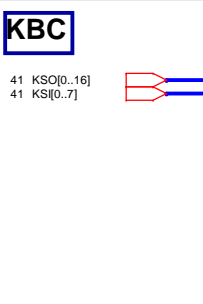
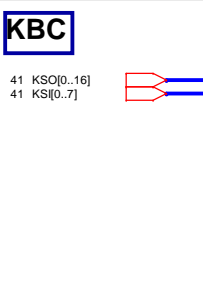
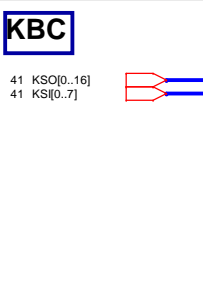
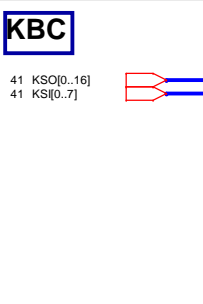
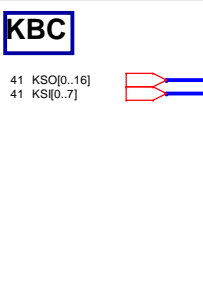
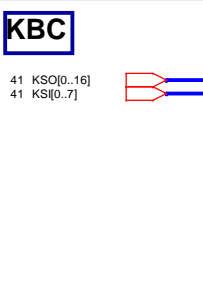
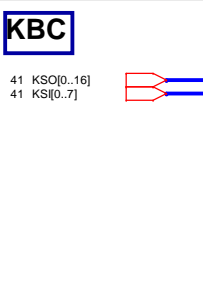
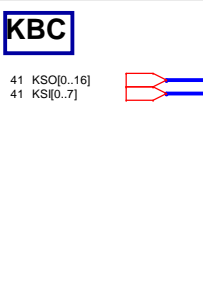
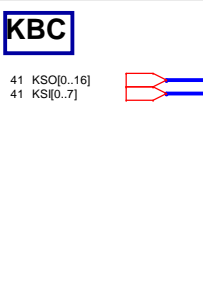
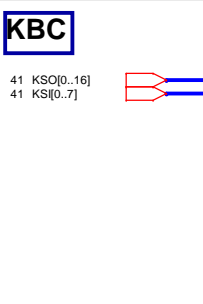
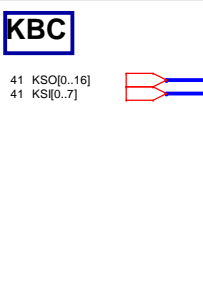
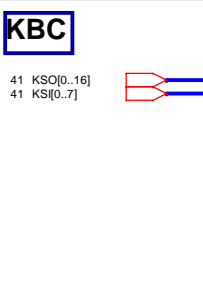
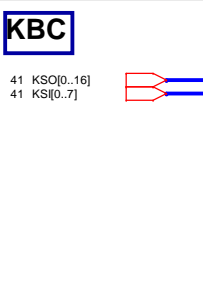
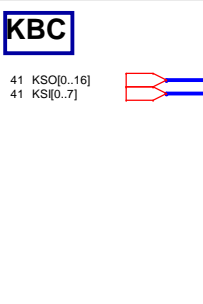
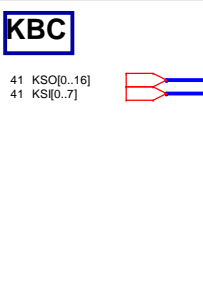
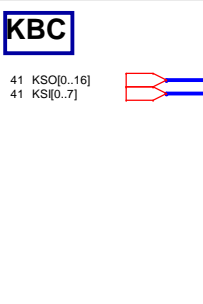
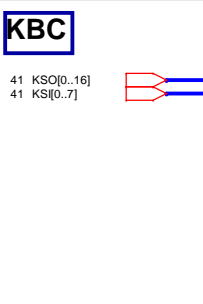
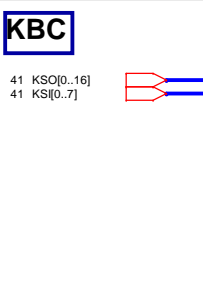
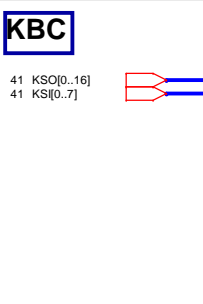
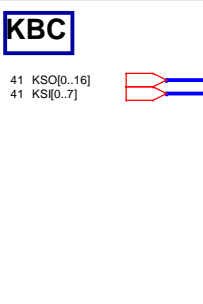
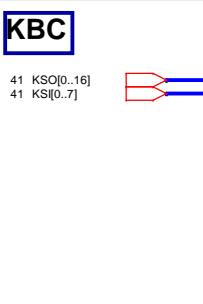
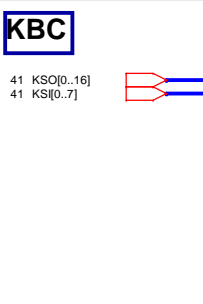
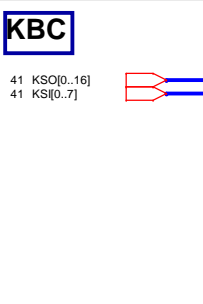
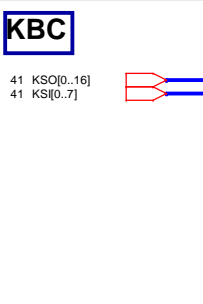
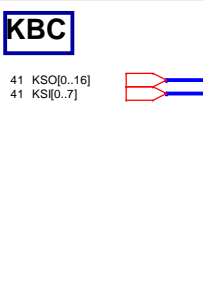
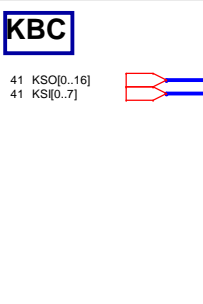
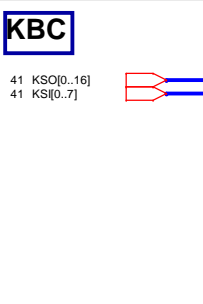
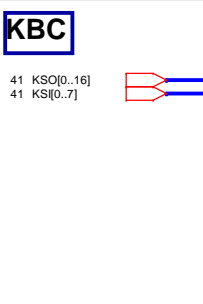
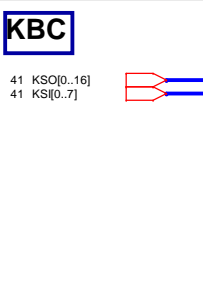
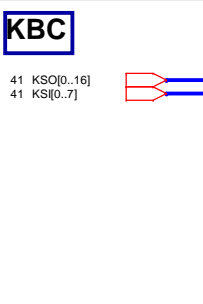
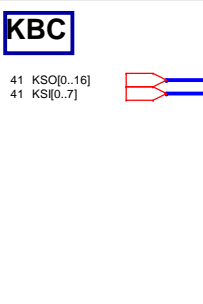
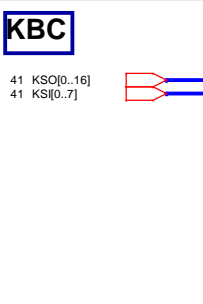
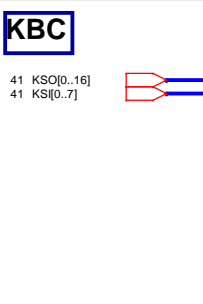
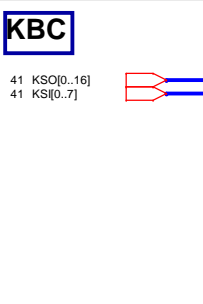
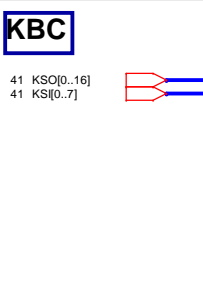
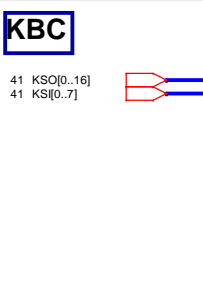
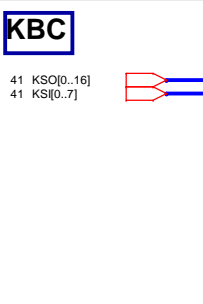
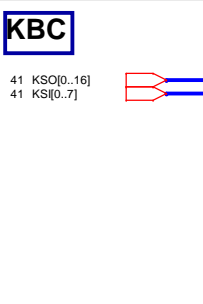
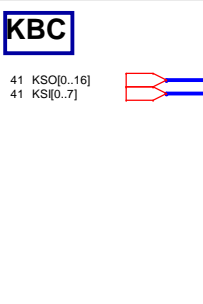
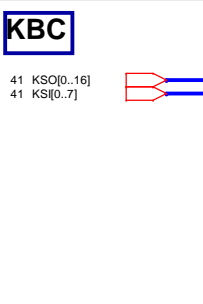
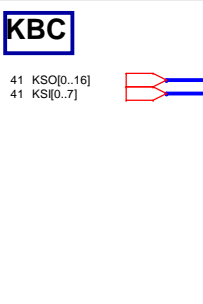
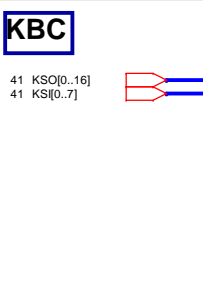
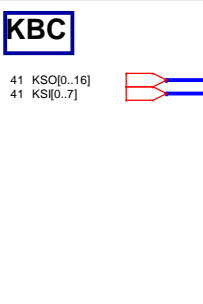
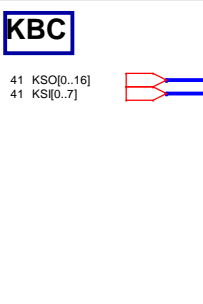
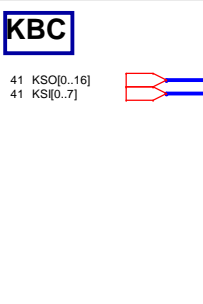
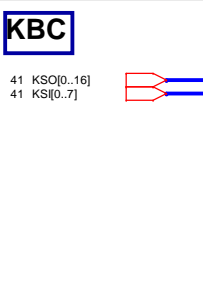
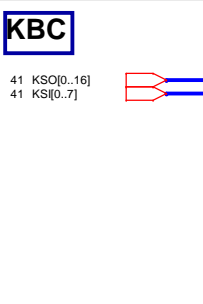
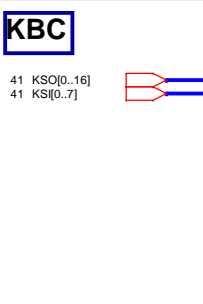
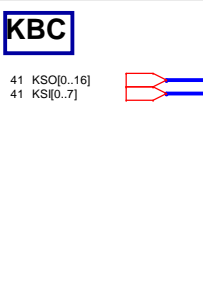
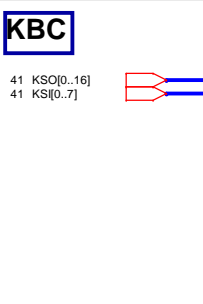
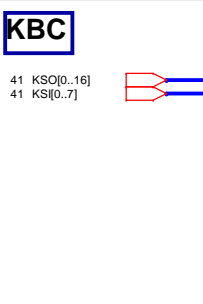
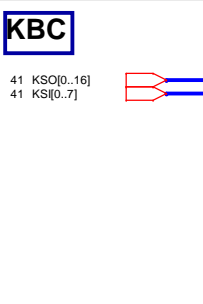
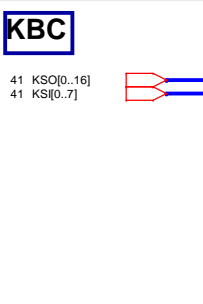
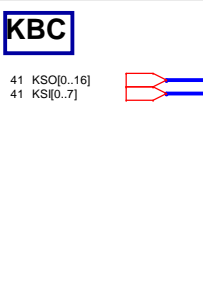
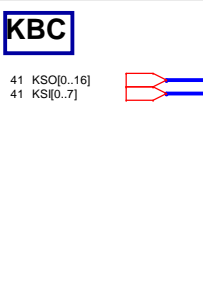
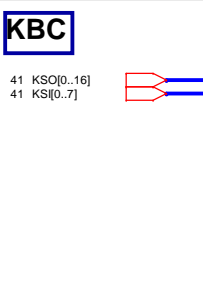
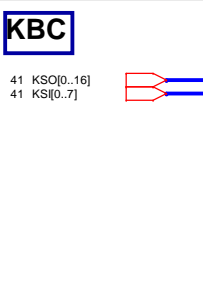
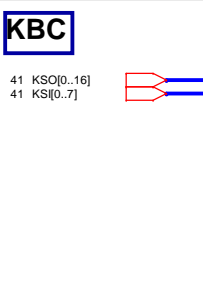
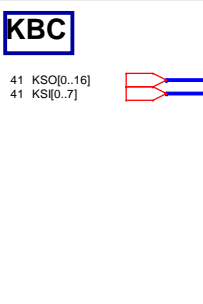
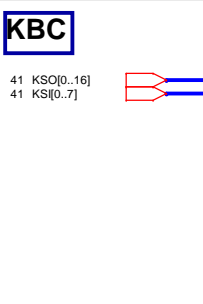
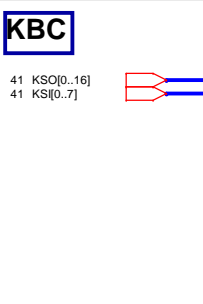
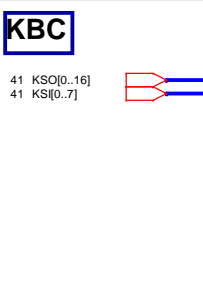
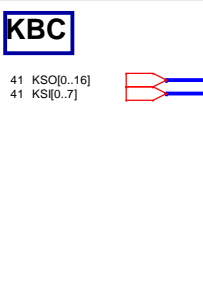
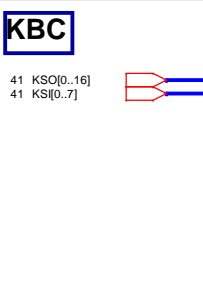
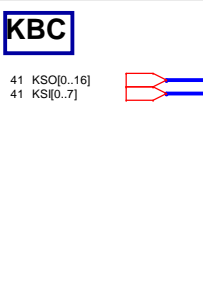
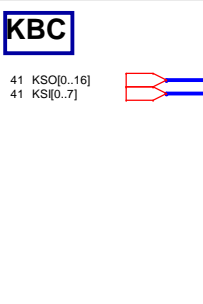
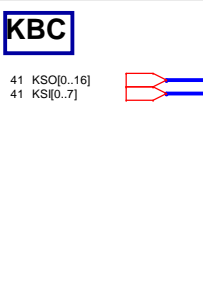
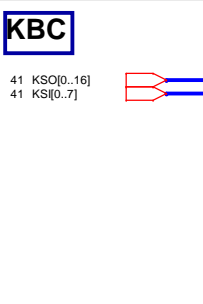
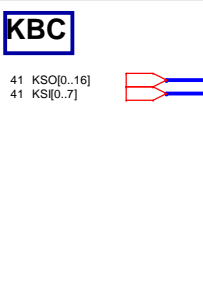
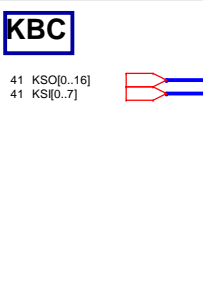
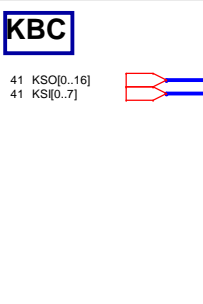
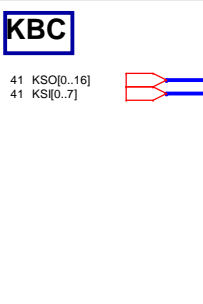
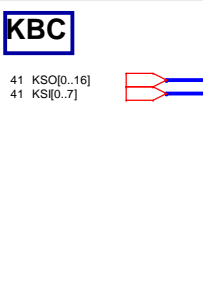
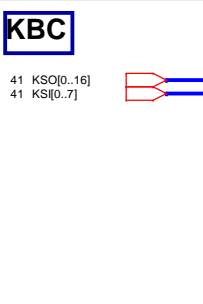
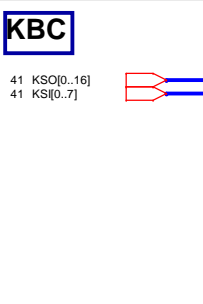
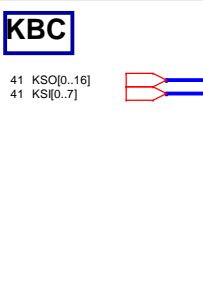
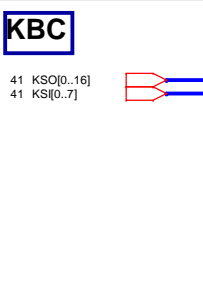
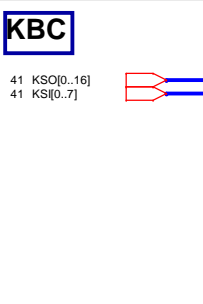
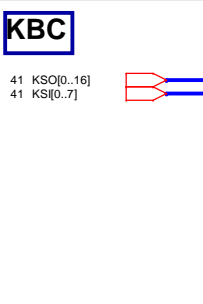
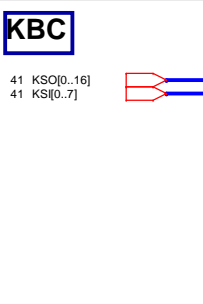
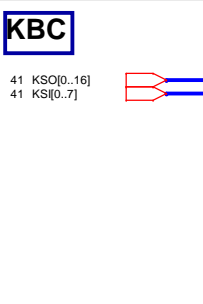
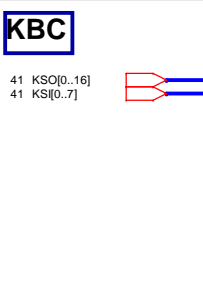
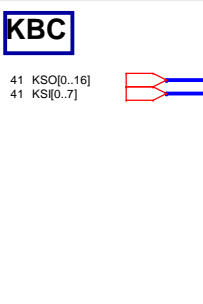
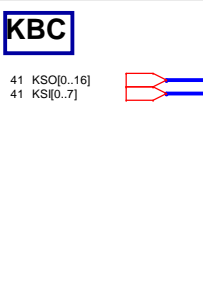
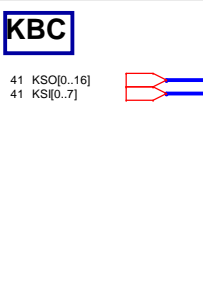
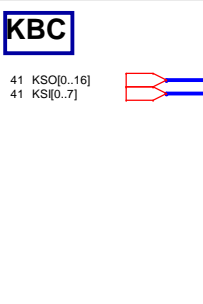
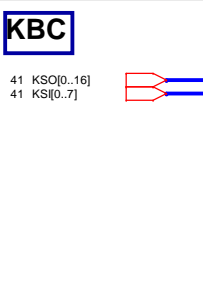
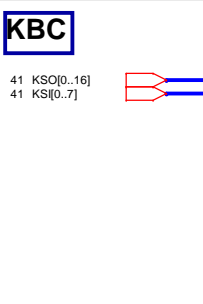
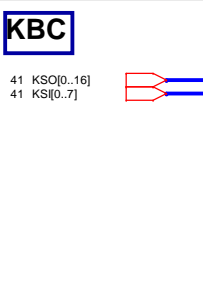
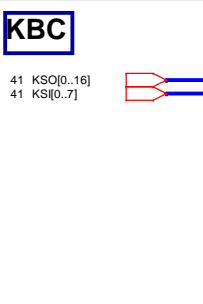
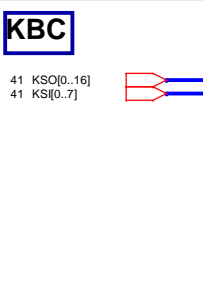
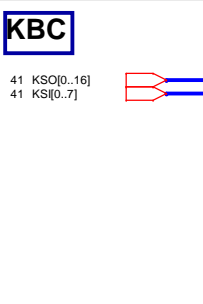
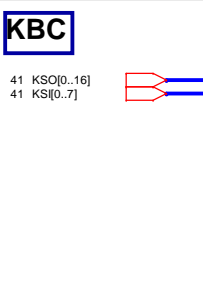
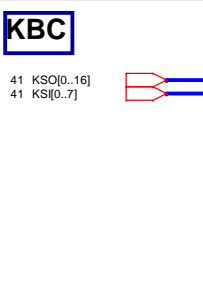
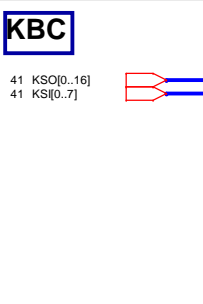
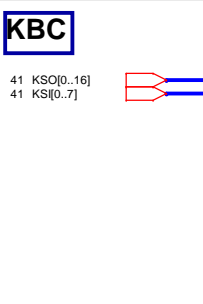
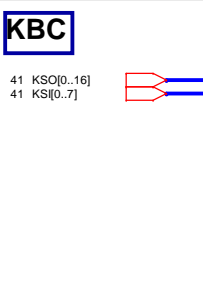
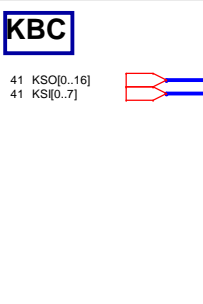
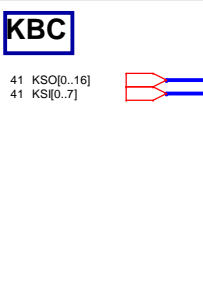
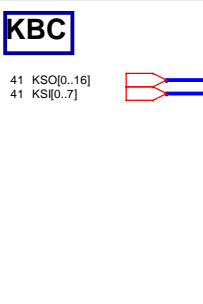
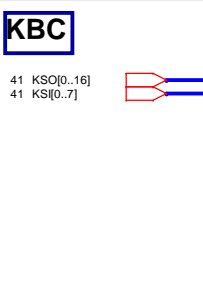
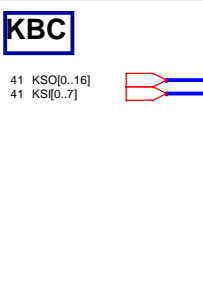
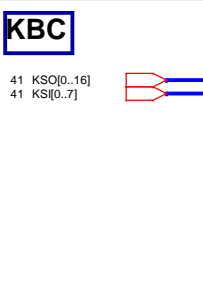
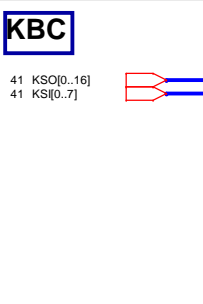
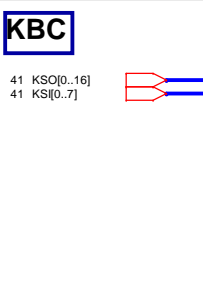
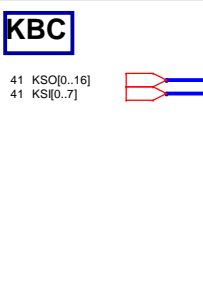
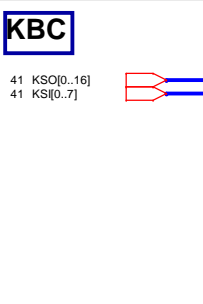
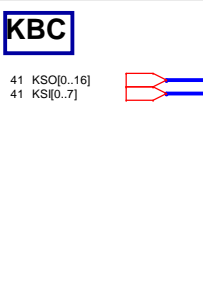
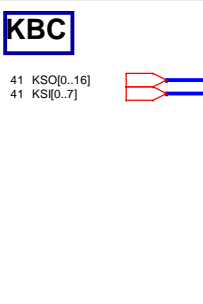
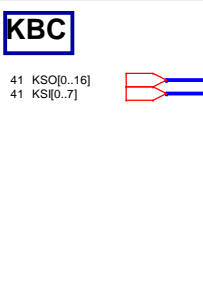
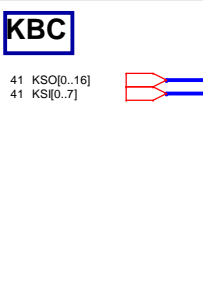
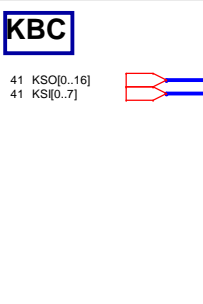
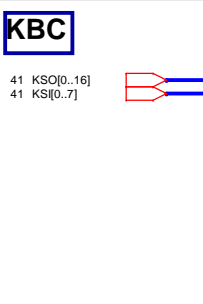
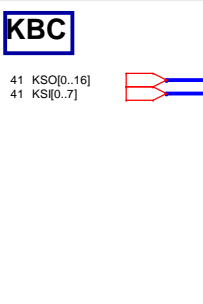
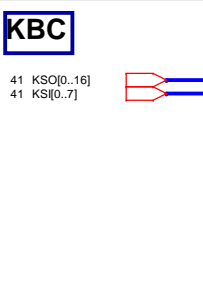
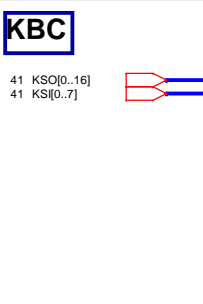
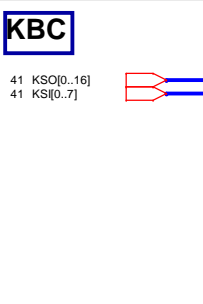
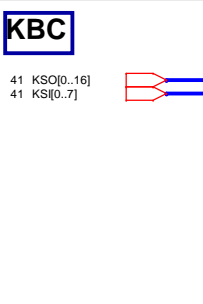
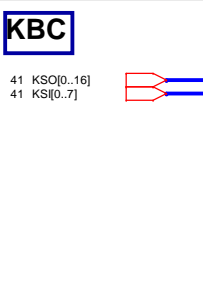
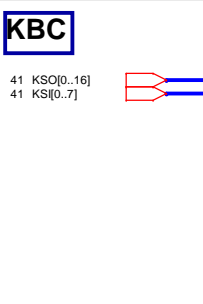
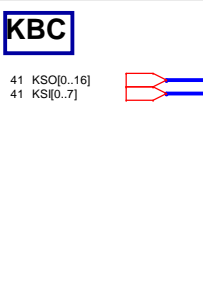
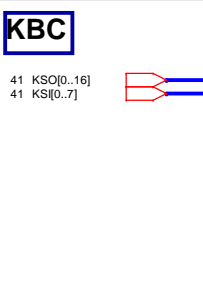
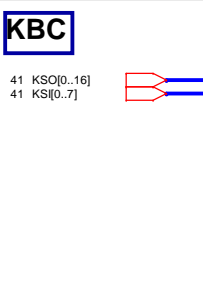
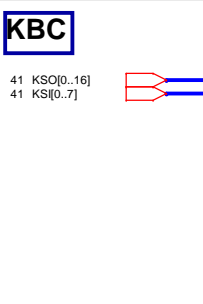
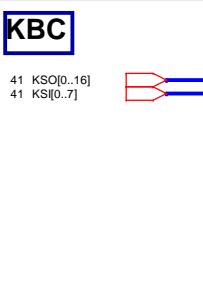
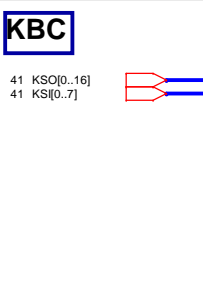
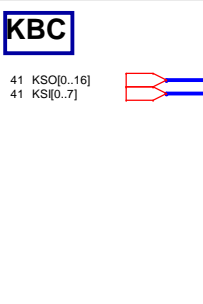
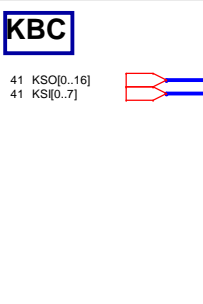
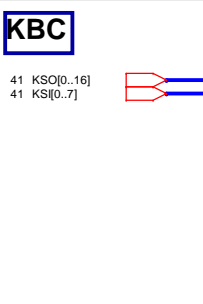
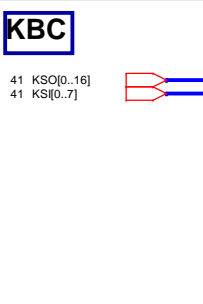
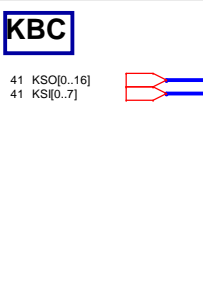
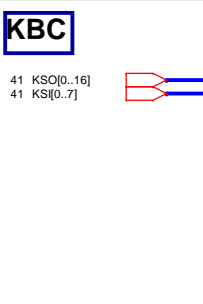
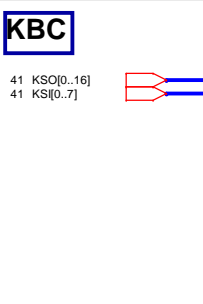
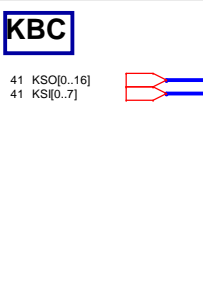
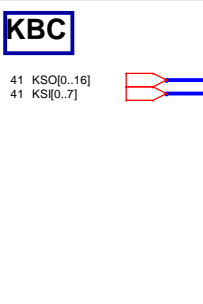
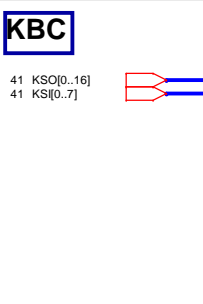
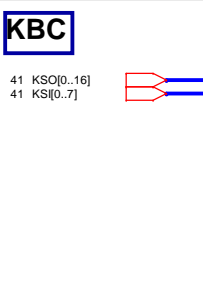
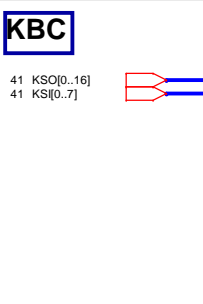
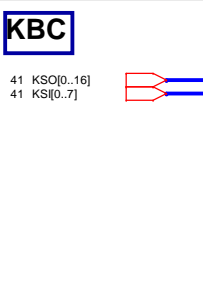
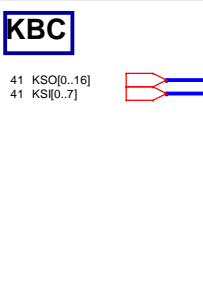
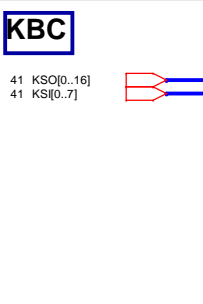
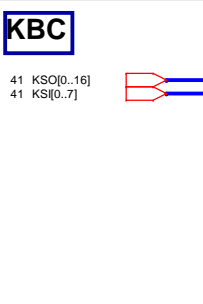
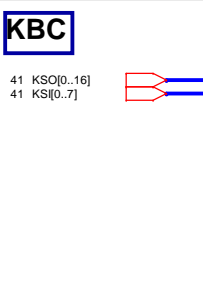
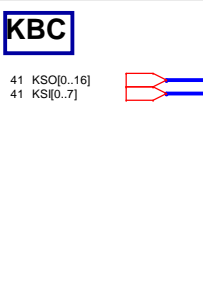
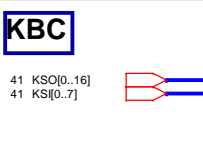
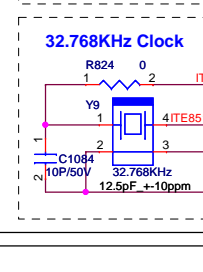
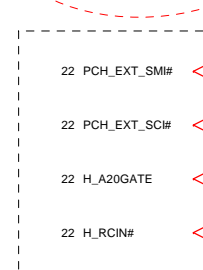
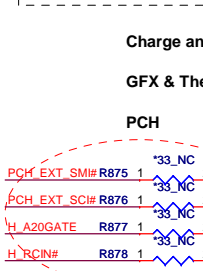
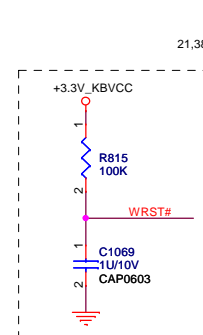
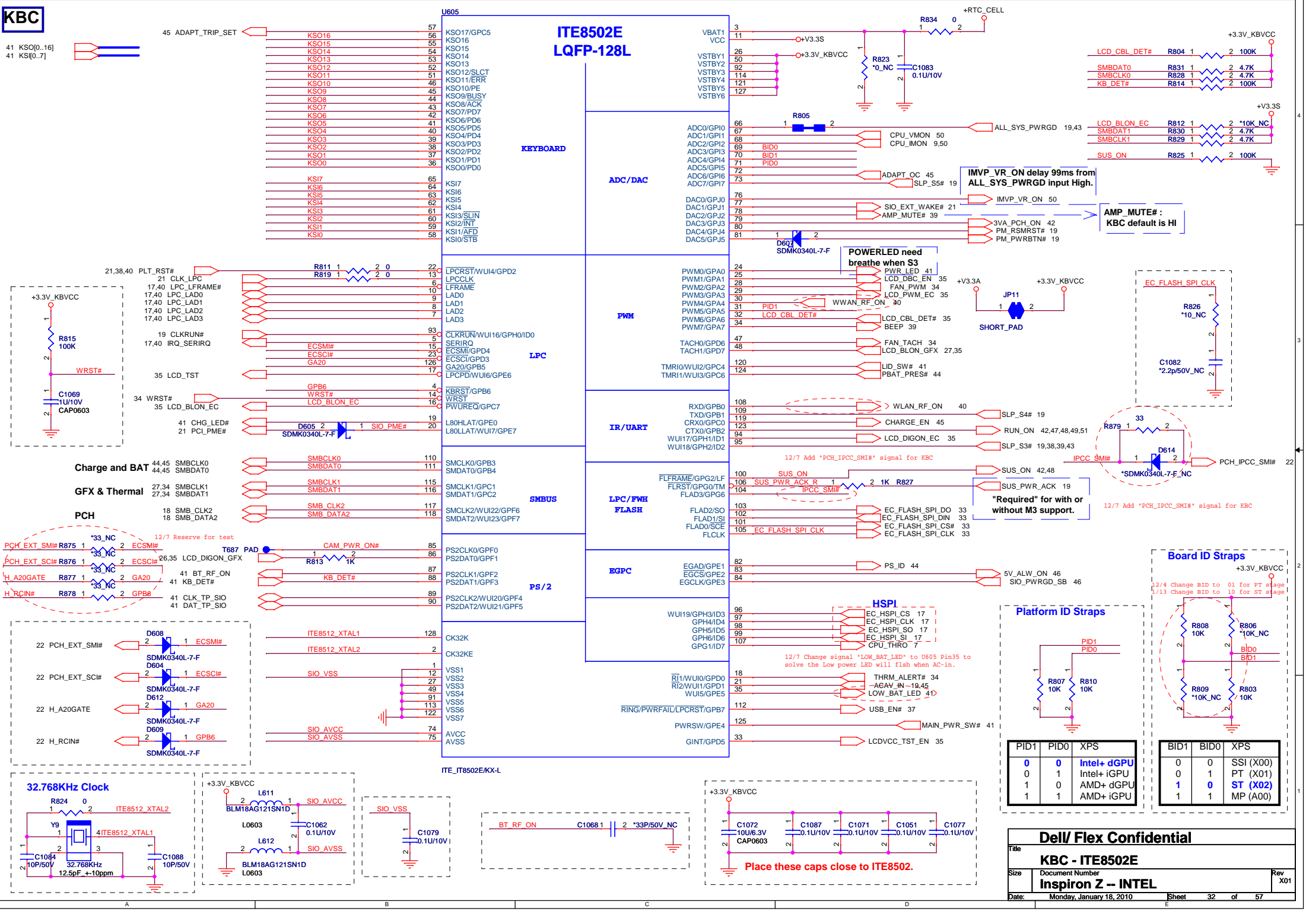
SAMSUNG_K4W2G1648B-HC12

SAMSUNG_K4W2G1648B-HC12

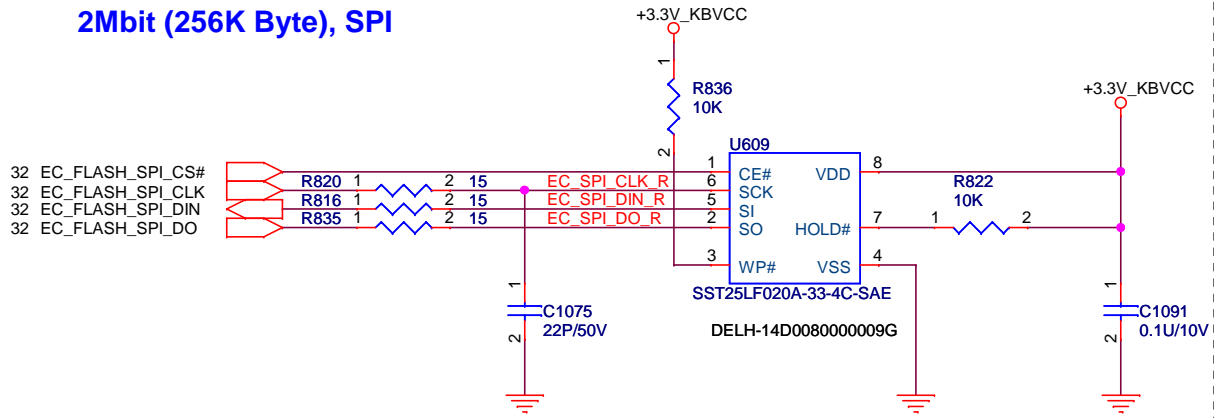
SAMSUNG_K4W2G1648B-HC12

SAMSUNG_K4W2G1648B-HC12





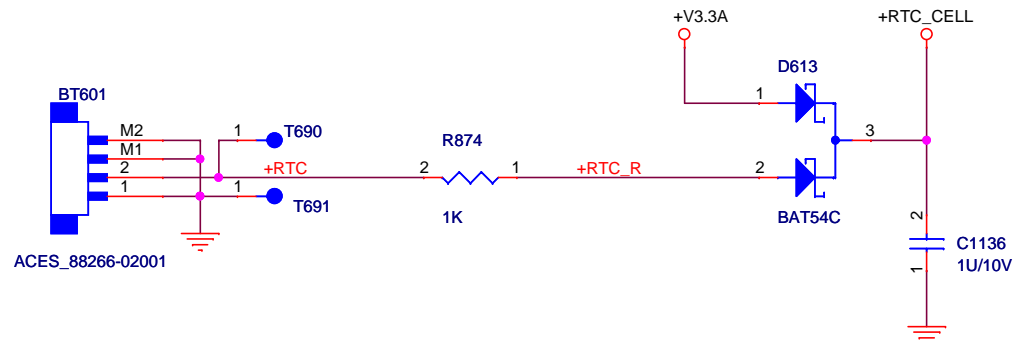
2Mbit (256K Byte), SPI



RFI

EC_FLASH_SPI_CS#	C1092 1	2	*33P/50V_NC
EC_FLASH_SPI_CLK	C1070 1	2	*33P/50V_NC
EC_FLASH_SPI_DO	C1090 1	2	*33P/50V_NC

RTC BATTERY



Dell/ Flex Confidential

Title

RTC BAT/ EC_ROM

Size

Document Number

Inspiron Z -- INTEL

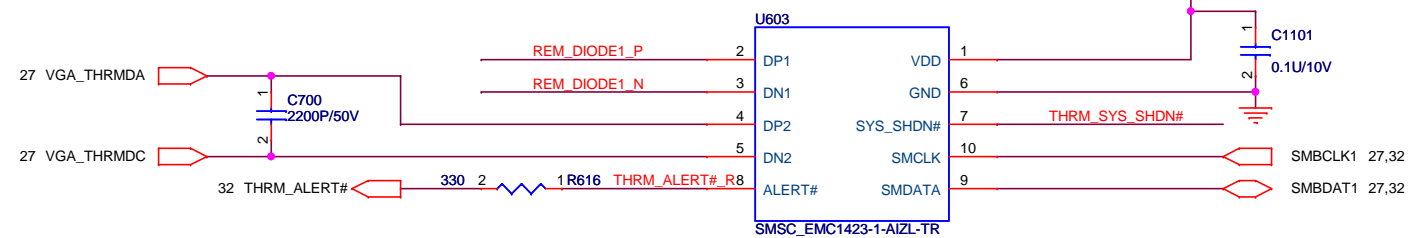
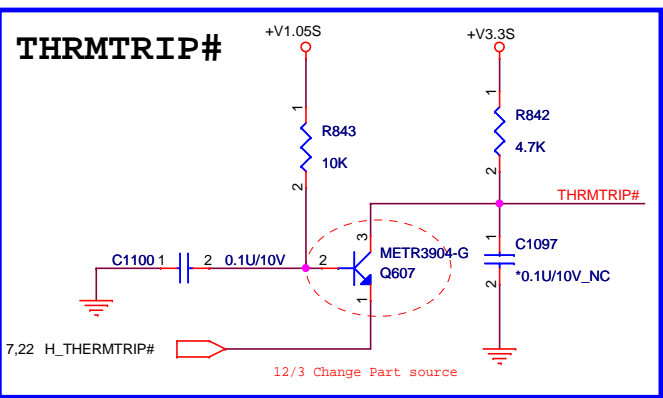
Rev

X01

Date: Monday, January 18, 2010

Sheet 33 of 57

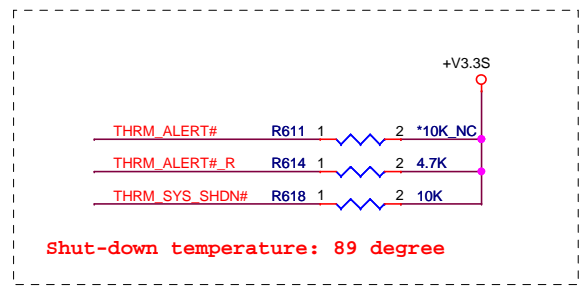
THRMTRIP#



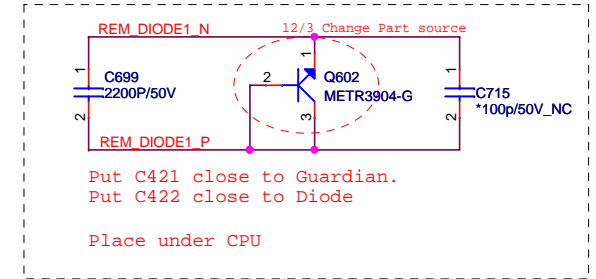
SM bus Address: 100_1100b

Table 5.2 SYS_SHDN Threshold Temperature

ALERT PULL-UP / SYS_SHD PULL-UP	4.7K OHM ±10%	6.8K OHM ±10%	10K OHM ±10%	15K OHM ±10%	22K OHM ±10%	33K OHM ±10%
4.7K OHM ±10%	77°C	83°C	89°C	95°C	101°C	107°C
6.8K OHM ±10%	78°C	84°C	90°C	96°C	102°C	108°C
10K OHM ±10%	79°C	85°C	91°C	97°C	103°C	109°C
15K OHM ±10%	80°C	86°C	92°C	98°C	104°C	110°C
22K OHM ±10%	81°C	87°C	93°C	99°C	105°C	111°C
33K OHM ±10%	82°C	88°C	94°C	100°C	106°C	112°C

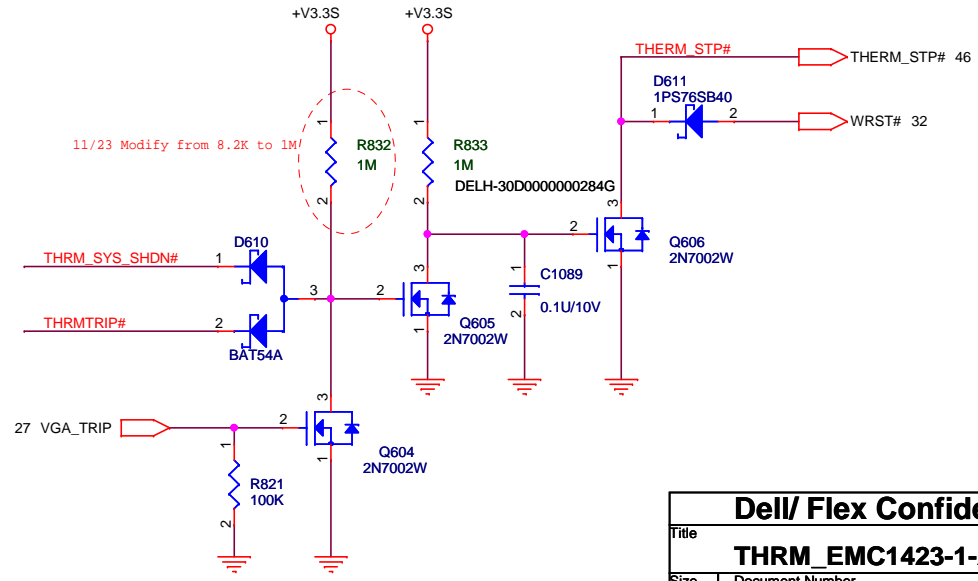
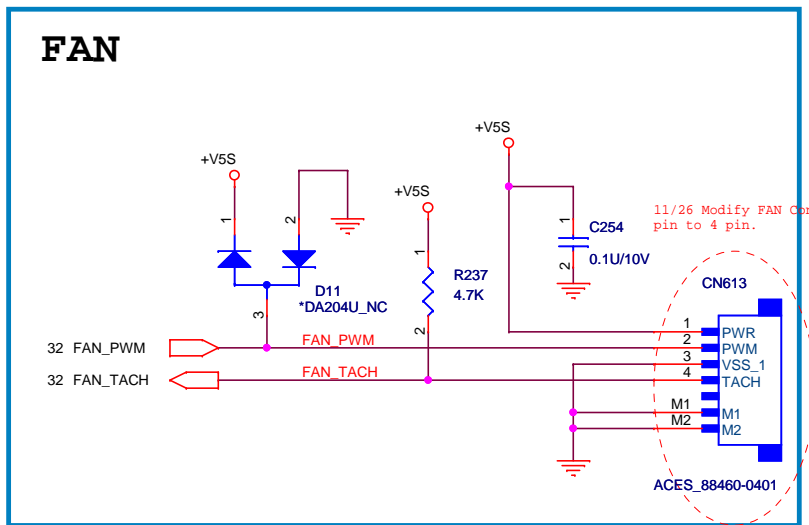


Shut-down temperature: 89 degree

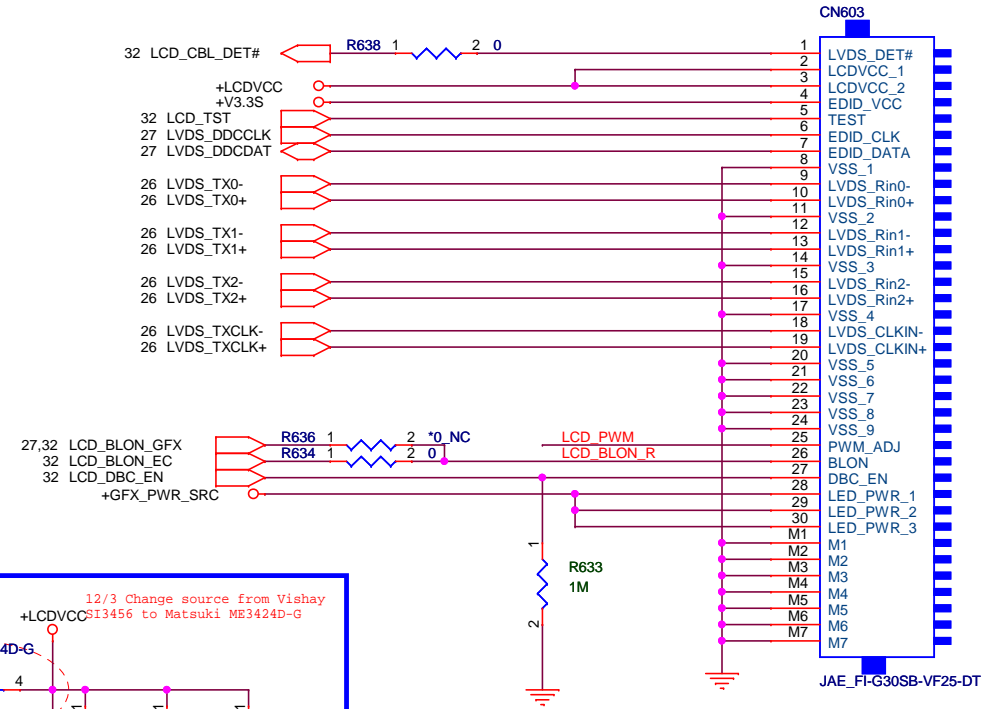
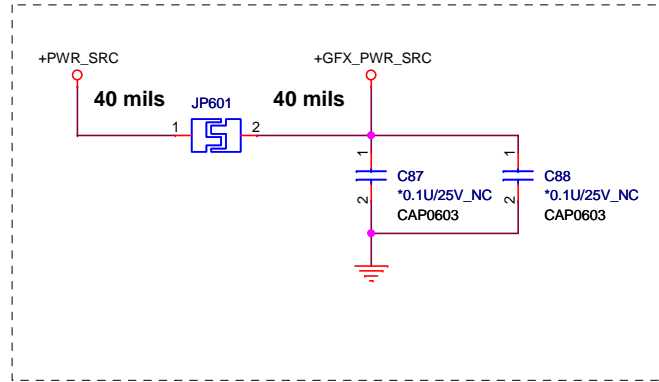


Put C421 close to Guardian.
Put C422 close to Diode
Place under CPU

FAN

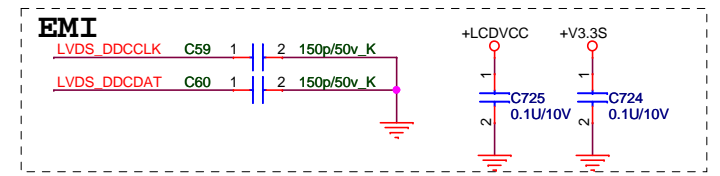
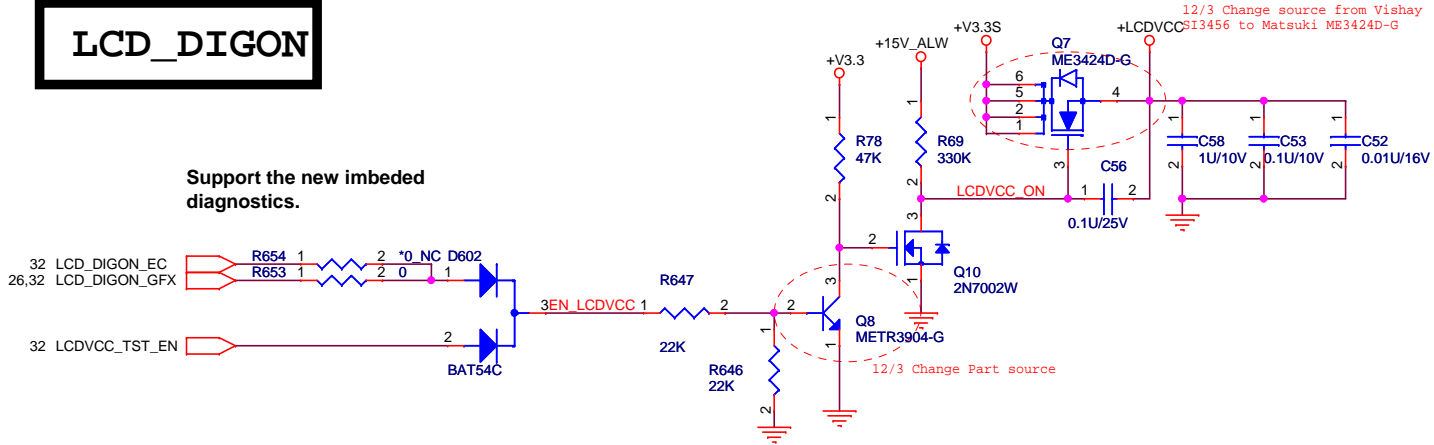


LVDS



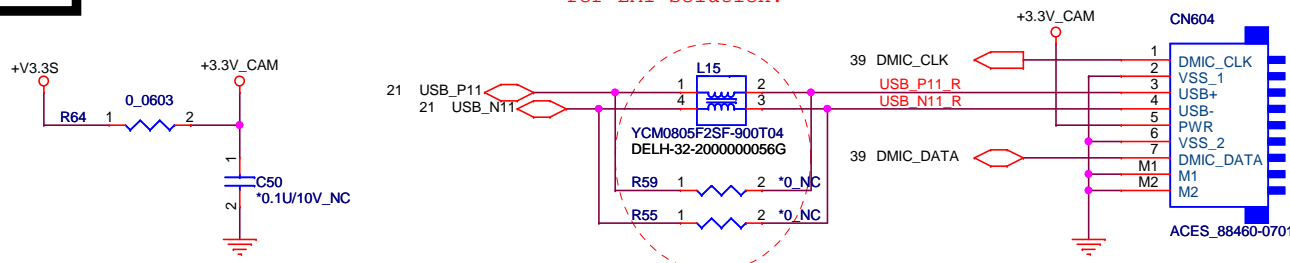
LCD_DIGON

Support the new imbedded diagnostics.



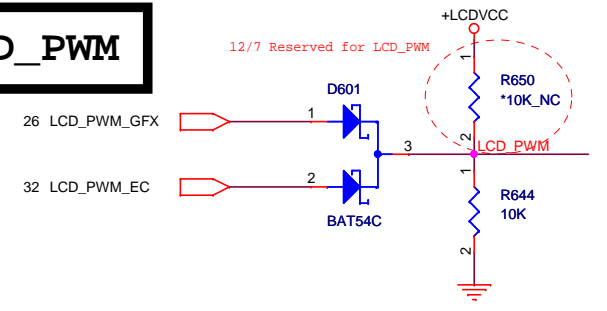
WEBCAM

12/3 Mount L15, & NA R59, R55 for EMI solution.



LCD_PWM

12/7 Reserved for LCD_PWM



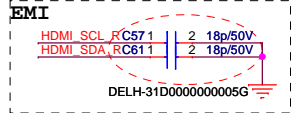
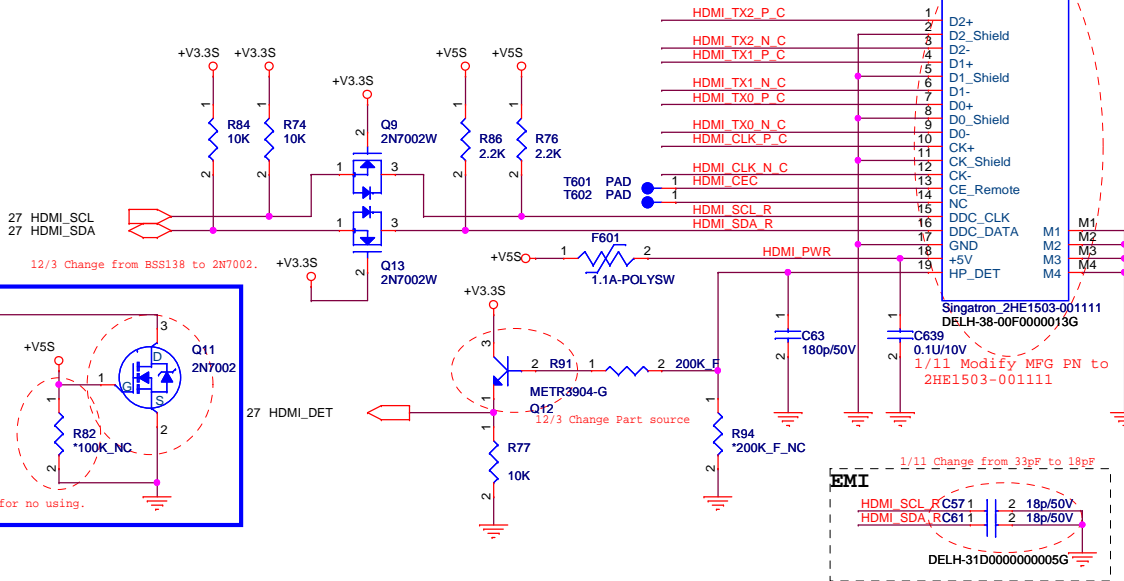
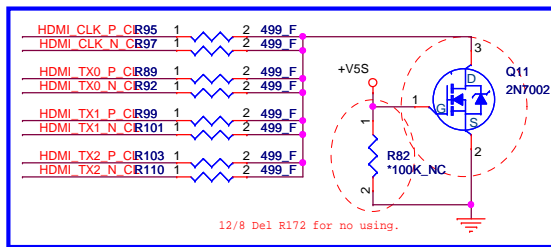
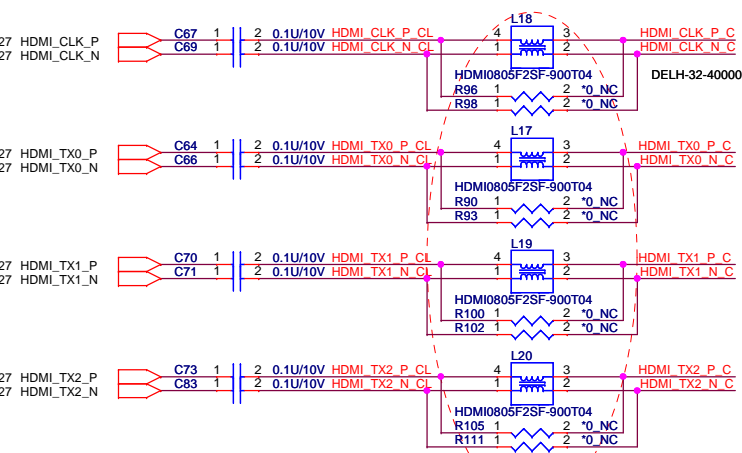
Dell/ Flex Confidential

LVDS / WEBCAM

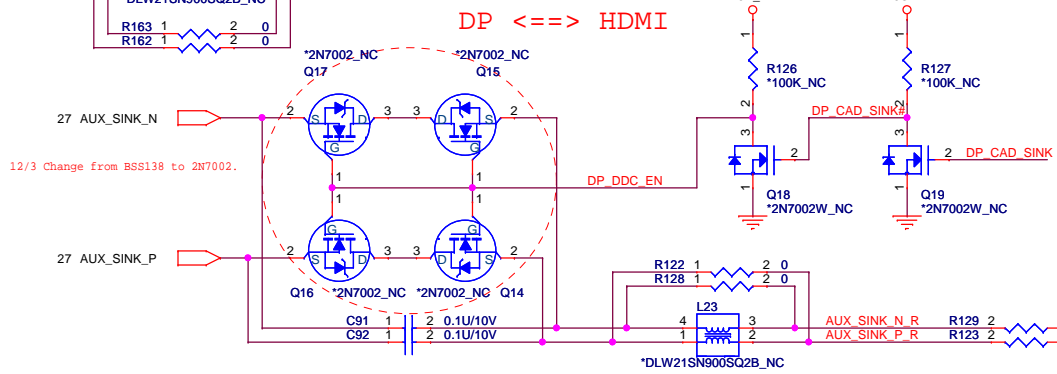
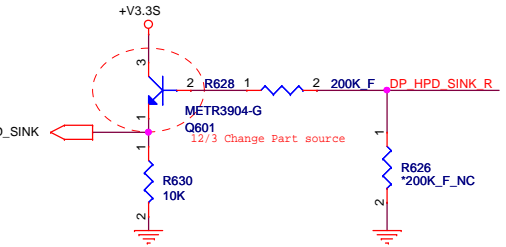
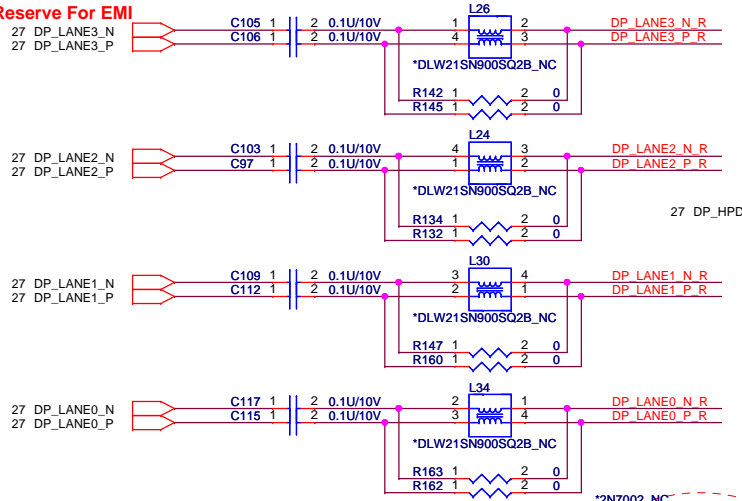
Size	Document Number	Rev
	Inspiron Z -- INTEL	X01
Date:	Monday, January 18, 2010	Sheet 35 of 57

Reserve For EMI

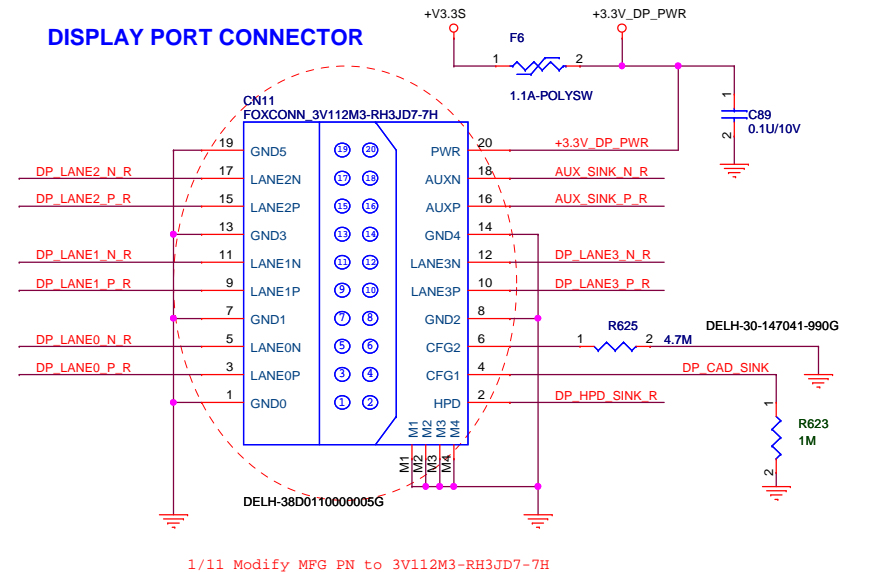
12/3 Mount L17, L18, L19, L20 & NA R90, R93, R96, R98, R100, R102, R105, R111 for EMI solution.



Reserve For EMI

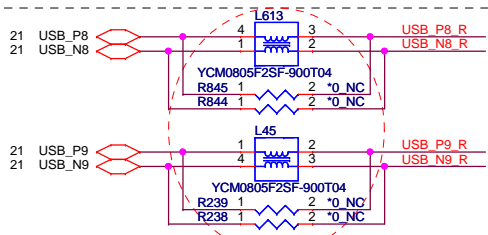


DISPLAY PORT CONNECTOR

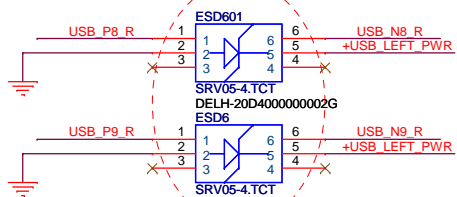


Dell/ Flex Confidential			
Title	HDMI / DP		
Size	Document Number	Inspiron Z -- INTEL	
Date:	Monday, January 18, 2010	Sheet	36 of 57
			Rev X01

USB Jack x 2 12/3 Mount L45, L613, & NA R238, R239, R844, R845 for EMI solution.

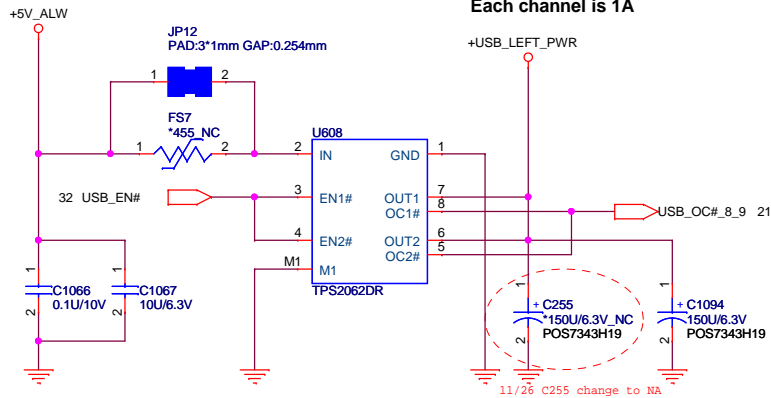


Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.



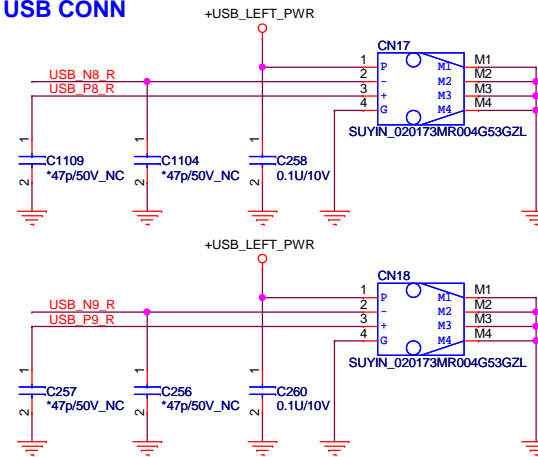
Place ESD diodes as close as USB connector.

USB POWER SW



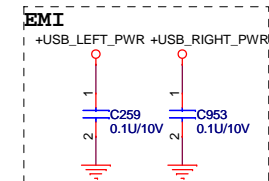
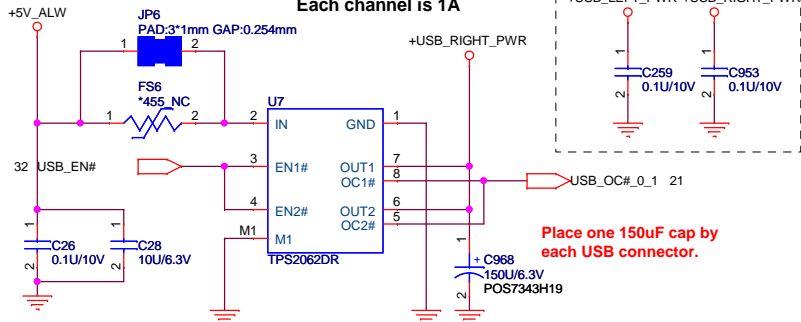
Place one 150uF cap by each USB connector.

USB CONN



USB POWER SW

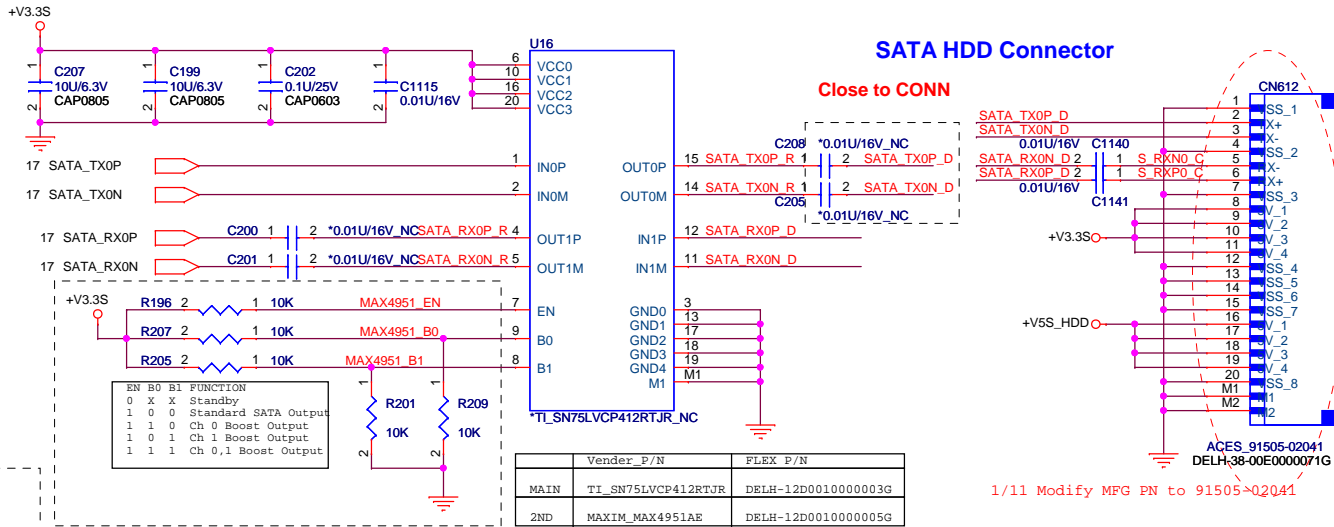
Each channel is 1A



Place one 150uF cap by each USB connector.

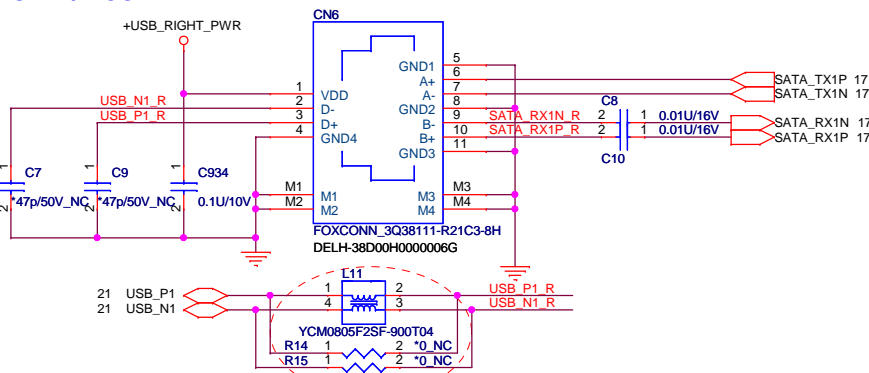
SATA HDD Connector

Close to CONN



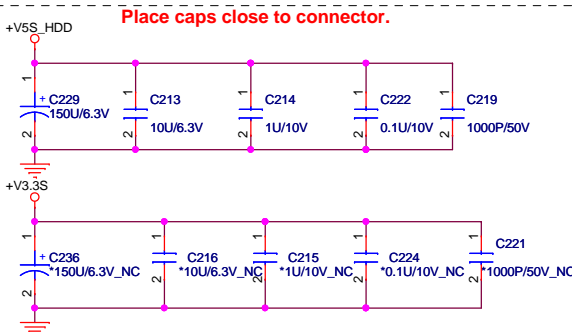
1/11 Modify MFG PN to 91505-02041

ESATA/B CONN

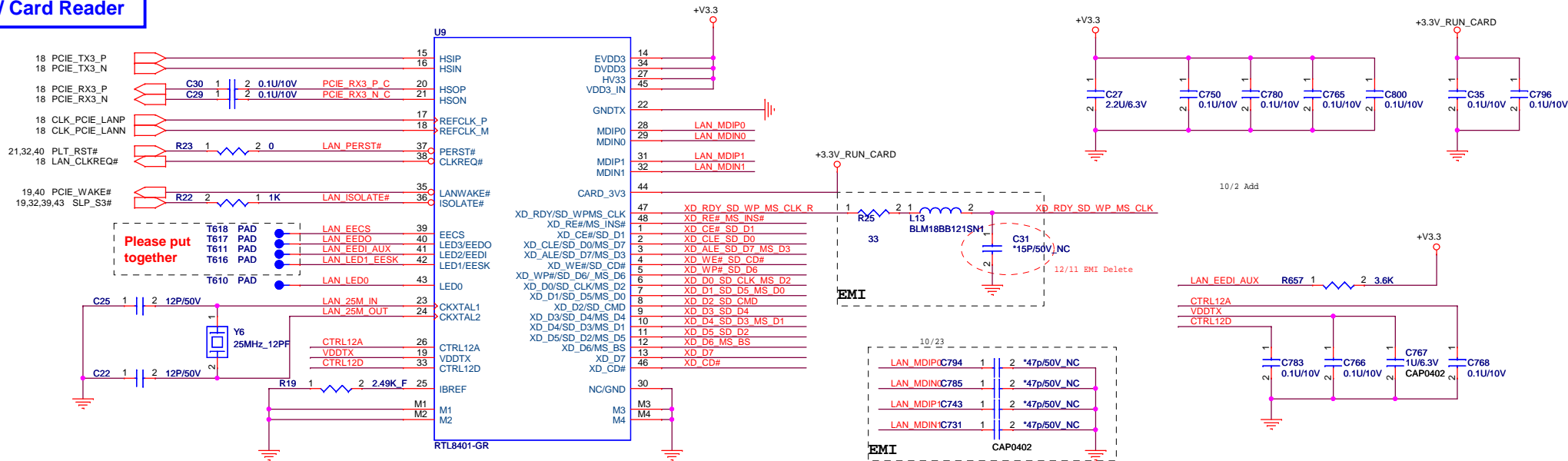


12/3 Mount L11, & NA R14, R15 for EMI solution.

Place caps close to connector.

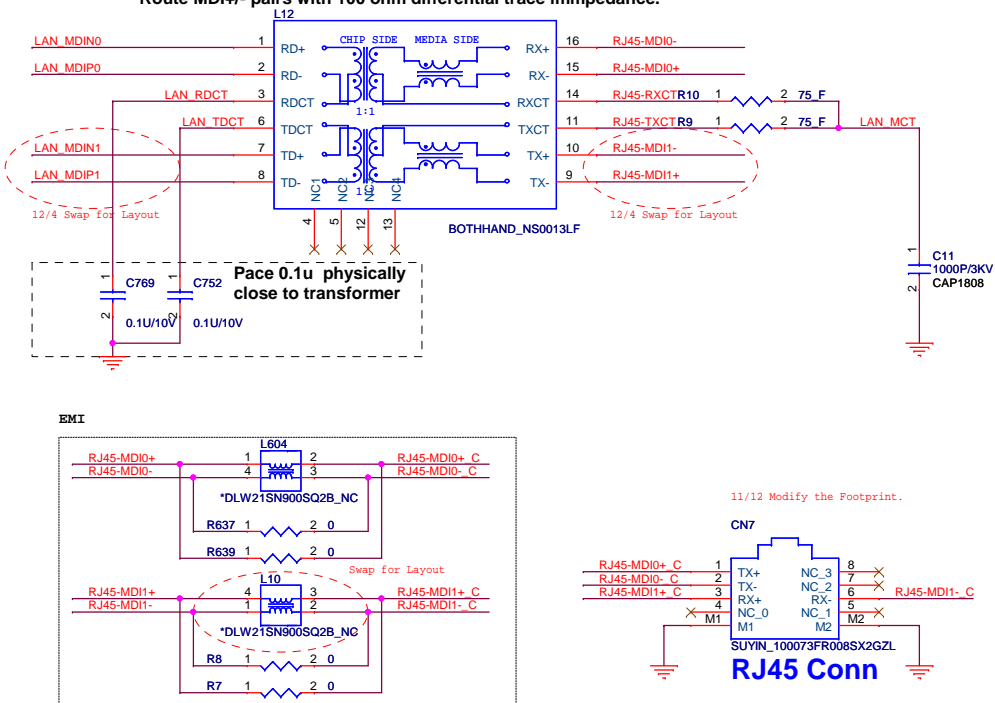


LAN/ Card Reader



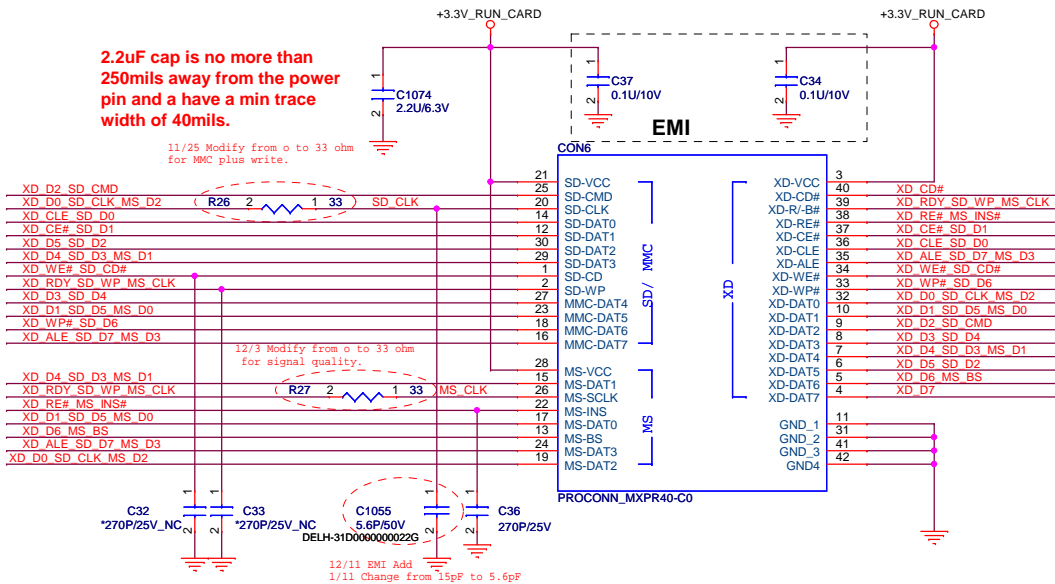
TRANSFORMER

Layout Note:
Route LAN MDI+/- pairs with 100 ohm differential trace impedance.

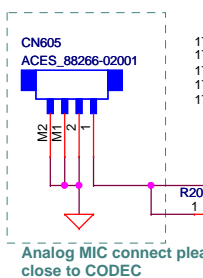
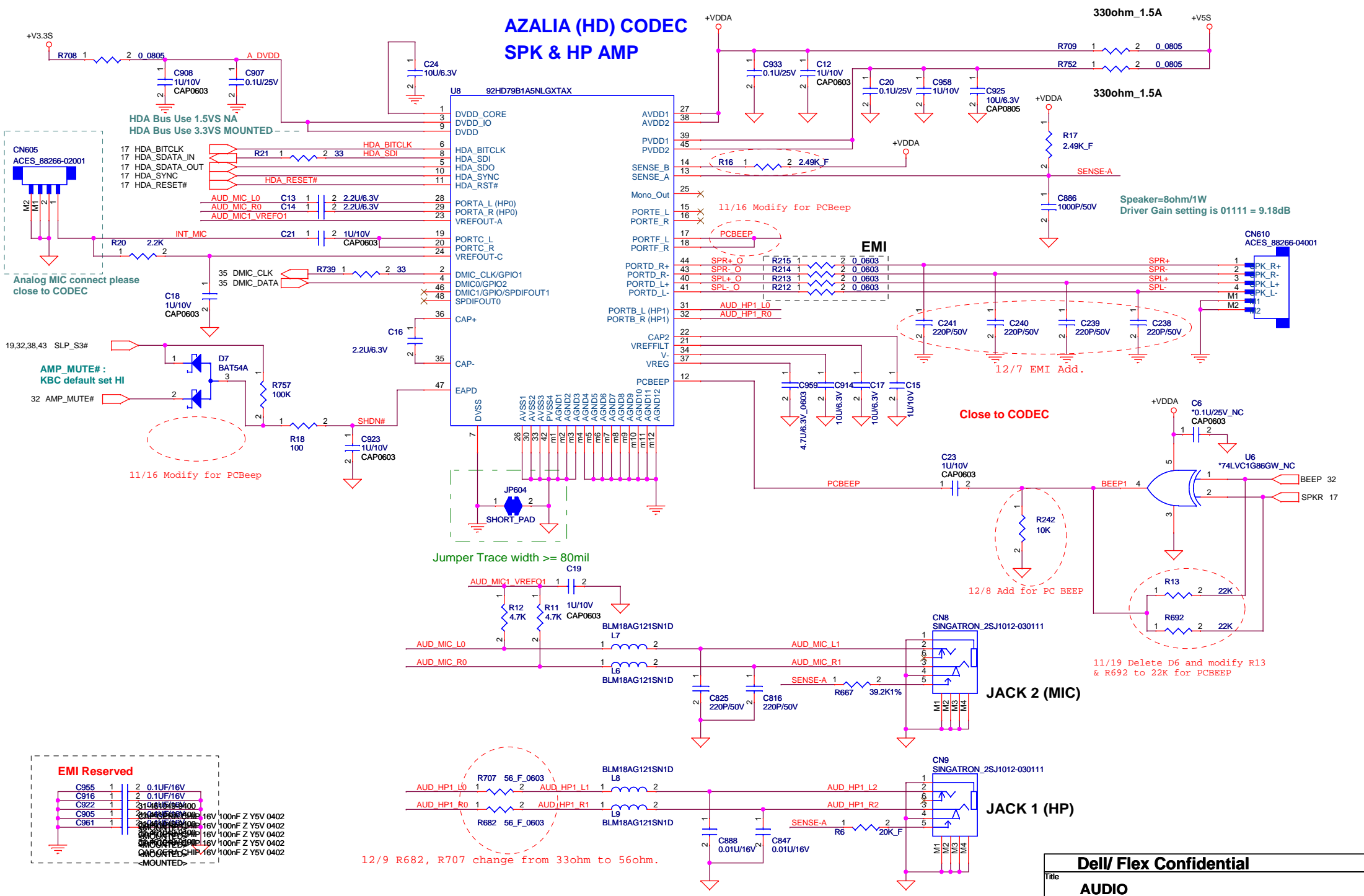


Card Reader Conn

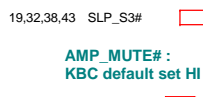
2.2uF cap is no more than 20mils away from the power pin and have a min trace width of 40mils.



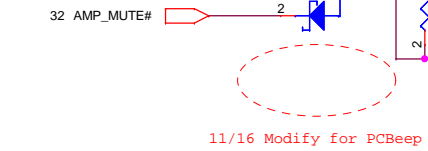
AZALIA (HD) CODEC SPK & HP AMP



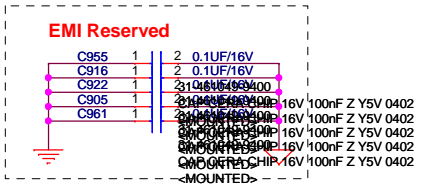
Analog MIC connect please close to CODEC



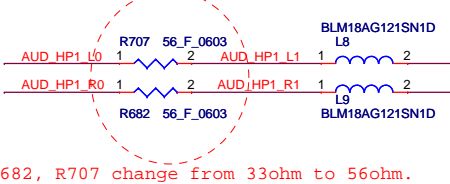
AMP_MUTE# : KBC default set HI



11/16 Modify for PCBEEP



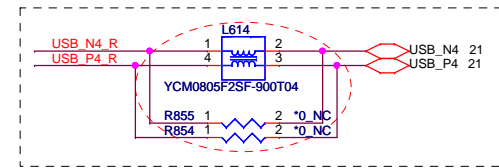
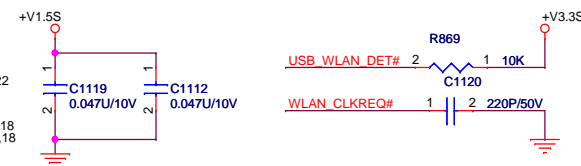
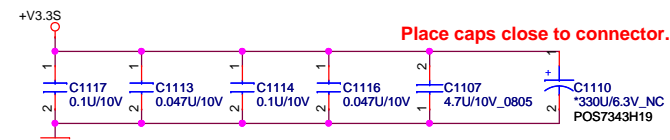
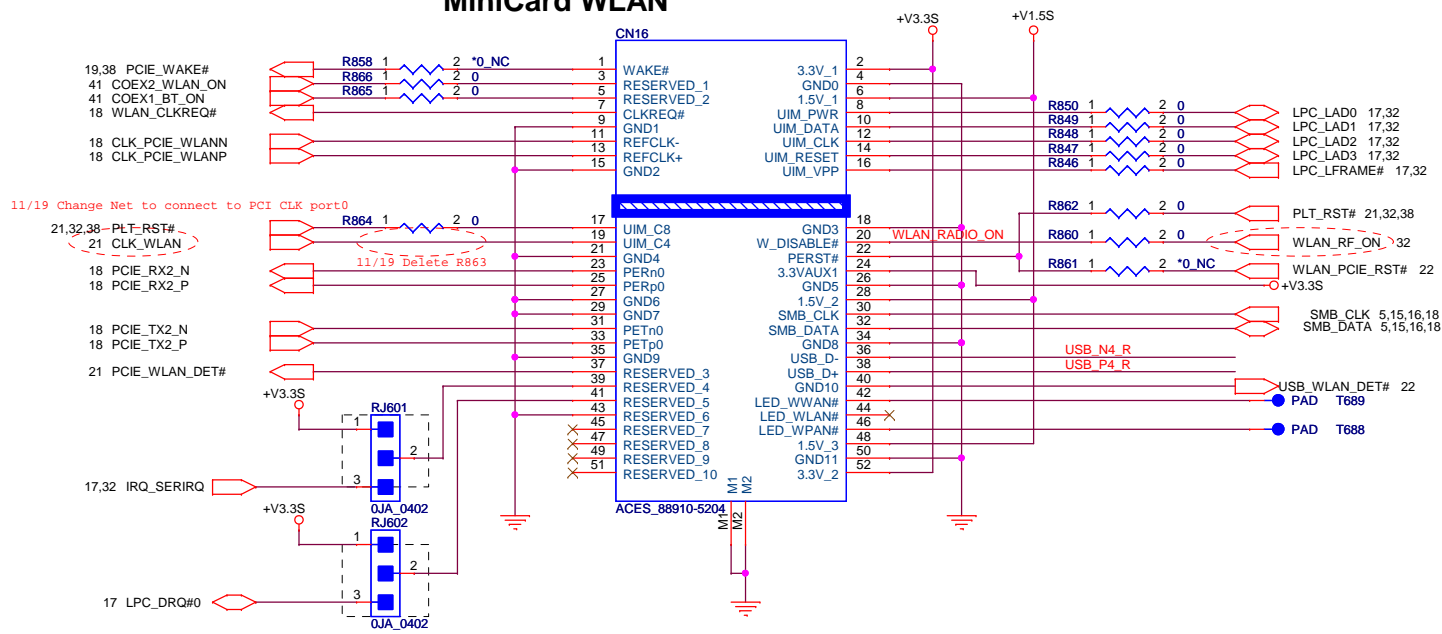
EMI Reserved



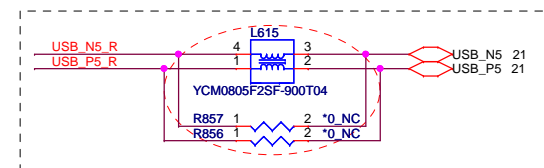
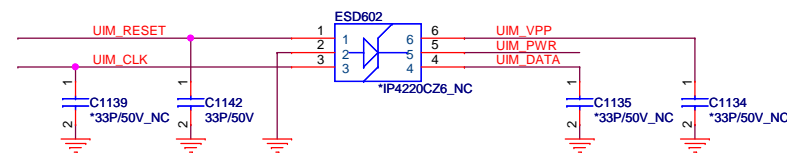
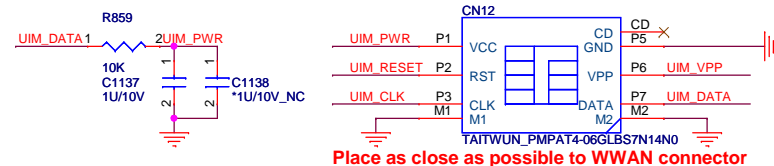
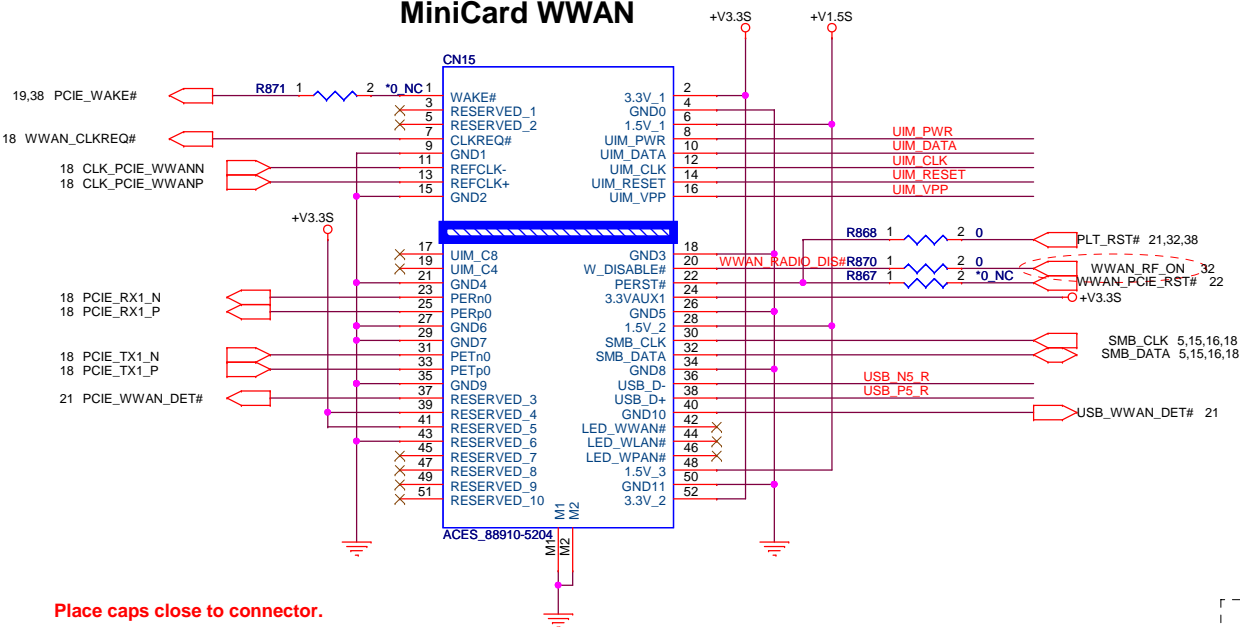
12/9 R682, R707 change from 330ohm to 56ohm.

Deliflex Confidential		
Title		
AUDIO		
Size	Document Number	Rev
	Inspiron Z – INTEL	X01
Date:	Monday, January 18, 2010	Sheet 39 of 57

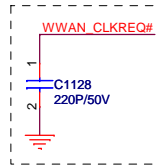
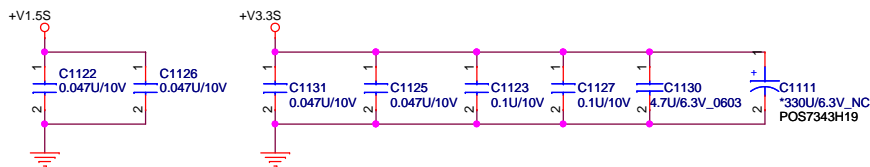
MiniCard WLAN 0929 update footprint



MiniCard WWAN

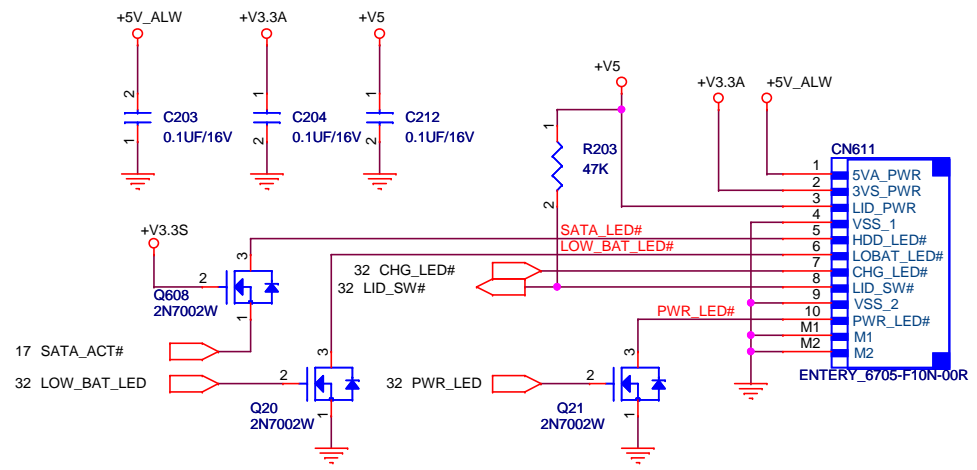
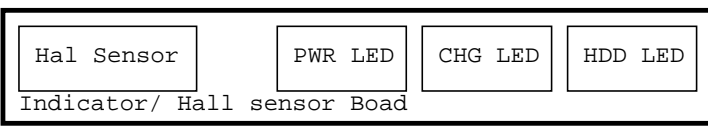


Place caps close to connector.

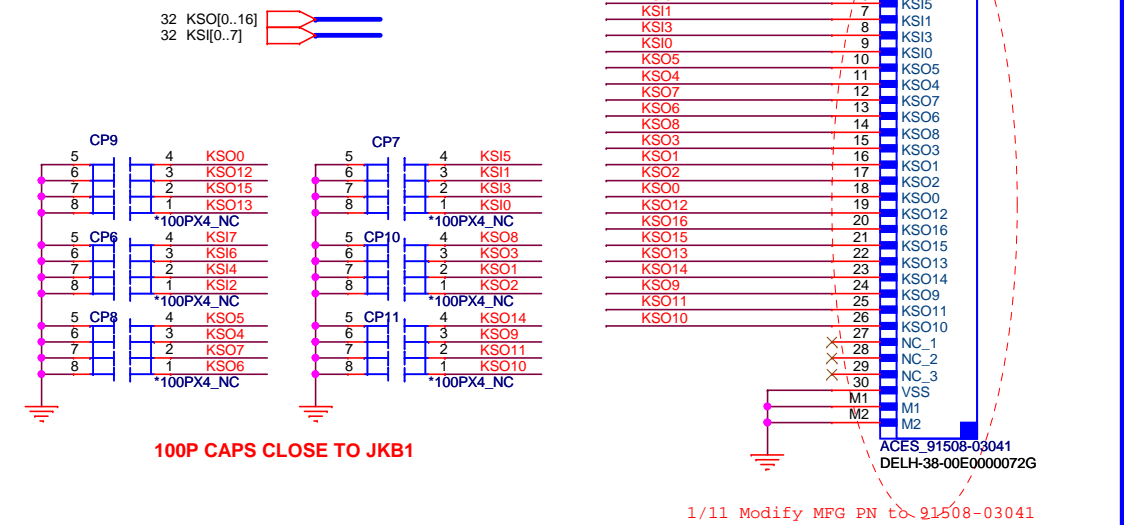


Dell/ Flex Confidential			
WLAN / WWAN			
Size	Document Number	Rev X01	
Inspiron Z -- INTEL		Date:	Monday, January 18, 2010
Sheet	40	of	57

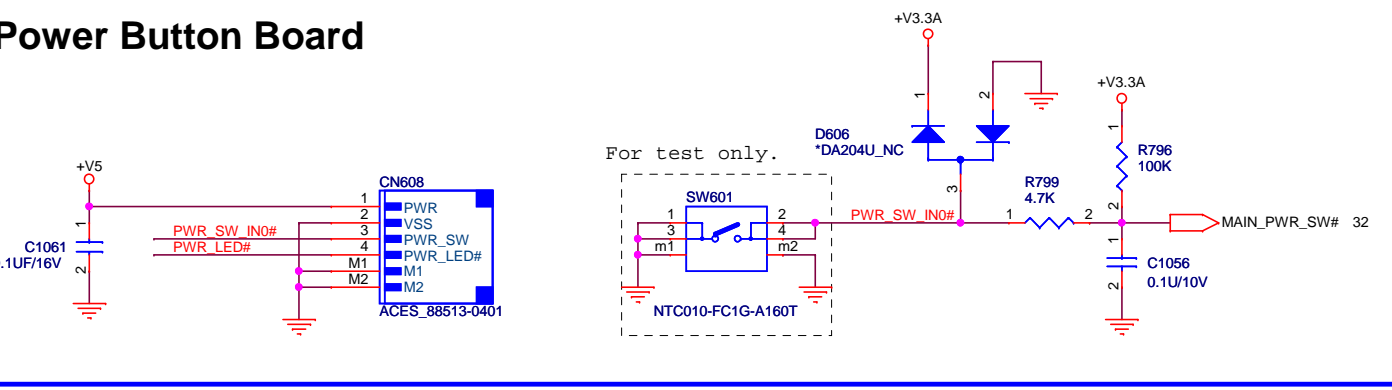
Indicator Board



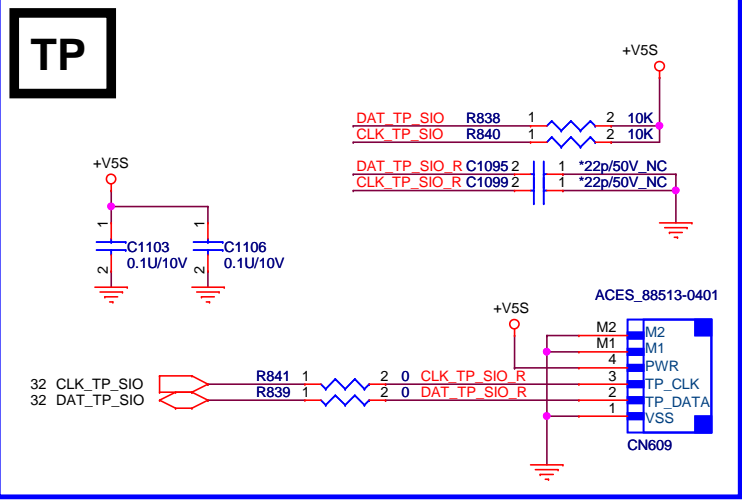
KB



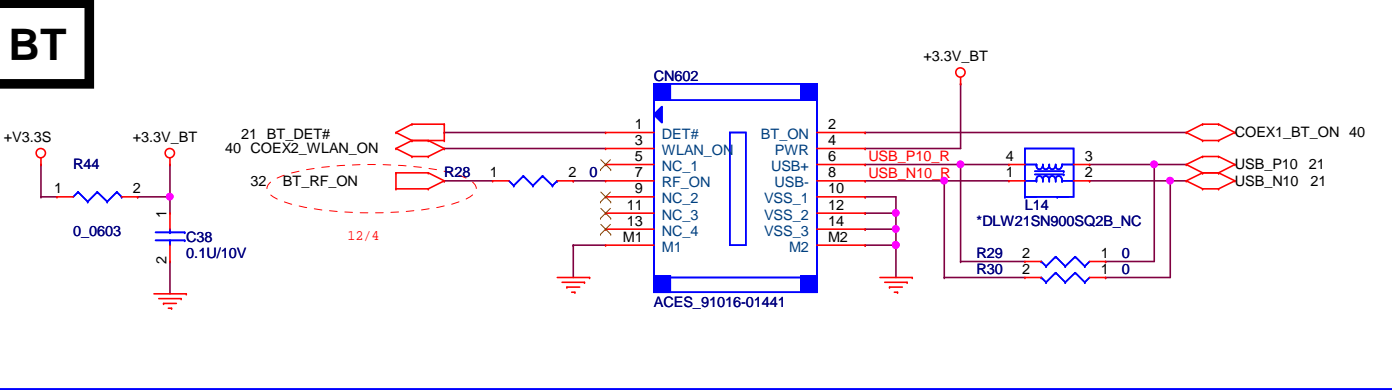
Power Button Board



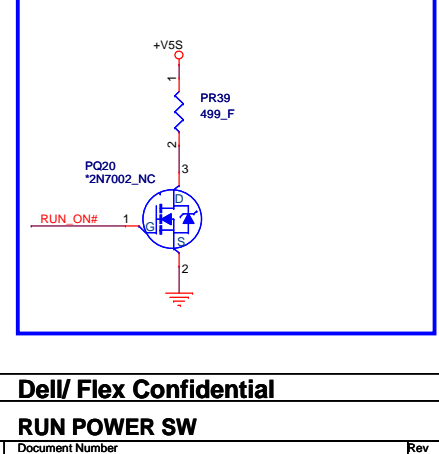
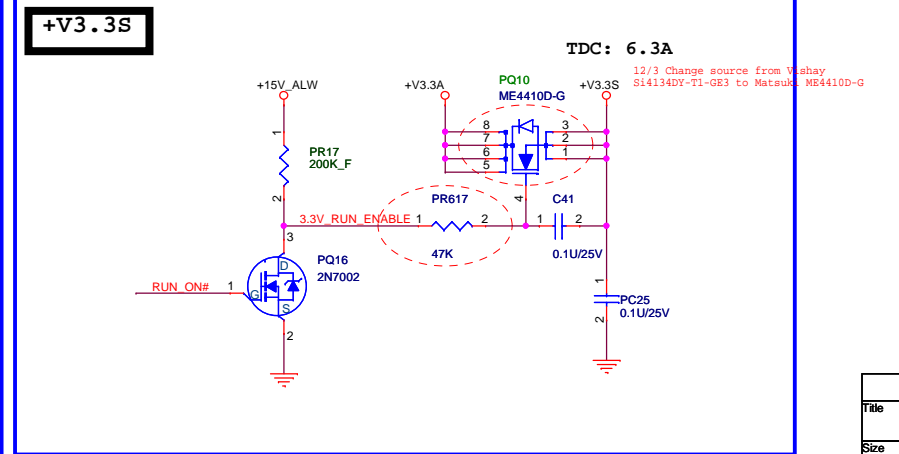
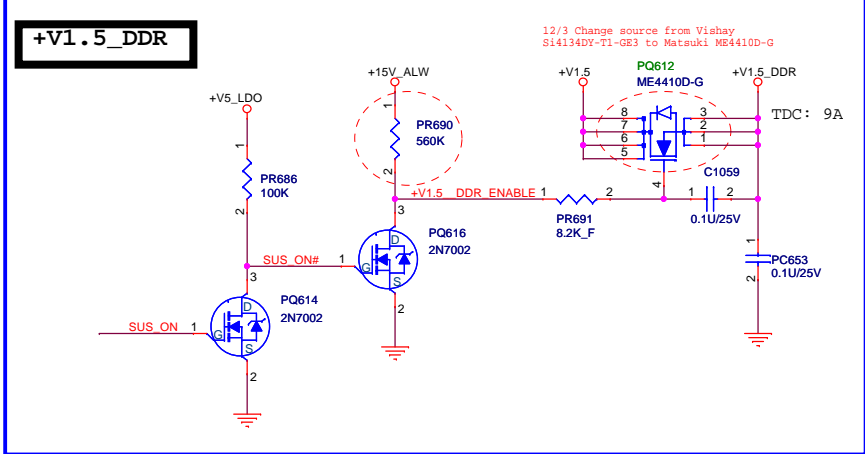
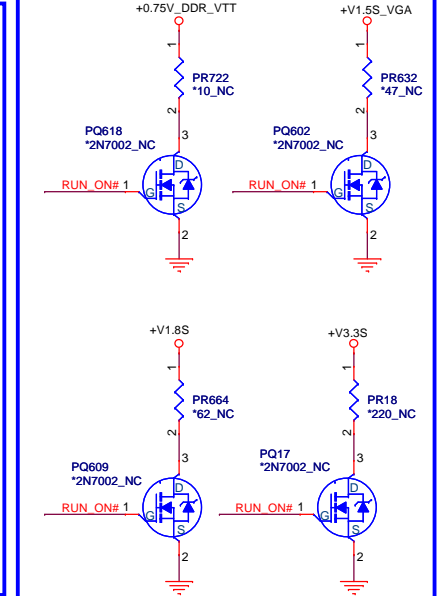
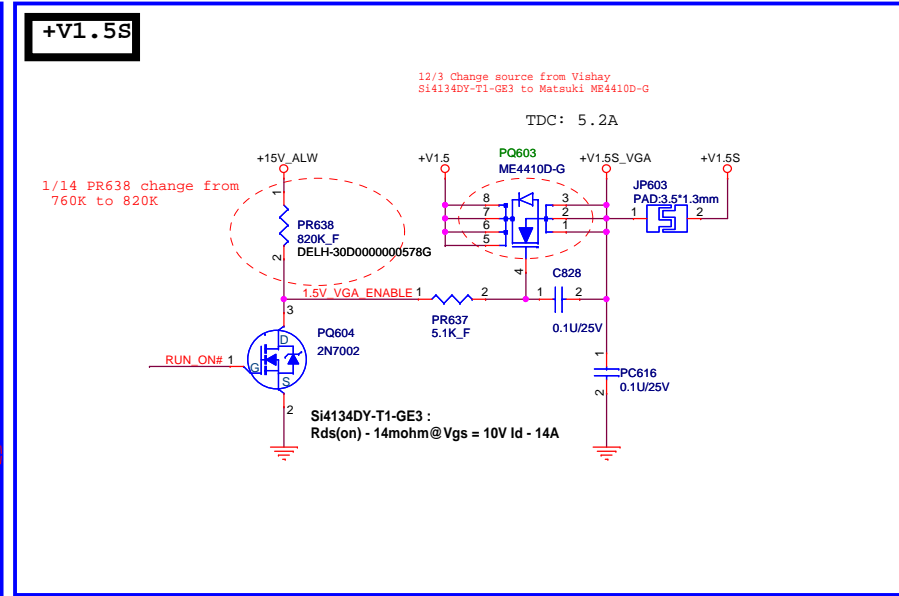
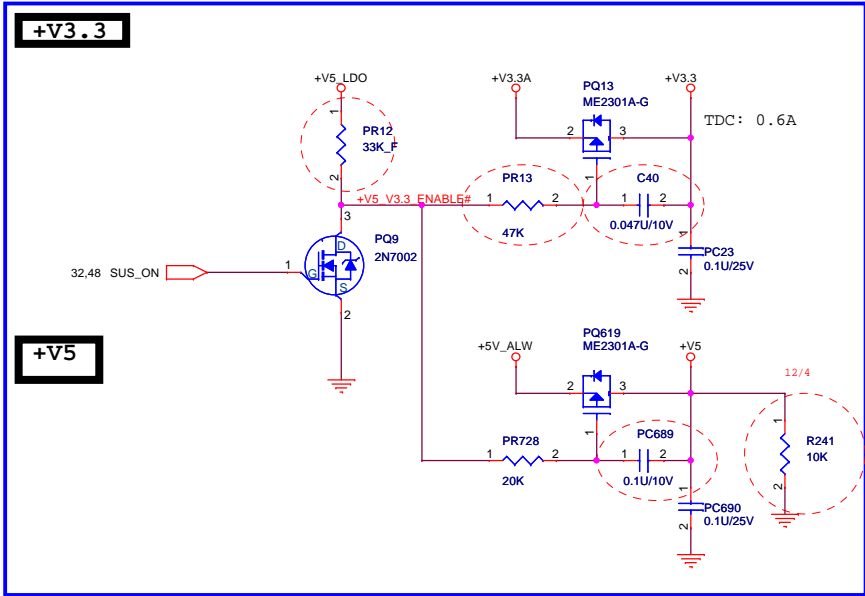
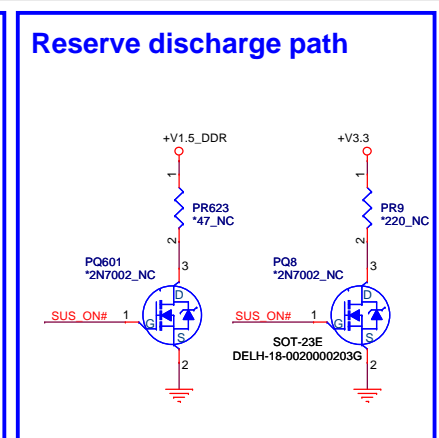
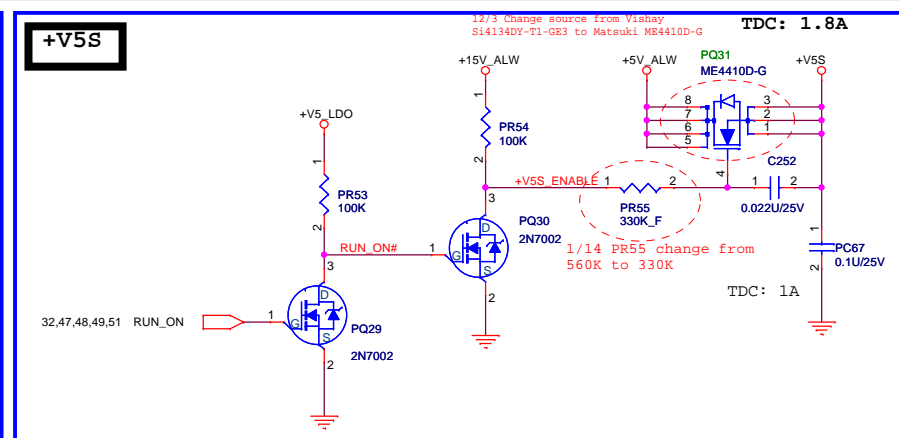
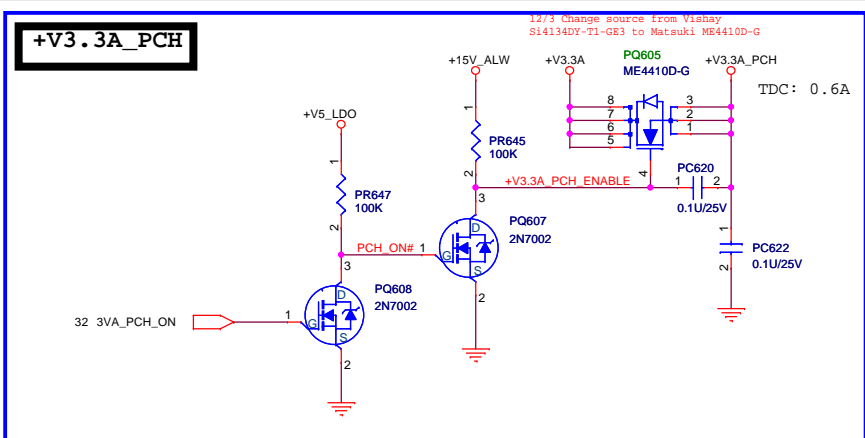
TP

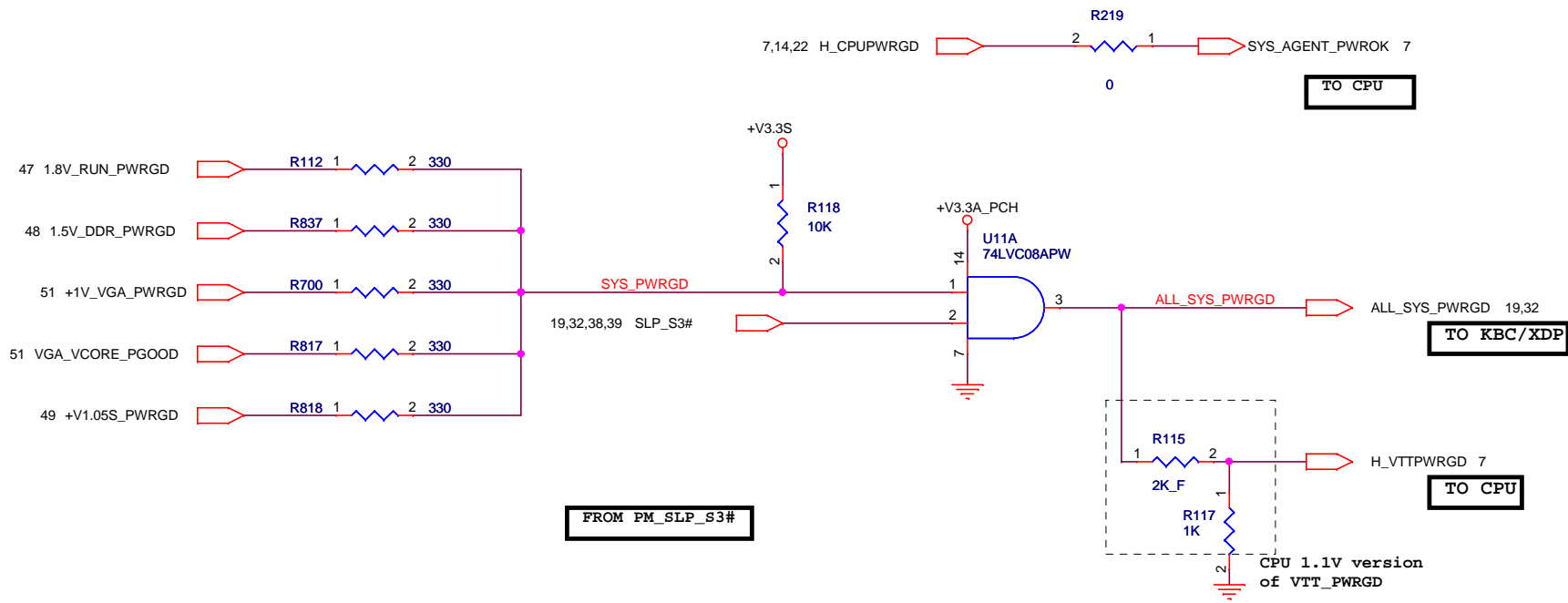


BT



Dell/ Flex Confidential		
Title BT / KB / TP / LED / SW		
Size	Document Number Inspiron Z -- INTEL	Rev X01
Date:	Monday, January 18, 2010	Sheet 41 of 57



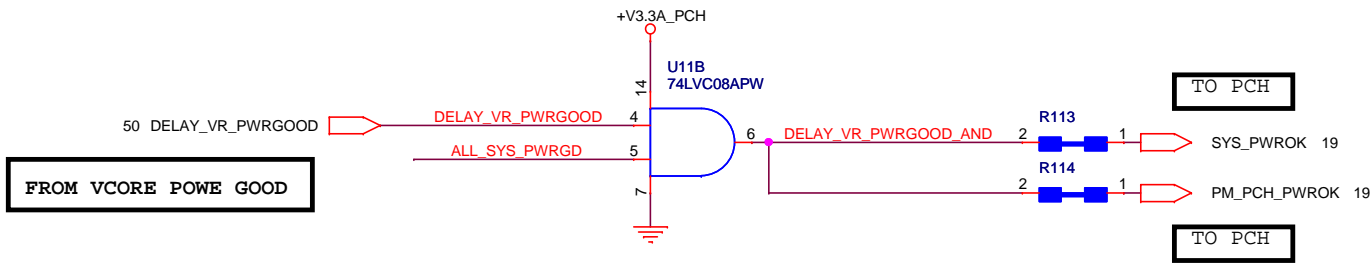


FROM PM_SLP_S3#

TO CPU

TO KBC/XDP

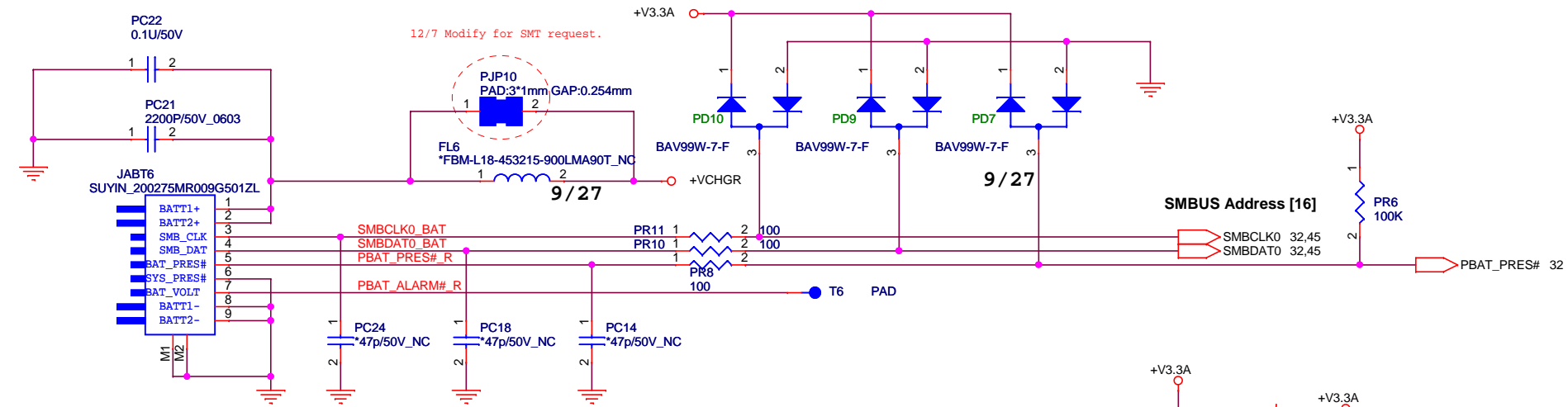
TO CPU



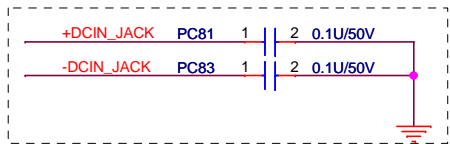
FROM VCORE POWE GOOD

TO PCH

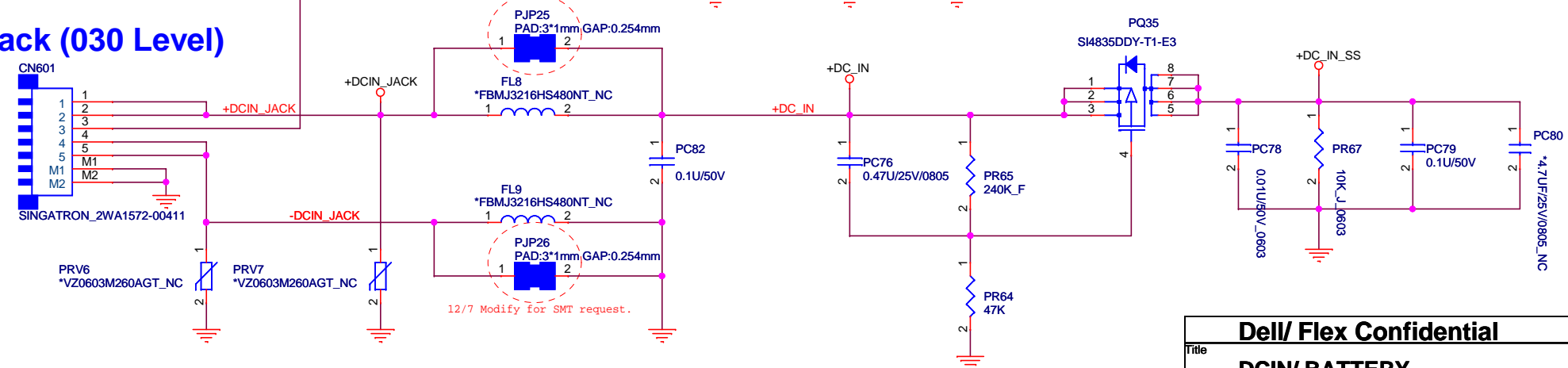
TO PCH



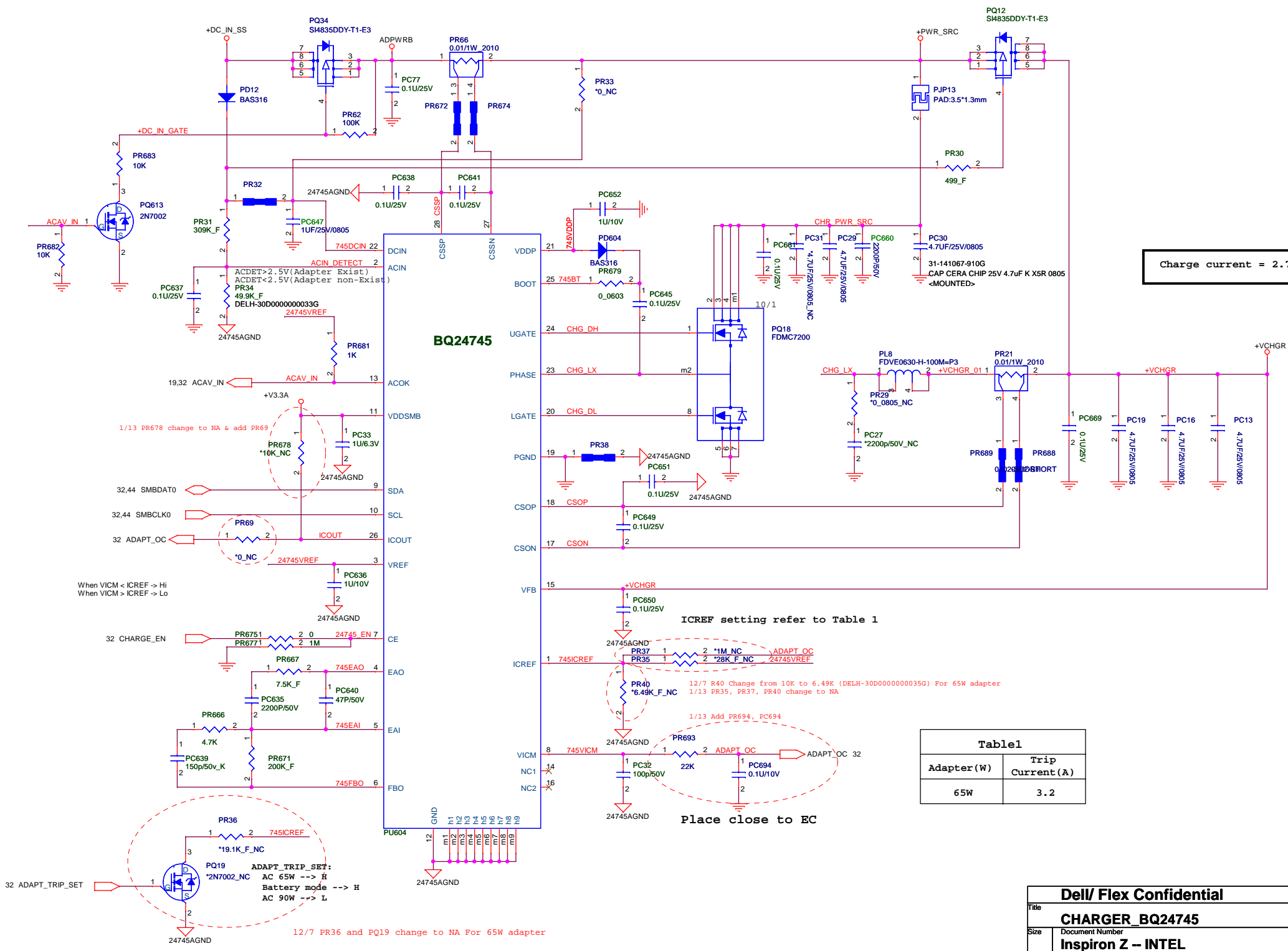
Battery Conn (030 Level)



DC Jack (030 Level)



Dell/ Flex Confidential		
Title		
DCIN/ BATTERY		
Size	Document Number	Rev
	Inspiron Z -- INTEL	X01
Date:	Monday, January 18, 2010	Sheet 44 of 57



Charge current = 2.7A

ICREF setting refer to Table 1

Adapter (W)	Trip Current (A)
65W	3.2

Place close to EC

When VICM < ICREF -> Hi
 When VICM > ICREF -> Lo

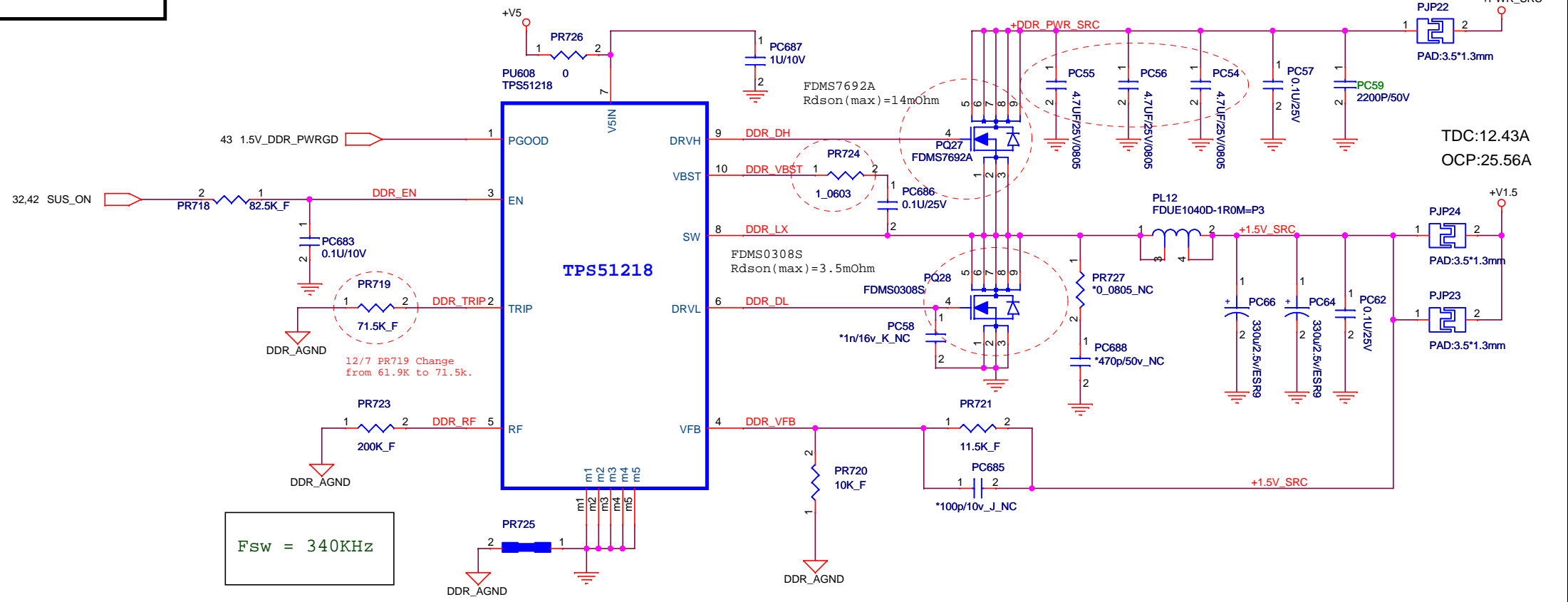
1/13 PR678 change to NA & add PR69

12/7 R40 Change from 10K to 6.49K (DELH-30D000000035G) For 65W adapter
 1/13 PR35, PR37, PR40 change to NA

12/7 PR36 and PQ19 change to NA For 65W adapter

12/7 PR36 and PQ19 change to NA For 65W adapter

1.5VDDR



0.75VS

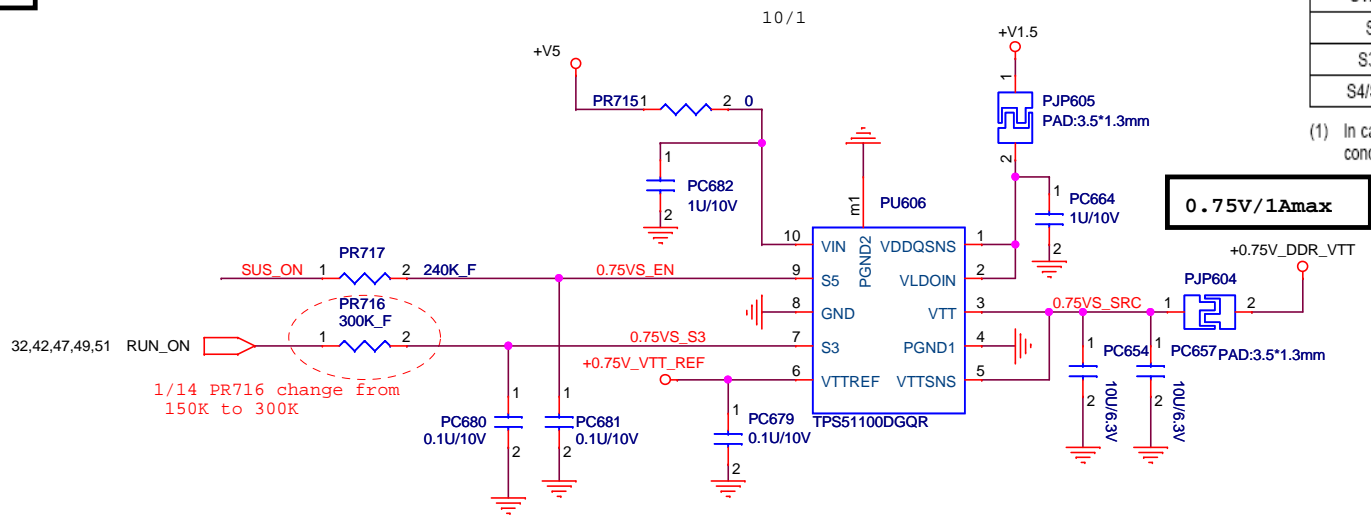


Table 1. S3 and S5 Control Tabl

STATE	S3	S5	VTTREF	VTT
S0	H	H	1	1
S3 ⁽¹⁾	L	H	1	0 (high-Z)
S4/S5 ⁽¹⁾	L	L	0 (discharge)	0 (discharge)

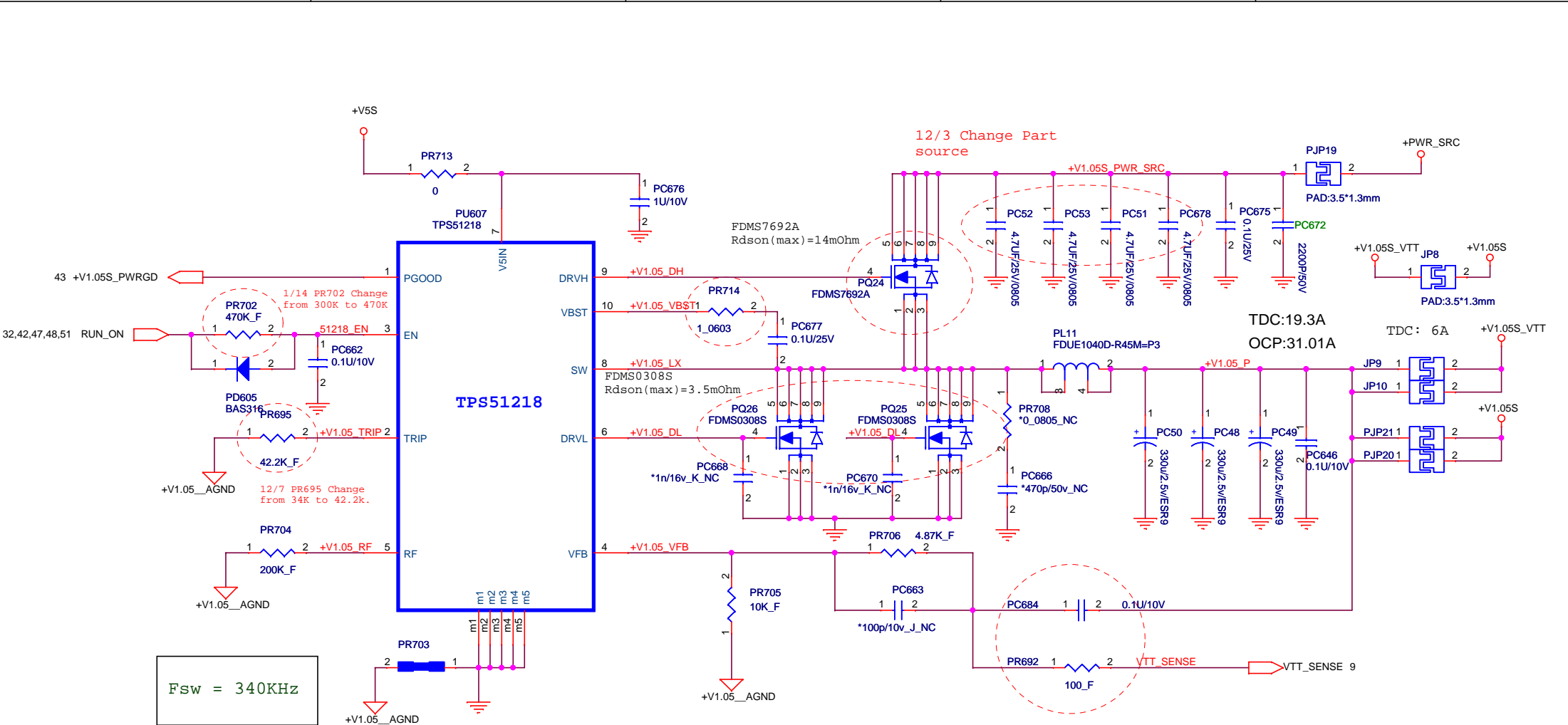
(1) In case S3 is forced to H and S5 to L, VTTREF is discharged and VTT is at High-Z state. This condition is NOT recommended.

Dell/ Flex Confidential

Title: **+V1.5 / +0.75VS**

Size: Document Number **Inspiron Z -- INTEL** Rev X01

Date: Monday, January 18, 2010 Sheet 48 of 57



Fsw = 340KHz

12/3 Change Part source

1/14 PR702 Change from 300K to 470K

12/7 PR695 Change from 34K to 42.2K.

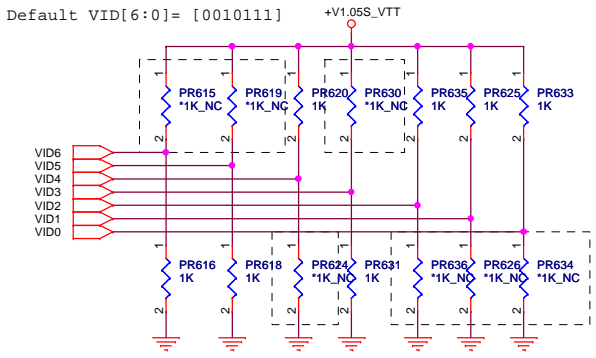
11/23 R692, R693 change from 0 ohm to 100 ohm & 0.1uF.

Dell/ Flex Confidential		
Title +V1.05S_TPS51218		
Size	Document Number	Rev X01
Date:	Monday, January 18, 2010	Sheet 49 of 57

Default VID[6:0]= [00101111]

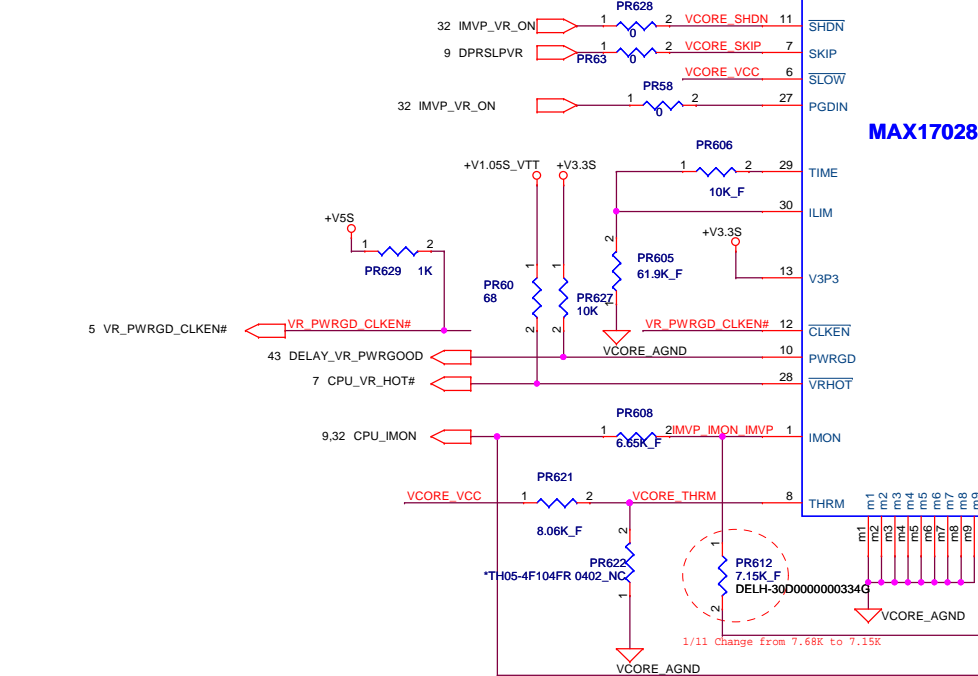
VID6
VID5
VID4
VID3
VID2
VID1
VID0

VID INPUTS



VID0 14
VID1 15
VID2 16
VID3 17
VID4 18
VID5 19
VID6 20

MAX17028



D0
D1
D2
D3
D4
D5
D6

SHDN
SKIP
SLOW
PGDIN
TIME
ILIM
V3P3
CLKEN
PWRGD
VRHOT
IMON
THRM
GNDS

Fsw = 297KHz

12/3 Change Part source

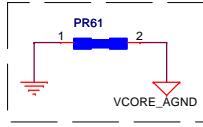
TDC=16.2A
OCP=33.75

*PR988, PR991, PC776 close to chip

$$\text{CURRENT LIMIT} = \left(\frac{2V \times R30}{R29 + R30} \right) \times \frac{1}{10 \times Rsense}$$

IMON Setting
415701_415701_PRD_HLL_CRB_UG_Rev1.1.pdf Table 18

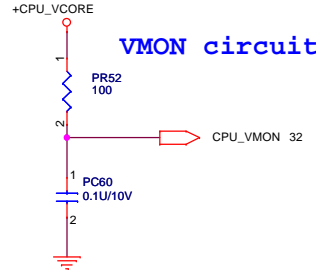
Processor	IccMax	IMON Resistor	VID [5:3]
ULV	27A	20 K ohm	010



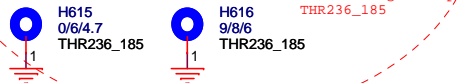
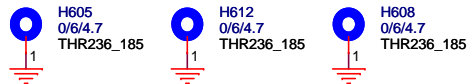
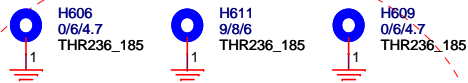
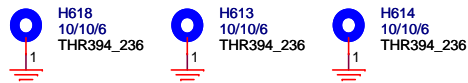
Locate Near Pin m1 of MAX17028

$$\text{LOAD LINE} = \frac{V}{A} = R38 \times RSENSE \times 0.6ms$$

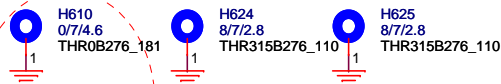
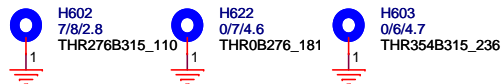
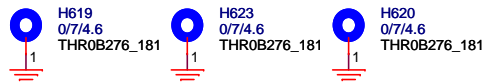
VMON circuit



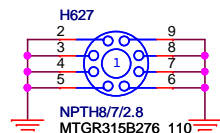
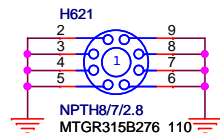
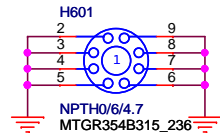
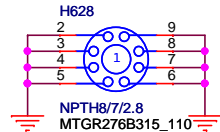
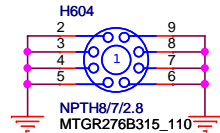
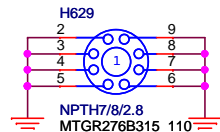
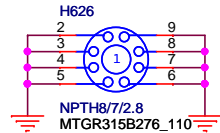
Screw Hole



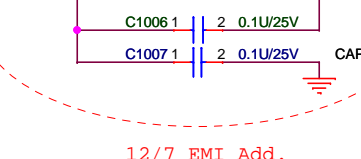
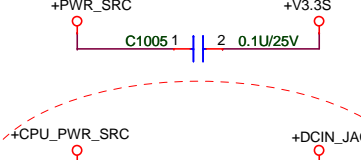
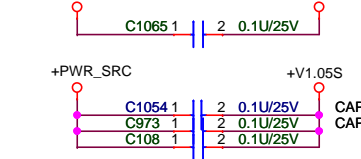
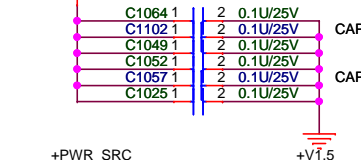
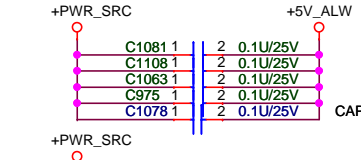
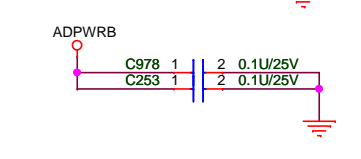
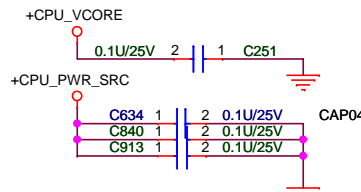
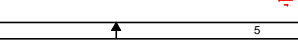
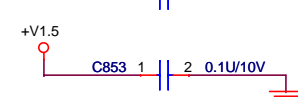
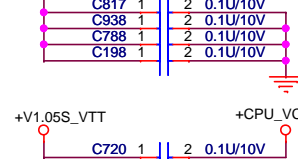
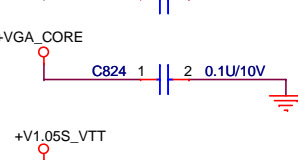
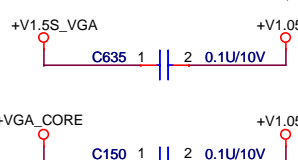
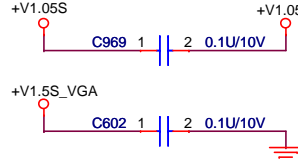
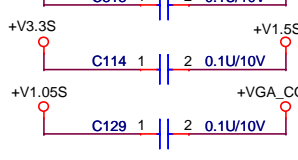
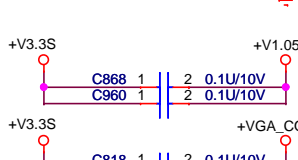
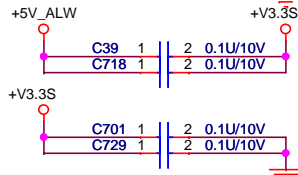
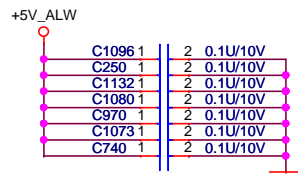
11/19 Change Footprint to THR236_185



11/19 Change Footprint to THROB276_181



Moat Cap



12/7 EMI Add.

FID

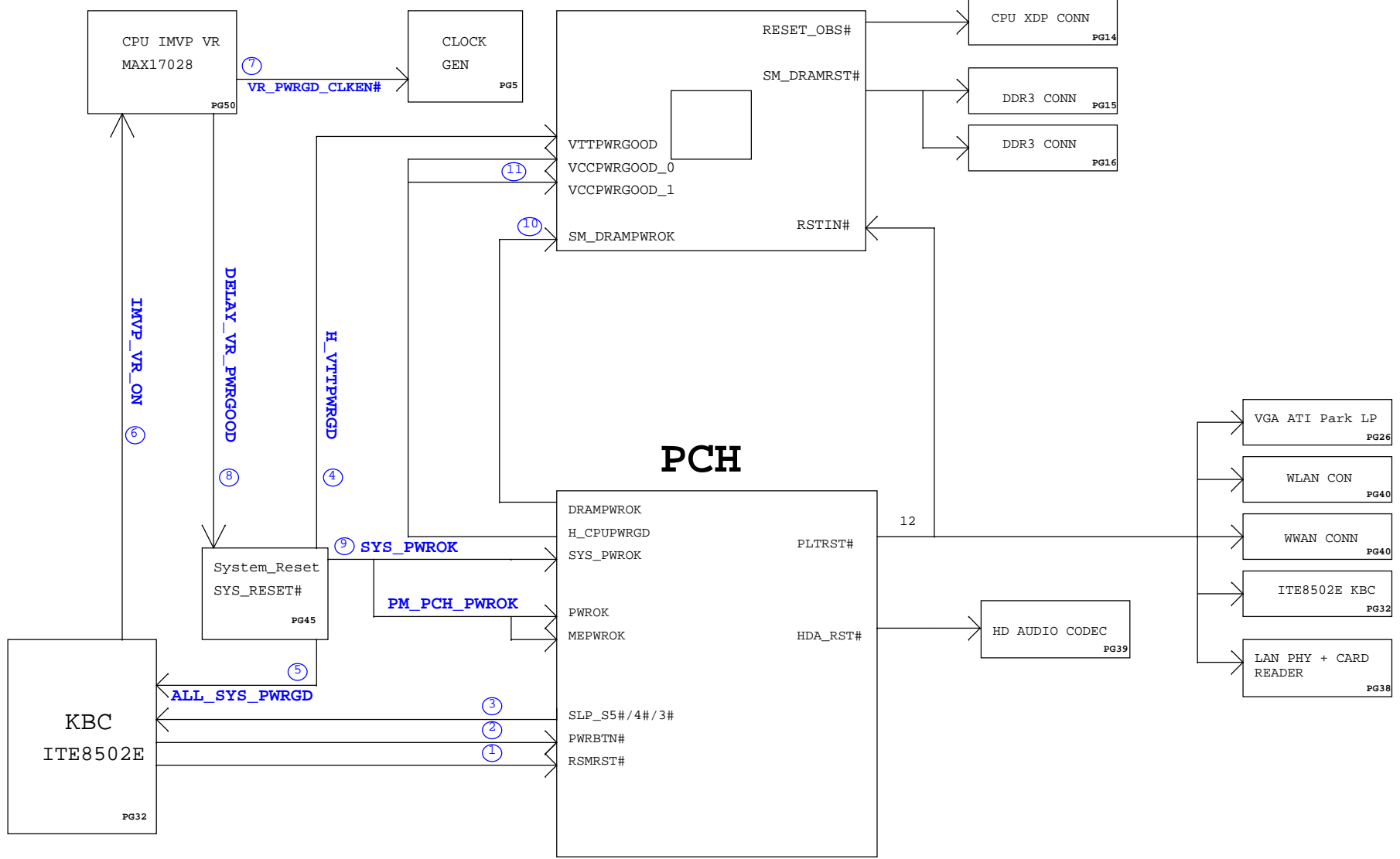


DE LH-31D0010000007G

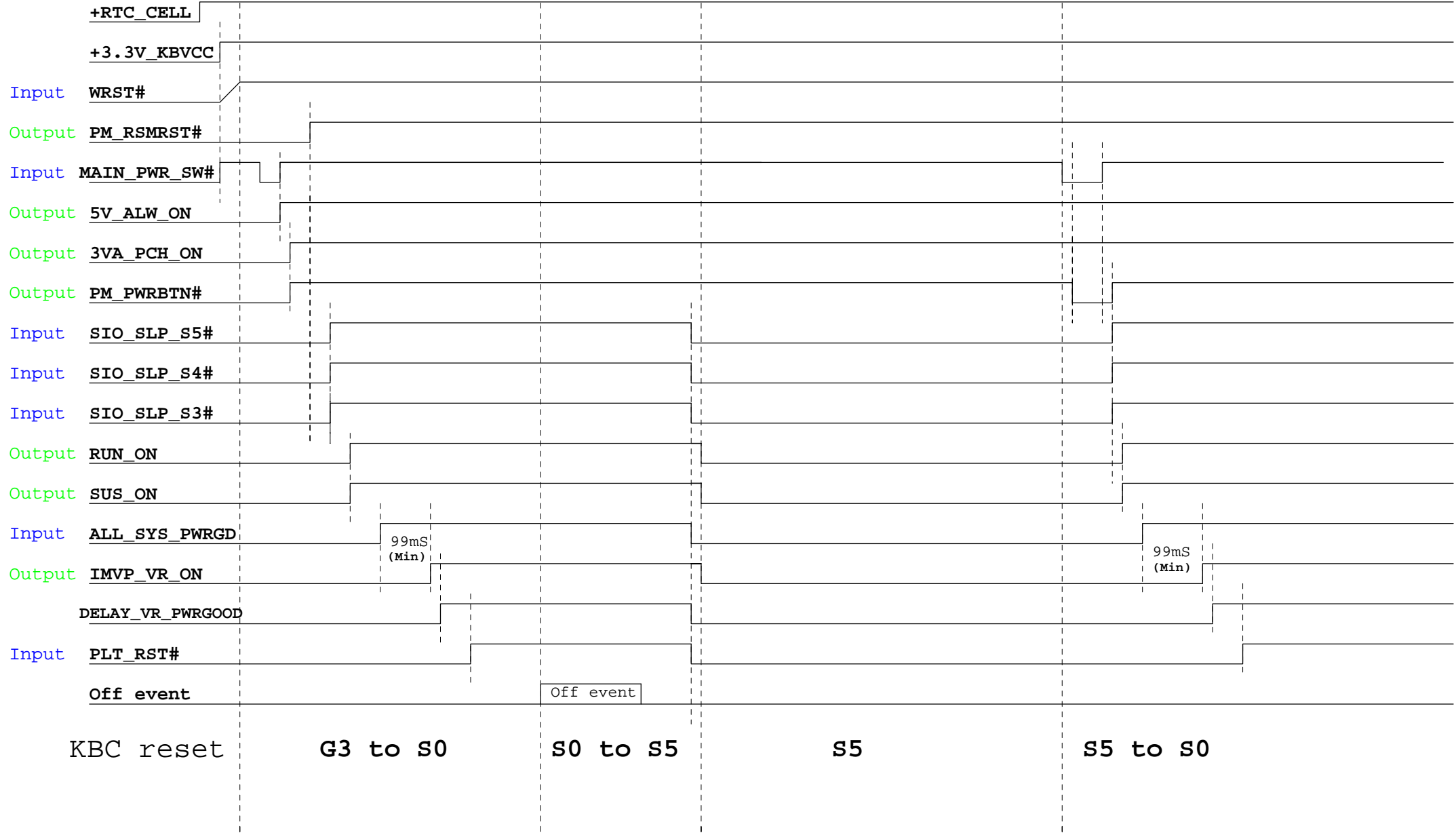
DE LH-31D0010000007G

Dell/ Flex Confidential		
Title SCREW / PAD		
Size	Document Number Inspiron Z -- INTEL	Rev X01
Date:	Monday, January 18, 2010	Sheet 52 of 57

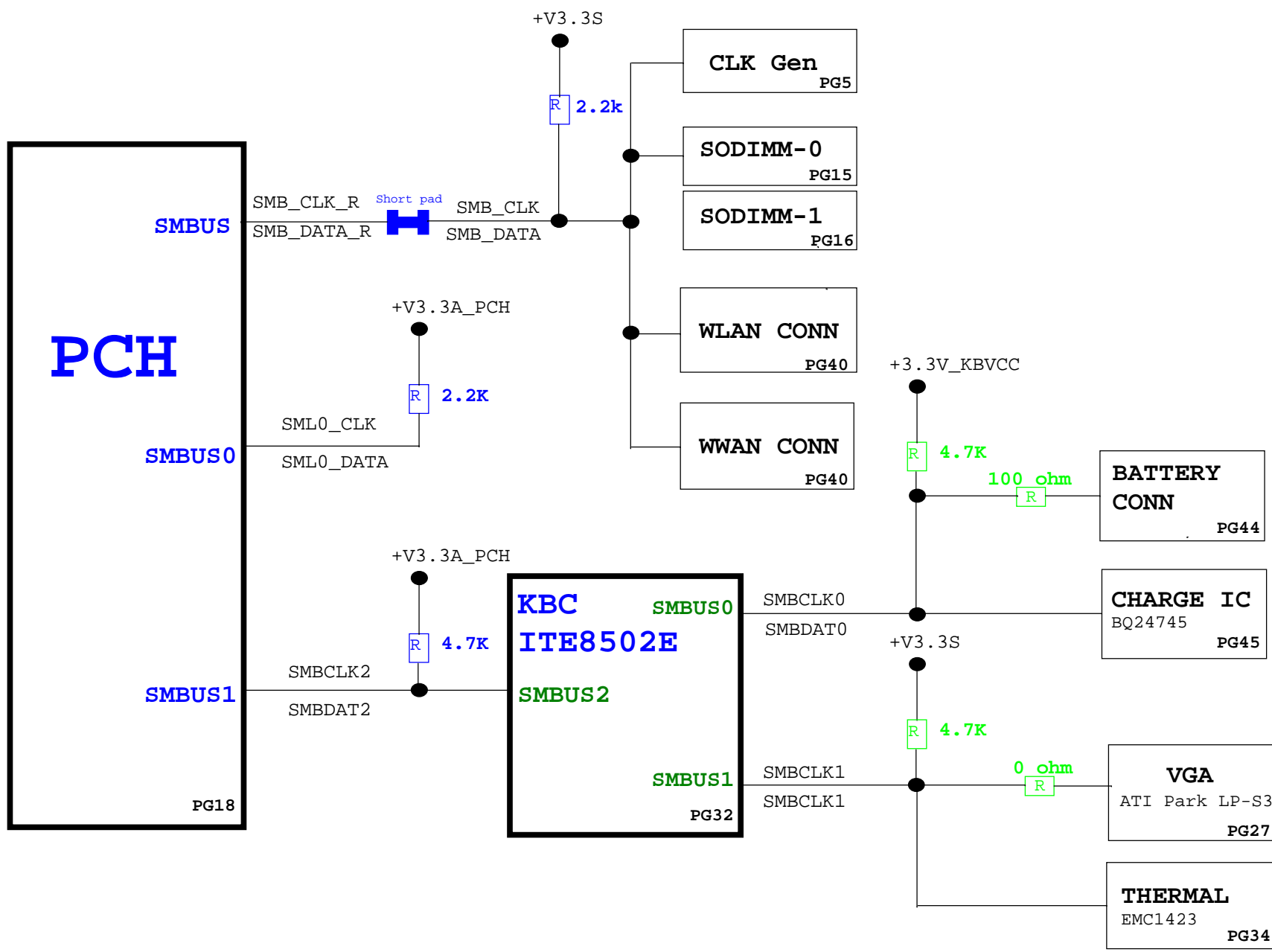
PCI RESET MAP



KBC Powre Up Sequence



Dell/ Flex Confidential			
Title: KBC Power Up Sequence			
Size:	Document Number:	Rev: X01	
Date:	Monday, January 18, 2010	Sheet:	55 of 57



EE change

Item	Fixed Issue	Reason for Change	Rev	PG#	Modify List
1	MMC Plus Can't Read	MMC Plus Can't Read	X01	38	C1055 change from 15pF to 5.6pF (DELH-31D0000000022G)
2	Update Conn MFR PN	Update Conn MFR PN	X01	36, 37, 41	CN10 (HDMI) Change to DELH-38-00F00000013G, CN11 (mDP) Change to DELH-38D01100000005G, CN612 (HDD) Change to DELH-38-00E00000071G, CN607 (KB) Change to DELH-38-00E00000072G
3	Update Chipset MFR PN	Update Chipset MFR PN	X01	7, 17	U17 CPU 1.2G (SLBMM) Change to DELH-11D00100000046G, U10 HM57 (SLGZR) Change to DELH-10D00100000012G
4	For HDMI SMBus Signal Quality	For HDMI SMBus Signal Quality	X01	36	C57, C67 Change from 33pF to 18pF DELH-31D0000000005G
5	Power Sequence	Power Sequence	X01	42	PR49 Change to 162K, PR55 Change to 330K, PR638 Change to 820K, PR642 Change to 240K, PR702 Change to 470K, PR716 Change to 300K.
6	Board ID Upgrade	Board ID Upgrade	X01	32	BID change from 01 to 10 for ST stage

POWER change

Item	Fixed Issue	Reason for Change	Rev	PG#	Modify List
1	Change Adapter OC control employment	Change Adapter OC control employment	X01	45	PR35, PR37, PR40, PR678 Change to NA. Add PR693 22K (DELH-30D00000000105G), Add PC694 0.1uF/10V(DELH-31D00200000012G), PR69 0ohm (NA) (DELH-30D00000000036G)
2	Improve 1.8V phase gain margin	Improve 1.8V phase gain margin	X01	47	PC658 change from 22pF to 33pF/50V(DELH-31D0000000009G)
3	PS_ID	DELL Suggestion	X01	44	PR685 Change from 100ohm to 33ohm.
4	VIMON RC Time Adjustment	From 196uS to 337uS	X01	50	PC609 change to 33nF/16V/X7R(DELH-31D00200000049G)
5	VIMON voltage precision	Vimon = 1V at load = 27A	X01	50	PR612 change to 7.15K_F_0402(DELH-30D00000000334G)
6	Improve load line precision	Improve load line precision	X01	50	PR614 change to 5.1K_F_0402(DELH-30D0000000061G)
7	Adjust the transeint response	Adjust the transeint response	X01	50	PC613 change to 1000pF/50V(DELH-31D00200000037G) and mounted
8	Update IC MFR PN	Update IC MFR PN	X01	47	Change PU6 MFR PN to RT8015DGQW (DELH-15D00B00000028G)

EMI change

Item	Fixed Issue	Reason for Change	Rev	PG#	Modify List