

COMPAL CONFIDENTIAL

MODEL NAME : *JAU00*

PCB NO : *LA-3741P*

COMPAL P/N : *DA800008W0L*

Carson Schematics Document

**uFCBGA Mobile Merom-ULV
Intel Calistoga-GMS + ICH7M**

2007-01-24

REV : 0.1 (DELL: X00)

HW POP option control table										
	01 BOM	02 BOM	03 BOM	04 BOM						
BOM No.	45148731L01	45148731L02	45148731L03	45148731L04						
CPU P/N	SA00001ND0L	SA00001MA1L	SA00001ND0L	SA00001MA1L						Location: U2
CPU Type	Dual core	Dual core	Dual core	Dual core						
Speed/power	1.2G ,9W	1.06G , 9W	1.2G ,9W	1.06G , 9W						
C41,C44	220 uf	220 uf	220 uf	220 uf						330 uf Poly Cap ; P/N : SGA00001P0L 220 uf Poly Cap ; P/N : SGA00002D0L
C42,C43	Pop	Pop	Pop	Pop						POP 2@ ; 220 uf for Dual core 220 uf Poly Cap ; (P/N : SGA00002D0L)
C21,C26,C29,C31 C34,C36,C28,C23	10 uf	10 uf	10 uf	10 uf						10 uf MLCC Cap ; P/N (SE00000110L) 22 uf MLCC Cap ; P/N (SE160106M8L)
C694,C697,C37,C39,C22 C698,C693,C25,C40,C35 C699,C700,C30,C33,C27 C703,C704,C38	Pop	Pop	Pop	Pop						POP 2@ ; 10 uf for Dual core 10 uf MLCC Cap ; P/N (SE160106M8L)
JP3	Depop	Depop	Pop	Pop						POP 4@ ; For with TAA Board
U50	Pop	Pop	Depop	Depop						POP 1@ ; For without TAA Board

MB PCB	
Part Number	Description
DA800008W0L	PCB 02P LA-3741P REV0 M/B

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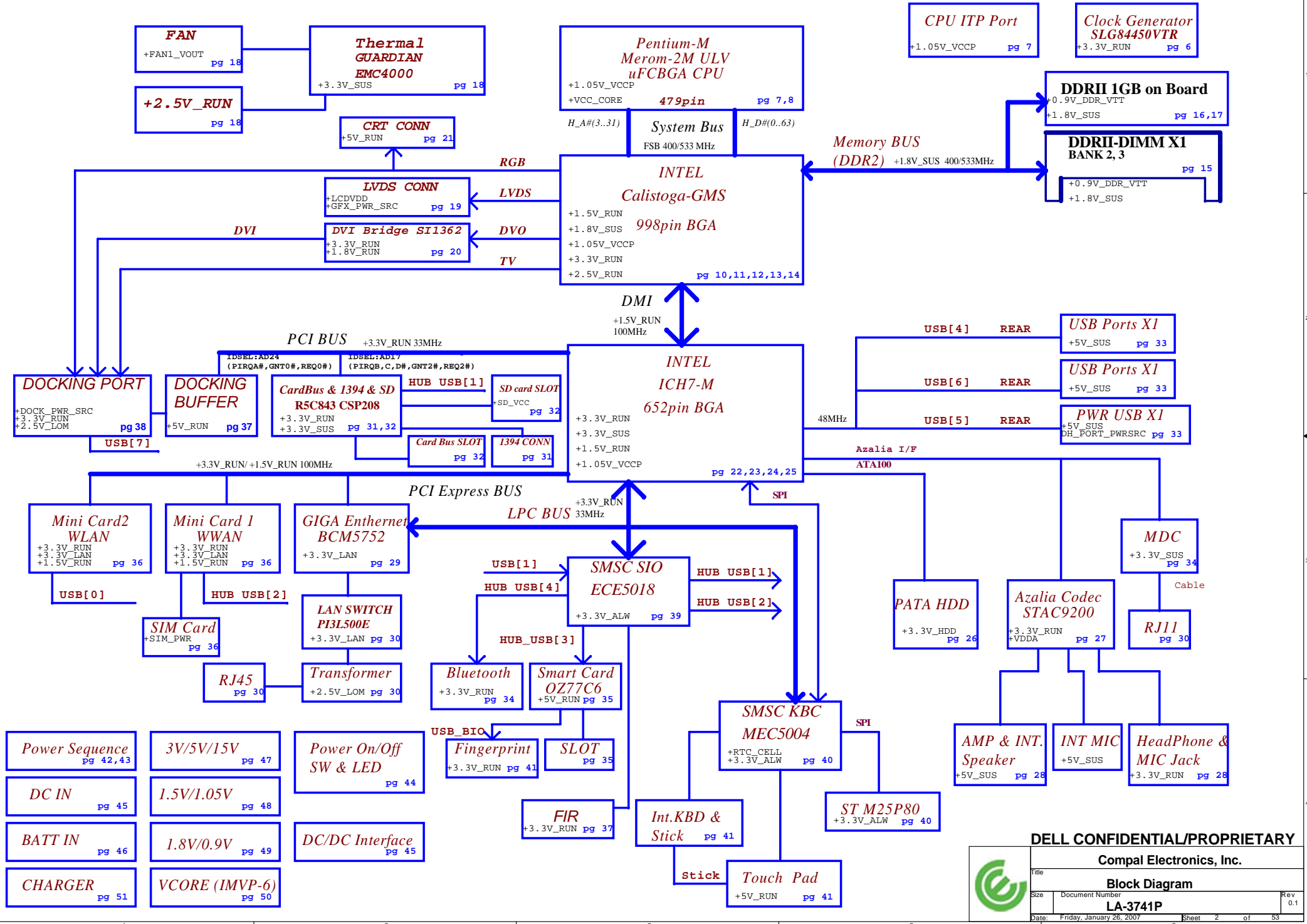
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Cover Sheet

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Rev 0.1

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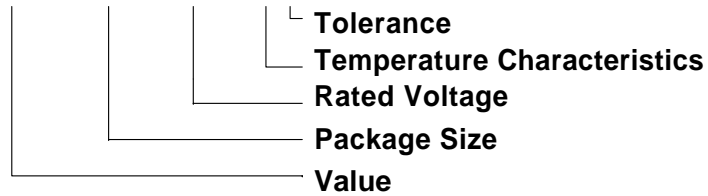


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Title Block Diagram		
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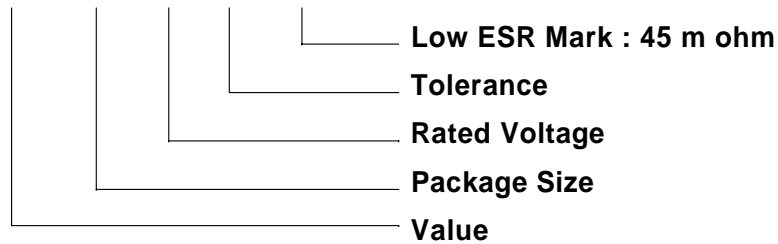
Ceramic Capacitors :

0.1U_0402_6.3VXX



Tantalum or Polymer Capacitors :

10U_D2_10VX_R45



Capacitor Spec Guide:

Temperature Characteristics:

Symbol	0	1	2	3	4	5	6	7
CODE	Z5U	Z5V	Z5P	Y5U	Y5V	Y5P	X5R	X7R

8	9	A	B	C	D	E	F	G
NPO	COG	X6S	BJ	CH	CJ	CK	SH	SJ

H	I	J	K
UJ	UK	SL	X5S

Tolerance:

Symbol	A	B	C	D	F	G	H	J
CODE	+0.05PF	+0.1PF	+0.25PF	+0.5PF	+1PF	+2%	+3%	+5%

K	M	N	P	Q	V	X	Z	
+10%	+20%	+30%	+100,-0%	+30,-10%	+20,-10%	+40,-20%	+80,-20%	

NOTE1:

@XX : Depop component

PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
CARD BUS	AD17	2	B,C,D
DOCKING	AD24	0	A

PM TABLE

power plane / State	+3.3V_ALW +5V_ALW	+3.3V_SRC +3.3V_SUS +5V_SUS +1.8V_SUS +15V_SUS	+5V_RUN +3.3V_RUN +1.8V_RUN +0.9V_DDR_VTT +1.5V_RUN +VCC_CORE +1.05V_VCCP +2.5V_RUN
S0	ON	ON	ON
S1	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

USB TABLE

USB PORT#	DESTINATION	USB HUB	DESTINATION
0	Mini 2(WLAN)	1	PC Card Bay
1	USB Hub (5018)	2	Mini 1(WWAN)
2	N/A	3	SMART CARD
3	N/A	4	Blue tooth
4,6	REAR		
5	PWR USB		
7	Docking		
		USB HUB on OZ77C6LN	DESTINATION
		DP_HUB	Fingerprint

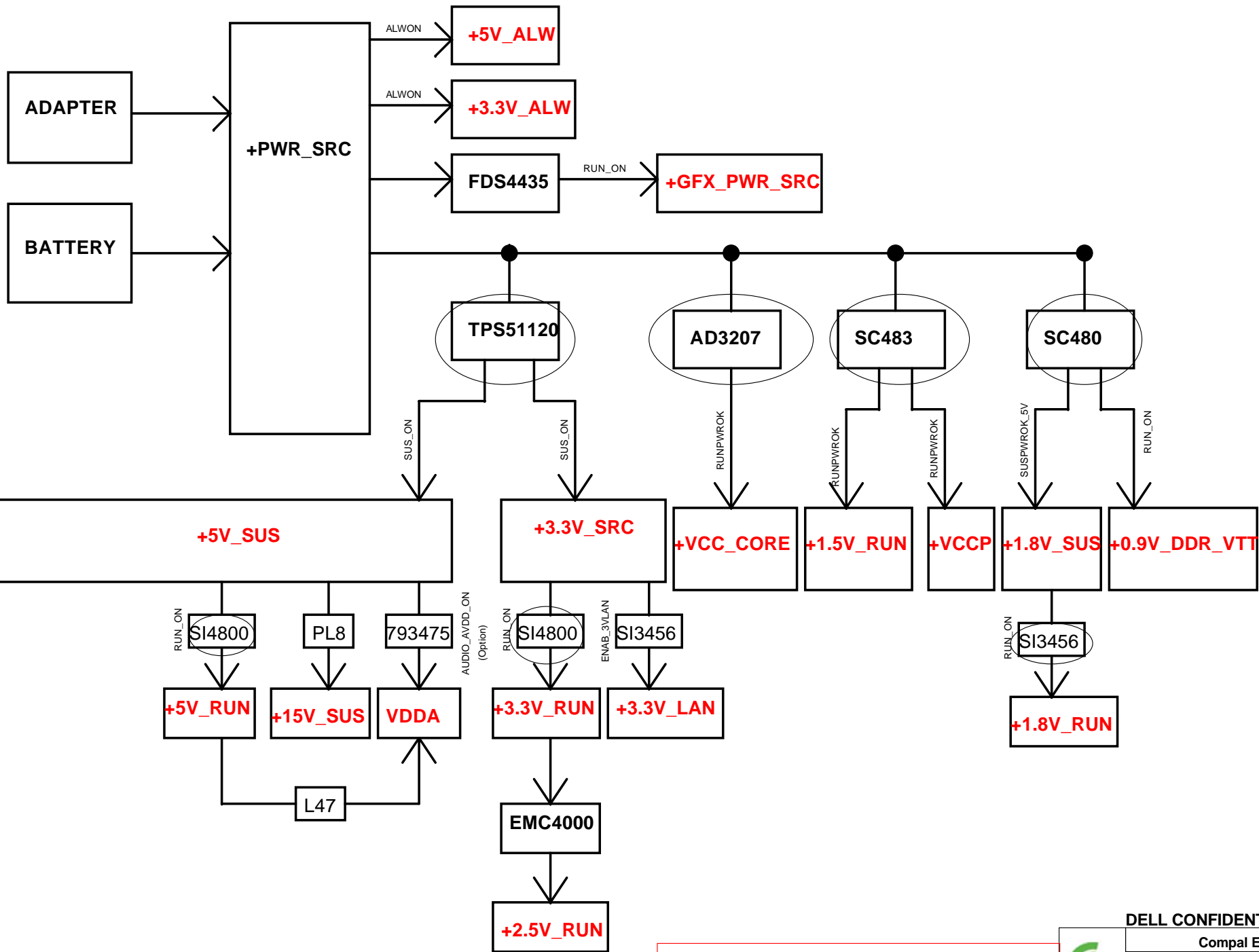
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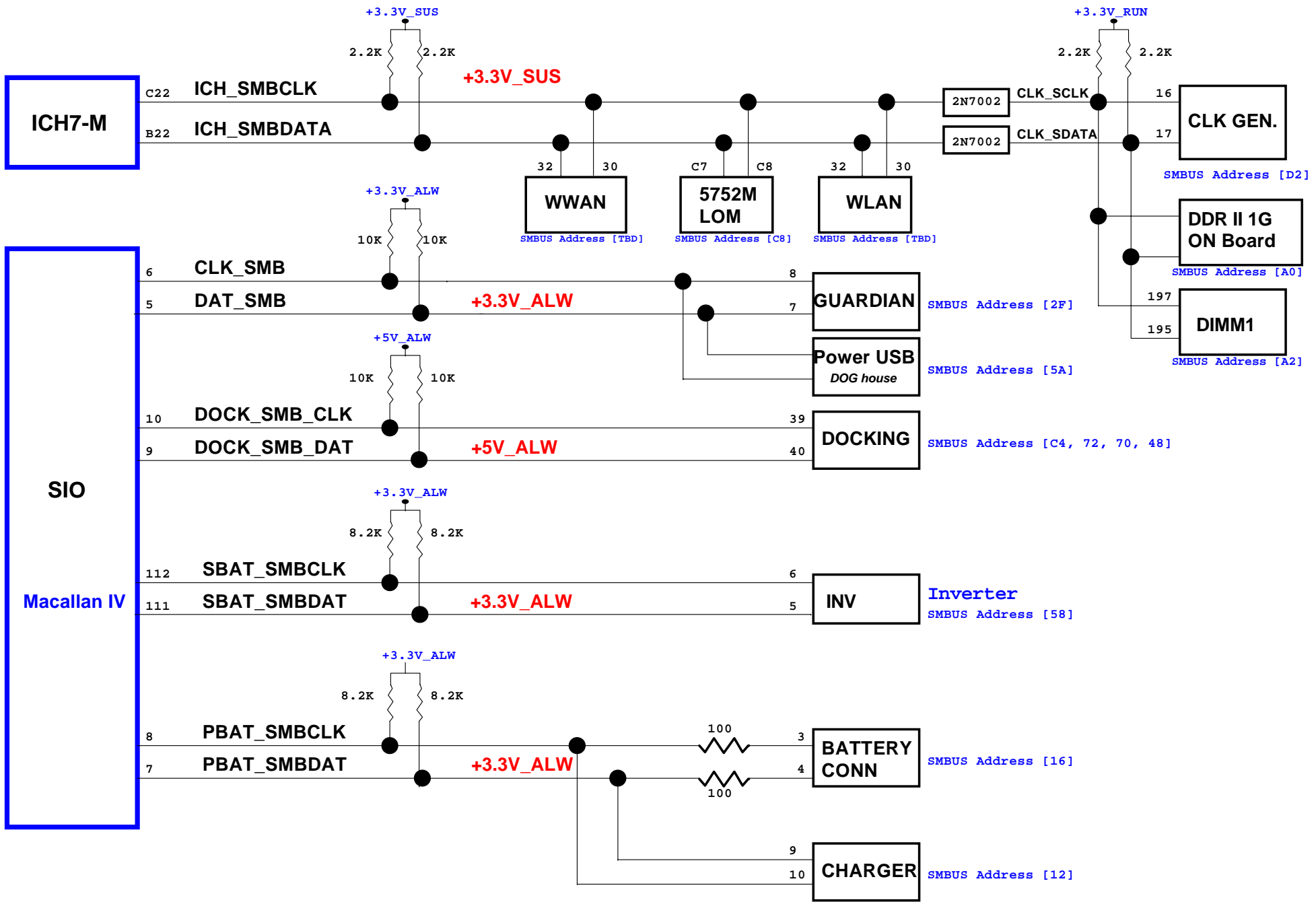
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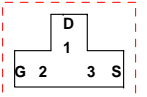
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Title			SMBUS TOPOLOGY		
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2N7002

<24,29,36> ICH_SMBDATA <<> ICH_SMBDATA

<24,29,36> ICH_SMBCLK <<> ICH_SMBCLK

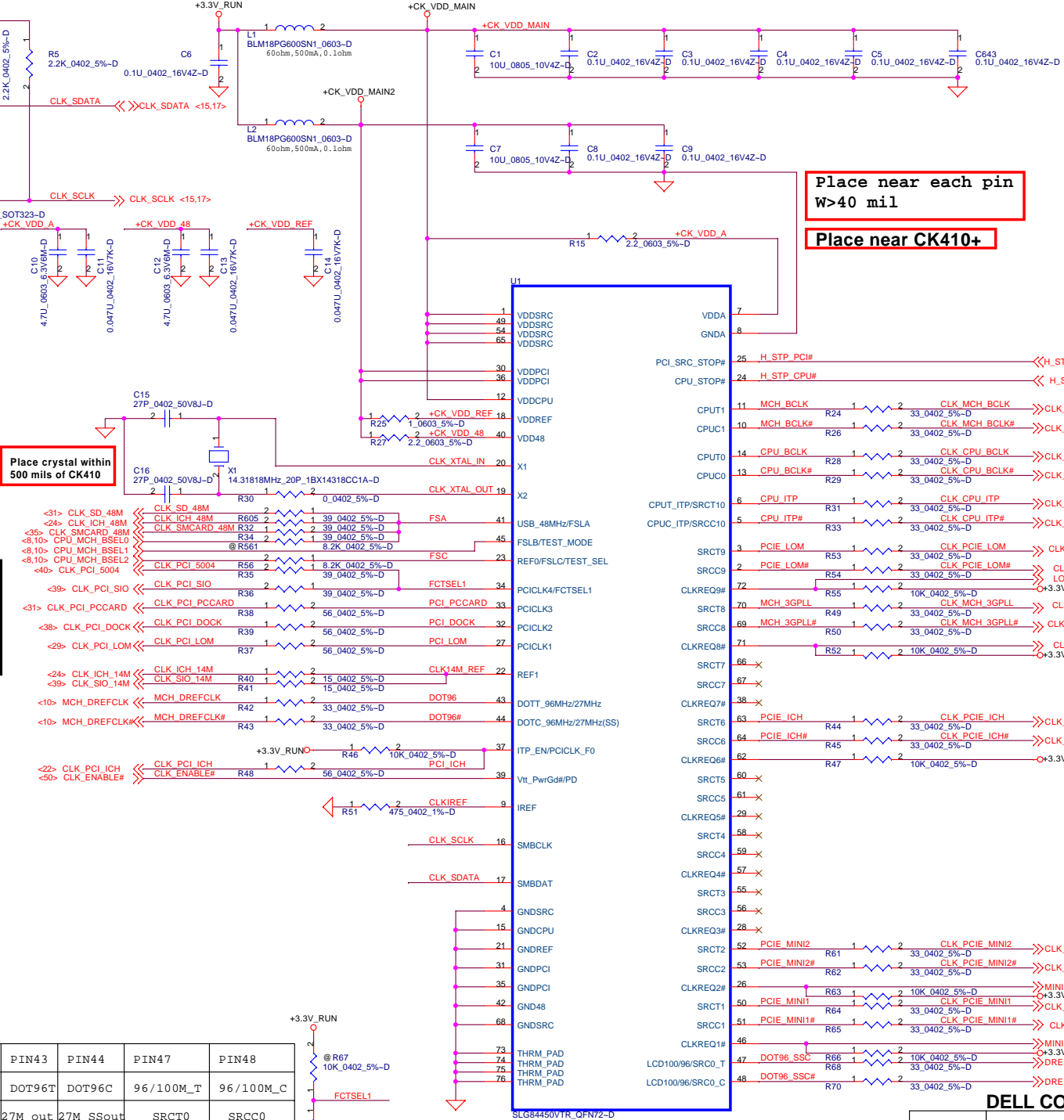
<15,17> CLK_SDATA <<> CLK_SDATA

<15,17> CLK_SCLK <<> CLK_SCLK

FSC	FSB	FSA	CPU	SRC	PCI
CLKSEL2	CLKSEL1	CLKSELO	MHz	MHz	MHz
0	0	0	266	100	33.3
0	0	1	133	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3
1	0	0	333	100	33.3
1	0	1	100	100	33.3
1	1	0	400	100	33.3
1	1	1			Reserve

CPU_BSEL	CPU_BSEL2 (FSC)	CPU_BSEL1 (FSB)
133	0	0
166	0	1

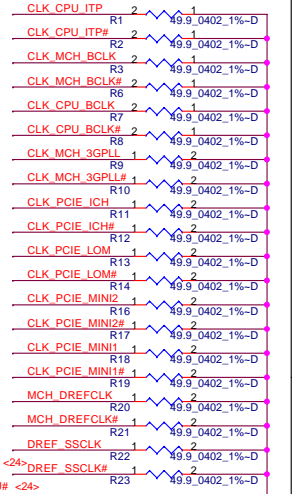
FCTSEL1	PIN43	PIN44	PIN47	PIN48
0	DOT96T	DOT96C	96/100M_T	96/100M_C
1	27M_out	27M SSout	SRCT0	SRCC0



Place near each pin
W>40 mil

Place near CK410+

Place crystal within
500 mils of CK410



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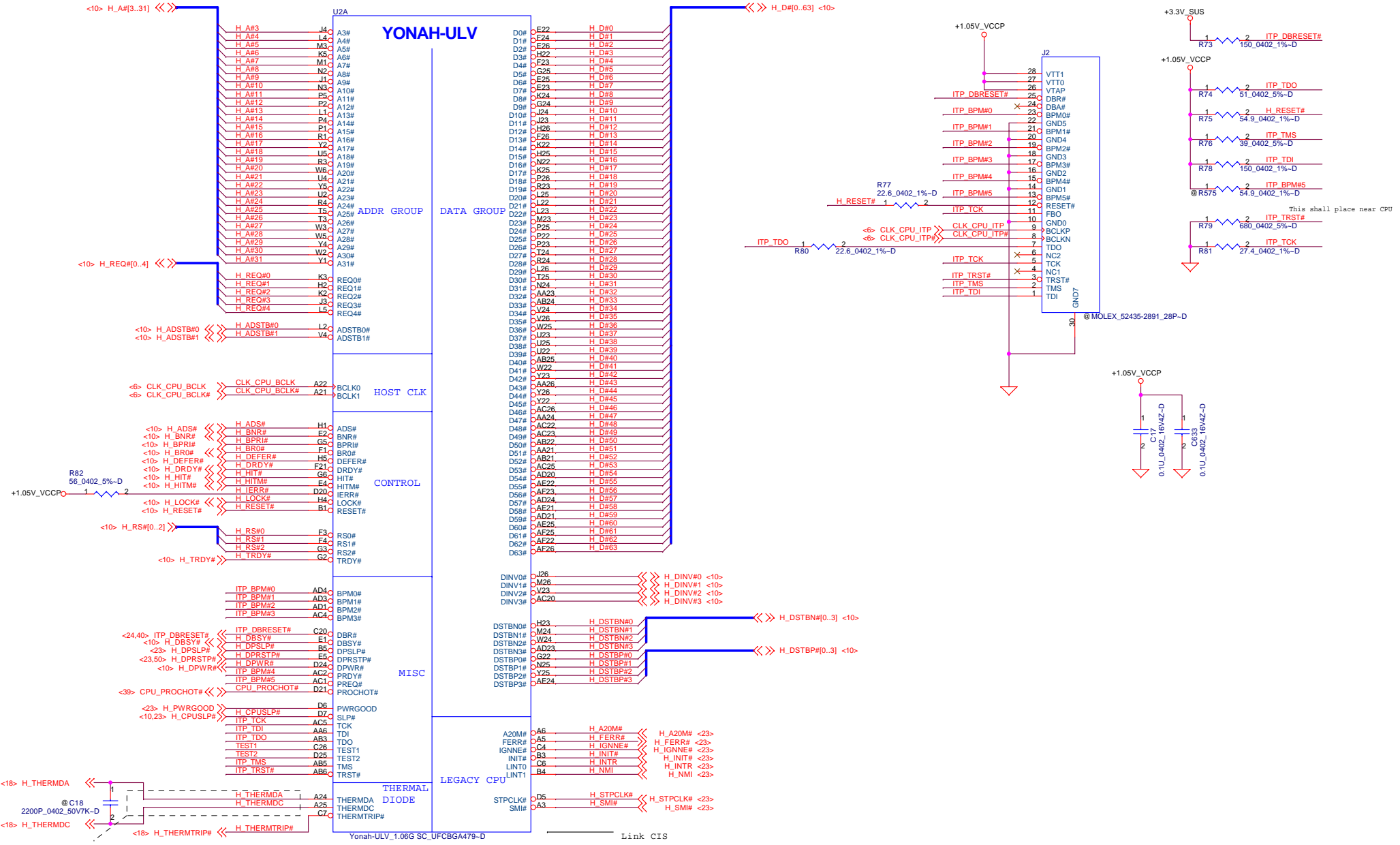
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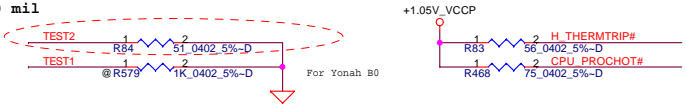
Clock Generator

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H_THERMDA, H_THERMDC routing together.
Trace width / Spacing = 10 / 10 mil



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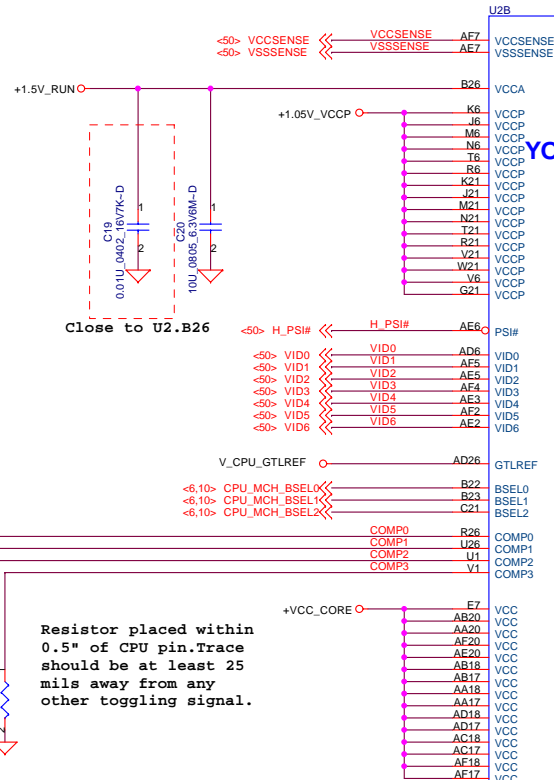
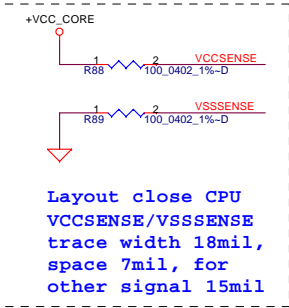
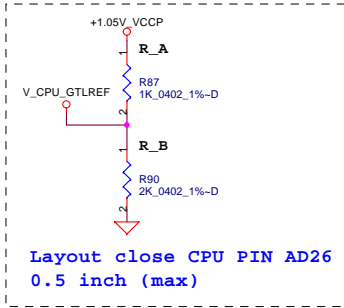
Yonah-ULV in mFCPGA479

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Length match within 25 mils



CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1

YONAH-ULV

YONAH-ULV

POWER, GROUING, RESERVED SIGNALS AND NC

POWER, GROUND

Yonah-ULV_1.06G_SC_UFCBGA479-D

Yonah-ULV_1.06G_SC_UFCBGA479-D

Link CIS

Link CIS

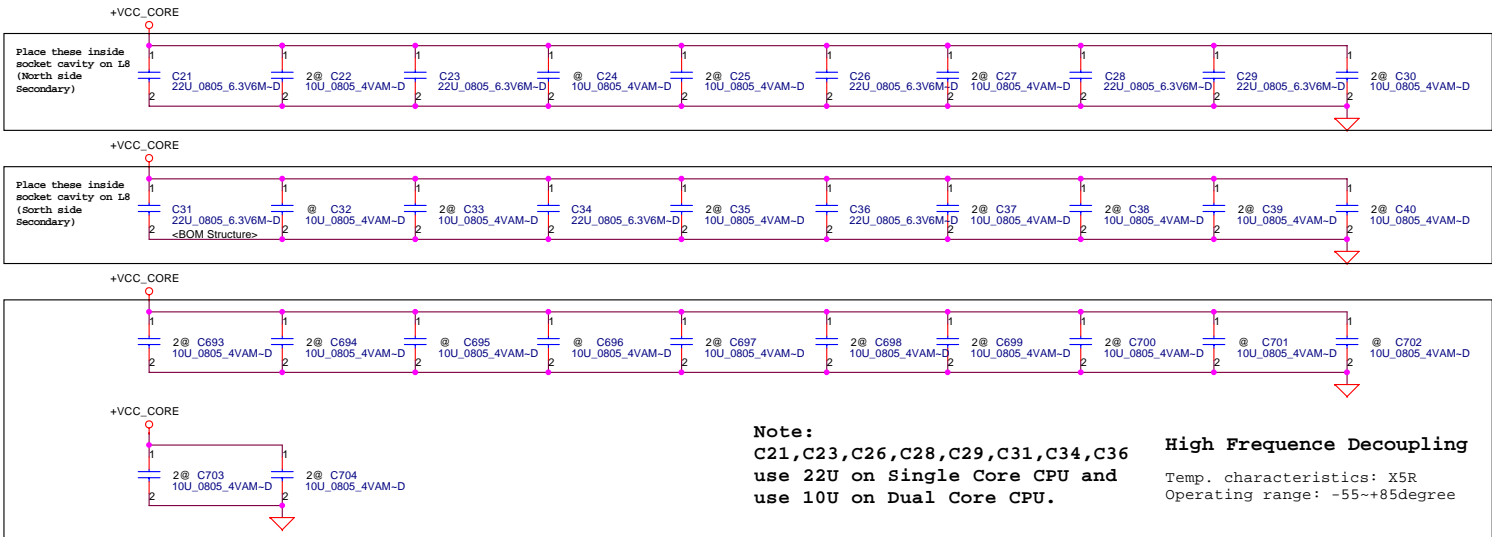
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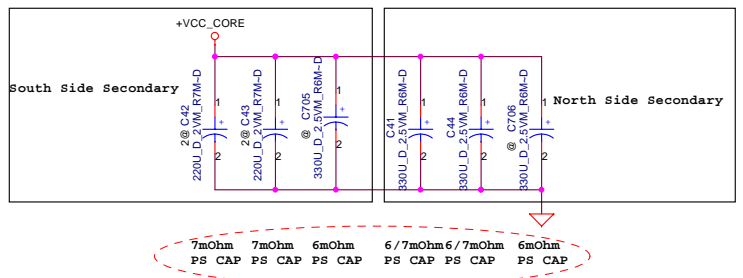
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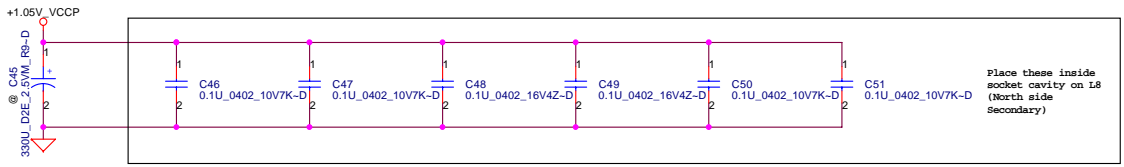


Note:
C21,C23,C26,C28,C29,C31,C34,C36 High Frequency Decoupling
 use 22U on Single Core CPU and
 use 10U on Dual Core CPU.
 Temp. characteristics: X5R
 Operating range: -55~+85degree

Near VCORE regulator.



Note: C41,C44
 will change to
 220U 2.5V 6M on
 Dual Core CPU for
 CPU transition
 noise
ESR <= 1.5m ohm
Capacitor = 1320uF



CRB was 270uF

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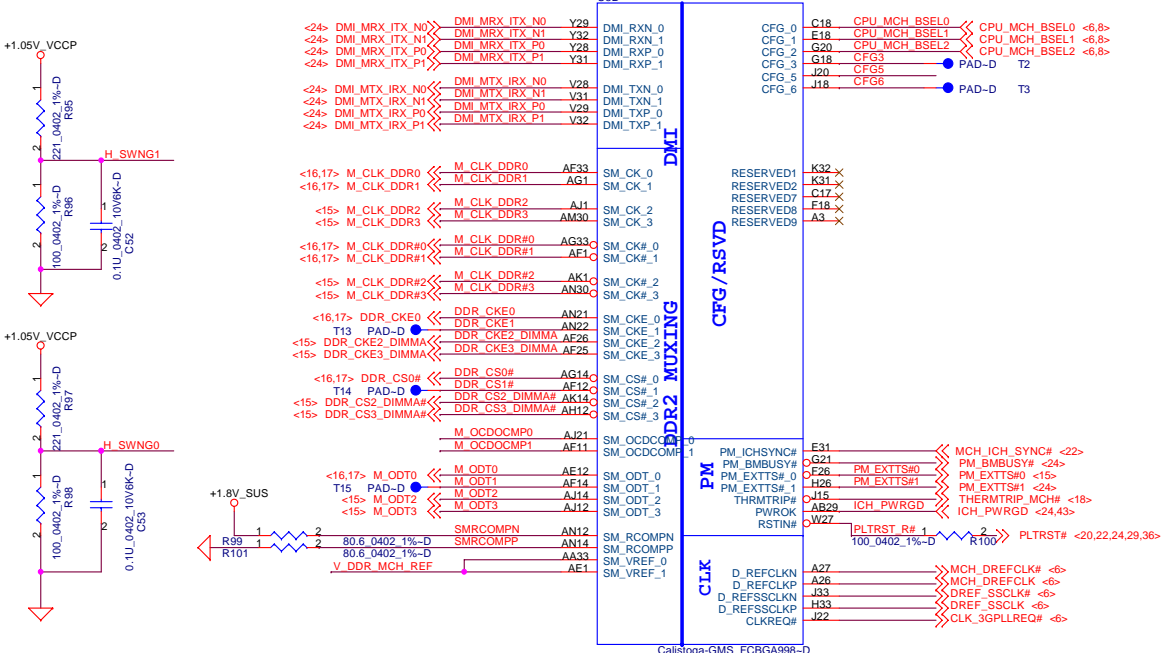
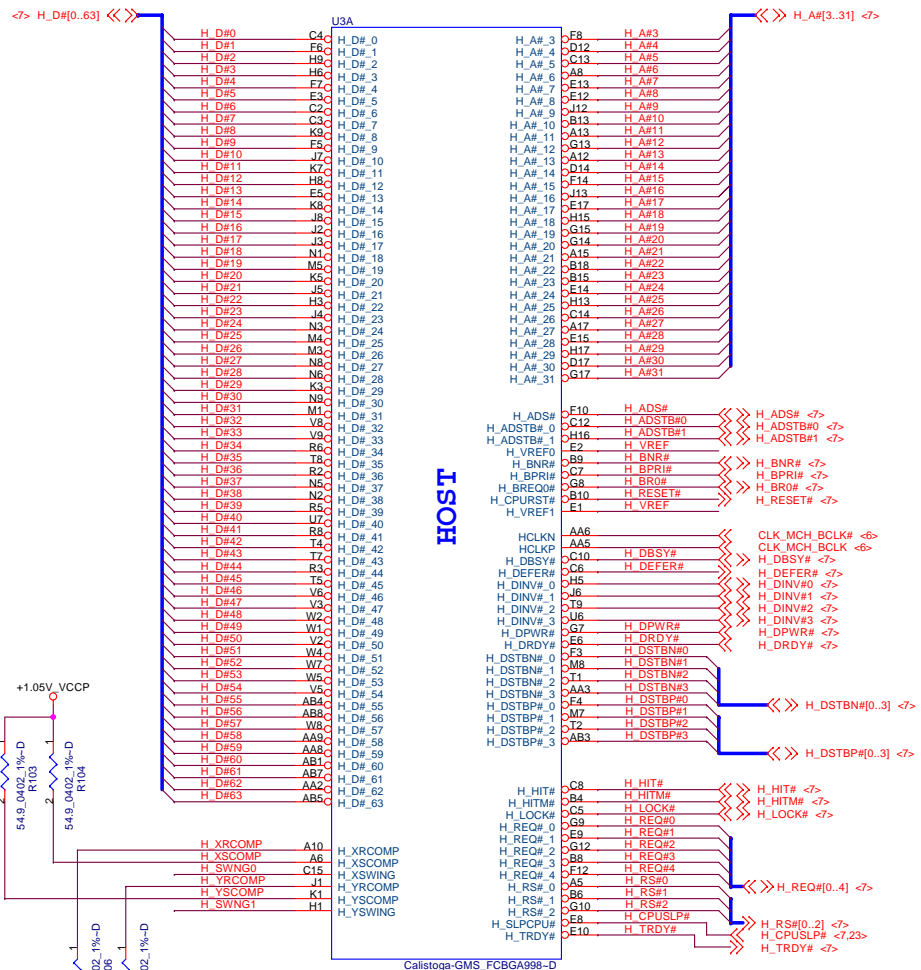
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CPU Bypass

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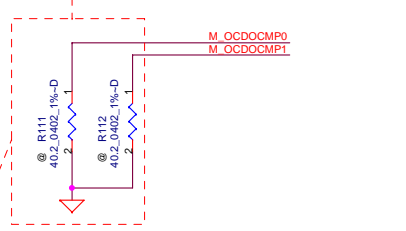


Strap Pin Table

CFG5	Low = DMI x 2 *
	High = DMI x 4
CFG19 (DMI Lane Reversal)	Low = Normal
	Operation (Default): Lane number in Order
	High = Reverse Lane

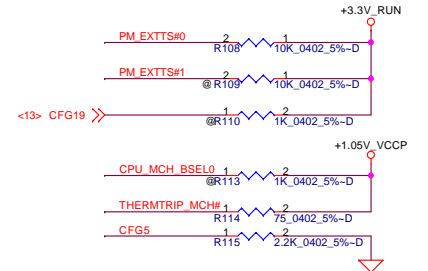
Calistoga-GMS not have CFG4,CFG7..18,CFG20
Need to double check

Layout Note:
Route as short as possible



Stuff R111 & R112 for A1 Calistoga

Layout Note:
H_XRCOMP & H_YRCOMP trace width and spacing is 10/20



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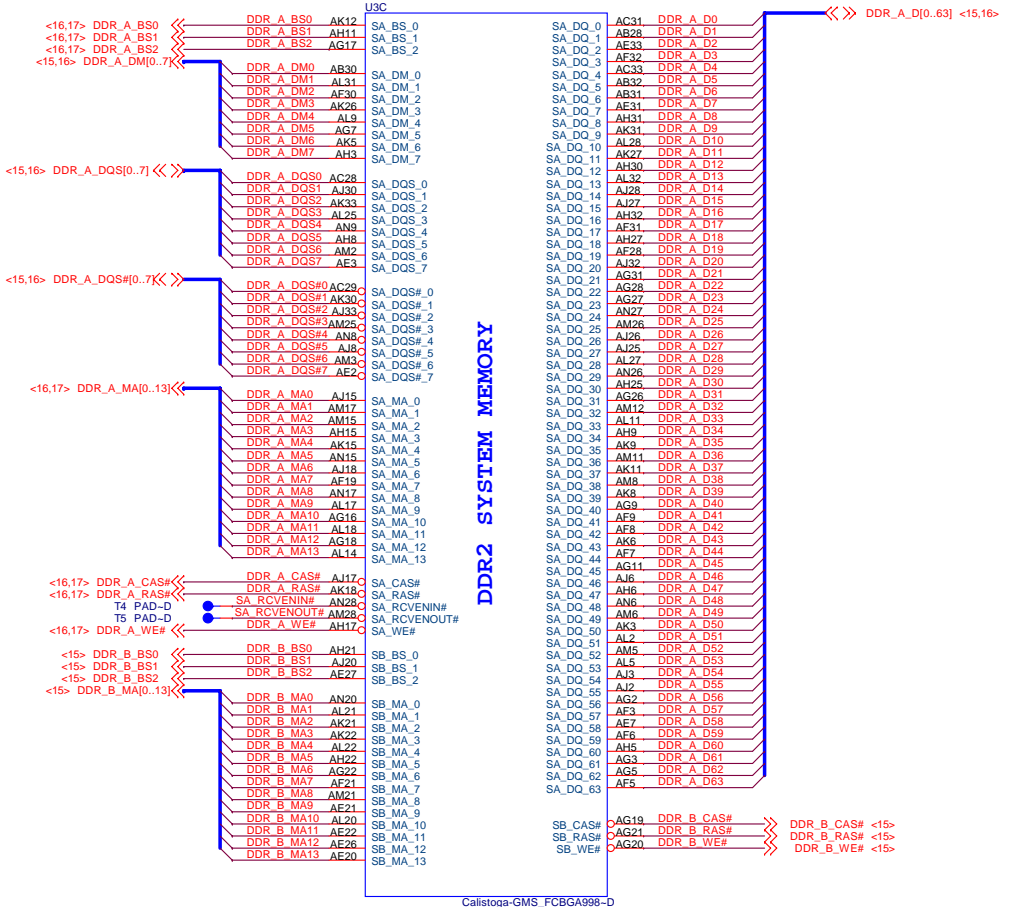
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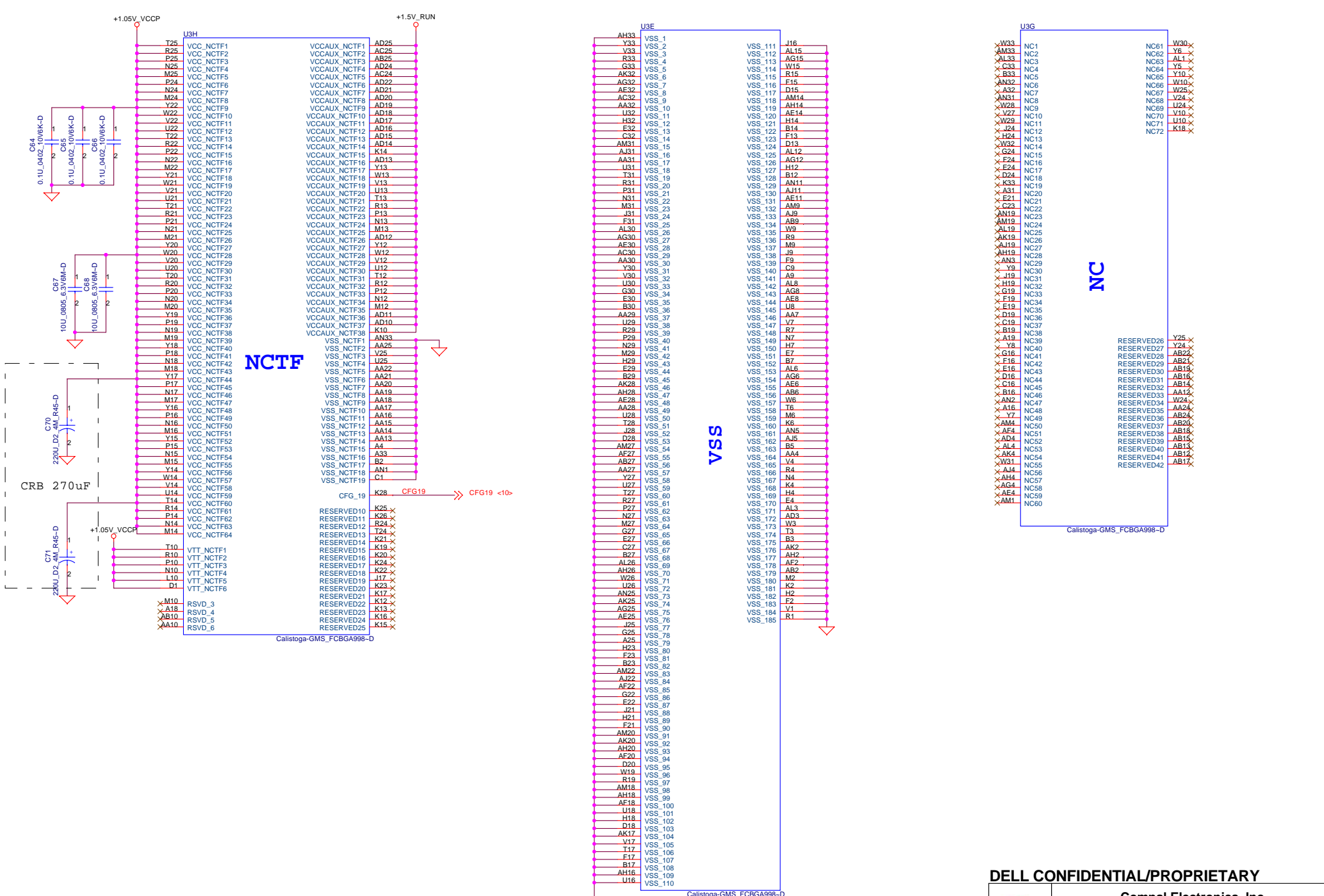
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NCTF

VSS

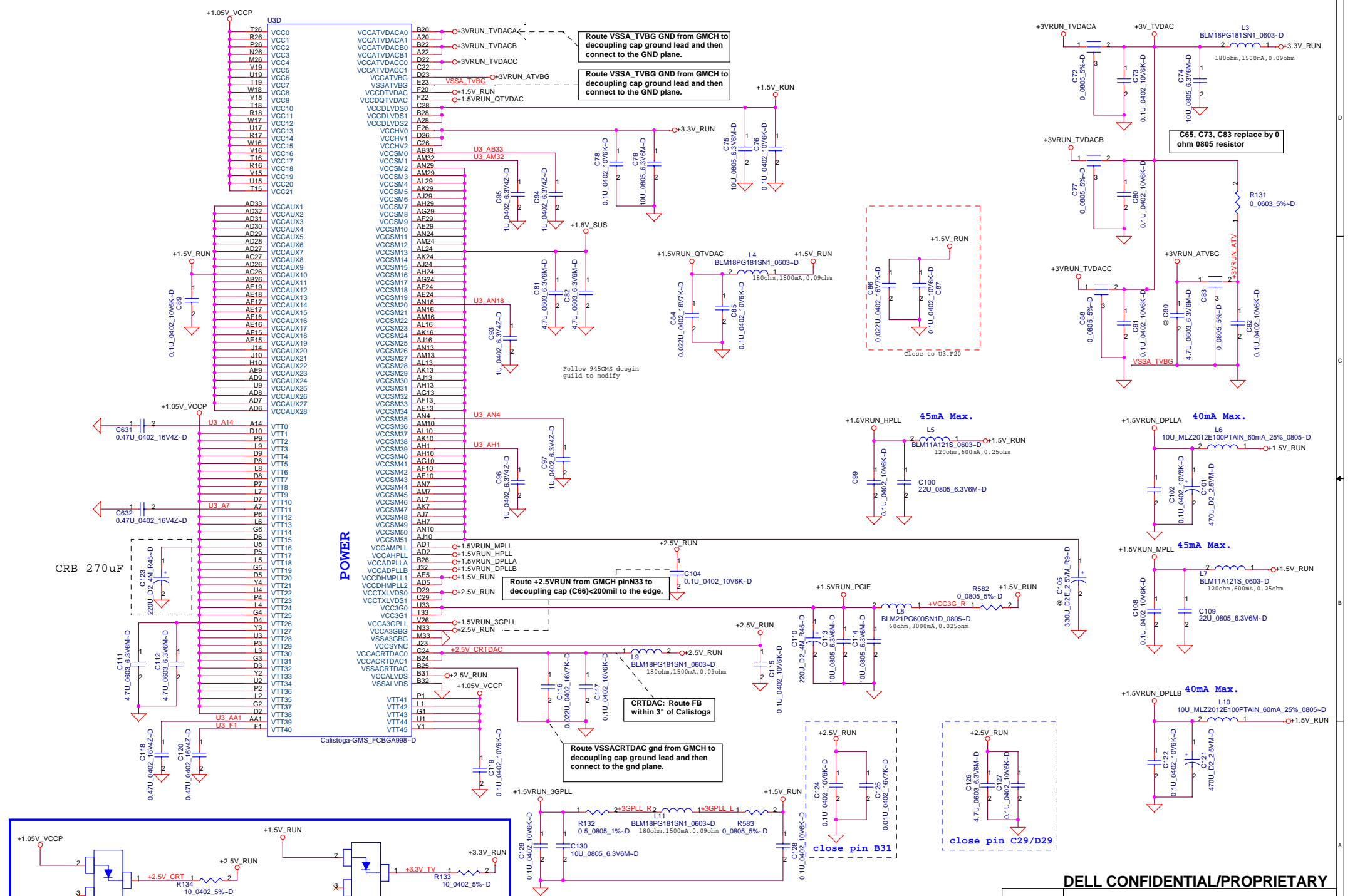
NC

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<p align="center">Calistoga (4 of 5)</p>		
<p>File</p>	<p>Document Number</p>	<p>Rev</p>
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Route VSSA_TVBG GND from GMCH to decoupling cap ground lead and then connect to the GND plane.

Route VSSA_TVBG GND from GMCH to decoupling cap ground lead and then connect to the GND plane.

Follow 945GMS design guid to modify

Route +2.5VRUN from GMCH pinN33 to decoupling cap (C66)-200mil to the edge.

Route VSSACTRDAC gnd from GMCH to decoupling cap ground lead and then connect to the gnd plane.

close pin B31

close pin C29/D29

C65, C73, C83 replace by 0 ohm 0805 resistor

CRB 270uF

CRT DAC Voltage Follower Circuit - 700mV

TV DAC Voltage Follower Circuit - 700mV

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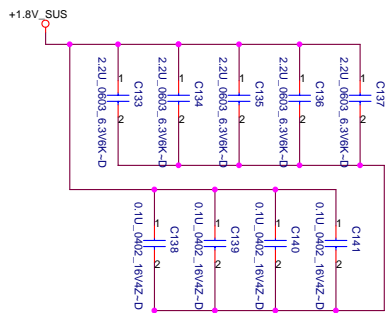
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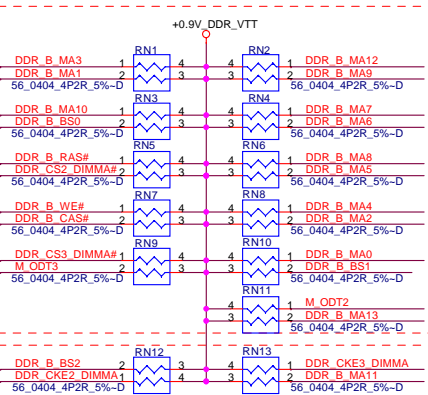
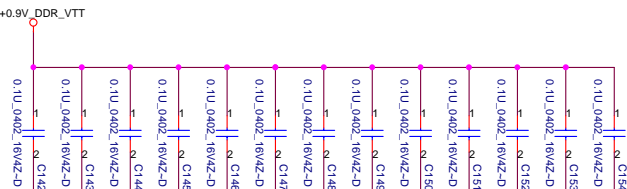
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<11,16> DDR_A_DQS#[0..7] <<>
 <11,16> DDR_A_D[0..63] <<>
 <11,16> DDR_A_DM[0..7] <<>
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 <1> DDR_B_MA[0..13] <<>

Layout Note:
Place near JDIM1



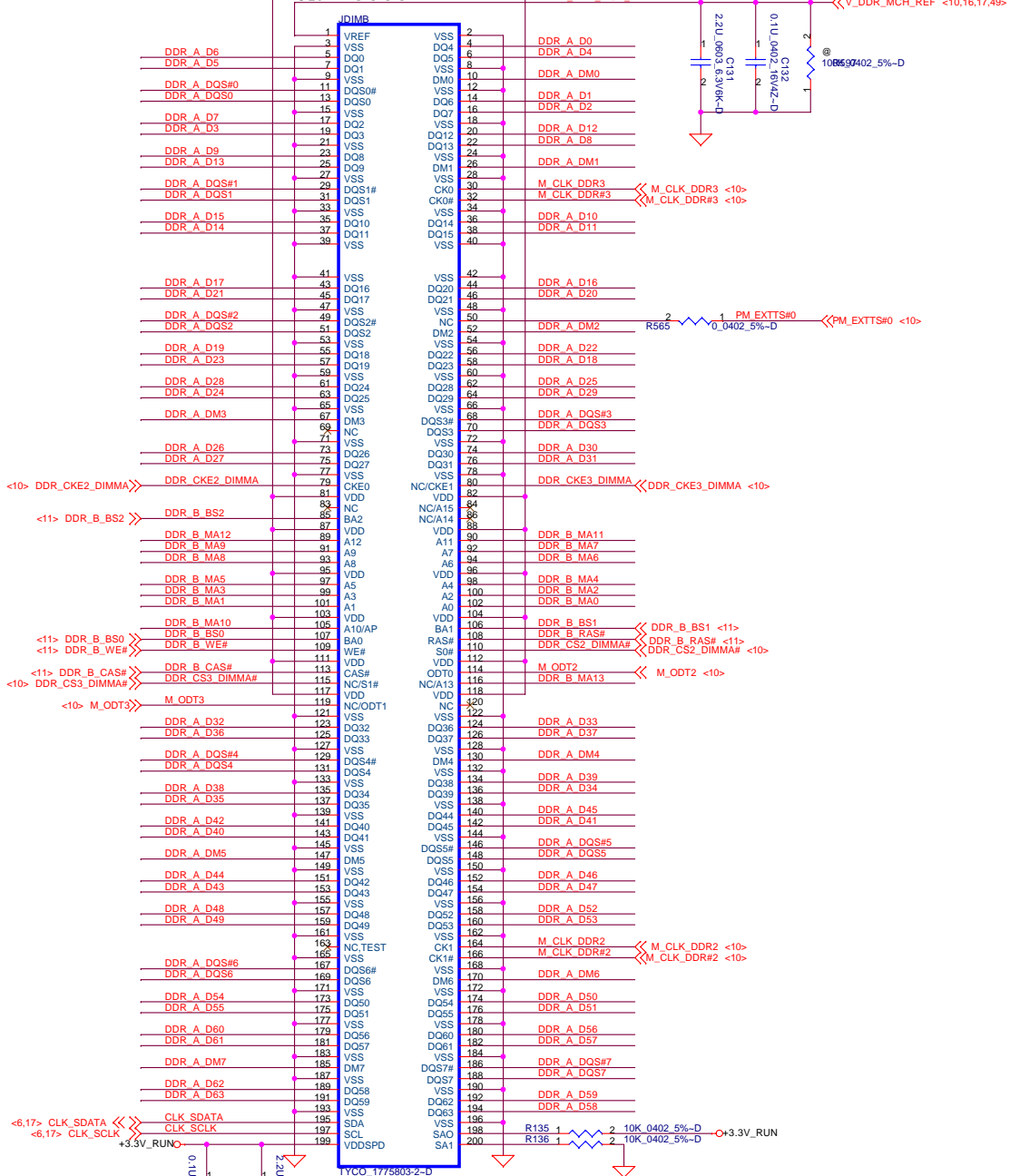
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V_DDR_VTT



Layout Note:
Place these resistor closely DIM0, all trace length < 750 mil

Layout Note:
Place these resistor closely DIM0, all trace length Max=1.3"

ON Bottom SIDE



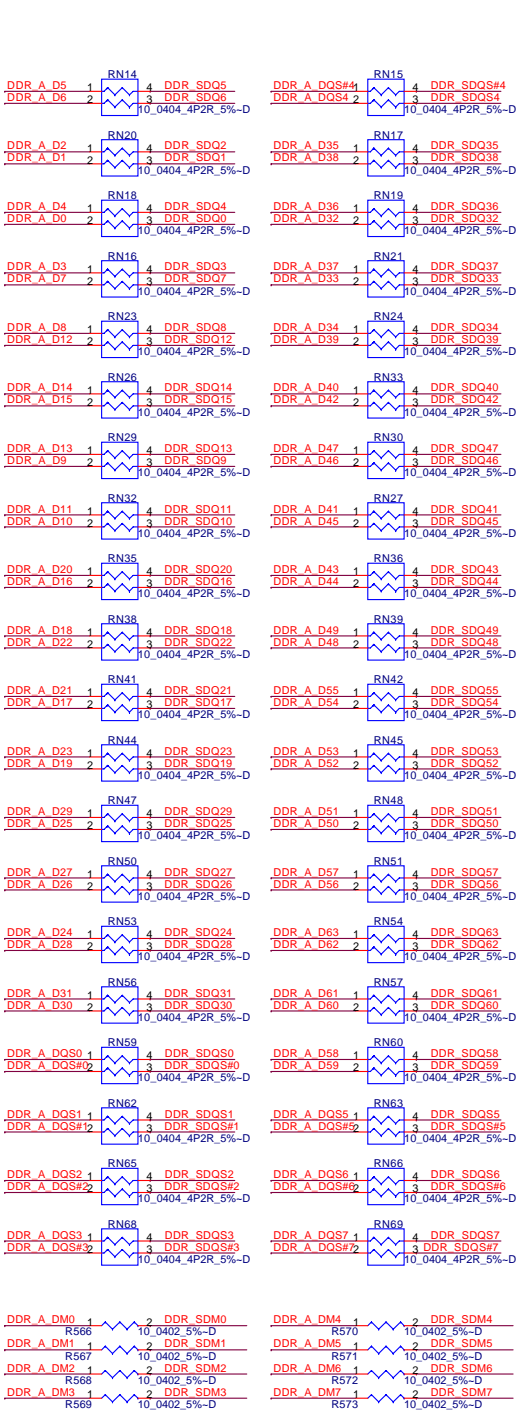
DIMMA STANDARD

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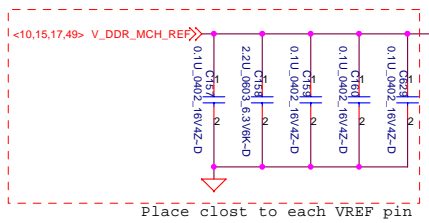


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DDRII-SODIMM SLOT1
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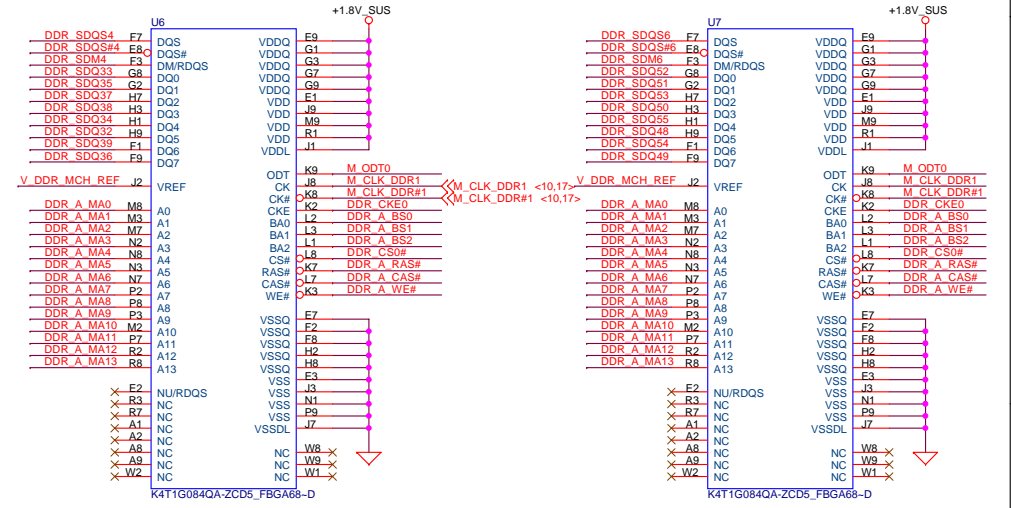
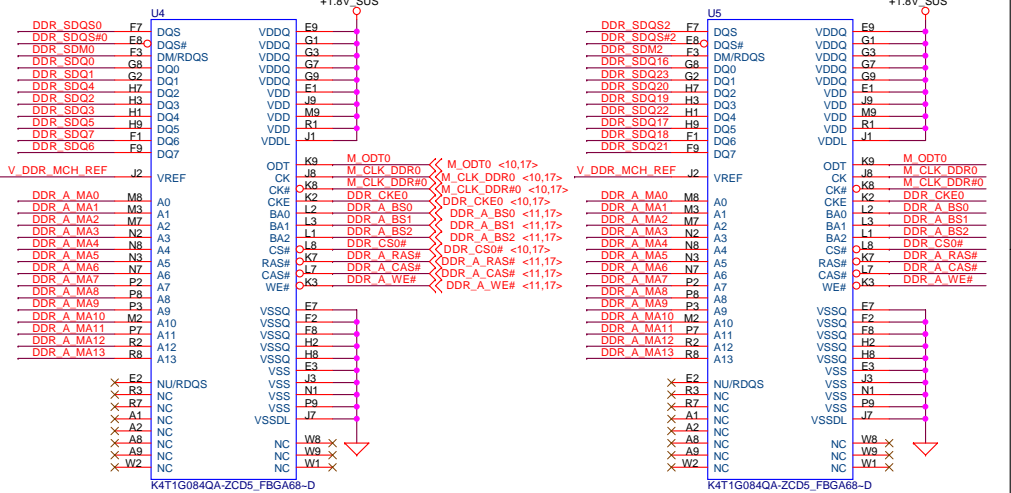
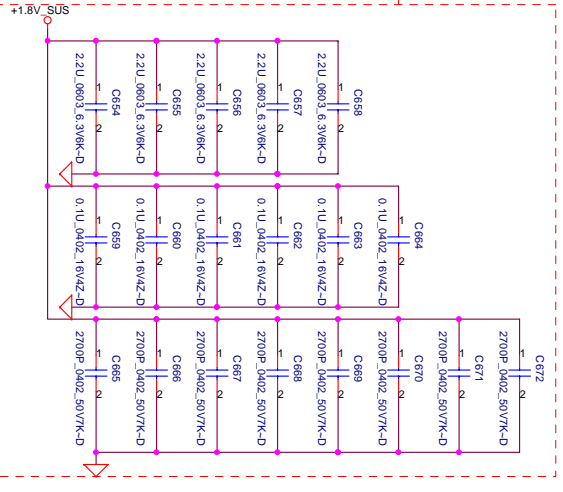
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 <11,15> DDR_A_D[0.63] <<>
 <11,15> DDR_A_DM[0.7] <<>
 <11,15> DDR_A_DQS[0.7K] <<>
 <17> DDR_SQS#0.7K] <<>
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 <17> DDR_SQ[0.63] <<>
 <17> DDR_SDM[0.7] <<>



Layout Note:
Place near U4,U5,U6,U7



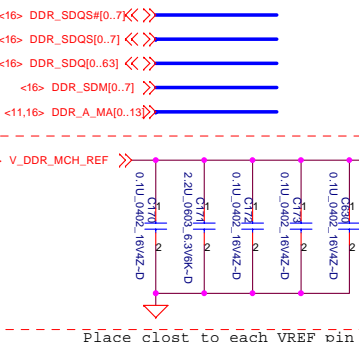
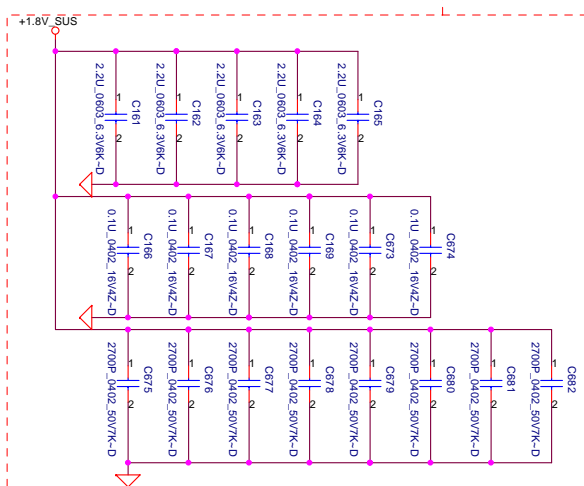
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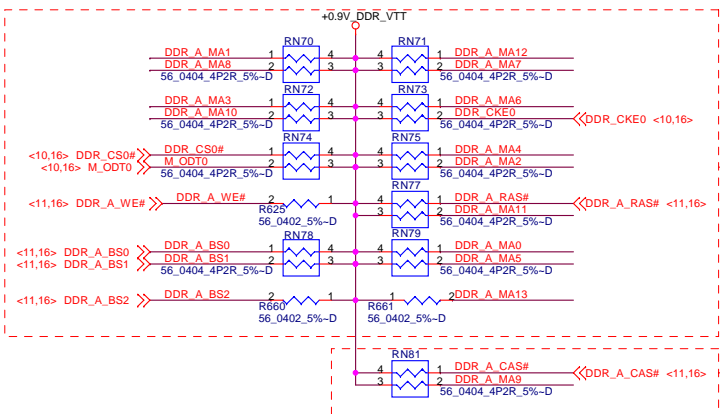
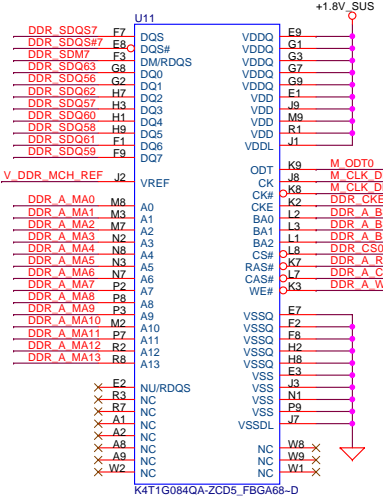
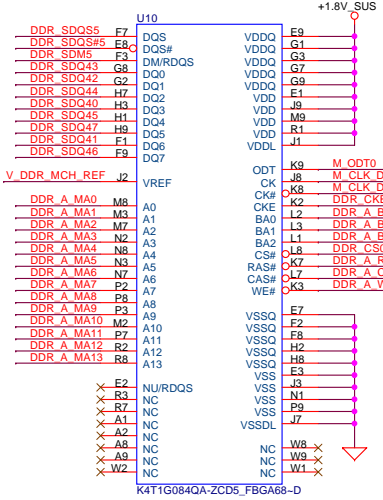
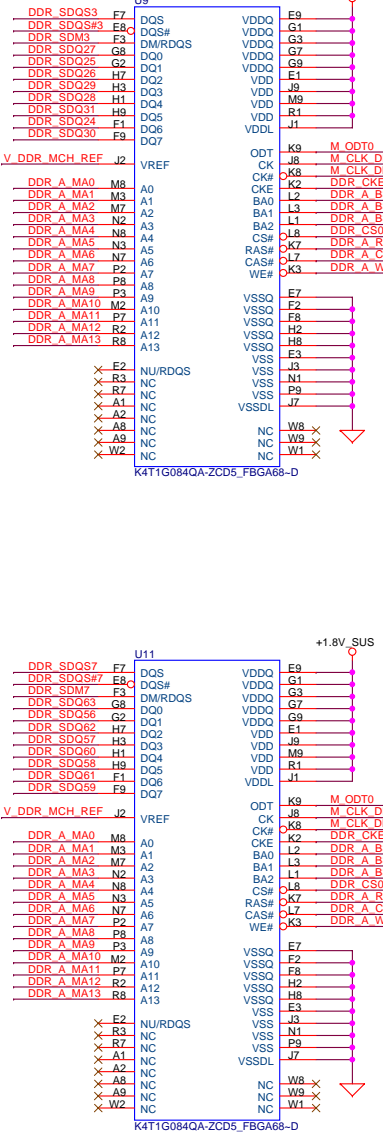
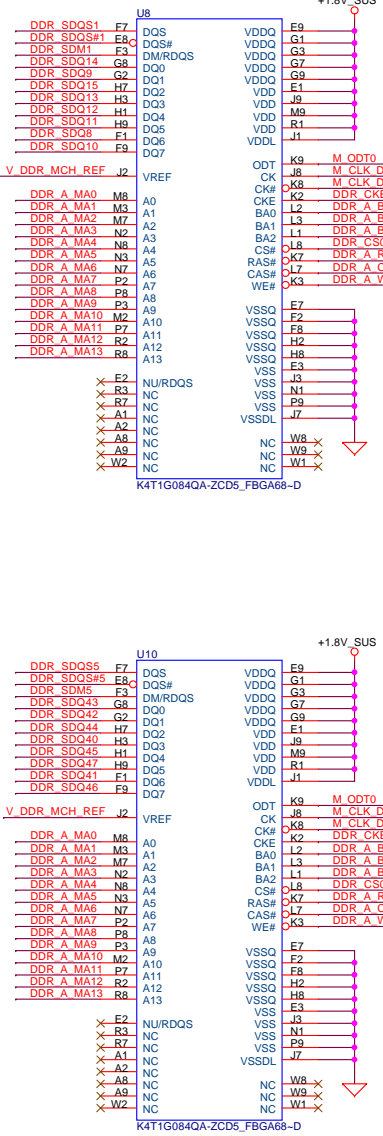
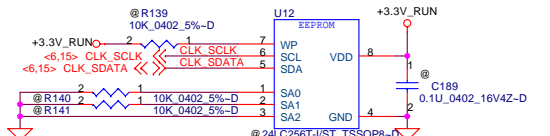
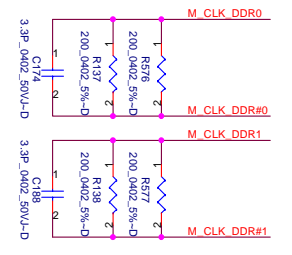
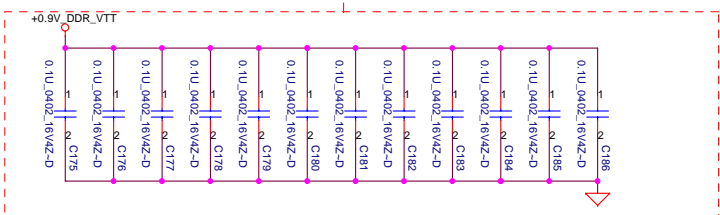
Compal Electronics, Inc.		
DDR1-ON BOARD I		
File	Document Number	Rev
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Layout Note:
Place near U8,U9,U10,U11



Place closest to each VREF pin

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V_DDR_VTT



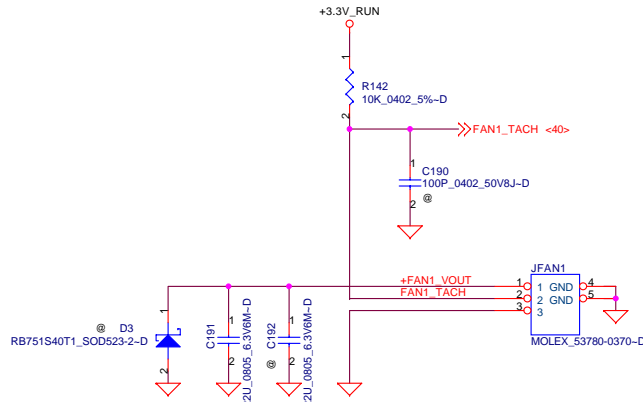
Layout Note:
Place these resistor closely DIMM0, all trace length < 750 mil

Layout Note:
Place these resistor closely DIMM0, all trace length Max=1.3"

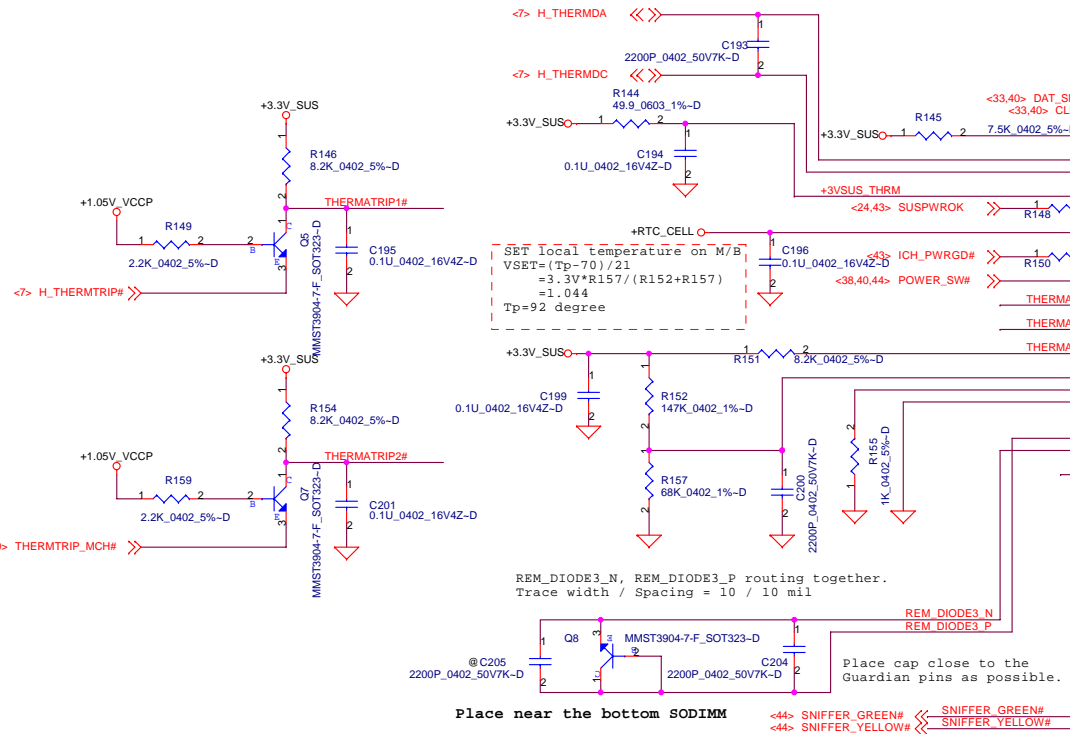
Compal Electronics, Inc.
Title: **DDRII-ON BOARD II**
Size: Document Number **LA-3741P** Rev 0.1
Date: Friday, January 26, 2007 Sheet 17 of 53

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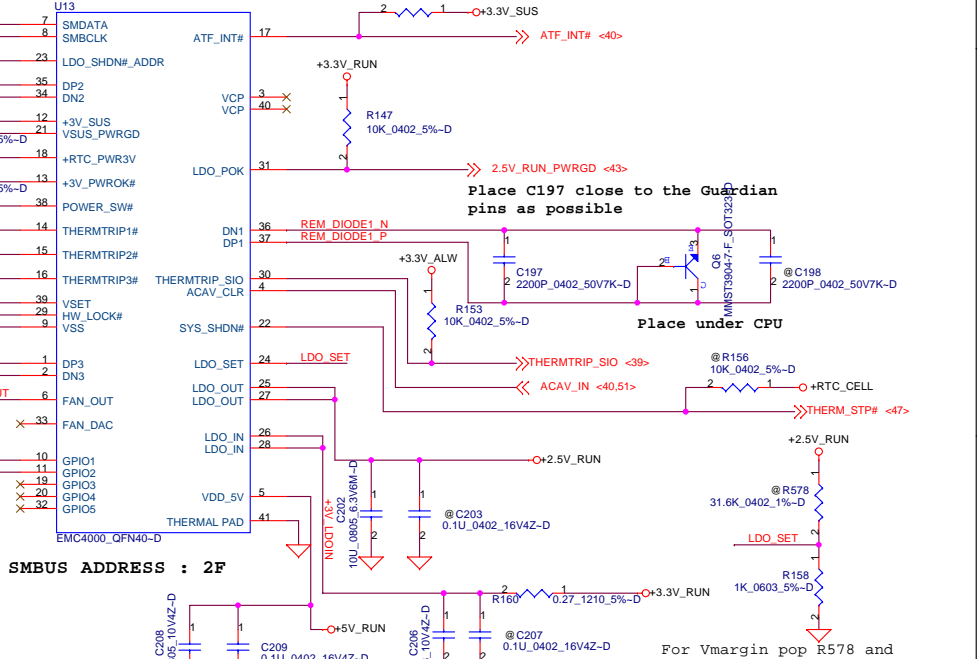
FAN1 Control and Tachometer



Place C341 close to the Guardian pins as possible



Use Rev:C
Need create P/N



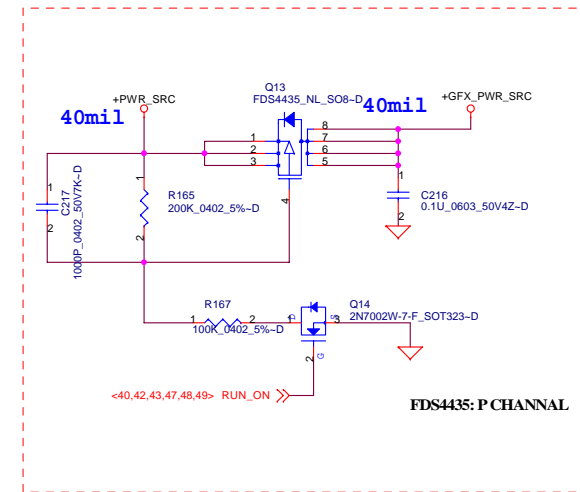
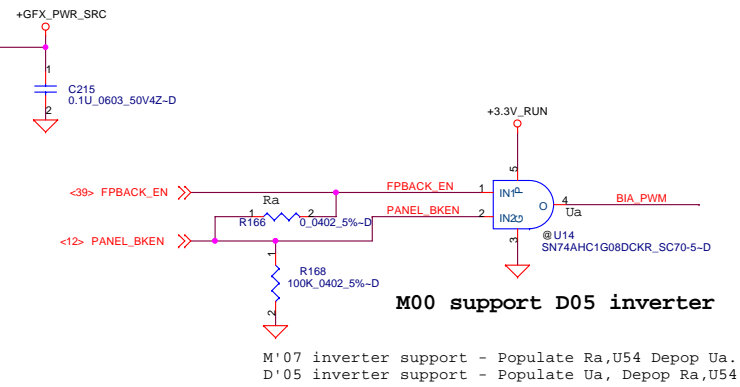
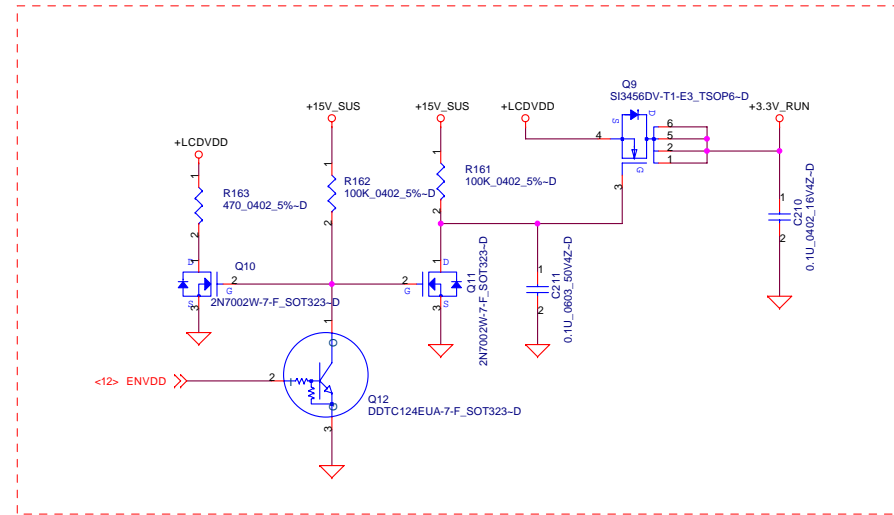
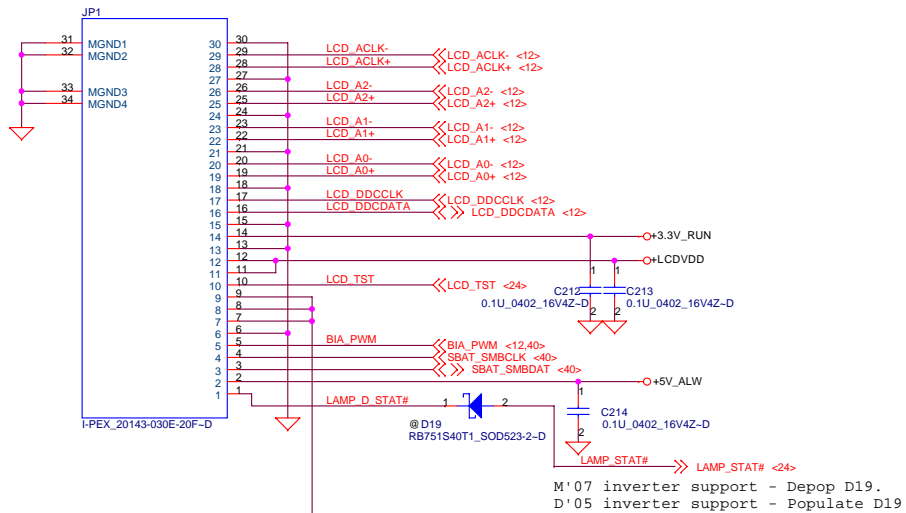
SMBUS ADDRESS : 2F

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Compal Electronics, Inc.		
Title FAN & Thermal Sensor		
Size	Document Number LA-3741P	Rev 0.1
Date	Friday, January 26, 2007	Sheet 18 of 53



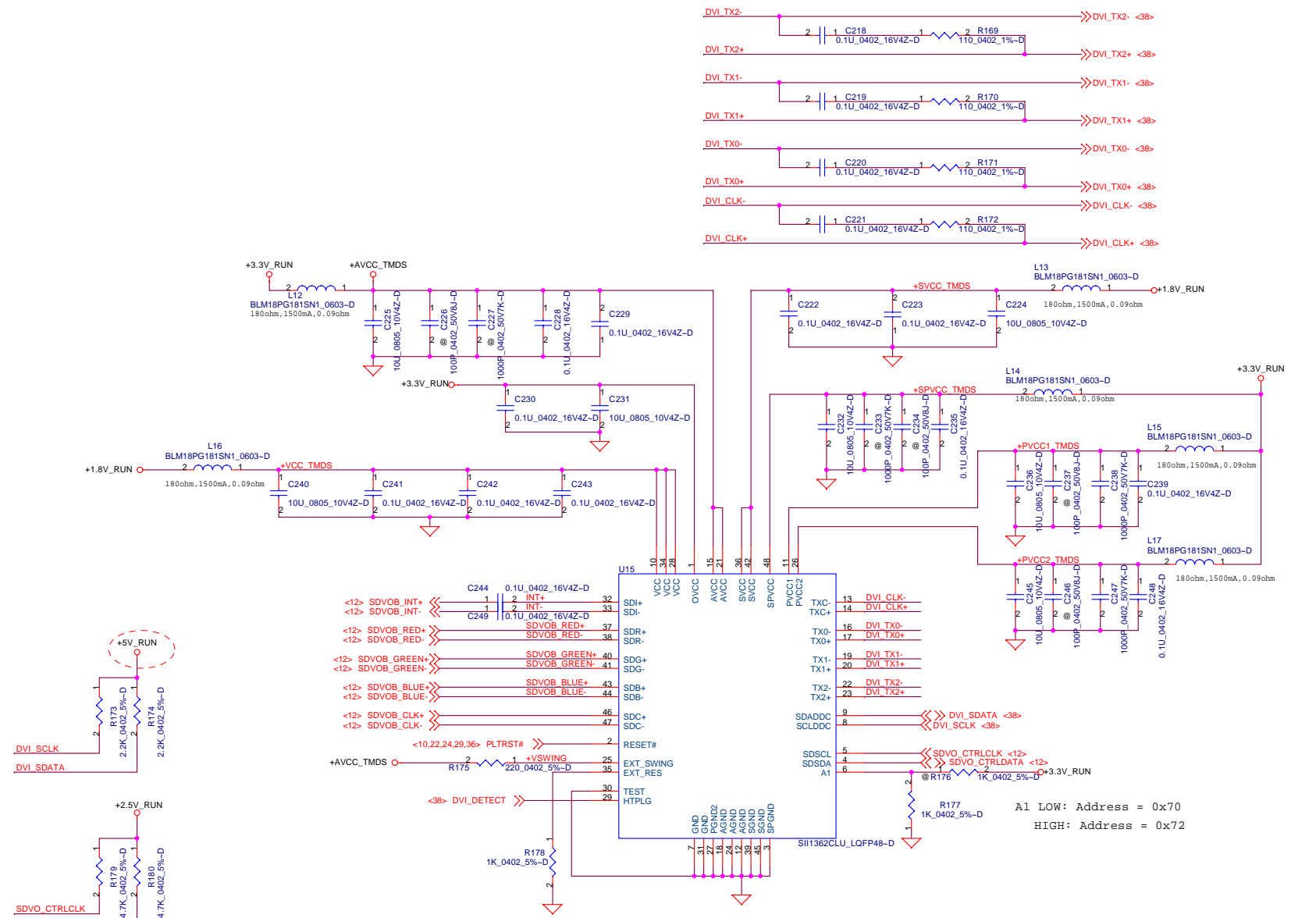
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Compal Electronics, Inc.

Title		
Internal LVDS		
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Date:	Friday, January 26, 2007	Sheet 19 of 53



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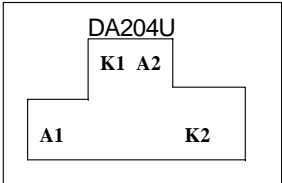
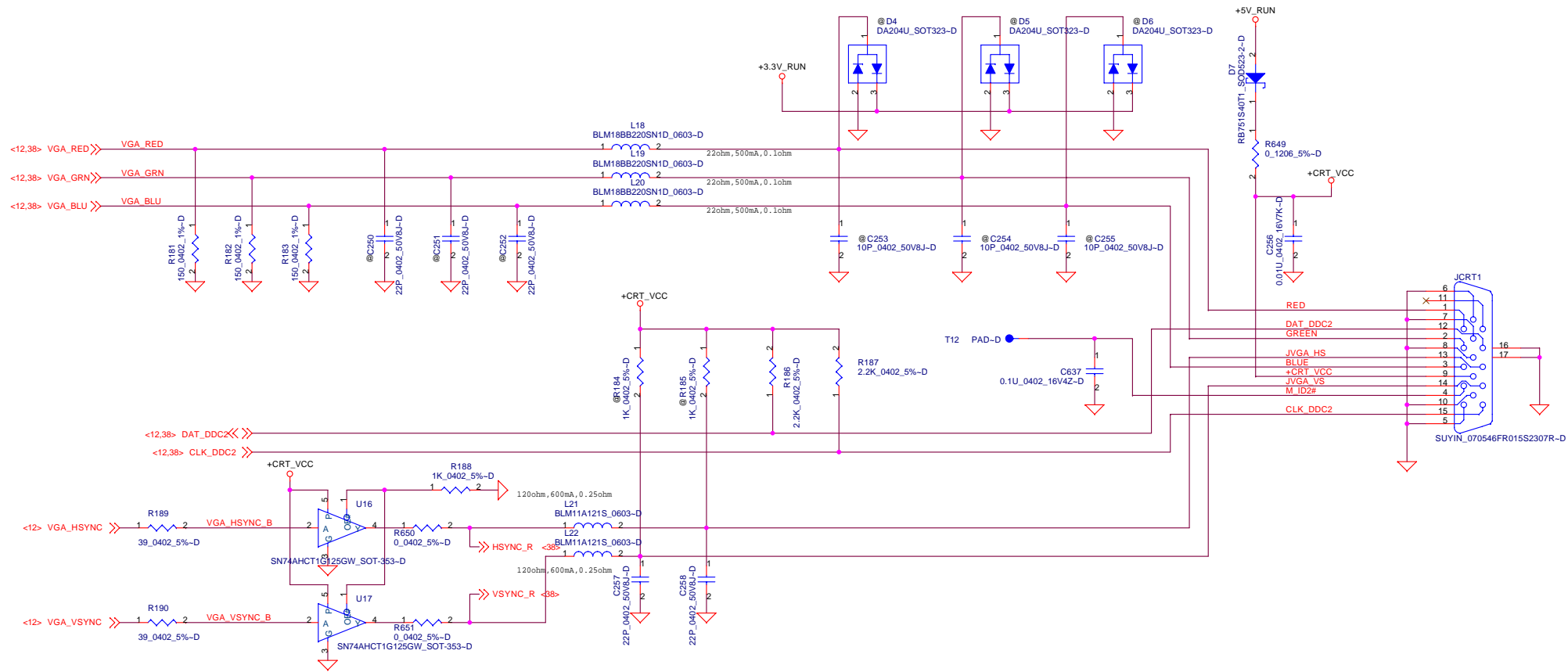


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Compal Electronics, Inc.

Internal LVDS

LA-3741P



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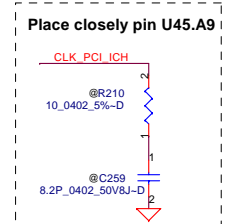
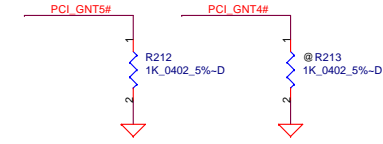
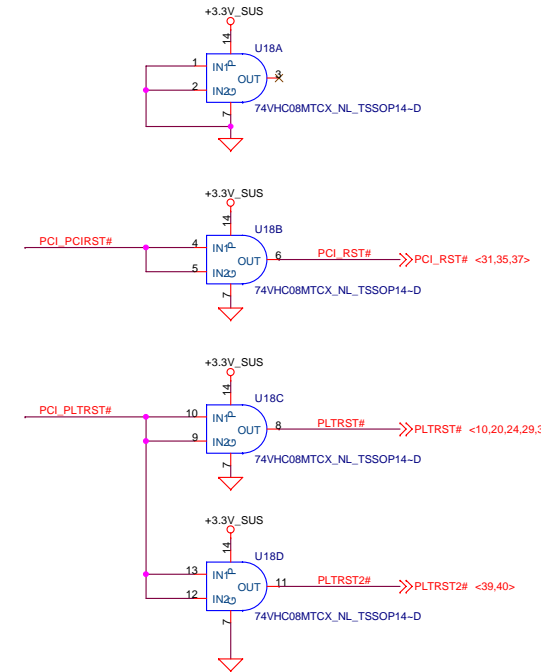
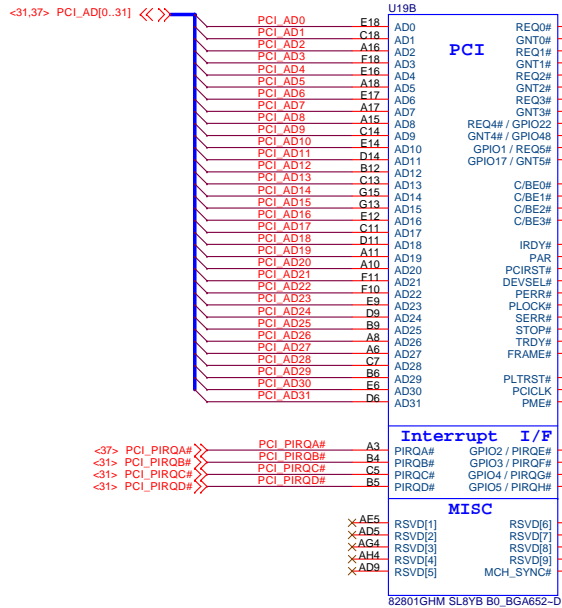
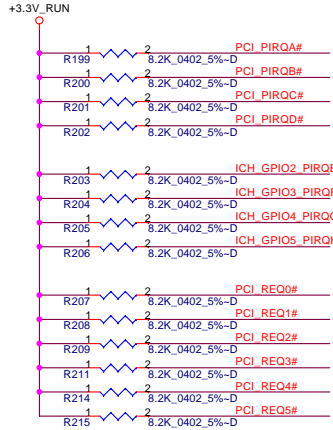
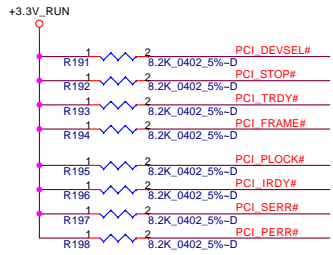
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Compal Electronics, Inc.

CRT Connector

LA-3741P

Title	CRT Connector		Rev	0.1
Size	Document Number			
Date:	Friday, January 26, 2007	Sheet	21	of 53



	GNT5# R214	GNT4# R213
LPC (11)	unstuff	unstuff
PCI (10)	unstuff	stuff
SPI (01)	stuff	unstuff

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Compal Electronics, Inc.

Title: ICH7(1/4)

Size: Document Number

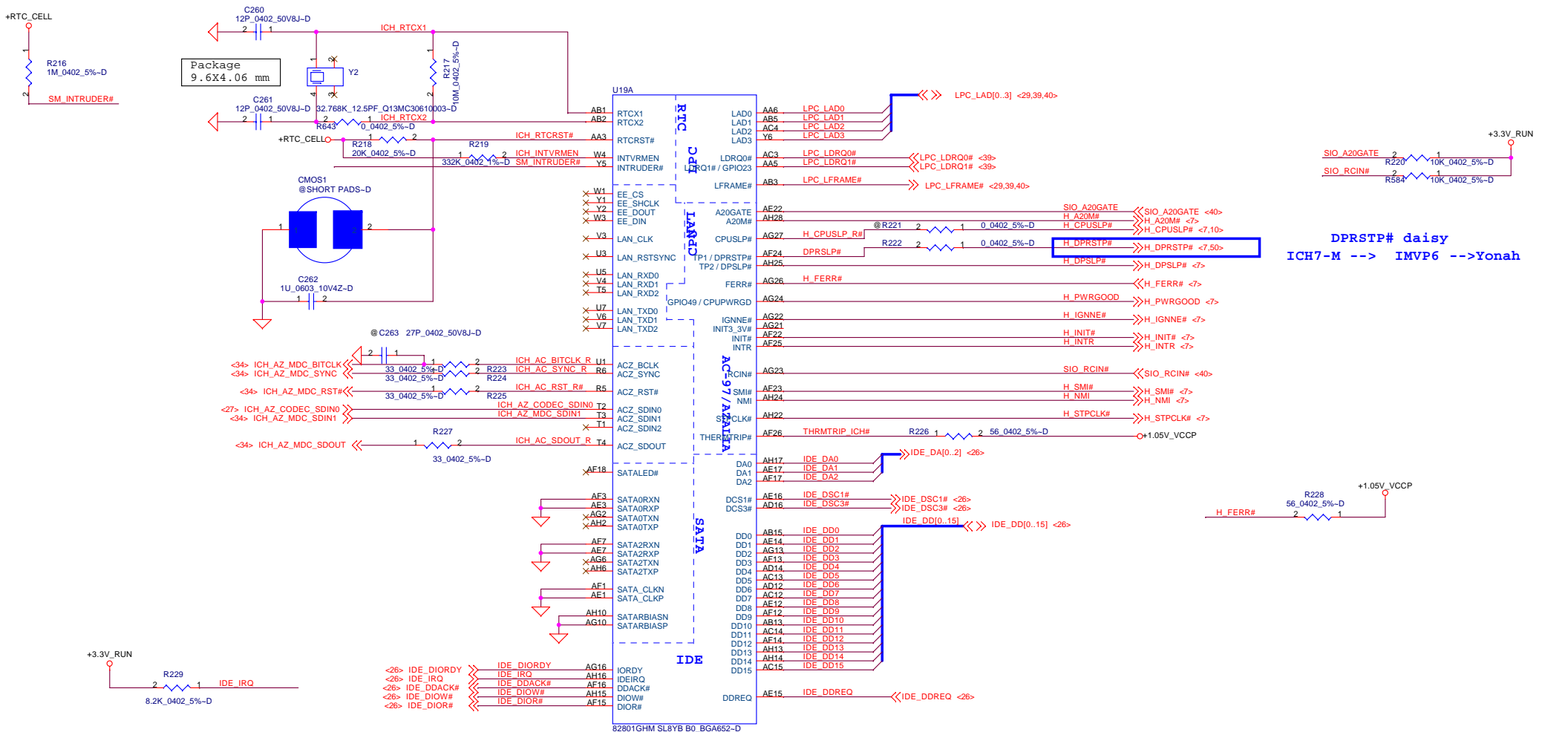
Date: Friday, January 26, 2007

Sheet: 22 of 53

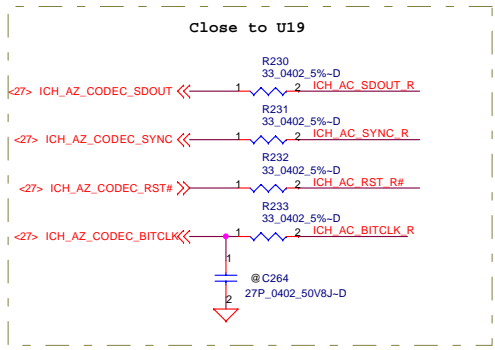
Rev: 0.1

LA-3741P

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DPRSTP# daisy
 ICH7-M --> IMVP6 --> Yonah



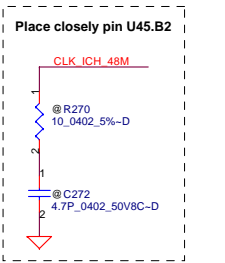
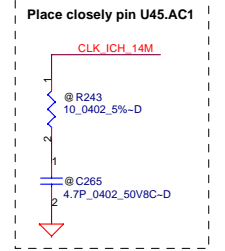
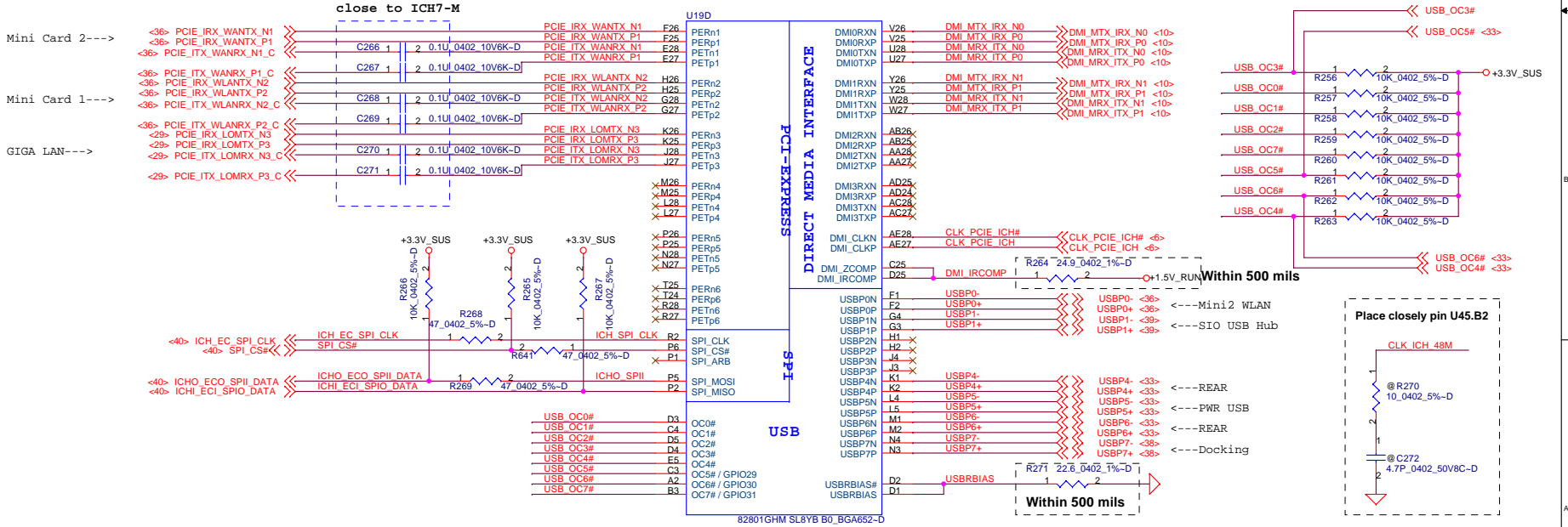
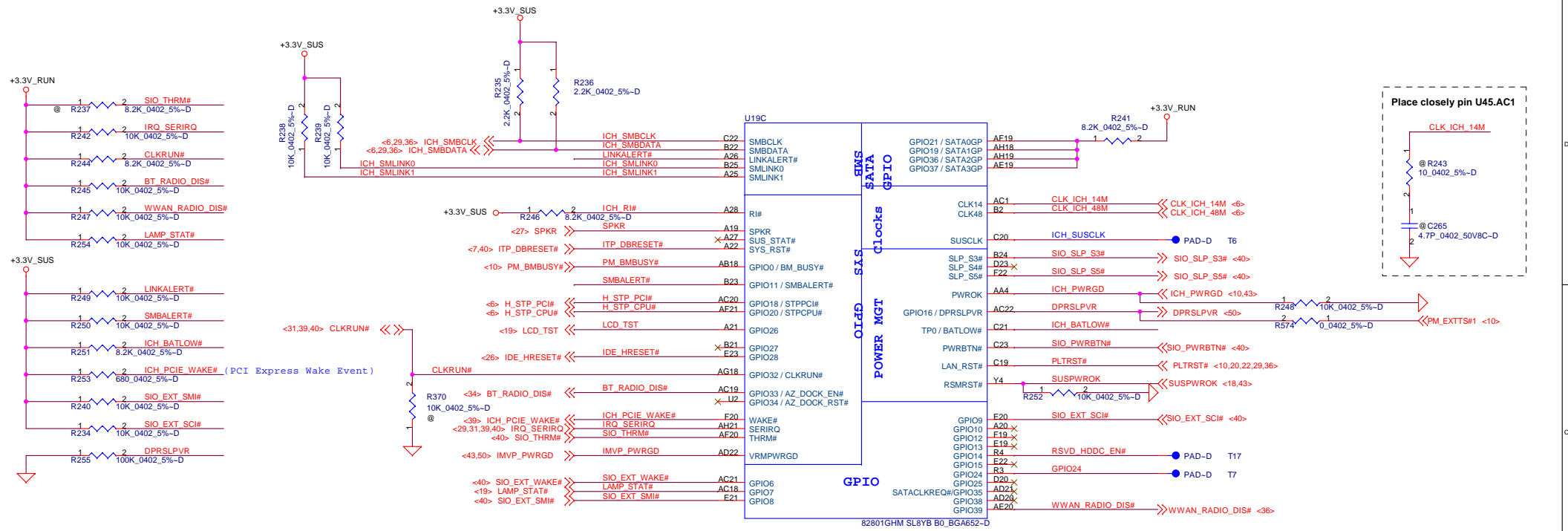
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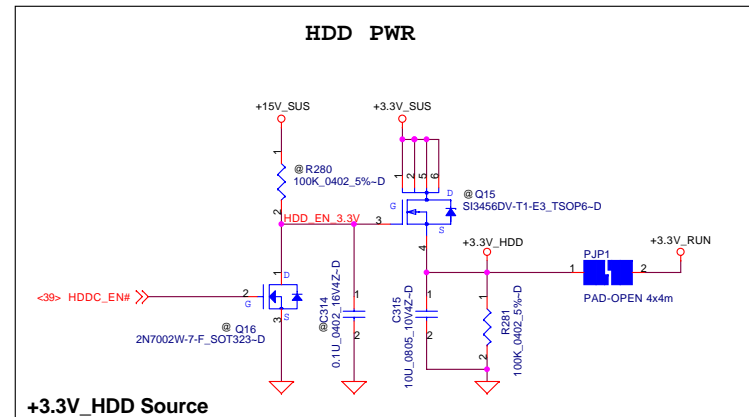
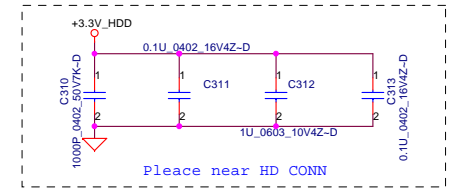
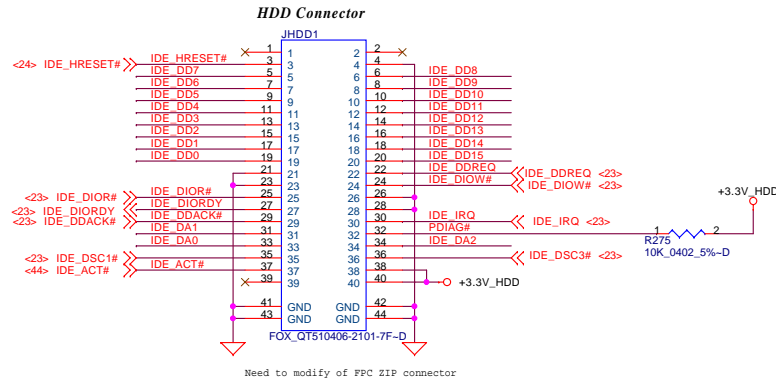
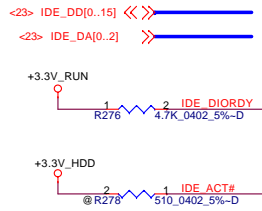
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Size	Document Number LA-3741P	Rev 0.1
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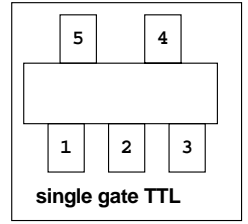
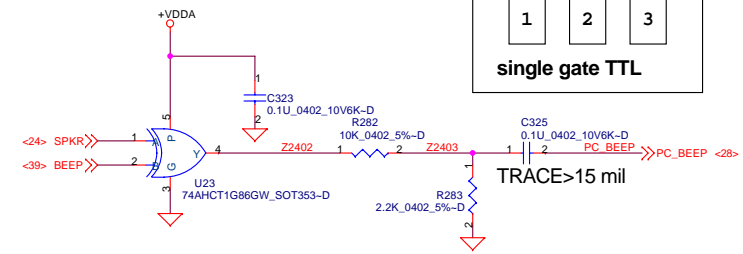
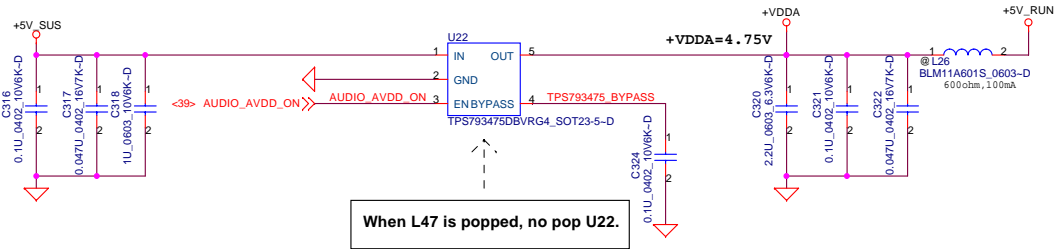
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 ICH7(3/4)
 LA-3741P
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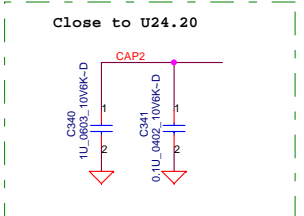
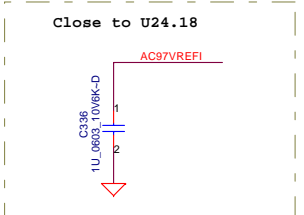
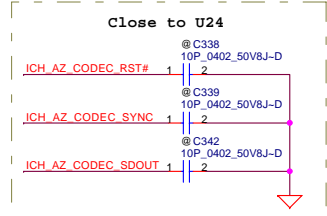
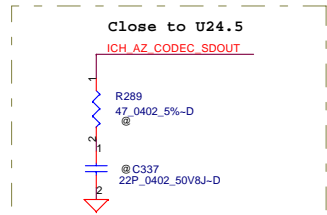
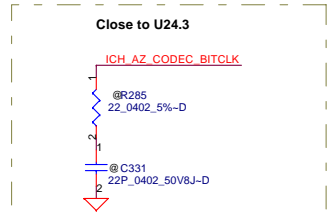
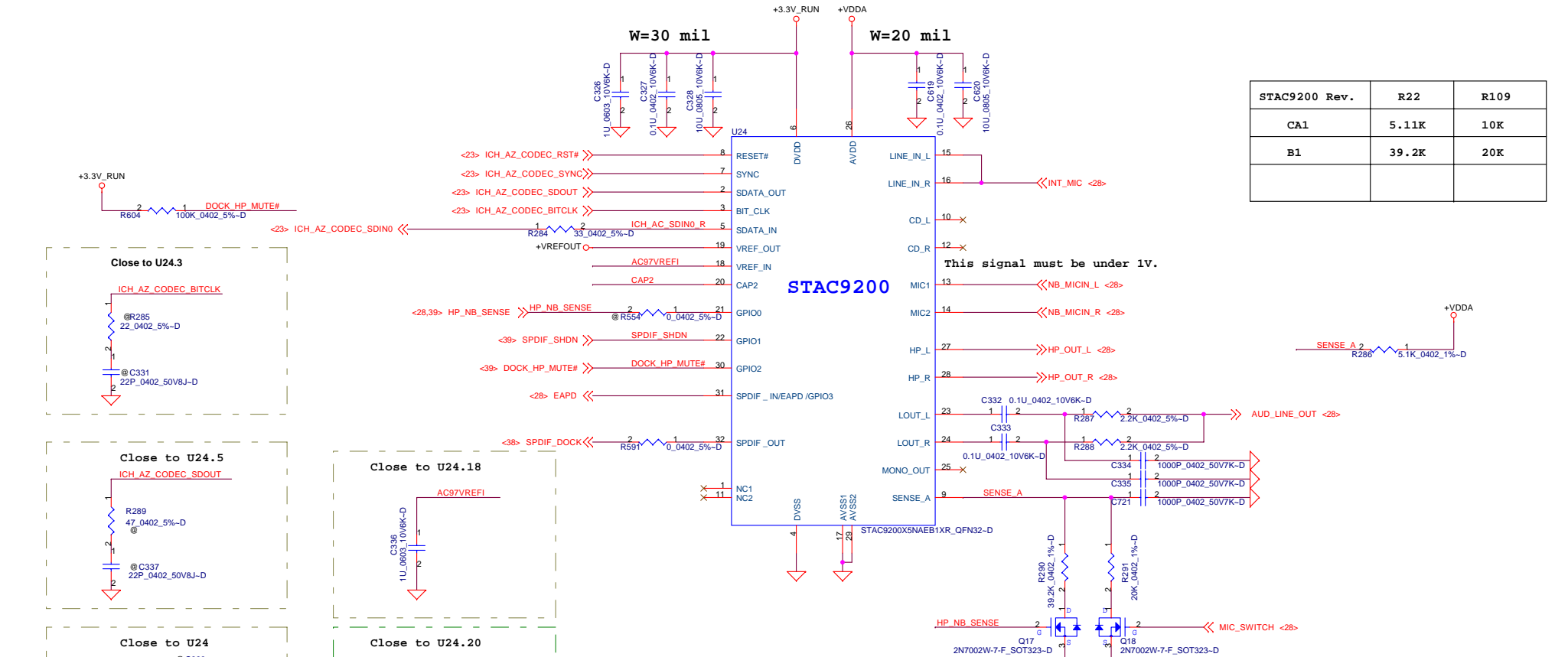


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Title IDE HDD Connector			
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STAC9200 Rev.	R22	R109
CA1	5.11K	10K
B1	39.2K	20K



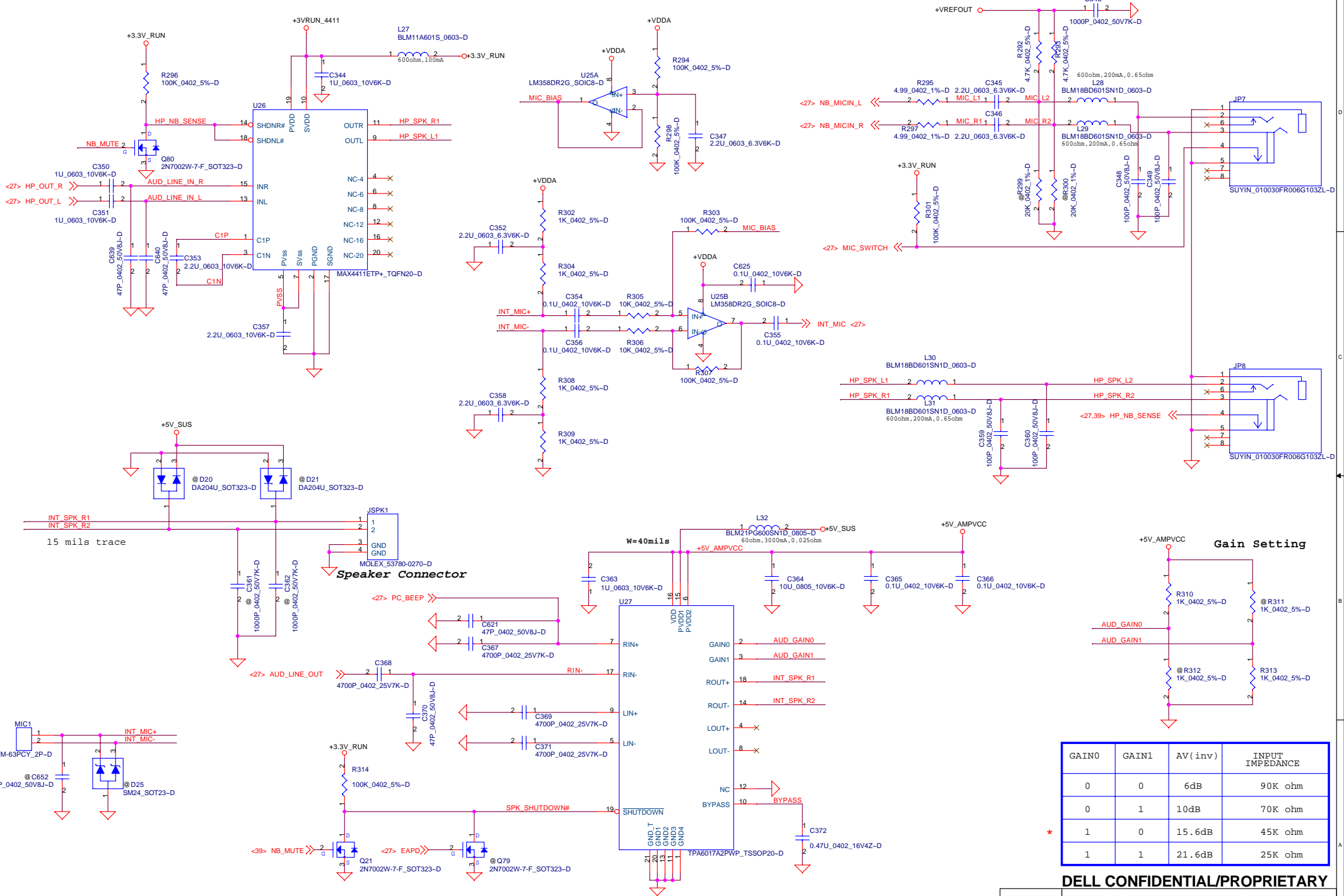
Note: C336, C340, C341, C326, C327, C328, C619, C620 use Temp. characteristics: X5R
Operating range: -55~+85degree

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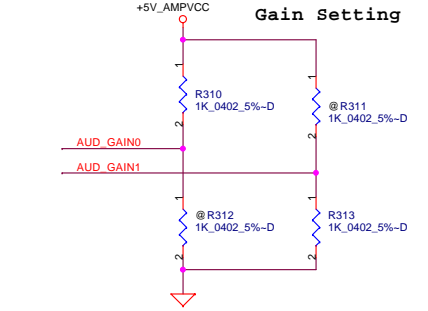
Compal Electronics, Inc.		
Azalia (HD) Codec		
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Date: Friday, January 26, 2007	Sheet 27 of 53	Rev 0.1

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Note:
 C343, C344, C345, C346, C350, C351, C353, C354, C355, C356, C357 use
 Temp. characteristics: X5R
 Operating range: -55~+85degree

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GAIN0	GAIN1	AV (inv)	INPUT IMPEDANCE
0	0	6dB	90K ohm
0	1	10dB	70K ohm
1	0	15.6dB	45K ohm
1	1	21.6dB	25K ohm

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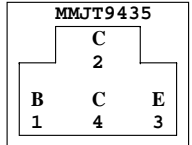
Compal Electronics, Inc.

AMP and PHONE JACK

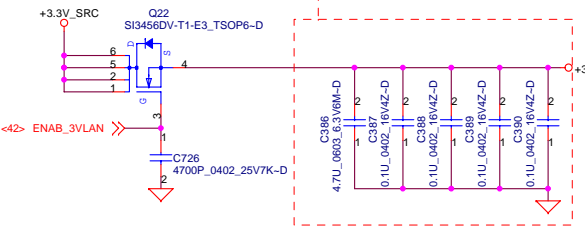
LA-3741P

File	Document Number	Rev
Date: Friday, January 26, 2007	Sheet 28 of 53	0.1

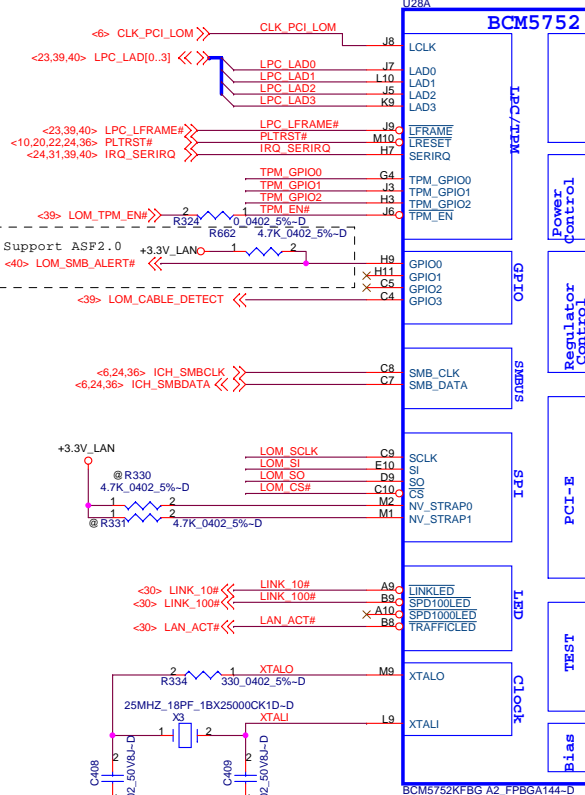
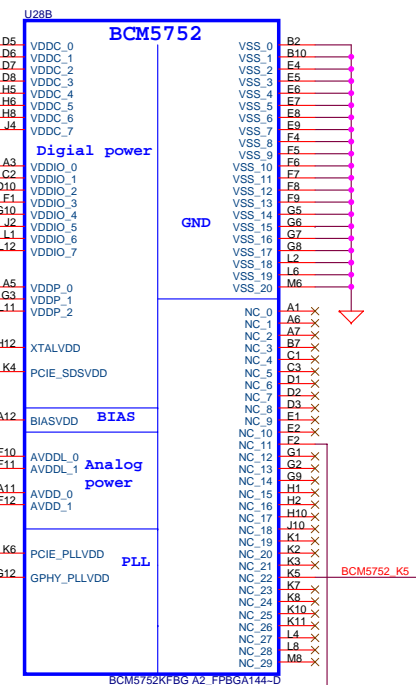
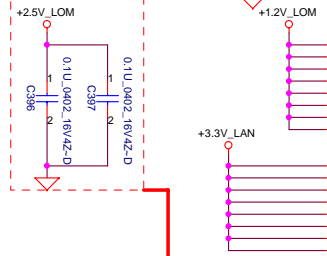
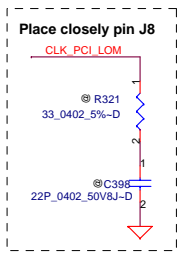
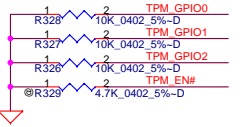
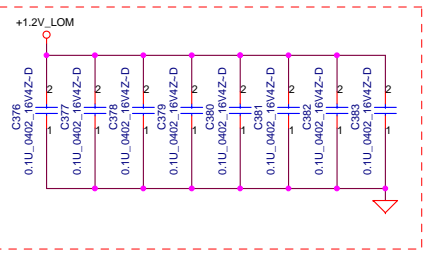
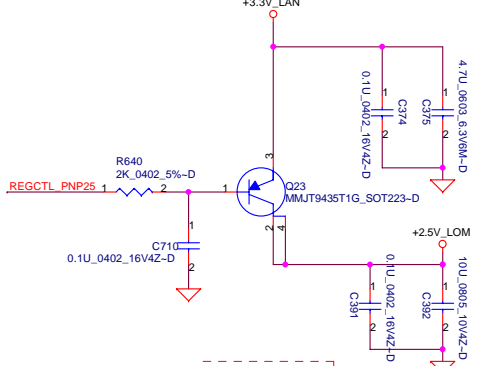
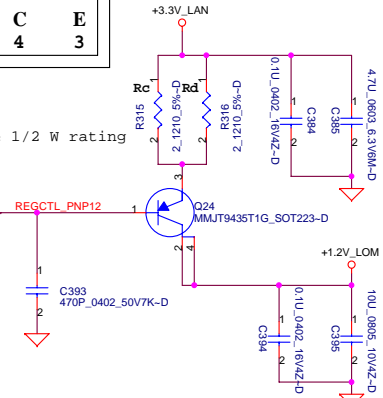
Layout Notice : Place as close chip as possible.



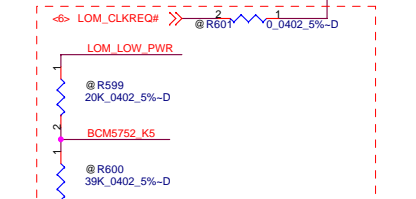
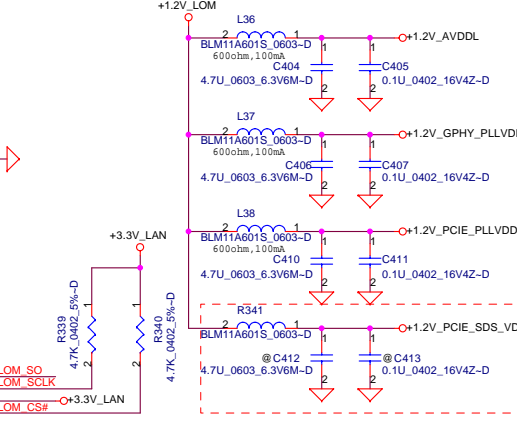
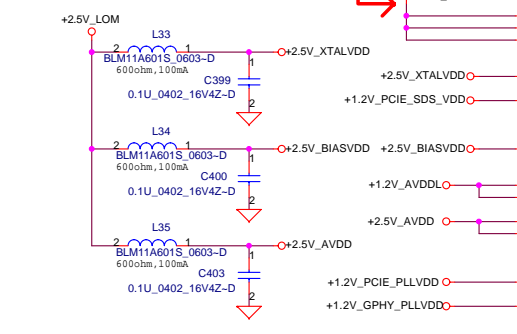
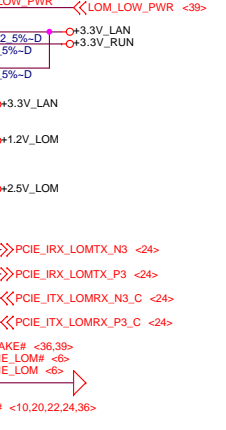
Layout Notice : 1.2V filter. Place as close chip as possible.



Rc, Rd are 1/2 W rating



Layout Notice : No high speed signal should be routed near RDAC or on adjacent layer to RDAC



Follow Travis to add that Broadcom will update for next version.
Follow M07 schematic
Pop R341 to use BLM11A601S if noise margin on SDSVDD so that pop C412, C413

	NV_STRAP1	NV_STRAP0	SO	SI	CS#	SCLK
Atmel AT45BCM021B	0	0	1	0	1	1
ST M45PE20	0	1	1	0	0	1

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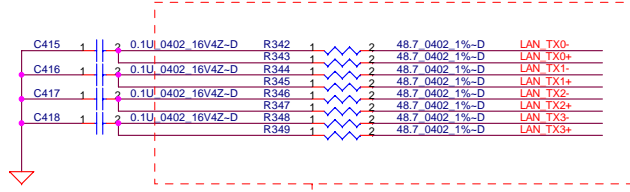


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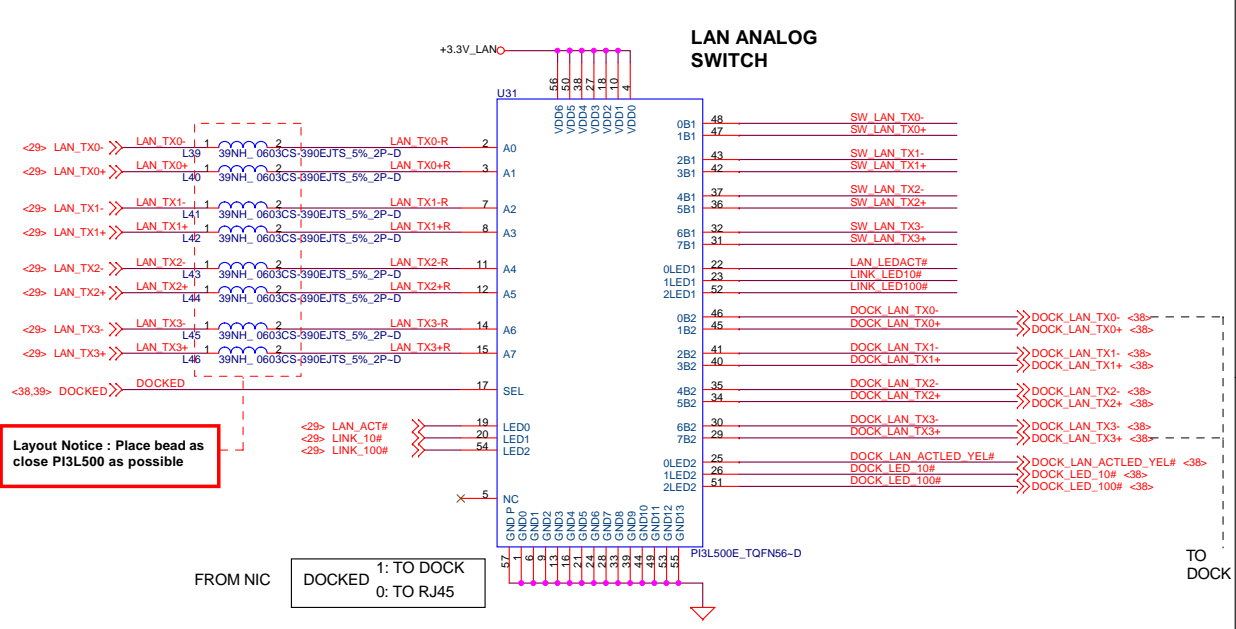
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Size: Document Number **LA-3741P**

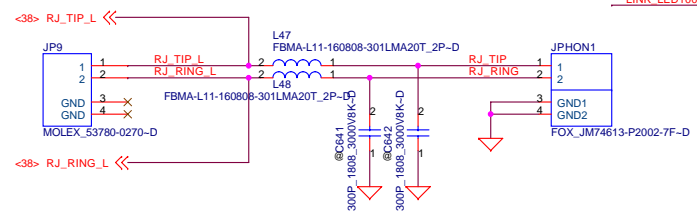
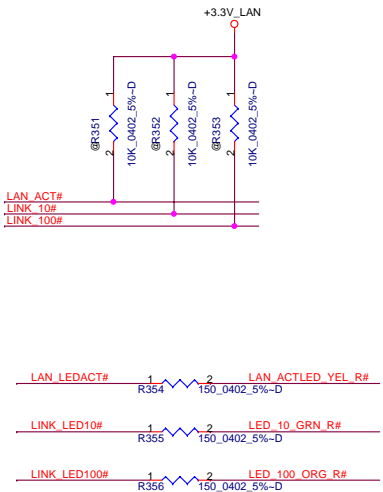
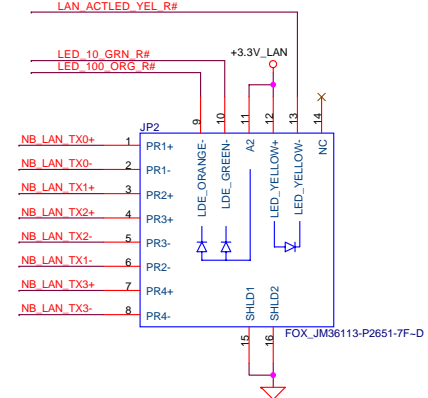
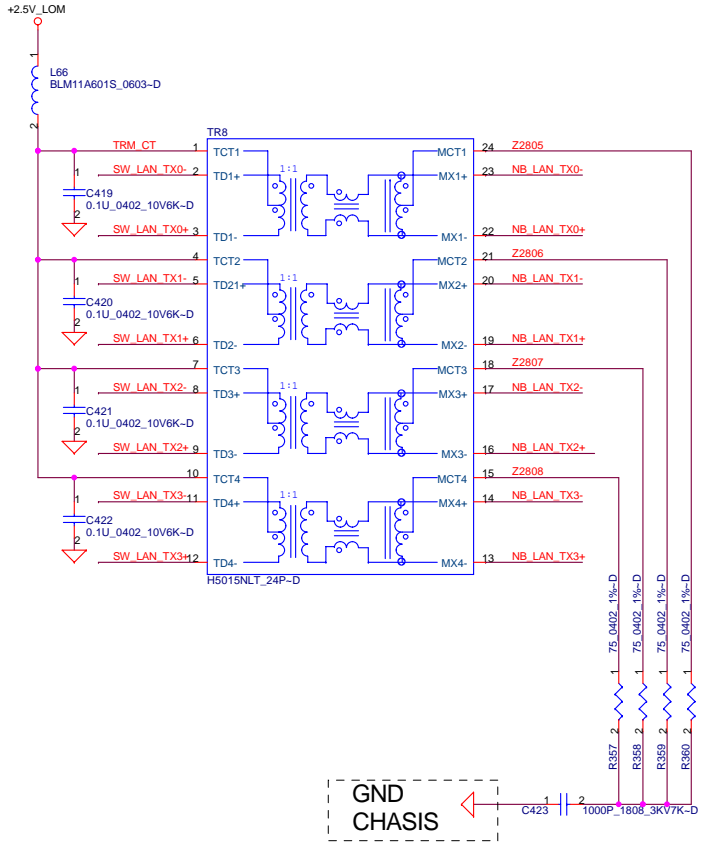
Date: Friday, January 26, 2007 Sheet 29 of 33



Layout Notice : Place termination as close as ASIC as possible
The resistors need at least 1/16W



Layout Notice : Place bead as close PI3L500 as possible



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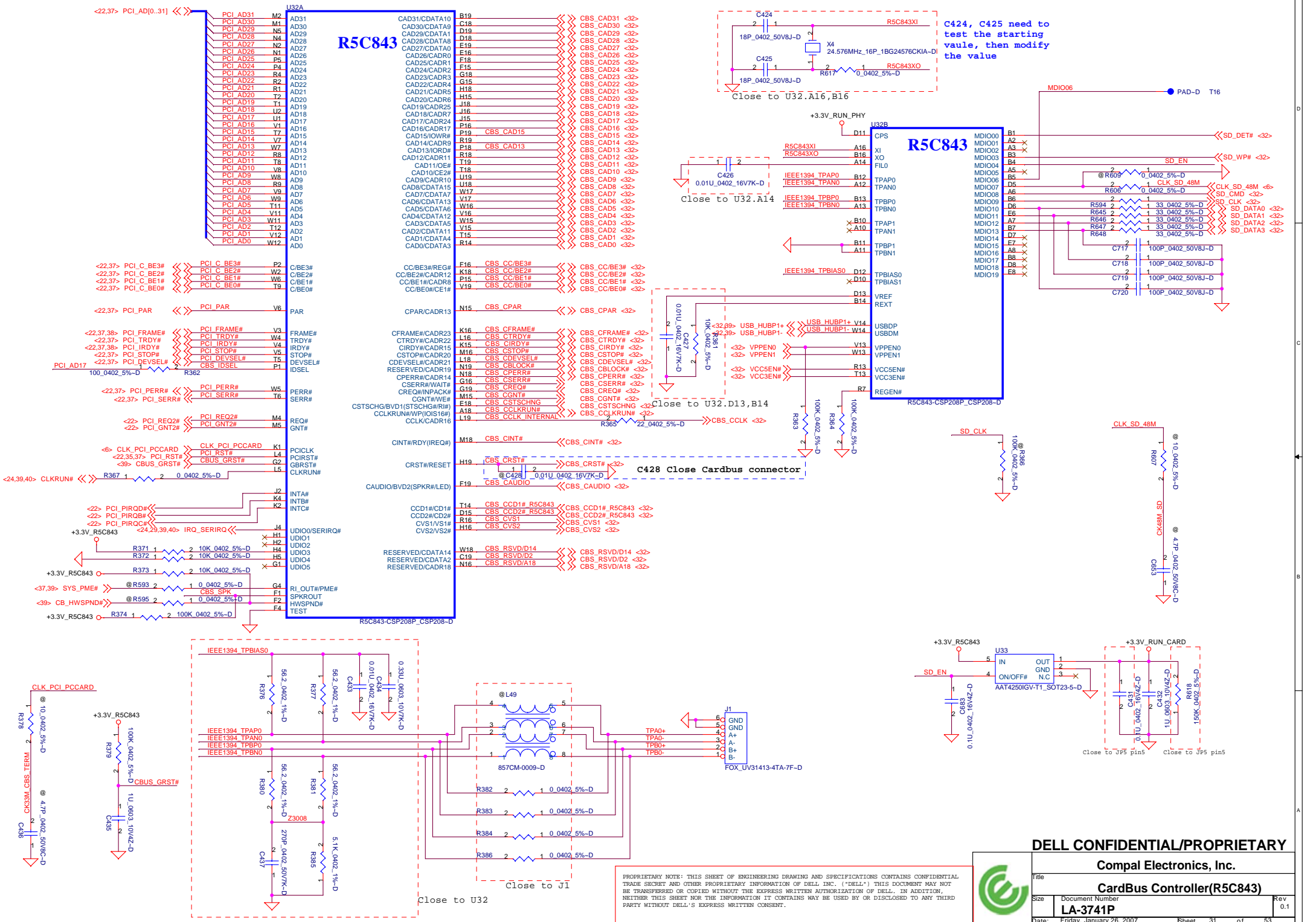
Title: **LAN TRANSFORMER**

Size: Document Number

Rev: 0.1

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Date: Friday, January 26, 2007 Sheet 30 of 33



C424, C425 need to test the starting value, then modify the value

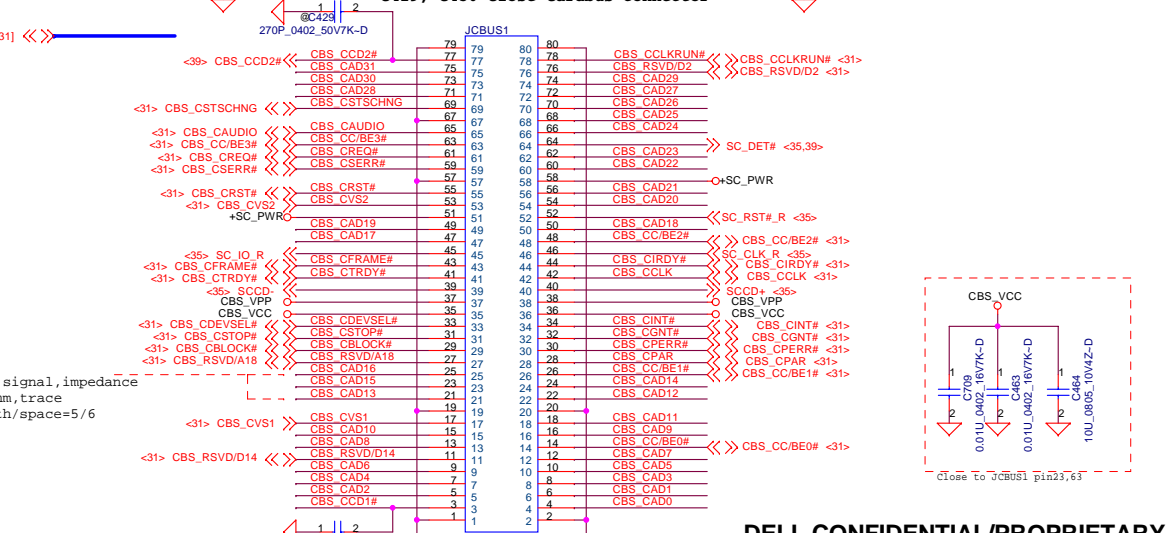
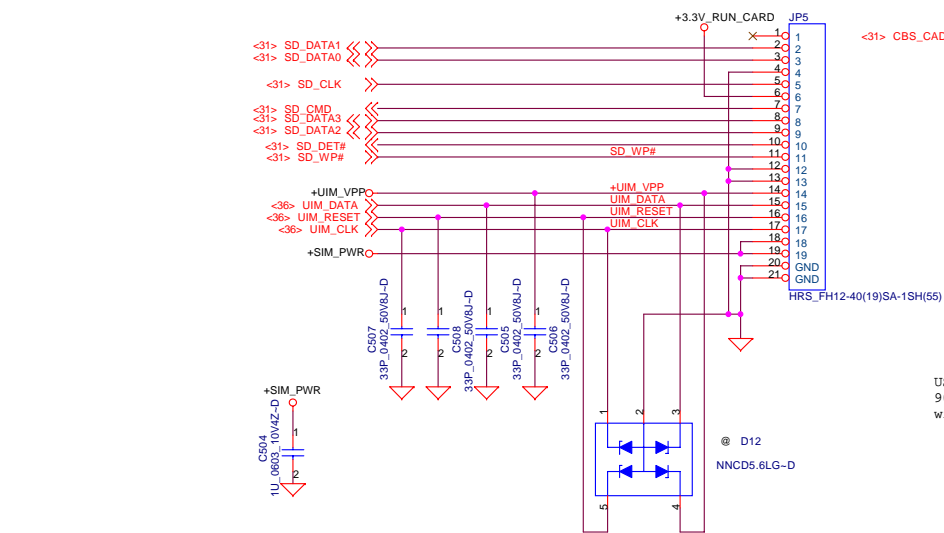
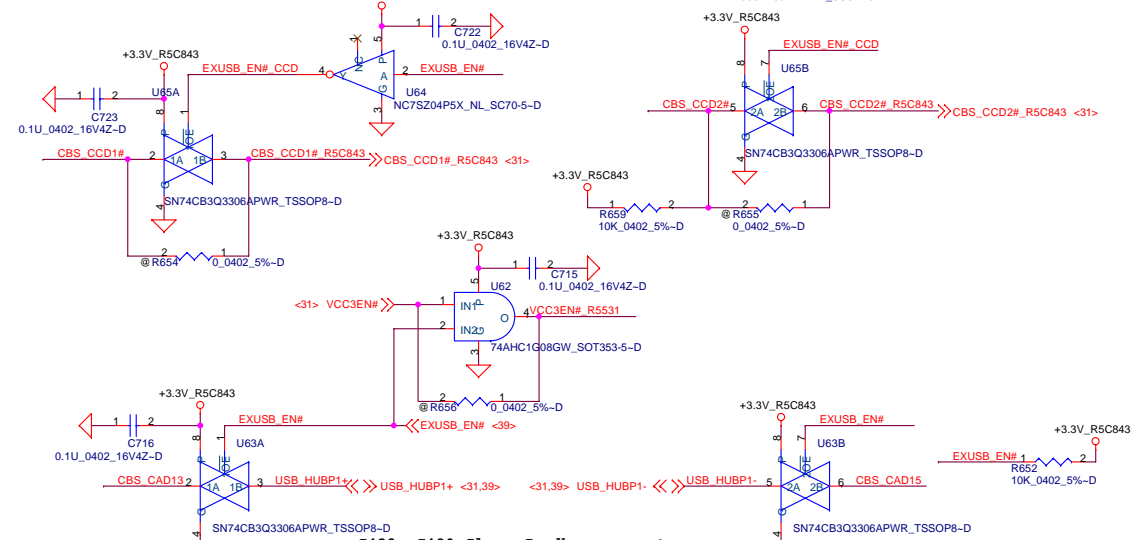
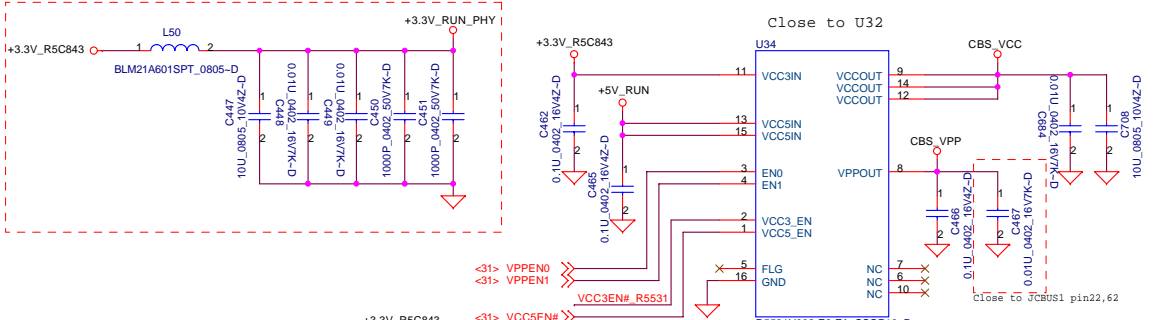
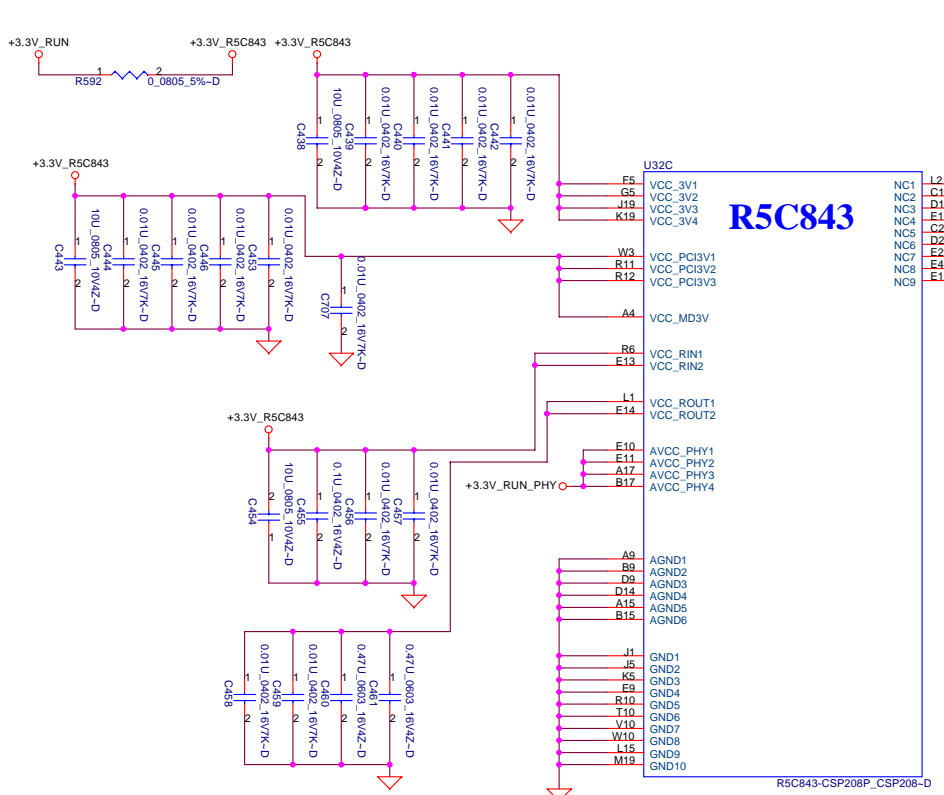
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CardBus Controller(R5C843)			
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SIM & SD CARD will combine together, the connector will update to 18pin

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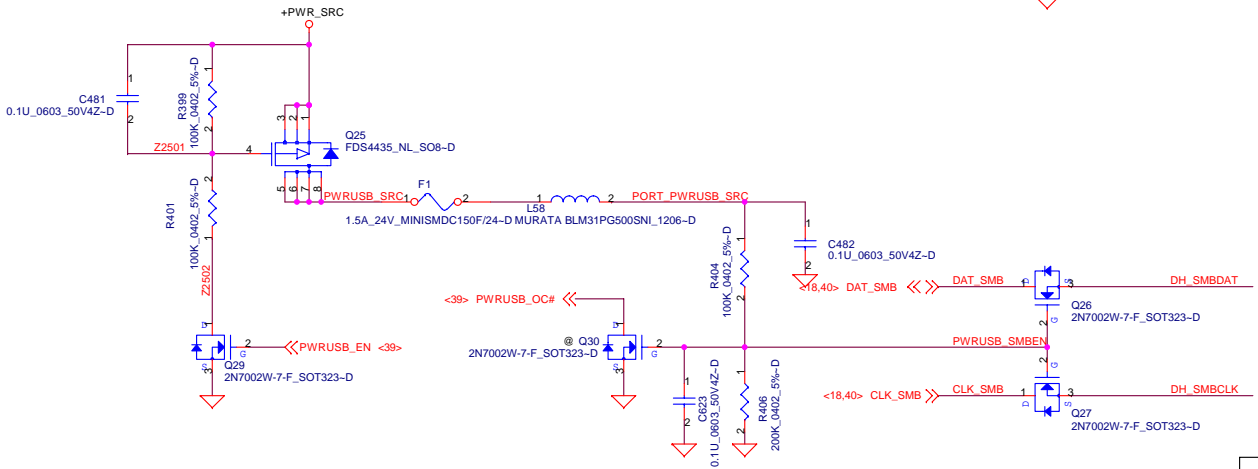
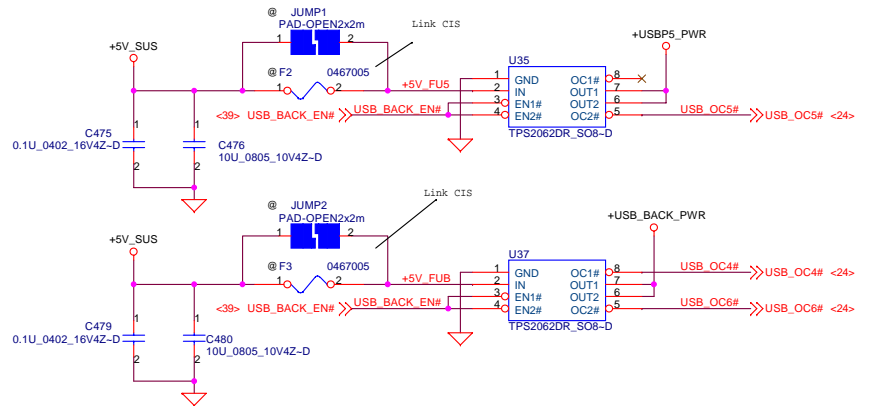
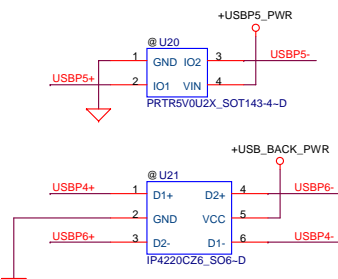
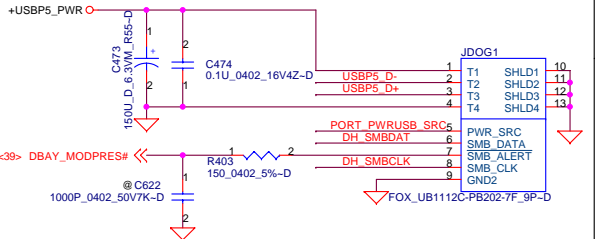
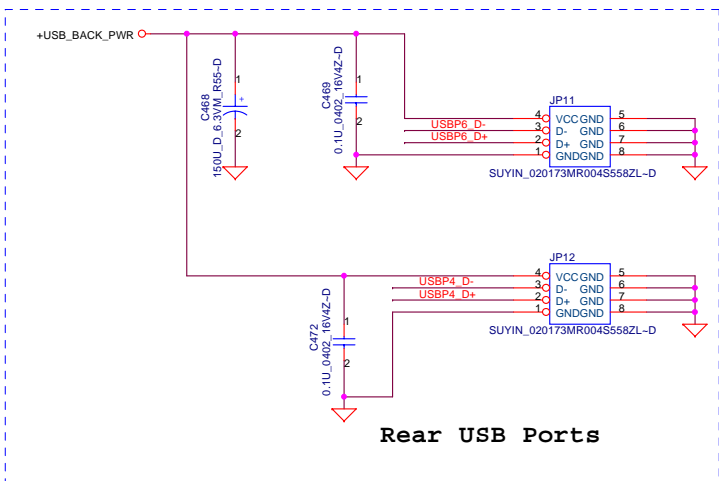
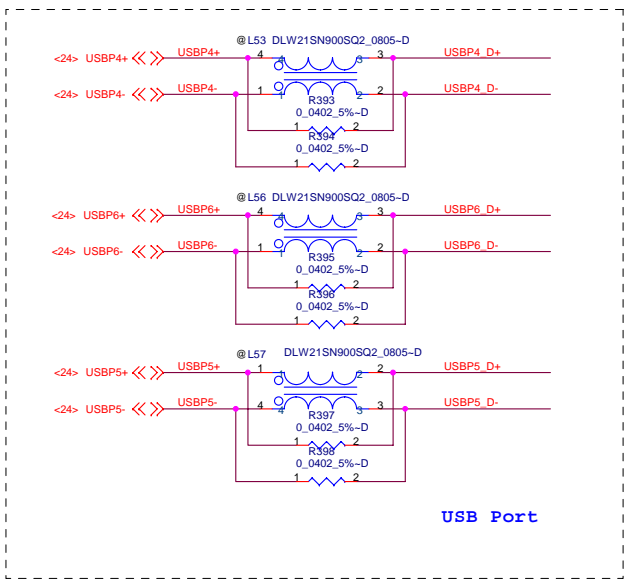


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CardBus/SD card Socket

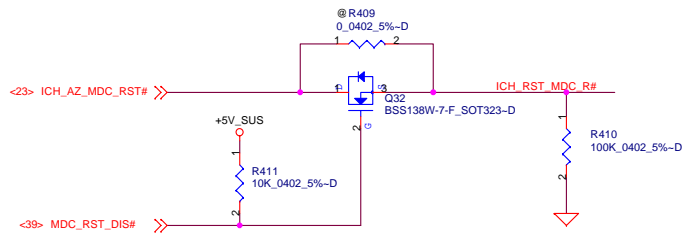
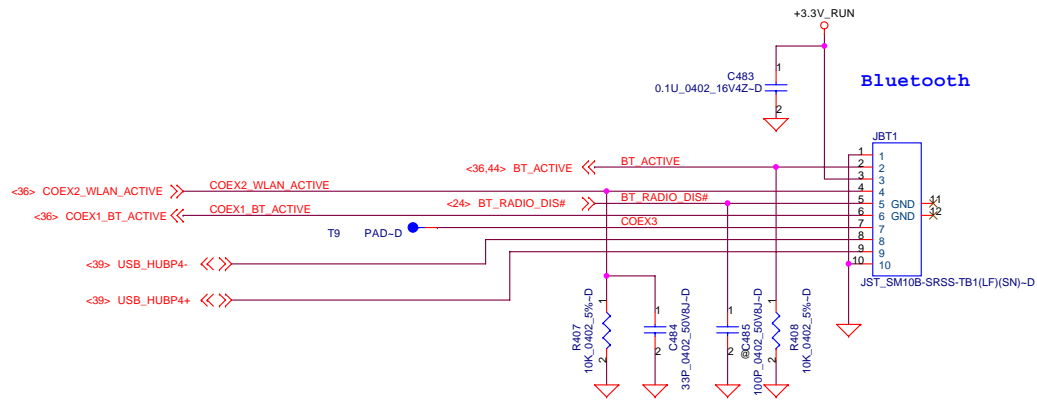
File	Document Number	Rev
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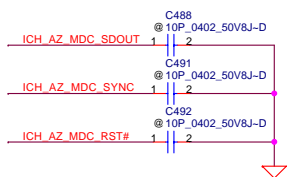
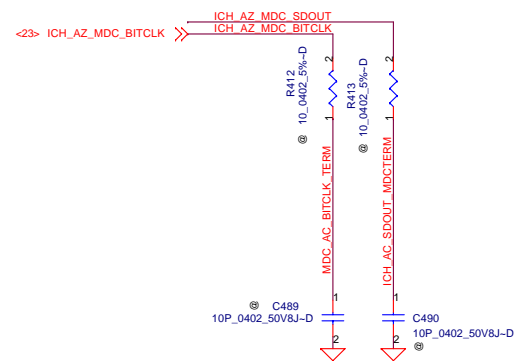
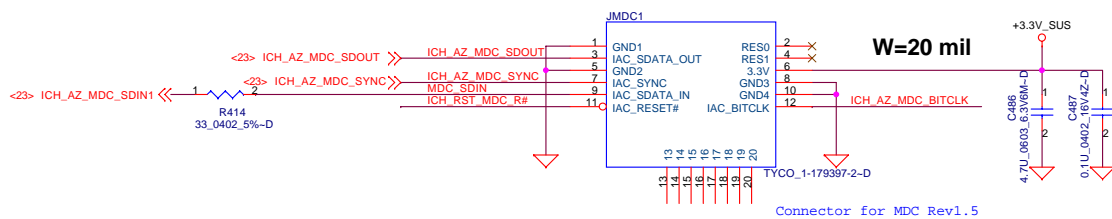
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Title: **USB 2.0 Port**
 Size: **LA-3741P**
 Date: Friday, February 02, 2007
 Sheet: 33 of 53



New MDC connector.

1	GND	RES	2
3	IAC_SDATA0	RES	4
5	GND	3.3V	6
7	IAC_SYNC	GND	8
9	IAC_SDATAIN	GND	10
11	IAC_RESET#	IAC_BITCLK	12



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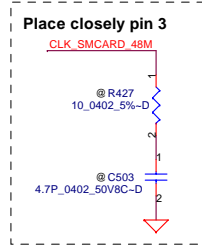
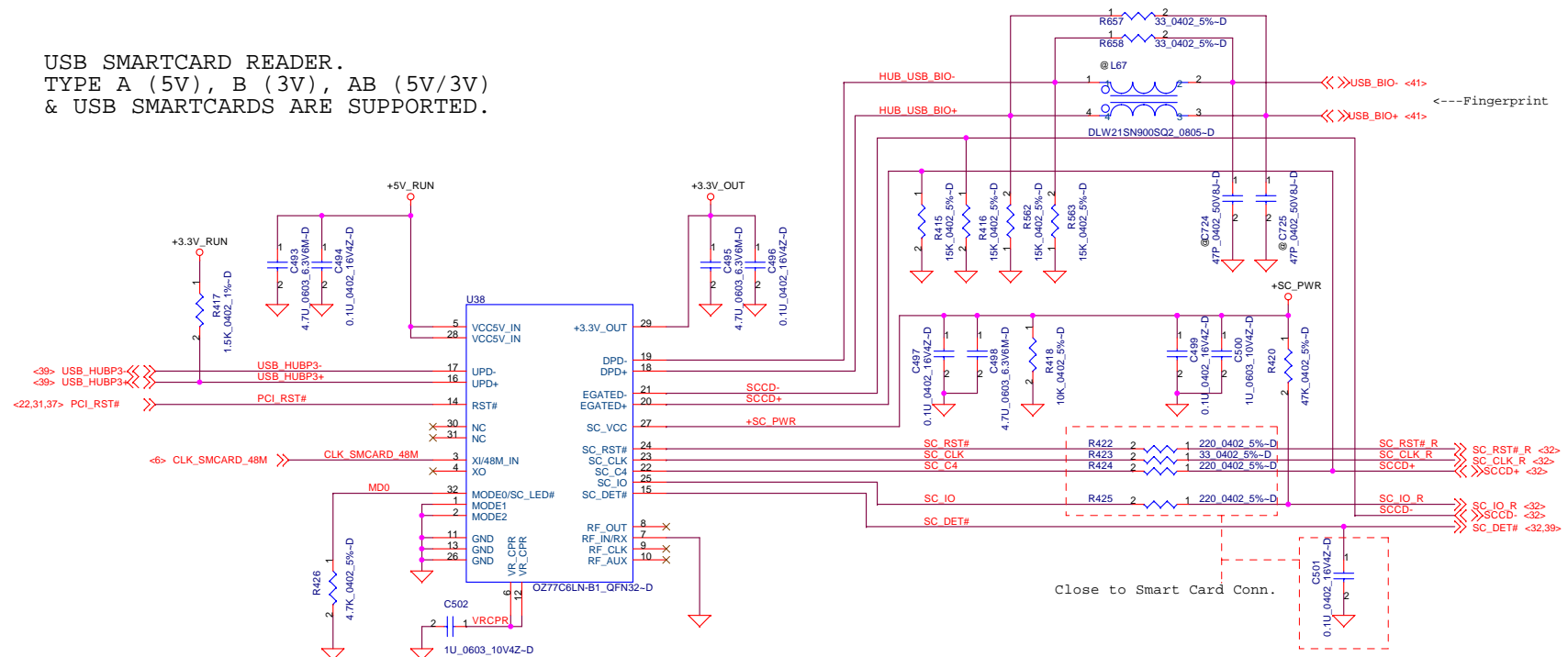


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Title			BT PORT & MDC		
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USB SMARTCARD READER.
 TYPE A (5V), B (3V), AB (5V/3V)
 & USB SMARTCARDS ARE SUPPORTED.



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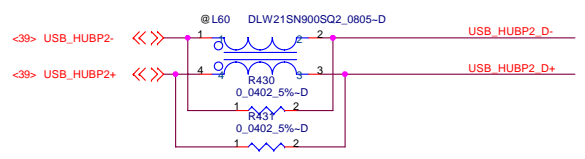
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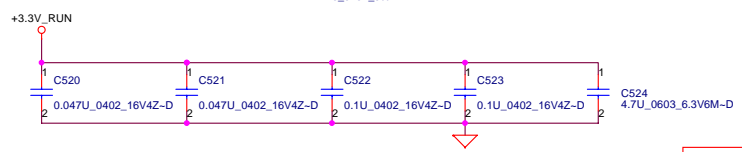
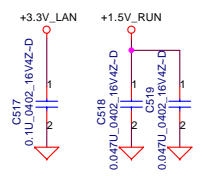
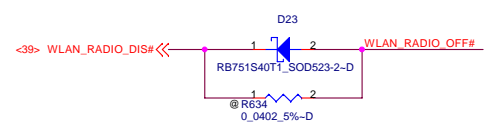
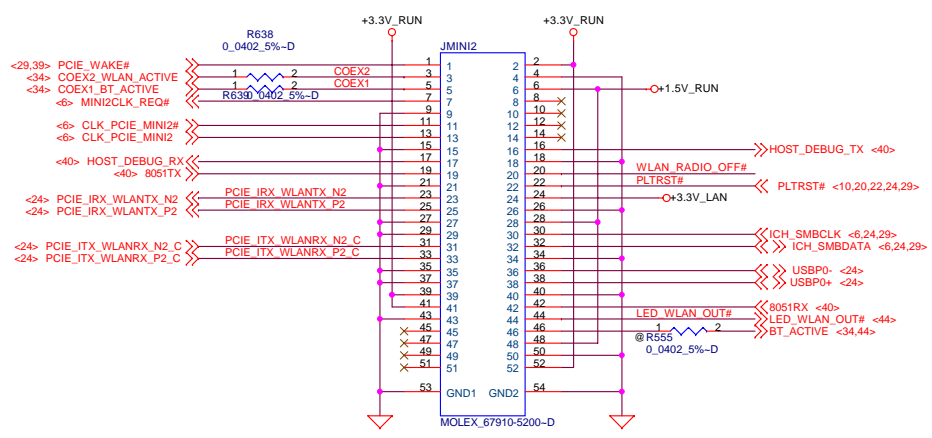
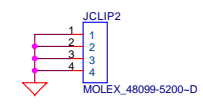
Smart Card OZ77C6

LA-3741P

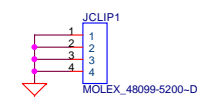
Friday, January 26, 2007 Sheet 35 of 53



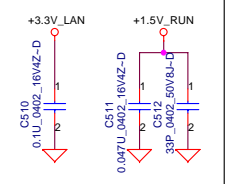
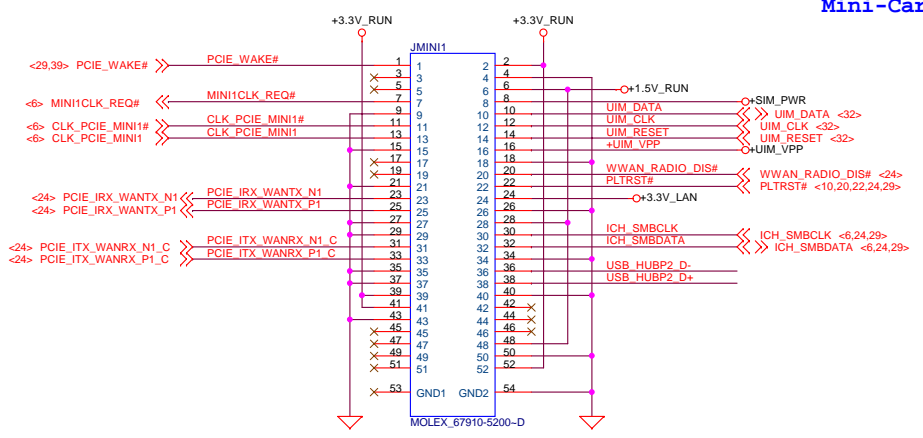
Mini Card Wire less LAN



Mini Card Wire less WAN



Mini-Card Latch



PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+ -9%	1000	750	
+3.3Vaux	+ -9%	330	250	250 (Wake enable) 5 (Not wake enable)
+1.5V	+ -5%	500	375	NA

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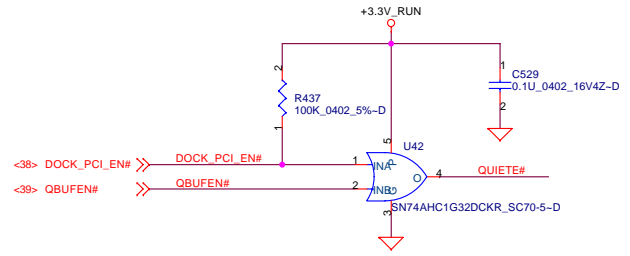
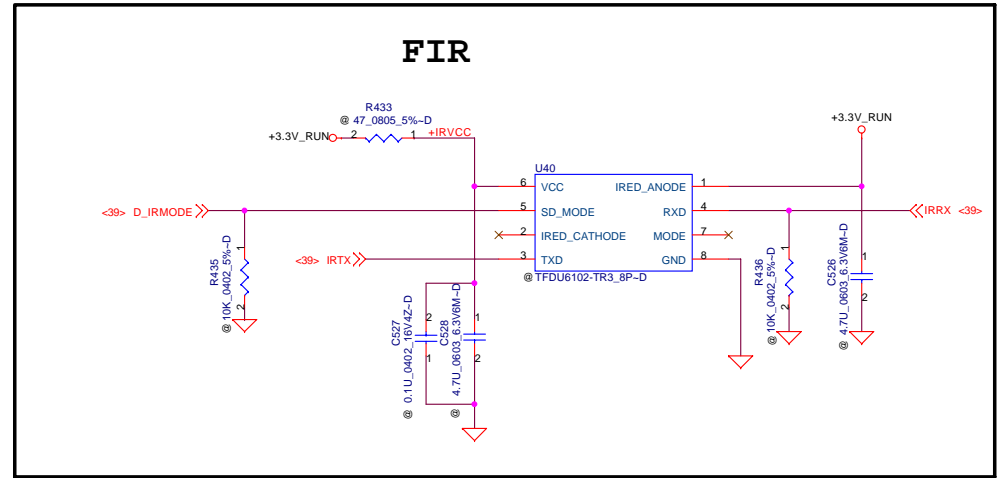
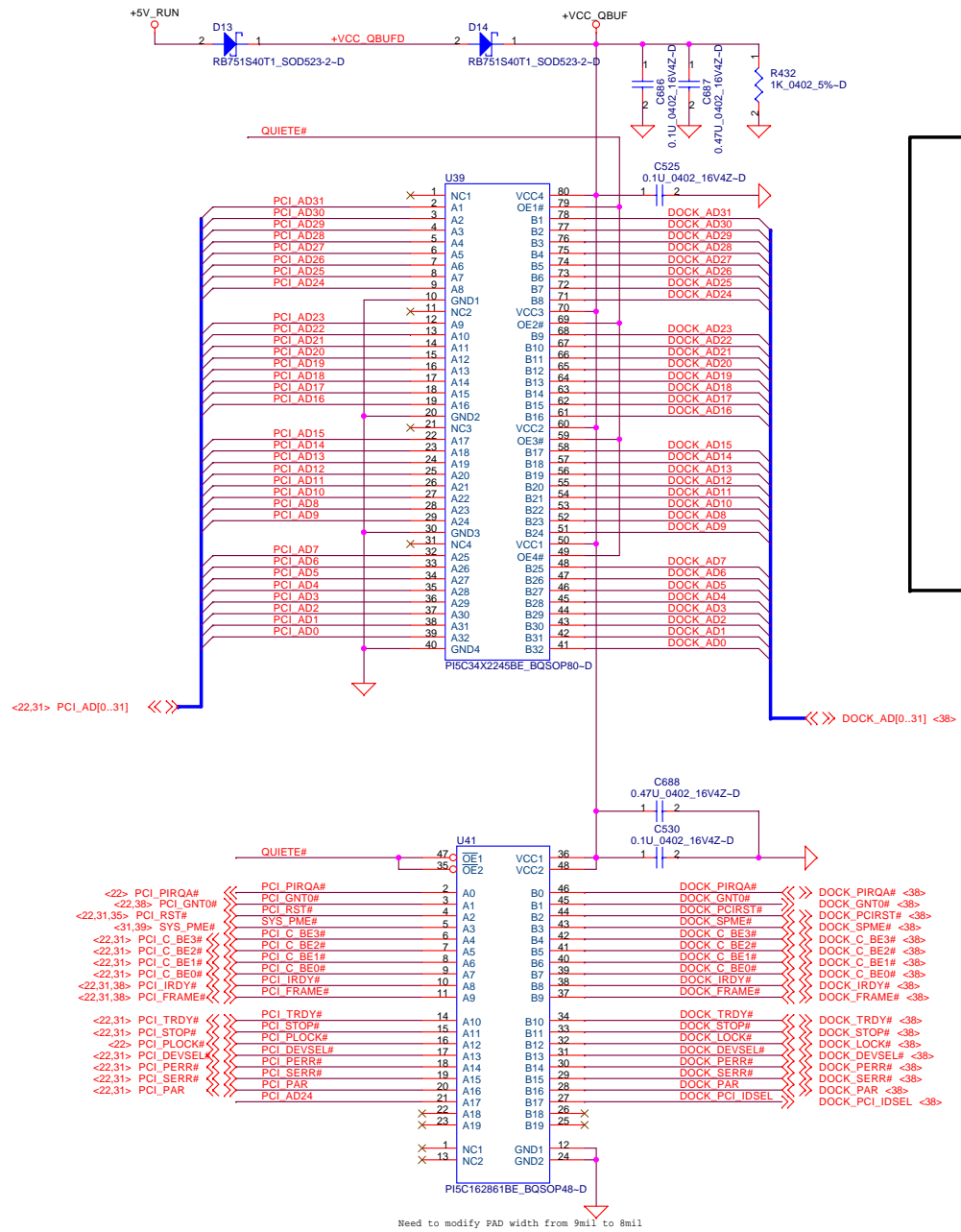
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Title: Mini Card

Size: Document Number LA-3741P Rev 0.1

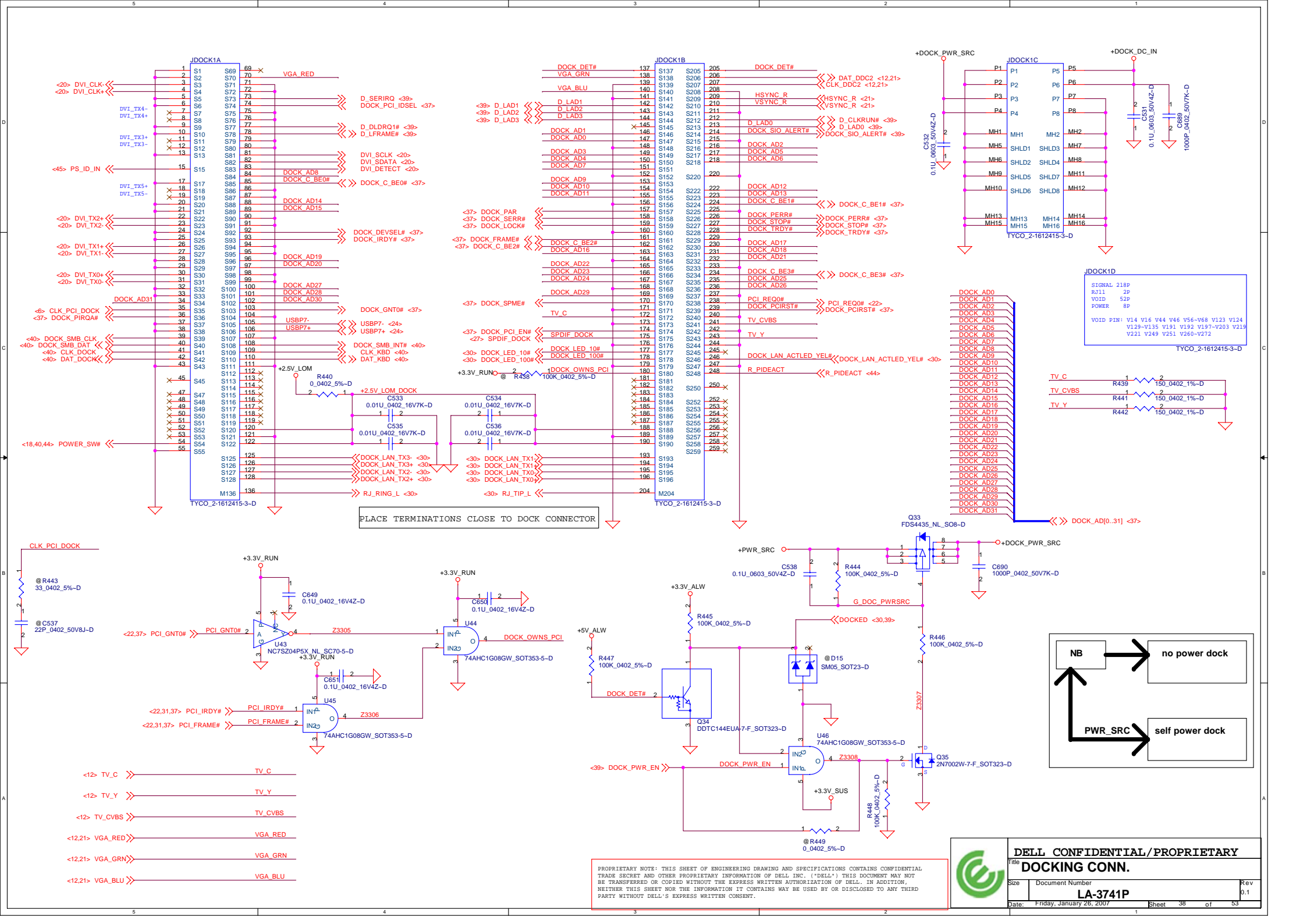
Date: Friday, January 26, 2007 Sheet 36 of 33



Need to modify PAD width from 9mil to 8mil

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	DELL CONFIDENTIAL/PROPRIETARY		
	Title DOCKING BUFFER & FIR		
	Size	Document Number LA-3741P	Rev 0.1
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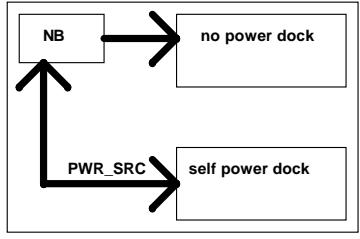


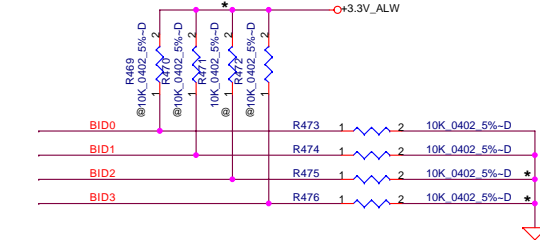
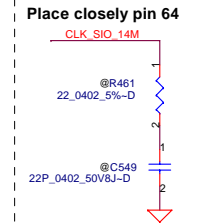
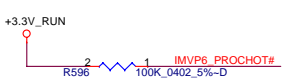
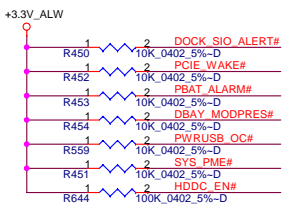
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TITLE DOCKING CONN.

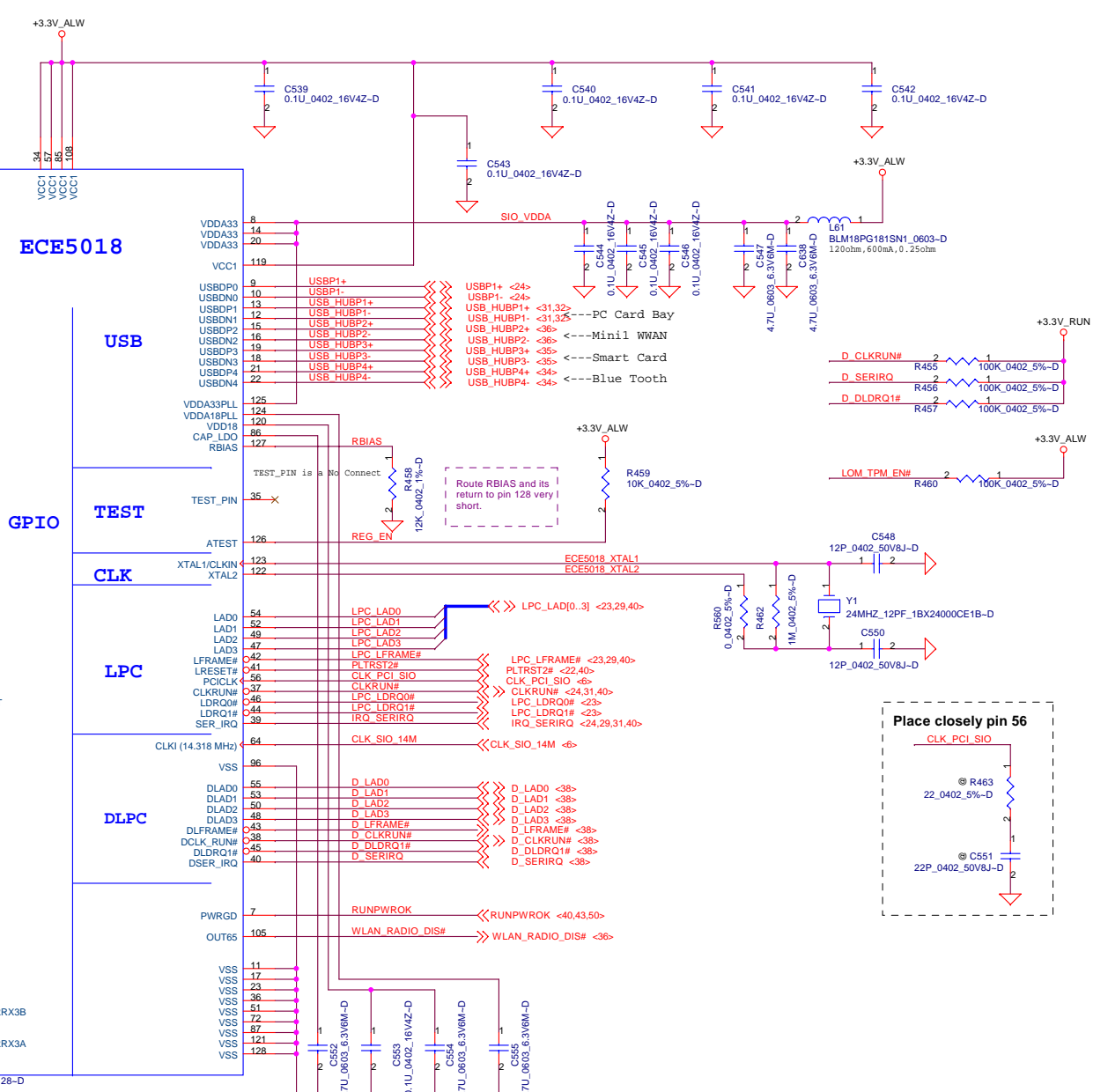
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<31,37> SYS_PME#	SYS_PME#	98	GPIOA[1]
<38> DOCK_SIO_ALERT#	DOCK_SIO_ALERT#	99	GPIOA[2]
<46> PBAT_ALARM#	PBAT_ALARM#	100	GPIOA[3]
		101	GPIOA[4]
		102	GPIOA[5]
		103	GPIOA[6]
		104	GPIOA[7]
<30,38> DOCKED	DOCKED	24	GPIOH[0]
<37> OBUFEN#	OBUFEN#	25	GPIOH[1]
<38> DOCK_PWR_EN	DOCK_PWR_EN	26	GPIOH[4]
<44> SNIFFER_WIRELESS_ON/OFF#	SNIFFER_WIRELESS_ON/OFF#	27	GPIOH[5]
<40> BC_INT#	BC_INT#	58	GPIOH[2]
<40> BC_DAT#	BC_DAT#	59	GPIOH[3]
<40> BC_CLK#	BC_CLK#	60	BC_CLK
		1	GPIOE[0]RXD
		2	GPIOE[1]TXD
		3	GPIOE[2]RTS#
		4	GPIOE[3]DSR#
		5	GPIOE[4]CTS#
		84	GPIOE[5]DTR#
		83	GPIOE[6]RX#
		6	GPIOE[7]DCD#
<33> PWRUSB_OC#	PWRUSB_OC#	65	GPIOB[0]JNIT#
<33> PWRUSB_EN	PWRUSB_EN	66	GPIOB[1]SCLTIN#
<34> MDC_RST_DIS#	MDC_RST_DIS#	67	GPIOC[2]SCLT
<51> ADAPT_OC#	ADAPT_OC#	68	GPIOC[3]PE
		69	GPIOC[4]BUSY
		70	GPIOC[5]ACK#
		71	GPIOC[6]ERROR#
		73	GPIOC[7]ALF#
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<27> SPDIF_SHDN	SPDIF_SHDN	76	GPIOC[0]PD6
<50> IMVP6_PROCHOT#	IMVP6_PROCHOT#	77	GPIOB[7]PD5
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<32> EXUSB_EN#	EXUSB_EN#	79	GPIOB[5]PD3
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		81	GPIOB[2]PD0
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		62	GPIOD[2]
<29> LOM_TPM_EN#	LOM_TPM_EN#	63	GPIOD[3]VBUS_DET
<29> LOM_LOW_PWR	LOM_LOW_PWR	28	GPIOD[0]CS1_N
<27> AUDIO_AVDD_ON	AUDIO_AVDD_ON	29	GPIOD[5]OCS2_N
<27> BEEP	BEEP	30	GPIOD[6]OCS3_N
<51> ADAPT_TRIP_SEL	ADAPT_TRIP_SEL	31	GPIOD[7]OCS4_N
		32	GPIOH[6]
<32,35> SC_DET#	SC_DET#	33	GPIOH[7]
<24> ICH_PCIE_WAKE#	ICH_PCIE_WAKE#	88	GPIOG[0]
<22> ICH_PME#	ICH_PME#	89	GPIOG[1]
<18> THERMTRIP_SIO	THERMTRIP_SIO	90	GPIOG[2]
<31> CBUS_GRS1#	CBUS_GRS1#	91	GPIOG[3]
		92	GPIOG[4]
<19> FPBACK_EN	FPBACK_EN	93	GPIOG[5]
<31> CB_HWSPND#	CB_HWSPND#	94	GPIOG[6]
<7> CPU_PROCHOT#	CPU_PROCHOT#	95	GPIOG[7]
<26> HDDC_EN#	HDDC_EN#	106	SYSOPT1/GPIOH[2]
		107	SYSOPT0/GPIOH[3]
		109	BID3
		110	BID2
		111	BID1
		112	BID0
<37> IRTX	IRTX	113	IRTX
<37> IRRX	IRRX	114	IRRX
<37> D_IRMODE	D_IRMODE	115	GPIOF[3]IRMODE/IRRX3B
<33> USB_BACK_EN#	USB_BACK_EN#	117	GPIOF[1]IRRX2
<33> DBAY_MODPRES#	DBAY_MODPRES#	118	GPIOF[0]IRMODE/IRRX3A

BID3	BID2	BID1	BID0	REV
0	0	0	0	X00
0	0	0	1	X01
0	0	1	0	X02
0	0	1	1	X03
0	1	0	0	A00



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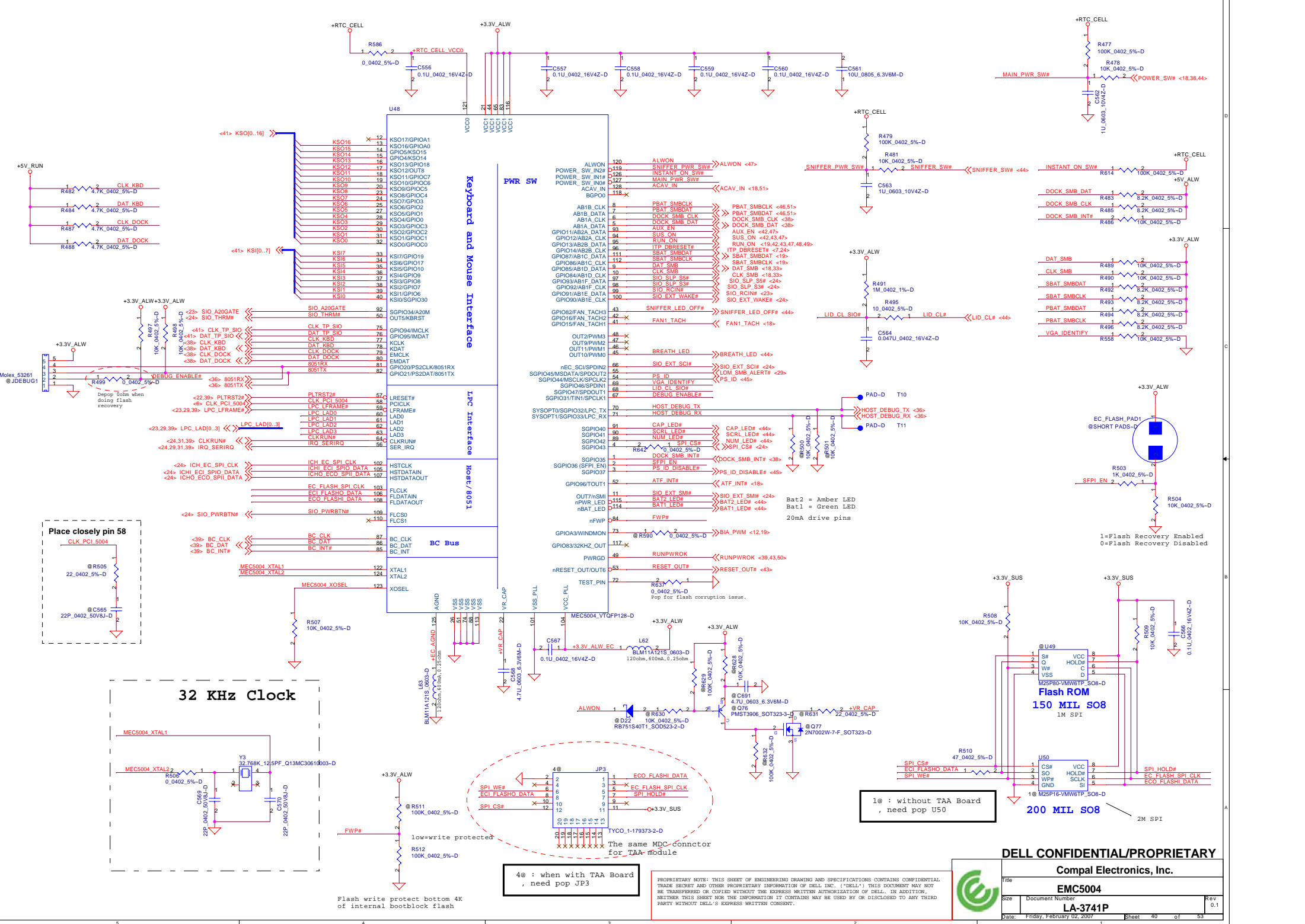
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Title: ECE5018

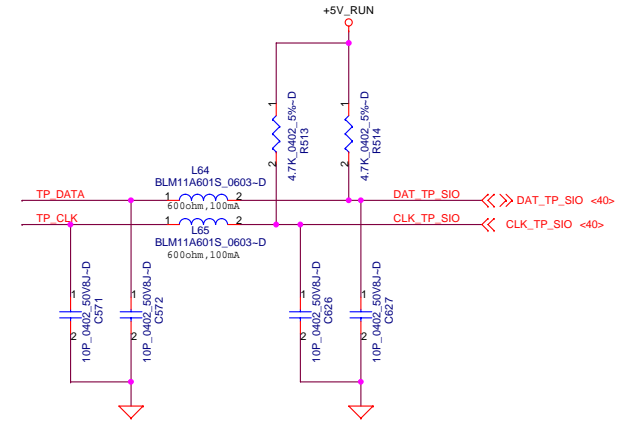
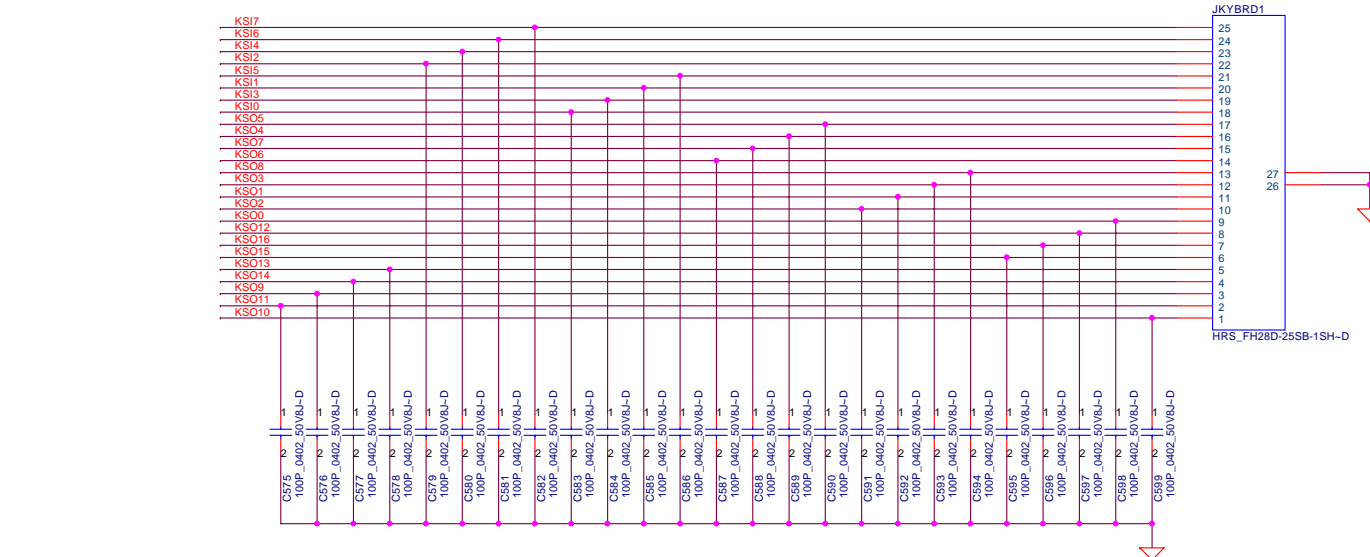
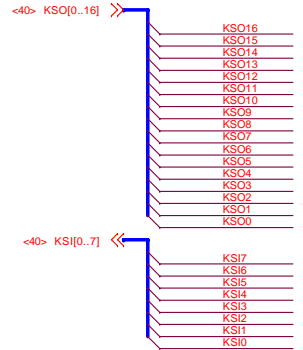
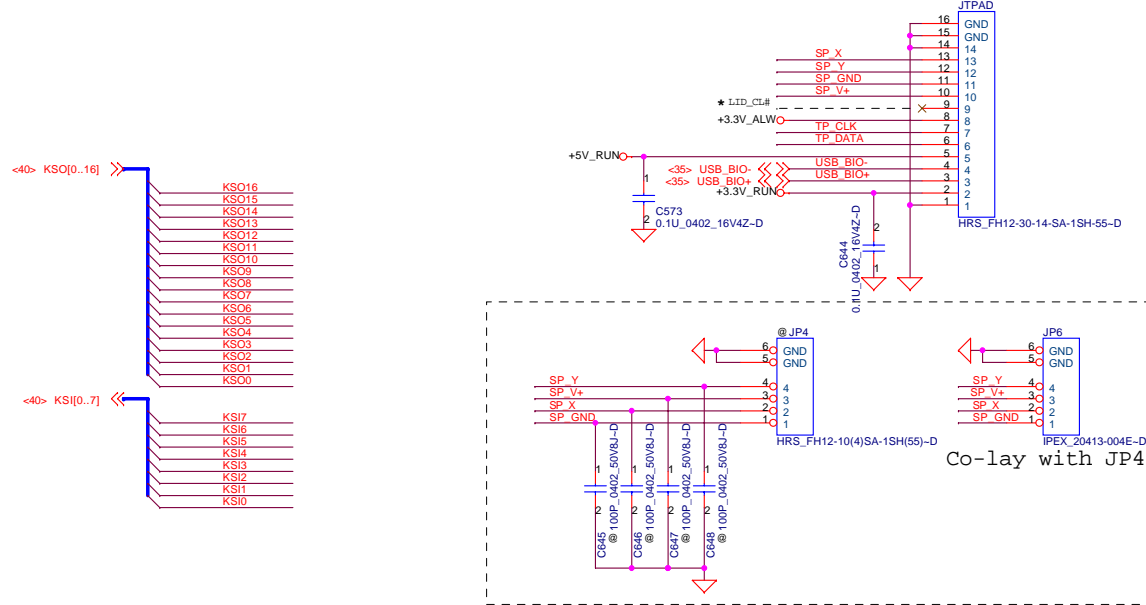
Size: Document Number: LA-3741P

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Touch PAD



SPKER1

Part Number	Description
PK230005C0L	SPK PACK 00B 1W 80HM

PCMCIA BODY

Part Number	Description
DC000002T0L	PCMCIA FOXCONN 1CA86501-CR-4F

Bluetooth wire set cable

Part Number	Description
DC02000980L	H-CONN SET 00B M/B-B/T

MDC wire set cable

Part Number	Description
DC02000960L	H-CONN SET 00B M/B-MDC

T/P FPC

Part Number	Description
DA30000101L	FPC 00B LP-3072P REV1 T/P FPC WITH BIO

LCD cable

Part Number	Description
DC020008Q0L	H-CONN SET 00B MB-LCD 12 WXGA

HDD FPC cable

Part Number	Description
DA300001N1L	FPC 00B LP-3071P REV1 HITACHI

RTC BATT

Part Number	Description
GC020008R00	BATT CR2025 W/CABLE 170MAH MB 00B 0PFD

Touch-PAD MODULE

Part Number	Description
PK090003M0L	TRACK PAD ALPS KGDEN101A BIOSSENSOR

LED FPC cable

Part Number	Description
DA300001S1L	FPC 00B LP-3073P REV1 LED FPC

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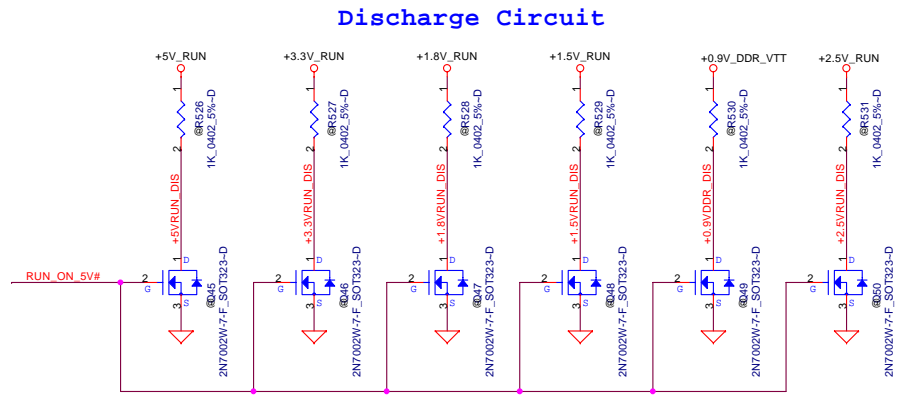
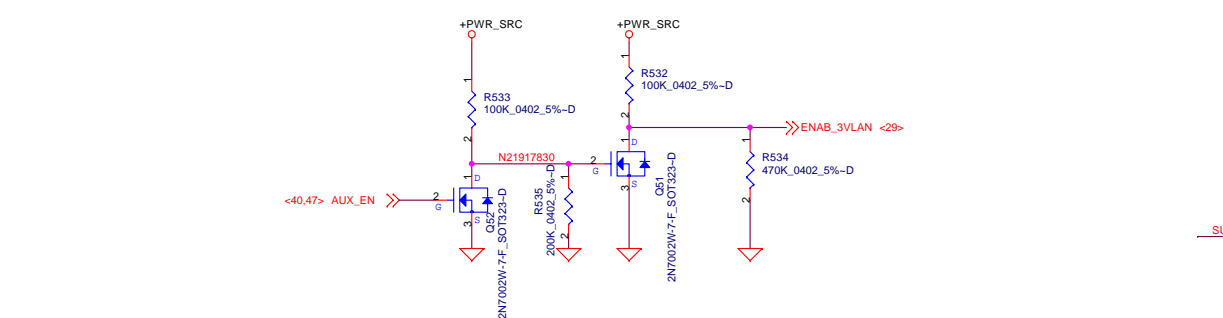
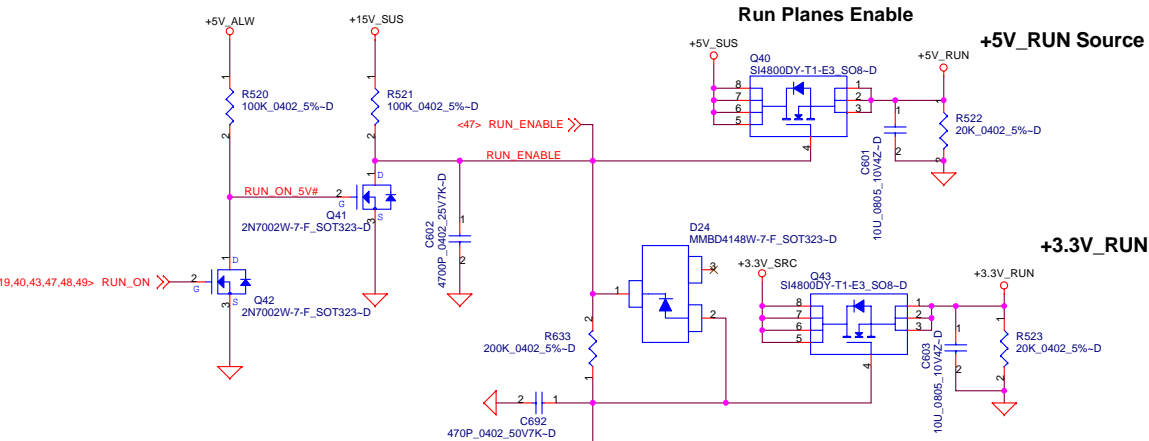
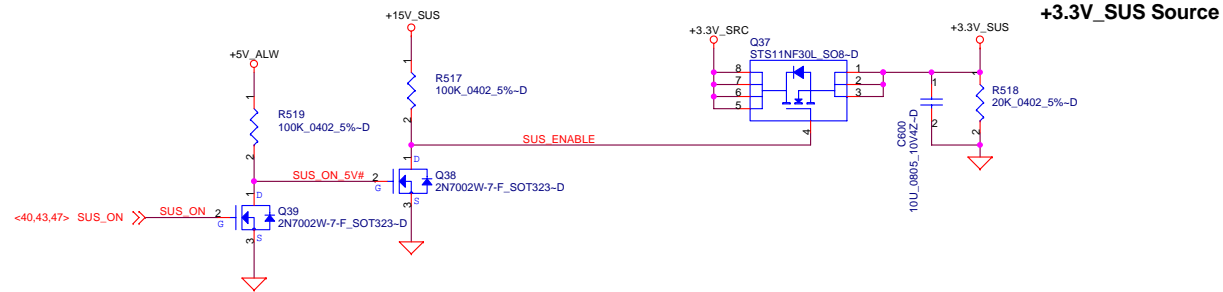


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INT KB & FT & LID & TOUCH PAD		
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DC/DC Interface



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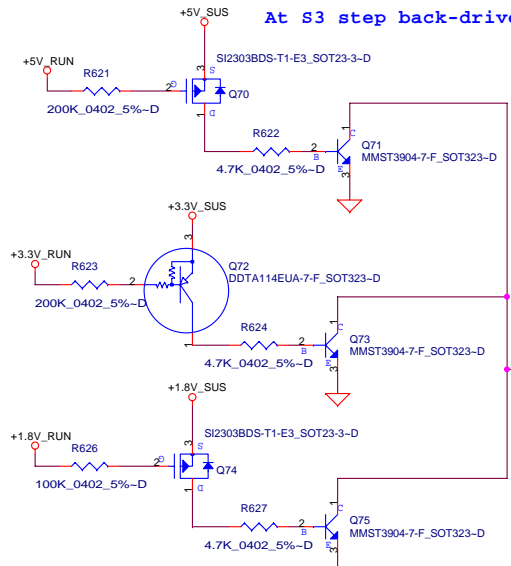
POWER CONTROL

LA-3741P

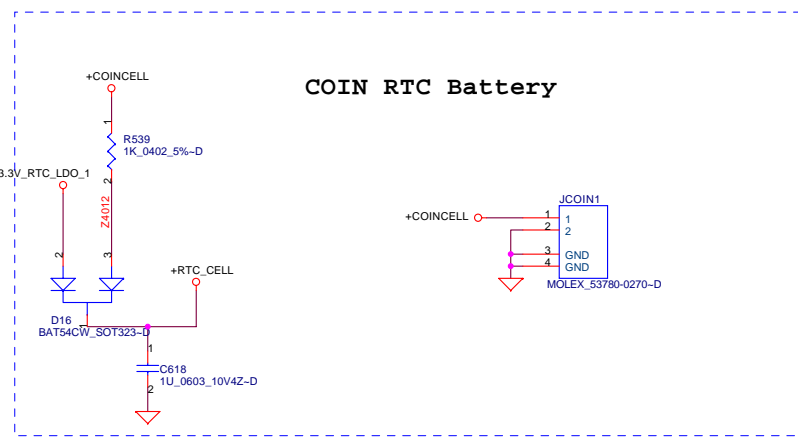
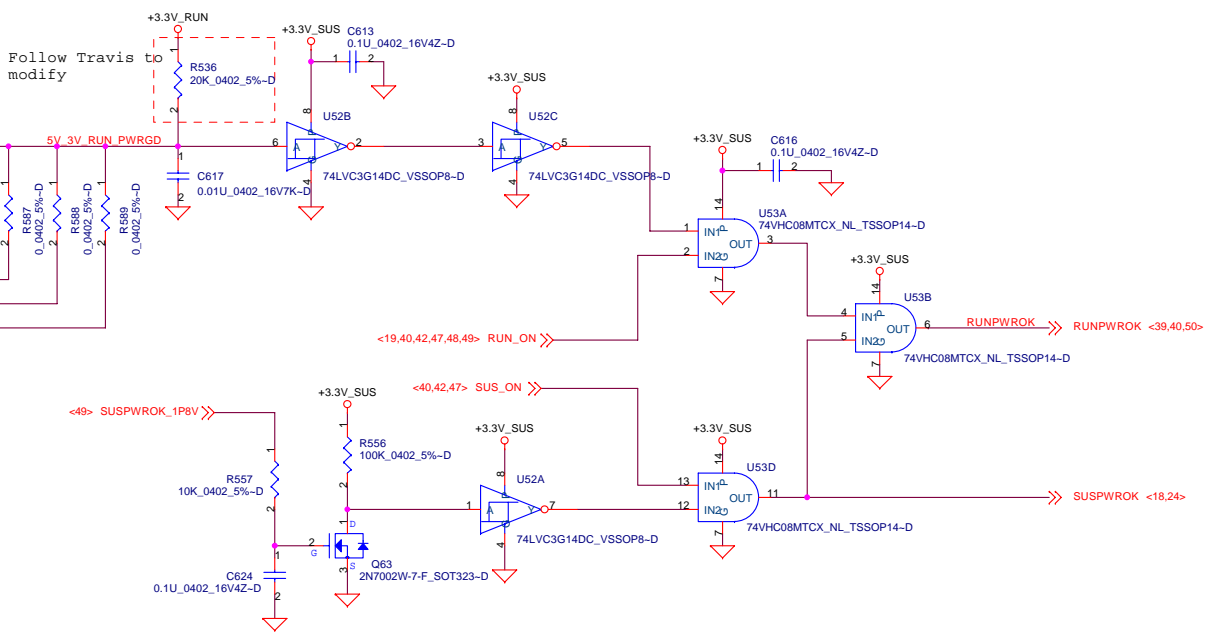
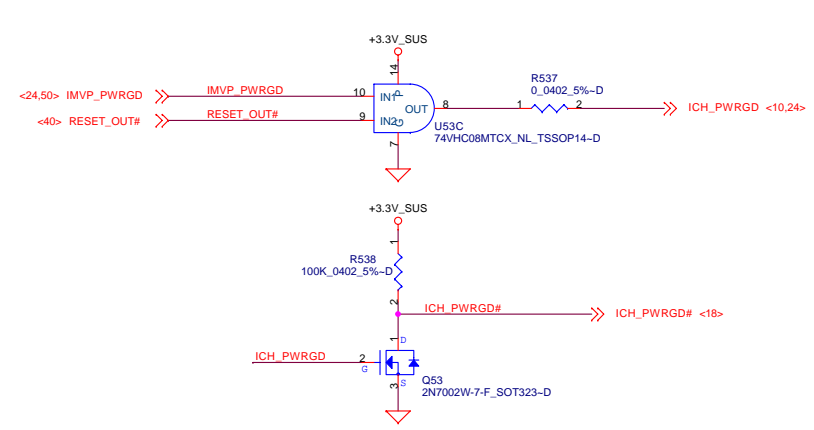
Date: Friday, January 26, 2007 Sheet 42 of 53

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At S3 step back-drive: 78mV, change to SI2303



At S3 step back-drive: 198mV, change to SI2303



<18> 2.5V_RUN_PWRGD >>
 <48> 1.5V_RUN_PWRGD >>
 <48> 1.05V_RUN_PWRGD >>
 <19,40,42,47,48,49> RUN_ON >>
 <40,42,47> SUS_ON >>
 <49> SUSPWROK_1P8V >>
 <24,50> IMVP_PWRGD >> IMVP_PWRGD
 <40> RESET_OUT# >> RESET_OUT#
 ICH_PWRGD <10,24> >>
 ICH_PWRGD# <18> >>
 SUSPWROK <18,24> >>
 RUNPWROK <39,40,50> >>

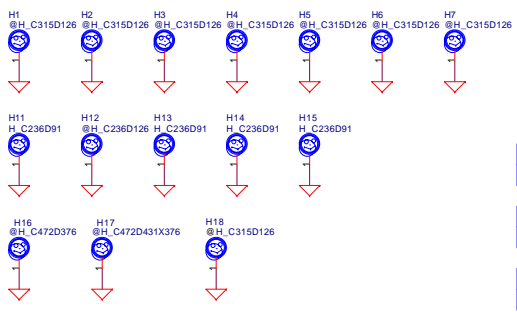
Follow Travis to modify

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Compal Electronics, Inc.		
Power Good		
LA-3741P	Rev 0.1	
Date: Friday, January 26, 2007	Sheet 43 of 53	

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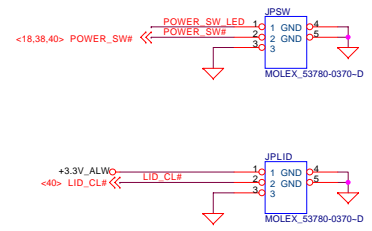
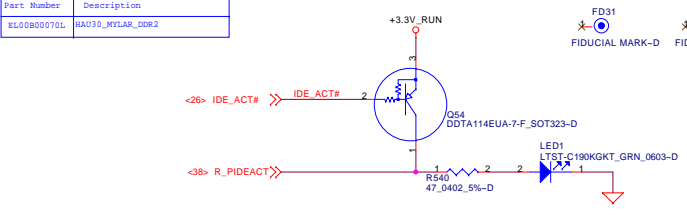
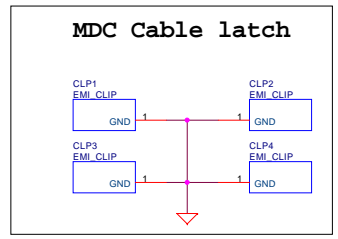
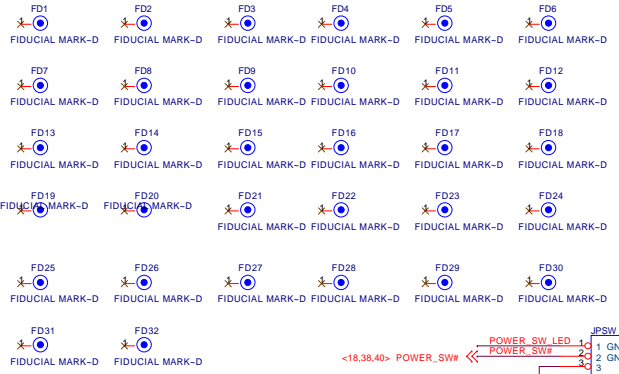
MYLAR1	Description	MYLAR5	Description
Part Number	EL00800040L	Part Number	EL00800080D
Description	HAU30_DOCKING_HOLE_MYLAR	Description	HAU30_MYLAR_WLAN_MWAN

MYLAR2	Description	MYLAR6	Description
Part Number	EL00800050L	Part Number	EL008000X0D
Description	HAU30_DOCKING_LOCK_L_MYLAR	Description	HAU30_MYLAR_RDD

MYLAR3	Description	MYLAR7	Description
Part Number	EL00800060L	Part Number	EL008000A0L
Description	HAU30_DOCKING_LOCK_R_MYLAR	Description	HAU30_MYLAR_FAN

MYLAR4	Description
Part Number	EL00800070L
Description	HAU30_MYLAR_DDR2

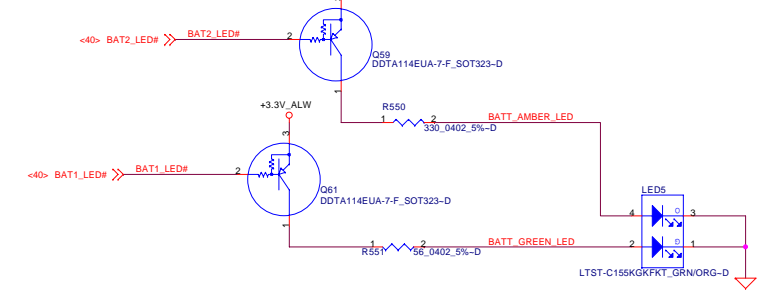
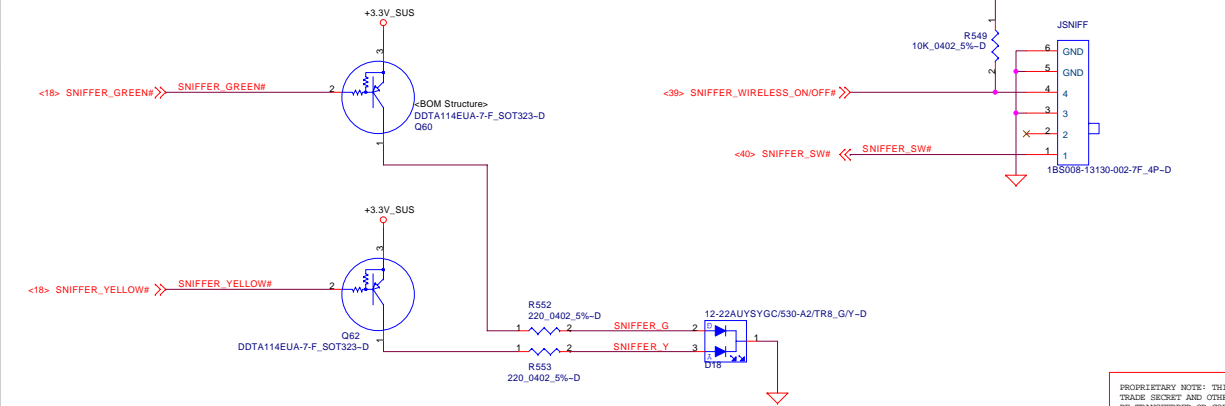
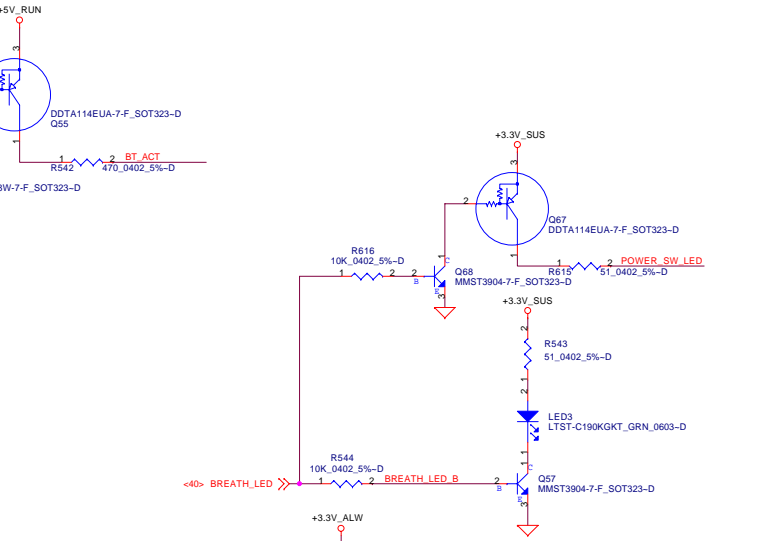
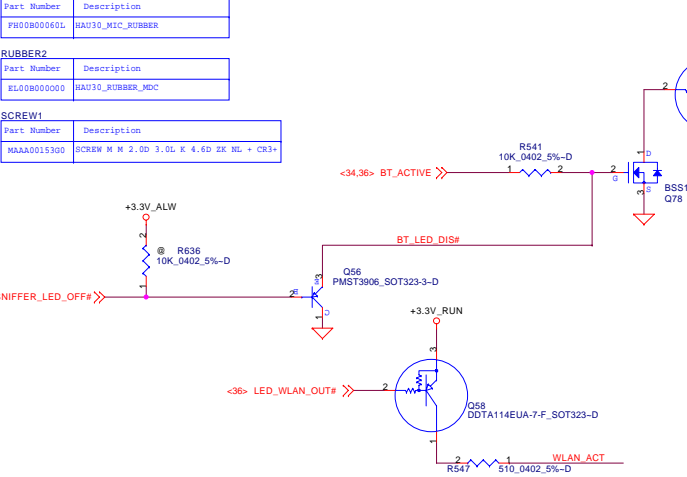
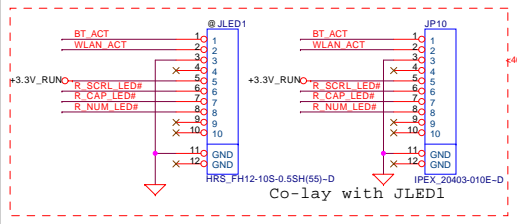
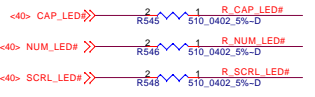
Fiducial Mark



RUBBER1	Description
Part Number	PH00800060L
Description	HAU30_MIC_RUBBER

RUBBER2	Description
Part Number	EL00800000D
Description	HAU30_RUBBER_MDC

SCREW1	Description
Part Number	MAAA001530D
Description	SCREW M M 2.0D 3.0L X 4.6D ZK NL + CR3+



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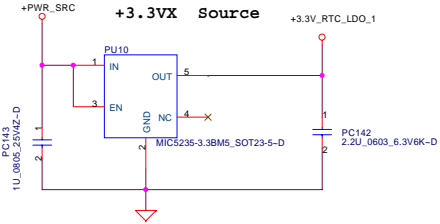
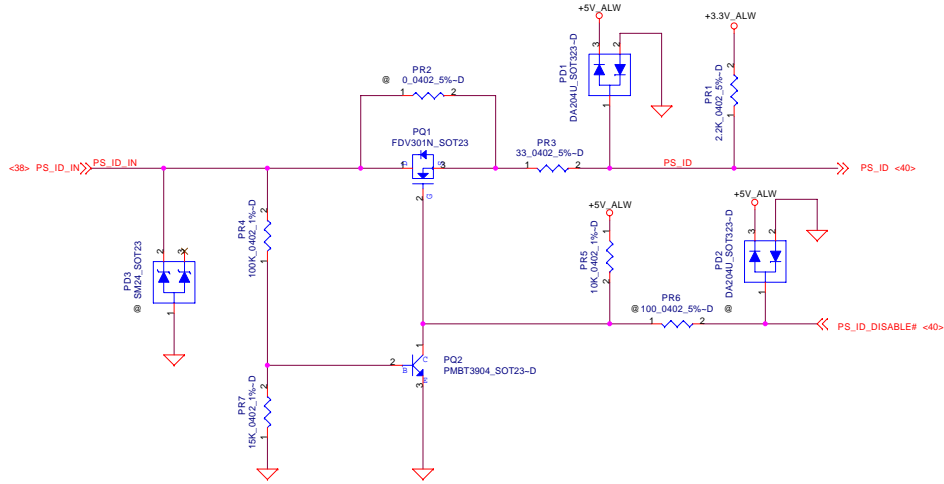
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Size: Document Number **LA-3741P**

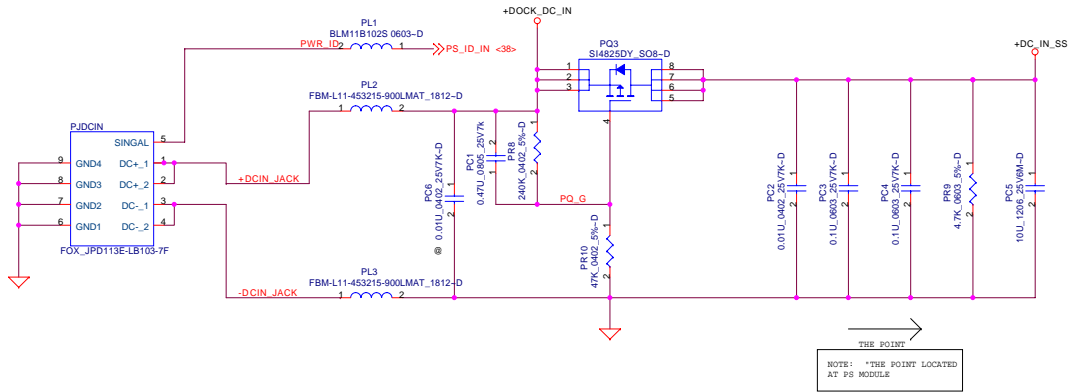
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PS_ID Detector



+DC_IN Source



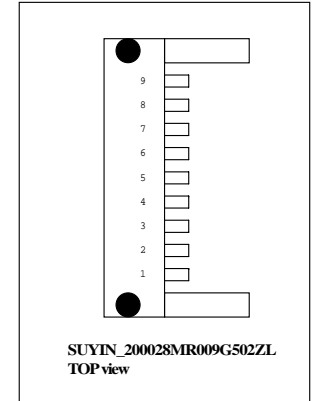
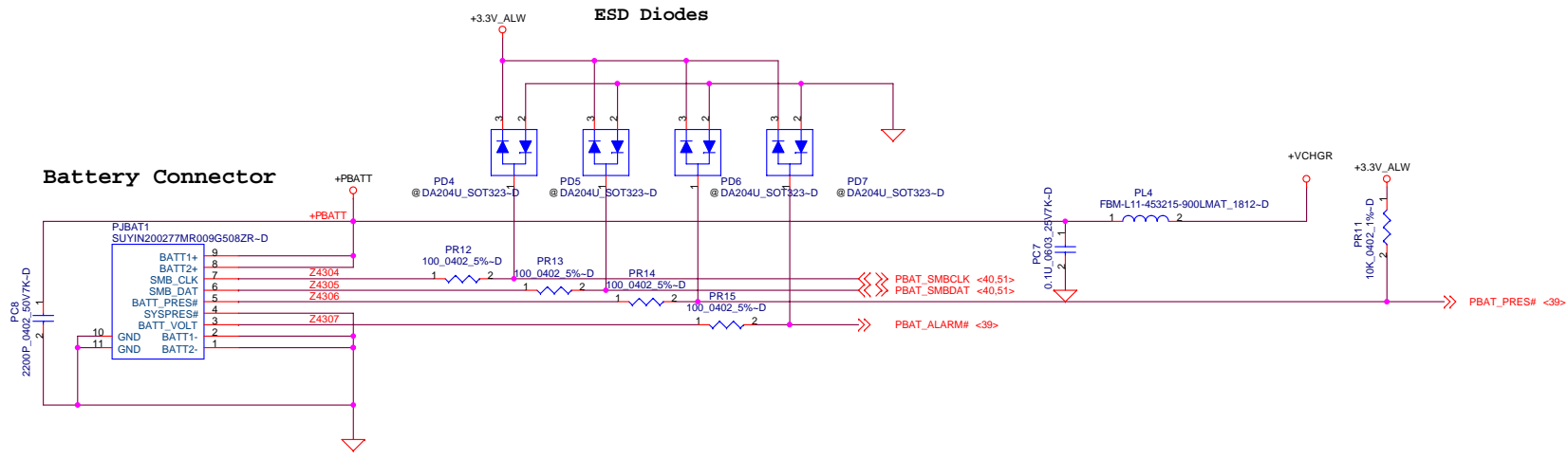
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+DCIN

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Title: Battery Conn		
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DC/DC +3V/ +5V/ +15V

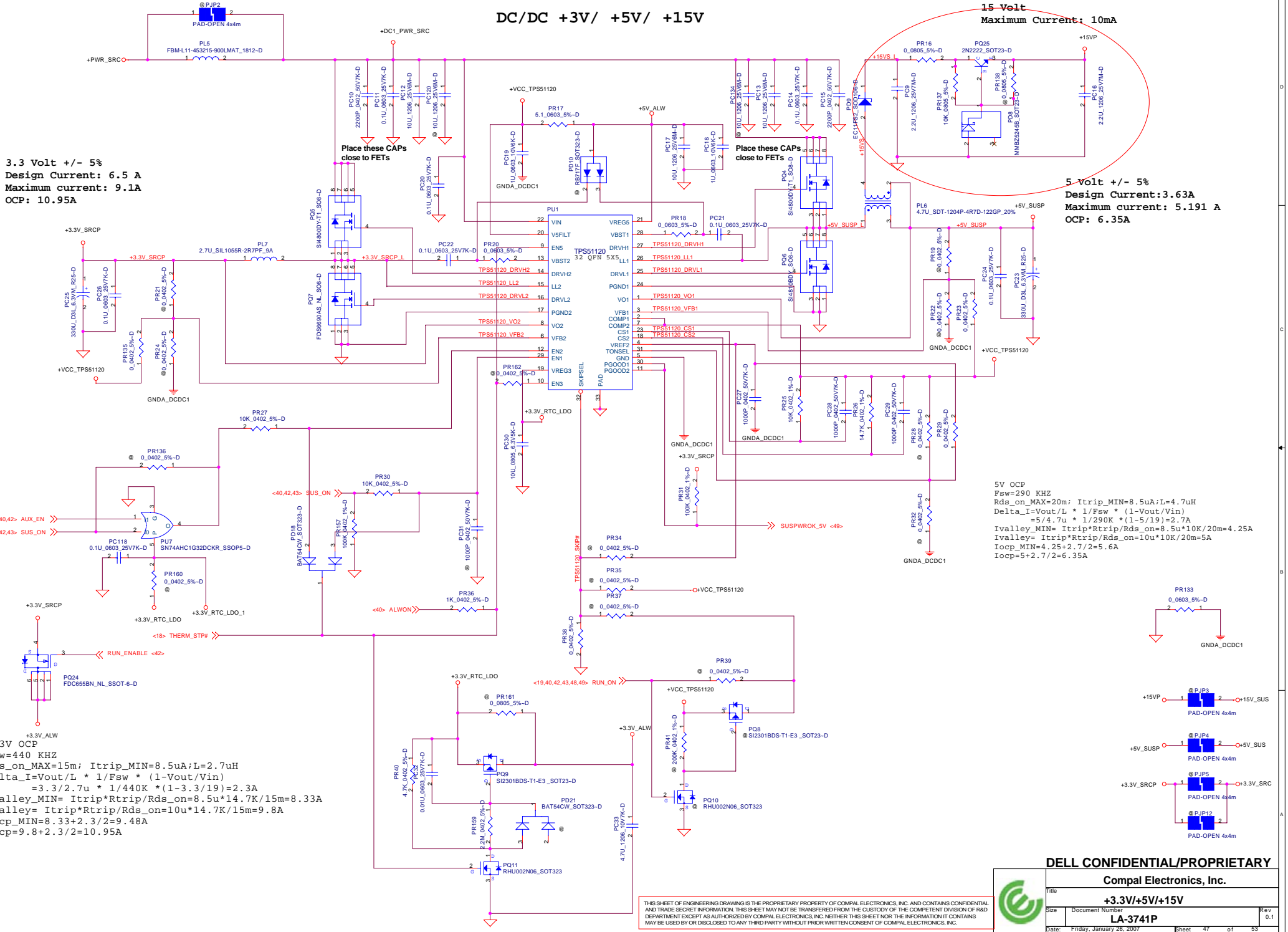
15-Volt
Maximum Current: 10mA

3.3 Volt +/- 5%
Design Current: 6.5 A
Maximum current: 9.1A
OCP: 10.95A

5 Volt +/- 5%
Design Current: 3.63A
Maximum current: 5.191 A
OCP: 6.35A

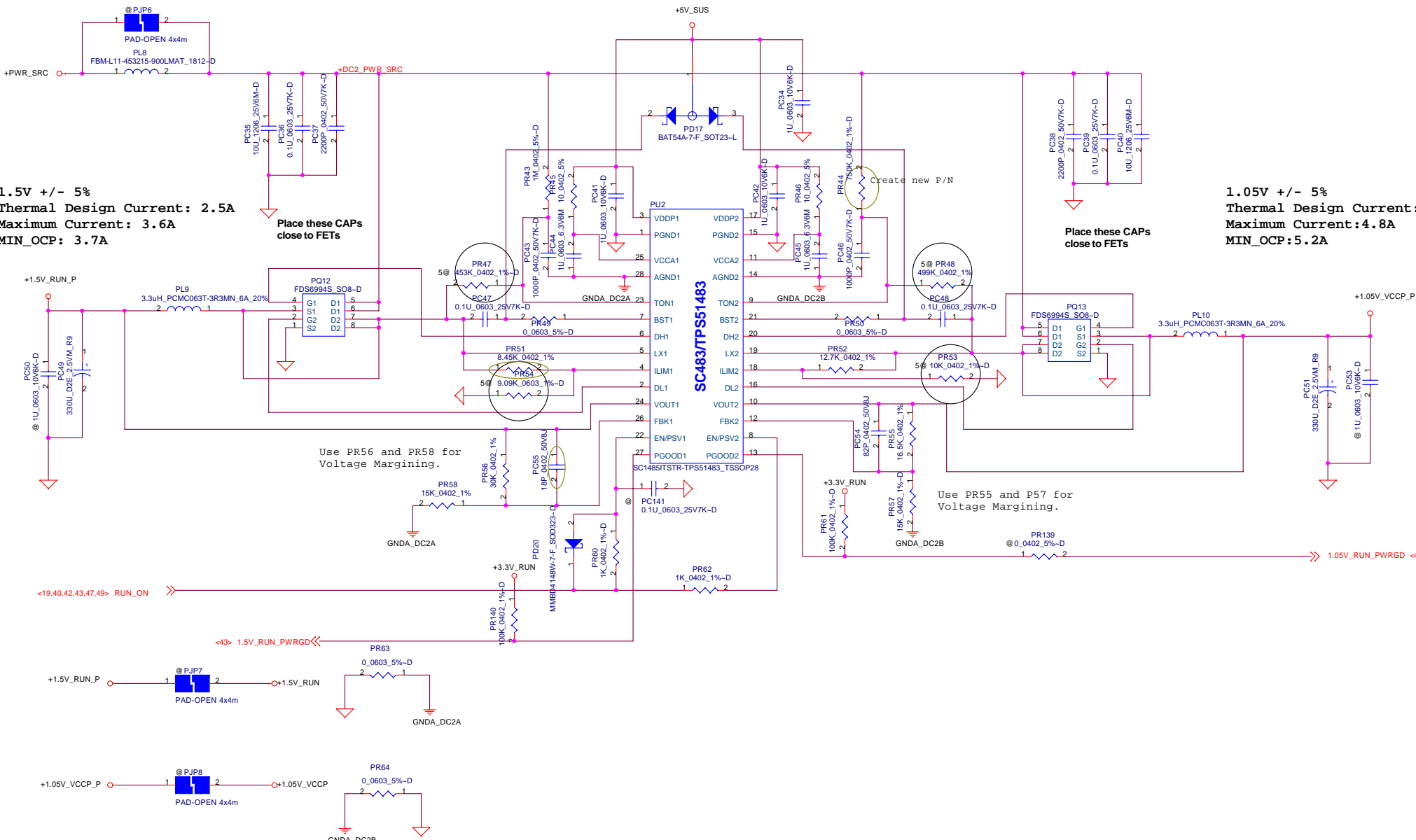
5V OCP
Fsw=290 KHZ
Rds_on_MAX=20m; Itrip_MIN=8.5uA;L=4.7uH
Delta_I=Vout/L * 1/Fsw * (1-Vout/Vin)
=5/4.7u * 1/290K * (1-5/19)=2.7A
Ivalley_MIN= Itrip*Rtrip/Rds_on=8.5u*10K/20m=4.25A
Ivalley= Itrip*Rtrip/Rds_on=10u*10K/20m=5A
Iocp_MIN=4.25+2.7/2=5.6A
Iocp=5+2.7/2=6.35A

3.3V OCP
Fsw=440 KHZ
Rds_on_MAX=15m; Itrip_MIN=8.5uA;L=2.7uH
Delta_I=Vout/L * 1/Fsw * (1-Vout/Vin)
=3.3/2.7u * 1/440K * (1-3.3/19)=2.3A
Ivalley_MIN= Itrip*Rtrip/Rds_on=8.5u*14.7K/15m=8.33A
Ivalley= Itrip*Rtrip/Rds_on=10u*14.7K/15m=9.8A
Iocp_MIN=8.33+2.3/2=9.48A
Iocp=9.8+2.3/2=10.95A



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		Compal Electronics, Inc.	
+3.3V/+5V/+15V			
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1.5V +/- 5%
 Thermal Design Current: 2.5A
 Maximum Current: 3.6A
 MIN_OCP: 3.7A

1.05V +/- 5%
 Thermal Design Current: 3.36A
 Maximum Current: 4.8A
 MIN_OCP: 5.2A


BOM

Structure	Description
@	Do Not Populate
4@	Populate for Semtech - SC483 Only
5@	Populate for Ti - TPS51483 Only

Ref Des	SC483	TPS52483
PR56	30.0K	15.0K
PR58	15.0K	15.0K
PR55	16.5K	11.8K
PR57	15.0K	29.4K

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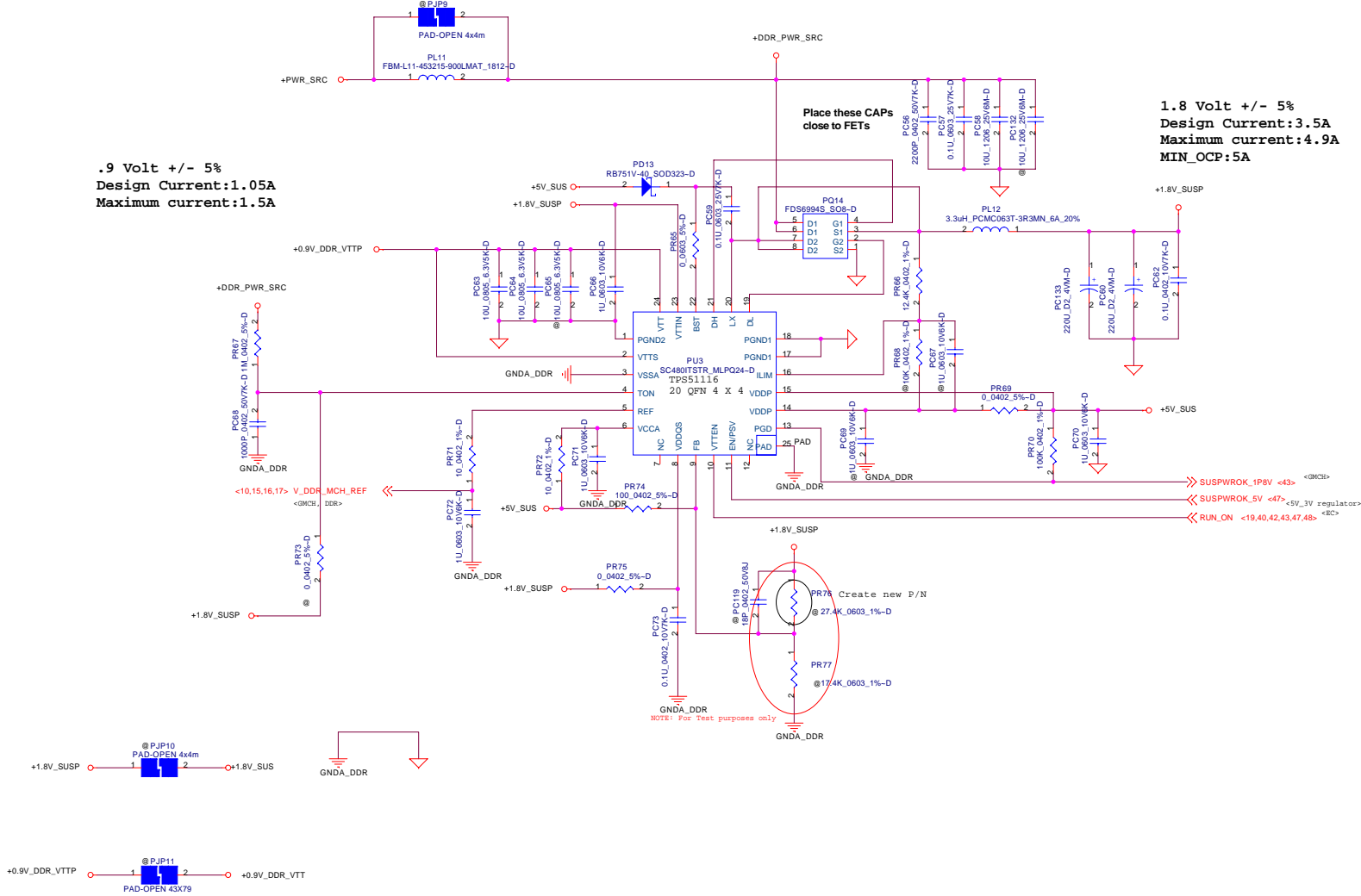
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			+1.5VRUNP /+VCCP_1P05VP		
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NOTE: Component Values shown for SEMTECH SC480 ONLY.
For Texas Instruments TPS51116, Please USE Reference BOM.

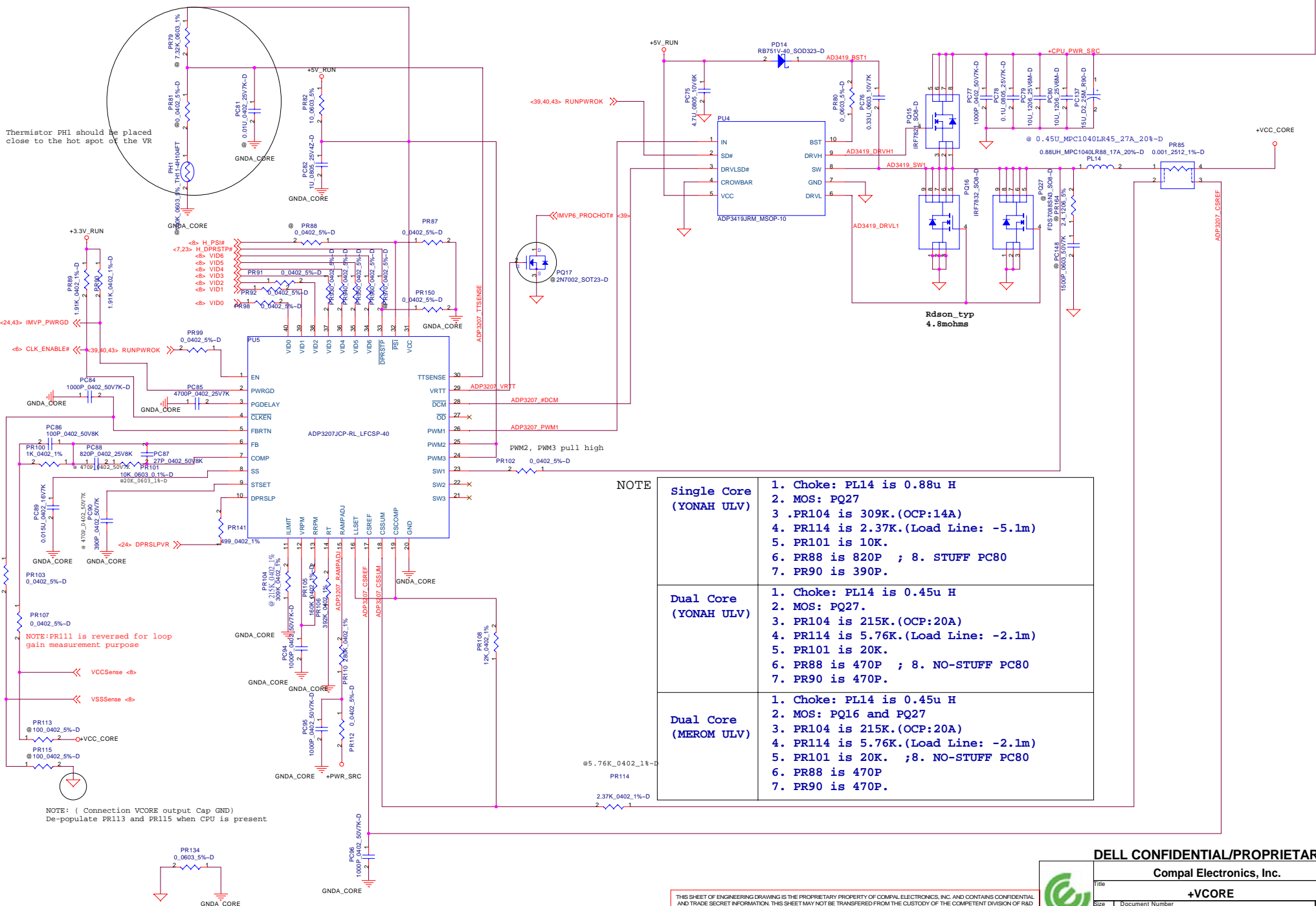
.9 Volt +/- 5%
Design Current:1.05A
Maximum current:1.5A

1.8 Volt +/- 5%
Design Current:3.5A
Maximum current:4.9A
MIN_OCP:5A



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		File +1.8VSUSP/ +0.9V_DDR_VT	
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Thermistor PH1 should be placed close to the hot spot of the VR

<24.43> IMVP_PWRGD

<39.40.43> RUNPWOK

<24> DPRSLPVR

VCCSense

VSSSense

NOTE: (Connection VCORE output Cap GND)
De-populate PR113 and PR115 when CPU is present

<39.40.43> RUNPWOK

<IMVP6_PROCHOT>#39

NOTE

Single Core (YONAH ULV)	<ol style="list-style-type: none"> 1. Choke: PL14 is 0.88u H 2. MOS: PQ27 3. PR104 is 309K.(OCP:14A) 4. PR114 is 2.37K.(Load Line: -5.1m) 5. PR101 is 10K. 6. PR88 is 820P ; 8. STUFF PC80 7. PR90 is 390P.
Dual Core (YONAH ULV)	<ol style="list-style-type: none"> 1. Choke: PL14 is 0.45u H 2. MOS: PQ27. 3. PR104 is 215K.(OCP:20A) 4. PR114 is 5.76K.(Load Line: -2.1m) 5. PR101 is 20K. 6. PR88 is 470P ; 8. NO-STUFF PC80 7. PR90 is 470P.
Dual Core (MEROM ULV)	<ol style="list-style-type: none"> 1. Choke: PL14 is 0.45u H 2. MOS: PQ16 and PQ27 3. PR104 is 215K.(OCP:20A) 4. PR114 is 5.76K.(Load Line: -2.1m) 5. PR101 is 20K. ; 8. NO-STUFF PC80 6. PR88 is 470P 7. PR90 is 470P.

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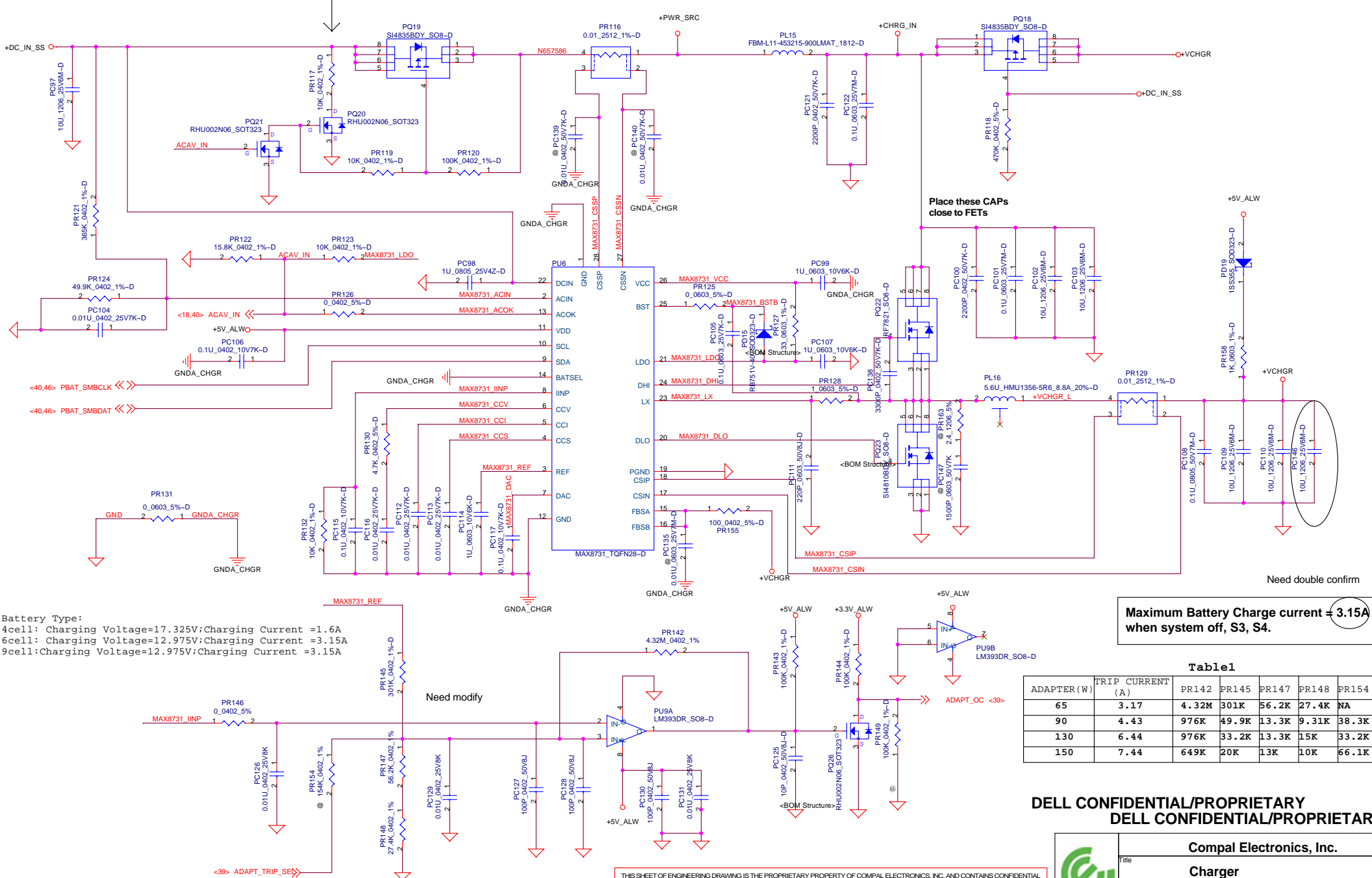
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Title		+VCORE	
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Smart Charger

+DC_IN discharge path



Battery Type:
 4cell: Charging Voltage=17.325V;Charging Current =1.6A
 6cell: Charging Voltage=12.975V;Charging Current = 3.15A
 9cell:Charging Voltage=12.975V;Charging Current = 3.15A

Maximum Battery Charge current = 3.15A when system off, S3, S4.

Table1

ADAPTER (W)	TRIP CURRENT (A)	PR142	PR145	PR147	PR148	PR154
65	3.17	4.32M	301K	56.2K	27.4K	NA
90	4.43	976K	49.9K	13.3K	9.31K	38.3K
130	6.44	976K	33.2K	13.3K	1.5K	33.2K
150	7.44	649K	20K	13K	10K	66.1K

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Compal Electronics, Inc.
Charger
LA-3741P

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	16,17	DDR On board	01/09/07'	Compal	Update Memory symbol form 64M*8 to 128M*8	Update U4~U11 Symbol	0.1
2	17	DDR On board	01/09/07'	Compal	Add Termination resistors	Add R660 and R661(56_0402)	0.1
3	39	ECE5018	01/09/07'	Compal	Setting board ID from A00(Crockett) to X00(Carson)	Pop R475 and depop R471	0.1
4	29,40	LOM	01/11/07'	Dell	Support ASF2.0	MEC5004 pin55(SGPI045) connect to BCM5752 ball H9 (GPIO0), net name is LOM_SMB_ALERT# ; Add R662(4.7K ohm)pull up resistor to +3.3V_LAN	0.1
5	50	SPI ROM	01/23/07'	Dell	Add code to support different version of WLAN.	Change U50 from M25P16-VMW6TP(1M) to M25P16-VMW6TP(2M)	0.1
6	37	IrDA	01/23/07'	Dell	For cost saving	Depop U40, R433,R435,R436,C526~C528	0.1
7	28		01/23/07'	Dell	For best audio performance(Vista)	Change L28~L31 to BLM18BD601SN1D	0.1
8	33	USB	01/24/07'	Dell	For meet TUV's USB requirement	Reserved F2,F3(depop),JUMP1 and JUMP3. Short Jump for X00 build.	0.1


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Title Changed-List History 1			
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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	page 51		1/09/07	Dell	M08 charger update for potential audible noise.	Add PC146 10uf/25V X5R Cap on charger output Cap.	X00
2	page 51		1/26/07	Dell	M08 charger update for EMC.	Add PC147 and PR163 from phase node to GND	X00
3	page 50		1/26/07	Dell	M08 Vcore update for EMC.	Add PC148 and PR164 from phase node to GND	X00

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