FOOSE 15" UMA Schematics Document

uFCPGA Mobile Penryn

Intel Cantiga-GM + ICH9M

2008-06-04

REV : -1

DY : Nopop Component
5761 : Use BCM5761E
5756 : Use BCM5756M
B_TPM : Use LOM TPM
C_TPM : Use China TPM

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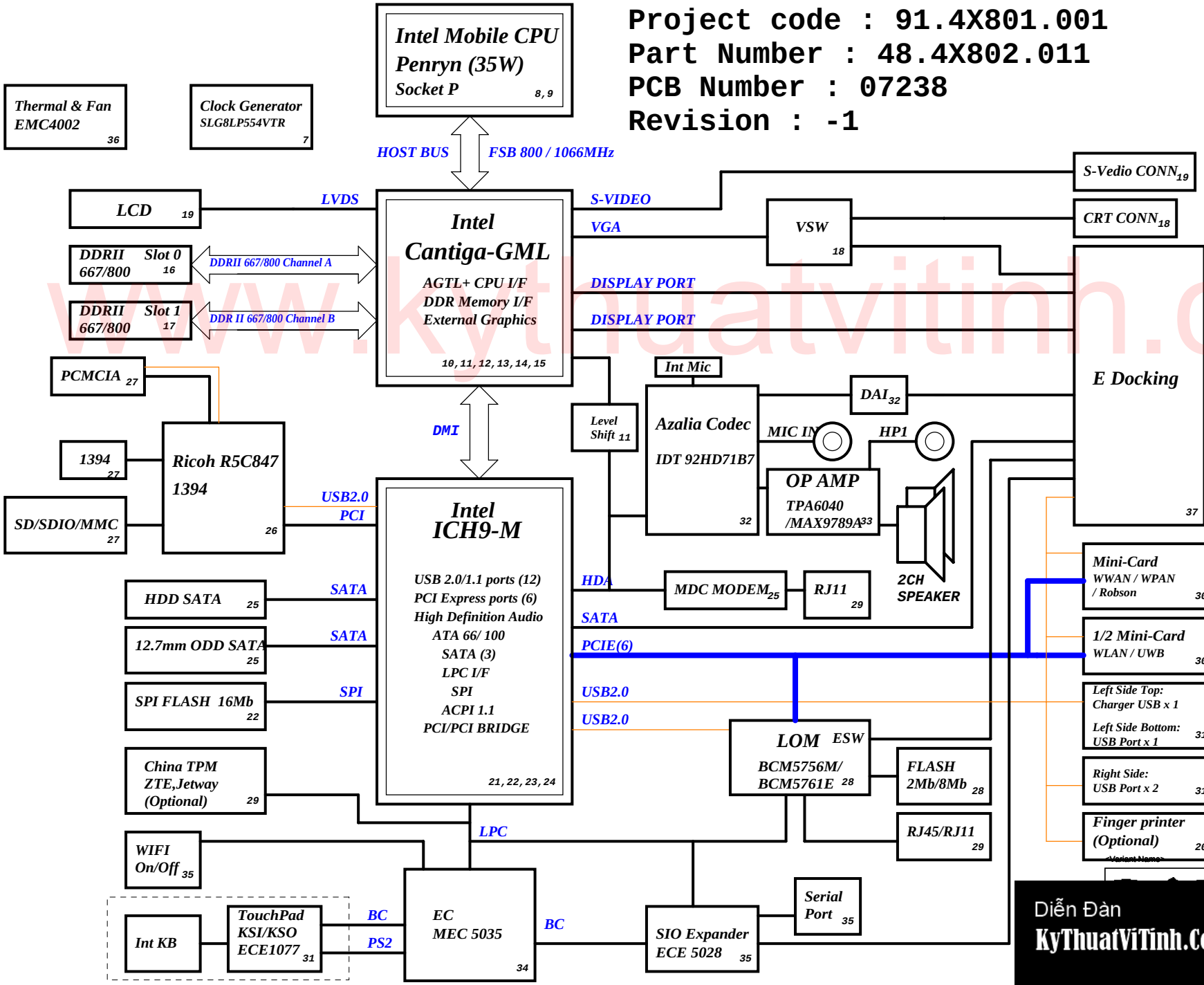
Title	Foose Intel	
Size: A3	Document Number: COVER PAGE	Rev: SC
Date: Wednesday, June 04, 2008	Sheet 1 of 58	

Foose Intel UMA Block Diagram

Project code : 91.4X801.001
Part Number : 48.4X802.011
PCB Number : 07238
Revision : -1



CPU DC/DC ISL6260		
INPUTS	OUTPUTS	
+PWR_SRC	VCC_CORE	43 44

SYSTEM DC/DC SN0608098		
INPUTS	OUTPUTS	
+PWR_SRC	+3.3V_ALW +5V_ALW	45

SYSTEM DC/DC TPS5117		
INPUTS	OUTPUTS	
+PWR_SRC	+1.05V_VCCP	46

SYSTEM DC/DC L6935TR(LDO)		
INPUTS	OUTPUTS	
+1.8V_SUS	+1.5V_RUN	46

SYSTEM DC/DC TPS5116		
INPUTS	OUTPUTS	
+PWR_SRC	+1.8V_SUS	47

SYSTEM DC/DC TPS5116(LDO)		
INPUTS	OUTPUTS	
+1.8V_SUS	+V_DDR_MCH_REF +0.9V_DDR_VTT	47

SYSTEM DC/DC EMC4002(LDO)		
INPUTS	OUTPUTS	
+3.3V_RUN	+2.5V_RUN	36

TI CHARGER BQ24745		
INPUTS	OUTPUTS	
+DC_IN +VCHGR	+PWR_SRC	42

Digitally signed by dd
DN: cn=dd, ou=dd,
email=dddd@yahoo.com,
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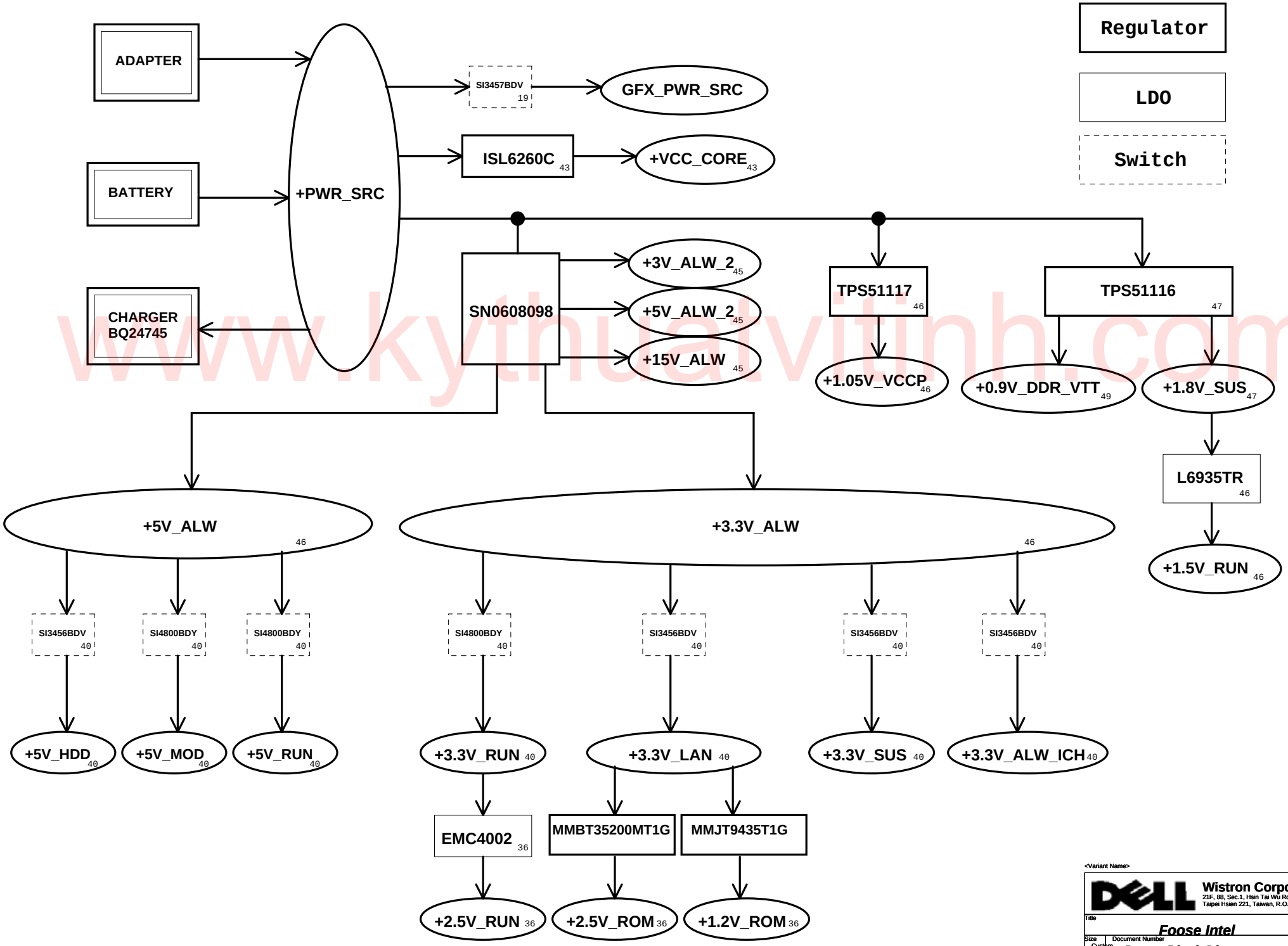
Size: Intel | Date: 2009.12.04 19:36:07 | Sheet 2 of 58 | Rev SC



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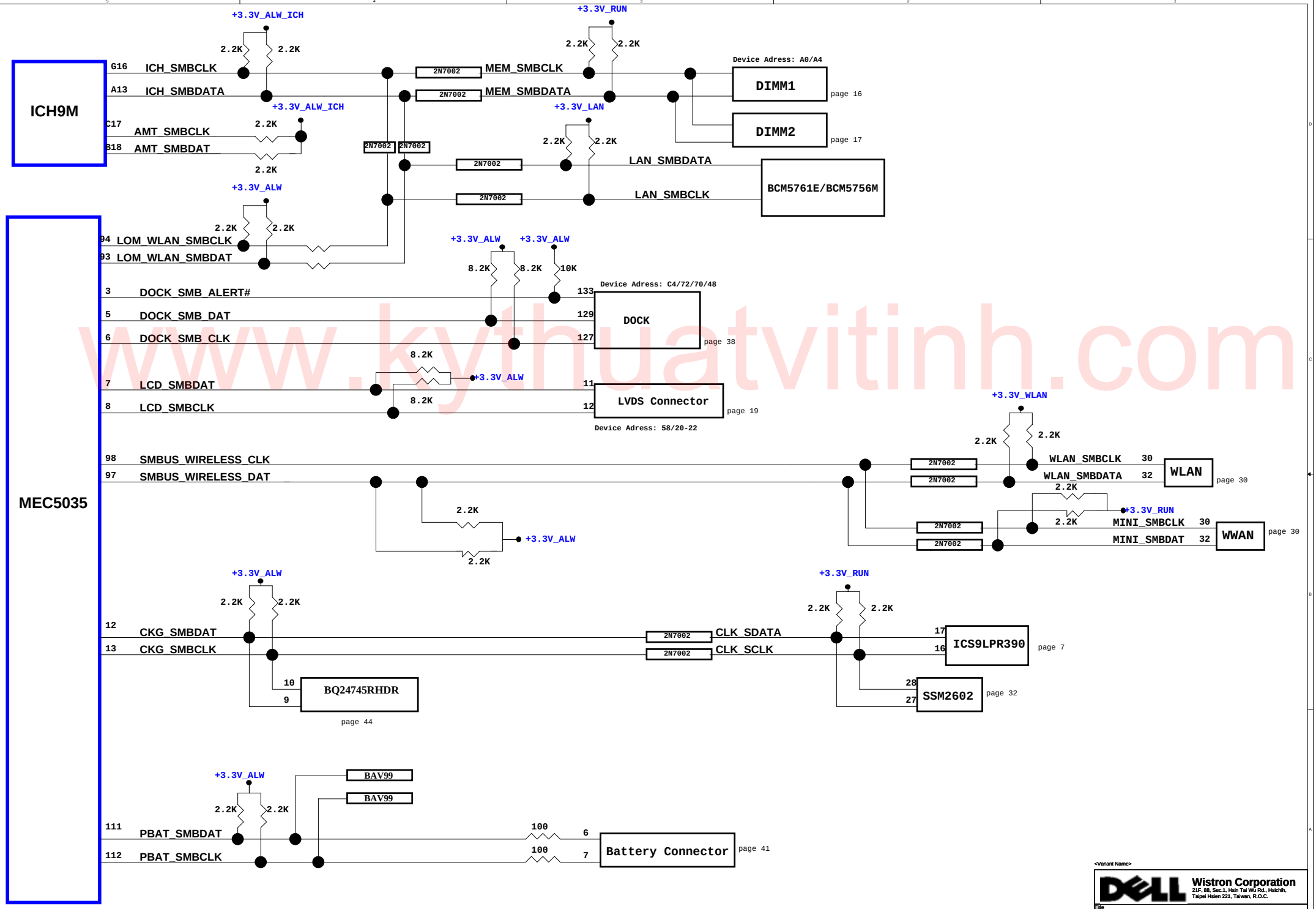
Title: Foose Intel

Size: Custom | Document Number: Power Block Diagram | Rev: SC

Date: Friday, May 30, 2008 | Sheet 3 of 58



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Title: Foose Intel

Size: A2 | Document Number: SMBus Block Diagram | Rev: SC

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INTEL ICH9-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK. When TP3 not pulled low at rising edge of PWROK, sets bit 1 of RPC.PC (Chipset Config Registers: Offset224h).This signal has a weak internal pull-down.
HDA_SYNC	PCIE Port Config 1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit 0 of RPC.PC (Chipset Config Registers: Offset 224h)
GNT2# / GPIO53	PCIE Port Config 2 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit 2 of RPC.PC2 (Chipset Config Registers:Offset 0224h) when sampled low.
GPIO20	Reserved	This signal has a weak internal pull-down. NOTE: This signal should not be pulled high
GNT1#/ GPIO51	ESI Strap, Rising Edge of PWROK.	Tying this strap low configures DMI for ESI compatible operation. This signal has a weak internal pull-up. NOTE: ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3# / GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	The signal has a weak internal pull-up. If the signal is sampled low, this indicates that the system is strapped to the "top-block swap" mode (IntelR ICH9 inverts A16 for all cycles targeting BIOS space). The status of this strap is readable via the Top Swap bit (Chipset Config Registers:Offset 3414h:bit 0). Note that software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	This field determines the destination of accesses to the BIOS memory range. Signals have weak internal pull-ups. Also controllable via Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:bit 11).This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.
SATALED#	PCIE LAN REVERSAL.Rising Edge of PWROK.	Signal has weak internal pull-up.Sets bit 27 of MPC.LR (Device 28: Function 0: Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	The signal has a weak internal pull-down. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (ICH9 will disable the TCO Timer system reboot feature). The status of this strap is readable via the NO REBOOT bit (Chipset Config Registers:Offset 3410h:bit 5).
TP3	XOR Chain Entrance. Rising Edge of PWROK.	See IntelR ICH9 Family XOR Chains In-Circuit Tester Package for functionality information. This signal has a weak internal pull-up. NOTE: This signal should not be pulled low unless using XOR Chain testing.
GPIO33 / HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	This signal has a weak internal pull-up resistor. If sampled low, the Flash Descriptor Security will be overridden. If high, the security measures defined in the Flash Descriptor will be in effect.NOTE: This strap should only be enabled in manufacturing environments.
GPIO49	DMI Termination Voltage Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SPI_MOSI	Integrated TPM Enable Rising Edge of PWROK.	This signal has a weak internal pull-down resistor. When the signal is sampled low the Integrated TPM will be disabled. When the signal is sampled high, the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enabled.NOTE: This signal is required to be floating or pulled low for desktop applications.

XOR Chain Entrance Strap

ICH_RSVD_tp3	AZ_DOUT_ICH	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation(default)
1	1	Set PCIE port cofig bit1

A16 swap override strap

PCI_GNT#3	low = A16 swap override enable
	high = default

BOOT BIOS Strap

PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

Enable VccSus1_05,VccSus1_5,VccCL1_5

SM_INTVRMEN	High=Enable	Low=Disable

integrated VccLan1_05VccCL1_05

LAN100_SLP	High=Enable	Low=Disable

No Reboot Strap

SPKR	LOW = Defaule
	High=No Reboot

PCIE Routing

LANE1	MiniCard WWAN
LANE2	MiniCard WLAN
LANE3	No use
LANE4	No use
LANE5	GIGA LAN
LANE6	No use

SATA Routing

SATA0	HDD
SATA1	ODD
SATA4	No use
SATA5	Dock eSATA

PCI ROUTING

	IDSEL	INT	REQ	GNT
1394/ MediaCard	AD17	1	B C D	1

USB TABLE

USB	
Pair	Device
0	Charge USB (LEFT SIDE TOP)
1	USB1(LEFT SIDE BOTTOM)
2	USB2(RIGHT SIDE TOP)
3	USB3(RIGHT SIDE BOTTOM)
4	WLAN
5	WWAN/WPAN
6	Reserve
7	Card Bus/Express Card
8	DOCK1
9	DOCK2
10	Biometric
11	BCM5761E

ICH9-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 10K
DPRSLPVR/GPIO16	PULL-DOWN 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LAD[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

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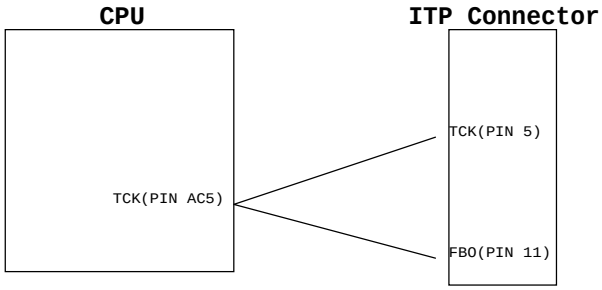

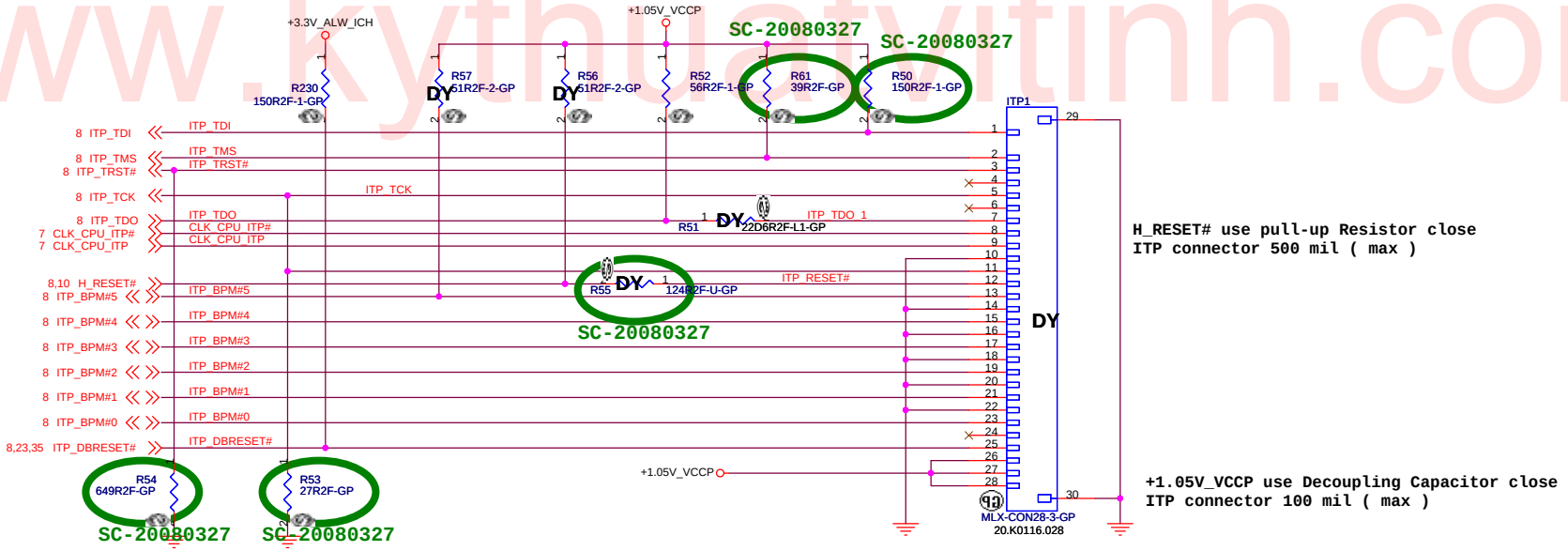

ITP Debug Connector

5756

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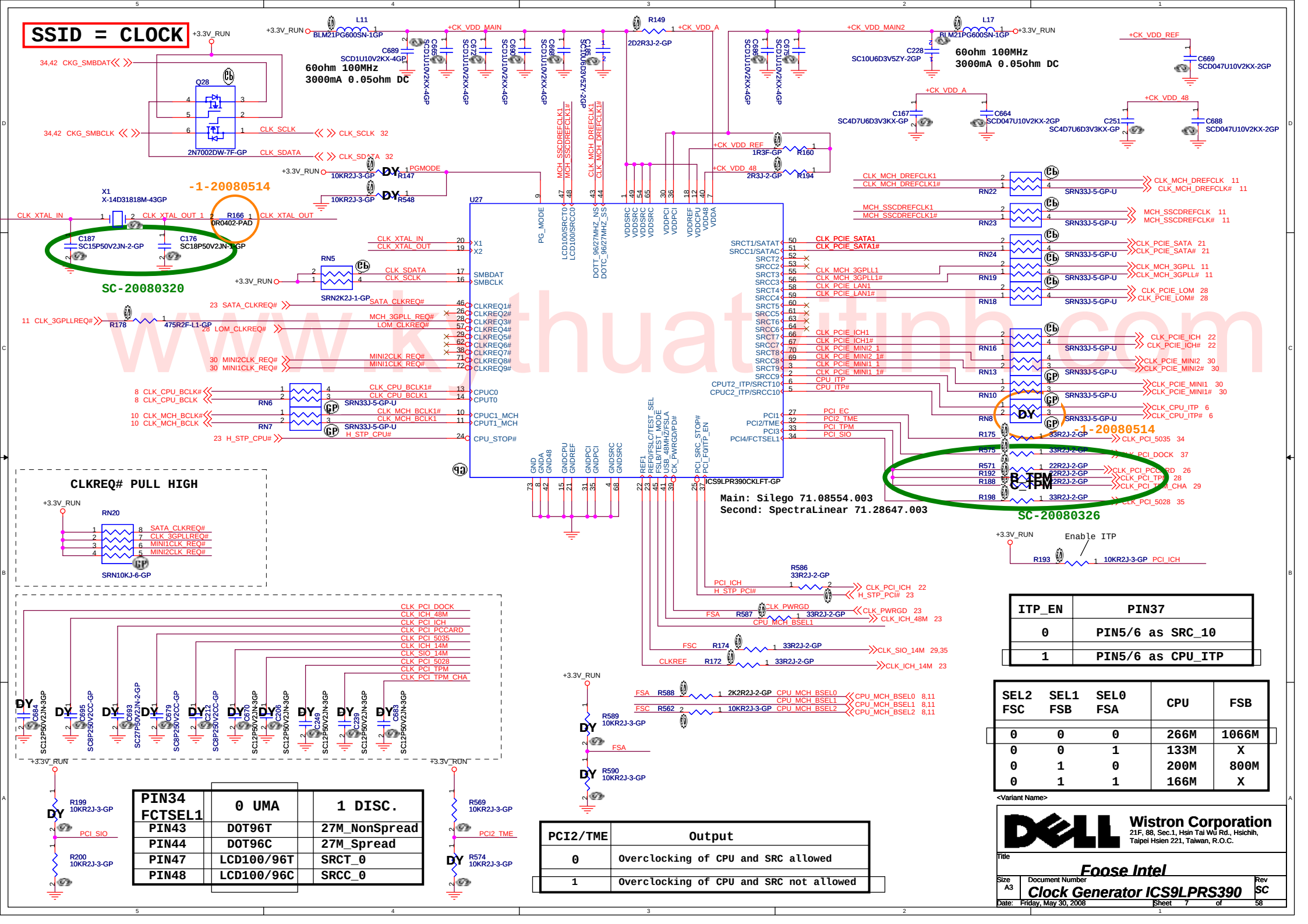
Title	*Foose Intel*	
Size A3	Document Number *ITP Debug Connector*	Rev SC
Date: Friday, May 30, 2008	Sheet 6 of 58	

SSID = CLOCK



PIN34 FCTSEL1	0 UMA	1 DISC.
PIN43	DOT96T	27M_NonSpread
PIN44	DOT96C	27M_Spread
PIN47	LCD100/96T	SRCT_0
PIN48	LCD100/96C	SRCC_0

PCI2/TME	Output
0	Overclocking of CPU and SRC allowed
1	Overclocking of CPU and SRC not allowed

ITP_EN	PIN37
0	PIN5/6 as SRC_10
1	PIN5/6 as CPU_ITP

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
0	0	0	266M	1066M
0	0	1	133M	X
0	1	0	200M	800M
0	1	1	166M	X

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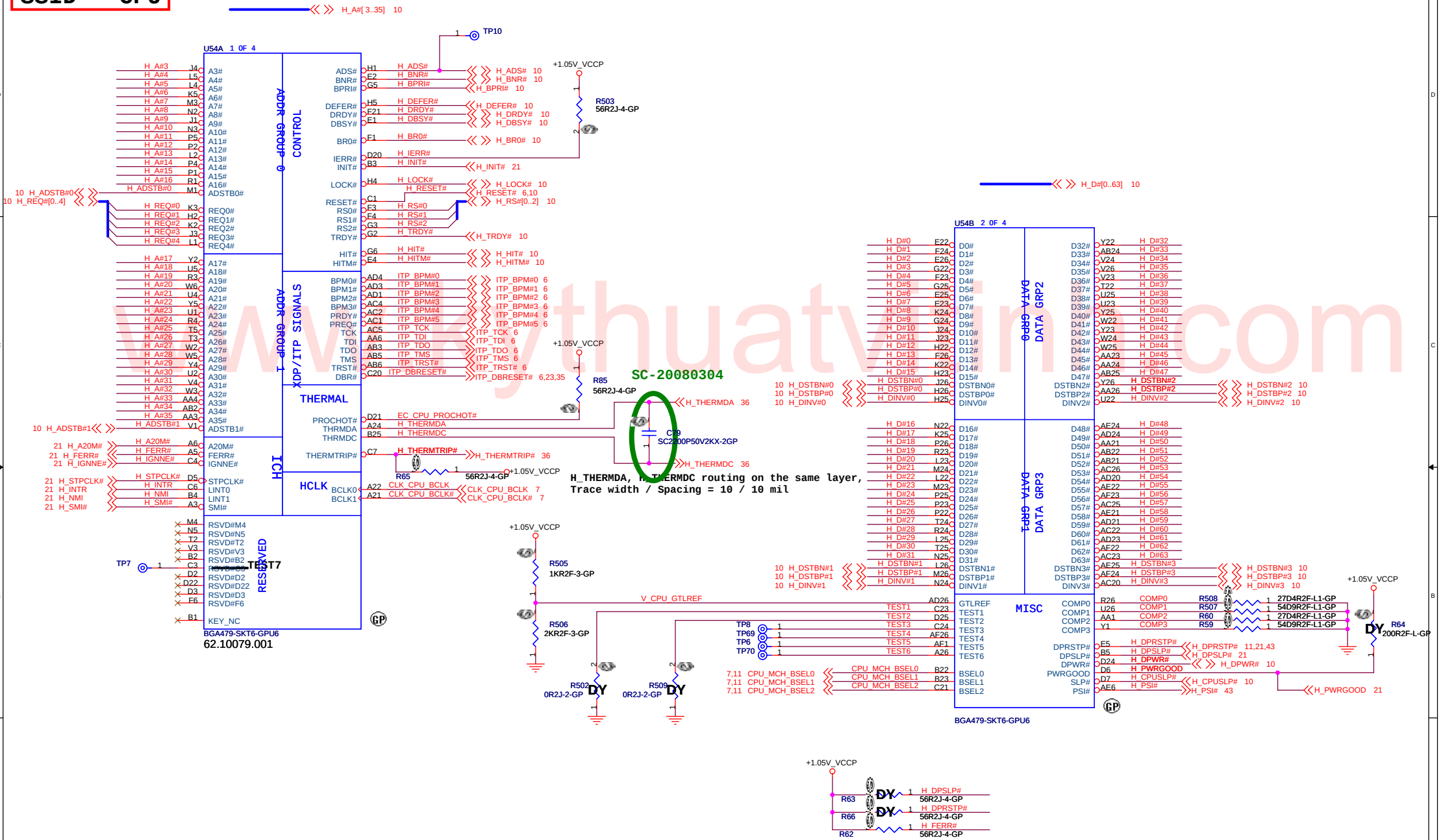
Title: Foose Intel

Size: A3 | Document Number: Clock Generator ICS9LPRS390 | Rev: SC

Date: Friday, May 30, 2008 | Sheet 7 of 58

SSID = CPU



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Title: Foose Intel

Size	Document Number	Rev
A3	CPU-FSB(1/2)	SC

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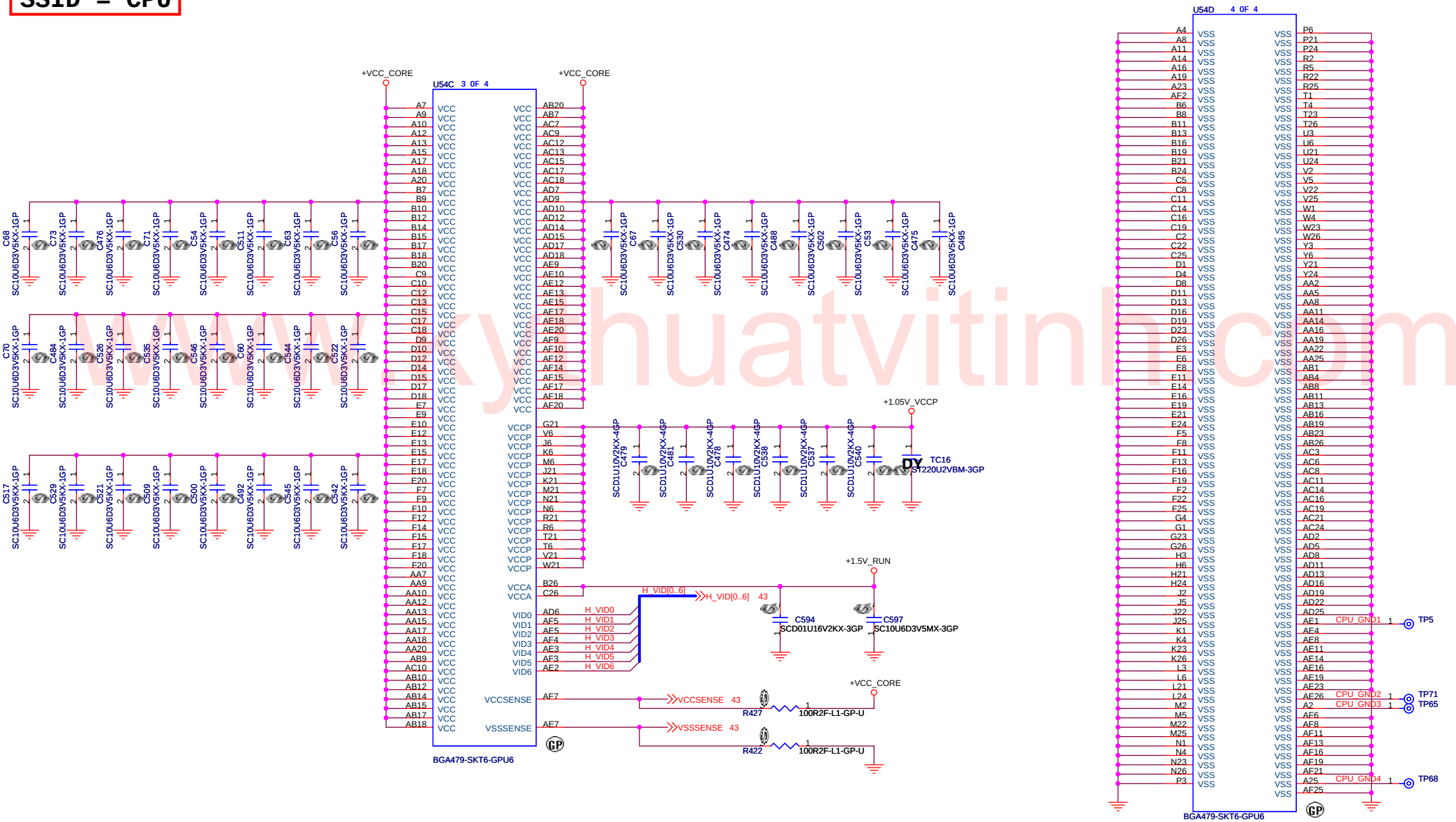
SSID = CPU



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Size: A3 | Document Number: CPU-POWER(2/2) | Rev: SC

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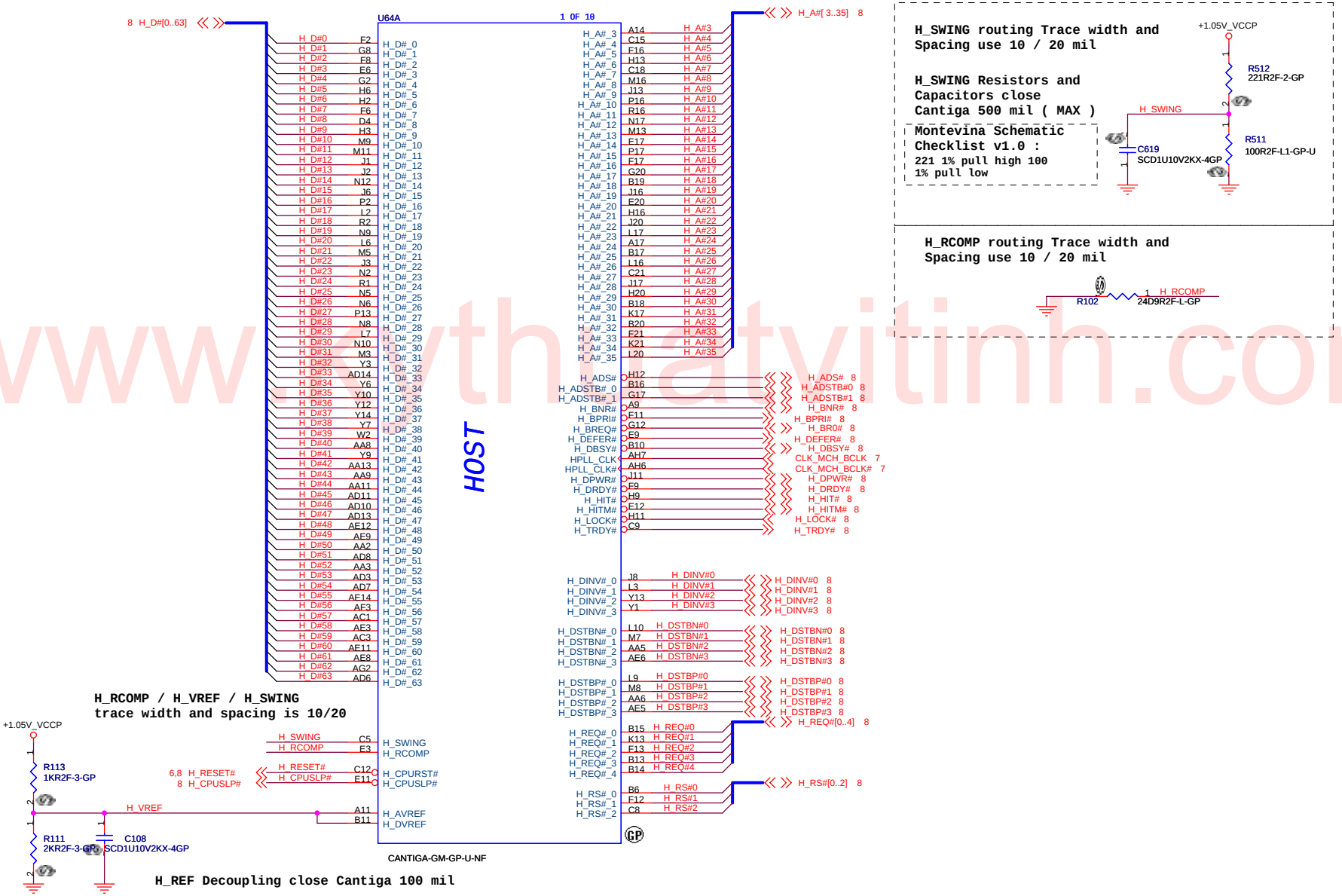
SSID = MCH

NB Nwe Part Number
71.CNTIG.G0U



H_SWING routing Trace width and Spacing use 10 / 20 mil

H_SWING Resistors and Capacitors close Cantiga 500 mil (MAX)

Montevina Schematic Checklist v1.0 :
221 1% pull high 100
1% pull low

H_RCOMP routing Trace width and Spacing use 10 / 20 mil

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Size	Document Number	Rev
A3	CANTIGA-FSB(1/6)	SC

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SSID = MCH

* is current setting

CFG Strap	Low	High
CFG 5	DMI X 2	DMI X 4 *
CFG 6	ITPM enable	ITPM disable *
CFG 7	TLS cipher suite with no confidentiality	TLS cipher suite with confidentiality *
CFG 9	Reverse Lanes	Normal Operation *
CFG 16	FSB dynamic ODT disable	FSB Dynamic ODT enable *
CFG 19 DMI Lane Reserved	Normal operation *	Reverse DMI lanes
CFG 20 PCIE/SDVO Select	Only PCIE or SDVO is operational *	PCIE and SDVO are operatiing simultaneously
SDVO_CTRLDATA	iHDMI/DP interface disabled	iHDMI/DP interface enabled *
DDPC_CTRLDATA	SDVO/iHDMI/DP interface disabled	SDVO/iHDMI/DP interface enabled *

U64B — 2 OF 10

RSVD: RESERVED#M36, RESERVED#N36, RESERVED#R33, RESERVED#T33, RESERVED#AH9, RESERVED#AH10, RESERVED#AH12, RESERVED#AH13, RESERVED#K12, RESERVED#AL34, RESERVED#AK34, RESERVED#AN35, RESERVED#AM35, RESERVED#T24, RESERVED#B31, RESERVED#B2, RESERVED#M1, RESERVED#AY21, RESERVED#BG23, RESERVED#BF23, RESERVED#BH18, RESERVED#BF18

DDR CLK/ CONTROL/COMPENSATION: SA_CK_0/1, SB_CK_0/1, SA_CK#_0/1, SB_CK#_0/1, SA_CKE_0/1, SB_CKE_0/1, SA_CS#_0/1, SB_CS#_0/1, SA_ODT_0/1, SB_ODT_0/1, SM_RCOMP, SM_RCOMP#, SM_RCOMP_VOH, SM_RCOMP_VOL, SM_VREF, SM_PWROK, SM_REXT, SM_DRAMRST#

CLK: DPLL_REF_CLK, DPLL_REF_CLK#, DPLL_REF_SSCLK, DPLL_REF_SSCLK#, PEG_CLK, PEG_CLK#

DMI: DMI_RXN_0..3, DMI_RXP_0..3, DMI_TXN_0..3, DMI_TXP_0..3

CFG: CFG_0..CFG_20

PM: PM_SYNC#, PM_DPRSTP#, PM_EXT_TS#_0, PM_EXT_TS#_1, PWROK, RSTIN#, THERMTRIP#, DPRSLPVR

GRAPHICS VID: GFX_VID_0..4, GFX_VR_EN

ME: CL_CLK, CL_DATA, CL_PWROK, CL_RST#, CL_VREF

MISC: DDPC_CTRLCLK, DDPC_CTRLDATA, SDVO_CTRLCLK, SDVO_CTRLDATA, CLKREQ#, ICH_SYNC#, TSATN#

HDA: HDA_BCLK, HDA_RST#, HDA_SDI, HDA_SDO, HDA_SYNC

NC: NC#BG48, NC#BF48, NC#BD48, NC#BC48, NC#BH47, NC#BG47, NC#BE47, NC#BH46, NC#BF46, NC#BG45, NC#BH44, NC#BH43, NC#BH6, NC#BH5, NC#BG4, NC#BH3, NC#BF3, NC#BH2, NC#BG2, NC#BE2, NC#BG1, NC#BF1, NC#BD1, NC#BC1, NC#F1, NC#A47

CANTIGA-GM-GP-U-NF

Please place it near ICH9(U73).

-1-20080514 — R373 0R0402-PAD

-1-20080522 — +1.5V_RUN, C7279 SCD1U10V2KX-4GP, C7280 SCD1U10V2KX-4GP, +3.3V_LEVELSHIFT

U90 FXL2SD106BQX-GP: CLK_IN, CLK_OUT, B0, B1, B2, B3, NC#17, GND, VCCA, VCCB, A0, A1, A2, A3, CMD_A, CMD_B, OE

ICH_AZ_MCH_RST# → ICH_AZ_MCH_RST#_R R359 33R2J-2-GP GMCH_HDA_RST#
ICH_AZ_MCH_SDOUT → ICH_AZ_MCH_SDOUT_R R355 33R2J-2-GP GMCH_HDA_SDOUT
ICH_AZ_MCH_SYNC → ICH_AZ_MCH_SYNC_R R379 33R2J-2-GP GMCH_HDA_SYNC
MCH_SDIN2
ICH_AZ_MCH_BITCLK_R R363 33R2J-2-GP GMCH_HDA_BITCLK
ICH_AZ_MCH_BITCLK_R 21
ICH_AZ_MCH_SDIN2 — R377 33R2J-2-GP

-1-20080522 — +3.3V_LEVELSHIFT, R455 10KR2F-2-GP, R8154 8K25R2F-1-GP, C377 SC100P50V2JN-3GP

SC-20080328

+3.3V_RUN — R144 DY 4K02R2F-GP CFG19; R145 DY 4K02R2F-GP CFG20; R135 DY 2K21R2F-GP CFG5; R131 DY 2K21R2F-GP CFG6; R124 DY 2K21R2F-GP CFG7; R119 DY 2K21R2F-GP CFG9; R121 DY 2K21R2F-GP CFG16

TP82 R563 TP87 R570 TP80 R558 TP85 R567 DY 100R2J-2-GP: ME_JTAG_TCK, ME_JTAG_TDI, ME_JTAG_TDO, ME_JTAG_TMS

TP12, TP78, TP72, TP16, TP77, TP21, TP75

7,8 CPU_MCH_BSEL0/1/2 → CPU_MCH_BSEL0/1/2

TP15, TP23, TP22, TP76, TP19, TP18, TP20, TP13, TP14, TP17, TP24

-1-20080514 — R411 0R0402-PAD

23 PM_SYNC# → PM_SYNC#; 8,21,43 H_DPRSTP# → H_DPRSTP#; PM_EXTTS#0_1; 36 PM_EXTTS#

22 PLTRST1# → PLTRST1#_R; R510 100R2J-2-GP; 23,43 DPRSLPVR

23,41 ICH_PWRGD; 36 THERMTRIP_MCH# → THERMTRIP_MCH#; DPRSLPVR

+1.05V_VCCP — R128 56R2J-4-GP

RN9 SRN10KJ-5-GP

+1.8V_SUS — R525 80D6R2F-L-GP; R520 80D6R2F-L-GP; R539 1KR2F-3-GP; R534 3K01R2F-3-GP; R530 1KR2F-3-GP; C652 SC2D2U6D3V3KX-GP; C650 SCD01U16V2KX-3GP; C647 SC2D2U6D3V3KX-GP; C648 SCD01U16V2KX-3GP

+V_DDR_MCH_REF — C205 SCD1U10V2KX-4GP; C192 SCD1U10V2KX-4GP

-1-20080514 — R164 0R0402-PAD

Use for DDR3 signls, if support DDR2 need connect to GND

R123 499R2F-2-GP; TP25

SC-20080303

RN15 SRN2K2J-1-GP: SDVO_CTRLCLK, SDVO_CTRLDATA

RN4 SRN2K2J-1-GP: DDPC_CTRLCLK, DDPC_CTRLDATA

+3.3V_RUN

+1.05V_VCCP — R152 1KR2F-3-GP; R162 499R2F-2-GP; C173 SCD1U10V2KX-4GP; R106 330R2J-3-GP; R110 54D9R2F-L1-GP

+3.3V_RUN — RN3 SRN1KJ-7-GP

MCH_TSATN_EC ↔ MCH_TSATN_EC 35

TSATN# 1 — Q24 PMBS3904-1-GP; Q22 PMBS3904-1-GP

MCH_ICH_SYNC# 23; CLK_3GPLLREQ# 7; MCH_TSATN# 1

R158 33R2J-2-GP MCH_SDIN2

SC-20080328

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Size: Custom | Document Number: CANTIGA-DMI/CFG(2/6) | Rev: SC

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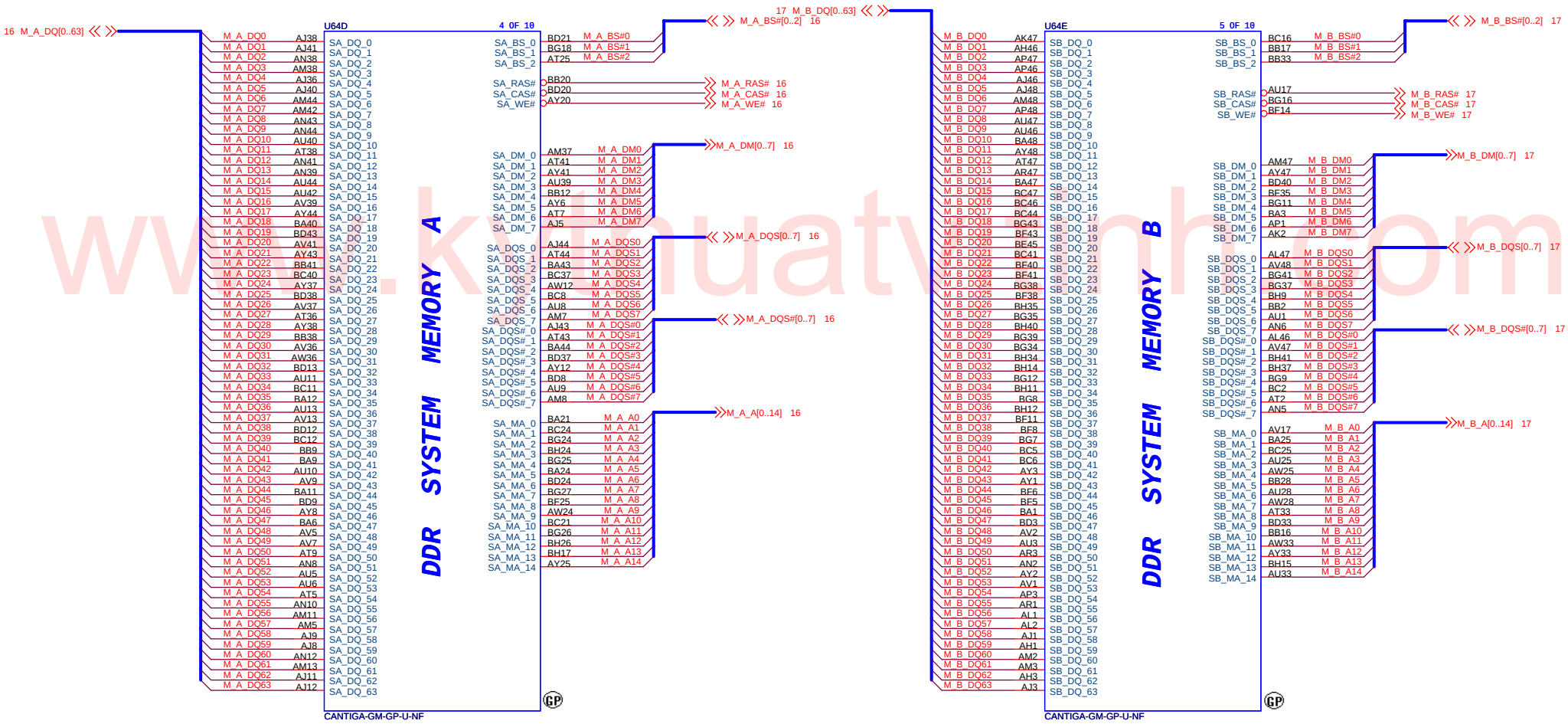
SSID = MCH



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Title: Foose Intel

Size	Document Number	Rev
A3	CANTIGA-DDR	SC

Date: Friday, May 30, 2008 Sheet 12 of 58

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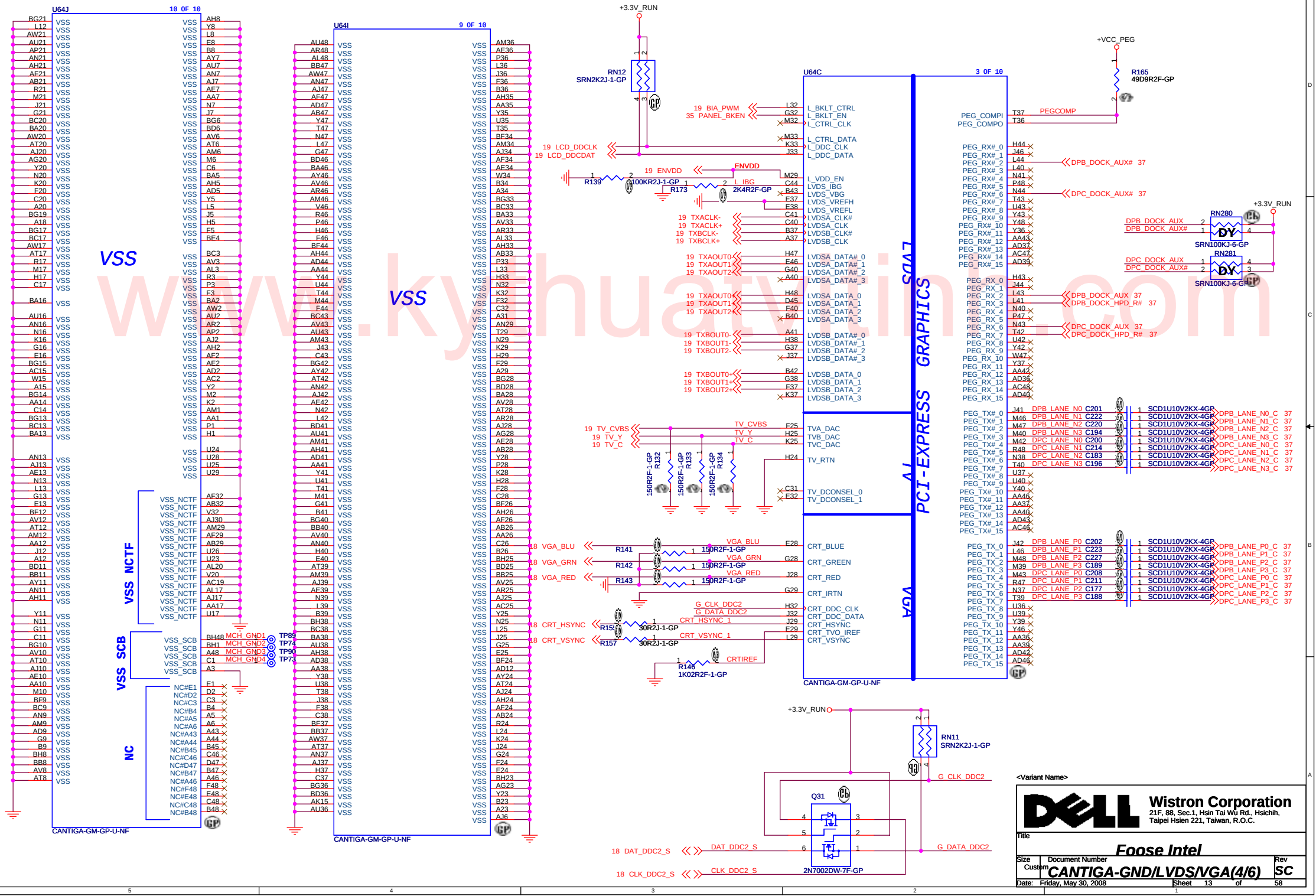

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Size: Custom | Document Number: CANTIGA-GND/LVDS/VGA(4/6) | Rev: SC

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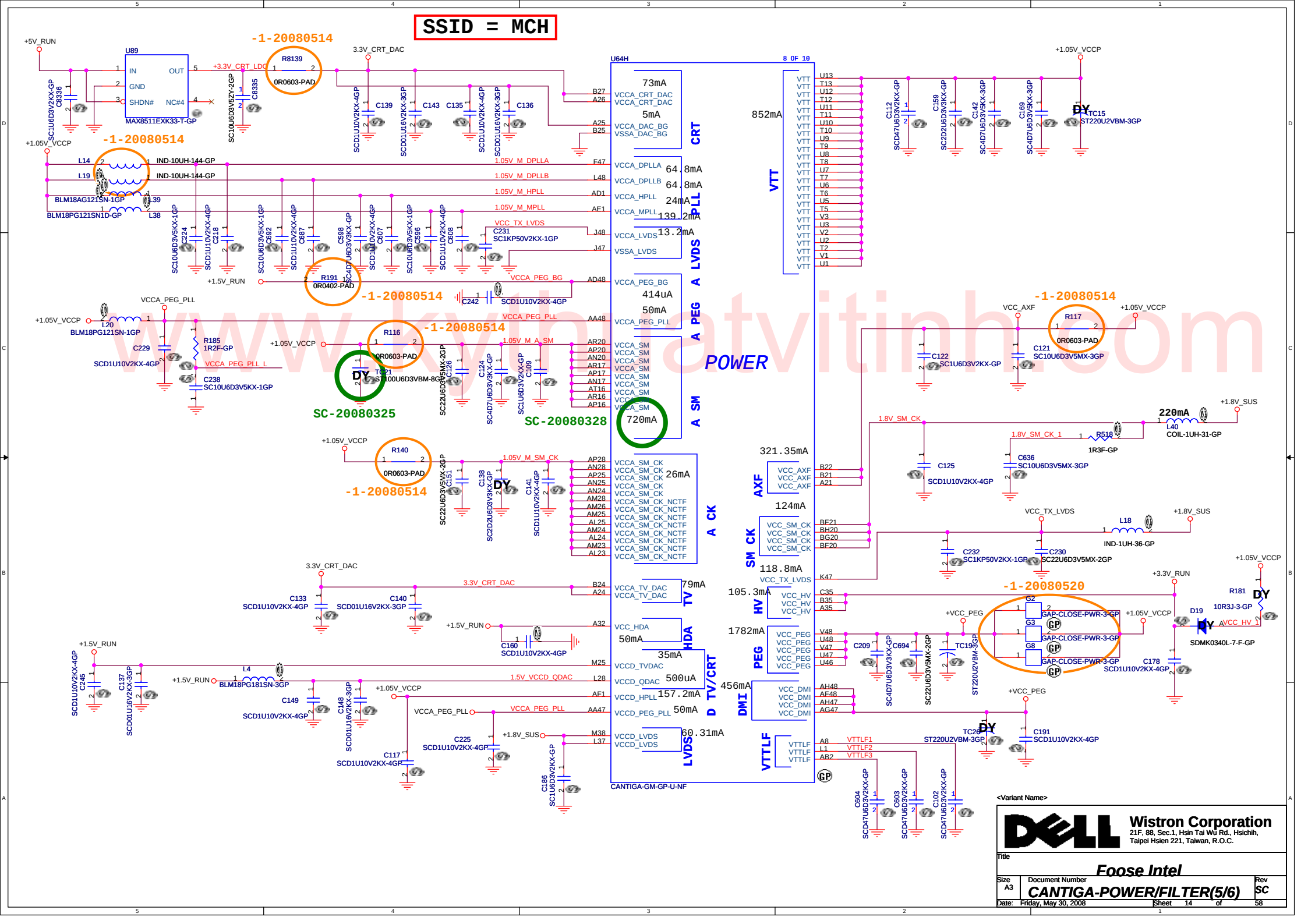
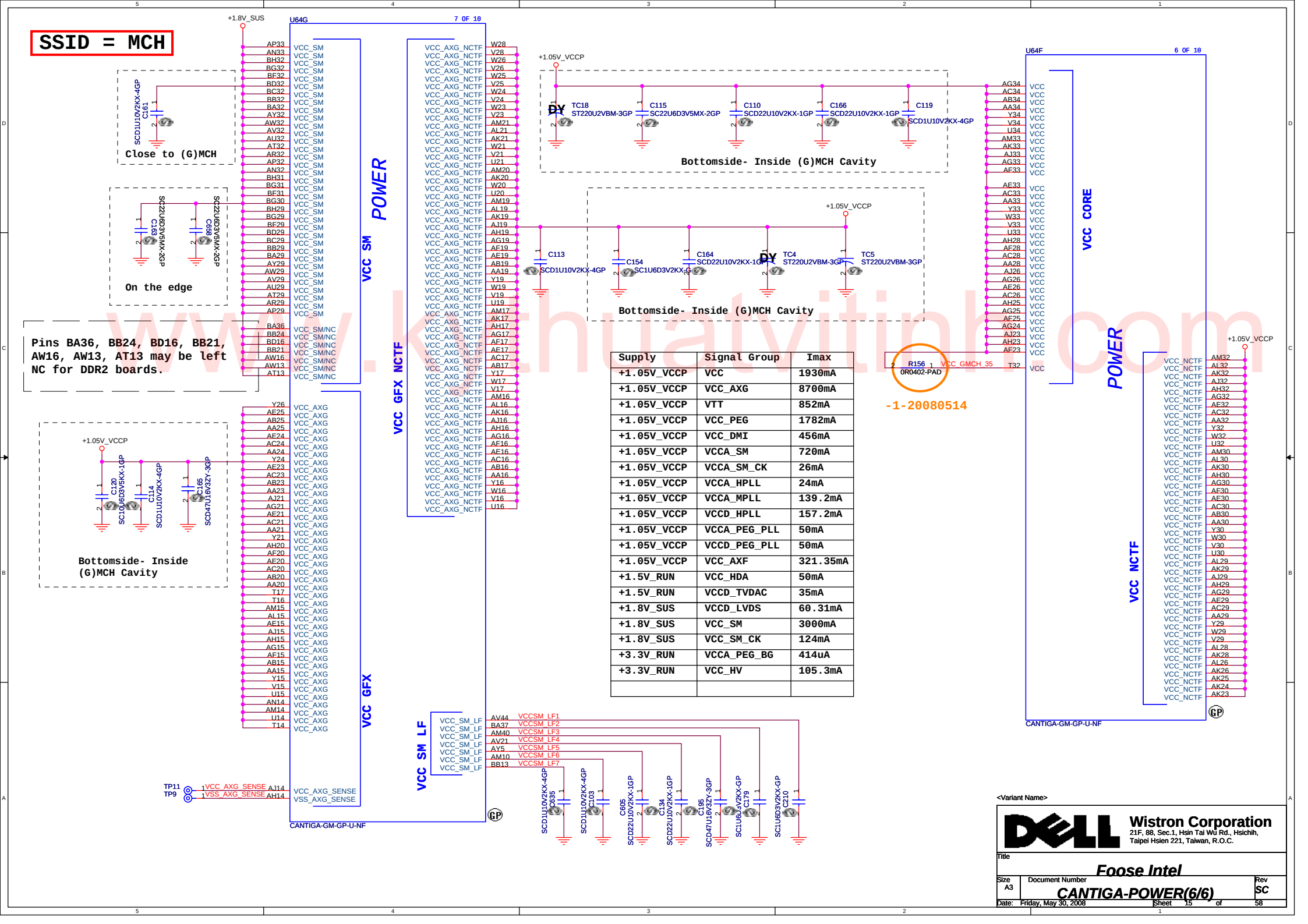

SSID = MCH
U89
MAX8511EXK33-T-GP
R8139
0R0603-PAD
-1-20080514
U64H
8 OF 10
CANTIGA-GM-GP-U-NF
POWER
CRT
PLL
LVDS
PEG
SM CK
AXF
HV
TV/CRT
DMI
VTTLF
HDA
VTT
SC-20080325
SC-20080328
-1-20080520
R191
0R0402-PAD
R116
R140
R117
R181
10R3J-3-GP
L20
BLM18PG121SN-1GP
L14
L19
IND-10UH-144-GP
BLM18AG121SN-1GP
L39
BLM18PG121SN1D-GP
L38
L4
BLM18PG181SN-3GP
L40
COIL-1UH-31-GP
L18
IND-1UH-36-GP
D19
SDMK0340L-7-F-GP
R185
1R2F-GP
R518
1R3F-GP
GAP-CLOSE-PWR-3-GP
TC21
ST100U6D3VBM-8GP
TC15
ST220U2VBM-3GP
TC19
TC26
C242
SCD1U10V2KX-4GP
C231
SC1KP50V2KX-1GP
C232
SC1KP50V2KX-1GP
C230
SC22U6D3V5MX-2GP
C238
SC10U6D3V5KX-1GP
C122
SC1U6D3V2KX-GP
C121
SC10U6D3V5MX-3GP
C125
SCD1U10V2KX-4GP
C636
SC10U6D3V5MX-3GP
C160
SCD1U10V2KX-4GP
C225
SCD1U10V2KX-4GP
C117
SCD1U10V2KX-4GP
C191
SCD1U10V2KX-4GP
C178
SCD1U10V2KX-4GP
C209
SC4D7U6D3V3KX-GP
C694
SC22U6D3V5MX-2GP
C604
SCD47U6D3V2KX-GP
C603
SCD47U6D3V2KX-GP
C102
SCD47U6D3V2KX-GP
73mA
5mA
64.8mA
64.8mA
24mA
139.2mA
13.2mA
414uA
50mA
720mA
26mA
79mA
50mA
35mA
500uA
157.2mA
50mA
60.31mA
852mA
321.35mA
124mA
118.8mA
105.3mA
1782mA
456mA
220mA
+5V_RUN
+3.3V_CRT_LDO
+3.3V_CRT_DAC
+1.05V_VCCP
+1.5V_RUN
+1.8V_SUS
VCCA_PEG_PLL
VCC_TX_LVDS
+VCC_PEG
VCC_AXF
1.8V_SM_CK
1.8V_SM_CK_1
VCCA_PEG_PLL_L
1.05V_M_DPLLA
1.05V_M_DPLLB
1.05V_M_HPLL
1.05V_M_MPLL
1.05V_M_A_SM
1.05V_M_SM_CK
1.5V_VCCD_QDAC
VCC_HV_1
DY
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Foose Intel
Size A3
Document Number CANTIGA-POWER/FILTER(5/6)
Rev SC
Date: Friday, May 30, 2008
Sheet 14 of 58

SSID = MCH



Supply	Signal Group	Imax
+1.05V_VCCP	VCC	1930mA
+1.05V_VCCP	VCC_AXG	8700mA
+1.05V_VCCP	VTT	852mA
+1.05V_VCCP	VCC_PEG	1782mA
+1.05V_VCCP	VCC_DMI	456mA
+1.05V_VCCP	VCCA_SM	720mA
+1.05V_VCCP	VCCA_SM_CK	26mA
+1.05V_VCCP	VCCA_HPLL	24mA
+1.05V_VCCP	VCCA_MPLL	139.2mA
+1.05V_VCCP	VCCD_HPLL	157.2mA
+1.05V_VCCP	VCCA_PEG_PLL	50mA
+1.05V_VCCP	VCCD_PEG_PLL	50mA
+1.05V_VCCP	VCC_AXF	321.35mA
+1.5V_RUN	VCC_HDA	50mA
+1.5V_RUN	VCCD_TVDAC	35mA
+1.8V_SUS	VCCD_LVDS	60.31mA
+1.8V_SUS	VCC_SM	3000mA
+1.8V_SUS	VCC_SM_CK	124mA
+3.3V_RUN	VCCA_PEG_BG	414uA
+3.3V_RUN	VCC_HV	105.3mA

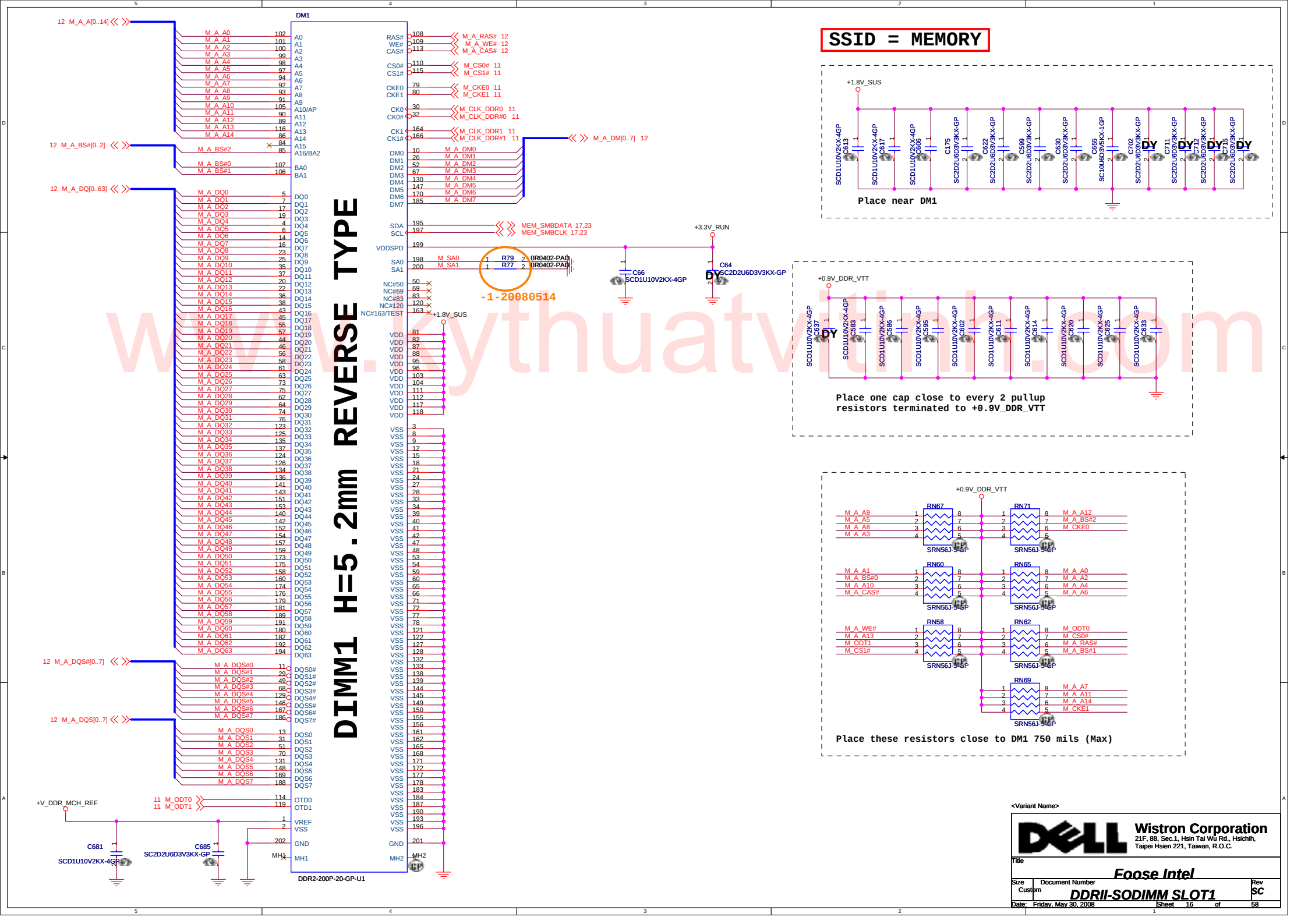
<Variant Name>

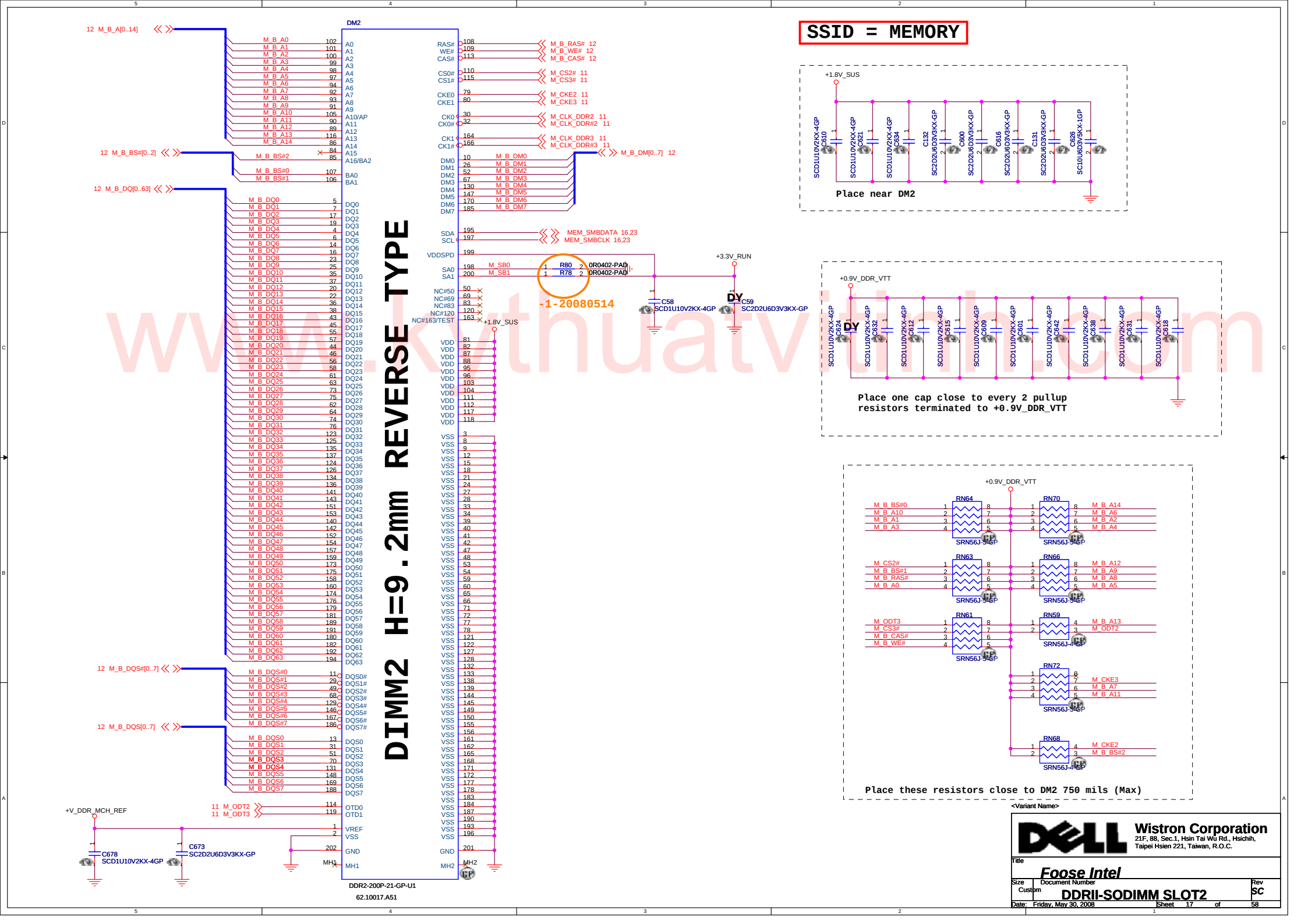
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Foose Intel

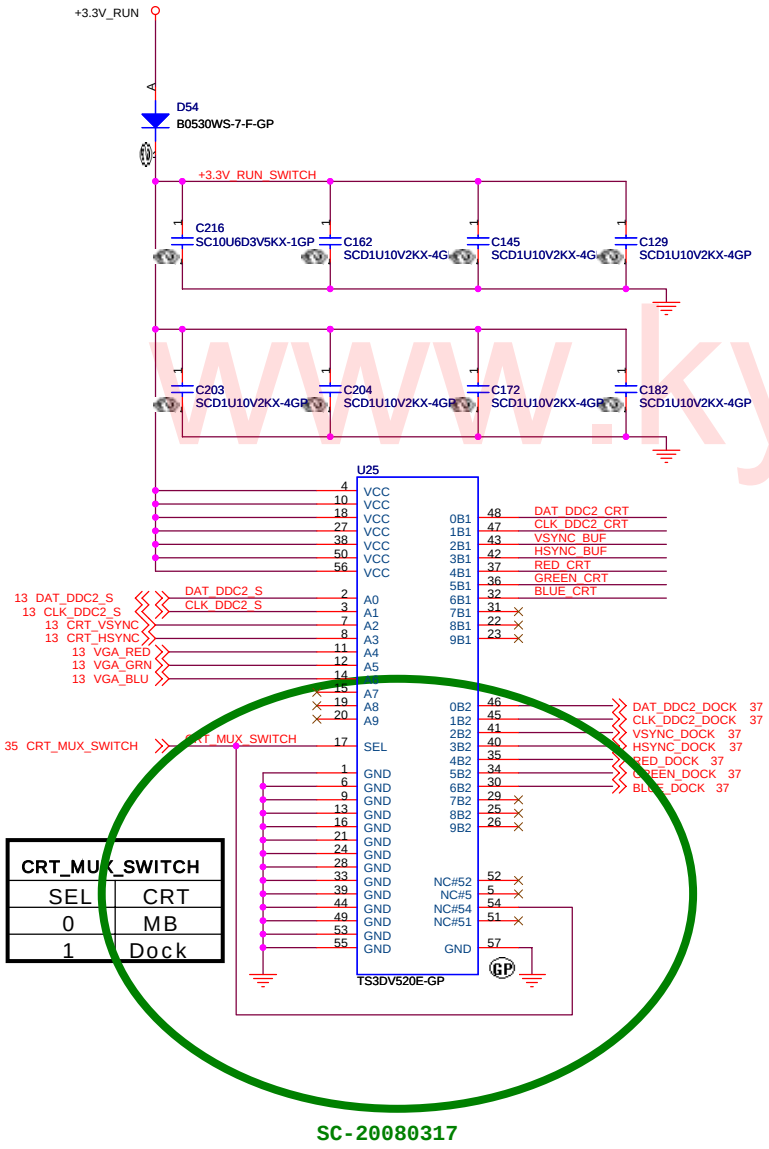
Size: A3 | Document Number: CANTIGA-POWER(6/6) | Rev: SC

Date: Friday, May 30, 2008 | Sheet 15 of 58


DIMM1 H=5.2mm REVERSE TYPE
DM1
DDR2-200P-20-GP-U1
SSID = MEMORY
Place near DM1
Place one cap close to every 2 pullup
resistors terminated to +0.9V_DDR_VTT
Place these resistors close to DM1 750 mils (Max)
-1-20080514
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Foose Intel
DDRII-SODIMM SLOT1
Friday, May 30, 2008
Sheet 16 of 58

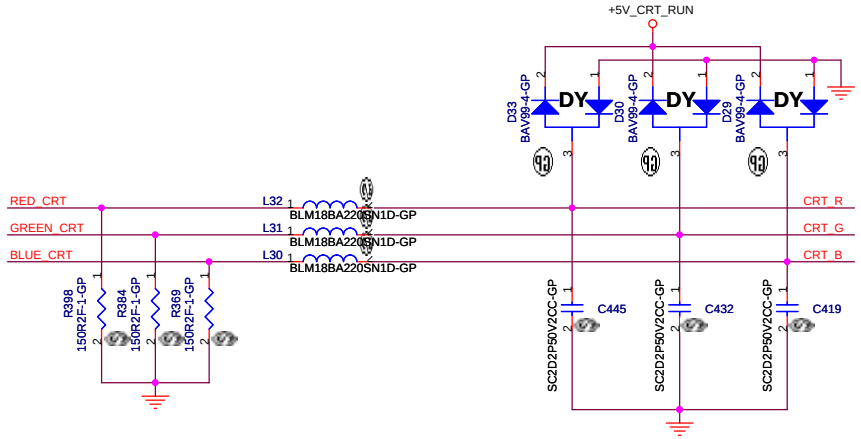

SSID = MEMORY
DIMM2 H=9.2mm REVERSE TYPE
DM2
12 M_B_A[0..14]
12 M_B_BS#[0..2]
12 M_B_DQ[0..63]
12 M_B_DQS#[0..7]
12 M_B_DQS[0..7]
11 M_ODT2
11 M_ODT3
12 M_B_RAS# 12
M_B_WE# 12
M_B_CAS# 12
M_CS2# 11
M_CS3# 11
M_CKE2 11
M_CKE3 11
M_CLK_DDR2 11
M_CLK_DDR2#2 11
M_CLK_DDR3 11
M_CLK_DDR3#3 11
12 M_B_DM[0..7]
MEM_SMBDATA 16,23
MEM_SMBCLK 16,23
M_SB0
M_SB1
R80 0R0402-PAD
R78 0R0402-PAD
-1-20080514
+3.3V_RUN
C58 SCD1U10V2KX-4GP
DY
C59 SC2D2U6D3V3KX-GP
+1.8V_SUS
+V_DDR_MCH_REF
C678 SCD1U10V2KX-4GP
C673 SC2D2U6D3V3KX-GP
DDR2-200P-21-GP-U1
62.10017.A51
+1.8V_SUS
SCD1U10V2KX-4GP C610
SCD1U10V2KX-4GP C621
SCD1U10V2KX-4GP C634
C132 SC2D2U6D3V3KX-GP
C600 SC2D2U6D3V3KX-GP
C616 SC2D2U6D3V3KX-GP
C131 SC2D2U6D3V3KX-GP
C626 SC10U6D3V5KX-1GP
Place near DM2
+0.9V_DDR_VTT
SCD1U10V2KX-4GP C624
DY
SCD1U10V2KX-4GP C632
SCD1U10V2KX-4GP C612
SCD1U10V2KX-4GP C615
SCD1U10V2KX-4GP C609
SCD1U10V2KX-4GP C601
SCD1U10V2KX-4GP C642
SCD1U10V2KX-4GP C638
SCD1U10V2KX-4GP C631
SCD1U10V2KX-4GP C618
Place one cap close to every 2 pullup
resistors terminated to +0.9V_DDR_VTT
+0.9V_DDR_VTT
RN64 SRN56J-4GP
RN70 SRN56J-4GP
RN63 SRN56J-4GP
RN66 SRN56J-4GP
RN61 SRN56J-4GP
RN59 SRN56J-4GP
RN72 SRN56J-4GP
RN68 SRN56J-4GP
M_B_BS#0
M_B_A10
M_B_A1
M_B_A3
M_B_A14
M_B_A6
M_B_A2
M_B_A4
M_CS2#
M_B_BS#1
M_B_RAS#
M_B_A0
M_B_A12
M_B_A9
M_B_A8
M_B_A5
M_ODT3
M_CS3#
M_B_CAS#
M_B_WE#
M_B_A13
M_ODT2
M_CKE3
M_B_A7
M_B_A11
M_CKE2
M_B_BS#2
Place these resistors close to DM2 750 mils (Max)
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Foose Intel
Size Custom
Document Number
DDRII-SODIMM SLOT2
Rev SC
Date: Friday, May 30, 2008
Sheet 17 of 58

SSID = VIDEO

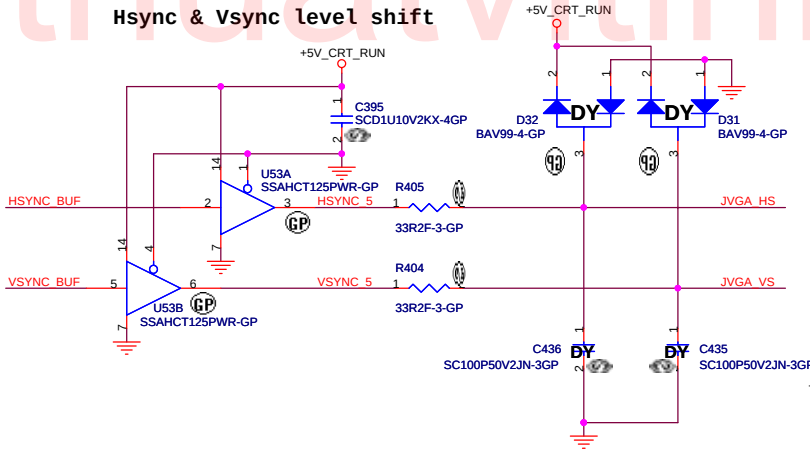


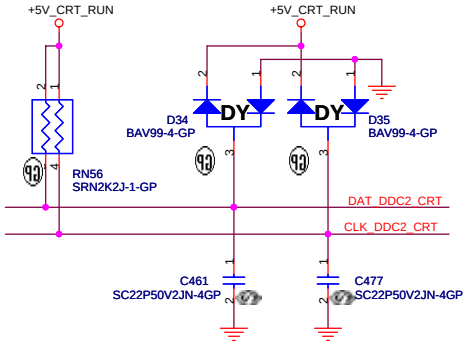
CRT_MUX_SWITCH	
SEL	CRT
0	MB
1	Dock

SC-20080317



Hsync & Vsync level shift



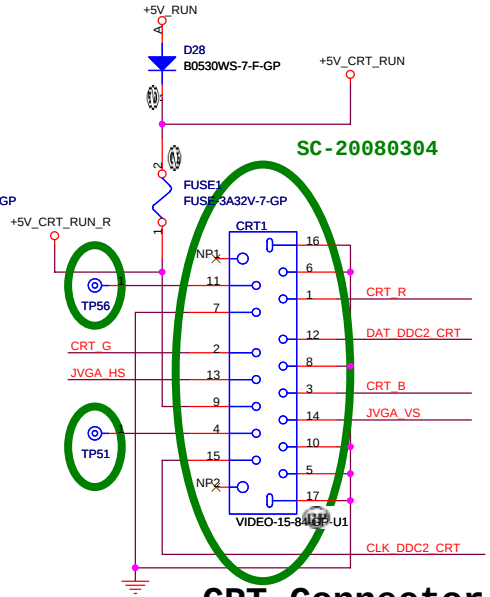


Layout Note:

***Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.**

*** RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.**

Change CRT CONN From 20.20736.015 to 20.20735.015



SC-20080304

CRT Connector

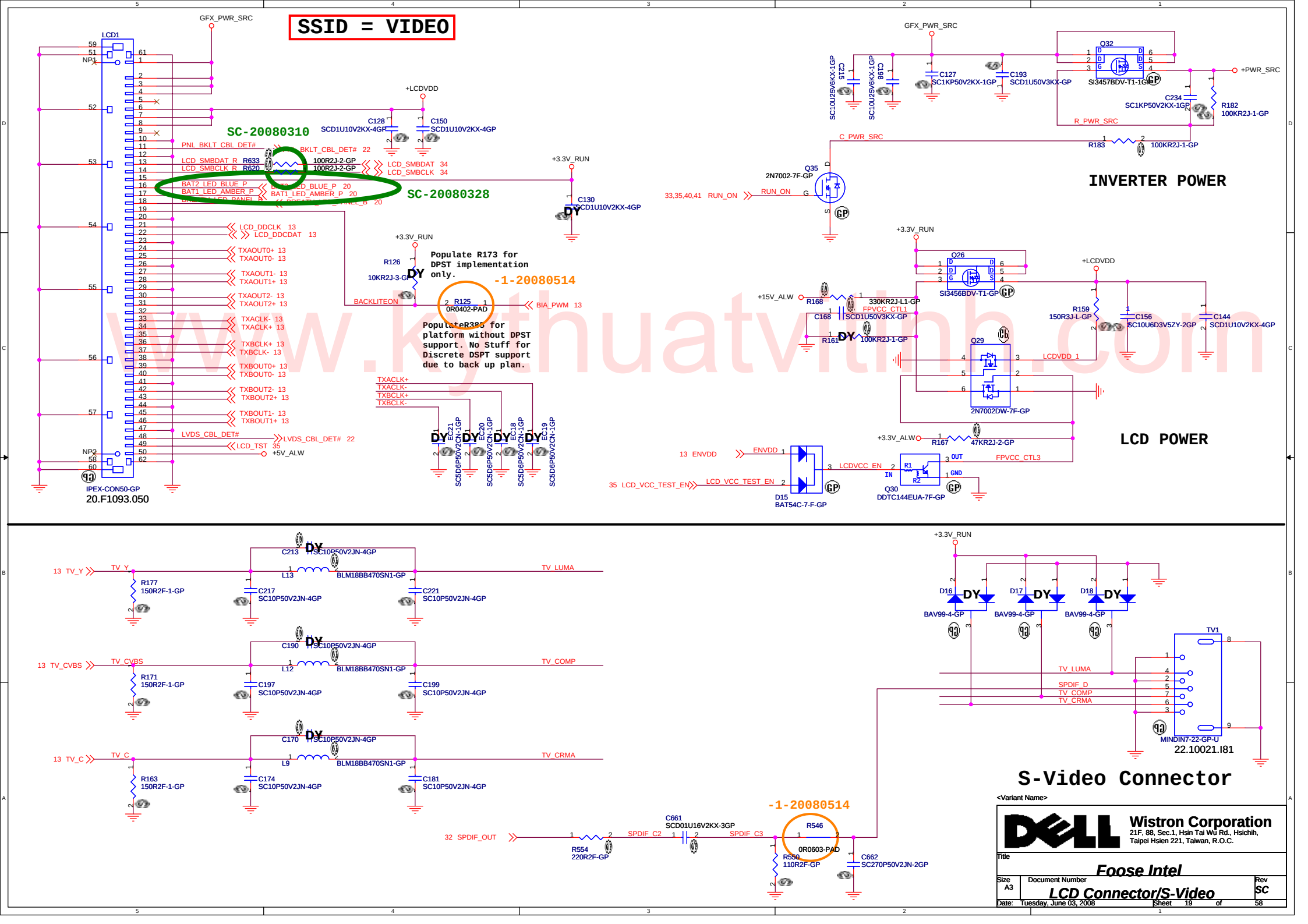
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

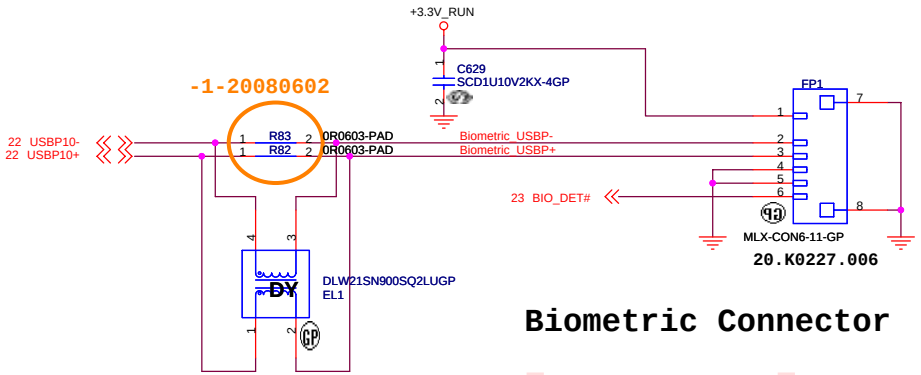
Title: Foose Intel

Size: A3 | Document Number: CRT | Rev: SC

Date: Friday, May 30, 2008 | Sheet 18 of 58


SSID = VIDEO
LCD1
IPEX-CON50-GP
20.F1093.050
SC-20080310
SC-20080328
Populate R173 for DPST implementation only.
PopulateR389 for platform without DPST support. No Stuff for Discrete DSPT support due to back up plan.
-1-20080514
INVERTER POWER
LCD POWER
S-Video Connector
TV1
MINDIN7-22-GP-U
22.10021.I81
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Foose Intel
LCD Connector/S-Video
Date: Tuesday, June 03, 2008
Sheet 19 of 58

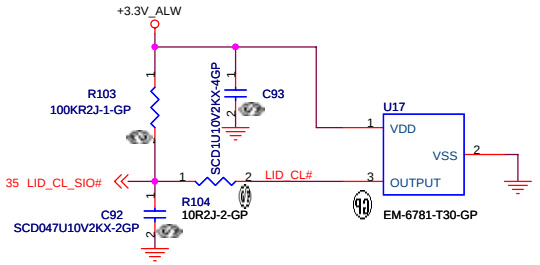
SSID = User.Interface

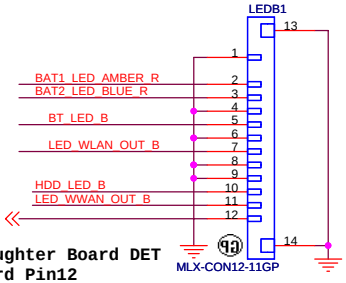


Biometric Connector

1st : AKE 74.06781.07B
2nd : Allegro 75.03212.060

Hall switch





*Pin12 for Daughter Board DET
*Daughter Board Pin12
connect to Pin1

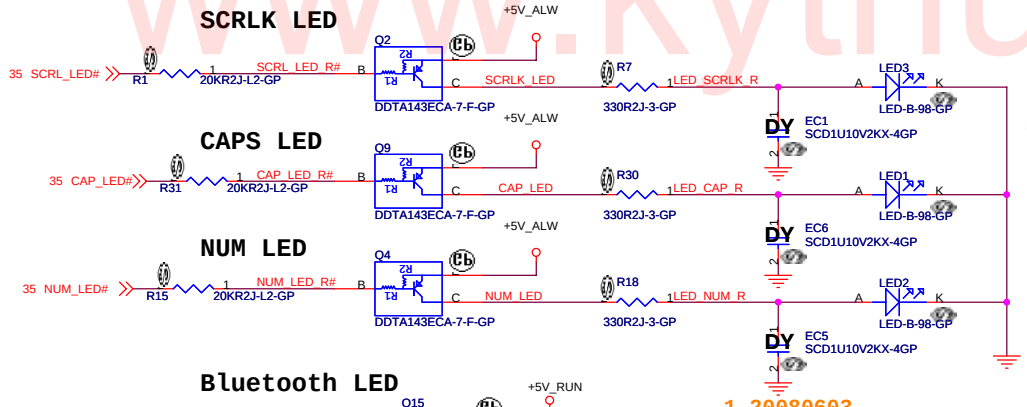
20.K0227.012

LED BD Connetor

LED Location from left to right

HDD	BATTERY	WLAN	BLUE TOOTH	WWAN

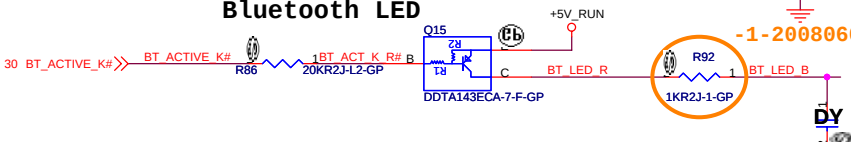
SCRLK LED



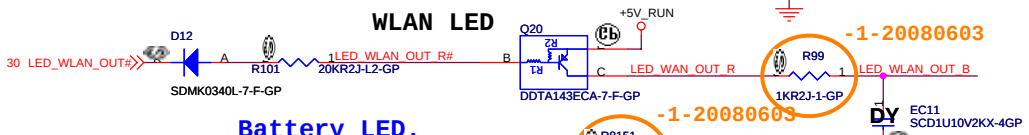
CAPS LED

NUM LED

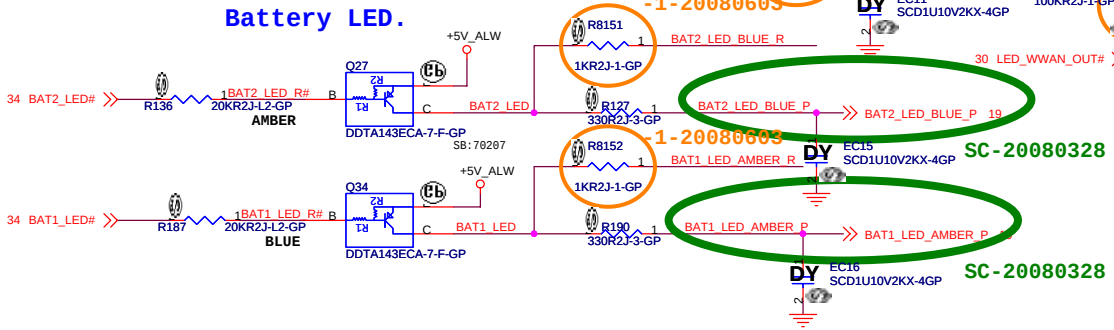
Bluetooth LED



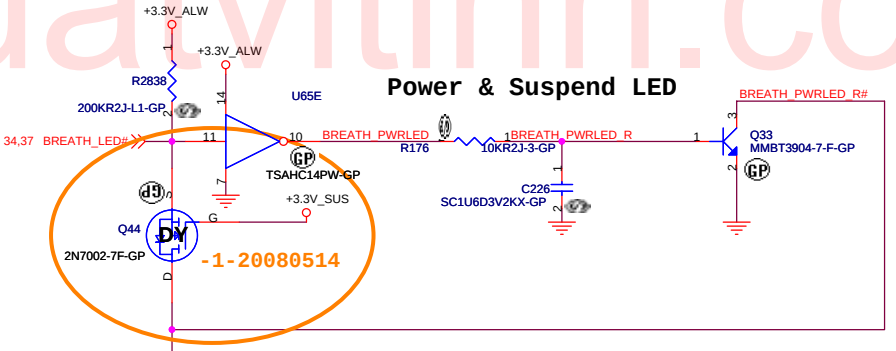
WLAN LED

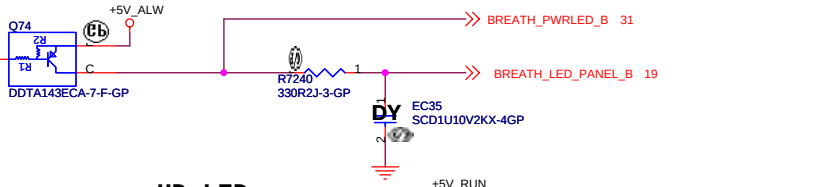


Battery LED.

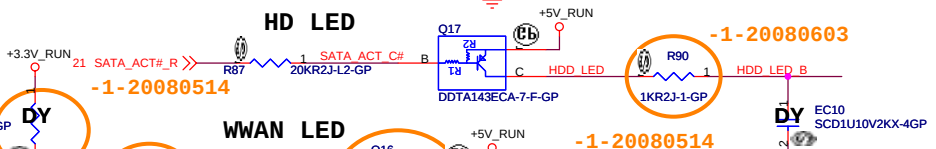


Power & Suspend LED

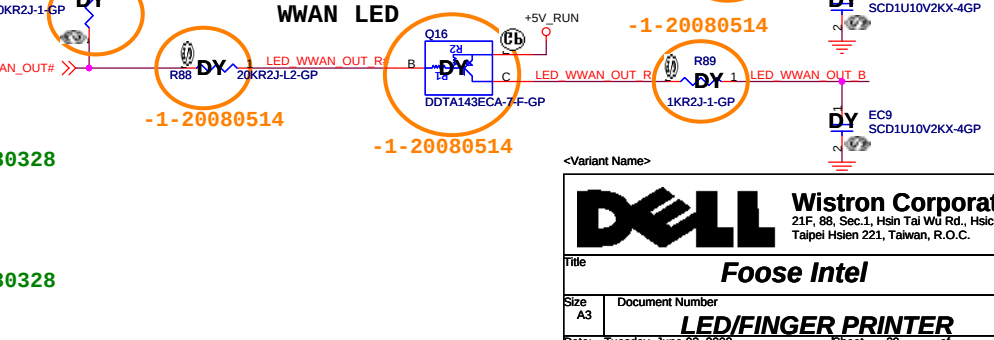




HD LED



WWAN LED



<Variant Name>

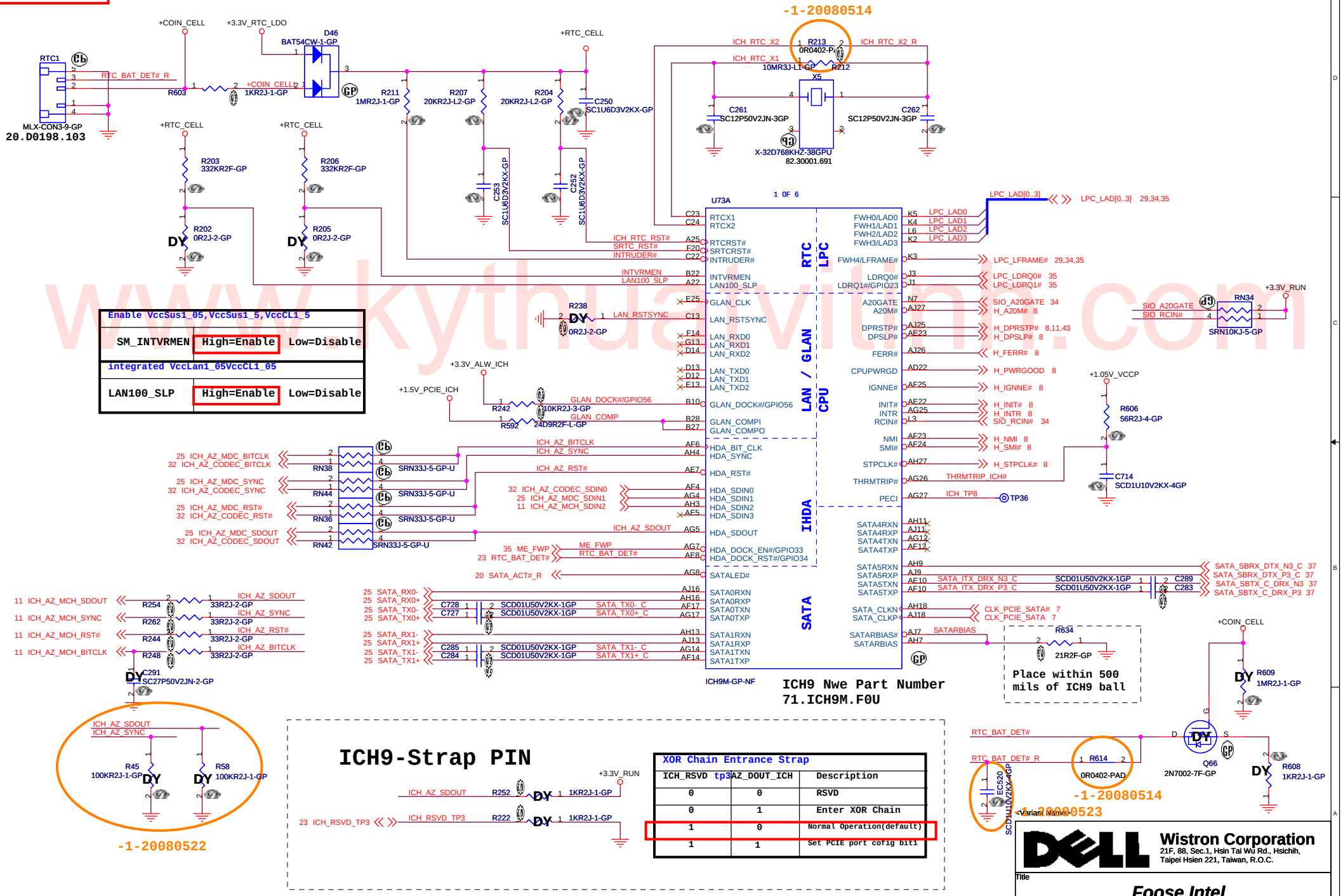
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Foose Intel

Size	Document Number	Rev
A3	LED/FINGER PRINTER	SC

Date: Tuesday, June 03, 2008 Sheet 20 of 58

SSID = ICH



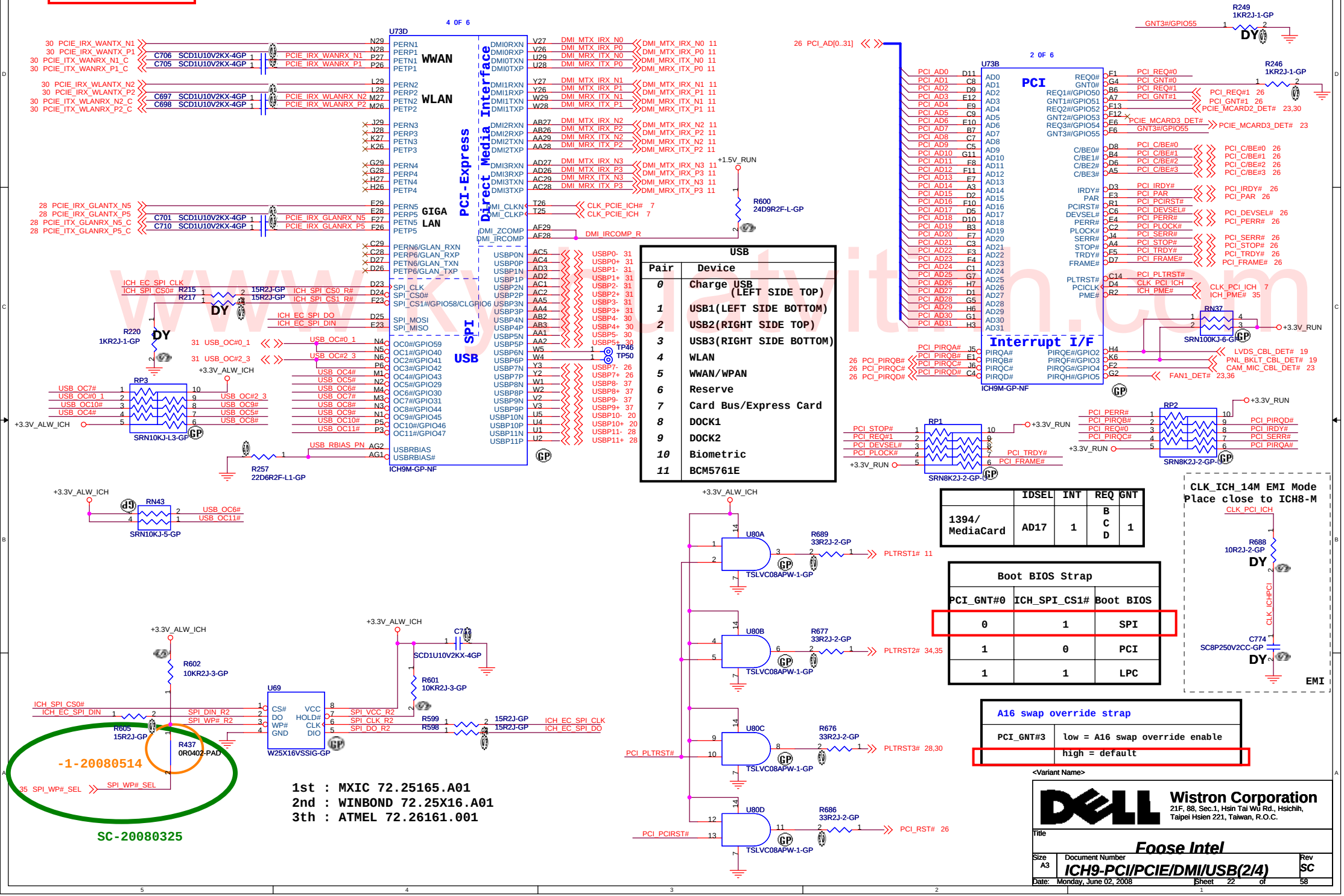
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Foose Intel

Size	Document Number	Rev
A3	ICH9-LAN/HDA/SATA/LPC(1/4)	SC

Date: Monday, June 02, 2008 Sheet 21 of 58

SSID = ICH



SSID = ICH

CLK_ICH_48M and CLK_ICH_14M EMI Mode
Place close to ICH8-M

CLK_ICH_48M → R255 10R2J-2-GP DY → CLK_ICH48M → C303 SC4D7P50V2CN-1GP DY
CLK_ICH_14M → R667 10R2J-2-GP DY → CLK_ICH14M → C762 SC4D7P50V2CN-1GP DY
EMI

3 OF 6

U73C

TPM_ID	ID0=0	ID0=1
ID1=0	C_TPM	RSVD
ID1=1	NONE	B_TPM

No Reboot Strap

SPKR	LOW = Defaule
	High=No Reboot

Option to " Disable " clkrun. Pulling it down will keep the clks running.

-1-20080529
-1-20080514
-1-20080603
-1-20080603
-1-20080514

ICH9M-GP-NF

<Variant Name>

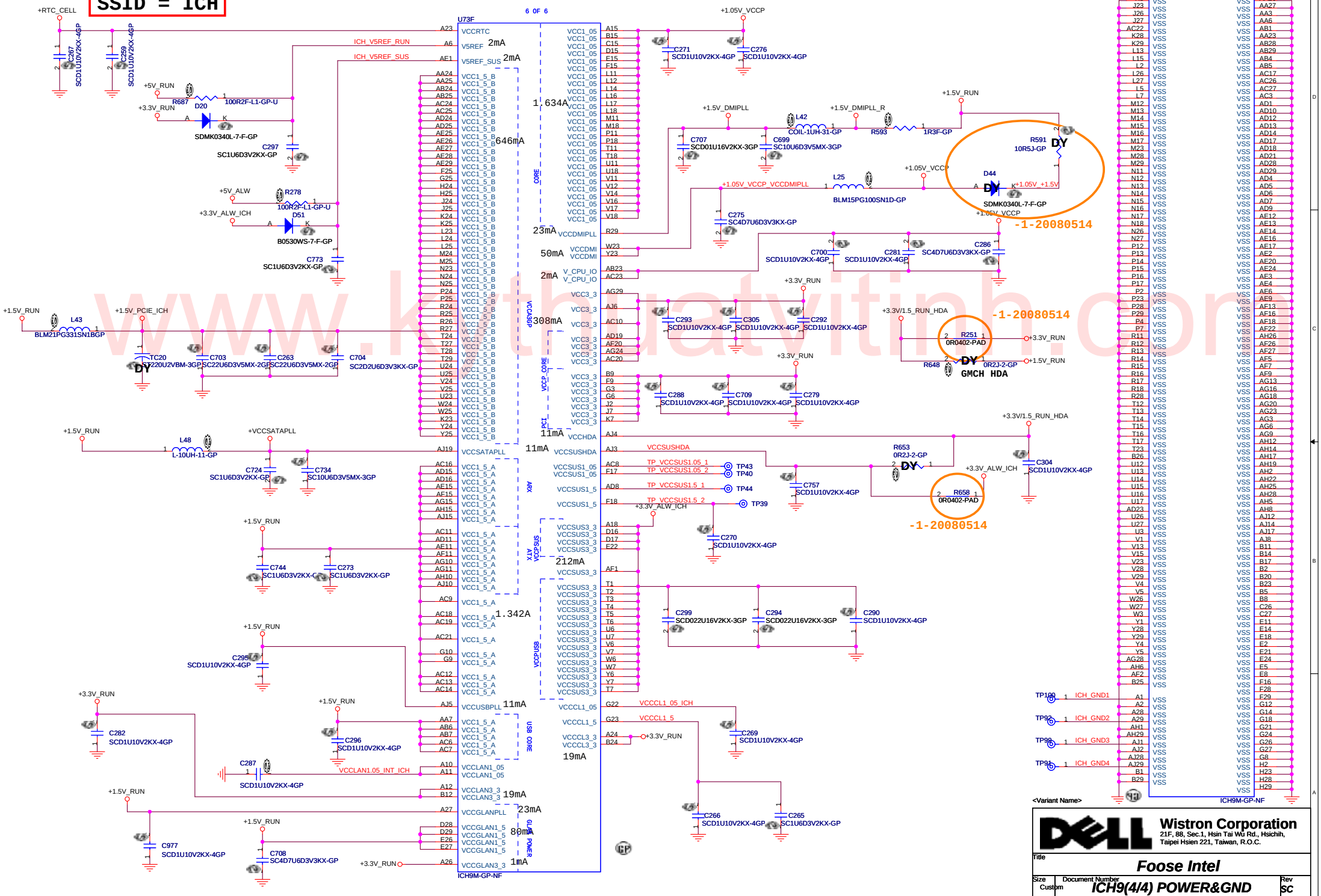
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Foose Intel

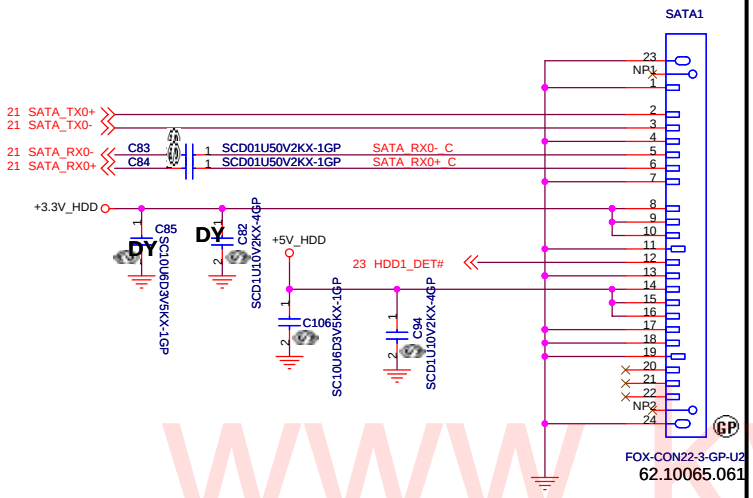
Size	Document Number	Rev
A3	ICH9-CL/PM/GPIO(3/4)	SC

Date: Thursday, June 05, 2008 Sheet 23 of 58

SSID = ICH

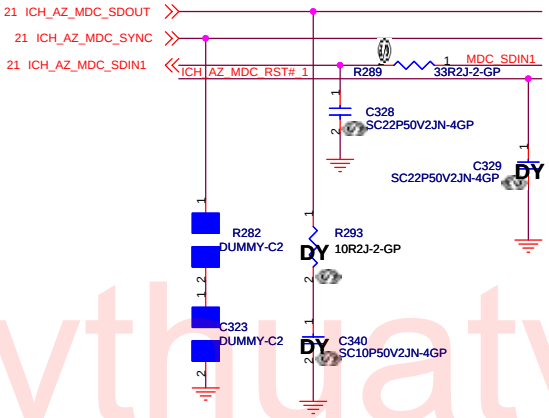


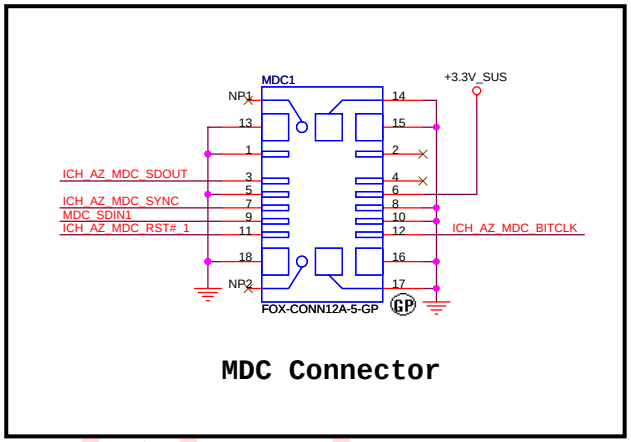
SSID = SATA



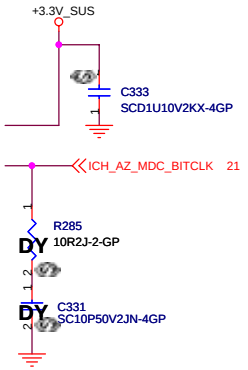
SATA HDD Connector

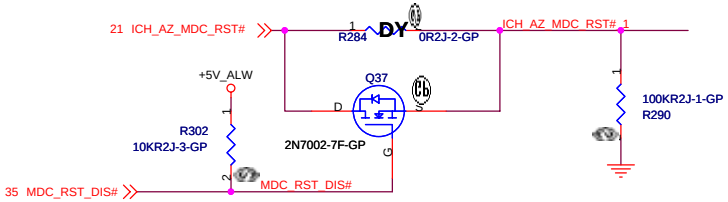
SSID = Modem





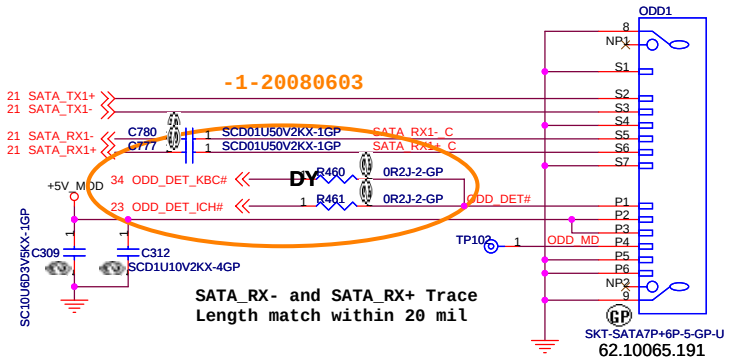
MDC Connector





NOTE : MDC DISABLE
If platform requires MDC disable,populate this circuit.
If MDC disable isn't required, connect SB_AZ_MDC_RST# directly to JMDC connector.

SSID = SATA

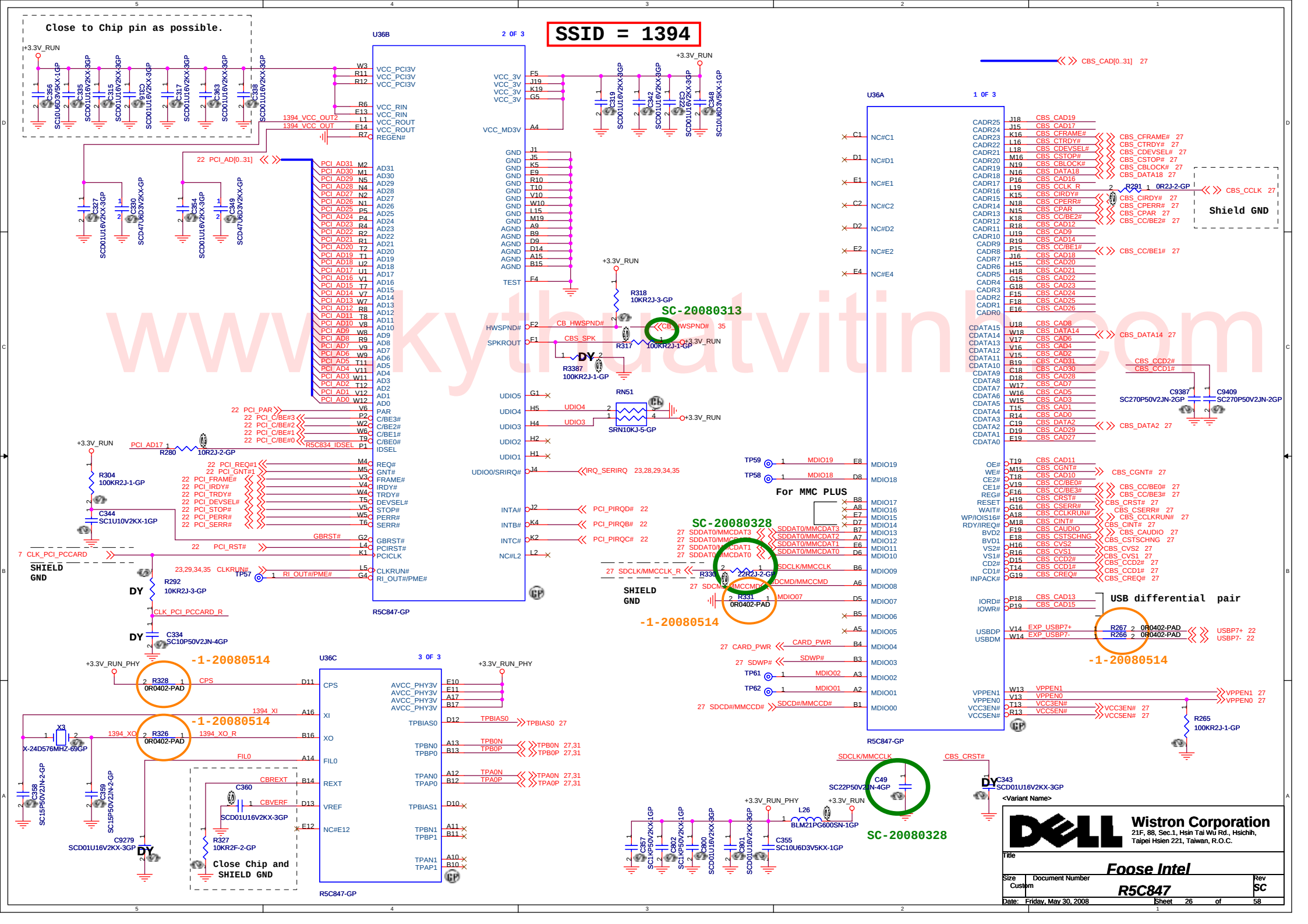


SATA ODD Connector

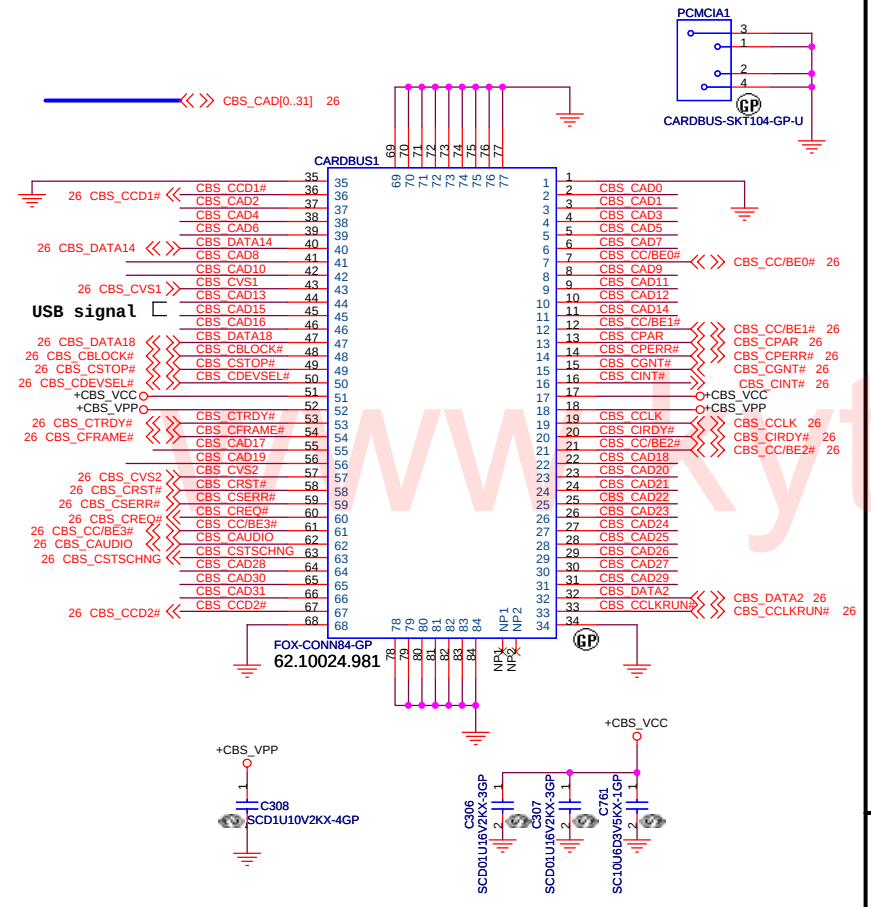
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

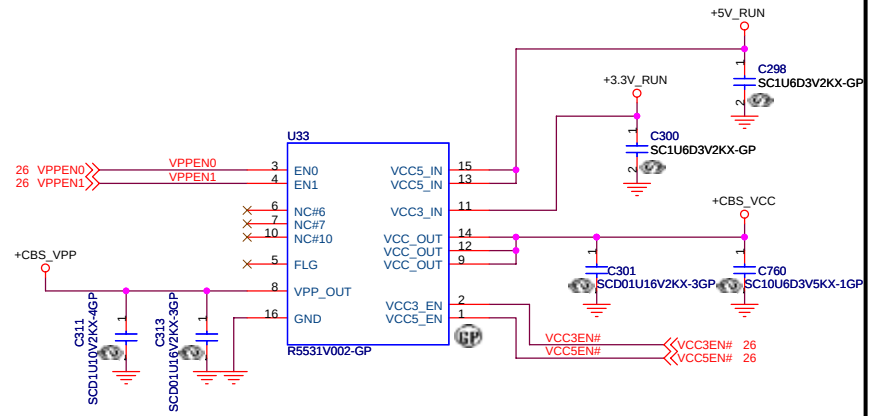
Title	Foose Intel	
Size A3	Document Number HDD/ODD/MDC	Rev SC
Date: Tuesday, June 03, 2008	Sheet 25 of 58	


SSID = 1394
Close to Chip pin as possible.
U36B
2 OF 3
R5C847-GP
U36A
1 OF 3
U36C
3 OF 3
SC-20080313
SC-20080328
-1-20080514
For MMC PLUS
USB differential pair
Shield GND
SHIELD GND
Close Chip and SHIELD GND
Foose Intel
R5C847
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Friday, May 30, 2008

SSID = CARDBUS



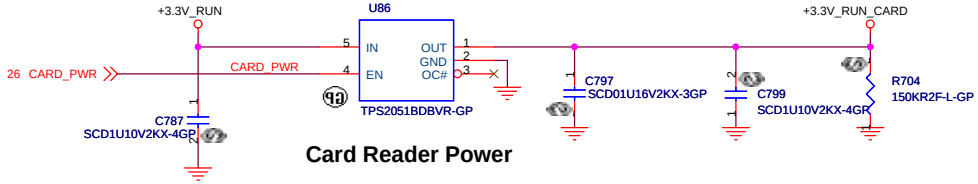
CBS_CAD13, CBS_CAD15 Can be used as Express Card USB differential pair.



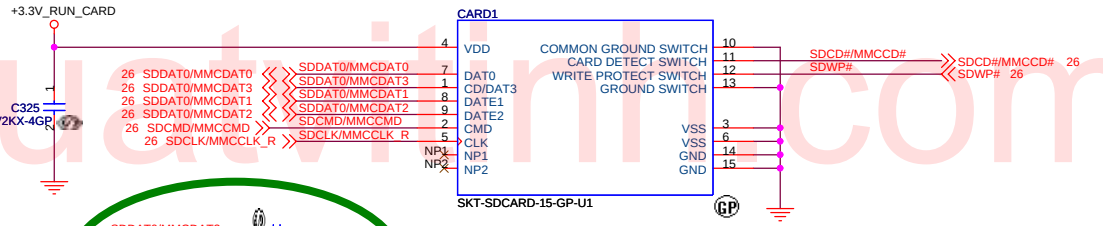
SSID = 1394

Main TI 74.02051.07F
Second ST 74.S2151.07F

40mil

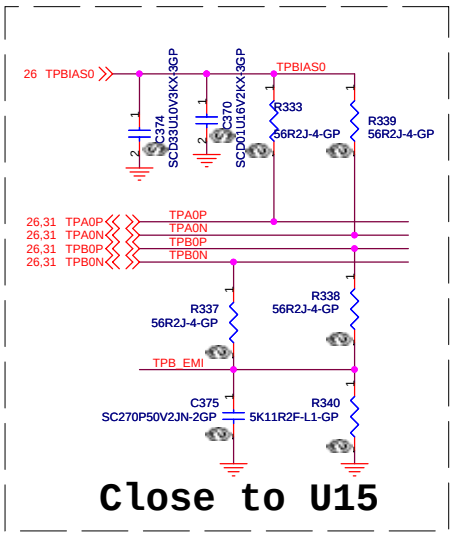


Card Reader Power



SC-20080328

SSID = 1394



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

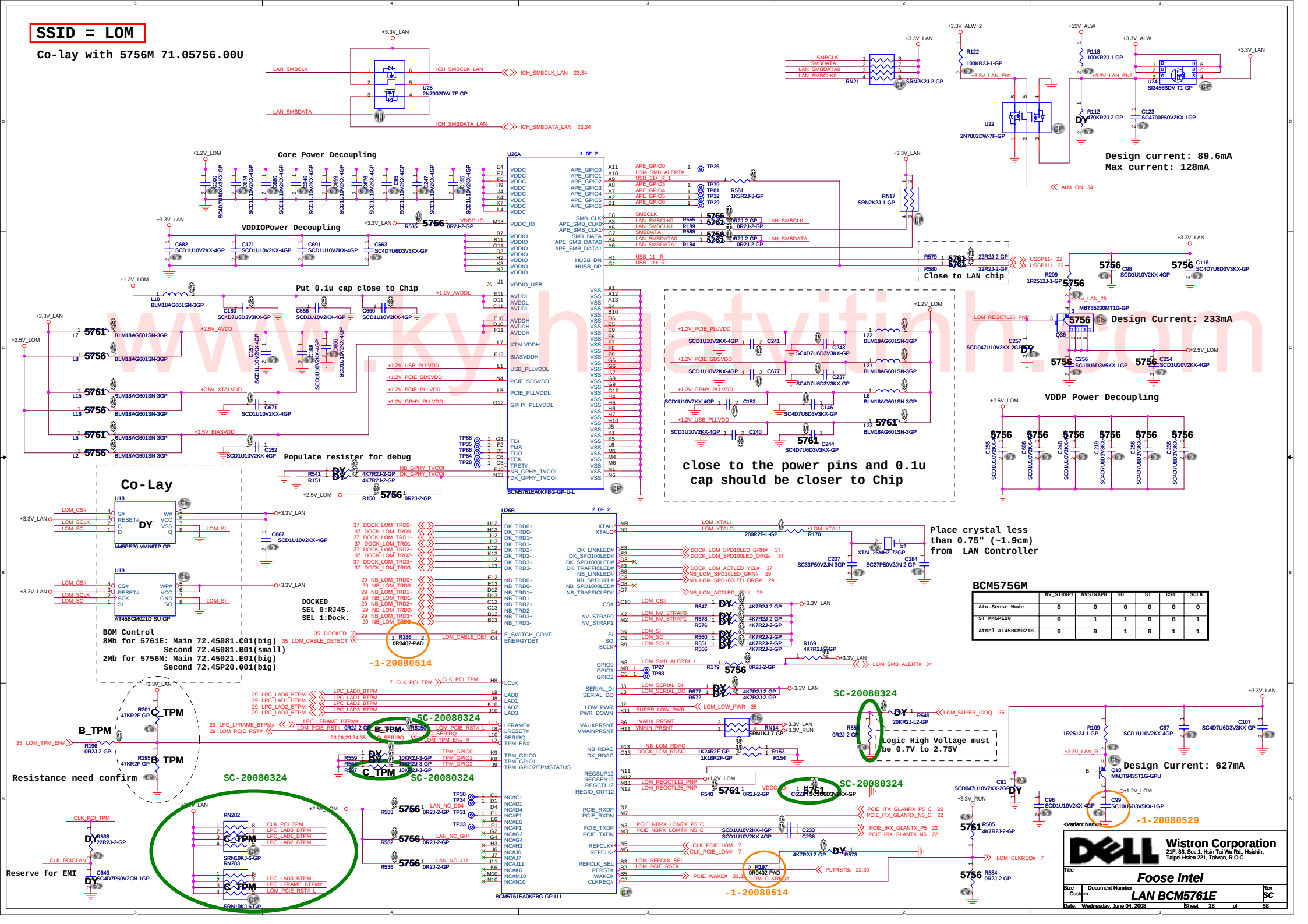
Title: Foose Intel

Size	Document Number	Rev
A3	1394 CONN/CardBus/3in1	SC

Date: Friday, May 30, 2008 Sheet 27 of 58

SSID = LOM

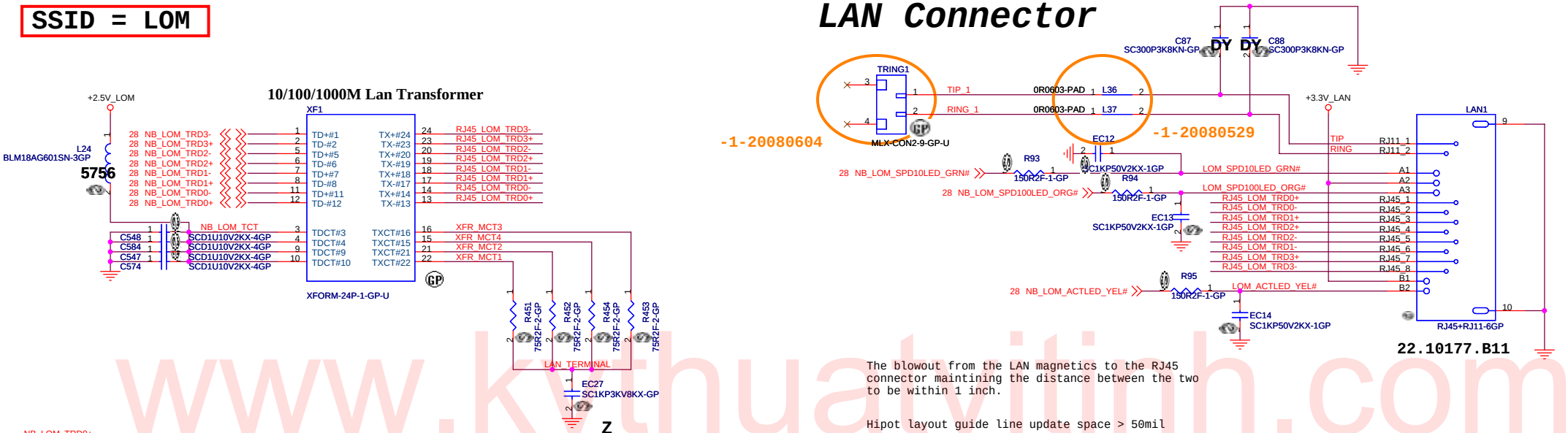
Co-lay with 5756M 71.05756.00U



	NV_STRAP1	NVSTRAP0	SO	SI	CS#	SCLK
Ato-Sense Mode	0	0	0	0	0	0
ST M45PE20	0	1	1	0	0	1
Atmel AT45BCM021B	0	0	1	0	1	1

SSID = LOM

LAN Connector



The blowout from the LAN magnetics to the RJ45 connector maintining the distance between the two to be within 1 inch.

Hipot layout guide line update space > 50mil

Rj11 layout guide line update > 100mil

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

Z

Base Address	BA1 PIN3	BA0 PIN9
EE/EF	0	0
7E/7F	0	1
2E/2F	1	0
4E/4F	1	1

Default EE/EF as Amy recommended

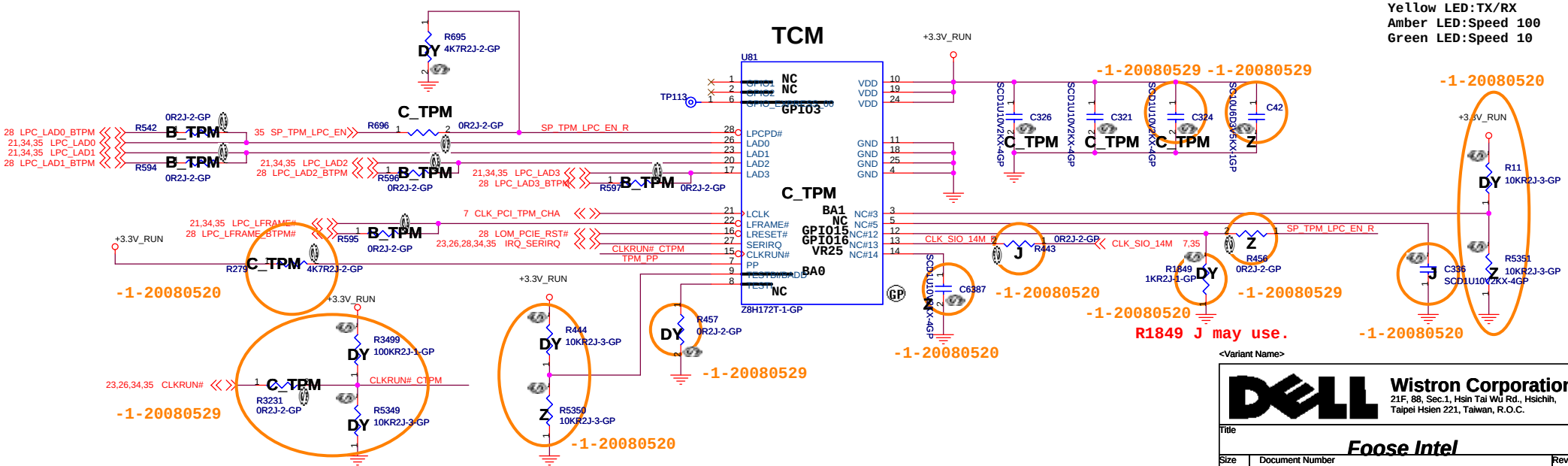
J

	1(default)	0
PIN12	FLASH	SRAM

J has internal PU with PIN12.

Yellow LED:TX/RX
Amber LED:Speed 100
Green LED:Speed 10

TCM



<Variant Name>

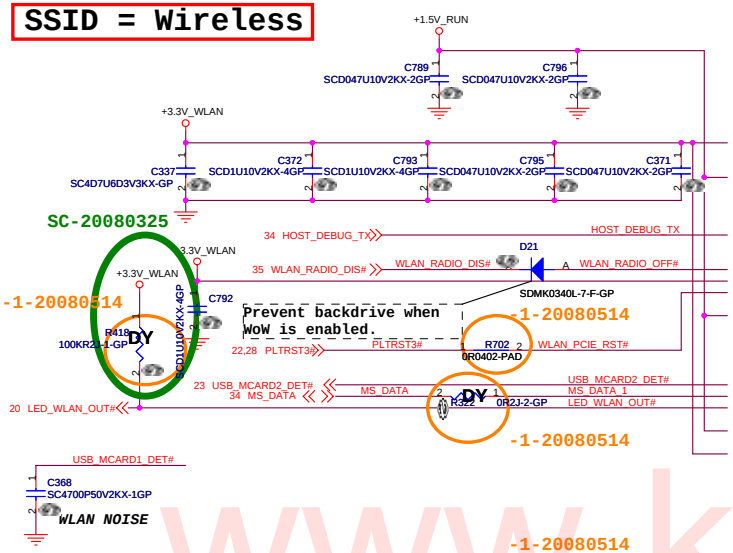
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Foose Intel**

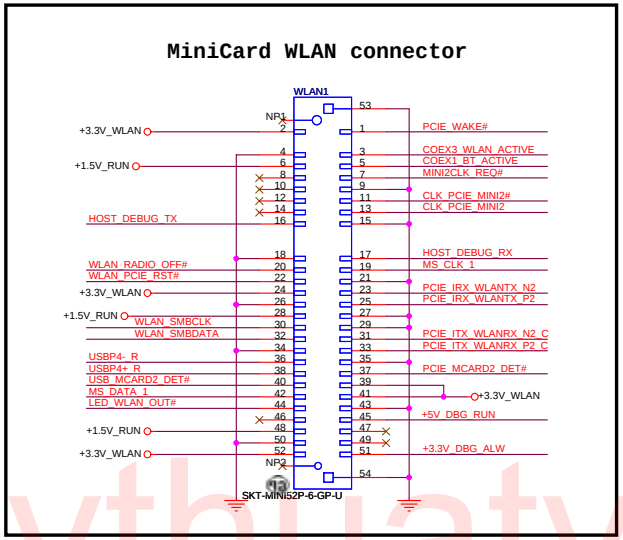
Size	Document Number	Rev
A3	LAN CONNECTOR/China TPM	SC

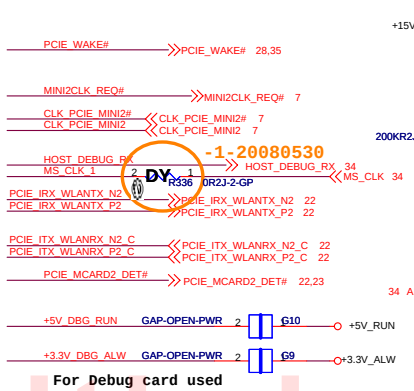
Date: Thursday, June 05, 2008 Sheet 29 of 58

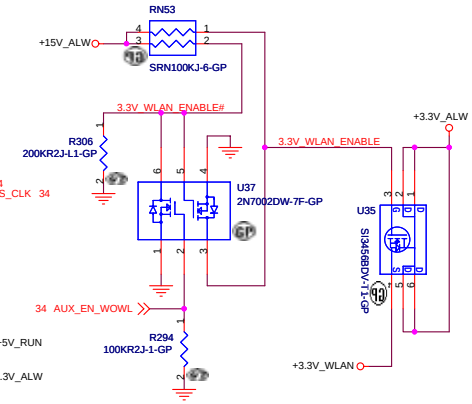
SSID = Wireless



MiniCard WLAN connector

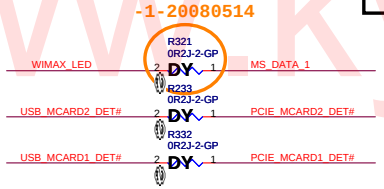


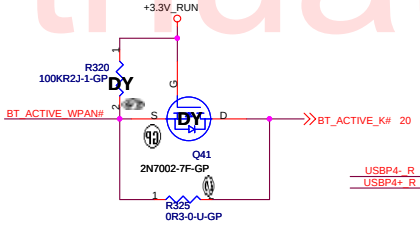


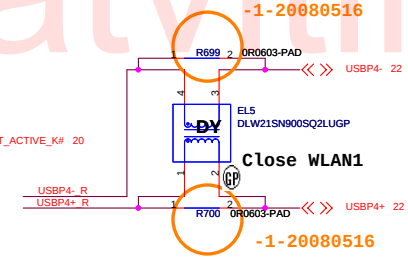


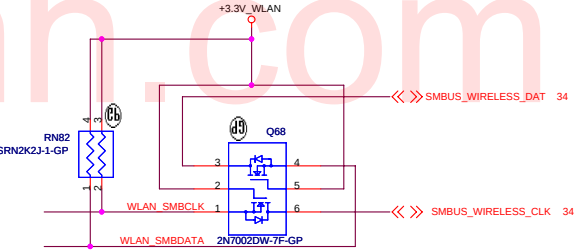
JMINI Pin	Debug Pin Name	EC Pin
16	HOST_DEBUG_TX	70
17	HOST_DEBUG_RX	71
19	8051_TX	82
42	8051_RX	81

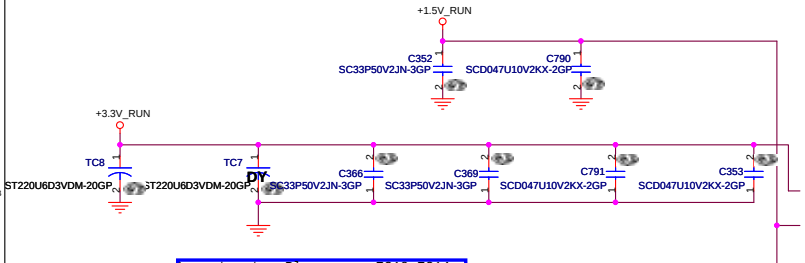
DEBUG PINS



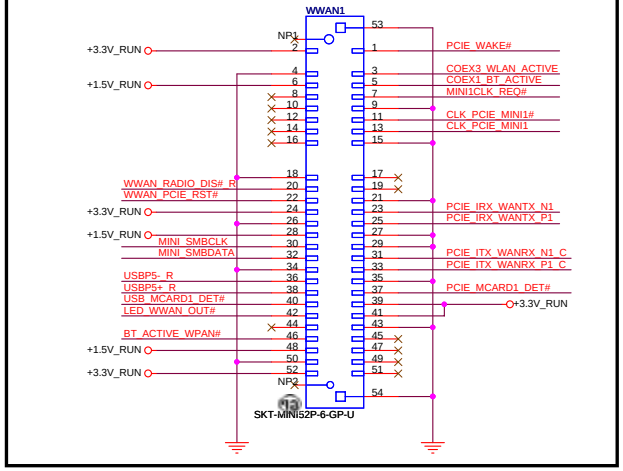


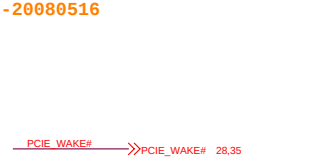


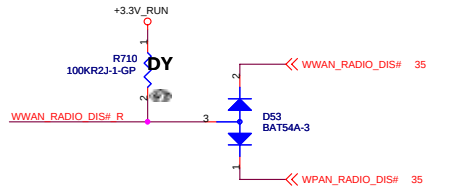


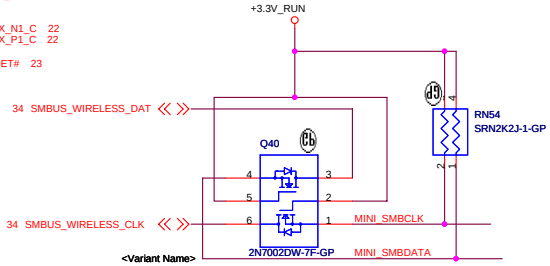


MiniCard WWAN connector









<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

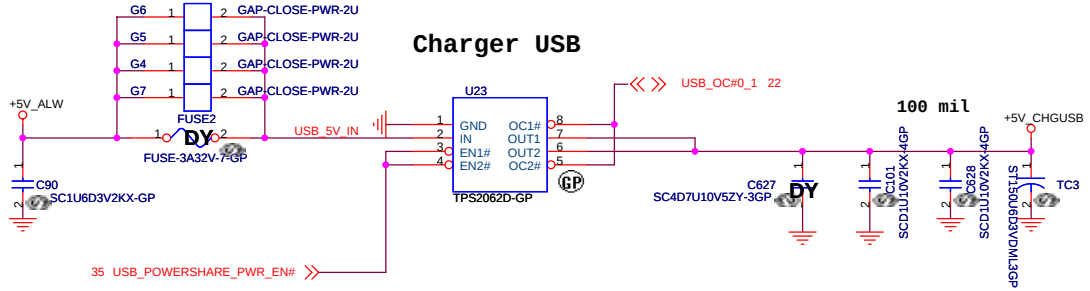
Title: Foose Intel

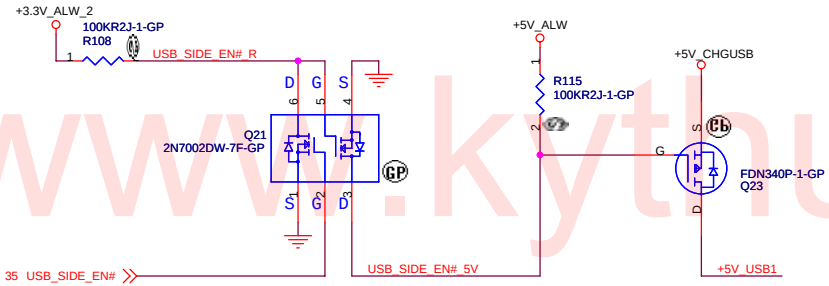
Size: Custom | Document Number: Minicard WLAN/WWAN CONN | Rev: SC

Date: Friday, May 30, 2008 | Sheet 30 of 58

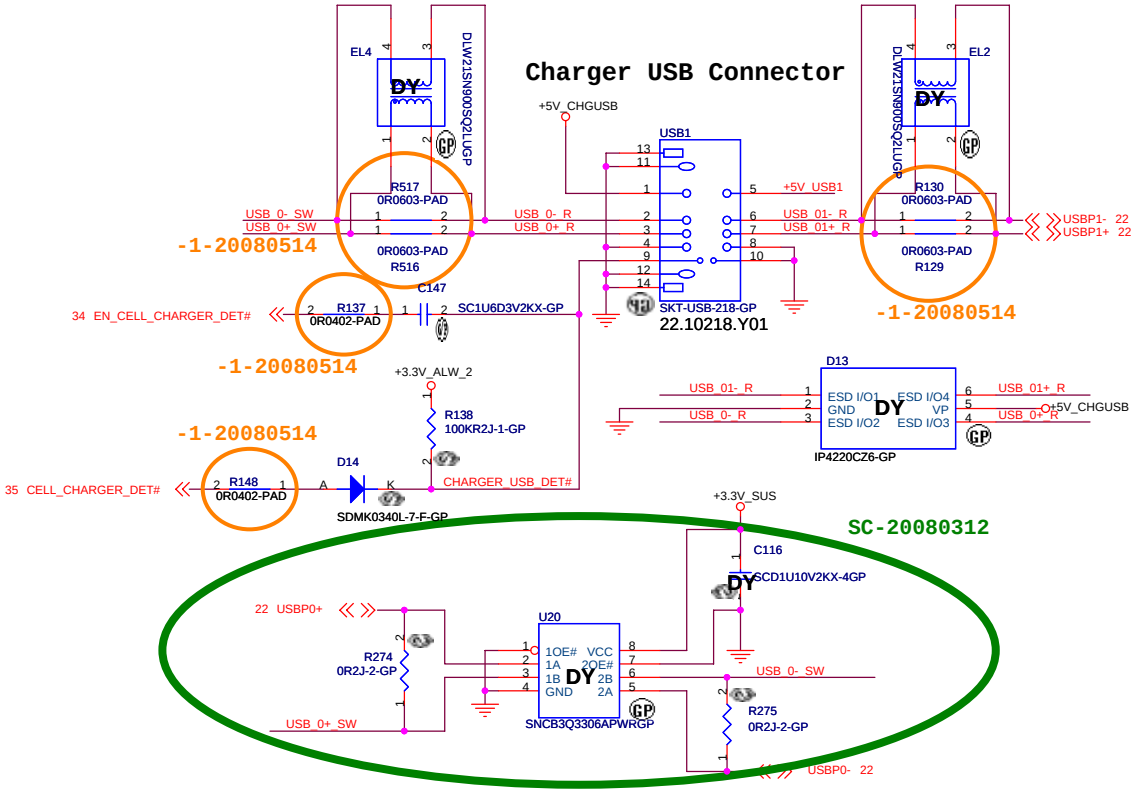
SSID = USB

Charger USB

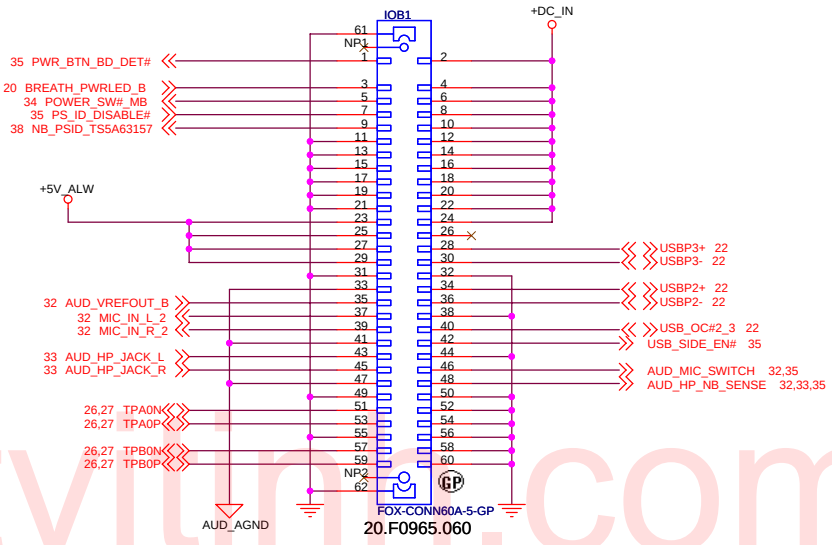




Charger USB Connector

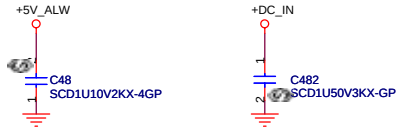


SSID = User.Interface

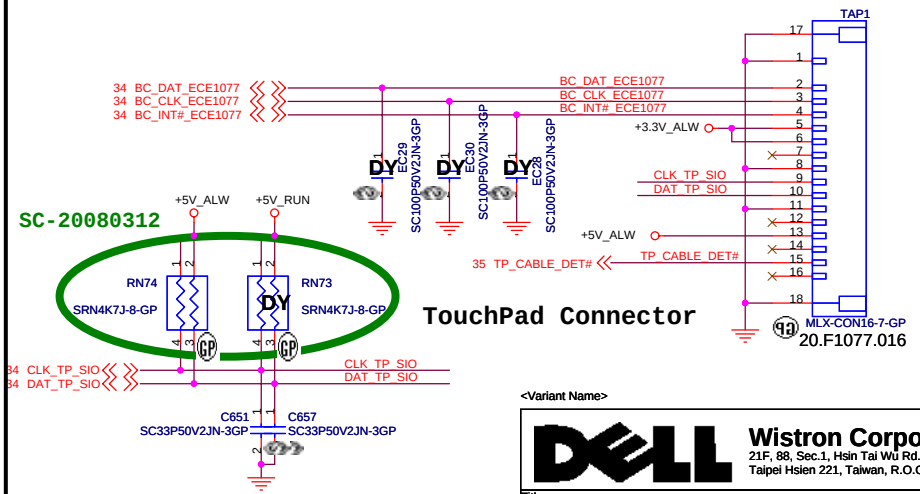


IO Board Connector

*Pin60 for Daughter Board DET
*Daughter Board Pin1 connect to Pin60



SSID = Touch.Pad



TouchPad Connector

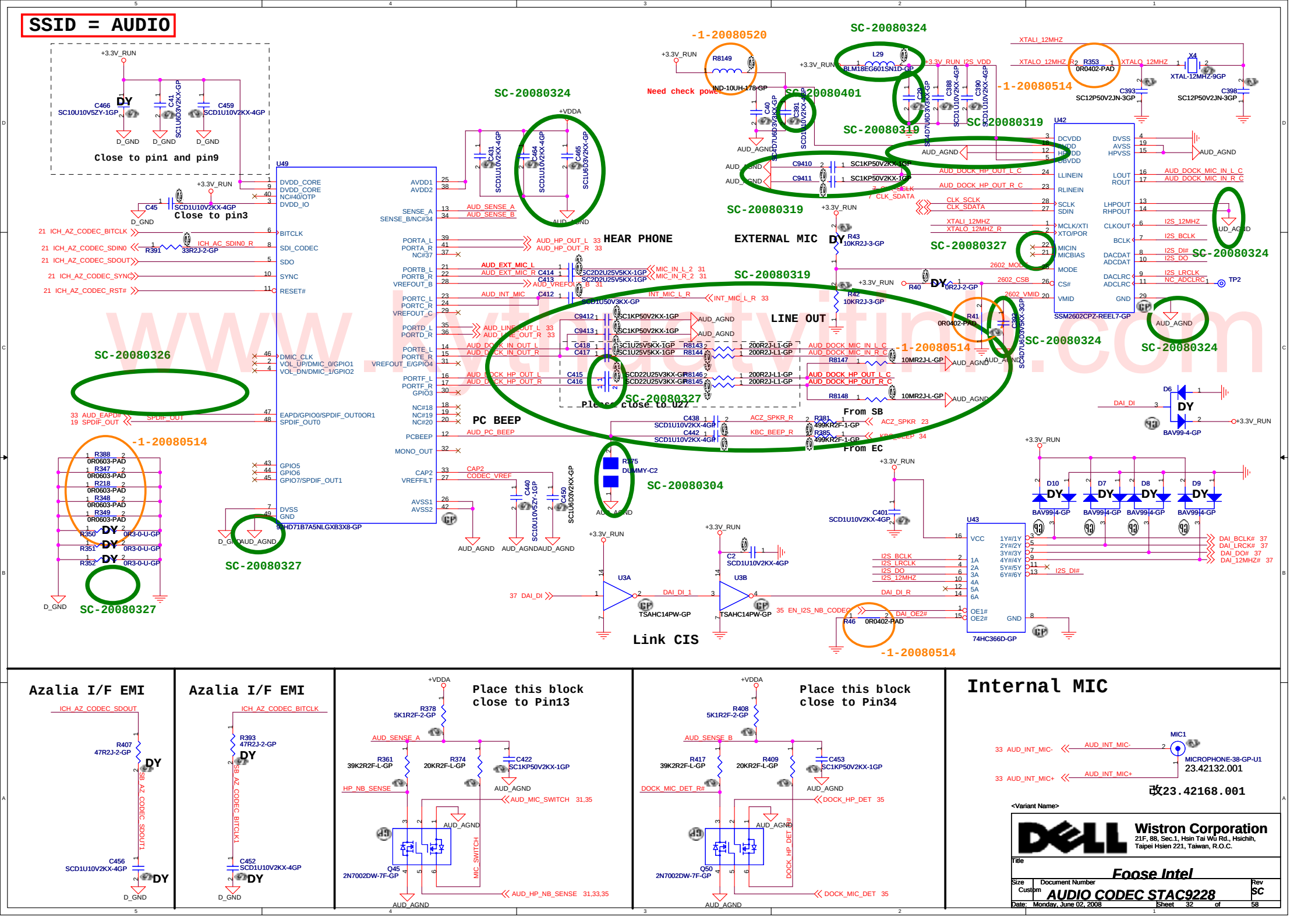
<Variant Name>

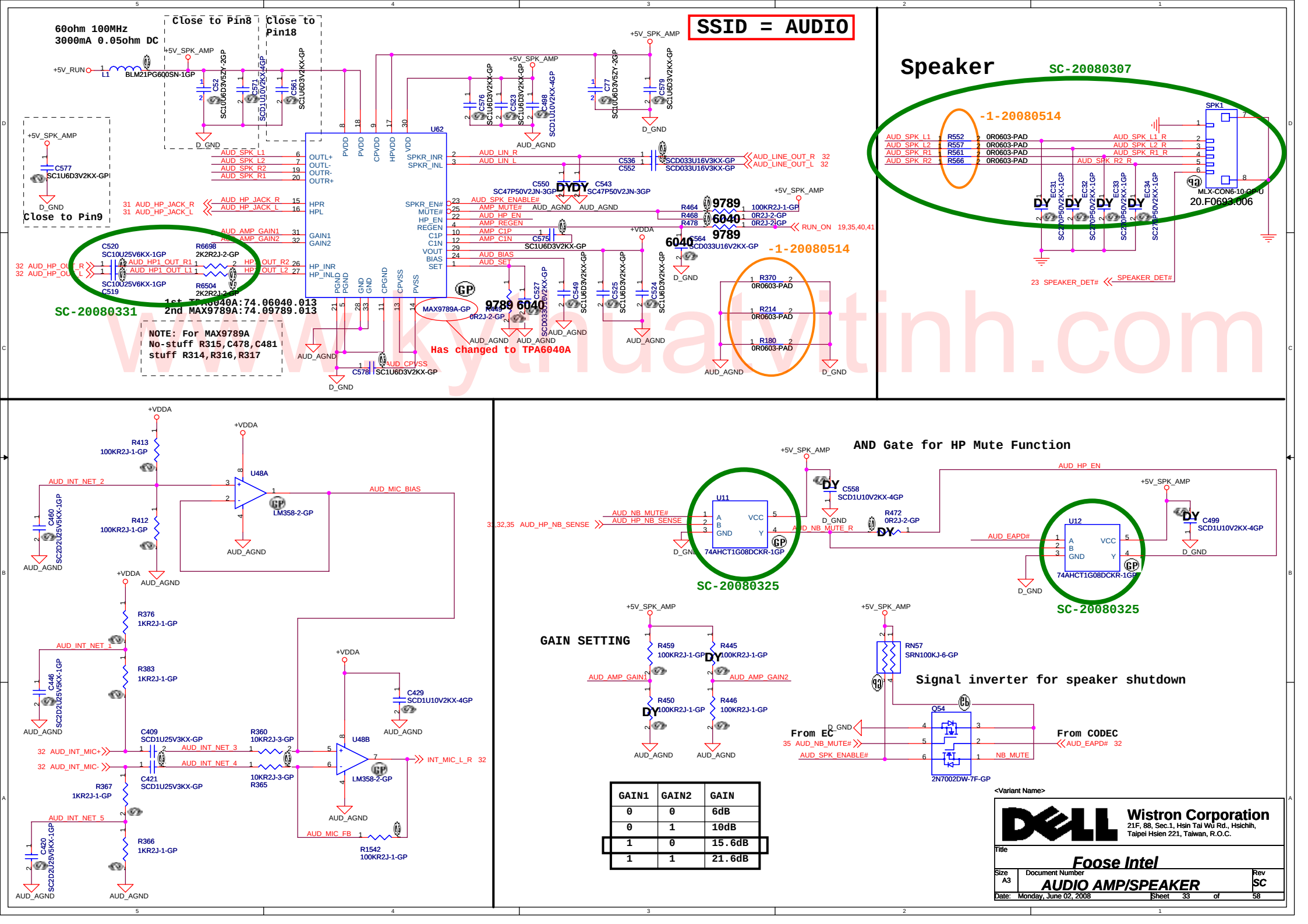
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Foose Intel

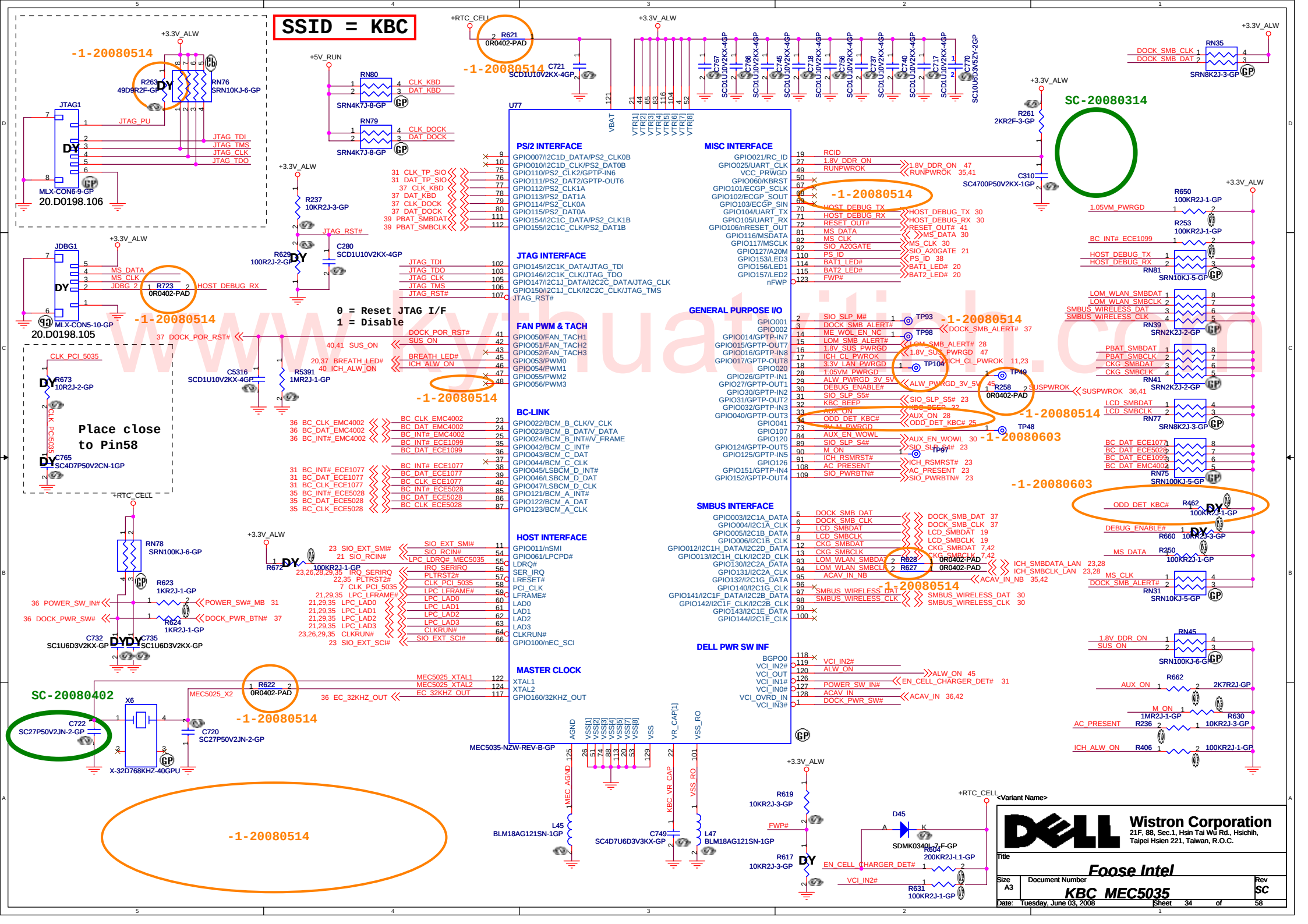
Size	Document Number	Rev
A3	IO Board/USB Port/TP CONN	SC

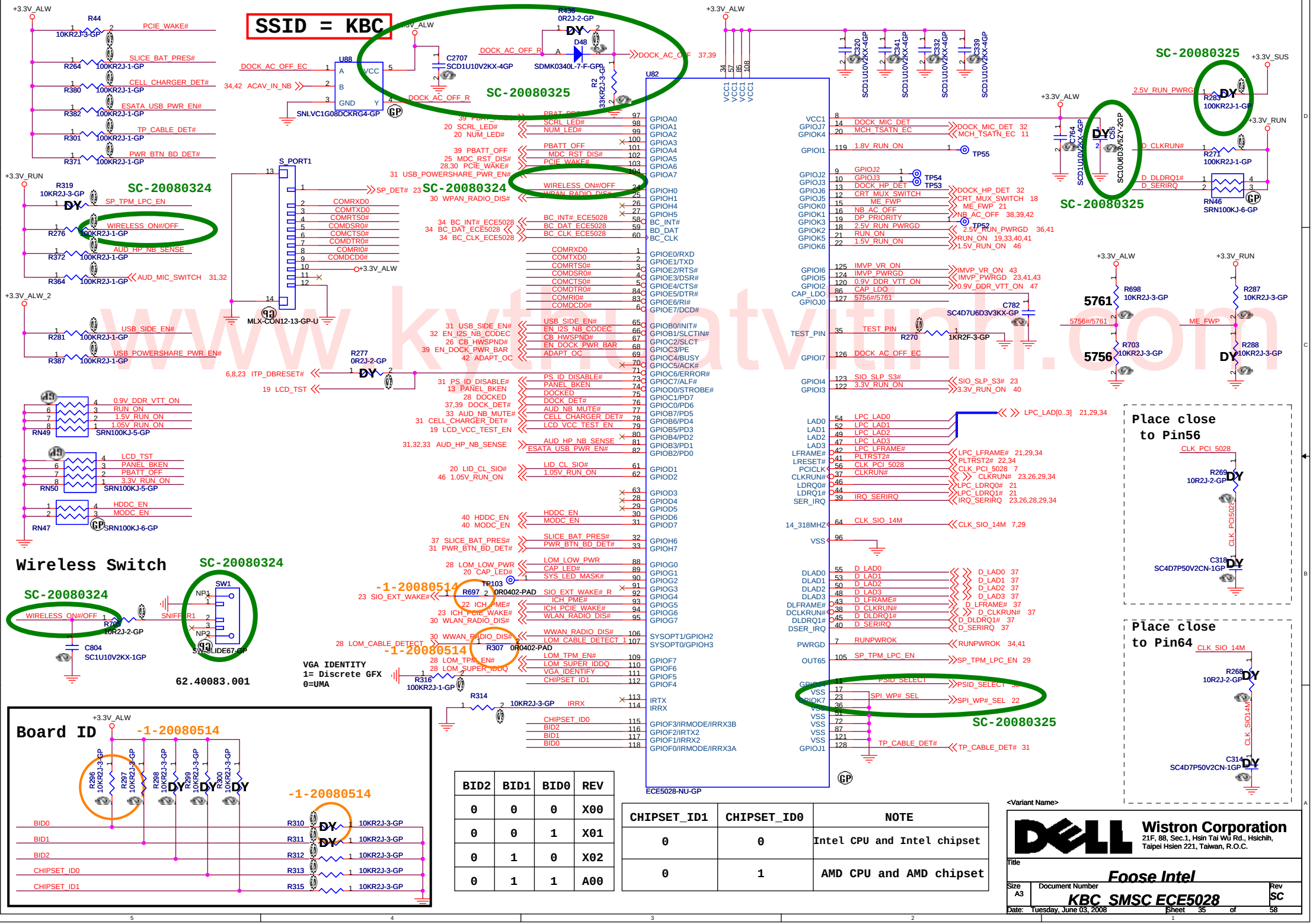
Date: Tuesday, June 03, 2008 Sheet 31 of 58


SSID = AUDIO
Close to pin1 and pin9
Close to pin3
U49
HEAR PHONE
EXTERNAL MIC
LINE OUT
PC BEEP
From SB
From EC
Link CIS
Please close to U27
U42
U43
SSM2602CPZ-REEL7-GP
74HC366D-GP
SC-20080324
SC-20080319
SC-20080327
SC-20080326
SC-20080304
SC-20080401
-1-20080520
-1-20080514
Need check power
Azalia I/F EMI
Place this block close to Pin13
Place this block close to Pin34
Internal MIC
MICROPHONE-38-GP-U1
23.42132.001
23.42168.001
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Foose Intel
AUDIO CODEC STAC9228
Monday, June 02, 2008


SSID = AUDIO
60ohm 100MHz
3000mA 0.05ohm DC
Close to Pin8
Close to Pin18
Close to Pin9
+5V_RUN
L1
BLM21PG600SN-1GP
+5V_SPK_AMP
D_GND
AUD_AGND
U62
MAX9789A-GP
SC-20080331
1st TPA6040A:74.06040.013
2nd MAX9789A:74.09789.013
NOTE: For MAX9789A
No-stuff R315,C478,C481
stuff R314,R316,R317
Has changed to TPA6040A
Speaker
SC-20080307
-1-20080514
MLX-CON6-10-GD-U
20.F0693.006
SPEAKER_DET#
AND Gate for HP Mute Function
74AHCT1G08DCKR-1GP
SC-20080325
GAIN SETTING
Signal inverter for speaker shutdown
2N7002DW-7F-GP
From EC
From CODEC
LM358-2-GP
GAIN1
GAIN2
GAIN
0
6dB
10dB
15.6dB
21.6dB
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Foose Intel
AUDIO AMP/SPEAKER
Monday, June 02, 2008
Sheet 33 of 58

SSID = KBC


-1-20080514
SC-20080314
SC-20080402
-1-20080603
U77
MEC5035-NZW-REV-B-GP
PS/2 INTERFACE
JTAG INTERFACE
FAN PWM & TACH
BC-LINK
HOST INTERFACE
MASTER CLOCK
MISC INTERFACE
GENERAL PURPOSE I/O
SMBUS INTERFACE
DELL PWR SW INF
0 = Reset JTAG I/F
1 = Disable
Place close to Pin58
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Foose Intel
KBC MEC5035
Tuesday, June 03, 2008



BID2	BID1	BID0	REV
0	0	0	X00
0	0	1	X01
0	1	0	X02
0	1	1	A00

CHIPSET_ID1	CHIPSET_ID0	NOTE
0	0	Intel CPU and Intel chipset
0	1	AMD CPU and AMD chipset

SSID = Thermal

34 BC_DAT_EMC4002
34 BC_CLK_EMC4002

BC Bus clock and data signal trace length should be matched with +/- 1 inch.

REM_DIODE3_N, REM_DIODE3_P routing together.
Trace width / Spacing = 10 / 10 mil
Place near the bottom SODIMM

Diode circuit at DP4/DN4 is used for skin temp sensor (placed optimally between CPU,MCH and MEM).

Q11 and C514 Place under CPU

C480 SC100P50V2JN-3GP DY
MMBT3904-7-F-GP Q55
Place C514 close to the Q11 as possible

C408 SC2200P50V2KX-2GP close to the Guardian pins

Place C516 close to the Guardian pins

C33 SC2200P50V2KX-2GP
MMBT3904-7-F-GP Q57
C592 SC100P50V2JN-3GP DY

PWR_MON ISL88731_ICM_4002
R2202 4K7R2J-2-GP
PWR_MON_43 ISL88731_ICM_42

8 H_THERMDA
C403 SC470P50V2KX-3GP close to the Guardian pins
8 H_THERMDC

Q13 and C520 Place nead DIMM

C640 SC100P50V2JN-3GP DY
MMBT3904-7-F-GP Q63
C402 SC2200P50V2KX-2GP close to the Guardian pins

+3.3V_SUS
R362 0R0603-PAD -1-20080514
+3.3V_ALW
R357 100KR2J-1-GP DY
C424 SCD1U10V2KX-4GP

+RTC_CELL
C454 SC1U6D3V2KX-GP

U47

SMDATA/BC-LINK_DATA
SMBCLK/BC-LINK-CLK
DP1/VREF_T
DN1/THERM
DP2
DN2
DP3/DN7
DN3/DP7
VDD
RTC_PWR3V
VDD_PWRGD
3V_PWROK#
THERMTRIP1#
THERMTRIP2#
THERMTRIP3#
VSET
ADDR_MODE/XEN
VDDH1
VDDH1
VDDL1
FAN_OUT1
FAN_OUT1
TACH1/GPIO3
CLK_IN/GPIO2
GND
VIN1
VCP1
VCP2
DP4/DN8
DN4/DP8
DP5/DN9
DN5/DP9
DP6/VREF_T2
DN6/VIN2
ATF_INT#/BC-LINK_IRQ#
POWER_SW#
ACAVAIL_CLR
THERMTRIP_SIO/PWM1/GPIO5
SYS_SHDN#
LDO_SHDN#
LDO_POK
LDO_SET
VDDH2
VDDH2
VDDL2
LDO_OUT/FAN_OUT2
LDO_OUT/FAN_OUT2
TACH2/GPIO4
PWM2/GPIO1

EMC4002-HZH-REV-C-GP-U1

REM_DIODE1_P
REM_DIODE1_N
H_THERMDA
H_THERMDC
REM_DIODE3_P
REM_DIODE3_N
3VSUS_THRM
REM_DIODE4_P
REM_DIODE4_N
THERMAL_DP6
THERMAL_DN6
R396 10KR2J-3-GP +3.3V_ALW
POWER_SW_IN# 4002
BC_INT#_EMC4002 34
ACAV_IN 34,42
THERMTRIP_SIO
THERM_VDD_PWRGD
THERM_3V_PWROK#
THERM_LDO_SHDN#
2.5V_RUN_PWRGD 35,41
THERMAL_VSET
3VSUS_THRM
3VSUS_THRM_1
R47 4K7R2J-2-GP
LDO_SET
FAN1_VOUT
FAN1_TACH_FB
34 EC_32KHZ_OUT
PM_EXTTS# R

THERMISTOR OPTION:
Single-ended routing to thermistor is permissible (ground return). Place R364 and C240 near EMC4002

WWAN
R358 1K2R2F-1-GP
THERMISTOR RT1 NTC-10K-17-GP
C439 SCD1U10V2KX-4GP

SC-20080328
R400 10KR2J-3-GP +3.3V_SUS
THERM_STP# 45
R392 47KR2J-2-GP +RTC_CELL
R399 10KR2J-3-GP +3.3V_SUS
R607 10KR2J-3-GP

+2.5V_RUN
R48 31K6R2F-GP DY Ra
Voltage margining circuit for LDO output. Adjustable from 1.2 to 2.5V.
Ra=((LDO_OUT/1.2)-1)*Rb.
R368 1KR2F-3-GP Rb

Rset=953,Tp=88degree

34,41 SUSPWROK
0,41 ICH_PWRGD#
RN55 SRN1KJ-7-GP
R401 8K2R2J-3-GP
+1.05V_VCCP
R421 2K2R2J-2-GP
THERM_B1
Q48 MMBT3904-7-F-GP
C406 SCD1U10V2KX-4GP
8 H_THERMTRIP#

C400 SCD1U10V2KX-4GP
R356 953R2F-GP

R402 8K2R2J-3-GP
+1.05V_VCCP
R403 2K2R2J-2-GP
THERM_B2
Q47 MMBT3904-7-F-GP
C399 SCD1U10V2KX-4GP
11 THERMTRIP_MCH#

+3.3V_SUS
R395 8K2R2J-3-GP
C457 SCD1U10V2KX-4GP

+5V_RUN
C437 SC10U10V5KX-2GP
C428 SCD1U10V2KX-4GP

+2.5V_RUN
C404 SCD1U10V2KX-4GP
C433 SC10U10V5KX-2GP
C405 SCD1U10V2KX-4GP
+3.3V_RUN
C427 SC1U6D3V2KX-GP

At maximum load current of 600mA,the voltage across the LDO should be kept in the range of 0.5V to 1V

+3.3V_RUN
R434 10KR2J-3-GP
EC26 SCD1U10V2KX-4GP

R397 0R0402-PAD -1-20080514
PM_EXTTS# PM_EXTTS# 11
-1-20080514
R386 0R0402-PAD DOCK_PWR_SW# 34
-1-20080514
R389 0R0402-PAD POWER_SW_IN# 34

+RTC_CELL
R2504 100KR2J-1-GP
D757 BAT54A-3
POWER_SW_IN# 4002
R2542 0R2J-2-GP DY
R2594 0R2J-2-GP DY

FAN1
D36 SDMK0340L-7-F-GP
C491 SC22U6D3V5MX-2GP
MLX-CON4-19-GP
20.D0198.104
22,23 FAN1_DET#

+3.3V_RUN
C444 SC10U10V5KX-2GP
C451 SCD1U10V2KX-4GP

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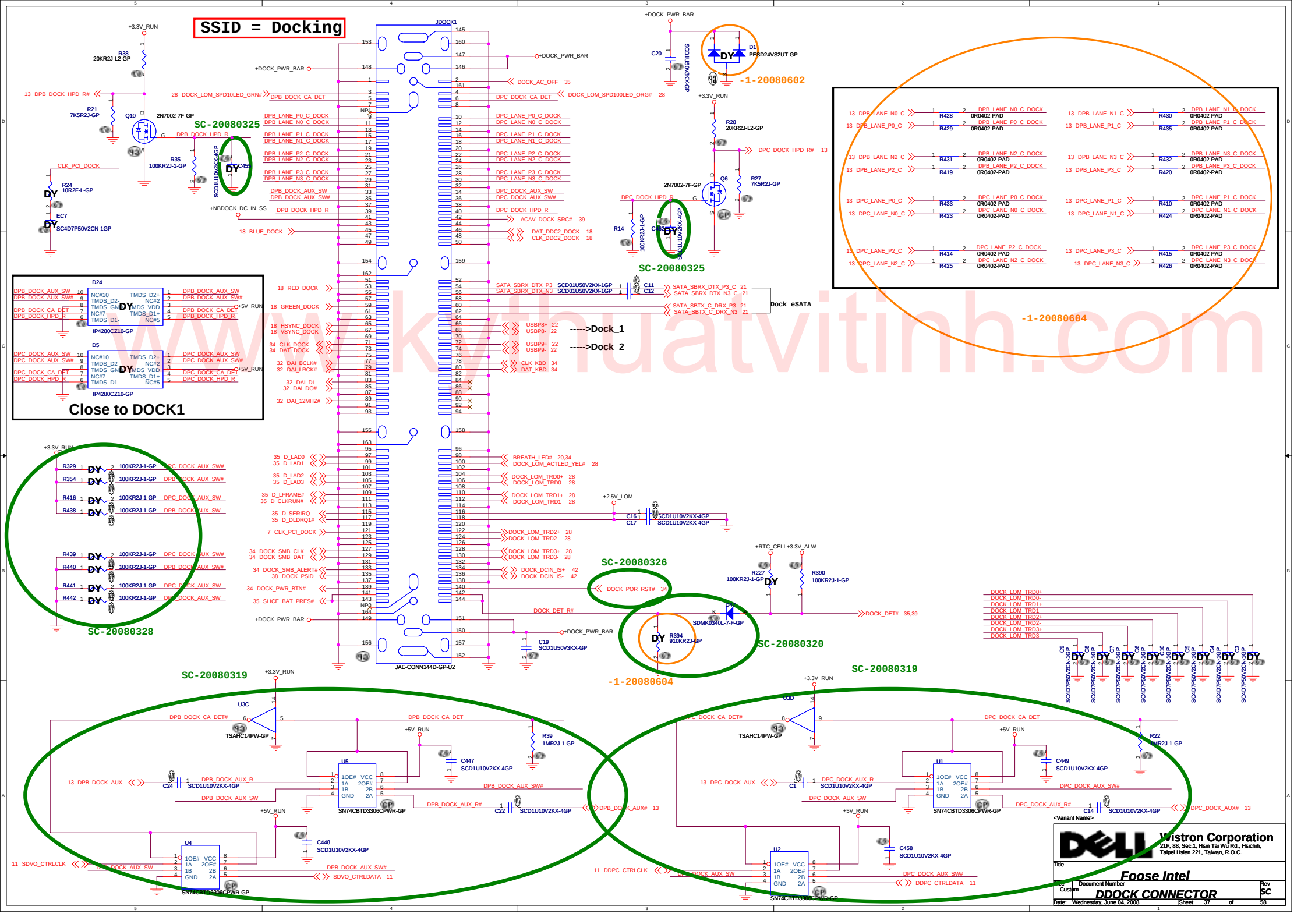
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Foose Intel
Size: A3
Document Number: Thermal/Fan EMC 4002
Rev: SC
Date: Friday, May 30, 2008
Sheet 36 of 58


SSID = Docking
JDOCK1
JAE-CONN144D-GP-U2
SC-20080325
SC-20080326
SC-20080328
SC-20080319
SC-20080320
-1-20080602
-1-20080604
Close to DOCK1
Dock eSATA
----->Dock_1
----->Dock_2
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Foose Intel
DDOCK CONNECTOR
Wednesday, June 04, 2008
Sheet 37 of 58

SSID = PWR.Support

PIN NAME DIFFERENCES

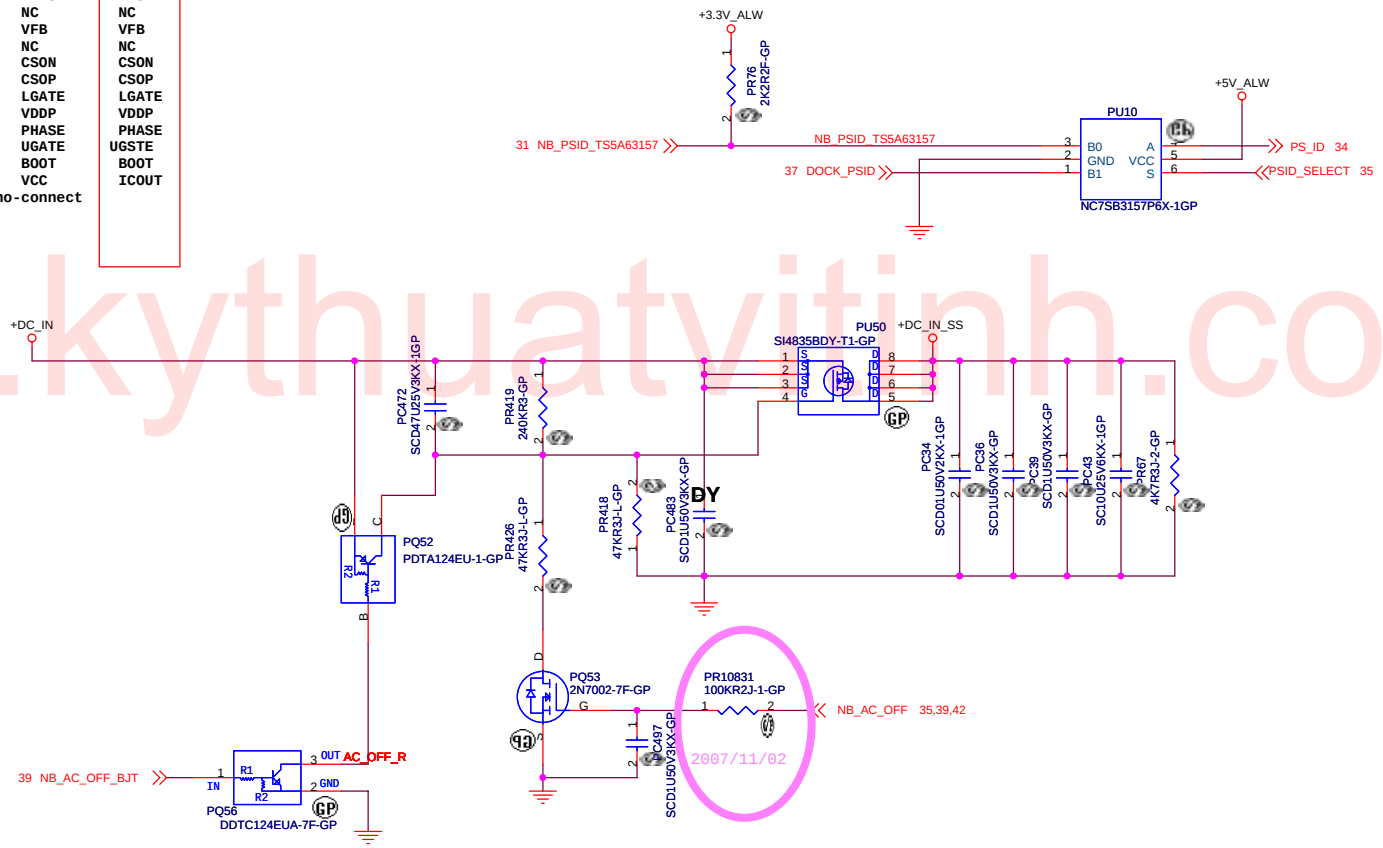
PIN	MAXIM	INTERSIL	BQ24745
1	GND	NC	ICREF
3	REF	VREF	VREF
4	CCS	ICOMP	EAO
5	CCI	NC	EAI
6	CCV	VCOMP	FBO
7	DAC	NC	CE
8	IINP	ICM	VICM
11	VDD	VDDSMB	VDDSMB
14	BATSEL	NC	NC
15	FBSA	VFB	VFB
16	FBSB	NC	NC
17	CSIN	CSON	CSON
18	CSIP	CSOP	CSOP
20	DLO	LGATE	LGATE
21	LDO	VDDP	VDDP
23	LX	PHASE	PHASE
24	DHI	UGATE	UGSTE
25	BST	BOOT	BOOT
26	VCC	VCC	ICOUT

"NC" means no-connect

TABLE

MAXIM & INTERSIL BOM DIFFERENCES

REF DES	MAXIM	INTERSIL	TI
R415	8.45K 1%	DUMMY	DUMMY
C489	0.01uF	0.1uF	0.1uF
C462	0.1uF 10V	DUMMY	200P 10V
C51	1uF 10V	DUMMY	1uF 10V
R75	365K 1%	215K 1%	309K 1%
R379	0 5%	10 5%	0 5%
R68	0 5%	10 5%	0 5%
C441	DUMMY	0.22uF	0.1uF
C463	DUMMY	0.22uF	0.1uF
C470	0.01uF	DUMMY	DUMMY
C471	0.1uF 10V	DUMMY	DUMMY
C30	220pF 50V	DUMMY	DUMMY
D11	RB751V-40	DUMMY	RB751V-40
C28	3.3nF	DUMMY	DUMMY
R44	1 1%	0 5%	0 5%
R388	100 5%	0 5%	0 5%
R489	0 5%	8.45K 1%	8.45K 1%
R424	10K 5%	2.2K 5%	4.7K 5%
C487	0.01uF	0.01uF	DUMMY
C467	0.01uF	0.01uF	DUMMY
R20	1K 5%	DUMMY	DUMMY
Q7	ISS355	DUMMY	DUMMY
C47	1uF 10V	1uF 10V	DUMMY
R73	33 1%	33 1%	DUMMY
R420	DUMMY	DUMMY	0 5%
R425	DUMMY	DUMMY	200K 5%
R423	DUMMY	DUMMY	7.5K 5%
C468	DUMMY	DUMMY	51P 10V
C485	DUMMY	DUMMY	2000P 10V
C469	DUMMY	DUMMY	130P 10V
C473	DUMMY	DUMMY	0.1uF
C42	DUMMY	DUMMY	0.1uF
R71	10K 1%	10K 1%	DUMMY
R352	DUMMY	DUMMY	10k 5%
R70	15.8K 1%	15.8K 1%	DUMMY
R58	DUMMY	10K 5%	DUMMY
R69	0 5%	10 5%	0 5%
C430	DUMMY	DUMMY	DUMMY
C49	DUMMY	DUMMY	DUMMY
R380	0 5%	10 5%	0 5%



MAX 8731A/ISL88731

Adapter (W)	Trip Current (A)	R377	R371	R373	R370
65	3.17	57.6K	13.0K	105	24.9K
90	4.43	51.1K	17.8K	348	33.2K

*R370 is populated if ADAPT_TRIP_SEL is used to program for the next lower adapter.

BQ247451

Adapter (W)	Trip Current (A)	R377	R371	R373	R370
65	3.17	57.6K	12.4K	205	24.3K
90	4.43	51.1K	16.9K	499	32.4K

*R370 is populated if ADAPT_TRIP_SEL is used to program for the next lower adapter.

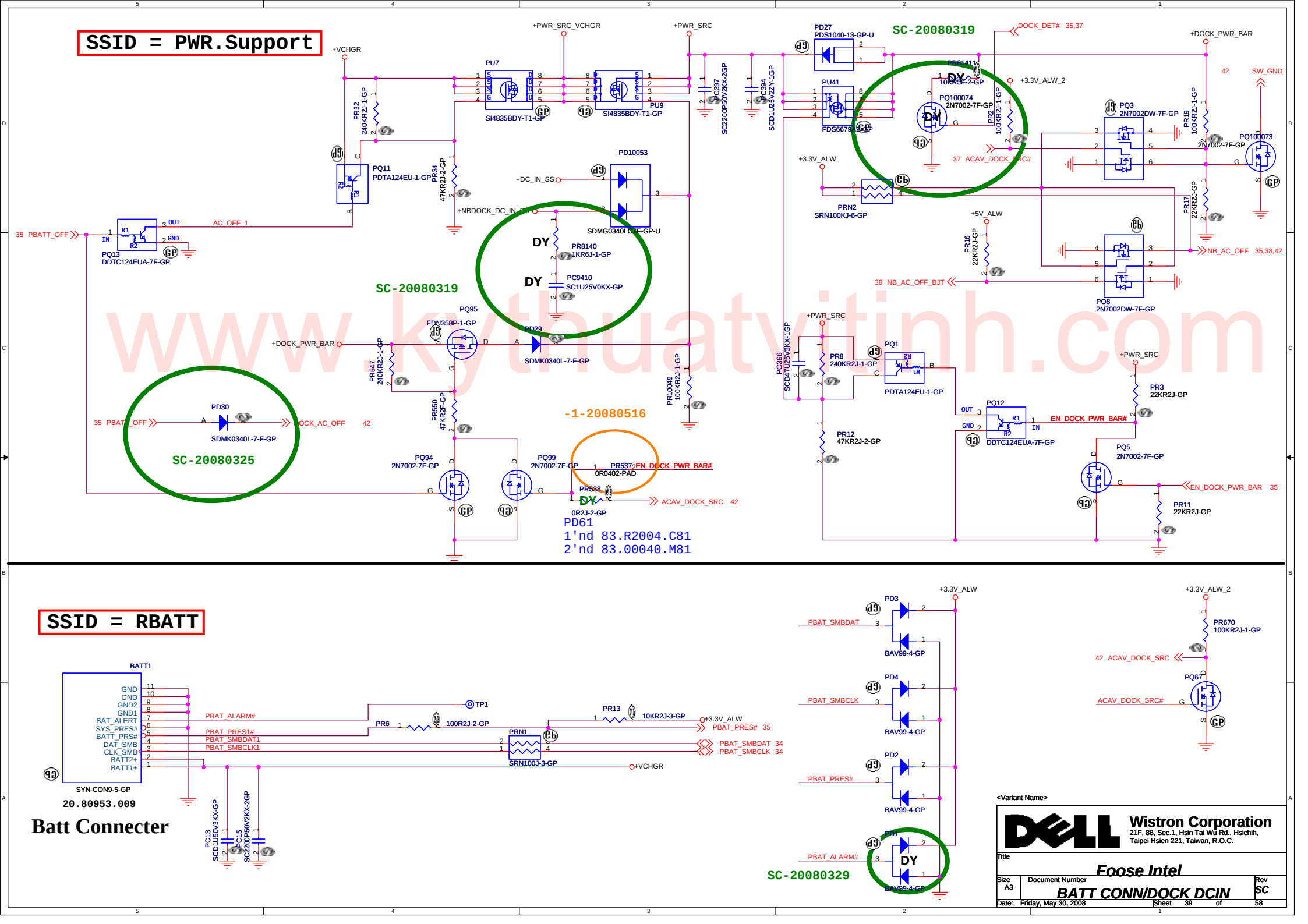
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

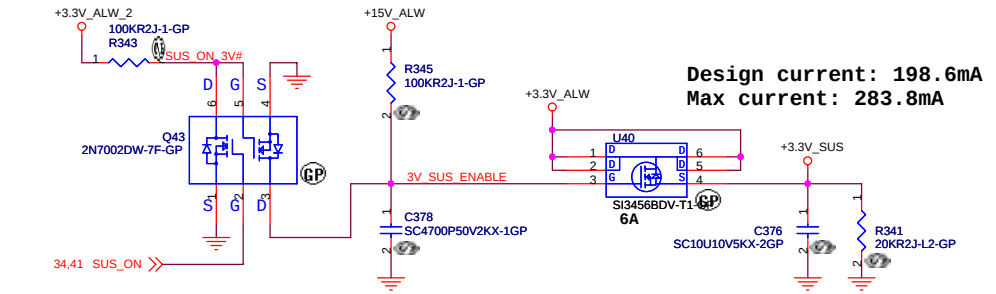
Title: Foose Intel

Size: A3 | Document Number: DCIN CONN | Rev: SC

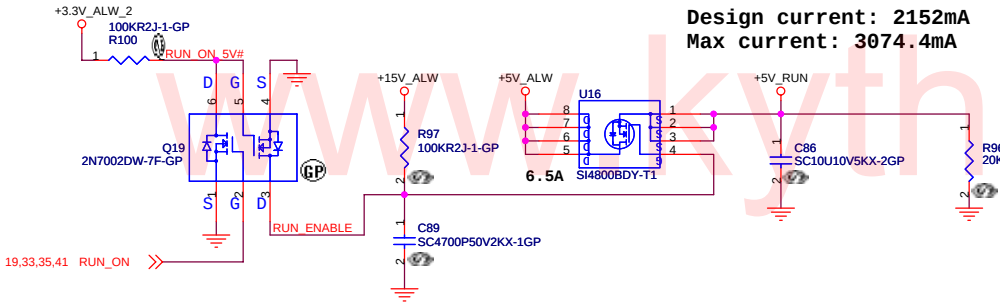
Date: Friday, May 30, 2008 | Sheet 38 of 58



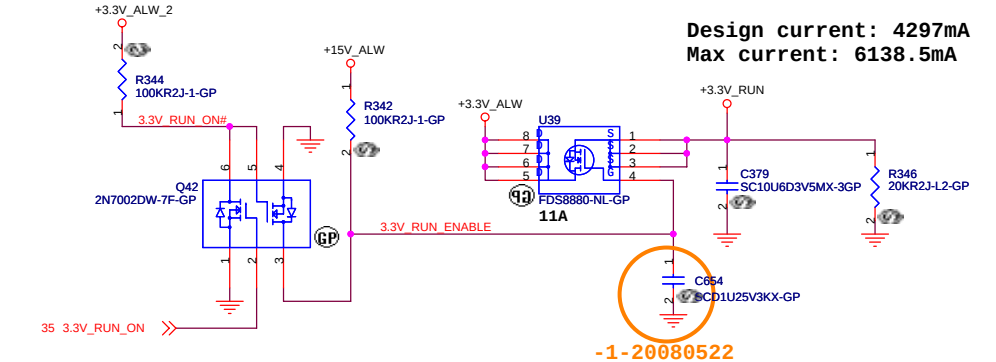
SSID = Reset.Suspend



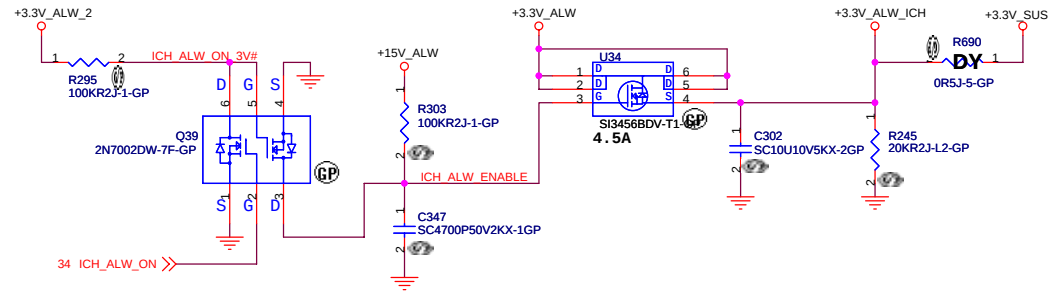
Design current: 198.6mA
Max current: 283.8mA



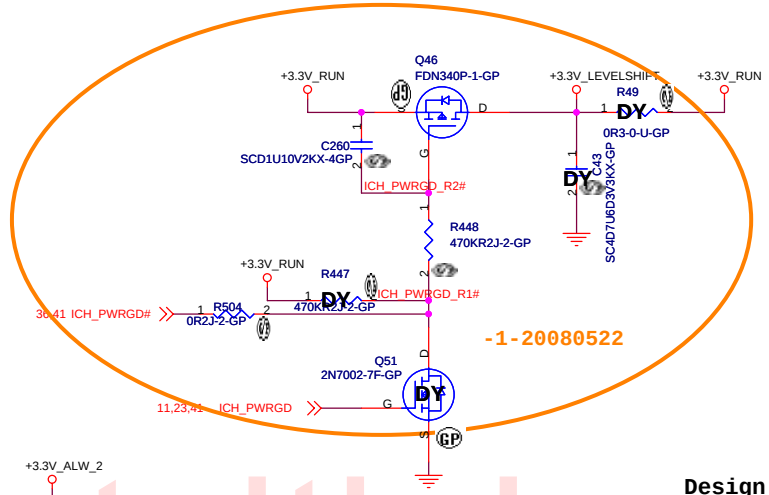
Design current: 2152mA
Max current: 3074.4mA

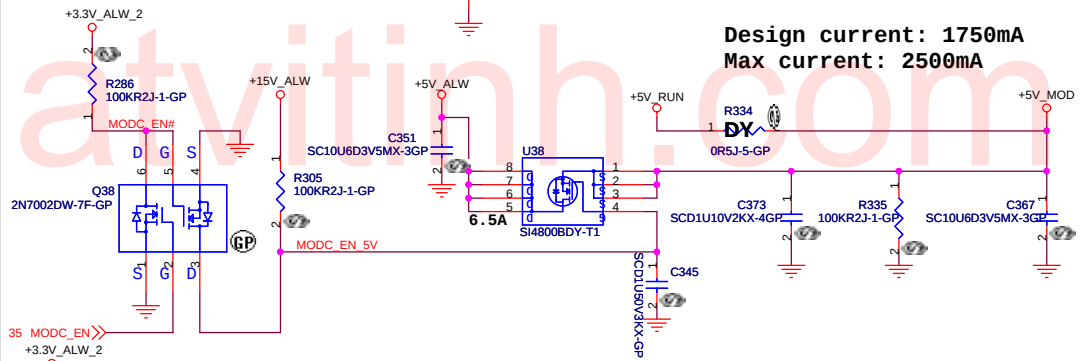


Design current: 4297mA
Max current: 6138.5mA

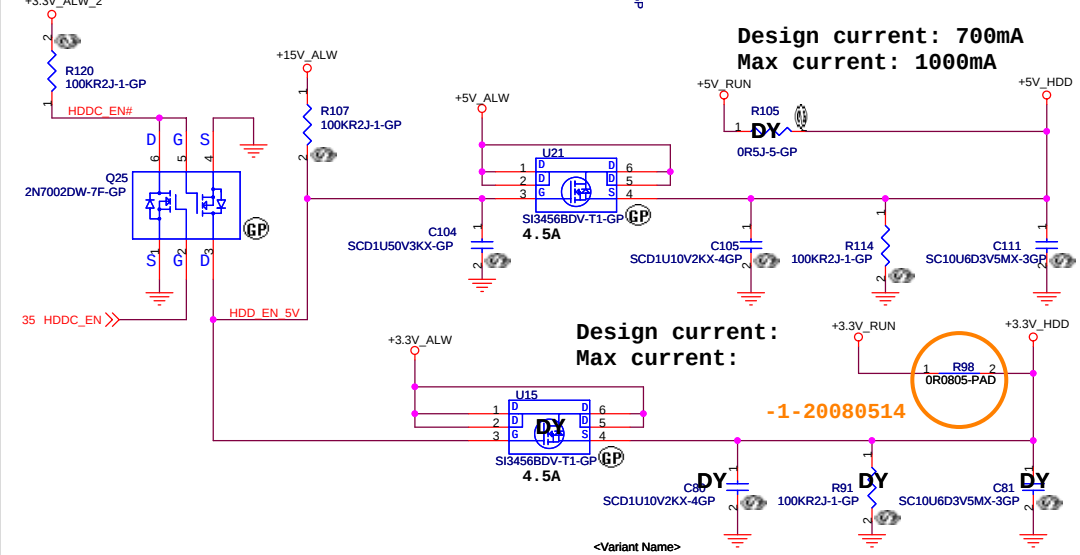


Design current: 682mA





Design current: 1750mA
Max current: 2500mA



Design current: 700mA
Max current: 1000mA

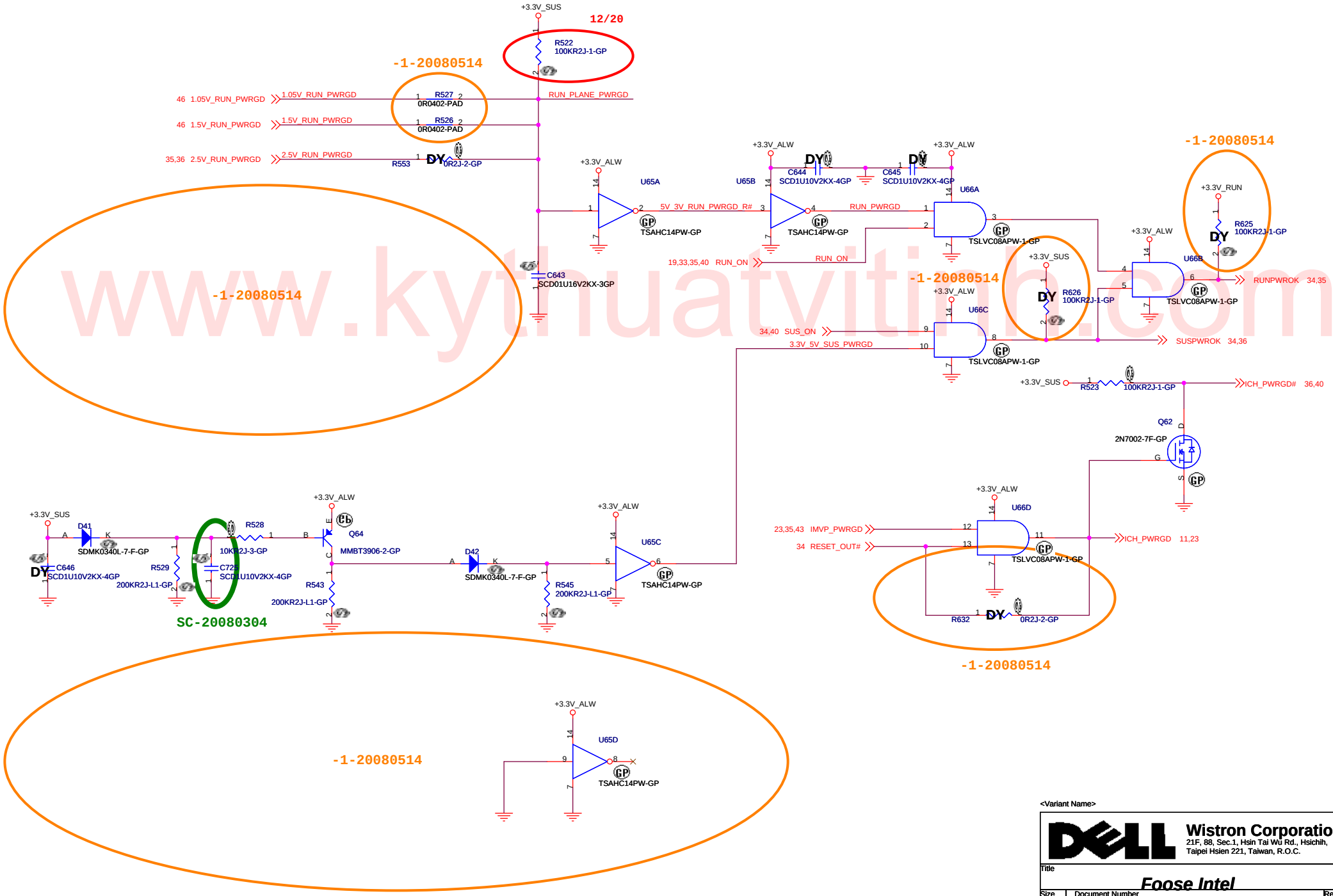
Design current:
Max current:

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Foose Intel	
Size: A3	Document Number: Power Plane Enable	Rev: SC
Date: Monday, June 02, 2008	Sheet 40 of 58	

SSID = Reset.Suspend



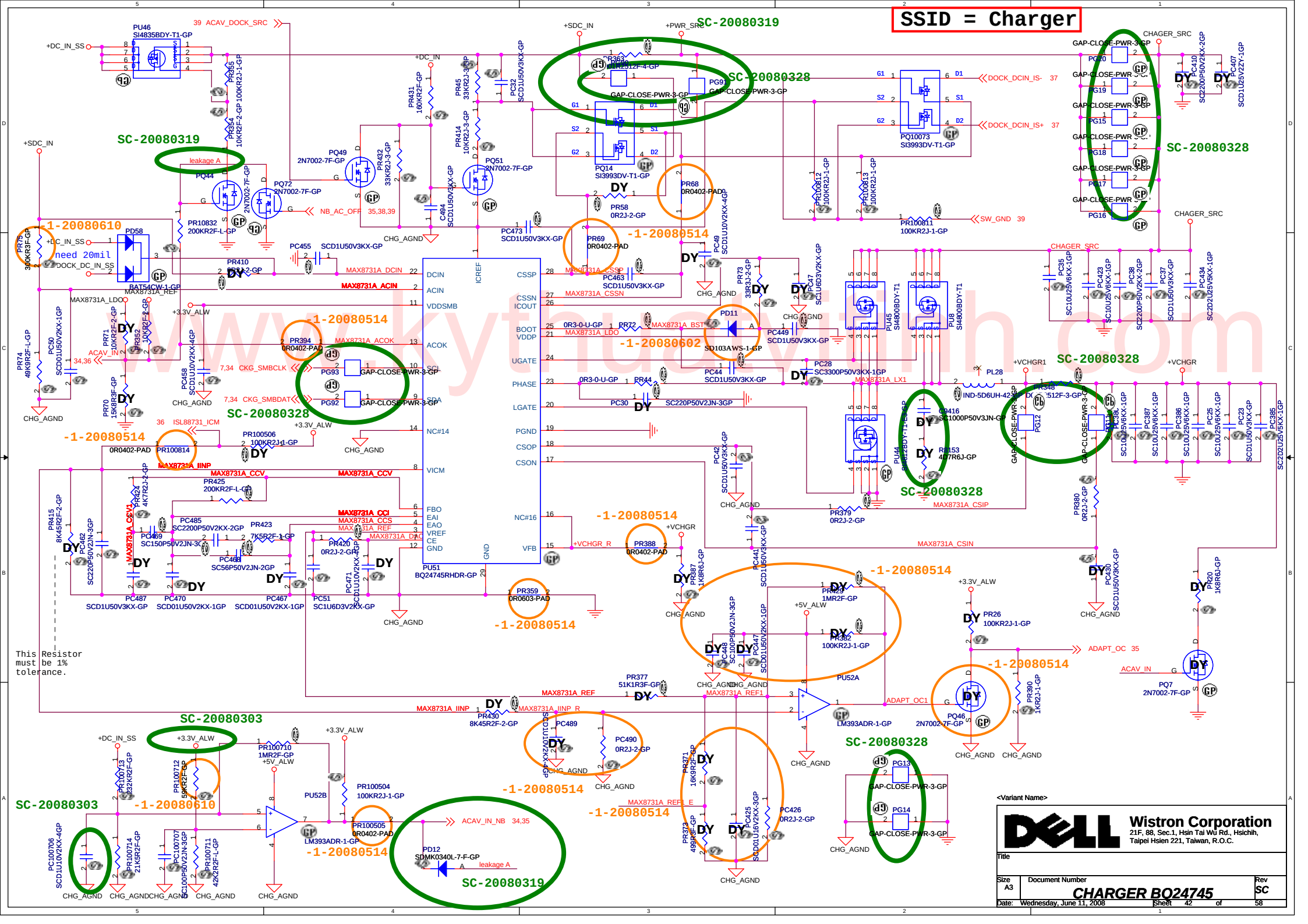
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Foose Intel

Size: A3 | Document Number: Power On Logic | Rev: SC

Date: Friday, May 30, 2008 | Sheet 41 of 58


SSID = Charger
SC-20080319
SC-20080328
SC-20080303
-1-20080610
-1-20080514
-1-20080602
This Resistor must be 1% tolerance.
need 20mil
leakage A
MAX8731A_ACIN
MAX8731A_IINP
MAX8731A_CCV
MAX8731A_CCI
MAX8731A_CCS
MAX8731A_REF
MAX8731A_DAC
MAX8731A_CSSP
MAX8731A_CSSN
MAX8731A_BST
MAX8731A_LX1
MAX8731A_CSIP
MAX8731A_CSIN
MAX8731A_LDO
MAX8731A_ACOK
MAX8731A_DCIN
MAX8731A_REF1
MAX8731A_IINP_R
MAX8731A_REF_E
ISL88731_ICM
CKG_SMBCLK
CKG_SMBDAT
NB_AC_OFF
ADAPT_OC
ADAPT_OC1
ACAV_IN
ACAV_IN_NB
DOCK_DCIN_IS-
DOCK_DCIN_IS+
SW_GND
+DC_IN_SS
+SDC_IN
+PWR_SRC
+DC_IN
+3.3V_ALW
+5V_ALW
+VCHGR
+VCHGR1
+VCHGR_R
CHAGER_SRC
CHG_AGND
ICREF
GND
DCIN
ACIN
VDDSMB
CSSP
CSSN
ICOUT
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#14
NC#16
VICM
FBO
EAI
EAO
VREF
CE
VFB
SCL
SDA
PU51 BQ24745RHDR-GP
PU52A LM393ADR-1-GP
PU52B LM393ADR-1-GP
PQ14 SI3993DV-T1-GP
PQ10073 SI3993DV-T1-GP
PU45 SI4800BDY-T1
PU8 SI4800BDY-T1
PU44 SI4812BDY-T1-E3-GP
PD11 SD103AWS-1-GP
PD12 SDMK0340L-7-F-GP
PL28 IND-5D6UH-42-GP
BAT54CW-1-GP
GAP-CLOSE-PWR-3-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
<Variant Name>
Title
Size A3
Document Number CHARGER BQ24745
Rev SC
Date: Wednesday, June 11, 2008
Sheet 42 of 58

SSID = CPU.Regulator

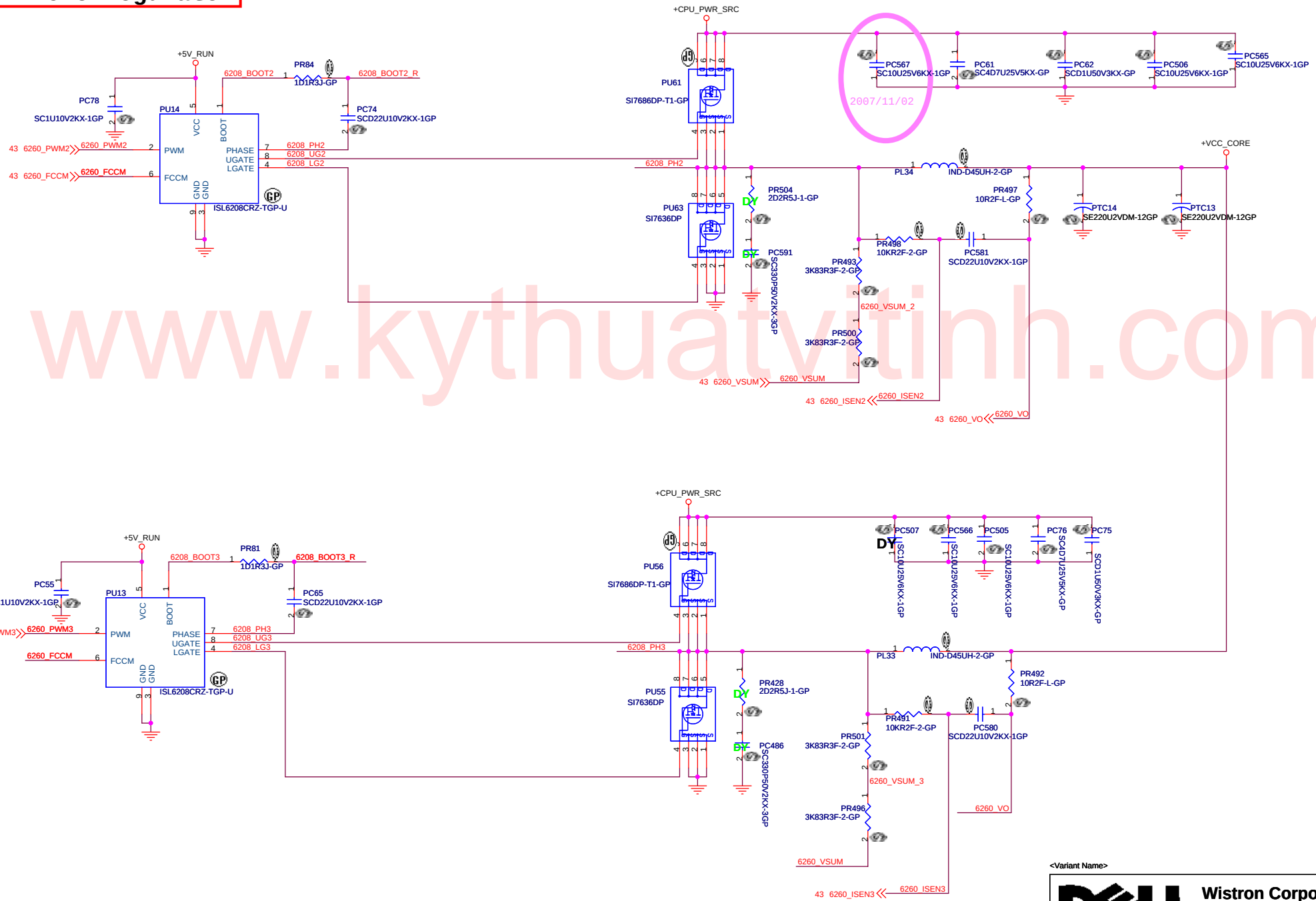
I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.45UH ETQP4LR45XFC/ 68.R4510.10A
O/P cap: 330U 2V EEFSX0D331XE/ 79.33719.20L
H/S: SI7686DP/ POWERPAK-8/ 14mOhm/ 4.5Vgs/ 84.07686.037
L/S: SI7336ADP/ POWERPAK-8/ 4.8mOhm/ 4.5Vgs/ 84.07636.037

SC-20080320
SC-20080328
SC-20080401
-1-20080514

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Foose Intel
Size: A3 | Document Number: CPU Core-01 | Rev: SC
Date: Monday, June 02, 2008 | Sheet 43 of 58

SSID = CPU.Regulator



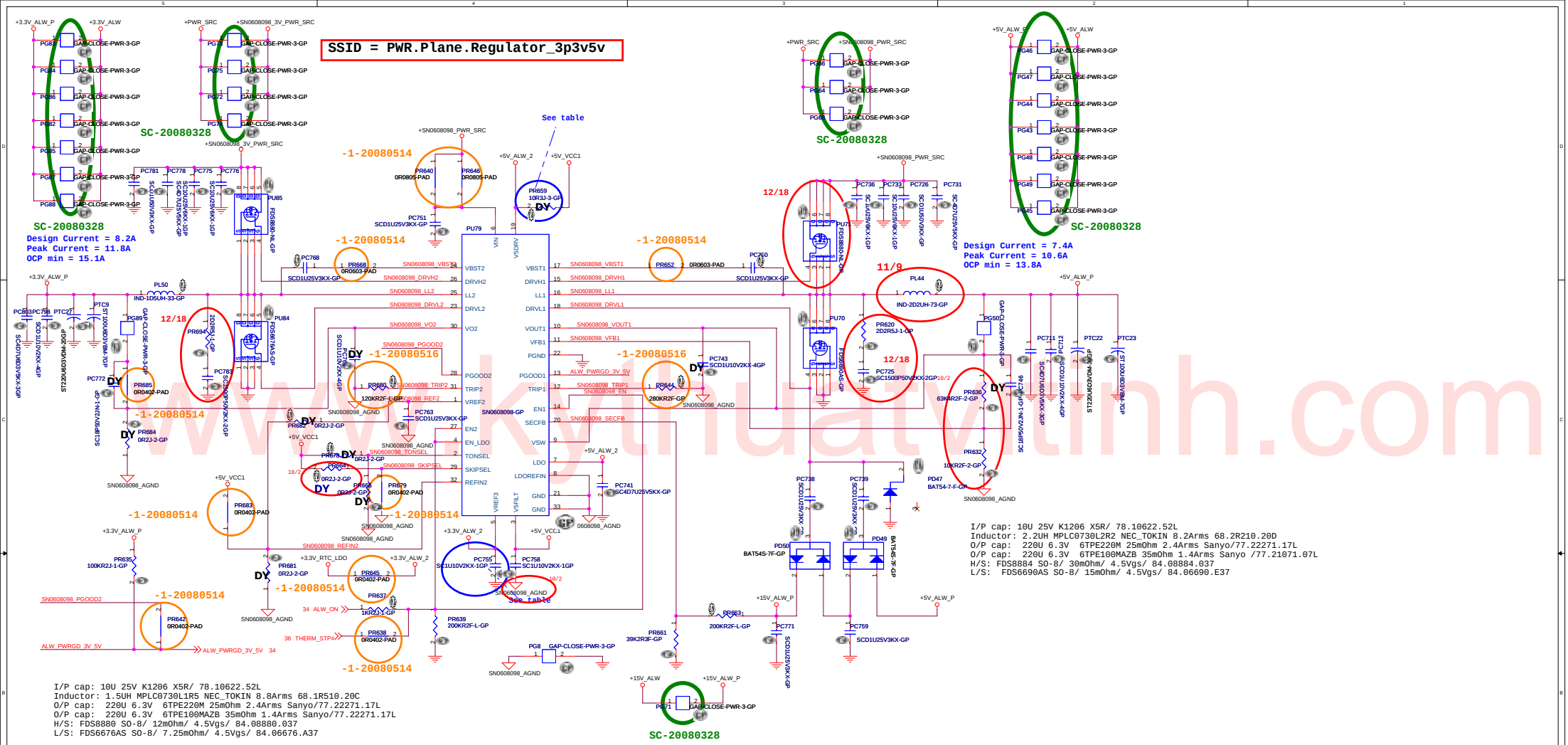
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Foose Intel

Size: A3 | Document Number: CPU Core-02 | Rev: SC

Date: Friday, May 30, 2008 | Sheet 44 of 58



SKIPSEL	GND	FLOAT/VREF2	V5IN
Operating Mode	Auto Skip	OATM	PWM

TONSEL	GND	VREF2 or Float	V5FILT
CH1 Freq	400kHz	400kHz	200kHz
CH2 Freq	500kHz	300kHz	300kHz

	TABLE1		
	MAXIM ,INTERSIL & TI BOM differences		
	MAXIM	INTERSIL	TI
R	10ohm	NO STUFF	NO STUFF
C	1uF	0.1uF	1uF

		Min	Typ	Max
VOUT2 Output	3.3V Preset Output: REFIN2 = 5V, VIN = 5.5V to 28V, SKIPSEL = 5V	3.285 (-1.4%)	3.33	3.375 (+1.4%)
	1.05V Preset Output: REFIN2 = 3.3V, VIN = 5.5V to 28V, SKIPSEL=5V	1.038 (-1.2%)	1.05	1.062 (+1.2%)
	Tracking Output: REFIN2 = 1.0V, VIN = 5.5V to 28V, SKIPSEL = 5V	0.99 (-1%)	1.00	1.01 (+1%)

5756

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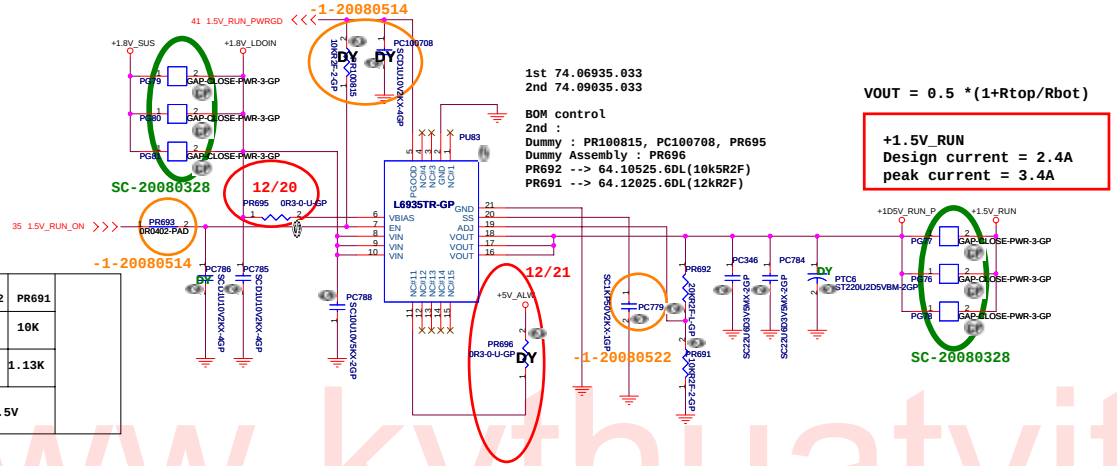
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Foose Intel

Size: A2 | Document Number: DCDC 5V/3V (SN0608098) | Rev: SC

Date: Tuesday, June 03, 2008 | Sheet 45 of 58

SSID = PWR.Plane.Regulator_1p5v1p05v



1st 74.06935.033
2nd 74.09035.033

BOM control
2nd :
Dummy : PR100815, PC100708, PR695
Dummy Assembly : PR696
PR692 --> 64.10525.6DL(10k5R2F)
PR691 --> 64.12025.6DL(12KR2F)

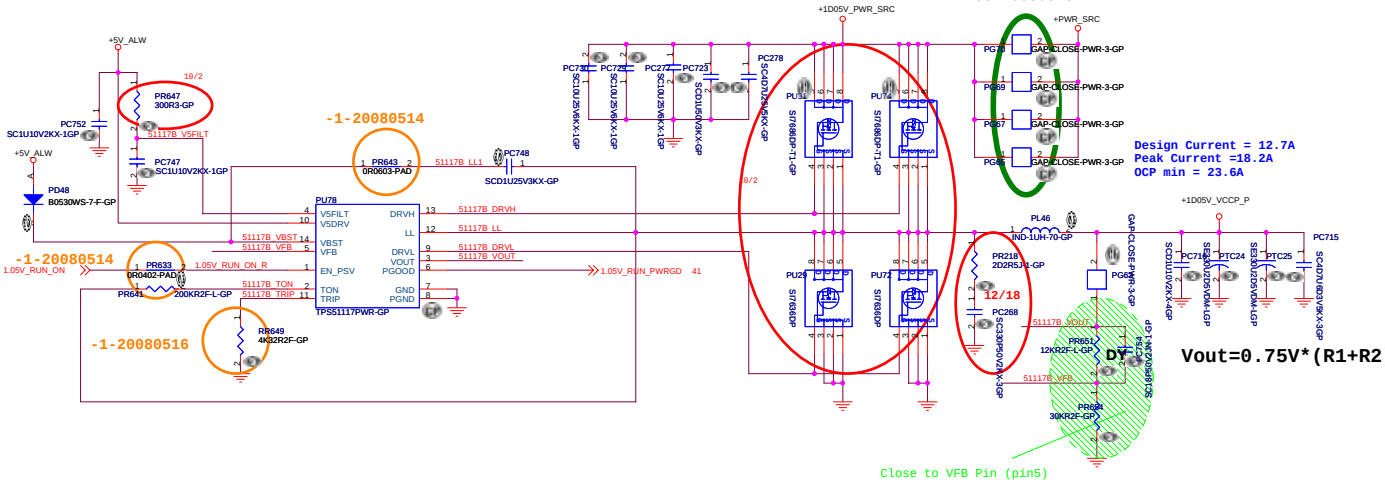
VOUT = 0.5 *(1+Rtop/Rbot)

+1.5V_RUN
Design current = 2.4A
peak current = 3.4A

Vendor	PIN6	PIN11	PIN20
L6935	VBIAS	N.C.	SS
RTXX35	N.C.	VBIAS	N.C.

Vendor	PR696	PR695	PR692	PR691
L6935	DY	ASM	20K	10K
RTXX35	ASM	DY	1K	1.13K
			1.5V	

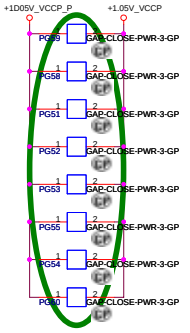
Vendor	PR586/PR588	PR585/PR587	PR572	PR573	PR615	PR612
L6935	DY	ASM	20K	10K	16K	10K
RTXX35	ASM	DY	1K	1.13K	1.4K	2K
			1.5V		1.35V	

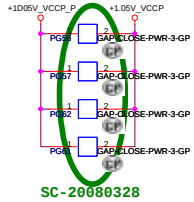


Design Current = 12.7A
Peak Current =18.2A
OCP min = 23.6A

Vout=0.75V*(R1+R2)/R2

Close to VFB Pin (pin5)





I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH MPLC1040L1R0 NEC_TOKIN 16.2Arms 68.1R01A.20D
O/P cap: 330U 2.5V 2R5TPE330MF 15mOhm 3.1Arms Sanyo/ 77.23371.L01
H/S: SI7686DP PowerPAK/ 11mOhm/ 4.5Vgs/ 84.07686.037
L/S: SI7636DP PowerPAK/ 4mOhm/ 4.5Vgs/ 84.07636.037
Switching freq-->400KHz

<Variant Name>

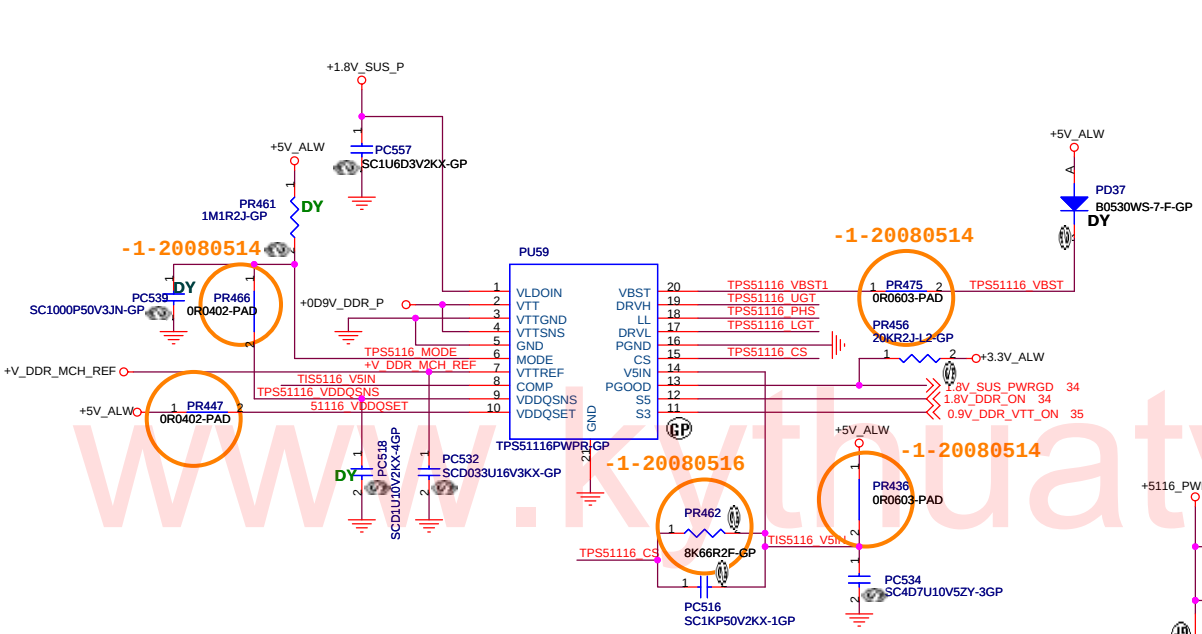
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

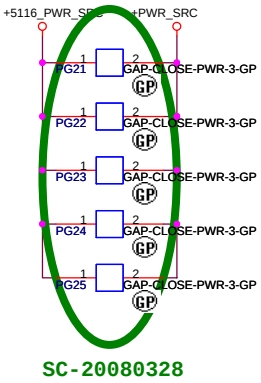
Title: Foose Intel

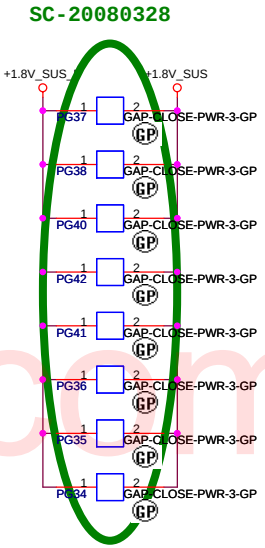
Size	Document Number	Rev
A2	DCDC 1D5V/1D05 (TPS5117)	SC

Date: Friday, May 30, 2008 Sheet 46 of 58

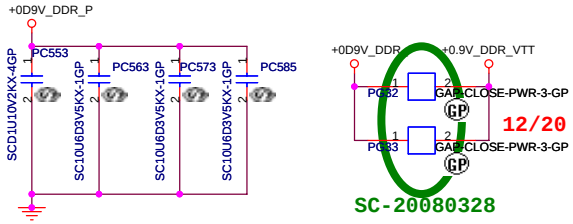
SSID = PWR.Plane.Regulator_1p8v0p9v

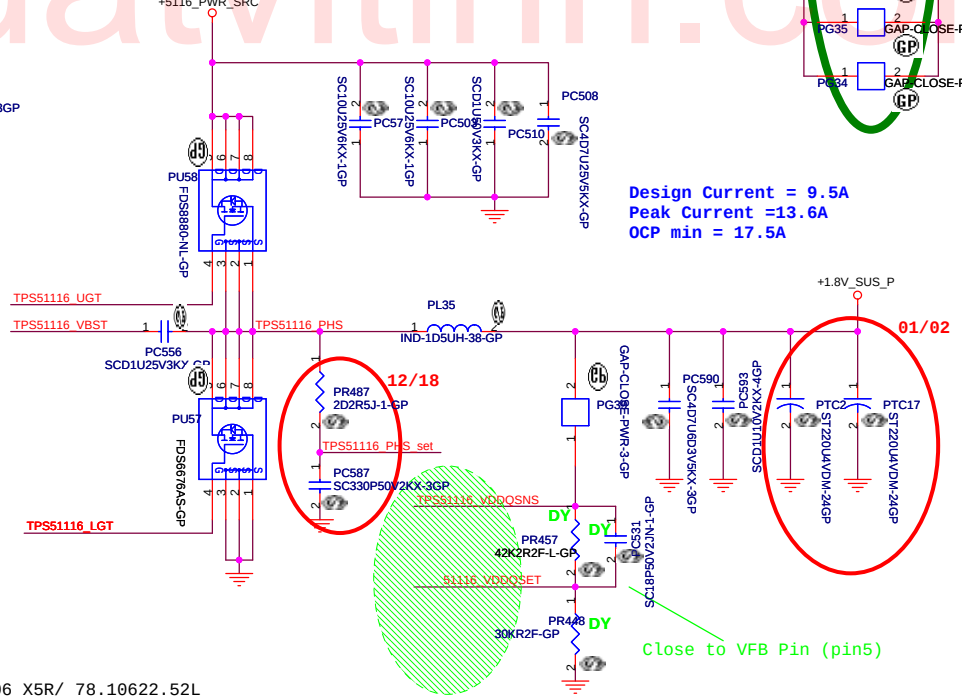






TI TPS51116 for 1.8V and 0.9V





Design Current = 9.5A
Peak Current =13.6A
OCP min = 17.5A

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

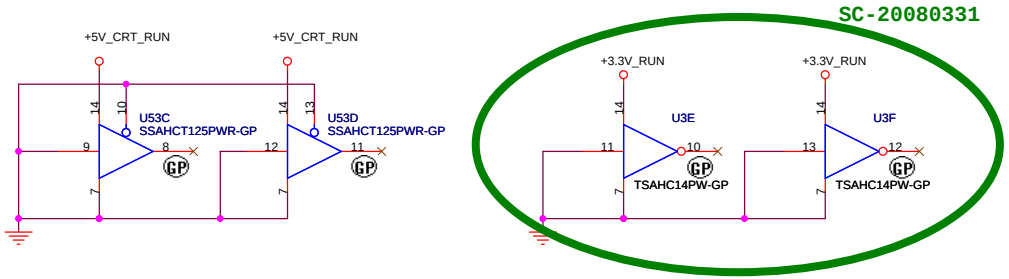
I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH MPLC1040L1R5 NEC_TOKIN 12.7Arms 68.1R510.20D
O/P cap: 220U 4V ST220U4VDM 40mOhm 1.9Arms Sanyo/77.22271.19L
H/S: FDS8880 SO-8/ 12mOhm/ 4.5Vgs/ 84.08880.037
L/S: FDS6676AS SO-8/ 7.25mOhm/ 4.5Vgs/ 84.06676.A37
Switching freq-->400KHz

<Variant Name>

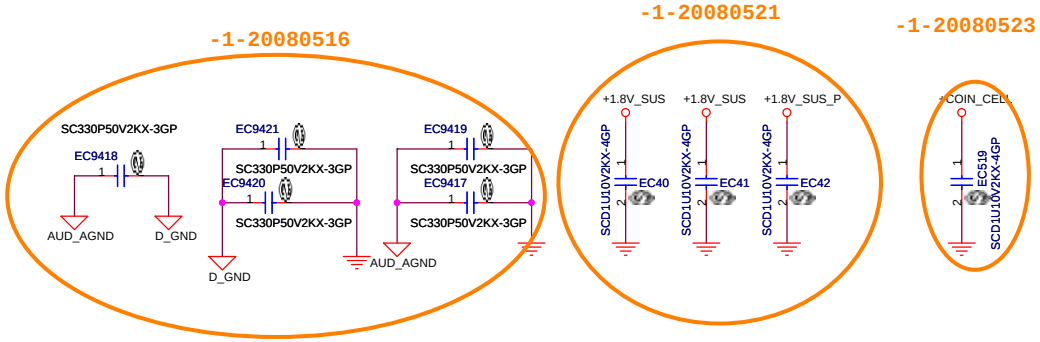
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Foose Intel
Size: A3 | Document Number: DCDC 1.8V/0.9V(TPS5116) | Rev: SC
Date: Friday, May 30, 2008 | Sheet 47 of 58

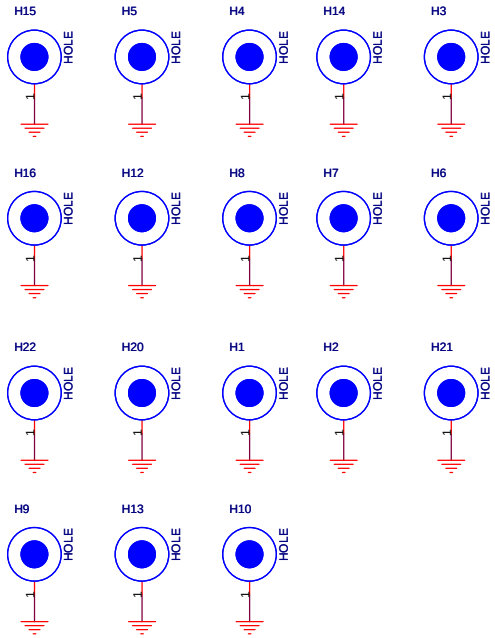
SSID = VIDEO



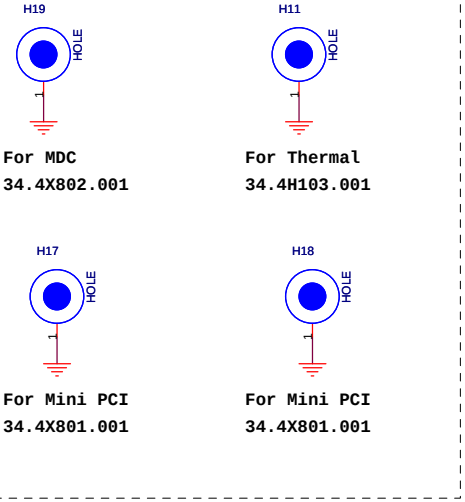
SSID = EMC



SSID = Mechanical



Stand off, all on the CPU socket side

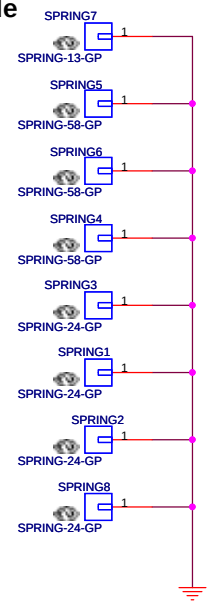


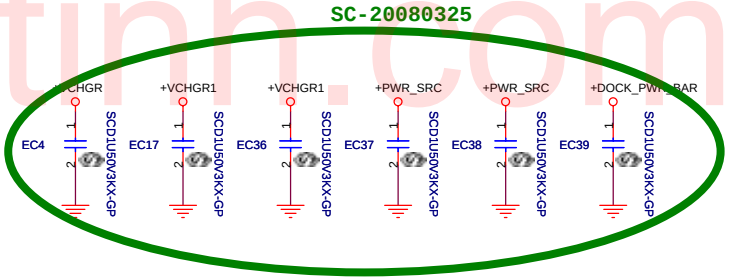
For MDC
34.4X802.001

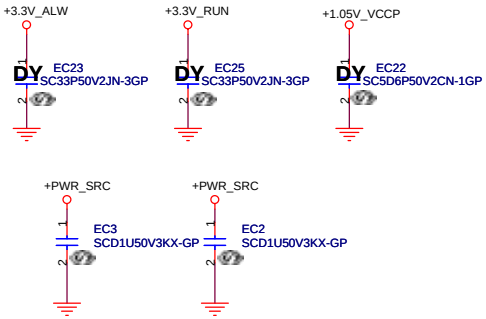
For Thermal
34.4H103.001

For Mini PCI
34.4X801.001

For Mini PCI
34.4X801.001







For RF team

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Version Change List

Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
1	32,19	2007/10/25	IDT	SPDIF_SHDN is no longer used in Dell's M09 audio architecture.	Remove net SPDIF_SHDN from U49 GPIO5 and delete U67.	X01
2	34	2007/10/25	DELL	MEC5035 pin 19 should be RC_ID and pin 30 should be connected with SUSPWROK	Pop R258 and Dummy R259.	X01
3	29	2007/10/25	DELL	Modify 2 capacitors for EMI protection.	Change C87,C88 from 1Kp to 300p.	X01
4	30	2007/10/25	DELL	Reserve an option for WiMAX LED.	Add R724(DUMMY).	X01
5	11	2007/12/26	DELL	Add level shift circuit for Cantiga HDA interface.	Add U90,R373,R377,C7280,C7279,R359,R355,R379,R363 Delete Q69,Q71,RN87,R727,R732,C827,R730,R729,Q70	X01
6	22	2007/11/06	DELL	Remove one SPI flash ROM.	Delete U68.	X01
7	23	2007/11/06	Wistron	Reserve an option for AC_PRESENT GPIO function.	Add R725(0 ohm)	X01
8	14	2007/11/06	Wistron	Follow Intel Montevina CRB Schematics for VCC_PEG.	Change L49 to R1836(0 ohm)	X01
9	22	2007/11/06	Wistron	Follow Intel Montevina design guide revision 1.0.	Change R600 PU from +1.05V_VCCP to +1.5V_RUN.	X01
10	40	2007/11/06	Wistron	Fine tune +3.3V_RUN power sequence.	Change C377(0.1u) to C654(470p).	X01
11	6	2007/11/06	Wistron	ITP connector dummy. So serial resistors dummy.	Dummy R51,R55.	X01
12	31	2007/11/06	Wistron	Correct USB differential pair connection.	U20 pin3,pin5 swap.	X01
13	24	2007/11/06	Wistron	Follow Intel Montevina design guide revision 1.0 to disable Intel LAN function.	Delete L41,C260,C702 and add C977(0.1u) for ICH PinA27.	X01
14	34,35	2007/11/08	DELL	GPIO table(10/25)update MEC5035: 1.Updated RC_ID system configurations ECE5028: 2.Changed pin82 GPIOB2 from USB_CHARGER_PWR_EN# to ESATA_USB_PWR_EN# 3.Change pin104 GPIOA7 from ESATA_USB_PWR_EN# to USB_POWERSHARE_PWR_EN#	1.Pop R261 and C310,Change C310 from 220p to 4700p. 2.Changed 5028 pin82 GPIOB2 from USB_CHARGER_PWR_EN# to ESATA_USB_PWR_EN# 3.Change 5028 pin104 GPIOA7 from ESATA_USB_PWR_EN# to USB_POWERSHARE_PWR_EN#	X01
15	22,25,35	2007/11/09	DELL	MDC_RST_DIS# change from ICH9M to 5028 pin102 MDC_RST_DIS# pullup voltage should be +5V_ALW	MDC_RST_DIS# change from ICH9M to 5028 pin102 R302 change PU from +3.3V_RUN to +5V_ALW	X01

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Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
16	35	2007/11/09	DELL	2.5V_RUN_PWRGD is OD pin need to PH.	Pop R283.	X01
17	37	2007/11/09	DELL	add "+NBDOCK_DC_IN_SS" to dock connector pin41 for battery protection.	add "+NBDOCK_DC_IN_SS" to dock connector pin41 for battery protection.	X01
18	33	2007/11/09	DELL	Correct Internal MIC schematics.	Add R1542(100k ohm) resistor between U48B pin6 and pin7.	X01
19	20	2007/11/09	Wistron	Correct LED leakage issue.	Change R1,R31,R15,R86,R101,R136,R187,R87,R88 from 10K ohm to 20K ohm.	X01
20	29	2007/11/15	Wistron	LAN connector LED color mapping correction.	RJ1 pinA1 change net name to green LED, pinA3 change net name to orange LED, pinB2 change net name to yellow LED.	X01
21	23	2007/11/16	DELL	ICH9 GPIO11 pull high power plan correction.	Change R224 pull high from +3.3V_RUN to +3.3V_ALW_ICH	X01
22	21	2007/11/21	Wistron	Follow Intel design guide for internal VRM pull high resistor.	Change R203, R206 pull high resistance from 330K 5% to 332K 1%.	X01
23	7,28,32	2007/11/21	KDS	Follow Crystal vendor KDS's test report to change capacitance.	Change C187,C176 from 12pF to 10pf. Change C207 from 27 pf to 33pf. Change C393,C398 from 27pf to 12pf.	X01
24	34	2007/11/22	Wistron	RoHS issue.	Change X6 crystal Vendor from KDS to EPSON. And change C722 from 27pf to 33pf.	X01
25	35	2007/11/23	Wistron	Change Board ID for X01.	Pop R296, Depop R310.	X01
26	31	2007/11/26	DELL	Follow DELL spec to change USB power switch.	Change U13 from TPS2062D to TPS2062AD.	X01
27	36	2007/11/29	DELL	Request by TDC,Peace. GG_List 20071128.	change R362 from 22 ohm to 0 ohm.	X01
28	36	2007/11/29	DELL	Request by TDC,Peace. GG_List 20071128.	Add U87,C2706,R2542(DY),R2594(DY).	X01
29	34	2007/11/29	DELL	Request by TDC,Peace. GG_List 20071128. Dummy SPI ROM and related component(R and C) on EC side.	Dummy R671,R625,R626,U75,R657,R656,R655,C753.	X01
30	34,36,37 39,42	2007/11/30	DELL	Request by TDC,Peace. GG_List 20071128.	Netname need to change as below: From "ACAV_IN_DOCK" to "ACAV_DOCK_SRC" From "ACAV_IN_DOCK#" to "ACAV_DOCK_SRC#" From "ACAV_IN_MB/DOCK" to"ACAV_IN"	X01
31	35	2007/11/30	DELL	Request by TDC,Peace. GG_List 20071128.	Add U88 and C2707.	X01

Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
32	35,42	2007/11/30	DELL	Request by TDC,Peace. GG_List 20071128.	ECE5028 pin70 NC(delete ADAPT_TRIP_SEL) and delete R370.	X01
33	36,42	2007/11/30	DELL	Request by TDC,Peace. GG_List 20071128.	Add connection from MAX8731A_IINP(Charger pin8) to EMC4002 pin45 and add R2202 resistor between the connection	X01
34	20	2007/11/30	Wistron	Correct I/O Board LED twinkle issue when adapter plug in.	Add R2838 PU to +3.3V_ALW and remove R180.	X01
35	7	2007/11/30	Wistron	Follow Intel CRB.	Change R562 from 2.2K to 10K.	X01
36	28	2007/12/03	Broadcom	Make sure the PWR_DOWN pin is only pulled to GND and never asserted (Sighting S2_5761_31695).	Dummy R549.	X01
37	32	2007/12/04	IDT	Change thermal pad from GND to NC pin.	U49 pin 49 NC.	X01
38	36	2007/12/05	Wistron	Request by Power Team	Change R2202 pin2 connect to ISL88731_ICM, Change R2202 pin1 net name to ISL88731_ICM_4002	X01
39	30	2007/12/05	DELL	Add OR gate for WWAN,WPAN radio disable.	Add D53 and R710(DY),	X01
40	36	2007/12/05	DELL	Use diode to implement OR gate.	Delete C2706 and U87. Add D757,R2504.	X01
41	30,31	2007/12/05	Wistron	IO board connector swap 180	Modify IOB1 schematics. WWAN1 pin8,10,12,14,16 change to NC. Delete C46,C31	X01
42	32,33	2007/12/05	Wistron	Audio GND noise issue.	Add R370,R214,R180 three 0 ohm resistance C576.2,C523.2,C498.2,U62.8,C525.2,C524.2,C431.2, C464.2,C465.2,U49.26,U49.42 connect to AUD_AGND	X01
43	18	2007/12/06	Wistron	CRT issue	C445, C432, C419 change from 6.8pF to 2.2pF. L30, L31, L32 change from 30 ohm to 22 ohm bead. Dummy C435, C436.	X01
44	28	2007/12/06	Wistron	BCM5756 request	When use BCM5756, R579,R580 Dummy When use BCM5761, R579,R580 Non-Dummy	X01
45	32	2007/12/06	IDT	Codec thermal pad needn't connect to GND.	U49 pin49 NC	X01
46	32	2007/12/06	Wistron	Follow M09 audio refence schematics.	Delete C411 short U49 pin23,24 Change C412 from 1uF to 0.1uF	X01

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47	21	2007/12/11	Wistron	Eye diagram fail.	Change R634 from 24.9 ohm to 21 ohm.	X01
48	18	2007/12/11	Wistron	Prevent leakage form CRT SWITCH to +3.3V_RUN	Add D54	X01
49	34	2007/12/14	Dell	Request by TDC,Peace. GG_List 20071213.	Remove U76 and C742	X01
50	23	2007/12/14	Dell	Change PCIE_MCARD1_DET# pull high power rail to +3.3V_ALW_ICH because ICH9M GPIO24 is suspend power plane.	Dummy R231 and add R309(PCIE_MCARD1_DET#) pull high to +3.3V_ALW_ICH	X01
51	11	2007/12/14	Dell	Intel recommend that SDVO_CTRLCLK/SDVO_CTRLDATA and DDPC_CTRLCLK/DDPC_CTRLDATA need to change PH resistor from 100K to 4.02K for Display Port	Change RN15 and RN4 from 100K to 4.7K ohm.	X01
52	6,14	2007/12/14	Dell	Intel recommend to depop D19,R181,R56	Dummy D19,R181,R56	X01
53	13	2007/12/14	Dell	Intel recommend to Change LVDS_IBG PD resistor to 2.4K	R173 change to 2.4K	X01
54	36	2007/12/14	Dell	Disable EMC4002 LDO.	Dummy R399. Add R607(10K) to GND.	X01
55	34	2007/12/14	Dell	Change RCID pull high resistor from 1K to 2K.	R261 change from 1K to 2K ohm.	X01
56	18,19	2007/12/14	Dell	Due to TV function be removed from LIO Docking, connect TV signals to MB TV connecter directly	NC U25 pin15,19,20,22,23,25,26,29,31 NB TV_CVBS,TV_C,TV_Y connect to page19 directly	X01
57	19,20	2007/12/14	Wistron	Battery LED color correction.	Use U20 GPIO156 to control amber battery LED, Use U20 GPIO157 to control blue battery LED.	X01
58	28,29	2007/12/15	Wistron	LPC concern for TPM and China TPM.	Add R542,R594,R595,R596,R597 and set BOM control.	X01
59	33	2007/12/15	Dell	To limit the headphone FSOV.	Add R6698,R6504(1K) to net AUD_HP1_OUT_R1 and AUD_HP1_OUT_L1.	X01
60	14	2007/12/17	Wistron	CRT water-wave issue.	Delete L3. Add U89, C8335(1uF),8336(1uF),R8139(0 ohm)	X01
61	19,20	2007/12/19	Wistron	Breath power LED color correction.	Add Q74,R7240,EC35	X01

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Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
62	32,33	2007/12/19	Wistron	Audio noise GND issue.	Change page 32,33 some GND to D_GND and AUD_AGND	X01
63	13,37	2007/12/28	DELL	DVI SMbus and Display port AUX,AUX# issue.	Add U2,U4,RN138,RN137,RN280,RN281,R5733, R5734,R5728,R5731. Modify U1,U3,U5.Delete R10, R36. Add dummy parts RN143,RN144,R4,R5,R6,R8.	X01
64	34,37	2007/12/28	DELL	GPIO table update.	Remove ACAV_DOCK_SRC# connection from 5035 pin41 and name pin41 as DOCK_POR_RST# and connect to docking connecter pin140.Add R5727,C5316,R5391,R5729(DUMMY).	X01
65	37	2007/12/28	DELL	Change DOCK_DET# PH to +3.3V_ALW to prevent RTC leakage when docked.Dummy original PH resistor and add a new 100K PH to +3.3V_ALW.	Add R390 pull-high to +3.3V_ALW. Dummy R277.	X01
66	26	2007/12/28	DELL	Follow Ricoh's suggestion to modify schematic. (1) Apply pull-down resistor to SPKROUT pin. (2) Add capacitors for CCD[2:1]# (3) Add capacitor for FIL0, 0.01uF	(1)Add dummy R3380(100K) to GND. (2)Add C9387 and C9409(270pF) to GND (3)Pin A14 add C9279(0.01uF) to GND	X01
67	35	2007/12/28	DELL	LCD/LED will keep had power with USB device when unplug AC & Battery	Delete RN48,RN52. Add R371,R44. USB_SIDE_EN# pull high R281(100K) to +3.3V_ALW_2 USB_POWERSHARE_PWR_EN# pull high R387(100K) to +3.3V_ALW_2	X01
68	42	2008/03/03	Wistron	ACAV_IN signal issue.	Change PC100706 to 0.1uF. Change PR100712 pull high to +3.3V_ALW.	X02
69	11,37	2008/03/03	Dell	Display port issue.	Exchange R5728 and C22 location. Exchange R5731 and C24 location. Exchange R5733 and C14 location. Exchange R7534 and C1 location. Change RN4,RN15 from 4.7K to 2.2K. Change RN143 Pull high to +3.3V_RUN	X02
70	8	2008/03/04	DELL	H_THERMDA/H_THERMDC corsstalk +PWR_SRC concern.	Pop C79.	X02
71	41	2008/03/04	Wistron	For better RUN power plane stability.	Add C716,C723,C725,C726	X02
72	32	2008/03/04	IDT	Audio PC Beep Issue.	Change R381,R385 to 499K. Dummy R375.	X02
73	33	2008/03/07	Wistron	Speaker left and right channal issue.	Change speaker pin define.	X02
74	19	2008/03/10	Wistron	Improve LVDS SMBUS. Prevent burn KBC.	Add R633,R620(100 ohm) to LCD_SMBUS.	X02
75	31	2008/03/12	Dell	De pop USB switch and add two 0 ohm resistors for USBP0+/USBP0-	Add R274,R275. DUMMY U20.	X02

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76	32,33	2008/03/12	DELL	TP leakage issue	Dummy RN73 and add PH RN74(100K) to +5V_ALW.	X02
77	34	2008/03/14	Wistron	Reduce RCID noise.	Remove R259.	X02
78	14	2008/03/14	Wistron	Current rating issue.	Change L14,L19 current rating from 60mA to 120mA bead.	X02
79	35	2008/03/14	Wistron	Change Board ID.	Depop R296,R311. Pop R297,R310.	X02
80	18	2008/03/17	Wistron	SW 2nd source pin 54 is seclect pin.	Short U25 pin 17 and pin 54.	X02
81	32	2008/03/19	Dell	PC beep schematic modify.	Exchange R381,C438 location. Exchange R385,C442 location. U42 pin 12 connect to AUD_AGND. Delete R389,C443. C392 change from 1uF to 10uF. C29 and C40 change from 1uF to 4.7uF. Add C9410,C9411,C9412,C9413(1000pF) to AUD_AGND. Add R8149(0 ohm) Add R8147,R8148(10M) to AUD_AGND. Change C415,C416 to 0.22uF. Change C391 to 0.1nF.	X02
82	37	2008/03/19	Wistron	Display port issue.	Change parts U1,U2,U4,U5. Delete R5728,R5731,R5733,R5734. Add C449,C447 Dummy RN137,RN143	X02
83	34	2008/03/20	DELL	Prevent leakage from docking.	Add D47 and R394.	X02
84	7,28	2008/03/20	TXC	Follow crystal test report to modify schematics	Change C176 to 15pf. Change C187 to 18pF.	X02
85	43	2008/03/20	Wistron	Hung up issue.	Change net name +CPU_PWR_SRC_PHASE1 to +CPU_PWR_SRC Add C9414,C9415(Dummy) 10uF/25V 1206	X02
86	35	2008/03/24	DELL	Change net name from WIRELESS_ON/OFF# to WIRELESS_ON#/OFF due to M09 EC code change.	Change net name from WIRELESS_ON/OFF# to WIRELESS_ON#/OFF.SW1_Pin1 change to GND, Pin3 change to NC.	X02
87	32	2008/03/24	ADI	For Docking Audio.	Connect U42 Pin 13 and 14 to AGND. Change C392 to4.7uF. Change the L29 to BLM18EG601SN1. Connect U42 Pin29 thermal pad to AGND. Change C415 and C416 to 0.22uF, 25V, and in X5R or X7R material. Change C417 and C418 to 1uF, 25V and in X5R or X7R material. Change C464 to 0.1uF and populate C465 with 1uF.	X02

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88	28	2008/03/24	DELL	LOM schematics modify to prevent wrong behavior when using China TPM or Broadbom TPM.	Change C653 to 1uF 0603. Change R555 to 0 ohm.Populate R537 when C_TPM. Add R8150 to LRESET#, Populate RN282,RN283 10k pull-up to LCLK, LAD0~3, LFRAME#, LRESET# when C_TPM.	X02
89	30	2008/03/25	DELL	LED_WLAN_OUT# need PH 100K to +3.3V_WLAN	Add R418 puu-high to +3.3V_WLAN	X02
90	35	2008/03/25	DELL	Add one 10uF caps on 5028 VCC1 power pin	Reserve C55 to 5028 VCC1.	X02
91	20,30	2008/03/25	DELL	For WIMAX LED support post RTS	Pop R321 and R724 and pop R88,Q16,R89	X02
92	37	2008/03/25	DELL	For E-Docking ESD issue,please reserve 0.1uF on DPB_DOCK_HPD_R and DPC_DOCK_HPD_R	Reserve C455 to DPB_DOCK_HPD_R. Reserve C462 to DPC_DOCK_HPD_R.	X02
93	37	2008/03/25	DELL	Reserve ESD diode for Docking power	Reserve D1 to +DOCK_PWR_SRC	X02
94	35	2008/03/25	DELL	Change DOCK_AC_OFF circuit	Add R436(Dummy),D48,R2	X02
95	22.35	2008/03/25	DELL	Add one GPIO to control SPI ROM write_protect function	Add connection named "SPI_WP#_SEL" from 5028 pin 23 to SPI ROM pin 3 trrough a 0 ohm(R437) resistor	X02
96	48	2008/03/25	Wistron	Add Caps for EMI demand	Add EC4,EC17,EC36,EC37,EC38,EC39	X02
97	35	2008/03/26	Wistron	Leakage Issue.	Dummy R283.	X02
98	37	2008/03/26	DELL	Docking connecter pin 140 connect to DOCK_POR_RST# directly.	Delete R5727,R5729	X02
99	7	2008/03/26	DELL	CLK_PCI_DOCK is shared with CLK_PCI_PCCARD. Change CLK_PCI_PCCARD net from pin32 to pin33 of CLKGEN.	Chagne CLK_PCI_PCCARD to U27 pin33. Change R575 to 33 ohm. Change R571,R192,R188 to 22 ohm	X02
100	32	2008/03/26	DELL	Can remove R416 to make trace routing smoother. This pull-up is not needed in 92HD71B codec	Remove R416.	X02
101	6	2008/03/27	DELL	ITP - To expedite M09 debug,system should have the correct ITP termination and resister pop options.	Change R53 to 27 ohm,R61 to 39 ohm,R54 to 649 ohm,R50 to 150 ohm, R55 to 124 ohm.	X02
102	32	2008/03/27	Wistron	No need these test point and resistor.	Remove R354 and NC U42 pin21,22	X02
103	33	2008/03/27	DELL	THD+N performance on codec Port A is too marginal	Change C519 and C520 to 2.2 uF.	X02
104	20	2008/03/28	DELL	Moudule internal pull high issue.	Add R259 pull high to +3.3V_RUN.	X02
105	19,20	2008/03/28	Wistron	Lesson learn from DB2. Can not drive 2 LEDs by the same resistor.	Add R8151,R8152.	X02

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106	26,27	2008/03/28	Wistron	For EMC request.	Pop C361,C362,C364,C365 Change R392 to EC49, R330 to 0ohm	X02
107	36	2008/03/28	Wistron	EMC4002 Pin20 is a Push-Pull output Pin. It's OK for no pull high.	Depop R400.	X02
108	11	2008/03/28	Wistron	Lost audio driver issue.	Change R158,R377 to 33 ohm	X02
109	39	2008/03/28	Wistron	EMI request.	Add R8153,C9416	X02
110	37	2008/03/28	Wistron	Dock pull high issue.	Delete RN137,RN143,RN144,RN138 Add R329,R354,R416,R438,R439,R440,R441,R442	X02
111	33	2008/03/31	IDT	Audio modification.	Change C520,C519 to 10uF. Change R6698,R6504 to 2.2K.	X02
112	34	2008/04/02	Epson	Crystal cap change.	Change C722 from 33p to 27p.	X02
113	7	2008/05/14	Wistron	IPT no used.	Dummy RN8.	A00
114	20	2008/05/14	Wistron	Breath LED schematics modify.	Reserve Q44	A00
115	20,30	2008/05/14	Wistron	15 with no WWAN LED.	DY R259,R88,Q16,R89,R89,R724	A00
116	40	2008/05/14	DELL	Modify power on logic section.	1. Remove 5V,3.3V,3.3V_LAN_PWRGOOD plane. 2. U65.8 NC, U65.9 connect to GND	A00
117	34	2008/05/16	Wistron	Remove BIOS ROM from KBC.	Remove U75,R671,R625,R626,R655,R656,C753,R657.	A00
118	32	2008/05/20	ADI	Audio modification by ADI's suggestion.	Add R8149 instead of 0 ohm.	A00
119	45,46,47	2008/05/16	Wistron	Modify OCP R trip request by Wistron power team	Change PR644 to 280kohm, PR680 to 120kohm, PR462 to 8.66kohm, PR649 to 4.32kohm	A00
120	11,40	2008/05/22	DELL	Minicard NG issue.	1. Add +3.3V_LEVELSHIFT power plane. 2. Change U90 pin16 to +3.3V_LEVELSHIFT. 3. Modify U90 pin8 to +3.3V_LEVELSHIFT power plane.	A00
121	46,40	2008/05/22	DELL	Modify capacitor for power sequence.	Change PC779 to 1kpF, C654 to 0.1uF.	A00
122	23,34	2008/06/03	DELL	Modify KBC GPIO.	Add R461. Reserve R460,R462.	A00
123	20	2008/06/03	DELL	LED brightness issue.	Modify R92,R99,R8151,R8152,R90,R89 to 1K ohm.	A00
124	37	2008/06/04	Wistron	EMI test pass while short the common choke pad.	Delete L46,L49,L50,L53,L54,L55,L56,L57.	A00
125	29	2008/06/04	Wistron	Change TCM BOM control description.	Modify R1849,R156 BOM description.	A00

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Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
1	38	2007/11/20	DELL	sequence issue	Change R10831 for NB_AC_OFF	X01
2	39	2007/11/20	DELL	leakage issue	ADD Q10072 R10050 D10053	X01
3	42	2007/11/20	DELL	thermal issue	change L28 R348	X01
4	42	2007/11/20	DELL	sequence issue	ADD Q72 R10832, R10832 pin2 connect R394 PIN 2 , R75 PIN1 +SDC_IN change to +DC_IN_SS	X01
5	39	2007/12/04	DELL	sequence issue	ADD Q100073 D connect SW_GND	X01
6	39	2007/12/04	DELL	leakage issue	ADD Q100073 G connect ACAV_DOCK_SRC#	X01
7	42	2007/12/04	DELL	A global signal name change for all notebooks	ACAV_IN_NB change ACAV_IN	X01
8	42	2007/12/04	DELL	A global signal name change for all notebooks	CHAGER_SRC change ACAV_IN	X01
9	42	2007/12/04	DELL	DOCK issue	add Q10073,R100811,R100812,R100811,SW_GND	X01
10	42	2007/12/04	DELL	DOCK issue	add R100713, R100712,C100706,R100714, C100707,R100711,R100710,R100504,R100505 ACAV_IN_NB	X01
11	42	2007/12/04	DELL	Change function	add R100506 pin2 and R100813 pin2 ISL88731_ICM	X01
12	42	2007/12/04	DELL	Change function	MAX8731A_IINP change ISL88731_ICM	X01
13	42	2007/12/04	DELL	Change function	Dummy R430,C489,C490,R377,R371,R373,C425,C426, C448,C447,R429,R382,Q46,R390,R26	X01
14	38,39,42 43,44,45 46,47	2007/12/17	Wistron	To identify power parts and EE parts	Add power team component "P"	X01
15	39	2007/12/28	DELL	DOCK issue	Add PQ95(84.00358.A31) , PQ547, PR550, PQ94, PQ99 , PR537,PQ538, EN_DOCK_PWR_BAR#	X01
16	42	2008/03/19	DELL	convenient test	Add PG90,PG91,PG92,PG93	X02

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Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
17	42	2008/03/19	DELL	DOCK ACIN and main board ACIN , but main board adapter no power , test remove DOCK ACIN have leakage.	Add Diode (PD12) , NET(leakage A)	X02
18	42	2008/03/19	DELL	Can't check ACAV_IN_NB	Change NET(+3.3_ALW) , Cap (PC100706)	X02
19	39	2008/03/19	DELL	remove DOCK ACIN have leakage current(roush)	ADD PR8140 ,PC9410	X02
20	39	2008/03/19	DELL	Leakage current issue	ADD PR81411	X02
21	39	2008/03/25	DELL	Pull and insert adapter	ADD PD30	X02

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