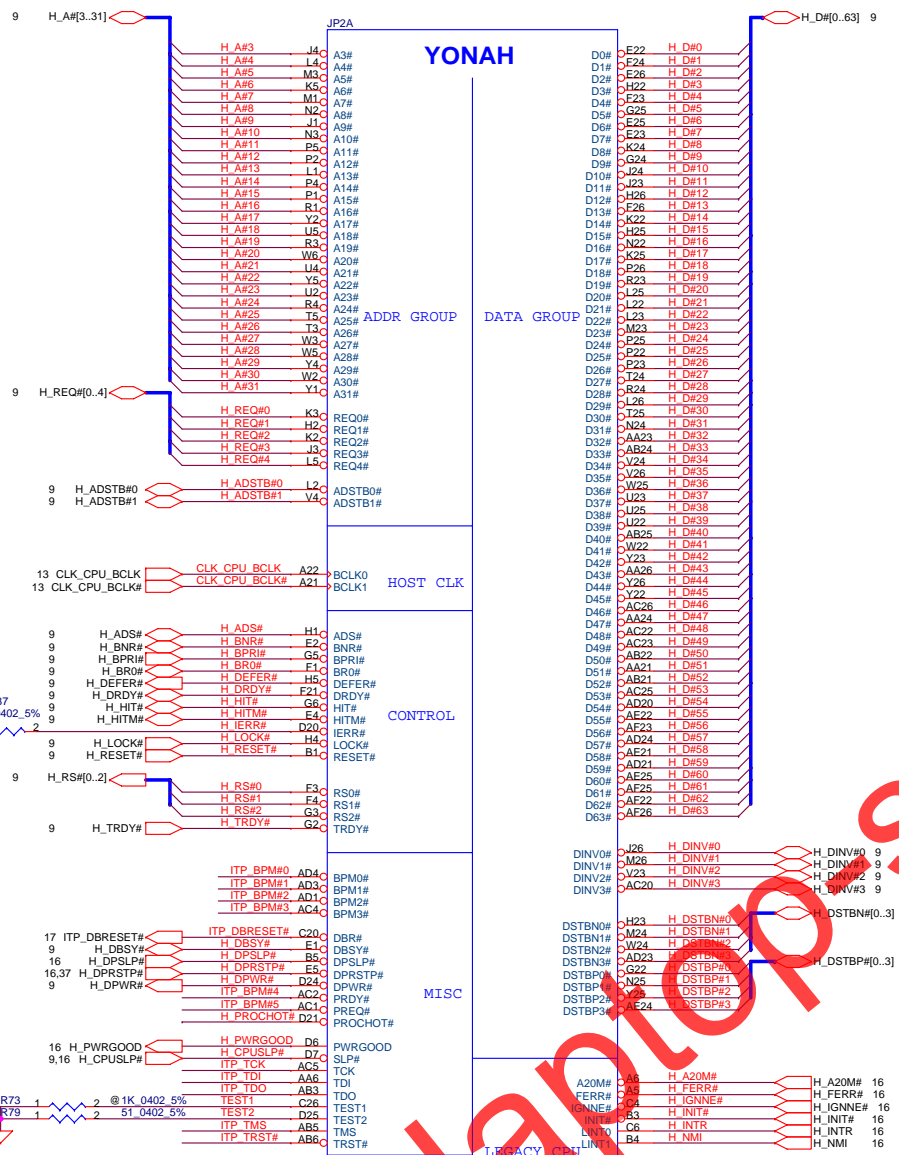
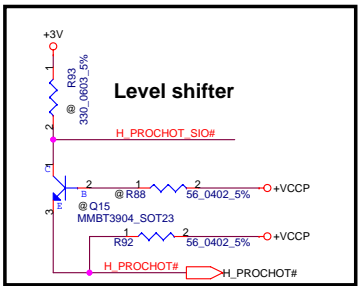
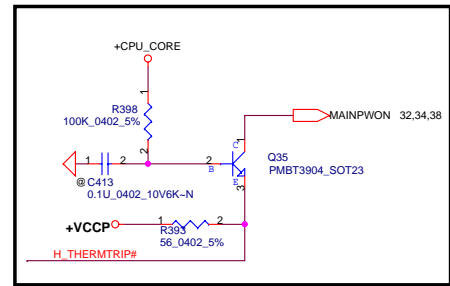
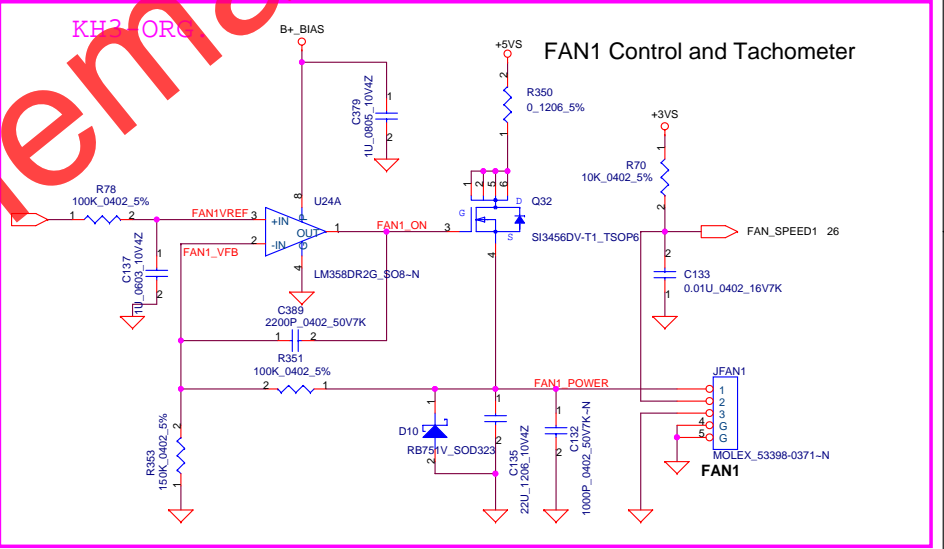
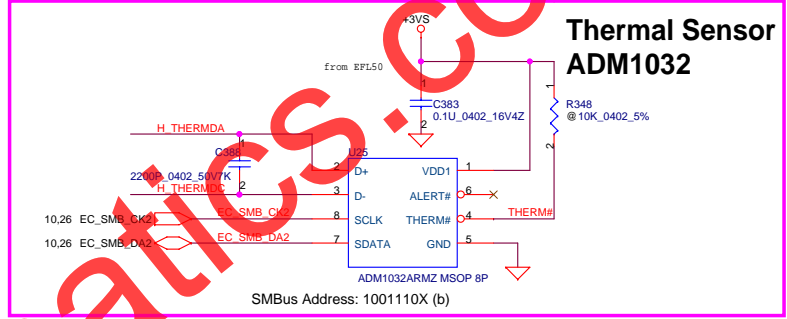
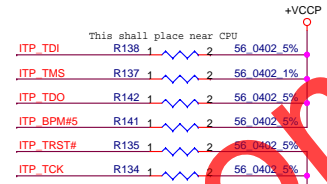
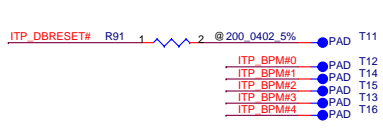
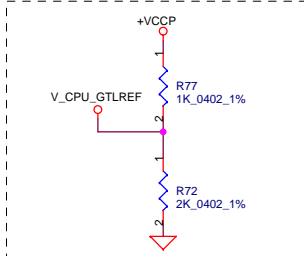


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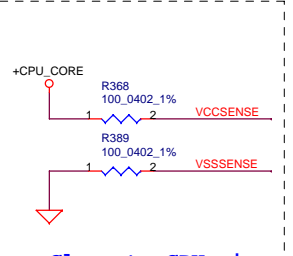


H\_THERMDA, H\_THERMDC routing together.  
Trace width / Spacing = 10 / 10 mil





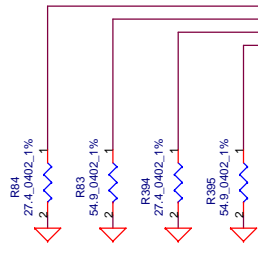
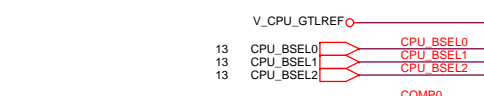
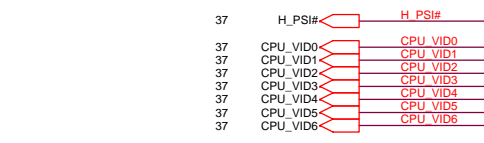
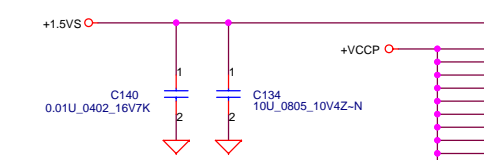
Close to CPU pin AD26 within 0.5 inch



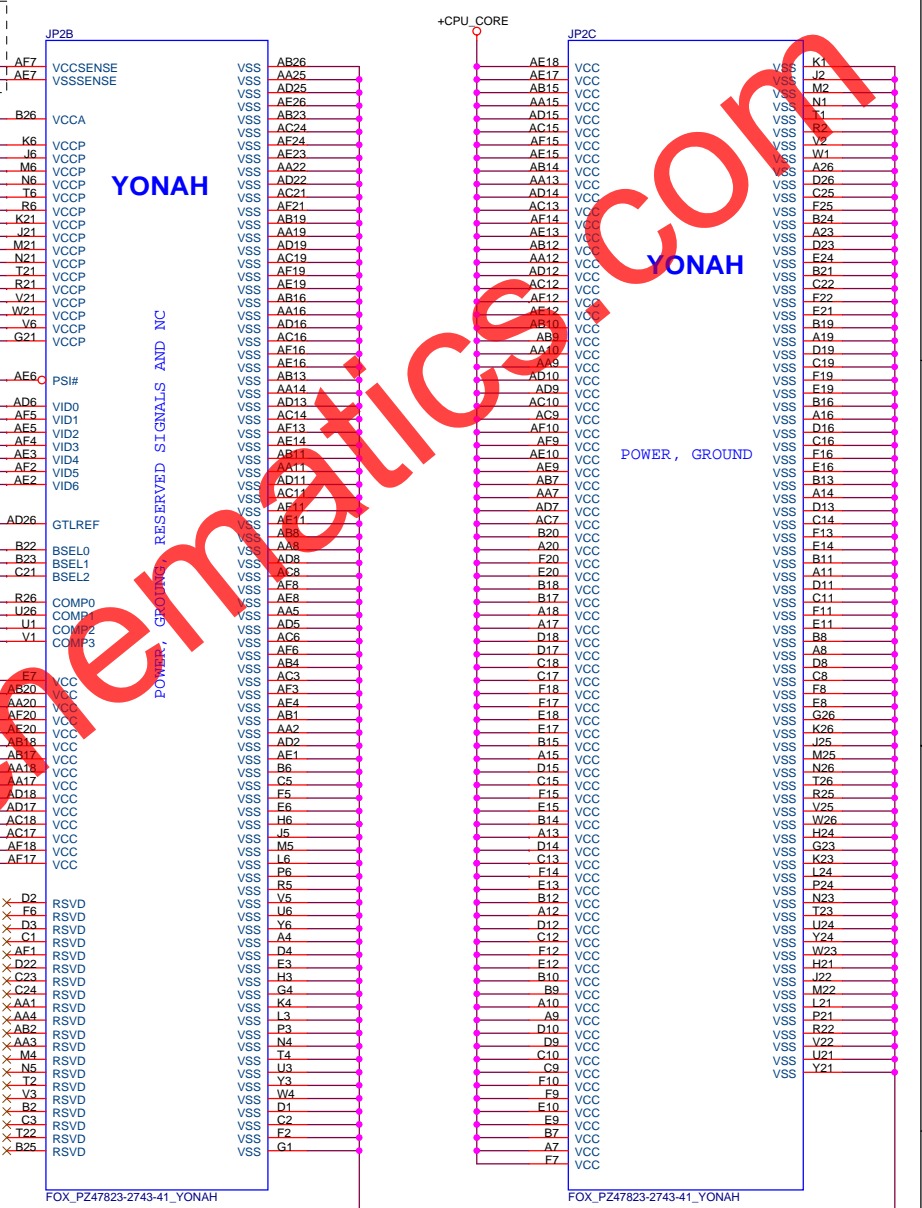
Close to CPU pin within 500mils.

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1

Length match within 25 mils  
The trace width 18 mils space  
7 mils



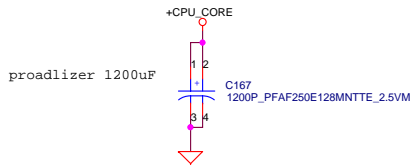
Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal.



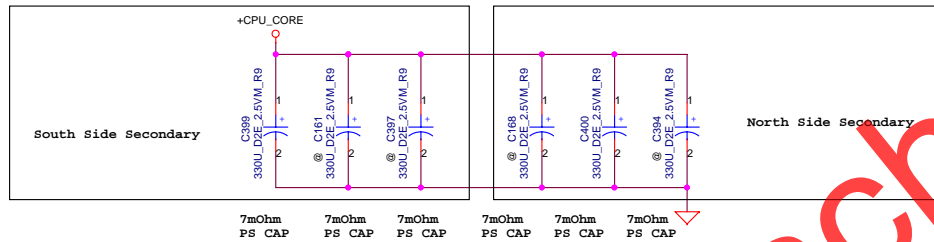
FOX\_PZ47823-2743-41\_YONAH

FOX\_PZ47823-2743-41\_YONAH

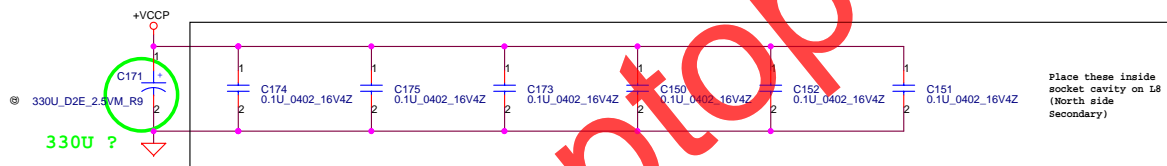
www.laptop-schematics.com



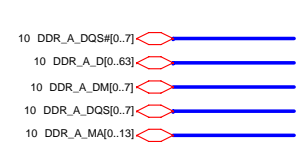
Mid Frequency Decoupling



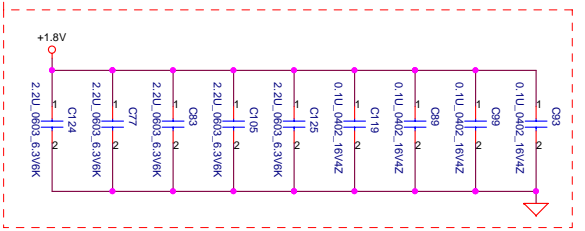
ESR <= 1.5m ohm  
Capacitor > 1980uF



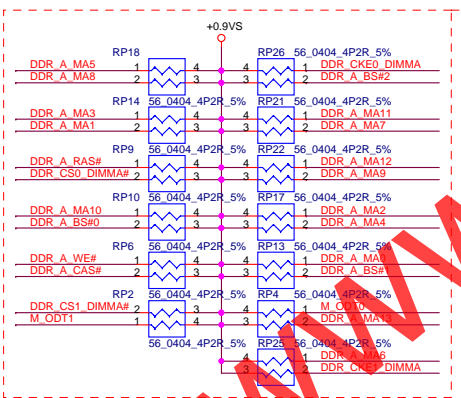
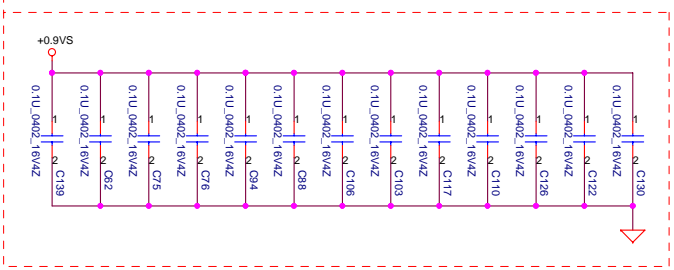
www.laptop-schematics.com



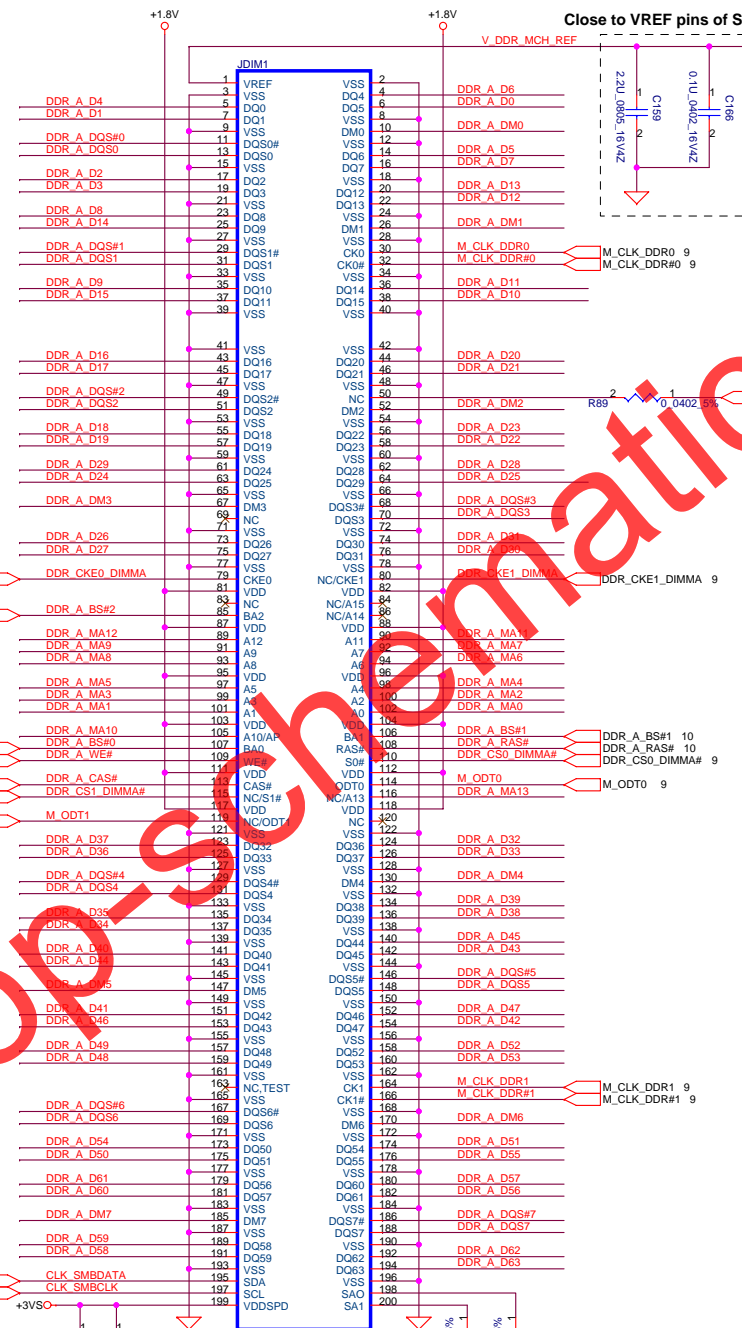
Layout Note:  
Place near JP41



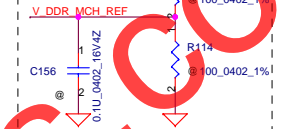
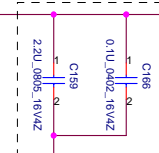
Layout Note:  
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:  
Place these resistor closely JP41, all trace length Max=1.5"



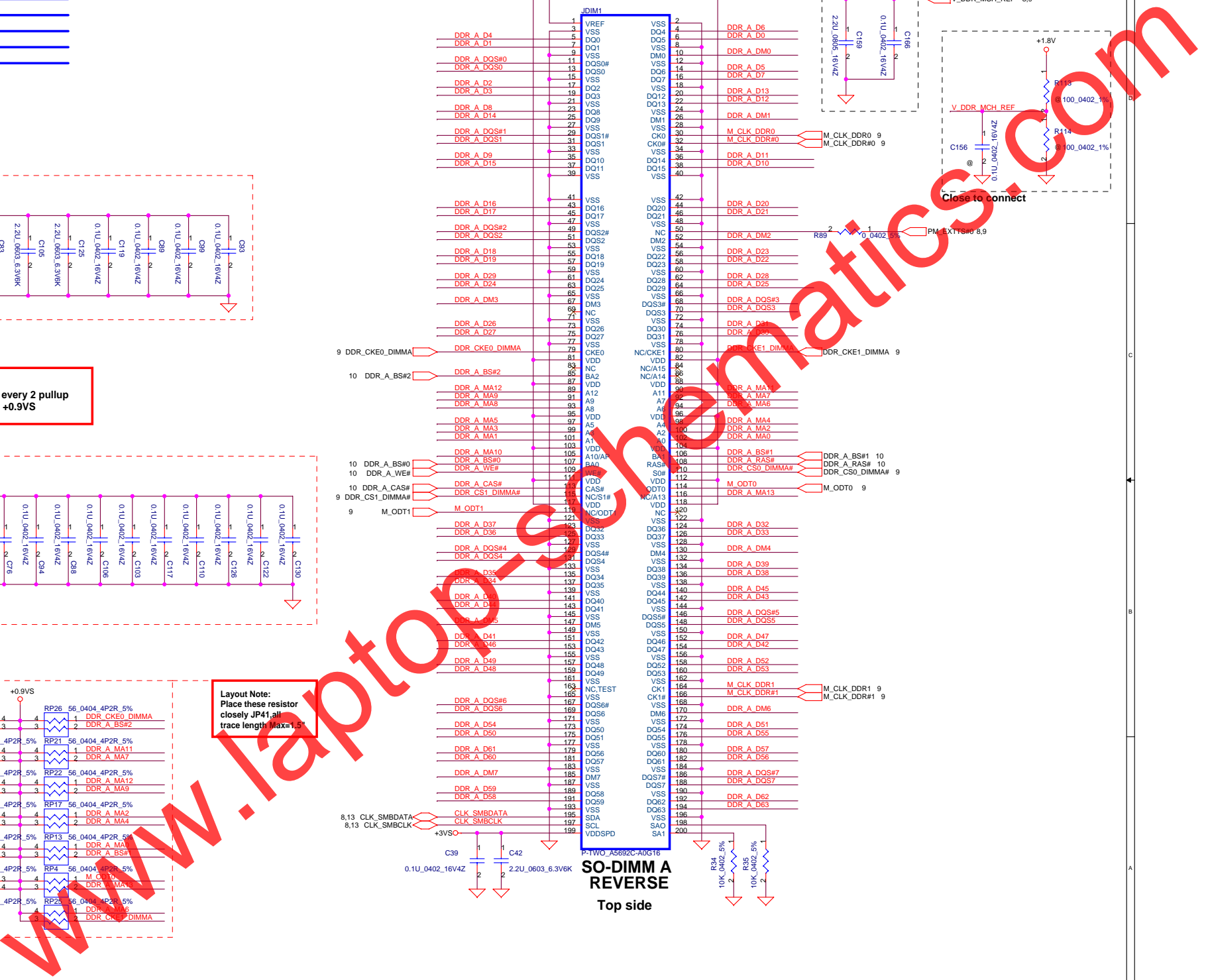
Close to VREF pins of SO-DIMM

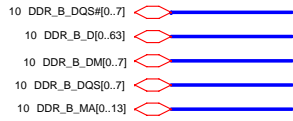


Close to connect

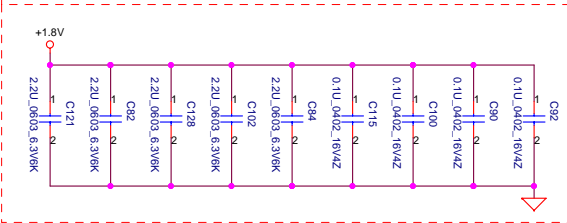


SO-DIMM A  
REVERSE  
Top side

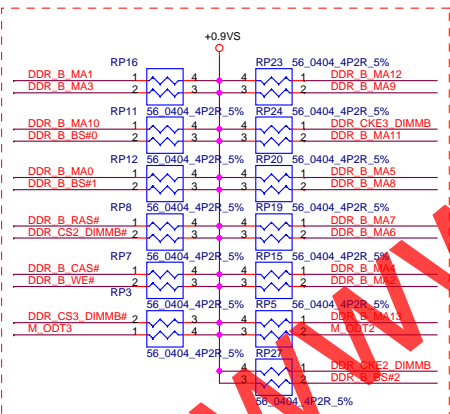
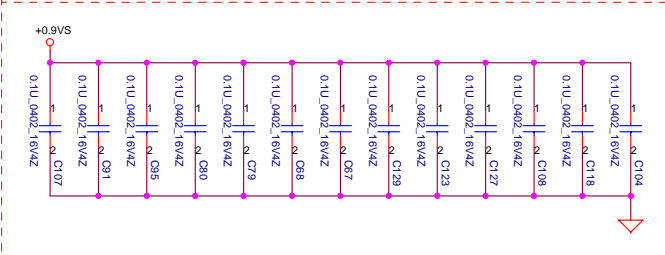




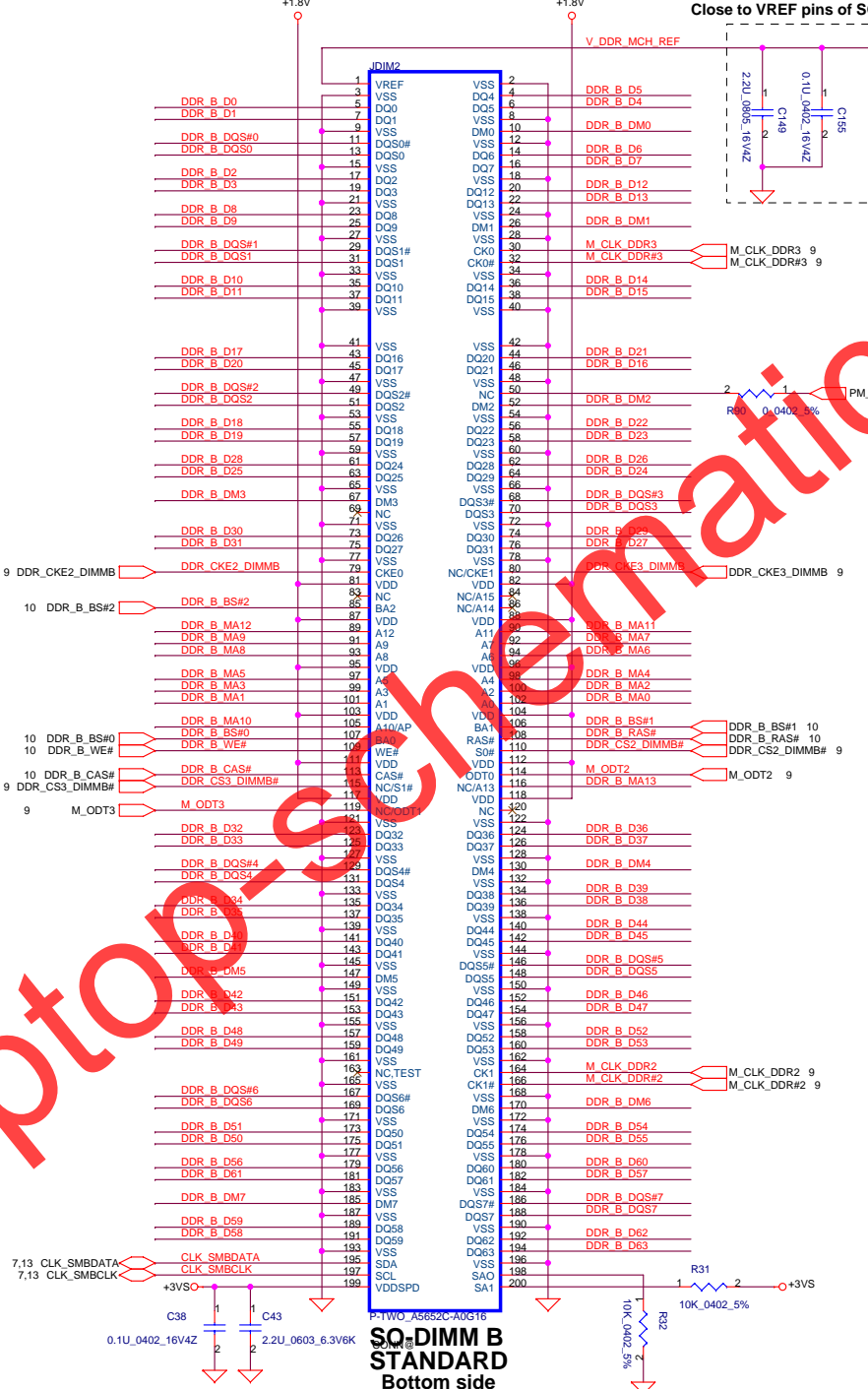
**Layout Note:**  
Place near JP42



**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9VS



**Layout Note:**  
Place these resistor closely JP42, all trace length Max=1.5"

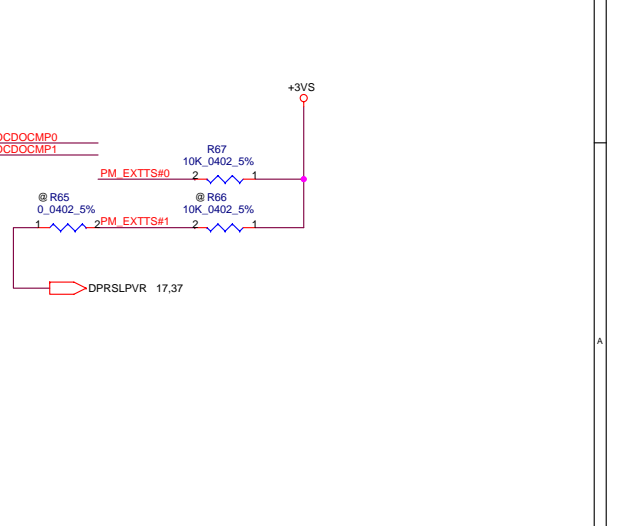
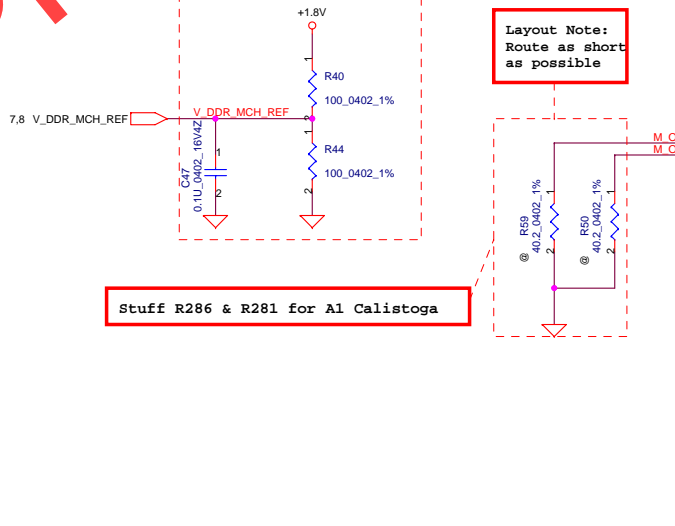
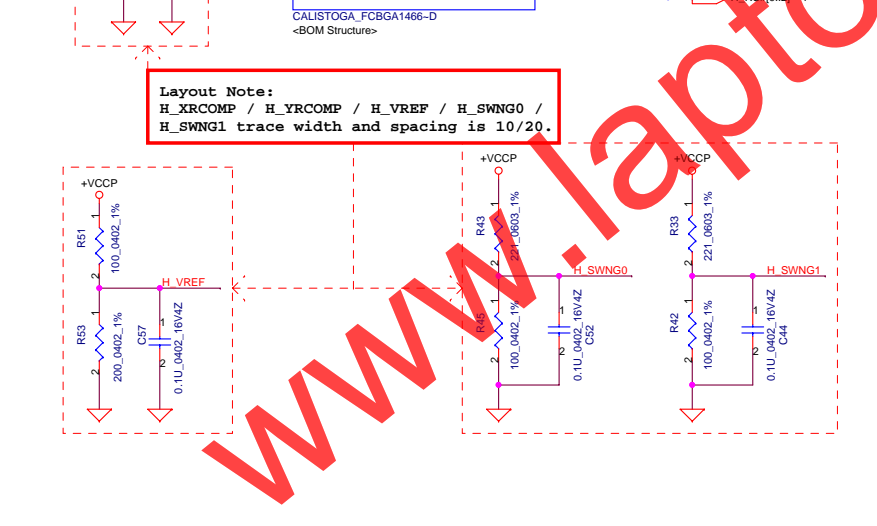
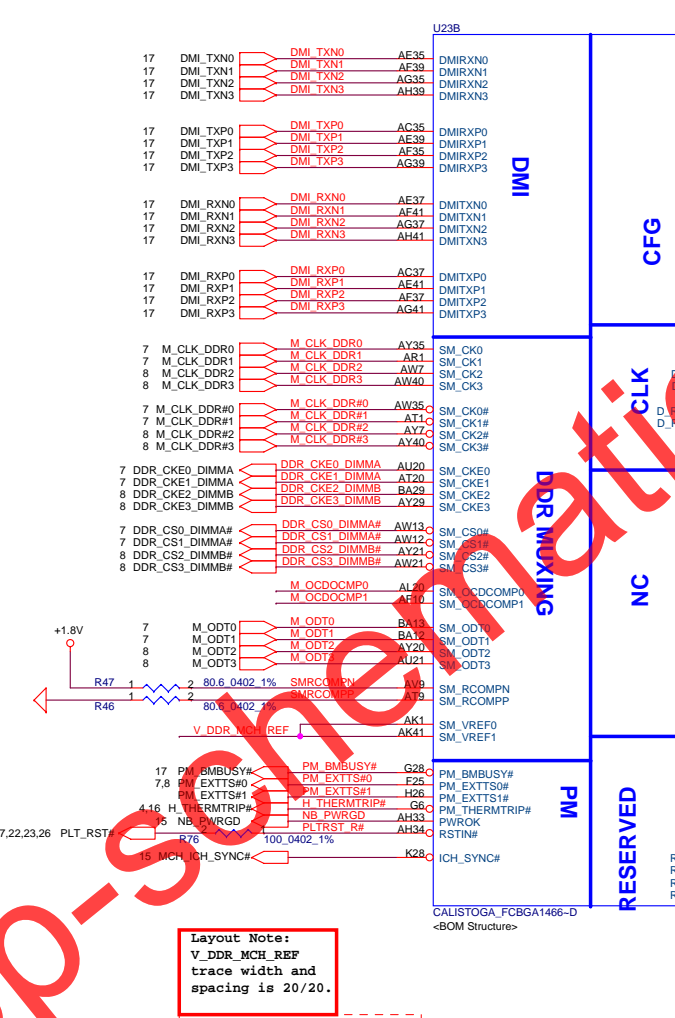
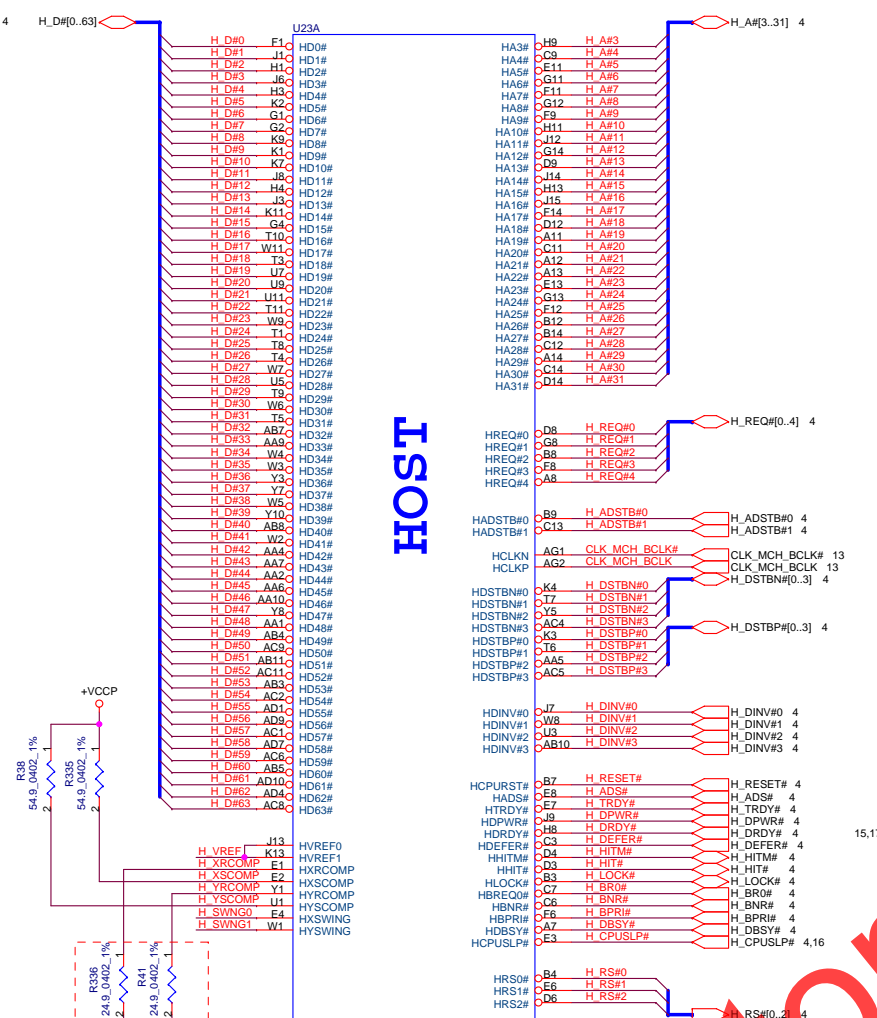


Close to VREF pins of SO-DIMM

**SO-DIMM B  
STANDARD  
Bottom side**

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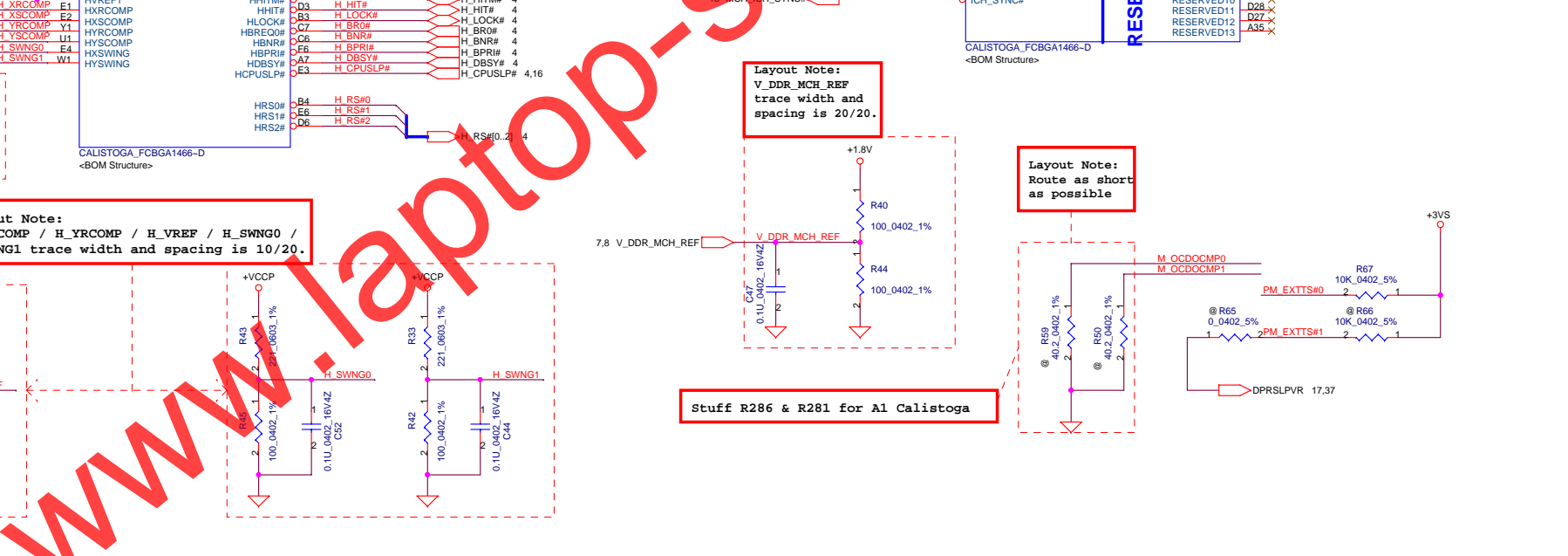


**Layout Note:**  
H\_XRCOMP / H\_YRCOMP / H\_VREF / H\_SWNG0 / H\_SWNG1 trace width and spacing is 10/20.

**Layout Note:**  
V\_DDR\_MCH\_REF trace width and spacing is 20/20.

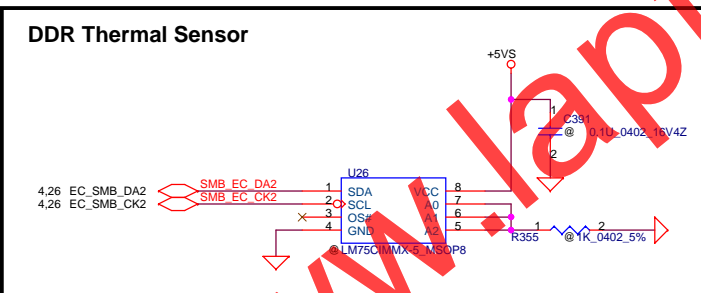
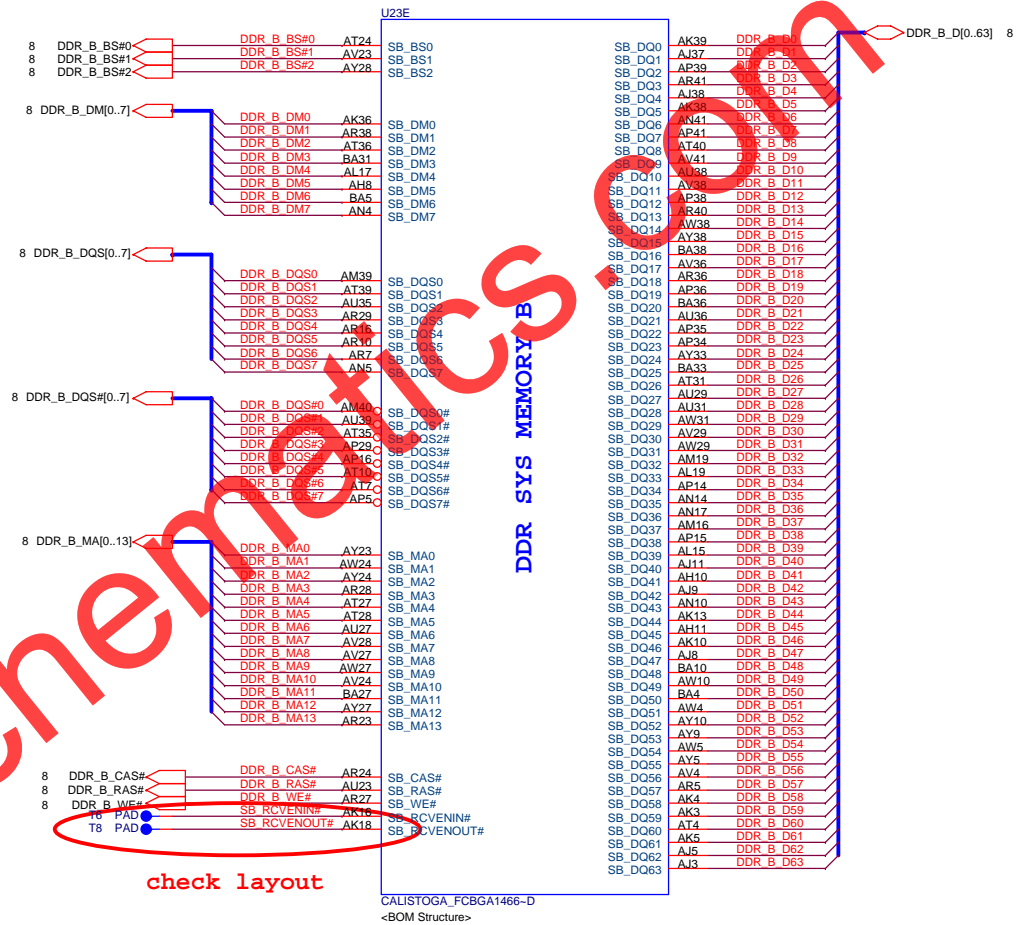
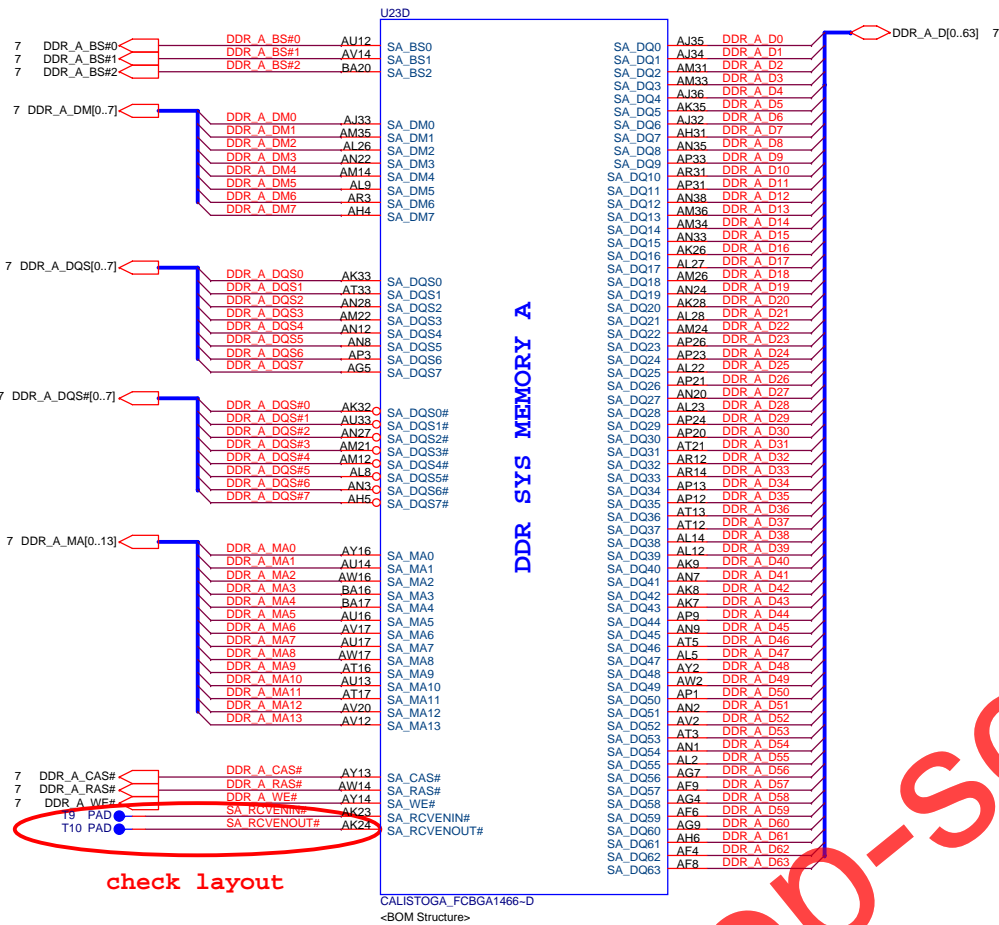
**Layout Note:**  
Route as short as possible

Stuff R286 & R281 for A1 Calistoga

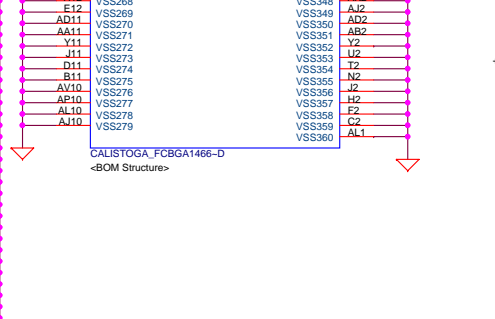
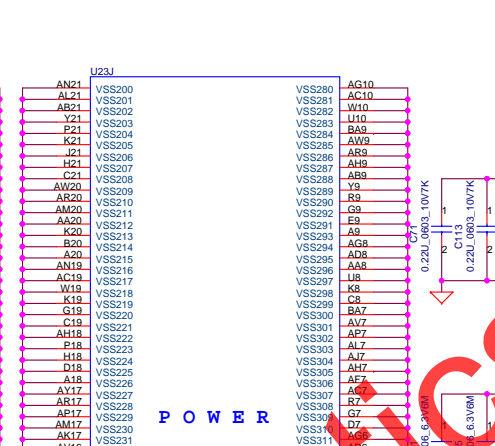
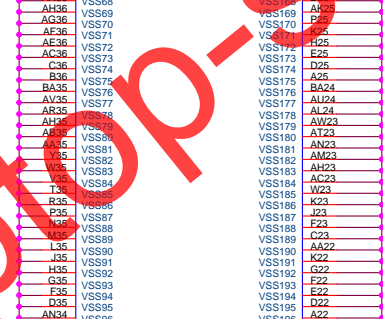
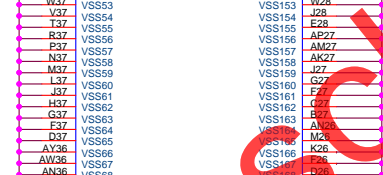
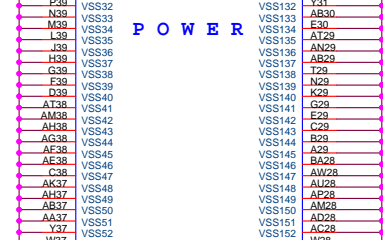
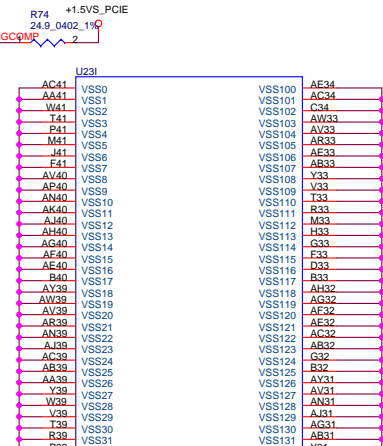
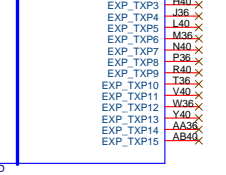
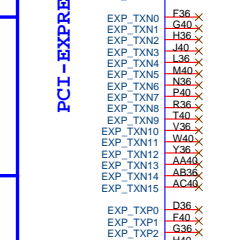
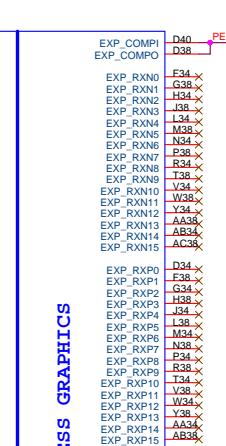
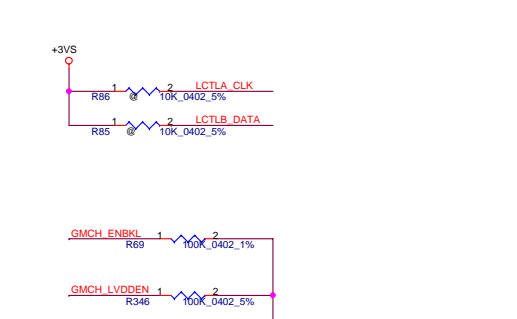
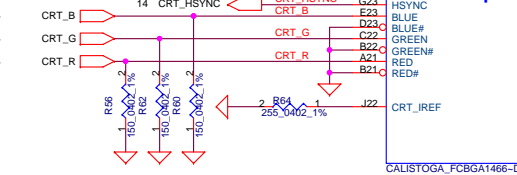
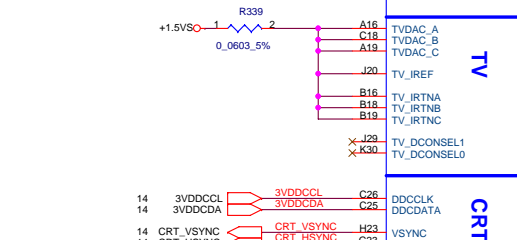
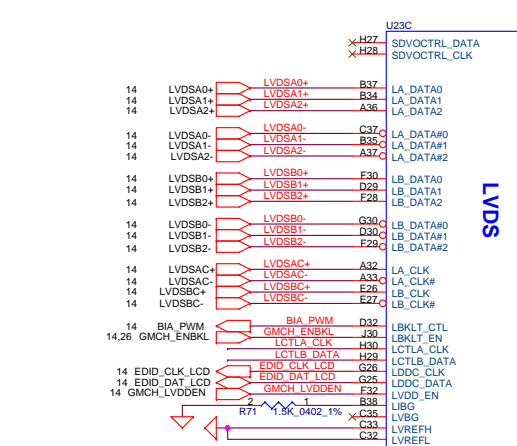
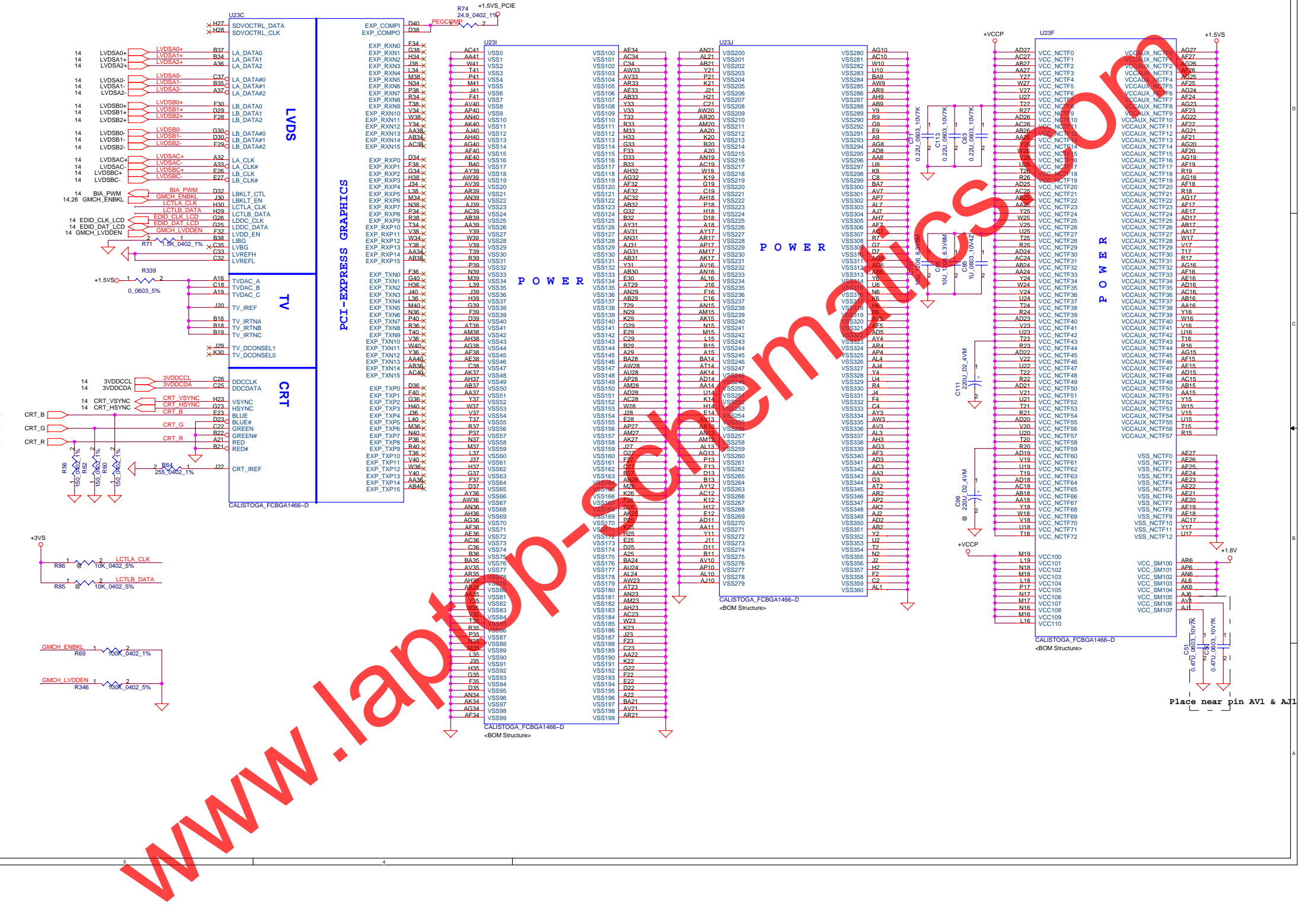


Description at pagel3.

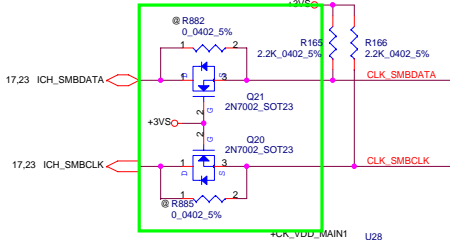
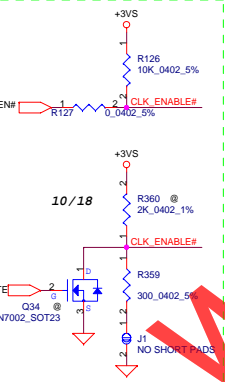
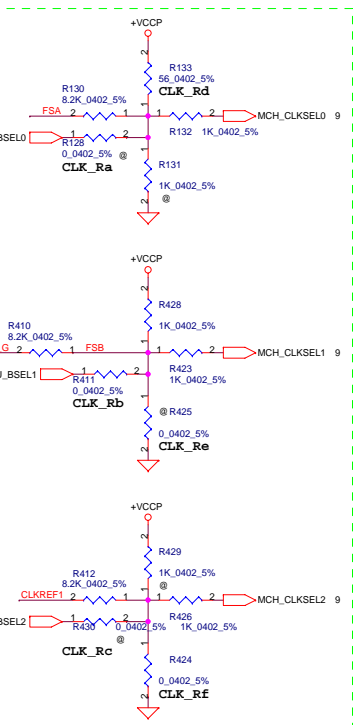
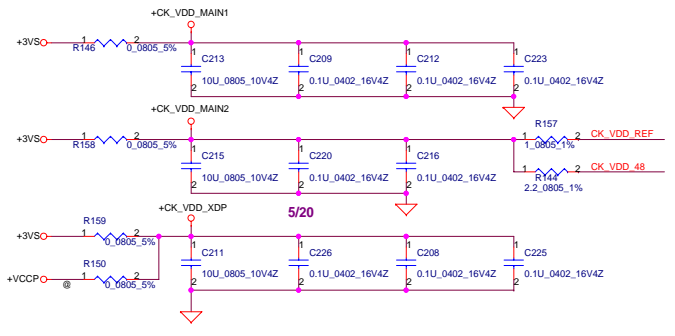
CALISTOGA\_FCBGA1466-D  
-<BOM Structures>



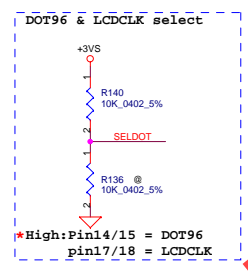




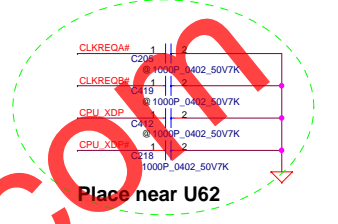
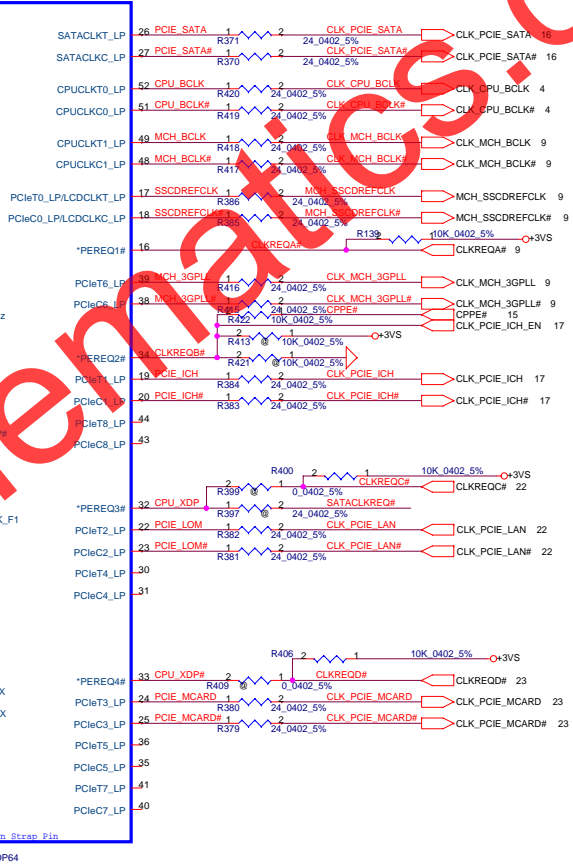
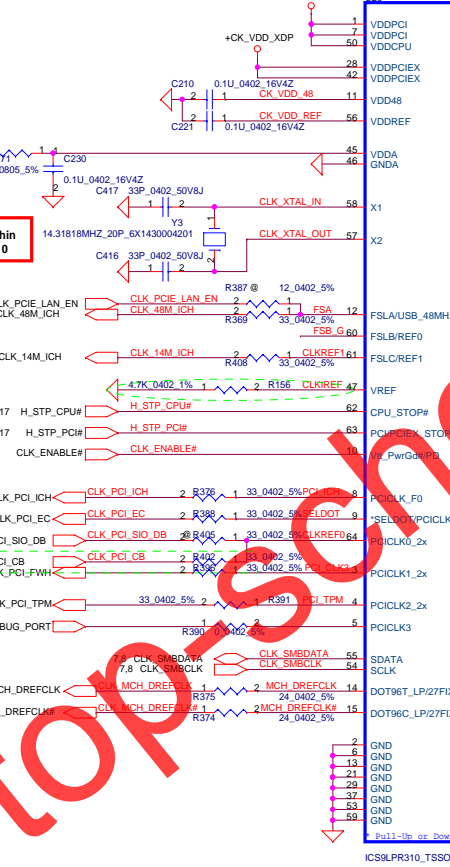




Place crystal within 500 mils of CK410

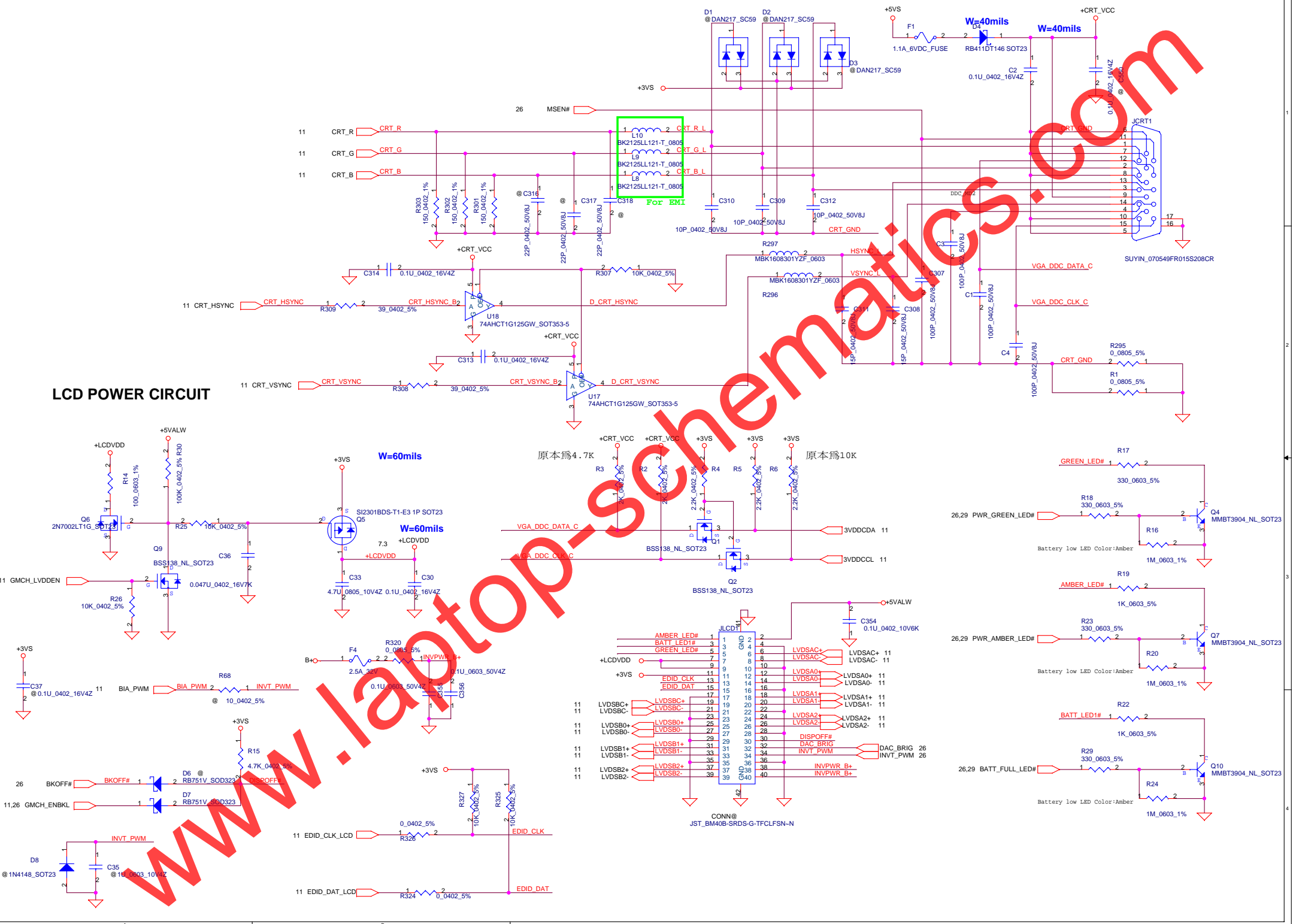


FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSELO	CPU MHZ	SRC MHZ	PCI MHZ
0	0	1	133	100	33.3
0	1	1	166	100	33.3



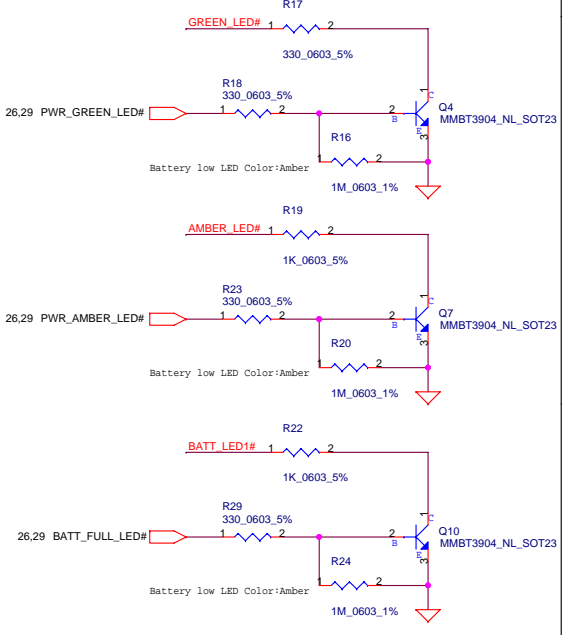
www.laptoprepair.com

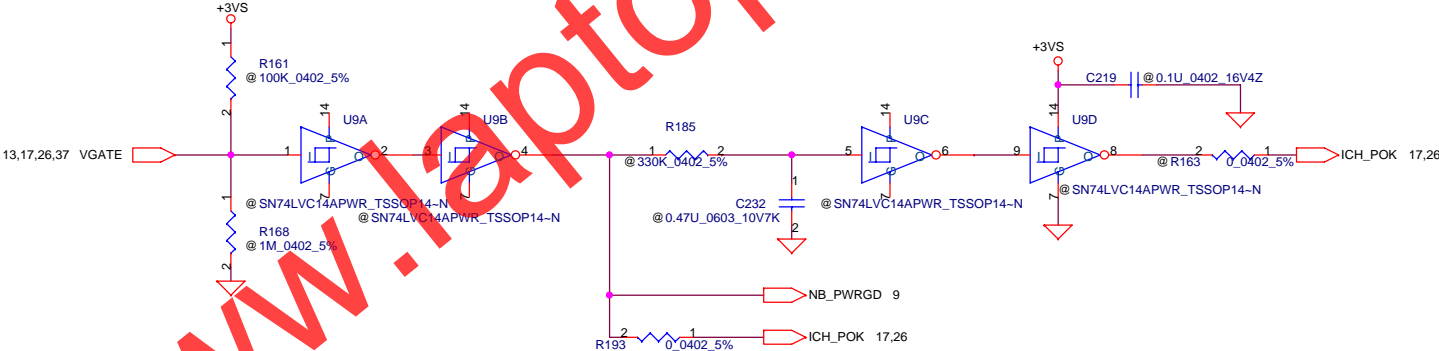
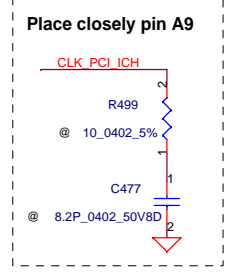
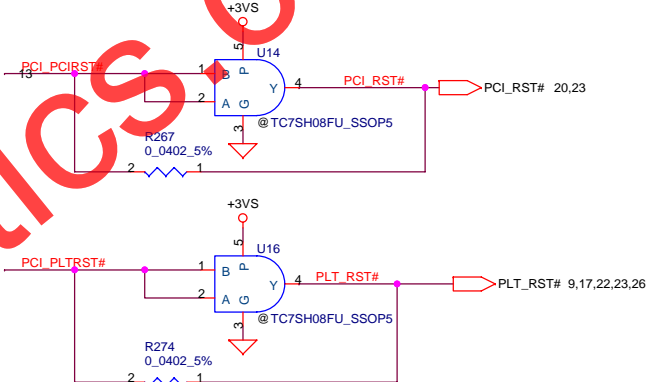
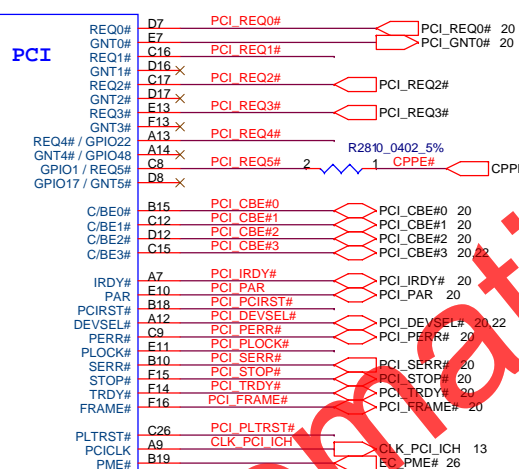
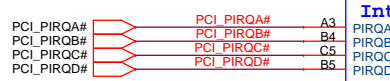
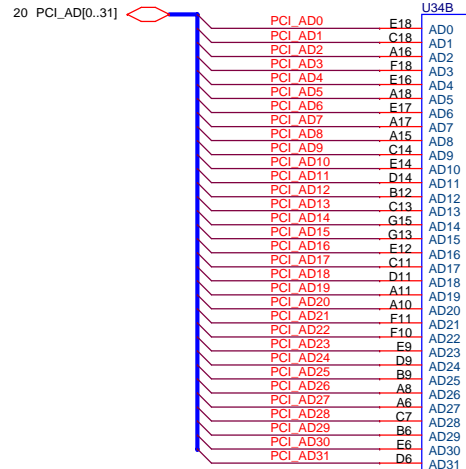
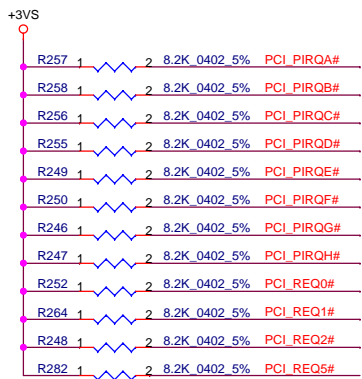
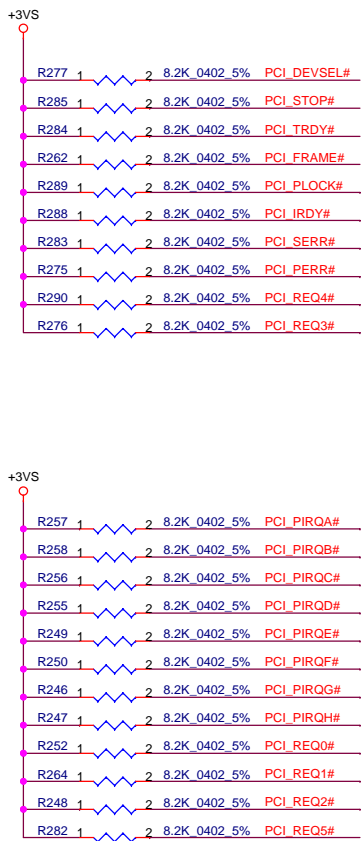
# LCD POWER CIRCUIT



原本為4.7K  
原本為10K

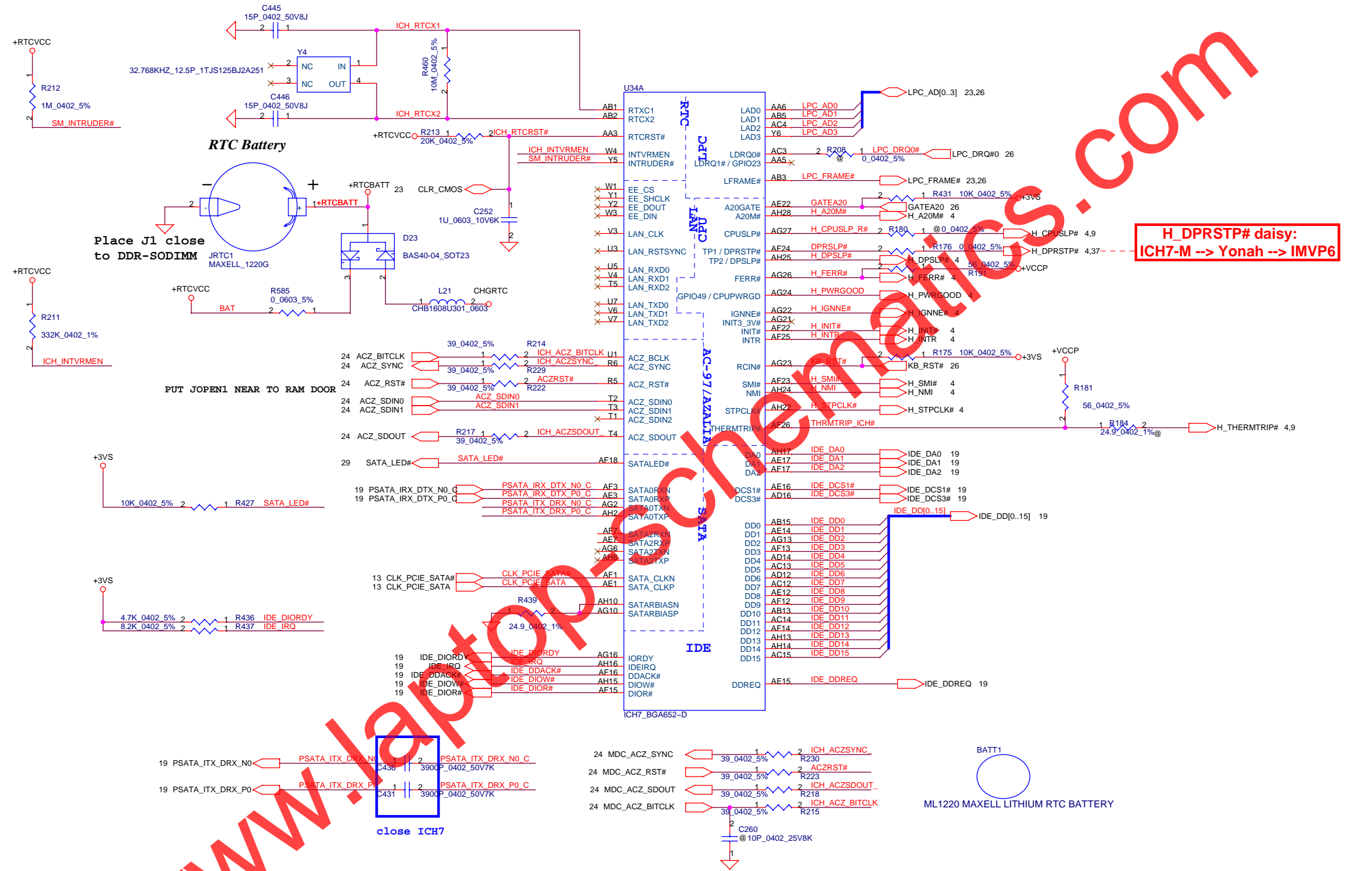
CONN@ JST\_BM40B-SRDS-G-TFCLFSN-N





www.laptop-schematics.com





www.laptopchips.com

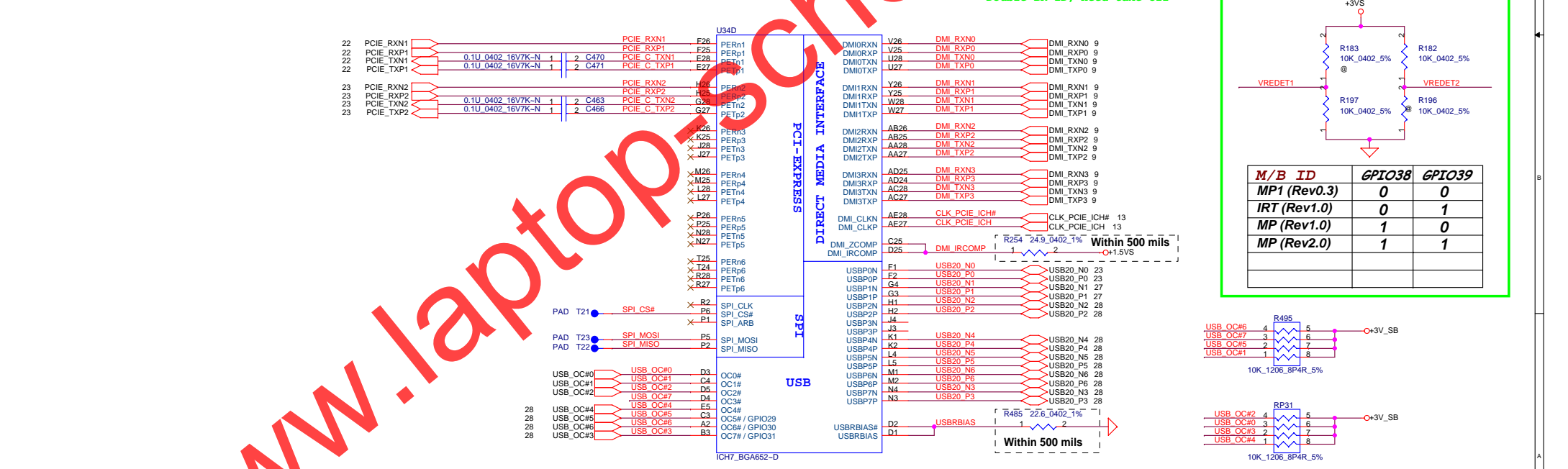
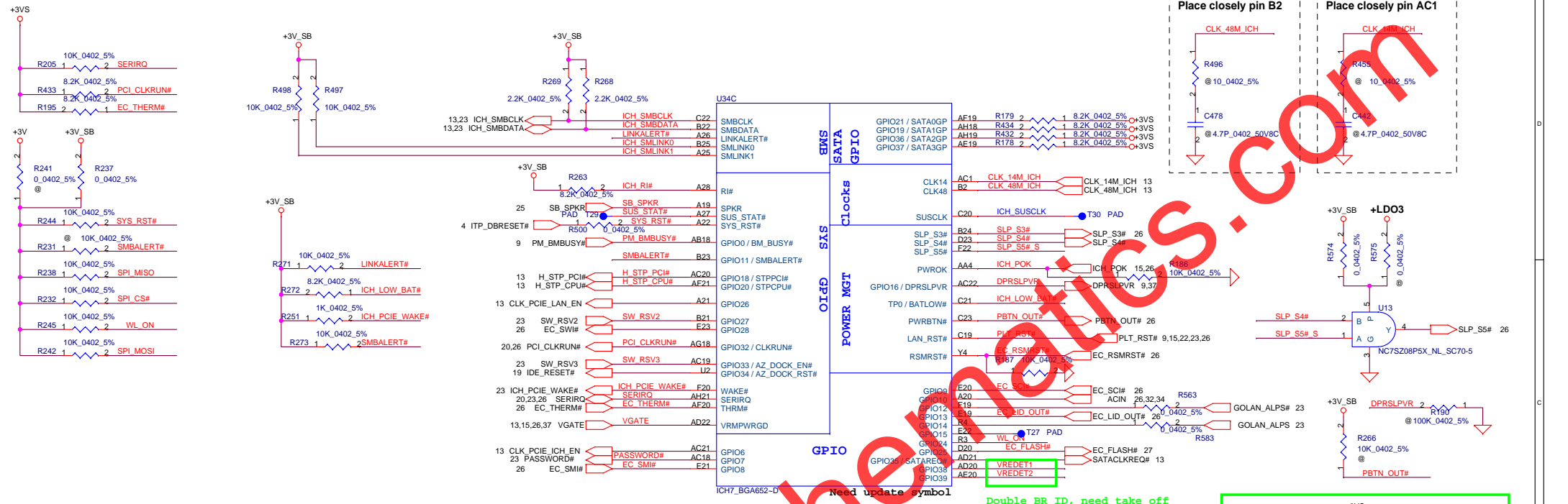
www.laptopchips.com

H\_DPRSTP# daisy:  
ICH7-M --> Yonah --> IMVP6

close ICH7

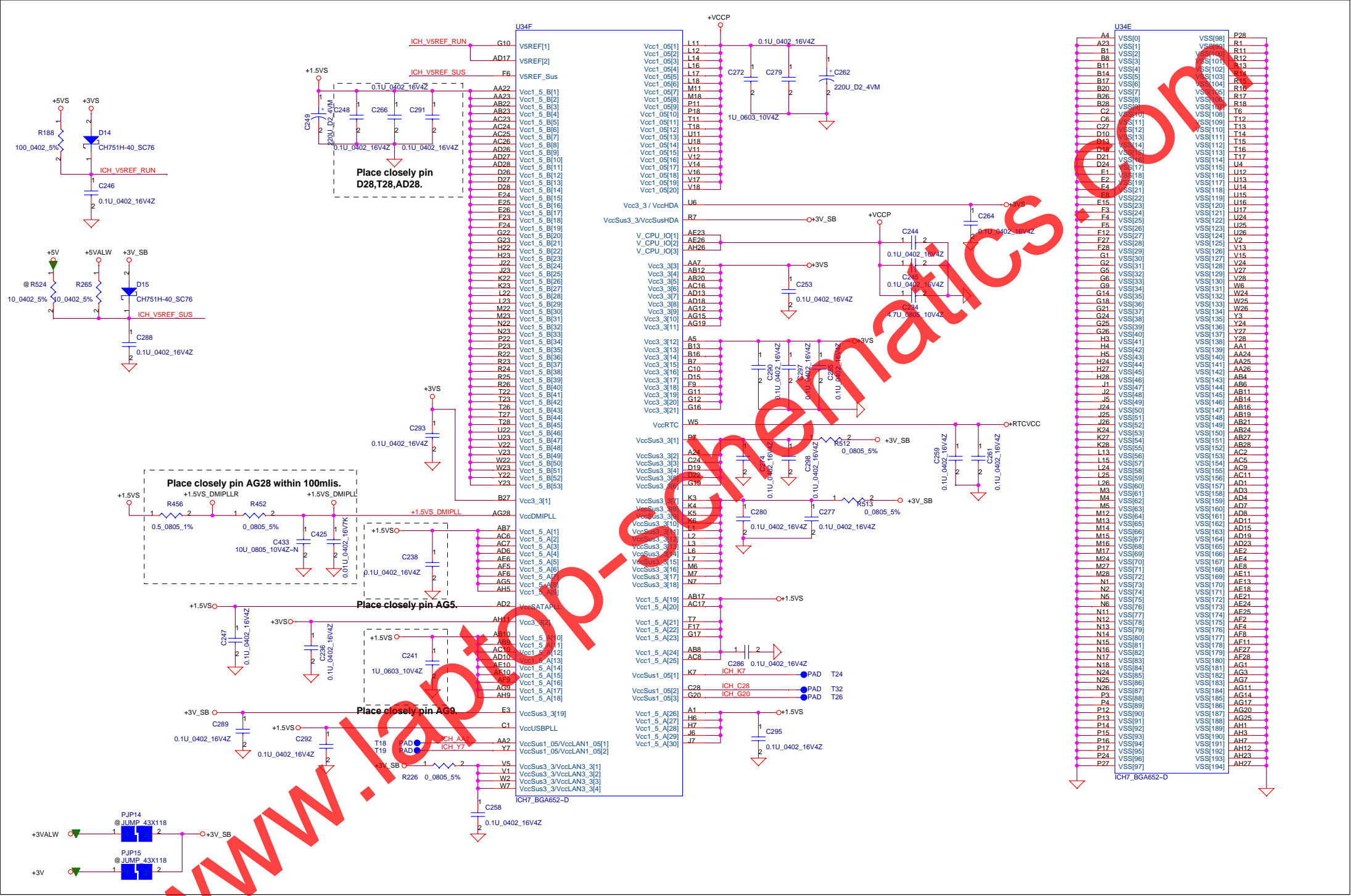
ML1220 MAXELL LITHIUM RTC BATTERY



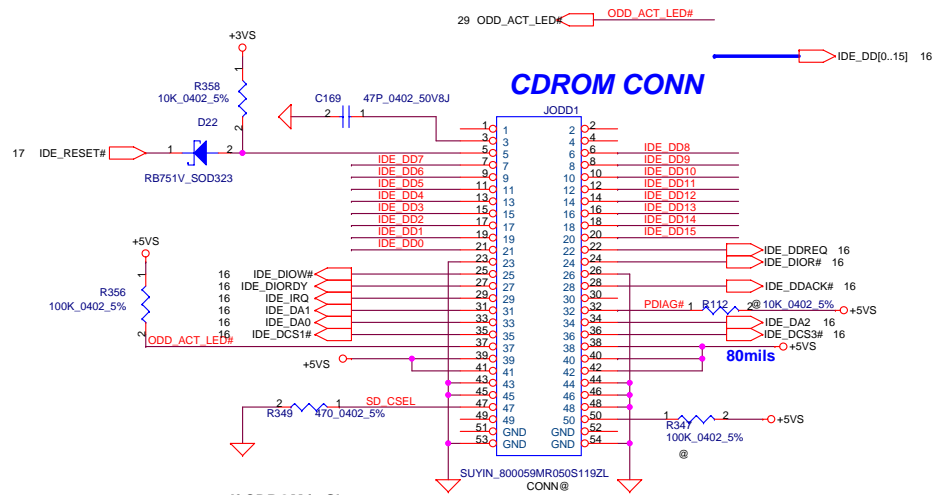


M/B ID	GPIO38	GPIO39
MP1 (Rev.0.3)	0	0
IRT (Rev1.0)	0	1
MP (Rev1.0)	1	0
MP (Rev2.0)	1	1

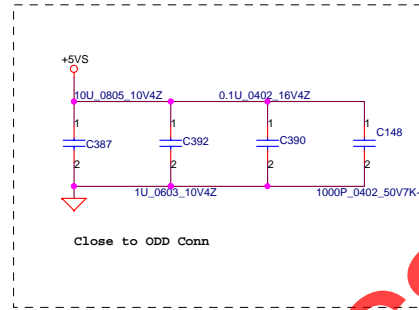
www.laptopcomponents.com



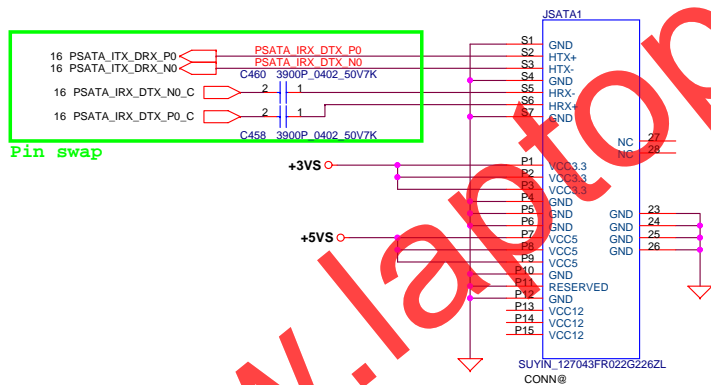
www.geminaelectronics.com



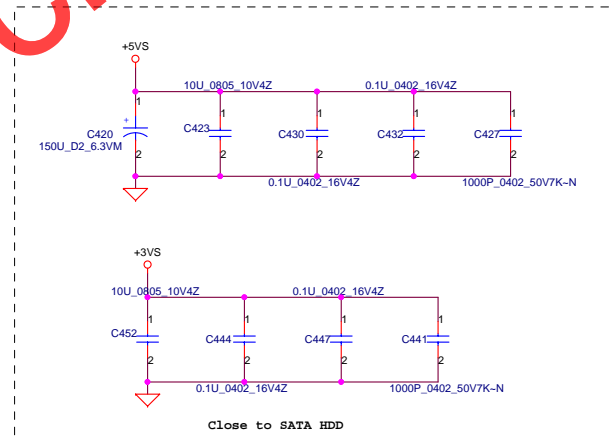
If CDROM is Slave  
then SD\_CSEL= Floating  
else SD\_CSEL= Low

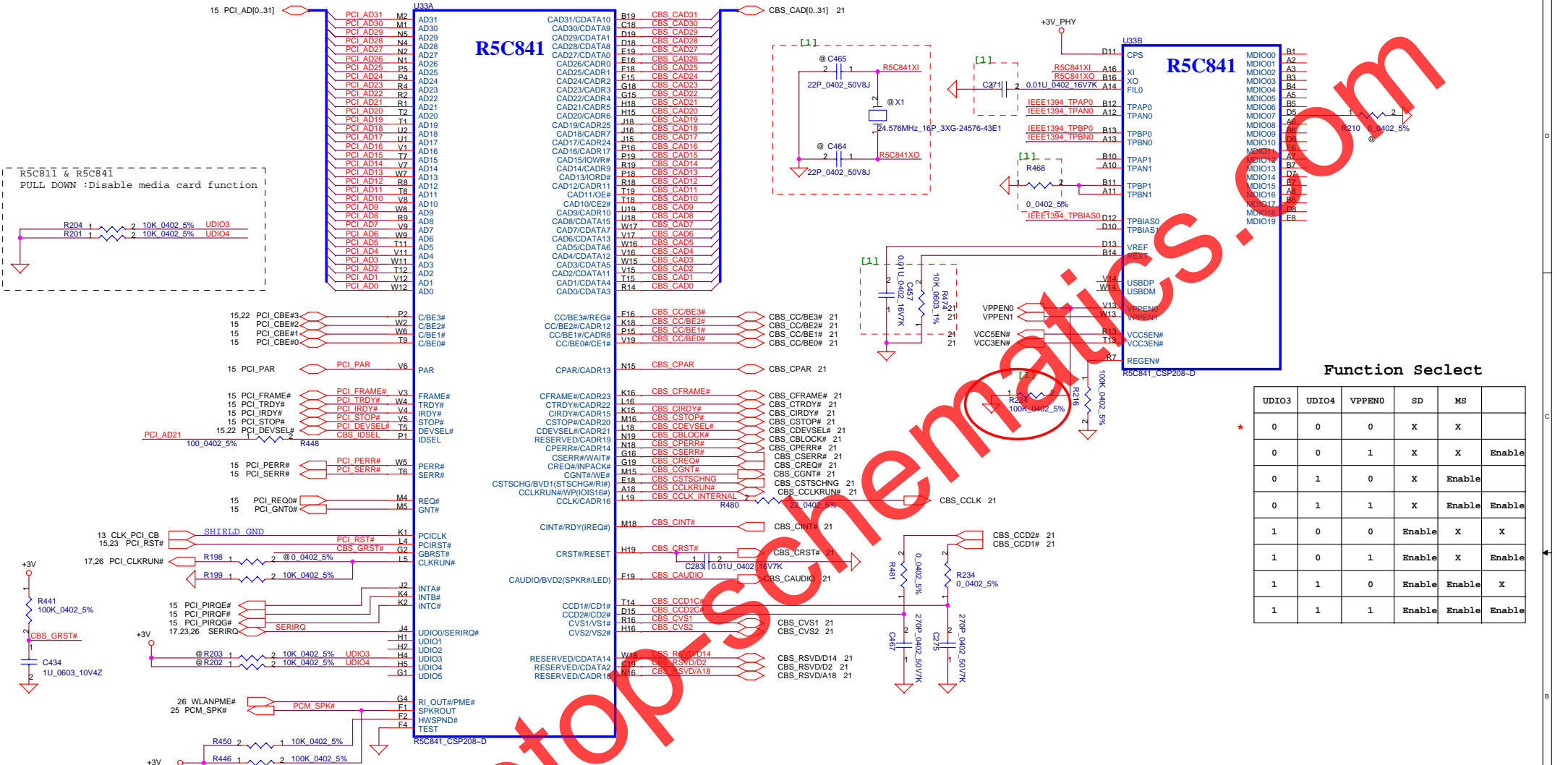


**SATA HDD CONN**



Pin swap





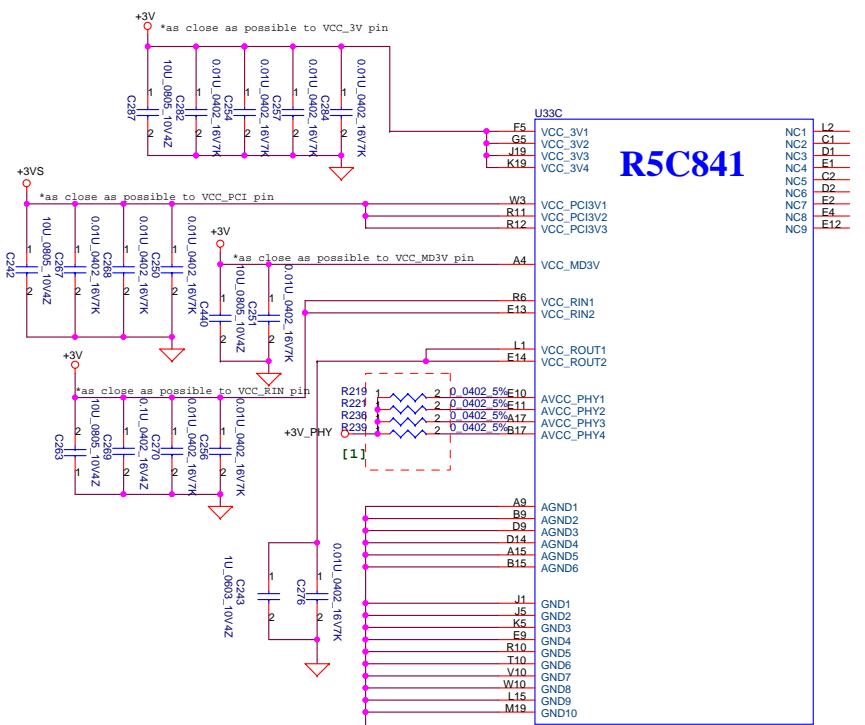
**Function Select**

UDIO3	UDIO4	VPPEN0	SD	MS	
0	0	0	X	X	
0	0	1	X	X	Enable
0	1	0	X	Enable	
0	1	1	X	Enable	Enable
1	0	0	Enable	X	X
1	0	1	Enable	X	Enable
1	1	0	Enable	Enable	X
1	1	1	Enable	Enable	Enable

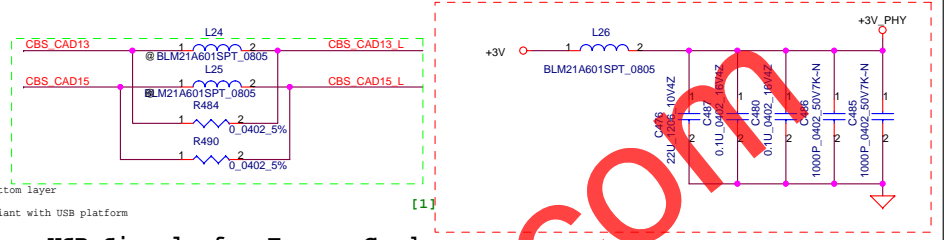
R5C811 & R5C841  
PULL DOWN :Disable media card function

apply same labels for all of TP+ ,TFA-and TPB-

Placement Near Card Bus Controller

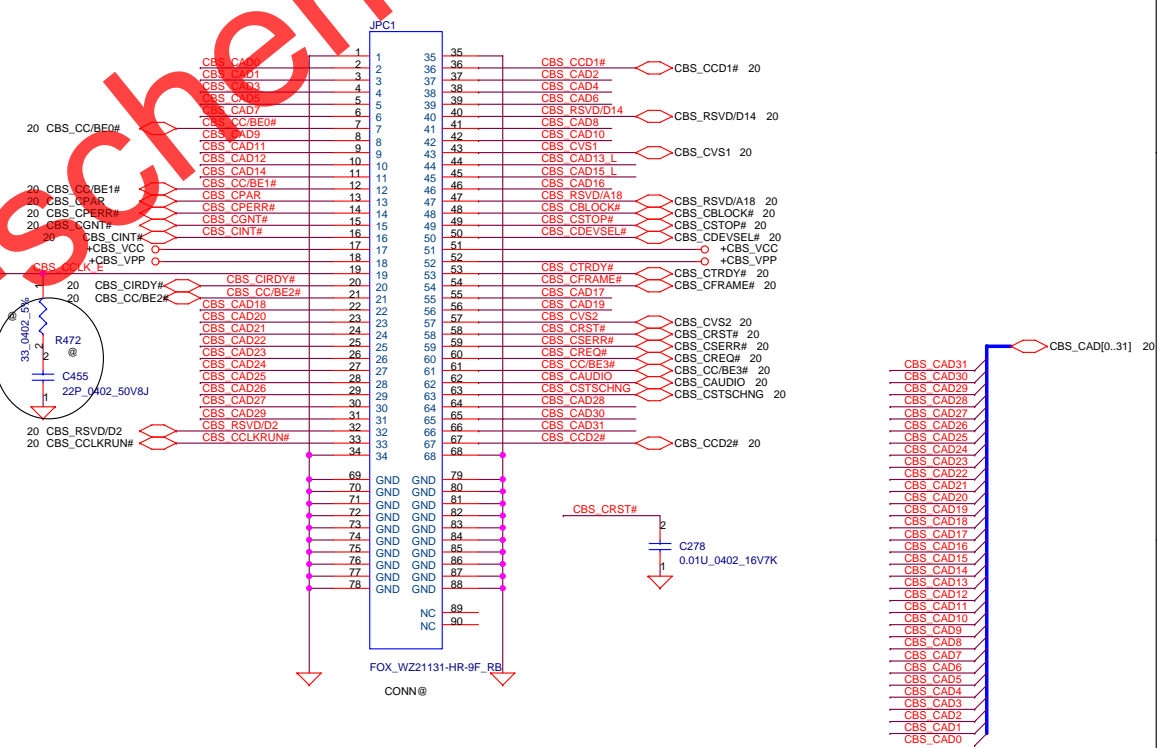
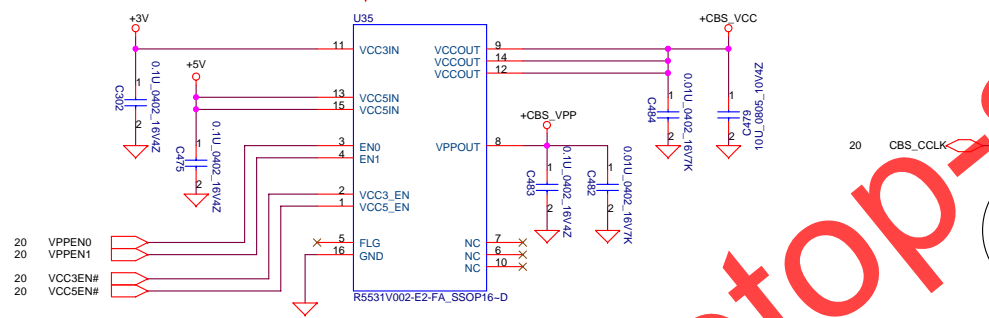


**R5C841**



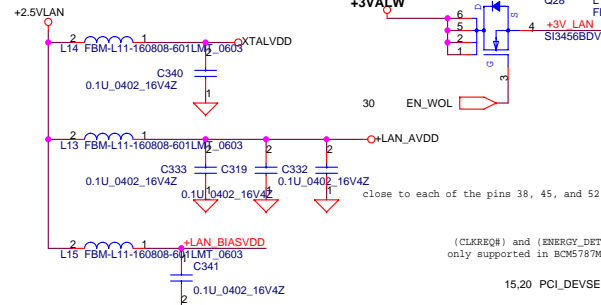
- 1. on top or bottom layer
- 2. no via hole
- 3. 90 ohm compliant with USB platform

**USB Signals for Epress Card**

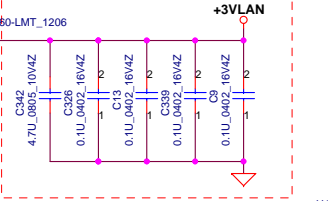


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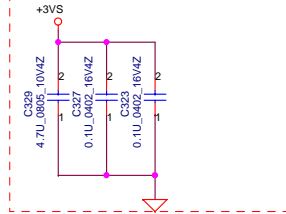
Layout Notice : Filter place as close chip as possible.



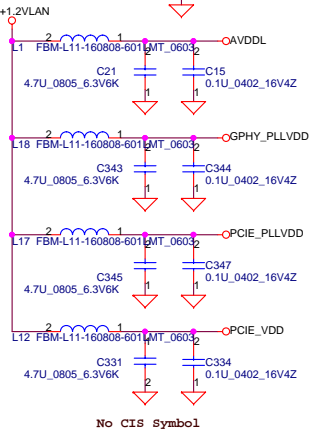
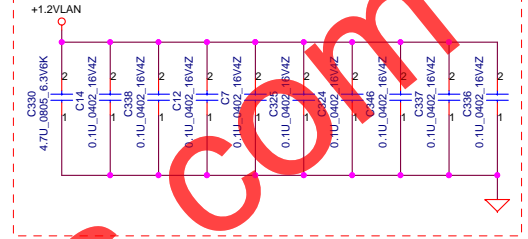
Layout Notice : Place as close chip as possible.



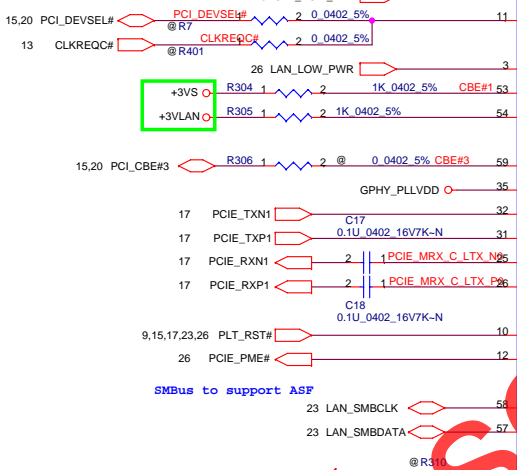
Layout Notice : 3.3V filter. Place as close chip as possible.



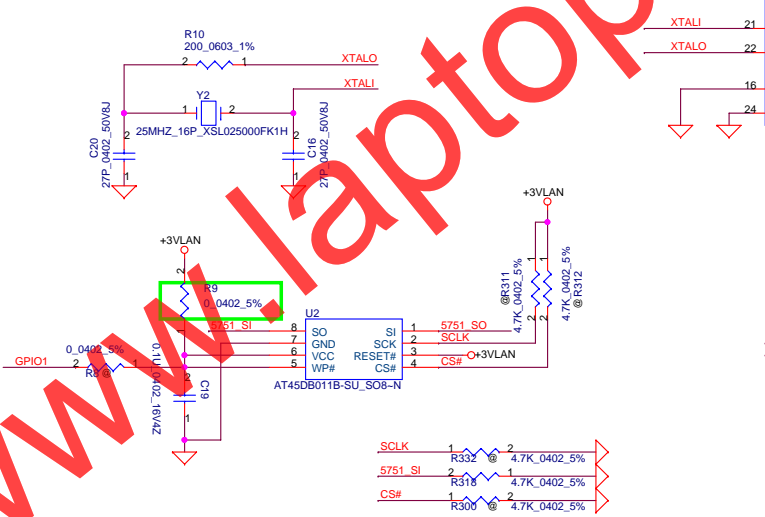
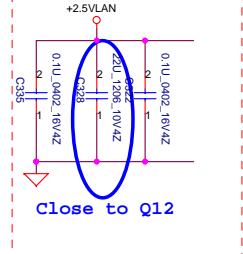
Layout Notice : 1.2V filter. Place as close chip as possible.



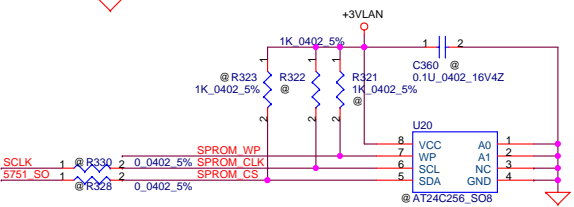
(CLKREQ#) and (ENERGY\_DET) are only supported in BCM5787M



Layout Notice : Place as close chip as possible.

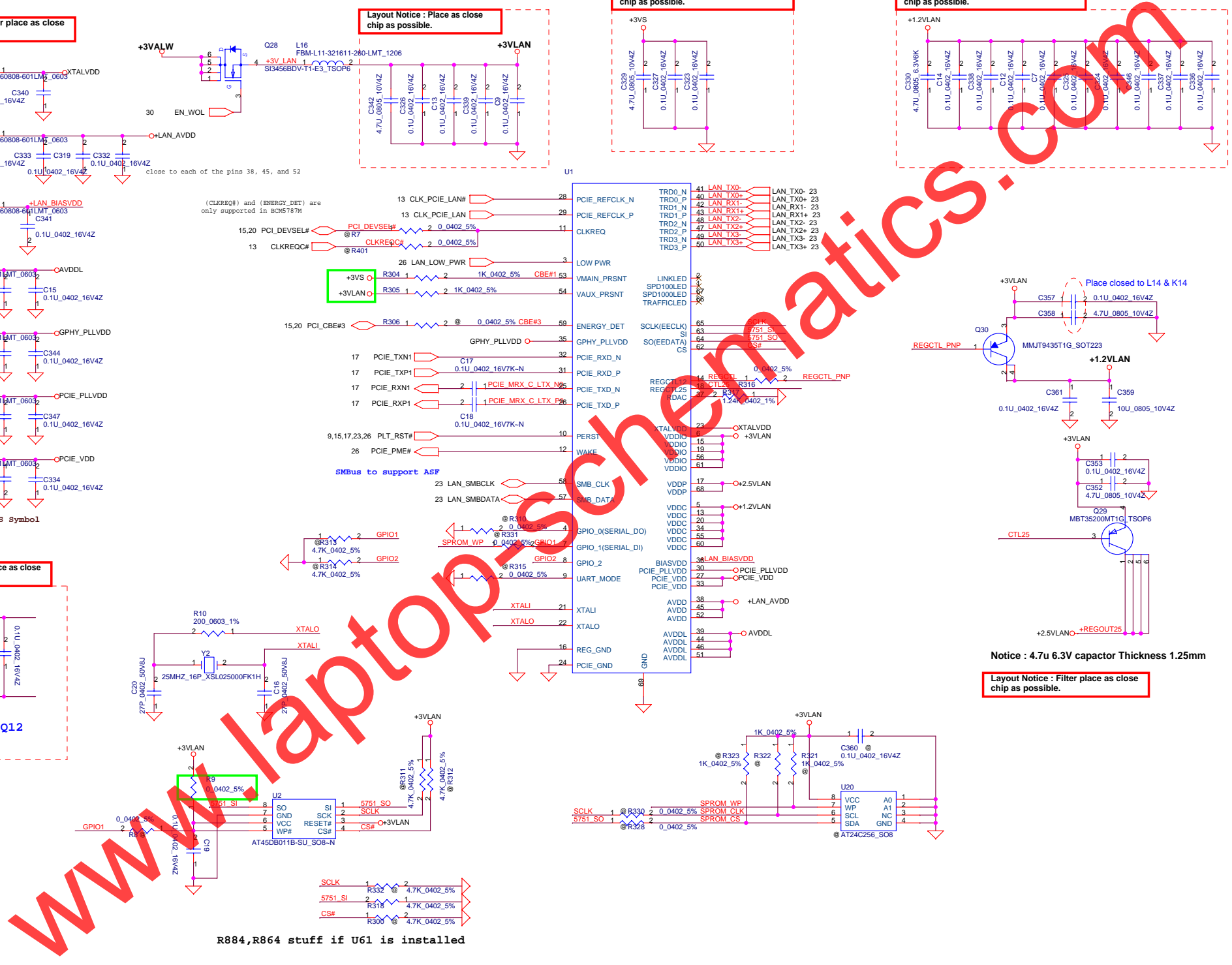
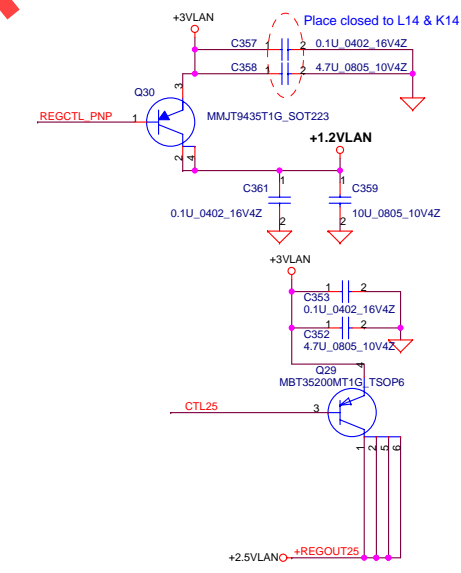


R884,R864 stuff if U61 is installed

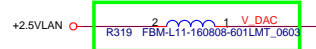


Notice : 4.7u 6.3V capacitor Thickness 1.25mm

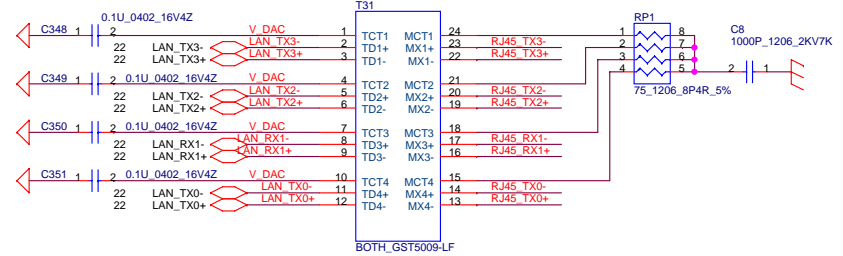
Layout Notice : Filter place as close chip as possible.



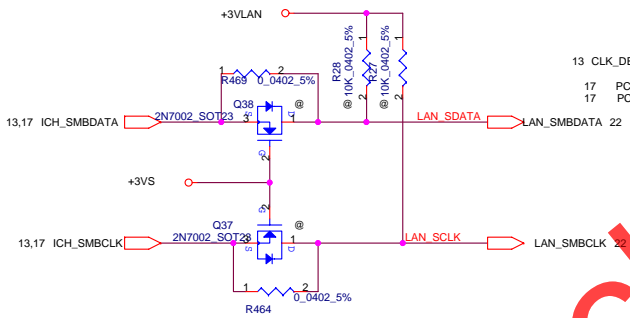
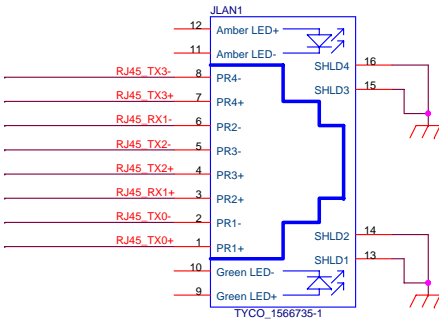




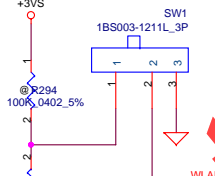
1. ES2 by rework form 0805 to 0603
2. Part name will modify in next phase



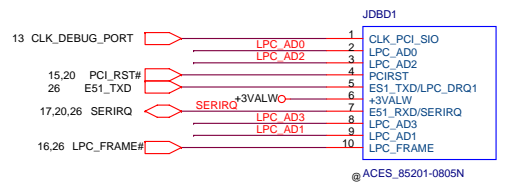
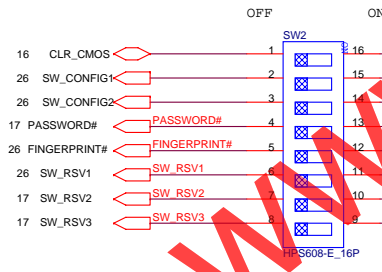
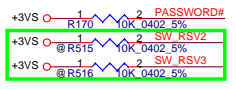
**Layout Note**  
24HST1041A-3 pls close to conn.



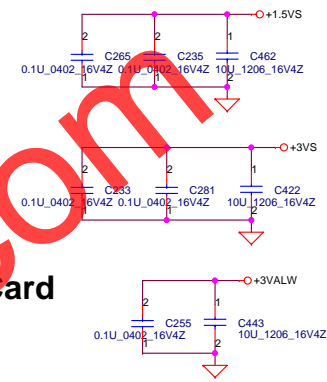
### Wireless\_BTN Killer switch



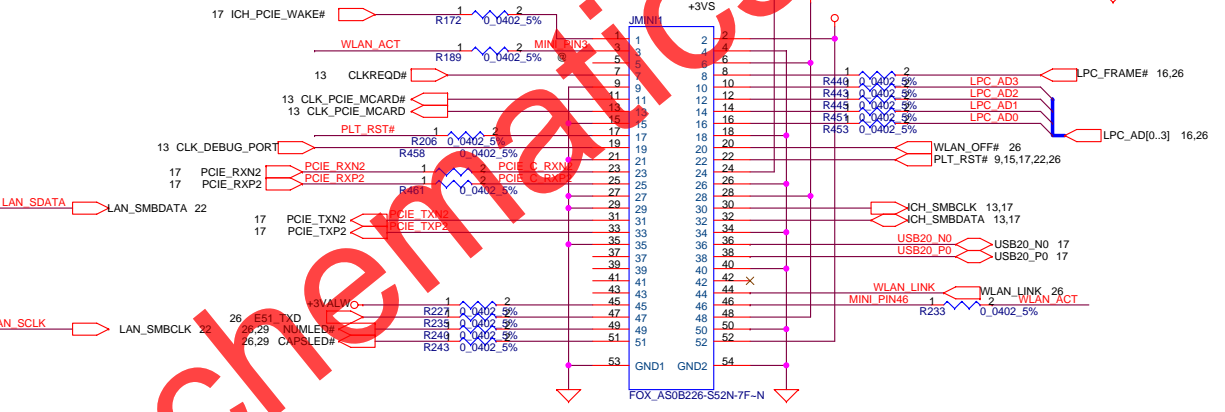
All 49.9 ohm + 0.1 uF termination components close to BCM5751M



For DEBUG

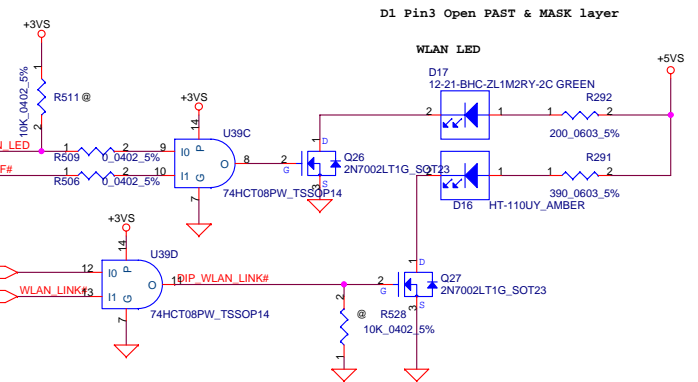
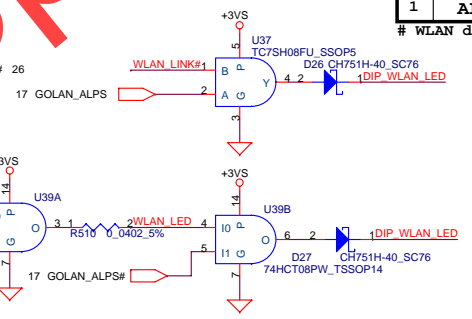


### Mini-Express Card

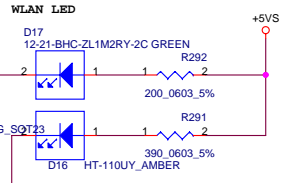


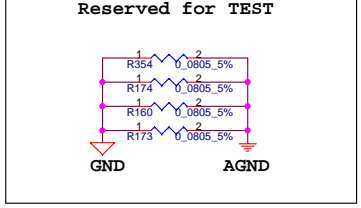
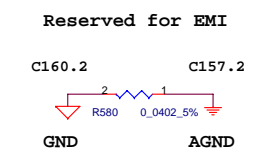
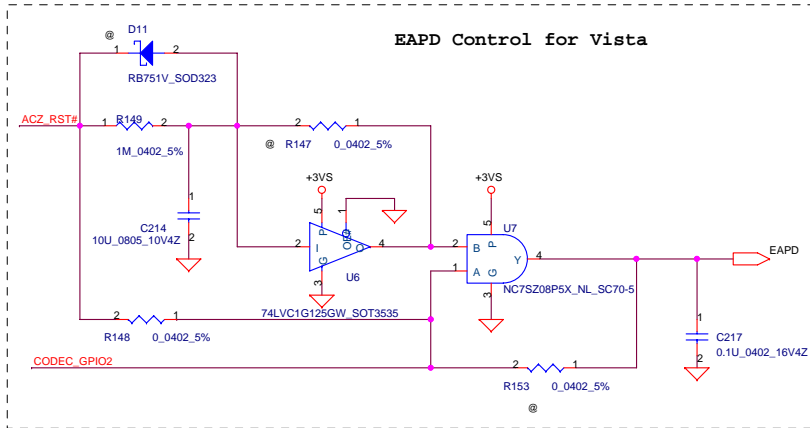
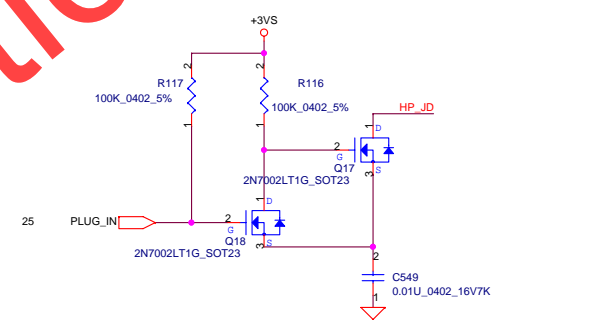
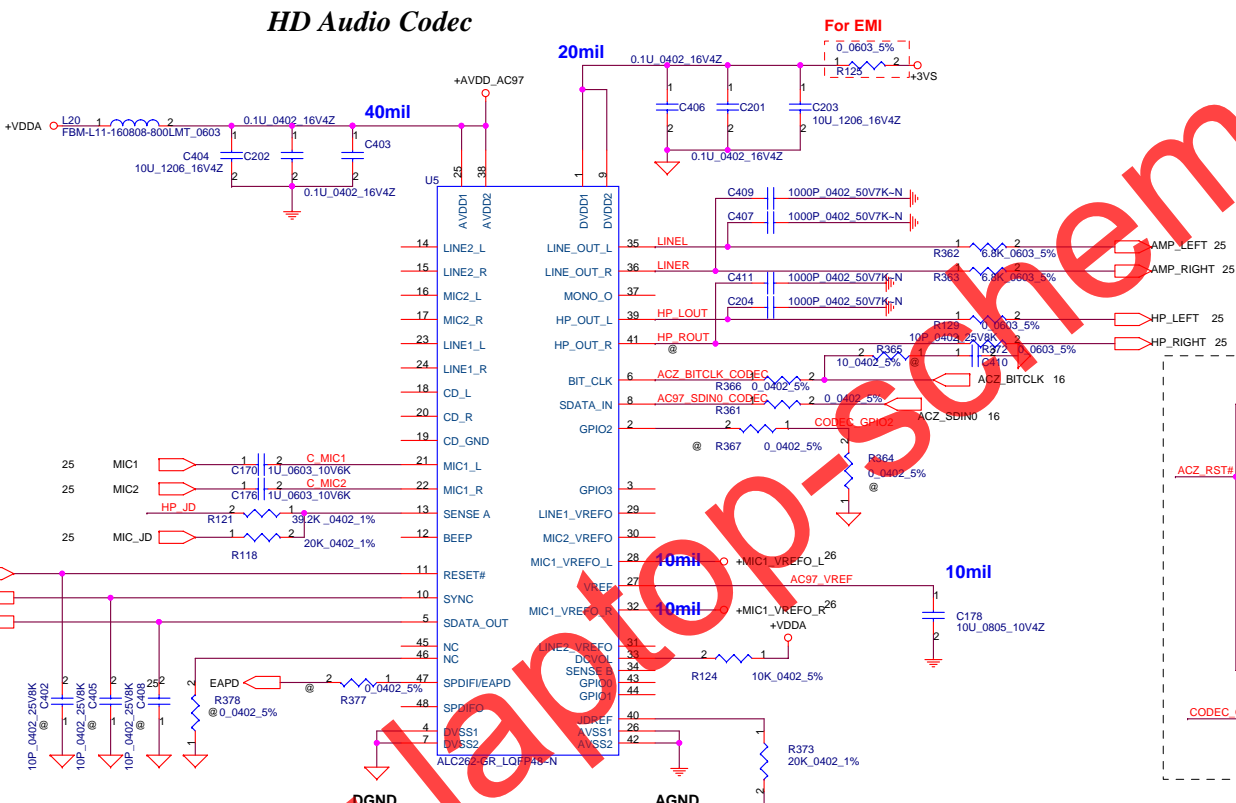
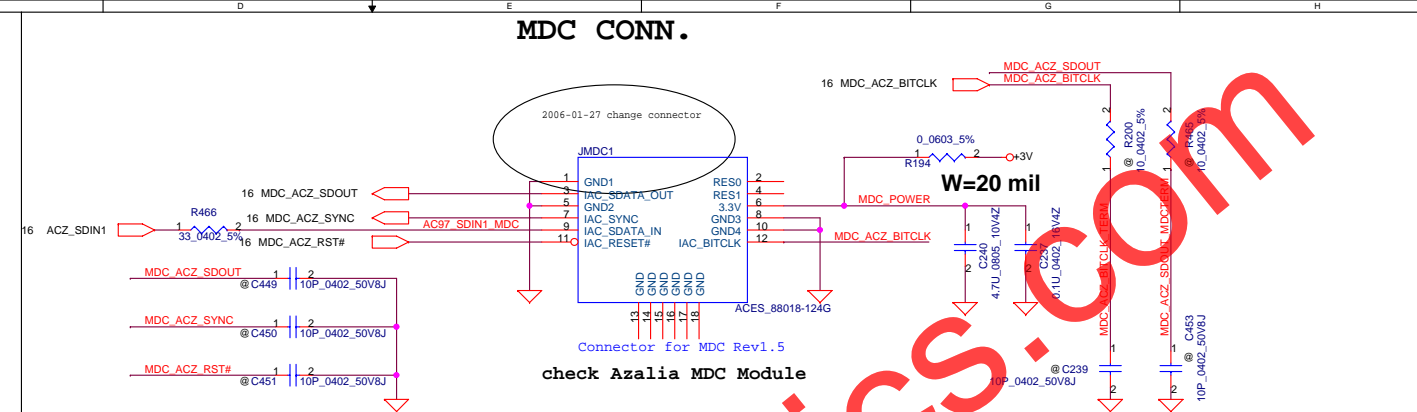
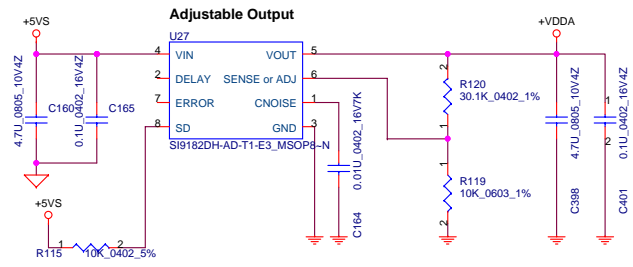
GOLAN_ALPS#	
0	GOLAN
1	ALPS

# WLAN detect by BIOS and program GOLAN\_ALPS# to control WLAN LED

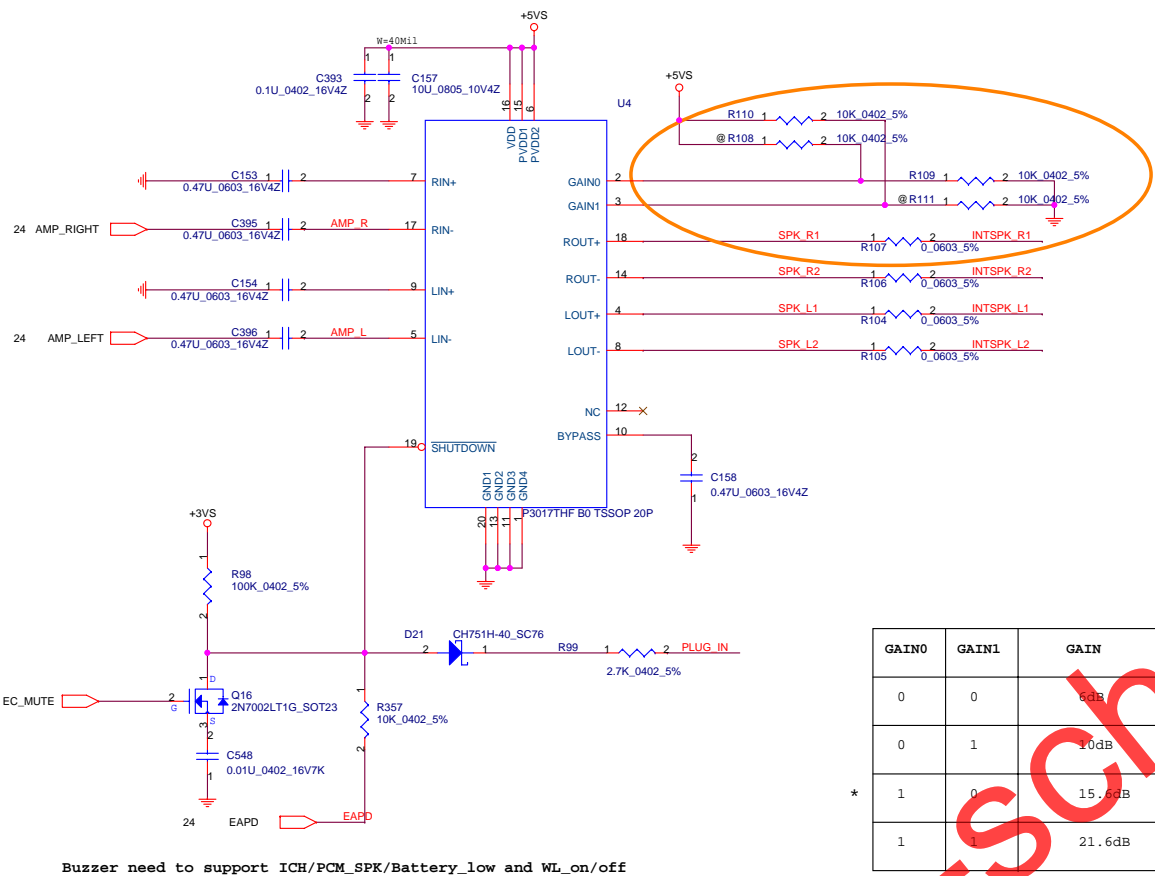


D1 Pin3 Open PAST & MASK layer

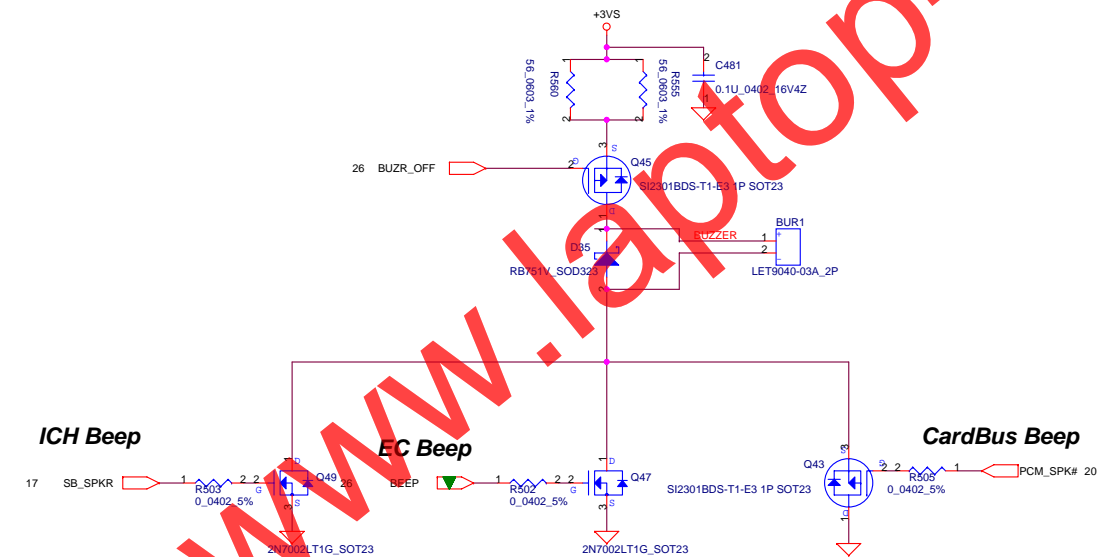




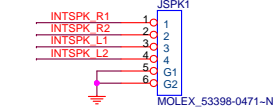
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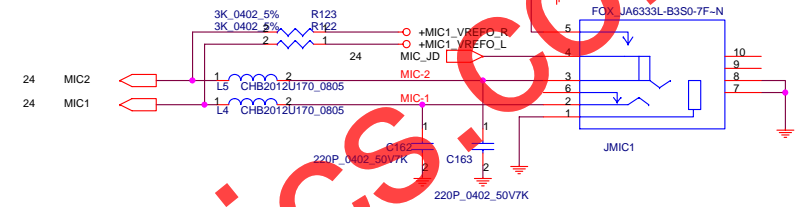
Buzzer need to support ICH/PCM\_SPK/Battery\_low and WL\_on/off



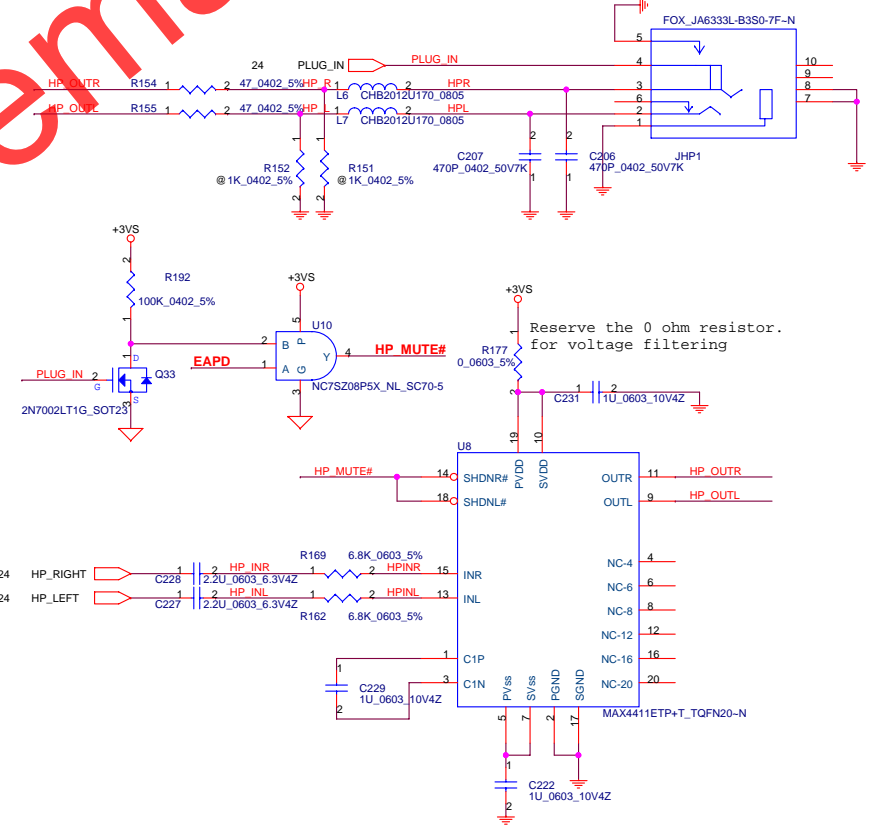
### Speaker Connector

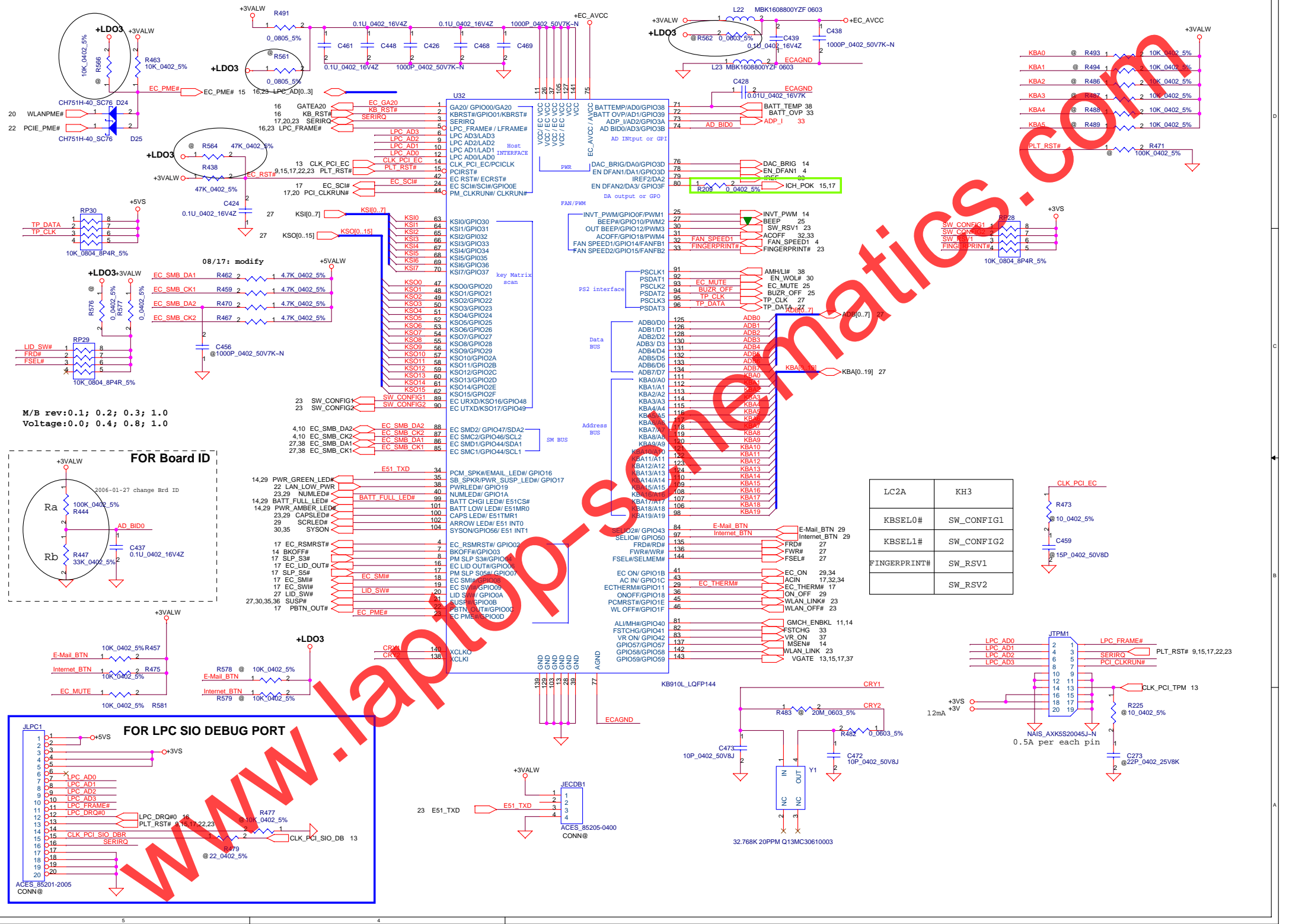


### MICROPHONE IN JACK



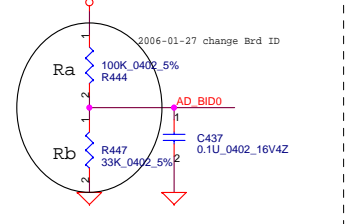
### HEADPHONE OUT JACK



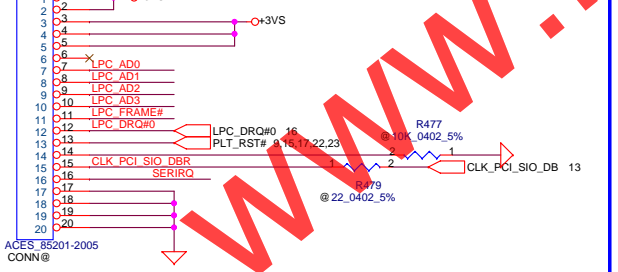


M/B rev:0.1; 0.2; 0.3; 1.0  
 Voltage:0.0; 0.4; 0.8; 1.0

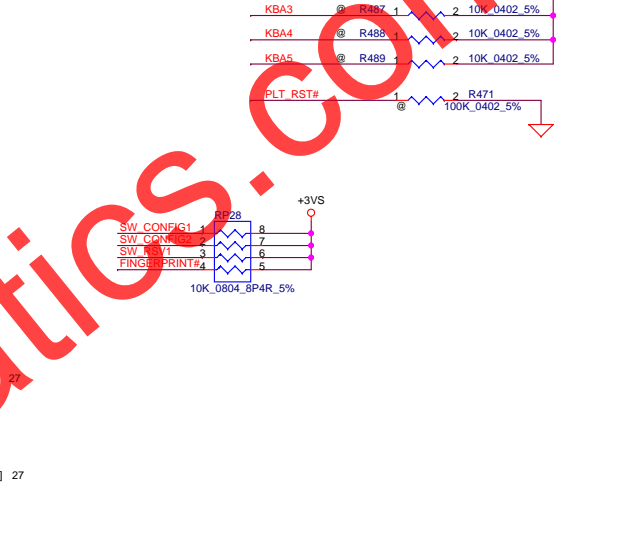
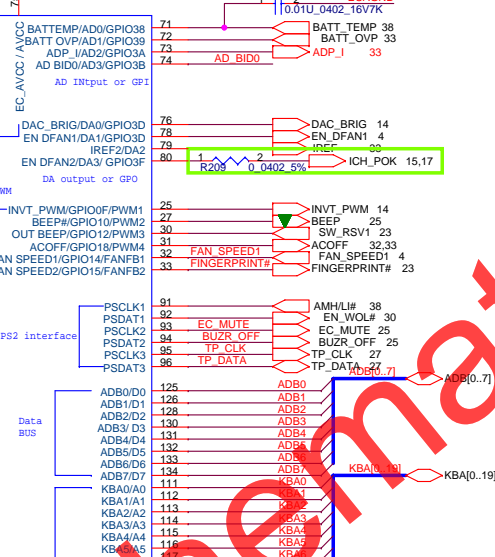
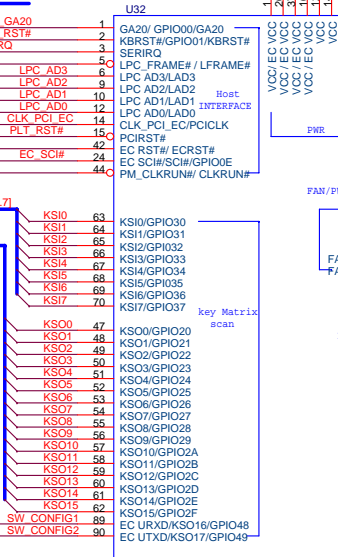
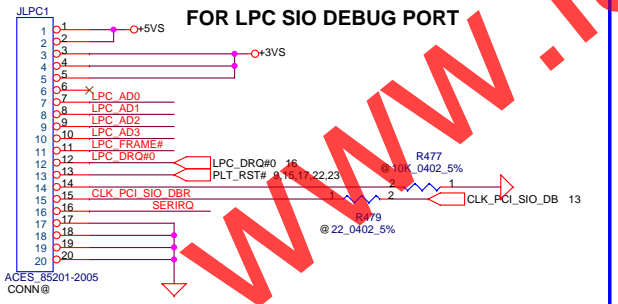
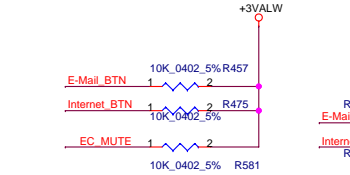
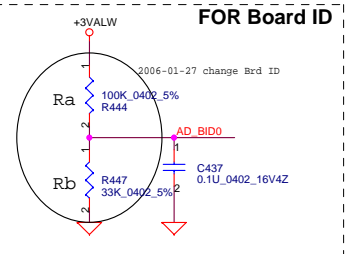
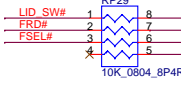
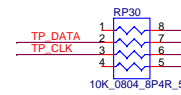
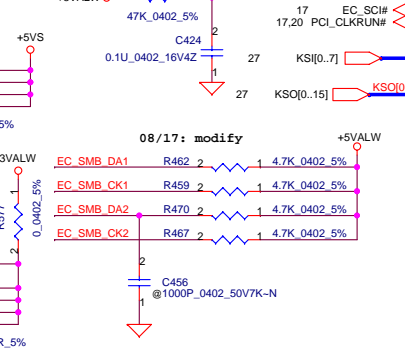
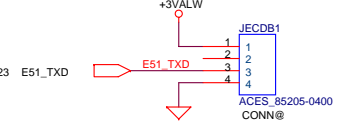
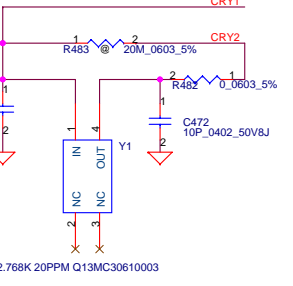
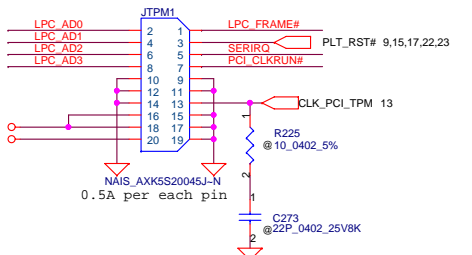
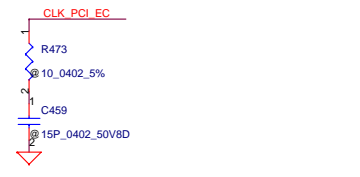
**FOR Board ID**

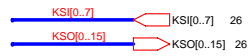
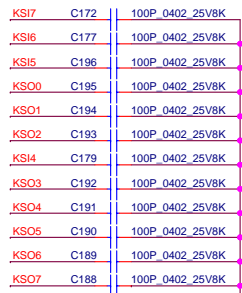
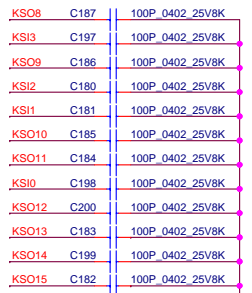


**FOR LPC SIO DEBUG PORT**

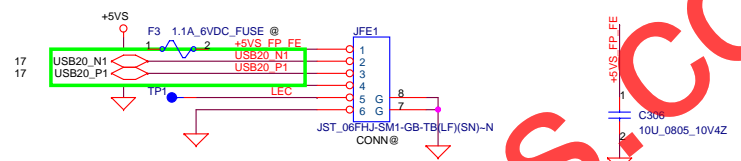


LC2A	KH3
KBSEL0#	SW_CONFIG1
KBSEL1#	SW_CONFIG2
FINGERPRINT#	SW_RS1
	SW_RS2

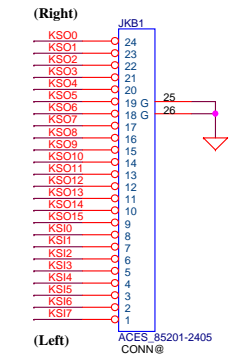




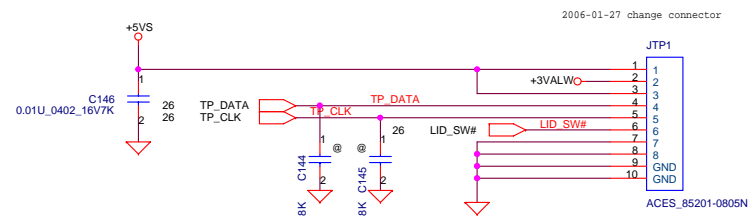
### Felica Conn



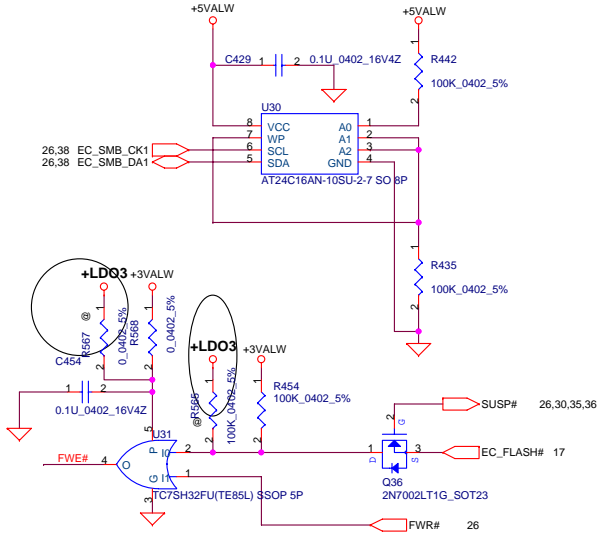
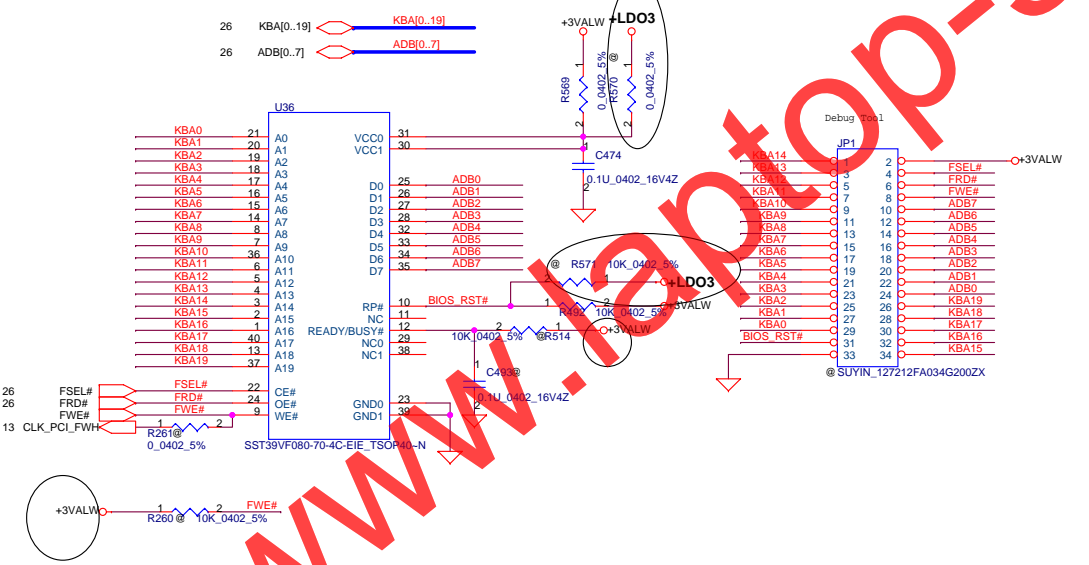
### INT\_KBD CONN.



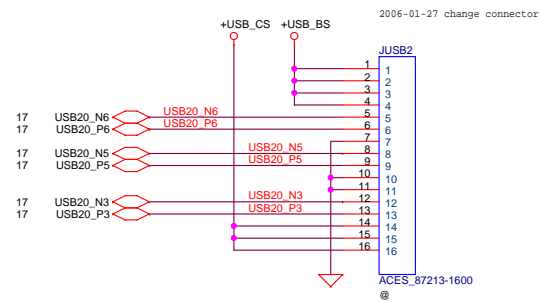
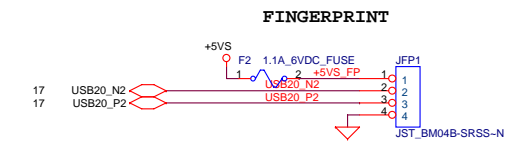
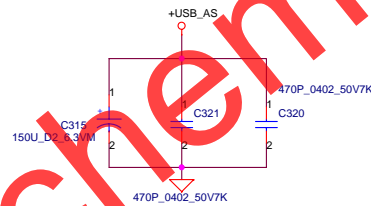
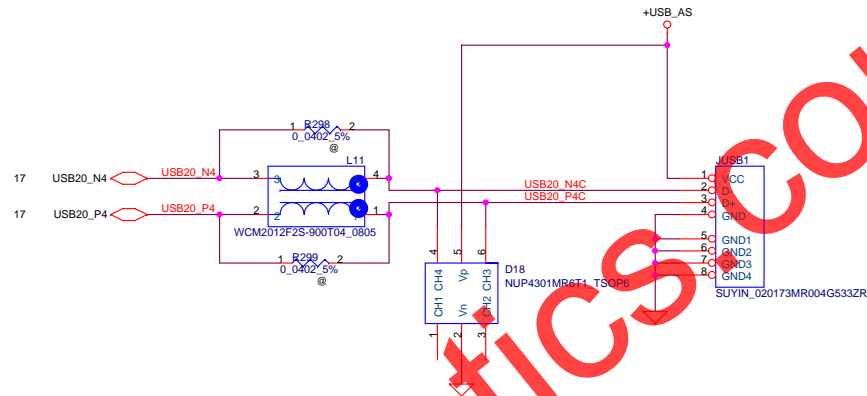
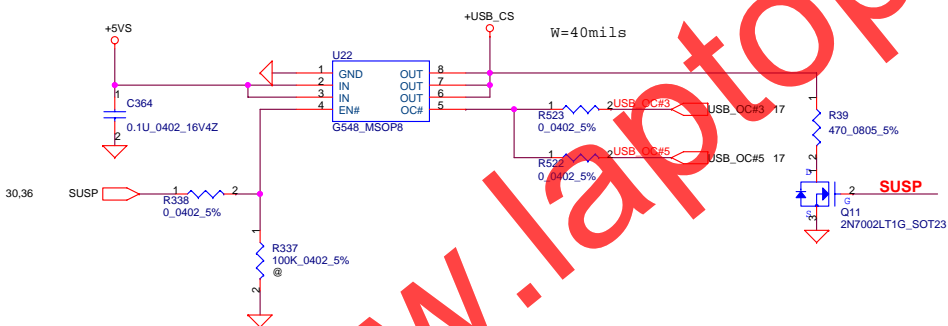
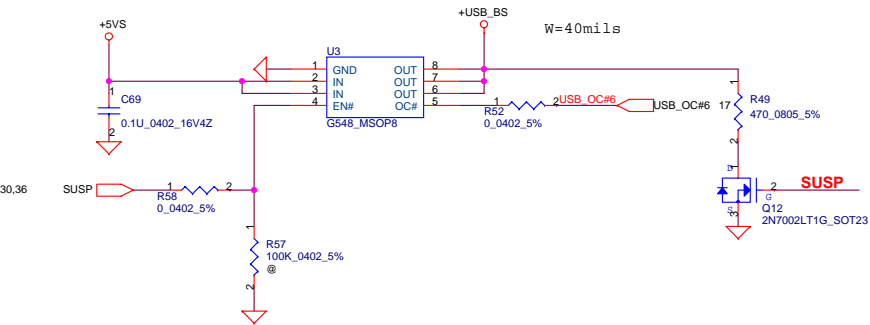
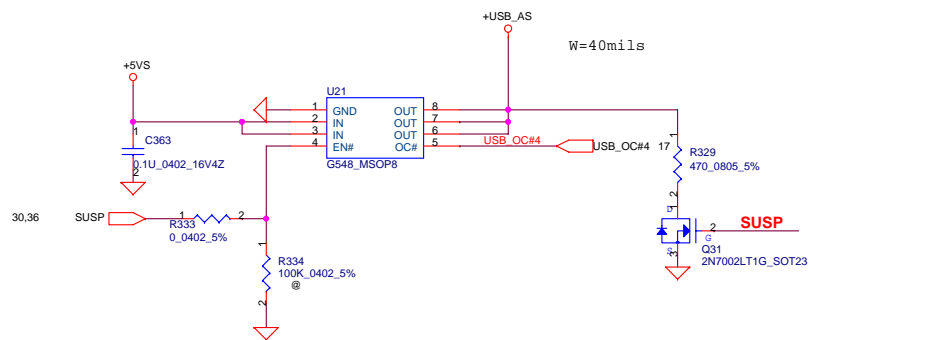
### TO M/B



### 1M Byte BIOS ROM



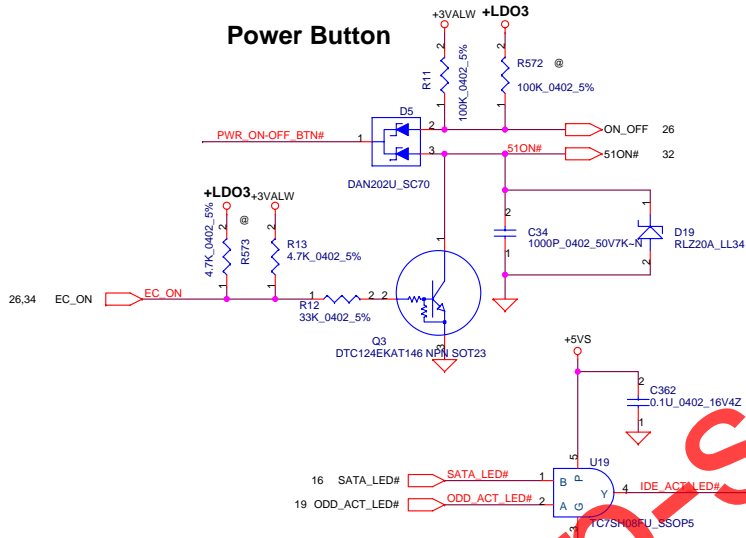
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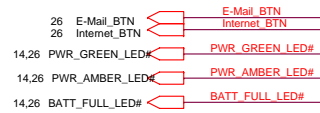
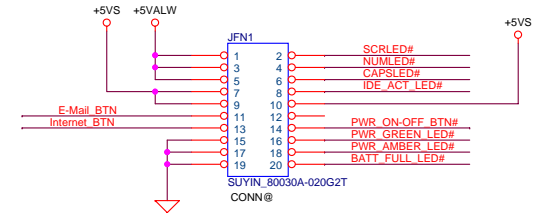
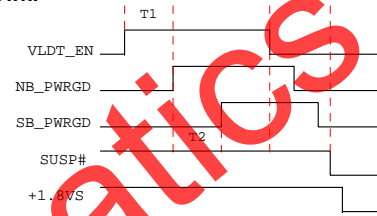
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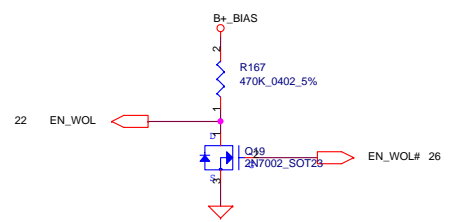
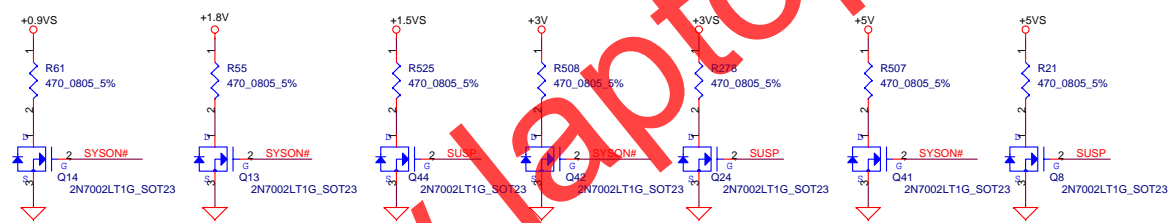
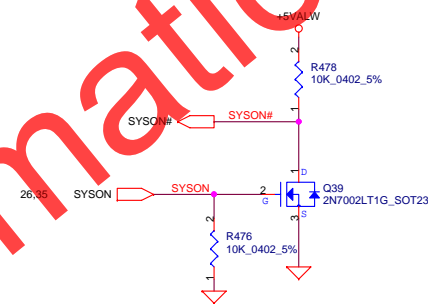
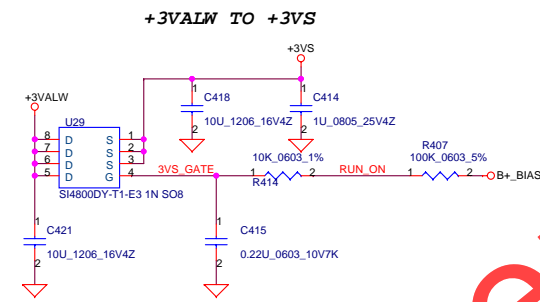
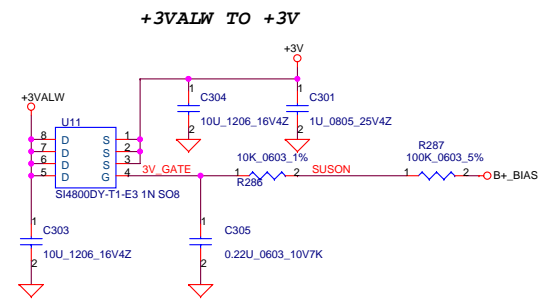
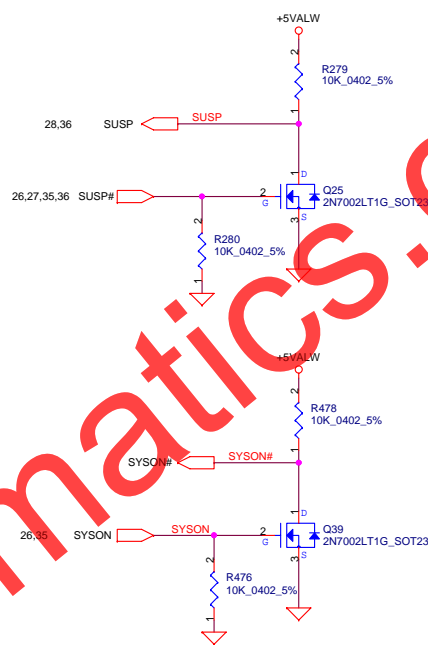
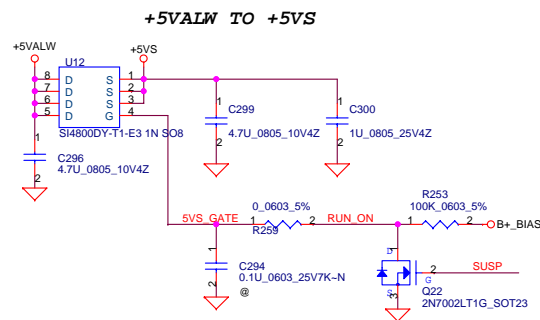
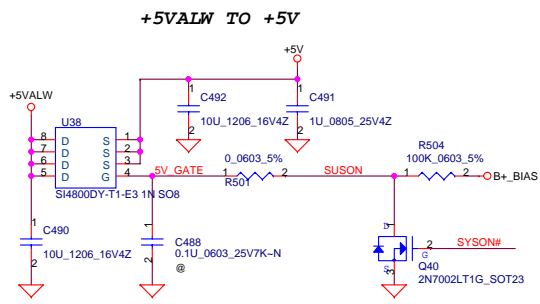
### Power Button



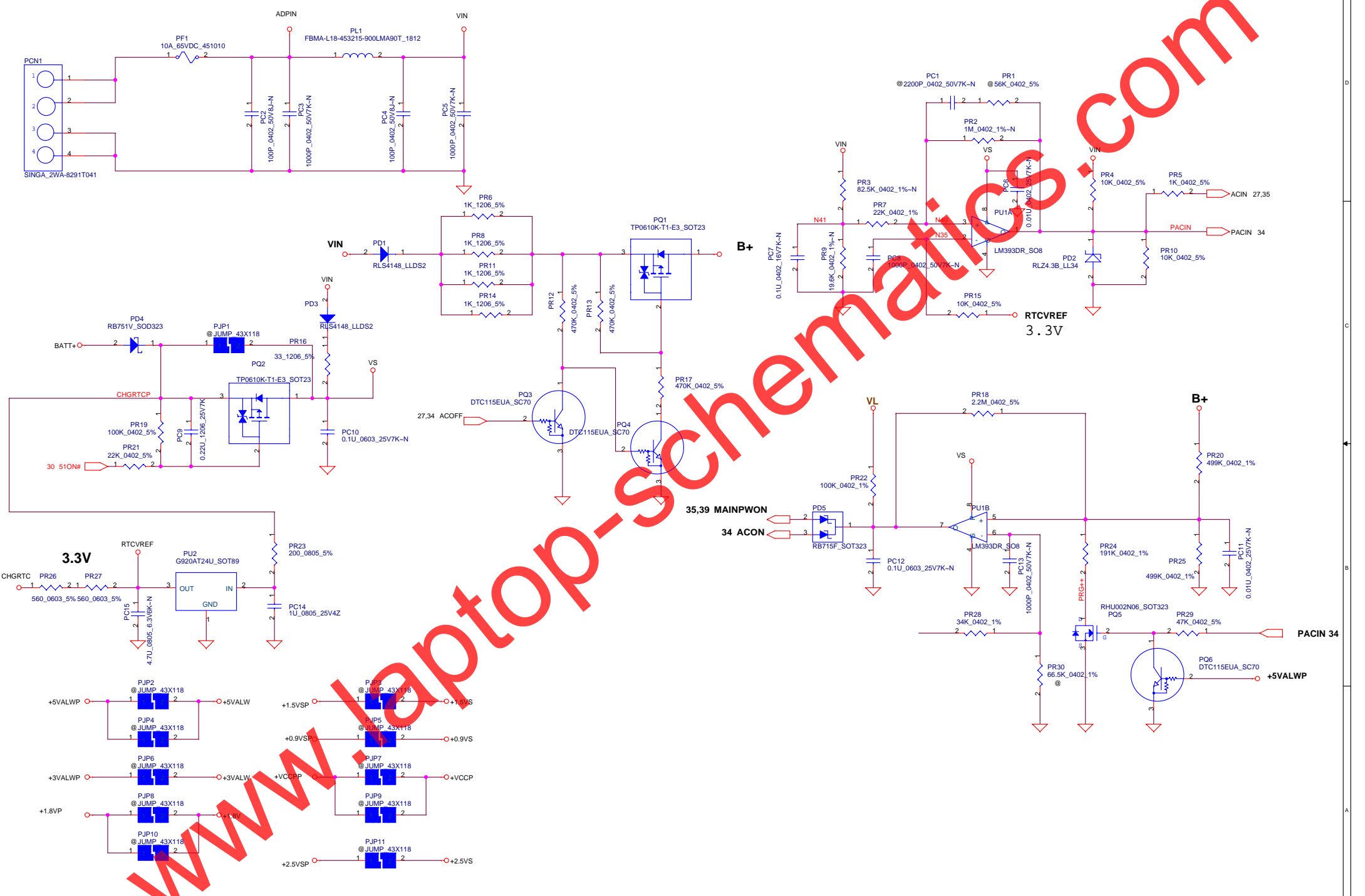
note:T1 minimum 15ms,T2 minimum 33ms/maximum 500ms, SUSP# goes to low after SB\_PWRGD goes to low for power down.



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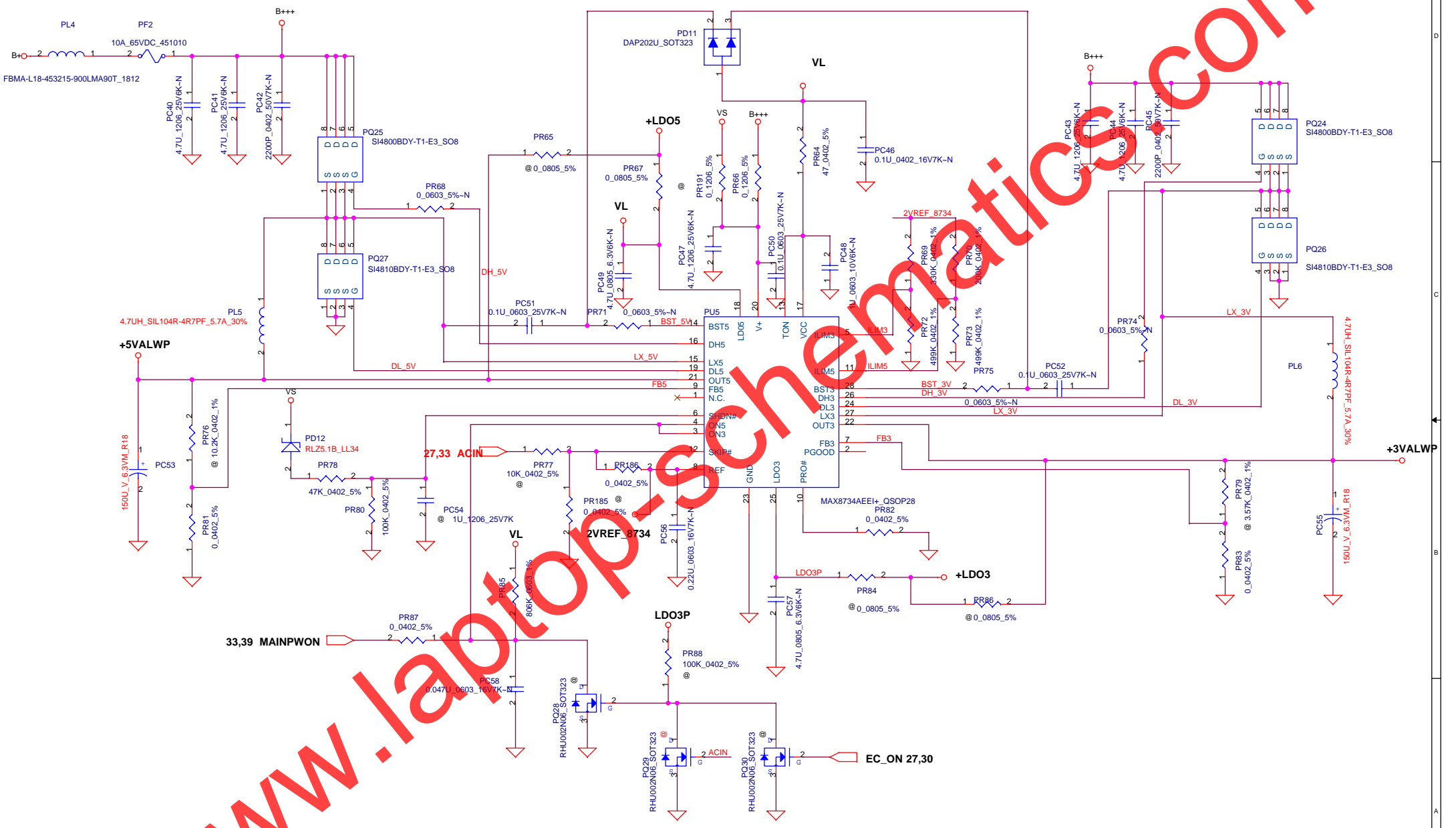
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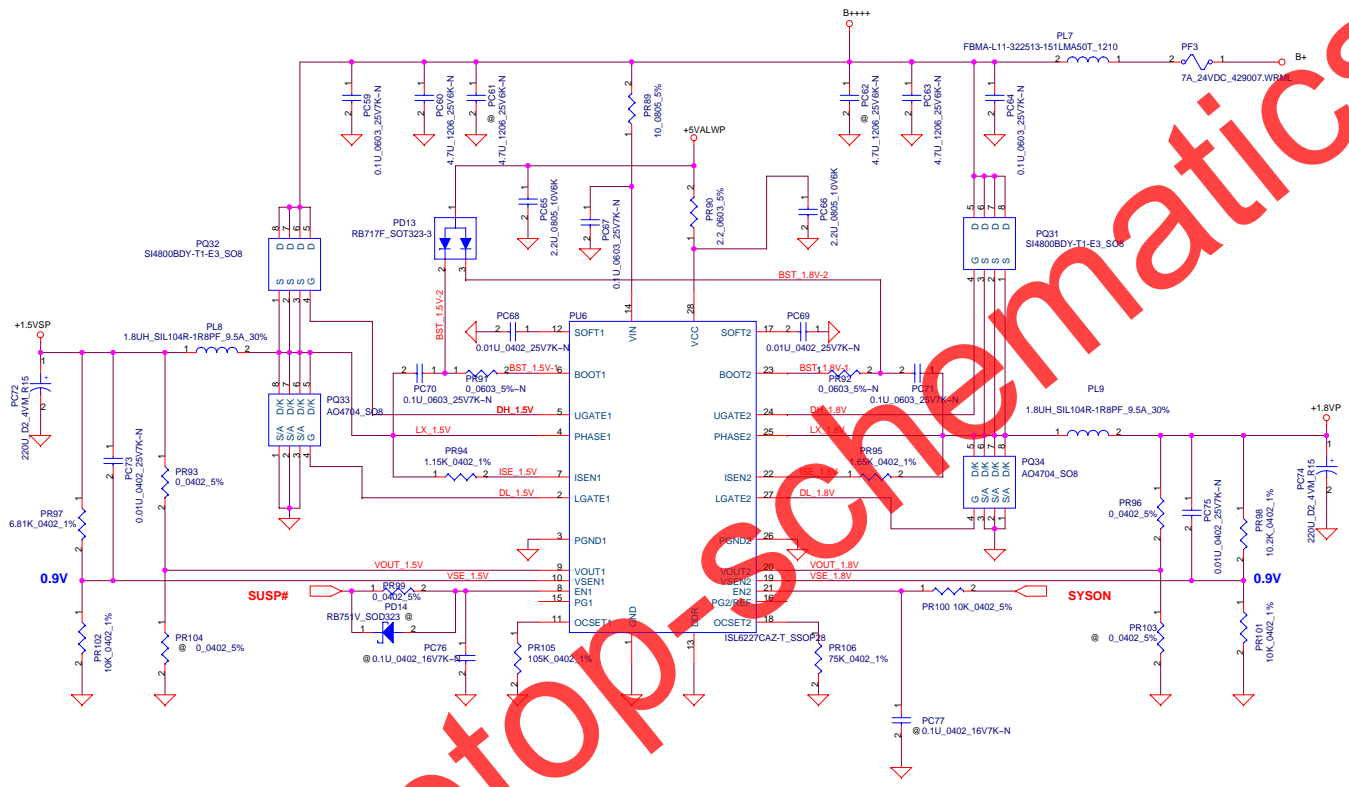


+3.3VALWP/+5VALWP

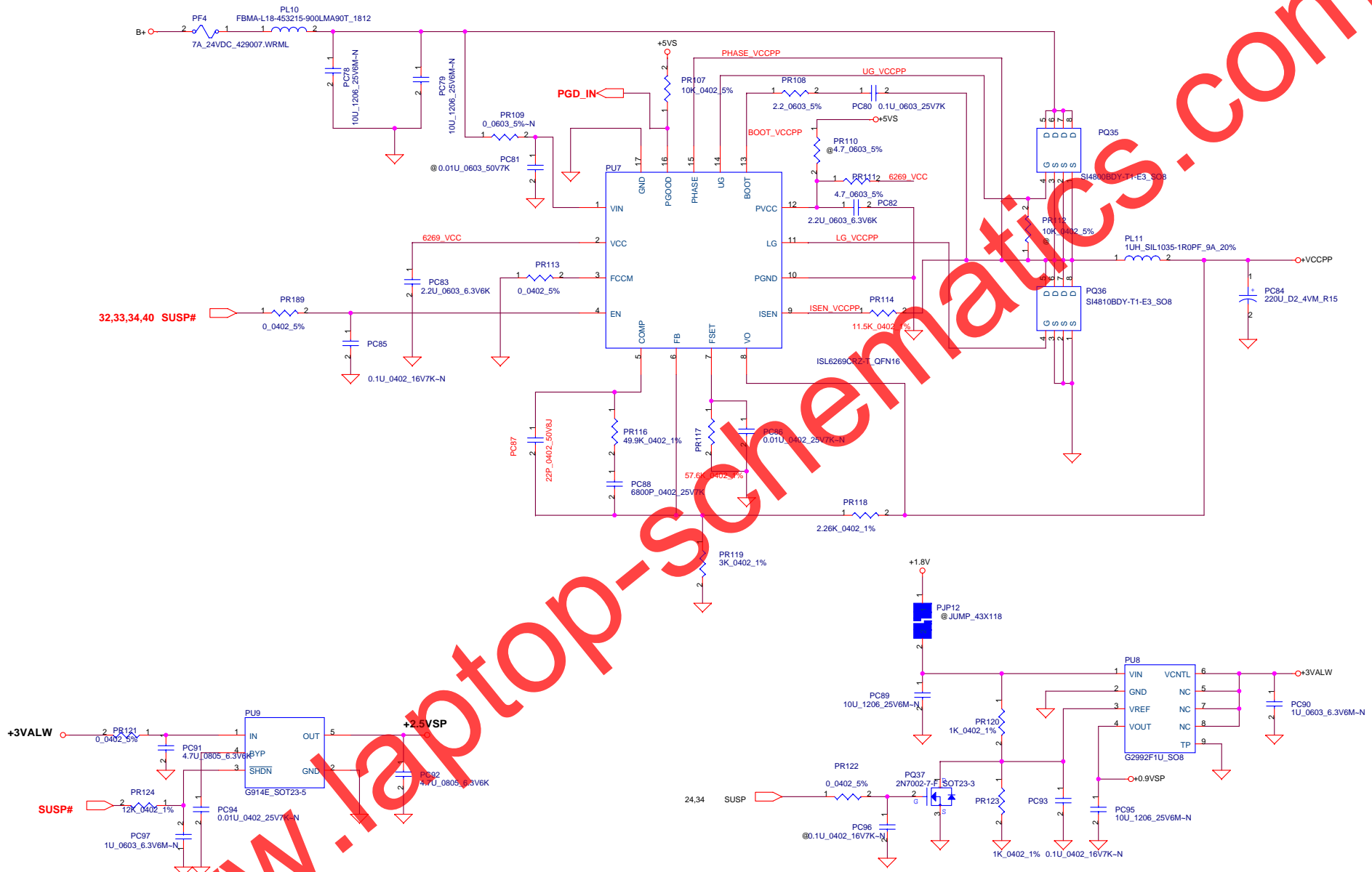


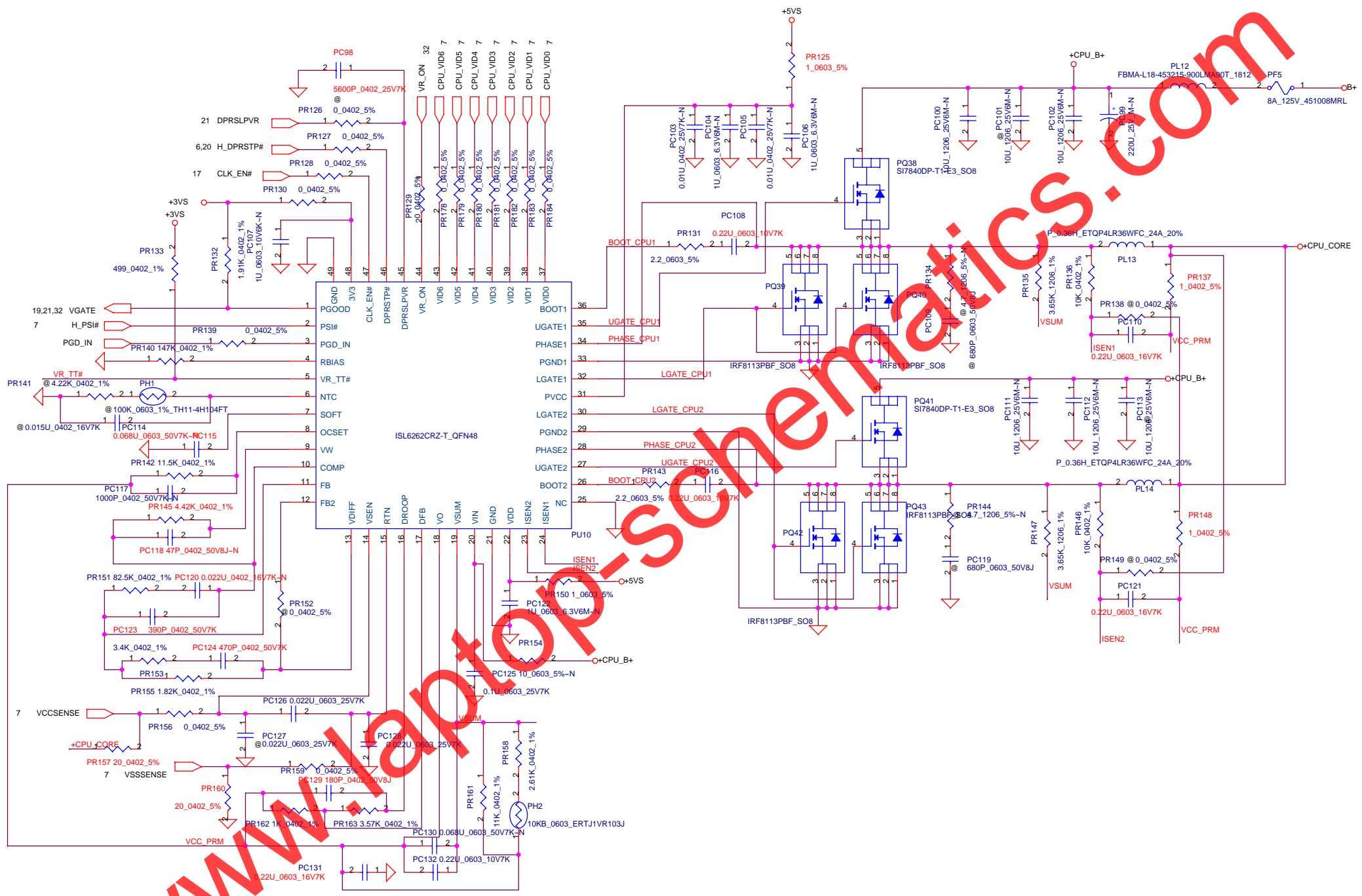
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www.laptopcircuitdiagramatics.com



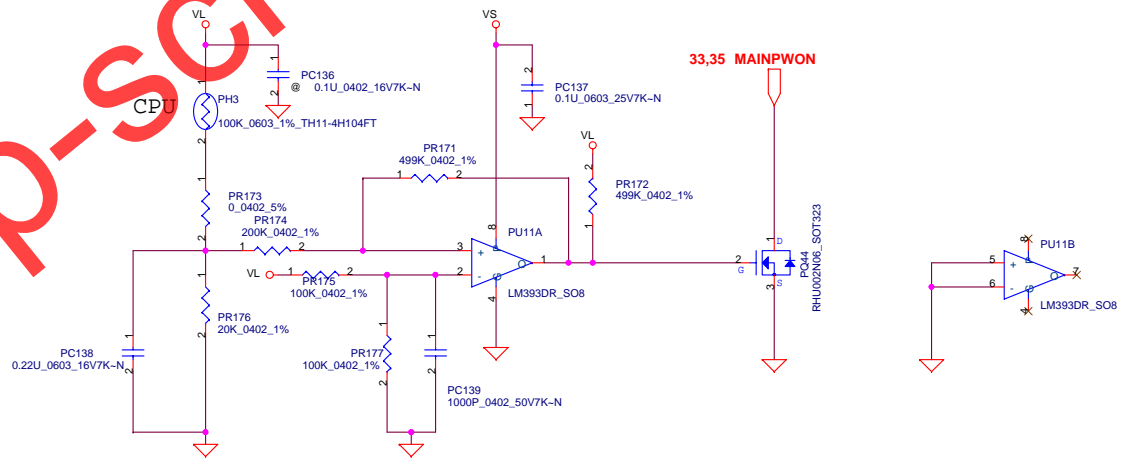
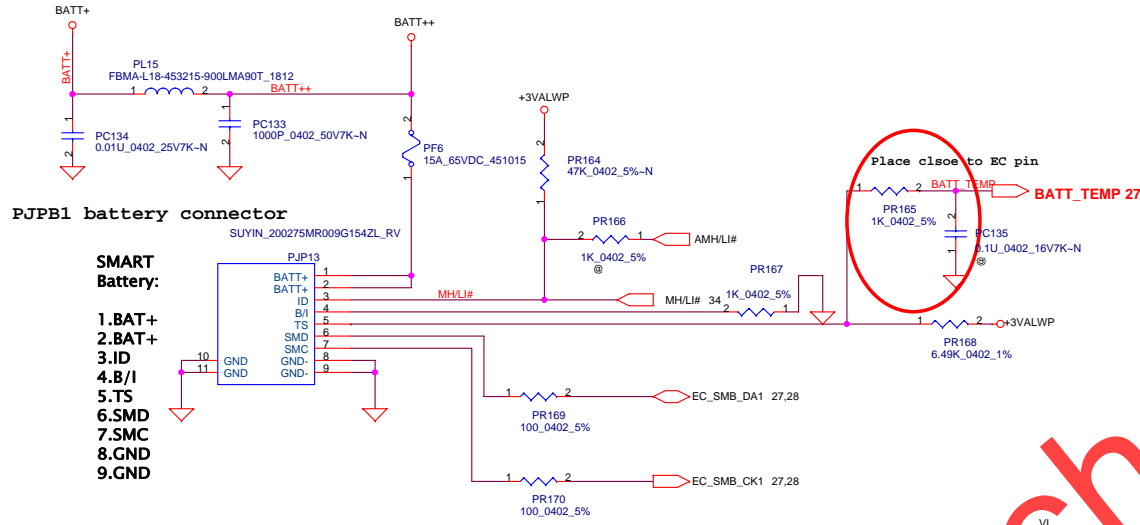






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Battery Connect/OTP



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