DW70 CALPELLA N11P-GE1 Schematics

uFCPGA Mobile Arrandale/Clarksfield

Intel Ibex Peak-M

2009-09-03

REV : SA

DY : Nopop Component
UMA : Pop when schematic is UMA
DIS : Pop when schematic is DIS
ARD : Pop when schematic is Arrandale
CFD : Pop when schematic is Clarksfield

UMA

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Title: *Cover Page*

Size: Custom | Document Number: *Vostro Calpella* | Rev: *SA*

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Winery CALPELLA Block Diagram

Project code : 91.4RU01.001
Part Number : 48.4RU06.0SA
PCB P/N : 09290
Revision : SA

PCB LAYER

L1: Top
L2: VCC
L3: Signal
L4: Signal
L5: GND
L6: Bottom

Clock Generator
SLG8SP585 7

VRAM(gDDR3)
64Mbx16x8 (1GB)
84,85,89,90

VRAM

Nvidia
N11P-GE1(40nm)
80,81,82,83

100MHz/
2.5Gbps
PCIe x 16
Bandwidth
:8GB

Intel CPU
Arrandale
Clarksfield
8,9,10,11,12,13,14

DDRIII Channel A
Arrandale 800/1066MHz
Clarksfield 1066/1333MHz

DDRIII DM1 18
Arrandale 1066MHz
Clarksfield 1333MHz

DDRIII Channel B
Arrandale 800/1066MHz
Clarksfield 1066/1333MHz

DDRIII DM2 19
Arrandale 1066MHz
Clarksfield 1333MHz

HDMI 57
CRT 55
LCD 54

HDMI
RGB CRT
LVDS

Switchable

(Dual Channel)

DMIx4
FDI

Intel
PCH

14 USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
SATA ports (6)
PCIE ports (8)
LPC I/F
ACPI 1.1
PCI/PCI BRIDGE
20,21,22,23,24,25,26,27,28

PCIE x 1
10/100/1000LOM
RTL8111DL
RJ45 CONN
(On LAN board)

Power SW
TPS2231R
New Card
(On I/O board)

PCIE
100MHz
2.5Gbps

PCIE x 1
USB 2.0 x 1

Mini-Card
802.11a/b/g/n 64

Touch Panel
(On LAN board)

Left Side:
USB x 2
63

Right Side:
USB x 2
(On LAN board)

CAMERA
(Option) 73

Bluetooth
(On Audio board)

Biometric 78

USB 2.0
480Mbps

SM Bus
400KHz

Free fall sensor 40

LPC Bus
33MHz

TPM CONN 76

DEBUG BOARD
GOLDEN FINGER 70

1394 Connector

(8 in 1)SD/MMC
MS/MS Pro/xD

(On I/O board)

CardReader
1394

RICOH
R5U230

PCIE
100MHz
2.5Gbps

Digital Mic Array
(Option)

MIC IN
HP OUT

(On Audio board)

HD AUDIO
CODEC
OP AMP

IDT
92HD81-UA

HD AUDIO

2CH SPEAKER

SATA, USB
SATA
SPI

KBC
NUVOTON
NPCE781BA0DX 37

SPI
SM Bus

USB,ESATA
Multi-Port x1 63

ODD
HDD 59

Flash ROM
4MB

Flash ROM
256kB 62

Touch
PAD 68

Int.
KB 68

Thermal
& Fan
EMC2102 39,58

Capacity Board

CPU DC/DC ISL62883 47,48	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

SYSTEM DC/DC TPS51125 46	
INPUTS	OUTPUTS
+PWR_SRC	+15V_ALW +3.3V_RTC_LDO +5V_ALW +3.3V_ALW

SYSTEM DC/DC TPS51116 50	
INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS +0.75V_DDR_VTT +V_DDR_REF

SYSTEM DC/DC ADP3211 53	
INPUTS	OUTPUTS
+PWR_SRC	+CPU_GFXCORE

SYSTEM DC/DC TPS51218 86	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_GFX_CORE

CHARGER BQ24745 45	
INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC

SYSTEM DC/DC TPS51218 49	
INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VTT

SYSTEM DC/DC TPS51117 52	
INPUTS	OUTPUTS
+PWR_SRC	+1.05V_PCH

LDO APL5930 51	
INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN

LDO RT9025 87	
INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN_GPU

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Title: Block Diagram

Size	Document Number	Rev
Custom	Vostro Calpella	SA

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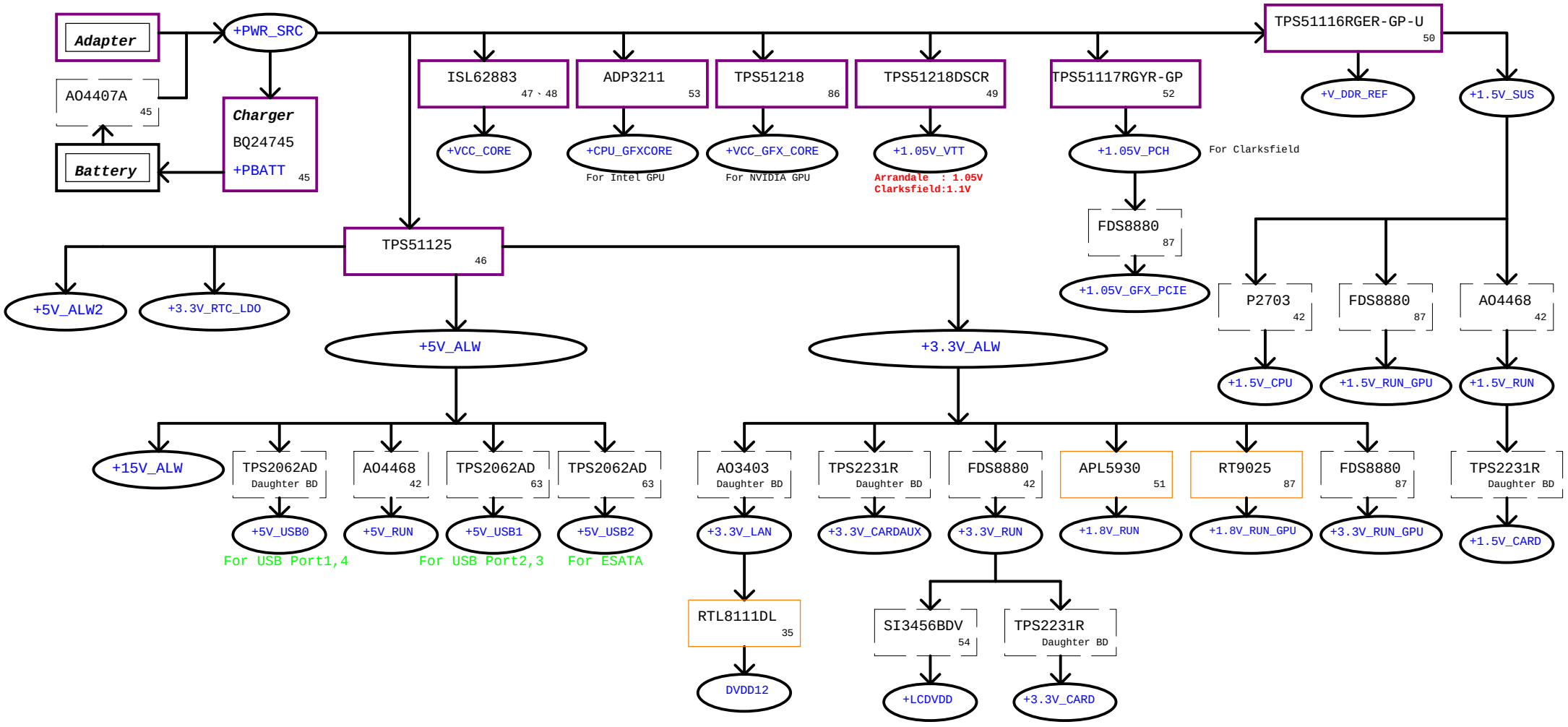

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Title	Power Block Diagram	
Size: Custom	Document Number: Vostro Calpella	Rev: SA
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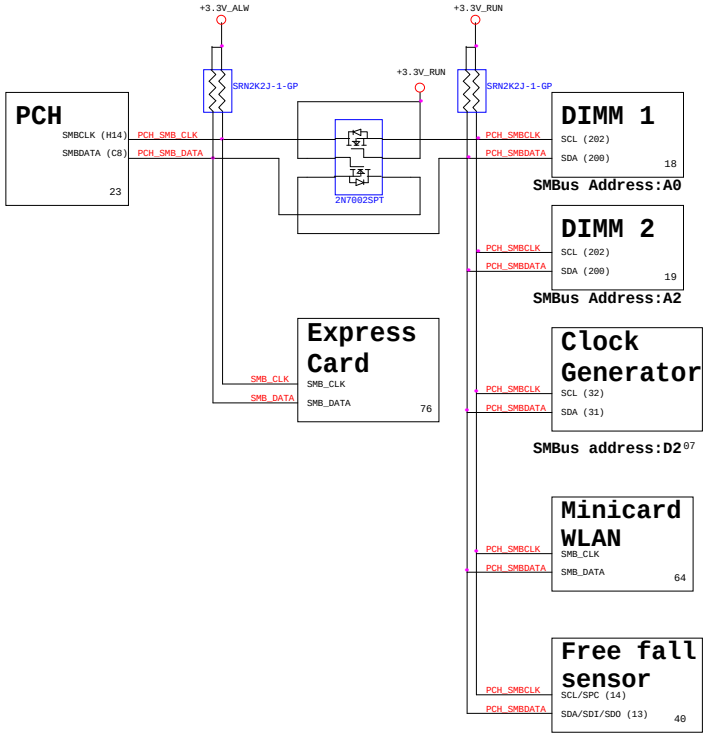
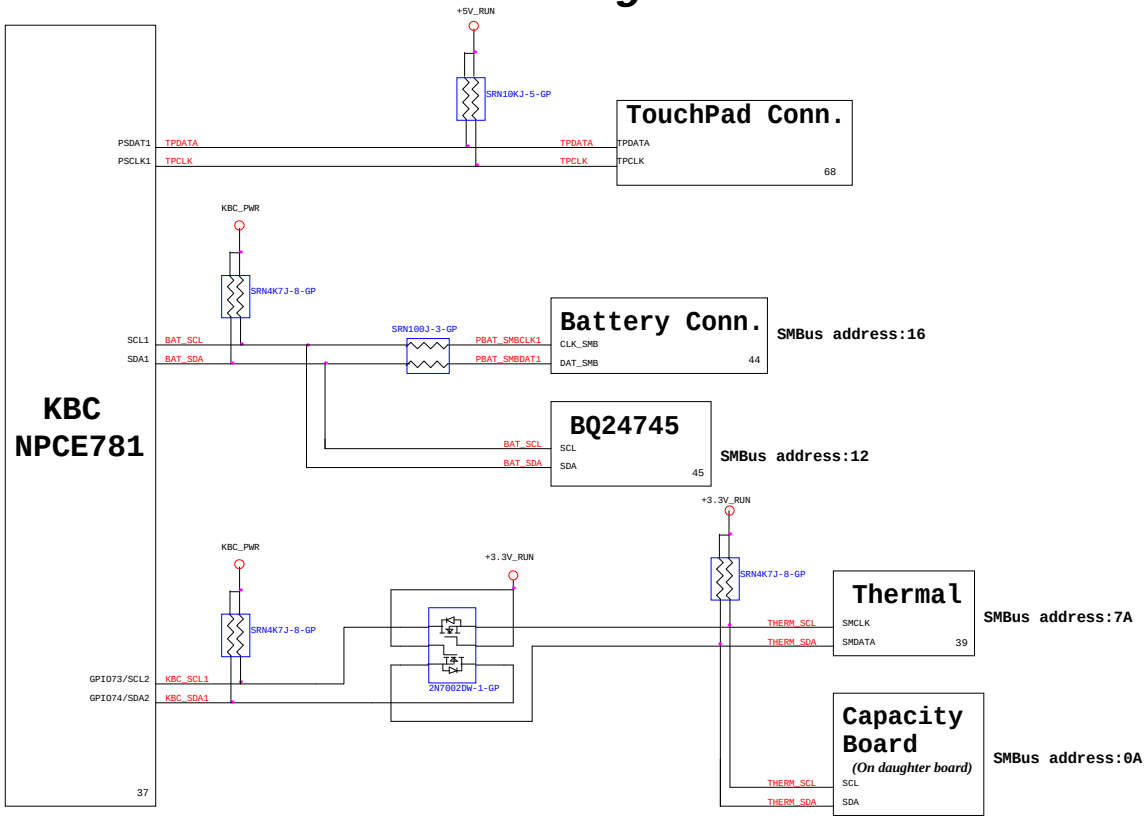
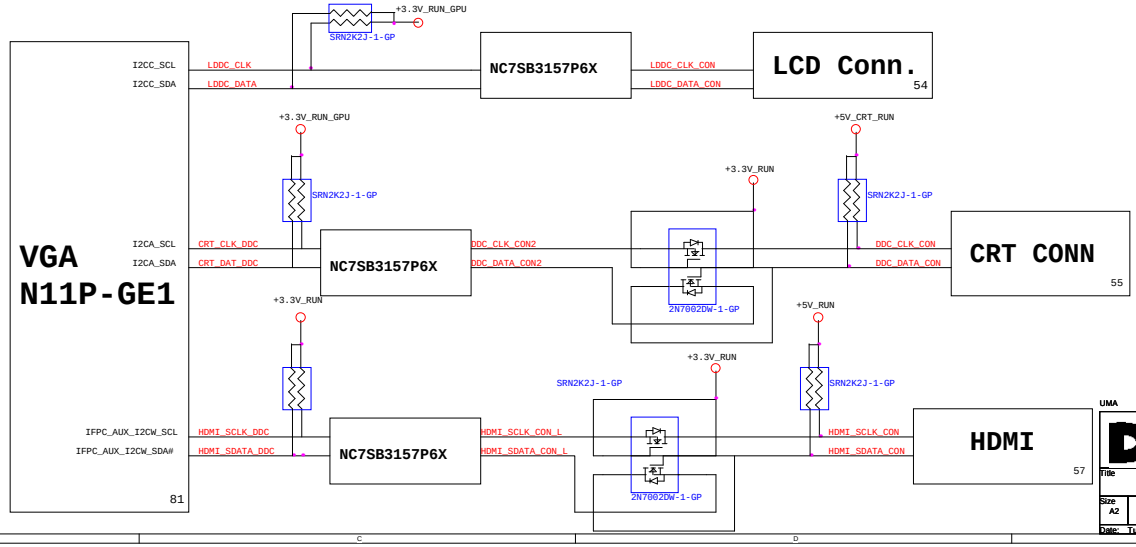
PCH SMBus Block Diagram



KBC SMBus Block Diagram



VGA SMBus Block Diagram



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Title: SMBUS Block Diagram

Size	Document Number	Rev
A2	Vostro Calpella	SA

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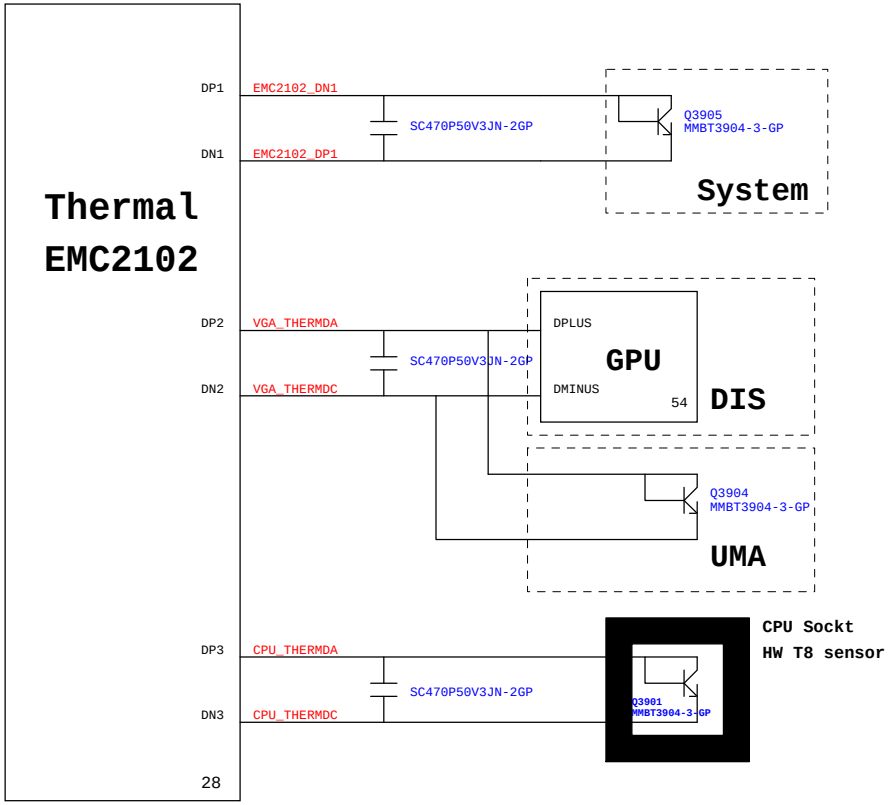
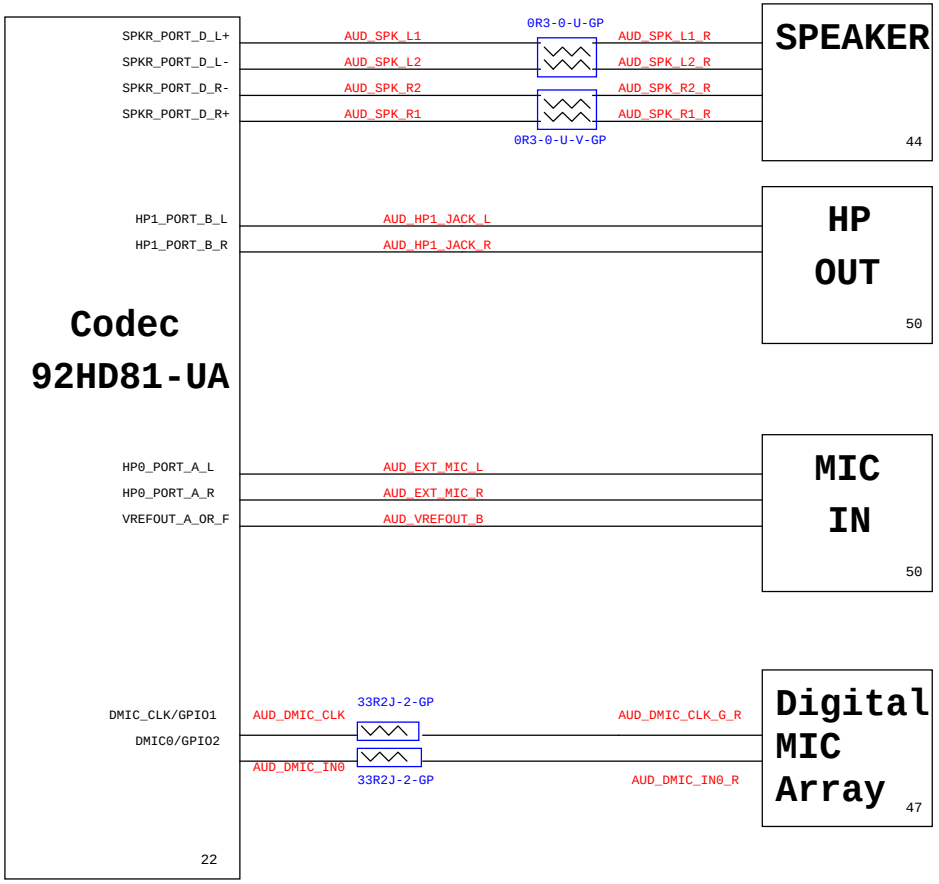
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

Size	Document Number	Rev
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PCH Strapping

Calpella Schematic Checklist Rev.1_6

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Internal pull-up. Leave as "No Connect"
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** Note: Connect to ground with 4.7-kΩ weak pull-down resistor. CRB uses a 1 kΩ; do not stuff resistor.
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled** **Note:** CRB uses a 330-kΩ resistor.
GNT0#, GNT1#	**Default (SPI):** Leave both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default - Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
SPI_MOSI	**Enable Intel Anti-Theft Technology:**Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Intel Anti-Theft Technology:**Left floating, no pull-down required.
NV_ALE	**Enable Intel Anti-Theft Technology:**Connect to +NVRAM_Vccq with 8.2-kΩ weak pull-up resistor.[CRB has it pulled up with 1-kΩ no-stuff resistor] **Disable Intel Anti-Theft Technology:**Leave floating. (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0)-** Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. **High (1)--**Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. CRB recommends 1-kΩ pull-down for FD Override. **Note:** There is an internal pull-up of 20 kΩ for HDA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	**Low (0)-**Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality **High (1)--**Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality **Note:** This is an unmuxed signal. This signal has a weak internal pull-down of 20 KΩ which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kΩ pull-up on this signal to +3.3VA rail.
GPIO8	Weak internal pull-up. Do not pull low. Sampled at rising edge of RSMRST#.
GPIO27	**Default = Do not connect (floating). Internal pull-up.** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Calpella Schematic Checklist Rev.1_6

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connected to the Embedded Display Port.	**1**
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	**1**

PCIE Routing

LANE1	Card reader
LANE2	MiniCard WLAN
LANE3	LAN
LANE4	NC
LANE5	New Card

USB Table

USB	
Pair	Device
0	USB1 > LAN BOARD
1	USB4 > LAN BOARD
2	USB2 > M/B
3	USB3 > M/B
4	USB for ESATA
5	RESERVED
6	RESERVED (Not available for HM55)
7	RESERVED (Not available for HM55)
8	BLUETOOTH
9	Touch Panel
10	Biometric
11	CAMERA
12	New Card
13	WLAN

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Title: Table of Content

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68.00119.131 0603
68.00084.521 0805

+3.3V_RUN
R708 0R3J-0-U-GP
+3.3V_RUN_SL585
C701 SC1U10V2KX-1GP
C702 SC10U10V5ZY-1GP
C703 SC1U10V2KX-4GP
C704 SC1U10V2KX-4GP
C705 SC1U10V2KX-4GP
C707 SC1U10V2KX-4GP
C708 SC1U10V2KX-4GP

+1.05V_PCH
68.00119.131
R709 0R3J-0-U-GP
+1.05V_RUN_SL585_IO
C709 SC1U10V2KX-1GP
C710 SC10U10V5ZY-1GP
C711 SC1U10V2KX-4GP
C712 SC1U10V2KX-4GP

U701
SLG8SP585VTR-GP
VDD_CPU VDD_SRC VDD_REF VDD_DOT VDD_27 VDD_SRC_IO VDD_CPU_IO
GND VSS_REF VSS_CPU VSS_SRC VSS_DOT VSS_27 VSS_SATA

RN701 SRN0J-6-GP
23 DREFCLK#
23 DREFCLK
CLK_MCH_DREFCLK1#
CLK_MCH_DREFCLK1
DOT_96#
DOT_96

RN702 SRN0J-6-GP
23 CLKIN_DMI#
23 CLKIN_DMI
CLK_IN_DMI#
CLK_IN_DMI
SRC_2#
SRC_2

RN703 SRN0J-6-GP
23 CLK_PCIE_SATA#
23 CLK_PCIE_SATA
CLK_PCIE_SATA1#
CLK_PCIE_SATA1
SRC_1/SATA#
SRC_1/SATA

RN704 SRN0J-6-GP
23 CLK_CPU_BCLK#
23 CLK_CPU_BCLK
CLK_CPU_BCLK1#
CLK_CPU_BCLK1
CPU_0#
CPU_0

Do Not Stuff TP0701
Do Not Stuff TP702
TP_CPU_1#
TP_CPU_1
CPU_1#
CPU_1

27MHZ
27MHZ_SS
CLK_27M
CLK_27M_SS
R706 33R2J-2-GP
R710 33R2J-2-GP
CLK_VGA_27M 81

CPU_STOP#
CKPWRGD/PD#
REF_0/CPU_SEL
CPU_STOP#
CK_PWRGD
FSC
R701 2K2R2J-2-GP
R703 33R2J-2-GP
+3.3V_RUN
CLK_PCH_14M 23

XTAL_IN
XTAL_OUT
CLK_XTAL_IN
CLK_XTAL_OUT
EC701 SC4D7P50V2CN-1GP

SDA
SCL
PCH_SMBDATA 18,19,23,40,64
PCH_SMBCLK 18,19,23,40,64

VGA 27M	R706	R710
SS	DY	Mount
NON-SS	Mount	DY

+3.3V_RUN_SL585
R705 10KR2J-3-GP
CK_PWRGD
VR_CLKEN# 47
2N7002A-7-GP
Q701
2009/07/28
Change 2N7002 ESD pretect from standard to 1KV type
P/N:84.2N702.E31

X701 X-14D31818M-37GP
C714 SC12P50V2JN-3GP
C715 SC12P50V2JN-3GP

+1.05V_PCH
R704 4K7R2J-2-GP
R707 10KR2J-3-GP
FSC

FSC	0	1
SPEED	133MHz (Default)	100MHz

2009/07/15
Added R,C For CLK_VGA_27M EMI
CLK_VGA_27M
R749 0R2J-2-GP
CLK_VGA_27M_RC
C718 SC4D7P50V2CN-1GP

1st Silego 71.08585.003
2nd ICS 71.93197.003

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Title: Clock Generator SLG8SP585
Size: Document Number: Vostro Calpella
Rev: SA
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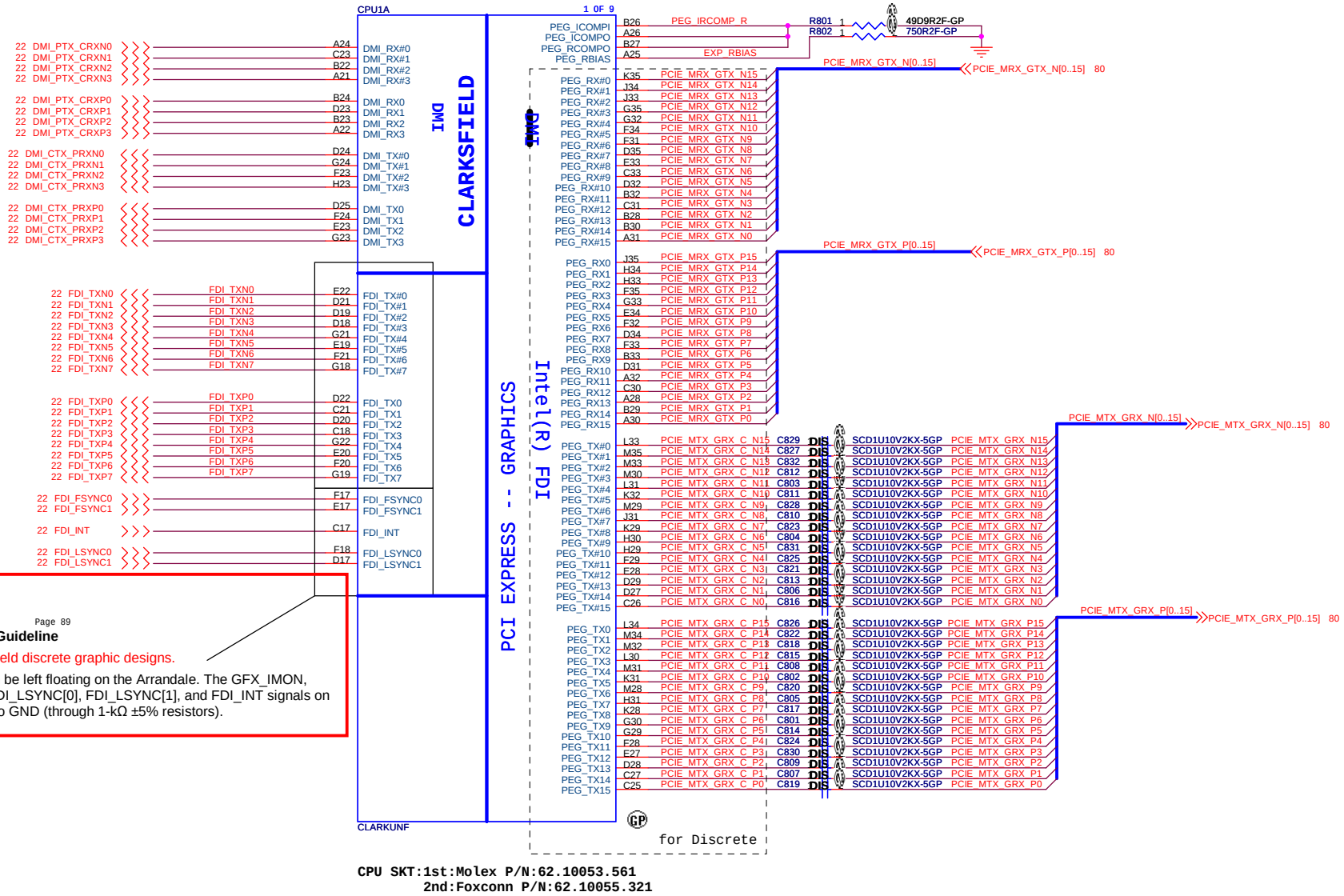

Calpella Platform Design Guide
Revision 1.6

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2.4 Arrandale Graphics Disable Guideline

It applies to Arrandale and Clarksfield discrete graphic designs.

FDI_TX[7:0] and FDI_TX#[7:0] can be left floating on the Arrandale. The GFX_IMON, FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT signals on the Arrandale side should be tied to GND (through 1-kΩ ±5% resistors).

CPU SKT:1st:Molex P/N:62.10053.561
2nd:Foxconn P/N:62.10055.321

UMA

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Title: **CPU (PCIE/DMI/FDI)**

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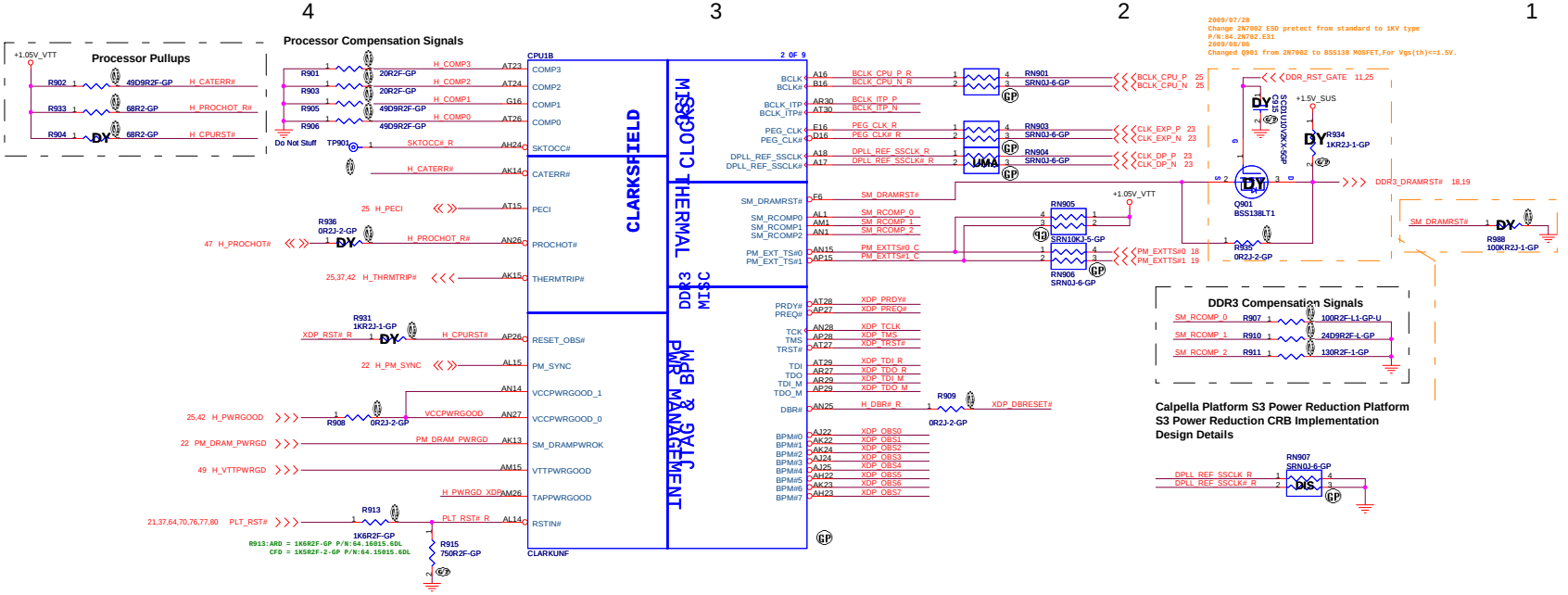
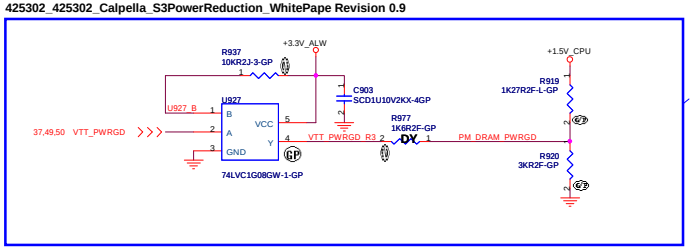


425302_425302_Calpella_S3PowerReduction_WhitePape Revision 0.9



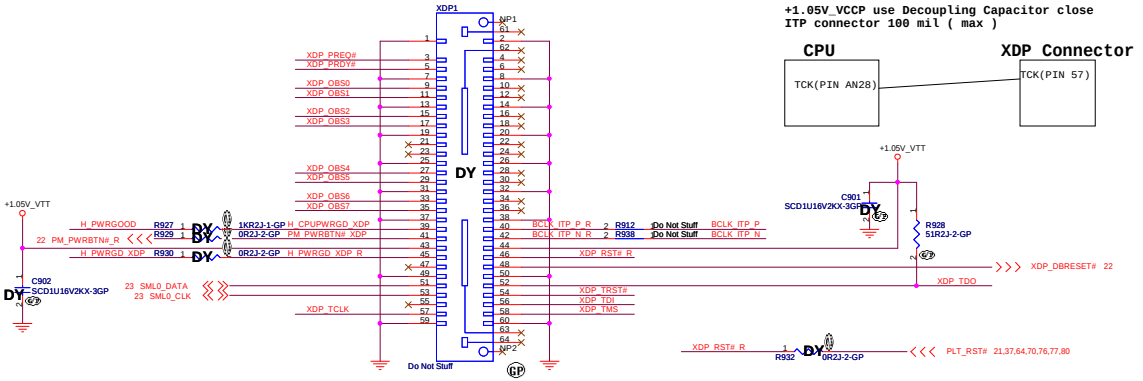
Normal

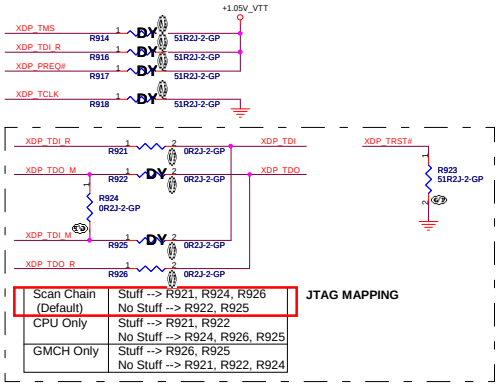
	R919	R920	R977
AUB	1.27k	3k	1.6k(DY)
CFD	1.1k	3k	1.5k(DY)

S3 Power Reduction circuit

	R919	R920	R977
AUB	1.1k(DY)	0.75k	1.6k
CFD	1.1k(DY)	0.75k	1.5k

XDP Connector





Scan Chain (Default)	Stuff --> R921, R924, R926 No Stuff --> R922, R925
CPU Only	Stuff --> R921, R922 No Stuff --> R924, R926, R925
GMCH Only	Stuff --> R926, R925 No Stuff --> R921, R922, R924

JTAG MAPPING

UMA

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Title: CPU (THERMAL/CLOCK/PM)

Size	Document Number	Rev
	Vostro Calpella	SA

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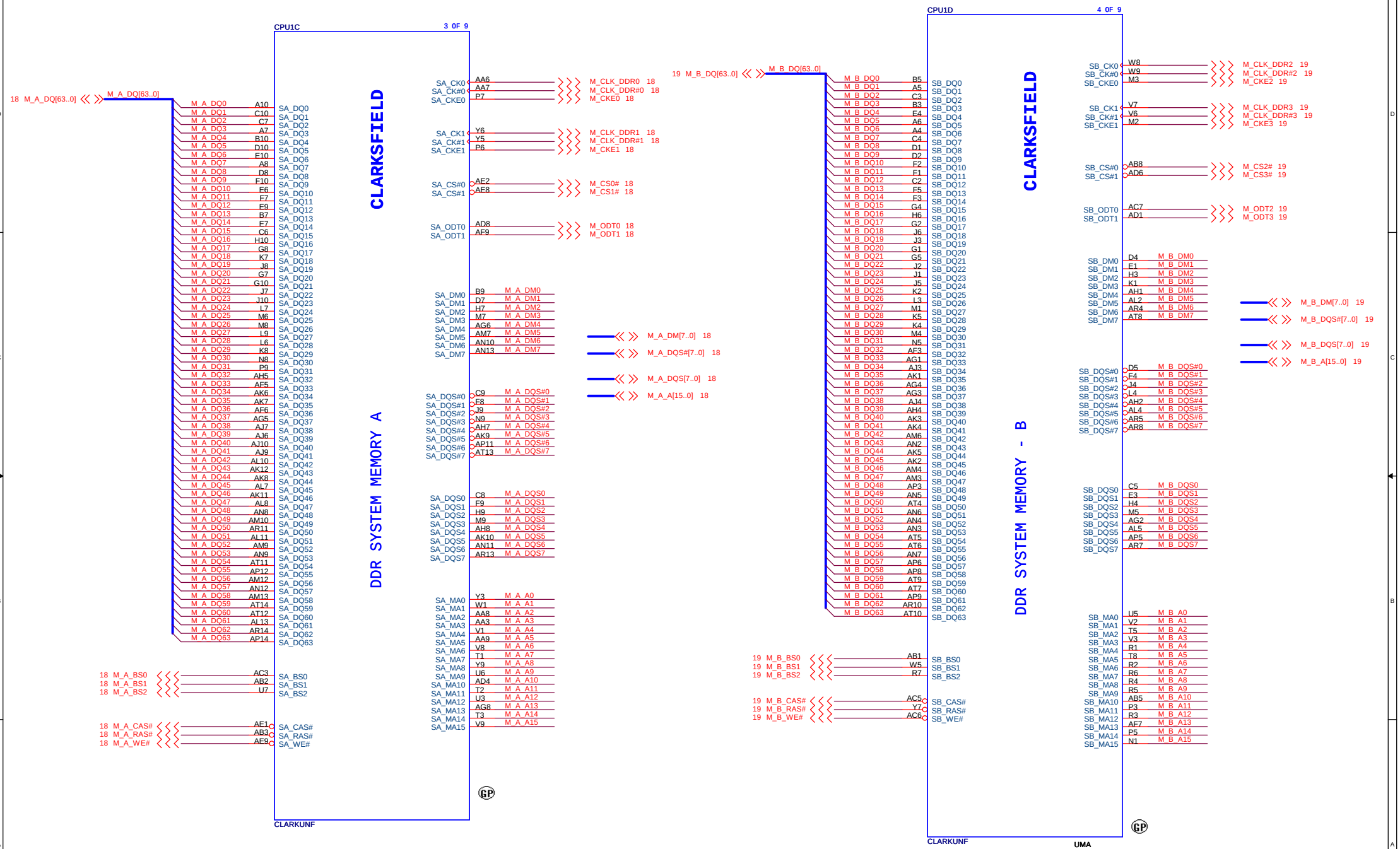

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Title: CPU (DDR)

Size | Document Number: Vostro Calpella | Rev: SA

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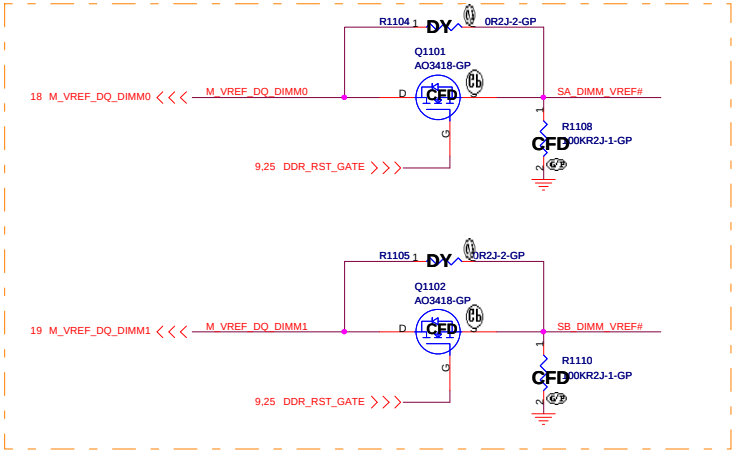
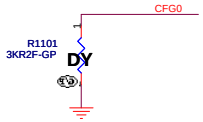
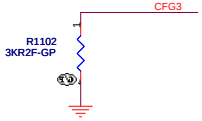


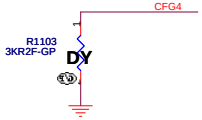


PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

DIS改5%



CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...



CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

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4.8.3.1 LVDS Switching

Switchable GFX, just like integrated GFX only, to enable LVDS it is required that the OEM set the LDVS (L_DDC_DATA) strap to present (pulled up) and the eDP strap (CFG[4]) to disabled (not pulled down).

4.8.3.2 eDP Switching

eDP for Switchable GFX can only be driven out of Port D of PCH. To configure Port D for embedded DP it is required to set the DDPD_CTRLDATA strap high to 3.3V Core rail through 2.2 kΩ ±5% resistor, LVDS (L_DDC_DATA) strap as no connect and the eDP strap CFG[4] as no connect.

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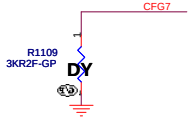
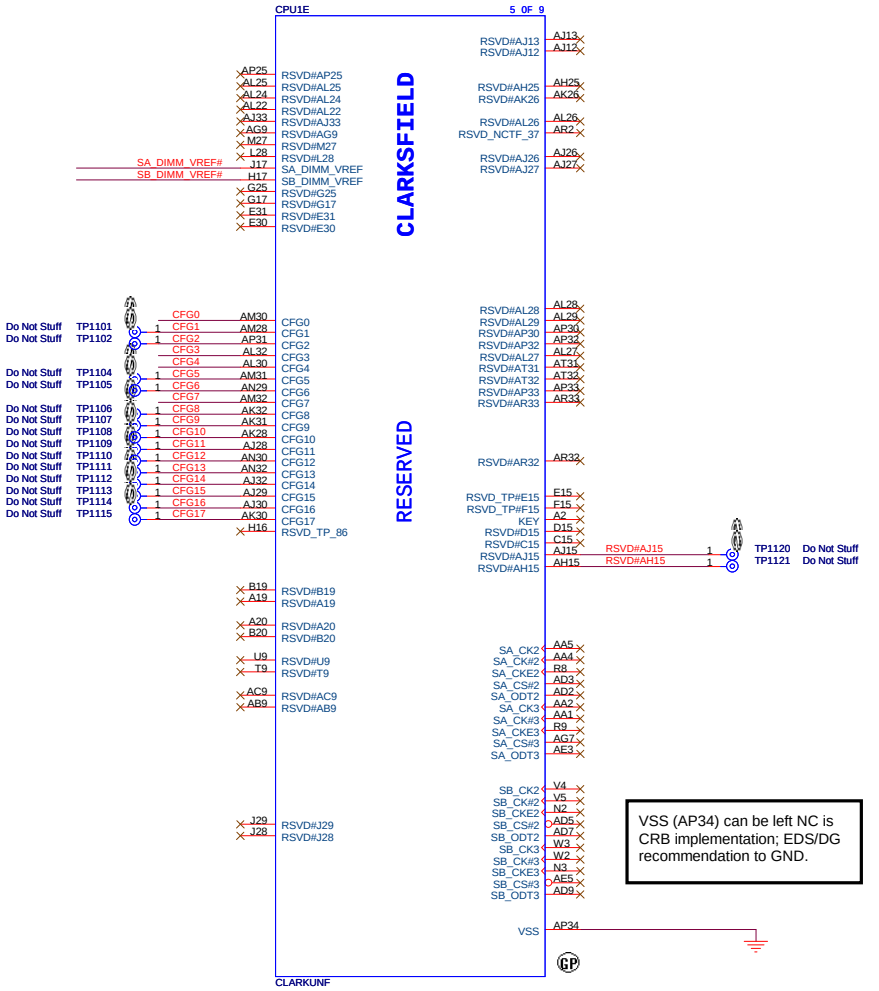


CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality.



VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.

UMA

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Title: **CPU (RESERVED)**

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	Vostro Calpella	SA

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PROCESSOR CORE POWER

Clarksfield = 52A

Arrandale = 48A

+VCC_CORE

CPU1F

6 OF 9

CLARKSFIELD

1.1V RAIL POWER

CPU CORE SUPPLY

CLARKUNF

C1206 C1207 C1208 C1209 C1220 C1210 — SC10U6D3V5MX-3GP

C1212 C1213 C1214 C1215 C1223 C1224 — SC10U6D3V5MX-3GP

C1225 C1226 C1227 C1228 C1229 C1230 C1231 C1232 — SC22U6D3V5MX-2GP / SC10U6D3V5MX-3GP

C1235 C1236 C1237 C1238 C1239 C1240 C1241 C1242 — SC10U6D3V5MX-3GP / SC22U6D3V5MX-2GP

C1243 DY SC10U6D3V5MX-3GP

AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26 AF35 AF34 AF33 AF32 AF31 AF30 AF29 AF28 AF27 AF26 AD35 AD34 AD33 AD32 AD31 AD30 AD29 AD28 AD27 AD26 AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26 AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26 Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26 V35 V34 V33 V32 V31 V30 V29 V28 V27 V26 U35 U34 U33 U32 U31 U30 U29 U28 U27 U26 R35 R34 R33 R32 R31 R30 R29 R28 R27 R26 P35 P34 P33 P32 P31 P30 P29 P28 P27 P26 — VCC

AH14 AH12 AH11 AH10 J14 J13 H14 H12 G14 G13 G12 G11 F14 F13 F12 F11 E14 E12 D14 D13 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11 — VTT0

+1.05V_VTT

C1201 C1202 C1217 C1218 C1204 C1205 — SC10U10V5ZY-1GP

AE10 AE10 AC10 AB10 Y10 W10 U10 T10 J12 J11 J16 J15 — VTT0

C1234 SC10U6D3V5MX-3GP

The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Rail Values are
Arrandale VTT=1.05V;
Clarksfield VTT=1.1V

DIS(Clarksfield +1.05V_VTT) = 14.4A

DIS(Arrandale +1.05V_VTT) = 20.95A

UMA(Arrandale +1.05V_VTT) = 19.84A

POWER

CPU VIDS

PSI# — AN33 — PSI# 47

VID — AK35 CPU_VID0; AK33 CPU_VID1; AK34 CPU_VID2; AL35 CPU_VID3; AL33 CPU_VID4; AM33 CPU_VID5; AM35 CPU_VID6 — CPU_VID[6..0] 47

PROC_DPRSLPVR — AM34 — PM_DPRSLPVR 47

VTT_SELECT — G15 — TP_VTT_SELECT — TP1203 Do Not Stuff

VTT_SELECT = Low, 1.1V
VTT_SELECT = High, 1.05V

SENSE LINES

ISENSE — AN35 — IMVP_IMON 47

VCC_SENSE — AJ34 VCC_SENSE; VSS_SENSE AJ35 — VCC_SENSE 47; VSS_SENSE 47

VTT_SENSE — B15; VSS_SENSE_VTT A15 — TP_VSS_SENSE_VTT — TP1202 Do Not Stuff — VTT_SENSE 49

+VCC_CORE

R1201 100R2F-L1-GP-U

R1204 100R2F-L1-GP-U

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Title: CPU (VCC_CORE)

Size | Document Number: Vostro Calpella | Rev: SA

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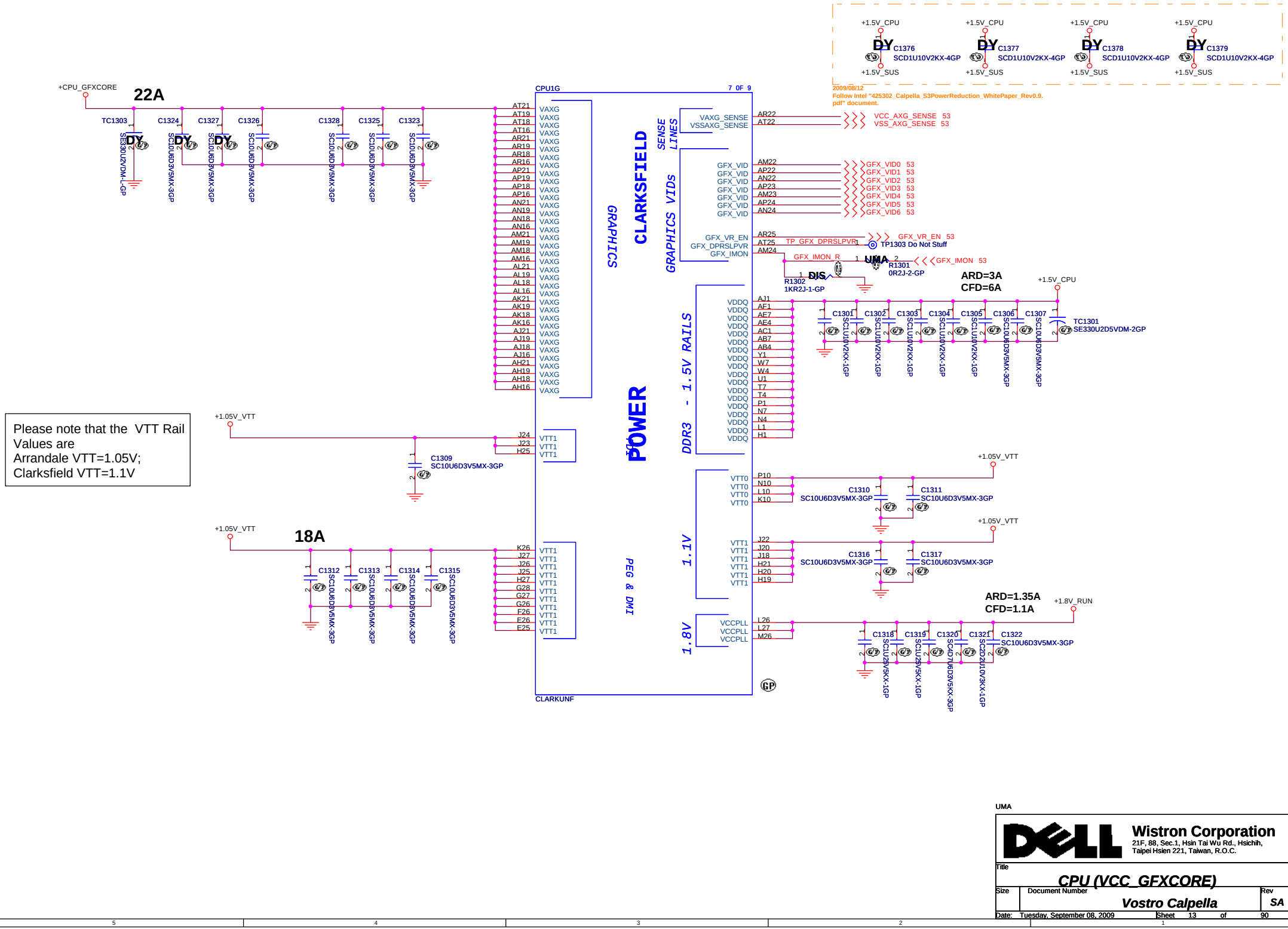
+1.5V_CPU
DY C1376 SCD1U10V2KX-4GP
DY C1377 SCD1U10V2KX-4GP
DY C1378 SCD1U10V2KX-4GP
DY C1379 SCD1U10V2KX-4GP
+1.5V_SUS
2009/08/12
Follow Intel "425302_Calpella_S3PowerReduction_WhitePaper_Rev0.9.pdf" document.
+CPU_GFXCORE
22A
TC1303 SE330U2VDM-L-GP
C1324 C1327 C1326 C1328 C1325 C1323 SC10U6D3V5MX-3GP
CPU1G
7 0F 9
AT21 AT19 AT18 AT16 AR21 AR19 AR18 AR16 AP21 AP19 AP18 AP16 AN21 AN19 AN18 AN16 AM21 AM19 AM18 AM16 AL21 AL19 AL18 AL16 AK21 AK19 AK18 AK16 AJ21 AJ19 AJ18 AJ16 AH21 AH19 AH18 AH16
VAXG
GRAPHICS
CLARKSFIELD
POWER
SENSE LINES
VAXG_SENSE
VSSAXG_SENSE
AR22
AT22
VCC_AXG_SENSE 53
VSS_AXG_SENSE 53
GRAPHICS VIDs
GFX_VID
AM22 AP22 AN22 AP23 AM23 AP24 AN24
GFX_VID0 53
GFX_VID1 53
GFX_VID2 53
GFX_VID3 53
GFX_VID4 53
GFX_VID5 53
GFX_VID6 53
GFX_VR_EN
GFX_DPRSLPVR
GFX_IMON
AR25
AT25
AM24
GFX_VR_EN 53
TP_GFX_DPRSLPVR
TP1303 Do Not Stuff
GFX_IMON_R
UMA
DIS
R1301 0R2J-2-GP
R1302 1KR2J-1-GP
GFX_IMON 53
ARD=3A
CFD=6A
+1.5V_CPU
DDR3 - 1.5V RAILS
VDDQ
AJ1 AF1 AE7 AE4 AC1 AB7 AB4 Y1 W7 W4 U1 T7 T4 P1 N7 N4 L1 H1
C1301 C1302 C1303 C1304 C1305 C1306 C1307 SC10U6D3V5MX-3GP
TC1301 SE330U2D5VDM-2GP
+1.05V_VTT
J24 J23 H25
VTT1
C1309 SC10U6D3V5MX-3GP
1.1V
VTT0
P10 N10 L10 K10
C1310 C1311 SC10U6D3V5MX-3GP
VTT1
J22 J20 J18 H21 H20 H19
C1316 C1317 SC10U6D3V5MX-3GP
18A
K26 J27 J26 J25 H27 G28 G27 G26 F26 E26 E25
C1312 C1313 C1314 C1315 SC10U6D3V5MX-3GP
PEG & DMI
1.8V
VCCPLL
L26 L27 M26
+1.8V_RUN
ARD=1.35A
CFD=1.1A
C1318 C1319 C1320 C1321 C1322
SC1U25V5KX-1GP
SC4D7U6D3V5KX-3GP
SC2D2U10V3KX-1GP
SC10U6D3V5MX-3GP
CLARKUNF
Please note that the VTT Rail Values are
Arrandale VTT=1.05V;
Clarksfield VTT=1.1V
UMA
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Title
CPU (VCC_GFXCORE)
Size
Document Number
Vostro Calpella
Rev
SA
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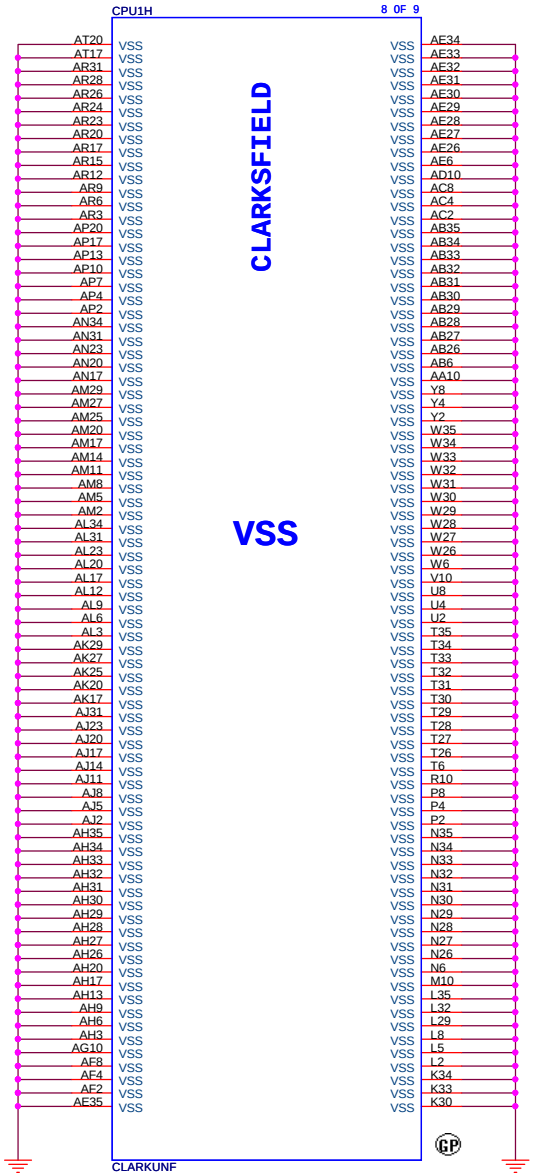

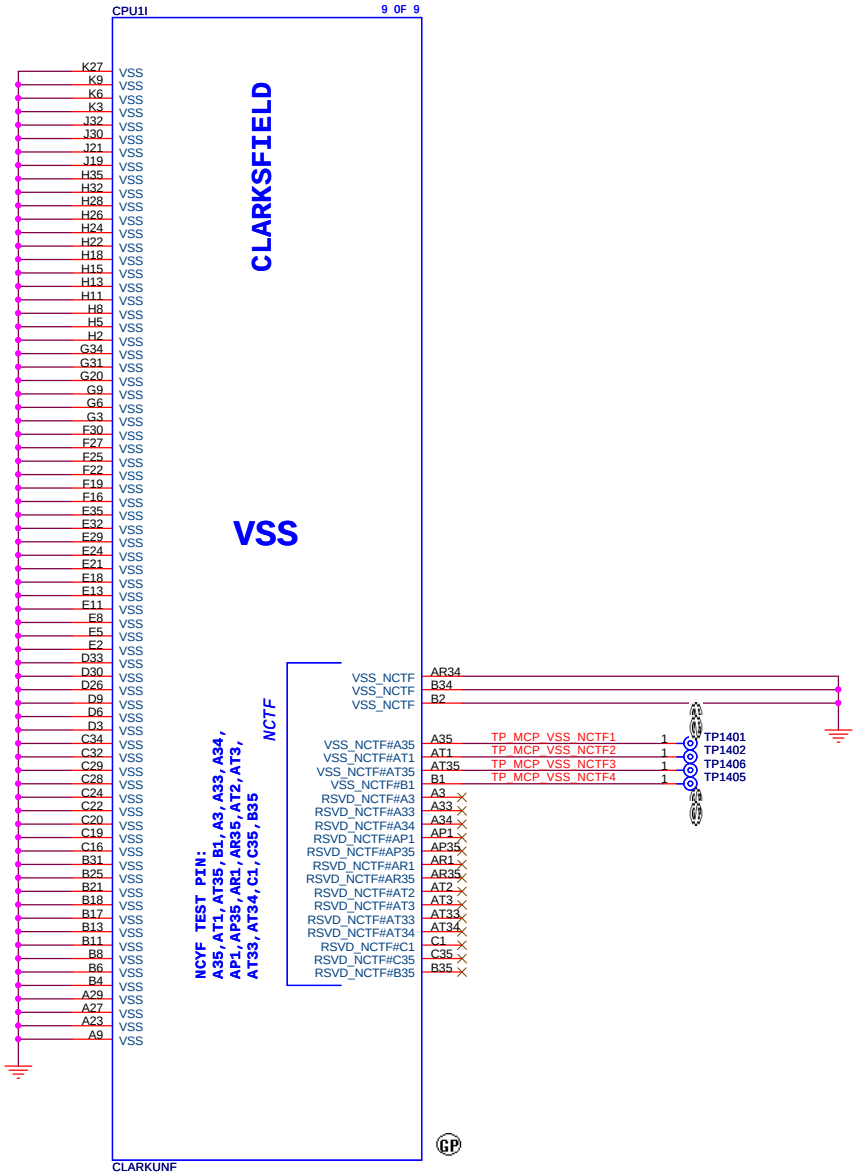

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Title	***CPU (VSS)***	
Size	Document Number: ***Vostro Calpella***	Rev: ***SA***
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Title: *Reserved*

Size: A3 | Document Number: *Vostro Calpella* | Rev: *SA*

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Title: *Reserved*

Size	Document Number	Rev
A3	*Vostro Calpella*	*SA*

(Blank)

UMA

Wistron Corporation
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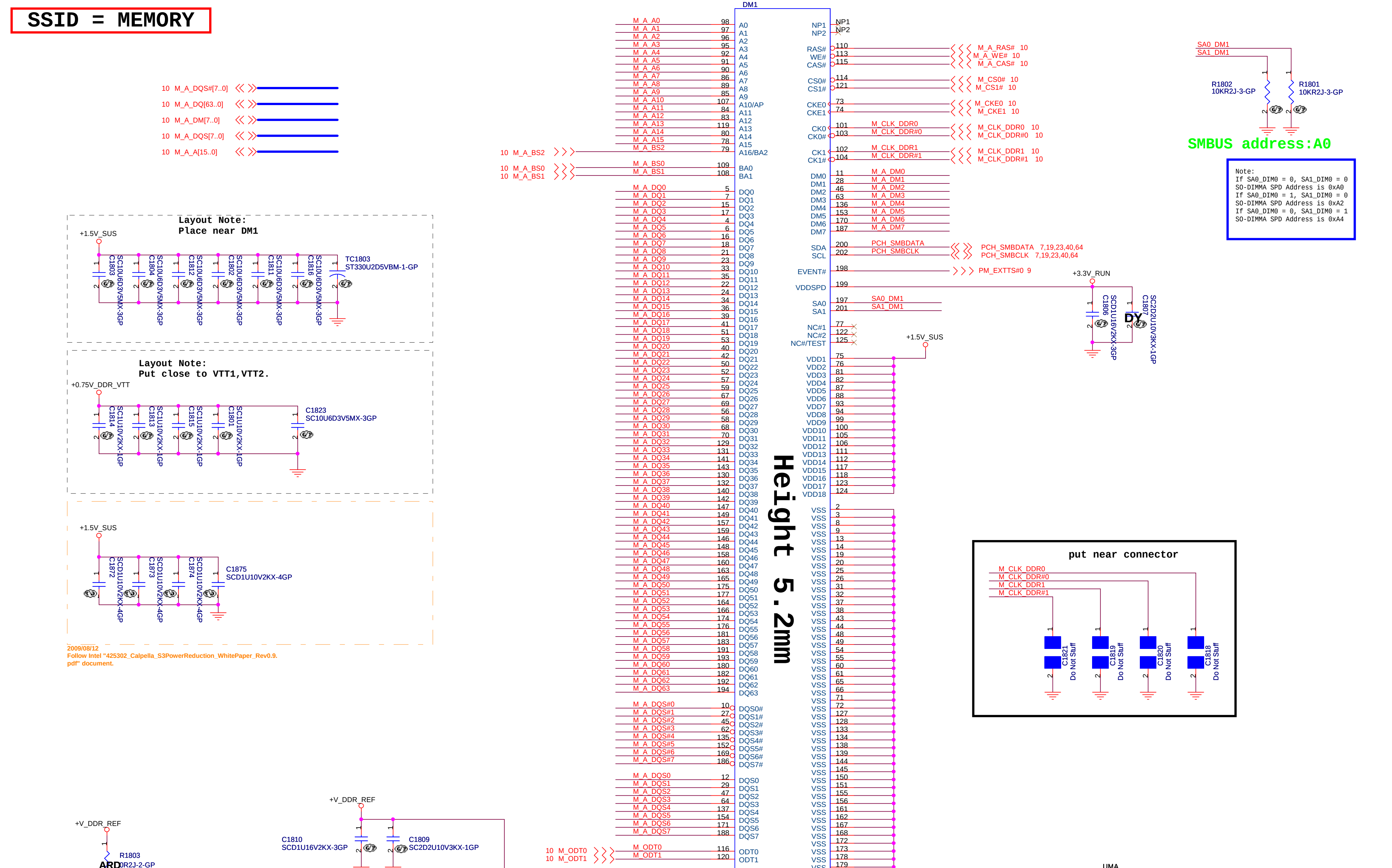
Title: *(Reserve)*

Size: A3 | Document Number: *Vostro Calpella* | Rev: *SA*

Date: Tuesday, September 08, 2009 | Sheet 17 of 90


SSID = MEMORY
10 M_A_DQS#[7..0]
10 M_A_DQ[63..0]
10 M_A_DM[7..0]
10 M_A_DQS[7..0]
10 M_A_A[15..0]
Layout Note:
Place near DM1
+1.5V_SUS
C1803 SC10U6D3V5MX-3GP
C1804 SC10U6D3V5MX-3GP
C1812 SC10U6D3V5MX-3GP
C1802 SC10U6D3V5MX-3GP
C1811 SC10U6D3V5MX-3GP
C1816 SC10U6D3V5MX-3GP
TC1803
ST330U2D5VBM-1-GP
Layout Note:
Put close to VTT1,VTT2.
+0.75V_DDR_VTT
C1814 SC1U10V2KX-1GP
C1813 SC1U10V2KX-1GP
C1815 SC1U10V2KX-1GP
C1801 SC1U10V2KX-1GP
C1823
SC10U6D3V5MX-3GP
+1.5V_SUS
C1872 SCD1U10V2KX-4GP
C1873 SCD1U10V2KX-4GP
C1874 SCD1U10V2KX-4GP
C1875
SCD1U10V2KX-4GP
2009/08/12
Follow Intel "425302_Calpella_S3PowerReduction_WhitePaper_Rev0.9.
pdf" document.
+V_DDR_REF
R1803
ARD
0R2J-2-GP
C1817
SCD1U16V2KX-3GP
C1805
SC2D2U10V3KX-1GP
M_VREF_DQ_DIMM0 11
+V_DDR_REF
C1810
SCD1U16V2KX-3GP
C1809
SC2D2U10V3KX-1GP
DM1
M_A_A0 98 A0
M_A_A1 97 A1
M_A_A2 96 A2
M_A_A3 95 A3
M_A_A4 92 A4
M_A_A5 91 A5
M_A_A6 90 A6
M_A_A7 86 A7
M_A_A8 89 A8
M_A_A9 85 A9
M_A_A10 107 A10/AP
M_A_A11 84 A11
M_A_A12 83 A12
M_A_A13 119 A13
M_A_A14 80 A14
M_A_A15 78 A15
10 M_A_BS2 M_A_BS2 79 A16/BA2
10 M_A_BS0 M_A_BS0 109 BA0
10 M_A_BS1 M_A_BS1 108 BA1
M_A_DQ0 5 DQ0
M_A_DQ1 7 DQ1
M_A_DQ2 15 DQ2
M_A_DQ3 17 DQ3
M_A_DQ4 4 DQ4
M_A_DQ5 6 DQ5
M_A_DQ6 16 DQ6
M_A_DQ7 18 DQ7
M_A_DQ8 21 DQ8
M_A_DQ9 23 DQ9
M_A_DQ10 33 DQ10
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M_A_DQ16 39 DQ16
M_A_DQ17 41 DQ17
M_A_DQ18 51 DQ18
M_A_DQ19 53 DQ19
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M_A_DQ21 42 DQ21
M_A_DQ22 50 DQ22
M_A_DQ23 52 DQ23
M_A_DQ24 57 DQ24
M_A_DQ25 59 DQ25
M_A_DQ26 67 DQ26
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M_A_DQ39 142 DQ39
M_A_DQ40 147 DQ40
M_A_DQ41 149 DQ41
M_A_DQ42 157 DQ42
M_A_DQ43 159 DQ43
M_A_DQ44 146 DQ44
M_A_DQ45 148 DQ45
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M_A_DQ47 160 DQ47
M_A_DQ48 163 DQ48
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M_A_DQ58 191 DQ58
M_A_DQ59 193 DQ59
M_A_DQ60 180 DQ60
M_A_DQ61 182 DQ61
M_A_DQ62 192 DQ62
M_A_DQ63 194 DQ63
M_A_DQS#0 10 DQS0#
M_A_DQS#1 27 DQS1#
M_A_DQS#2 45 DQS2#
M_A_DQS#3 62 DQS3#
M_A_DQS#4 135 DQS4#
M_A_DQS#5 152 DQS5#
M_A_DQS#6 169 DQS6#
M_A_DQS#7 186 DQS7#
M_A_DQS0 12 DQS0
M_A_DQS1 29 DQS1
M_A_DQS2 47 DQS2
M_A_DQS3 64 DQS3
M_A_DQS4 137 DQS4
M_A_DQS5 154 DQS5
M_A_DQS6 171 DQS6
M_A_DQS7 188 DQS7
10 M_ODT0 M_ODT0 116 ODT0
10 M_ODT1 M_ODT1 120 ODT1
126 VREF_CA
M_VREF_DQ_DIMM0 1 VREF_DQ
9,19 DDR3_DRAMRST# 30 RESET#
+0.75V_DDR_VTT 203 VTT1
204 VTT2
Height 5.2mm
NP1 NP1
NP2 NP2
RAS# 110 M_A_RAS# 10
WE# 113 M_A_WE# 10
CAS# 115 M_A_CAS# 10
CS0# 114 M_CS0# 10
CS1# 121 M_CS1# 10
CKE0 73 M_CKE0 10
CKE1 74 M_CKE1 10
CK0 101 M_CLK_DDR0 M_CLK_DDR0 10
CK0# 103 M_CLK_DDR#0 M_CLK_DDR#0 10
CK1 102 M_CLK_DDR1 M_CLK_DDR1 10
CK1# 104 M_CLK_DDR#1 M_CLK_DDR#1 10
DM0 11 M_A_DM0
DM1 28 M_A_DM1
DM2 46 M_A_DM2
DM3 63 M_A_DM3
DM4 136 M_A_DM4
DM5 153 M_A_DM5
DM6 170 M_A_DM6
DM7 187 M_A_DM7
SDA 200 PCH_SMBDATA PCH_SMBDATA 7,19,23,40,64
SCL 202 PCH_SMBCLK PCH_SMBCLK 7,19,23,40,64
EVENT# 198 PM_EXTTS#0 9
VDDSPD 199 +3.3V_RUN
SA0 197 SA0_DM1
SA1 201 SA1_DM1
NC#1 77
NC#2 122
NC#/TEST 125
+1.5V_SUS
VDD1 75 VDD2 76 VDD3 81 VDD4 82 VDD5 87 VDD6 88 VDD7 93 VDD8 94 VDD9 99 VDD10 100 VDD11 105 VDD12 106 VDD13 111 VDD14 112 VDD15 117 VDD16 118 VDD17 123 VDD18 124
VSS 2 3 8 9 13 14 19 20 25 26 31 32 37 38 43 44 48 49 54 55 60 61 65 66 71 72 127 128 133 134 138 139 144 145 150 151 155 156 161 162 167 168 172 173 178 179 184 185 189 190 195 196 205 206
DDR3-204P-25-GP
62.10017.K11
C1806 SCD1U16V2KX-3GP
C1807 SC2D2U10V3KX-1GP
DY
2009/07/30
Change connector to 62.10017.K11
SA0_DM1
SA1_DM1
R1802
10KR2J-3-GP
R1801
10KR2J-3-GP
SMBUS address:A0
Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
If SA0_DIM0 = 0, SA1_DIM0 = 1
SO-DIMMA SPD Address is 0xA4
put near connector
M_CLK_DDR0
M_CLK_DDR#0
M_CLK_DDR1
M_CLK_DDR#1
C1821 Do Not Stuff
C1819 Do Not Stuff
C1820 Do Not Stuff
C1818 Do Not Stuff

UMA

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Title: DDRIII-SODIMM SLOT1		
Size: Custom	Document Number: Vostro Calpella	Rev: SA
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SSID = MEMORY

10 M_B_DQS#[7..0]
10 M_B_DQ[63..0]
10 M_B_DM[7..0]
10 M_B_DQS[7..0]
10 M_B_A[15..0]

Layout Note:
Place near DM2

+1.5V_SUS

C1919 SC10U6D3V5MX-3GP
C1905 SC10U6D3V5MX-3GP
C1911 SC10U6D3V5MX-3GP
C1916 SC10U6D3V5MX-3GP
C1913 SC10U6D3V5MX-3GP
C1920 SC10U6D3V5MX-3GP
TC1903 ST330U2D5VBM-1-GP

Layout Note:
Put close to VTT1,VTT2.

+0.75V_DDR_VTT

C1908 SC1U10V2KX-1GP
C1917 SC1U10V2KX-1GP
C1909 SC1U10V2KX-1GP
C1918 SC1U10V2KX-1GP

+1.5V_SUS

C1976 SCD1U10V2KX-4GP
C1977 SCD1U10V2KX-4GP
C1978 SCD1U10V2KX-4GP
C1979 SCD1U10V2KX-4GP

2009/08/12
Follow Intel "425302_Calpella_S3PowerReduction_WhitePaper_Rev0.9. pdf" document.

+V_DDR_REF

R1905 ARD 0R2J-2-GP
C1910 SCD1U16V2KX-3GP
C1912 SC2D2U10V3KX-1GP
M_VREF_DQ_DIMM1 11

+V_DDR_REF

C1907 SCD1U16V2KX-3GP
C1914 SC2D2U10V3KX-1GP
M_VREF_DQ_DIMM1

DM2

M_B_A0	98	A0	
M_B_A1	97	A1	
M_B_A2	96	A2	
M_B_A3	95	A3	
M_B_A4	92	A4	
M_B_A5	91	A5	
M_B_A6	90	A6	
M_B_A7	86	A7	
M_B_A8	89	A8	
M_B_A9	85	A9	
M_B_A10	107	A10/AP	
M_B_A11	84	A11	
M_B_A12	83	A12	
M_B_A13	119	A13	
M_B_A14	80	A14	
M_B_A15	78	A15	
10 M_B_BS2 / M_B_BS0	79 / 109	A16/BA2 / BA0	
10 M_B_BS0 / 10 M_B_BS1	109 / 108	BA0 / BA1	
M_B_DQ0	5	DQ0	
M_B_DQ1	7	DQ1	
M_B_DQ2	15	DQ2	
M_B_DQ3	17	DQ3	
M_B_DQ4	4	DQ4	
M_B_DQ5	6	DQ5	
M_B_DQ6	16	DQ6	
M_B_DQ7	18	DQ7	
M_B_DQ8	21	DQ8	
M_B_DQ9	23	DQ9	
M_B_DQ10	33	DQ10	
M_B_DQ11	35	DQ11	
M_B_DQ12	22	DQ12	
M_B_DQ13	24	DQ13	
M_B_DQ14	34	DQ14	
M_B_DQ15	36	DQ15	
M_B_DQ16	39	DQ16	
M_B_DQ17	41	DQ17	
M_B_DQ18	51	DQ18	
M_B_DQ19	53	DQ19	
M_B_DQ20	40	DQ20	
M_B_DQ21	42	DQ21	
M_B_DQ22	50	DQ22	
M_B_DQ23	52	DQ23	
M_B_DQ24	57	DQ24	
M_B_DQ25	59	DQ25	
M_B_DQ26	67	DQ26	
M_B_DQ27	69	DQ27	
M_B_DQ28	56	DQ28	
M_B_DQ29	58	DQ29	
M_B_DQ30	68	DQ30	
M_B_DQ31	70	DQ31	
M_B_DQ32	129	DQ32	
M_B_DQ33	131	DQ33	
M_B_DQ34	141	DQ34	
M_B_DQ35	143	DQ35	
M_B_DQ36	130	DQ36	
M_B_DQ37	132	DQ37	
M_B_DQ38	140	DQ38	
M_B_DQ39	142	DQ39	
M_B_DQ40	147	DQ40	
M_B_DQ41	149	DQ41	
M_B_DQ42	157	DQ42	
M_B_DQ43	159	DQ43	
M_B_DQ44	146	DQ44	
M_B_DQ45	148	DQ45	
M_B_DQ46	158	DQ46	
M_B_DQ47	160	DQ47	
M_B_DQ48	163	DQ48	
M_B_DQ49	165	DQ49	
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M_B_DQ51	177	DQ51	
M_B_DQ52	164	DQ52	
M_B_DQ53	166	DQ53	
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M_B_DQ55	176	DQ55	
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M_B_DQ57	183	DQ57	
M_B_DQ58	191	DQ58	
M_B_DQ59	193	DQ59	
M_B_DQ60	180	DQ60	
M_B_DQ61	182	DQ61	
M_B_DQ62	192	DQ62	
M_B_DQ63	194	DQ63	
M_B_DQS#0	10	DQS0#	
M_B_DQS#1	27	DQS1#	
M_B_DQS#2	45	DQS2#	
M_B_DQS#3	62	DQS3#	
M_B_DQS#4	135	DQS4#	
M_B_DQS#5	152	DQS5#	
M_B_DQS#6	169	DQS6#	
M_B_DQS#7	186	DQS7#	
M_B_DQS0	12	DQS0	
M_B_DQS1	29	DQS1	
M_B_DQS2	47	DQS2	
M_B_DQS3	64	DQS3	
M_B_DQS4	137	DQS4	
M_B_DQS5	154	DQS5	
M_B_DQS6	171	DQS6	
M_B_DQS7	188	DQS7	
10 M_ODT2	116	ODT0	
10 M_ODT3	120	ODT1	
M_VREF_DQ_DIMM1	126	VREF_CA	
	1	VREF_DQ	
9,18 DDR3_DRAMRST#	30	RESET#	
+0.75V_DDR_VTT	203	VTT1	
	204	VTT2	

	NP1	NP1	
	NP2	NP2	
RAS#	110	M_B_RAS# 10	
WE#	113	M_B_WE# 10	
CAS#	115	M_B_CAS# 10	
CS0#	114	M_CS2# 10	
CS1#	121	M_CS3# 10	
CKE0	73	M_CKE2 10	
CKE1	74	M_CKE3 10	
CK0	101	M_CLK_DDR2 / M_CLK_DDR2 10	
CK0#	103	M_CLK_DDR#2 / M_CLK_DDR#2 10	
CK1	102	M_CLK_DDR3 / M_CLK_DDR3 10	
CK1#	104	M_CLK_DDR#3 / M_CLK_DDR#3 10	
DM0	11	M_B_DM0	
DM1	28	M_B_DM1	
DM2	46	M_B_DM2	
DM3	63	M_B_DM3	
DM4	136	M_B_DM4	
DM5	153	M_B_DM5	
DM6	170	M_B_DM6	
DM7	187	M_B_DM7	
SDA	200	PCH_SMBDATA / PCH_SMBDATA 7,18,23,40,64	
SCL	202	PCH_SMBCLK / PCH_SMBCLK 7,18,23,40,64	
EVENT#	198	PM_EXTTS#1 9	
VDDSPD	199		
SA0	197	SA0_DM2	
SA1	201	SA1_DM2	
NC#1	77		
NC#2	122		
NC#/TEST	125		
+1.5V_SUS			
VDD1	75		
VDD2	76		
VDD3	81		
VDD4	82		
VDD5	87		
VDD6	88		
VDD7	93		
VDD8	94		
VDD9	99		
VDD10	100		
VDD11	105		
VDD12	106		
VDD13	111		
VDD14	112		
VDD15	117		
VDD16	118		
VDD17	123		
VDD18	124		
VSS	2		
VSS	3		
VSS	8		
VSS	9		
VSS	13		
VSS	14		
VSS	19		
VSS	20		
VSS	25		
VSS	26		
VSS	31		
VSS	32		
VSS	37		
VSS	38		
VSS	43		
VSS	44		
VSS	48		
VSS	49		
VSS	54		
VSS	55		
VSS	60		
VSS	61		
VSS	65		
VSS	66		
VSS	71		
VSS	72		
VSS	127		
VSS	128		
VSS	133		
VSS	134		
VSS	138		
VSS	139		
VSS	144		
VSS	145		
VSS	150		
VSS	151		
VSS	155		
VSS	156		
VSS	161		
VSS	162		
VSS	167		
VSS	168		
VSS	172		
VSS	173		
VSS	178		
VSS	179		
VSS	184		
VSS	185		
VSS	189		
VSS	190		
VSS	195		
VSS	196		
VSS	205		
VSS	206		

Height 9.2mm

DDR3-204P-24-GP
62.10017.K01

2009/07/30
Change connector to 62.10017.K01

+3.3V_RUN

R1903 10KR2J-3-GP DY
R1904 10KR2J-3-GP
SA1_DM2
SA0_DM2
R1901 10KR2J-3-GP
R1902 10KR2J-3-GP DY

SMBUS address:A4

+3.3V_RUN

C1906 SCD1U16V2KX-3GP DY
C1921 SC2D2U10V3KX-1GP

put near connector

M_CLK_DDR2
M_CLK_DDR#2
M_CLK_DDR3
M_CLK_DDR#3

C1901 Do Not Stuff
C1904 Do Not Stuff
C1902 Do Not Stuff
C1903 Do Not Stuff

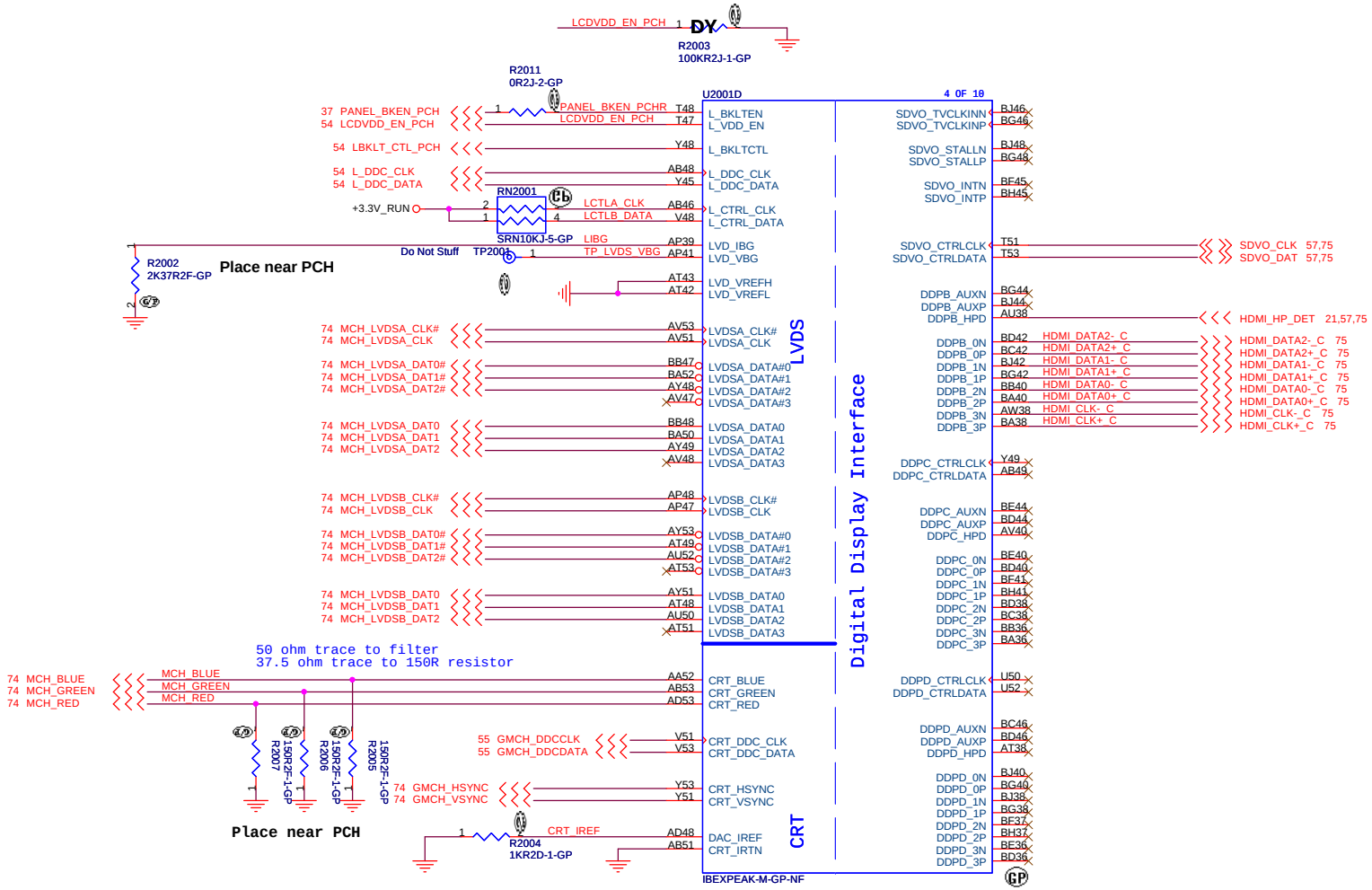
UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDRIII-SODIMM SLOT2

Size: Custom | Document Number: Vostro Calpella | Rev: SA

Date: Tuesday, September 08, 2009 | Sheet 19 of 90



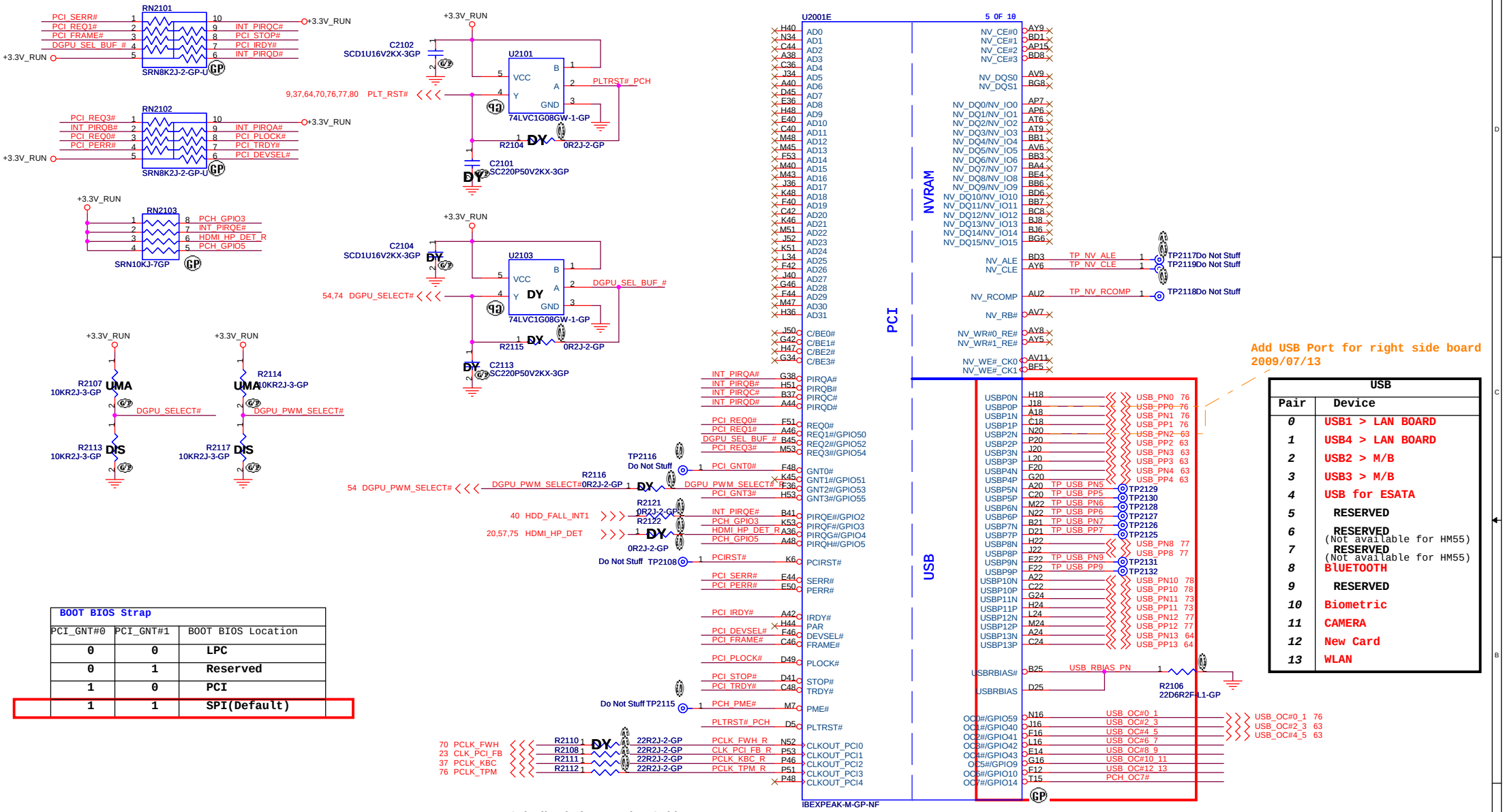
UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (LVDS/CRT/DDI)**

Size | Document Number: **Vostro Calpella** | Rev: **SA**

Date: Tuesday, September 08, 2009 | Sheet 20 of 90



Calpella Platform Design Guide
Revision 1.6

Table 111. Overcurrent Pin Example Configuration

These OC7# pins are not used for USB overcurrent protection and should be configured as GPIOs. The unused USB ports can be left as no connect.

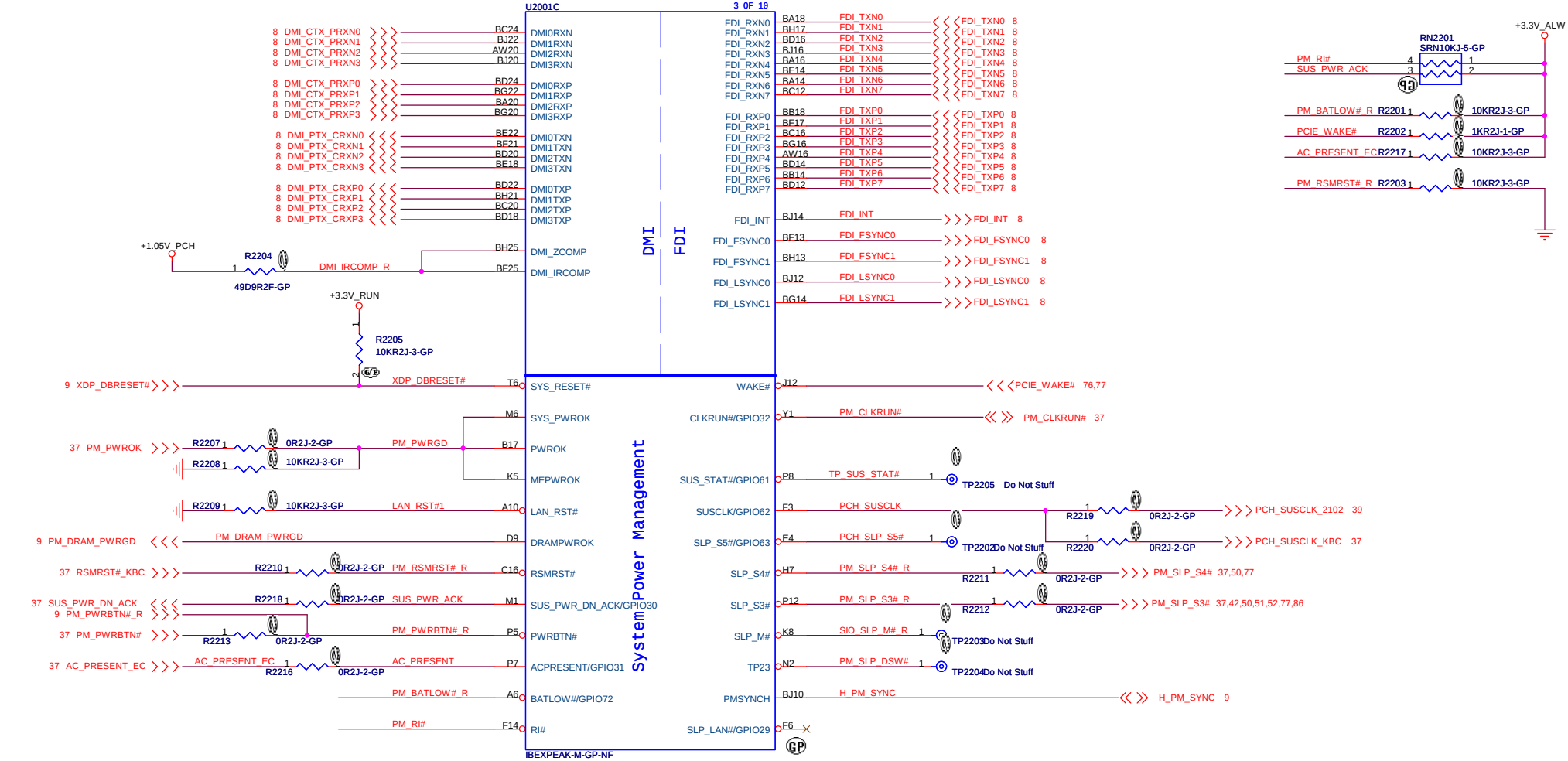
UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI/USB/NVRAM)

Size | Document Number: Vostro Calpella | Rev: SA

Date: Tuesday, September 08, 2009 | Sheet 21 of 90



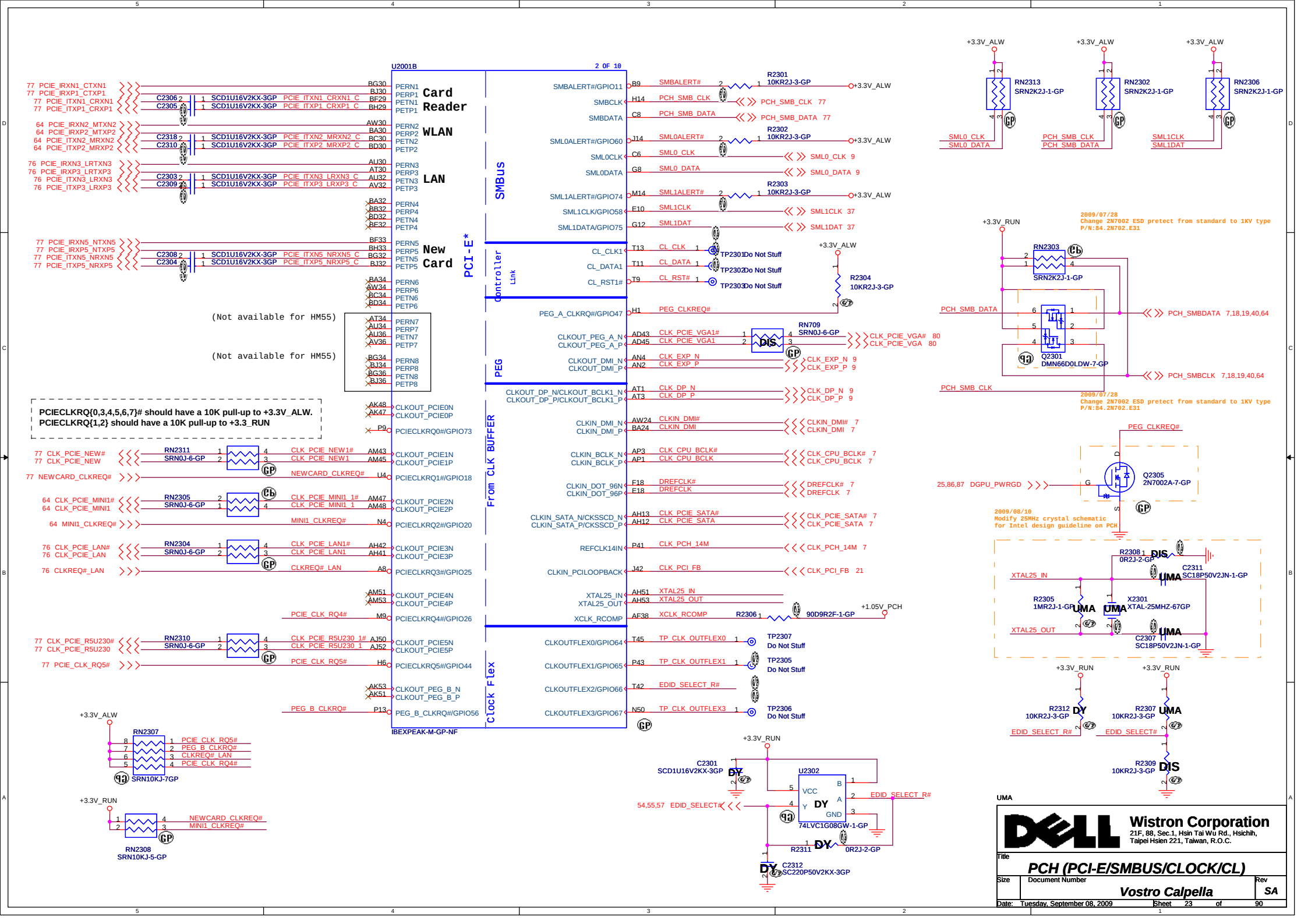
UMA

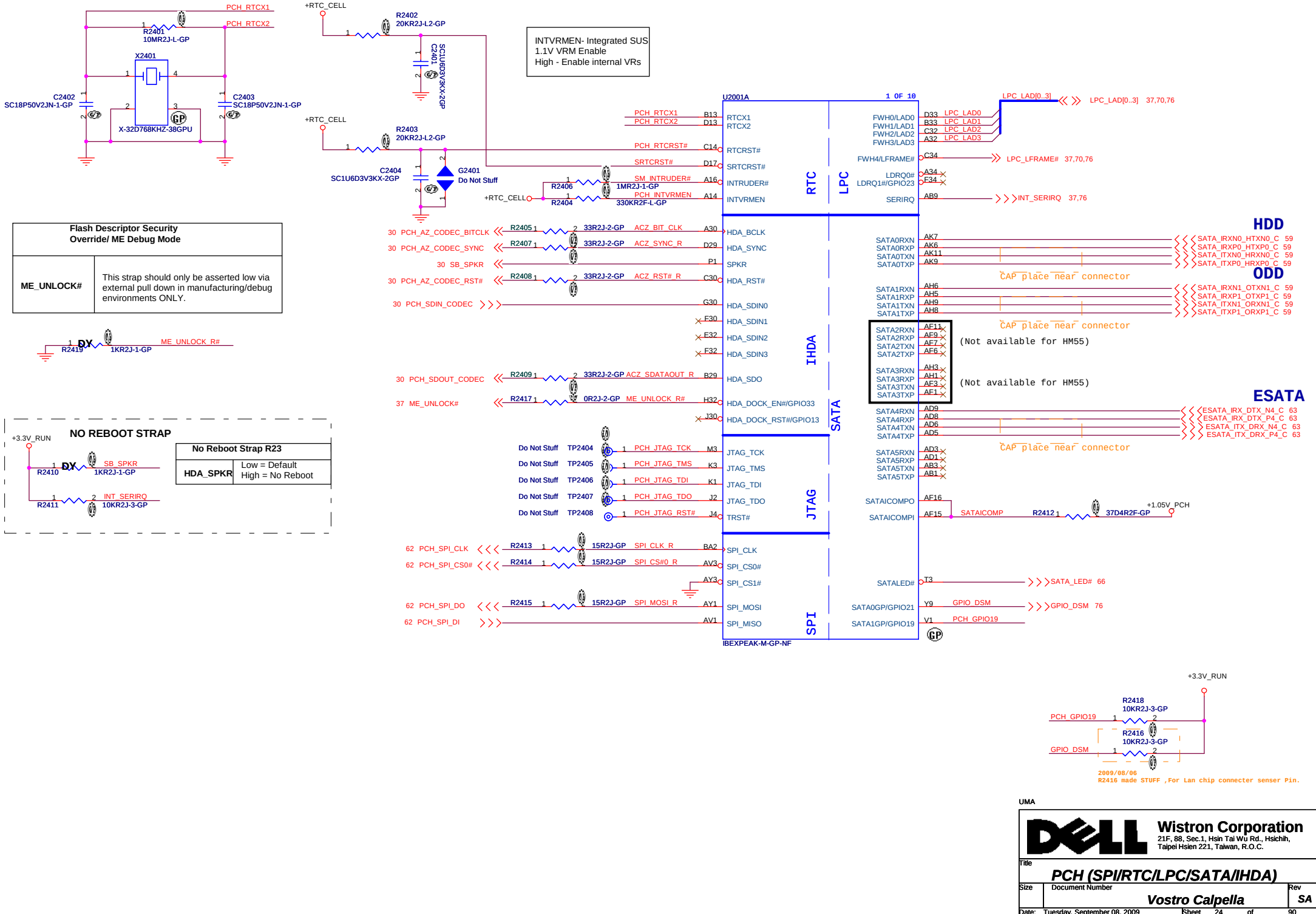
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (DM I/FDI/PM)**

Size | Document Number: ***Vostro Calpella*** | Rev: SA

Date: Tuesday, September 08, 2009 | Sheet 22 of 90


U2001B
2 OF 10
IBEXPEAK-M-GP-NF
PCI-E*
SMBus
Controller Link
PEG
From CLK BUFFER
Clock Flex
Card Reader
WLAN
LAN
New Card
(Not available for HM55)
(Not available for HM55)
PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3.3V_ALW.
PCIECLKRQ{1,2} should have a 10K pull-up to +3.3_RUN
SMBALERT#/GPIO11
SMBCLK
SMBDATA
SML0ALERT#/GPIO60
SML0CLK
SML0DATA
SML1ALERT#/GPIO74
SML1CLK/GPIO58
SML1DATA/GPIO75
CL_CLK1
CL_DATA1
CL_RST1#
PEG_A_CLKRQ#/GPIO47
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
CLKOUT_DMI_N
CLKOUT_DMI_P
CLKOUT_DP_N/CLKOUT_BCLK1_N
CLKOUT_DP_P/CLKOUT_BCLK1_P
CLKIN_DMI_N
CLKIN_DMI_P
CLKIN_BCLK_N
CLKIN_BCLK_P
CLKIN_DOT_96N
CLKIN_DOT_96P
CLKIN_SATA_N/CKSSCD_N
CLKIN_SATA_P/CKSSCD_P
REFCLK14IN
CLKIN_PCILOOPBACK
XTAL25_IN
XTAL25_OUT
XCLK_RCOMP
CLKOUTFLEX0/GPIO64
CLKOUTFLEX1/GPIO65
CLKOUTFLEX2/GPIO66
CLKOUTFLEX3/GPIO67
CLKOUT_PCIE0N
CLKOUT_PCIE0P
PCIECLKRQ0#/GPIO73
CLKOUT_PCIE1N
CLKOUT_PCIE1P
PCIECLKRQ1#/GPIO18
CLKOUT_PCIE2N
CLKOUT_PCIE2P
PCIECLKRQ2#/GPIO20
CLKOUT_PCIE3N
CLKOUT_PCIE3P
PCIECLKRQ3#/GPIO25
CLKOUT_PCIE4N
CLKOUT_PCIE4P
PCIECLKRQ4#/GPIO26
CLKOUT_PCIE5N
CLKOUT_PCIE5P
PCIECLKRQ5#/GPIO44
CLKOUT_PEG_B_N
CLKOUT_PEG_B_P
PEG_B_CLKRQ#/GPIO56
RN2311 SRN0J-6-GP
RN2305 SRN0J-6-GP
RN2304 SRN0J-6-GP
RN2310 SRN0J-6-GP
RN2307 SRN10KJ-7GP
RN2308 SRN10KJ-5-GP
R2301 10KR2J-3-GP
R2302 10KR2J-3-GP
R2303 10KR2J-3-GP
R2304 10KR2J-3-GP
RN709 SRN0J-6-GP
R2306 90D9R2F-1-GP
+1.05V_PCH
TP2301 Do Not Stuff
TP2302 Do Not Stuff
TP2303 Do Not Stuff
TP2305 Do Not Stuff
TP2306 Do Not Stuff
TP2307 Do Not Stuff
C2301 SCD1U16V2KX-3GP
C2312 SC220P50V2KX-3GP
U2302 74LVC1G08GW-1-GP
R2311 0R2J-2-GP
RN2313 SRN2K2J-1-GP
RN2302 SRN2K2J-1-GP
RN2306 SRN2K2J-1-GP
RN2303 SRN2K2J-1-GP
Q2301 DMN66D0LDW-7-GP
Q2305 2N7002A-7-GP
R2308 0R2J-2-GP
C2311 SC18P50V2JN-1-GP
R2305 1MR2J-1-GP
X2301 XTAL-25MHZ-67GP
C2307 SC18P50V2JN-1-GP
R2312 10KR2J-3-GP
R2307 10KR2J-3-GP
R2309 10KR2J-3-GP
2009/07/28 Change 2N7002 ESD pretect from standard to 1KV type P/N:84.2N702.E31
2009/08/10 Modify 25MHz crystal schematic for Intel design guideline on PCH
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
PCH (PCI-E/SMBUS/CLOCK/CL)
Vostro Calpella
Tuesday, September 08, 2009
Sheet 23 of 90


PCH_RTCX1
PCH_RTCX2
R2401
10MR2J-L-GP
X2401
C2402
SC18P50V2JN-1-GP
C2403
SC18P50V2JN-1-GP
X-32D768KHZ-38GPU
+RTC_CELL
R2402
20KR2J-L-GP
C2401
SC1U6D3V3KX-2GP
R2403
20KR2J-L-GP
C2404
SC1U6D3V3KX-2GP
G2401
Do Not Stuff
R2406
1MR2J-1-GP
R2404
330KR2F-L-GP
INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable internal VRs
Flash Descriptor Security Override/ ME Debug Mode
ME_UNLOCK#
This strap should only be asserted low via external pull down in manufacturing/debug environments ONLY.
R2419
1KR2J-1-GP
ME_UNLOCK_R#
NO REBOOT STRAP
+3.3V_RUN
R2410
1KR2J-1-GP
SB_SPKR
R2411
10KR2J-3-GP
INT_SERIRQ
No Reboot Strap R23
HDA_SPKR
Low = Default
High = No Reboot
U2001A
1 OF 10
RTC
LPC
IHDA
SATA
JTAG
SPI
RTCX1
RTCX2
RTCRST#
SRTCRST#
INTRUDER#
INTVRMEN
HDA_BCLK
HDA_SYNC
SPKR
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDO
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO13
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
TRST#
SPI_CLK
SPI_CS0#
SPI_CS1#
SPI_MOSI
SPI_MISO
IBEXPEAK-M-GP-NF
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
SERIRQ
LPC_LAD[0..3]
LPC_LFRAME#
INT_SERIRQ
HDD
ODD
ESATA
CAP place near connector
(Not available for HM55)
SATAICOMPO
SATAICOMPI
SATAICOMP
SATALED#
SATA0GP/GPIO21
SATA1GP/GPIO19
GPIO_DSM
PCH_GPIO19
R2412
37D4R2F-GP
+1.05V_PCH
R2418
10KR2J-3-GP
R2416
10KR2J-3-GP
2009/08/06
R2416 made STUFF ,For Lan chip connecter senser Pin.
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (SPI/RTC/LPC/SATA/IHDA)
Size
Document Number
Vostro Calpella
Rev
SA
Date: Tuesday, September 08, 2009
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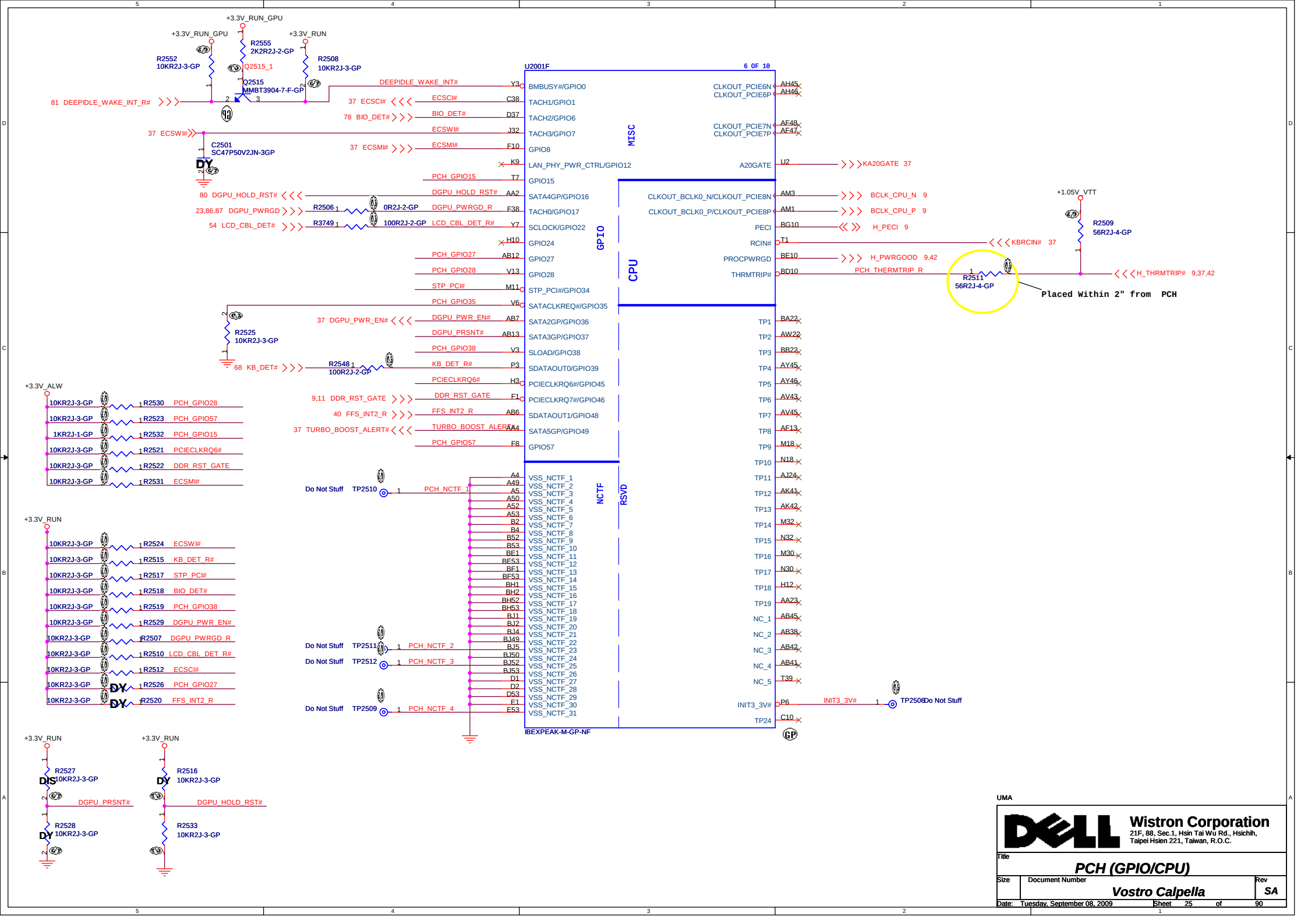
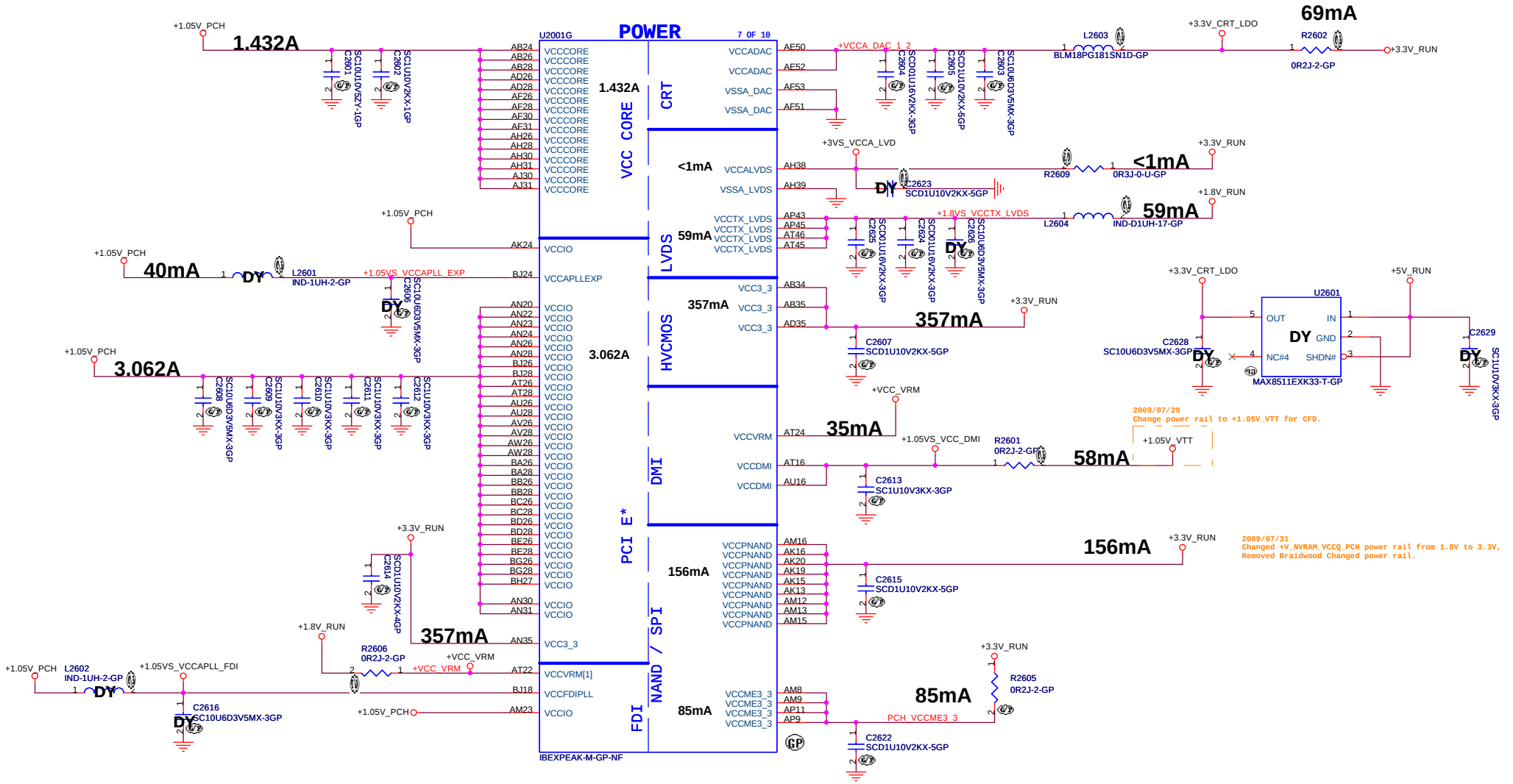

+3.3V_RUN_GPU
+3.3V_RUN_GPU
+3.3V_RUN
R2555
2K2R2J-2-GP
R2552
10KR2J-3-GP
R2508
10KR2J-3-GP
Q2515_1
Q2515
MMBT3904-7-F-GP
81 DEEPIDLE_WAKE_INT_R#
DEEPIDLE_WAKE_INT#
37 ECSCI#
ECSCI#
78 BIO_DET#
BIO_DET#
37 ECSWI#
ECSWI#
37 ECSMI#
ECSMI#
C2501
SC47P50V2JN-3GP
DY
U2001F
6 OF 10
BMBUSY#/GPIO0
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
LAN_PHY_PWR_CTRL/GPIO12
GPIO15
SATA4GP/GPIO16
TACH0/GPIO17
SCLOCK/GPIO22
GPIO24
GPIO27
GPIO28
STP_PCI#/GPIO34
SATACLKREQ#/GPIO35
SATA2GP/GPIO36
SATA3GP/GPIO37
SLOAD/GPIO38
SDATAOUT0/GPIO39
PCIECLKRQ6#/GPIO45
PCIECLKRQ7#/GPIO46
SDATAOUT1/GPIO48
SATA5GP/GPIO49
GPIO57
MISC
GPIO
CPU
NCTF
RSVD
IBEXPEAK-M-GP-NF
CLKOUT_PCIE6N
CLKOUT_PCIE6P
CLKOUT_PCIE7N
CLKOUT_PCIE7P
A20GATE
KA20GATE 37
CLKOUT_BCLK0_N/CLKOUT_PCIE8N
CLKOUT_BCLK0_P/CLKOUT_PCIE8P
BCLK_CPU_N 9
BCLK_CPU_P 9
PECI
H_PECI 9
RCIN#
KBRCIN# 37
PROCPWRGD
H_PWRGOOD 9,42
THRMTRIP#
PCH_THERMTRIP_R
H_THRMTRIP# 9,37,42
80 DGPU_HOLD_RST#
DGPU_HOLD_RST#
23,86,87 DGPU_PWRGD
R2506
0R2J-2-GP
DGPU_PWRGD_R
54 LCD_CBL_DET#
R3749
100R2J-2-GP
LCD_CBL_DET_R#
PCH_GPIO15
PCH_GPIO27
PCH_GPIO28
STP_PCI#
PCH_GPIO35
37 DGPU_PWR_EN#
DGPU_PWR_EN#
DGPU_PRSNT#
PCH_GPIO38
68 KB_DET#
R2548
100R2J-2-GP
KB_DET_R#
R2525
10KR2J-3-GP
PCIECLKRQ6#
9,11 DDR_RST_GATE
DDR_RST_GATE
40 FFS_INT2_R
FFS_INT2_R
37 TURBO_BOOST_ALERT#
TURBO_BOOST_ALERT
PCH_GPIO57
+1.05V_VTT
R2509
56R2J-4-GP
R2511
56R2J-4-GP
Placed Within 2" from PCH
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
TP10
TP11
TP12
TP13
TP14
TP15
TP16
TP17
TP18
TP19
NC_1
NC_2
NC_3
NC_4
NC_5
INIT3_3V#
TP24
INIT3_3V#
TP2506 Do Not Stuff
+3.3V_ALW
10KR2J-3-GP
1KR2J-1-GP
R2530 PCH_GPIO28
R2523 PCH_GPIO57
R2532 PCH_GPIO15
R2521 PCIECLKRQ6#
R2522 DDR_RST_GATE
R2531 ECSMI#
+3.3V_RUN
R2524 ECSWI#
R2515 KB_DET_R#
R2517 STP_PCI#
R2518 BIO_DET#
R2519 PCH_GPIO38
R2529 DGPU_PWR_EN#
R2507 DGPU_PWRGD_R
R2510 LCD_CBL_DET_R#
R2512 ECSCI#
R2526 PCH_GPIO27
R2520 FFS_INT2_R
DY
Do Not Stuff
TP2510
TP2511
TP2512
TP2509
PCH_NCTF_1
PCH_NCTF_2
PCH_NCTF_3
PCH_NCTF_4
VSS_NCTF_1
VSS_NCTF_2
VSS_NCTF_3
VSS_NCTF_4
VSS_NCTF_5
VSS_NCTF_6
VSS_NCTF_7
VSS_NCTF_8
VSS_NCTF_9
VSS_NCTF_10
VSS_NCTF_11
VSS_NCTF_12
VSS_NCTF_13
VSS_NCTF_14
VSS_NCTF_15
VSS_NCTF_16
VSS_NCTF_17
VSS_NCTF_18
VSS_NCTF_19
VSS_NCTF_20
VSS_NCTF_21
VSS_NCTF_22
VSS_NCTF_23
VSS_NCTF_24
VSS_NCTF_25
VSS_NCTF_26
VSS_NCTF_27
VSS_NCTF_28
VSS_NCTF_29
VSS_NCTF_30
VSS_NCTF_31
+3.3V_RUN
R2527
10KR2J-3-GP
DIS
DGPU_PRSNT#
R2528
10KR2J-3-GP
+3.3V_RUN
R2516
10KR2J-3-GP
DGPU_HOLD_RST#
R2533
10KR2J-3-GP
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (GPIO/CPU)
Size
Document Number
Vostro Calpella
Rev
SA
Date: Tuesday, September 08, 2009
Sheet 25 of 90



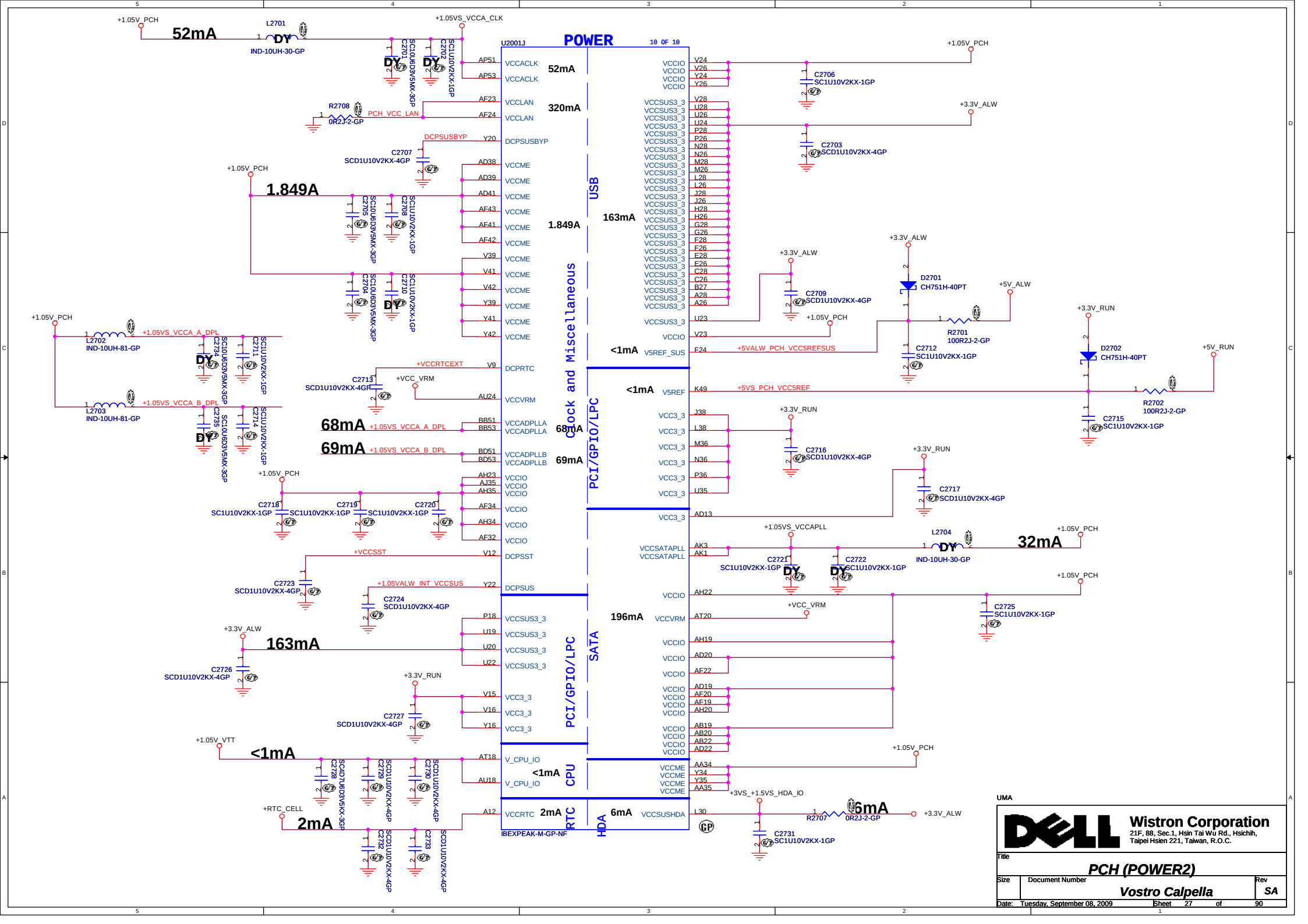
UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (POWER1)

Size | Document Number: Vostro Calpella | Rev: SA

Date: Tuesday, September 08, 2009 | Sheet 26 of 90


POWER
10 OF 10
U2001J
IBEXPEAK-M-GP-NF
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
+1.05V_PCH
+1.05VS_VCCA_CLK
+1.05VS_VCCA_A_DPL
+1.05VS_VCCA_B_DPL
+1.05VALW_INT_VCCSUS
+1.05VS_VCCAPLL
+1.05V_VTT
+3.3V_ALW
+3.3V_RUN
+5V_ALW
+5V_RUN
+VCC_VRM
+VCCRTCEXT
+VCCSST
+RTC_CELL
+3VS_+1.5VS_HDA_IO
+5VALW_PCH_VCC5REFSUS
+5VS_PCH_VCC5REF
PCH_VCC_LAN
DCPSUSBYP
52mA
1.849A
320mA
163mA
68mA
69mA
196mA
32mA
6mA
2mA
<1mA
L2701
IND-10UH-30-GP
L2702
IND-10UH-81-GP
L2703
IND-10UH-81-GP
L2704
IND-10UH-30-GP
R2708
0R2J-2-GP
R2701
100R2J-2-GP
R2702
100R2J-2-GP
R2707
0R2J-2-GP
D2701
CH751H-40PT
D2702
CH751H-40PT
C2706
SC1U10V2KX-1GP
C2703
SCD1U10V2KX-4GP
C2709
SCD1U10V2KX-4GP
C2712
SC1U10V2KX-1GP
C2715
SC1U10V2KX-1GP
C2716
SCD1U10V2KX-4GP
C2717
SCD1U10V2KX-4GP
C2721
SC1U10V2KX-1GP
C2722
SC1U10V2KX-1GP
C2725
SC1U10V2KX-1GP
C2731
SC1U10V2KX-1GP
C2707
SCD1U10V2KX-4GP
C2713
SCD1U10V2KX-4GP
C2723
SCD1U10V2KX-4GP
C2724
SCD1U10V2KX-4GP
C2726
SCD1U10V2KX-4GP
C2727
SCD1U10V2KX-4GP
C2718
SC1U10V2KX-1GP
C2719
SC1U10V2KX-1GP
C2720
SC1U10V2KX-1GP
C2701
SC10U6D3V5MX-3GP
C2702
SC1U10V2KX-1GP
C2705
SC10U6D3V5MX-3GP
C2708
SC1U10V2KX-1GP
C2704
SC10U6D3V5MX-3GP
C2710
SC1U10V2KX-1GP
C2734
SC10U6D3V5MX-3GP
C2711
SC1U10V2KX-1GP
C2735
SC10U6D3V5MX-3GP
C2714
SC1U10V2KX-1GP
C2728
SC4D7U6D3V5KX-3GP
C2729
SCD1U10V2KX-4GP
C2730
SCD1U10V2KX-4GP
C2732
SCD1U10V2KX-4GP
C2733
SCD1U10V2KX-4GP
DY
GP
UMA
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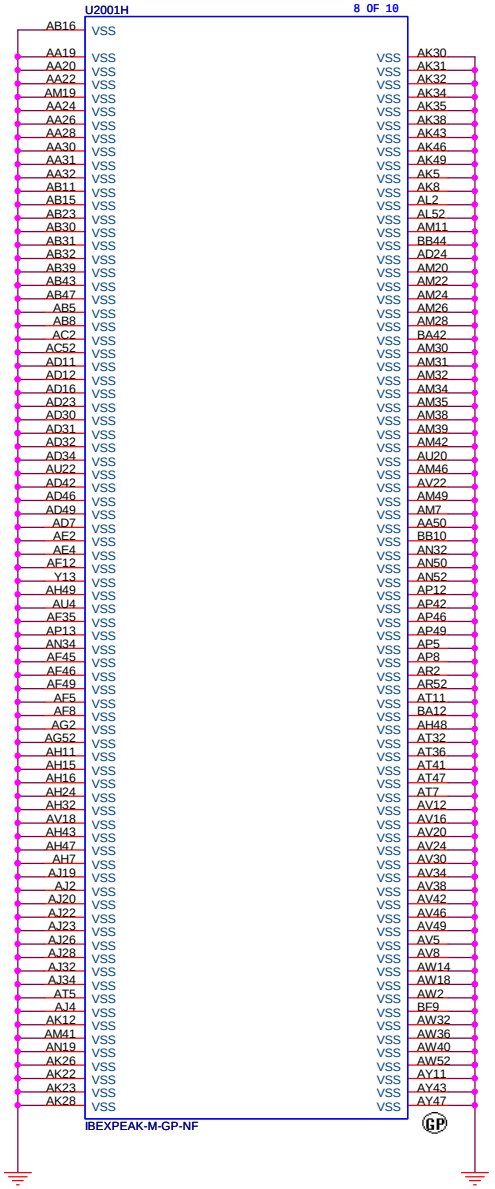
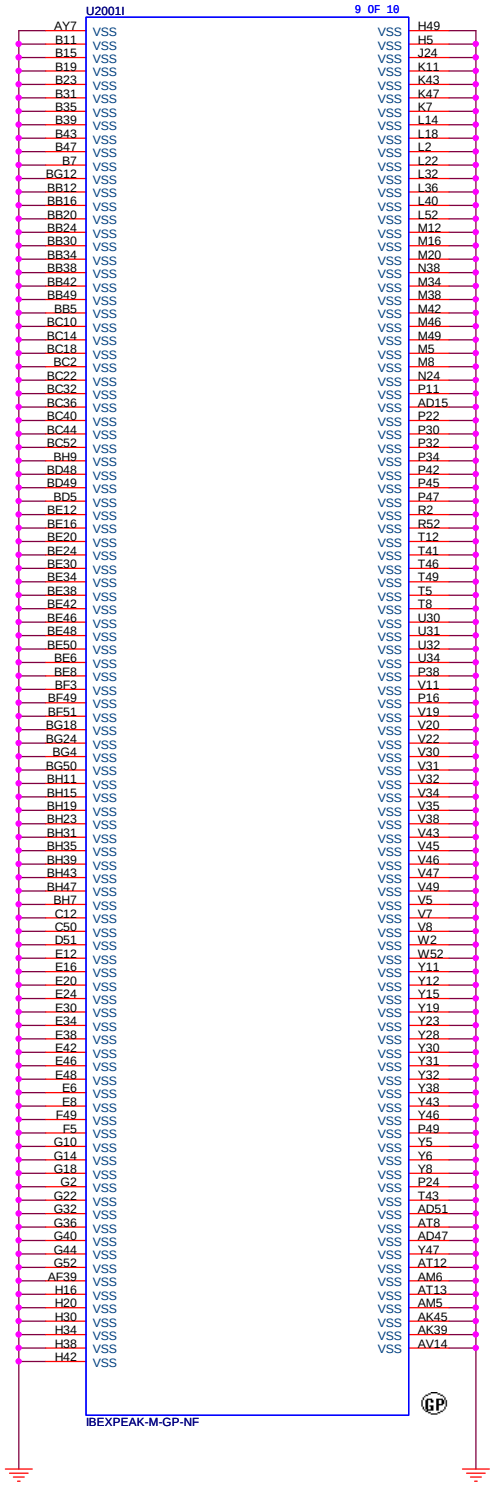
Title
PCH (POWER2)
Size
Document Number
Vostro Calpella
Rev
SA
Date: Tuesday, September 08, 2009
Sheet 27 of 90





UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PCH (VSS)***

Size | Document Number: ***Vostro Calpella*** | Rev: SA

Date: Tuesday, September 08, 2009 | Sheet 28 of 90

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UMA

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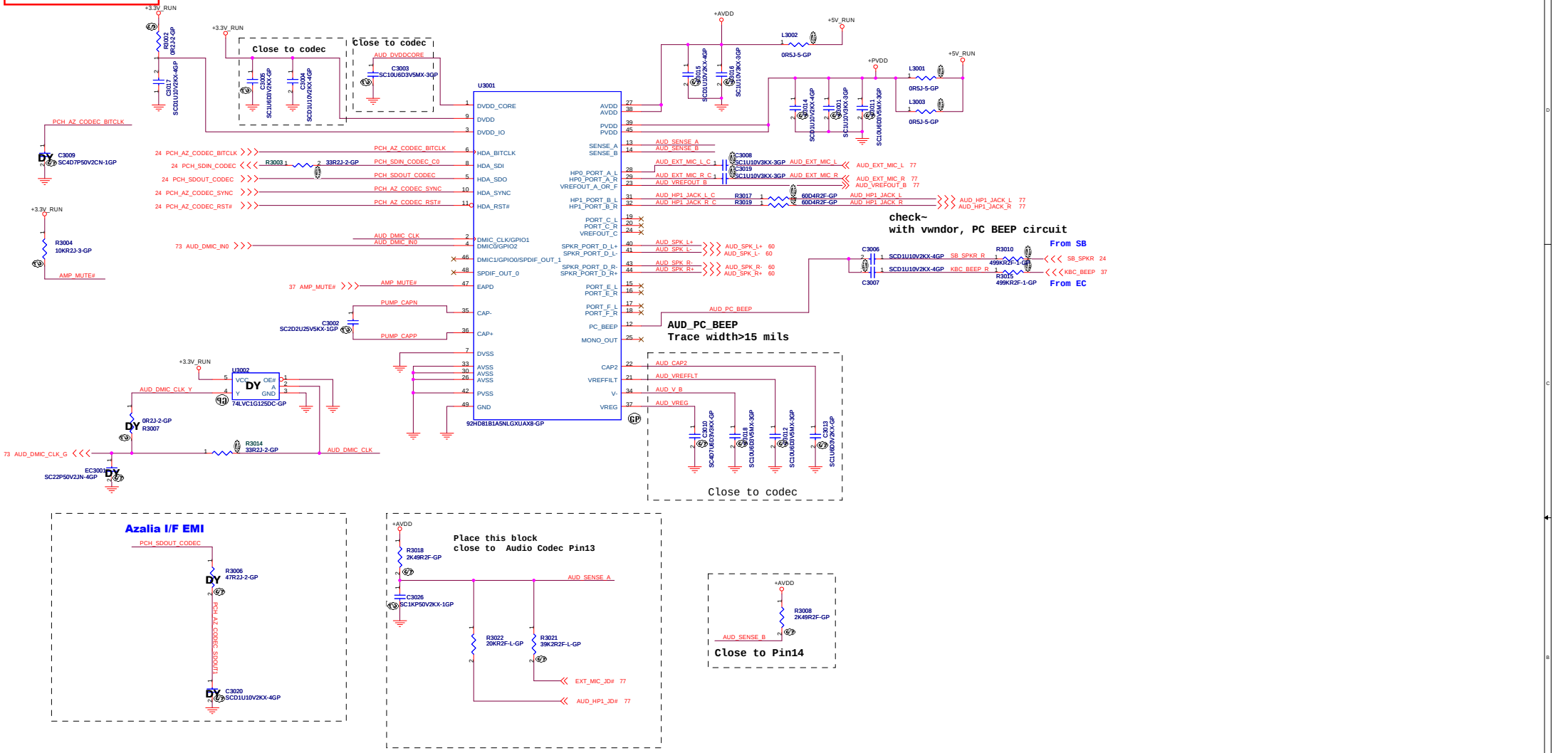
Title

(Reserve)

Size	Document Number	Rev
Custom	*Vostro Calpella*	*SA*

Date: Tuesday, September 08, 2009 Sheet 29 of 90

SSID = AUDIO



UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO CODEC 92HD81

Size	Document Number	Rev
A2	Vostro Calpella	SA

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Title

(Reserve)

Size	Document Number	Rev
Custom	*Vostro Calpella*	*SA*

Date: Tuesday, September 08, 2009 Sheet 31 of 90

(Blank)

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Title: *Reserve*

Size: A3 | Document Number: *Vostro Calpella* | Rev: *SA*

Date: Tuesday, September 08, 2009 | Sheet 32 of 90

(Blank)

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Title

(Reserve)

Size	Document Number	Rev
Custom	*Vostro Calpella*	*SA*

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(Blank)

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Title: *(Reserve)*

Size	Document Number	Rev
Custom	*Vostro Calpella*	*SA*

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Title

(Reserve)

Size	Document Number	Rev
A3	*Vostro Calpella*	*SA*

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Title: TPM

Size: Custom | Document Number: Vostro Calpella | Rev: SA

Date: Tuesday, September 08, 2009 | Sheet 36 of 90

SSID = KBC

Added 10mW circuit
2009/06/04

Check~

Put 0.1uf close to VCC-GND pin pair.

Pull High : Discrete
internal Pull Low for UMA

Remove
HDD_FALL_INT1

MB VERSION		
ID	VER1	VER0
SA	0	0
SB	0	1
SC	1	0
-1	1	1

KBC CLK
EMI

2009/07/28
Change 2N7002 ESD pretect from standard to 1KV type
P/N:84.2N702.E31
2009/0806
Changed Q3714 from N-MOS to BJT Gate,For cost down.

2009/07/28
Change 2N7002 ESD pretect from standard to 1KV type
P/N:84.2N702.E31

2009/08/05
Added BJT Gate Q3709
For prevent electric leakage issue

UMA

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Title: KBC Nuvoton NPCE781BA0DX

Size: Custom | Document Number: Vostro Calpella | Rev: SA

Date: Tuesday, September 08, 2009 | Sheet 37 of 90

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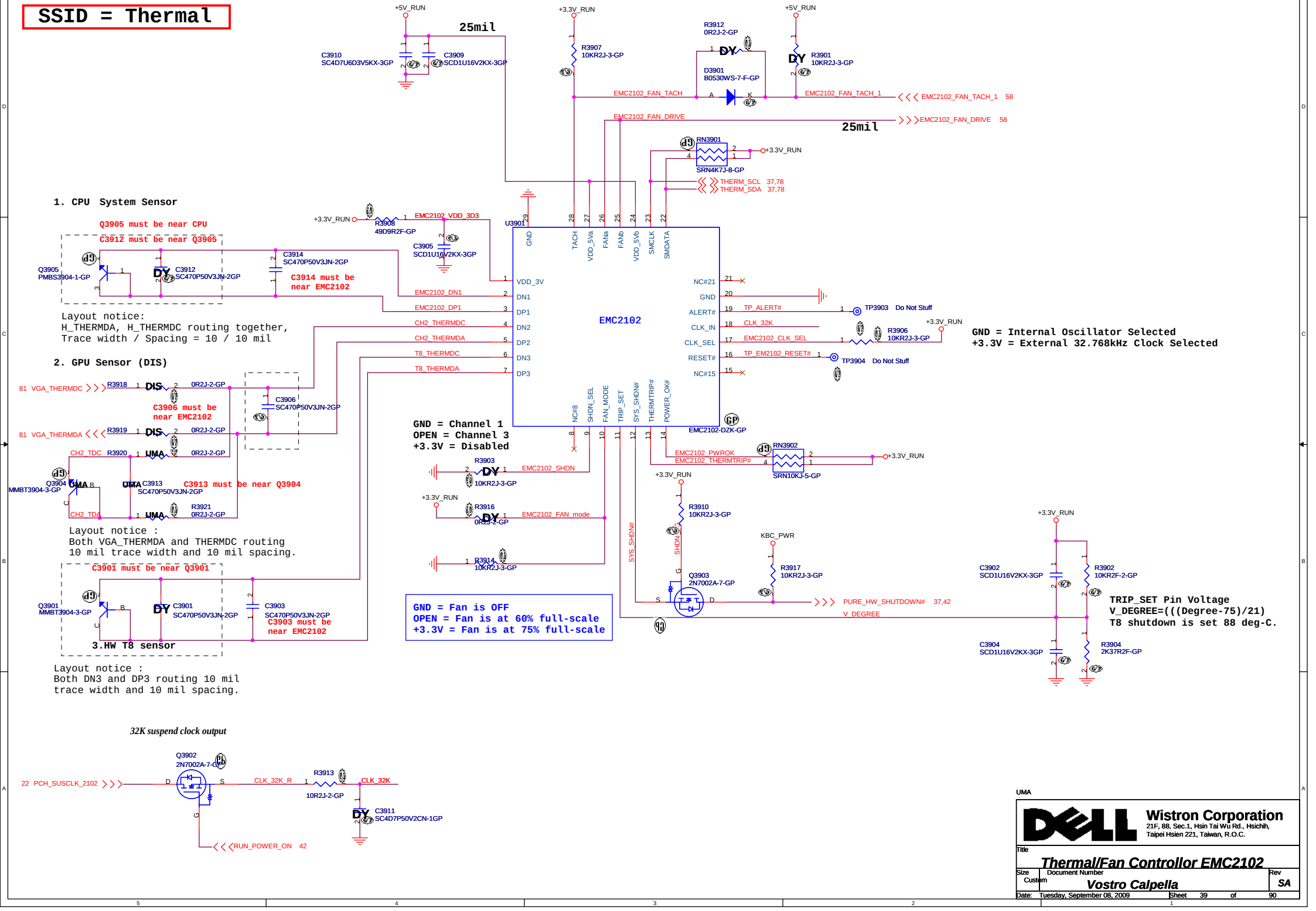
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserve)

Size	Document Number	Rev
Custom	*Vostro Calpella*	*SA*

SSID = Thermal



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Title: Thermal/Fan Controllor EMC2102

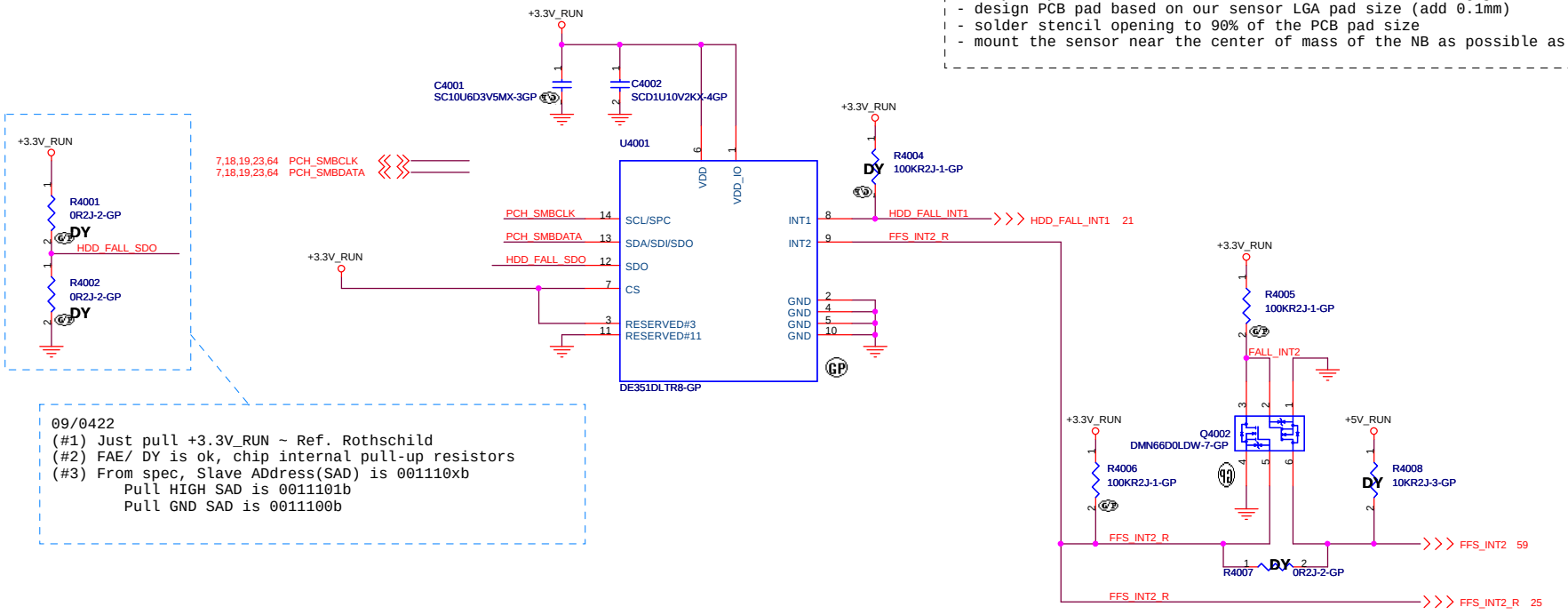
Size	Document Number	Rev
Custom	Vostro Calpella	SA

Date: Tuesday, September 08, 2009 Sheet 39 of 90

SSID = User.Interface

Free Fall Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



09/0422
(#1) Just pull +3.3V_RUN ~ Ref. Rothschild
(#2) FAE/ DY is ok, chip internal pull-up resistors
(#3) From spec, Slave ADdress(SAD) is 001110xb
Pull HIGH SAD is 0011101b
Pull GND SAD is 0011100b

Note
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

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Title: Free Fall Sensor

Size	Document Number	Rev
Custom	Vostro Calpella	SA

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Title: *(Reserve)*

Size	Document Number	Rev
Custom	*Vostro Calpella*	*SA*

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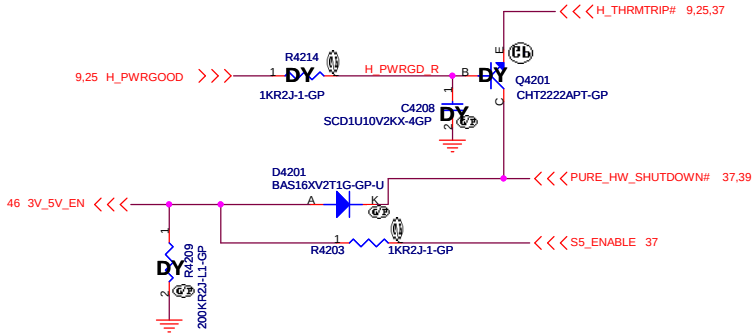
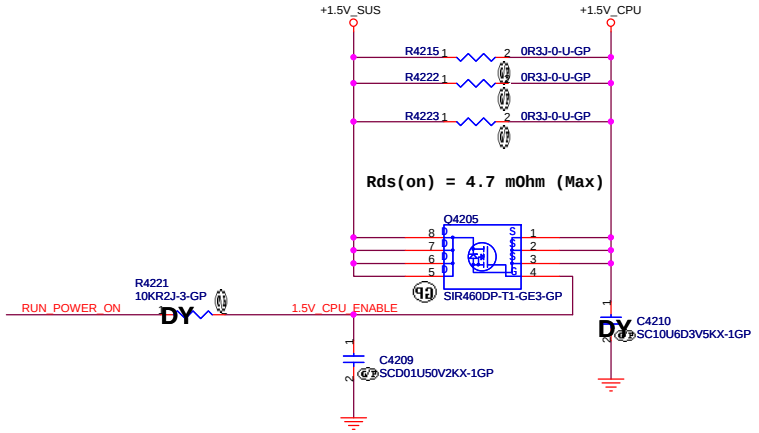
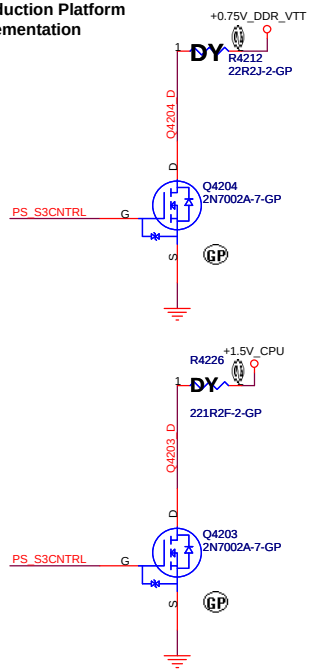
SSID = Reset.Suspend

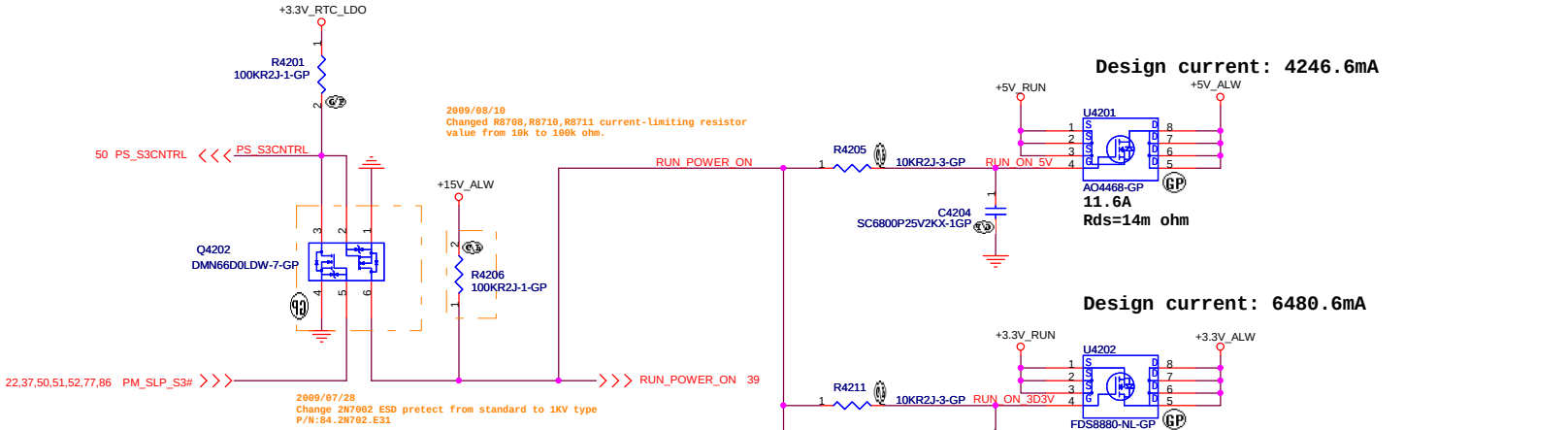


+1.5V_CPU:



Calpella Platform S3 Power Reduction Platform
S3 Power Reduction CRB Implementation
Design Details

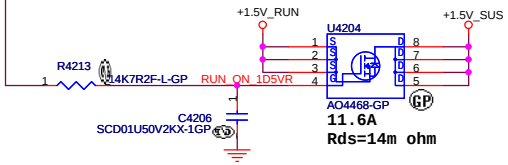




Design current: 4246.6mA

Design current: 6480.6mA

Design current: 2783.6mA



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Title: Power Plane Enable

Size	Document Number	Rev
Custom	Vostro Calpella	SA

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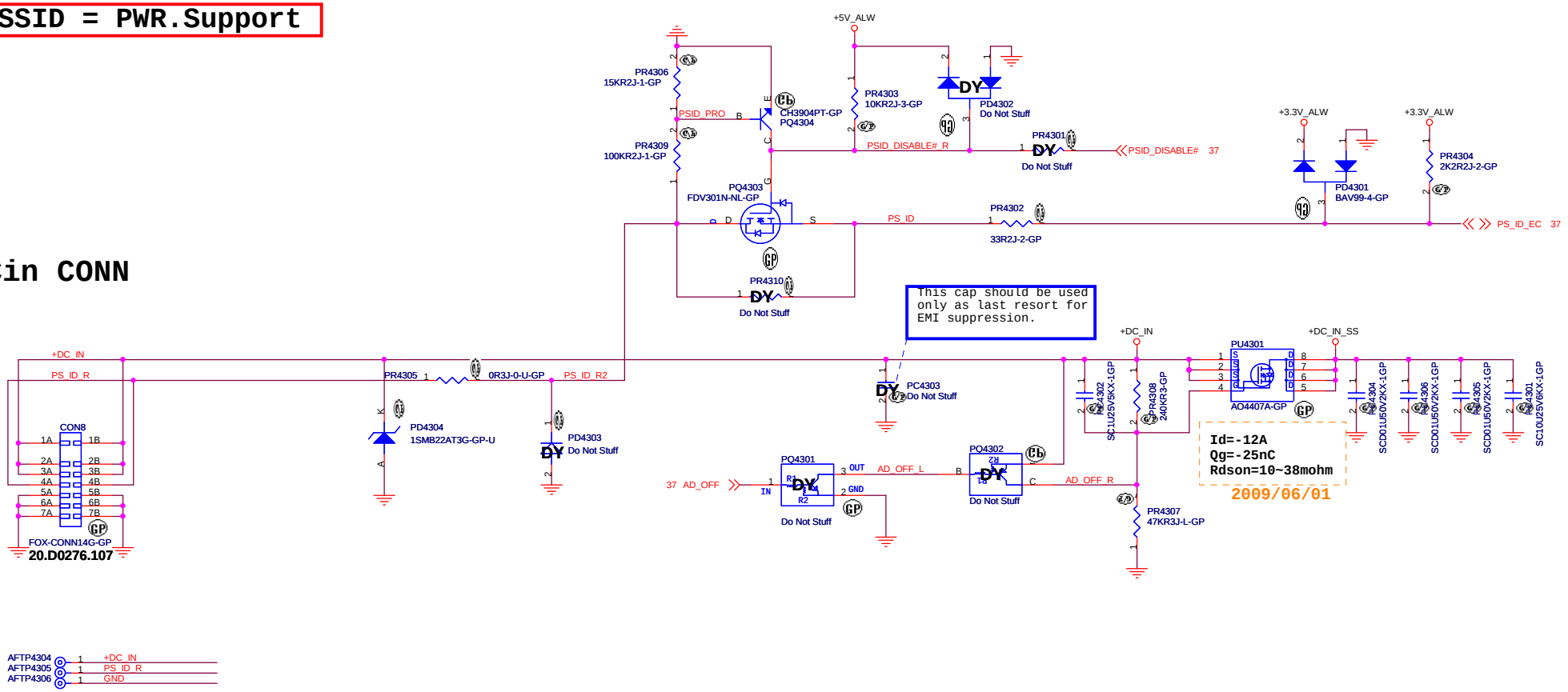
SSID = PWR.Support

DCin CONN



UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title	DC IN	
Size: Custom	Document Number: Vostro Montevina Discrete	Rev: SA
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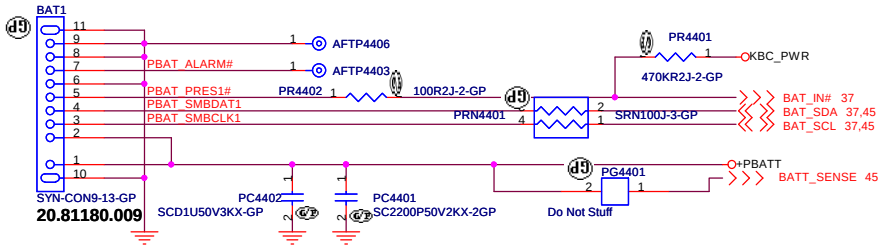
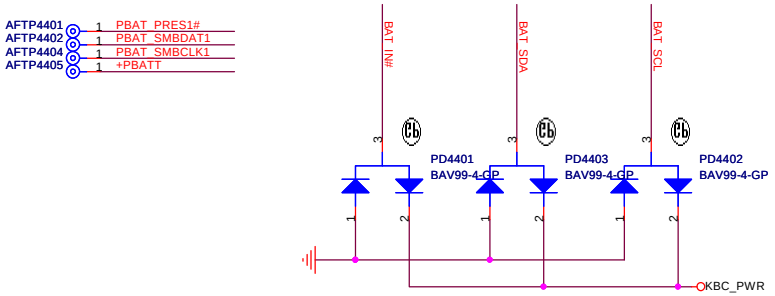
Batt Connecter





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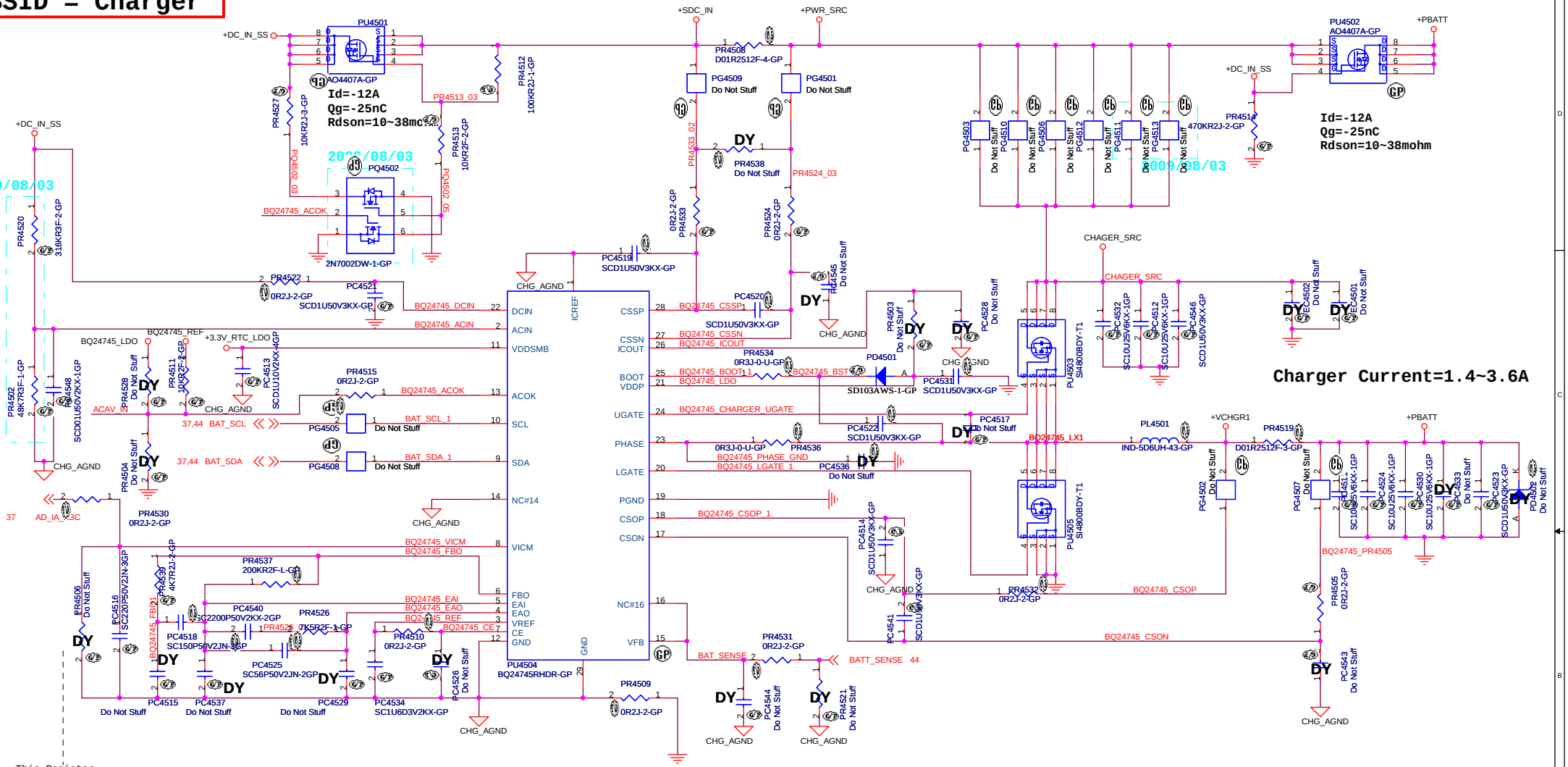
Taipei Hsien 221, Taiwan, R.O.C.

Title	BATT CONN	
Size: A3	Document Number: Vostro Montevina Discrete	Rev: SA
Date: Tuesday, September 08, 2009	Sheet 44 of 90	

SSID = Charger



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Title: CHARGER BQ24745

Size: Custom | Document Number: DW Calpella | Rev: SA

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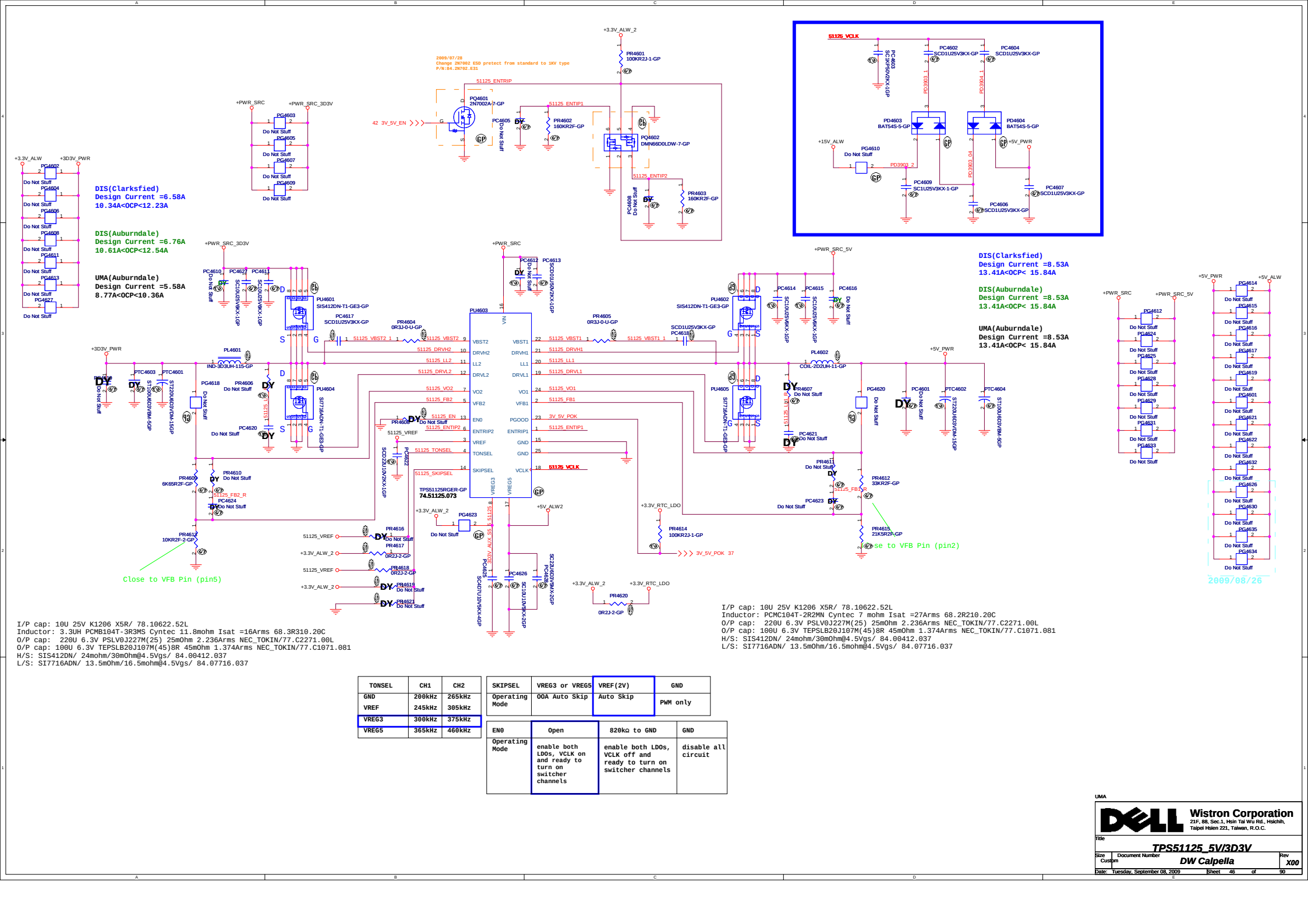

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 3.3UH PCMB104T-3R3MS Cyntec 11.8mohm Isat =16Arms 68.3R310.20C
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V TEPSLB20J107M(45)8R 45mOhm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: SIS412DN/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S: SI7716ADN/ 13.5mOhm/16.5mohm@4.5Vgs/ 84.07716.037

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: PCMC104T-2R2MN Cyntec 7 mohm Isat =27Arms 68.2R210.20C
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V TEPSLB20J107M(45)8R 45mOhm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: SIS412DN/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S: SI7716ADN/ 13.5mOhm/16.5mohm@4.5Vgs/ 84.07716.037

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

UMA

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Title: TPS51125_5V/3D3V

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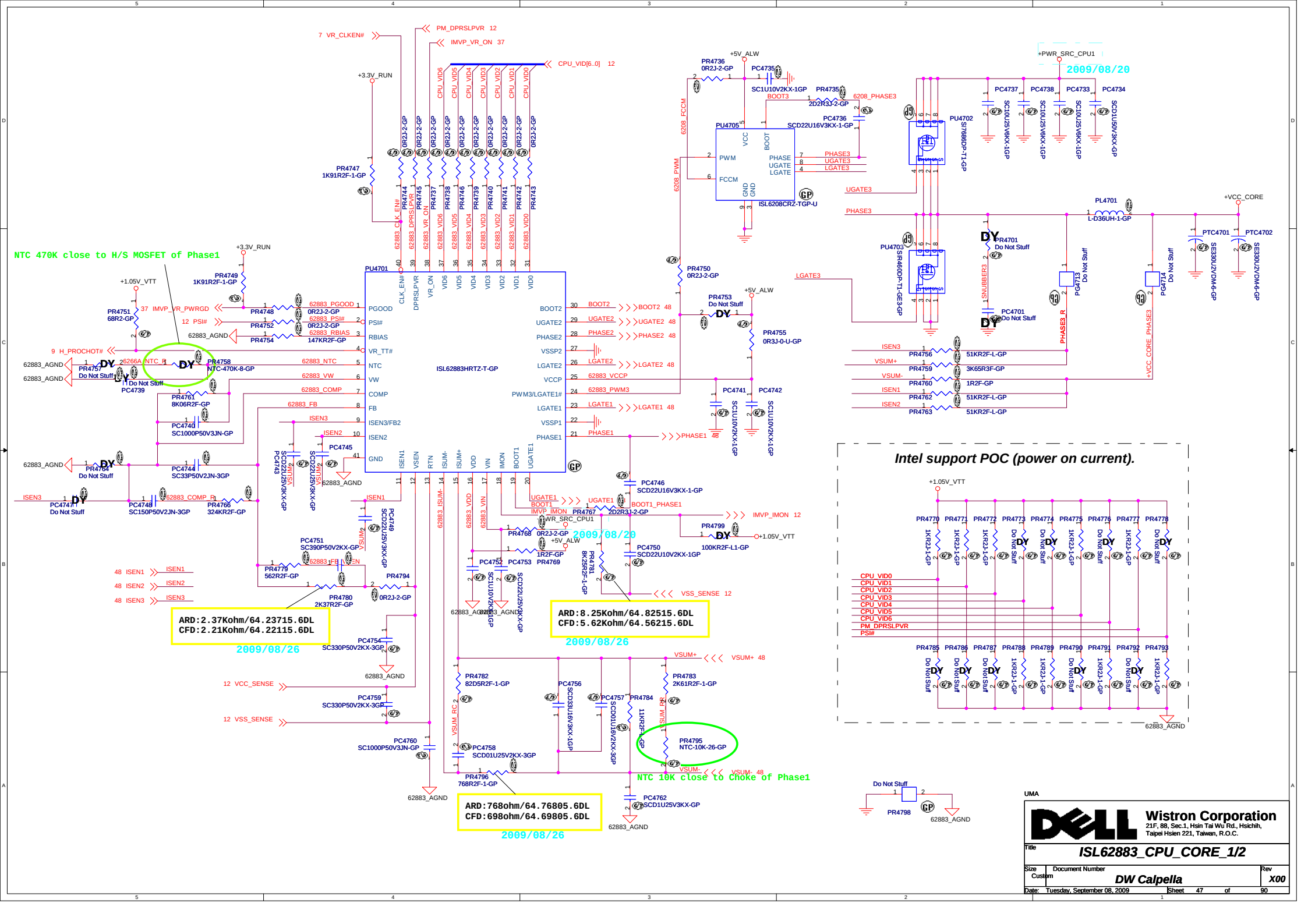
NTC 470K close to H/S MOSFET of Phase1
ISL62883HRTZ-T-GP
PU4701
ISL6208CRZ-TGP-U
PU4705
PU4702
PU4703
SI7686DP-T1-GP
SIR460DP-T1-GE3-GP
ARD:2.37Kohm/64.23715.6DL
CFD:2.21Kohm/64.22115.6DL
2009/08/26
ARD:8.25Kohm/64.82515.6DL
CFD:5.62Kohm/64.56215.6DL
2009/08/26
ARD:768ohm/64.76805.6DL
CFD:698ohm/64.69805.6DL
2009/08/26
NTC 10K close to Choke of Phase1
2009/08/20
2009/08/20
Intel support POC (power on current).
Wistron Corporation
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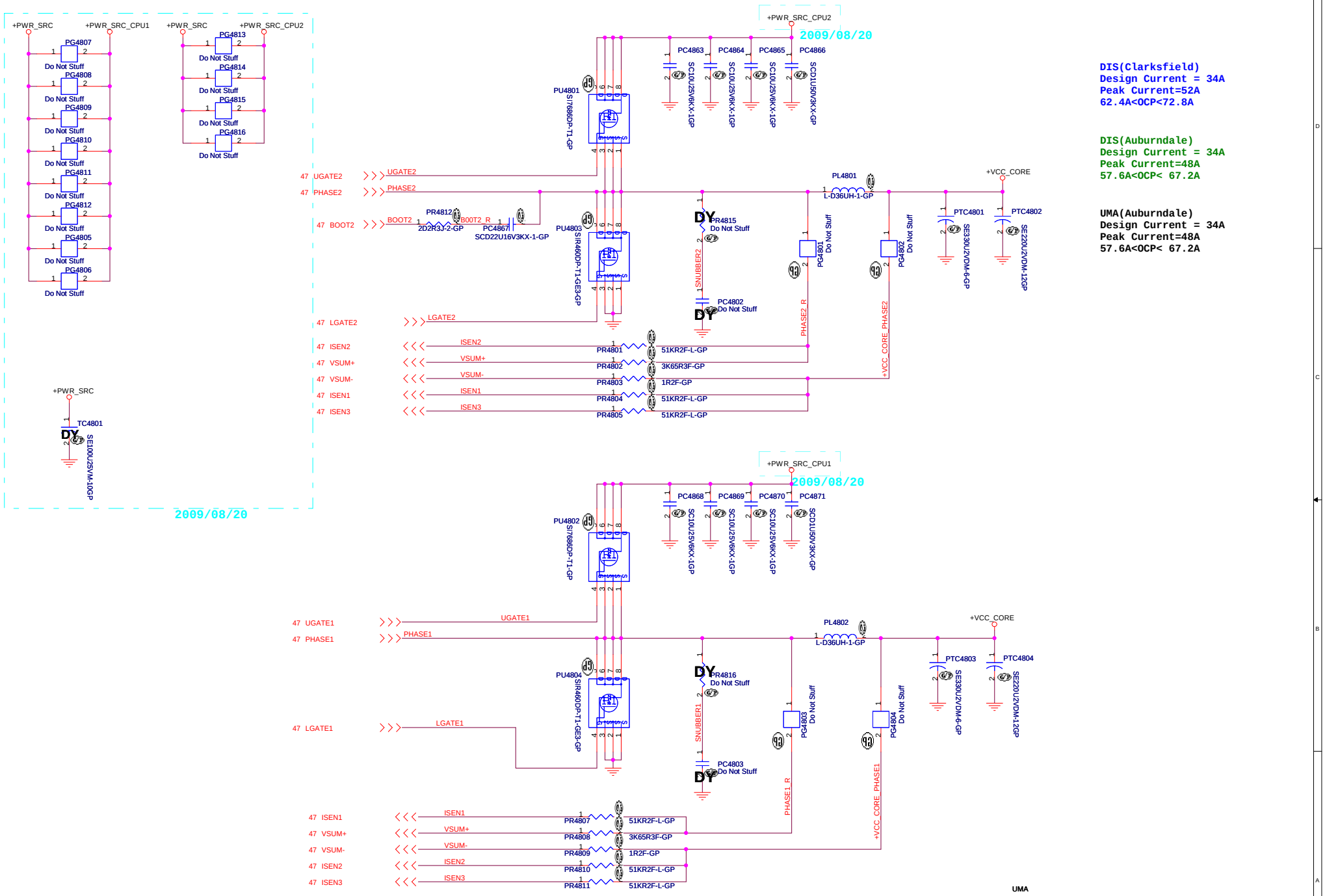
Taipei Hsien 221, Taiwan, R.O.C.
ISL62883_CPU_CORE_1/2
DW Calpella
X00
Tuesday, September 08, 2009
47
90



2009/08/20

DIS(Clarksfield)
Design Current = 34A
Peak Current=52A
62.4A<OCP<72.8A

DIS(Auburndale)
Design Current = 34A
Peak Current=48A
57.6A<OCP< 67.2A

UMA(Auburndale)
Design Current = 34A
Peak Current=48A
57.6A<OCP< 67.2A

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.36UH ETQP4LR36WFC PANASONIC 1.1mohm/ 68.R3610.20A
O/P cap: 330U 2V EEFSX0D221E7 6mOhm 3.0Arms Panasonic/79.33719.20L
O/P cap: 220U 2V EEFSX0D331XE 7mOhm 3.4Arms Panasonic/79.22719.90L
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037
Freq=300KHz@PER PHASE

UMA

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Title: ISL62883_CPU_CORE_2/2

Size: Custom | Document Number: DW Calpella | Rev: X00

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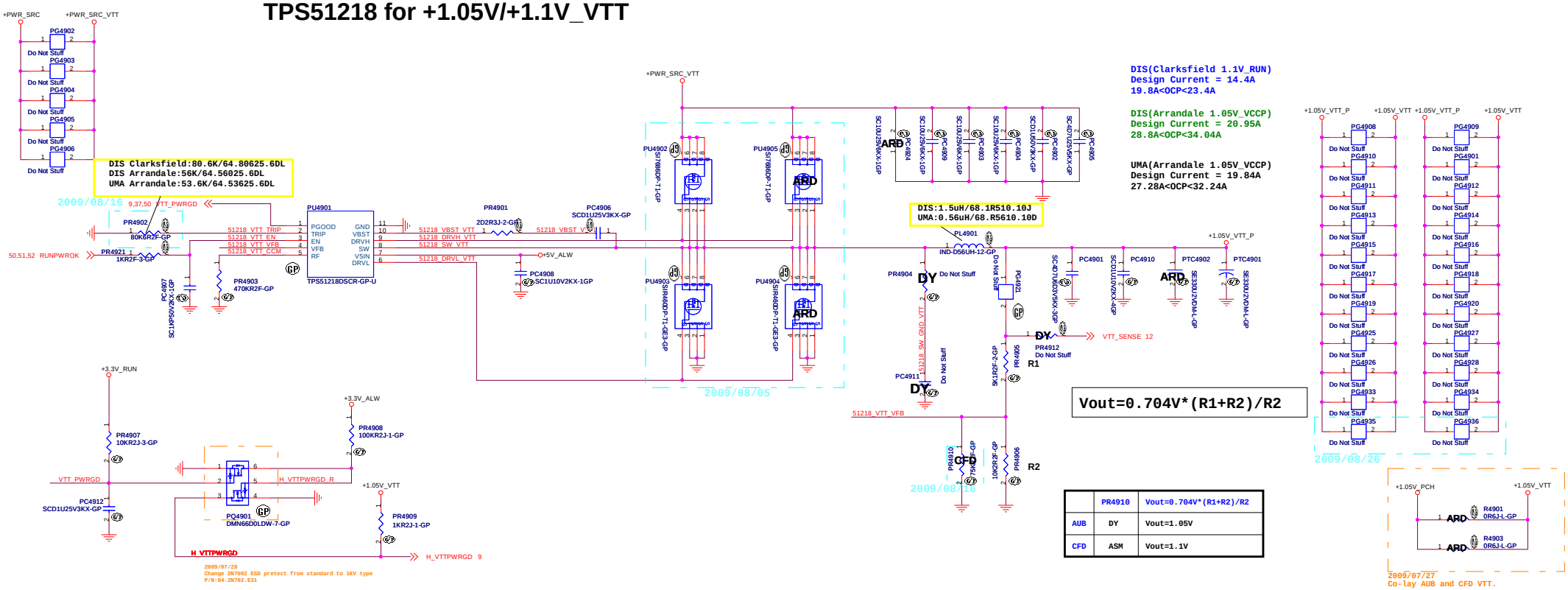
TPS51218 for +1.05V/+1.1V_VTT



	PR4910	Vout=0.704V*(R1+R2)/R2
AUB	DY	Vout=1.05V
CFD	ASM	Vout=1.1V

Frequency setting	
470K	-->290KHz
200K	-->340KHz
100K	-->380KHz
39K	-->430KHz

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.8mohm Isat=25Arms 68.R5610.10D
Inductor: 1.5uH PCMC104T-1R5MN Cyntec DCR:4.2mohm Isat=33Arms 68.1R510.10J
O/P cap: 330U 2.5V EEFSX0D331ER 9mOhm 3Arms PANASONIC/ 79.33719.L01
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

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Title: TPS51218_+1.05V_VTT

Size	Document Number	Rev
Custom	DJ1 Discrete	X00

Date: Tuesday, September 08, 2009 Sheet 49 of 90

SSID = PWR.Plane.Regulator_1p5v0p75v

DIS Clarksfield:11.5K/64.11525.6DL
DIS Arrandale:9.76K/64.97615.6DL
UMA Arrandale:6.65K/64.66515.6DL

2009/08/16

2009/07/09
follow vostro 15 inch schematic

2009/07/29
Reserved R,C By PM_SLP_S4# ,for time delay

2009/08/05

Design Current = 0.7A

DIS(Clarksfied)
Design Current = 14.52A
22.82A<OCP<26.97A

DIS(Auburndale)
Design Current = 12.42A
19.52A<OCP<23.07A

UMA(Auburndale)
Design Current = 8.51A
13.37A<OCP<15.8A

DIS:1.0uH/68.1R01A.20A
UMA:1.5uH/68.1R510.10J

DIS:EEFSX0D331ER/79.33719.L01
UMA:EEFCX0D221R/79.22719.20L

Close to VFB Pin (pin5)

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.0uH PCMC104T-1R0MN Cyntec DCR:3.5mohm Isat=40Arms 68.1R01A.20A
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3Arms PANASONIC/ 79.33719.L01
O/P cap: 220U 2V EEFCX0D221R 15mOhm 2.7Arms PANASONIC/ 79.22719.20L
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037
Switching freq-->400KHz

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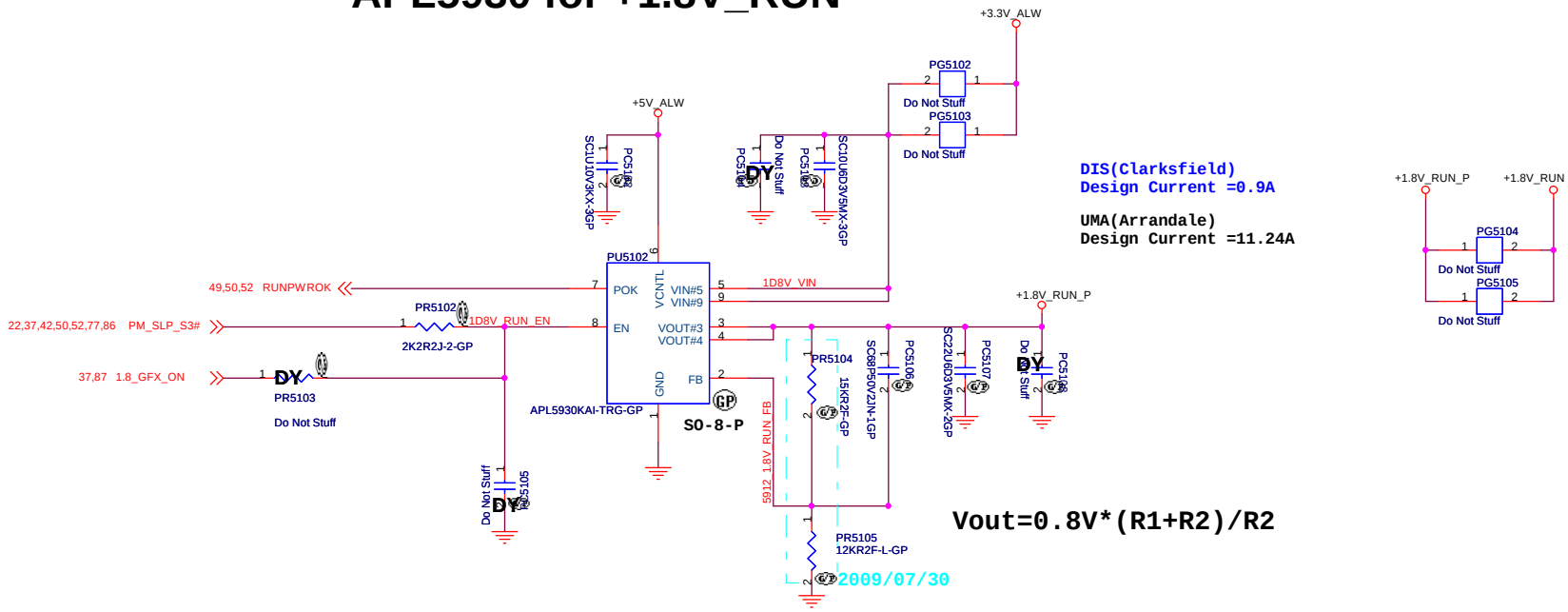
Title: TPS51116_+1.5V_SUS

Size	Document Number	Rev
Custom	DW Calpella	X00

Date: Tuesday, September 08, 2009 Sheet 50 of 90

SSID = PWR.Plane.Regulator_1p8v

APL5930 for +1.8V_RUN



UMA

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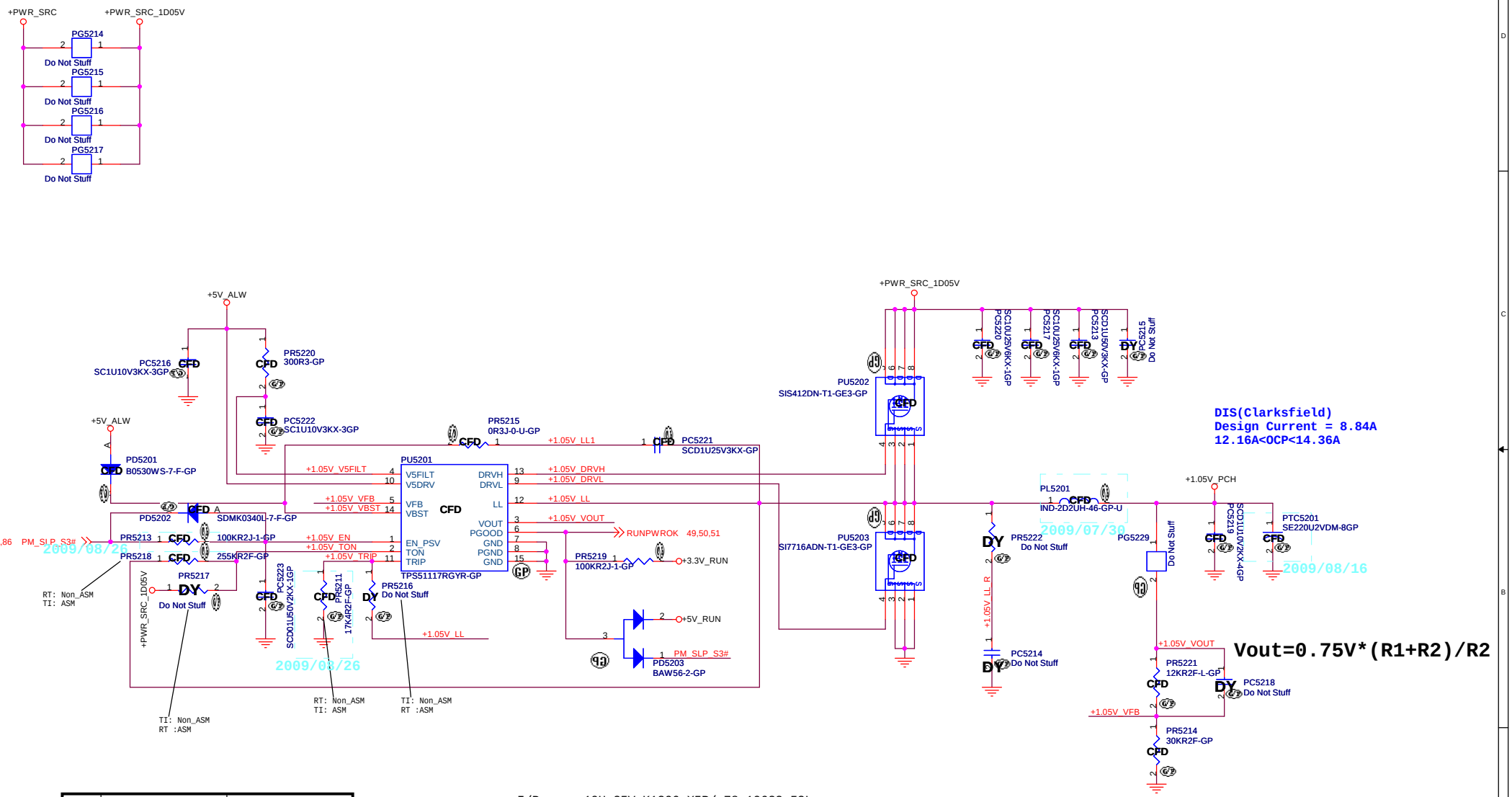
Taipei Hsien 221, Taiwan, R.O.C.

Title		
APL5930 +1.8V_RUN		
Size: A3	Document Number: DW Calpella	Rev: X00
Date: Tuesday, September 08, 2009	Sheet 51 of 90	

SSID = PWR.Plane.Regulator_1p05v



	ASM	Non_ASM
TI	PR5218, PR5211	PR5217, PR5216
RT	PR5217, PR5216	PR5218, PR5211

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor:2.2UH PCMC063T-2R2MN Cyntec DCR:20mohm Isat =14Arms 68.2R210.20B
O/P cap: 220U 2V EEFCX0D221R 15mOhm 2.7Arms PANASONIC/ 79.22719.20L
H/S: SIS412DN/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S: SI7716ADN/ 13.5mOhm/16.5mohm@4.5Vgs/ 84.07716.037
Switching freq-->320KHz

UMA

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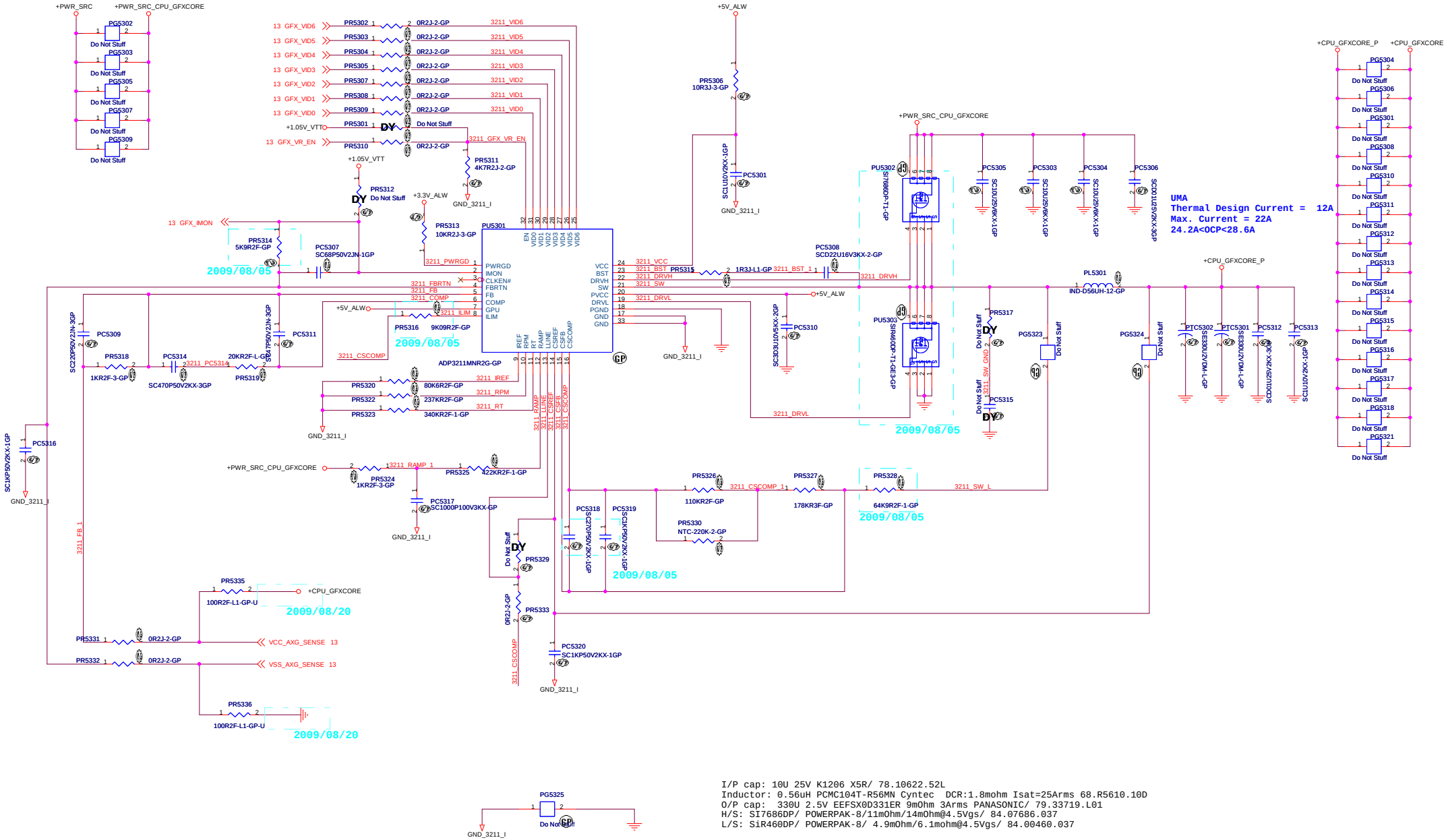
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC 1.05V

Size	Document Number	Rev
A3	DW Calpella (Clarksfield)	SA

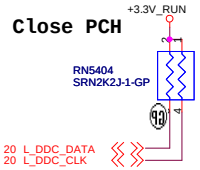
Date: Tuesday, September 08, 2009 Sheet 52 of 90

SSID = CPU.GFX.Regulator

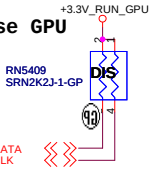


SSID = VIDEO

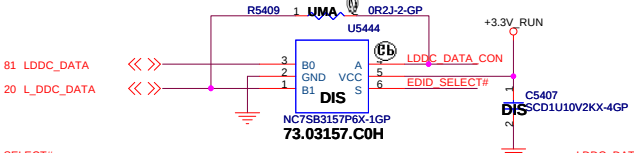
Close PCH



Close GPU

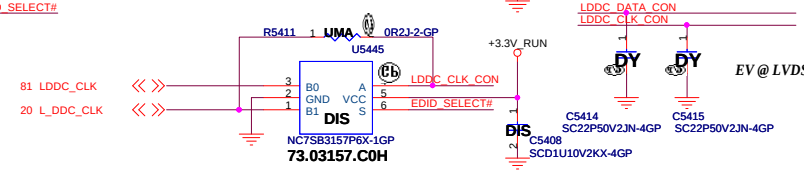


UMA/DIS LVDS DDC_CLK/DAT select circuit

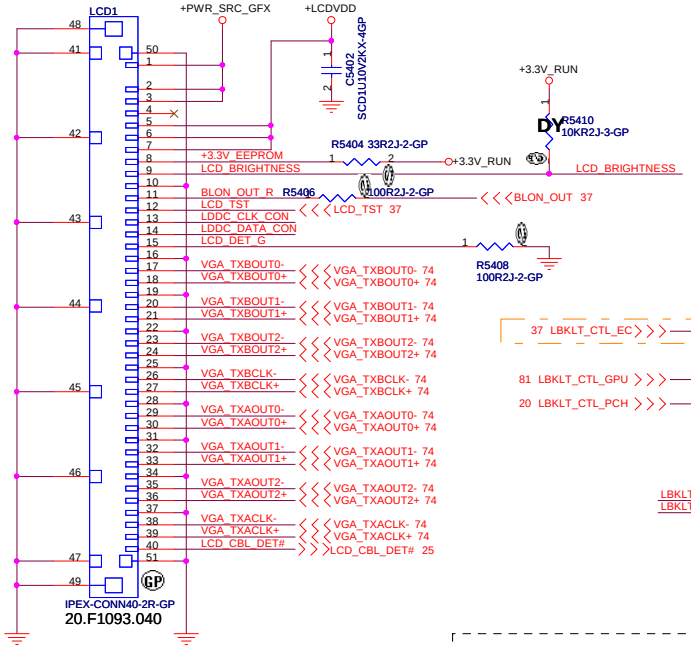


23,55,57 EDID_SELECT# >> EDID_SELECT#

H=>B1 -iGPU PCH (UMA)
L=>B0 -dGPU GPU (DIS)

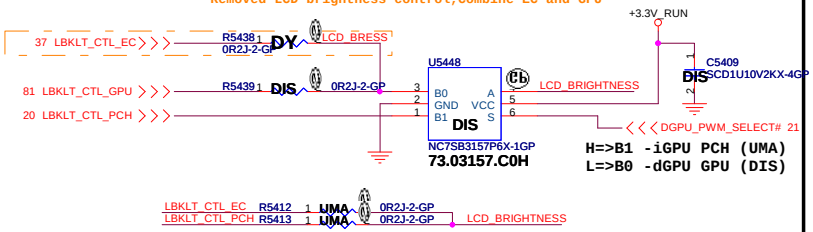


LVDS CONNECTOR

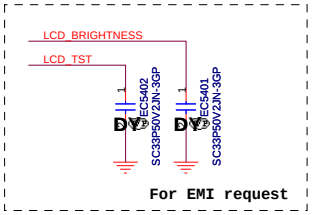


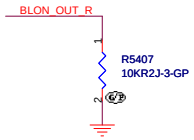
UMA/DIS LVDS PWM select circuit

2009/07/27
Added LCD brightness control by EC.
2009/07/29
Removed LCD brightness control,Combine EC and GPU



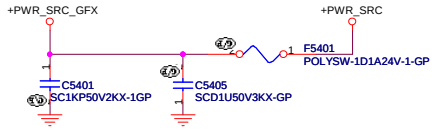
H=>B1 -iGPU PCH (UMA)
L=>B0 -dGPU GPU (DIS)





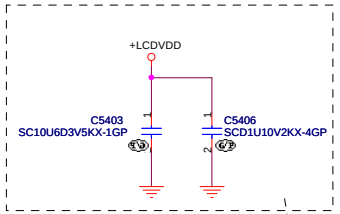
SSID = Inverter

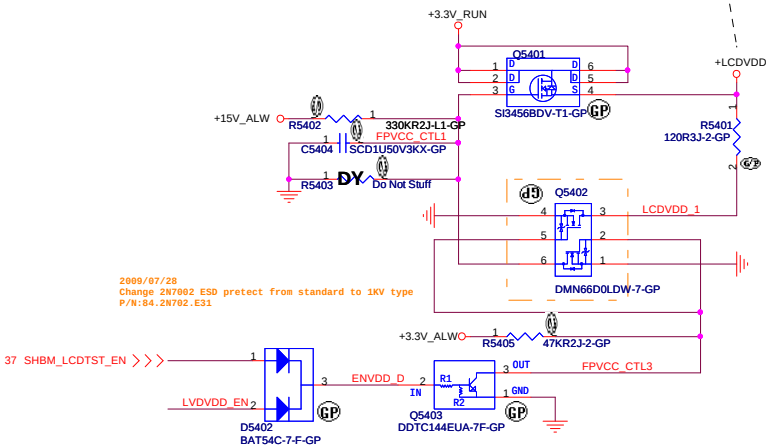
INVERTER POWER

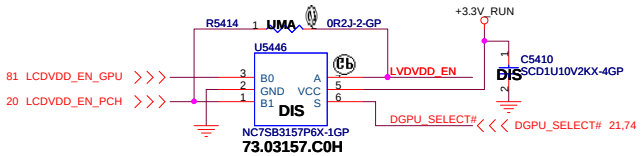


SSID = VIDEO

LCD POWER







H=>B1 -iGPU PCH (UMA)
L=>B0 -dGPU GPU (DIS)

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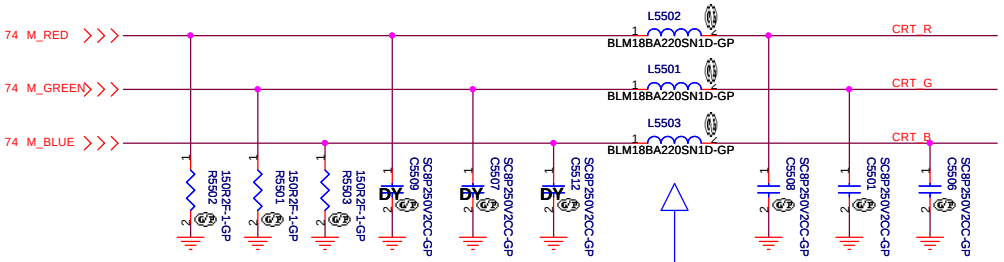
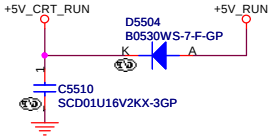
Title: LCD/Inverter Connector

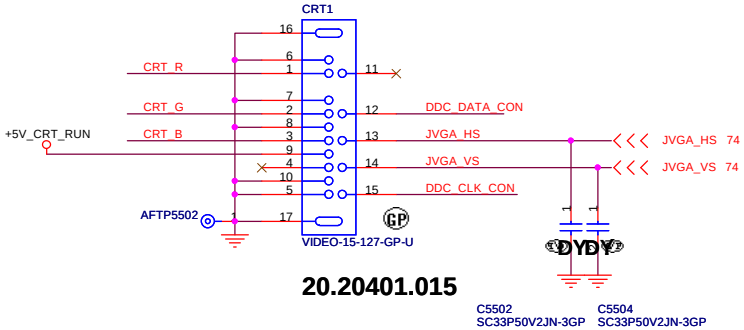
Size	Document Number	Rev
Custom	Vostro Calpella	SA

Date: Tuesday, September 08, 2009 Sheet 54 of 90

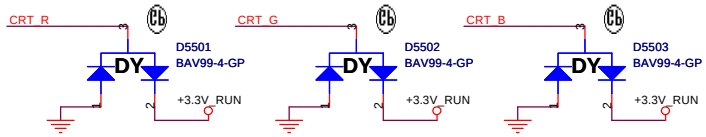
SSID = VIDEO





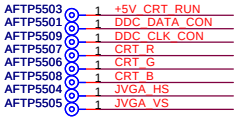


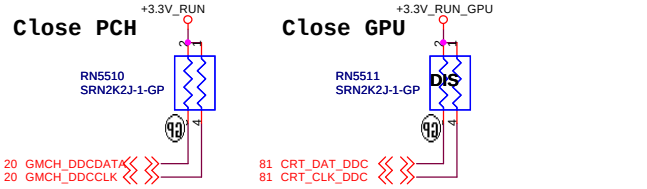
20.20401.015



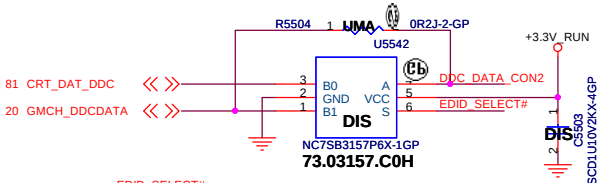
Layout Note:

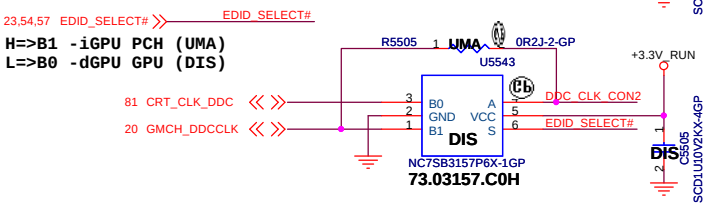
*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
* RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.

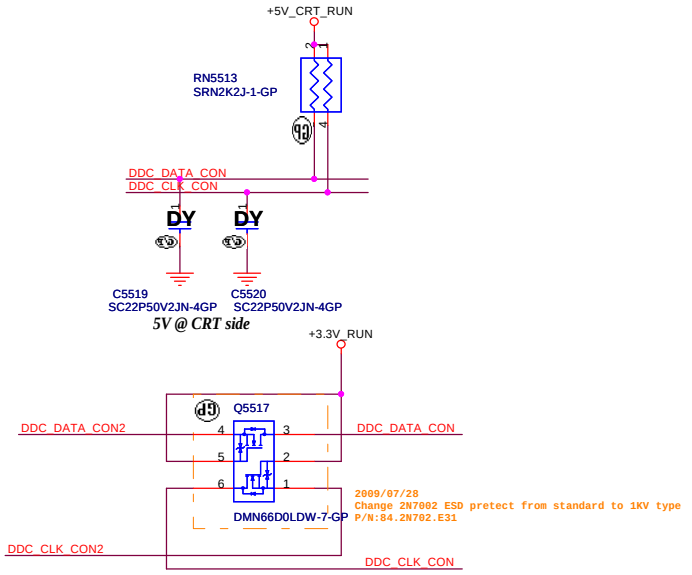




UMA/DIS CRT DDC CLK/DAT select circuit







UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: ***CRT Connector***		
Size: A3	Document Number: ***Vostro Calpella***	Rev: ***SA***
Date: Tuesday, September 08, 2009	Sheet 55 of 90	

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Title

(Reserve)

Size	Document Number	Rev
Custom	*Vostro Calpella*	*SA*

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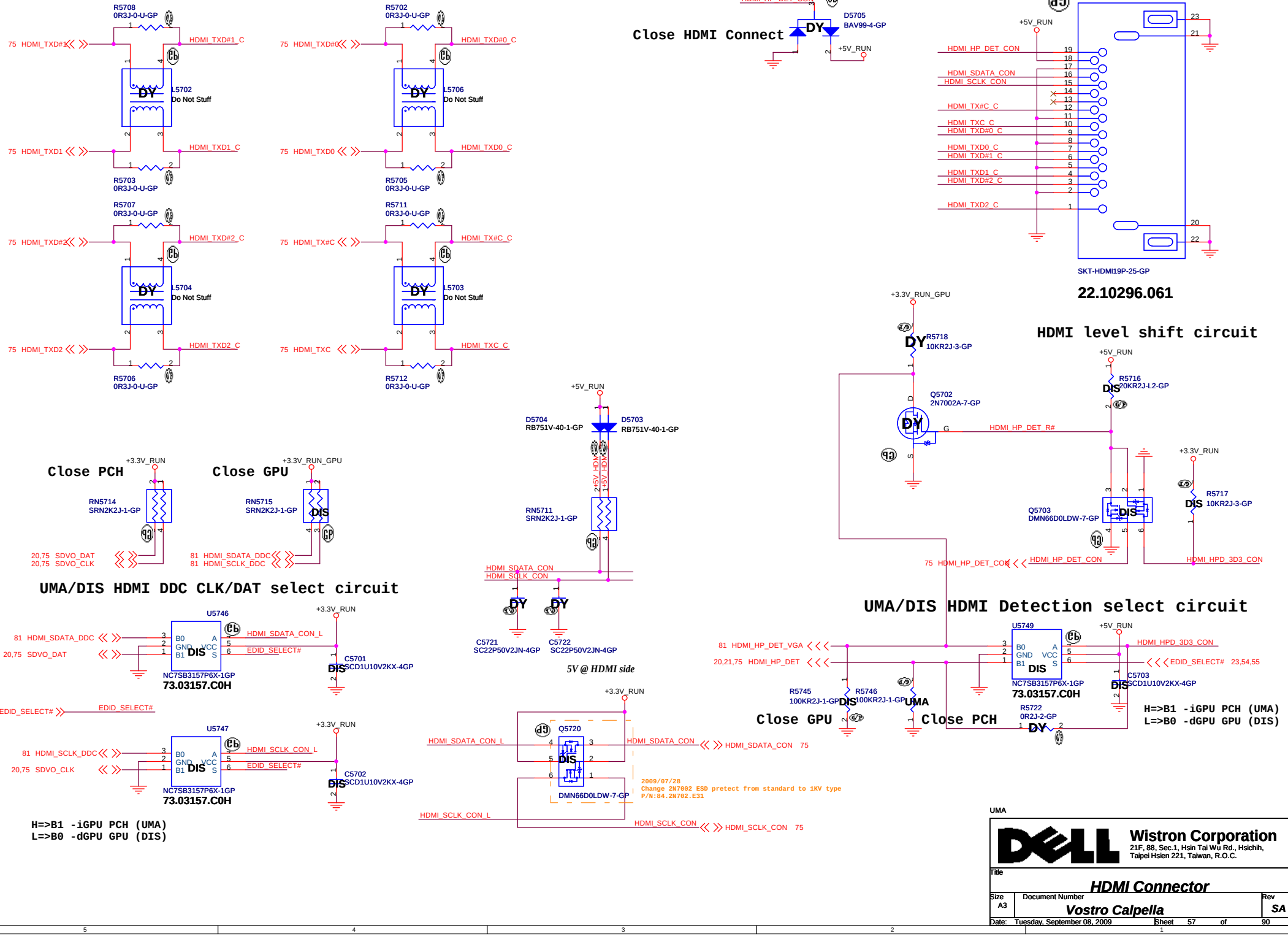
R5708 0R3J-0-U-GP
75 HDMI_TXD#1
HDMI_TXD#1_C
L5702 Do Not Stuff
75 HDMI_TXD1
HDMI_TXD1_C
R5703 0R3J-0-U-GP
R5702 0R3J-0-U-GP
75 HDMI_TXD#0
HDMI_TXD#0_C
L5706 Do Not Stuff
75 HDMI_TXD0
HDMI_TXD0_C
R5705 0R3J-0-U-GP
R5707 0R3J-0-U-GP
75 HDMI_TXD#2
HDMI_TXD#2_C
L5704 Do Not Stuff
75 HDMI_TXD2
HDMI_TXD2_C
R5706 0R3J-0-U-GP
R5711 0R3J-0-U-GP
75 HDMI_TX#C
HDMI_TX#C_C
L5703 Do Not Stuff
75 HDMI_TXC
HDMI_TXC_C
R5712 0R3J-0-U-GP
Close HDMI Connect
HDMI_HP_DET_CON
D5705 BAV99-4-GP
+5V_RUN
HDMI1
HDMI_HP_DET_CON
HDMI_SDATA_CON
HDMI_SCLK_CON
HDMI_TX#C_C
HDMI_TXC_C
HDMI_TXD#0_C
HDMI_TXD0_C
HDMI_TXD#1_C
HDMI_TXD1_C
HDMI_TXD#2_C
HDMI_TXD2_C
SKT-HDMI19P-25-GP
22.10296.061
HDMI level shift circuit
+3.3V_RUN_GPU
R5718 10KR2J-3-GP
Q5702 2N7002A-7-GP
HDMI_HP_DET_R#
R5716 20KR2J-L2-GP
Q5703 DMN66D0LDW-7-GP
R5717 10KR2J-3-GP
75 HDMI_HP_DET_CON
HDMI_HP_DET_CON
HDMI_HPD_3D3_CON
Close PCH
+3.3V_RUN
RN5714 SRN2K2J-1-GP
20,75 SDVO_DAT
20,75 SDVO_CLK
Close GPU
+3.3V_RUN_GPU
RN5715 SRN2K2J-1-GP
81 HDMI_SDATA_DDC
81 HDMI_SCLK_DDC
D5704 RB751V-40-1-GP
D5703 RB751V-40-1-GP
+5V_RUN
+5V HDMI
RN5711 SRN2K2J-1-GP
HDMI_SDATA_CON
HDMI_SCLK_CON
C5721 SC22P50V2JN-4GP
C5722 SC22P50V2JN-4GP
5V @ HDMI side
UMA/DIS HDMI DDC CLK/DAT select circuit
U5746
81 HDMI_SDATA_DDC
20,75 SDVO_DAT
B0 B1 GND VCC A S
HDMI_SDATA_CON_L
EDID_SELECT#
+3.3V_RUN
C5701 SCD1U10V2KX-4GP
NC7SB3157P6X-1GP
73.03157.C0H
23,54,55 EDID_SELECT#
EDID_SELECT#
U5747
81 HDMI_SCLK_DDC
20,75 SDVO_CLK
HDMI_SCLK_CON_L
EDID_SELECT#
+3.3V_RUN
C5702 SCD1U10V2KX-4GP
NC7SB3157P6X-1GP
73.03157.C0H
H=>B1 -iGPU PCH (UMA)
L=>B0 -dGPU GPU (DIS)
+3.3V_RUN
Q5720
HDMI_SDATA_CON_L
HDMI_SDATA_CON
HDMI_SDATA_CON 75
DMN66D0LDW-7-GP
2009/07/28
Change 2N7002 ESD pretect from standard to 1KV type
P/N:84.2N702.E31
HDMI_SCLK_CON_L
HDMI_SCLK_CON
HDMI_SCLK_CON 75
UMA/DIS HDMI Detection select circuit
81 HDMI_HP_DET_VGA
20,21,75 HDMI_HP_DET
U5749
B0 B1 GND VCC A S
HDMI_HPD_3D3_CON
EDID_SELECT# 23,54,55
C5703 SCD1U10V2KX-4GP
NC7SB3157P6X-1GP
73.03157.C0H
+5V_RUN
R5745 100KR2J-1-GP
R5746 100KR2J-1-GP
UMA
R5722 0R2J-2-GP
Close GPU
Close PCH
H=>B1 -iGPU PCH (UMA)
L=>B0 -dGPU GPU (DIS)
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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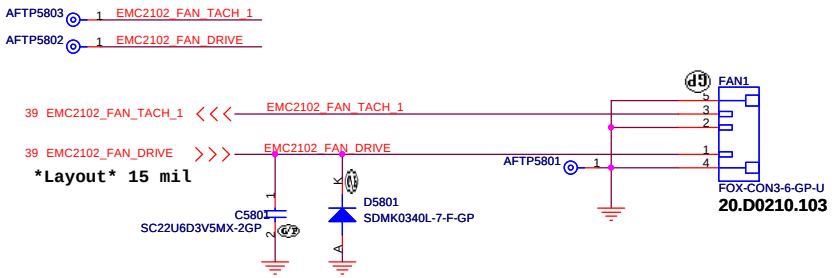
Title
HDMI Connector
Size A3
Document Number
Vostro Calpella
Rev SA
Date: Tuesday, September 08, 2009
Sheet 57 of 90

SSID = Thermal

Fan Connector



UMA

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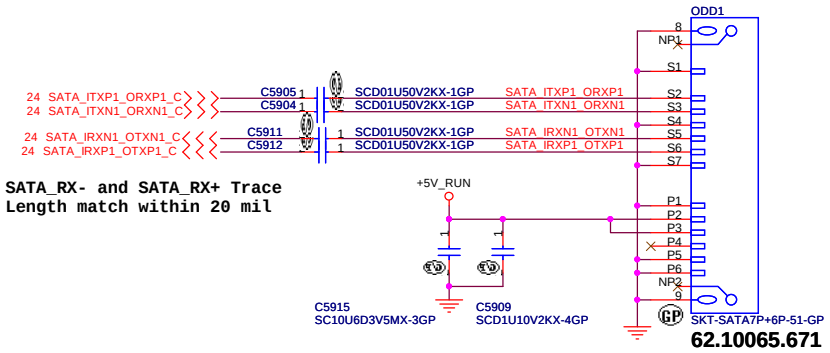
Title	58_FAN	
Size: A3	Document Number: Vostro Calpella	Rev: SA
Date: Tuesday, September 08, 2009	Sheet 58 of 90	

SSID = SATA

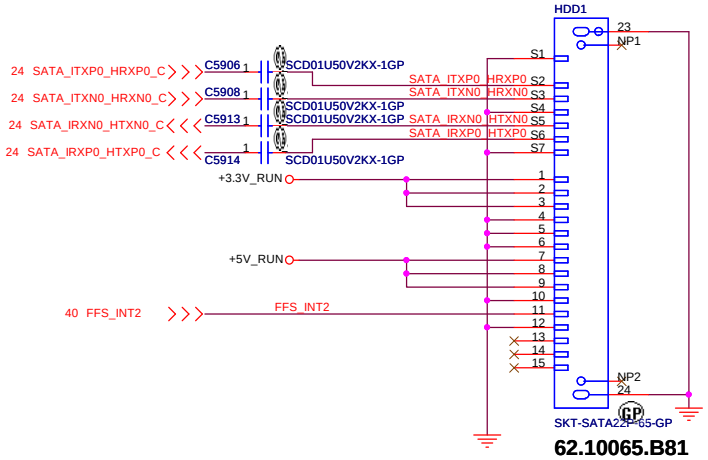
ODD Connector



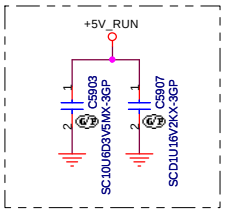
SATA_RX- and SATA_RX+ Trace
Length match within 20 mil

SSID = SATA

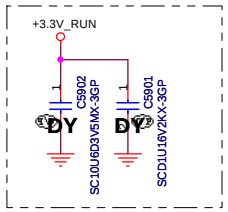
SATA HDD Connector



Close to CONN
5V power pin



Close to CONN
3.3V power pin




```
SATA HDD Interface comment
*******************************
--- GND
RX+
RX-
--- GND
TX-
TX+
--- GND
*******************************
------------ 3.3V
------------ 3.3V
------------ 3.3V
--- GND
--- GND / Dell Detected Pin
--- GND
------------ 5V
------------ 5V
------------ 5V
--- GND
(Dell: FFS_INT for supported HDD)
--- GND
------------ 12V
------------ 12V
------------ 12V
*******************************
```

UMA

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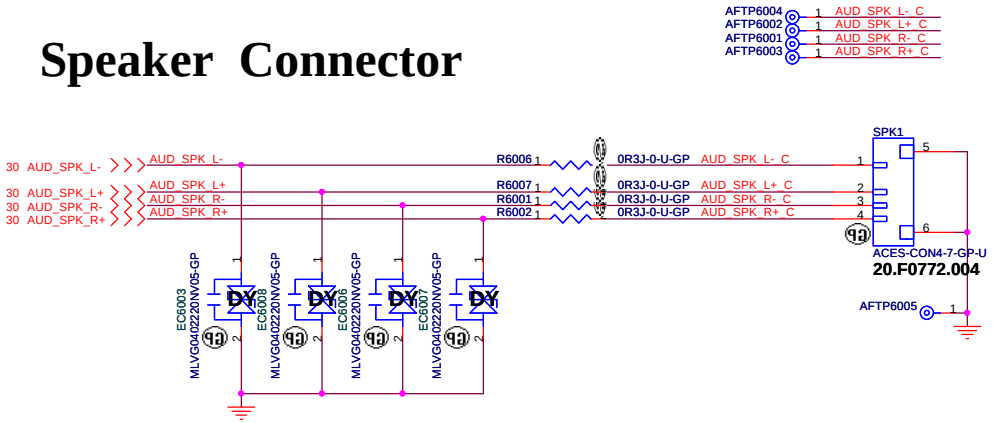
Title		
HDD/ODD Connector		
Size: A3	Document Number: Vostro Calpella	Rev: SA
Date: Tuesday, September 08, 2009	Sheet 59 of 90	

SSID = AUDIO

Speaker Connector



UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title	***Speaker/HP/MIC Jack***	
Size: A3	Document Number: ***Vostro Calpella***	Rev: ***SA***
Date: Tuesday, September 08, 2009	Sheet 60 of 90	

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Title: *(Reserve)*

Size	Document Number	Rev
A3	*Vostro Calpella*	*SA*

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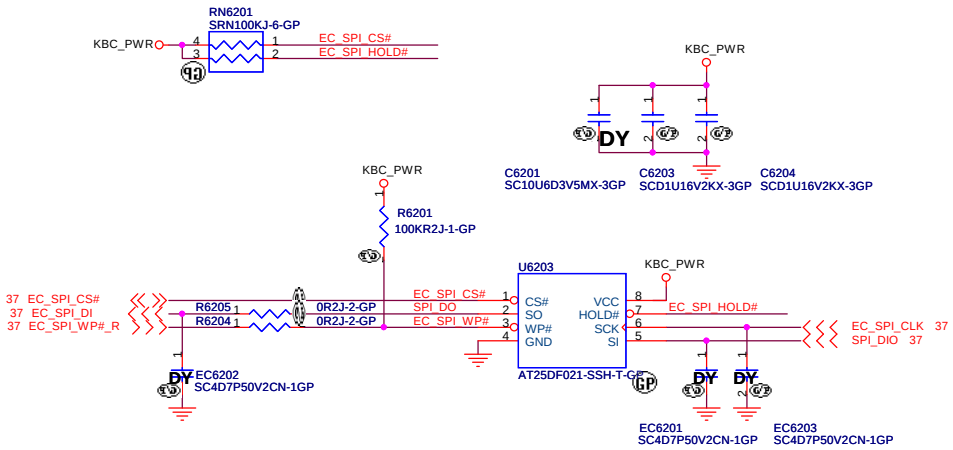
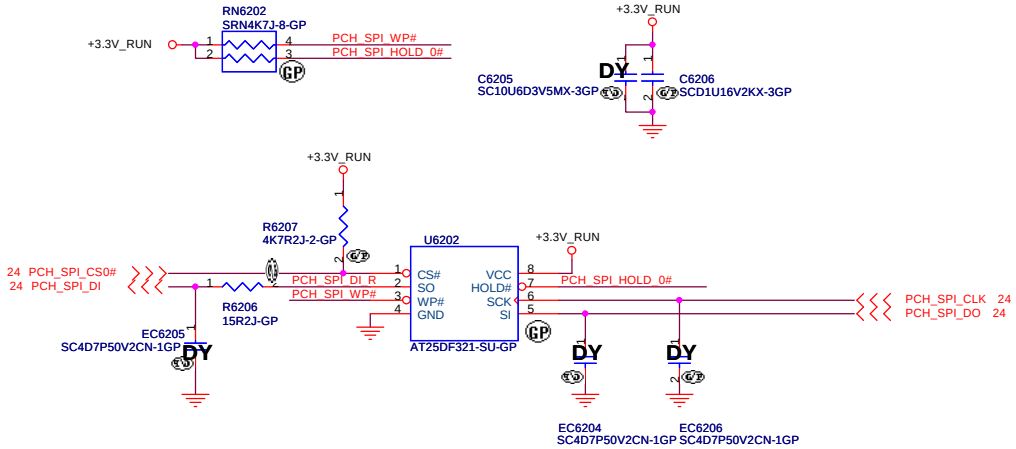
SSID = Flash.ROM

SPI FLASH ROM (256K Bytes) for KBC

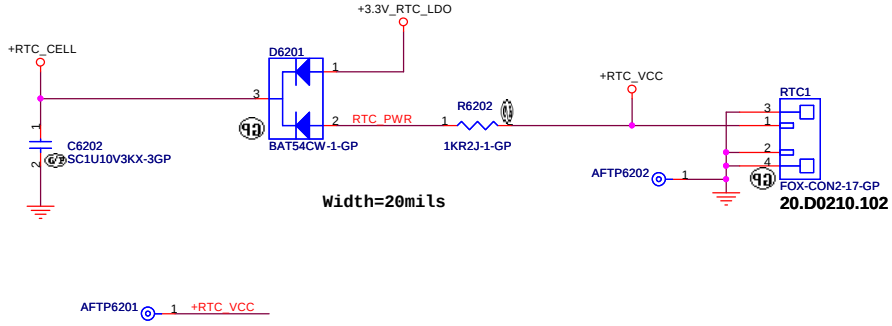


SPI FLASH ROM (4M Bytes) for PCH



SSID = RBATT

RTC Connector



UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

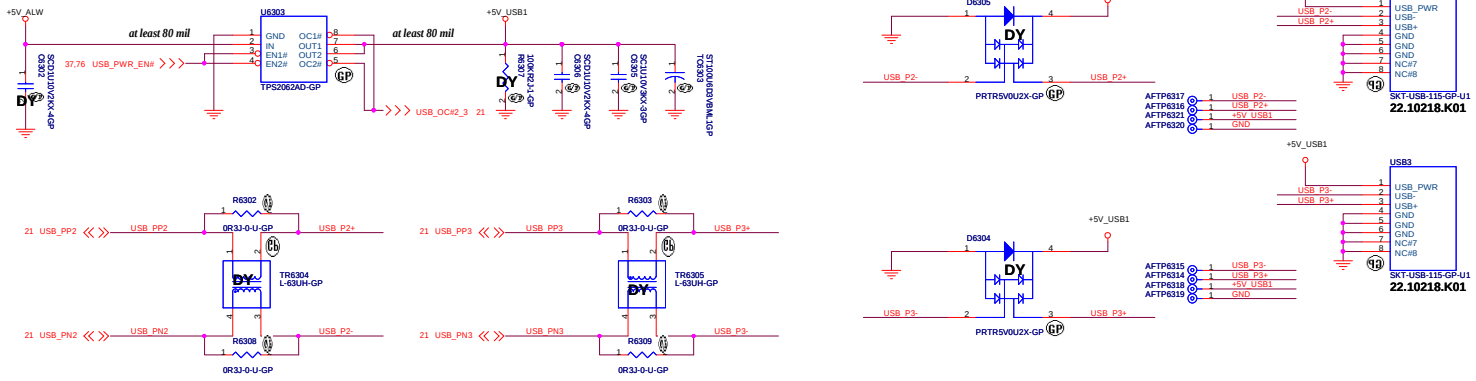
Title: EEPROM/RTC Connector

Size	Document Number	Rev
A3	Vostro Calpella	SA

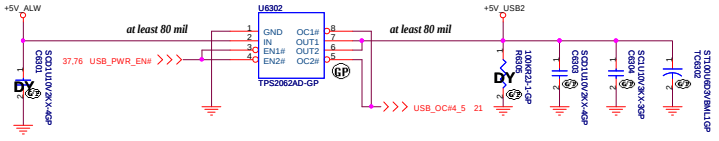
Date: Tuesday, September 08, 2009 Sheet 62 of 90

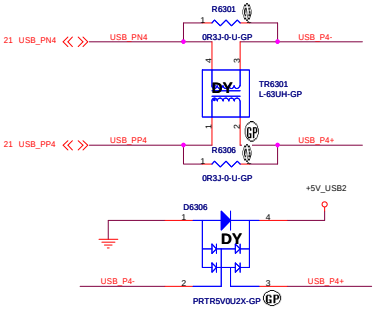
SSID = USB

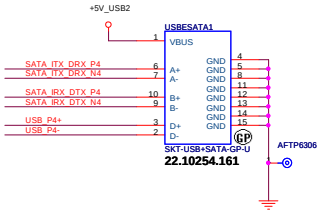
USB Power

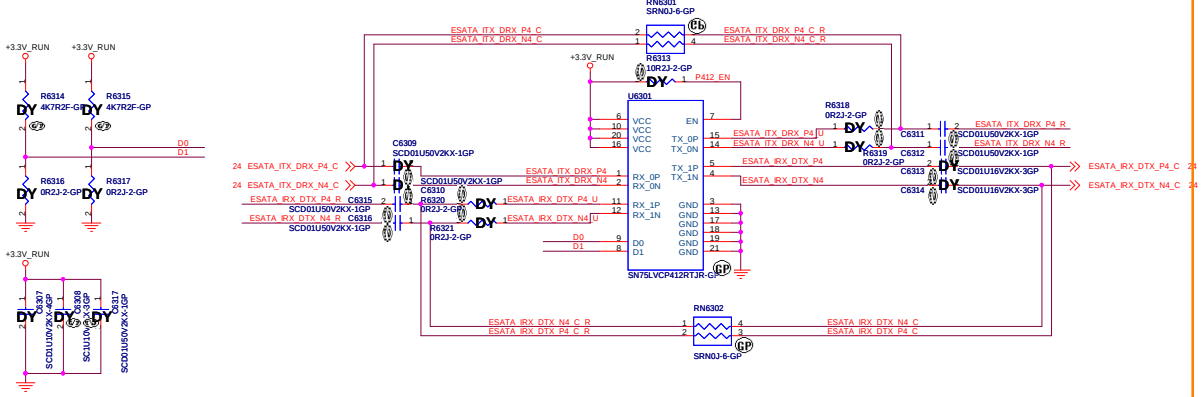


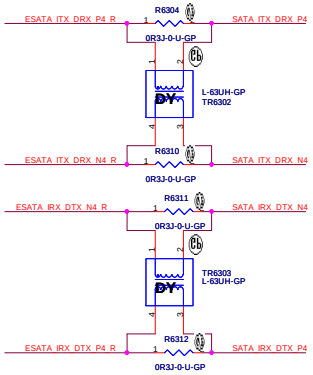
ESATA Power











	If you added U6301(SN75LVCP412RTJR-GP). You need to BOM change
ASM	R6313, R6314, R6315, R6318, R6319, R6320, R6321 C6309, C6310, C6313, C6314, C6307, C6308, C6317
DY	RN6301, RN6302

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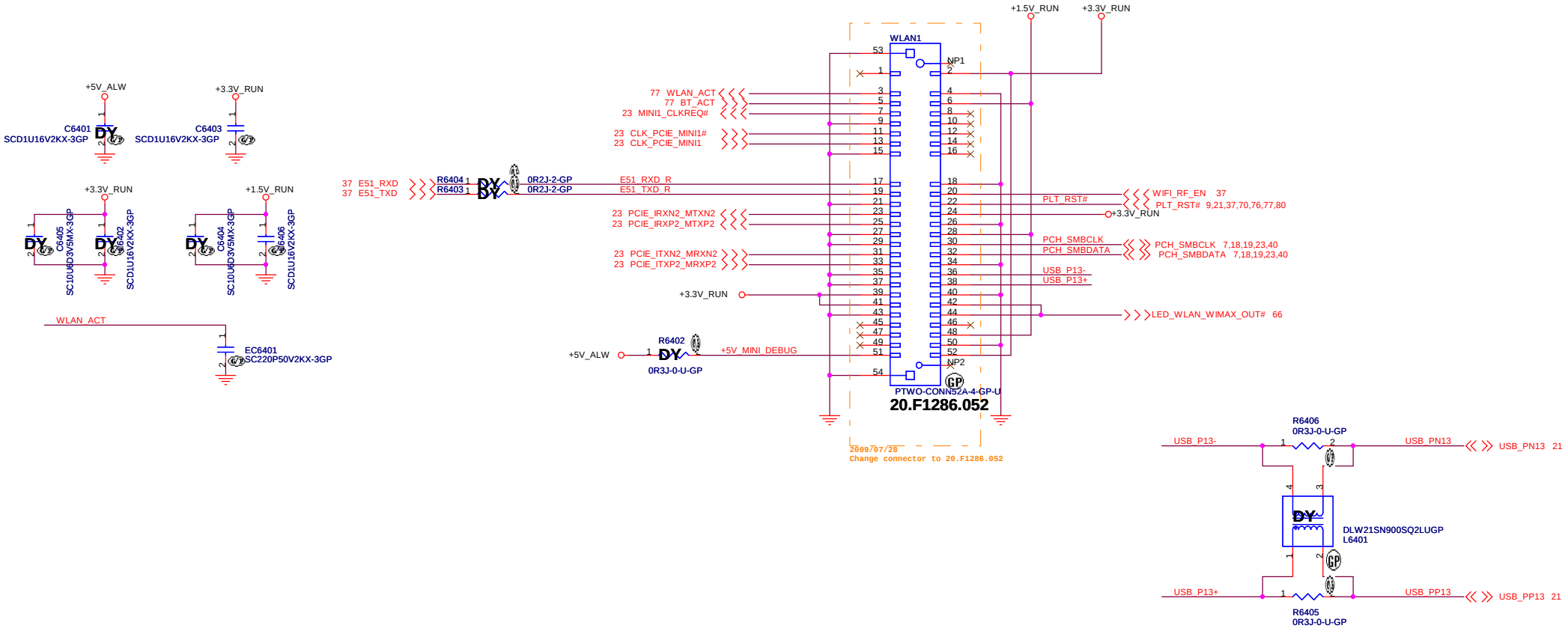
Title: USB /ESATA Port

Size: A2 | Document Number: Vostro Calpella | Rev: SA

Date: Tuesday, September 08, 2009 | Sheet 63 of 90

SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



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Taipei Hsien 221, Taiwan, R.O.C.

Title: *MINICARD(WLAN)/ITP CONN*

Size	Document Number	Rev
A3	*Vostro Calpella*	*SA*

Date: Tuesday, September 08, 2009 Sheet 64 of 90

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Title

WWAN Connector

Size	Document Number	Rev
A3	***Vostro Calpella***	***SA***

Date: Tuesday, September 08, 2009 Sheet 65 of 90

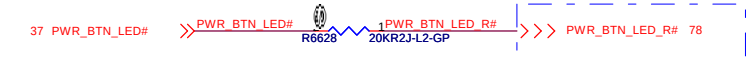
For LED & Capacity board:

LED Type	Color	Power rail
SCRL LED	White	ALW
CAP LED	White	ALW
NUM LED	White	ALW
PWR BTN LED	White	ALW
SATA ACT LED1	White	RUN
BT ACT LED	White	RUN
WLAN WIMAX LED	White	RUN

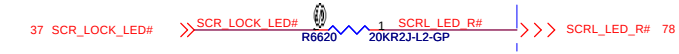
For IO board:

LED Type	Color	Power rail
PWR LED2	White(Multi-color)	ALW
BATTERY LED2	Amber(Multi-color)	ALW
	White(Multi-color)	ALW

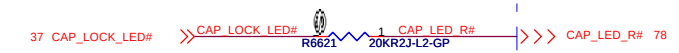
PWR BTN LED



SCRLK LED

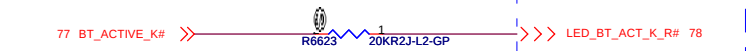


CAPS LED



NUM LED

Bluetooth LED



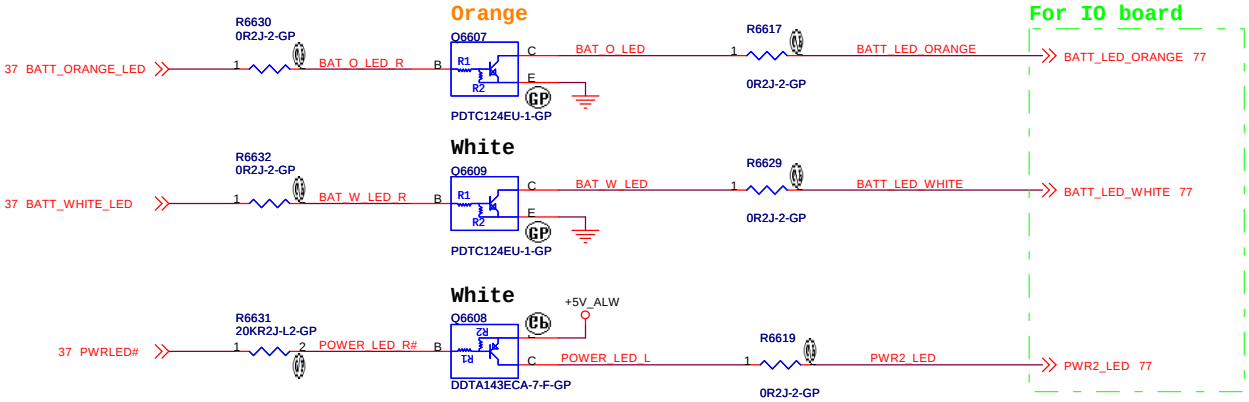
WLAN LED

HD LED

2009/07/29
Update R6625 from 10k to 20k ohm

Power & Battery LED

2009/08/12
Changed battery LED be one LED with bi-color (white and amber). For I/O board. Update Spec.



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Title: LED

Size	Document Number	Rev
A3	Vostro Calpella	SA

Date: Tuesday, September 08, 2009 Sheet 66 of 90

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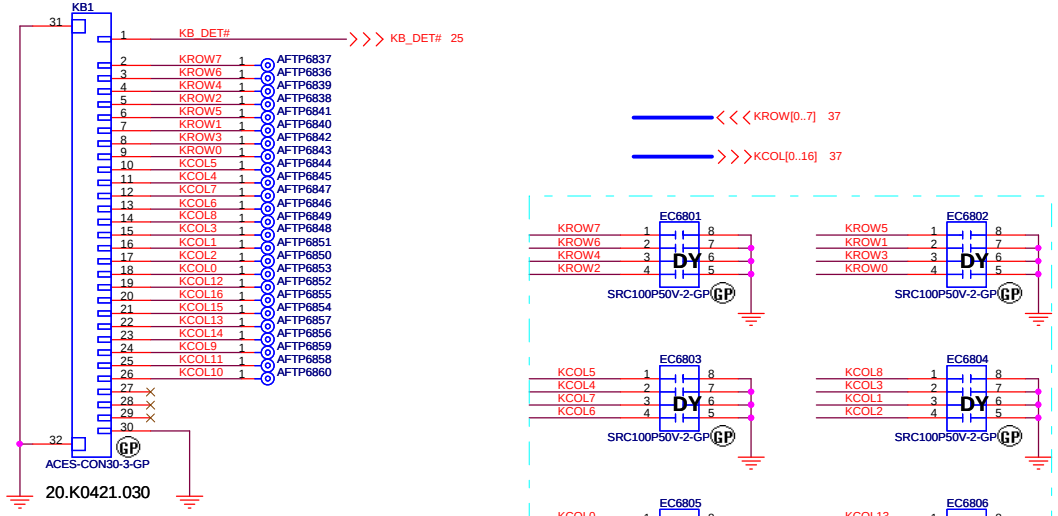
Title: *(Reserve)*

Size	Document Number	Rev
A2	*Vostro Calpella*	*SA*

Date: Tuesday, September 08, 2009 Sheet 67 of 90

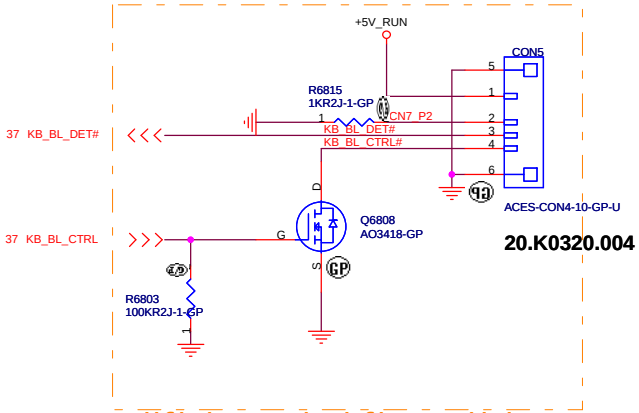
SSID = KBC

Internal KeyBoard Connector



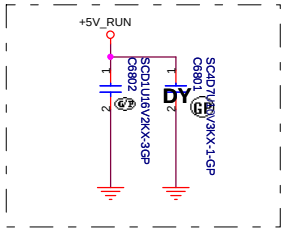
Added KB1 EMI Cap
2009/06/17

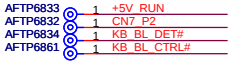
KB Backlight CONN



Modified CON5 pin define & added N-MOS
2009/07/17

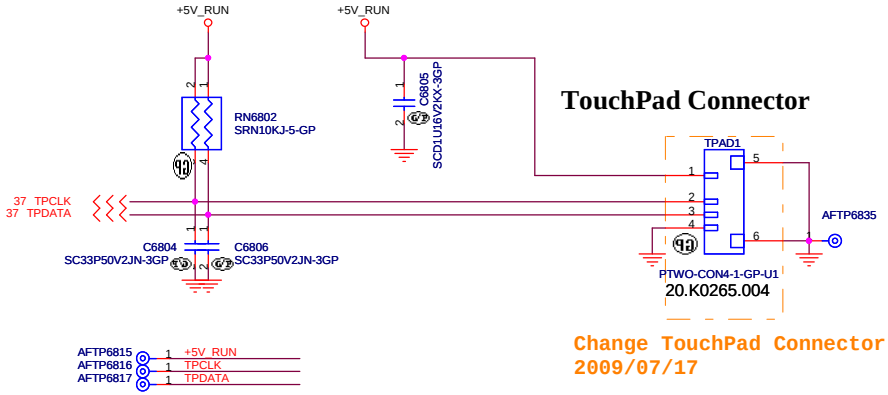
Place near CON5





SSID = Touch.Pad

TouchPad Connector



Change TouchPad Connector
2009/07/17

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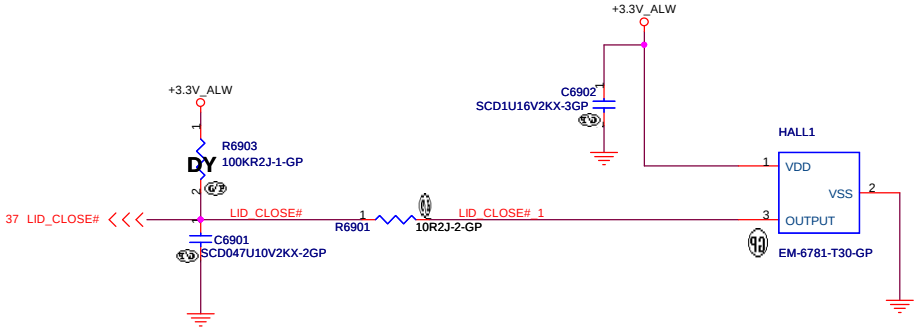
Title: Keyboard/Touch Pad

Size	Document Number	Rev
Custom	Vostro Calpella	SA

Date: Tuesday, September 08, 2009 Sheet 68 of 90

Hall Sensor Connector



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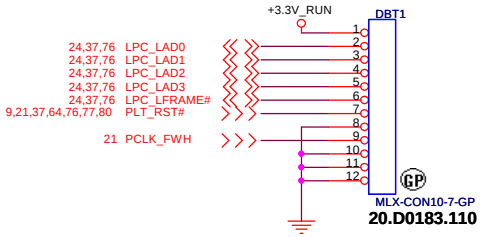
Title: ***Hall sensor***

Size	Document Number	Rev
A3	***Vostro Calpella***	***SA***

Date: Tuesday, September 08, 2009 Sheet 69 of 90

GOLDEN FINGER FOR DEBUG BOARD



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Title: ***Debug port***

Size	Document Number	Rev
A3	***Vostro Calpella***	***SA***

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UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *PX Swith-2*

Size: A3 | Document Number: *Vostro Calpella* | Rev: *SA*

Date: Tuesday, September 08, 2009 | Sheet 71 of 90

UMA

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Title

Braidwood

Size	Document Number	Rev
A3	***Vostro Calpella***	***SA***

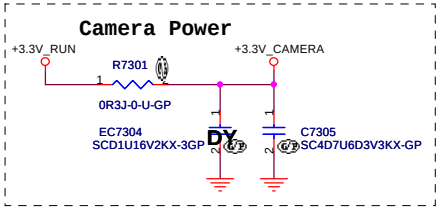
Date: Tuesday, September 08, 2009 Sheet 72 of 90

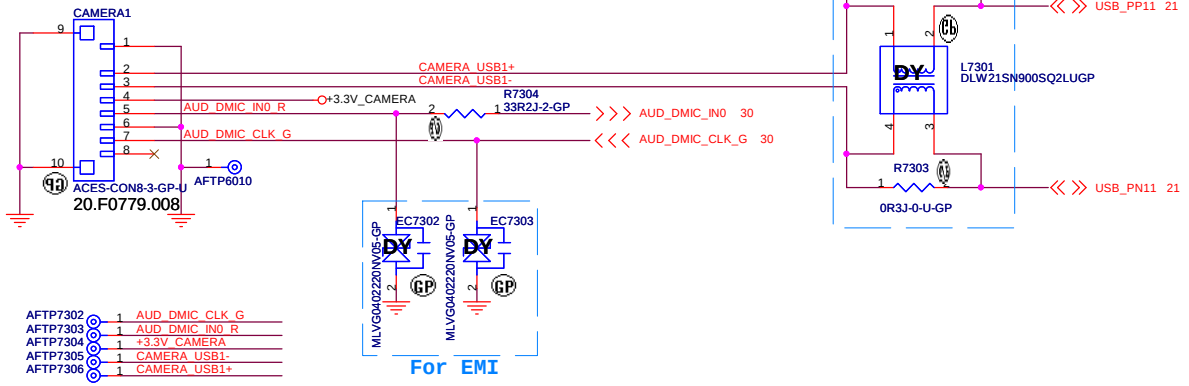
SSID = User.Interface

Camera Connector

2009/07/31
Change CAMERA1 connector pin define.
For cable is already to be finished

Camera Power





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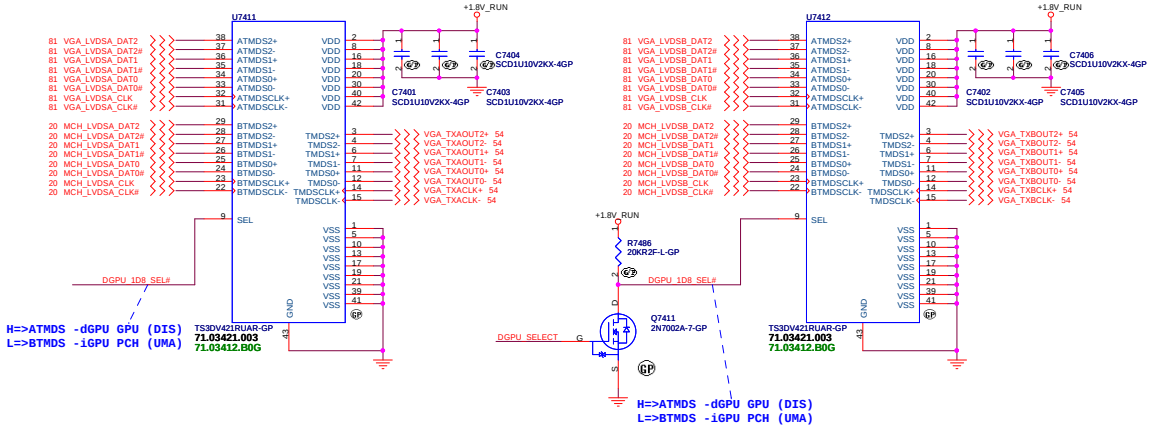
Title: Camera Connector		
Size: A3	Document Number: Vostro Calpella	Rev: SA
Date: Tuesday, September 08, 2009	Sheet 73 of 90	

UMA/DIS LVDS signal select circuit



FUNCTION TABLE

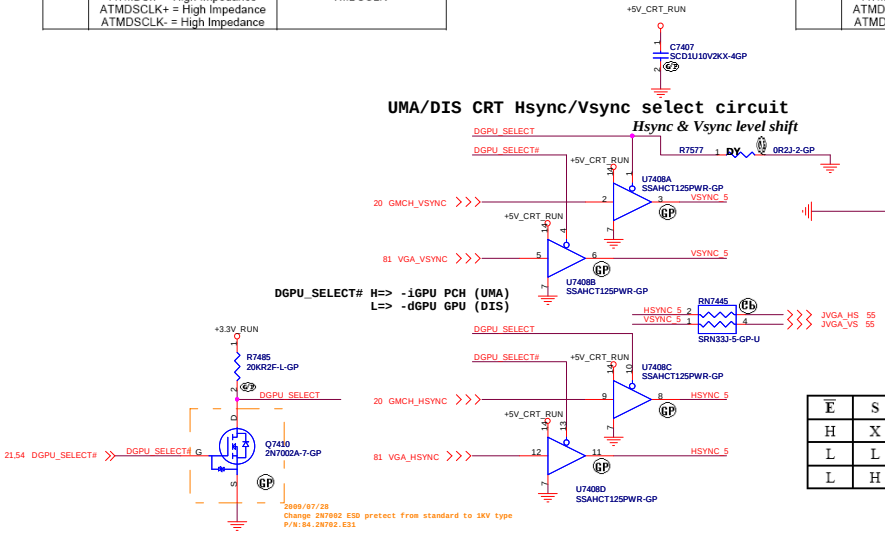
SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-

FUNCTION TABLE

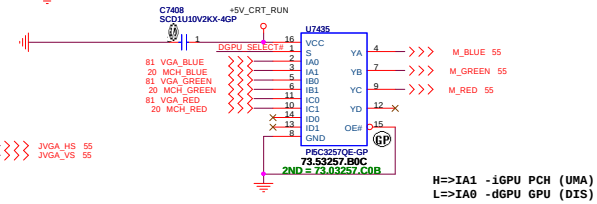
SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-

UMA/DIS CRT Hsync/Vsync select circuit

Hsync & Vsync level shift



UMA/DIS CRT signal select circuit



$\overline{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

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Title: PX Swith-1

Size: Custom | Document Number: Vostro Calpella | Rev: SA

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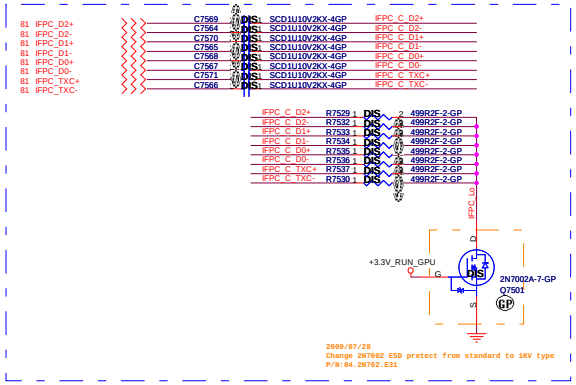
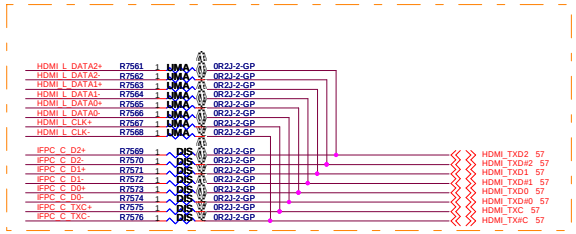
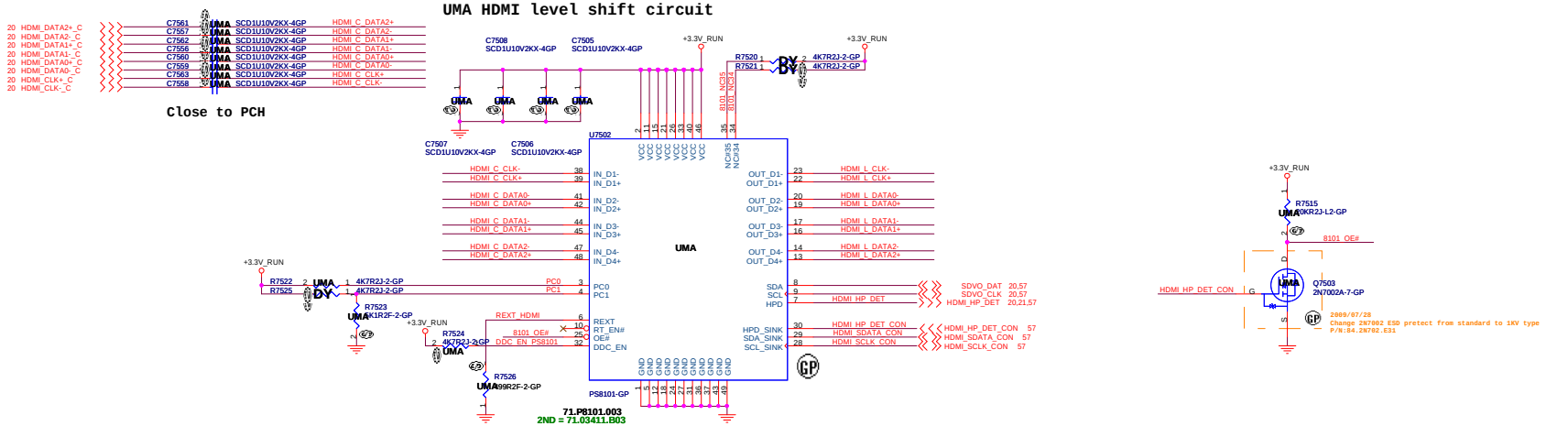
Close to connector



UMA/DIS HDMI signal select circuit



UMA HDMI level shift circuit



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Title: *(Reserve)*

Size	Document Number	Rev
A2	*Vostro Calpella*	SA

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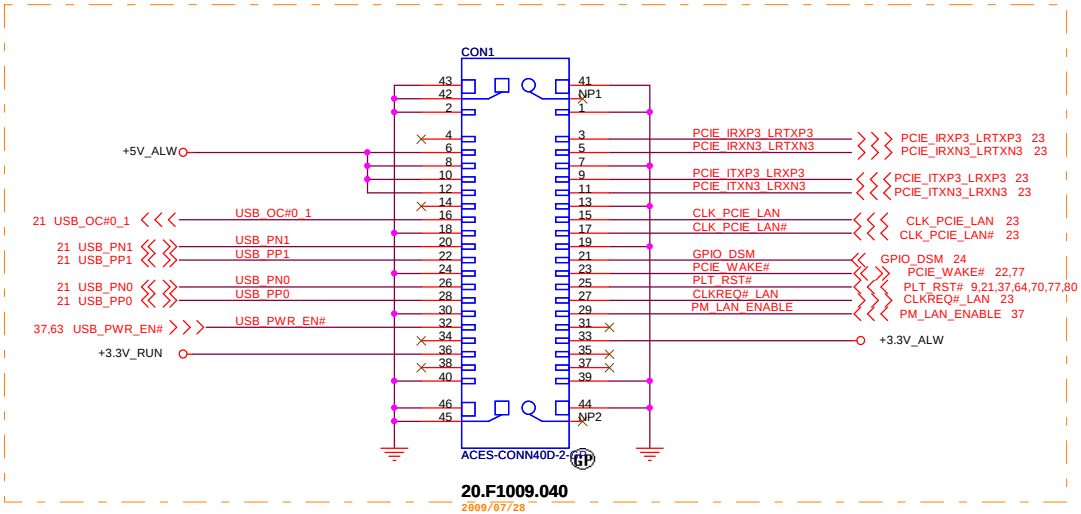
LAN baord CON

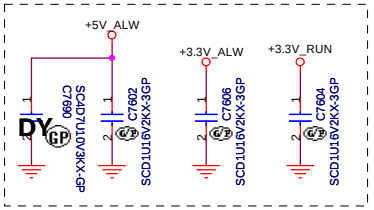


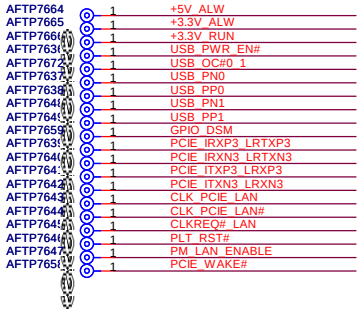
20.F1009.040

2009/07/28
Change connector to 20.F0692.060
2009/08/17
Change connector to 20.F1044.040
and chenge pin define
2009/08/25
Change connector to 20.F1009.040

2009/07/27
Change TPM to connector
2009/07/30
Change TPM1 connector to 20.K0238.010

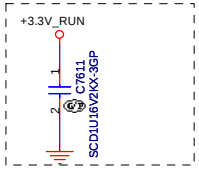
Place near CON1

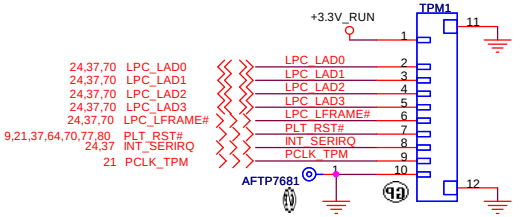




TPM board CON

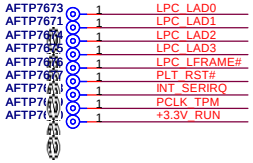
Place near TPM1





+3.3V_RUN : 30mA

20.K0238.010



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Title: ***LAN Board Connector***

Size	Document Number	Rev
A3	***Vostro Calpella***	SA

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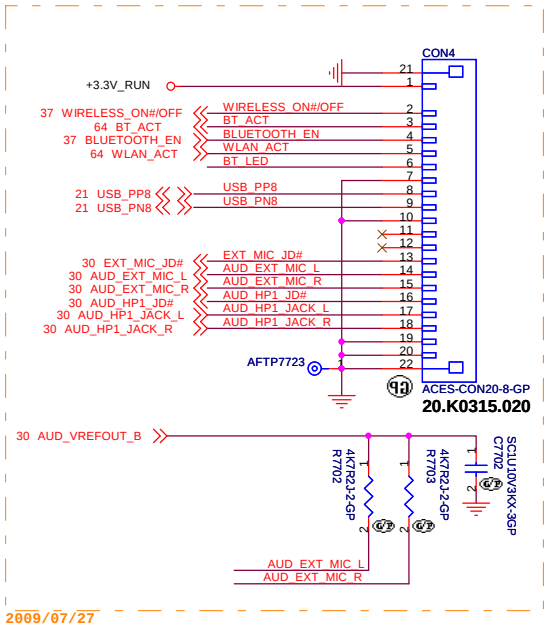
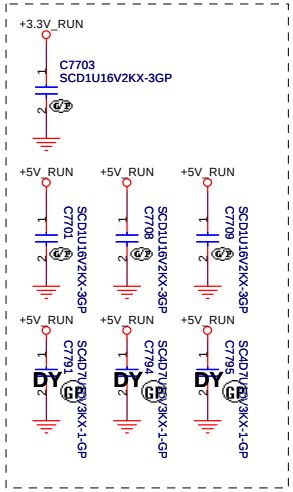
SSID = User.Interface

Audio board CON

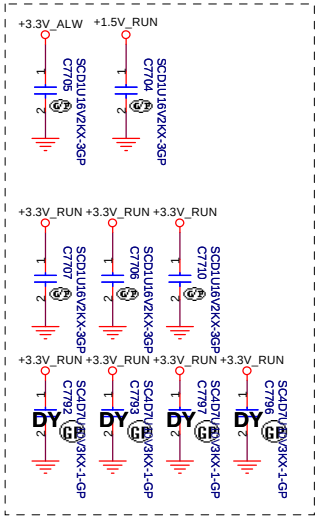


2009/07/27
Change CON4 PIN define
Remove +15V_ALW
2009/07/29
Change CON4 connector to 20.K0275.028
And change CON4 pin define
2009/08/03
Change CON4 pin define.
2009/08/18
Change CON4 connector P/N:20.K0315.020
2009/08/19
Remove AUD_VREFOUT_B from Audio board to main board.

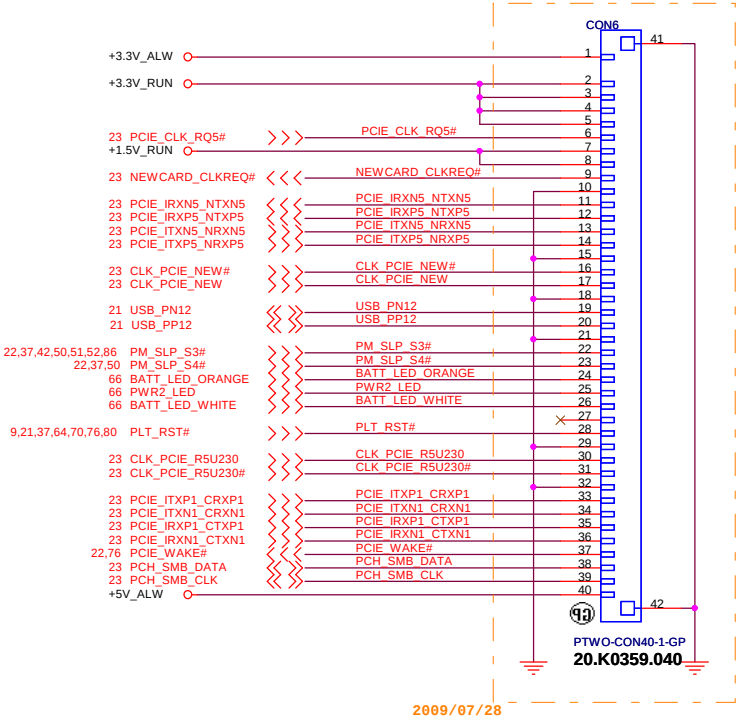
Place near CON4



Place near CON6



IO baord CON



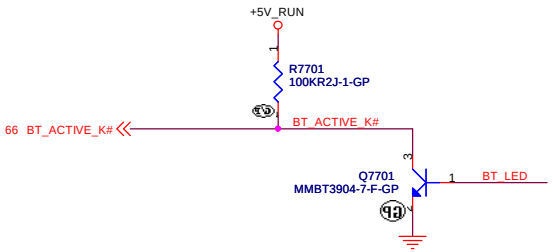
2009/07/28
Change CON6 connector to 20.K0286.040
2009/08/05
Change CON6 pin define
2009/08/12
Change CON6 pin define

AFTP7706 +3.3V_RUN
AFTP7709 WIRELESS_ON#/OFF

AFTP7702 WLAN_ACT
AFTP7703 BLUETOOTH_EN
AFTP7704 BT_LED
AFTP7705 BT_ACT
AFTP7707 USB_PP8
AFTP7708 USB_PN8

AFTP7713 EXT_MIC_JD#
AFTP7714 AUD_EXT_MIC_L
AFTP7715 AUD_EXT_MIC_R
AFTP7716 AUD_HP1_JD#
AFTP7717 AUD_VREFOUT_B
AFTP7718 AUD_HP1_JACK_L
AFTP7719 AUD_HP1_JACK_R

AFTP7786 PCIE_CLK_RQ5#
AFTP7758 +3.3V_ALW
AFTP7757 +3.3V_RUN
AFTP7760 +1.5V_RUN
AFTP7762 USB_PN12
AFTP7759 USB_PP12
AFTP7761 PCIE_IRXN5_NTXN5
AFTP7765 PCIE_IRXP5_NTXP5
AFTP7764 PCIE_ITXN5_NRXN5
AFTP7763 PCIE_ITXP5_NRXP5
AFTP7771 CLK_PCIE_NEW#
AFTP7770 CLK_PCIE_NEW
AFTP7766 PCIE_WAKE#
AFTP7769 NEWCARD_CLKREQ#
AFTP7768 PCH_SMB_CLK
AFTP7767 PCH_SMB_DATA
AFTP7777 PM_SLP_S3#
AFTP7776 PM_SLP_S4#
AFTP7774 BATT_LED_WHITE
AFTP7773 BATT_LED_ORANGE
AFTP7772 PWR2_LED
AFTP7775 CLK_PCIE_R5U230
AFTP7780 CLK_PCIE_R5U230#
AFTP7779 PCIE_ITXP1_CRXP1
AFTP7778 PCIE_ITXN1_CRXN1
AFTP7783 PCIE_IRXP1_CTXP1
AFTP7782 PCIE_IRXN1_CTXN1
AFTP7781 PLT_RST#



UMA

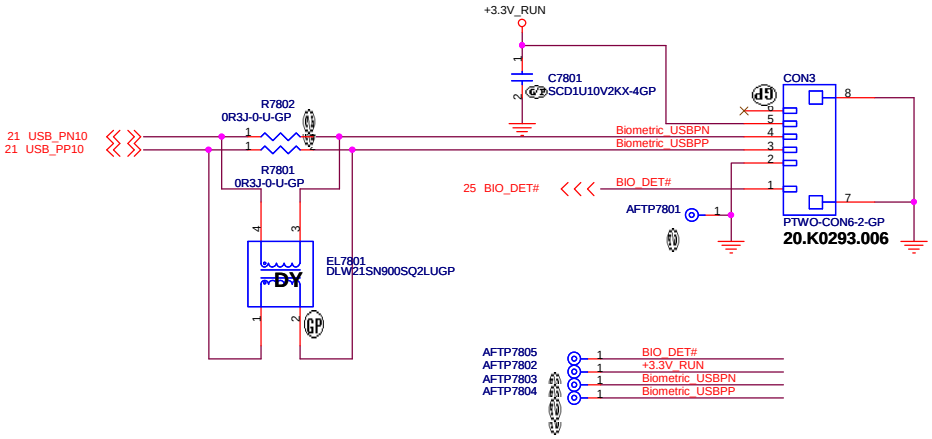
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board/Audio Board Connector

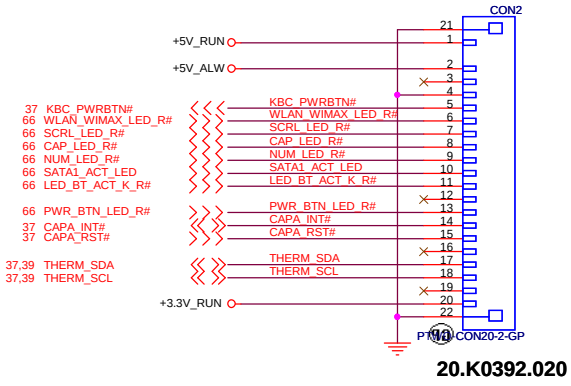
Size	Document Number	Rev
A3	Vostro Calpella	SA

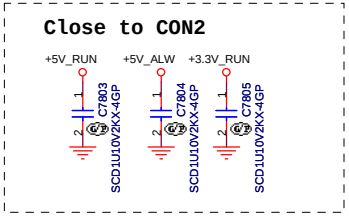
Date: Tuesday, September 08, 2009 Sheet 77 of 90

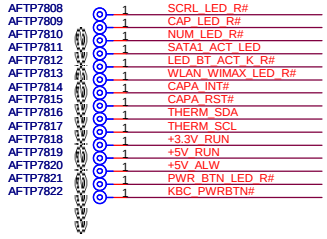
Finger Printer Connector



LED&Capacity board CONN







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Taipei Hsien 221, Taiwan, R.O.C.

Title: Finger Printer

Size: Custom | Document Number: Vostro Calpella | Rev: SA

Date: Tuesday, September 08, 2009 | Sheet 78 of 90

SSID = Mechanical

BOSS:

WLAN

BOSS2
STF256R89H178-GP
34.4B417.001

Thermal

BOSS3
STF237R117H83-1-GP
34.4CK01.001

2009/07/30
Change connector

For CPU HOLE:

H13 Do Not Stuff
H14 Do Not Stuff
H15 Do Not Stuff

Do Not Stuff Do Not Stuff Do Not Stuff

H16 Do Not Stuff

Do Not Stuff

HOLE:

H1 Do Not Stuff
H2 Do Not Stuff
H3 Do Not Stuff

Do Not Stuff Do Not Stuff Do Not Stuff

H4 Do Not Stuff

Do Not Stuff

H5 Do Not Stuff
H6 Do Not Stuff

Do Not Stuff Do Not Stuff

H8 Do Not Stuff

Do Not Stuff

H10 Do Not Stuff
H11 Do Not Stuff
H12 Do Not Stuff

Do Not Stuff Do Not Stuff Do Not Stuff

EMI Request

+PWR_SRC
EC7901 SCD1U25V2ZY-1GP

+1.8V_RUN
EC7902 SCD1U25V2ZY-1GP

+3.3V_RUN
EC7903 SCD1U25V2ZY-1GP

+1.05V_PCH
EC7904 SCD1U25V2ZY-1GP

+3.3V_RUN_GPU
EC7905 SCD1U25V2ZY-1GP
EC7906 SCD1U25V2ZY-1GP
EC7907 SCD1U25V2ZY-1GP
EC7908 SCD1U25V2ZY-1GP

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Title: Miscellaneous Components

Size: Custom | Document Number: Vostro Calpella | Rev: SA

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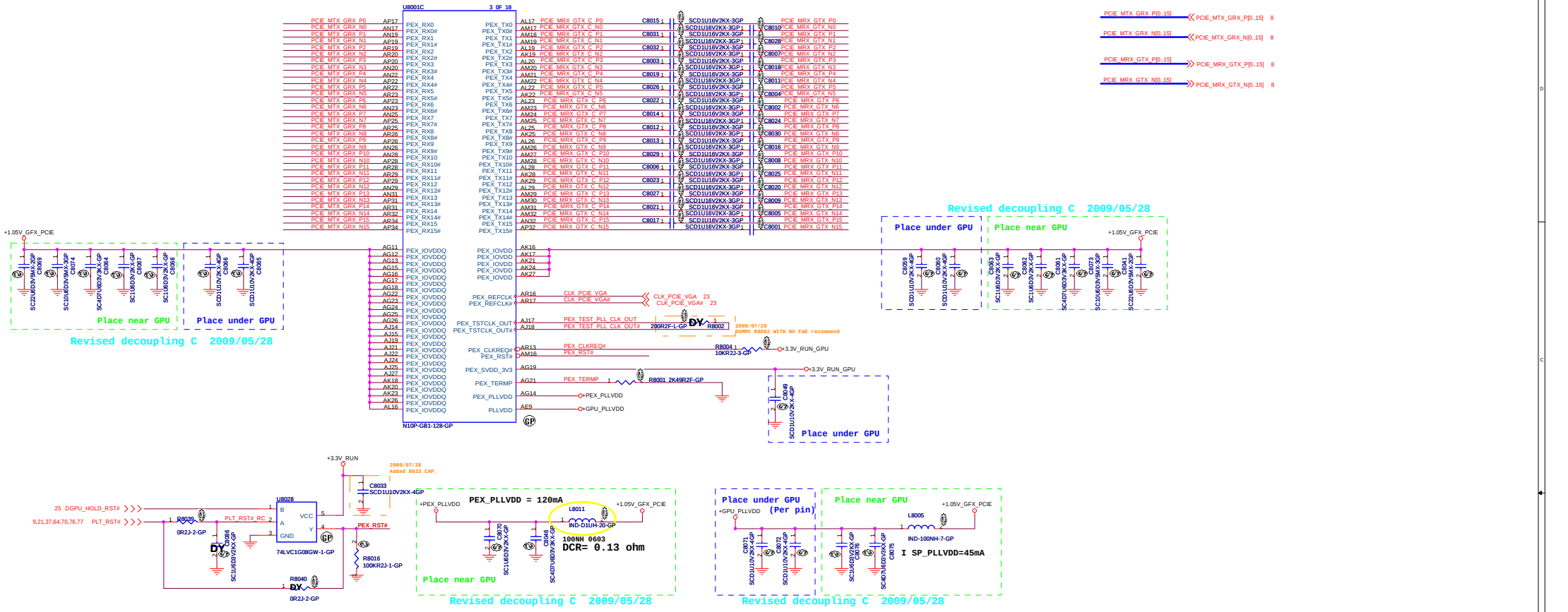
SSID = VIDEO



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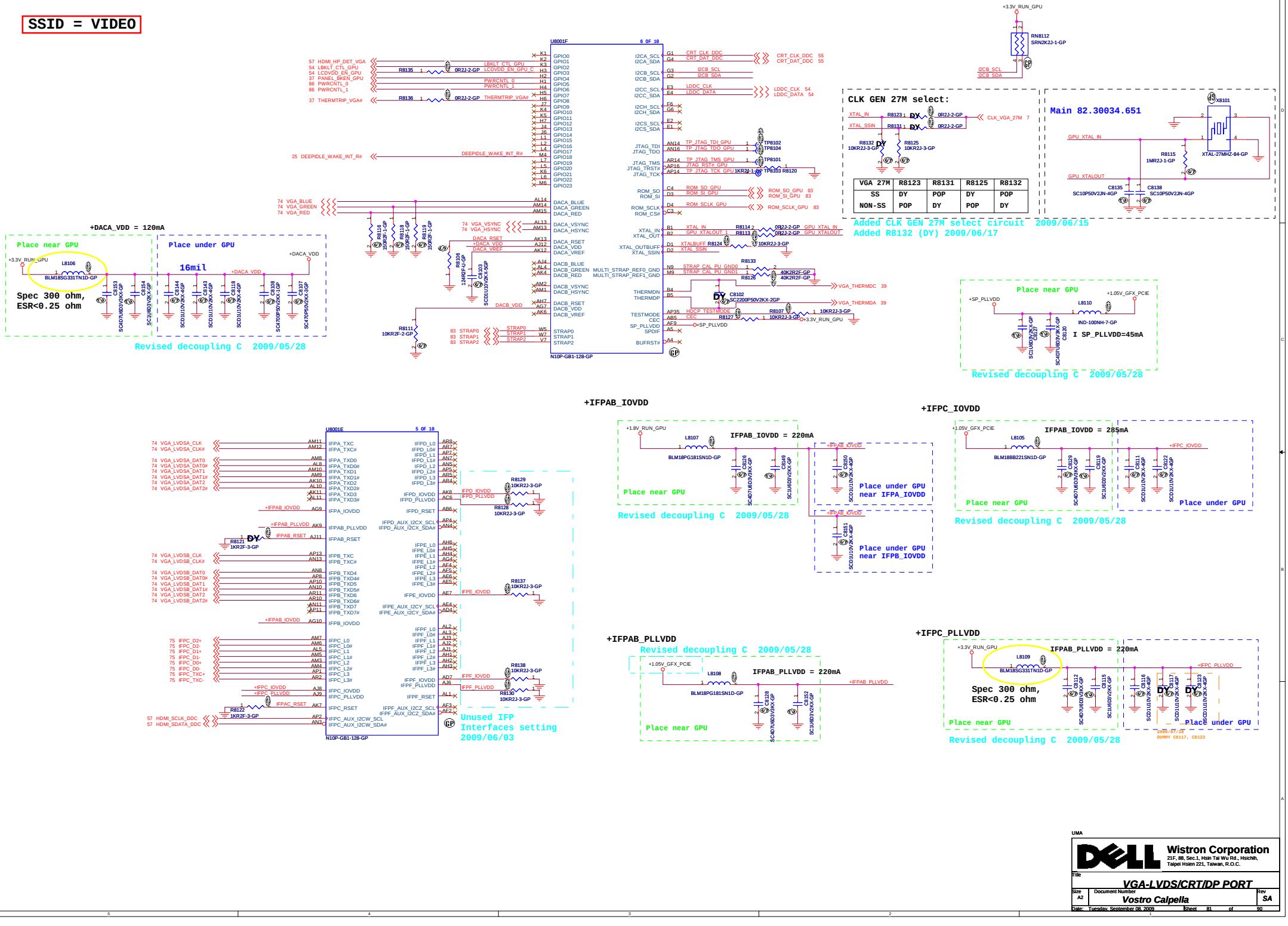
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA-PCIE/LVDS(1/4)

Size	Document Number	Rev
A2	Vostro Calpella	SA

Date: Tuesday, September 08, 2009 Sheet 80 of 90

SSID = VIDEO



UMA

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Title: VGA-LVDS/CRT/DP PORT

Size	Document Number	Rev
A2	Vostro Calpella	SA

Date: Tuesday, September 08, 2009 Sheet 81 of 90

SSID = VIDEO

+VCC_GFX_CORE = 31.66A

Place under GPU

Place near GPU

Revised decoupling C 2009/05/28

Layout notice:
VDD_SENSE need check layout SPEC.

2009/08/05
Added +VCC_GFX_CORE and +1.5V_RUN_GPU power decoupling capacitors.

FBVDD/Q = 2.24A

Place under GPU

Place near GPU

Revised decoupling C 2009/05/28

Do Not Stuff

2009/07/28
Added 8246 CAP.

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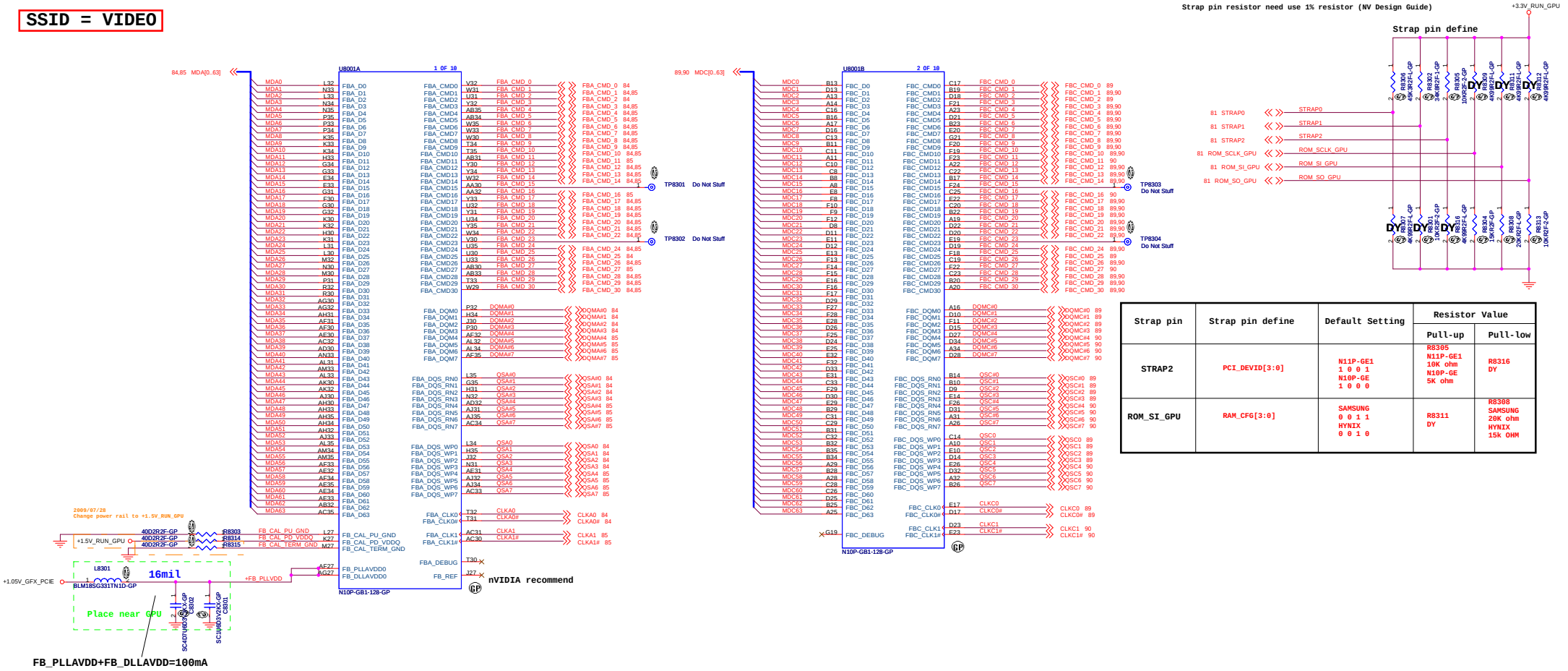
Title: VGA-POWER/GND(3/4)

Size: A2 | Document Number: Vostro Calpella | Rev: SA

Date: Tuesday, September 08, 2009 | Sheet 82 of 90

SSID = VIDEO



Strap pin	Strap pin define	Default Setting	Resistor Value	
			Pull-up	Pull-low
STRAP2	PCI_DEVID[3:0]	N11P-GE1 1 0 0 1 N10P-GE 1 0 0 0	R8305 N11P-GE1 10K ohm N10P-GE 5K ohm	R8316 DY
ROM_SI_GPU	RAM_CFG[3:0]	SAMSUNG 0 0 1 1 HYNIX 0 0 1 0	R8311 DY	R8308 SAMSUNG 20K ohm HYNIX 15K OHM

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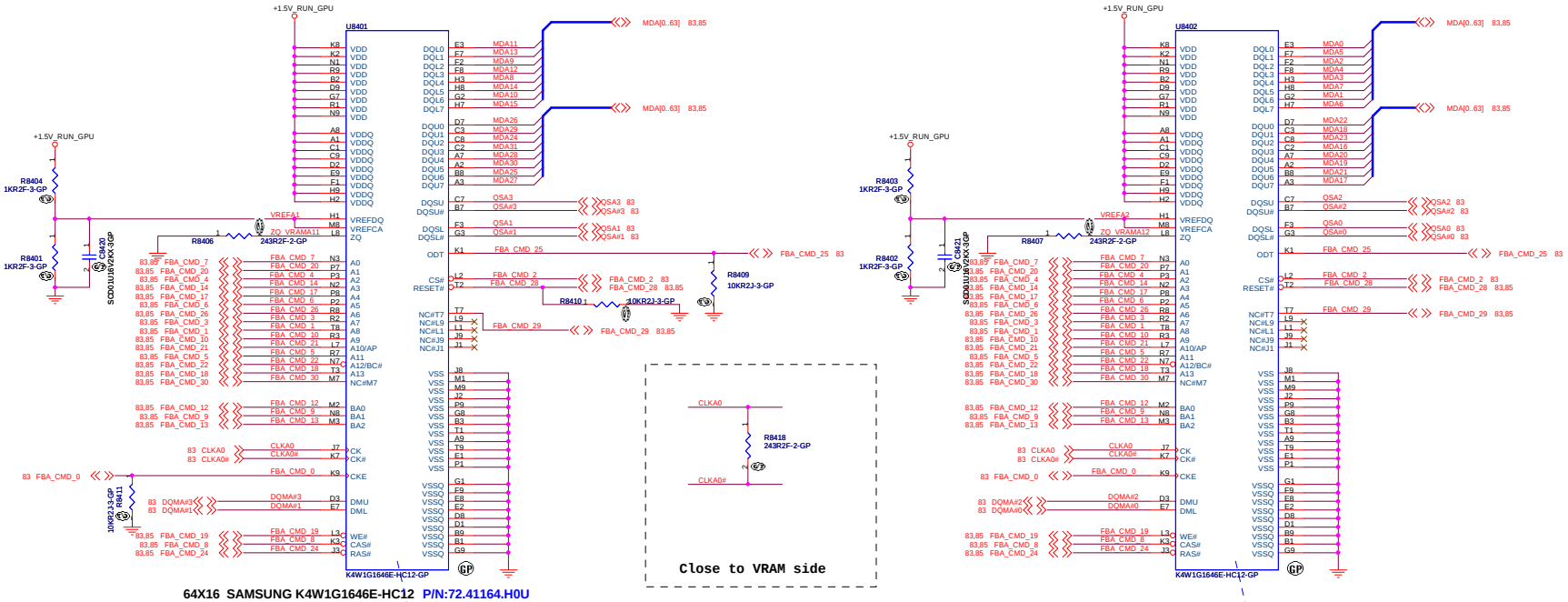
Title: VGA-MEMORY(5/5)

Size	Document Number	Rev
A2	Vostro Calpella	SA

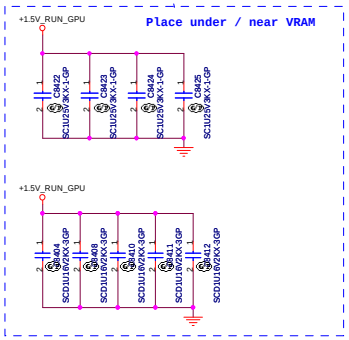
Date: Tuesday, September 08, 2009 Sheet 83 of 90

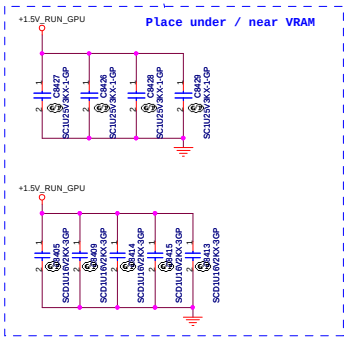
SSID = VIDEO



64X16 SAMSUNG K4W1G1646E-HC12 P/N:72.41164.H0U

64X16 HYNIX H5TQ1G63BFR-12C P/N:72.51G63.C0U





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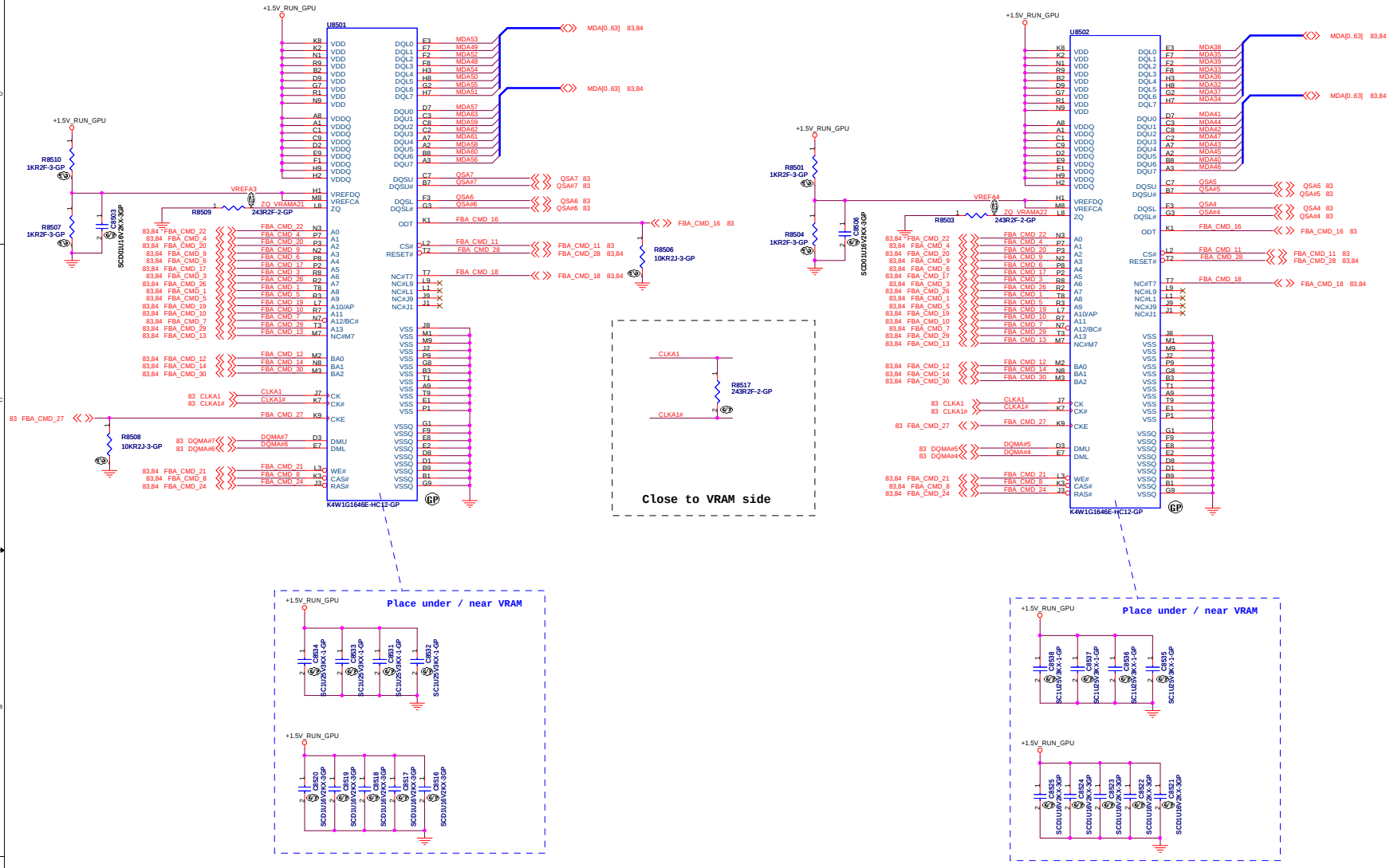
Title: VRAM(1/2)

Size	Document Number	Rev
A2	Vostro Calpella	SA

Date: Tuesday, September 08, 2009 Sheet 84 of 90

SSID = VIDEO



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Title: **VRAM**

Size	Document Number	Rev
A2	*Vostro Calpella*	SA

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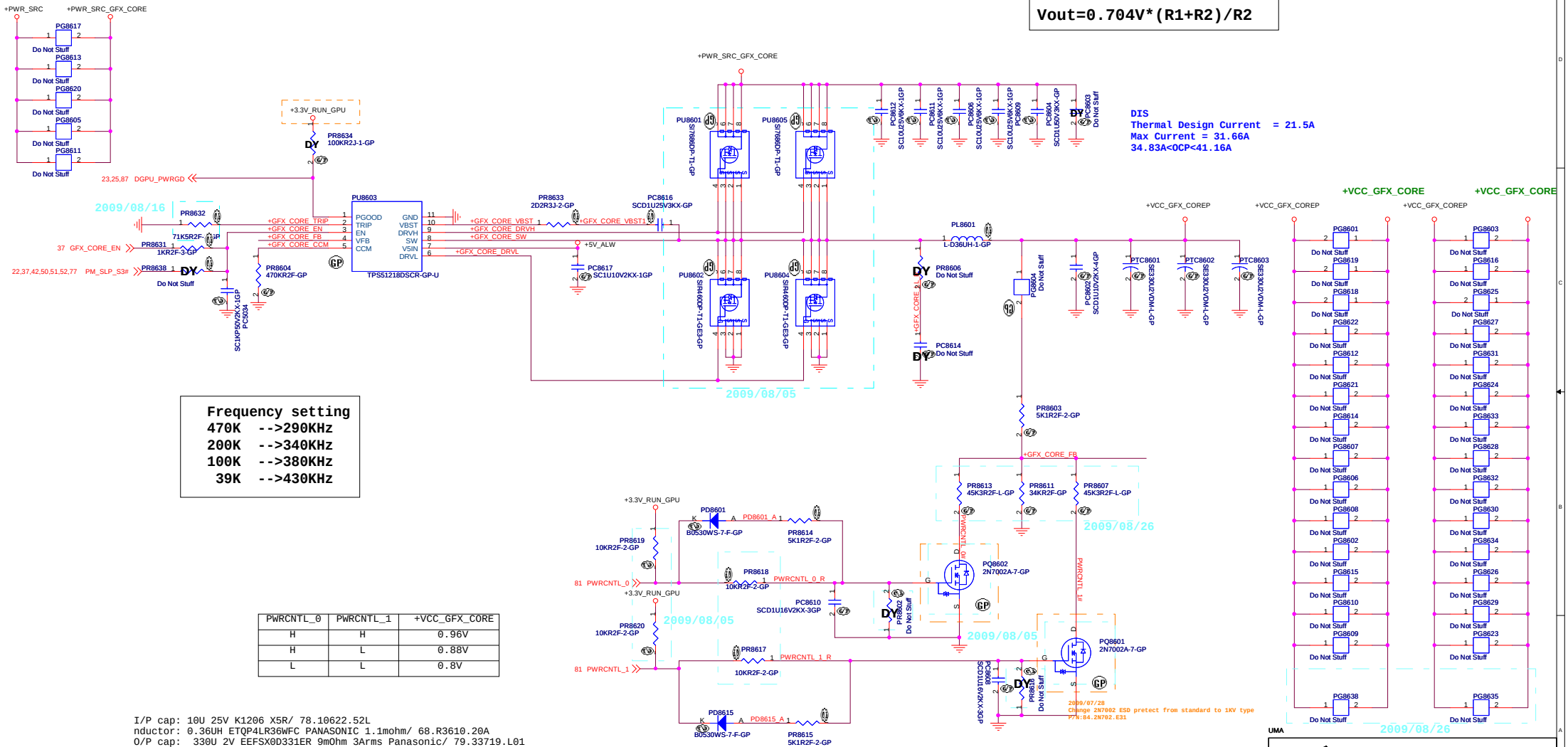
SSID = PWR.Plane.Regulator_GFX

Vout=0.704V*(R1+R2)/R2



PWRCNTL_0	PWRCNTL_1	+VCC_GFX_CORE
H	H	0.96V
H	L	0.88V
L	L	0.8V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
nductor: 0.36UH ETQP4LR36WFC PANASONIC 1.1mohm/ 68.R3610.20A
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3Arms Panasonic/ 79.33719.L01
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037
Switching freq-->350KHz

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Title: TPS51218 +VCC_GFX_CORE

Size: Custom | Document Number: DW Calpella (Discrete) | Rev: X00

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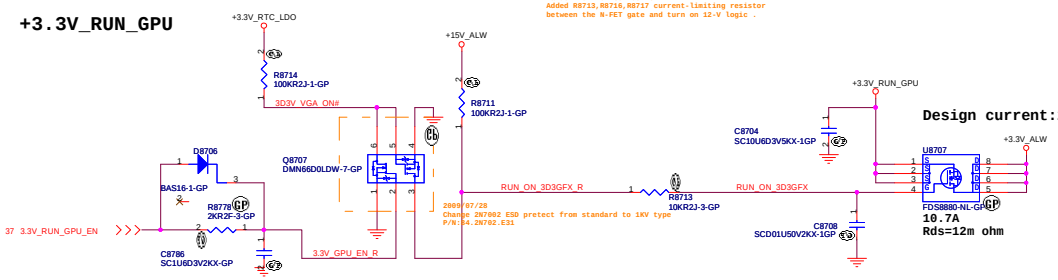
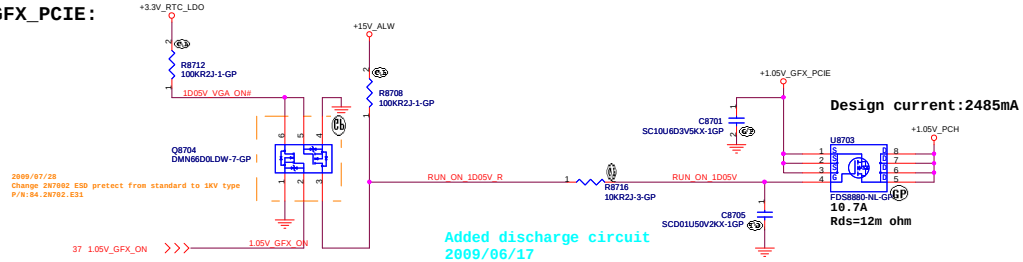
+3.3V_RUN_GPU

2009/08/10
Changed R8708,R8710,R8711 current-limiting resistor value from 10k to 100k ohm.
Added R8713,R8716,R8717 current-limiting resistor between the N-FET gate and turn on 12-V logic .



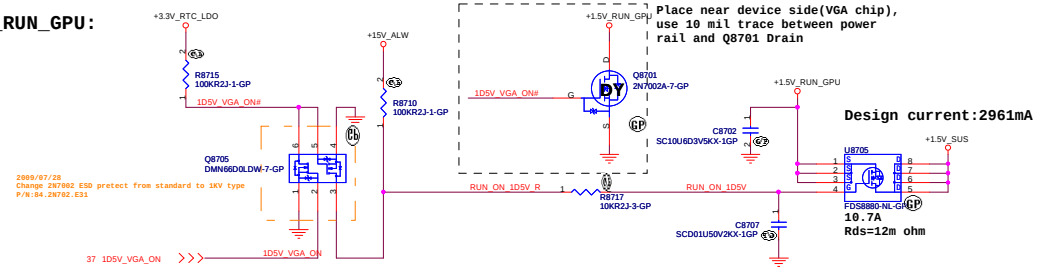
Added +1.05V_GFX_PCIE, +1.5V_RUN_GPU power switch 2009/05/25

+1.05V_GFX_PCIE:



Added discharge circuit
2009/06/17

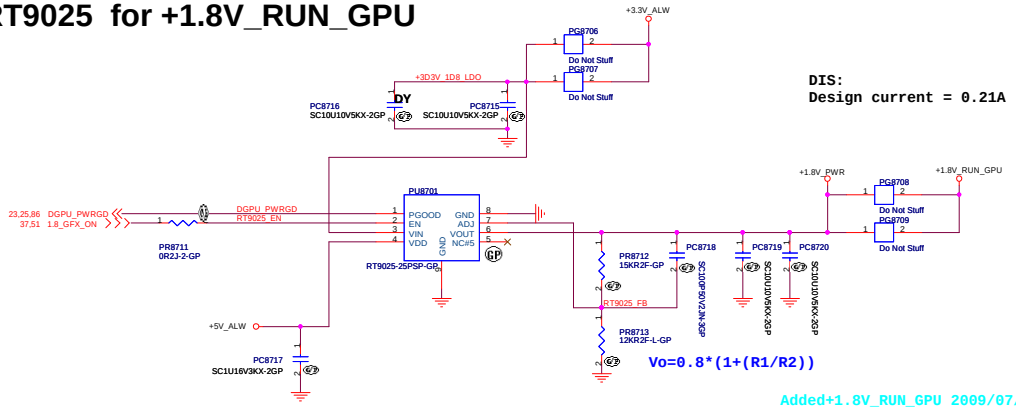
+1.5V_RUN_GPU:



Place near device side(VGA chip), use 10 mil trace between power rail and Q8701 Drain

+1.8V_RUN_GPU

RT9025 for +1.8V_RUN_GPU



DIS:
Design current = 0.21A

Added+1.8V_RUN_GPU 2009/07/17

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Title: LDO 1.8V

Size	Document Number	Rev
Custom	Vostro Calpella	SA

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Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
1	12	2009/07/13		DW70 need support Clarksfield(Qual core)	Add VTT_SELECT pin to control VTT_CORE voltage level	SA
2	21	2009/07/13			Add USB port for right side board	SA
3	23	2009/07/13			Follow 15 inch PCI-E port	SA
4	65	2009/07/13			Add SIM card schematic	SA
5	76	2009/07/13			Add LAN board connector schematic	SA
6	77	2009/07/13			Change IO board connector and add Audio board connector	SA
7	78	2009/07/13			Add Finger Printer Connector schematic	SA
8	30,60	2009/07/14			Remove AUDIO Schematic and speaker connector	SA
9	35	2009/07/14			Remove LAN Schematic	SA
10	54	2009/07/14			LCD_BRIGHTNESS follow 15 inch schematic	SA

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Title: *Change List(1/3)*

Size: A3 | Document Number: *Vostro Calpella* | Rev: *SA*

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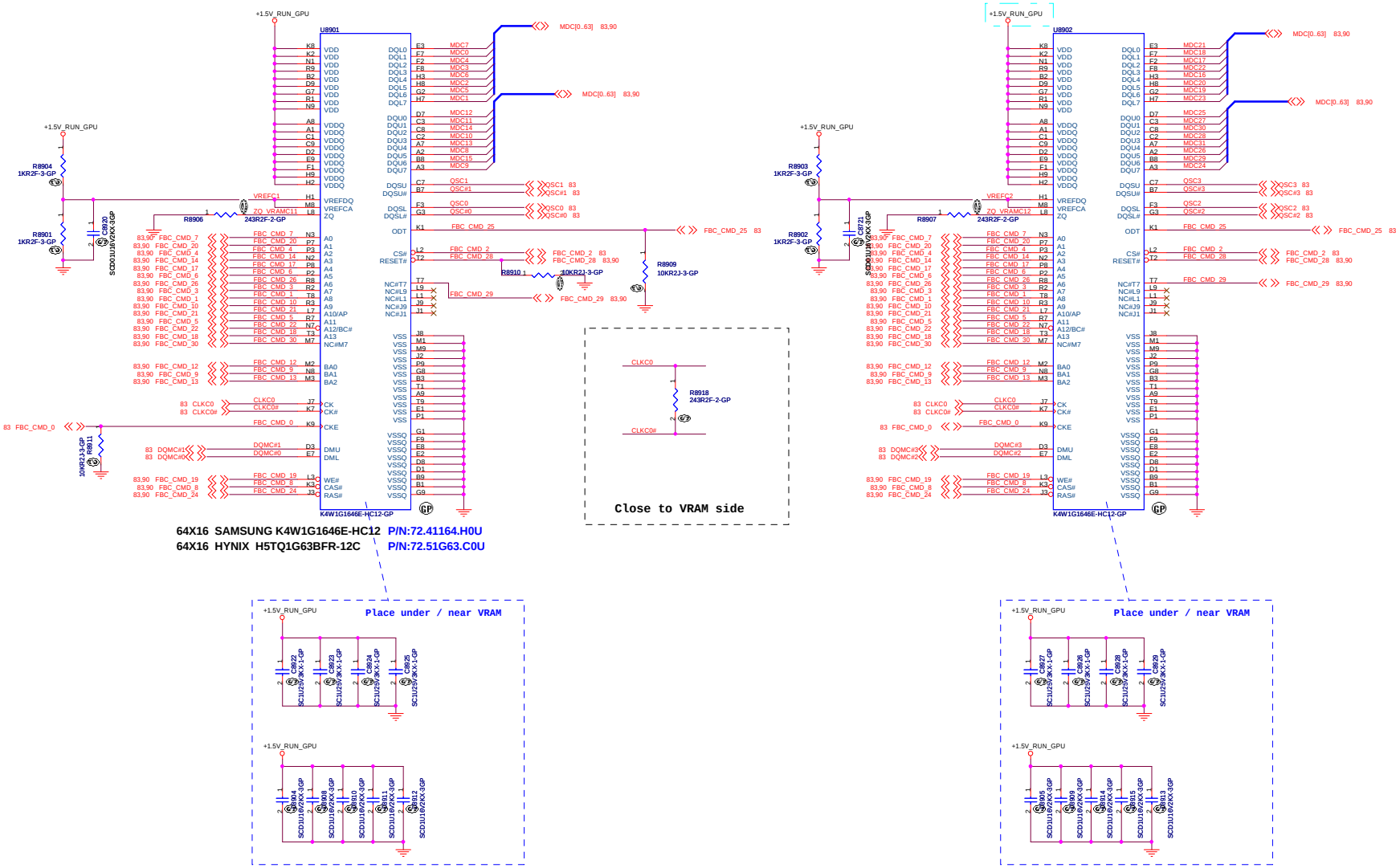
SSID = VIDEO



64X16 SAMSUNG K4W1G1646E-HC12 P/N:72.41164.H0U

64X16 HYNIX H5TQ1G63BFR-12C P/N:72.51G63.C0U

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Title: VRAM(1/2)

Size: A2 | Document Number: Vostro Calpella | Rev: SA

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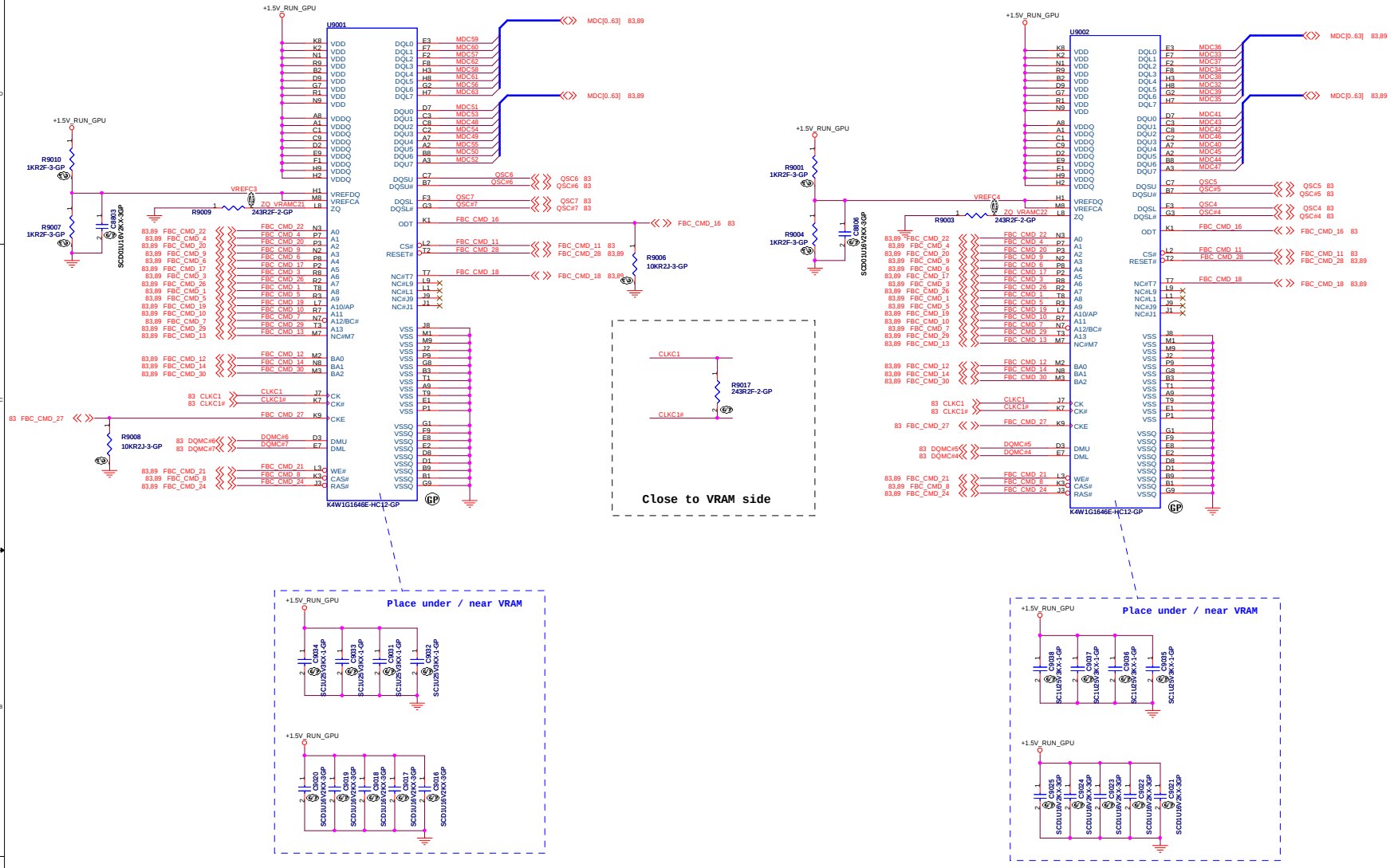
SSID = VIDEO



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Title			
VRAM			
Size: A2	Document Number: Vostro Calpella		Rev: SA
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