

Model Name : *Diaz Discrete*
Project Code : *91.4AR01.001*
Revision : *08218-1*


Diaz Discrete VGA ATI M82-S Schematics Document

uFCPGA Mobile Merom
Intel Crestline-PM + ICH8M

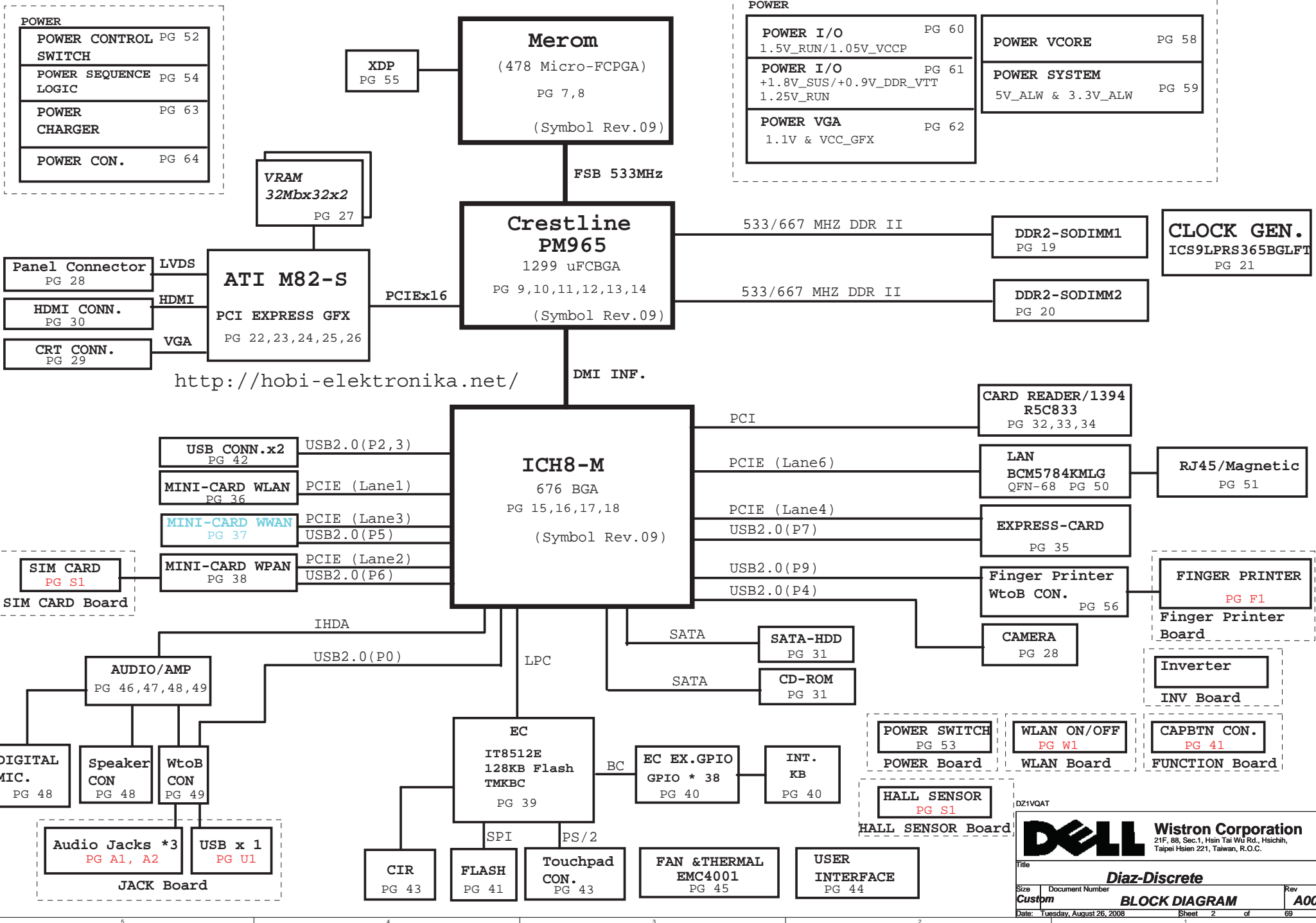
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REV : A00

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Diaz Block Diagram of Intel PM



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Pg#	Description	DNI LIST
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Footprint Definition	
Resistor	Footprint is 0402 if there is no description
Capacitor	Footprint is 0402 if there is no description
Ferrite Bead	Footprint is 0603 if there is no description

Layout Note

For all of ESD diode, they should be placed as close as possible to connectors and the signals from connectors should be routed to ESD diodes first. There is no branch or via before diodes

PCI TABLE			
PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
R5C833	PCI_AD17	PCI_REQ1# PCI_GNT1#	PCI_PIRQC# PCI_PIRQD#

PCI Express TABLE	
Lane 1	<input type="radio"/> WLAN / Mini Card
Lane 2	<input type="radio"/> WPAN / Mini Card
Lane 3	<input type="radio"/> WWAN / Mini Card
Lane 4	<input type="radio"/> ExpressCard
Lane 5	
Lane 6	<input type="radio"/> LAN BCM5784KMLG

USB TABLE	
ICH8-0 (EHCI#1)	User1 (Single port , in USB BD)
ICH8-1 (EHCI#1)	<input type="radio"/>
ICH8-2 (EHCI#1)	<input type="radio"/> User2 (Dual port-bottom , in I/O BD)
ICH8-3 (EHCI#1)	<input type="radio"/> User3 (Dual port-top , in I/O BD)
ICH8-4 (EHCI#1)	Camera
ICH8-5 (EHCI#1)	<input type="radio"/> WWAN / Mini Card
ICH8-6 (EHCI#2)	<input type="radio"/> WPAN / Mini Card
ICH8-7 (EHCI#2)	<input type="radio"/> ExpressCard
ICH8-8 (EHCI#2)	
ICH8-9 (EHCI#2)	<input type="radio"/> Finger Printer

Note : No USB for WLAN

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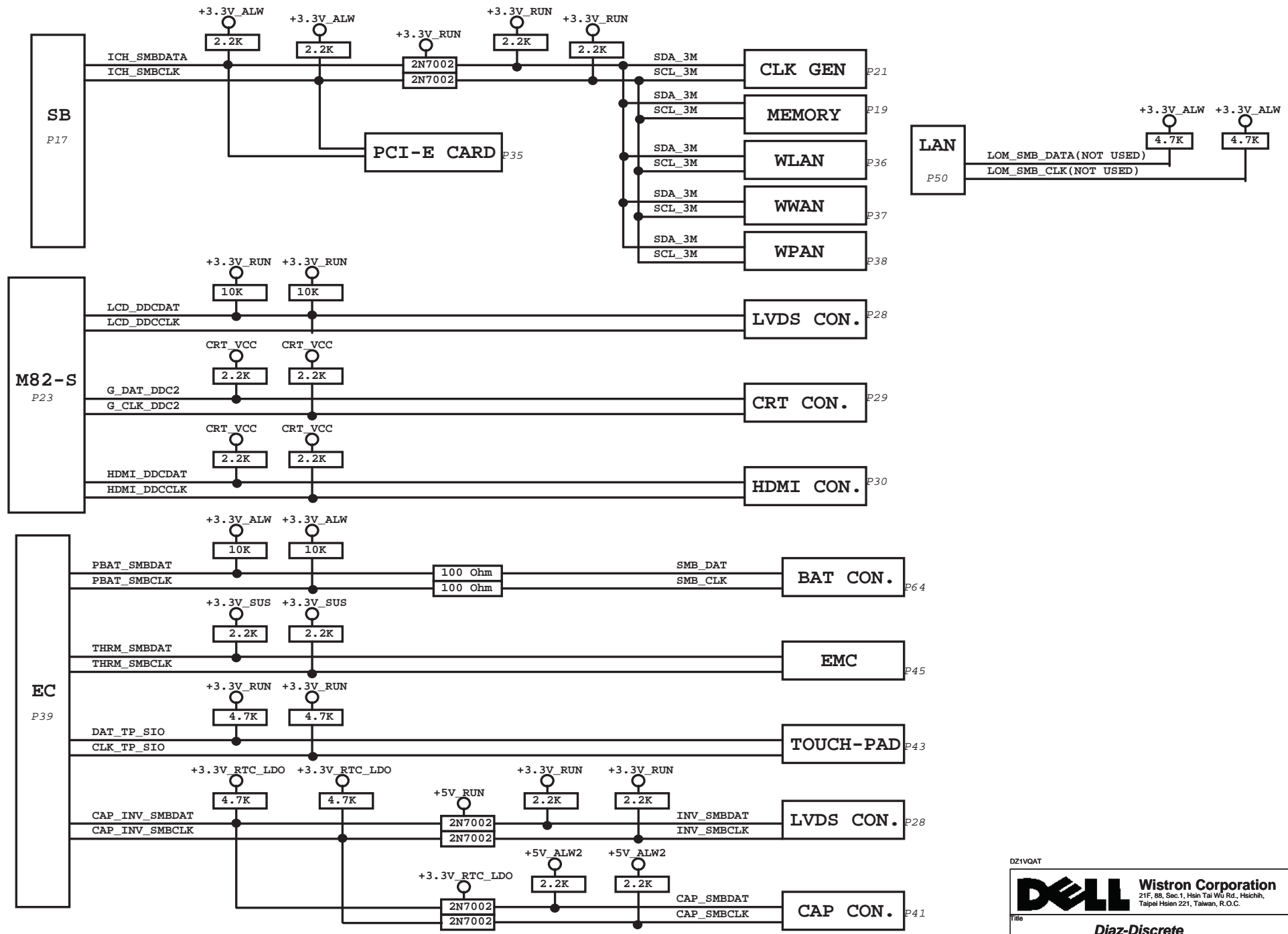
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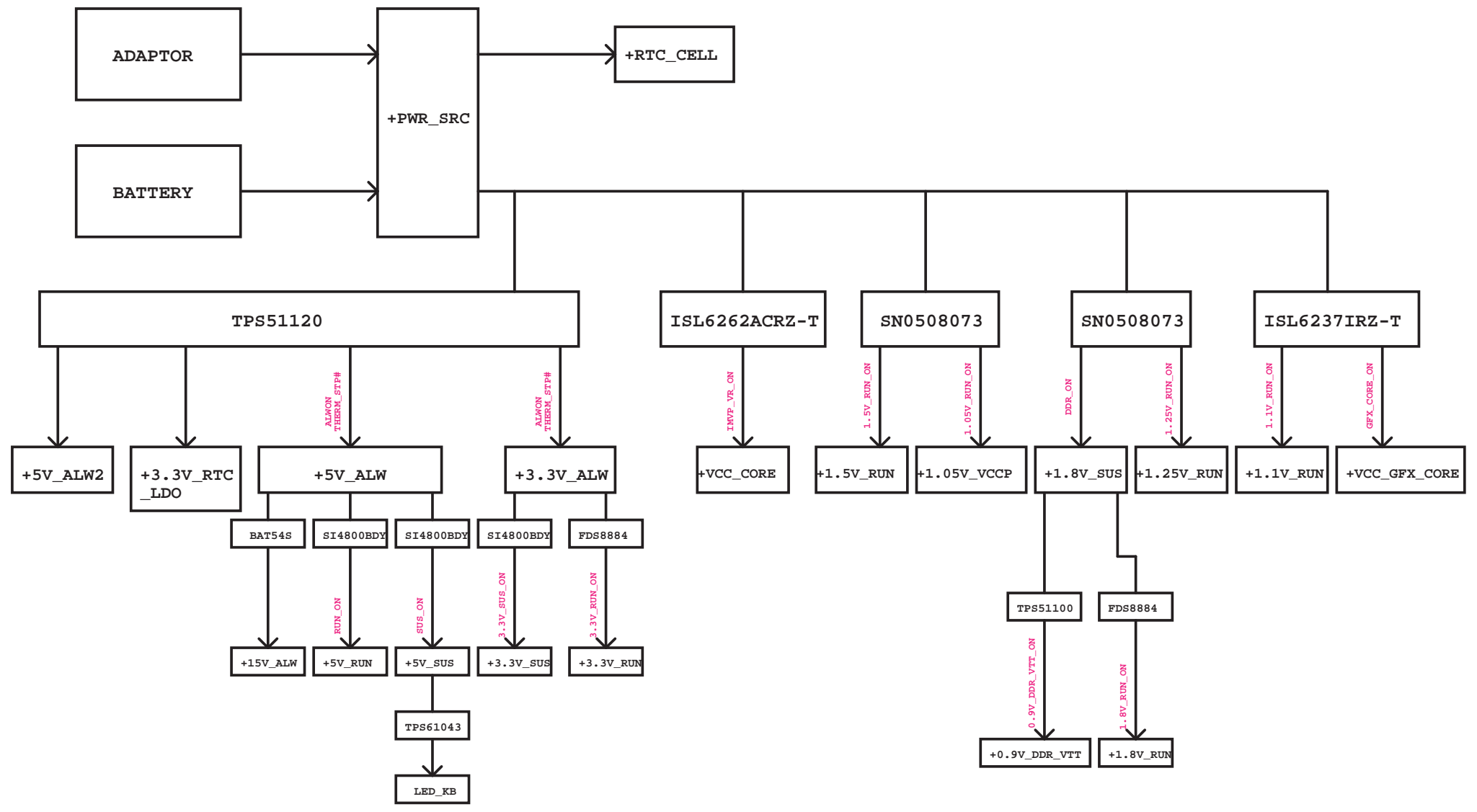
Bus Connection

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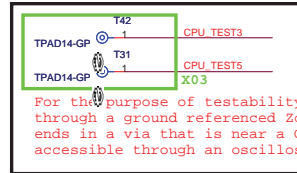
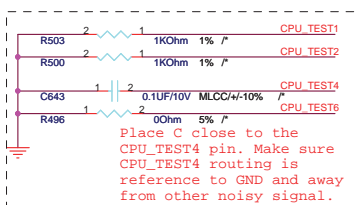
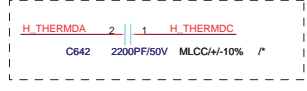
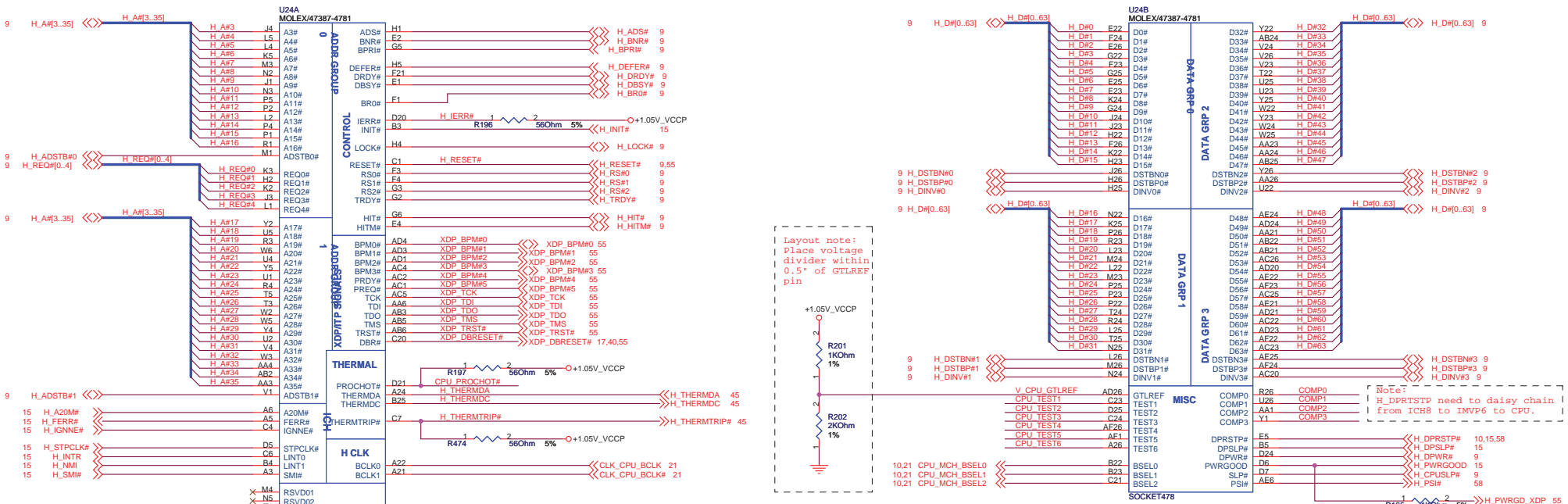




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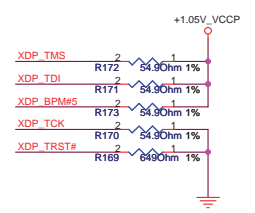
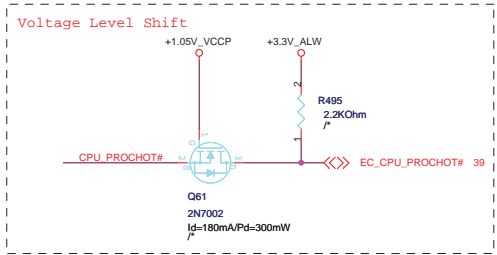
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Title			Rev
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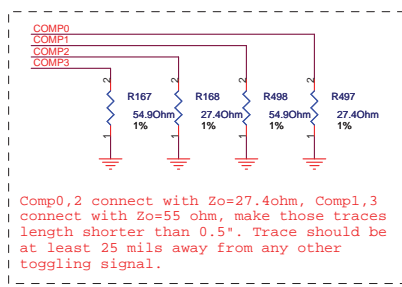


For the purpose of testability, route these signals through a ground referenced Zo=55 ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

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FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0



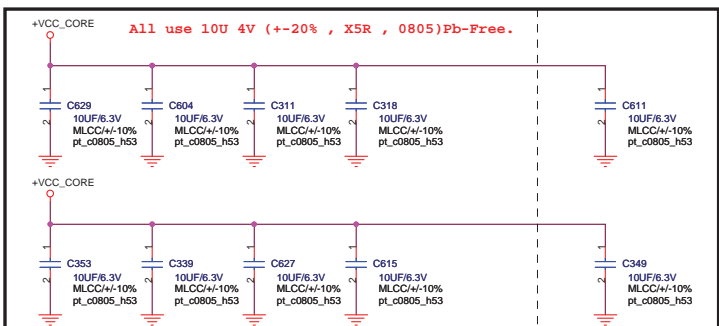
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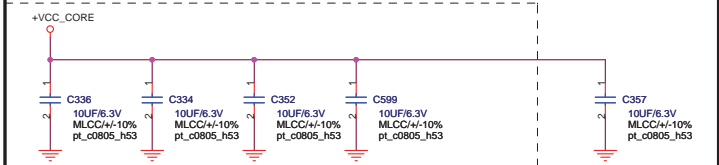
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Size: Document Number: **Custpm MEROM CPU (1)** Rev: **A00**

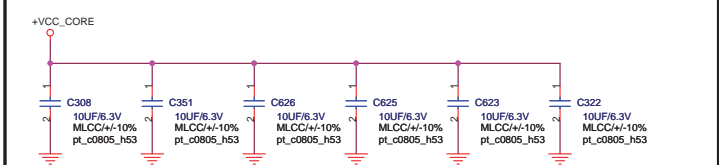
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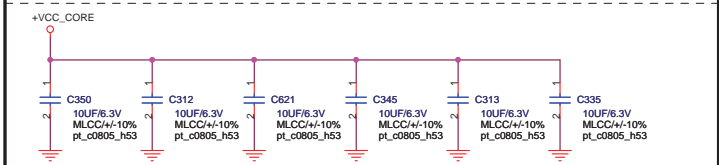
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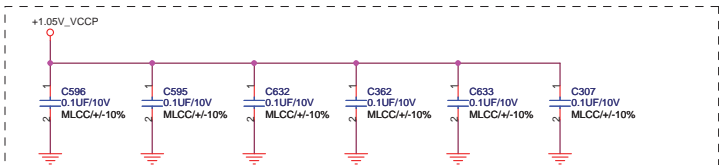
8 inside cavity, south side, secondary layer.



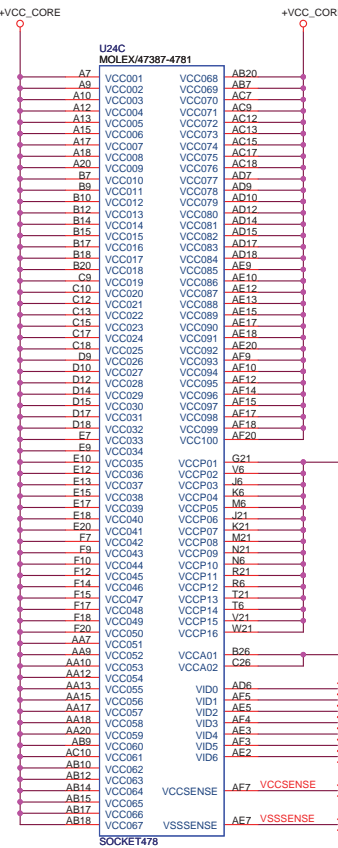
6 inside cavity, north side, primary layer.



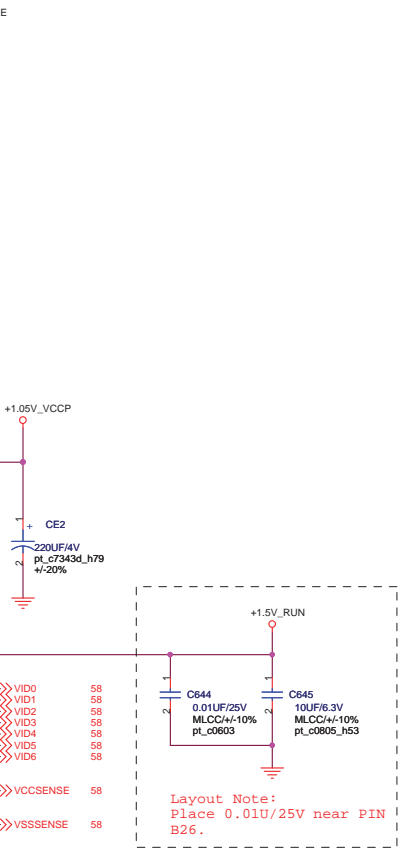
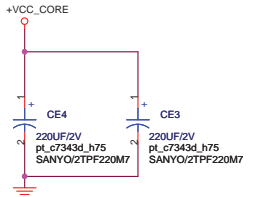
6 inside cavity, south side, primary layer.



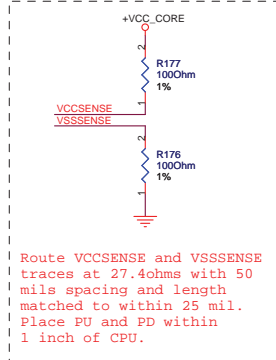
Layout out:
Place these inside socket cavity on North side secondary.



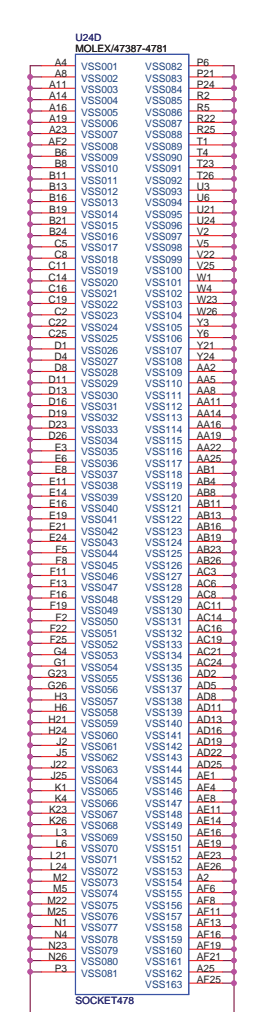
100U/25V *4 Remove to POWER CIRCUIT .



Layout Note:
Place 0.01u/25V near PIN B26.



Route VCCSENSE and VSSSENSE traces at 27.4ohms with 50 mils spacing and length matched to within 25 mil. Place PU and PD within 1 inch of CPU.



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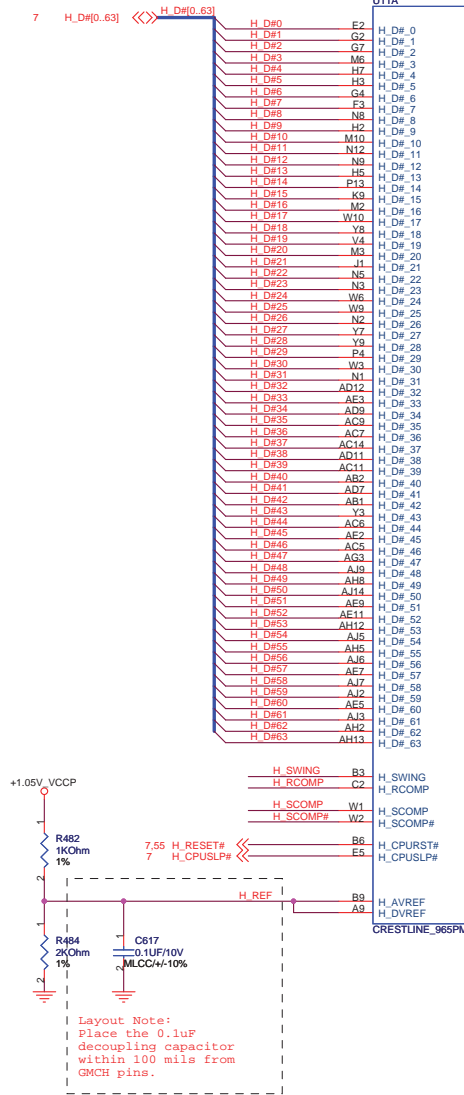
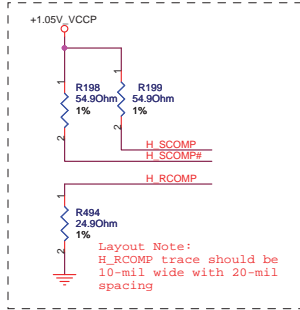
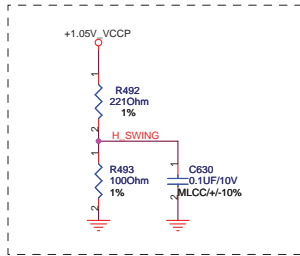
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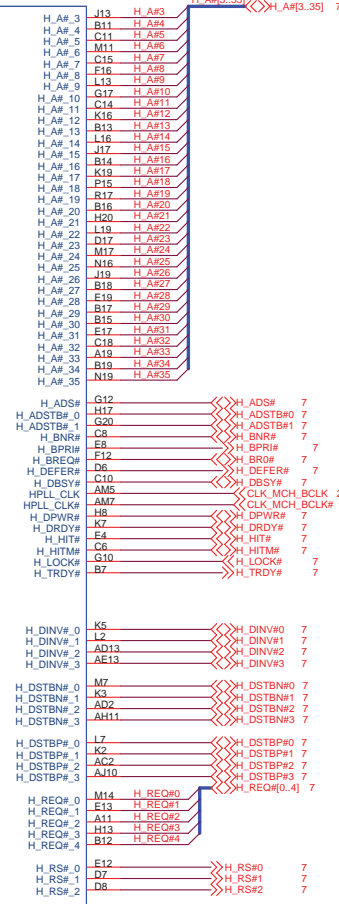
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U11A	Pin	Signal
H_D#0	E2	H_D#_0
H_D#1	G2	H_D#_1
H_D#2	M6	H_D#_2
H_D#3	H7	H_D#_3
H_D#4	H3	H_D#_4
H_D#5	G4	H_D#_5
H_D#6	F3	H_D#_6
H_D#7	N8	H_D#_7
H_D#8	H2	H_D#_8
H_D#9	M10	H_D#_9
H_D#10	N12	H_D#_10
H_D#11	N9	H_D#_11
H_D#12	H5	H_D#_12
H_D#13	P13	H_D#_13
H_D#14	K9	H_D#_14
H_D#15	M2	H_D#_15
H_D#16	W10	H_D#_16
H_D#17	Y8	H_D#_17
H_D#18	V4	H_D#_18
H_D#19	M3	H_D#_19
H_D#20	J1	H_D#_20
H_D#21	N3	H_D#_21
H_D#22	W6	H_D#_22
H_D#23	V9	H_D#_23
H_D#24	N2	H_D#_24
H_D#25	Y7	H_D#_25
H_D#26	Y9	H_D#_26
H_D#27	D4	H_D#_27
H_D#28	W3	H_D#_28
H_D#29	N1	H_D#_29
H_D#30	AD12	H_D#_30
H_D#31	AE3	H_D#_31
H_D#32	AD9	H_D#_32
H_D#33	AC9	H_D#_33
H_D#34	AC7	H_D#_34
H_D#35	AC14	H_D#_35
H_D#36	AD11	H_D#_36
H_D#37	AC11	H_D#_37
H_D#38	AB2	H_D#_38
H_D#39	AD7	H_D#_39
H_D#40	AB1	H_D#_40
H_D#41	Y3	H_D#_41
H_D#42	AC6	H_D#_42
H_D#43	AE2	H_D#_43
H_D#44	AC5	H_D#_44
H_D#45	AG3	H_D#_45
H_D#46	AJ9	H_D#_46
H_D#47	AH8	H_D#_47
H_D#48	AJ4	H_D#_48
H_D#49	AE9	H_D#_49
H_D#50	AH12	H_D#_50
H_D#51	AJ5	H_D#_51
H_D#52	AH5	H_D#_52
H_D#53	AH6	H_D#_53
H_D#54	AH7	H_D#_54
H_D#55	AJ2	H_D#_55
H_D#56	AE5	H_D#_56
H_D#57	AJ3	H_D#_57
H_D#58	AH2	H_D#_58
H_D#59	AH13	H_D#_59

HOST



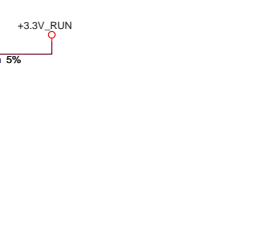
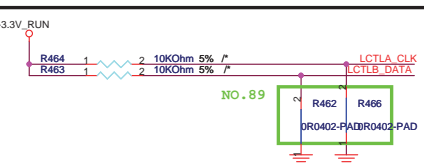
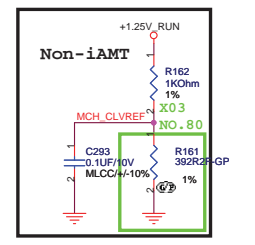
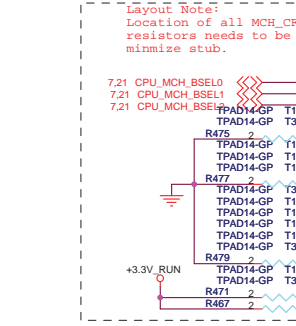
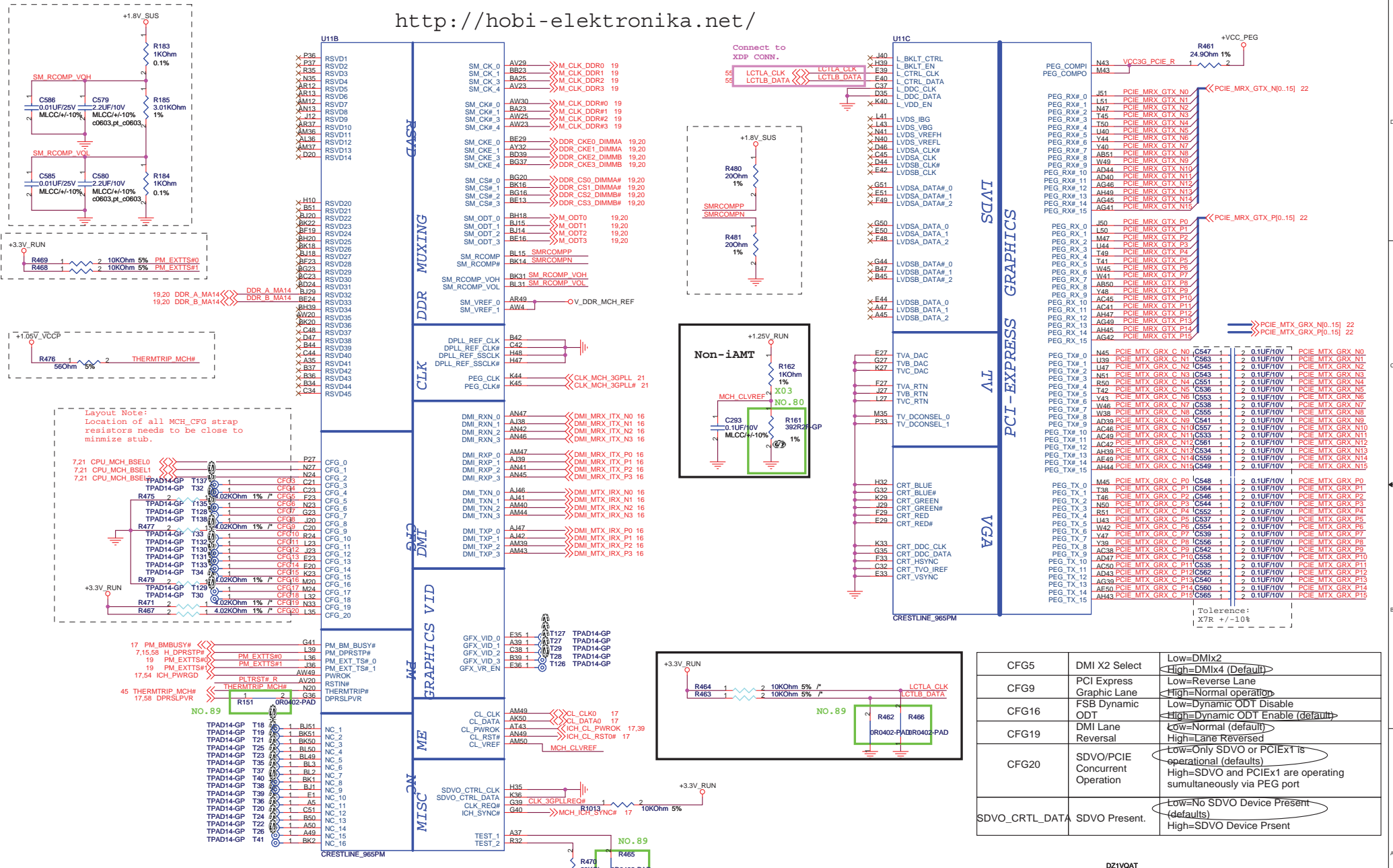
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CFG5	DMI X2 Select	Low=DMix2 High=DMix4 (Default)
CFG9	PCI Express Graphic Lane	Low=Reverse Lane High=Normal operation
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable (default)
CFG19	DMI Lane Reversal	Low=Normal (default) High=Lane Reversed
CFG20	SDVO/PCIe Concurrent Operation	Low=Only SDVO or PCIe1 is operational (defaults) High=SDVO and PCIe1 are operating simultaneously via PEG port
SDVO_CRTL_DATA	SDVO Present.	Low=No SDVO Device Present (defaults) High=SDVO Device Present

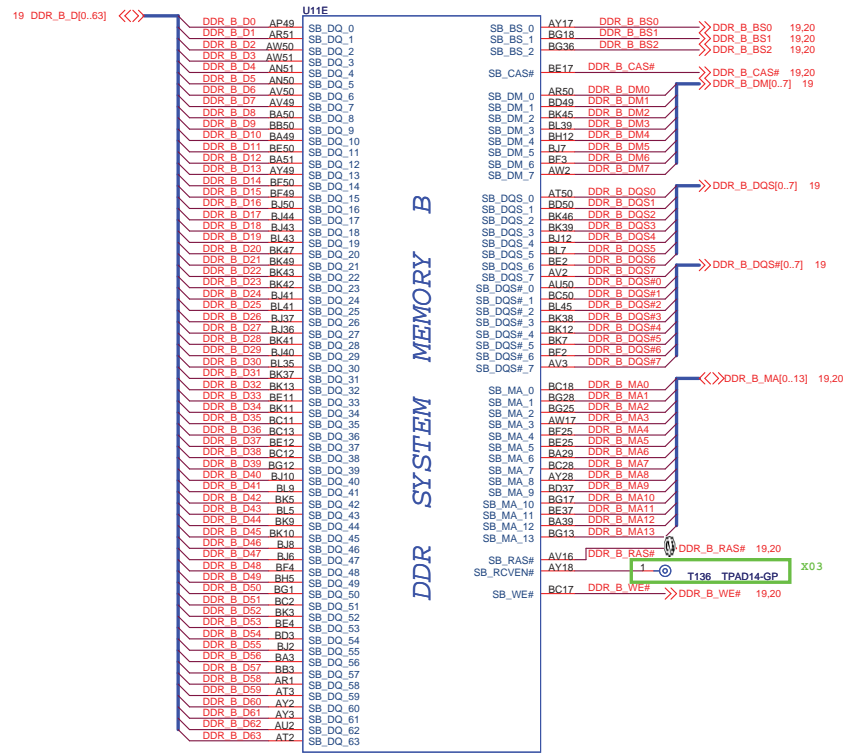
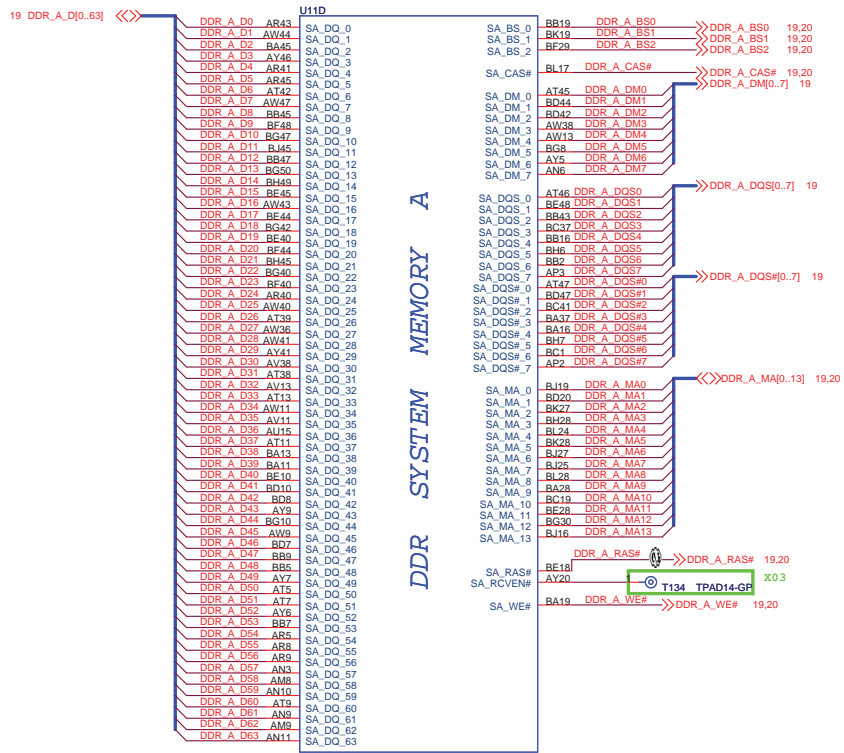
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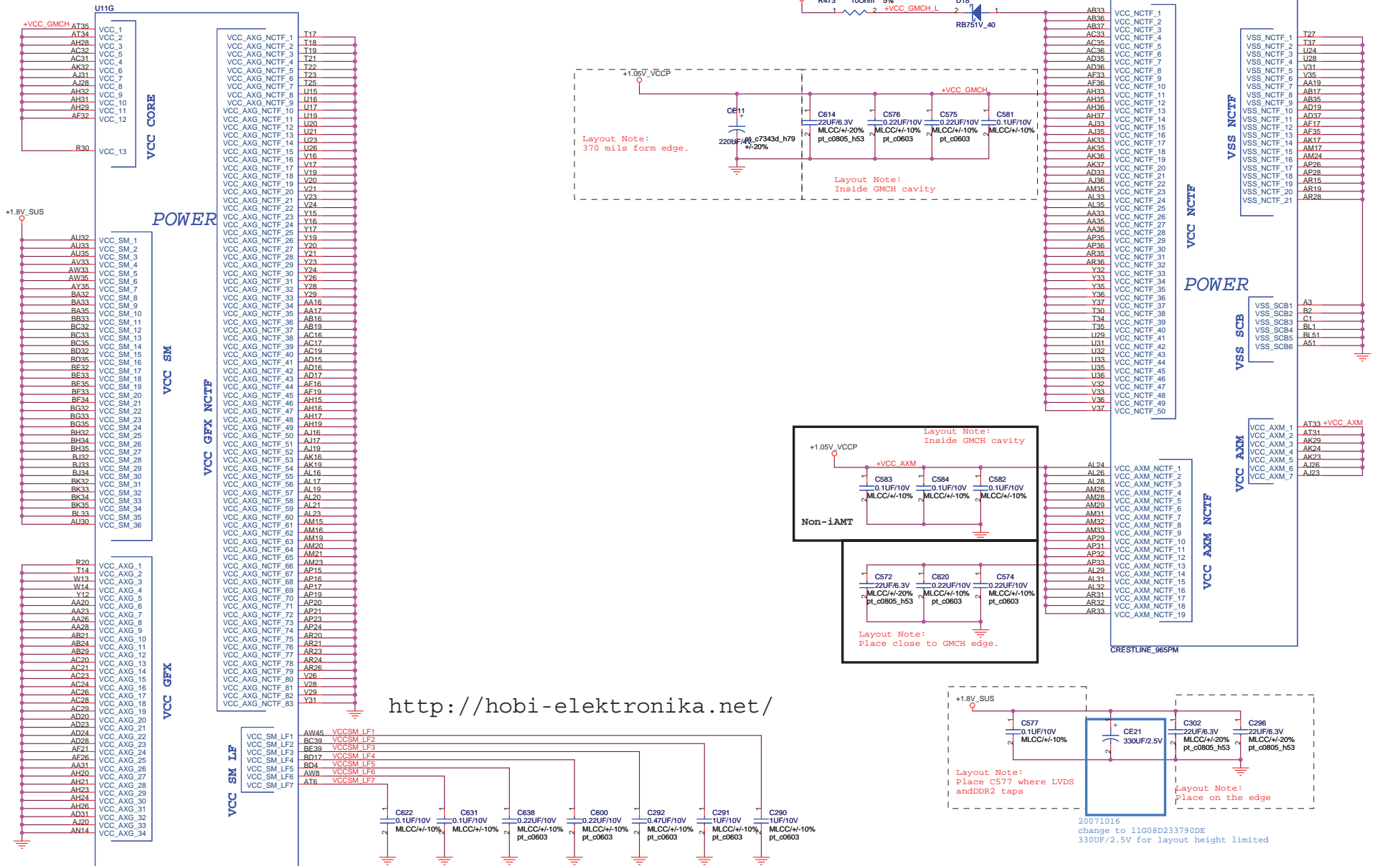
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330UF/2.5V for layout height limited

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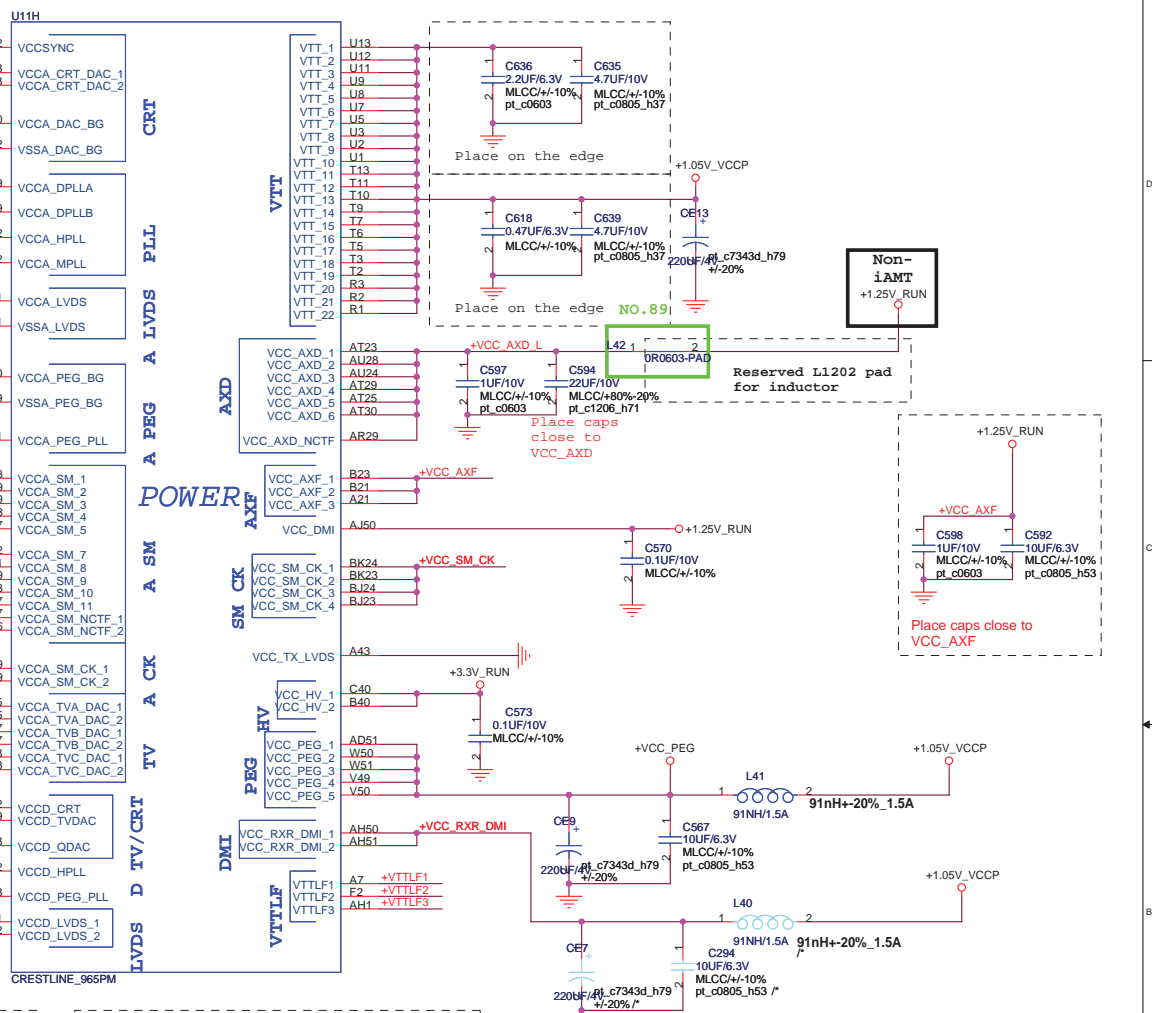
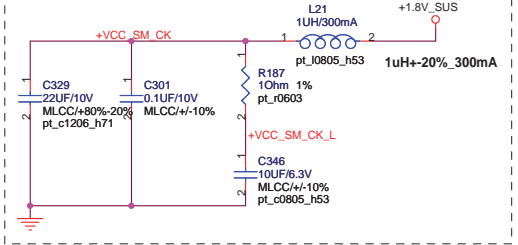
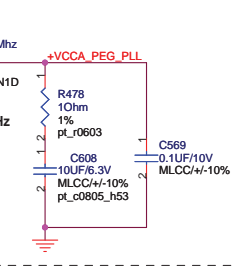
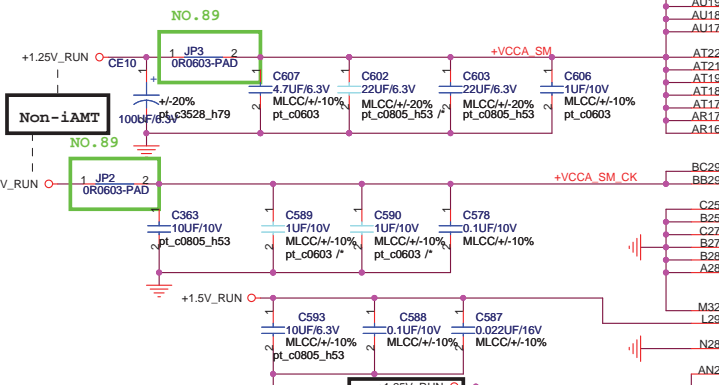
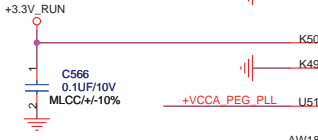
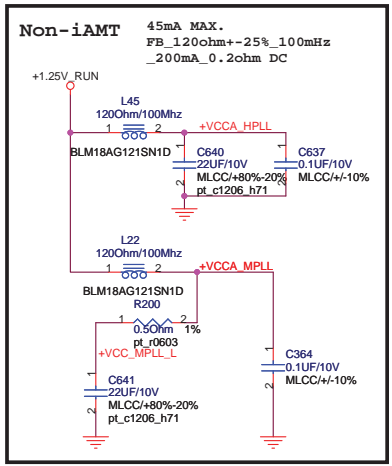


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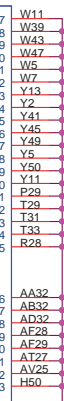
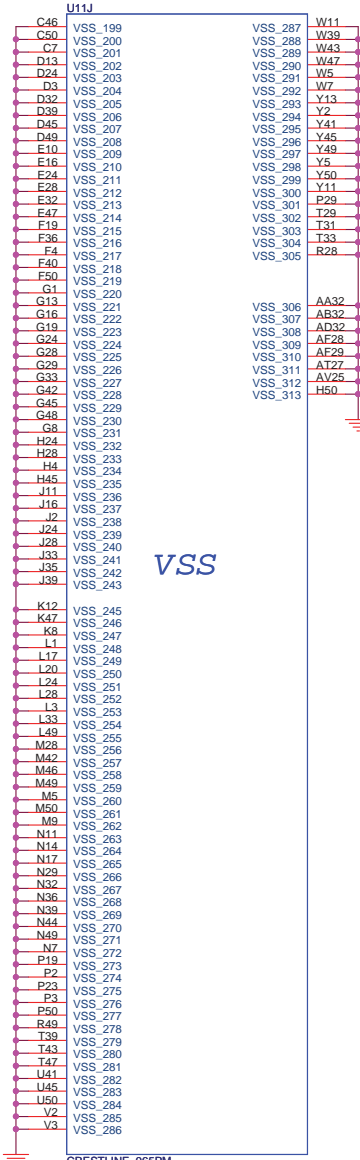
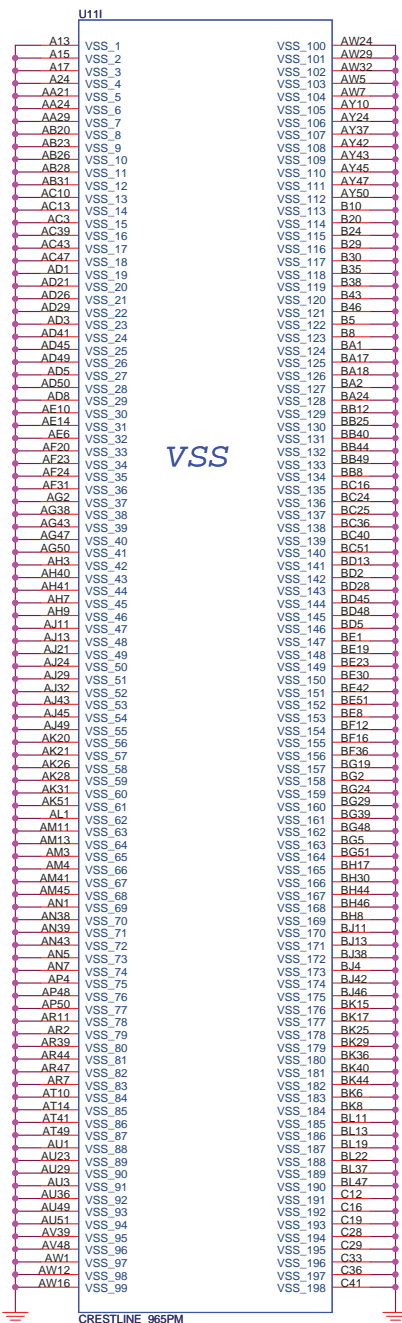
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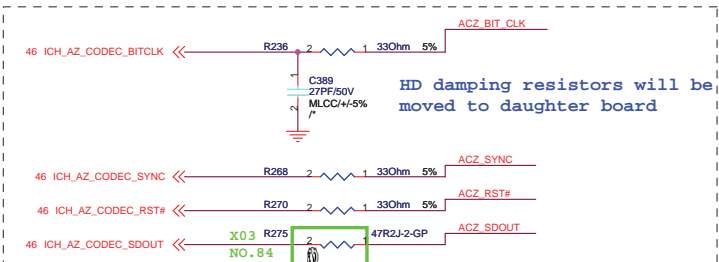
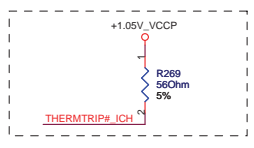
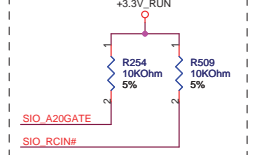
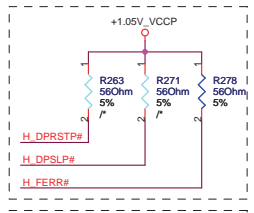
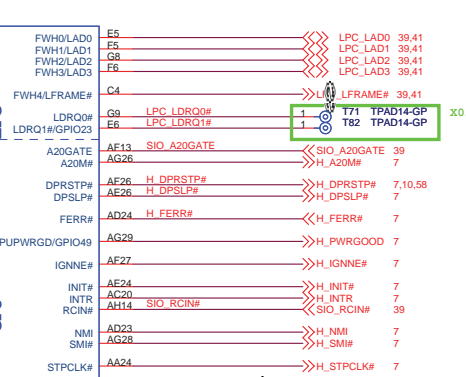
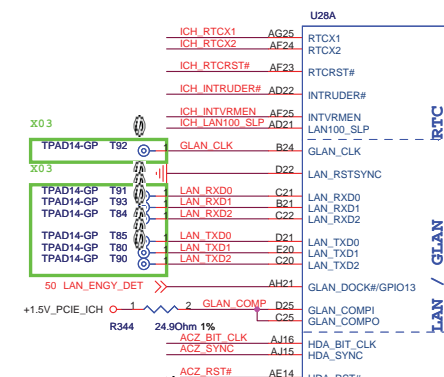
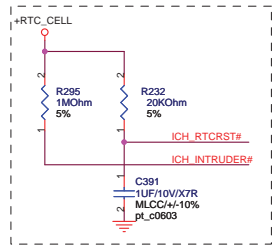
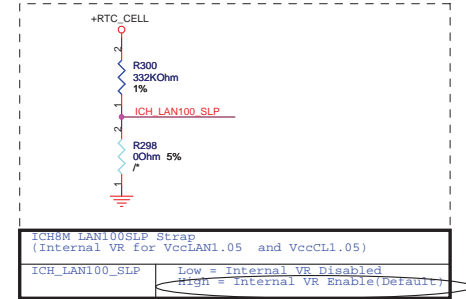
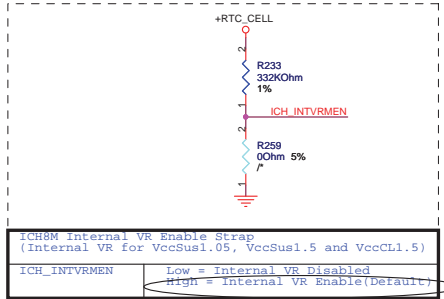
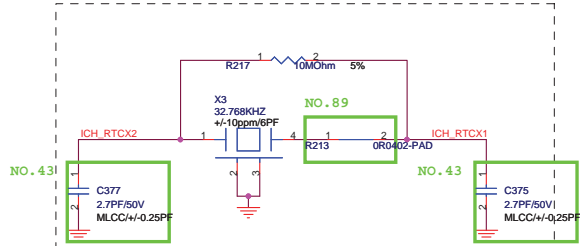
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Title			Rev
Diaz-Discrete			
Size	Document Number	Rev	
A3	Crestline(VSS)	A00	
Date:	Monday, August 25, 2008	Sheet	14 of 69

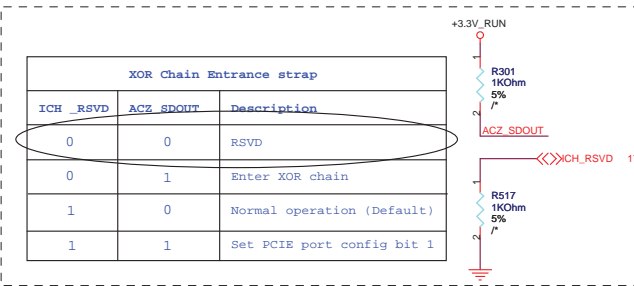


Place all series terms close to ICH8 except for SDIN input lines, which should be close to source. Placement of R235, R264, R265, R265, R258 should equal distance to the T split trace point as R236, R268, R270, R275 respective. Basically, keep the same distance from T for all series termination resistors.

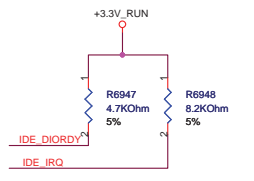
31	SATA_TX0- <<>	C648	MLCC/±10%	2	1	3900PF/50V	SATA_TX0- C
31	SATA_TX0+ <>>	C650	MLCC/±10%	2	1	3900PF/50V	SATA_TX0+ C
31	SATA_TX1- <<>	C764	MLCC/±10%	2	1	3900PF/50V/X7R	SATA_TX1- C
31	SATA_TX1+ <>>	C751	MLCC/±10%	2	1	3900PF/50V/X7R	SATA_TX1+ C

Distance between the ICH-8 M and cap on the "P" signal should be identical distance between the ICH-8 M and cap on the "N" signal for same pair.

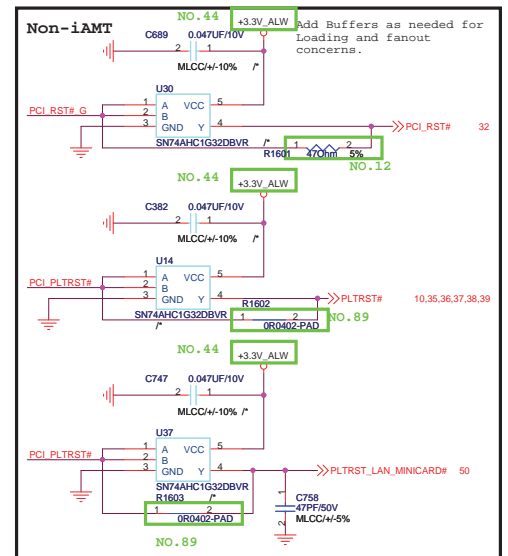
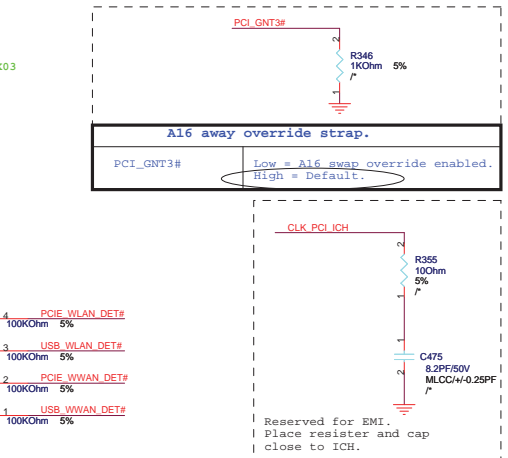
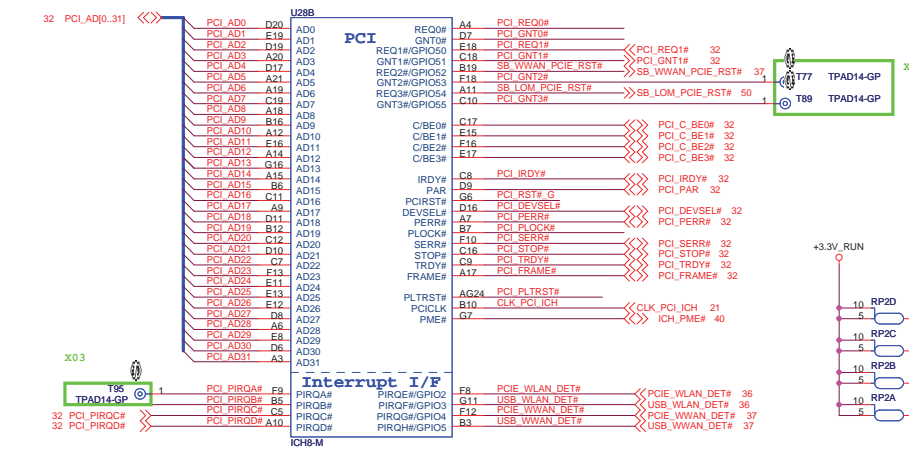
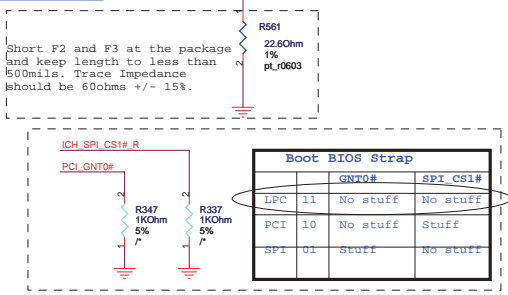
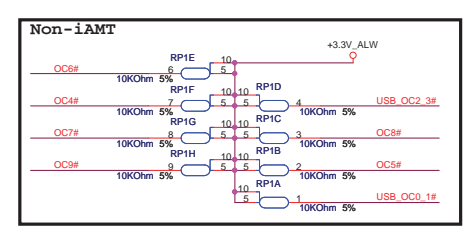
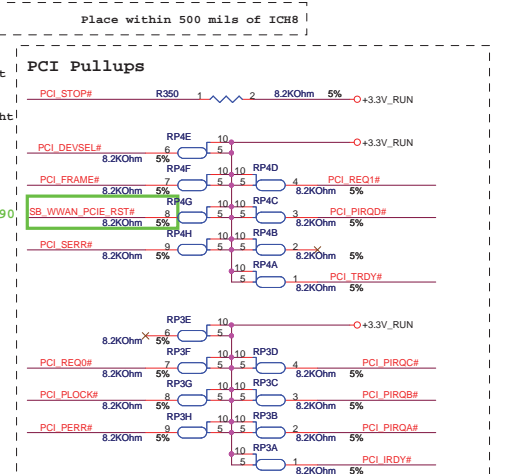
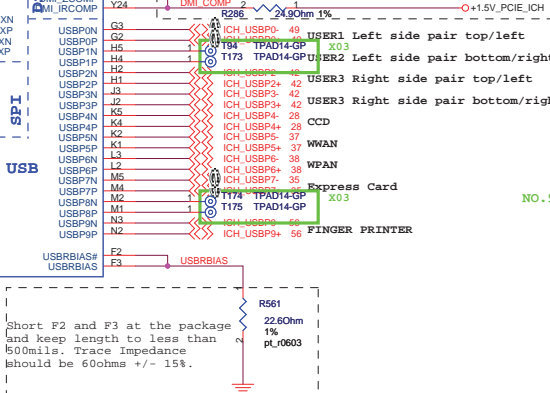
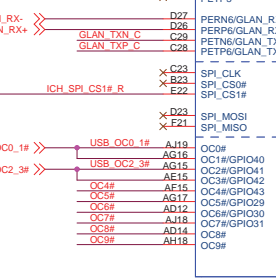
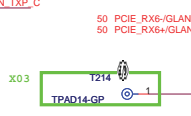
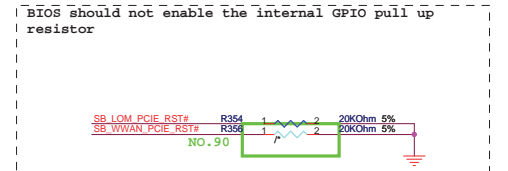
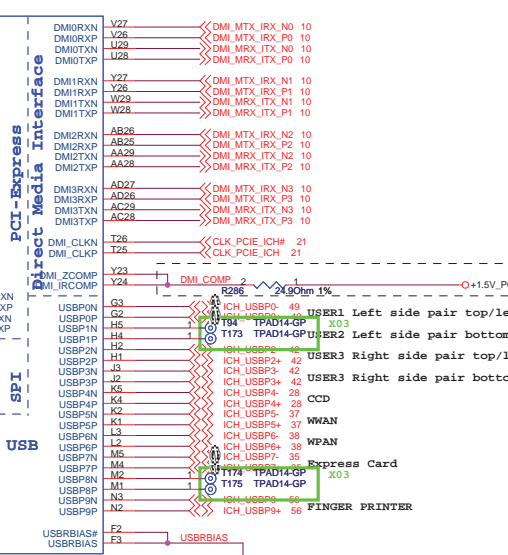
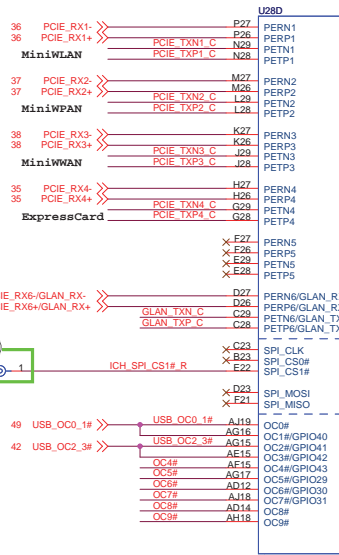
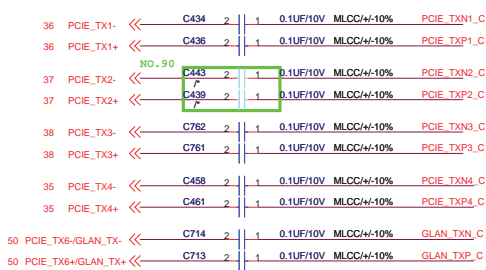
Place within 500 mils of ICH8 ball



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Place TX DC blocking caps close ICH8.



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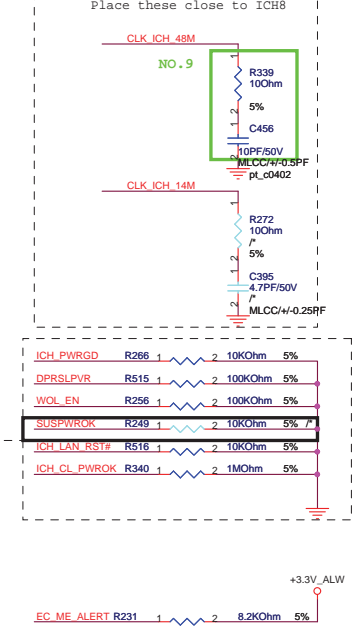
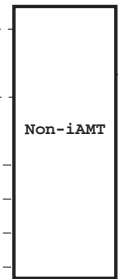
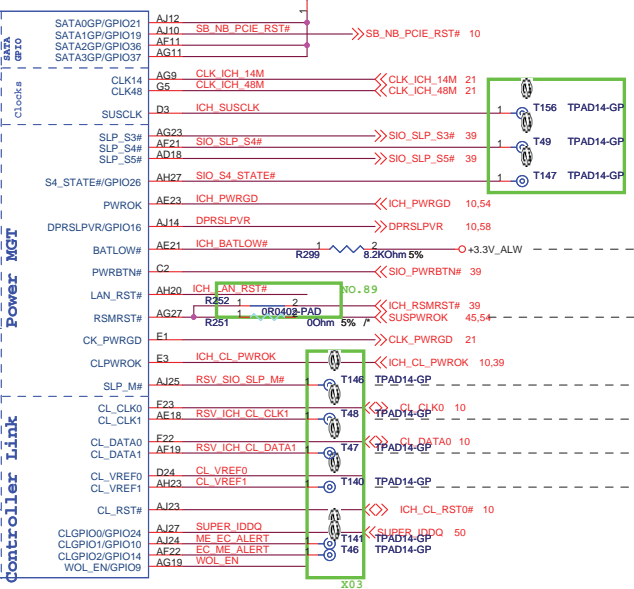
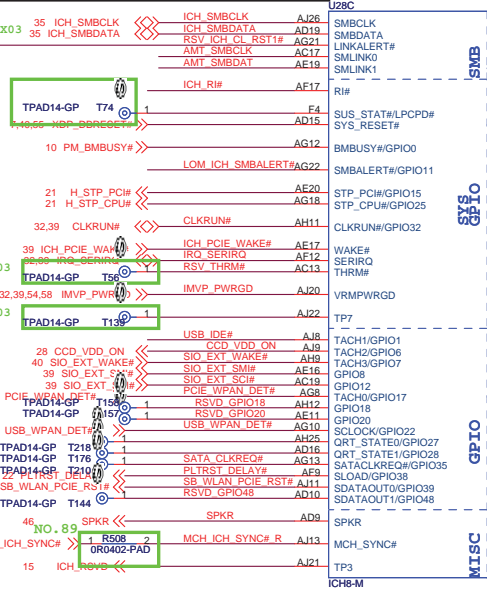
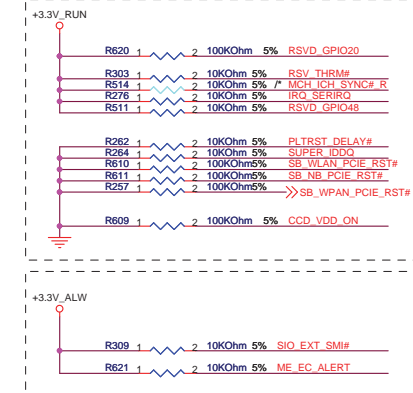
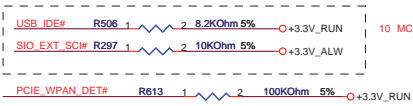
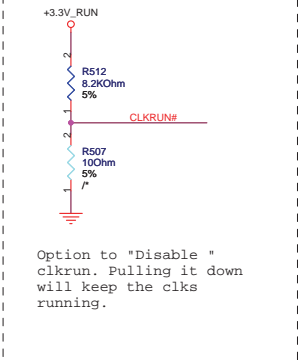
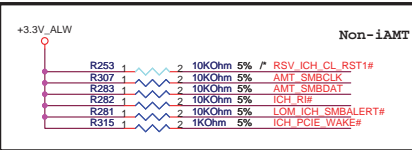
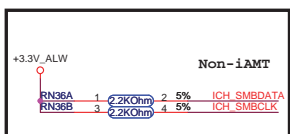
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Title: **Diaz-Discrete**

Doc Number: **IC8B: PCI/INT/DMI/USB**

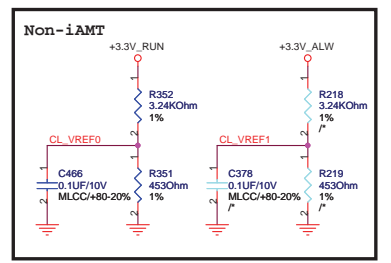
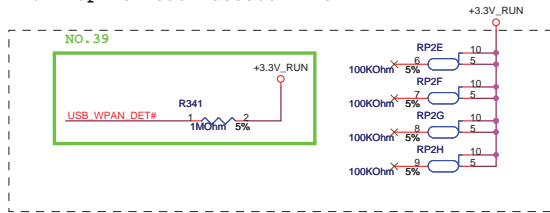
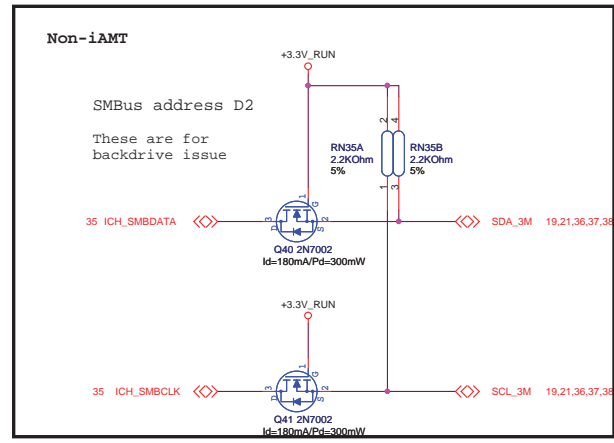
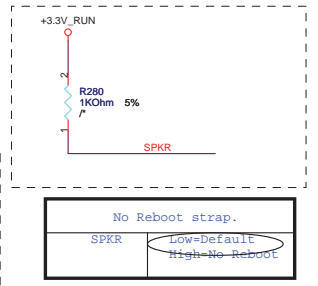
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Pull up for each detect line



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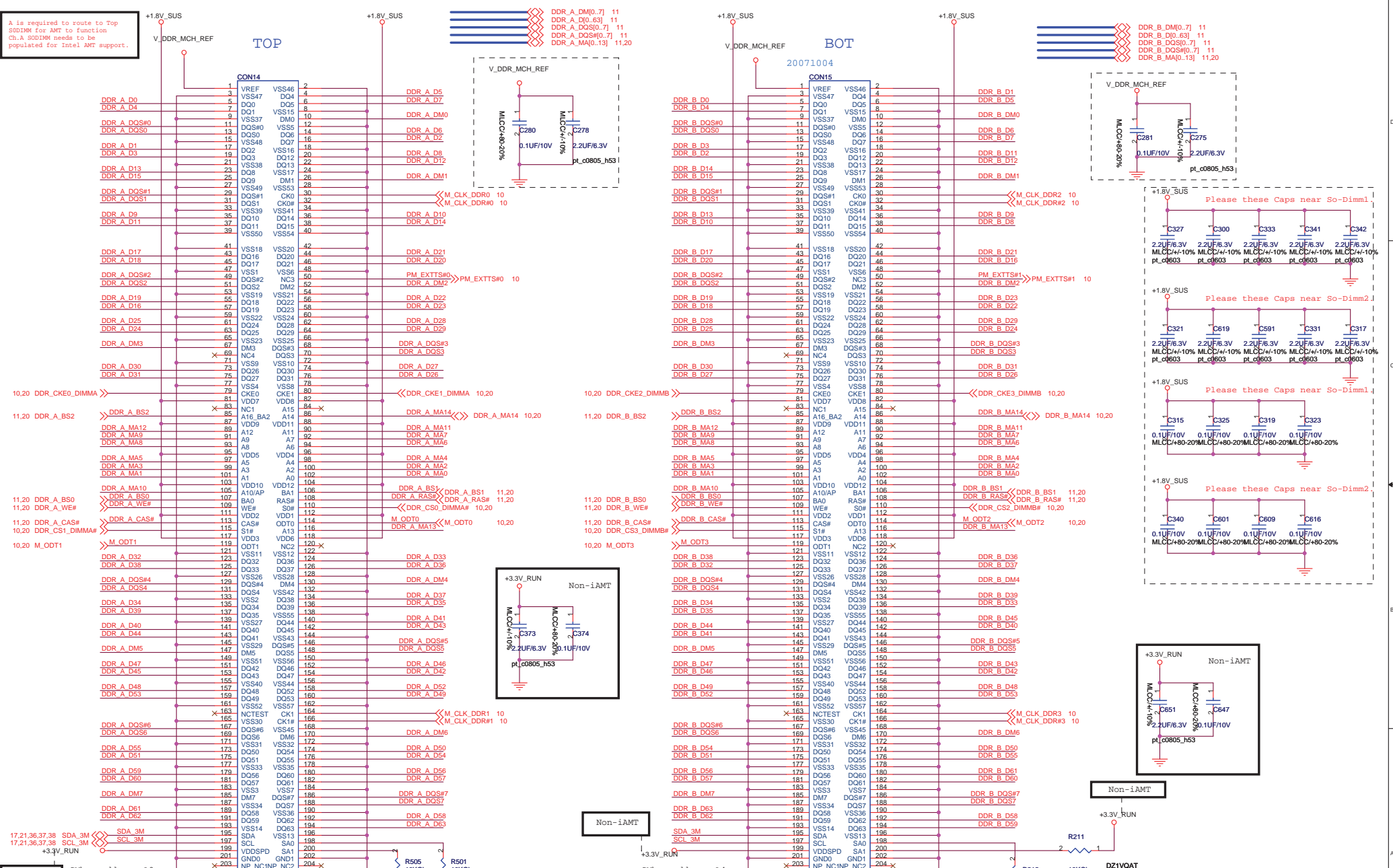
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File: **Diaz-Discrete**

Size: Document Number
Custm: **ICH8: SMB/PWR/CLK/GPIO** Rev: **A00**

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A is required to route to Top 8021M for AMT to function. Ch.A 8021M needs to be populated for Intel AMT support.



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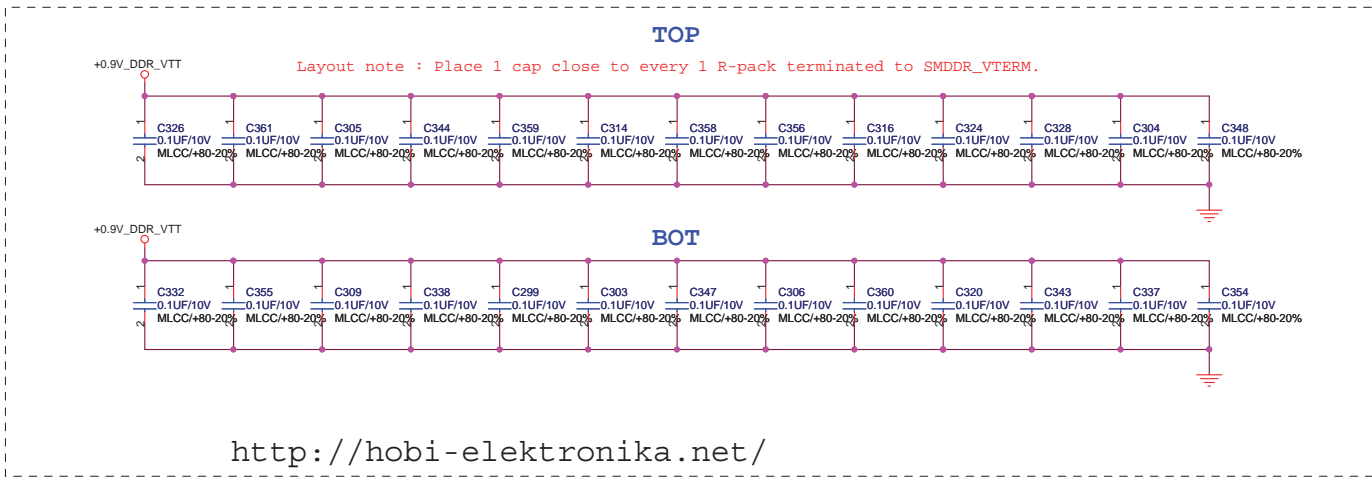
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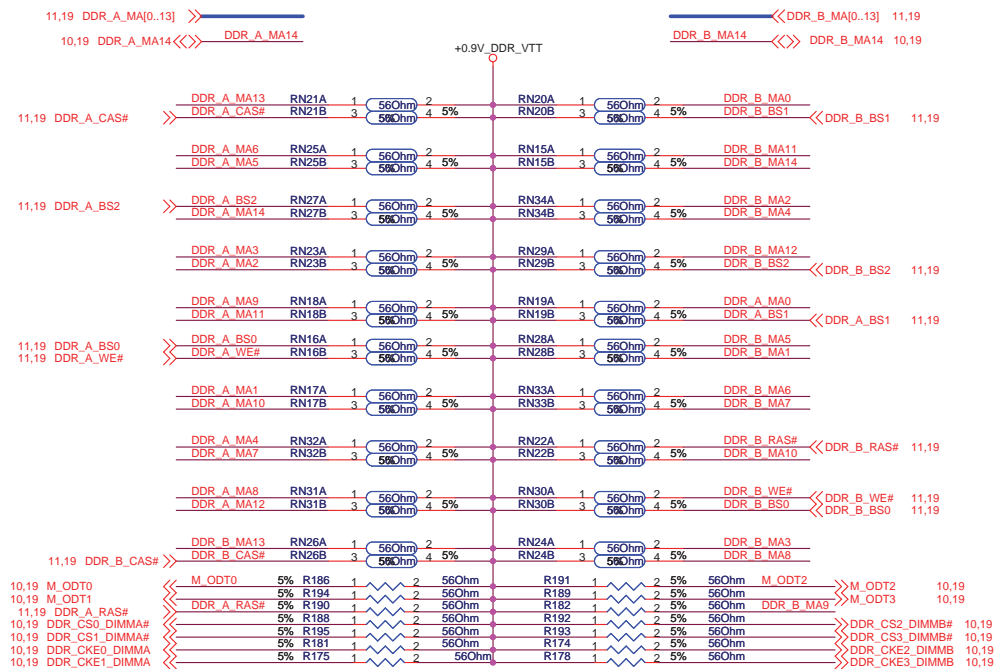
File: **Diaz-Discrete**

Size: Document Number **DDR2 SO-DIMM (0)** Rev: **A00**

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Please these resistor closely DIMMA, all trace length<750 mil.

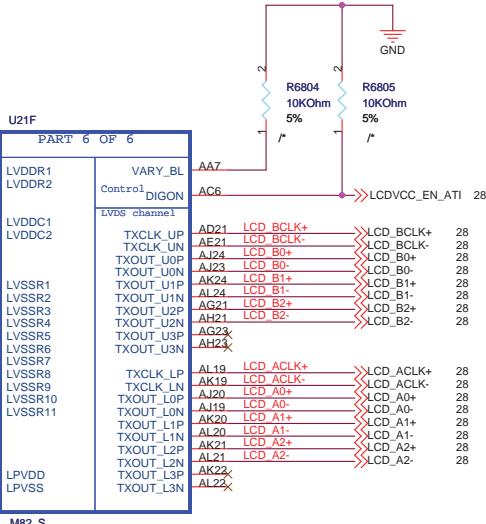
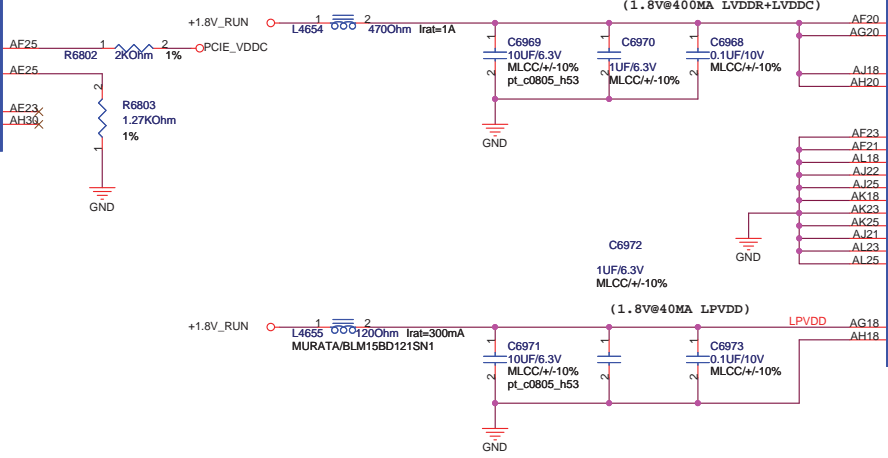
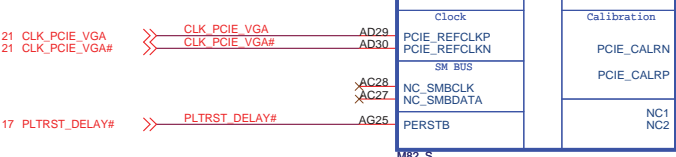
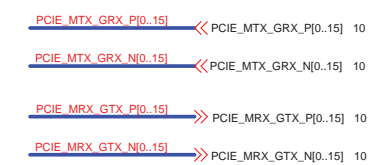
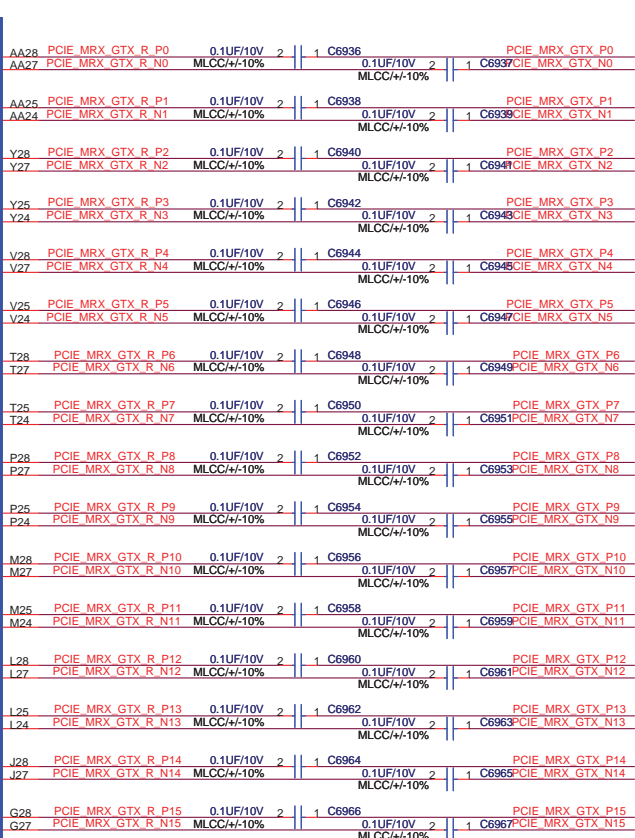
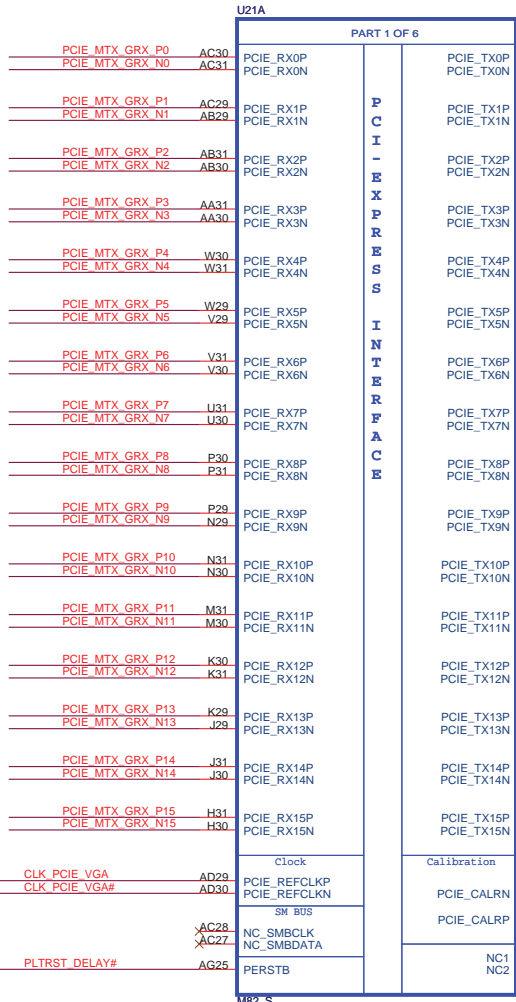


Please these resistor closely DIMMB, all trace length<750 mil.

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Title		
Diaz-Discrete		
Size	Document Number	Rev
A3	DDR2 SO-DIMM (1)	A00
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Taipei Hsien 221, Taiwan, R.O.C.

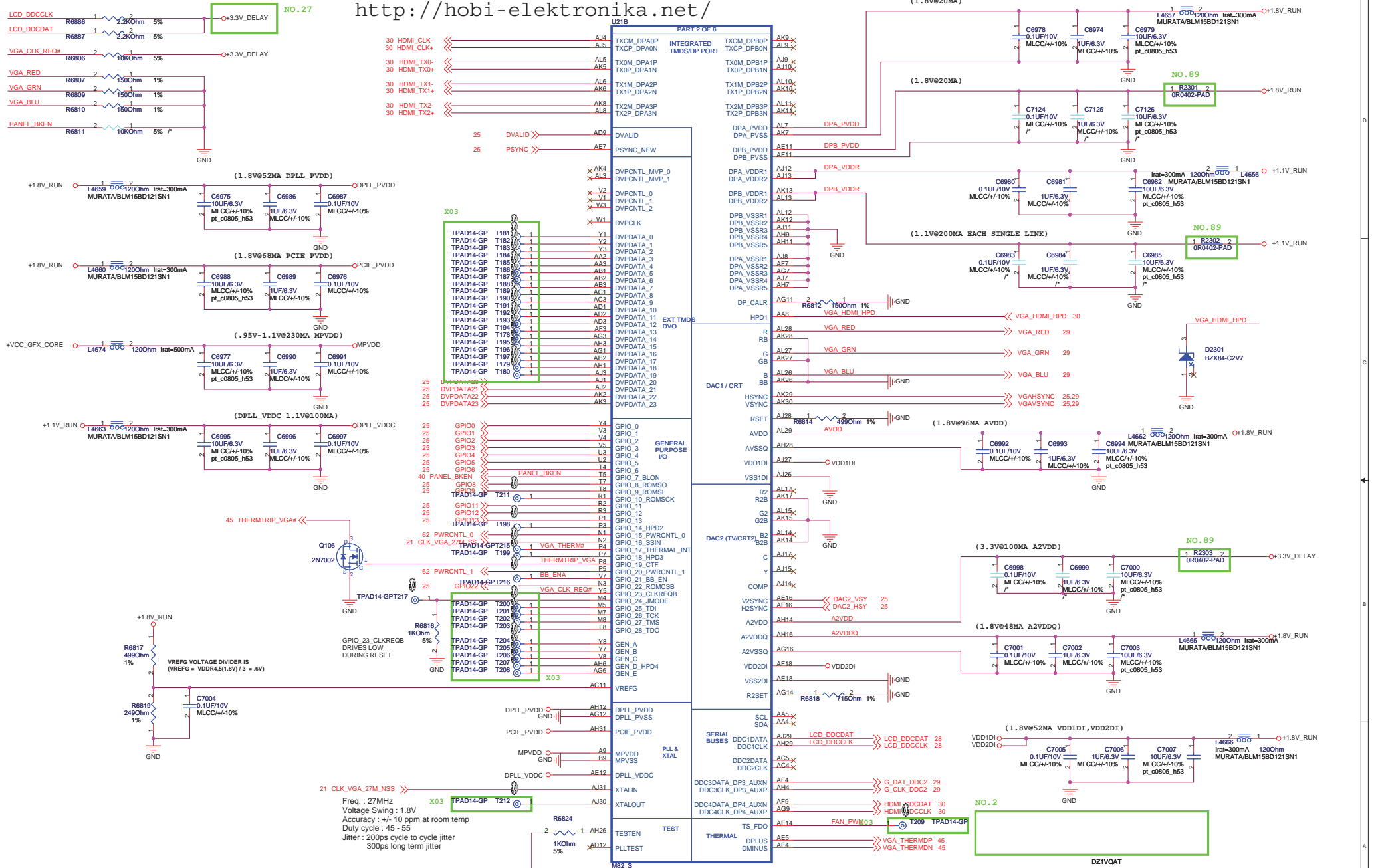
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Diaz-Discrete

Size **A3** Document Number **M82-MAIN(1)** Rev **A00**

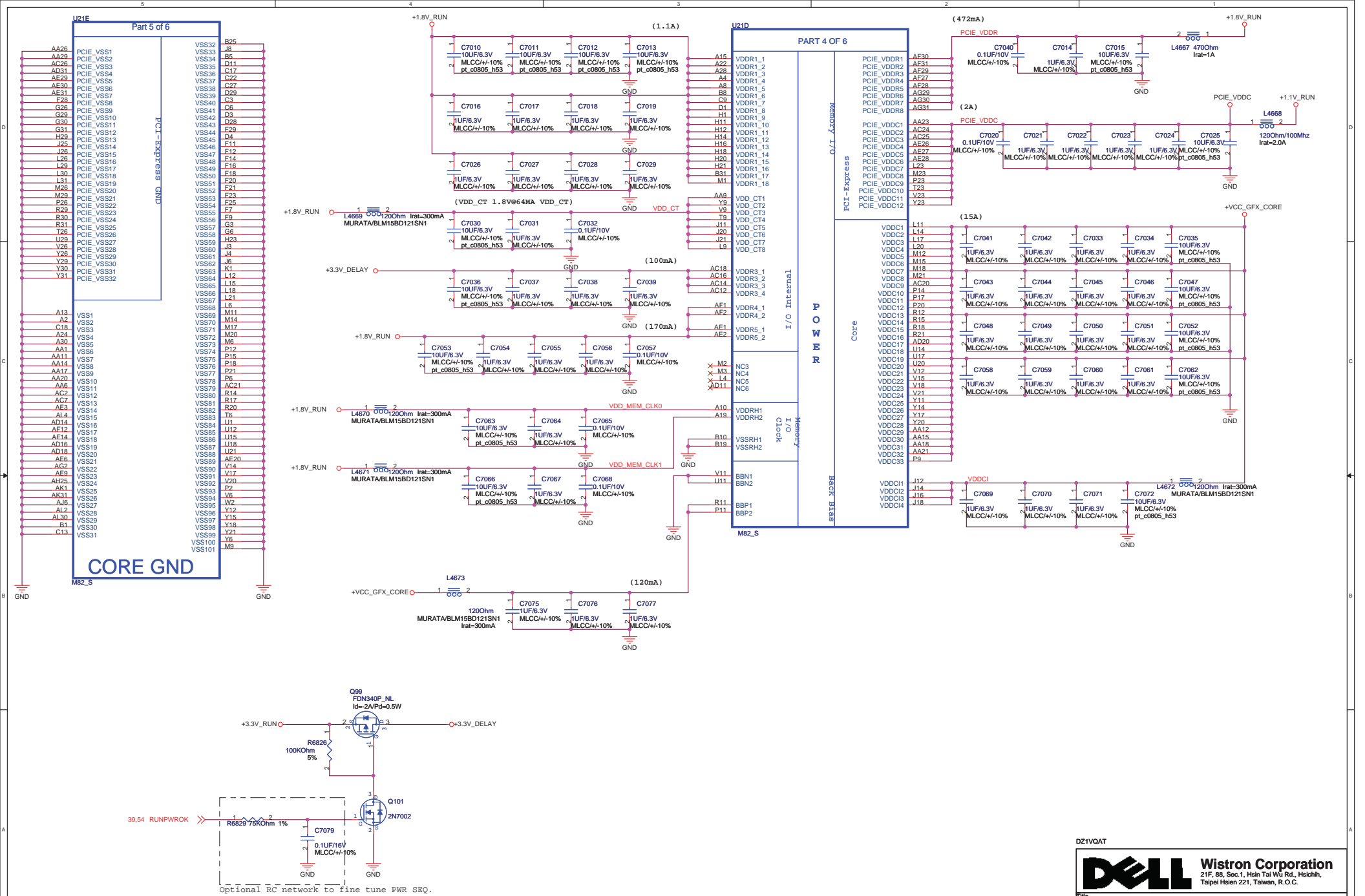
Date: Monday, August 25, 2008 Sheet 22 of 69

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Title: **Diaz-Discrete**
 Size: **Custpm** Document Number: **M82-MAIN(2)** Rev: **A00**
 Date: Monday, August 25, 2008 Sheet 23 of 69



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DZ1VQAT

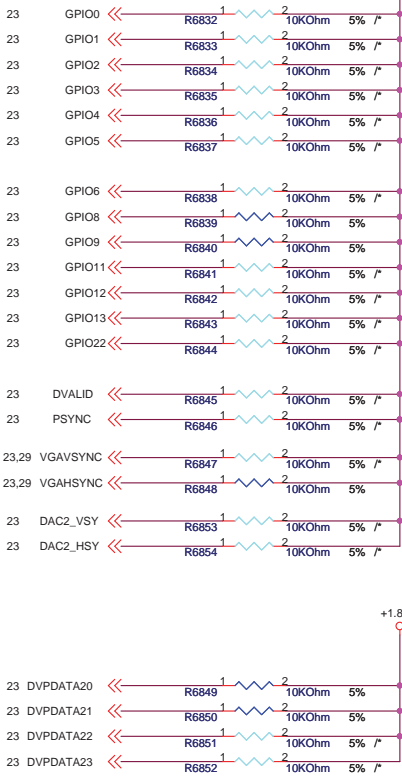
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Title: **Diaz-Discrete**

Size	Document Number	Rev
Custpm	M82-PWR_GND	A00
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NO. 27

+3.3V_DELAY



STRAPS	PIN	DESCRIPTION
TX_PWRS_ENB (Internal PD)	GPIO0	Transmitter Power Savings Enable V 0 = 50% Tx output swing 1 = Full Tx output swing
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable V 0 = Tx de-emphasis disabled 1 = Tx de-emphasis enabled
DEBUG_ACCESS (Internal PD)	GPIO4	DEBUG SIGNALS MUXED OUT
BIF_GEN2_EN_A	GPIO5	V 0 = Advertises the PCI-E device as 2.5GT/s 1 = Advertises the PCI-E device as 5GT/s
DEBUG_I2C_ENABLE (Internal PD)	GPIO6	Internal use only
AUDIO_EN (Internal PD)	GPIO8	0 = Disable HD Audio V 1 = Enable HD Audio
ROMIDCFG[3:0] (Internal PD)	GPIO[13:11,9]	if BIOS_ROM_EN=1, then Config[3:0] defines the ROM type if BIOS_ROM_EN=0, then Config[3:0] defines the primary memory aperture size
BIOS_ROM_EN (Internal PD)	GPIO_22_ROMCSB	Enable external BIOS ROM device V 0 = Disable external BIOS ROM device 1 = Enable external BIOS ROM device
VGA DIS (Internal PD)	PSYNC	V 0 = VGA Controller capacity enabled 1 = The device will not be recognized as the system's VGA Controller
HDMI_EN (Internal PD)	HSYNC	0 = Disable HDMI V 1 = Enable HDMI

ATI RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO2 , GPIO3 , DVALID , H2SYNC , V2SYNC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13:11,9]	Manufacturer	Part Number	GPIO[13:11,9]
V 128MB 256MB 64MB 32MB 512MB 1GB 2GB 4GB	x000	ST Microelectronics	M25P05A	0100
	x001		M25P10A	0101
	x010		M25P20	0101
	x011		M25P40	0101
	x100		M25P80	0101
		Chingis (formerly PMC)	Pm25LV512	0100
			Pm25LV010	0101

STRAPS	PIN	DESCRIPTION
MEM_TYPE (Internal PD)	DVPDATA(23:20)	MEMORY TYPE, MAKE AND SIZE INFO 0000 - GDDR3 16Mx32 Qimonda / HYB18H512321BF-14 0001 - GDDR3 16Mx32 Hynix / H5RS5223CFR-14 0010 - GDDR3 32Mx32 Qimonda / HYB18H1G321AF-14 0011 - GDDR3 32Mx32 Samsung / K4J10324QD-HC14 V 0100 - TBD 0101 - TBD 0110 - TBD 0111 - TBD 1000 - TBD

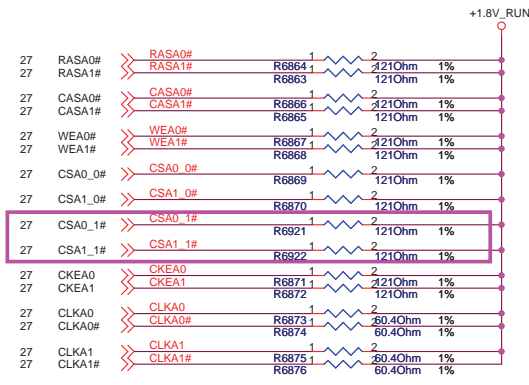
NO.11

DZ1VQAT



Title			Rev
Diaz-Discrete			
Size	Document Number	Rev	
A3	M82-STRAPPING	A00	
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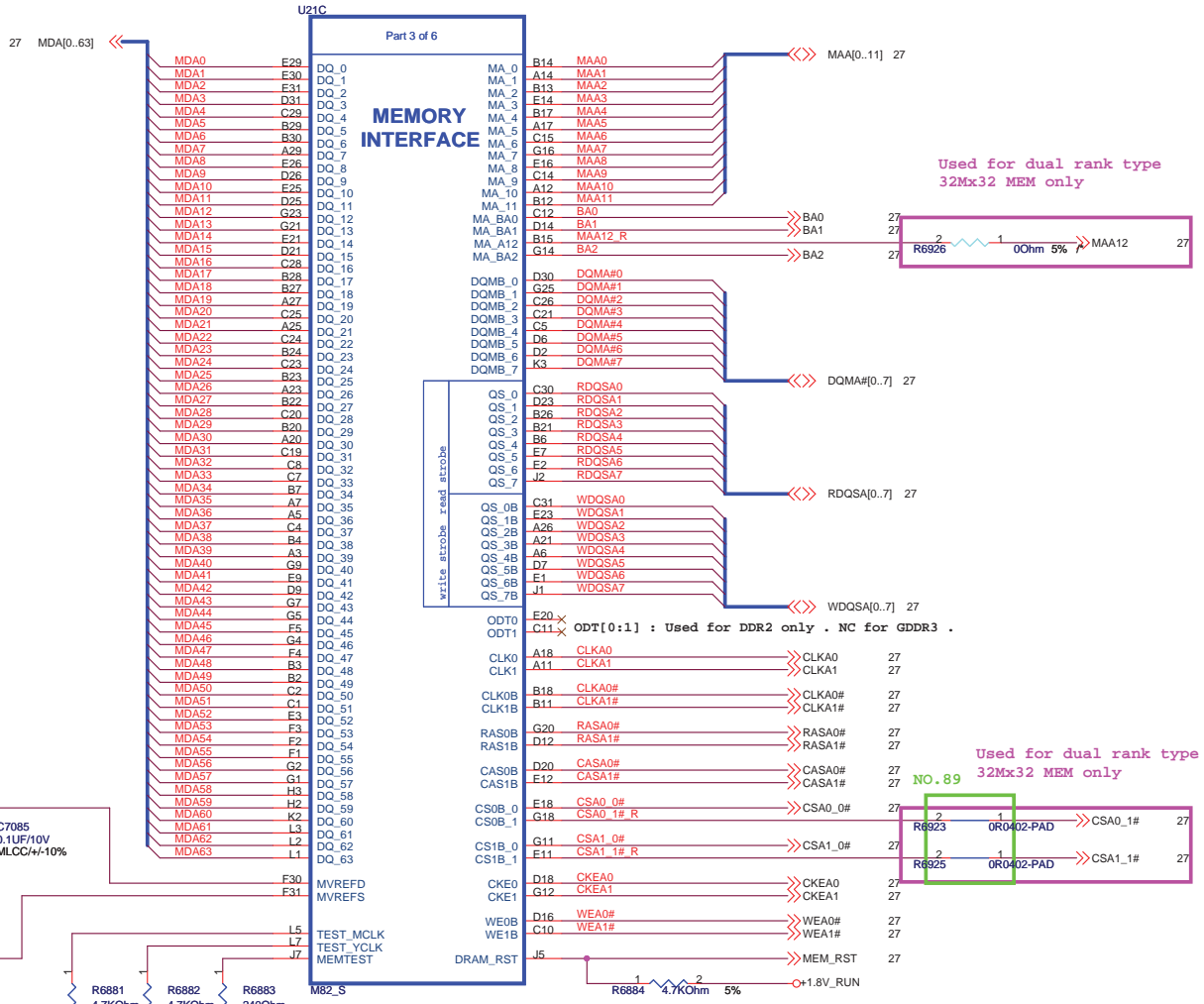
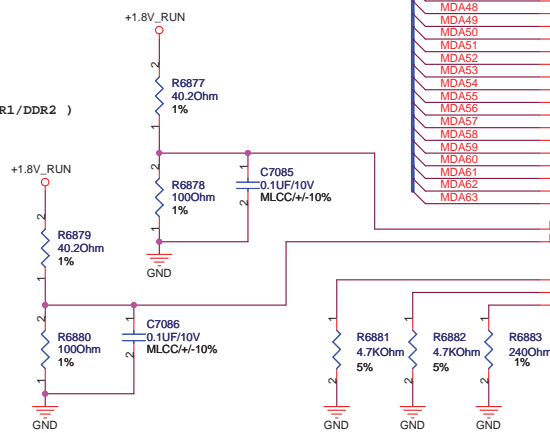
Place Close to VRAM



Used for dual rank type 32Mx32 MEM only

(0.5 * VDDR1) (for SSTL-1.8/SSTL-2/DDR1/GDDR1/DDR2)
 (0.7 * VDDR1) (for GDDR3/GDDR4)

DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R



Used for dual rank type 32Mx32 MEM only

Used for dual rank type 32Mx32 MEM only

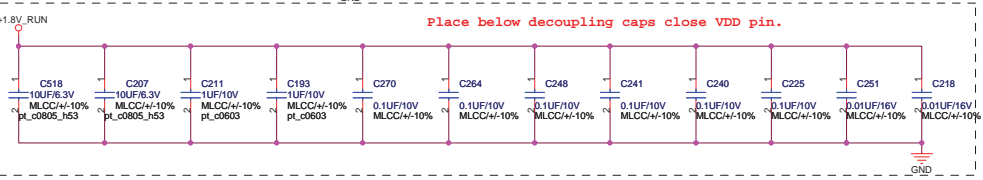
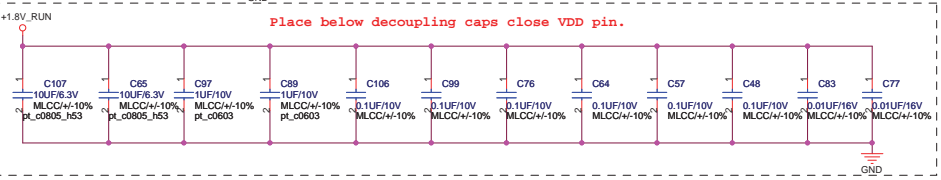
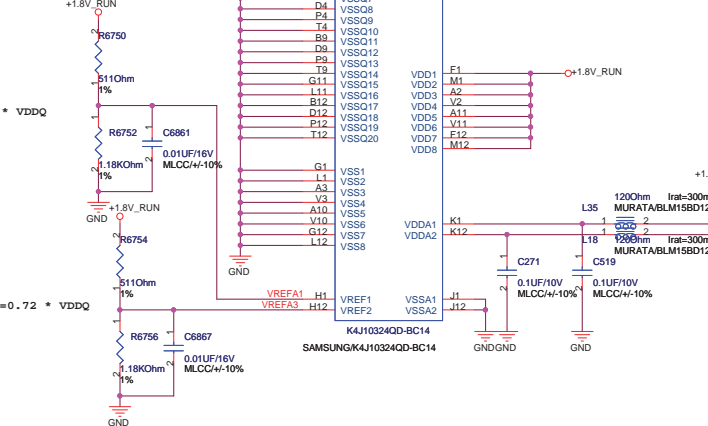
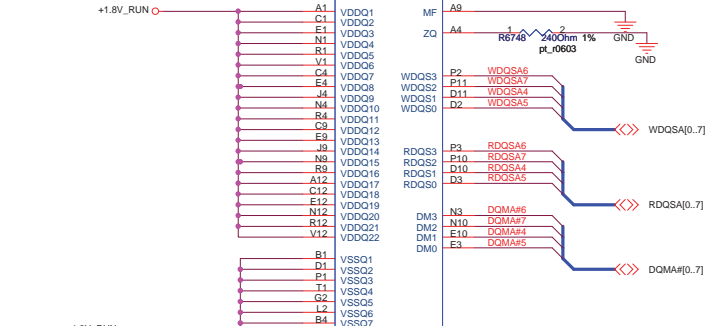
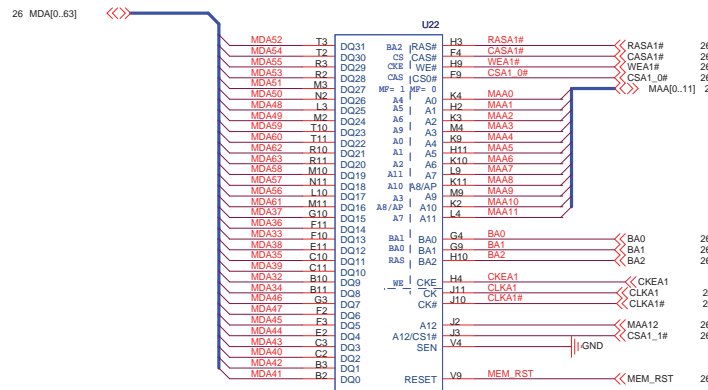
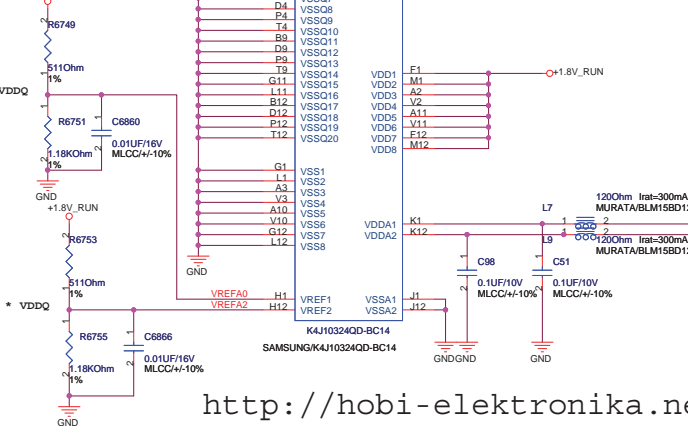
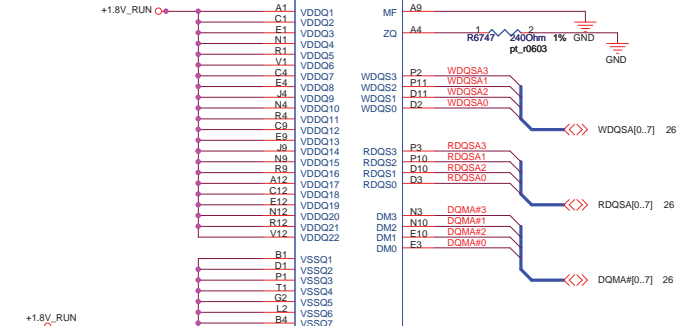
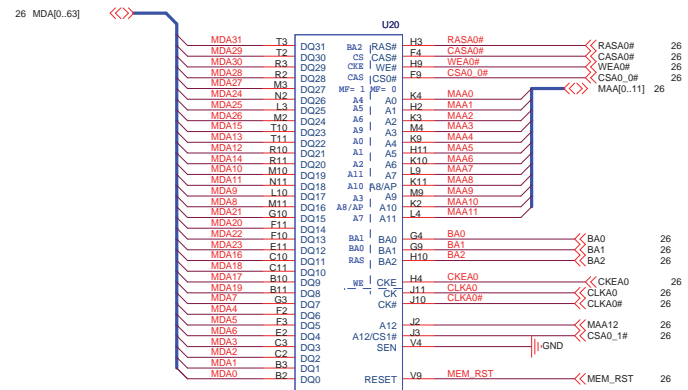
DZ1VQAT

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Title: **Diaz-Discrete**

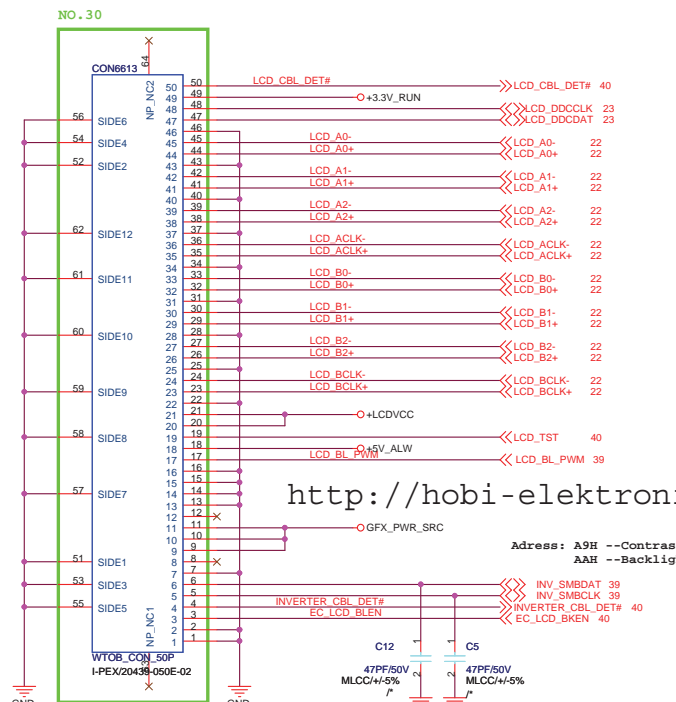
Size: **A3** Document Number: **M82-MEMORY INTERFACE** Rev: **A00**

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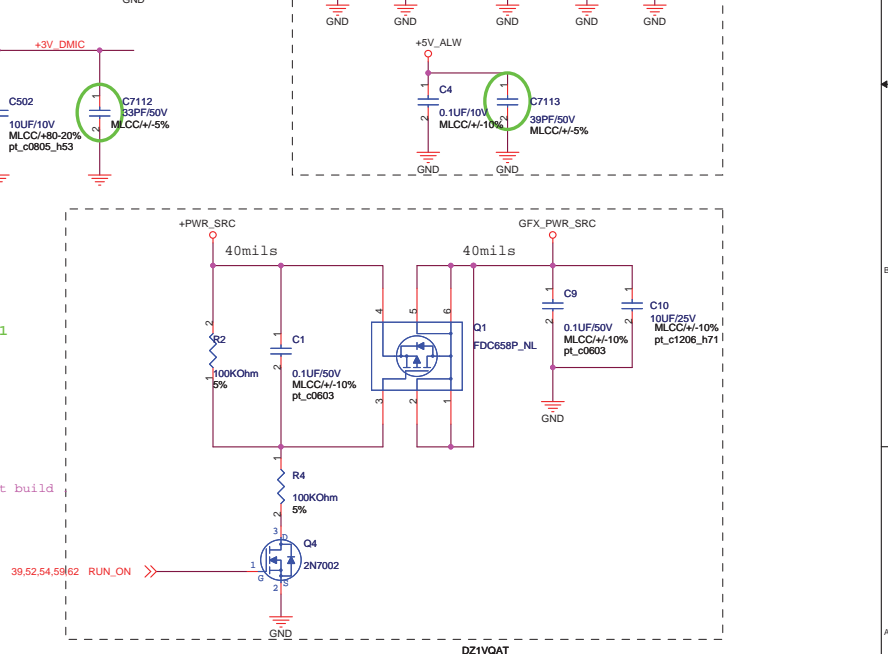
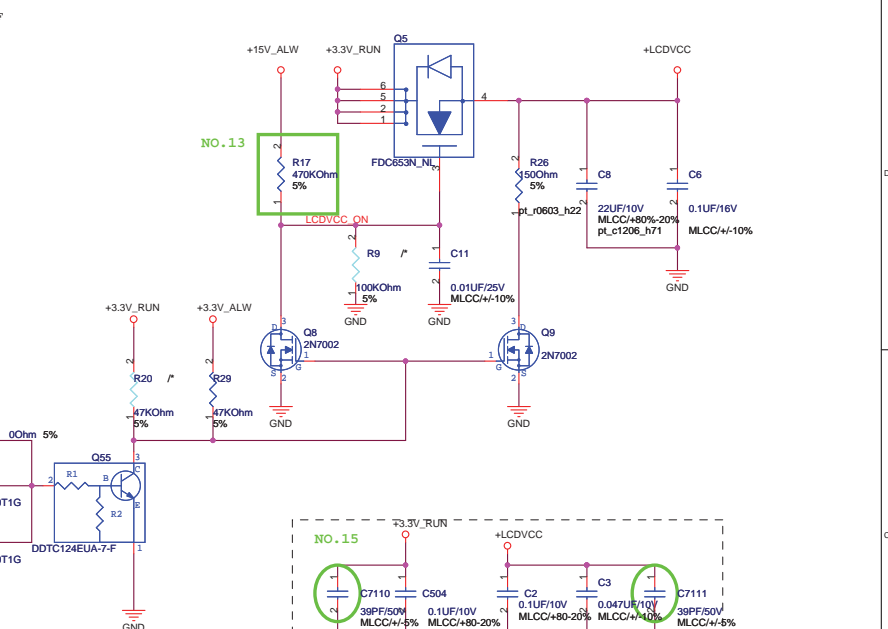
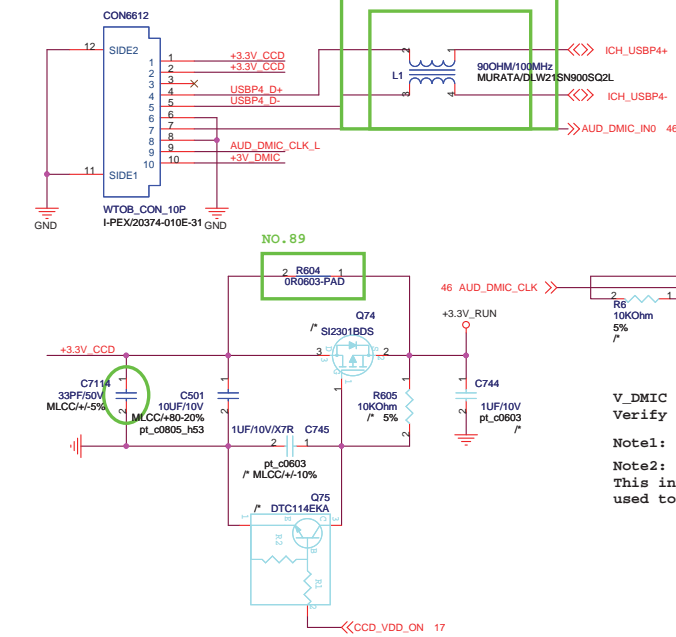
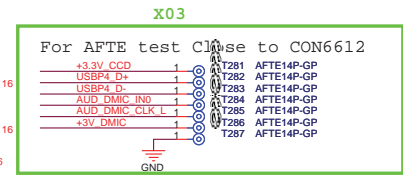
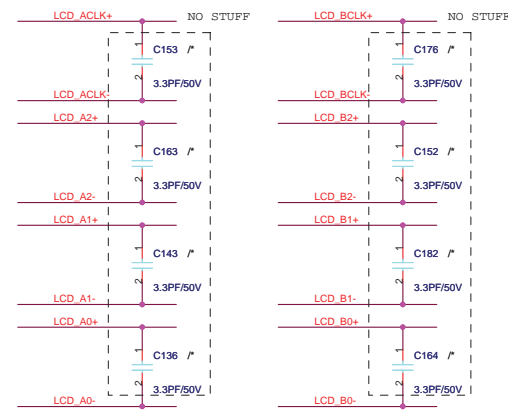
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 21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichin, Taipei Hsin Tai, Taiwan, R.O.C.
 Title: **Diaz-Discrete**
 Doc Number: **M82-GDDR3 32MX32 MEMORY**
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Address: A9H --Contrast
AAH --Backlight



Reserve for EMI
Change to 0ohm*2 from Bead and 47ohm for first build

V_DMIC IS DEPENDENT ON MIC SELECTION (1.8V - 3.3V TYP)
Verify to ensure operability with chosen mic supplier.

Notel: If only 1 digital mic, use AUD_DMIC_IN0.
Note2: If using 2 dig mics, also use AUD_DMIC_IN0.
This input supports 2 digimics. AUD_DMIC_IN1 is only used to support 4 dig mics.

DZ1VQAT

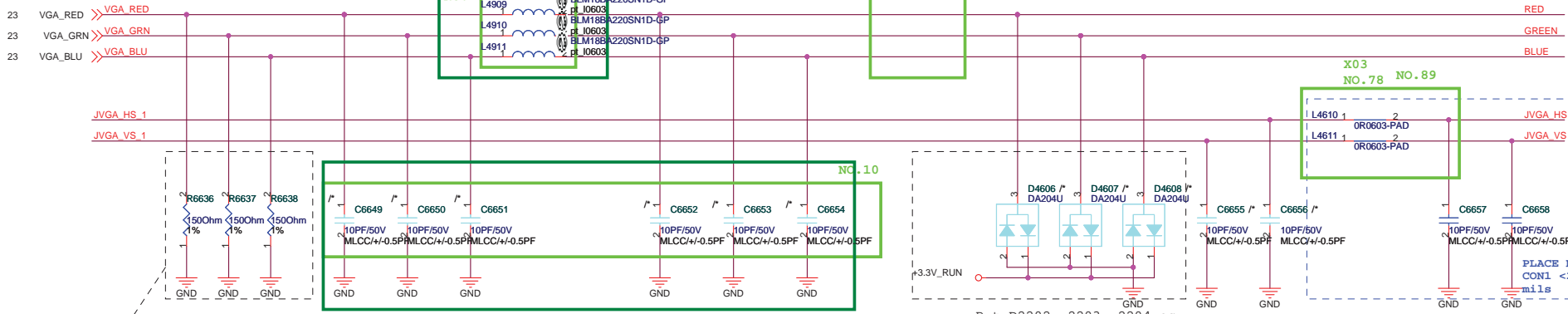
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Title: **Diaz-Discrete**

Size: Document Number
Custpm **LVDS CON** Rev: **A00**

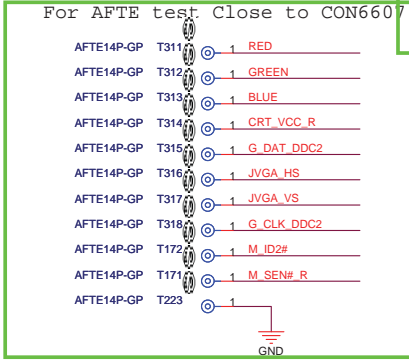
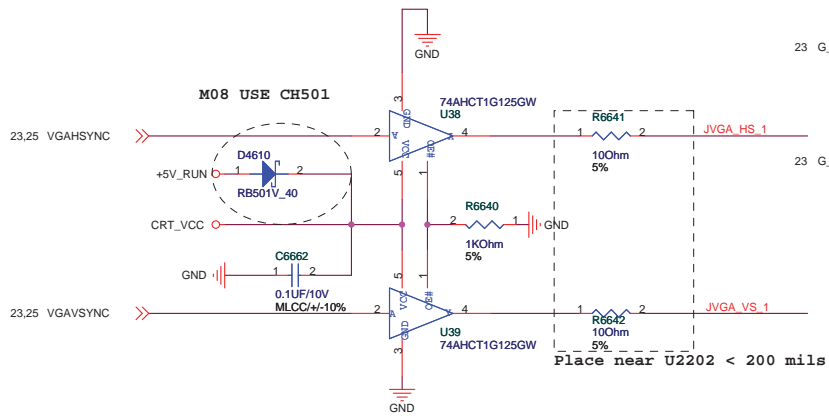
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Setting R,G,B treac impedance to 50 ohm.



In addition to these 150 ohm terminations at the connector, 150 ohm terminations are also required at the Source. Route from source (GPU) at 50 ohm target impedance.

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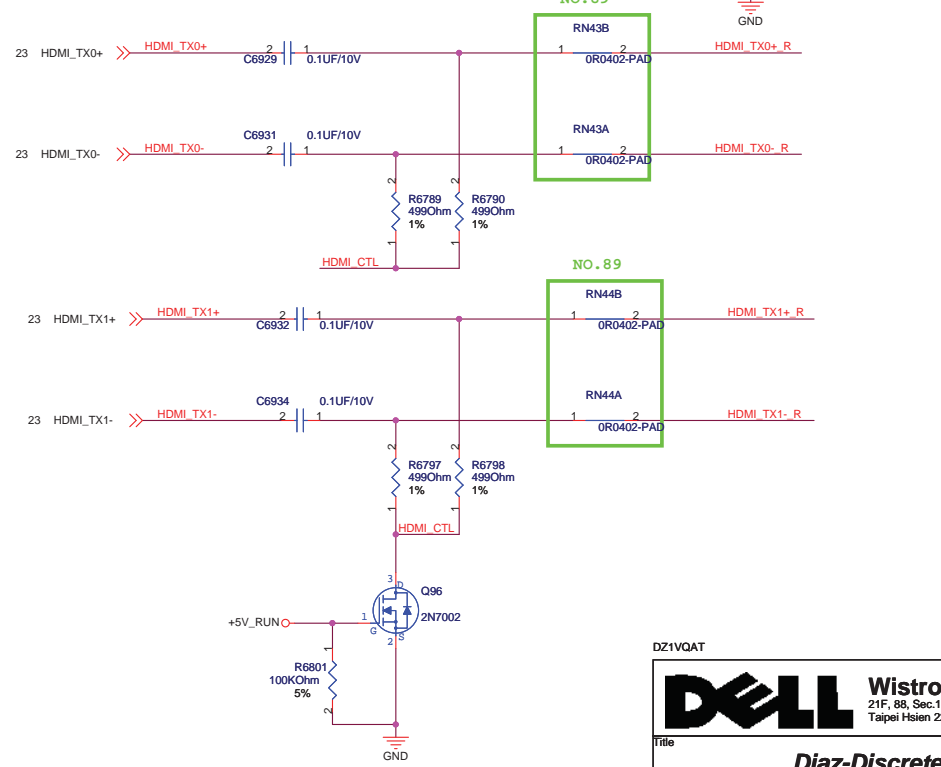
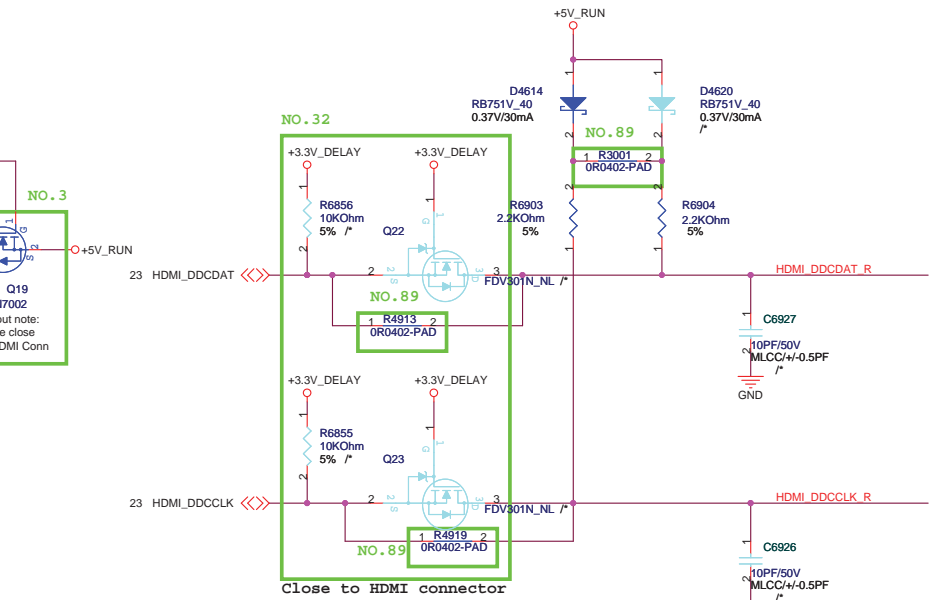
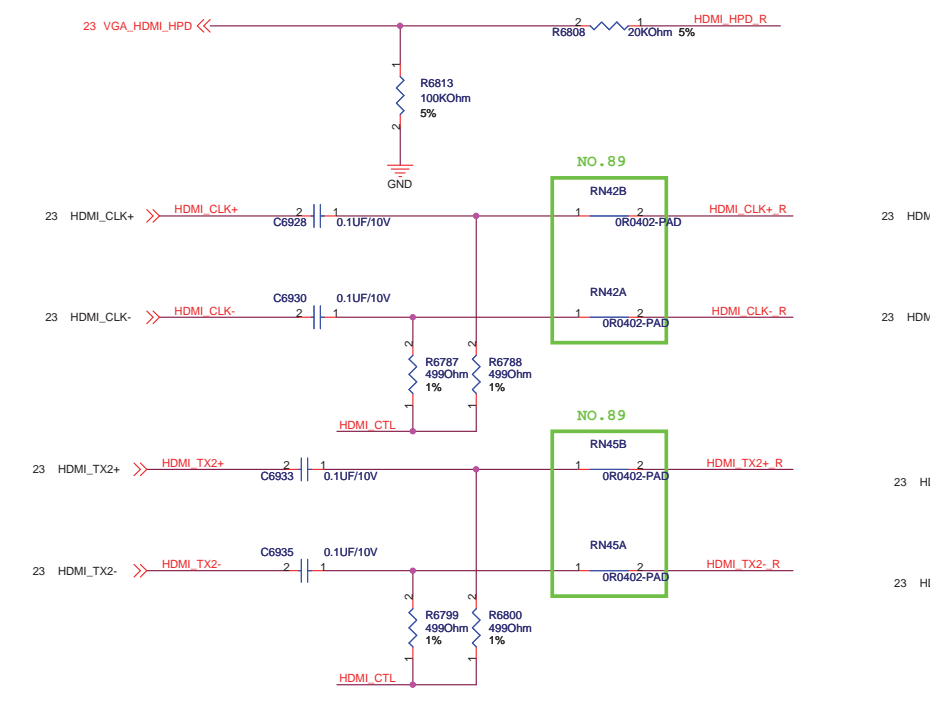
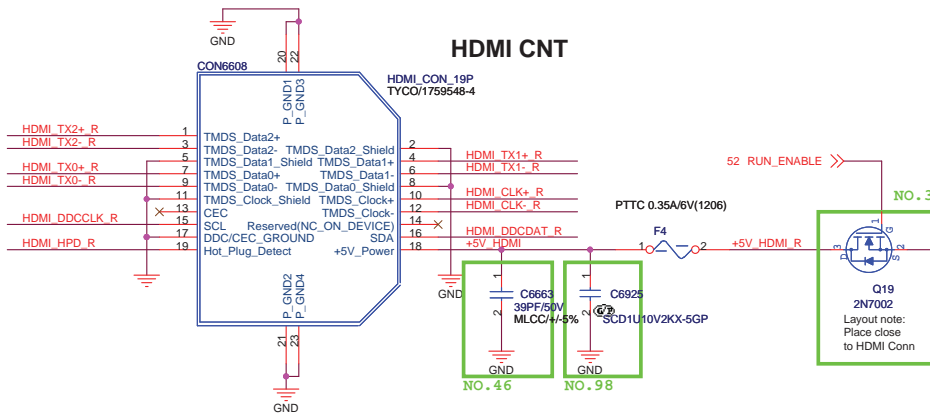
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title

Diaz-Discrete

Size **A3** Document Number **VGA CRT CON** Rev **A00**

Date: Monday, August 25, 2008 Sheet 29 of 69



<http://hobi-elektronika.net/>

DZ1VQAT

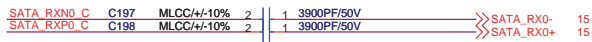
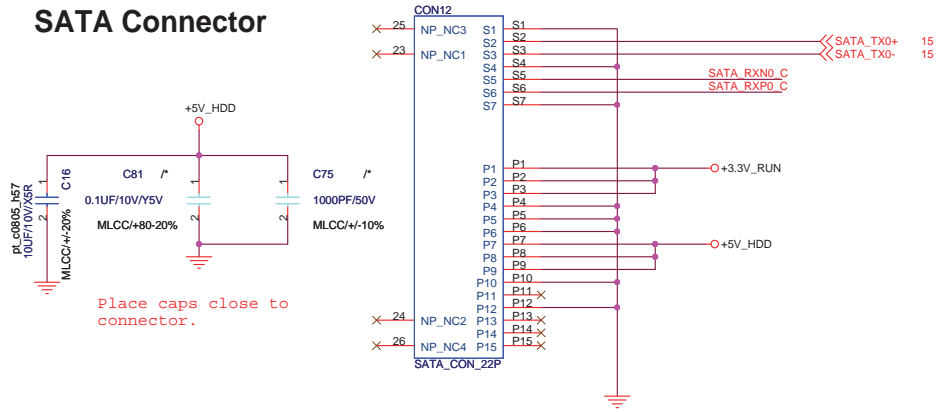
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

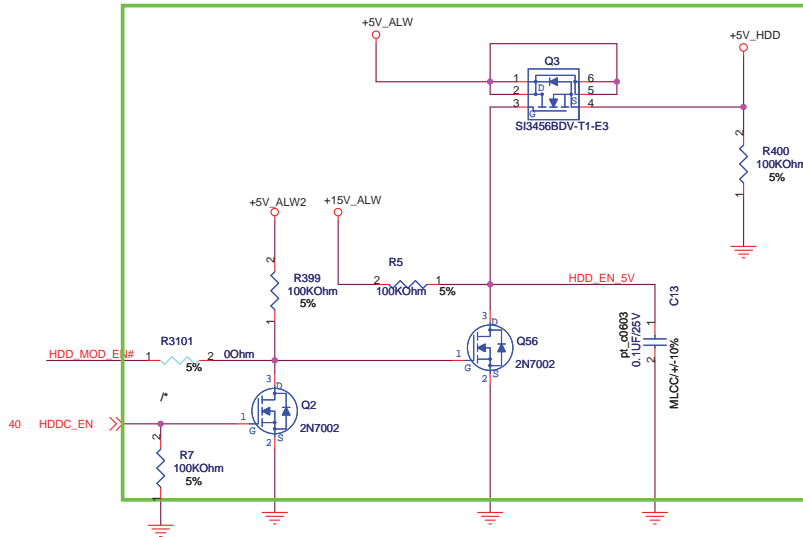
Size **A3** Document Number **HDMI** Rev **A00**

Date: Monday, August 25, 2008 Sheet 30 of 69

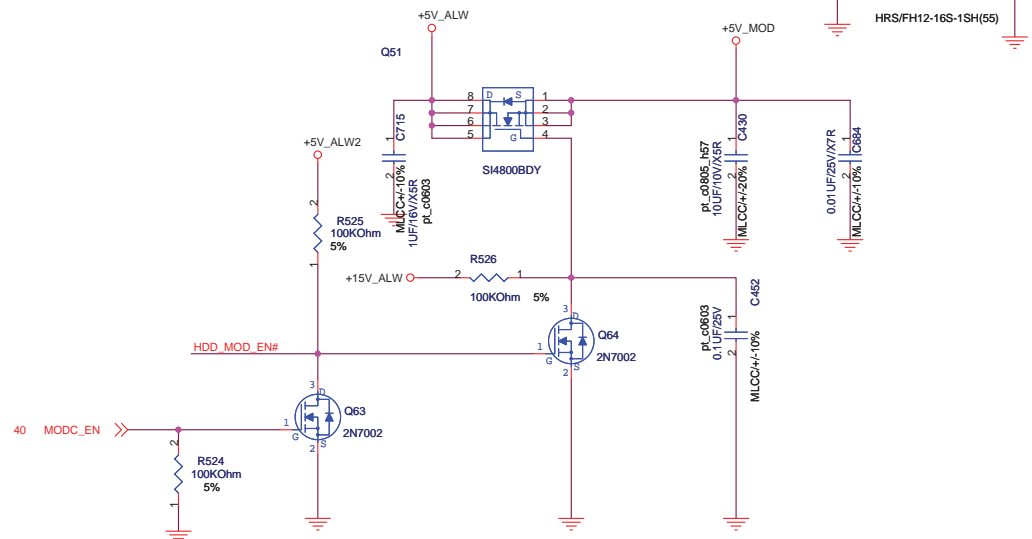
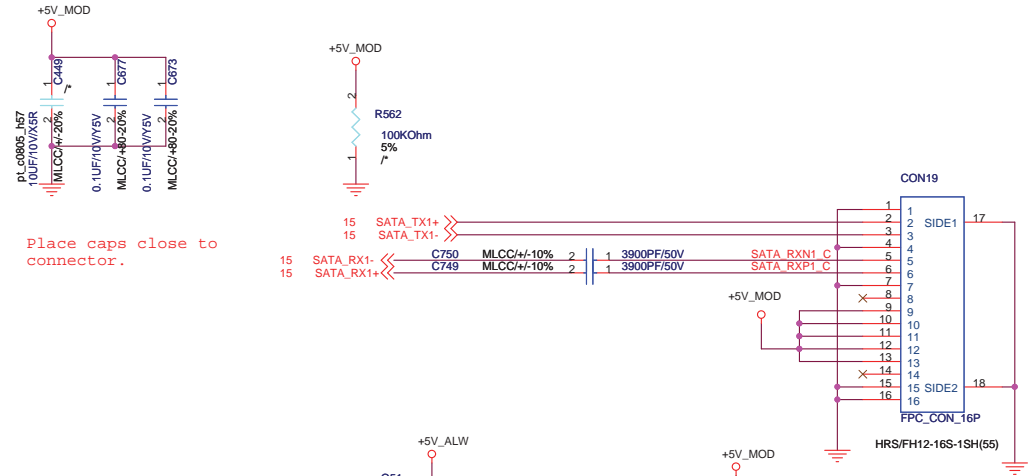
SATA Connector



NO. 34



ODD Connector



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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

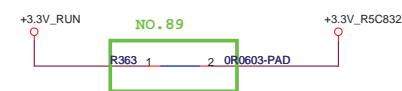
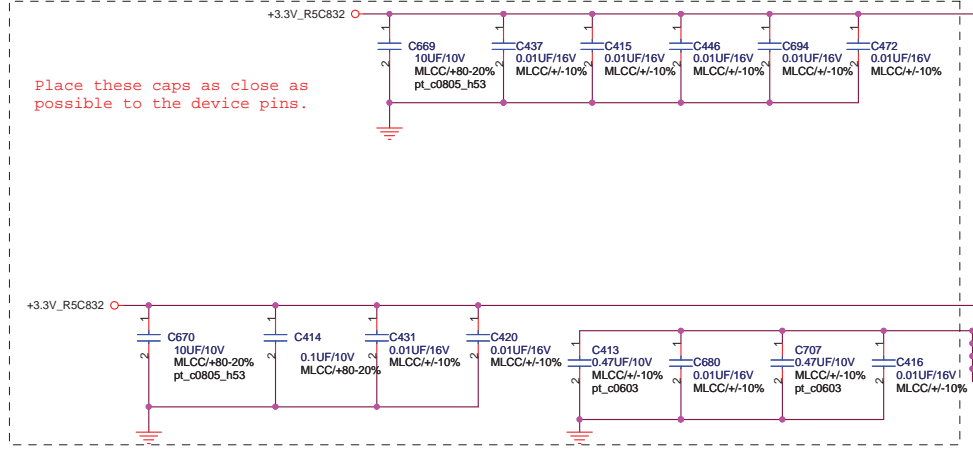
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Diaz-Discrete

Size **A3** Document Number **SATA(HDD & CD_ROM)** Rev **A00**

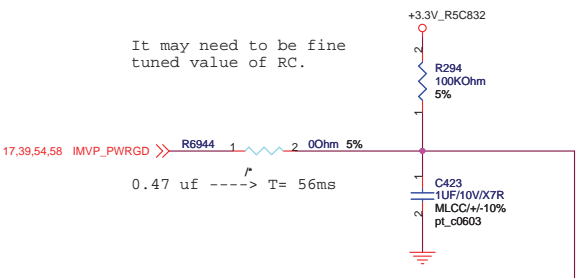
Date: Monday, August 25, 2008 Sheet 31 of 69

Place these caps as close as possible to the device pins.



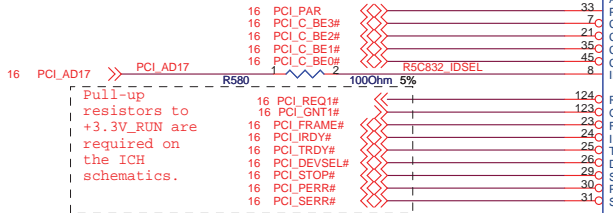
<http://hobi-elektronika.net/>

It may need to be fine tuned value of RC.



- PCI AD31 125 AD31
- PCI AD30 126 AD30
- PCI AD29 127 AD29
- PCI AD28 1 AD28
- PCI AD27 2 AD27
- PCI AD26 3 AD26
- PCI AD25 5 AD25
- PCI AD24 6 AD24
- PCI AD23 9 AD23
- PCI AD22 11 AD22
- PCI AD21 12 AD21
- PCI AD20 14 AD20
- PCI AD19 15 AD19
- PCI AD18 17 AD18
- PCI AD17 18 AD17
- PCI AD16 19 AD16
- PCI AD15 36 AD15
- PCI AD14 37 AD14
- PCI AD13 38 AD13
- PCI AD12 39 AD12
- PCI AD11 40 AD11
- PCI AD10 42 AD10
- PCI AD9 43 AD9
- PCI AD8 44 AD8
- PCI AD7 46 AD7
- PCI AD6 47 AD6
- PCI AD5 48 AD5
- PCI AD4 49 AD4
- PCI AD3 50 AD3
- PCI AD2 51 AD2
- PCI AD1 52 AD1
- PCI AD0 53 AD0

16 PCI_AD[0..31] <<>



16 PCI_AD17 >>> PCI_AD17

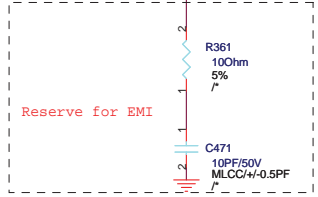
16 PCI_RST# >>>

40 SYS_PME# <<<

17.39 CLKRUN# <<<

Route to CLK GEN .

21 CLK_PCL_PCCARD >>>

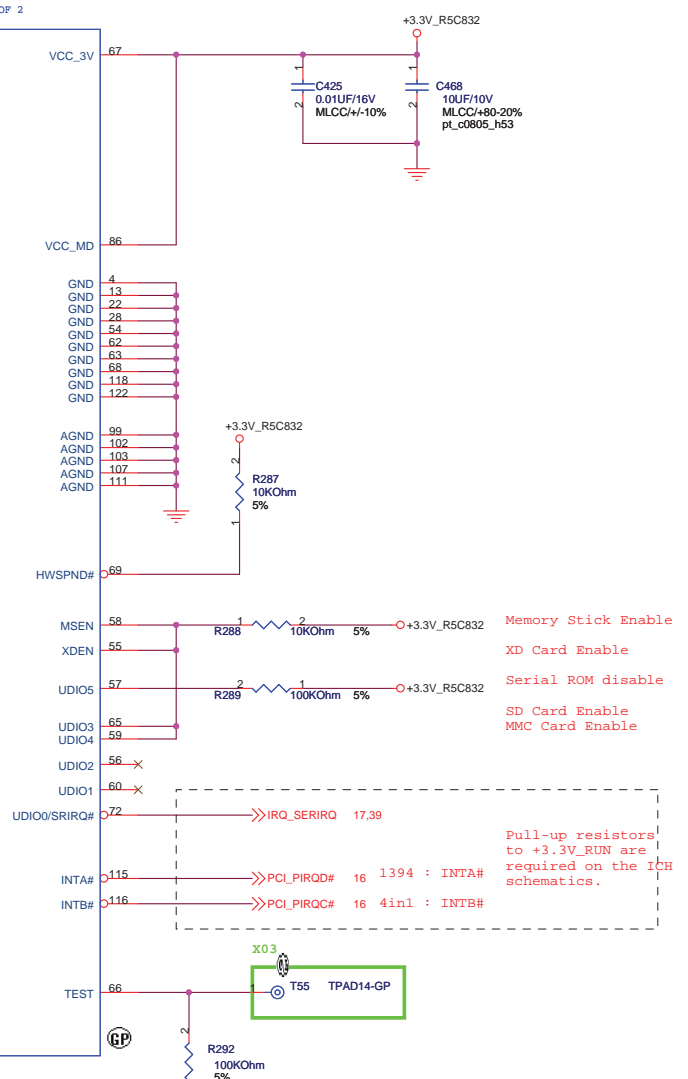


Reserve for EMI

Pull-up to +3.3V_ALW is required on SYS_PME# on EC schematics. (From EC). 0 ohm of PME# is no-stuff to prevent backdrive from this signal since the controller is powered of the RUN rail

The ICH schematics need to include a pull-up resistor to implement CLKRUN#, and the ICH schematics must have a pull-down, or constantly drive the signal low, in order to disable CLKRUN#.

Ricoh R5C832 Package Type : TQFP-128-P1 (141)



Memory Stick Enable
XD Card Enable
Serial ROM disable
SD Card Enable
MMC Card Enable

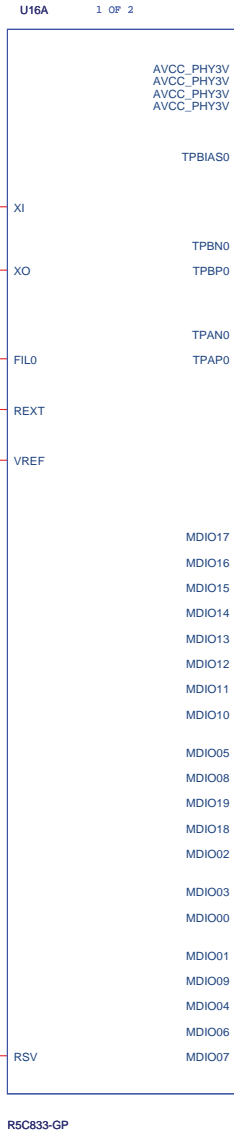
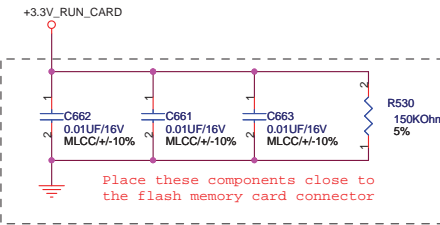
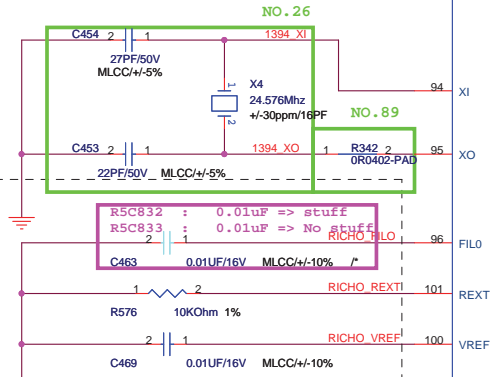
Pull-up resistors to +3.3V_RUN are required on the ICH schematics.



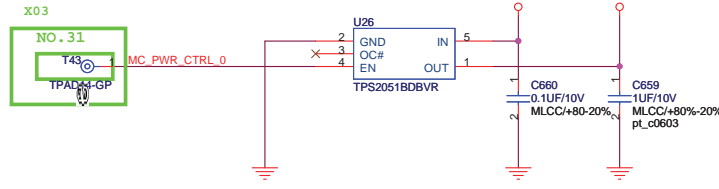
Title		
Diaz-Discrete		
Size	Document Number	Rev
A3	R5C833 - PCI INTERFACE	A00
Date:	Monday, August 25, 2008	Sheet 32 of 69

Recommended Crystal Specs from Data Sheet:

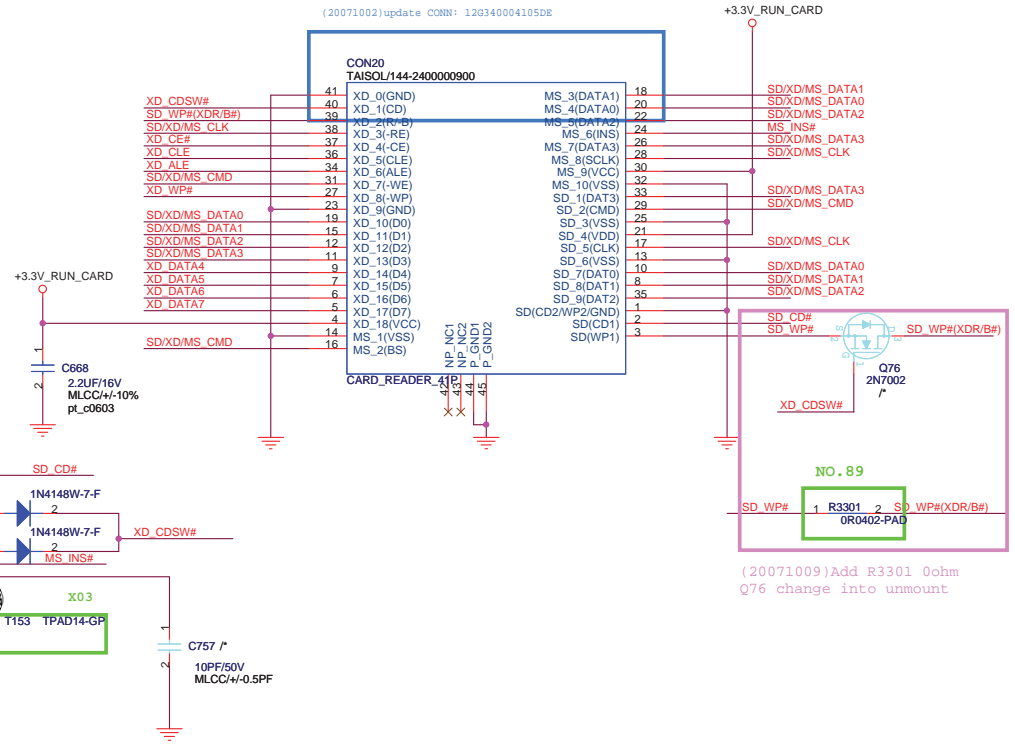
Normal Frequency : 24.576 MHz
 Frequency Tolerance : +/- 50ppm @ 25C
 Driver Level : .1 mW
 Load capacitance : 10pF
 Equ. Resistance : 50 Ohm Max
 Shunt Capacitance : 7.0pF Max



For SD/MS Card Power



(20071002)update CONN: 120340004105D8



<http://hobi-elektronika.net/>

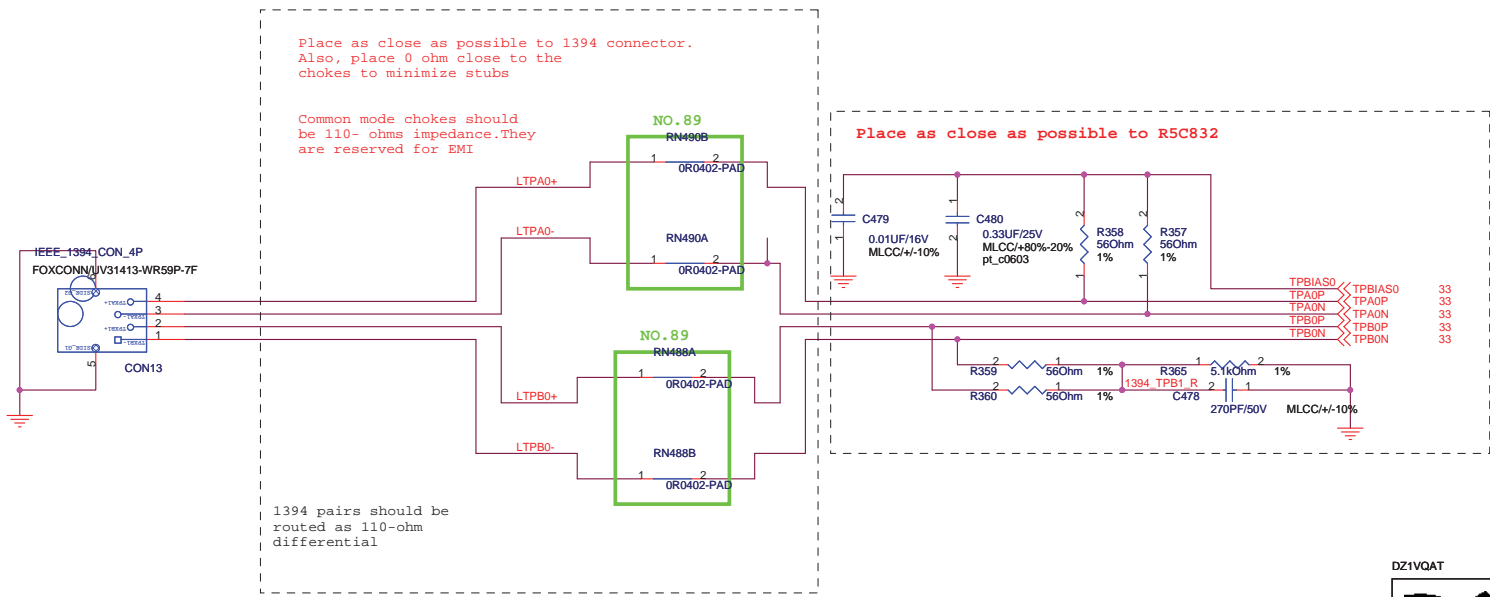
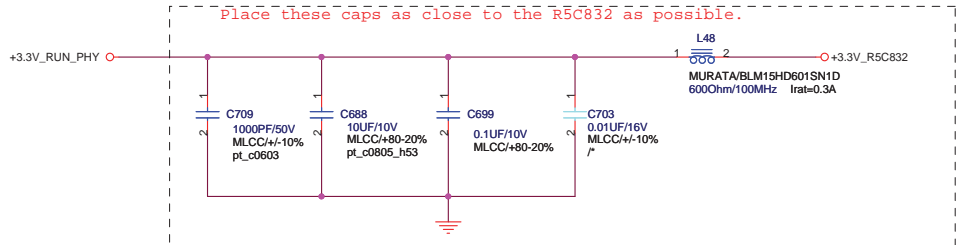
DZ1VQAT

Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **Diaz-Discrete**

Size: **A3** Document Number: **R5C833 - FLASH MEMORY PART A00** Rev: **A00**

Date: Monday, August 25, 2008 Sheet 33 of 69



DZ1VQAT

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Taipei Hsien 221, Taiwan, R.O.C.

Title

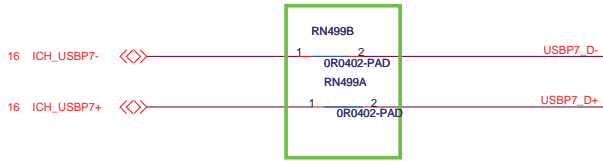
Diaz-Discrete

Size **A3** Document Number **R5C833 - IEEE1394 PART** Rev **A00**

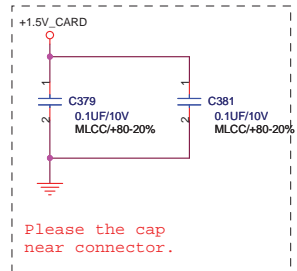
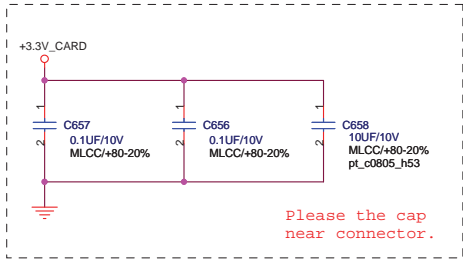
Date: Monday, August 25, 2008 Sheet 34 of 69

Express Card

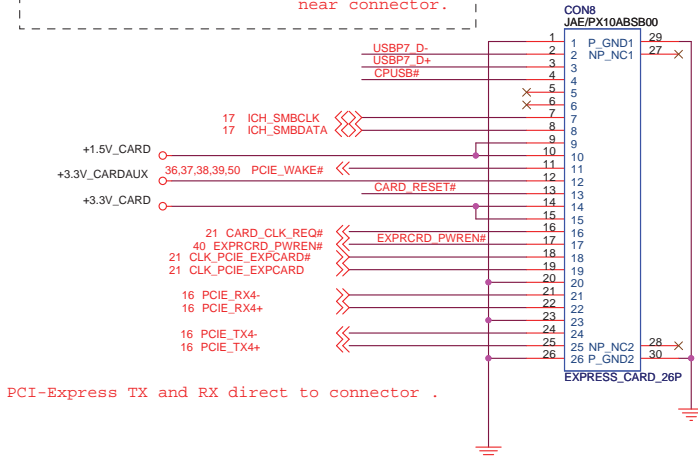
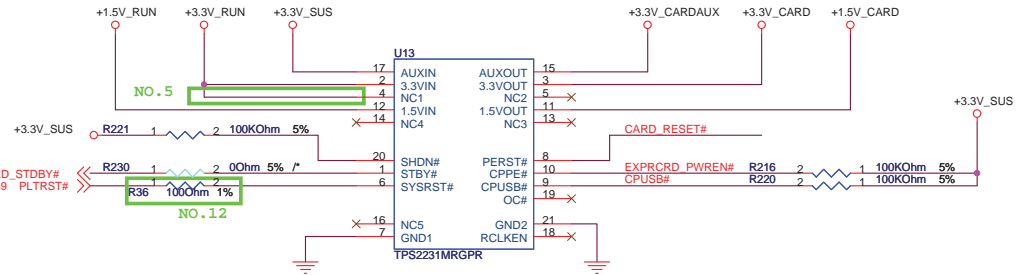
NO.89



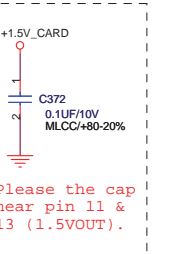
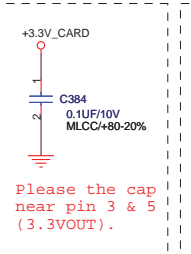
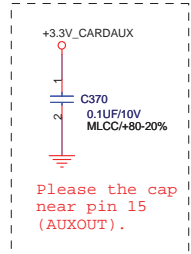
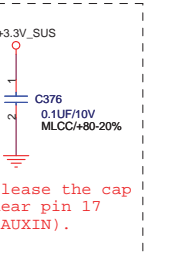
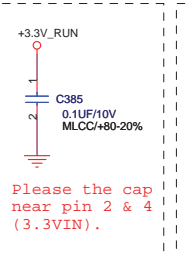
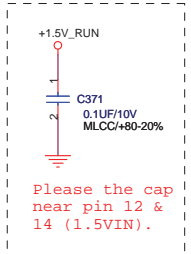
(20071005)for choke & 0ohm colayout



+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.



PCI-Express TX and RX direct to connector .

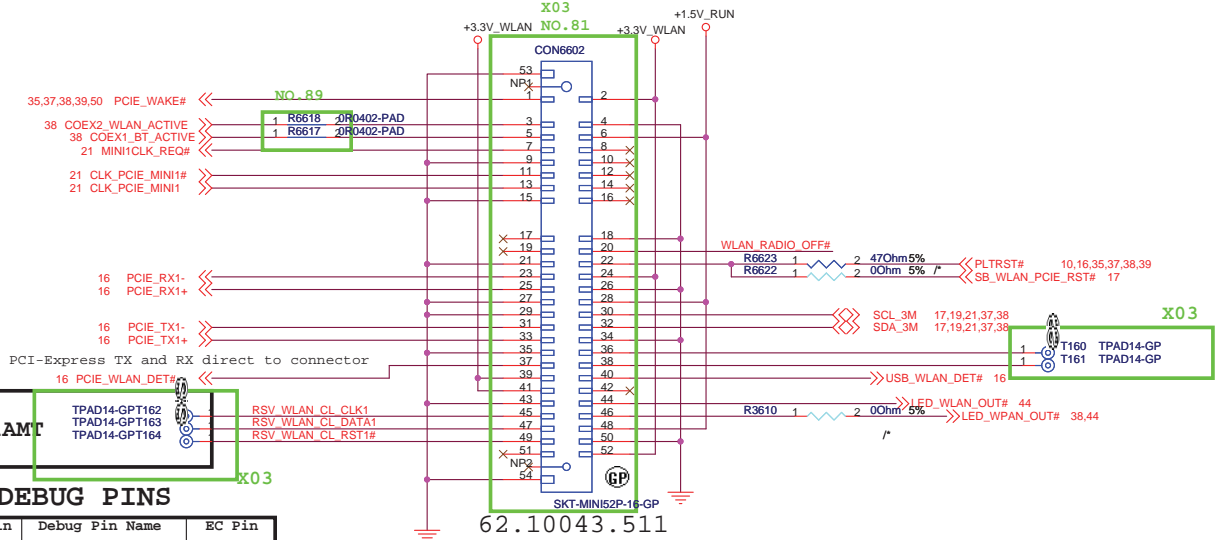


DZ1VQAT



Title		
Diaz-Discrete		
Size A3	Document Number PCI-Express Card	Rev A00
Date: Monday, August 25, 2008	Sheet 35 of 69	

MiniCard WLAN connector

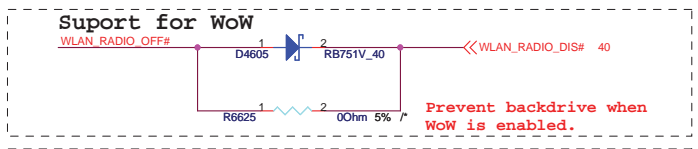
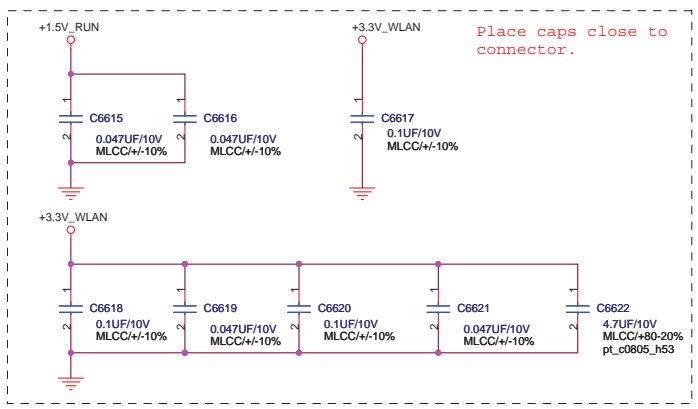


Non-iAMT

TPAD14-GPT162
TPAD14-GPT163
TPAD14-GPT164

DEBUG PINS

JMINI Pin	Debug Pin Name	EC Pin
16	HOST_DEBUG_TX	70
17	HOST_DEBUG_RX	71
19	8051_TX	82
42	8051_RX	81

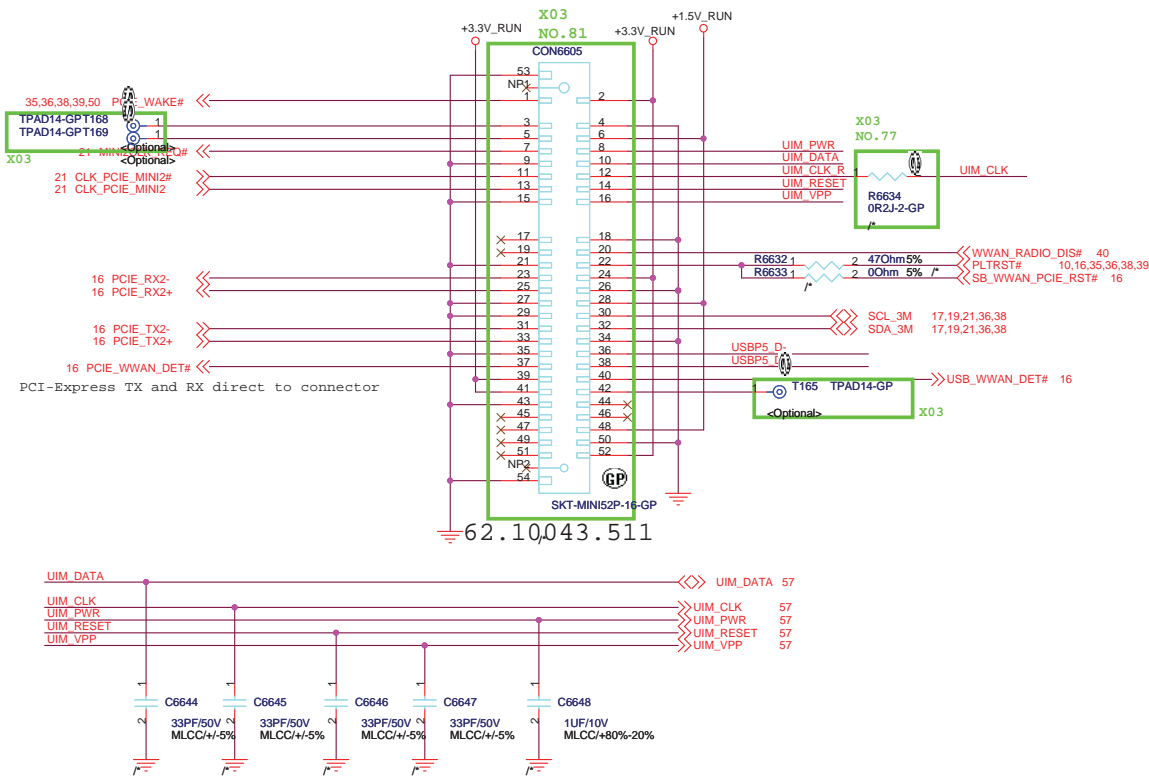


DZ1VQAT

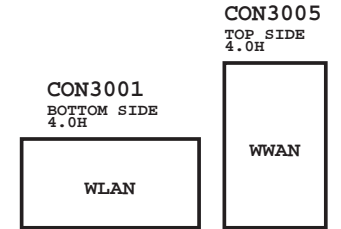
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title		
Diaz-Discrete		
Size	Document Number	Rev
A3	MINI CARD - Kedron	A00
Date: Monday, August 25, 2008	Sheet 36 of 69	

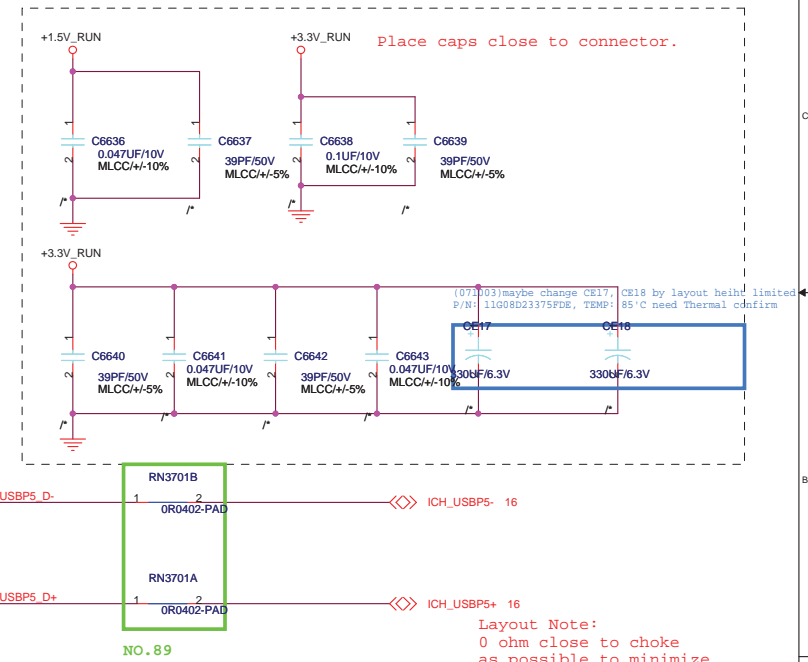
MiniCard WWAN connector



MiniCard Relative Location (TOP VIEW):



MiniCard * 2 Absolutely Location (TOP VIEW):
Upper / Right side on MB

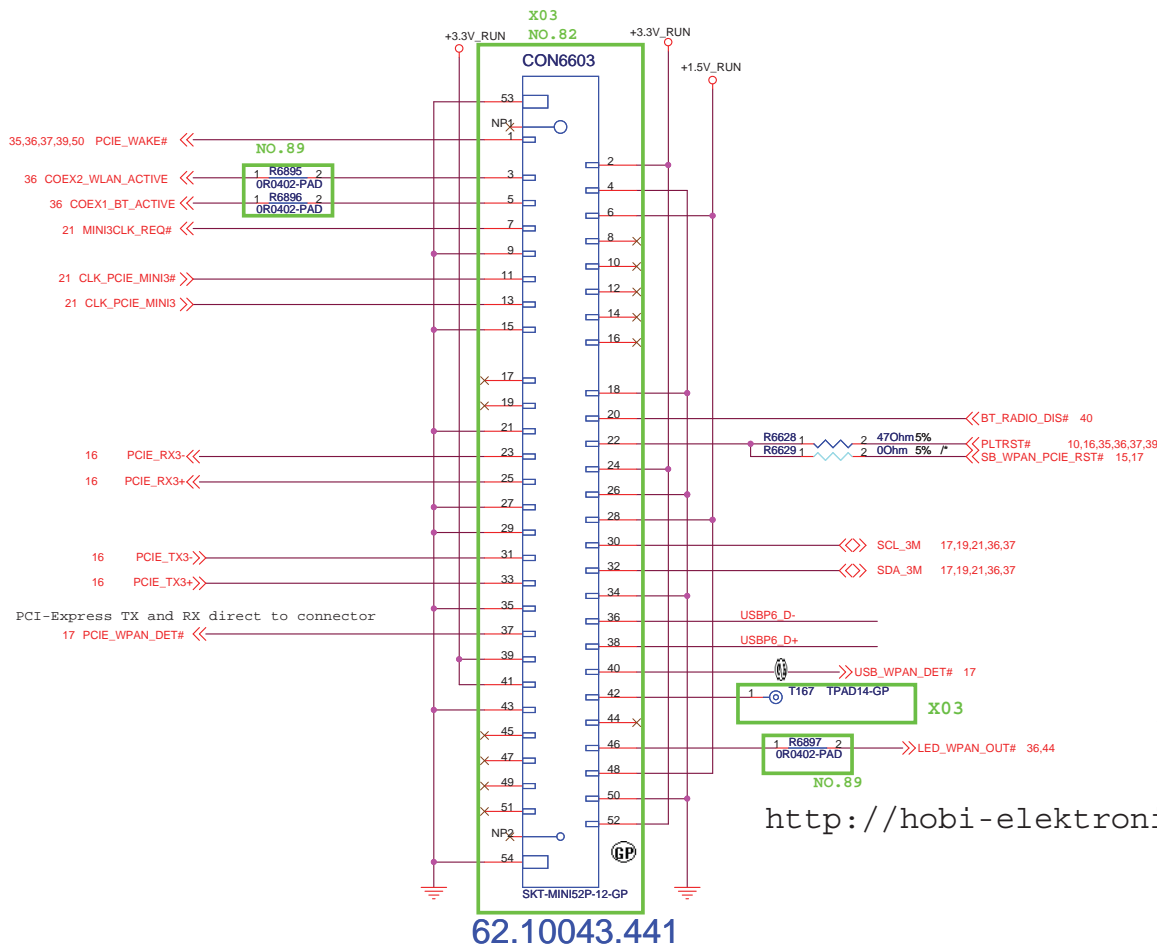


DZ1VQAT



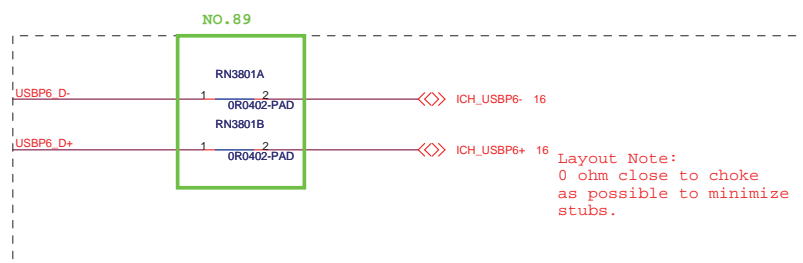
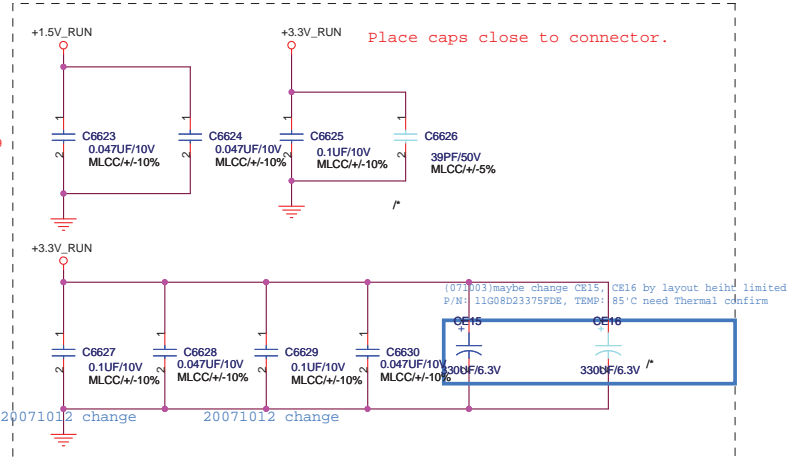
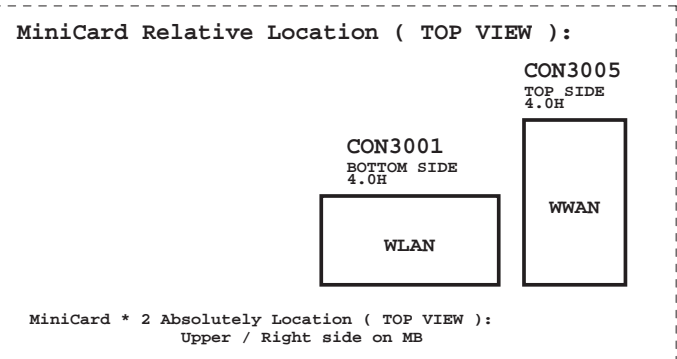
Title		
Diaz-Discrete		
Size A3	Document Number MINI CARD - Robson	Rev A00
Date: Monday, August 25, 2008	Sheet 37 of 69	

MiniCard WPAN connector



62.10043.441

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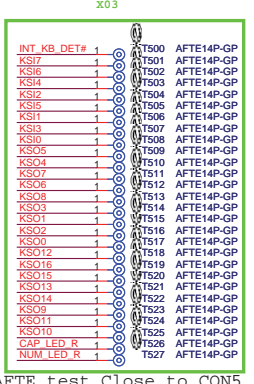
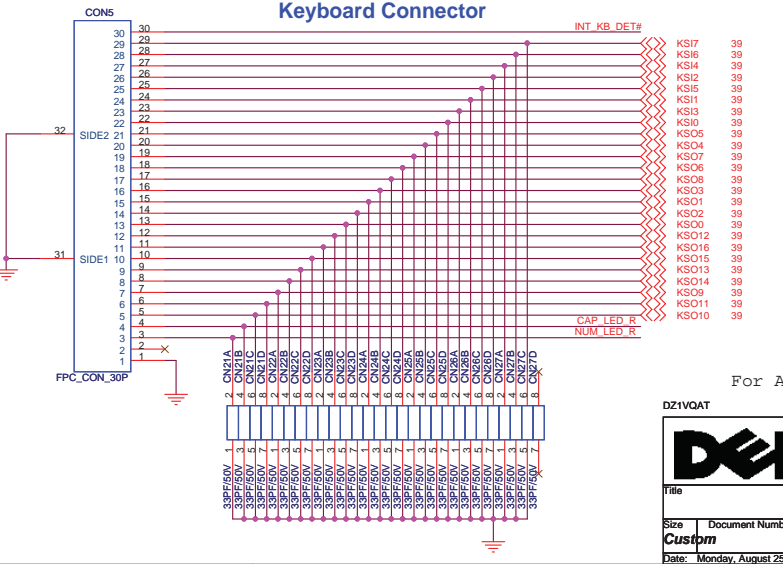
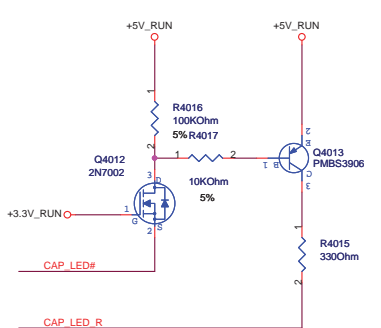
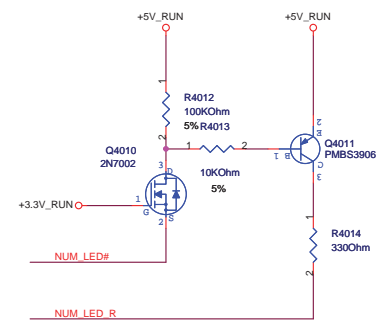
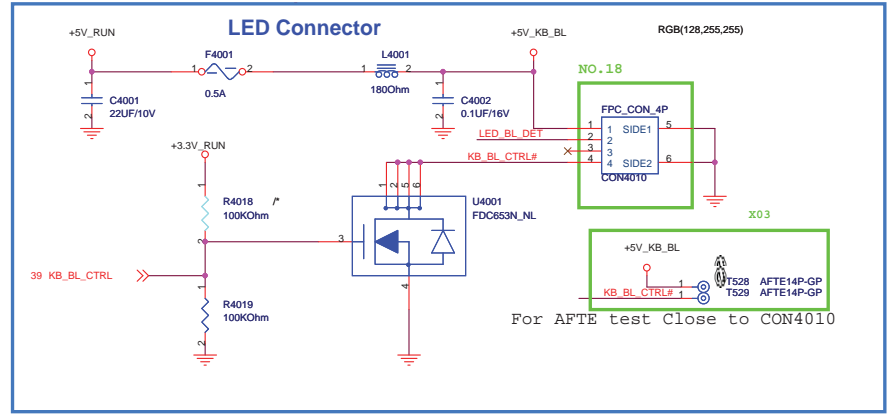
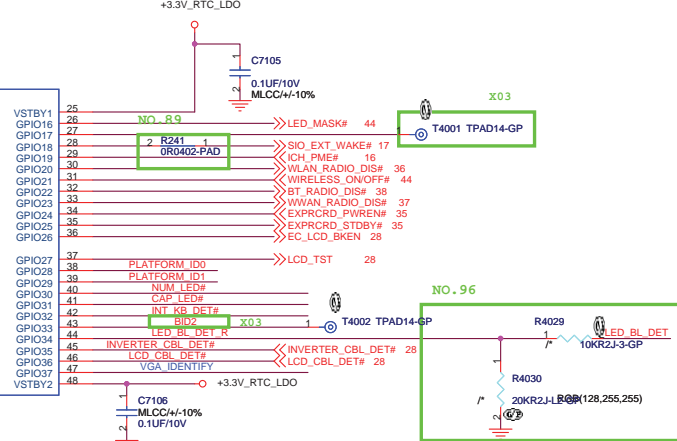
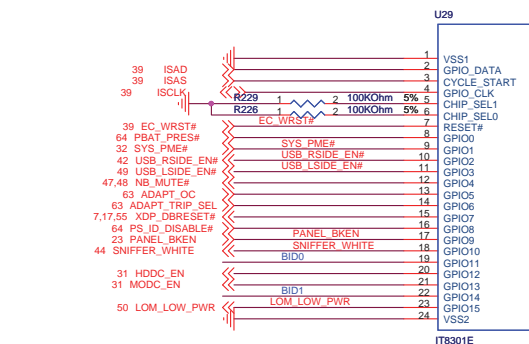
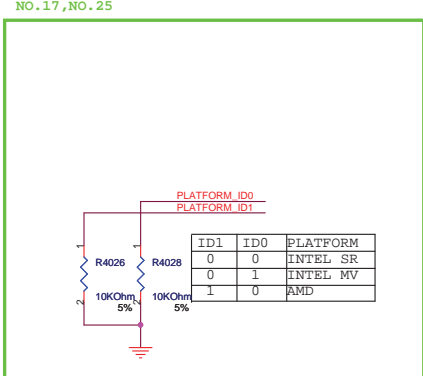
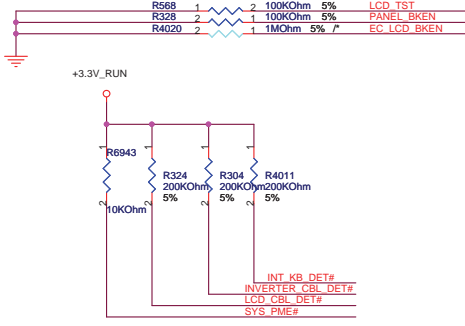
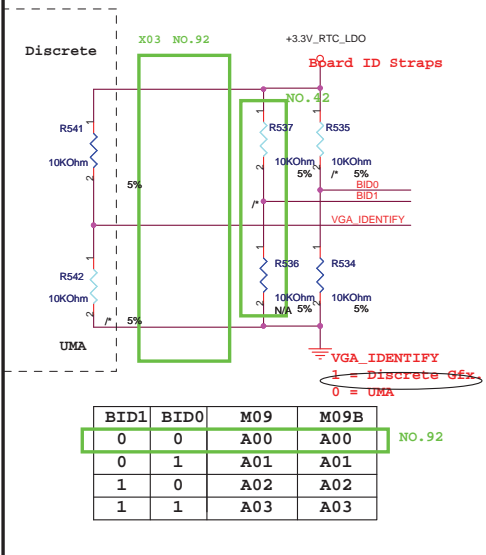
DZ1VQAT

Wistron Corporation
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Title: **Diaz-Discrete**

Size: **A3** Document Number: **MINI CARD - Robson** Rev: **A00**

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DZ1VQAT

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Taipei Hsien 221, Taiwan, R.O.C.

File: **Diaz-Discrete**

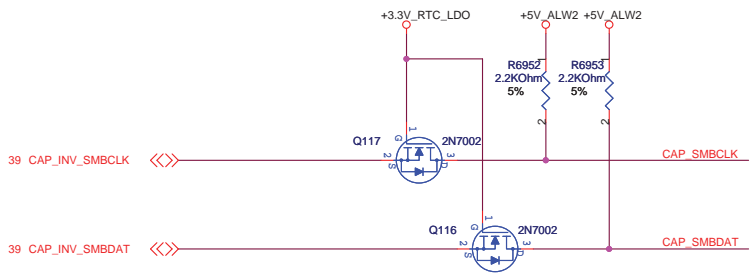
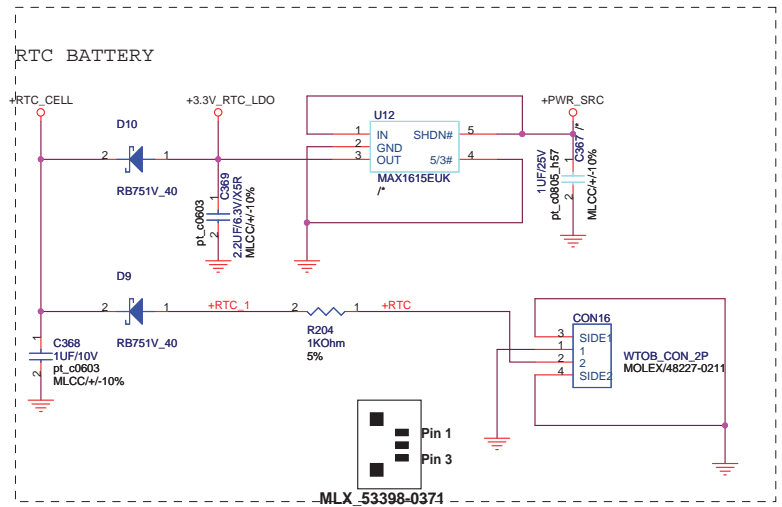
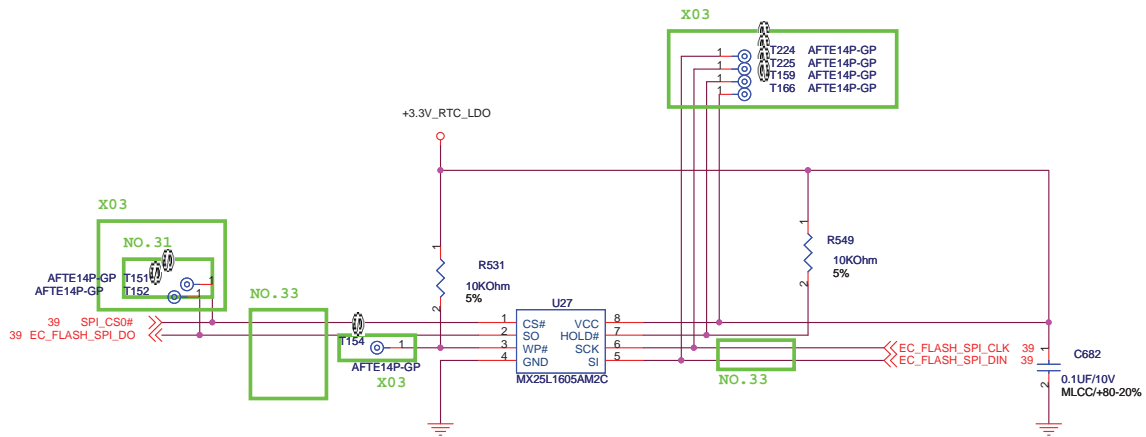
Size: Document Number

Customer: **IT8301E**

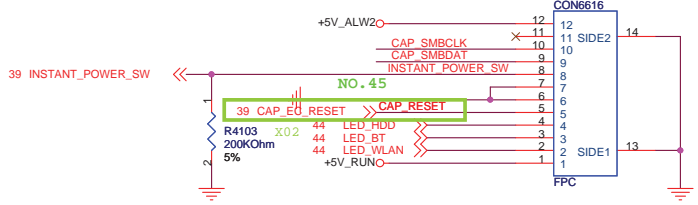
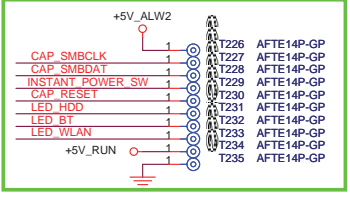
Date: Monday, August 25, 2008

Rev: **A00**

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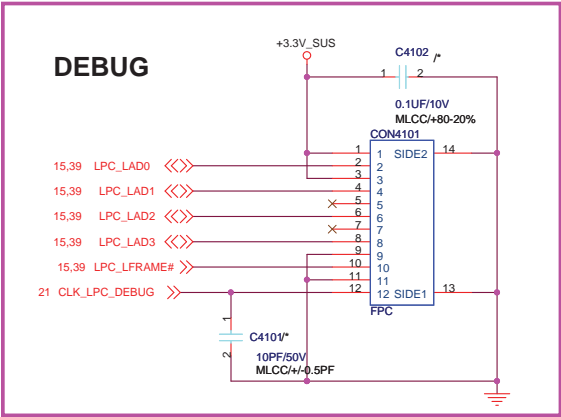


X03 For AFTE test Close to CON6616



CAPBTN CON.

Note:
+5V_ALW2 => for Capbutton PSOC and Media direct LED only.
+5V_RUN => for Capbutton LED and Photo sensor.



DZ1VQAT

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Diaz-Discrete

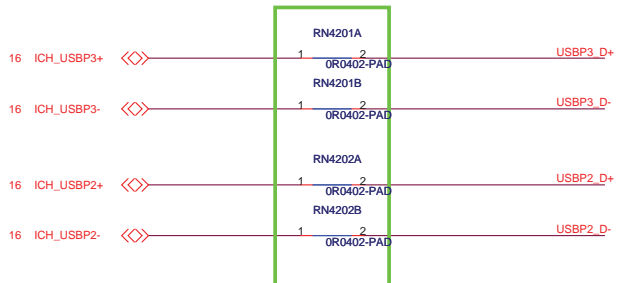
Size **A3** Document Number **FLASH & RTC** Rev **A00**

Date: Monday, August 25, 2008 Sheet 41 of 69

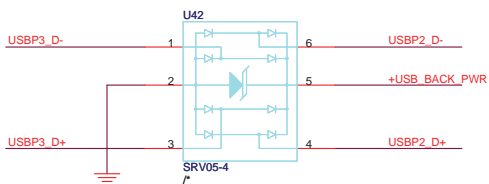
<http://hobi-elektronika.net/>

External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently .

NO. 89

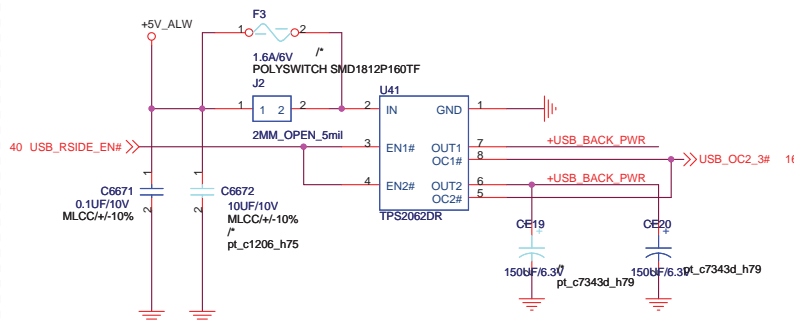


Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.



Place ESD diodes as close as USB connector. Semtech SRV05-4 can also be used but the Philips IP42220CZ6 have a lower input C (1pf vs 3pf).

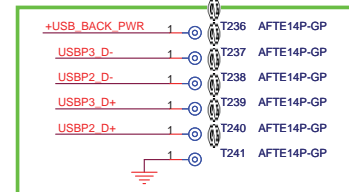
Place one 150uF cap by each USB connector



Each channel is 1A

Consult you ESD Engineer if you think you may need to add ESD Supression Components to your USB lines. Add PADS ONLY until proven diodes are really needed.

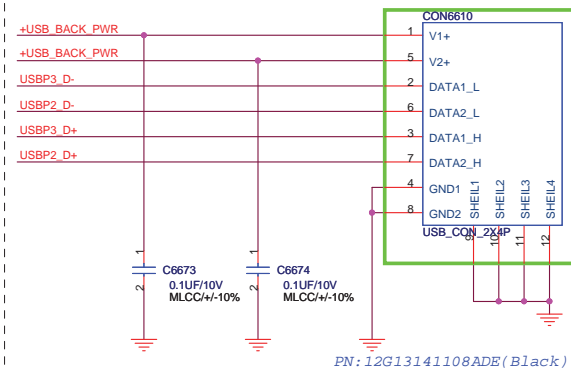
X03



For AFTE test Close to CON6610

Right side

NO. 41



PN: 12G13141108ADE(Black)

DZ1VQAT

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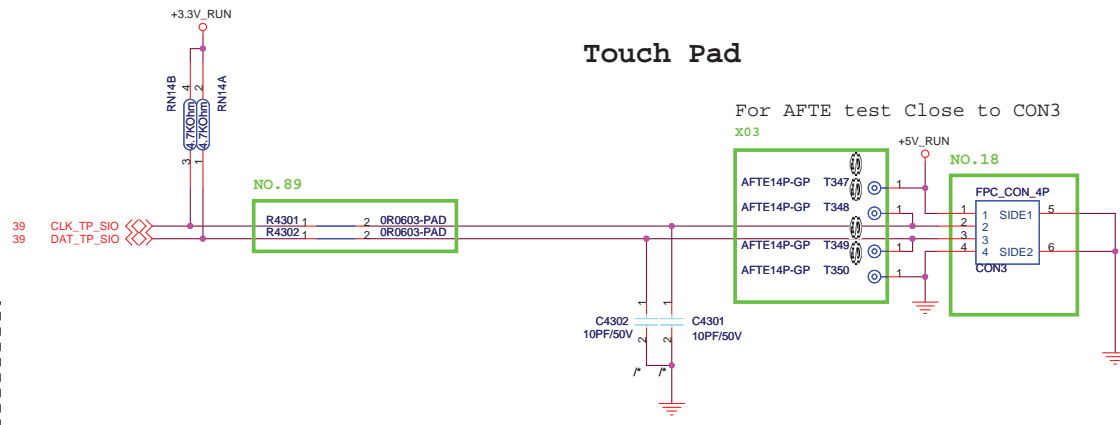
Title
Diaz-Discrete
Size **A3** Document Number
Date: Monday, August 25, 2008

USB PORT x 2

Rev **A00**

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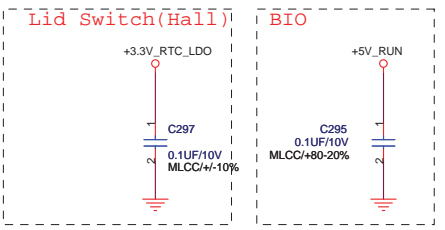
Touch Pad



For AFTE test Close to CON3

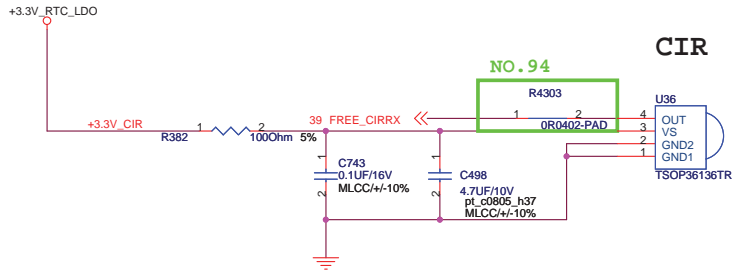
X03

NO.18



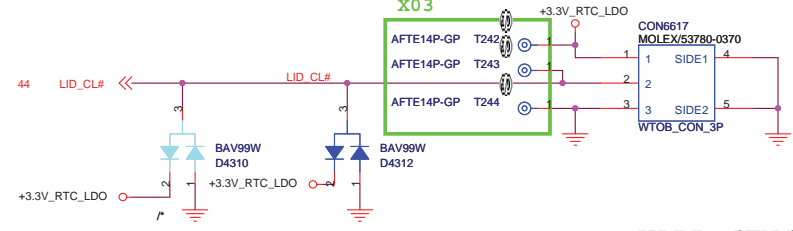
<http://hobi-elektronika.net/>

CIR



For AFTE test Close to CON6617

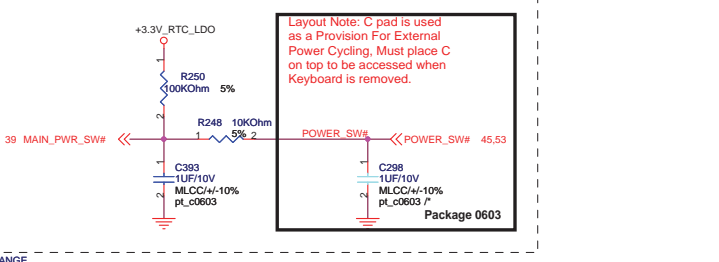
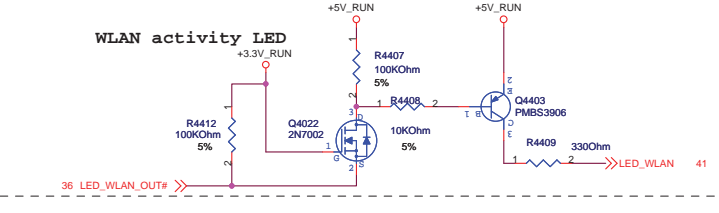
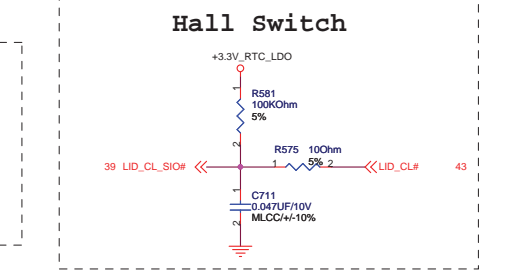
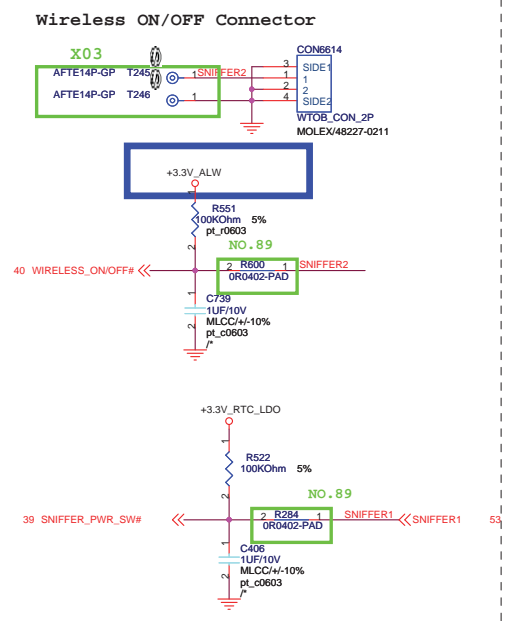
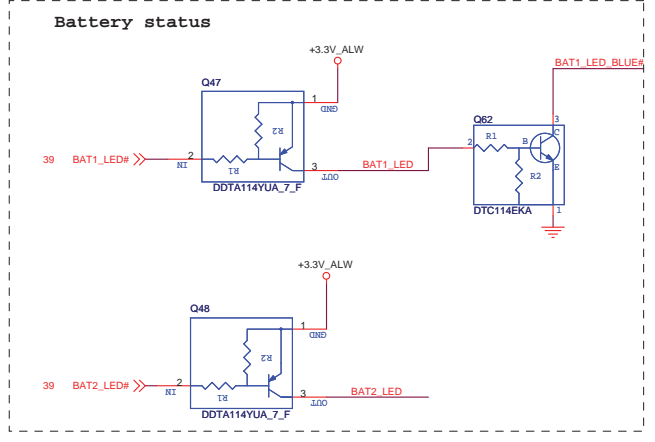
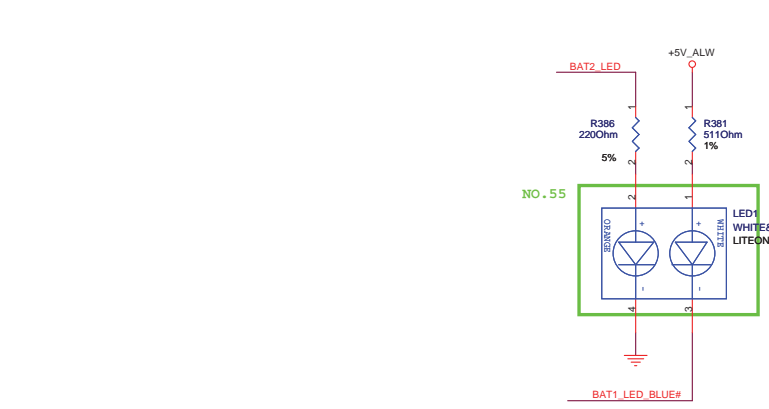
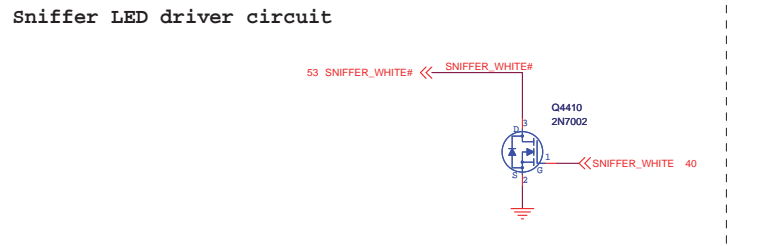
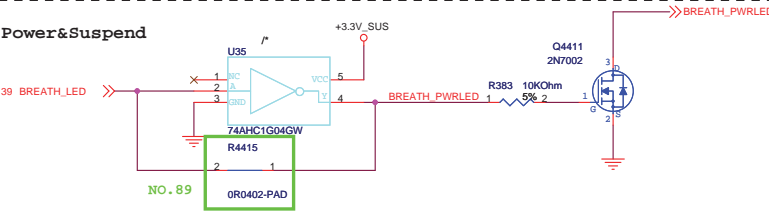
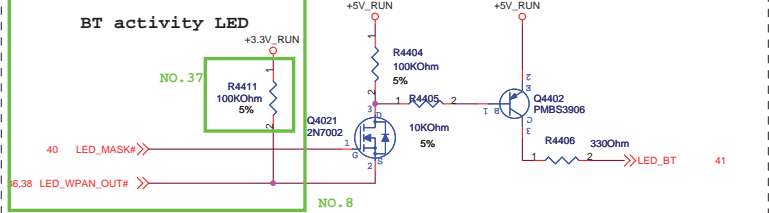
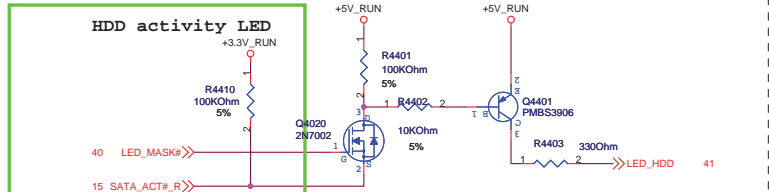
X03



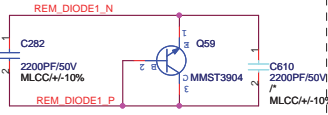
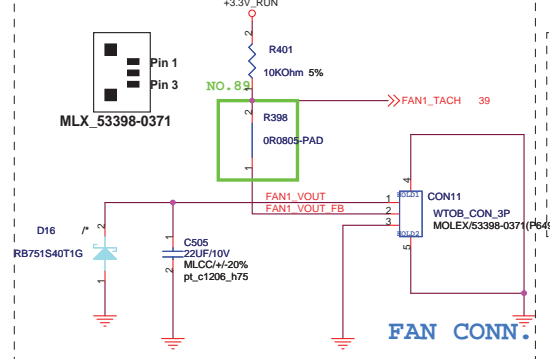
HALL SENSOR

DZ1VQAT

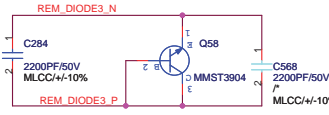
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Title Diaz-Discrete	
Size A3	Document Number TOUCH PAD & BT & CIR & LID	Rev A00	
Date: Monday, August 25, 2008	Sheet 43 of 69		



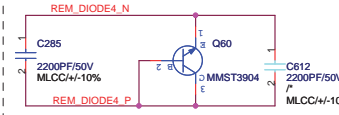
Layout Note: C pad is used as a Provision For External Power Cycling, Must place C on top to be accessed when Keyboard is removed.



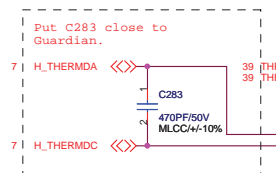
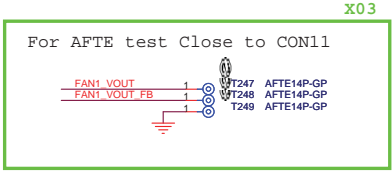
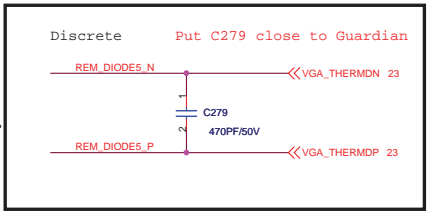
Put C282 close to Guardian.
Put C610 close Diode.
Place under CPU.



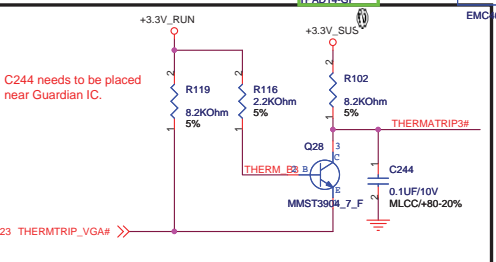
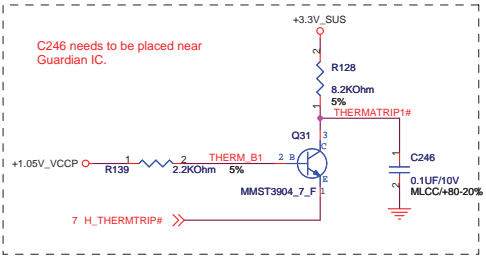
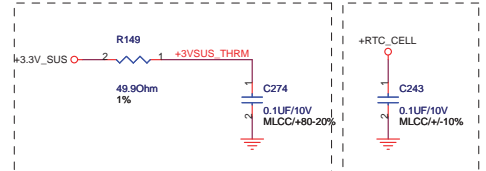
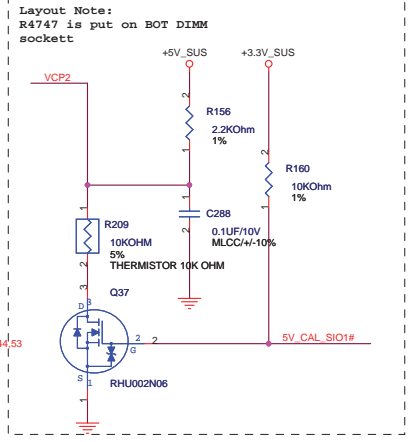
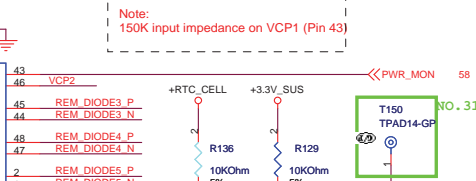
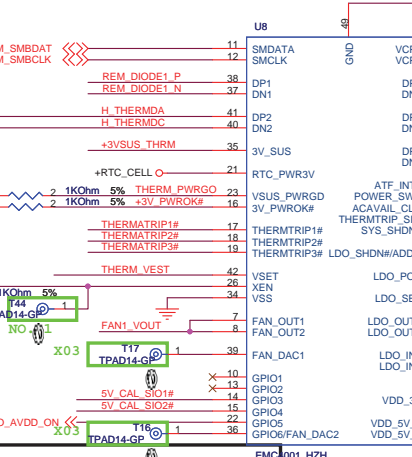
Put C284 close to Guardian.
Put C568 close Diode.
Place under DIMM.



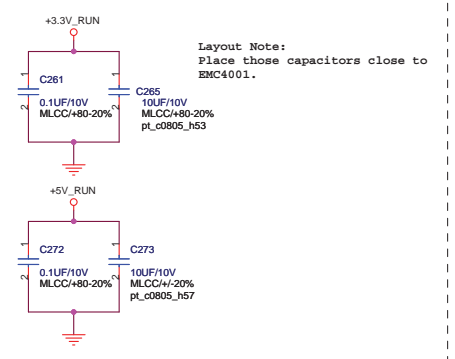
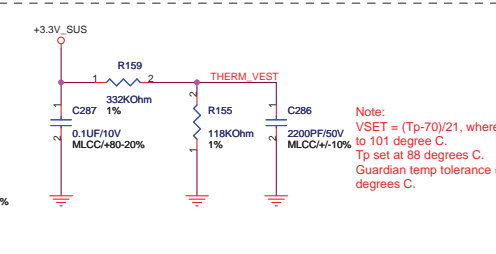
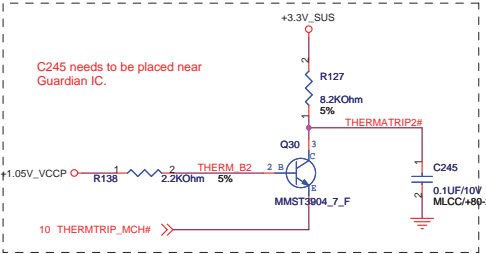
Put C285 close to Guardian.
Put C612 close Diode.
Place under Skin.



Guardian



<http://hobi-elektronika.net/>



DZ1VQAT

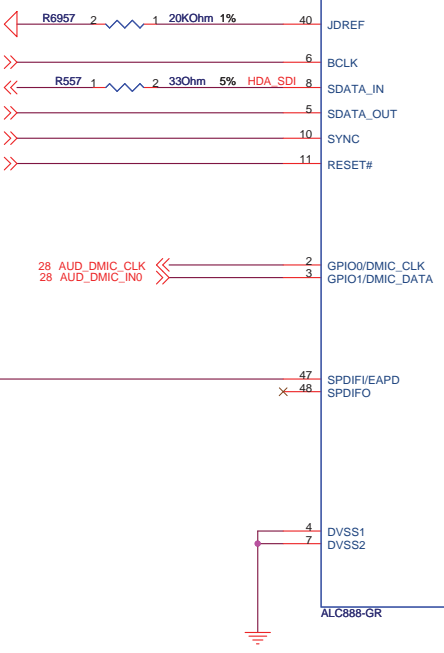
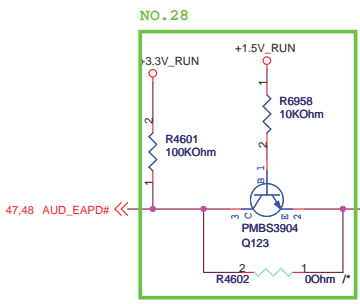
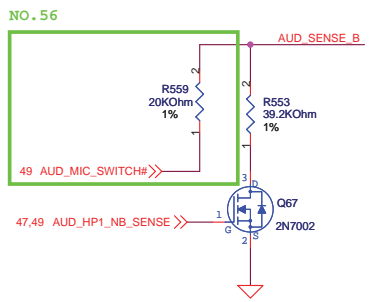
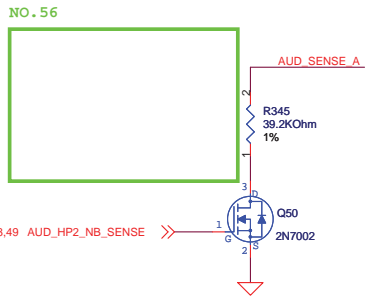
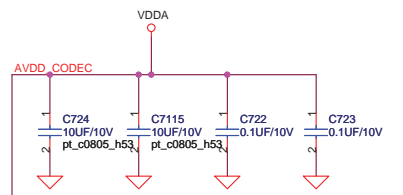
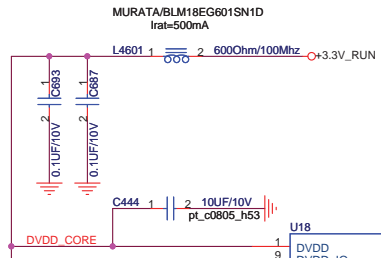
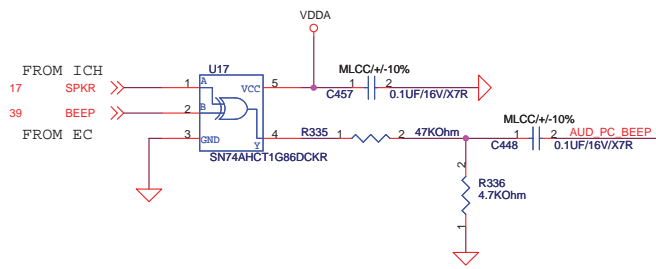
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Taipei Hsien 221, Taiwan, R.O.C.

Title **Diaz-Discrete**

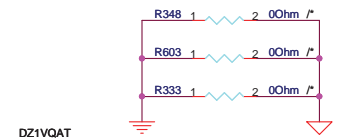
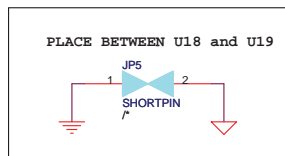
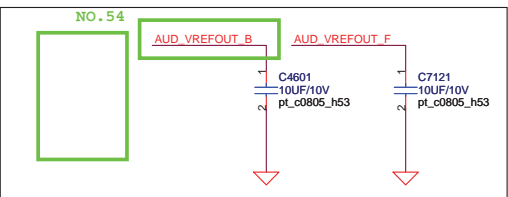
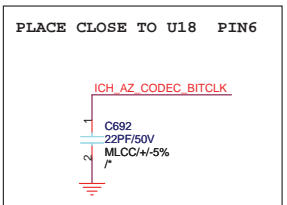
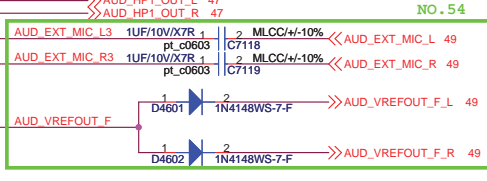
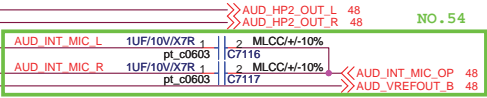
Size Document Number **EMC4001**

Customer **A00**

Date: Monday, August 25, 2008 Sheet 45 of 69



NO. 54
 Port A---> HP2
 Port E---> HP1
 Port F---> ext Mic
 Port B---> INT MIC
 Port D---> Speaker



DZ1VQAT

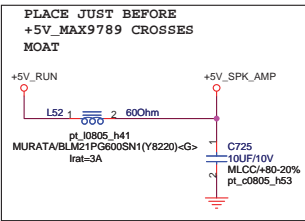
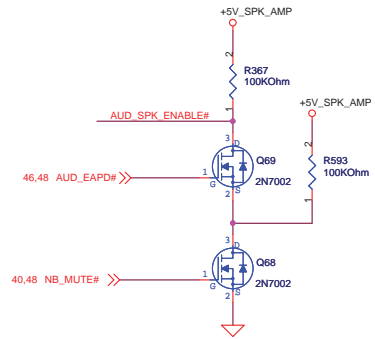
Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title _____

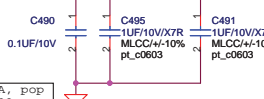
Size **A3** Document Number **ALC888** Rev **A00**

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Signal Inverter for Speaker Shutdown
 Allow speakers to work while class driver is installed

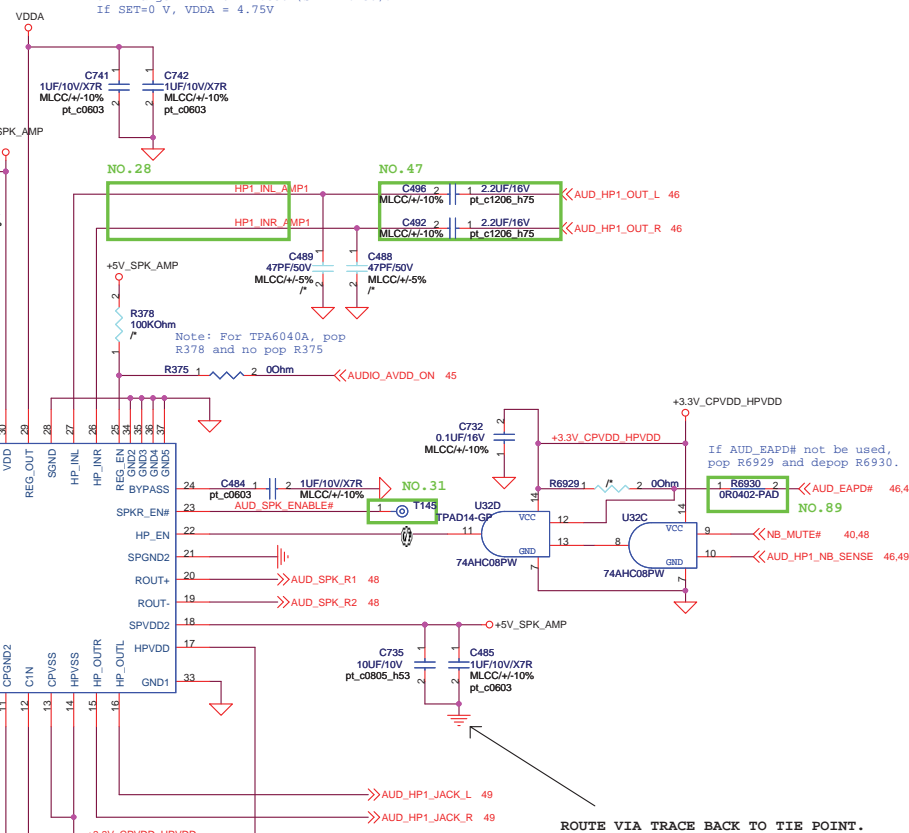


Place C490 close to Pin 30



NOTE: For TPA6040A, pop C487 and C486 (0402 XSR) and no pop R601 and R376. C487 and C486 value should match C494 and C493

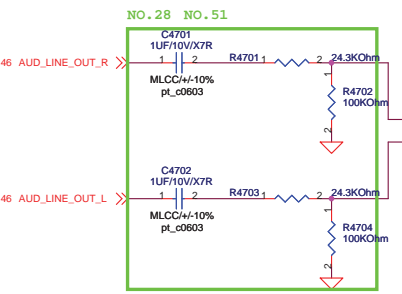
VDDA Range = 1.21V ~ 4.85V (SET=1.23V).
 If SET=0 V, VDDA = 4.75V



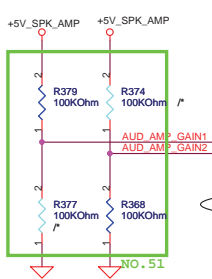
TEMPORARY VALUES. FINAL VALUES CHOSEN IN PT PHASE.

NOTE: For TPA6040A, pop C486 and no pop R376

If AUD_EAPD# not be used, pop R6929 and depop R6930.



GAIN SETTING RESISTORS



Gain1	Gain2	Gain
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB

ROUTE VIA TRACE BACK TO TIE POINT.

ROUTE VIA TRACE BACK TO TIE POINT.

ROUTE VIA TRACE BACK TO TIE POINT.

<http://hobi-elektronika.net/>

Location	TI TPA6040A	MAXIM MAX9789A
R376	DY	0 ohm
R601	DY	0 ohm
R378	DY	100K
R375	0 ohm	DY
C486	0.033uF	DY
C487	0.033uF	DY

DZ1VQAT

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Title: **Diaz-Discrete**

Size: Document Number
 Custom: **AMP TPA6040** Rev: **A00**

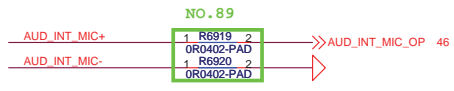
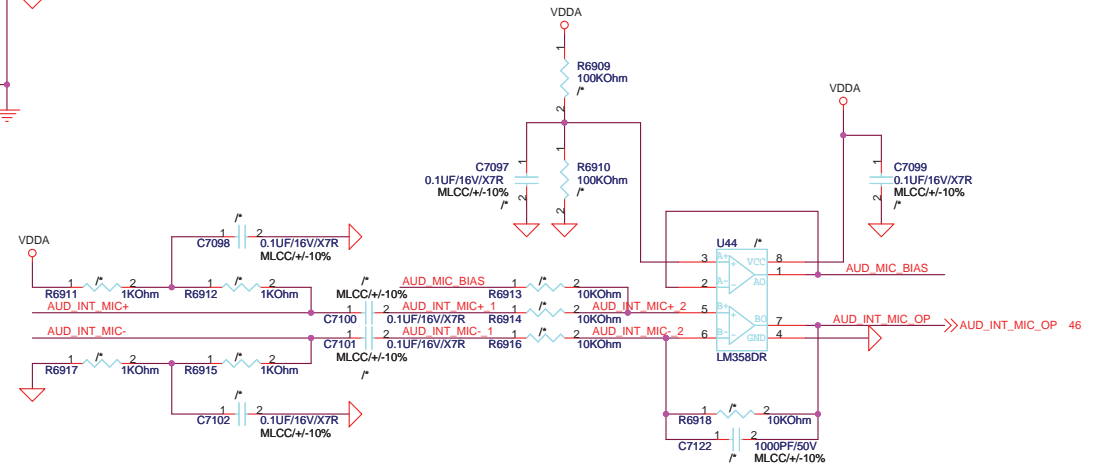
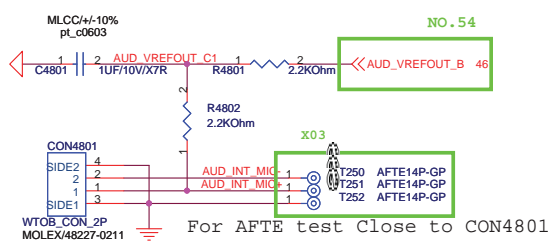
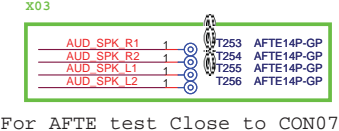
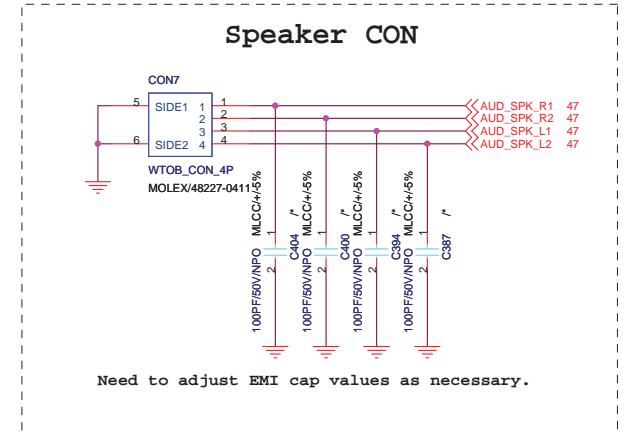
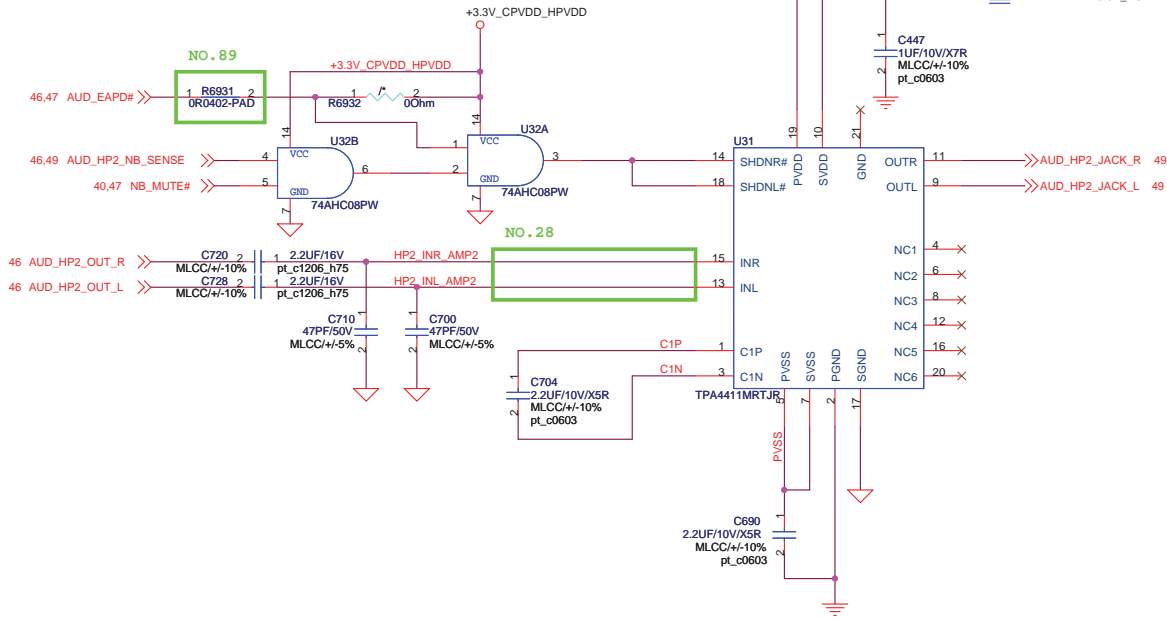
Date: Monday, August 25, 2008 Sheet 47 of 69

Maxim:1.8V ~ 3.6V
 TI:1.8V ~ 4.5V

NOTE: MAKE SURE THERMAL PAD
 (Pin21) UNDER MAX4411 IS NOT
 CONNECTED TO GND

If AUD_EAPD# not be used,
 pop R6932 and depop R6931.

MURATA/BLM18AG601SN1(J5535)<G>
 Irat=200mA



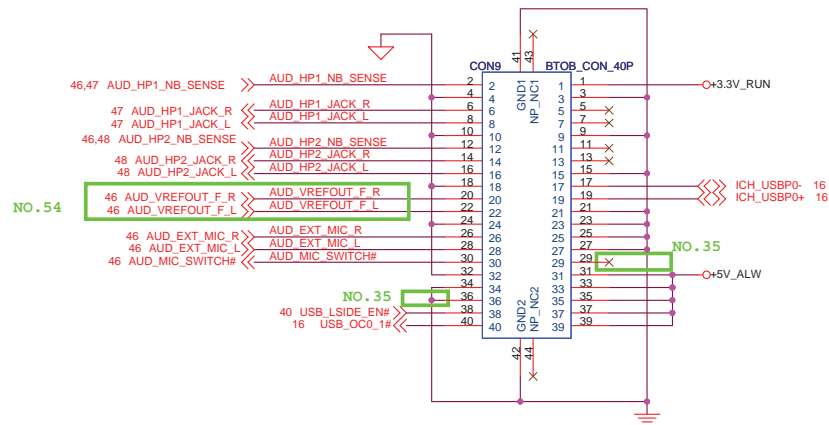
DZ1VQAT

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 Taipei Hsien 221, Taiwan, R.O.C.

Title: **Diaz-Discrete**

Size: **A3** Document Number: **AMP MAX4411 & MIC_AMP** Rev: **A00**

Date: Monday, August 25, 2008 Sheet 48 of 69



DZ1VQAT



Title

Diaz-Discrete

Size **A3** Document Number **AUDIO BtoB CON** Rev **A00**

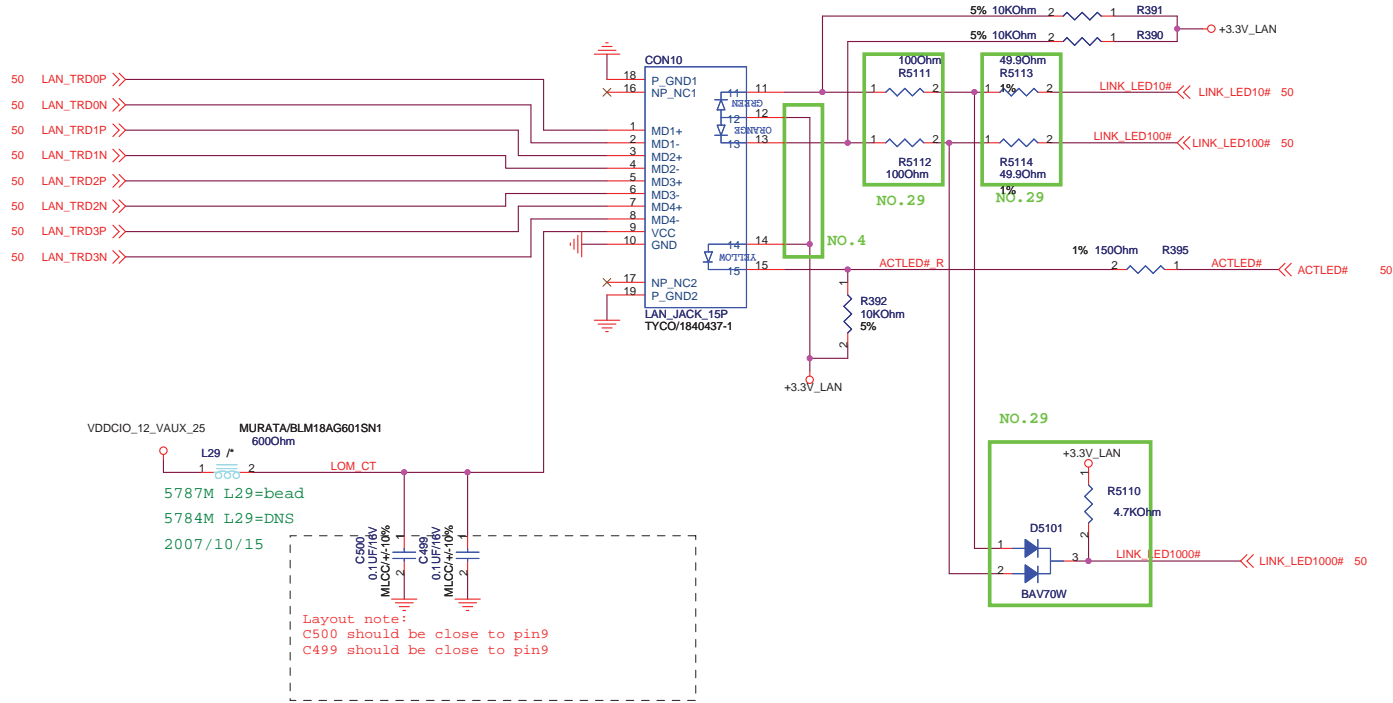
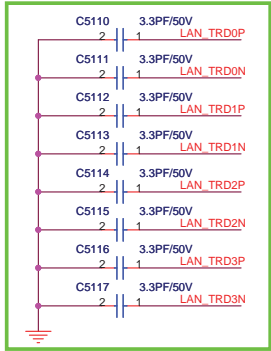
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This BOM is 5784M

require S3 support wake on LAN 2007/10/05

RJ45 should be 12G14801110KDE

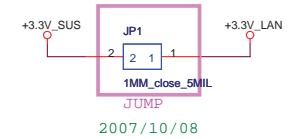
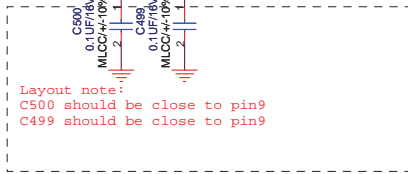
EMI solution place near con10 NO.29



+3.3V_LAN Source Guideline:

1. Use +3.3V_SUS if Wake-on-LAN is NOT required out of S4, S5
2. Use +3.3V_SRC if Wake-on_LAN is required out of S4, S5

VDDCIO_12_VAUX_25 MURATA/BLM18AG601SN1
600Ohm
L29 /
LOM CT
5787M L29=bead
5784M L29=DNS
2007/10/15

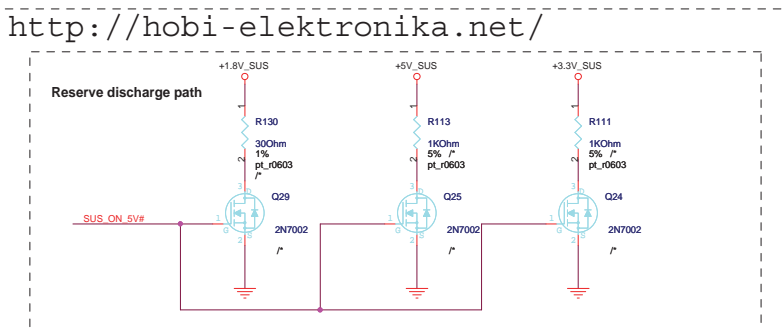
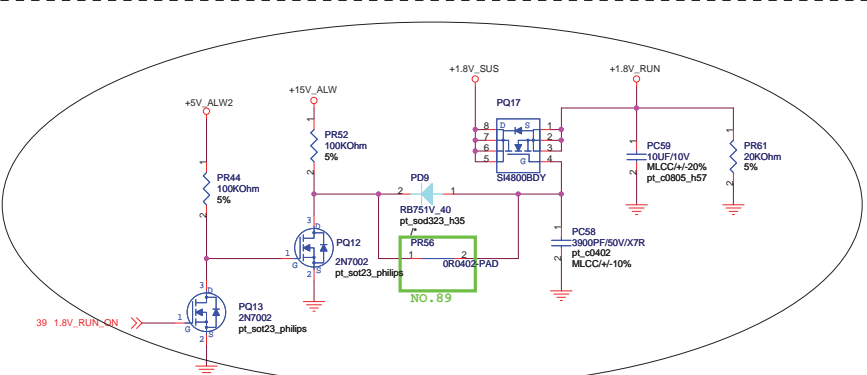
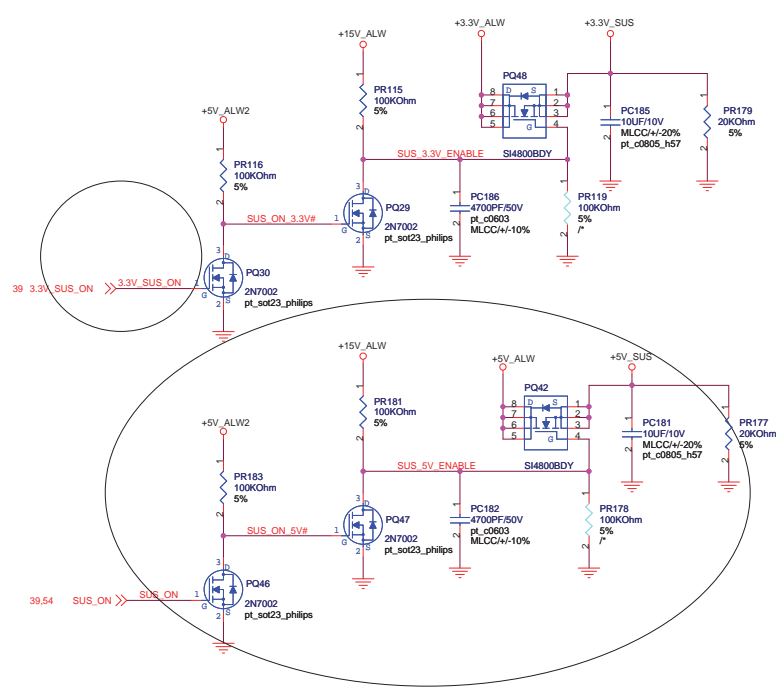
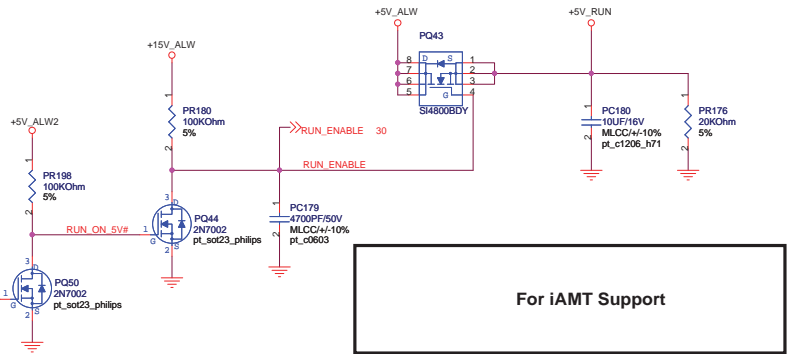


DZ1VQAT

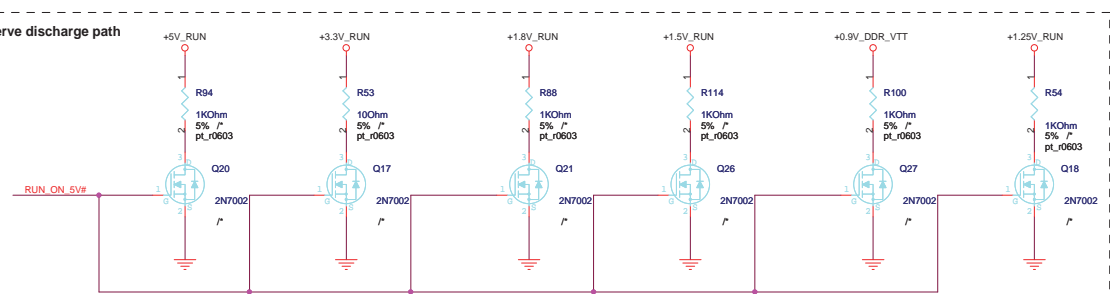
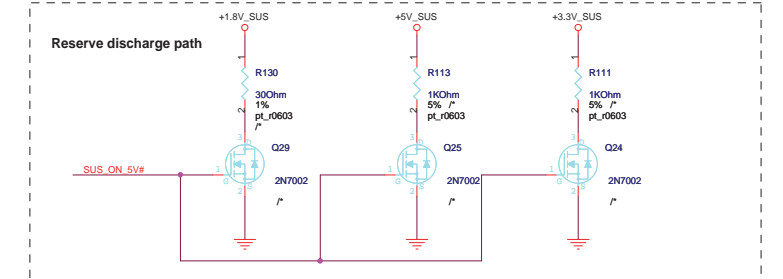
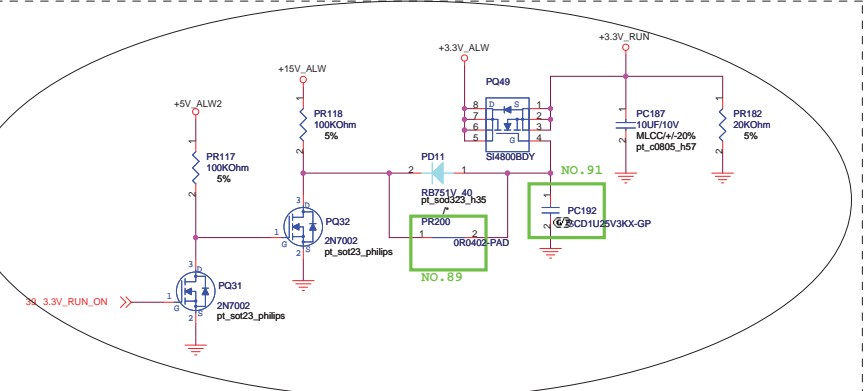
DELL Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title
Diaz-Discrete
Size A3 Document Number
Magnetics and RJ-45 Rev
A00

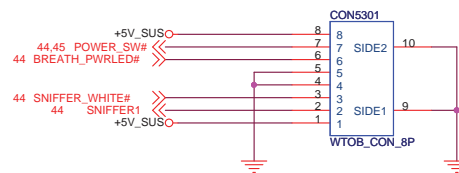
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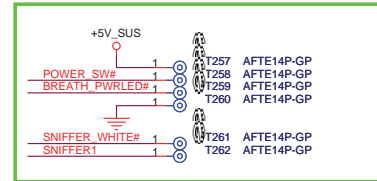
<http://hobi-elektronika.net/>



For iAMT Support



X03 For AFTE test Close to CON5301



DZ1VQAT

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Title

Diaz-Discrete

Size

A3

Document Number

Power Button Board

Rev

A00

Date: Monday, August 25, 2008

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Discrete

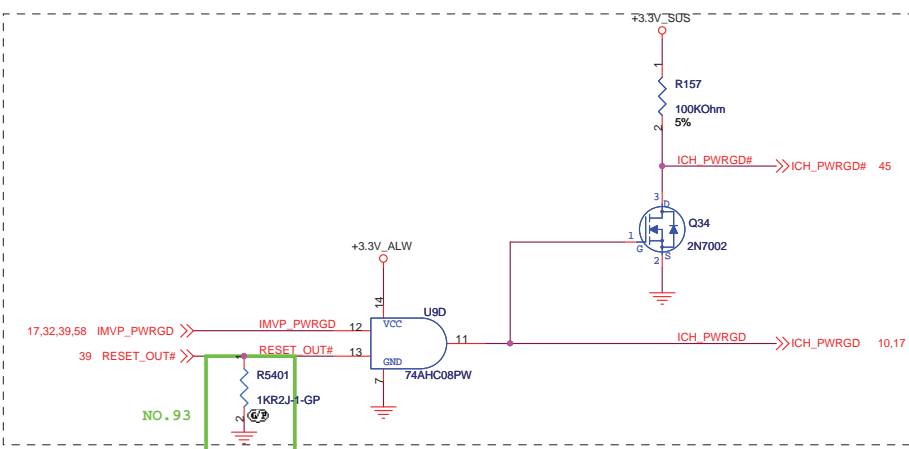
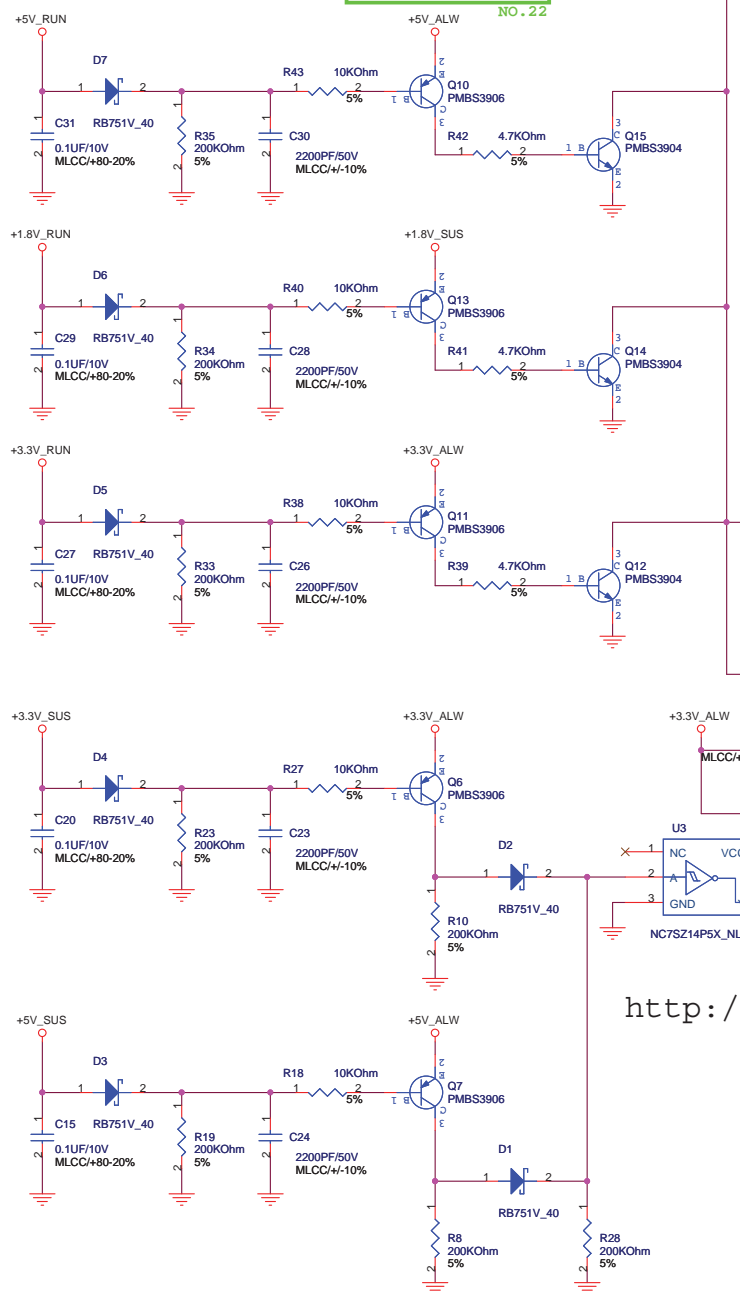
62 1.1V_RUN_PWRGD
62 GFX_CORE_PWRGD

NO. 89

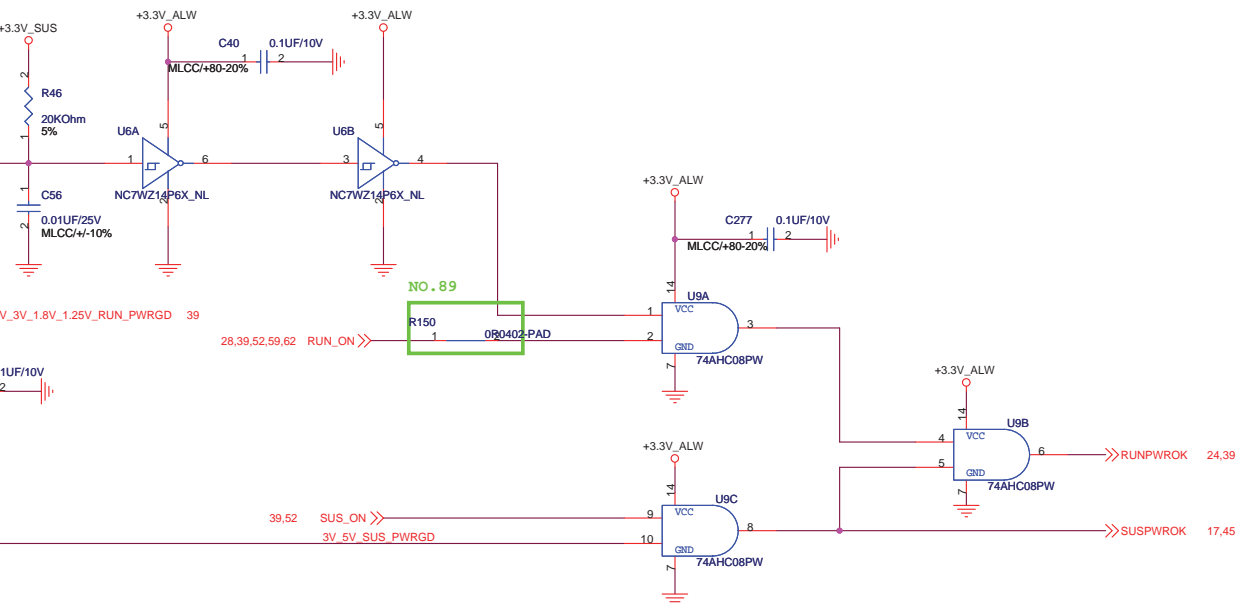
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60 1.05V_RUN_PWRGD

NO. 22

R52 0R0402-PAD
R427 0R0402-PAD
R504 0R0402-PAD
R519 0R0402-PAD



Keep Away from high speed buses
RGB(0,128,255)



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DZ1VQAT

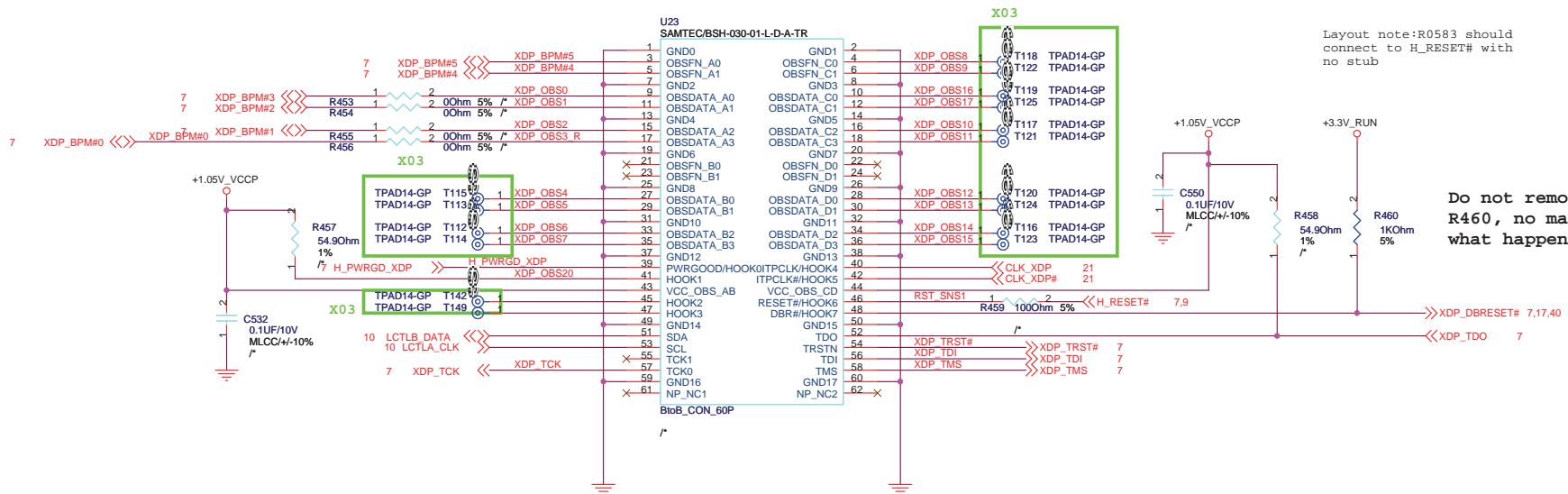
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Title: **Diaz-Discrete**

Size: **A3** Document Number: **Power Sequence Logic** Rev: **A00**

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XDP



Layout note:R0583 should connect to H_RESET# with no stub

Do not remove R460, no matter what happen.

CAD NOTE:
Place the XDP connector on the primary side of the CRB and place all components near the connector.

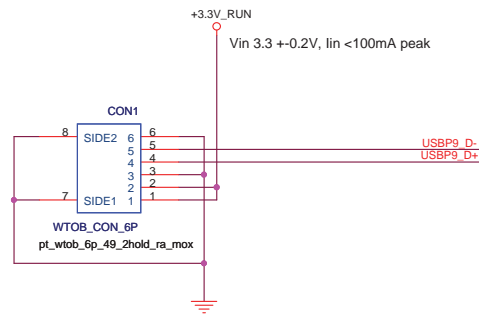
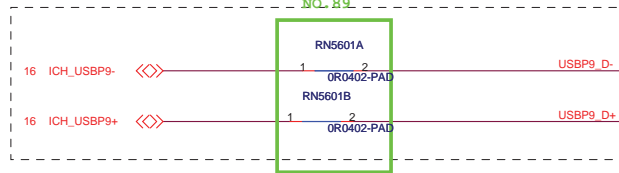
DZ1VQAT



Title		
Diaz-Discrete		
Size A3	Document Number XDP	Rev A00
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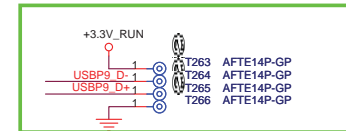
FINGER PRINTER

NO. 89



Vin 3.3 +0.2V, Iin <100mA peak

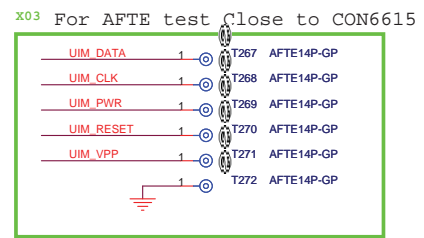
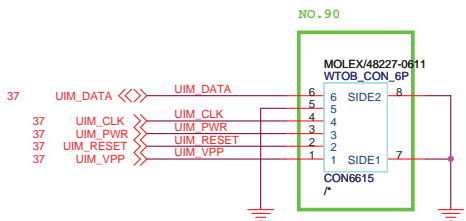
X03 For AFTE test Close to CON1



DZ1VQAT



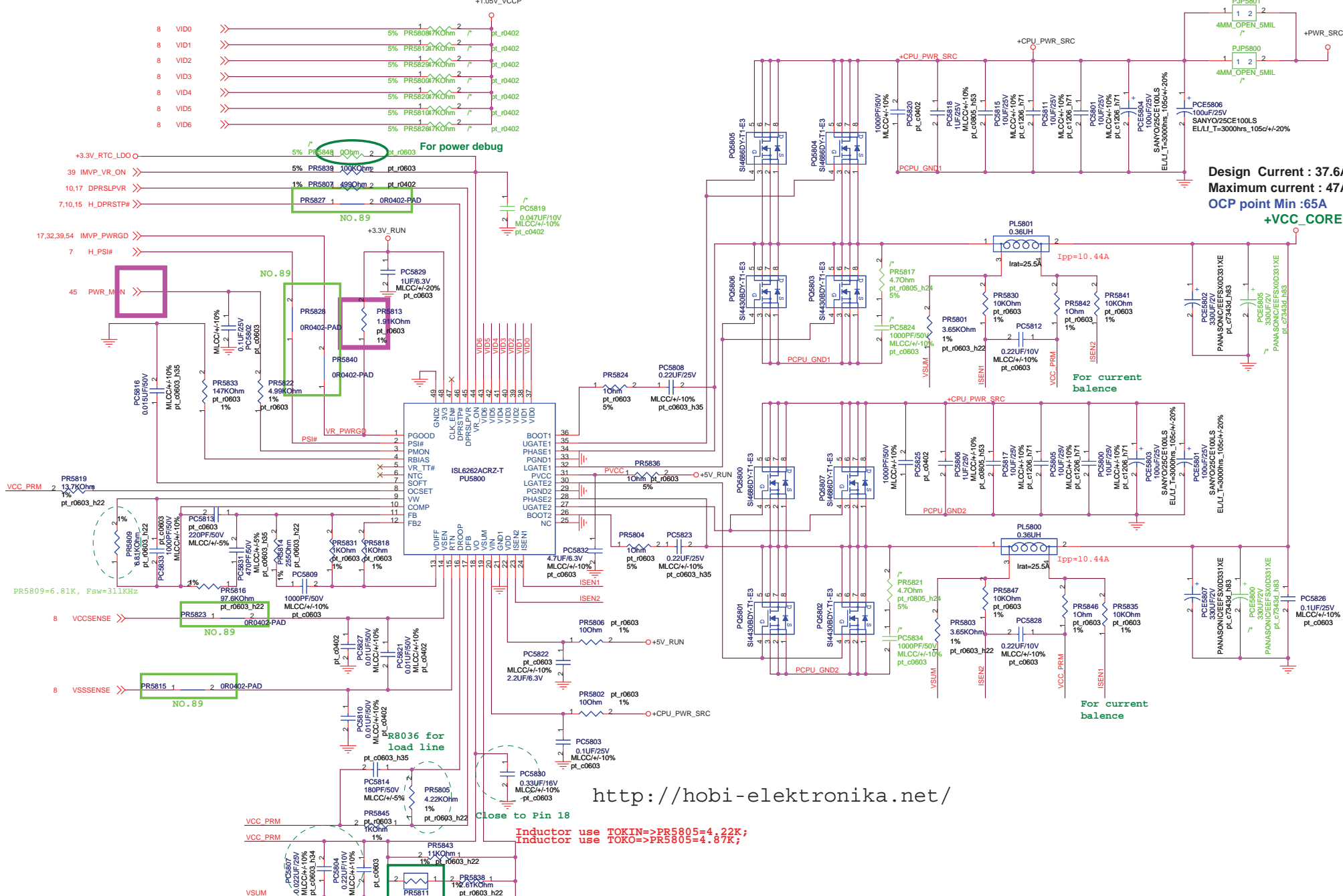
Title		
Diaz-Discrete		
Size	Document Number	Rev
A3	USB PORT (SINGLE * 2)	A00
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DZ1VQAT

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Title			
Diaz-Discrete			
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A3		SIM CARD	A00
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+1.05V_VCCP



Design Current : 37.6A
Maximum current : 47A
OCp point Min :65A
+VCC_CORE

For current balance

For current balance

R8036 for load line

**Inductor use TOKIN=>PR5805=4.22K;
 Inductor use TOKO=>PR5805=4.87K;**

Close to Pin 1 Inductor

C8021 & C8018 for transient response

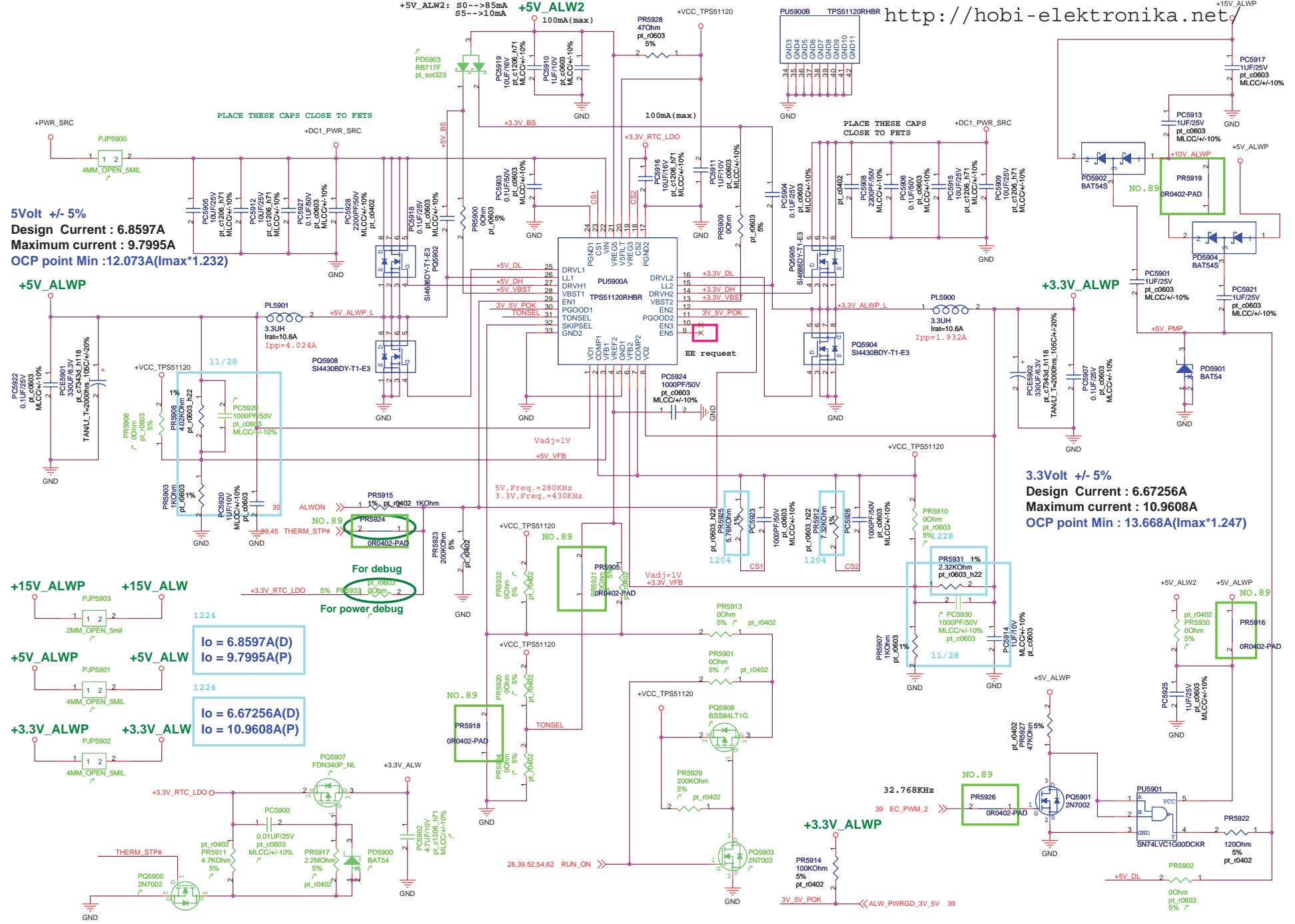
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File	Size	Document Number	Rev
	Custom	POWER_VCORE	A00

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5Volt +/- 5%
Design Current : 6.8597A
Maximum current : 9.7995A
OCP point Min :12.073A(I_{max}*1.232)

3.3Volt +/- 5%
Design Current : 6.67256A
Maximum current : 10.9608A
OCP point Min : 13.668A(I_{max}*1.247)

1224
Io = 6.8597A(D)
Io = 9.7995A(P)

1224
Io = 6.67256A(D)
Io = 10.9608A(P)

For debug
 For power debug

DZ1VQAT

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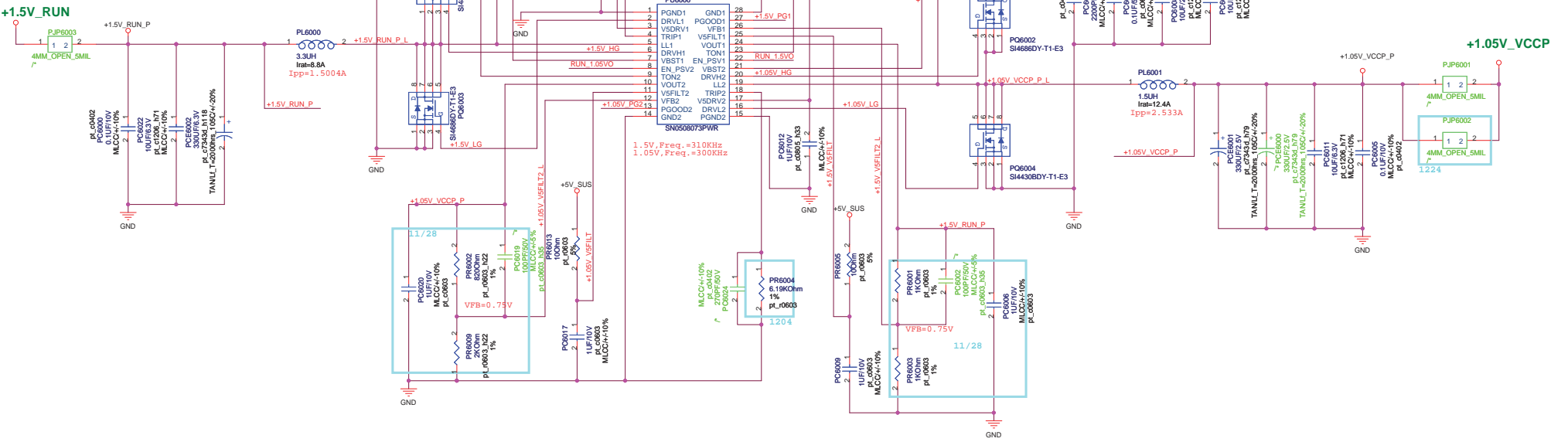
Title: **Diaz-Discrete**

Size: Document Number: **Customer POWER_SYSTEM 5V ALW&3.3V ALWA00** Rev: **1**

Date: Monday, August 25, 2008 Sheet: 59 of 69

1.5Volt +/- 5%
Design Current : 2.968A
Maximum current : 4.240A
OCp point Min :5.308A(I_{max}*1.252)

1.05Volt +/- 5%
Design Current : 6.9307A
Maximum current : 9.901A
OCp point Min : 12.277A(I_{max}*1.24)

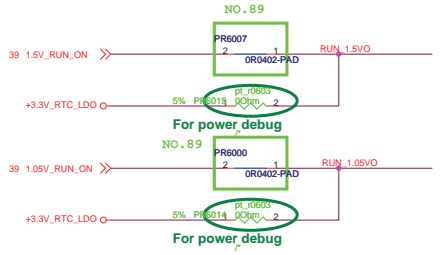


+1.5V_RUN

+1.05V_VCCP

<http://hobi-elektronika.net/>

54 1.5V_RUN_PWRGD << +1.5V_PG1
 54 1.05V_RUN_PWRGD << +1.05V_PG2



D21VQAT

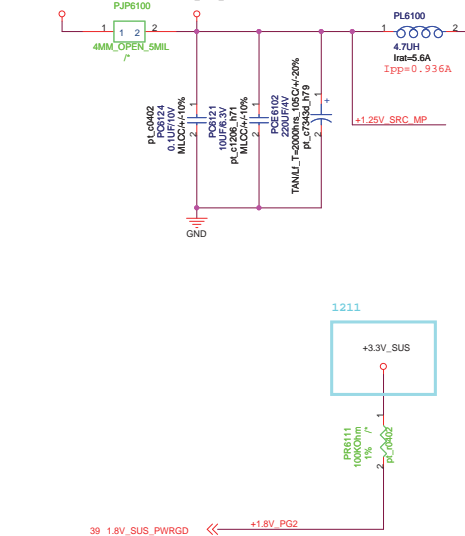
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Diaz-Discrete

Size	Document Number	Rev
C	POWER I/O 1.5VS & 1.05VS	A00
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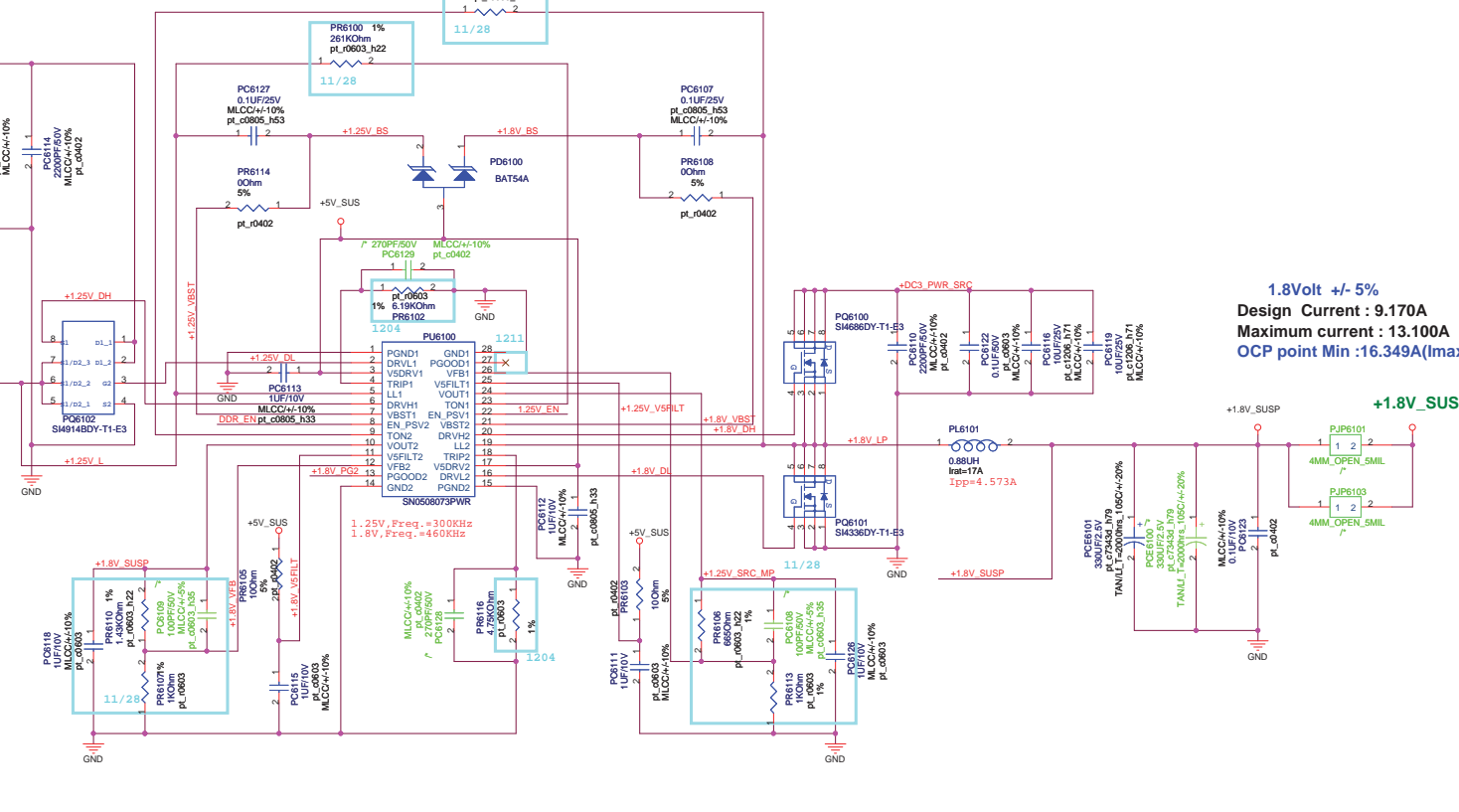
1.25Volt +/- 5%
Design Current : 1.729A
Maximum current : 2.470A
OCP point Min : 3.063A(I_{max}*1.24)

+1.25V_RUN



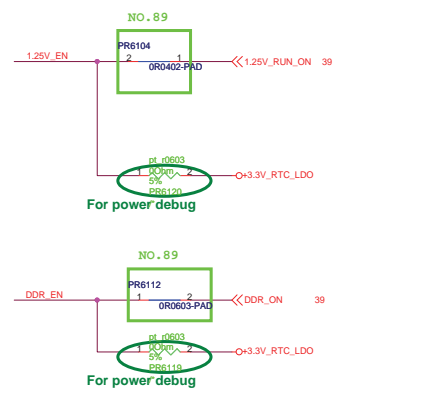
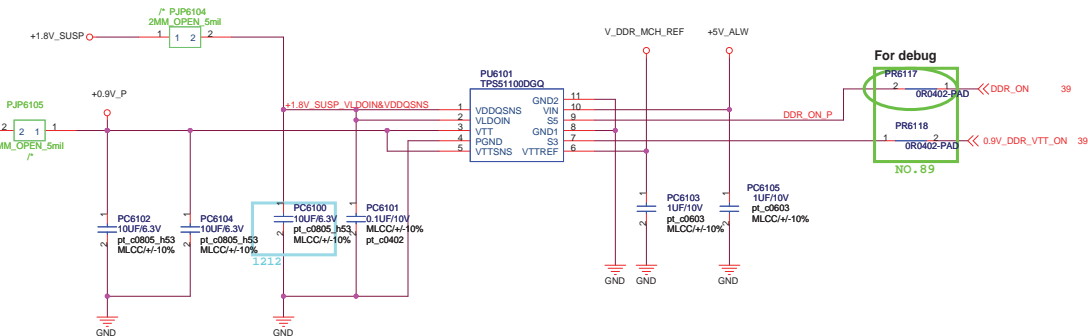
1.8Volt +/- 5%
Design Current : 9.170A
Maximum current : 13.100A
OCP point Min :16.349A(I_{max}*1.248)

+1.8V_SUS



0.9Volt +/- 5%
Design Current : 1.05A
Maximum current : 1.5A
OCP point Min : 3.8A

+0.9V_DDR_VTT



1.1Volt +/- 5%
Design Current : 1.232A
Maximum current : 1.760A
OCP point Min : 2.306A(max*1.31)

Design specs. in default:
Design Current : 6.664A
Maximum current : 9.520A
OCP point Min : 11.852A(max*1.245)

PWRCNTL_0	PWRCNTL_1	+VCC_GFX_CORE
L	L	1.2V
H	L	1.1V
H	H	1.0V
H	H	0.93V

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For power debug

For power debug

TOTAL POWER=65W
-->3.33A (Vin=19.5V)

TABLE3 PIN NAME DIFFERENCES		
PIN	MAXIM	INTERSIL
1	GNL	NC
3	REF	VREF
4	CCS	ICOMP
5	CCI	NC
6	CCV	VCOMP
7	DAC	NC
8	IINP	ICM
11	VDD	VDDSMB
14	BATSEL	NC
15	FBSA	VFB
16	FBSB	NC
17	CSIN	CSON
18	CSIP	CSOP
20	DLO	LGATE
21	LDO	VDDP
23	LX	PHASE
24	DHI	UGATE
25	BST	BOOT

NC means no-connect

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Charge Current : 4.68A
Discharge current : 6.6A

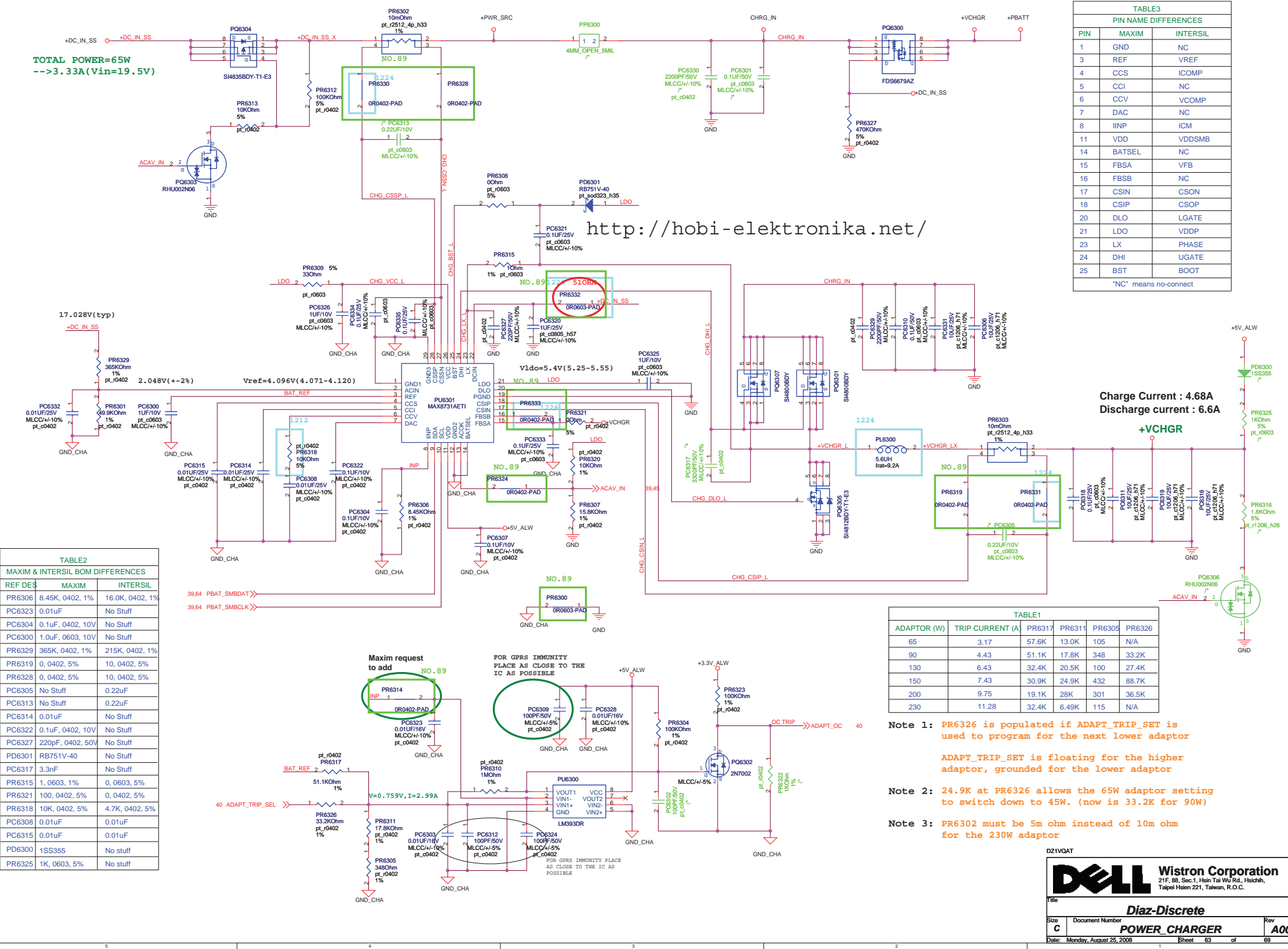
TABLE2 MAXIM & INTERSIL BOM DIFFERENCES		
REF DES	MAXIM	INTERSIL
PR6306	8.45K, 0402, 1%	16.0K, 0402, 1%
PC6323	0.01uF	No Stuff
PC6304	0.1uF, 0402, 10V	No Stuff
PC6300	1.0uF, 0603, 10V	No Stuff
PR6329	365K, 0402, 1%	215K, 0402, 1%
PR6319	0, 0402, 5%	10, 0402, 5%
PR6328	0, 0402, 5%	10, 0402, 5%
PC6305	No Stuff	0.22uF
PC6313	No Stuff	0.22uF
PC6314	0.01uF	No Stuff
PC6322	0.1uF, 0402, 10V	No Stuff
PC6327	220pF, 0402, 50V	No Stuff
PD6301	RB751V-40	No Stuff
PC6317	3.3nF	No Stuff
PR6315	1, 0603, 1%	0, 0603, 5%
PR6321	100, 0402, 5%	0, 0402, 5%
PR6318	10K, 0402, 5%	4.7K, 0402, 5%
PC6308	0.01uF	0.01uF
PC6315	0.01uF	0.01uF
PD6300	1SS355	No stuff
PR6325	1K, 0603, 5%	No stuff

TABLE1					
ADAPTOR (W)	TRIP CURRENT (A)	PR6317	PR6311	PR6305	PR6326
65	3.17	57.6K	13.0K	105	N/A
90	4.43	51.1K	17.8K	348	33.2K
130	6.43	32.4K	20.5K	100	27.4K
150	7.43	30.9K	24.9K	432	88.7K
200	9.75	19.1K	28K	301	36.5K
230	11.28	32.4K	6.49K	115	N/A

Note 1: PR6326 is populated if ADAPT_TRIP_SET is used to program for the next lower adaptor
ADAPT_TRIP_SET is floating for the higher adaptor, grounded for the lower adaptor

Note 2: 24.9K at PR6326 allows the 65W adaptor setting to switch down to 45W. (now is 33.2K for 90W)

Note 3: PR6302 must be 5m ohm instead of 10m ohm for the 230W adaptor



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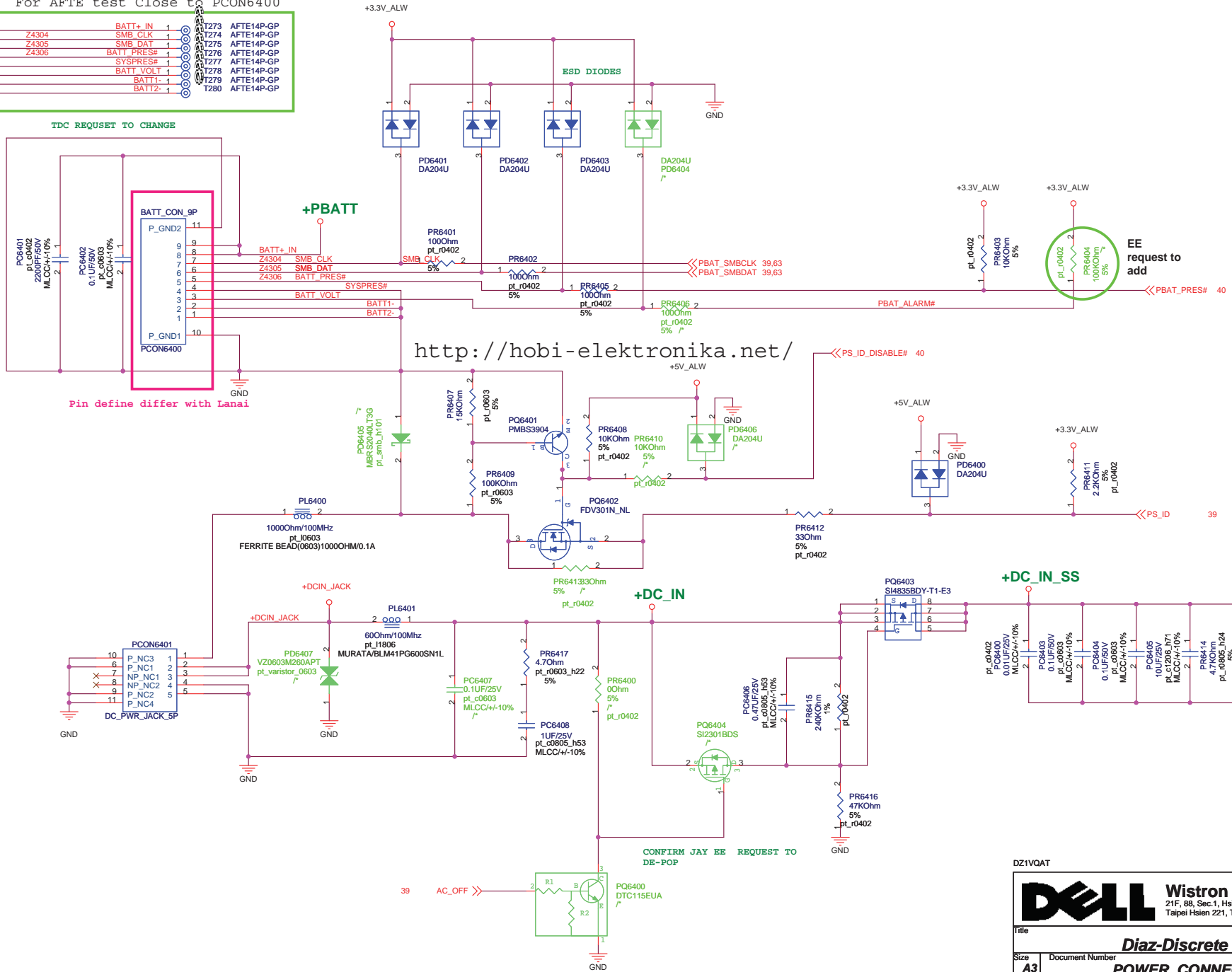
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Size C Document Number **POWER CHARGER** Rev **A00**

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x03 For AFTE test Close to PCON6400

Z4304	BATT+ IN	1	T273	AFTE14P-GP
Z4305	SMB_CLK	1	T274	AFTE14P-GP
Z4306	SMB_DAT	1	T275	AFTE14P-GP
Z4306	BATT_PRES#	1	T276	AFTE14P-GP
	SYSPRES#	1	T277	AFTE14P-GP
	BATT_VOLT	1	T278	AFTE14P-GP
	BATT1-	1	T279	AFTE14P-GP
	BATT2-	1	T280	AFTE14P-GP



DZ1VQAT

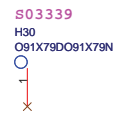
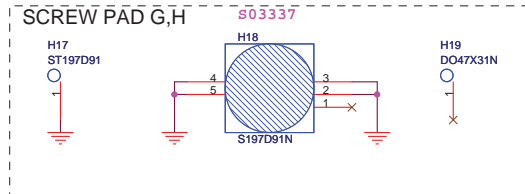
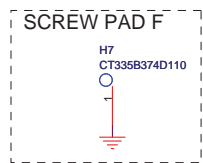
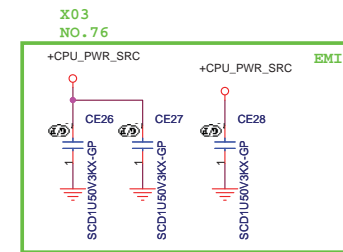
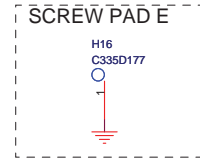
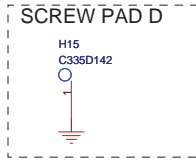
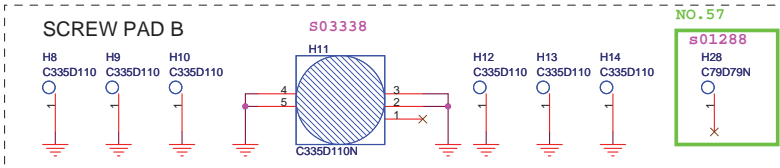
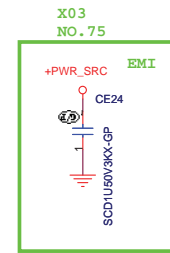
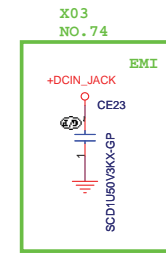
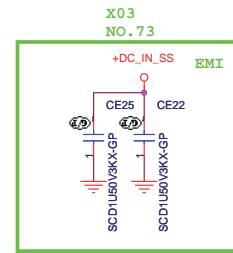
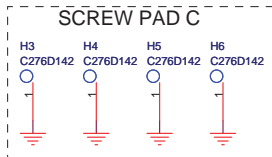
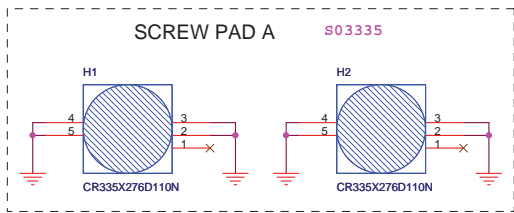
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Title

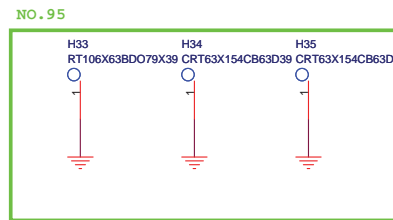
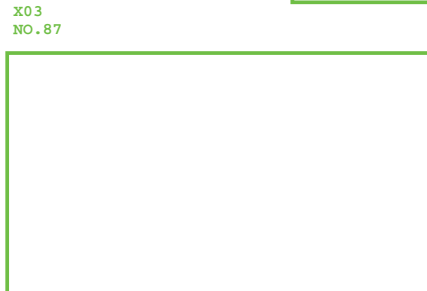
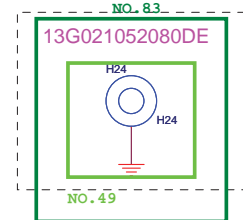
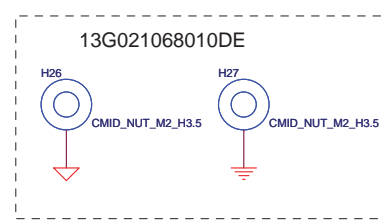
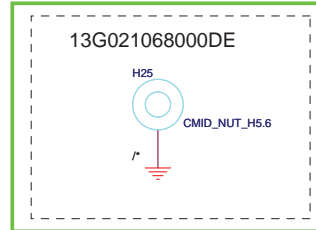
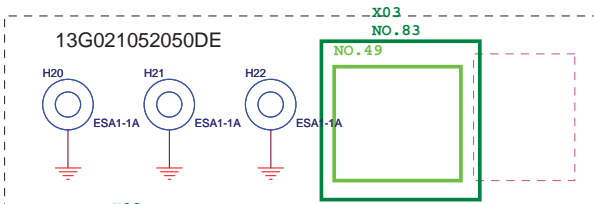
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Size **A3** Document Number **POWER_CONNECTOR** Rev **A00**

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NO. 90



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Size A3 Document Number
SCREW PAD Rev A00

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Version Change list for EE Circuit

Item	Page	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	all	X00 release	10/24/2007		X00 release		X00
2	23	LCD_DDCCLK/LCD_DDCDAT PU resistor	11/30/2007	AA EE	Delete redundant LCD_DDCCLK/LCD_DDCDAT PU resistor	Delete R6855,R6856	X01
3	30	HDMI power	11/30/2007	AA EE	Modify power diode to MOSFET for leakage current that can lower forward voltage and match HDMI 5V voltage range	Replace D4612 by Q19 and connect Q19 gate to RUN_ENABLE	X01
4	51	LAN LED	11/30/2007	AA EE	Changed LAN Jack (CON10) pin12 to +3.3V_LAN	Changed LAN Jack (CON10) pin12 to +3.3V_LAN	X01
5	35	Express card power switch	11/30/2007	AA EE	Express Card power switch (U13) pin4 should be connected to +3.3V_RUN for the purpose of using R1COH/R5538 as 2nd source	Connect U13 pin4 to +3.3V_RUN	X01
6	18	ICH8	11/30/2007	AA EE	ICH8 pin AD11 VCCSUSDA modify to +3.3V_ALW for +3.3V_RUN to solve S5 leakage issue	Connect ICH8 pin AD11 to +3.3V_ALW	X01
7	A1,A2	Audio Board	11/30/2007	AA EE	1.AH1change to NPTH;2.ACON5 change to 12G14200113DE; 3.AU3 pin1 rename to USBP0_D+;U4.AU3 pin3 rename to USBP0_D-U	1.AH1change to NPTH;2.ACON5 change to 12G14200113DE; 3.AU3 pin1 rename to USBP0_D+;U4.AU3 pin3 rename to USBP0_D-U	X01
8	15,44	LED mask circuit	12/05/2007	AA EE	1.Delete sniffer LED mask circuit 2.modify SATA and WPAN LED circuit.	1.Delete R246,R247,Q43 2.modify SATA and WPAN LED circuit	X01
9	17	CLK_ICH_48M	12/06/2007	AA EE	To improve 48MHz clock signal integrity , pop R339, change C456 to 10pF from 4.7pF and make it stuff.	To improve 48MHz clock signal integrity , pop R339, change C456 to 10pF from 4.7pF and make it stuff.	X01
10	29	CRT signals	12/06/2007	AA EE	Fine tune CRT signals	Delete L4912,L4913,L4914;change L4909,L4910,L4911 to 75ohm/100MHz bead;change C6649-C6654 to 10pF	X01
11	25	VRAM description	12/06/2007	AA EE	Modify VRAM Description: change HY5RS123235BFP-14 to H5RS5223CFR-14; change K4J10324QD-BC14 to K4J10324QD-HC14	Change HY5RS123235BFP-14 to H5RS5223CFR-14; Change K4J10324QD-BC14 to K4J10324QD-HC14	X01
12	16,35,50	Reset signals	12/06/2007	AA EE	To improve RESET signals integrity	1.LAN:LOW PERST#,change R32 to 100ohm 2.R1COH/U16: PCI_RST#, R1601 change to 47ohm 3.U13: PLTRST#, add R36=100ohm	X01
13	28	+LCDVCC	12/06/2007	AA EE	Fine tune LVDS power sequence T1 time	Change R17 to 470K ohm from 330K ohm	X01
14	21	PCI Clock	11/12/2007	AA EE	Swap PCI clock to improve skew(EA)	Swap net : CLK_PCI_PCCARD & CLK_PCI_8512	X01
15	21,28,40	Comm.team solution	11/12/2007	AA Comm.	Add components by comm. team's request	P21:Pop C2107, C177, C116, C115, C172, C194, C159 (10pF) P28:Pop C7110, C7111, C7113 (33pF);C7112, C7114 (33pF) ;depop RN2804,pop L1 P40:Pop CN21, CN22, CN23, CN24, CN25, CN26, CN27(33pF)	X01
16	39	IT8512	11/12/2007	AA EE	Add R3920, C3920, C3921 for IT8512E chip changed.	Add R3920, C3920, C3921	X01
17	40	Platform ID	11/12/2007	AA EE	Add platform indicator circuit	Add R4025-28, net name: PLATFORM_ID[0:1]	X01
18	40,43	Connector	11/12/2007	AA EE	Changed Connector by ME request.	page 40 -> change CON4010 page 43 -> change CON3	X01
19	C1	CAPBTN I2C	12/12/2007	AA EE	Fine tune CAPBTN I2C timing.	1.Change I2C damping R (CBT_R795) from 330ohm to 100ohm 2.Add through holes CBT_H15(s01291) & CBT_H28(s03350) F_U3(NCP584HSN181TG): Pin3(CE pin) & Pin4(ECO pin) connect to Pin1(Vin)	X01
20	F1	Finger printer	12/12/2007	AA EE	Correct the connection of F_U3	connect to Pin1(Vin)	X01
21	28	Digital MIC	12/14/2007	AA EE	DMIC clock EMI solution modify	1.R2802 change to L2802:80ohm Bead(Follow Lanai P/N) 2.R2803 change to 47ohm 3.Mount C748 (33p)	X01
22	54	Power Sequence	12/14/2007	AA EE	Follow power circuit.	Remove R73 & net name: 1.25V_RUN_PWRGD	X01
23	A2	Audio Board	12/14/2007	AA EE	Update eSATA connector for USB function only.	changed ACON5 = 12G14200113DE	X01
24	39	IT8512E	12/14/2007	AA EE	Del C3921 (IT8512E I version pop 0ohm, J version pop 0.1uF)	Del C3921	X01
25	40	Platform ID	12/14/2007	AA EE	Del R4025,R4027 to force PCB platform type (Intel SR)	Del R4025, R4027	X01
26	21,33,39,50	XTAL	12/14/2007	AA EE	Change XTAL for better capability	(1) X4 24.576MHz change to 07G010222452DE,C453 change to 22pF,C454 change to 27pF (2) X1 25MHz change to 07G010222509DE, C47,C55 change to 33pF (3) X2 14.318MHz change to 07G01021143CDE , (4) X5 32.768kHz change to 07G01020327ADE, change C667,C654 to 15pF	X01
27	23,25	M82-S PU power	12/17/2007	AA EE	Base on latest M82-S reference schematic to modify LCD I2C and M82-S strapping power	Change LCD_DDCCLK,LCD_DDCDAT and M82 strapping PU power to +3.3V_DELAY from +3.3V_RUN	X01
28	46-48	Audio	12/17/2008	AA EE	1.Modify BOM for BAPD function 2.Modify BOM for gain tunng	1.Unmount R4602 Mount R4601,Q123,R6958 2.Delete R6964,R6965,R6960,R6961,R6970,R6962,R6963,R6971 Add R4701,R4702,R4703,R4704,C4701,C4702	X01
29	50,51	LOM	12/17/2008	AA EE	1.Modify schematic for triple LED control 2.Add EMI solution	1.Add R5110-R5114,D5101; del T5004, add LINK_LED1000# intersheet 2.Add C5110-C5117	X01
30	28	LVDS CON	12/18/2007	AA EE	Change LVDS connector symbol due to connector changed	Update CON6613's symbol	X01
31	33,45,39,47,41,50	Test Point	12/18/2007	AA EE	Add Test Point to meet ICT request	Add T43 at U26 pin4,T44 at U8 pin26,TI45 at U19 pin23 Add Test point for U27,U2,U15 pin14 and U8_3 Add R6856,R4913,R6855,R4919,Q22,Q23	X01
32	30	HDMI	12/18/2007	AA EE	Add level shift circuit for HDMI DDC signals	Add R6856,R4913,R6855,R4919,Q22,Q23	X01
33	41	SPI Flash	12/18/2007	AA EE	Delete SPI Flash damping resistors	Delete R310, R316, R317, R4102	X01
34	31	HDD/ODD Power	12/18/2007	AA EE	Modify HDD/ODD power circuit by customer request	1. unmount: JP4, R3101 2. POP BOM: R5, R7, R399, R400, C13, Q2, Q3, Q56	X01
35	49,A1,A2	USB SWITCH	12/19/2007	AA EE	Remove USB charge function	Delete AU2; rename USBP0_D-U and USBP0_D+U to USBP0_D- and USBP0_D+; connect CON9,ACON1 pin36 to GND, pin29 NC	X01
36	A2	Audio board	12/20/2007	AA EE	Delete AL7, rename AU3 pin1,pin3 to AICH_USBP0+ and AICH_USBP0- for height limit	Delete AL7, rename AU3 pin1,pin3 to AICH_USBP0+ and AICH_USBP0-	X01
37	44	LED	12/20/2007	AA EE	Pop R4411 for WPAN LED PU	Pop R4411	X01
38	C1	Media BTN	12/26/2007	AA EE	Swap LED_PLAY#,LED_STOP#,LED_REWIND#; Swap SNS_REWIND and SNS_PLAY	Swap LED_PLAY#,LED_STOP#,LED_REWIND#; Swap SNS_REWIND and SNS_PLAY	X01

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39	17	USB_WPAN_DET#	12/26/2007	AA EE	Change USB_WPAN_DET# PU resistor to 1Mohm(R341) due to LittleRock BT card pin40 has 100K PD.	Change USB_WPAN_DET# PU resistor to 1Mohm	X01
40	C1	Media BTN	12/26/2007	AA EE	Swap signals due to ID modified	1) Swap LED_REWIND# and LED_PLAY# net names 2) Swap Sense pads net names SNS_REWIND and SNS_PLAY	X01
41	42	USB dual connector	12/26/2007	AA EE	Change CON6610 to 12G13141108ADE	Change CON6610 to 12G13141108ADE	X01
42	40	Board ID	02/14/2008	AA EE	Changed pcb id to X02	Changed pcb id to X02	X02
43	15	XTAL	02/14/2008	AA EE	Modify C375,C377 per XTAL report	Change C375,C377 to 2.7pF	X02
44	15	ICH8 reset signal	02/14/2008	AA EE	U14, U30, U37: power modify to +3.3V_ALW from +3.3V_RUN	U14, U30, U37: power modify to +3.3V_ALW from +3.3V_RUN	X02
45	41,39 C1	CapBTN	02/14/2008	AA EE	Add CapBTN IC reset signal	1. Add CBT_RESET pin(CBT_U7901 pin17,U15 pin19) Add CBT_JP1,CBT_JP2 2. Sense pad modify to elliptic through hole 3. Add a reserved 10uF capacitor parallel to +5V_ALW2 on the CapBtn board 4. Add CAP_EC_RESET off-page at CON6616 pin5 5. LED Mute/VD/VU connect to +5V_ALW2 power rail	X02
46	30,37	Comm. team solution	02/18/2008	AA Comm. Team	Add comm. team solutions	1.Pop L4606, depop RN3701 by comm. Team request 2.CMID: Add C6663 39PF close to C6925	X02
47	47,A1	Audio	02/18/2008	AA EE	Modify ACON2,ACON3,ACON4 footprint. Change value of C492,C496 to improve AP performance	1.ACON4 PCB footprint change to pt_phone_j_6p_4h_col_1f 2.ACON3,ACON2 footprint change to pt_phone_j_6p_4h_col_1f 3.C492 and C496 Bom change to 2.2U(11G236122511310DE) from 1UF	X02
48	21	Clock	02/18/2008	AA EE	Delete reserved resistors	Delete RN1, RN2, RN3, RN5, RN6, RN7, RN8, RN9, RN10, RN11	X02
49	65	Nut	02/18/2008	AA ME	Swap FN of H23,H24 base on updated DXF	Swap FN of H23,H24	X02
50	39	85I2	02/19/2008	AA EE	Chagne 85I2 to Rev.J, pop C3920, depop R3920	Chagne 85I2 to Rev.J, pop C3920, depop R3920	X02
51	47	Speaker gain	02/21/2008	AA EE	Fine tune gain	1.Unmount R374,R377, mount R379,R368 2.R4701,R4703 change to 24.3Kohm, R4702,R4704 mount 100Kohm	X02
52	39,62	85I2	02/21/2008	AA EE	Add another path to control GFX_EN signal to solve glitch issue of 85I2 pin104	1.Delete T3901,add net GFX_CORE_ON_1 at U15 pin104 2.Add PR6211	X02
53	F1	Finger Printer	02/22/2008	AA EE	Add TP:F_T14 at F_+3.3V_RUN	Add TP:F_T14 at F_+3.3V_RUN	X02
54	46,48 49	Audio	02/25/2008	AA EE	Modify Audio circuit to solve Pop sound issue	(1) SWAP port B and port F. (2).Delete C7120, (3)add D4601 and D4602	X02
55	44	LED	02/25/2008	AA EE	Change LED1 to White&Orange(07G01520097SDE) from Blue&Orange 07G01520053QDE	Change LED1 to White&Orange from Blue&Orange	X02
56	46	Audio	02/26/2008	AA EE	Connect R559 pin1 to AUD_SENSE_B from AUD_SENSE_A	Connect R559 pin1 to AUD_SENSE_B from AUD_SENSE_A	X02
57	65	Screw pad	02/26/2008	AA EE	Modify H28 size base on ME request	Modify H28 size base on ME request	X02
58	39	XTAL	03/13/2008	AA EE	Modify C667,C654 to 7pF from 15PF	Modify C667,C654 to 7PF from 15PF	X02
59	39	85I2	03/13/2008	AA EE	Depop C3920, pop 1uF at R3920 for 85I2.	Depop C3920, pop 1uF at R3920 for 85I2.	X02
60	52	SOFT START	05/15/2008	W EE	Change PC58 to 3900pF and populate it for soft star.	Change PC58 to 3900pF and populate it for soft star.	X02
61	63	POWER CCV	05/15/2008	W EE	Change PR6318 from 4.7K to 10K ohm by power team suggestion.	Change PR6318 from 4.7K to 10K ohm by power team suggestion.	X02
62	63	CHARGER	05/15/2008	W EE	Change PR6332 from 1 ohm to 0 ohm and populate it for charger function	Change PR6332 to 0 ohm and populate it for charger function.	X02
63	63	CHARGER	05/15/2008	W EE	Pop PR6333 for charger function	Pop PR6333 for charger function	X02
64	63	CHARGER	05/15/2008	W EE	Pop PR6330 for charger function	Pop PR6330 for charger function	X02
65	63	CHARGER	05/15/2008	W EE	Pop PR6331 for charger function	Pop PR6331 for charger function	X02
66	52	SOFT START	05/15/2008	W EE	Pop PC186	Pop PC186 for soft star.	X02
67	52	SOFT START	05/15/2008	W EE	Pop PC182	Pop PC182 for soft star.	X02

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68	62	+5V_SUS LEAKAGE	06/19/2008	Power team	+5V_SUS leakage in S5	Take off PR6225 by power team suggestion.	X03
69	L1	add conn.	06/24/2008	ME EE	To reduce the time of LID BD cable manual rework	Add connector HALL1.	X03
70	A2	Audio board	06/30/2008	EE	Change connector ACON5 to "22.10218.D31"	Change connector ACON5 to "22.10218.D31"	X03
71	40	Board ID	07/01/2008	EE	Board ID change to X03	R534 is depop and R535 is pop.	X03
72	66-72	I/O board	07/01/2008	EE	Remove I/O board schematic	Independence I/O board schematic for layout ME issue	X03
73	65	EMC suggestion	07/03/2008	EMC	By EMC team suggestion.	Add CE22 and CE25 between +DC_IN_SS and GND.	X03
74	65	EMC suggestion	07/03/2008	EMC	By EMC team suggestion.	Add CE23 between +DCIN_JACK and GND.	X03
75	65	EMC suggestion	07/03/2008	EMC	By EMC team suggestion.	Add CE24 between +PWR_SRC and GND.	X03
76	65	EMC suggestion	07/04/2008	EMC	By EMC team suggestion.	Add CE26, CE27 and CE28 between +CPU_PWR_SRC and GND.	X03
77	37	SIM CARD	07/04/2008	EE	For SI : UIM_CLK add R6634 0ohm	Add R6634 0 ohm resistance	X03
78	29	VGA CRT	07/05/2008	EE	For SI : CRT RGB rise/fall time and Hsync/Vsync signal issue	1. Depop 6 caps : C6649 C6650 C6651 C6652 C6653 C6654 2. Change L4610 and L4611 to 0 ohm resistance (63.00000.00L) 3. Change bead L4909 L4910 L4911 to 22 ohm/100MHz (68.00143.11L)	X03
79	18	IC88-M	07/05/2008	EE	Change bead dimension	L49 change dimension form 1210 to 0805 (68.1R090.10A)	X03
80	10	Crestline(VGA,DMI)	07/05/2008	EE	Change resistance dimension	R161 change dimension form 0603 to 0402 (64.39205.6DL)	X03
81	36 37	MINI CARD	07/05/2008	EE	Prevent pin short to pin	Change CON6602 and CON6605 to 62.10043.511	X03
82	38	MINI CARD	07/05/2008	EE	Prevent pin short to pin	Change CON6603 to 62.10043.441	X03
83	65	SCREW PAD	07/05/2008	EE	For ME suggestion	Remove H23 and change H24 to 34.4Z402.001	X03
84	15	IC88	07/08/2008	EE	For ICH_AZ_CODECS_SDOUT	Change R275 to 47 ohm resistance (63.47034.1DL)	X03
85		TEST PAD	07/08/2009	EE	For PSE suggestion	1. Add connector test pad (ZZ.AFT14.101) 2. Change all test pad to ZZ.PAD14.001	X03
86	40	IC IT8301E	07/08/2009	EE	For Board ID	Add R538 and R539 but depop	X03
87	65	SCREW PAD	07/08/2009	ME EE	Remove CIR scerw hole	Remove H32 and H33	X03
88	31	SATA	07/08/2009	EE	Separate HDD and ODD power plane	Remove J4	X03
89		CLOSE GAP	08/05/2009	EE	Replace 0 ohm resistance to close gap	Page 10 change R151, R462, R465, R466, R486 to close gap Page 13 change L42, R1301 to close gap Page 13 replace JP2, JP3 by close gap Page 15 change R213 to close gap Page 16 change R1602, R1603 to close gap Page 17 change R252, R508 to close gap Page 21 change R71 to close gap Page 23 change R2301, R2302, R2303 to close gap Page 26 change R6923, R6925 to close gap Page 28 change R2801, R604, R616 to close gap, remove RN2804 Page 29 change L4610, L4611, R6639 to close gap Page 30 change R3001, R4913, R4919, RN42A, RN42B, RN43A, RN43B, RN44A, RN44B, RN45A, RN45B to close gap and remove L4650, L4651, L4652, L4653 Page 32 change R363, R566 to close gap Page 33 change R342, R3301 to close gap Page 34 change RN488A, RN488B, RN490A, RN490B to close gap, remove L43, L44 Page 35 change RN499A, RN499B to close gap, remove L46 Page 36 change R6617, R6618, J3 to close gap Page 37 change RN3701A, RN3701B to close gap, remove L4606 Page 38 change R6895, R6896, R6897, RN3801A, RN3801B to close gap, remove L4605 Page 39 change R225, R274, R529, R592, R6934 to close gap Page 40 change R241 to close gap Page 42 change RN4201A, RN4201B, RN4202A, RN4202B to close gap, remove L4616, L4617 Page 43 change R4301, R4302 to close gap Page 44 change R284, R600, R4415 to close gap Page 45 change R398 to close gap Page 47 change R6930 to close gap Page 48 change R6919, R6920, R6931 to close gap Page 50 change R126, R4902, R4905, R4903, R4907, R4910, R4911, R4914, R4915, R4918, R4921, R4922, R4924 to close gap Page 52 change PR56, PR200 to close gap Page 54 change R52, R150, R427, R504, R519 to close gap Page 56 change RN5601A, RN5601B to close gap, remove L4915 Page 58 change PR5815, PR5823, PR5827, PR5828, PR5840 to close gap Page 59 change PR5905, PR5916, PR5918, PR5919, PR5924, PR5925 to close gap Page 60 change PR6000, PR6007 to close gap Page 61 change PR6104, PR6112, PR6117, PR6118 to close gap Page 62 change PR6204, PR6210, PR6211, PR6217, PR6229, PR6232 to close gap Page 63 change PR6300, PR6314, PR6319, PR6324, PR6328, PR6330, PR6331, PR6332, PR6333 to close gap	A00
90		WWAN	08/05/2009	EE	Remove WWAN function	Page 16 dummy C439, C443, R356 Page 21 dummy R66, R2118 Page 37 dummy C6636, C6637, C6638, C6639, C6640, C6641, C6642, C6643, C6644, C6645, C6646, C6647, C6648, CE17, CE18, CON6605 Page 57 dummy CON6615 Page 65 dummy H25	A00

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91	52	POWER CONTROL	08/05/2009	EE	Soft start	Change PC192 from 4700pF to 0.1uF	A00
92	40	Board ID	08/07/2008	EE	Change board ID for A00	Pop R534 and R536, depop R535 and R537, remove R538 and R539	A00
93	54	Power sequence logi	08/07/2008	EE	For RESET_OUT# pull low	Add 1K ohm resistance R5401	A00
94	43	CIR	08/07/2008	EE	For FSE suggestion	Add close gap R4303	A00
95	65	SCREW PAD	08/07/2008	EE	For CIR support to prevent CIR damage	Add H33, H34, H35	A00
96	40	EC IT8301E	08/12/2008	EE	For keyboard backlight detect	Add R4029 and R4030 but depop	A00
97	33	R5C833	08/18/2008	EE	For Ms/XD/SD clock overshoot/undershoot over spec	Change R545 from 0 ohm to 33 ohm	A00
98	30	HDMI	08/21/2008	EE	Reduce +5V_HDMI noise	Change C6925 from 100pF to 0.1uF	A00

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