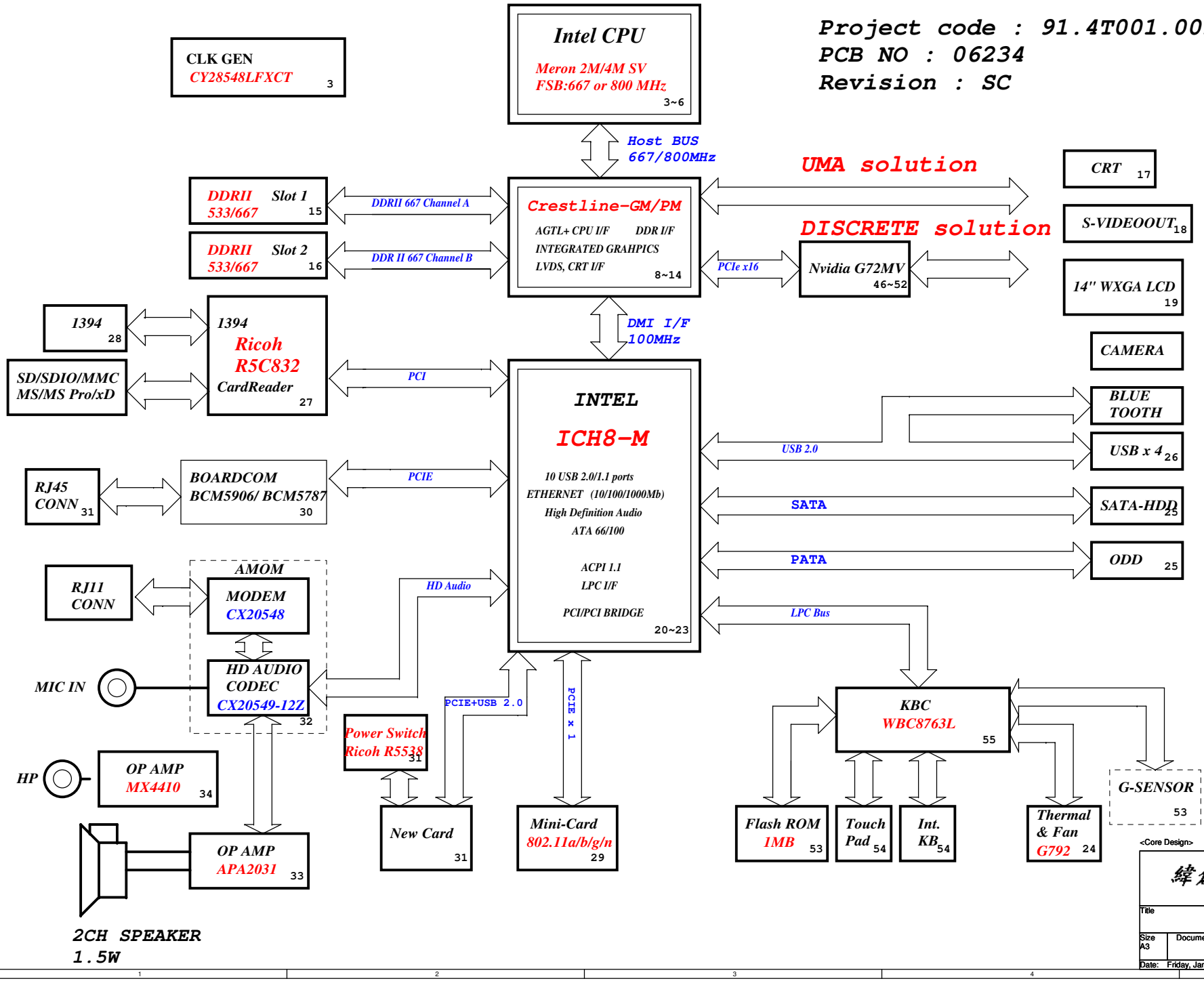
Anote2.0 Block Diagram

Project code : 91.4T001.001
PCB NO : 06234
Revision : SC



SYSTEM DC/D
TPS51120

INPUTS	OUTP
DCBATOUT	5V_S3 3D3V_S

SYSTEM DC/D
ISL6268CAZ

INPUTS	OUTPU
DCBATOUT	1D05V_

SYSTEM DC/D
TPS51116

INPUTS	OUTPU
DCBATOUT	1D8V_S 0D9V_S

CHARGER
ISL6255

INPUTS	OUTPU
DCBATOUT	BT+ 20V 3. 5V 1C

CPU DC/DC
ISL6262ACRZ

INPUTS	OUTPU
DCBATOUT	VCC_C

PCB LAYE

L1: Signal 1
L2: VCC
L3: Signal 2
L4: Signal 3
L5: GND
L6: Signal 4

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C

Title: Block Diagram
Size: A3
Document Number: Anote2.0 INTEL
Date: Friday, January 12, 2007
Sheet 1 of

INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIE Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCL1_5 VRM Enable/Disable.Always sampled.	Enables integrated VccSus1_05,VccSus1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIE LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overidden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap

ICH_RSVD_tp3	AZ_DOUT_ICH	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation(default)
1	1	Set PCIE port cofig bit1

A16 swap override strap

PCI_GNT#3	
low	= A16 swap override enable
high	= default

BOOT BIOS Strap

PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

integrated VccSus1_05,VccSus1_5,VccCL1_5

SM_INTVRMEN	High=Enable	Low=Disable

integrated VccLan1_05VccCL1_05

LAN100_SLP	High=Enable	Low=Disable

DEFAULE HIGH

No Reboot Strap

SPKR	LOW = Defaule
	High=No Reboot

8.2K PULL HIGH

INTEL CRESTLINE STRAP PIN

CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	DMI X 4 ★
CFG 8 Low Power PCI Express	Normal★	Low Power mode
CFG 9 PCI Express Graphics Lane Reversal	Lane Reversal	Normal Mode(Lanes number in order) ★
CFG 16 FSB Dynamic ODT	Disabled	Enabled ★
CFG 19 DMI Lane Reserved	Normal Operation ★	Reserved Lane
CFG 20 Concurrent SDVO/PCIE	Only PCIE or SDVO is operation ★	PCIE and SDVO are operation simultaneous
SDVO_CTRL_DATA SDVO Present	NO SDVO Card Present ★	SDVO Card Present

CFG 12 CFG 13	XOR/ALL-Z
LL(00)	Reserved
LH(01)	XOR Mode Enabled
HL(10)	All Z Mode Enabled
HH(11)	Normal Operation

INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	TBD

<21,23> +RTCVCC — +RTCVCC
<4,5,6,7,8,11,12,13,21,23,39> 1D05V_S0 — 1D05V_S
<3,10,12,23,42> 1D25V_S0 — 1D25V_S
<30> 1D2V_LAN_S5 — 1D2V_LA
<31,57> 1D5V_NEW_S0 — 1D5V_NE
<10,12,13,15,16,40,42,45> 1D8V_S3 — 1D8V_S3
<30,31> 2D5V_LAN_S5 — 2D5V_LA
<24,38,44,53,54,55> 3D3V_AUX_S5 — 3D3V_AU
<30,31> 3D3V_LAN_S5 — 3D3V_LA
<3,10,11,12,13,15,16,17,18,19,20,21,22,23,24,25,27,28,29,30,31,32,34,35,36,38,39,41,42,45,46,47,50,52,53,54,55,56,57,58> 3D3V_S0 — 3D3V_S0
<19,20,21,22,23,26,29,30,31,32,38,40,43,45,53,54,55,58> 3D3V_S5 — 3D3V_S5
<29,38,43> 5V_AUX_S5 — 5V_AUX_
<17,19,22,23,24,25,33,35,36,39,41,42,45,46,54,56,57> 5V_S0 — 5V_S0
<23,26,38,40,45,56> 5V_S5 — 5V_S5
<43,44> AD+ — AD+
<19,36,37,38,39,40,41,43,45,56> DCBATOUT — DCBATOU
<10,15,16,40> DDR_VREF_S3 — DDR_VRE
<19> LCDVDD_S0 — LCDVDD_
<5,6,37> VCC_CORE_S0 — VCC_COR

<Core Design>

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Taipei Hsien 221, Taiwan, R.O

Title: Table of Content

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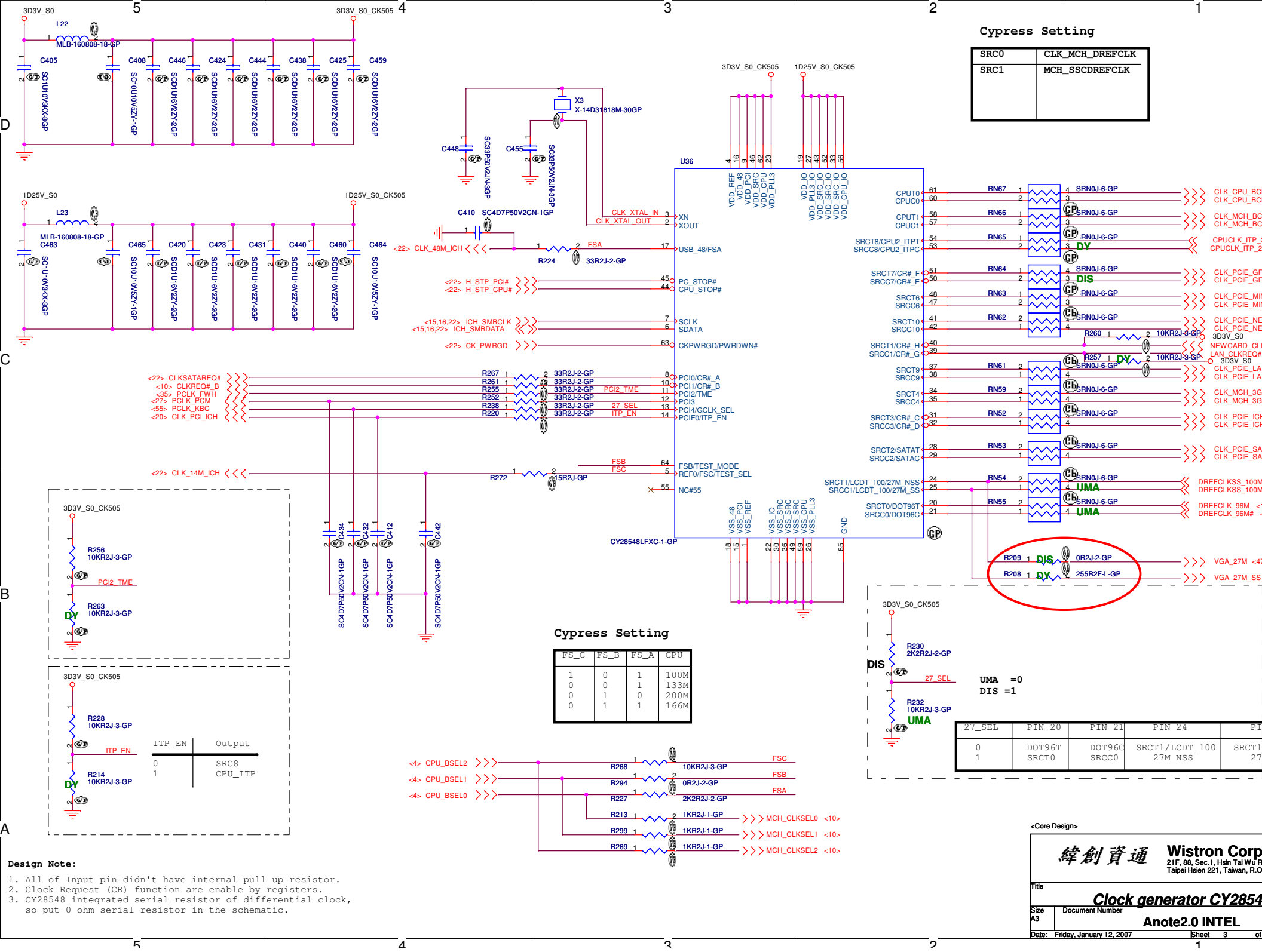
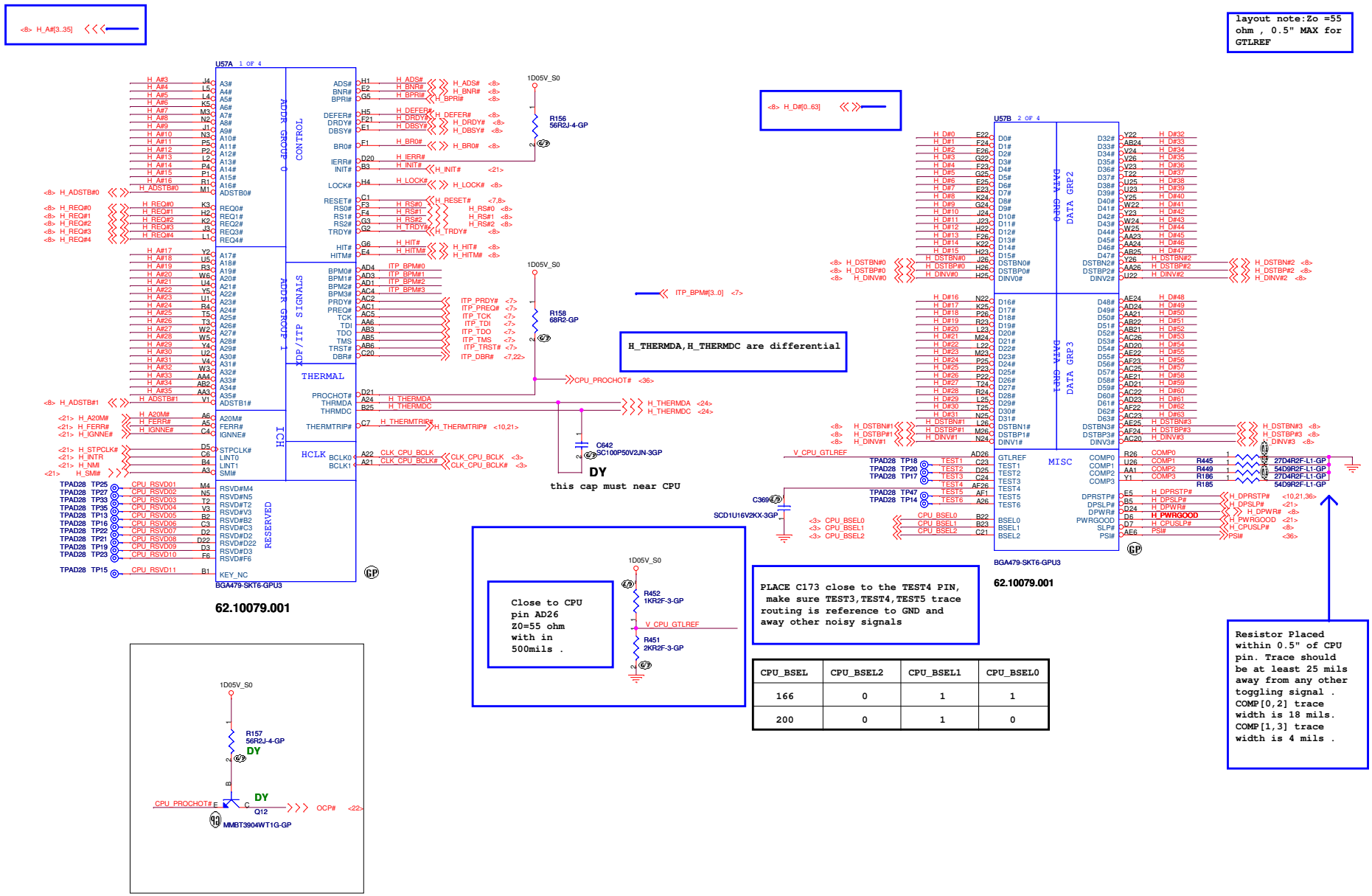

Cypress Setting
SRC0 CLK_MCH_DREFCLK
SRC1 MCH_SSCDREFCLK
U36
CY28548LFXC-1-GP
X3
X-14D31818M-30GP
Cypress Setting
FS_C FS_B FS_A CPU
1 0 1 100M
0 0 1 133M
0 1 0 200M
0 1 1 166M
ITP_EN Output
0 SRC8
1 CPU_ITP
UMA =0
DIS =1
27_SEL PIN 20 PIN 21 PIN 24
0 DOT96T DOT96C SRCT1/LCDT_100
1 SRCT0 SRCC0 27M_NSS
Design Note:
1. All of Input pin didn't have internal pull up resistor.
2. Clock Request (CR) function are enable by registers.
3. CY28548 integrated serial resistor of differential clock,
so put 0 ohm serial resistor in the schematic.
<Core Design>
Wistron Corp
Title
Clock generator CY2854
Size A3
Document Number
Anote2.0 INTEL
Date: Friday, January 12, 2007
Sheet 3



CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

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Title: Meron(1/3)-AGTL+/XDP

Size	Document Number	Rev
Custom	Anote2.0 INTEL	SC

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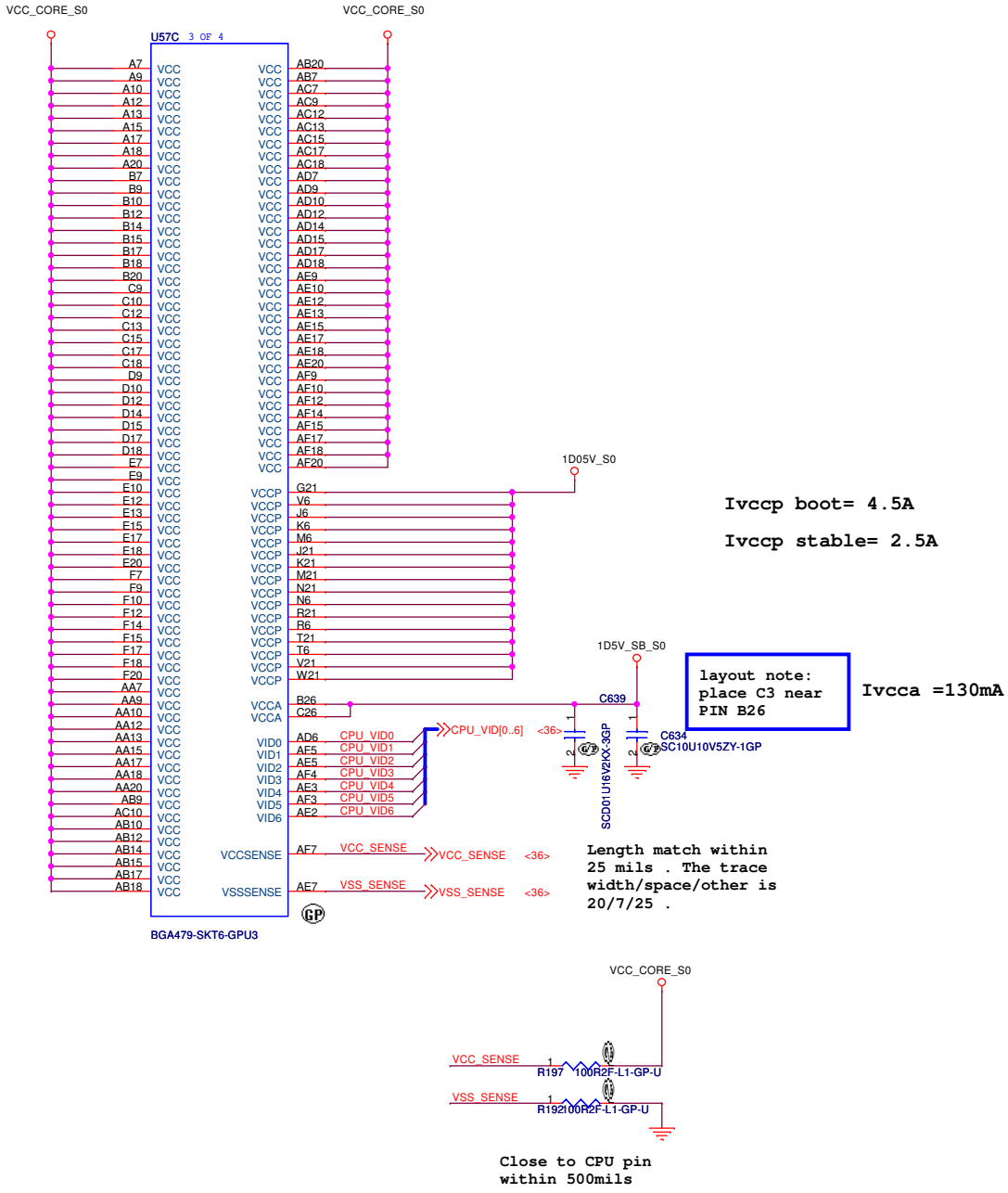

<Core Design>

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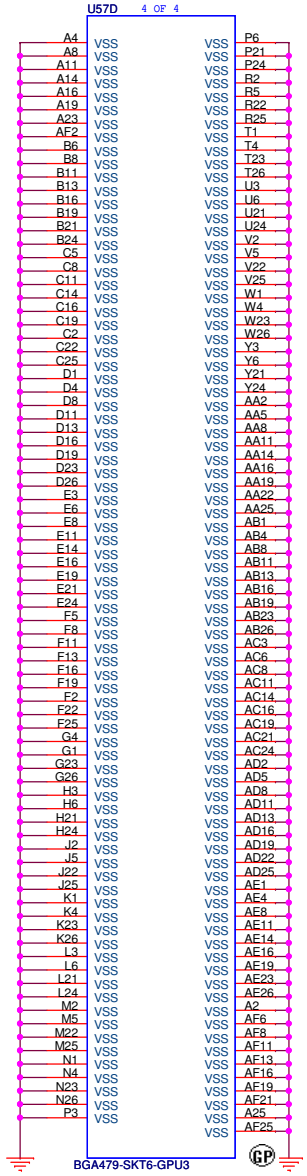
Taipei Hsien 221, Taiwan, R.O

Title: Meron(2/3)-AGTL+/PWR

Size: A3 | Document Number: Anote2.0 INTEL

Date: Friday, January 12, 2007 | Sheet 5 of



VCC_CORE_S0

Place these capacitors on L1
(North side ,Secondary Layer)

C686 C675 C676 C677 C678 C679 C680 C261
SC10U6D3V5MX-3GP

VCC_CORE_S0

Place these capacitors on L1
(North side ,Secondary Layer)

C273 C274 C260 C687 C688 C683 C684 C685
SC10U6D3V5MX-3GP

Mid Frequencd Decoupling

VCC_CORE_S0

Place these capacitors on L1
(North side ,Secondary Layer)

C358 C340 C341 C277 C276 C368 C375 C360
SC10U6D3V5MX-3GP

DY DY DY DY DY DY DY DY

1D05V_S0

C298 SCD1U16V2KX-3GP
C285 SCD1U16V2KX-3GP
C324 SCD1U16V2KX-3GP
C279 SCD1U16V2KX-3GP
C286 SCD1U16V2KX-3GP
C314 SCD1U16V2KX-3GP

Place these inside socket cavity on L1 (North side Secondary)

<Core Design>

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Title: Meron(3/3)-GND&Bypass

Size: A3 | Document Number: Anote2.0 INTEL

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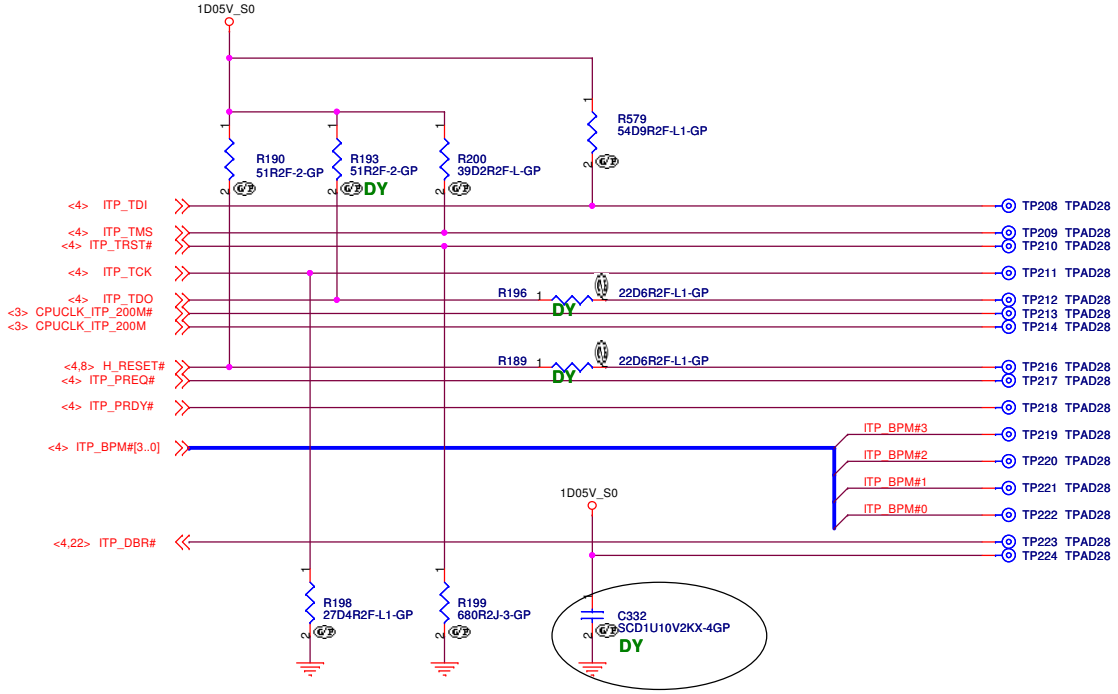
ITP Connector



<Core Design>

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Title: Meron(3/3)-GND&Bypass

Size: A3 | Document Number: Anote2.0 INTEL

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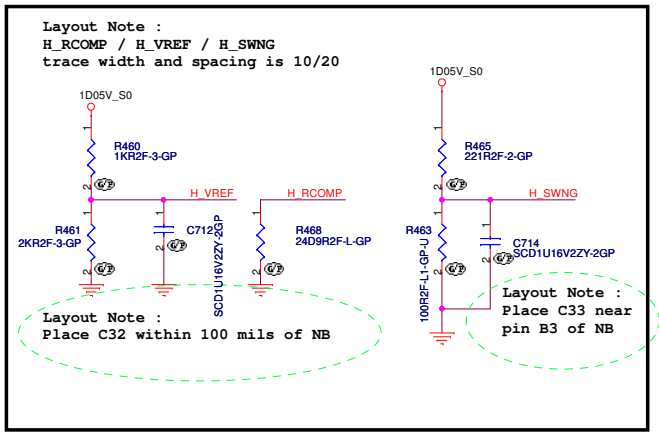
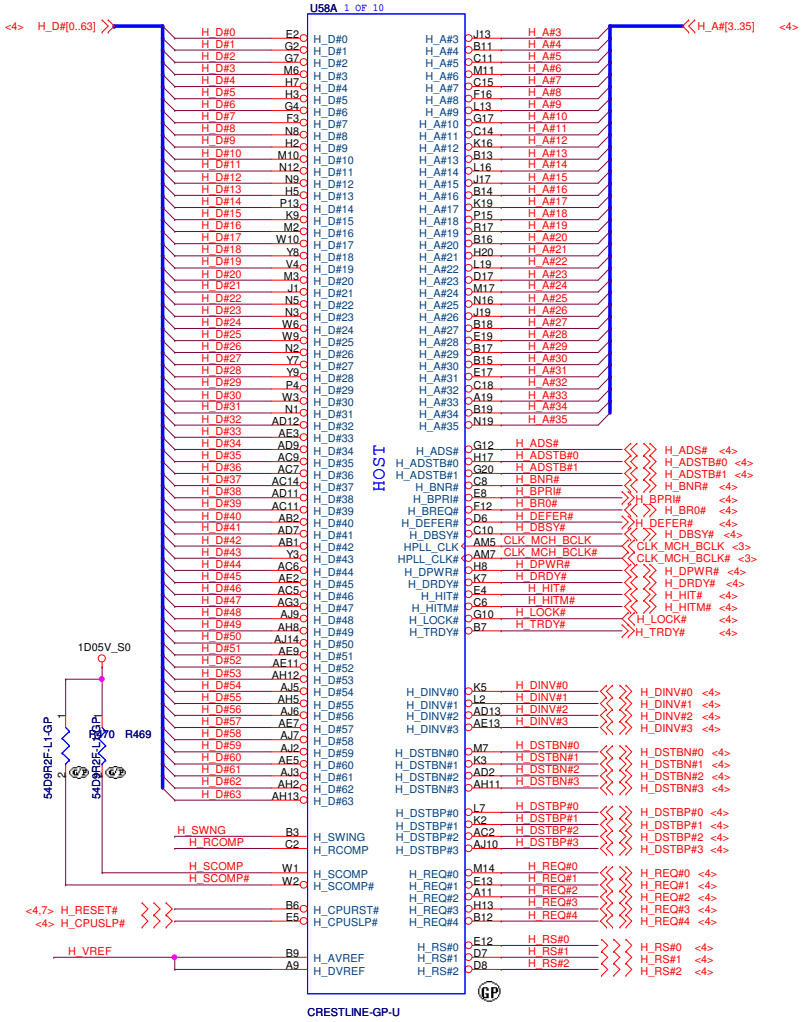
layout note :
Route H_SCOMP and H_SCOMP# with trace width, spacing
and impedance (55 ohm) same as FSB data traces





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Title: CRESTLINE(1/7)-AGTL+/DMI/DDR2

Size	Document Number	Rev
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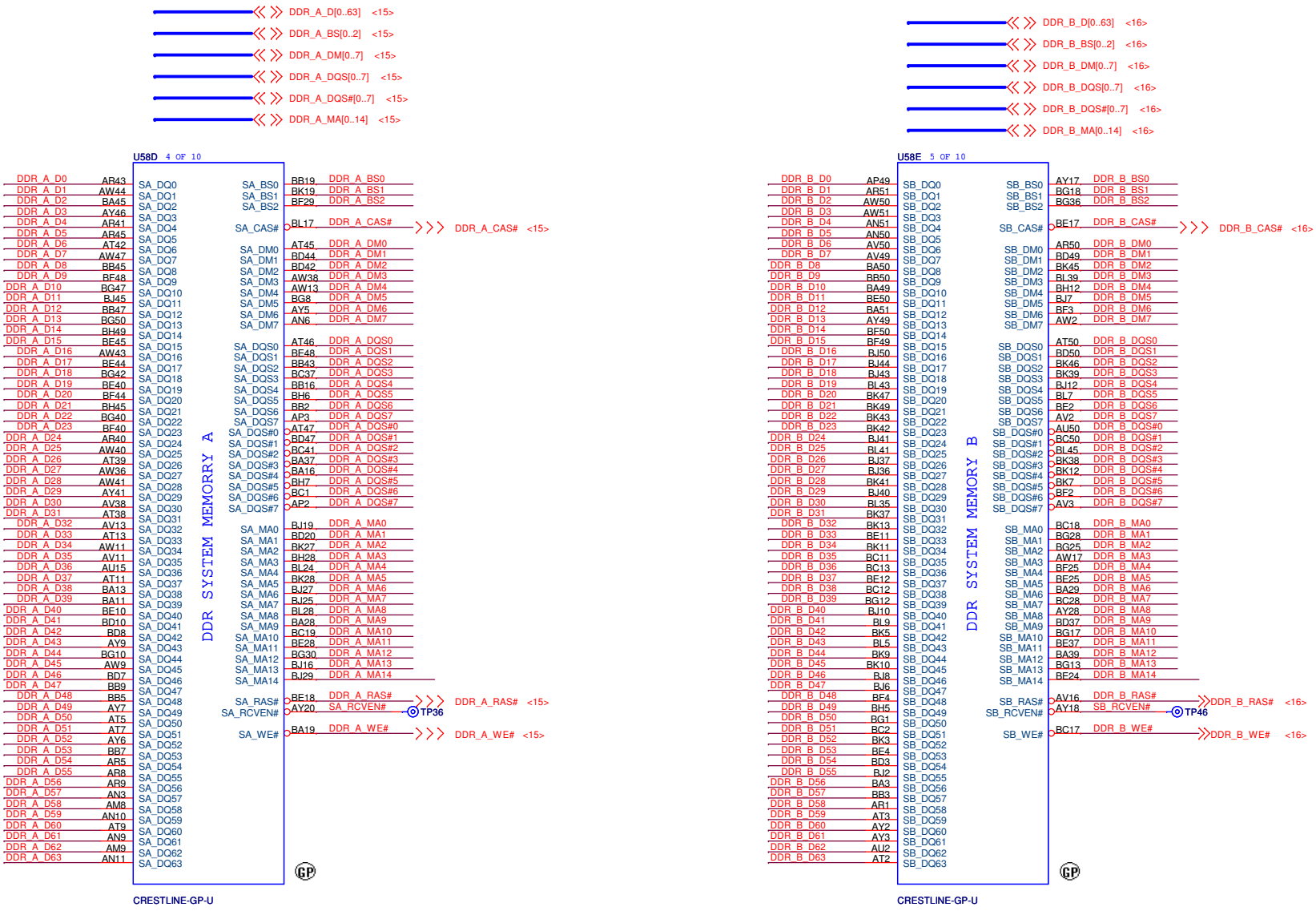

<Core Design>

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Title
CRESTLINE(2/7)-DDR2 A/B CH

Size A3 | Document Number **Anote2.0 INTEL**

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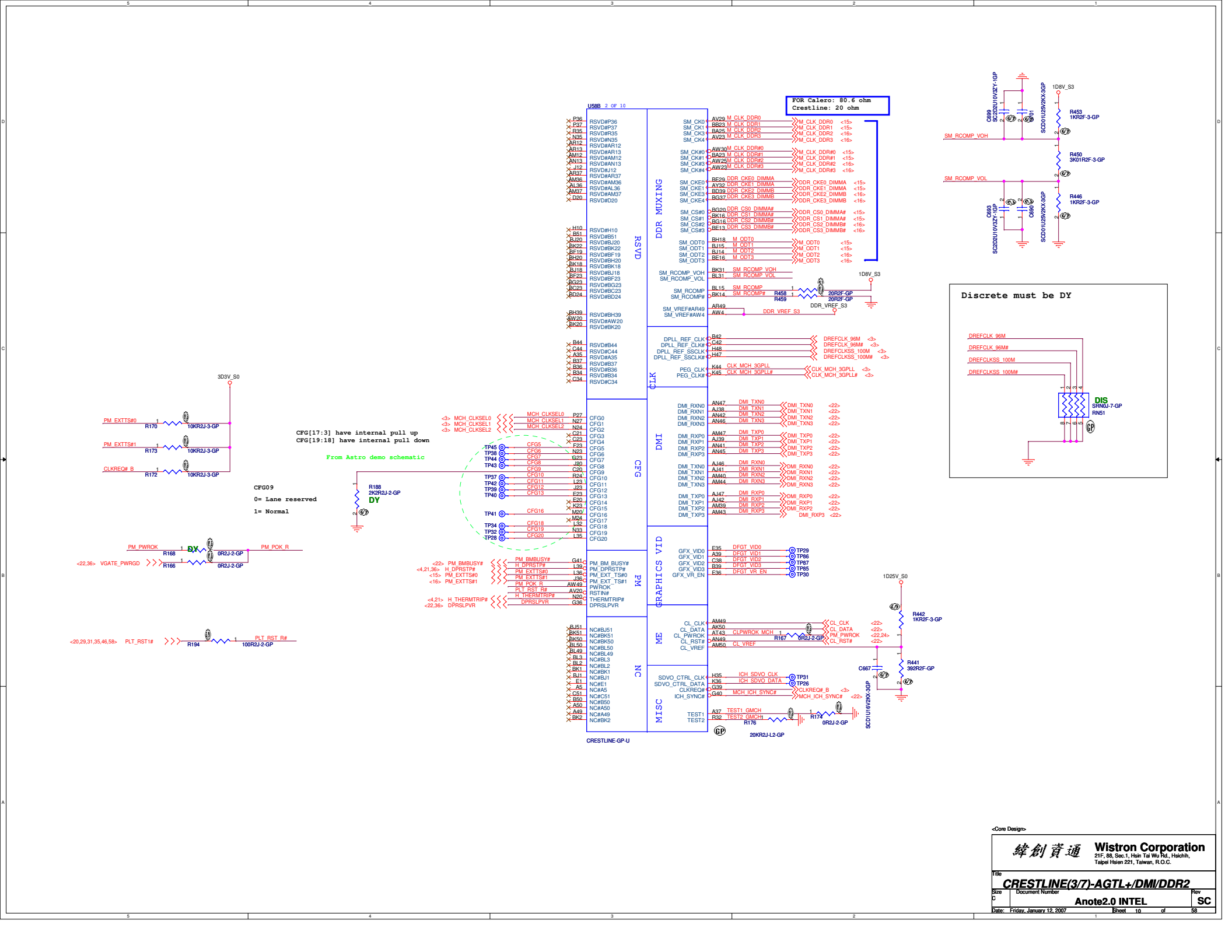

<Core Design>

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Title: CRESTLINE(3/7)-AGTL+/DMI/DDR2

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Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default)*
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disable 1 = Enable *
CFG[18:17]	Reversed
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19(DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse lane
CFG20(PCIE/SDVO consurrent)	0 = Only PCIE or SDVO is operation 1 = PCIE/SDVO are operating simu.

3D3V_S0 RN21 SRN10KJ-5-GP UMA

1D05V_S0 R171 24D9R2F-L-GP

PEGCOMP trace width and spacing is 20/25 mils.

U58C 3 OF 10

For Crestline : 2.4 Kohm
For Calero : 1.5Kohm

LVDS: L_BKLT_CTRL, L_BKLT_EN, L_CTRL_CLK, L_CTRL_DATA, L_DDC_CLK, L_DDC_DATA, L_VDD_EN, LVDS_IBG, LVDS_VBG, LVDS_VREFH, LVDS_VREFL, LVDSA_CLK#, LVDSA_CLK, LVDSB_CLK#, LVDSB_CLK, LVDSA_DATA#0..3, LVDSA_DATA0..3, LVDSB_DATA#0..2, LVDSB_DATA0..2

TV: TVA_DAC, TVB_DAC, TVC_DAC, TVA_RTN, TVB_RTN, TVC_RTN, TV_DCONSEL0, TV_DCONSEL1

VGA: CRT_BLUE, CRT_BLUE#, CRT_GREEN, CRT_GREEN#, CRT_RED, CRT_RED#, CRT_DDC_CLK, CRT_DDC_DATA, CRT_VSYNC, CRT_TVO_IREF, CRT_HSYNC

PCI_EXPRESS GRAPHICS: PEG_COMPI, PEG_COMPO, PEG_RX#0..15, PEG_RX0..15, PEG_TX#0..15, PEG_TX0..15

PEG_RXN[15..0] <46>
PEG_RXP[15..0] <46>
PEG_TXN[15..0] <46>
PEG_TXP[15..0] <46>

CRESTLINE-GP-U

FOR Calero: 255 ohm
Crestline: 1.3k ohm

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Title: CRESTLINE(4/7)-VGA/LVDS/

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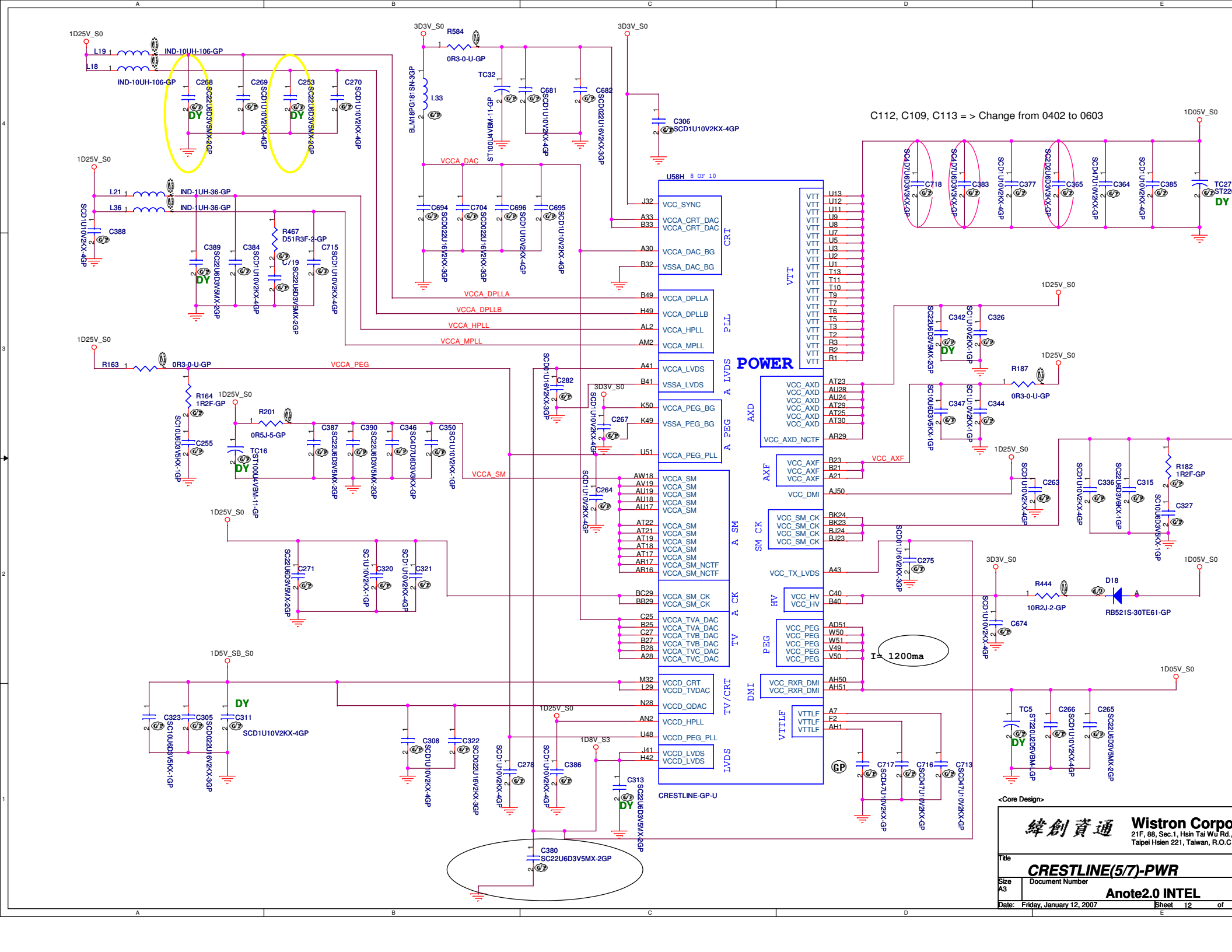
C112, C109, C113 = > Change from 0402 to 0603
POWER
CRESTLINE-GP-U
I= 1200ma
Wistron Corpo
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Title
CRESTLINE(5/7)-PWR
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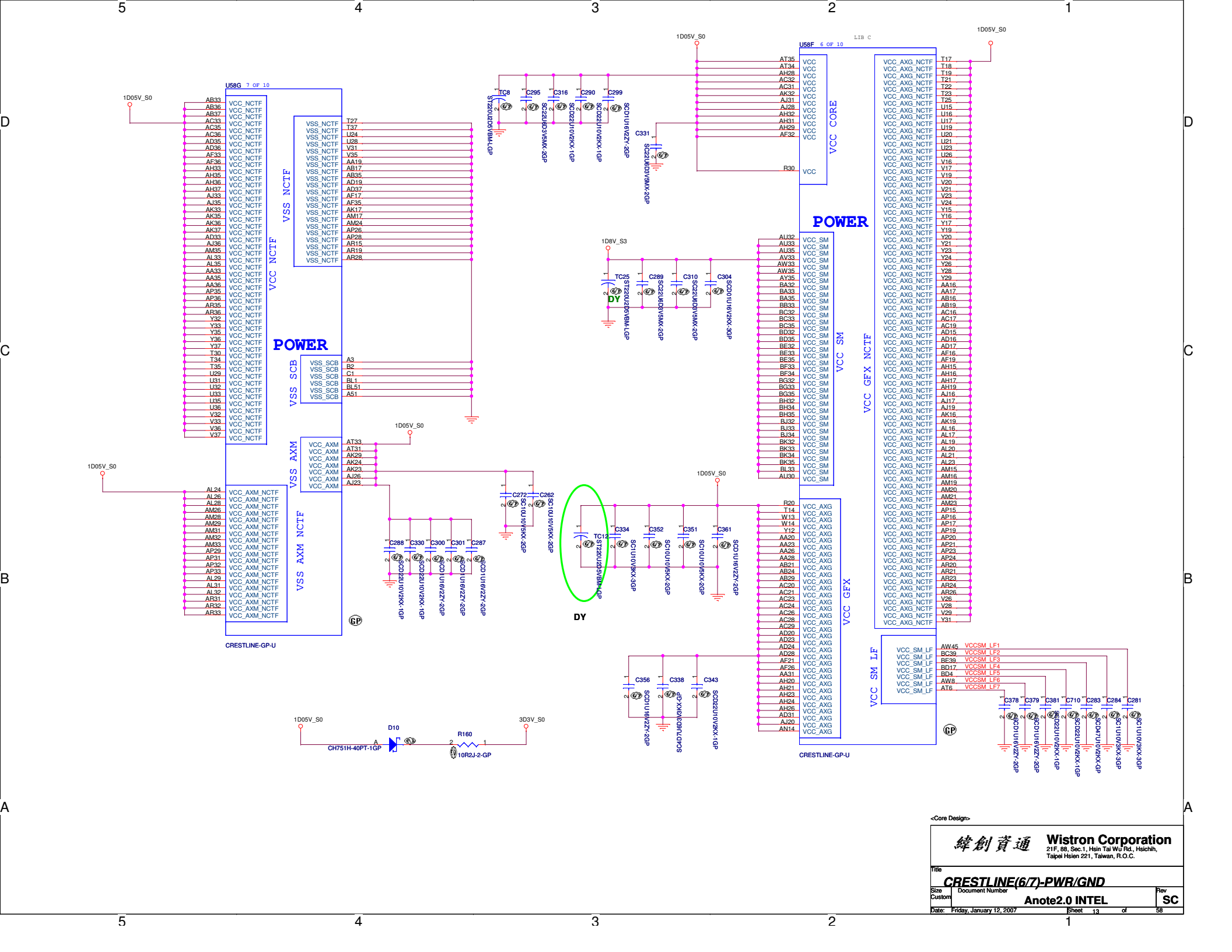

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<Core Design>

Title: CRESTLINE(6/7)-PWR/GND

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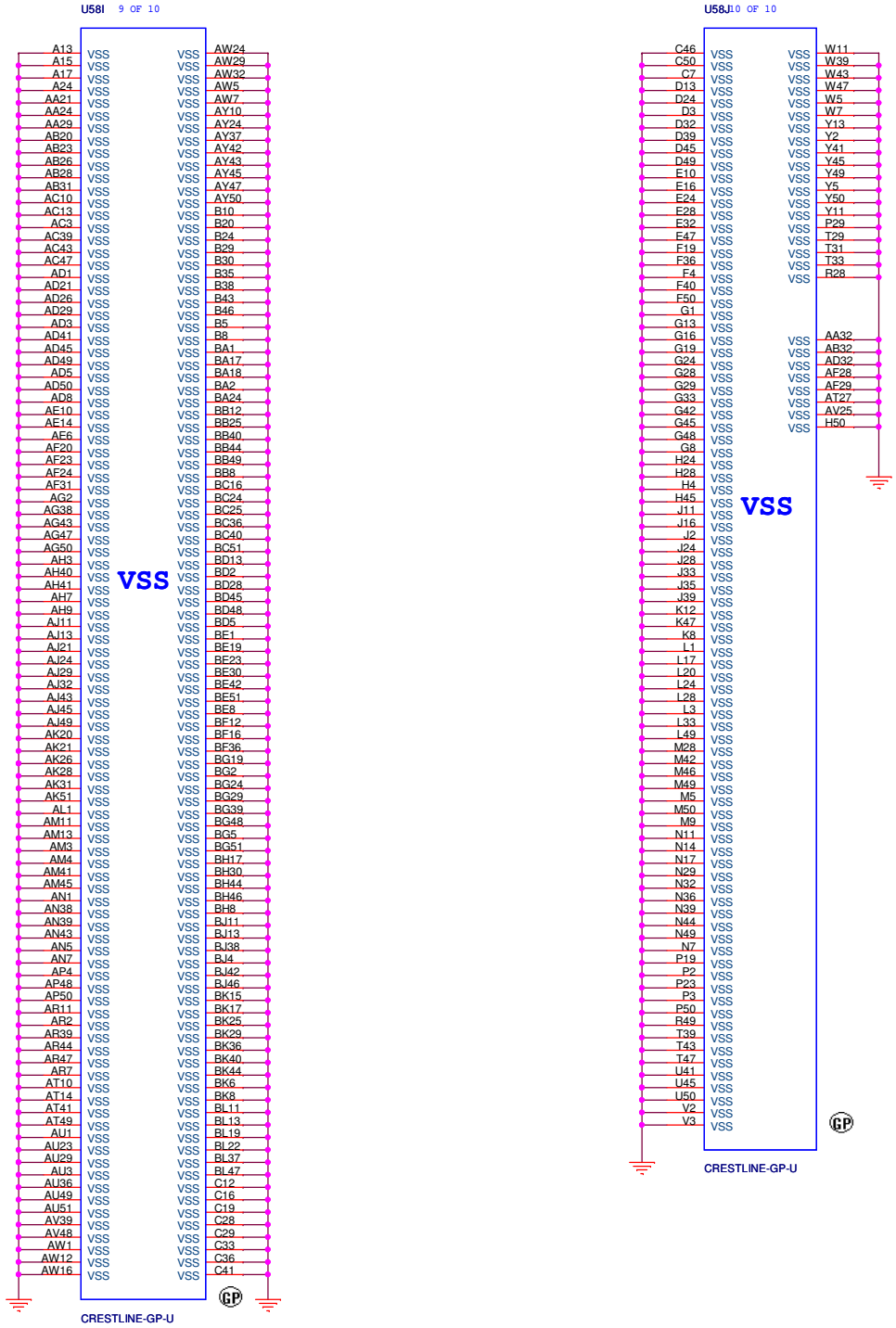

<Core Design>

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Title
CRESTLINE(7/7)-PWR/GND

Size A3 | Document Number Anote2.0 INTEL

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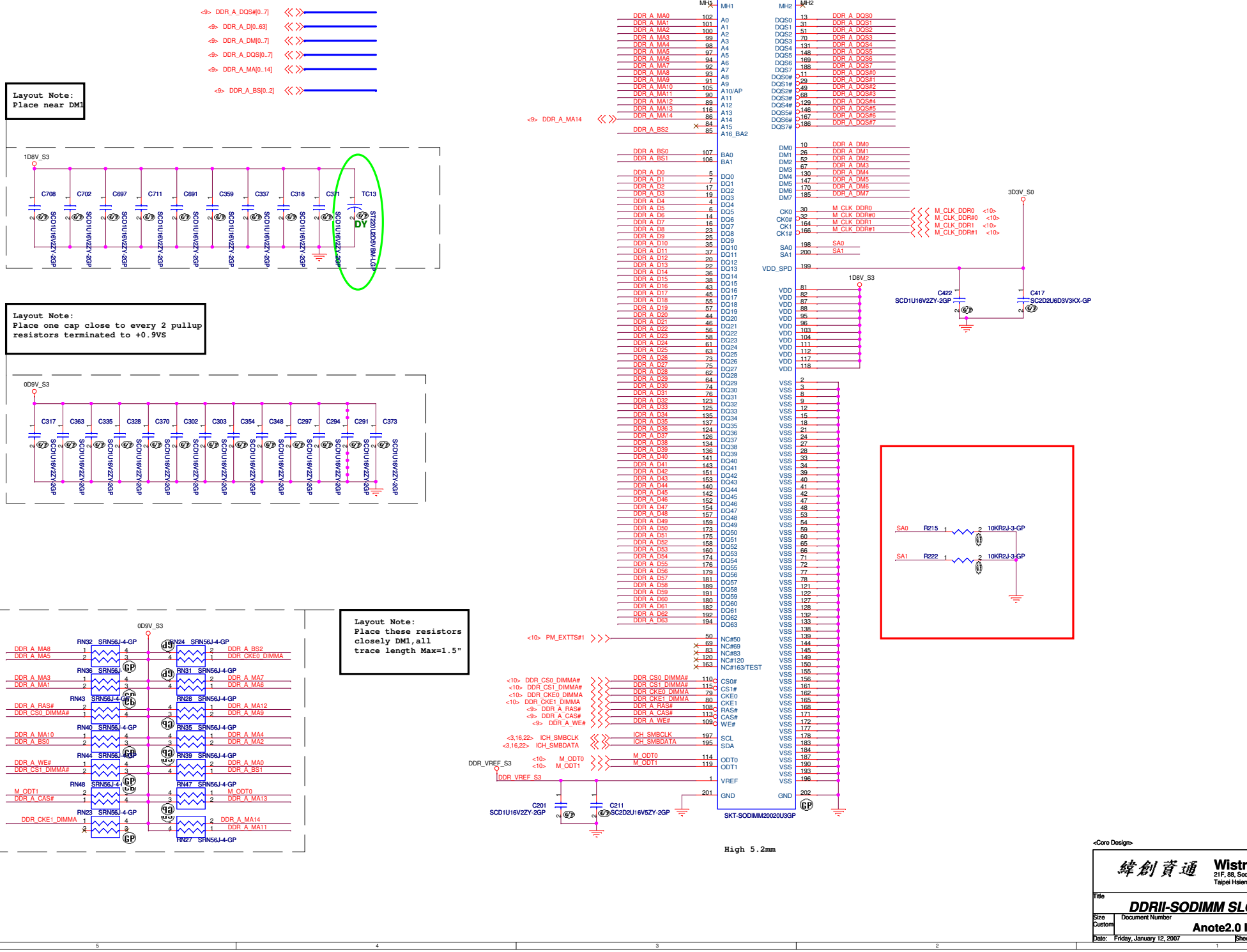

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Title: DDRII-SODIMM SLOT1

Size: Custom | Document Number: Anote2.0 INTEL

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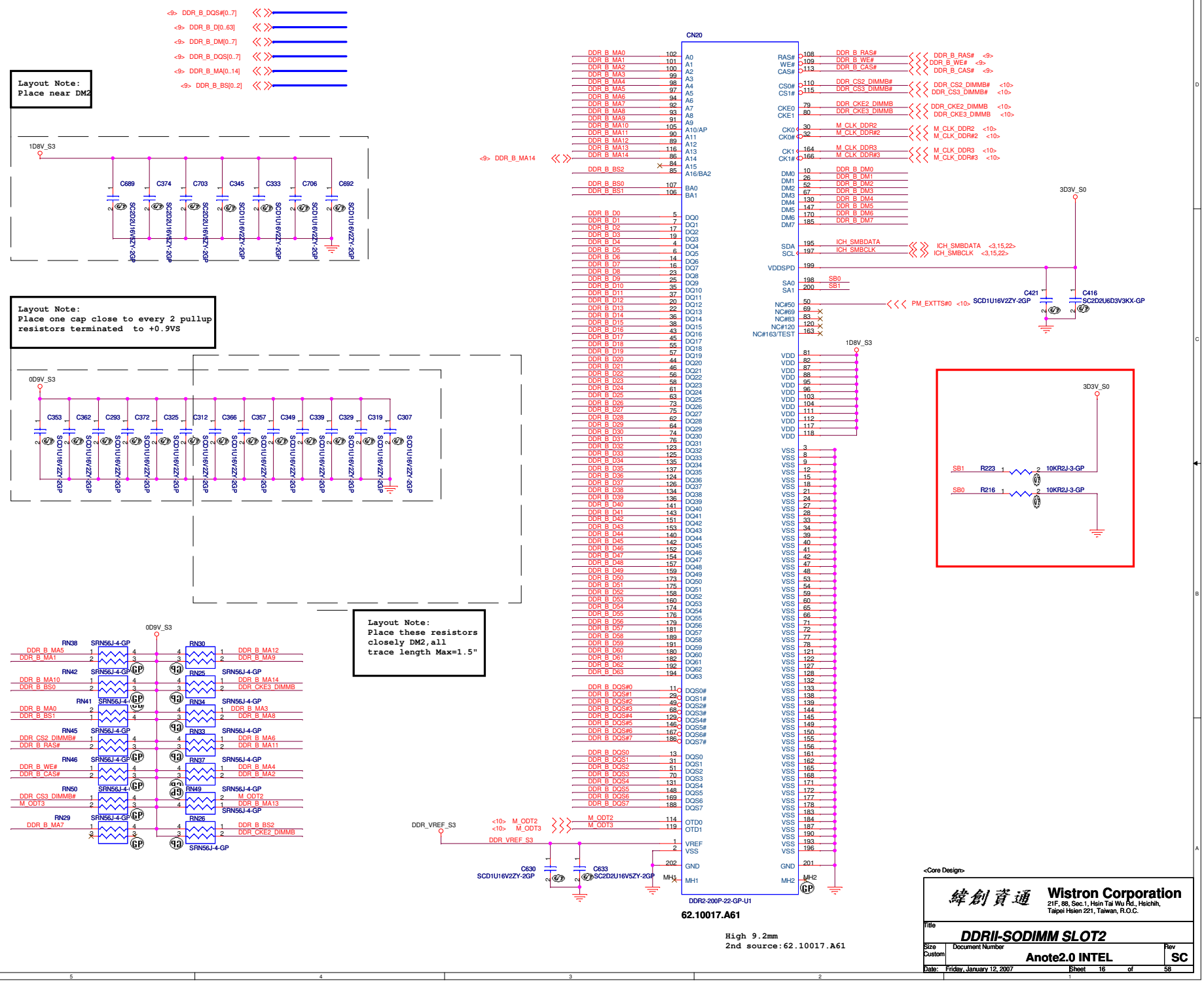
Layout Note:
Place near DM2
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS
Layout Note:
Place these resistors
closely DM2,all
trace length Max=1.5"
CN20
DDR2-200P-22-GP-U1
62.10017.A61
High 9.2mm
2nd source:62.10017.A61
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DDRII-SODIMM SLOT2
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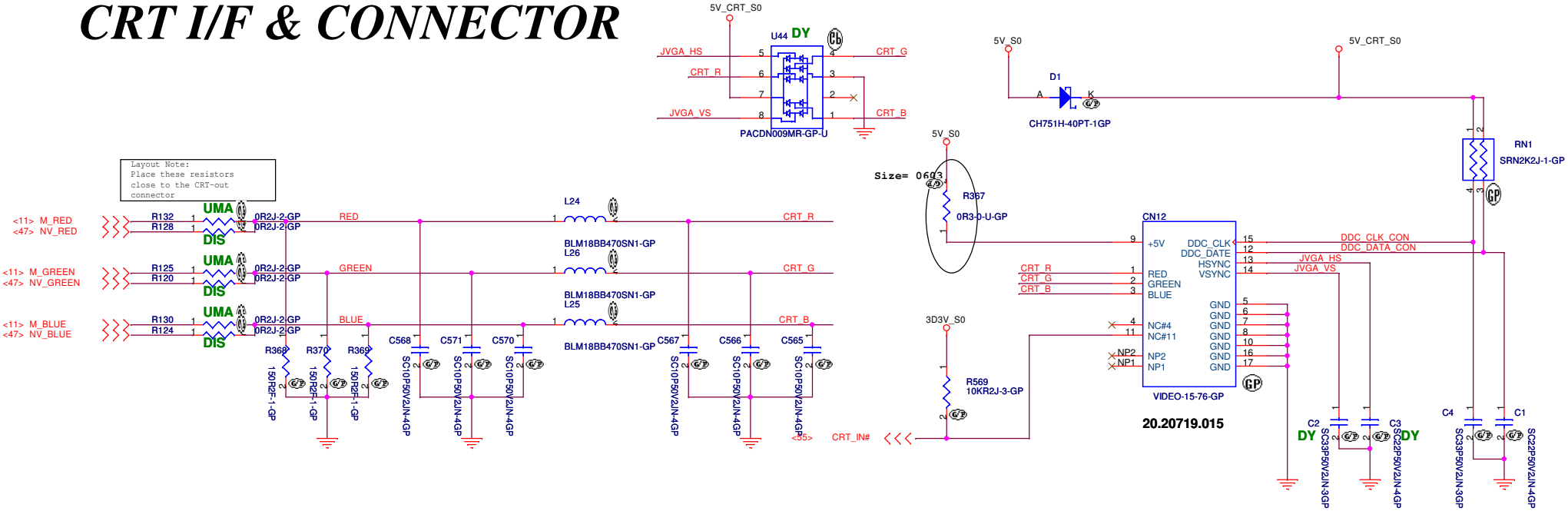
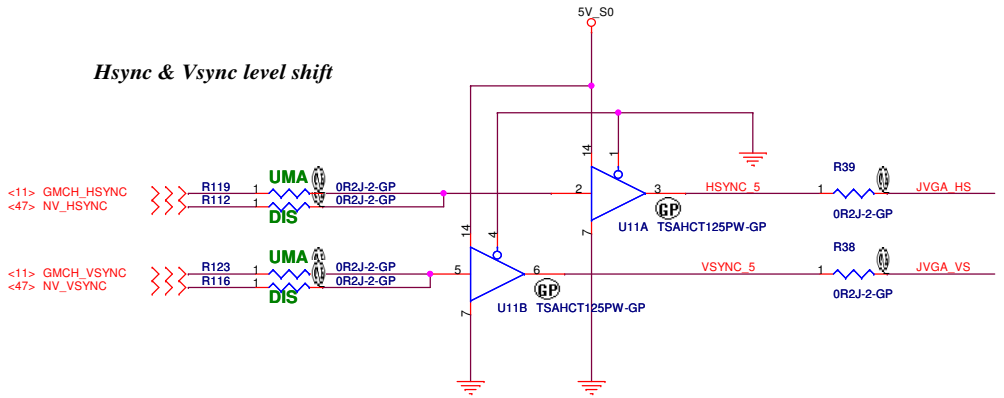
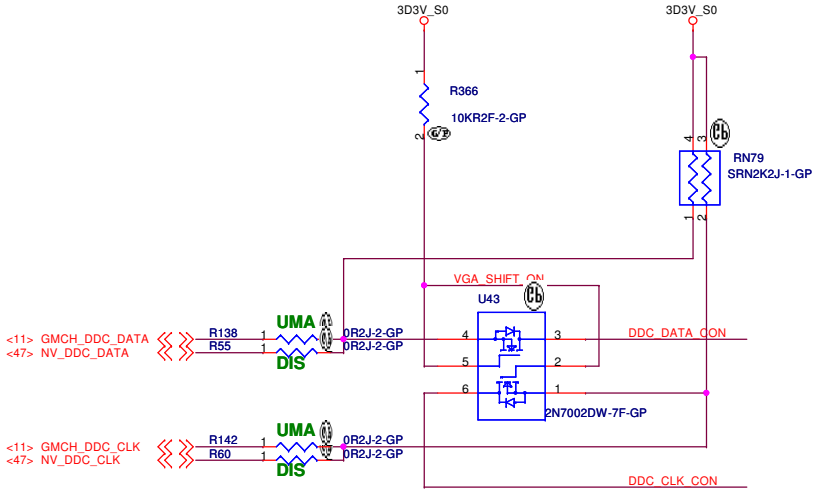
CRT I/F & CONNECTOR



Layout Note:
** Must be a ground return path between this ground and the ground on the VGA connector.*
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift





<Core Design>

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Title: CRT Connector

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TV OUT PORT

<57> TV_LUMA
<57> TV_CRMA

<11> M_CRMA
<47> NV_CRMA

R145 UMA
R64 DIS
0R2J-2-GP
0R2J-2-GP
TV_CRMA_R
R372
150R2F-1-GP
L28
BLM18BB470SN1-GP
C572
SC10P50V2JN-4GP
C573
SC10P50V2JN-4GP

TV_LUMA
TV_CRMA

CN14
GND
GND
LUMA
CRMA
GND
GND
MINDIN4-41-GP

22.10021.J11

<11> M_LUMA
<47> NV_LUMA

R143 UMA
R62 DIS
0R2J-2-GP
0R2J-2-GP
TV_LUMA_R
R373
150R2F-1-GP
L27
BLM18BB470SN1-GP
C575
SC10P50V2JN-4GP
C574
SC10P50V2JN-4GP

Place this 2 resistors close to the TV-out connector

D14
3D3V_S0
TV_LUMA
DY
BAV99-7-F-GP
C6
SCD1U16V2ZY-2GP
DY

D3
3D3V_S0
TV_CRMA
DY
BAV99-7-F-GP
C7
SCD1U16V2ZY-2GP
DY

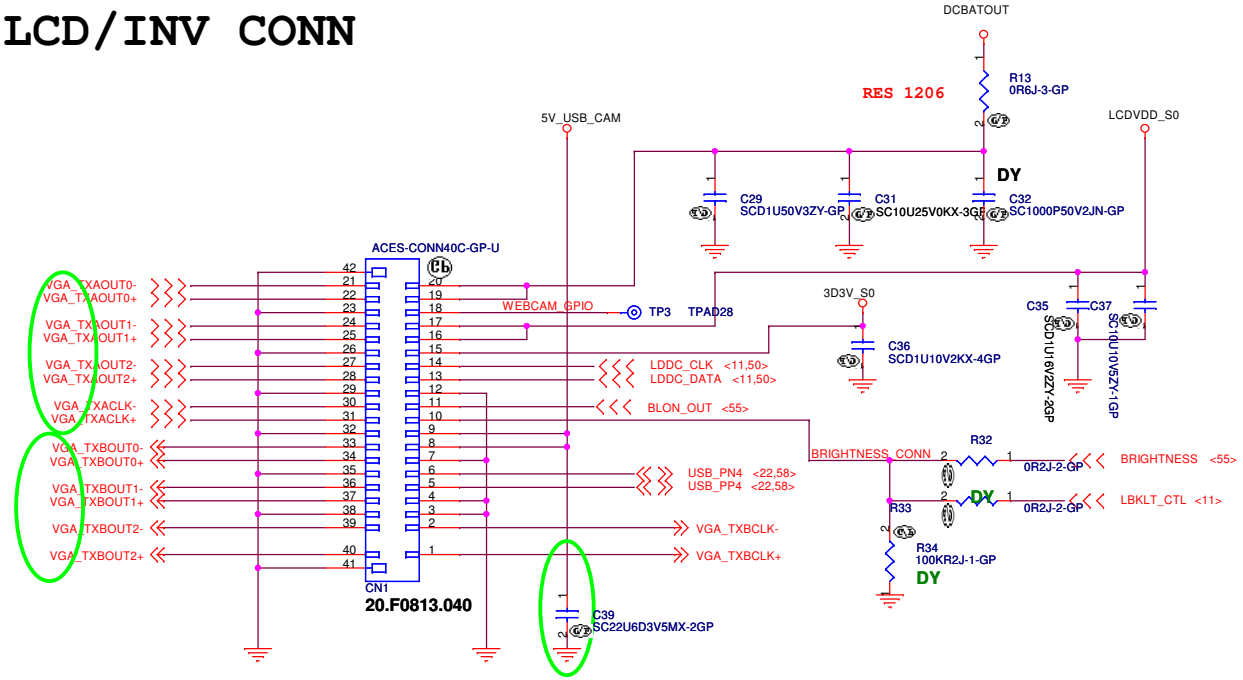
<Core Design>

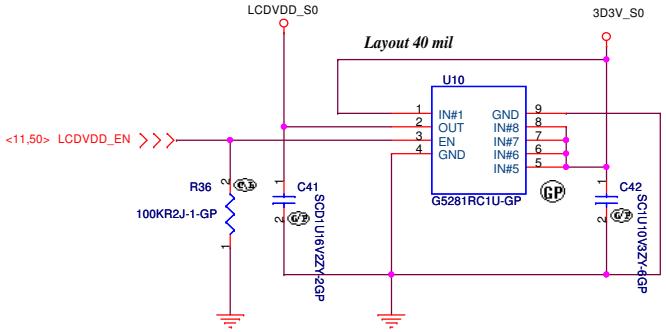
緯創資通 Wistron Corpor
21F, 88, Sec.1, Hsin Tai Wu Rd., H
Taipei Hsien 221, Taiwan, R.O.C.

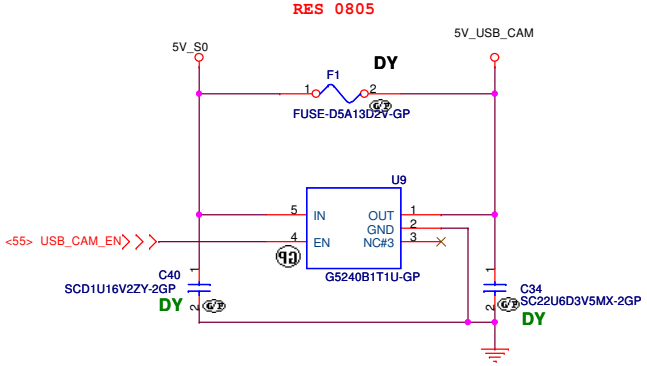
Title: TV Connector
Size: A4
Document Number: Anote2.0 INTEL
Date: Friday, January 12, 2007
Sheet 18 of

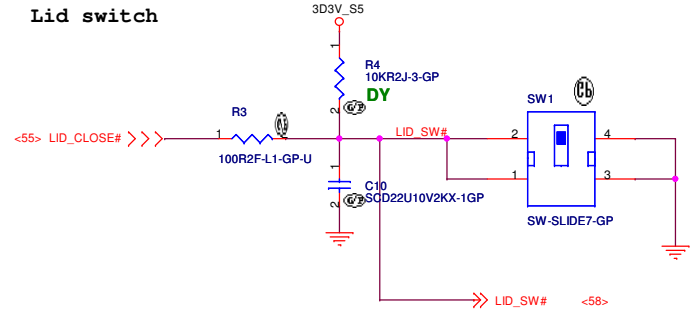
LED / INVERTER INTERFACE

LCD/INV CONN

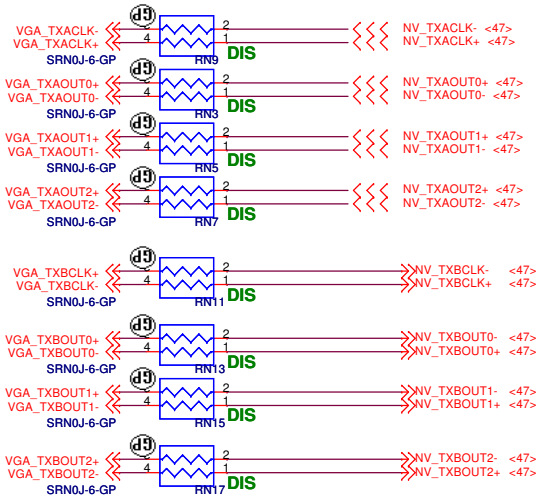




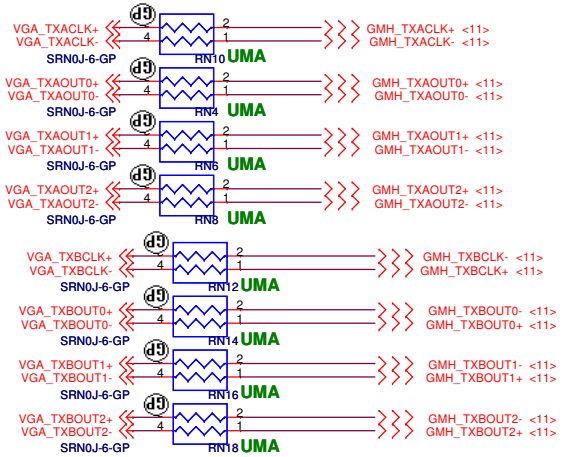




ATI LVDS INTERFACE



UMA LVDS INTERFACE



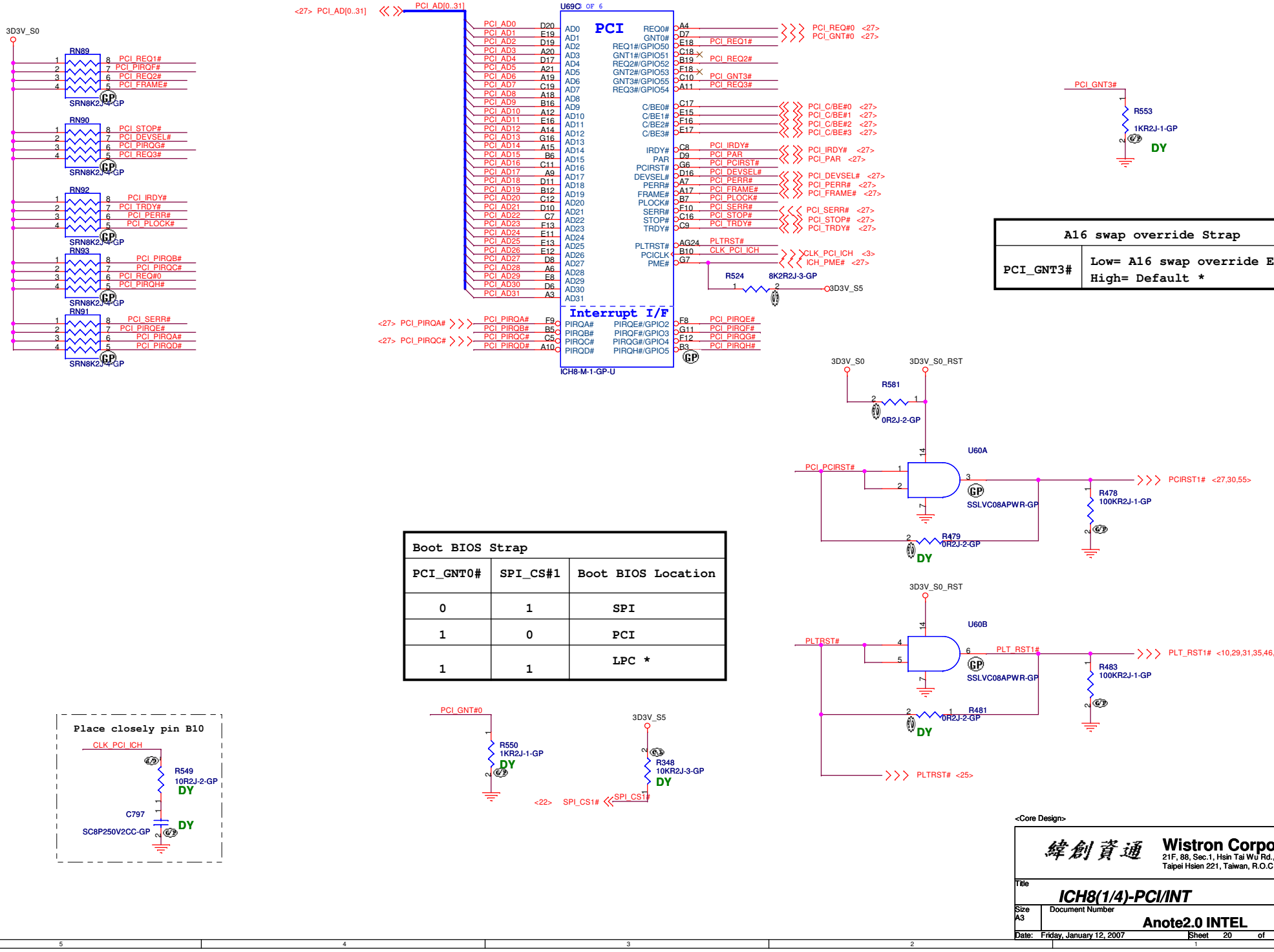
<Core Design>

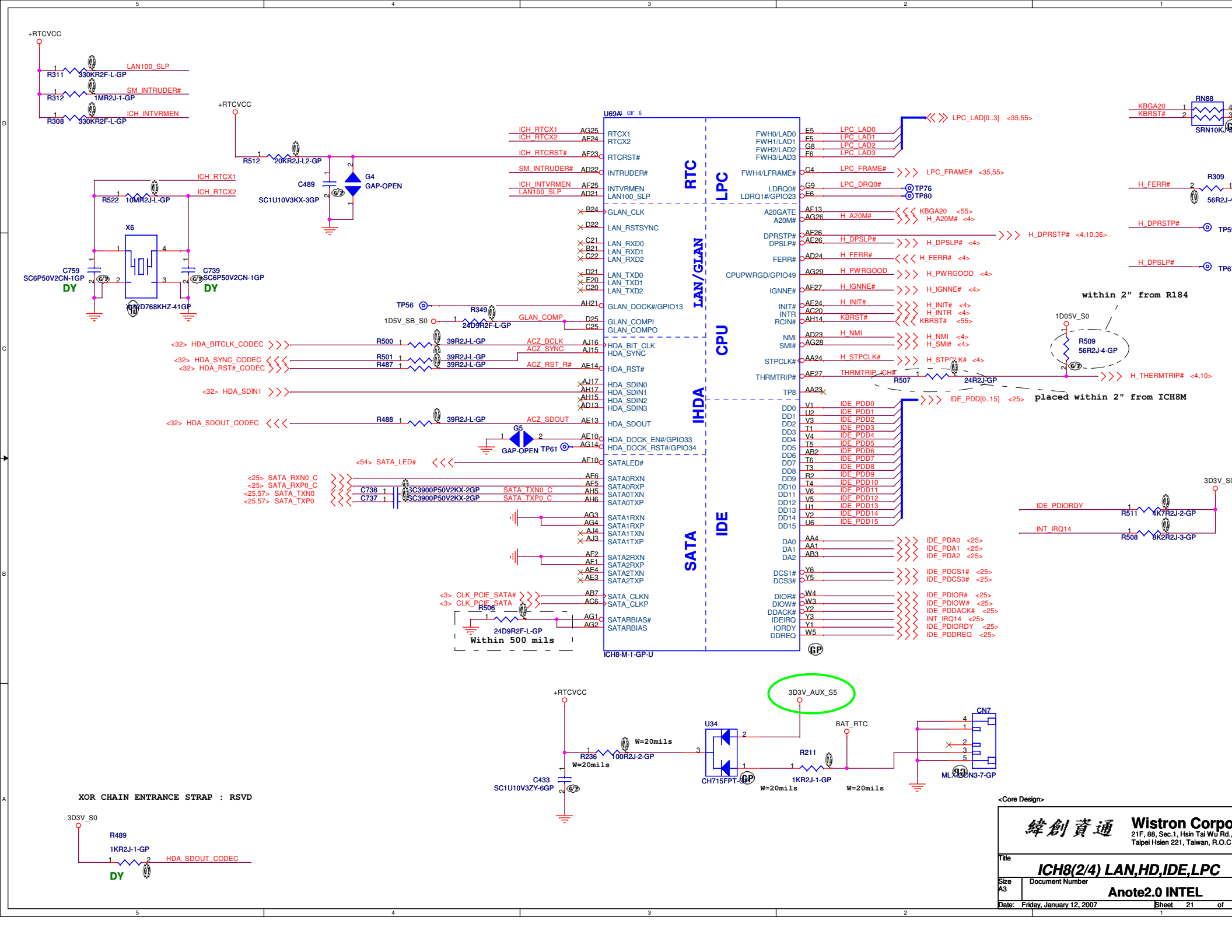
緯創資通 Wistron Corpor
21F, 88, Sec.1, Hsin Tai Wu Rd., H
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD/Inverter Connector

Size: A3 | Document Number: Anote2.0 INTEL

Date: Friday, January 12, 2007 | Sheet 19 of


3D3V_S0
RN89
PCI_REQ1#
PCI_PIRQF#
PCI_REQ2#
PCI_FRAME#
SRN8K2J-4-GP
RN90
PCI_STOP#
PCI_DEVSEL#
PCI_PIRQG#
PCI_REQ3#
RN92
PCI_IRDY#
PCI_TRDY#
PCI_PERR#
PCI_PLOCK#
RN93
PCI_PIRQB#
PCI_PIRQC#
PCI_REQ#0
PCI_PIRQH#
RN91
PCI_SERR#
PCI_PIRQE#
PCI_PIRQA#
PCI_PIRQD#
<27> PCI_AD[0..31]
PCI_AD[0..31]
U69C OF 6
PCI
Interrupt I/F
ICH8-M-1-GP-U
PCI_REQ#0 <27>
PCI_GNT#0 <27>
PCI_REQ1#
PCI_REQ2#
PCI_GNT3#
PCI_REQ3#
PCI_C/BE#0 <27>
PCI_C/BE#1 <27>
PCI_C/BE#2 <27>
PCI_C/BE#3 <27>
PCI_IRDY# <27>
PCI_PAR <27>
PCI_PCIRST#
PCI_DEVSEL# <27>
PCI_PERR# <27>
PCI_FRAME# <27>
PCI_PLOCK#
PCI_SERR# <27>
PCI_STOP# <27>
PCI_TRDY# <27>
PLTRST#
CLK_PCI_ICH <3>
ICH_PME# <27>
R524 8K2R2J-3-GP
3D3V_S5
<27> PCI_PIRQA#
<27> PCI_PIRQC#
PCI_PIRQE#
PCI_PIRQF#
PCI_PIRQG#
PCI_PIRQH#
PCI_GNT3#
R553
1KR2J-1-GP
DY
A16 swap override Strap
PCI_GNT3#
Low= A16 swap override E
High= Default *
3D3V_S0
3D3V_S0_RST
R581
0R2J-2-GP
U60A
PCI_PCIRST#
SSLVC08APWR-GP
PCIRST1# <27,30,55>
R478
100KR2J-1-GP
R479
0R2J-2-GP
DY
U60B
PLTRST#
PLT_RST1#
PLT_RST1# <10,29,31,35,46,
R483
100KR2J-1-GP
R481
0R2J-2-GP
PLTRST# <25>
Boot BIOS Strap
PCI_GNT0#
SPI_CS#1
Boot BIOS Location
0
1
SPI
1
0
PCI
1
1
LPC *
PCI_GNT#0
R550
1KR2J-1-GP
3D3V_S5
R348
10KR2J-3-GP
<22> SPI_CS1#
SPI_CS1#
Place closely pin B10
CLK_PCI_ICH
R549
10R2J-2-GP
C797
SC8P250V2CC-GP
<Core Design>
緯創資通
Wistron Corpo
21F, 88, Sec.1, Hsin Tai Wu Rd.,
Taipei Hsien 221, Taiwan, R.O.C
Title
ICH8(1/4)-PCI/INT
Size
A3
Document Number
Anote2.0 INTEL
Date: Friday, January 12, 2007
Sheet 20 of



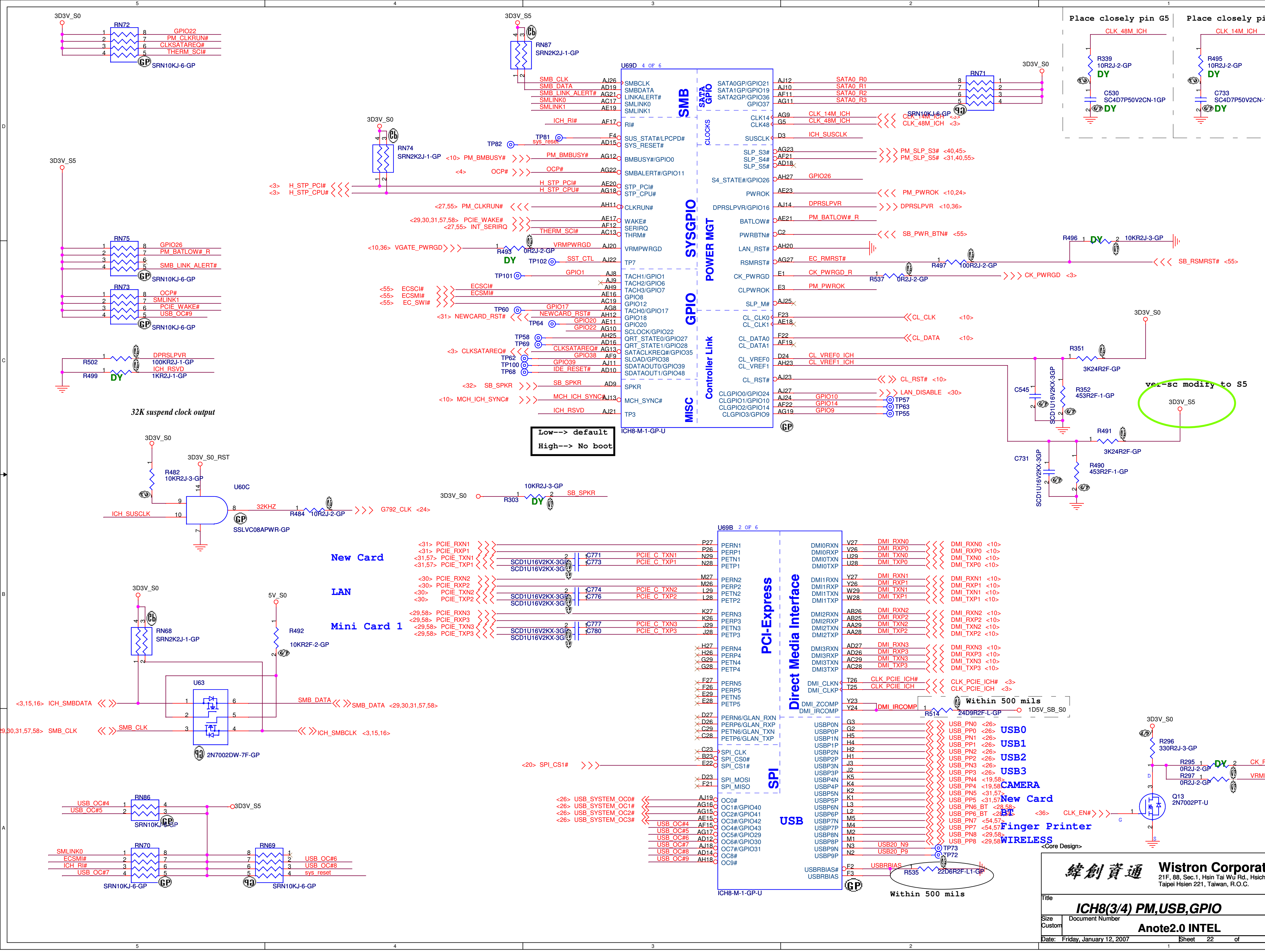
<Core Design>

緯創資通 Wistron Corpo
21F, 88, Sec.1, Hsin Tai Wu Rd.,
Taipei Hsien 221, Taiwan, R.O.C

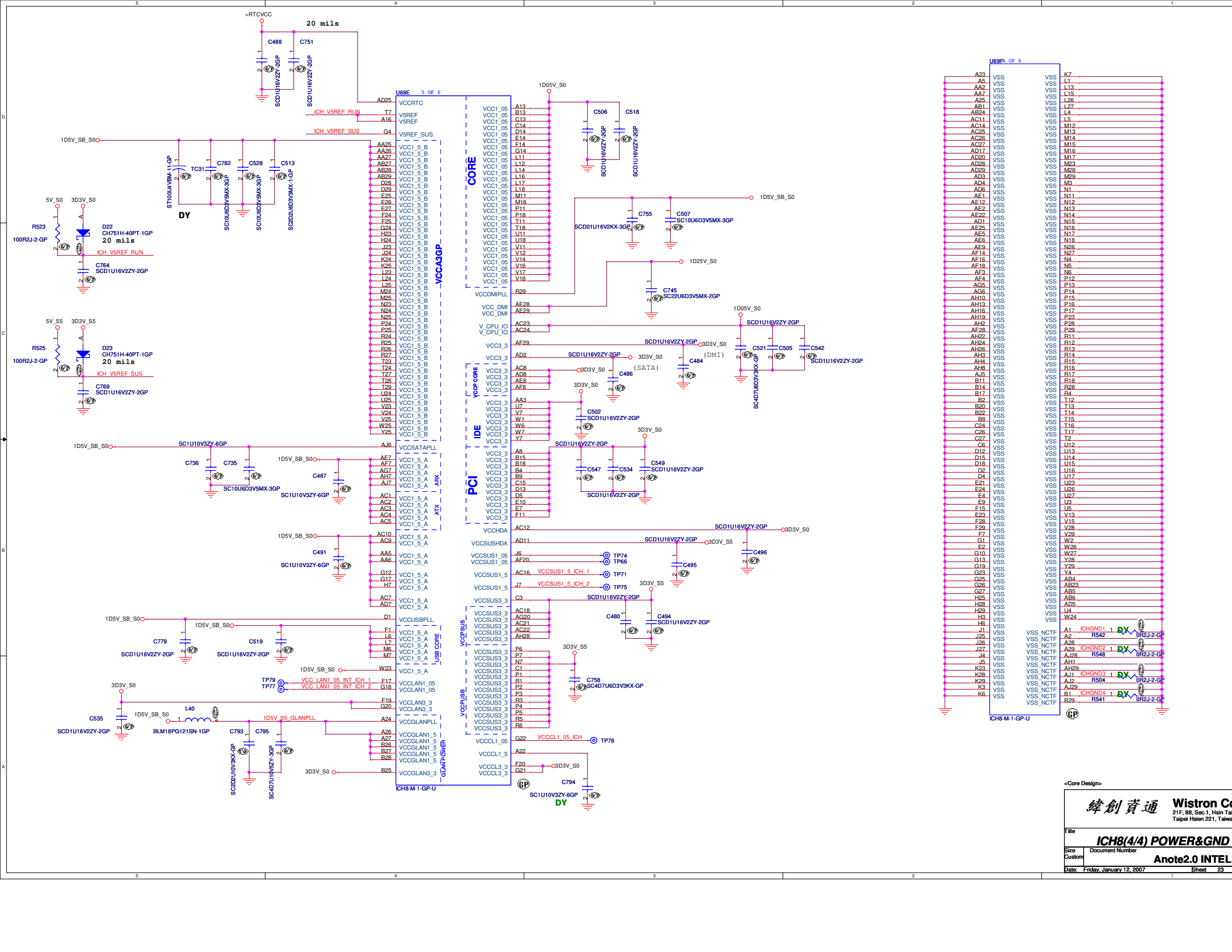
Title: ICH8(2/4) LAN,HD,IDE,LPC

Size: A3 | Document Number: Anote2.0 INTEL

Date: Friday, January 12, 2007 | Sheet 21 of



32K suspend clock output
Low--> default
High--> No boot
ver-sc modify to S5
New Card
LAN
Mini Card 1
Within 500 mils
Place closely pin G5
SMB
SATA GPIO
CLOCKS
SYSGPIO
POWER MGT
GPIO
Controller Link
MISC
PCI-Express
Direct Media Interface
SPI
USB
USB0
USB1
USB2
USB3
CAMERA
New Card
BT
Finger Printer
WIRELESS
ICH8-M-1-GP-U
U69D 4 OF 6
U69B 2 OF 6
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH8(3/4) PM,USB,GPIO
Size Custom
Document Number
Anote2.0 INTEL
Date: Friday, January 12, 2007
Sheet 22 of



<Core Design>

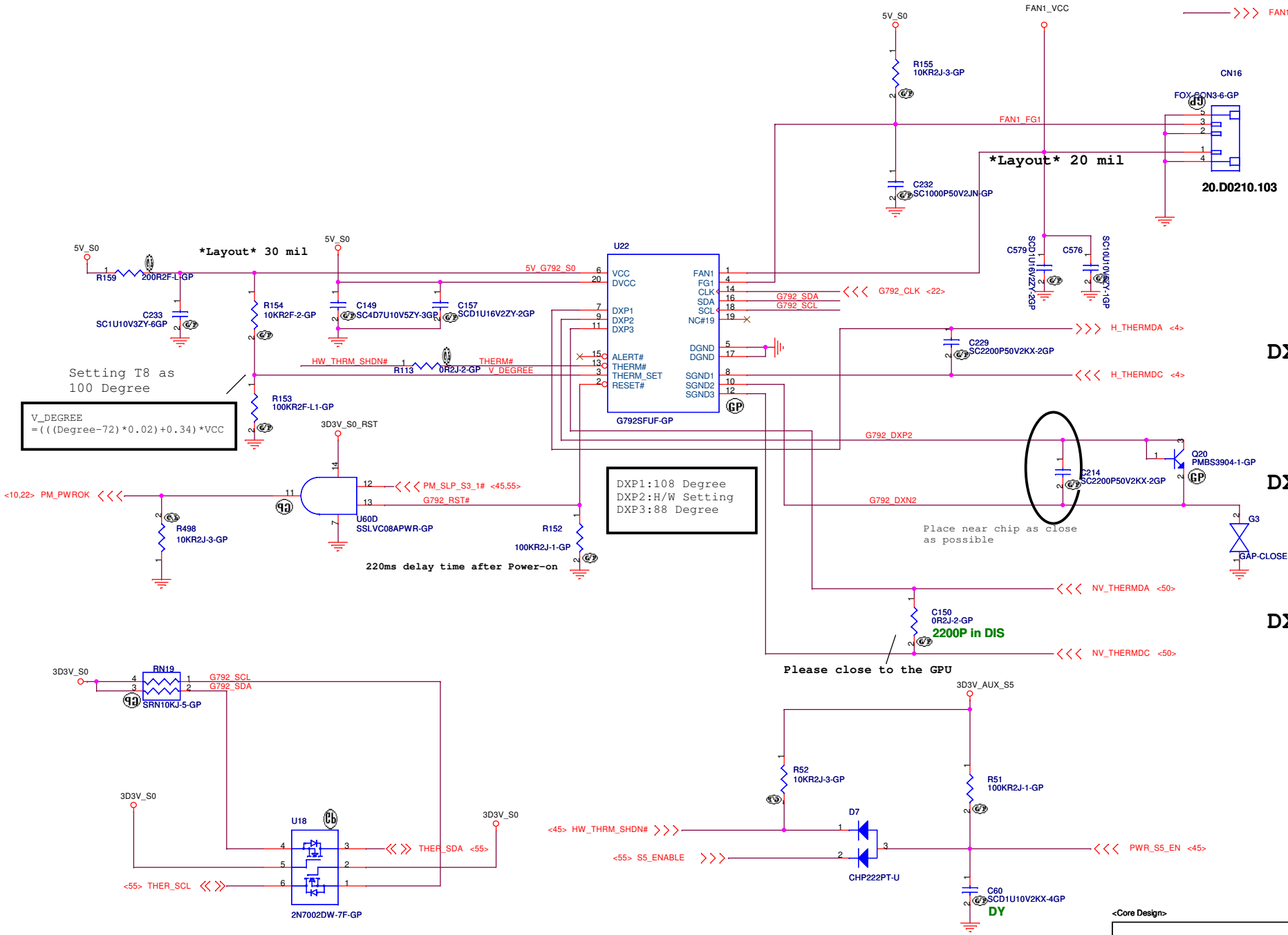
緯創資通 Wistron Co

21F, 88, Sec.1, Hsin Tai
Taipei Hsien 221, Taiwa

Title: ICH8(4/4) POWER&GND

Size: Custom | Document Number: Anote2.0 INTEL

Date: Friday, January 12, 2007 | Sheet 23



<Core Design>

緯創資通 Wistron Corp

21F, 88, Sec.1, Hsin Tai Wu R
Taipei Hsien 221, Taiwan, R.O

Title

Thermal/Fan Controllor G7

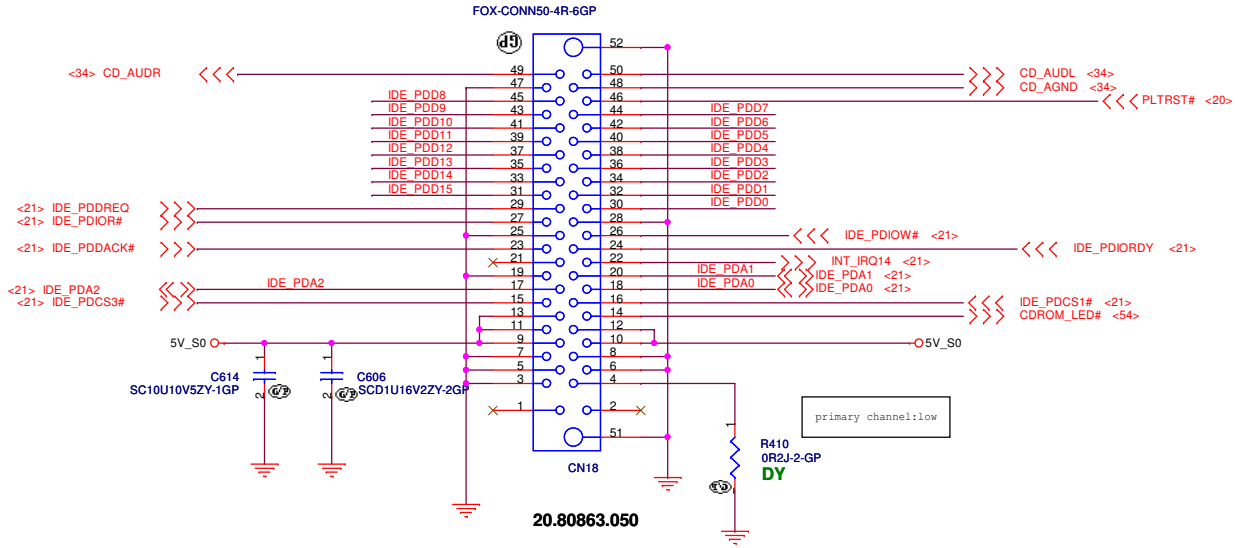
Size	Document Number	
Custom		Anote2.0 INTEL

Date: Friday, January 12, 2007 Sheet 24 of

CD-ROM CONNECTOR

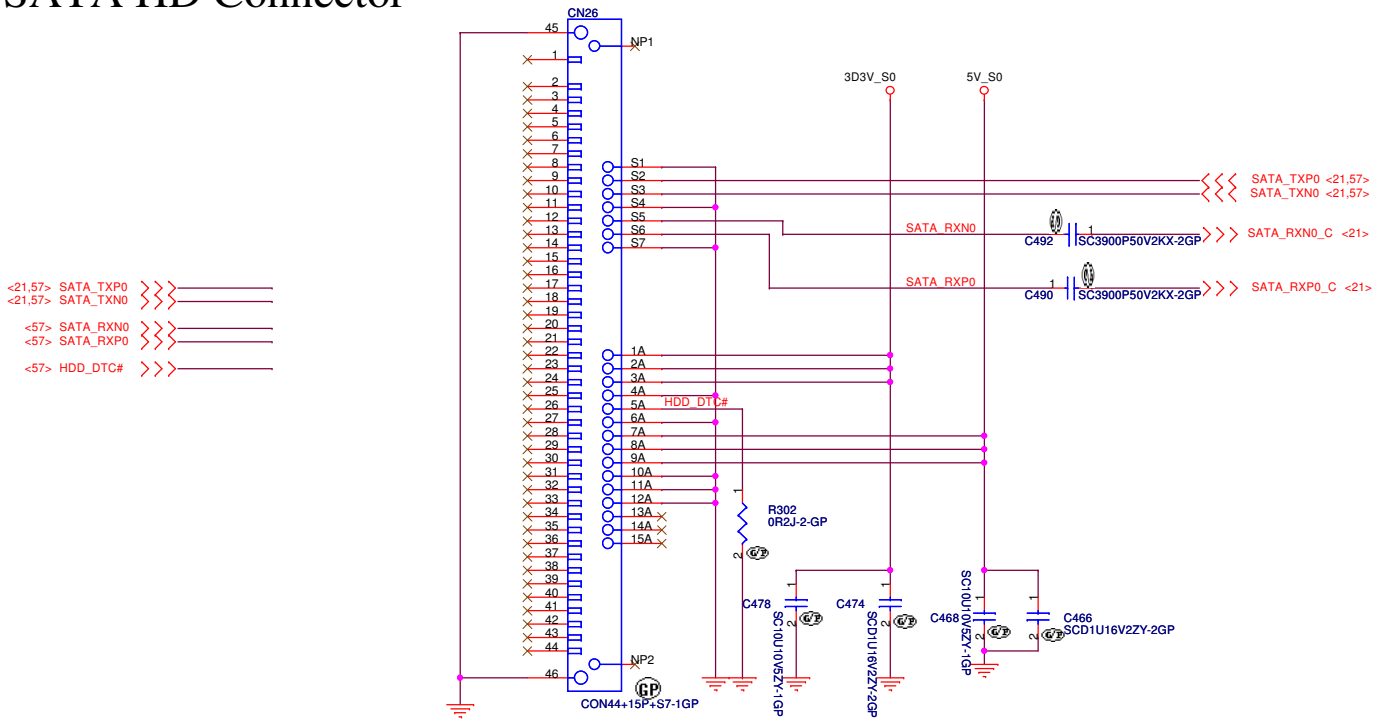
IDE_PDD[0..15] <21>

Lab1 20.80346.050
Lab2 20.80863.050



20.80863.050

SATA HD Connector



20.F0883.001

<Core Design>

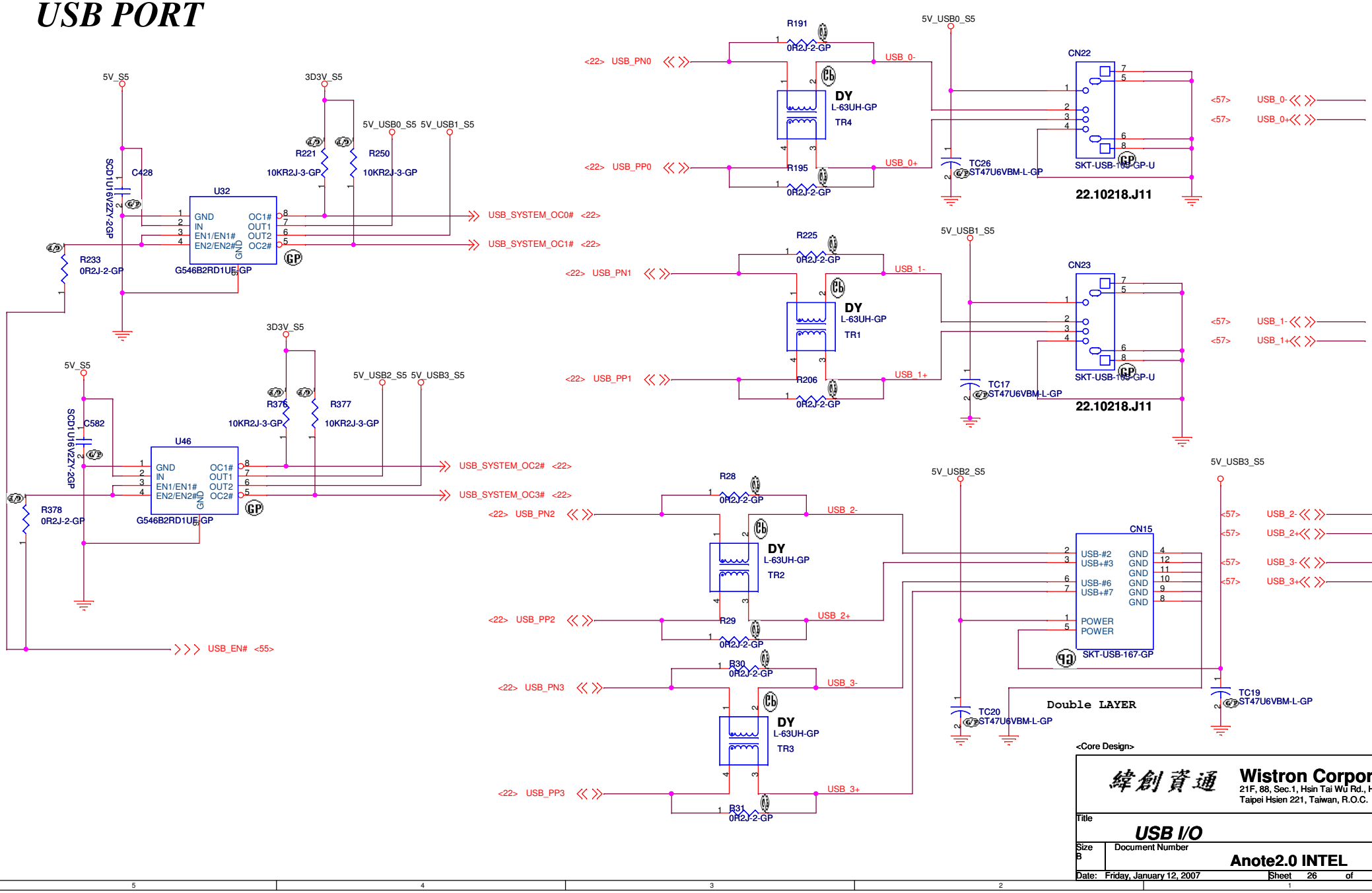
緯創資通 Wistron Corp
21F, 88, Sec.1, Hsin Tai Wu R
Taipei Hsien 221, Taiwan, R.O

Title: HD/CDROM/USB

Size: A3 | Document Number: Anote2.0 INTEL

Date: Friday, January 12, 2007 | Sheet 25 of

USB PORT



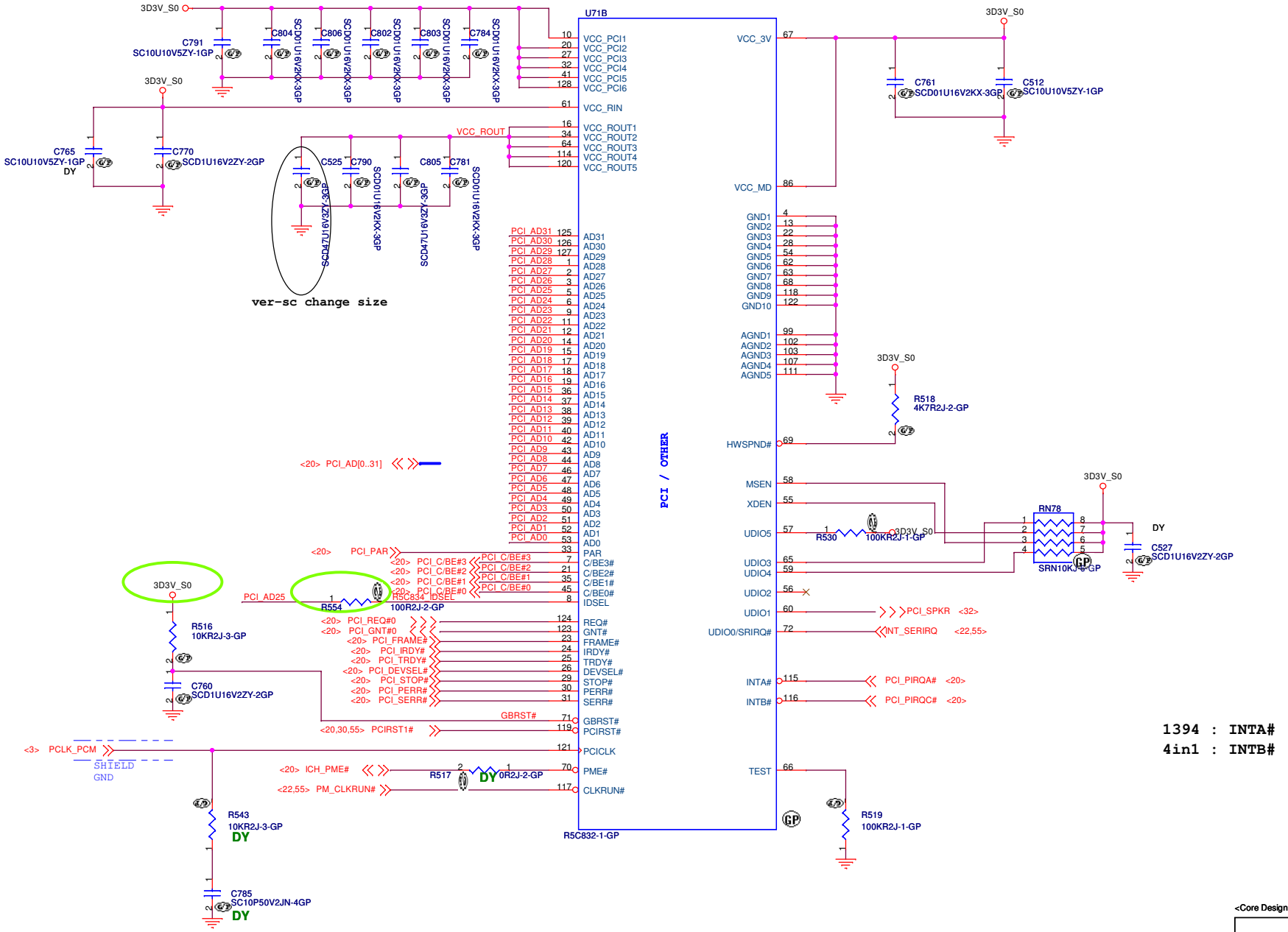
<Core Design>

緯創資通 Wistron Corpor
21F, 88, Sec.1, Hsin Tai Wu Rd., H
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB I/O**

Size: B | Document Number: **Anote2.0 INTEL**

Date: Friday, January 12, 2007 | Sheet 26 of



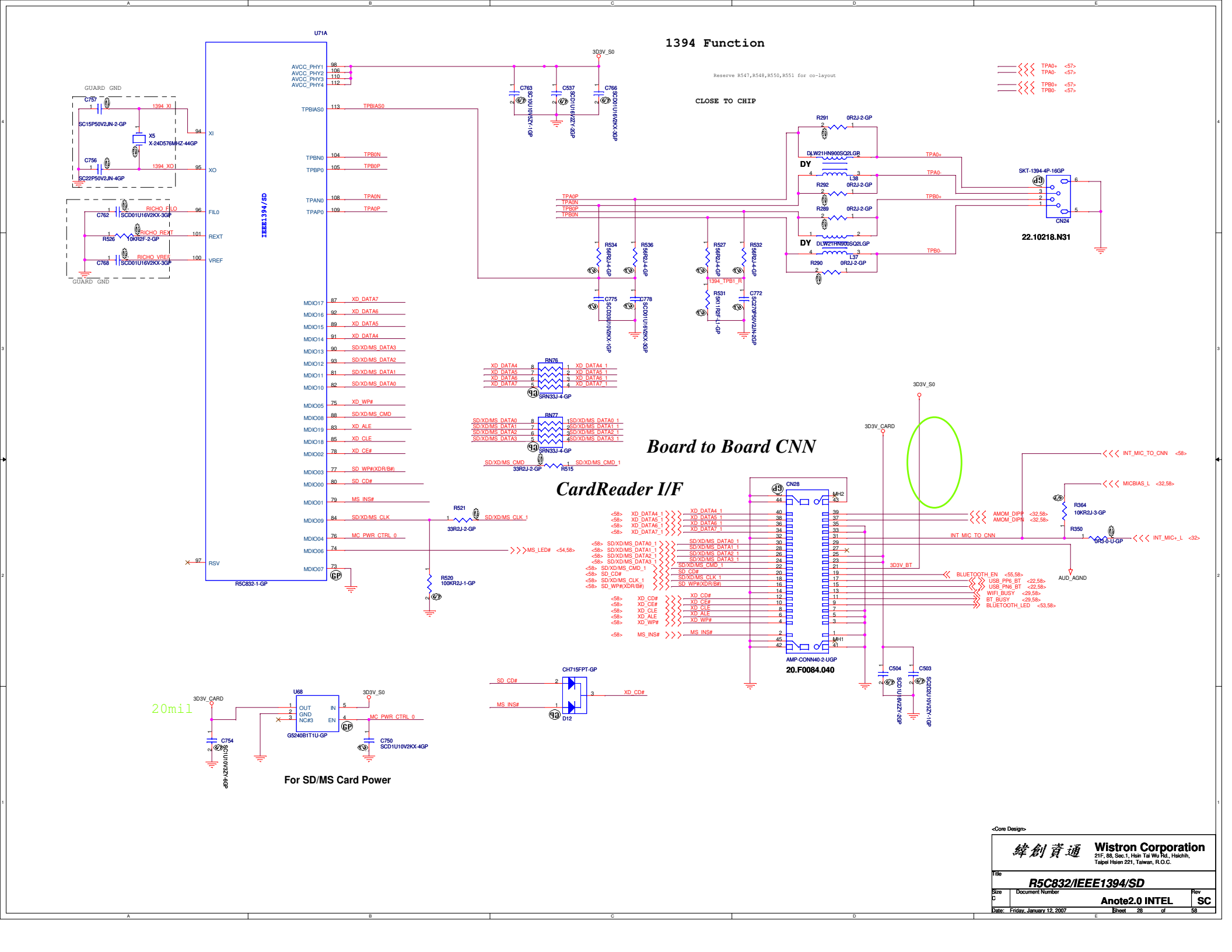
<Core Design>

Wistron Corp
21F, 88, Sec.1, Hsin Tai Wu R
Taipei Hsien 221, Taiwan, R.O

Title: R5C832/PCI

Size: A3 | Document Number: Anote2.0 INTEL

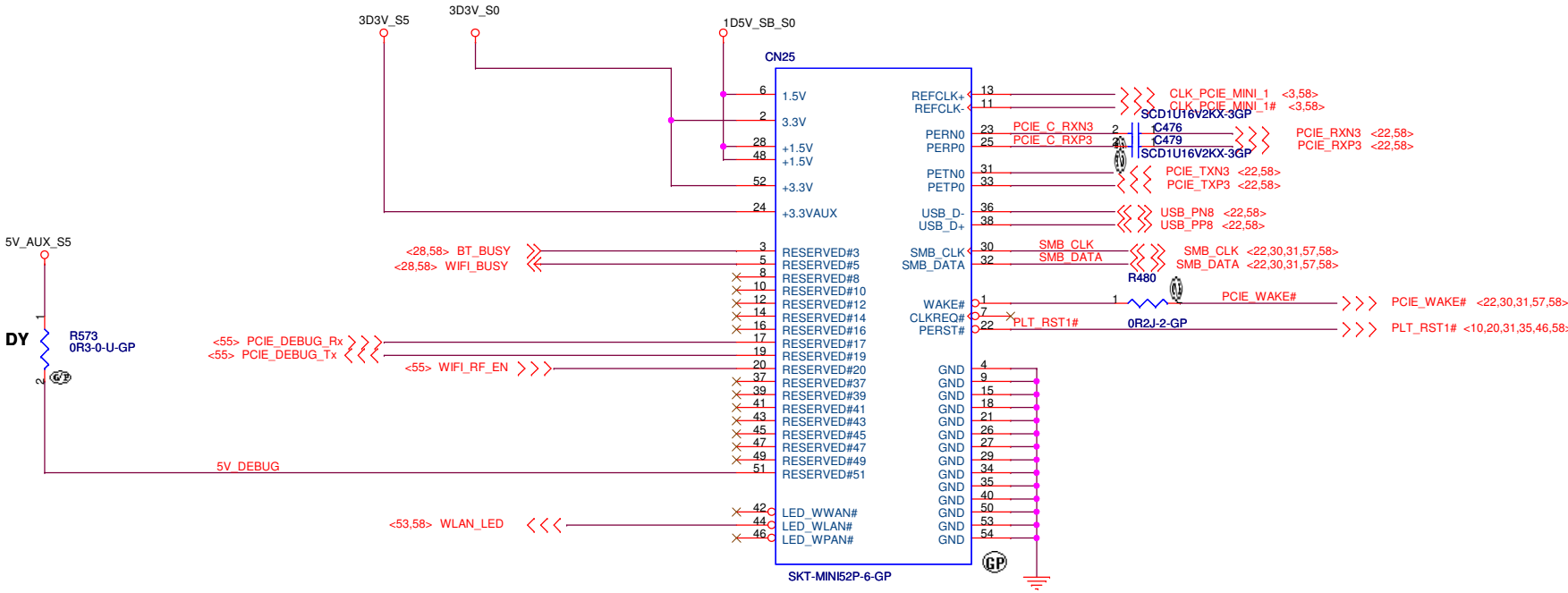
Date: Friday, January 12, 2007 | Sheet 27 of


1394 Function
Reserve R547,R548,R550,R551 for co-layout
CLOSE TO CHIP
U71A
IEEE1394/SD
R5C832-1-GP
Board to Board CNN
CardReader I/F
CN28
AMP-CONN40-2-UGP
20.F0084.040
22.10218.N31
SKT-1394-4P-16GP
CN24
CH715FPT-GP
D12
G5240B1T1U-GP
For SD/MS Card Power
20mil
DY
3D3V_S0
3D3V_CARD
AUD_AGND
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
R5C832/IEEE1394/SD
Anote2.0 INTEL
Friday, January 12, 2007

Mini PCI-E Connector

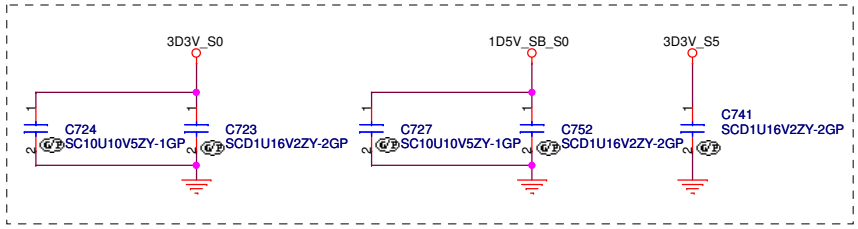
Port-1

Only port-1 support USB



62.10043.261

Note: 9/5 ME updata



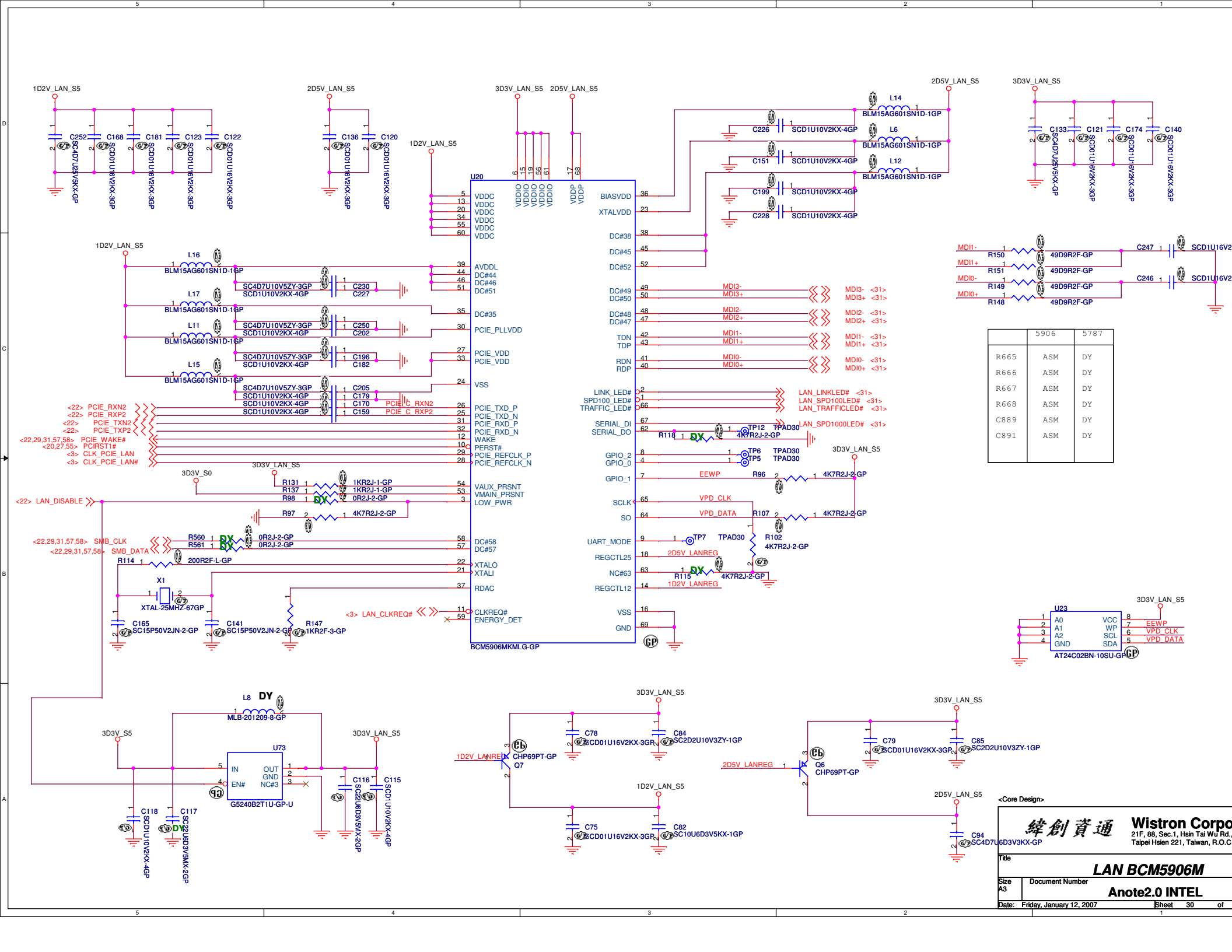
<Core Design>

緯創資通 Wistron Corpor
21F, 88, Sec.1, Hsin Tai Wu Rd., H
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINI CARD CONN .

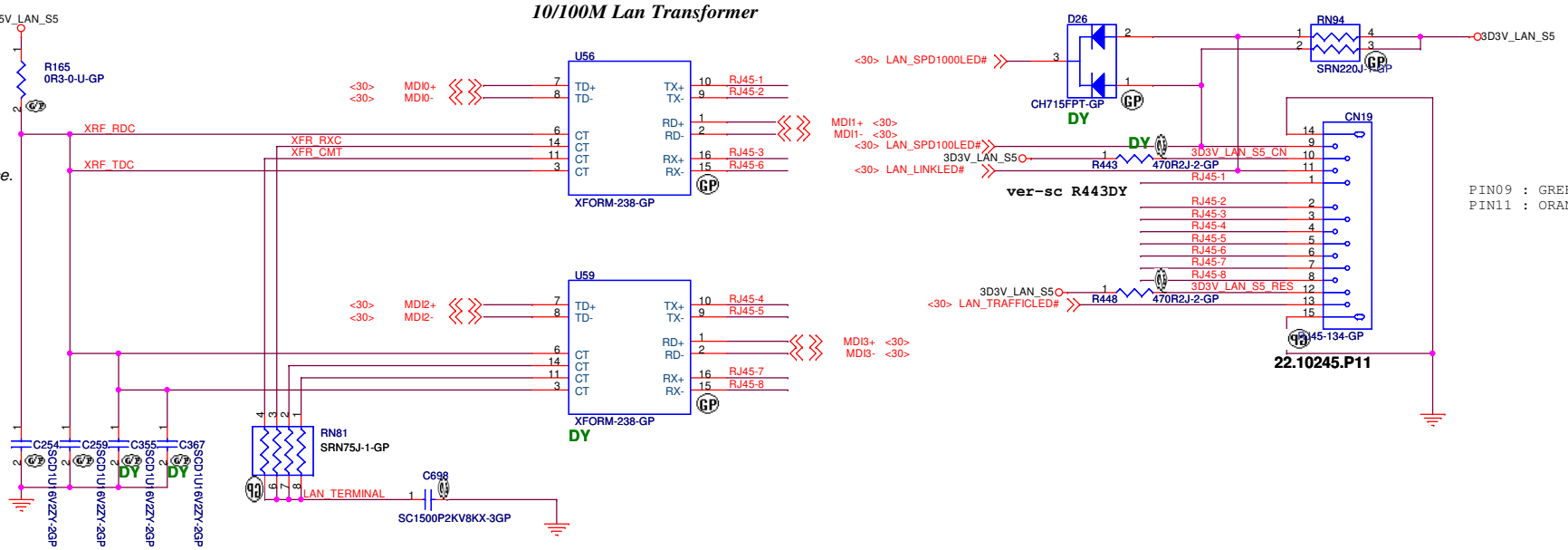
Size: B | Document Number: Anote2.0 INTEL

Date: Friday, January 12, 2007 | Sheet 29 of


1D2V_LAN_S5
2D5V_LAN_S5
3D3V_LAN_S5
U20
BCM5906MKMLG-GP
VDDC
AVDDL
DC#44
DC#46
DC#51
DC#35
PCIE_PLLVDD
PCIE_VDD
VSS
PCIE_TXD_P
PCIE_TXD_N
PCIE_RXD_P
PCIE_RXD_N
WAKE
PERST#
PCIE_REFCLK_P
PCIE_REFCLK_N
VAUX_PRSNT
VMAIN_PRSNT
LOW_PWR
DC#58
DC#57
XTALO
XTALI
RDAC
CLKREQ#
ENERGY_DET
BIASVDD
XTALVDD
DC#38
DC#45
DC#52
DC#49
DC#50
DC#48
DC#47
TDN
TDP
RDN
RDP
LINK_LED#
SPD100_LED#
TRAFFIC_LED#
SERIAL_DI
SERIAL_DO
GPIO_2
GPIO_0
GPIO_1
SCLK
SO
UART_MODE
REGCTL25
NC#63
REGCTL12
VSS
GND
L14
BLM15AG601SN1D-1GP
L6
L12
C226
C151
C199
C228
SCD1U10V2KX-4GP
L16
L17
L11
L15
C230
C227
C250
C202
C196
C182
C205
C179
C170
C159
PCIE_C_RXN2
PCIE_C_RXP2
<22> PCIE_RXN2
<22> PCIE_RXP2
<22> PCIE_TXN2
<22> PCIE_TXP2
<22,29,31,57,58> PCIE_WAKE#
<20,27,55> PCIRST1#
<3> CLK_PCIE_LAN
<3> CLK_PCIE_LAN#
<22> LAN_DISABLE
R131
R137
R98
R97
1KR2J-1-GP
0R2J-2-GP
4K7R2J-2-GP
DY
<22,29,31,57,58> SMB_CLK
<22,29,31,57,58> SMB_DATA
R560
R561
R114
200R2F-L-GP
X1
XTAL-25MHZ-67GP
C165
C141
R147
SC15P50V2JN-2-GP
1KR2F-3-GP
<3> LAN_CLKREQ#
MDI3-
MDI3+
MDI2-
MDI2+
MDI1-
MDI1+
MDI0-
MDI0+
LAN_LINKLED# <31>
LAN_SPD100LED# <31>
LAN_TRAFFICLED# <31>
LAN_SPD1000LED# <31>
R118
TP12
TPAD30
TP6
TP5
EEWP
R96
VPD_CLK
VPD_DATA
R107
TP7
R102
2D5V_LANREG
R115
1D2V_LANREG
C133
C121
C174
C140
SC4D7U25V5KX-GP
SCD01U16V2KX-3GP
MDI1-
MDI1+
MDI0-
MDI0+
R150
R151
R149
R148
49D9R2F-GP
C247
C246
SCD1U16V2
5906
5787
R665 ASM DY
R666 ASM DY
R667 ASM DY
R668 ASM DY
C889 ASM DY
C891 ASM DY
U23
AT24C02BN-10SU-GP
A0
A1
A2
GND
VCC
WP
SCL
SDA
L8
MLB-201209-8-GP
U73
G5240B2T1U-GP-U
IN
EN#
OUT
GND
NC#3
C118
C117
C116
C115
SCD1U10V2KX-4GP
SC22U6D3V5MX-2GP
C78
C84
C75
C82
C79
C85
C94
SCD01U16V2KX-3GP
SC2D2U10V3ZY-1GP
SC10U6D3V5KX-1GP
SC4D7U6D3V3KX-GP
Q7
Q6
CHP69PT-GP
<Core Design>
緯創資通
Wistron Corpo
21F, 88, Sec.1, Hsin Tai Wu Rd.,
Taipei Hsien 221, Taiwan, R.O.C
Title
LAN BCM5906M
Size
A3
Document Number
Anote2.0 INTEL
Date: Friday, January 12, 2007
Sheet 30 of

10/100M Lan Transformer

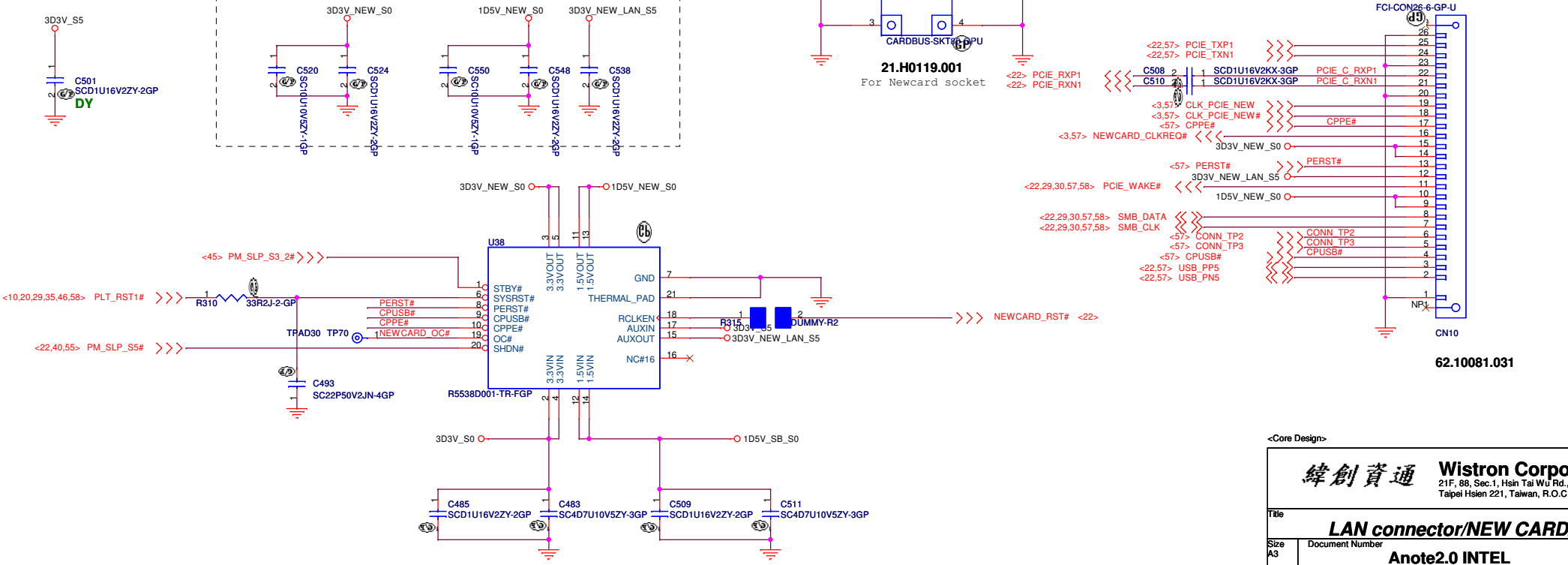
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.



NEWCARD Connector

Place them Near to Chip

Place them Near to Connector



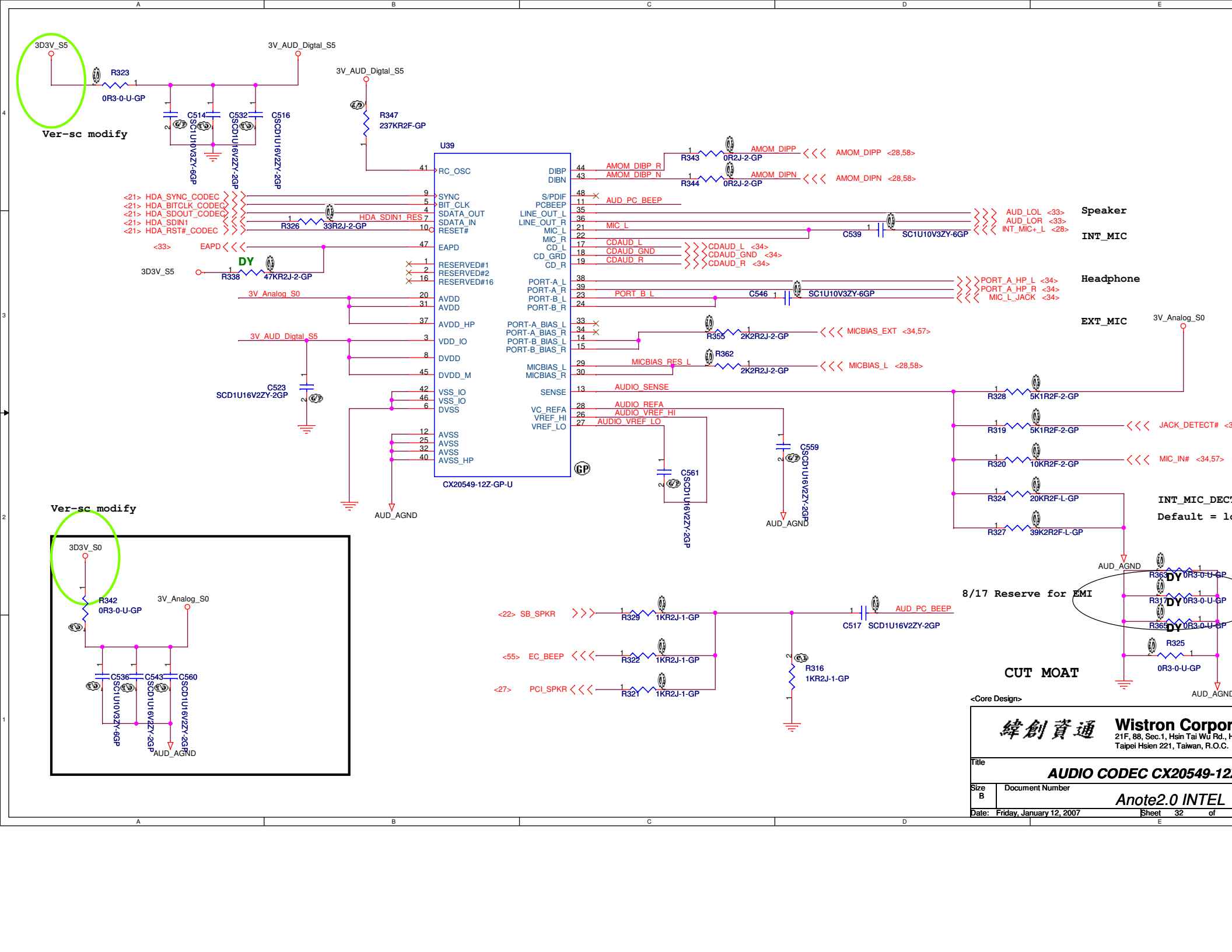
<Core Design>

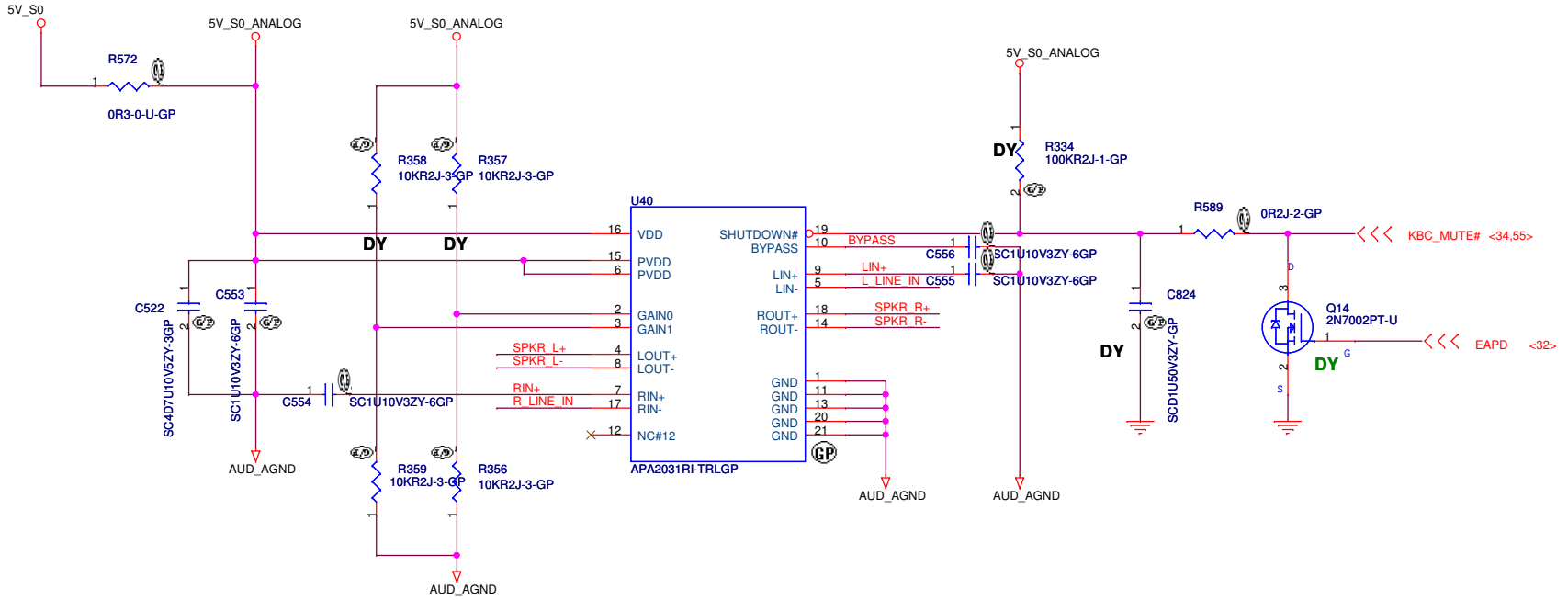
緯創資通 Wistron Corpo
21F, 88, Sec.1, Hsin Tai Wu Rd.,
Taipei Hsien 221, Taiwan, R.O.C

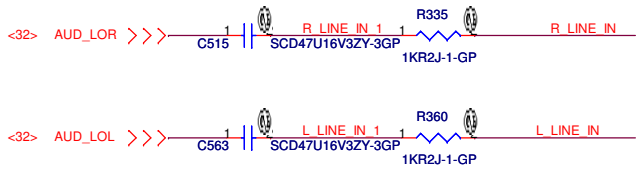
Title: LAN connector/NEW CARD

Size: A3 | Document Number: Anote2.0 INTEL

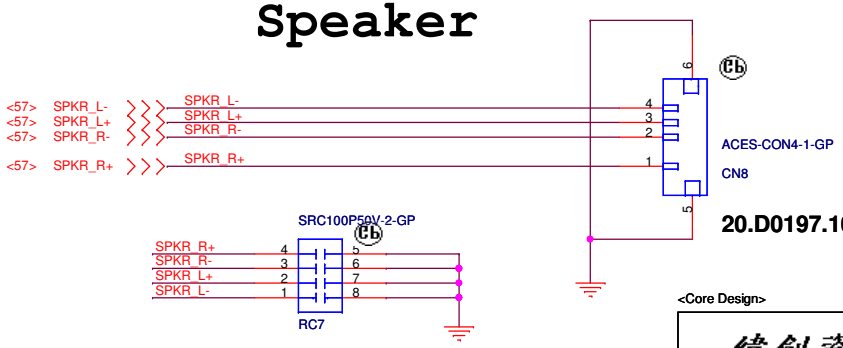
Date: Friday, January 12, 2007 | Sheet 31 of


3D3V_S5
3V_AUD_Digtal_S5
R323
0R3-0-U-GP
C514
SC1U10V3ZY-6GP
C532
SCD1U16V2ZY-2GP
C516
SCD1U16V2ZY-2GP
Ver-sc modify
R347
237KR2F-GP
U39
RC_OSC
SYNC
BIT_CLK
SDATA_OUT
SDATA_IN
RESET#
EAPD
RESERVED#1
RESERVED#2
RESERVED#16
AVDD
AVDD
AVDD_HP
VDD_IO
DVDD
DVDD_M
VSS_IO
VSS_IO
DVSS
AVSS
AVSS
AVSS
AVSS_HP
CX20549-12Z-GP-U
<21> HDA_SYNC_CODEC
<21> HDA_BITCLK_CODEC
<21> HDA_SDOUT_CODEC
<21> HDA_SDIN1
<21> HDA_RST#_CODEC
HDA_SDIN1_RES
R326
33R2J-2-GP
<33>
EAPD
DY
R338
47KR2J-2-GP
3V_Analog_S0
3V_AUD_Digtal_S5
C523
SCD1U16V2ZY-2GP
AUD_AGND
DIBP
DIBN
S/PDIF
PCBEEP
LINE_OUT_L
LINE_OUT_R
MIC_L
MIC_R
CD_L
CD_GRD
CD_R
PORT-A_L
PORT-A_R
PORT-B_L
PORT-B_R
PORT-A_BIAS_L
PORT-A_BIAS_R
PORT-B_BIAS_L
PORT-B_BIAS_R
MICBIAS_L
MICBIAS_R
SENSE
VC_REFA
VREF_HI
VREF_LO
AMOM_DIBP_R
AMOM_DIBN_N
R343
0R2J-2-GP
R344
0R2J-2-GP
AMOM_DIPP
AMOM_DIPN
AMOM_DIPP <28,58>
AMOM_DIPN <28,58>
AUD_PC_BEEP
MIC_L
C539
SC1U10V3ZY-6GP
AUD_LOL <33>
AUD_LOR <33>
INT_MIC+_L <28>
Speaker
INT_MIC
CDAUD_L
CDAUD_GND
CDAUD_R
CDAUD_L <34>
CDAUD_GND <34>
CDAUD_R <34>
PORT_B_L
C546
SC1U10V3ZY-6GP
PORT_A_HP_L <34>
PORT_A_HP_R <34>
MIC_L_JACK <34>
Headphone
EXT_MIC
R355
2K2R2J-2-GP
MICBIAS_EXT <34,57>
MICBIAS_RES_L
R362
2K2R2J-2-GP
MICBIAS_L <28,58>
AUDIO_SENSE
AUDIO_REFA
AUDIO_VREF_HI
AUDIO_VREF_LO
C561
SCD1U16V2ZY-2GP
C559
SCD1U16V2ZY-2GP
3V_Analog_S0
R328
5K1R2F-2-GP
R319
5K1R2F-2-GP
JACK_DETECT# <3
R320
10KR2F-2-GP
MIC_IN# <34,57>
R324
20KR2F-L-GP
R327
39K2R2F-L-GP
INT_MIC_DECT
Default = lo
AUD_AGND
R363
0R3-0-U-GP
DY
R317
0R3-0-U-GP
DY
R365
0R3-0-U-GP
DY
R325
0R3-0-U-GP
8/17 Reserve for EMI
CUT MOAT
Ver-sc modify
3D3V_S0
R342
0R3-0-U-GP
3V_Analog_S0
C536
SC1U10V3ZY-6GP
C543
SCD1U16V2ZY-2GP
C560
SCD1U16V2ZY-2GP
AUD_AGND
<22> SB_SPKR
R329
1KR2J-1-GP
<55> EC_BEEP
R322
1KR2J-1-GP
<27> PCI_SPKR
R321
1KR2J-1-GP
C517
SCD1U16V2ZY-2GP
AUD_PC_BEEP
R316
1KR2J-1-GP
<Core Design>
緯創資通
Wistron Corpor
21F, 88, Sec.1, Hsin Tai Wu Rd., H
Taipei Hsien 221, Taiwan, R.O.C.
Title
AUDIO CODEC CX20549-12
Size
B
Document Number
Anote2.0 INTEL
Date: Friday, January 12, 2007
Sheet 32 of





Speaker



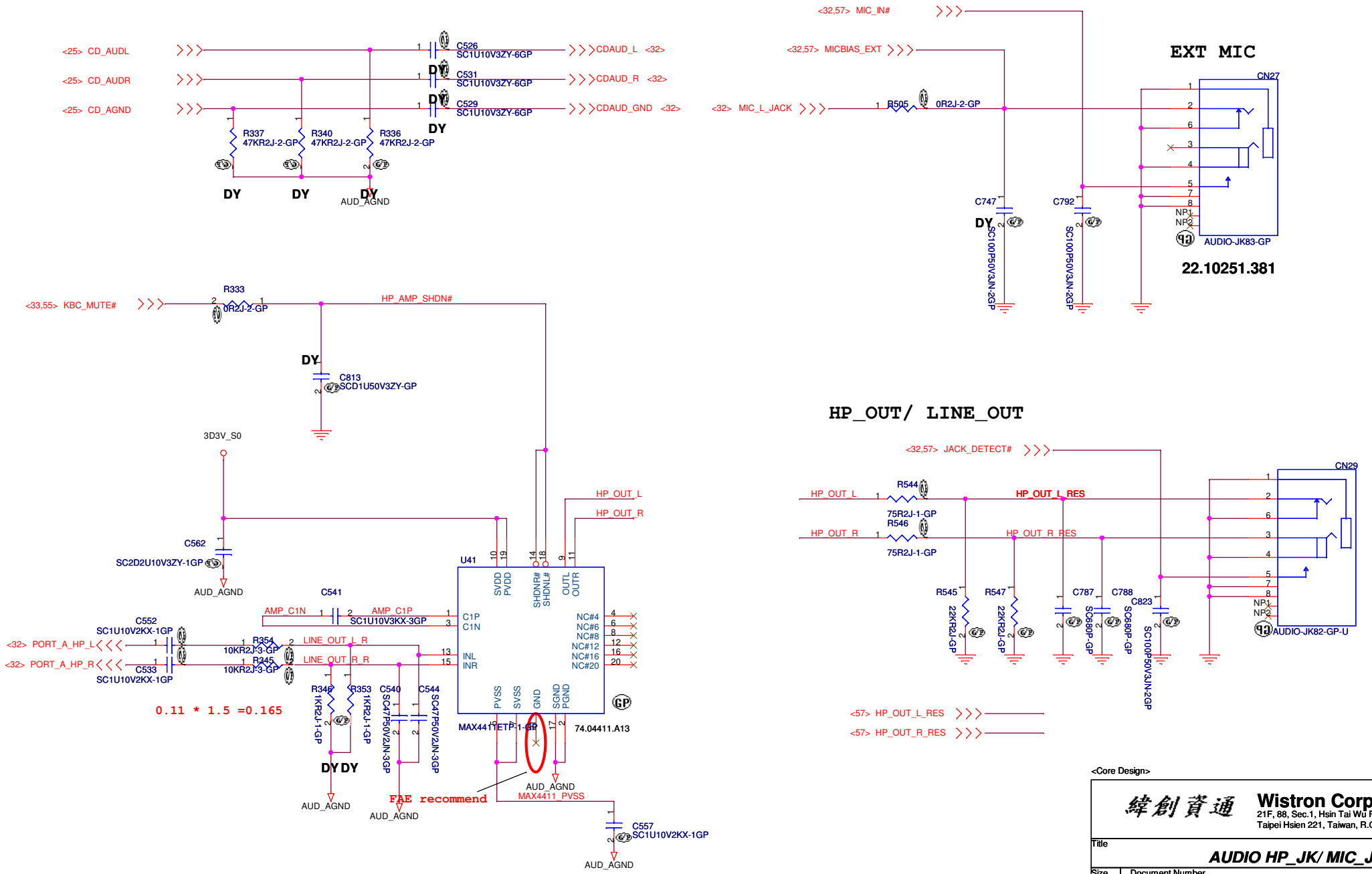
<Core Design>

緯創資通 Wistron Corpor
21F, 88, Sec.1, Hsin Tai Wu Rd., H
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO AMP/SPEAKER

Size: B | Document Number: Anote2.0 INTEL

Date: Friday, January 12, 2007 | Sheet 33 of



<Core Design>

緯創資通 Wistron Corpor
21F, 88, Sec.1, Hsin Tai Wu Rd., H
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO HP_JK/ MIC_JK

Size: B | Document Number: Anote2.0 INTEL

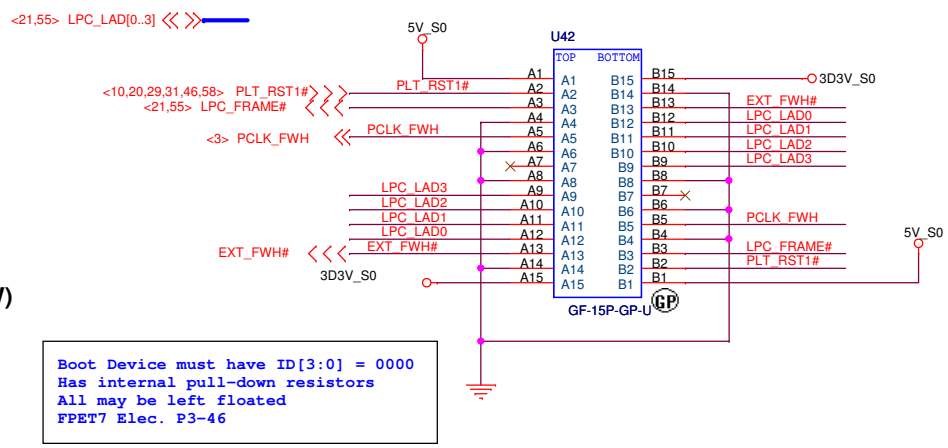
Date: Friday, January 12, 2007 | Sheet 34 of

GOLDEN FINGER FOR DEBUG BOARD

TOP VIEW

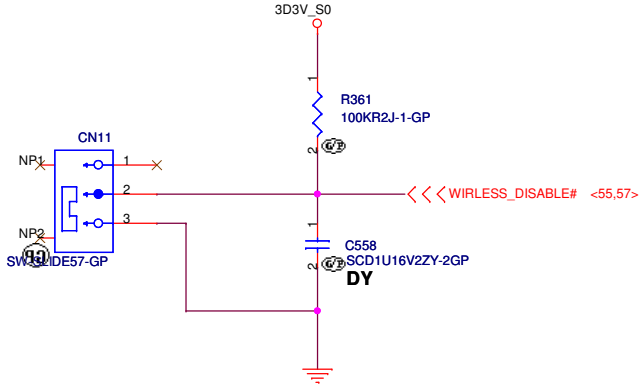
A15 (B1)
A14 (B2)
⋮ ⋮
A2 (B14)
A1 (B15)

(BOTTOM VIEW)



Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46

WIRELESS SWITCH



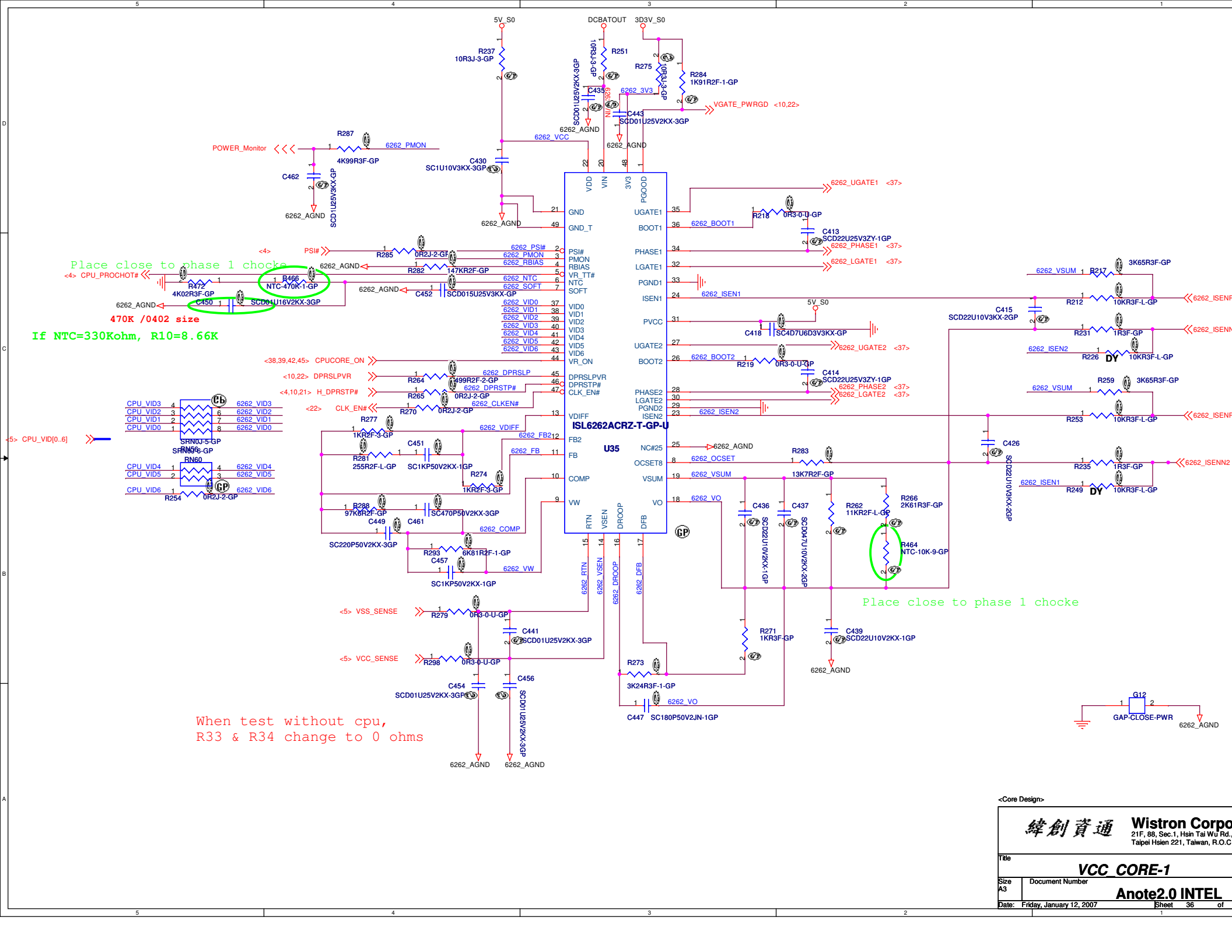
<Core Design>

緯創資通 Wistron Corpor
21F, 88, Sec.1, Hsin Tai Wu Rd., H
Taipei Hsien 221, Taiwan, R.O.C.

Title: *FWH and Debug*

Size: B | Document Number: Anote2.0 INTEL

Date: Friday, January 12, 2007 | Sheet 35 of



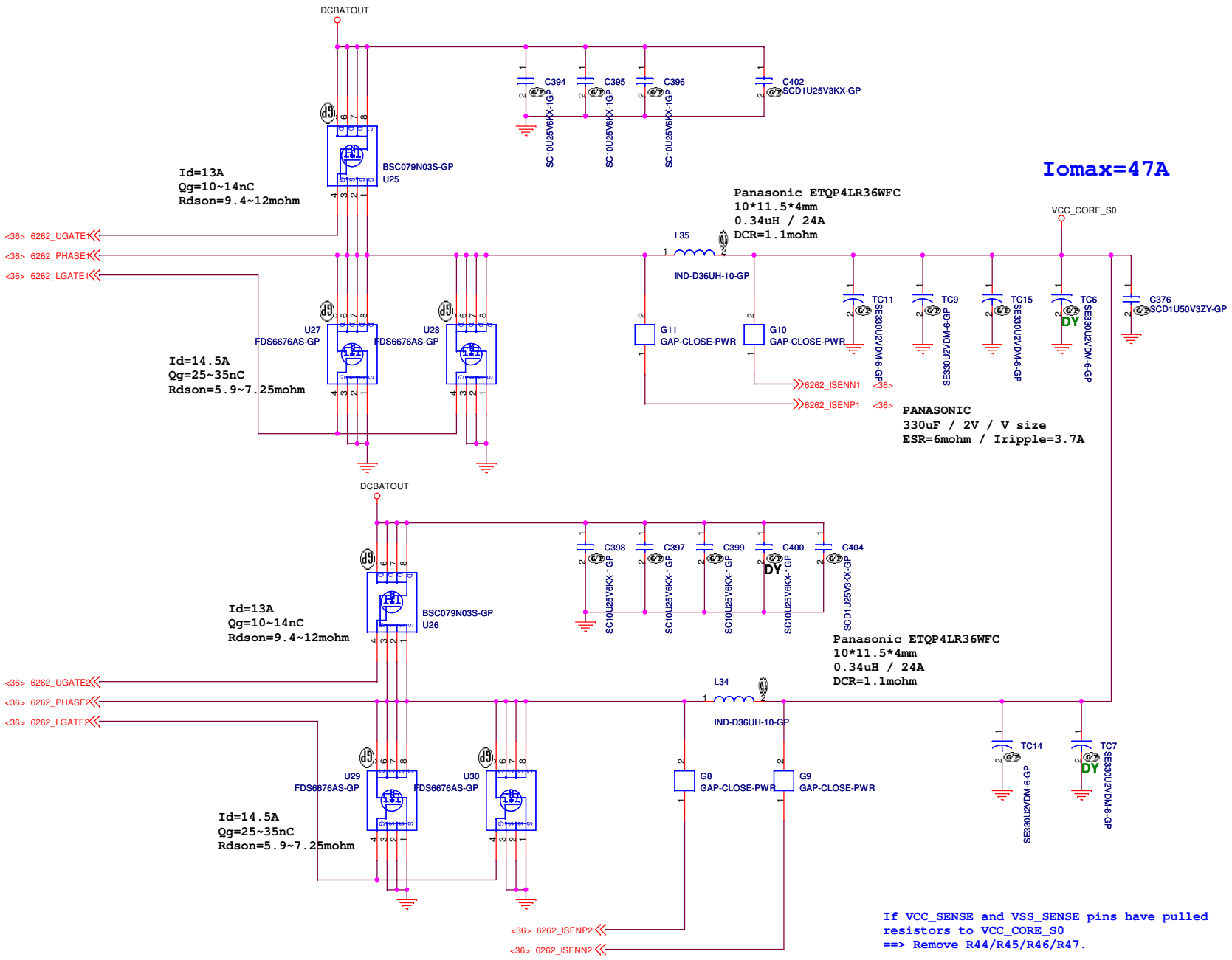
<Core Design>

緯創資通 Wistron Corpo
21F, 88, Sec.1, Hsin Tai Wu Rd.,
Taipei Hsien 221, Taiwan, R.O.C

Title: VCC_CORE-1

Size: A3 | Document Number: Anote2.0 INTEL

Date: Friday, January 12, 2007 | Sheet 36 of



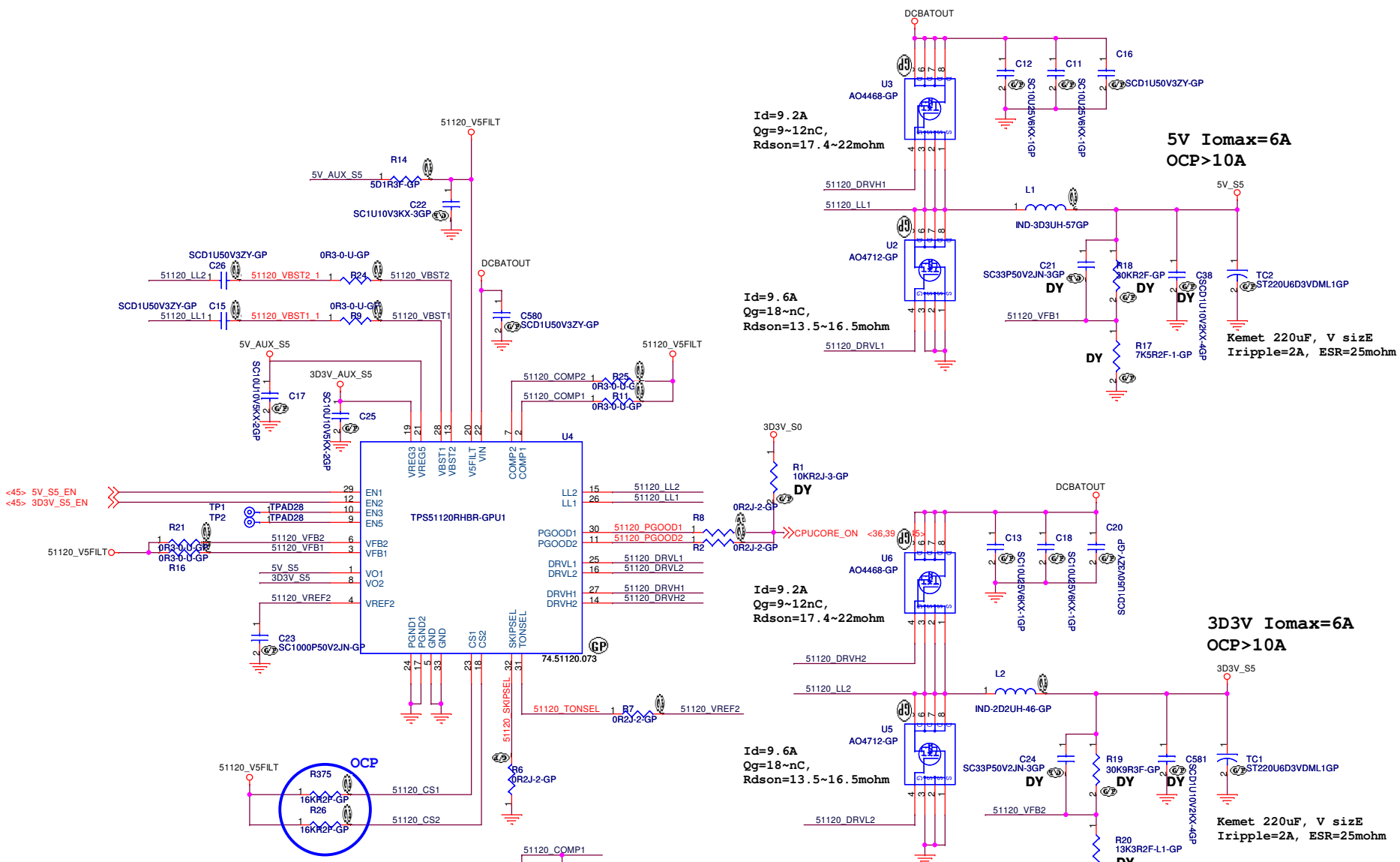
<Core Design>

緯創資通 Wistron Corpo
21F, 88, Sec.1, Hsin Tai Wu Rd.,
Taipei Hsien 221, Taiwan, R.O.C

Title: VCC_CORE_2

Size: A3 | Document Number: Anote2.0 INTEL

Date: Friday, January 12, 2007 | Sheet 37 of



Pin	GND	VREF2	FLOAT	V5FILT
COMP	N/A	N/A	Current Mode (apply R-C network)	D-CAP. Mode
TONSEL (CH1/CH2) [kHz]	380 / 580	280 / 430	220 / 330	180 / 270
VFB1	Adjustable output (connect to the resistor divider)			5V fixed output
VFB2	Adjustable output (connect to the resistor divider)			3.3 V fixed output
SKIPSEL	AUTO-SKIP	AUTO-SKIP (FAULTS OFF)	PWM	PWM
EN1, EN2	Switcher Off	Not used	Switcher on	Switcher on
EN3, EN5	LDO Off	Not used	LDO on	LDO on (EN3 only)

For TPS51120,
Vout=5V
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.
Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

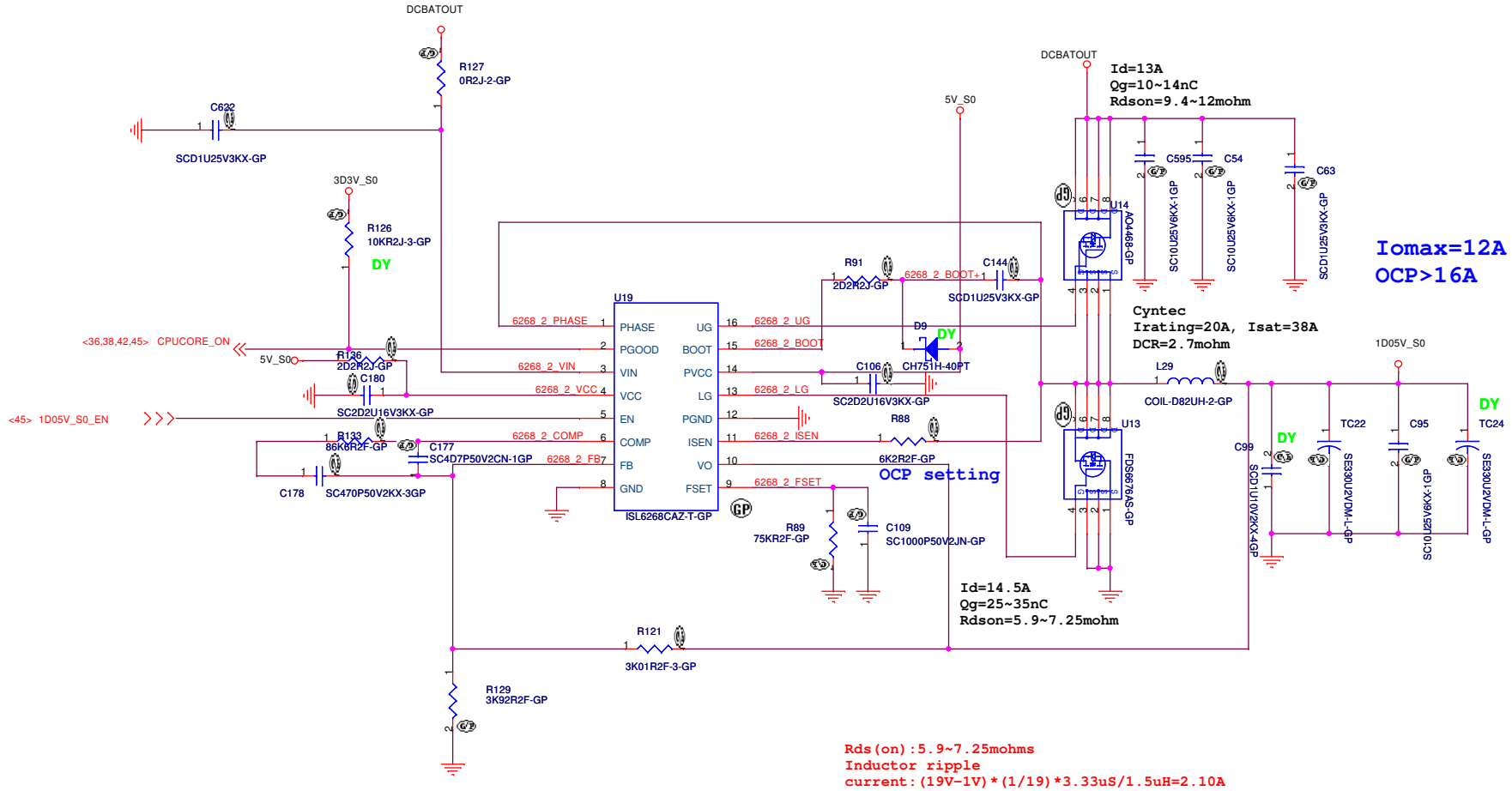
<Core Design>

緯創資通 Wistron Corpo
21F, 88, Sec.1, Hsin Tai Wu Rd.,
Taipei Hsien 221, Taiwan, R.O.C

Title: TPS51120 5V/3D3V

Size: A3 | Document Number: Anote2.0 INTEL

Date: Friday, January 12, 2007 | Sheet 38 of



<Core Design>

緯創資通 Wistron Corpo

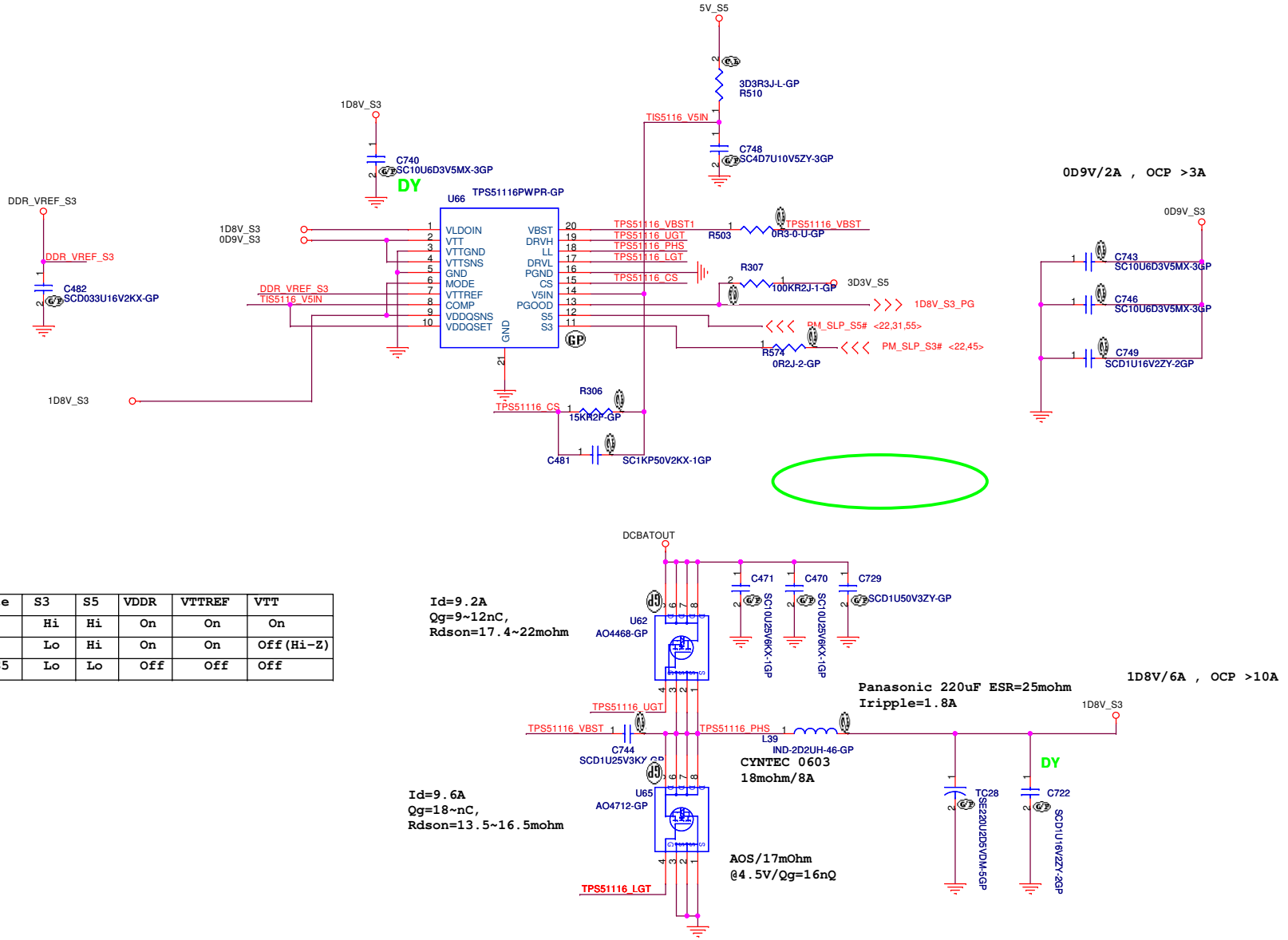
21F, 88, Sec.1, Hsin Tai Wu Rd.,
Taipei Hsien 221, Taiwan, R.O.C

Title: 1D05V_S0_ISL6268

Size: A3 | Document Number: Anote2.0 INTEL

Date: Friday, January 12, 2007 | Sheet 39 of

TI TPS51116 for 1D8V and 0D9V



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

<Core Design>

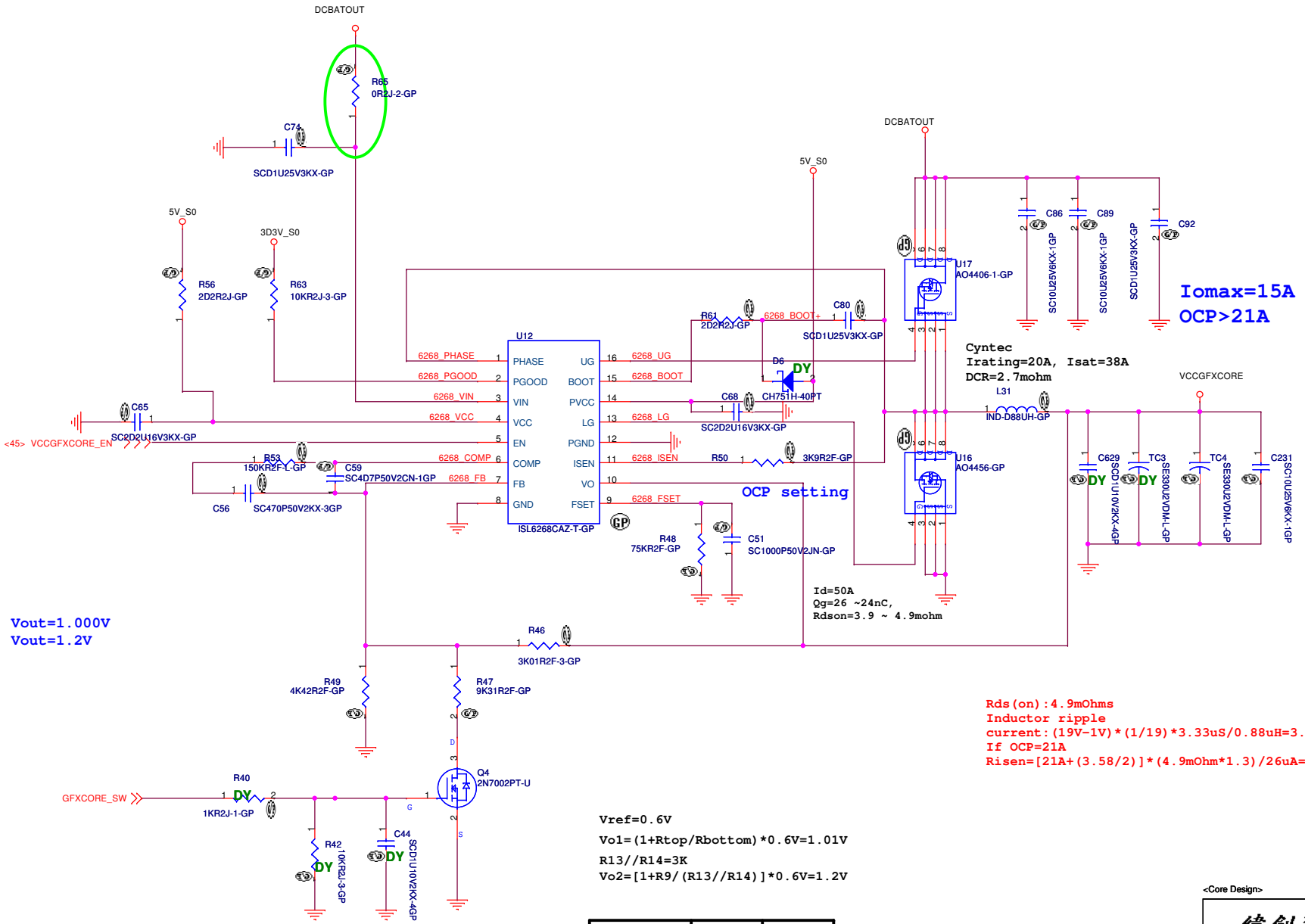
緯創資通 Wistron Corpo
21F, 88, Sec.1, Hsin Tai Wu Rd.,
Taipei Hsien 221, Taiwan, R.O.C

Title: TPS51116 1D8V/0D9V

Size: A3 | Document Number: Anote2.0 INTEL

Date: Friday, January 12, 2007 | Sheet 40 of

reserve for cost down



Vo_Select	Hi	Lo
Vout	1.2V	1.01V

<Core Design>

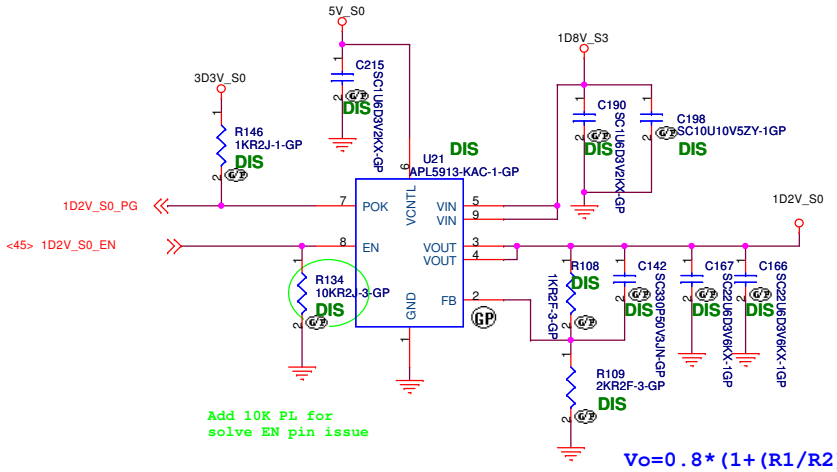
緯創資通 Wistron Corpo
21F, 88, Sec.1, Hsin Tai Wu Rd.,
Taipei Hsien 221, Taiwan, R.O.C

Title
DC/DC VCCGFXCORE(ISL6268)

Size A3 | Document Number Anote2.0 INTEL

Date: Friday, January 12, 2007 | Sheet 41 of

VGA 1.2V Power

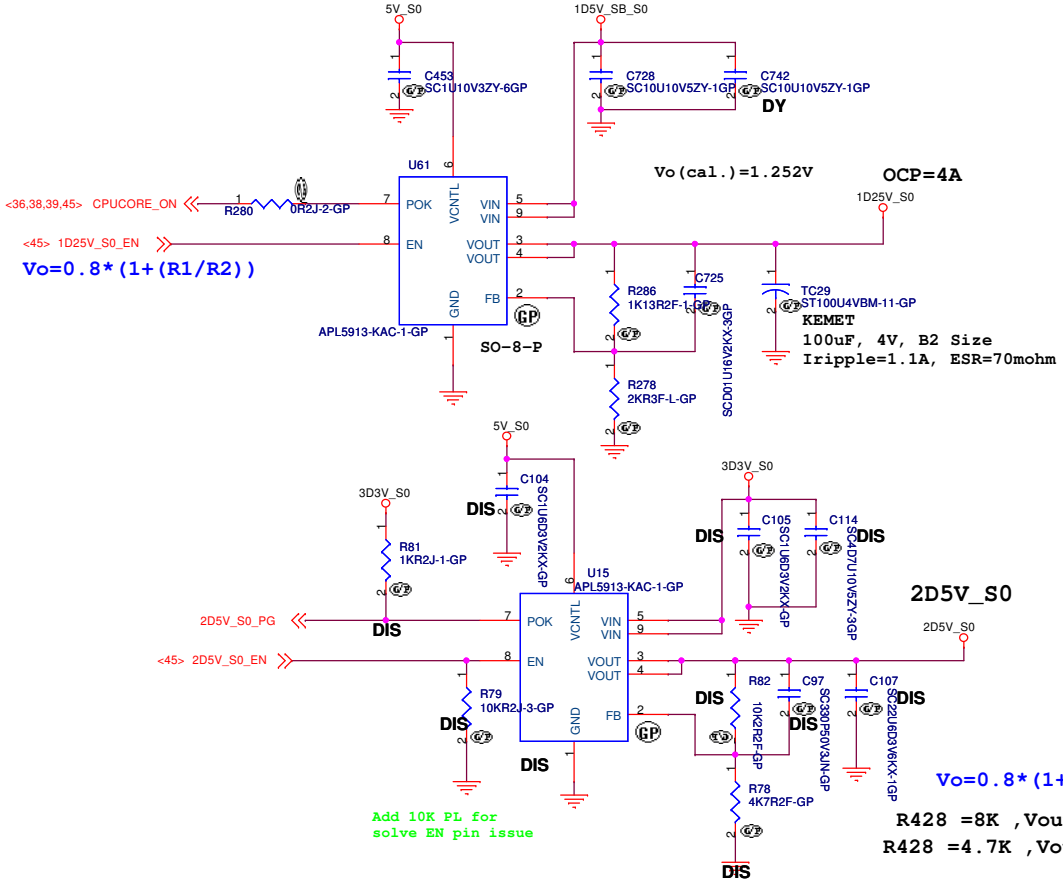


1D2V_S0
only for DISCRETE

1D5V_NB

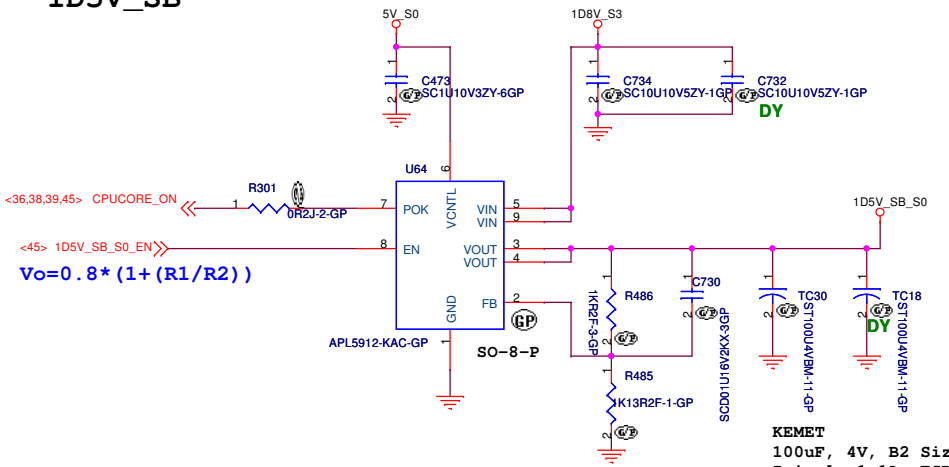
PS: SB del

1D25V_S0
Iomax=2.0A



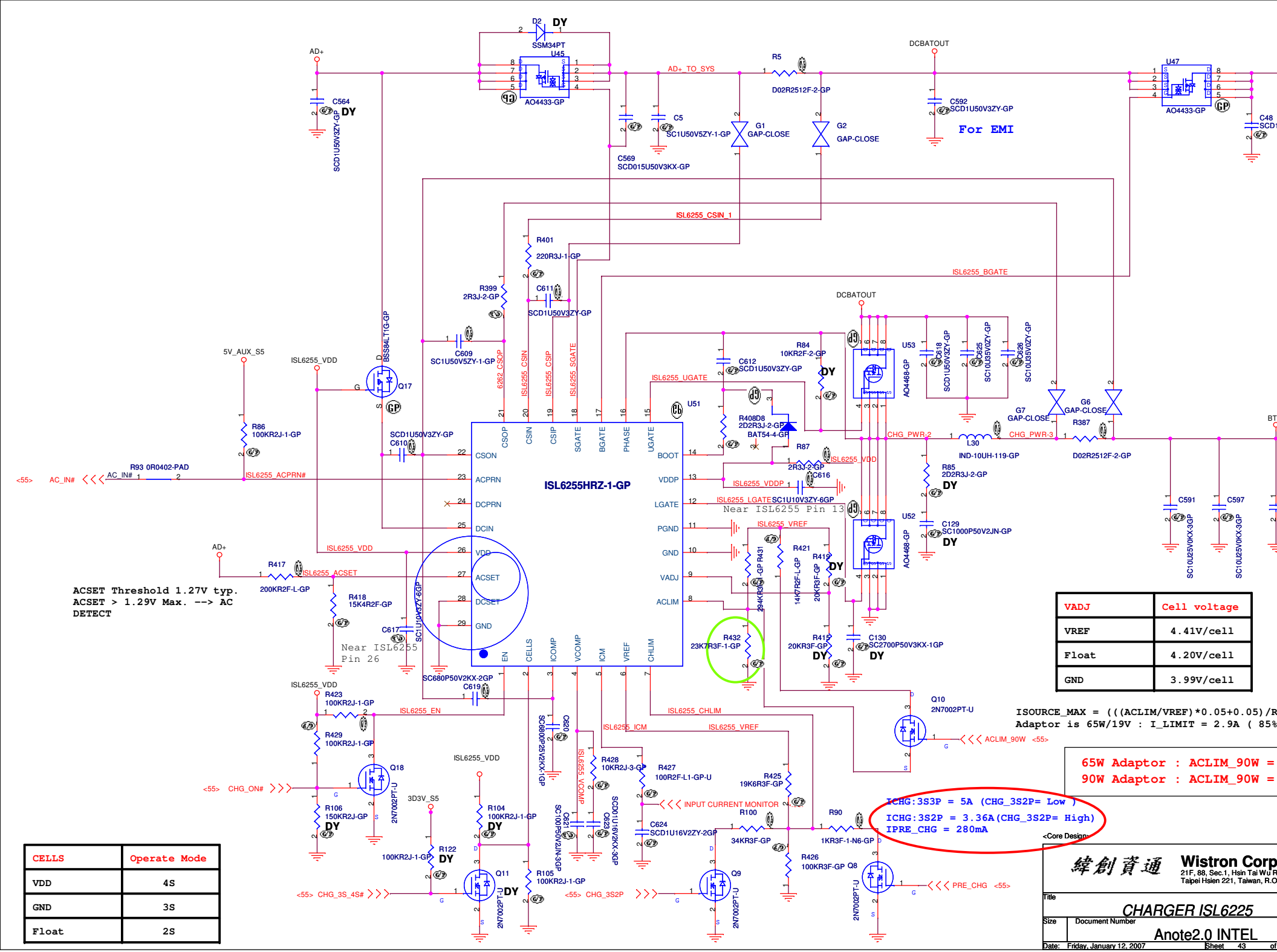
2D5V_S0
only for DISCRETE

1D5V_SB



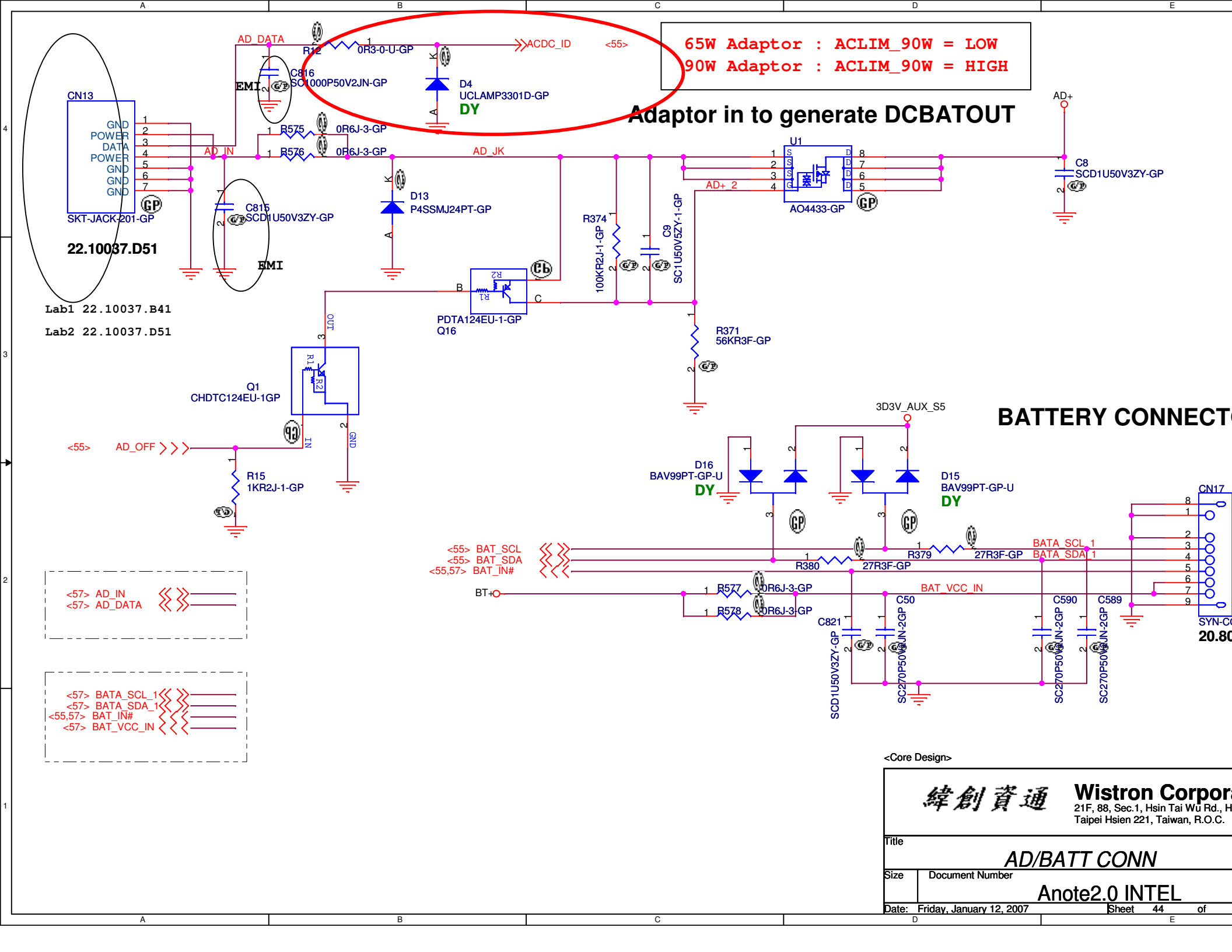
<Core Design>

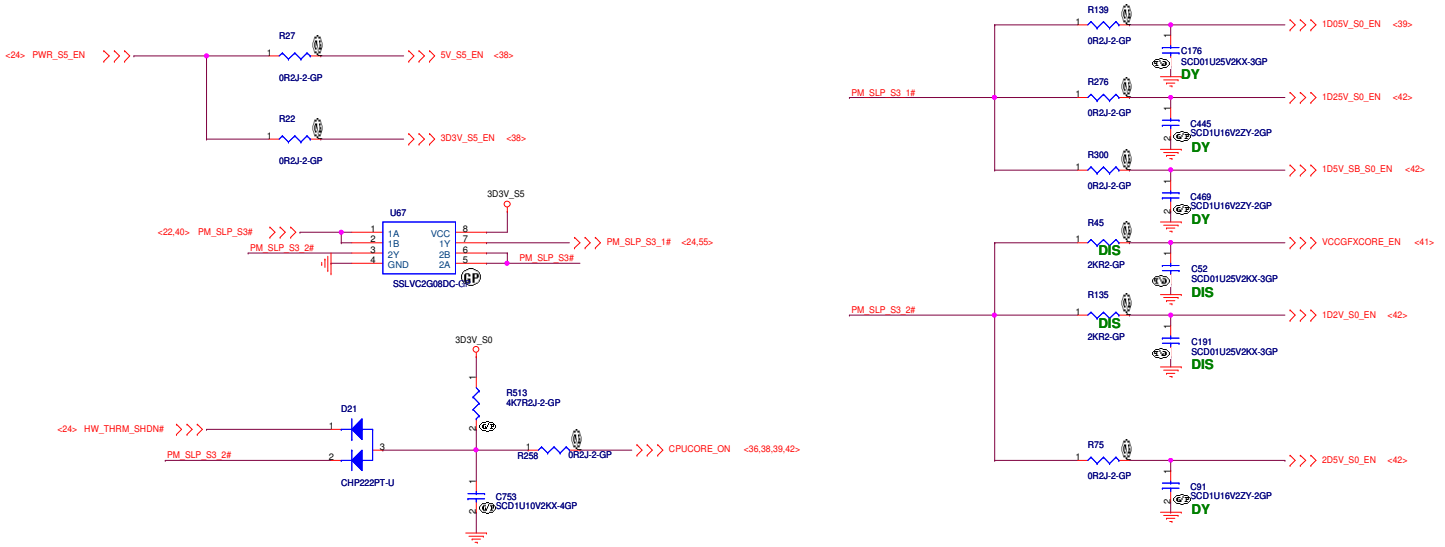
緯創資通	Wistron Corpo 21F, 88, Sec.1, Hsin Tai Wu Rd., Taipei Hsien 221, Taiwan, R.O.C
Title	1D2V_VGA/2D5V/1D25V/1D5V LDO
Size	Document Number: Anote2.0 INTEL
Date: Friday, January 12, 2007	Sheet 42 of



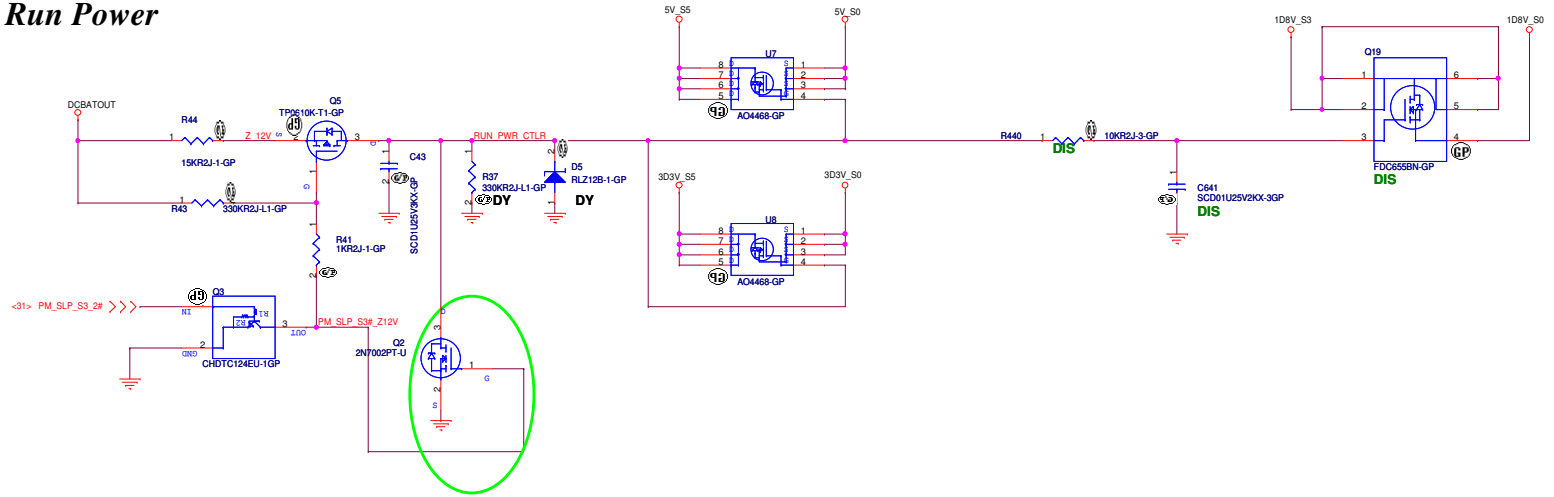
VADJ	Cell voltage
VREF	4.41V/cell
Float	4.20V/cell
GND	3.99V/cell

CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S


65W Adaptor : ACLIM_90W = LOW
90W Adaptor : ACLIM_90W = HIGH
Adaptor in to generate DCBATOUT
BATTERY CONNECT
CN13
SKT-JACK-201-GP
22.10037.D51
Lab1 22.10037.B41
Lab2 22.10037.D51
AD_DATA
R12
0R3-0-U-GP
ACDC_ID
<55>
C816
SC1000P50V2JN-GP
EMI
D4
UCLAMP3301D-GP
DY
R575
0R6J-3-GP
R576
0R6J-3-GP
AD_IN
AD_JK
C815
SCD1U50V3ZY-GP
D13
P4SSMJ24PT-GP
U1
AO4433-GP
AD+_2
AD+
C8
SCD1U50V3ZY-GP
R374
100KR2J-1-GP
C9
SC1U50V5ZY-1-GP
PDTA124EU-1-GP
Q16
R371
56KR3F-GP
Q1
CHDTC124EU-1GP
<55> AD_OFF
R15
1KR2J-1-GP
3D3V_AUX_S5
D16
BAV99PT-GP-U
DY
D15
BAV99PT-GP-U
DY
CN17
<55> BAT_SCL
<55> BAT_SDA
<55,57> BAT_IN#
BT+
R380
27R3F-GP
R379
27R3F-GP
BATA_SCL_1
BATA_SDA_1
R577
0R6J-3-GP
R578
0R6J-3-GP
BAT_VCC_IN
C50
C590
C589
C821
SCD1U50V3ZY-GP
SC270P50V2JN-2GP
SC270P50V2JN-2GP
SC270P50V2JN-2GP
<57> AD_IN
<57> AD_DATA
<57> BATA_SCL_1
<57> BATA_SDA_1
<55,57> BAT_IN#
<57> BAT_VCC_IN
<Core Design>
緯創資通
Wistron Corpor
21F, 88, Sec.1, Hsin Tai Wu Rd., H
Taipei Hsien 221, Taiwan, R.O.C.
Title
AD/BATT CONN
Size
Document Number
Anote2.0 INTEL
Date: Friday, January 12, 2007
Sheet 44 of

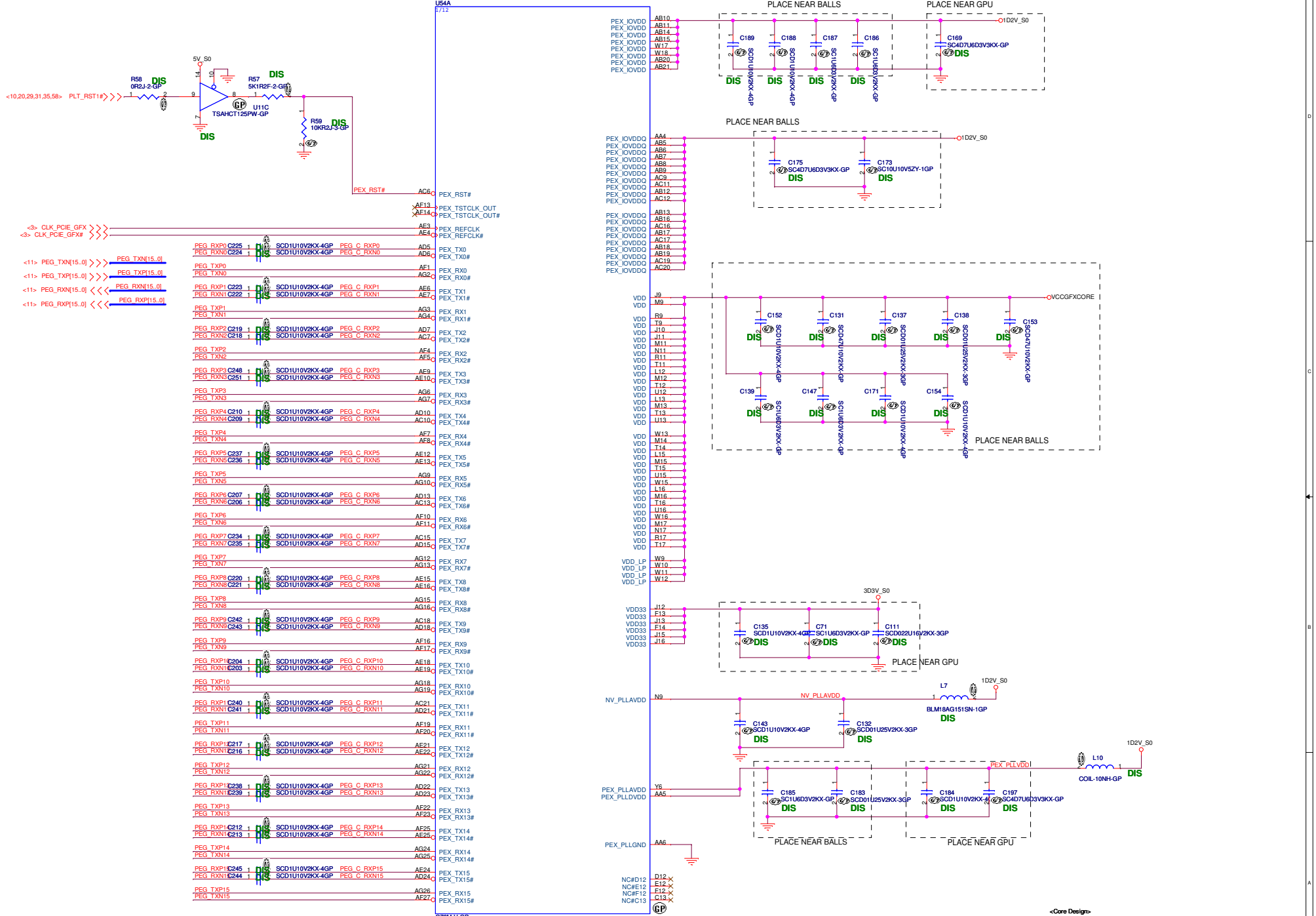


Run Power



<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***PWRPLANE&RESET LOGIC***	
Size: C	Document Number: Anote2.0 INTEL	Rev: SC
Date: Friday, January 12, 2007	Sheet 45 of 58	



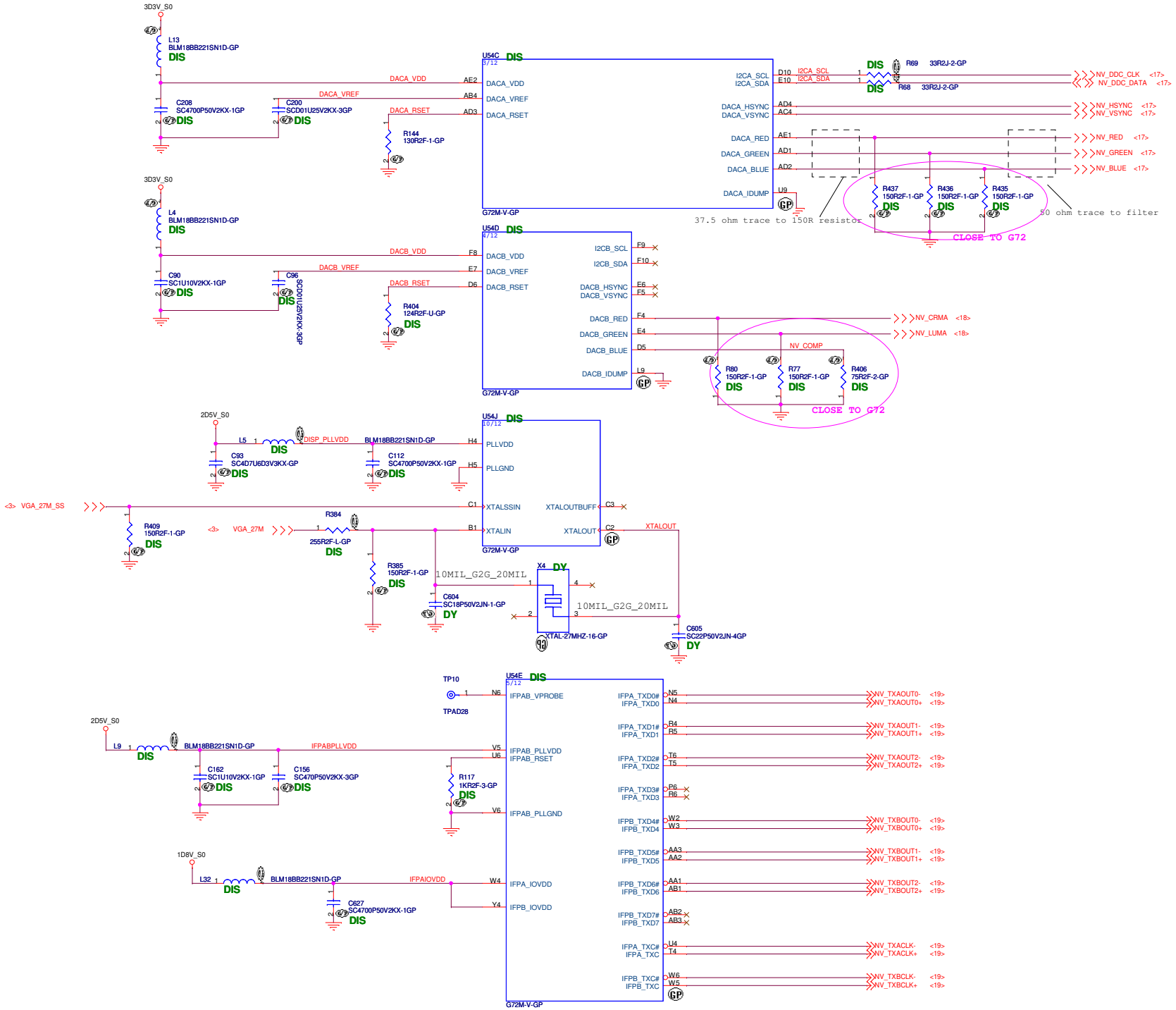
<Core Design>

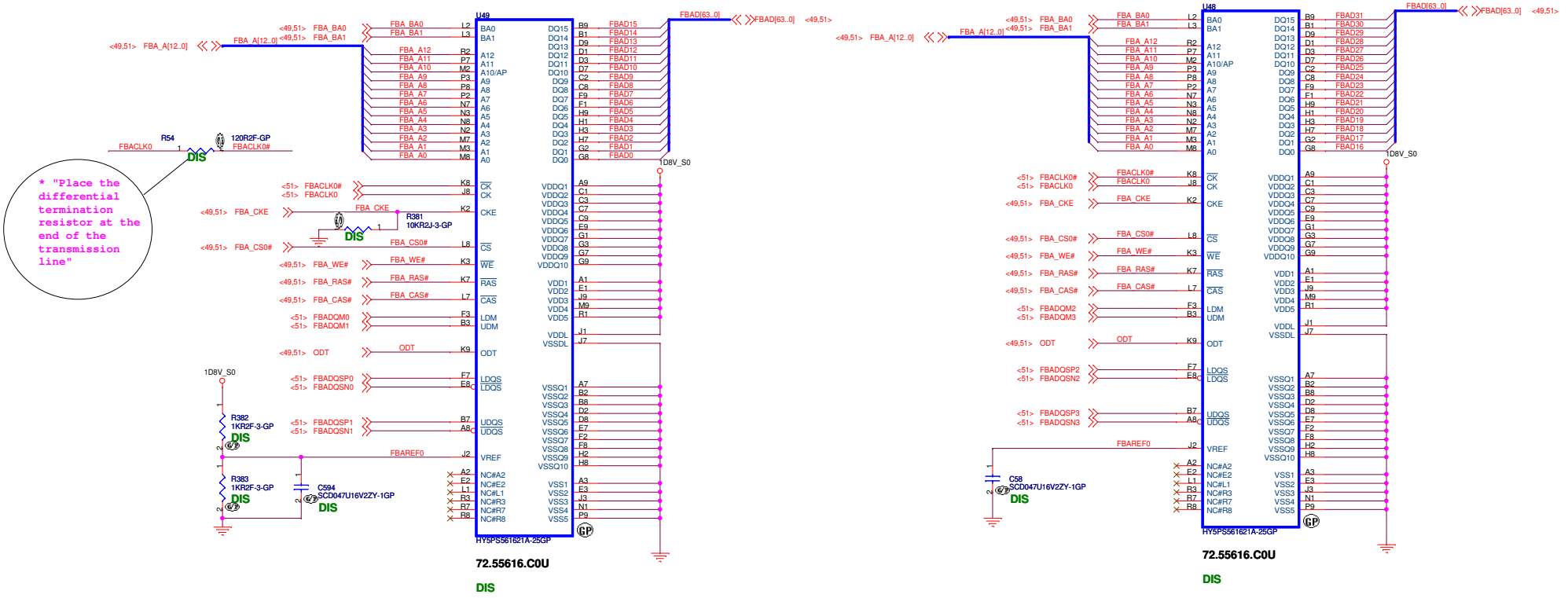
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: G72M PCIE

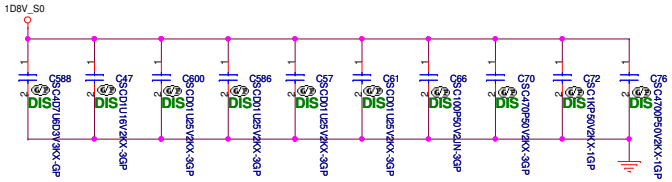
Size: | Document Number: Anote2.0 INTEL | Rev: SC

Date: Friday, January 12, 2007 | Sheet 46 of 58

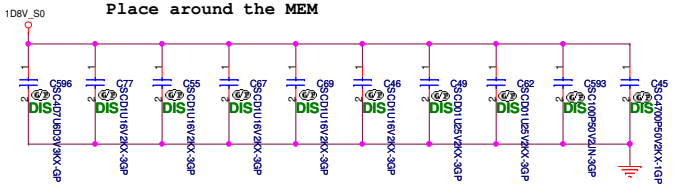

3D3V_S0
L13
BLM18BB221SN1D-GP
DIS
C208
SC4700P50V2KX-1GP
C200
SCD01U25V2KX-3GP
DACA_VDD
DACA_VREF
DACA_RSET
R144
130R2F-1-GP
U54C
DIS
G72M-V-GP
AE2
AB4
AD3
DACA_VDD
DACA_VREF
DACA_RSET
I2CA_SCL
I2CA_SDA
DACA_HSYNC
DACA_VSYNC
DACA_RED
DACA_GREEN
DACA_BLUE
DACA_IDUMP
D10
E10
AD4
AC4
AE1
AD1
AD2
U9
R69
33R2J-2-GP
R68
33R2J-2-GP
NV_DDC_CLK
NV_DDC_DATA
NV_HSYNC
NV_VSYNC
NV_RED
NV_GREEN
NV_BLUE
R437
150R2F-1-GP
R436
150R2F-1-GP
R435
150R2F-1-GP
37.5 ohm trace to 150R resistor
50 ohm trace to filter
CLOSE TO G72
3D3V_S0
L4
BLM18BB221SN1D-GP
C90
SC1U10V2KX-1GP
C96
SCD01U25V2KX-3GP
DACB_VDD
DACB_VREF
DACB_RSET
R404
124R2F-U-GP
U54D
G72M-V-GP
F8
E7
D6
DACB_VDD
DACB_VREF
DACB_RSET
I2CB_SCL
I2CB_SDA
DACB_HSYNC
DACB_VSYNC
DACB_RED
DACB_GREEN
DACB_BLUE
DACB_IDUMP
F9
F10
E6
F5
F4
E4
D5
L9
NV_CRMA
NV_LUMA
NV_COMP
R80
150R2F-1-GP
R77
150R2F-1-GP
R406
75R2F-2-GP
CLOSE TO G72
2D5V_S0
L5
DISP_PLLVDD
BLM18BB221SN1D-GP
C83
SC4D7U6D3V3KX-GP
C112
SC4700P50V2KX-1GP
U54J
G72M-V-GP
H4
H5
PLLVDD
PLLGND
<3> VGA_27M_SS
R409
150R2F-1-GP
<3> VGA_27M
R384
255R2F-L-GP
C1
B1
XTALSSIN
XTALIN
XTALOUTBUFF
XTALOUT
C3
C2
XTALOUT
R385
150R2F-1-GP
10MIL_G2G_20MIL
C604
SC18P50V2JN-1-GP
DY
X4
XTAL-27MHZ-16-GP
C605
SC22P50V2JN-4GP
U54L
G72M-V-GP
M5
IFPCD_VPROBE
G72_PLLVDD
M4
J3
IFPCD_PLLVDD
IFPCD_RSET
R103
10KR2J-3-GP
M6
IFPCD_PLLGND
G72_IFPC_IOVDD
L4
IFPC_IOVDD
R101
10KR2J-3-GP
TP10
TPAD28
U54E
G72M-V-GP
N6
IFPAB_VPROBE
2D5V_S0
L9
BLM18BB221SN1D-GP
IFPABPLLVDD
C162
SC1U10V2KX-1GP
C156
SC470P50V2KX-3GP
R117
1KR2F-3-GP
V5
U6
V6
IFPAB_PLLVDD
IFPAB_RSET
IFPAB_PLLGND
1D8V_S0
L32
BLM18BB221SN1D-GP
IFPAIOVDD
C627
SC4700P50V2KX-1GP
W4
Y4
IFPA_IOVDD
IFPB_IOVDD
IFPA_TXD0#
IFPA_TXD0
IFPA_TXD1#
IFPA_TXD1
IFPA_TXD2#
IFPA_TXD2
IFPA_TXD3#
IFPA_TXD3
IFPB_TXD4#
IFPB_TXD4
IFPB_TXD5#
IFPB_TXD5
IFPB_TXD6#
IFPB_TXD6
IFPB_TXD7#
IFPB_TXD7
IFPA_TXC#
IFPA_TXC
IFPB_TXC#
IFPB_TXC
N5
N4
R4
R5
T6
T5
P6
R6
W2
W3
AA3
AA2
AA1
AB1
AB2
AB3
U4
T4
W6
W5
NV_TXAOUT0-
NV_TXAOUT0+
NV_TXAOUT1-
NV_TXAOUT1+
NV_TXAOUT2-
NV_TXAOUT2+
NV_TXBOUT0-
NV_TXBOUT0+
NV_TXBOUT1-
NV_TXBOUT1+
NV_TXBOUT2-
NV_TXBOUT2+
NV_TXACLK-
NV_TXACLK+
NV_TXBCLK-
NV_TXBCLK+
<19>
<Core Design>
緯創資通
Wistron Co
21F, 88, Sec.1, Hsin Tai W
Taipei Hsien 221, Taiwan,
Title
G72M CRT & TV OUT
Size
Document Number
Anote2.0 INTEL
Date: Friday, January 12, 2007
Sheet 47



Decoupling for left MEMORY
Place around the MEM



Decoupling for right MEMORY
Place around the MEM

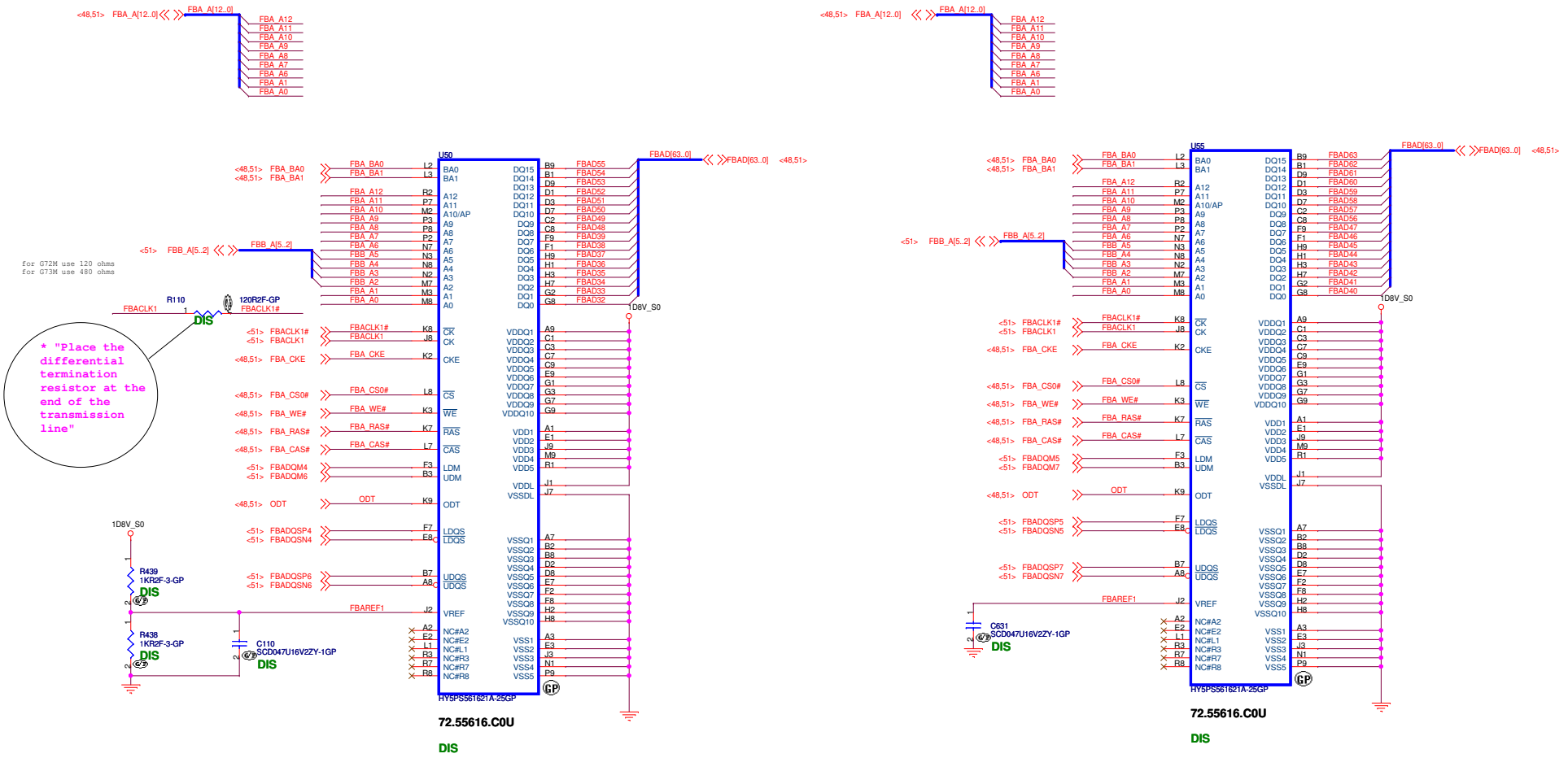


72.51216.D0U IC VRAM HY5PS121621BFP-25 FBGA(32M*16, 400Mhz)
72.55616.C0U IC VRAM HY5PS561621AFP-25 FBGAby Hynix (16M*16, 400Mhz)
72.18512.A0U IC VRAM HY5PS121621BFP-25 FBGA by Infineon (32M*16, 400Mhz)
72.18256.B0U IC VRAM HYB18T256161AFL25 BGA, by Infineon(16M*16, 400Mhz)

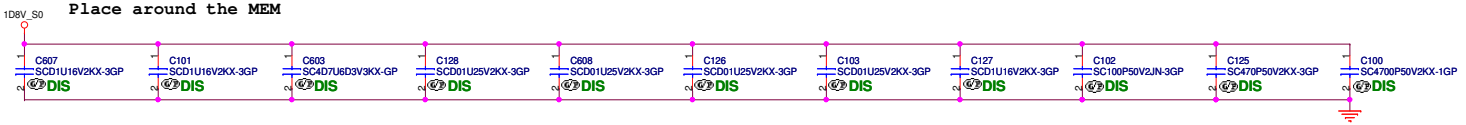
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

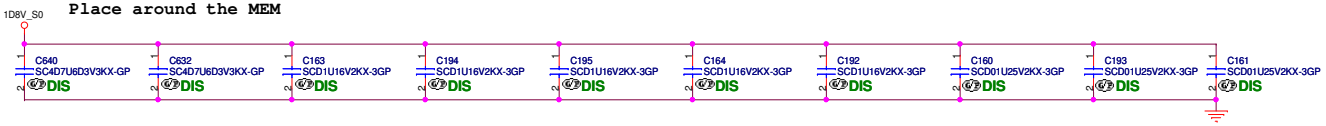
Title	*G72M VRAM (1ST 1/2)*	
Size	Document Number: Anote2.0 INTEL	Rev: SC
Date: Friday, January 12, 2007	Sheet 48 of 58	



Decoupling for left MEMORY
Place around the MEM



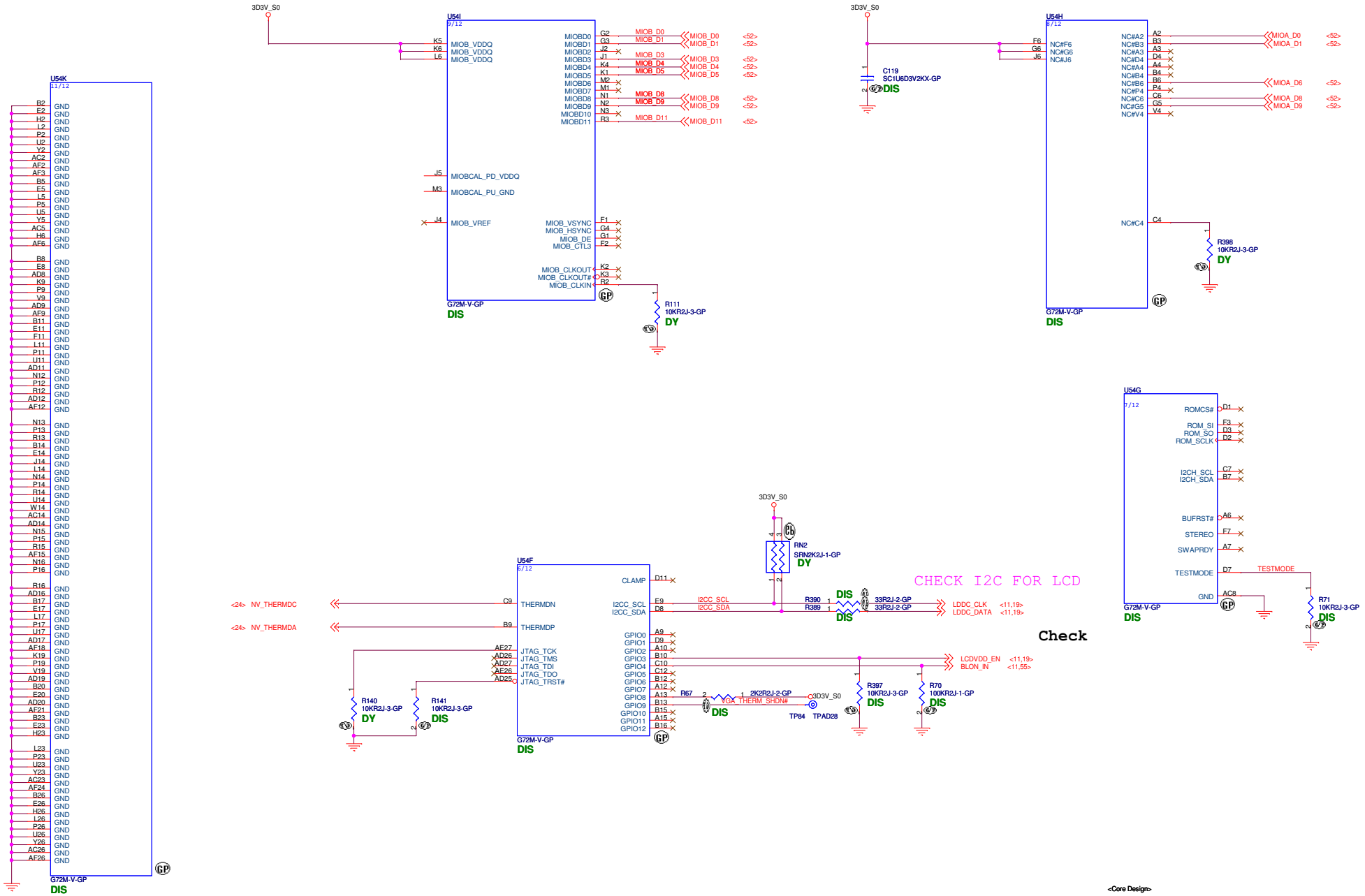
Decoupling for right MEMORY
Place around the MEM



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	G72M VRAM (1ST 2/2)	
Size	Document Number: Anote2.0 INTEL	Rev: SC
Date: Friday, January 12, 2007	Sheet 49 of 58	



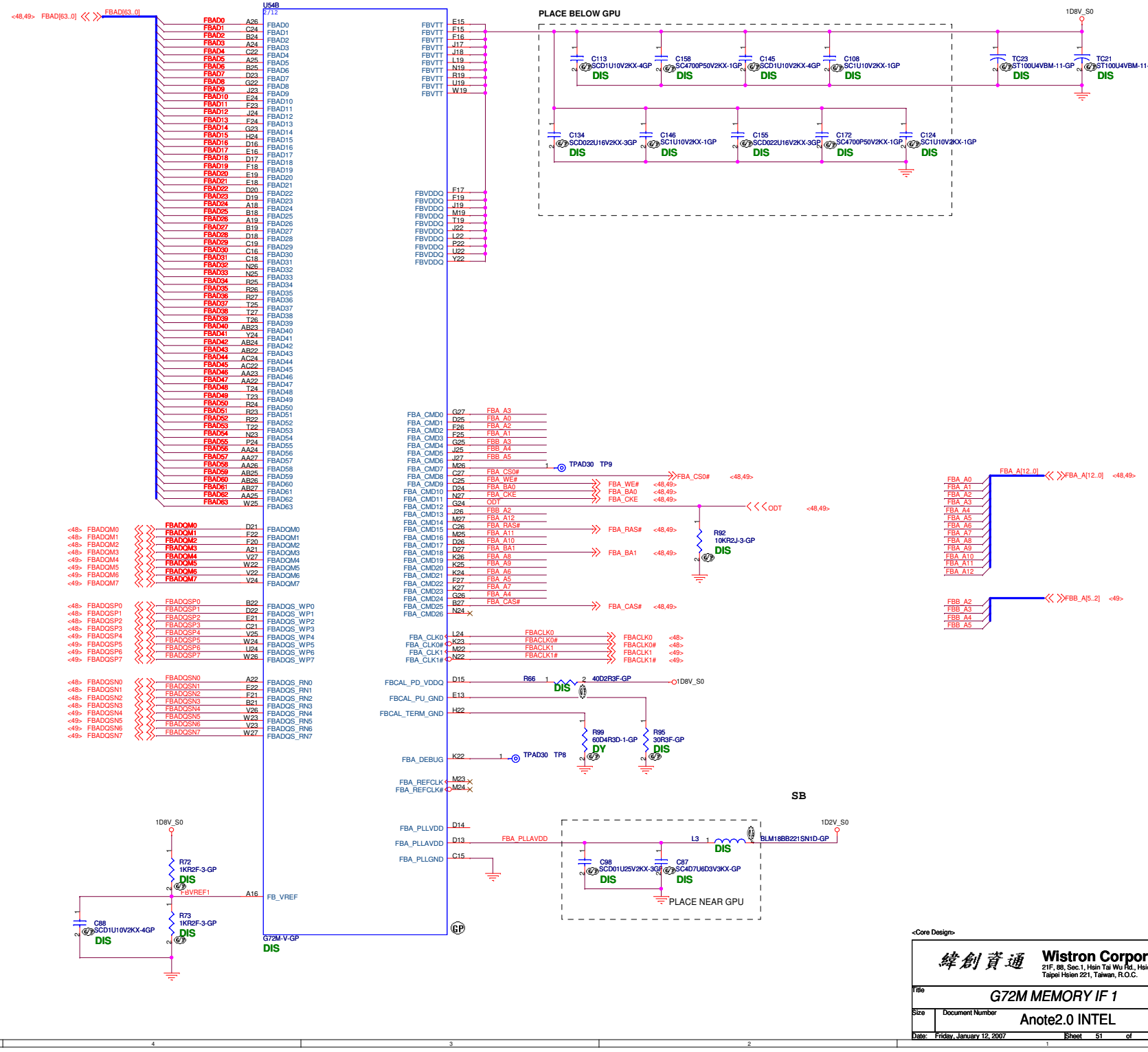
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: G72M ROM & Spread Specturm

Size	Document Number	Rev
	Anote2.0 INTEL	SC

Date: Friday, January 12, 2007 Sheet 50 of 58



<Core Design>

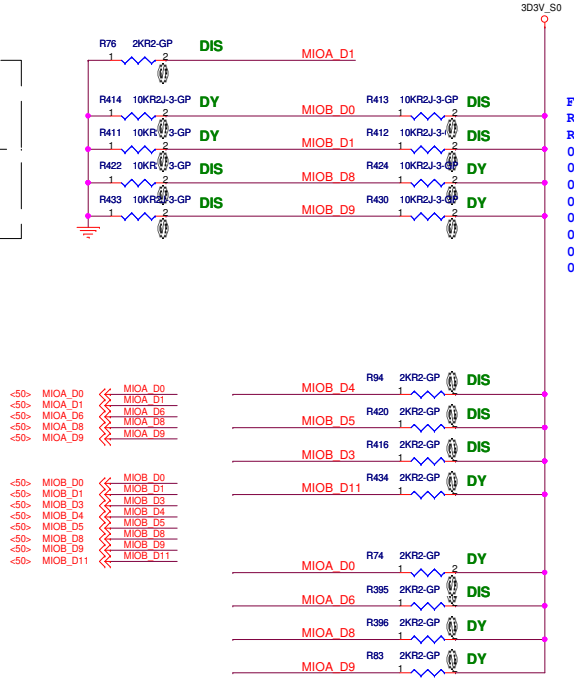
Wistron Corpor
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsi
Taipei Hsien 221, Taiwan, R.O.C.

Title	G72M MEMORY IF 1	
Size	Document Number	Anote2.0 INTEL
Date: Friday, January 12, 2007	Sheet 51	of

STRAPS, Mechanical Parts

Check

Hynix256MB :	R825_0	R824_1	R822_1	R820_1
Hynix128MB :	R825_0	R823_0	R822_1	R820_1
Hynix64MB :	R826_1	R823_0	R822_1	R820_1
Infineon256MB :	R825_0	R824_1	R822_1	R819_0
Infineon128MB :	R825_0	R823_0	R822_1	R819_0
Infineon64MB :	R826_1	R823_0	R822_1	R819_0



Bit	Signal	Values
MIOA_D1:	SUB_VENDOR	0 NO_BIOS 1 READ FROM BIOS

For MEM strapping, Please use below table:

RAM_CFG[9.8.1.0] RAM_CFG[3..0]	Config	FB Bus Width	Definitions
0000			
0001	16Mx16 DDR2	64-bit	Samsung
0010	16Mx16 DDR2	64-bit	Infineon
0011	16Mx16 DDR2	64-bit	Hynix
0100			
0101	32Mx16 DDR2	64-bit	Samsung
0110	32Mx16 DDR2	64-bit	Infineon
0111	32Mx16 DDR2	64-bit	Hynix

MIOB_D4:	PCI_DEVID_0		
MIOB_D5:	PCI_DEVID_1	1000 (default 0x00FC)	
MIOB_D3:	PCI_DEVID_2		
MIOB_D11:	PCI_DEVID_3	0111 G72MV	G72MZ=6,G73=8

MIOA_D0:	PEX_PLL_EN_TERM100	0 ENABLED 1 DISABLED
MIOA_D6:	3GIO_PADCFG_LUT_ADDR[0]	
MIOA_D8:	3GIO_PADCFG_LUT_ADDR[1]	
MIOA_D9:	3GIO_PADCFG_LUT_ADDR[2]	001 DEFAULT

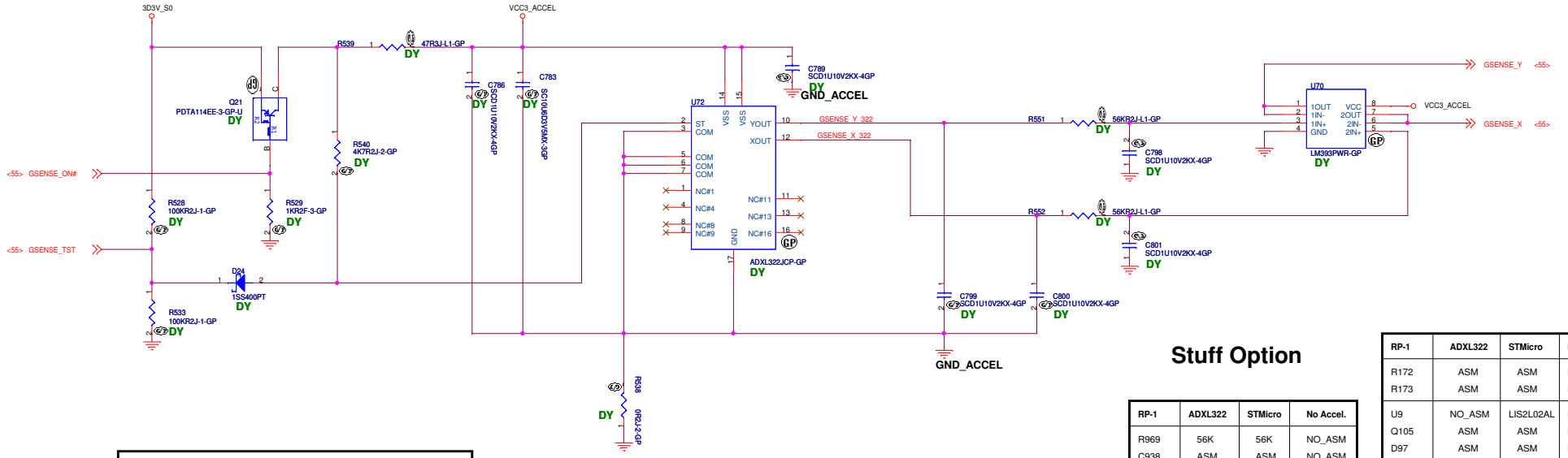
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: G72M STRAPPING

Size | Document Number: Anote2.0 INTEL | Rev: SC

Date: Friday, January 12, 2007 | Sheet 52 of 58



Stuff Option

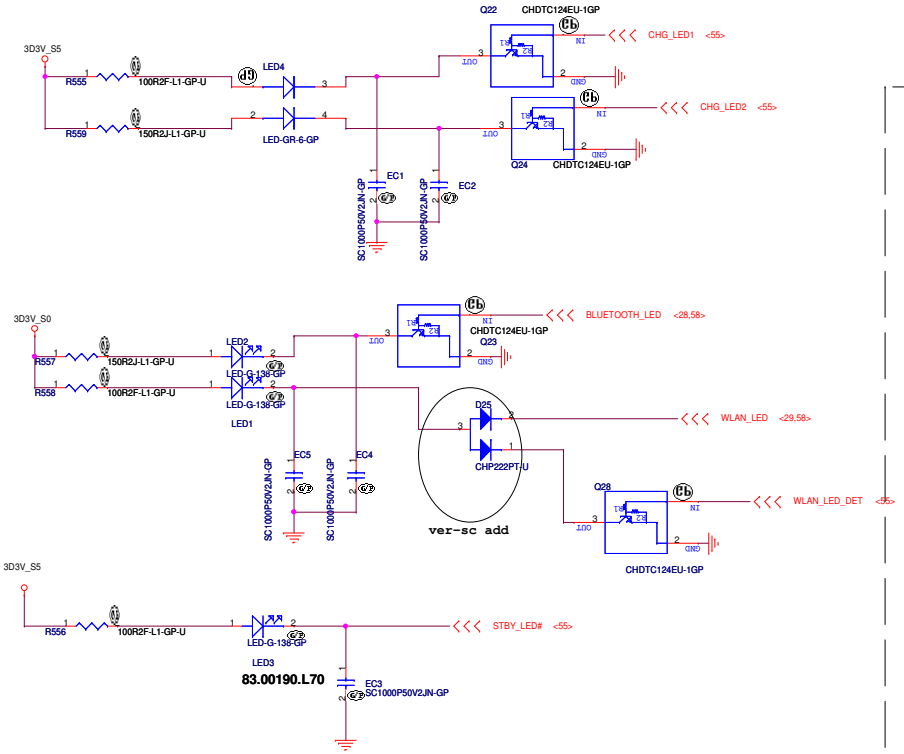
RP-1	ADXL322	STMicro	No Accel.
R969	56K	56K	NO_ASM
C938	ASM	ASM	NO_ASM
R970	56K	56K	NO_ASM
C956	ASM	ASM	NO_ASM
U66	ADXL322	NO_ASM	NO_ASM
C170	ASM	NO_ASM	NO_ASM
C178	ASM	NO_ASM	NO_ASM
C190	ASM	NO_ASM	NO_ASM
R31	ASM	NO_ASM	NO_ASM

RP-1	ADXL322	STMicro	No Accel.
R172	ASM	ASM	NO_ASM
R173	ASM	ASM	NO_ASM
U9	NO_ASM	LIS2L02AL	NO_ASM
Q105	ASM	ASM	NO_ASM
D97	ASM	ASM	NO_ASM
R956	NO_ASM	ASM	NO_ASM
R62	ASM	ASM	NO_ASM
R885	10 Ohm	10 Ohm	NO_ASM
C829	ASM	ASM	NO_ASM
C969	ASM	ASM	NO_ASM
R959	ASM	ASM	NO_ASM
C830	NO_ASM	0.033UF	NO_ASM
C847	NO_ASM	0.033UF	NO_ASM

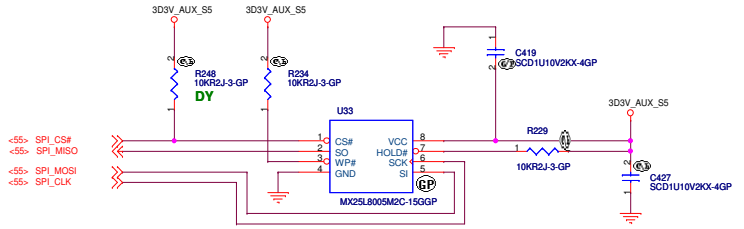
A-note 2.0 LED's Location and Sequence

Left side — Right side

WLAN Bluetooth Battery Suspend



SPI ROM for System & KBC



1. MXIC MX25L8005M2C
2. WINBOND W25X80
3. SST 8Mbit72.25080.G01

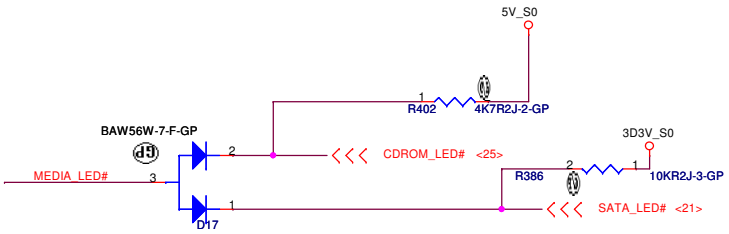
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

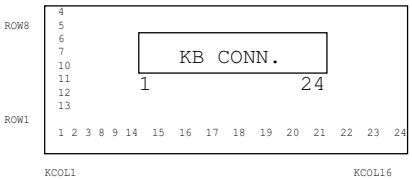
Title: ***G-sensor / SPI / LEDs***

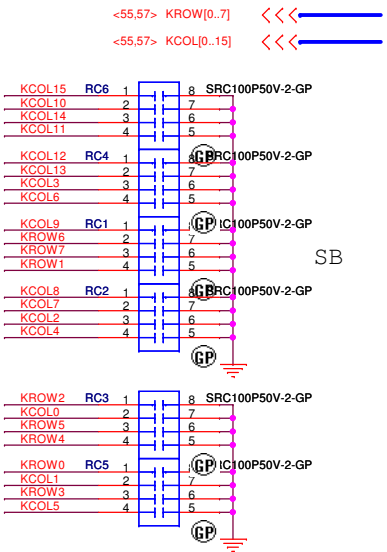
Size: C | Document Number: **Anote2.0 INTEL** | Rev: **SC**

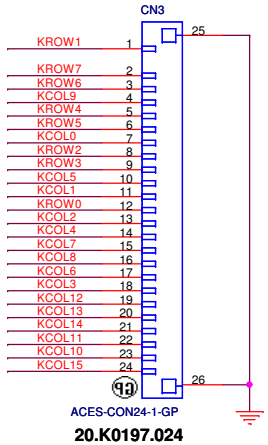
Date: Friday, January 12, 2007 | Sheet 53 of 58



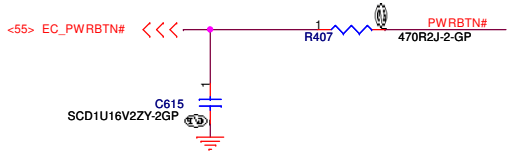
Internal KeyBoard Connector

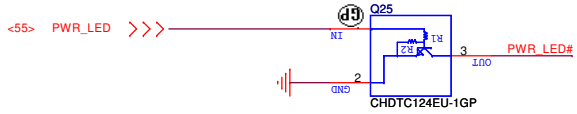


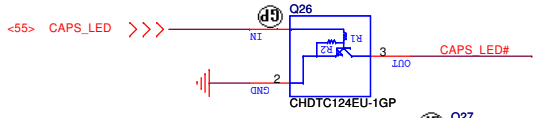


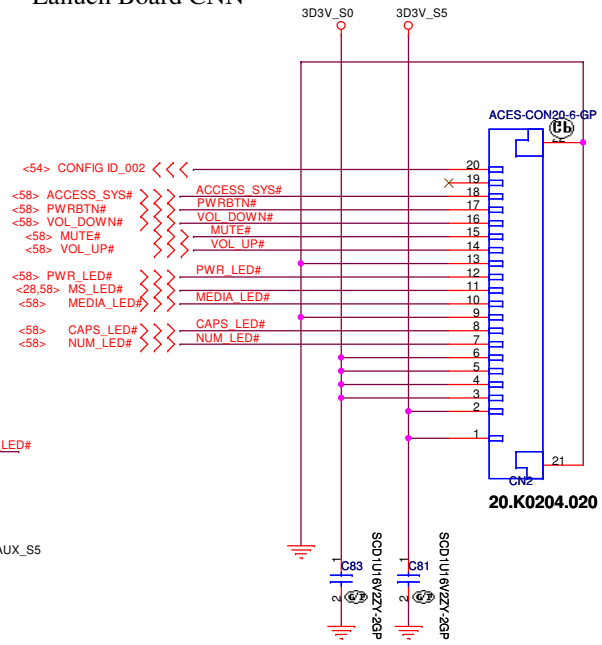


Lanuch Board CNN



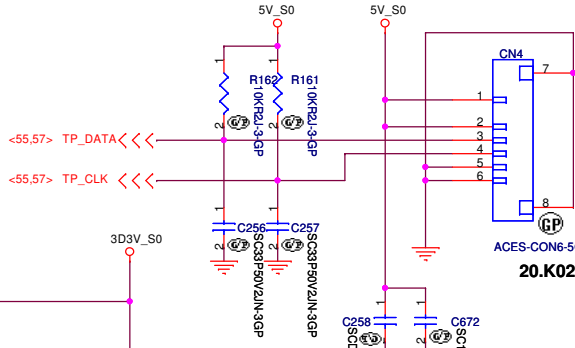


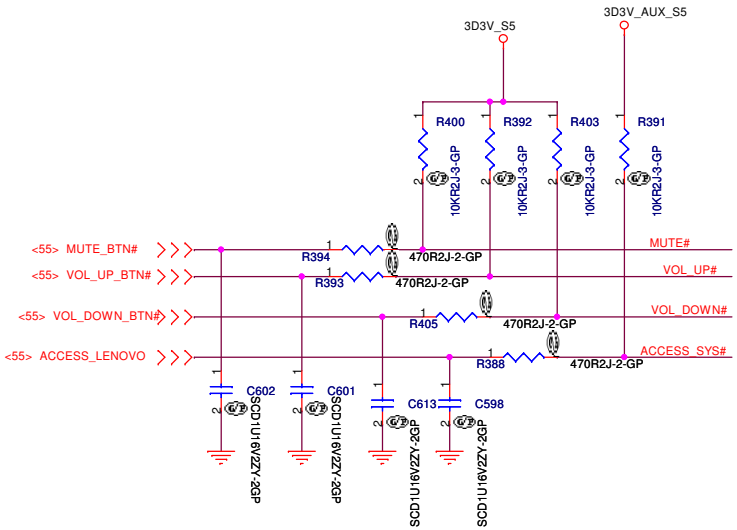




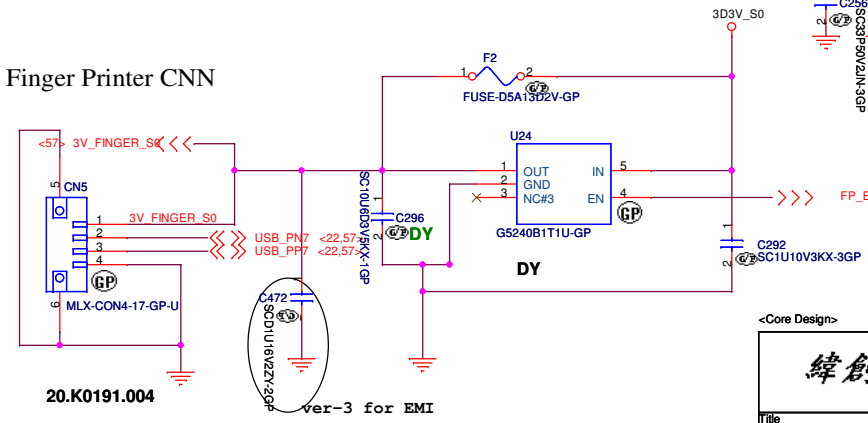
LAB2 20.K0204.020

TouchPad Connector





Finger Printer CNN



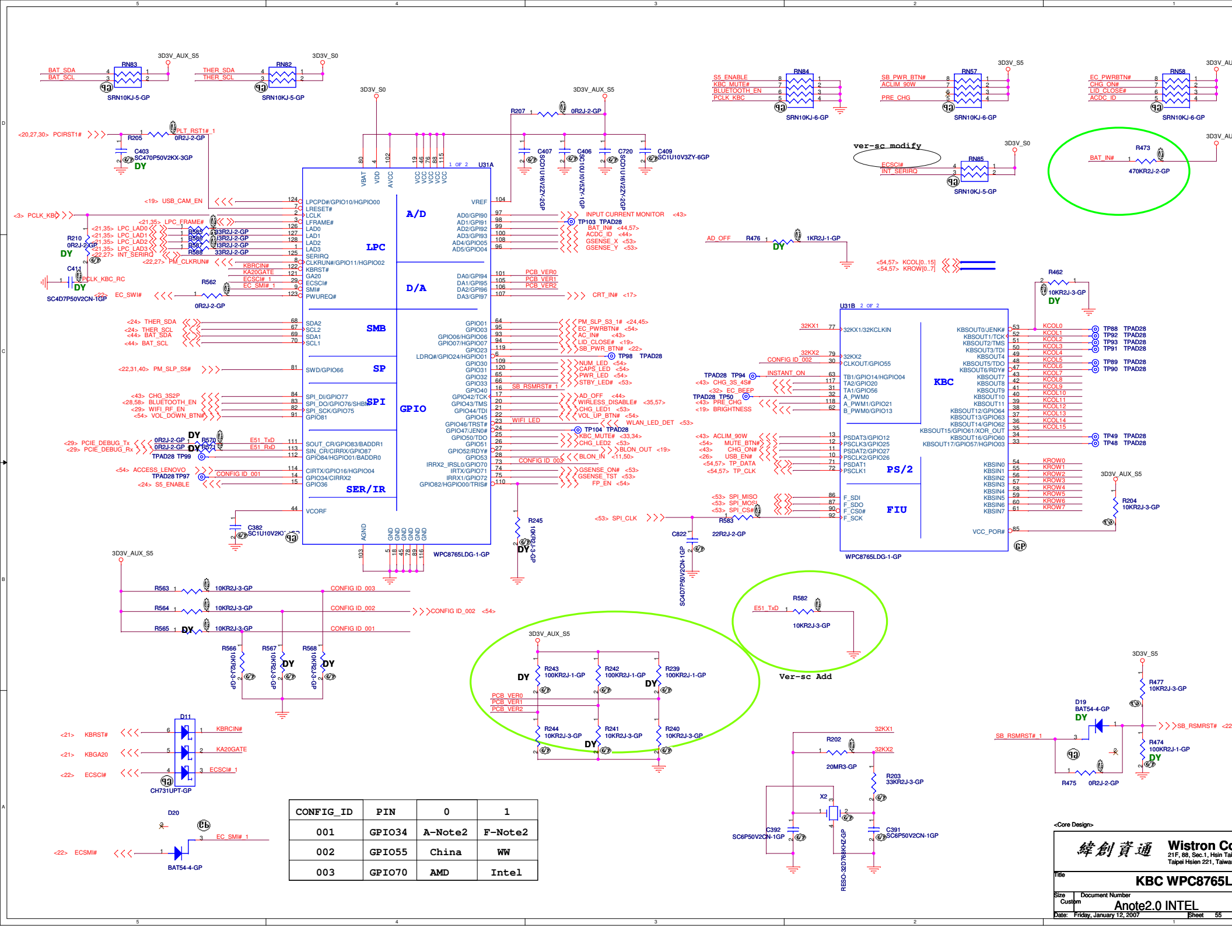
<Core Design>

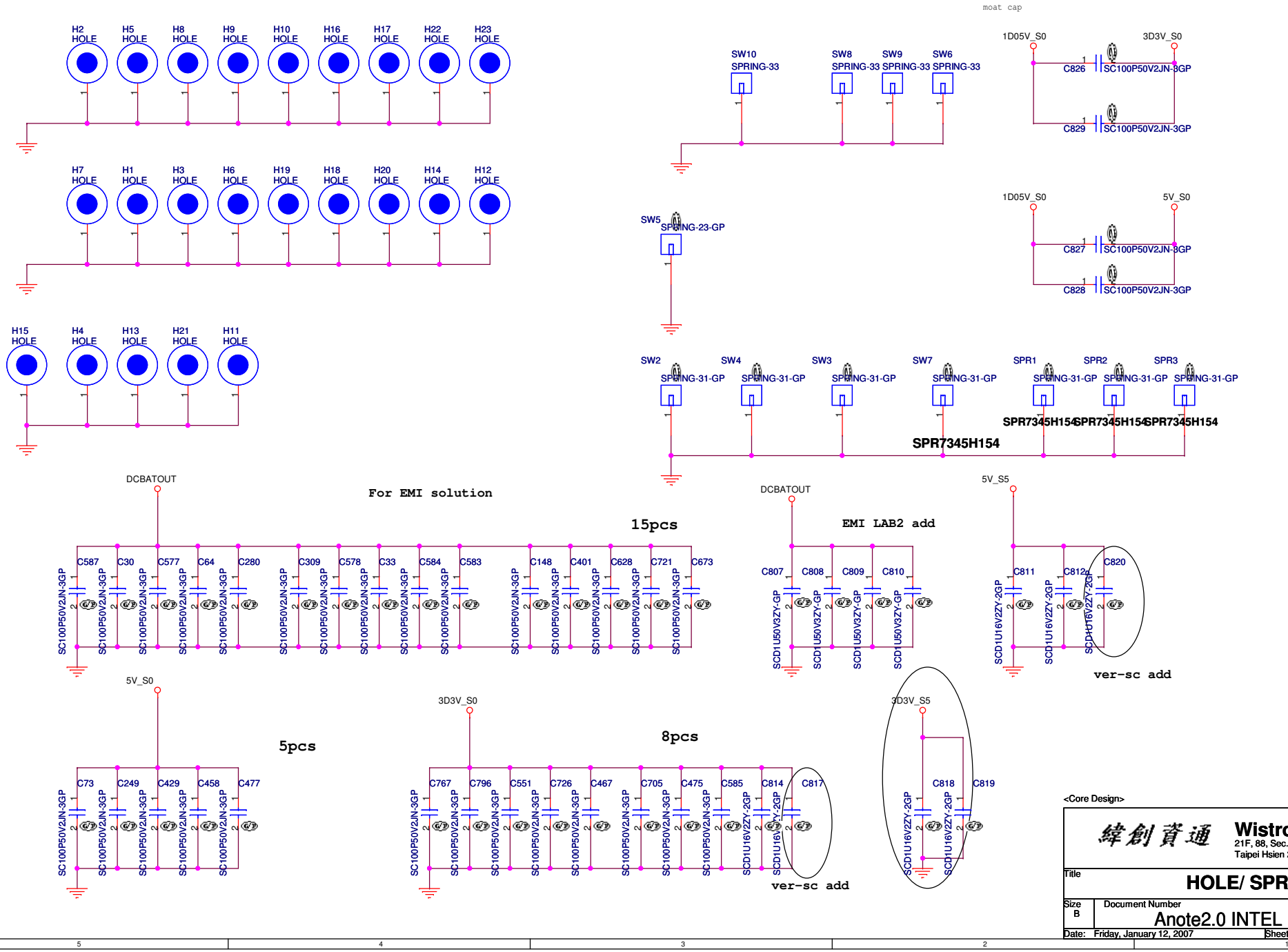
緯創資通 Wistron Corpora
21F, 88, Sec.1, Hsin Tai Wu Rd., Hs
Taipei Hsien 221, Taiwan, R.O.C.

Title: Keyboard /Touch Pad

Size: A3 | Document Number: Anote2.0 INTEL

Date: Friday, January 12, 2007 | Sheet 54 of


U31A
WPC8765LDG-1-GP
U31B 2 OF 2
A/D
D/A
SMB
SP
SPI
GPIO
LPC
SER/IR
KBC
PS/2
FIU
ver-sc modify
Ver-sc Add
CONFIG_ID | PIN | 0 | 1
001 | GPIO34 | A-Note2 | F-Note2
002 | GPIO55 | China | WW
003 | GPIO70 | AMD | Intel
Wistron Co
KBC WPC8765L
Anote2.0 INTEL
Friday, January 12, 2007



<Core Design>

緯創資通 Wistron Corpor
21F, 88, Sec.1, Hsin Tai Wu Rd., H
Taipei Hsien 221, Taiwan, R.O.C.

Title: HOLE/ SPRING

Size: B | Document Number: Anote2.0 INTEL

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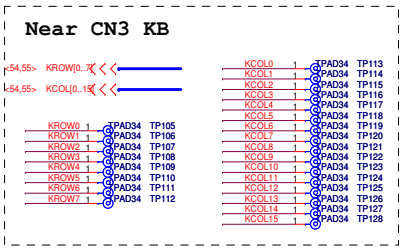

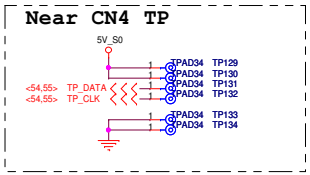

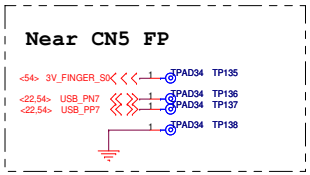

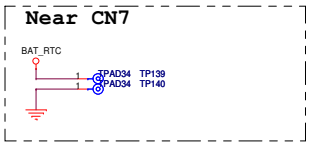

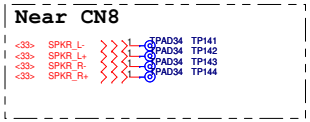

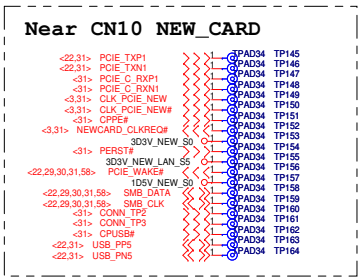

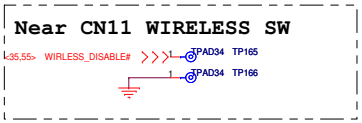

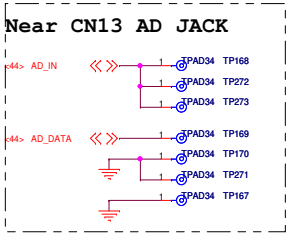

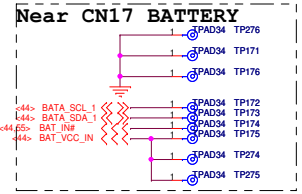

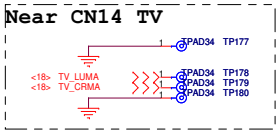

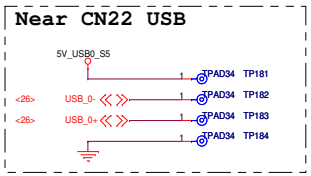

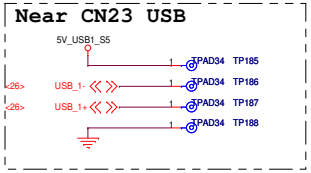

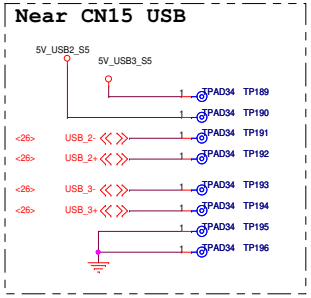

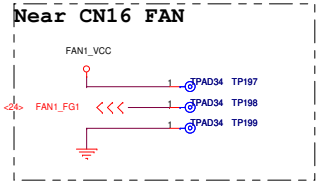

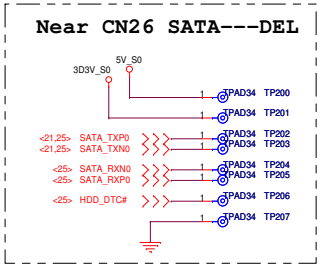

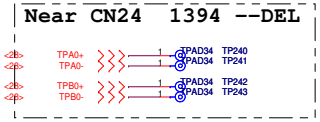

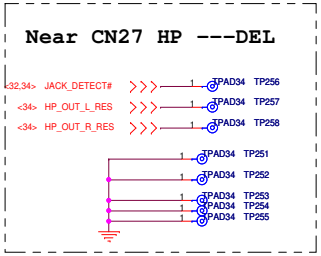

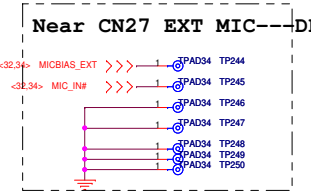

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **TEST_PAD**

Size	Document Number	Rev
C	Anote2.0 INTEL	SC

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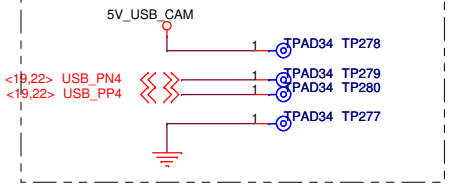
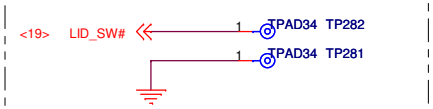
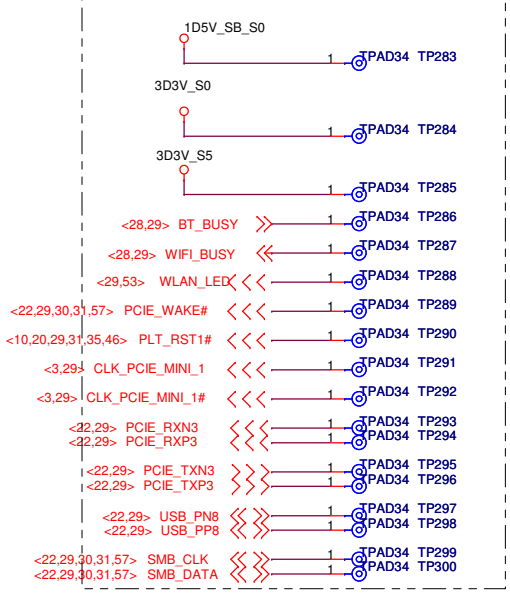
Near LCD CNN--CAM



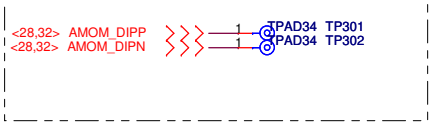
Near SW1



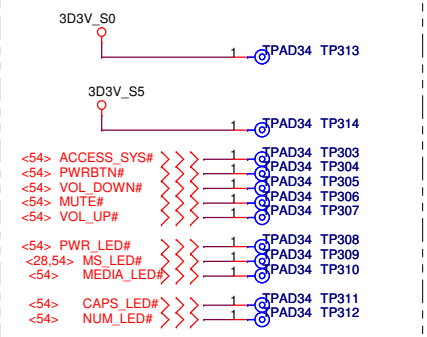
Near CN25--Mini -PCIE



Modem



Launch-BD



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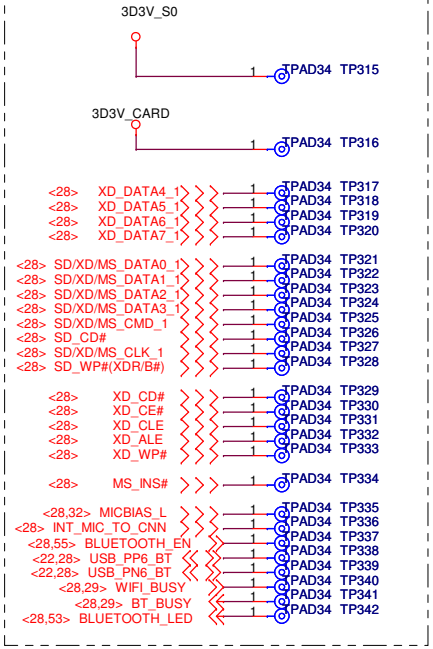

<Core Design>

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Title: TEST_PAD

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