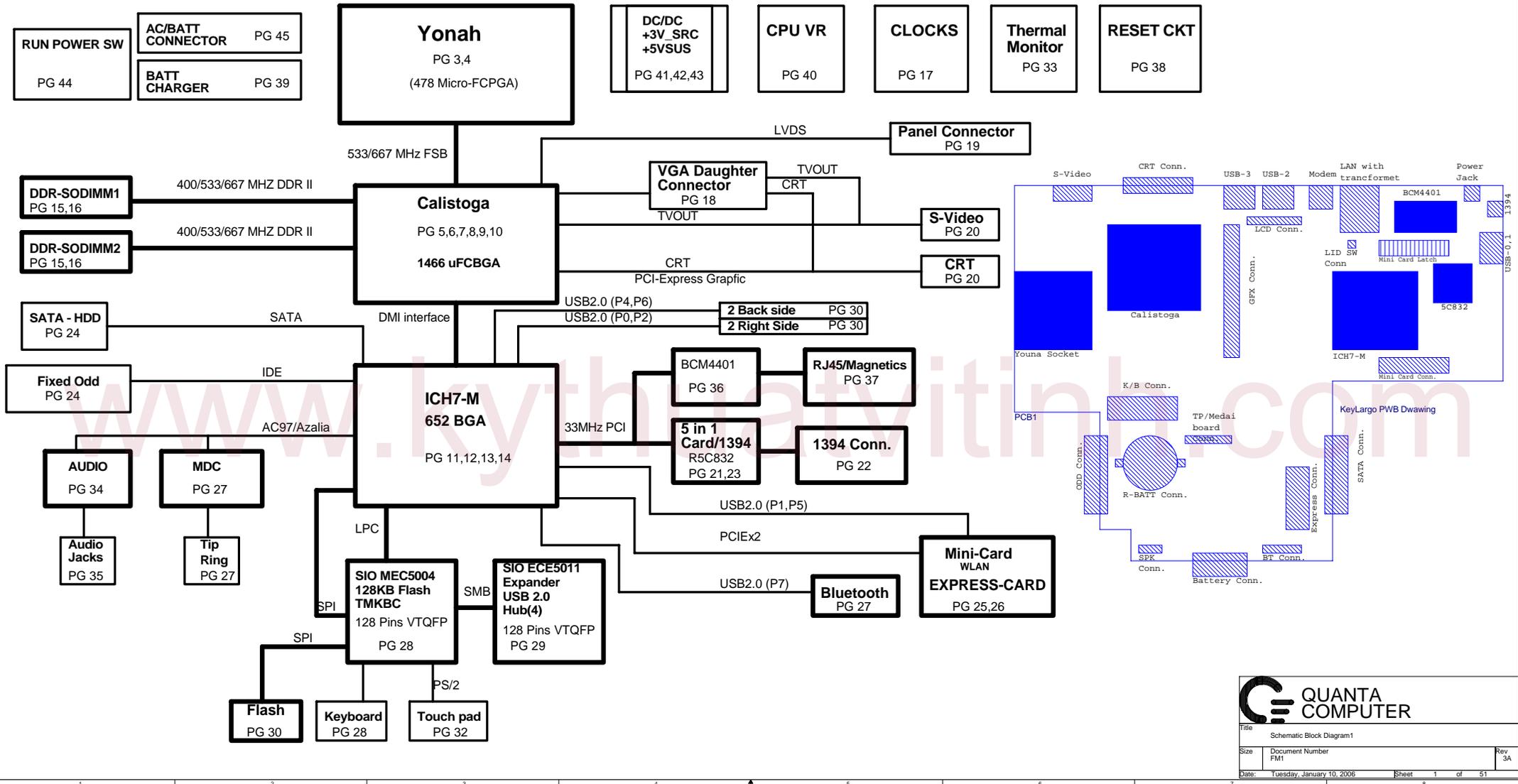


# KEYLARGO-Discrete

VER : 3A

01



**QUANTA COMPUTER**

Title: Schematic Block Diagram 1

Size	Document Number	Rev
	FM1	3A
Date:	Tuesday, January 10, 2006	Sheet 1 of 51

INDEX

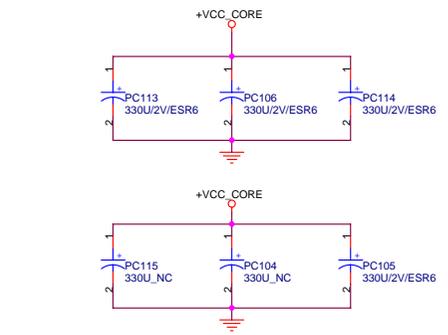
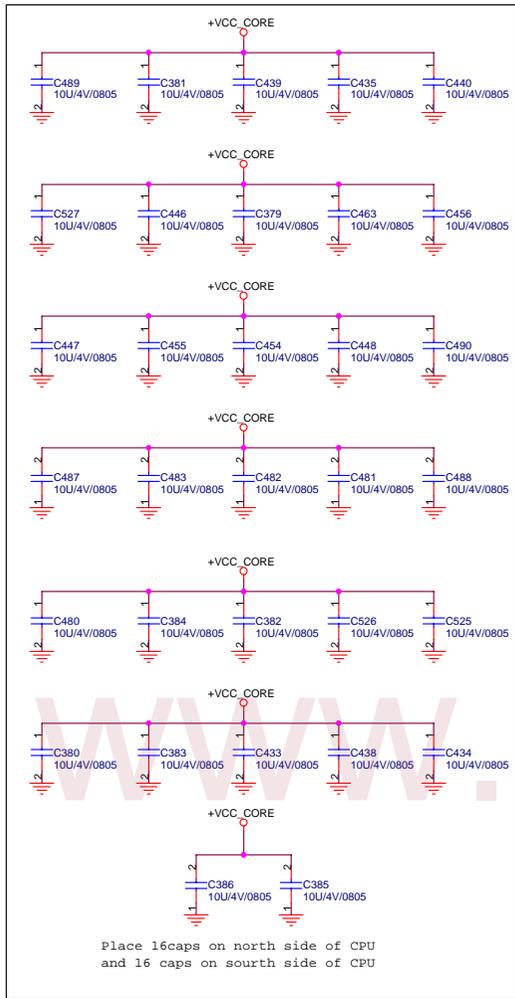
Pg#	Description	DNI LIST
1	Schematic Block Diagram 1	
2	Blank Page	
3	Front Page	
4-5	Dothan	
6-10	Alviso	
11-13	ICH6	
14-15	DDRII SO-DIMM(200P)	
16	Clock Generator	
17	CH7306/7	
18-19	Blank Pages	
20	LCD Conn. & SSP	
21	CRT & TV Conn.	
22	SATA & IDE Conn.	
23	Screw Hole	
24	TI PIC6515	
25	Mini PCI Conn.	
26	MDC Conn.	
27-28	SIO (LPC47N354)	
29	SERIAL PORT & USB	
30	PARALLEL CONN.	
31	Flash ROM	
32	TOUCH PAD & BLUE TOOTH	
33	Switch Board Conn. & LED	
34	FAN & Thermal	
35-36	Audio CODEC (STAC9751) & Phone Jack	
37-38	LOM (BCM5751), Switch	
39	FIR	
40-41	Docking Conn. & Q-Switch	
42	Power Good	
43-44	Battery Selector & Charger	
45	CPU Power	
46	1.8V,0.9V,1.5V,1.05V	
47	3VALW/5V/3V/Power ON	
48	RUN Power Switch	
49	VGA DC/DC	
50	DCIN/Batt Conn.	

Power & Ground

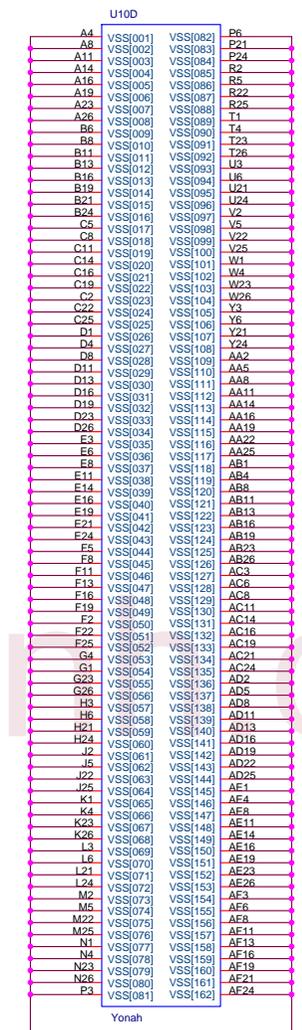
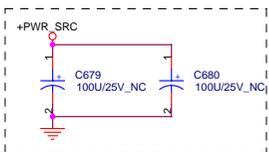
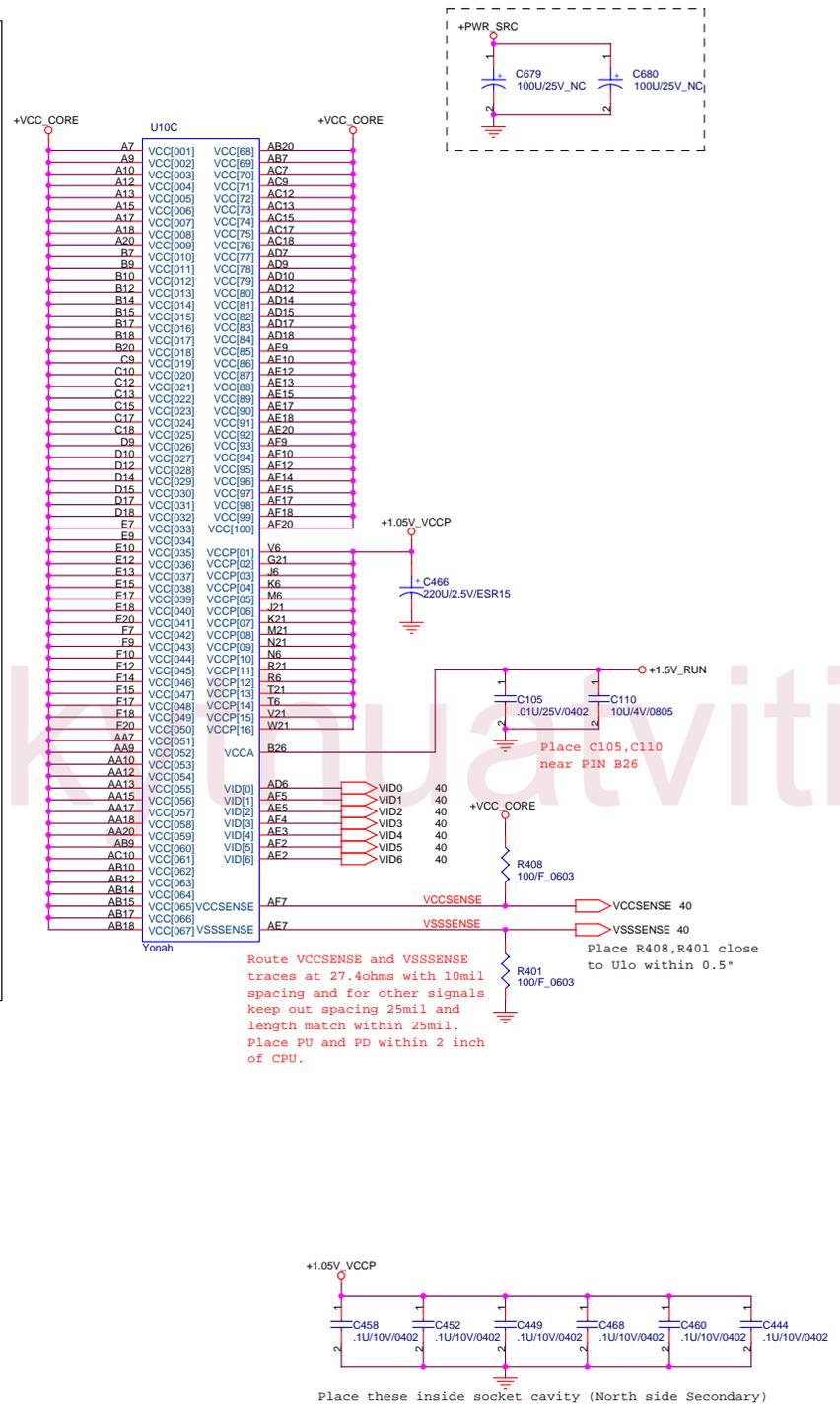
02

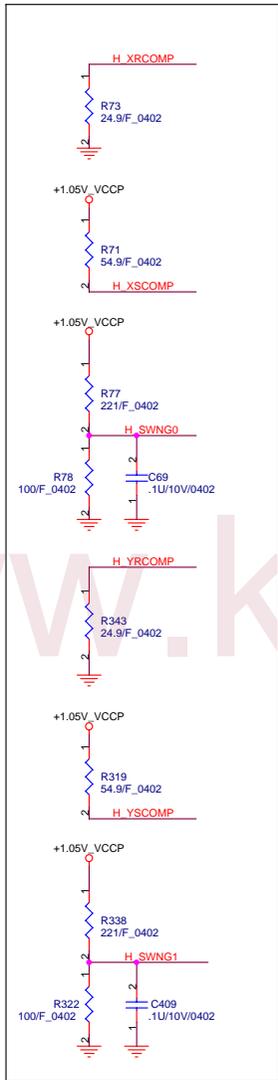
Label	Pg#	Description	Control Signal
DC_IN+		AC ADAPTER (20V)	
PBATT+		MAIN BATTERY + (10-17V)	
PWR_SRC		MAIN POWER (10-20V)	
RTC_PWR3_3V		RTC & PCL POWER (3_3V)	
+12V		+12V	DRUNPWROK
VHCORE		CPU CORE POWER (1.25/1.15V)	RUNPWROK
V1_2RUN		AGTL+ POWER (1.2V)	RUNPWROK
+3VRUN		SLP_S3# CTRLD POWER	RUN_ON
+3VSUS		SLP_S5# CTRLD POWER	SUS_ON
+5VALW		8051 POWER (5V)	
+5VRUN		SLP_S3# CTRLD POWER	RUN_ON
+5VSUS		SLP_S5# CTRLD POWER	SUS_ON
+5VHDD		HDD POWER (5V)	HDDC_EN#
+5VMOD		MODULE POWER (5V)	MODC_EN#
STRB#5V		EXTERNAL FDD POWER (5V)	FDD/LPT#
+5VFAN1, +5VFAN2		FAN POWER (5V)	FAN_OFF/ON#
VDDA		AUDIO ANALOG POWER (5V)	RUN_ON
1_8VSUS		RESUME WELL IN ICH	
1_8VRUN		SLP_S3# CTRLD POWER	
+3VALW		8051 POWER (3V)	
V1_5RUN		AGP I/O POWER	
 GND	ALL PAGES	DIGITAL GROUND	
 GNDP		CPU POWER GND	
 CGNDP		CHARGER GND	
 DGNDP		DC/DC POWER GND	
 LANGND		COMBO CONN GND	



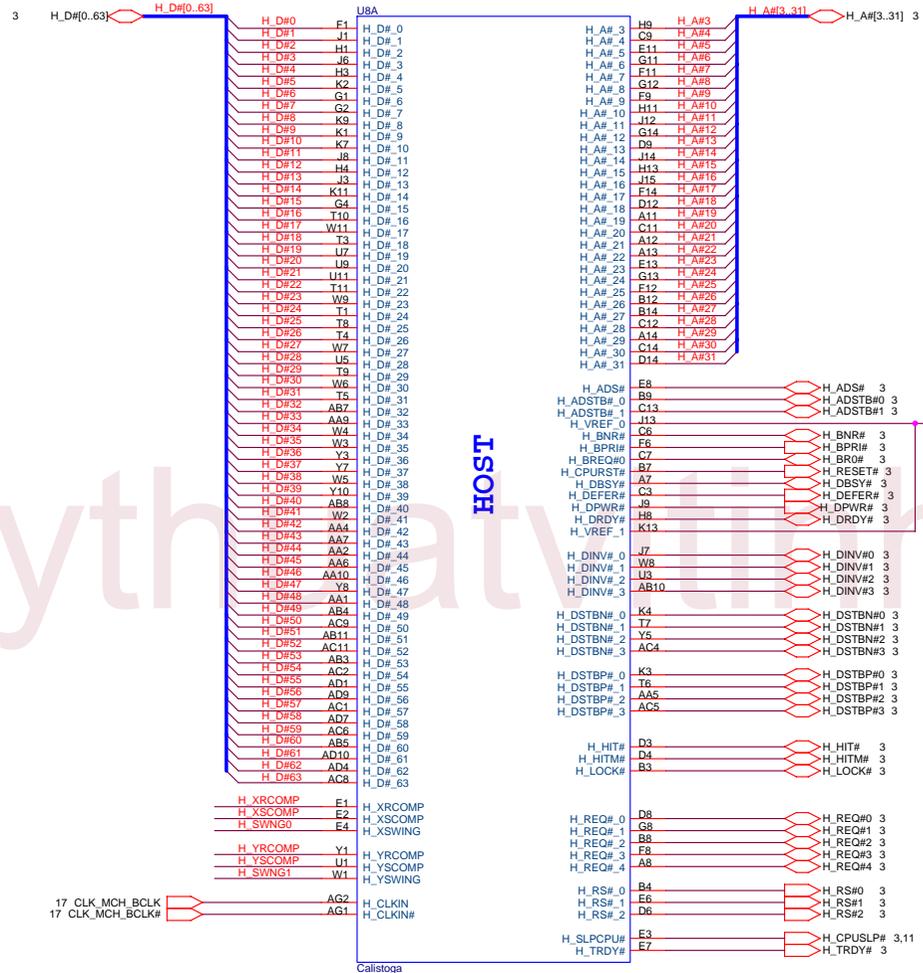


Total caps = 2684 uF  
ESR = 6m ohm/4 // 3m ohm/32





H\_XRCOMP, H\_XSCOMP, H\_YRCOMP, H\_YSCOMP, H\_SWNG0, H\_SWNG1 used W:10/S:20 mil.  
 R & C of H\_XRCOMP, H\_XSCOMP, H\_YRCOMP, H\_YSCOMP, H\_SWNG0, H\_SWNG1 trace length less 0.5" from U3



QUANTA  
COMPUTER

Title: Callistoga (Host)

Size: Document Number FM1

Date: Tuesday, January 10, 2006

Sheet: 5 of 51

Rev: 3A



15 DDR\_A\_D[0..63]

DDR_A_D0	AJ35	SA_DQ0
DDR_A_D1	AJ34	SA_DQ1
DDR_A_D2	AM31	SA_DQ2
DDR_A_D3	AK33	SA_DQ3
DDR_A_D4	AJ36	SA_DQ4
DDR_A_D5	AK35	SA_DQ5
DDR_A_D6	AJ32	SA_DQ6
DDR_A_D7	AL311	SA_DQ7
DDR_A_D8	AN35	SA_DQ8
DDR_A_D9	AP33	SA_DQ9
DDR_A_D10	AR31	SA_DQ10
DDR_A_D11	AP31	SA_DQ11
DDR_A_D12	AN38	SA_DQ12
DDR_A_D13	AM36	SA_DQ13
DDR_A_D14	AM34	SA_DQ14
DDR_A_D15	AK33	SA_DQ15
DDR_A_D16	AK26	SA_DQ16
DDR_A_D17	AL27	SA_DQ17
DDR_A_D18	AM26	SA_DQ18
DDR_A_D19	AN24	SA_DQ19
DDR_A_D20	AK28	SA_DQ20
DDR_A_D21	AL28	SA_DQ21
DDR_A_D22	AM24	SA_DQ22
DDR_A_D23	AP28	SA_DQ23
DDR_A_D24	AN24	SA_DQ24
DDR_A_D25	AL22	SA_DQ25
DDR_A_D26	AP21	SA_DQ26
DDR_A_D27	AN20	SA_DQ27
DDR_A_D28	AL23	SA_DQ28
DDR_A_D29	AP24	SA_DQ29
DDR_A_D30	AP20	SA_DQ30
DDR_A_D31	AT21	SA_DQ31
DDR_A_D32	AR12	SA_DQ32
DDR_A_D33	AR14	SA_DQ33
DDR_A_D34	AP13	SA_DQ34
DDR_A_D35	AP12	SA_DQ35
DDR_A_D36	AT13	SA_DQ36
DDR_A_D37	AT12	SA_DQ37
DDR_A_D38	AL14	SA_DQ38
DDR_A_D39	AL12	SA_DQ39
DDR_A_D40	AK9	SA_DQ40
DDR_A_D41	AN7	SA_DQ41
DDR_A_D42	AK8	SA_DQ42
DDR_A_D43	AK7	SA_DQ43
DDR_A_D44	AP9	SA_DQ44
DDR_A_D45	AN9	SA_DQ45
DDR_A_D46	AT5	SA_DQ46
DDR_A_D47	AL5	SA_DQ47
DDR_A_D48	AY2	SA_DQ48
DDR_A_D49	AW2	SA_DQ49
DDR_A_D50	AP1	SA_DQ50
DDR_A_D51	AN2	SA_DQ51
DDR_A_D52	AV2	SA_DQ52
DDR_A_D53	AT3	SA_DQ53
DDR_A_D54	AN1	SA_DQ54
DDR_A_D55	AL2	SA_DQ55
DDR_A_D56	AG7	SA_DQ56
DDR_A_D57	AF9	SA_DQ57
DDR_A_D58	AG4	SA_DQ58
DDR_A_D59	AF6	SA_DQ59
DDR_A_D60	AG9	SA_DQ60
DDR_A_D61	AH6	SA_DQ61
DDR_A_D62	AF4	SA_DQ62
DDR_A_D63	AF8	SA_DQ63

U8D

DDR SYSTEM MEMORY A

SA_BS_0	AU12	DDR_A_BS0 15,16
SA_BS_1	AV14	DDR_A_BS1 15,16
SA_BS_2	BA20	DDR_A_BS2 15,16
SA_CAS#	AY13	DDR_A_CAS# 15,16
SA_DM_0	AJ33	DDR_A_DM0 15
SA_DM_1	AM35	DDR_A_DM1 15
SA_DM_2	AL26	DDR_A_DM2 15
SA_DM_3	AN22	DDR_A_DM3 15
SA_DM_4	AM14	DDR_A_DM4 15
SA_DM_5	AL9	DDR_A_DM5 15
SA_DM_6	AR3	DDR_A_DM6 15
SA_DM_7	AH4	DDR_A_DM7 15
SA_DQS_0	AK33	DDR_A_DQS0 15
SA_DQS_1	AT33	DDR_A_DQS1 15
SA_DQS_2	AN28	DDR_A_DQS2 15
SA_DQS_3	AM22	DDR_A_DQS3 15
SA_DQS_4	AN12	DDR_A_DQS4 15
SA_DQS_5	AN8	DDR_A_DQS5 15
SA_DQS_6	AP3	DDR_A_DQS6 15
SA_DQS_7	AG5	DDR_A_DQS7 15
SA_DQS#_0	AK32	DDR_A_DQS#0 15
SA_DQS#_1	AU33	DDR_A_DQS#1 15
SA_DQS#_2	AN27	DDR_A_DQS#2 15
SA_DQS#_3	AM21	DDR_A_DQS#3 15
SA_DQS#_4	AM12	DDR_A_DQS#4 15
SA_DQS#_5	AL8	DDR_A_DQS#5 15
SA_DQS#_6	AN3	DDR_A_DQS#6 15
SA_DQS#_7	AH5	DDR_A_DQS#7 15
SA_MA_0	AY16	DDR_A_MA0 15,16
SA_MA_1	AU14	DDR_A_MA1 15,16
SA_MA_2	BA16	DDR_A_MA2 15,16
SA_MA_3	BA17	DDR_A_MA3 15,16
SA_MA_4	AU16	DDR_A_MA4 15,16
SA_MA_5	AU17	DDR_A_MA5 15,16
SA_MA_6	AW17	DDR_A_MA6 15,16
SA_MA_7	AT16	DDR_A_MA7 15,16
SA_MA_8	AU13	DDR_A_MA8 15,16
SA_MA_9	AT17	DDR_A_MA9 15,16
SA_MA_10	AV20	DDR_A_MA10 15,16
SA_MA_11	AV20	DDR_A_MA11 15,16
SA_MA_12	AV12	DDR_A_MA12 15,16
SA_MA_13	AV12	DDR_A_MA13 15,16
SA_RAS#	AW14	DDR_A_RAS# 15,16
SA_RCVENIN#	AK23	DDR_A_WE# 15,16
SA_RCVENOUT#	AK24	DDR_A_WE# 15,16
SA_WE#	AY14	DDR_A_WE# 15,16

Callistoga

15 DDR\_B\_D[0..63]

DDR_B_D0	AK39	SB_DQ0
DDR_B_D1	AJ37	SB_DQ1
DDR_B_D2	AP38	SB_DQ2
DDR_B_D3	AR41	SB_DQ3
DDR_B_D4	AJ38	SB_DQ4
DDR_B_D5	AK38	SB_DQ5
DDR_B_D6	AN41	SB_DQ6
DDR_B_D7	AR41	SB_DQ7
DDR_B_D8	AT40	SB_DQ8
DDR_B_D9	AV41	SB_DQ9
DDR_B_D10	AU38	SB_DQ10
DDR_B_D11	AV38	SB_DQ11
DDR_B_D12	AP38	SB_DQ12
DDR_B_D13	AR40	SB_DQ13
DDR_B_D14	AV38	SB_DQ14
DDR_B_D15	AV38	SB_DQ15
DDR_B_D16	BA38	SB_DQ16
DDR_B_D17	AV36	SB_DQ17
DDR_B_D18	AR36	SB_DQ18
DDR_B_D19	AP36	SB_DQ19
DDR_B_D20	BA36	SB_DQ20
DDR_B_D21	AU36	SB_DQ21
DDR_B_D22	AP35	SB_DQ22
DDR_B_D23	AP34	SB_DQ23
DDR_B_D24	AY33	SB_DQ24
DDR_B_D25	BA33	SB_DQ25
DDR_B_D26	AT31	SB_DQ26
DDR_B_D27	AU29	SB_DQ27
DDR_B_D28	AU31	SB_DQ28
DDR_B_D29	AW31	SB_DQ29
DDR_B_D30	AV28	SB_DQ30
DDR_B_D31	AV29	SB_DQ31
DDR_B_D32	AM19	SB_DQ32
DDR_B_D33	AL19	SB_DQ33
DDR_B_D34	AP14	SB_DQ34
DDR_B_D35	AV14	SB_DQ35
DDR_B_D36	AN17	SB_DQ36
DDR_B_D37	AM16	SB_DQ37
DDR_B_D38	AP15	SB_DQ38
DDR_B_D39	AL15	SB_DQ39
DDR_B_D40	AU11	SB_DQ40
DDR_B_D41	AH10	SB_DQ41
DDR_B_D42	AJ9	SB_DQ42
DDR_B_D43	AN10	SB_DQ43
DDR_B_D44	AK13	SB_DQ44
DDR_B_D45	AH11	SB_DQ45
DDR_B_D46	AK10	SB_DQ46
DDR_B_D47	AJ8	SB_DQ47
DDR_B_D48	BA10	SB_DQ48
DDR_B_D49	AV10	SB_DQ49
DDR_B_D50	BA4	SB_DQ50
DDR_B_D51	AV4	SB_DQ51
DDR_B_D52	AY10	SB_DQ52
DDR_B_D53	AY9	SB_DQ53
DDR_B_D54	AW5	SB_DQ54
DDR_B_D55	AY5	SB_DQ55
DDR_B_D56	AV4	SB_DQ56
DDR_B_D57	AR5	SB_DQ57
DDR_B_D58	AK4	SB_DQ58
DDR_B_D59	AK3	SB_DQ59
DDR_B_D60	AT4	SB_DQ60
DDR_B_D61	AK5	SB_DQ61
DDR_B_D62	AJ5	SB_DQ62
DDR_B_D63	AJ3	SB_DQ63

URE

DDR SYSTEM MEMORY B

SB_BS_0	AT24	DDR_B_BS0 15,16
SB_BS_1	AV23	DDR_B_BS1 15,16
SB_BS_2	AY23	DDR_B_BS2 15,16
SB_BS_2	AY23	DDR_B_CAS# 15,16
SB_CAS#	AR24	DDR_B_DM0 15
SB_DM_0	AK36	DDR_B_DM1 15
SB_DM_1	AR38	DDR_B_DM2 15
SB_DM_2	AT36	DDR_B_DM3 15
SB_DM_3	BA31	DDR_B_DM4 15
SB_DM_4	AL17	DDR_B_DM5 15
SB_DM_5	AH8	DDR_B_DM6 15
SB_DM_6	BA5	DDR_B_DM7 15
SB_DM_7	AN4	DDR_B_DM7 15
SB_DQS_0	AM39	DDR_B_DQS0 15
SB_DQS_1	AT39	DDR_B_DQS1 15
SB_DQS_2	AU35	DDR_B_DQS2 15
SB_DQS_3	AR29	DDR_B_DQS3 15
SB_DQS_4	AR16	DDR_B_DQS4 15
SB_DQS_5	AR10	DDR_B_DQS5 15
SB_DQS_6	AR7	DDR_B_DQS6 15
SB_DQS_7	AN5	DDR_B_DQS7 15
SB_DQS#_0	AM40	DDR_B_DQS#0 15
SB_DQS#_1	AU39	DDR_B_DQS#1 15
SB_DQS#_2	AT35	DDR_B_DQS#2 15
SB_DQS#_3	AP29	DDR_B_DQS#3 15
SB_DQS#_4	AP16	DDR_B_DQS#4 15
SB_DQS#_5	AT10	DDR_B_DQS#5 15
SB_DQS#_6	AT7	DDR_B_DQS#6 15
SB_DQS#_7	AP5	DDR_B_DQS#7 15
SB_MA_0	AY23	DDR_B_MA0 15,16
SB_MA_1	AW24	DDR_B_MA1 15,16
SB_MA_2	AV24	DDR_B_MA2 15,16
SB_MA_3	AR28	DDR_B_MA3 15,16
SB_MA_4	AT27	DDR_B_MA4 15,16
SB_MA_5	AT28	DDR_B_MA5 15,16
SB_MA_6	AU27	DDR_B_MA6 15,16
SB_MA_7	AV28	DDR_B_MA7 15,16
SB_MA_8	AV27	DDR_B_MA8 15,16
SB_MA_9	AW27	DDR_B_MA9 15,16
SB_MA_10	AV24	DDR_B_MA10 15,16
SB_MA_11	BA27	DDR_B_MA11 15,16
SB_MA_12	AY27	DDR_B_MA12 15,16
SB_MA_13	AR23	DDR_B_MA13 15,16
SB_RAS#	AU23	DDR_B_RAS# 15,16
SB_RCVENIN#	AK16	DDR_B_WE# 15,16
SB_RCVENOUT#	AK18	DDR_B_WE# 15,16
SB_WE#	AR27	DDR_B_WE# 15,16

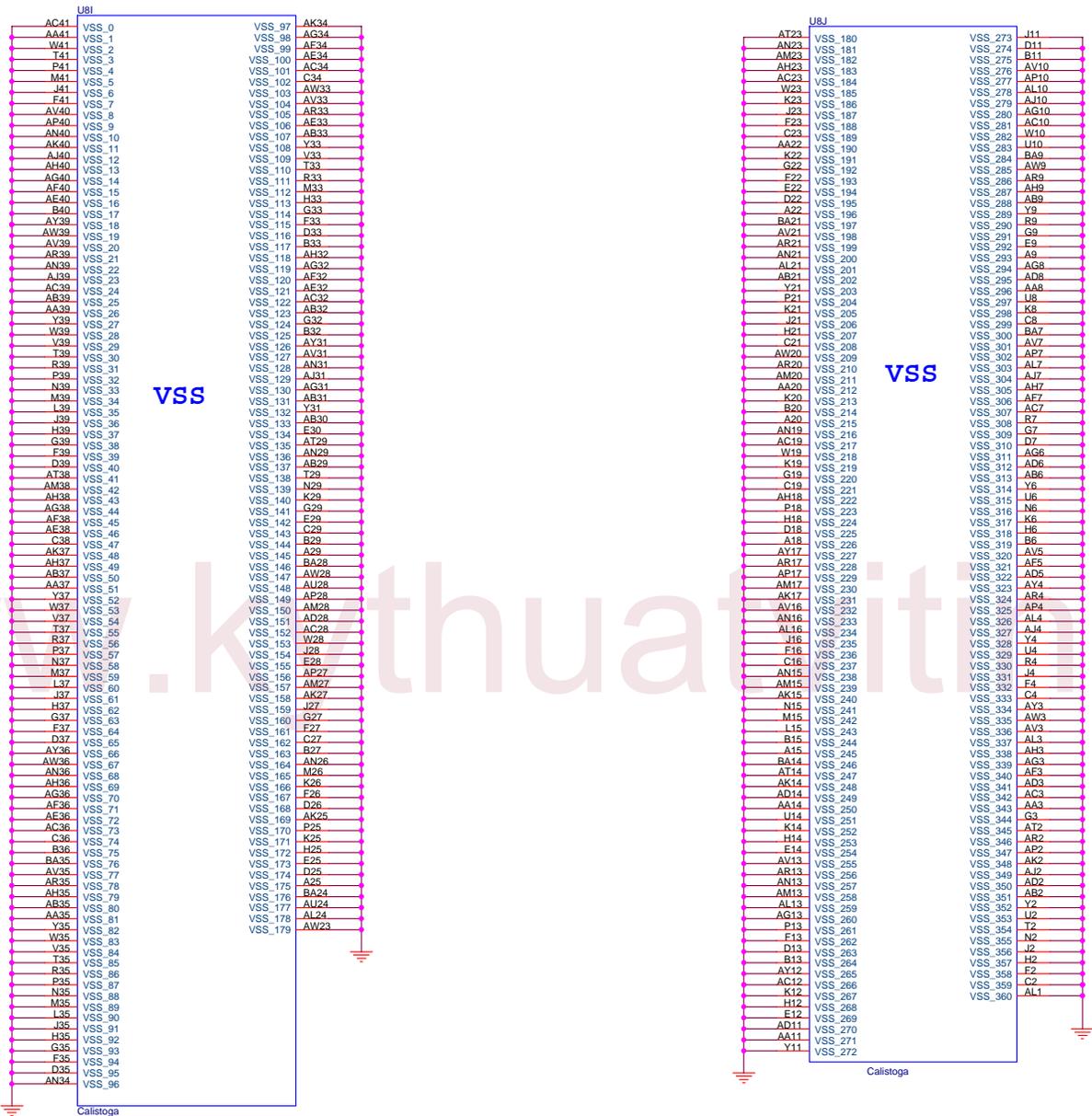
Callistoga



Title	Callistoga (DDR2)		
Size	Document Number	Rev	
	FM1	3A	
Date:	Tuesday, January 10, 2006	Sheet 7 of 51	







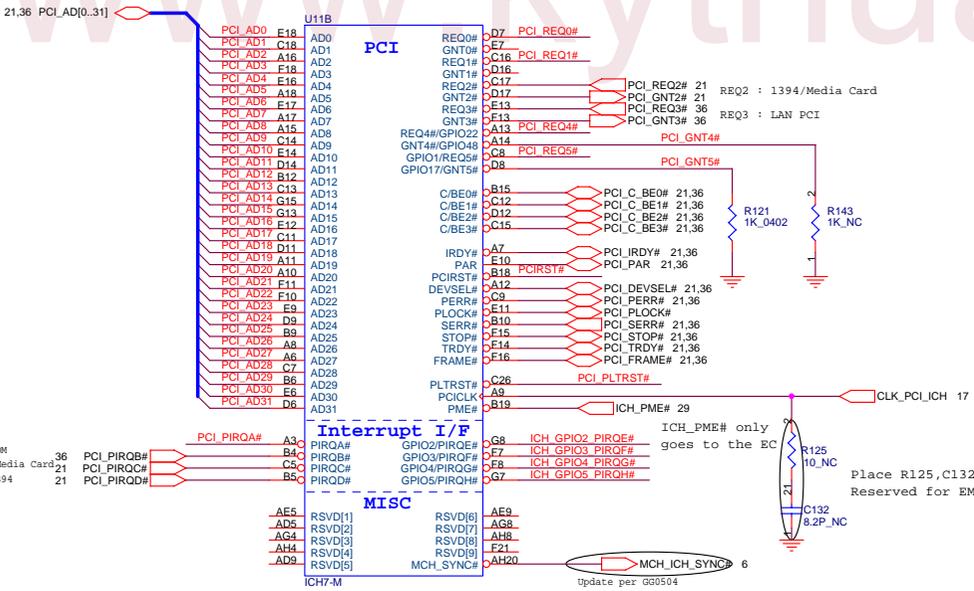
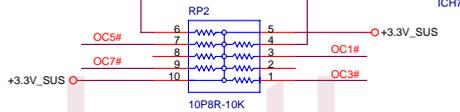
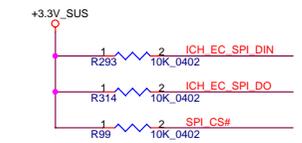
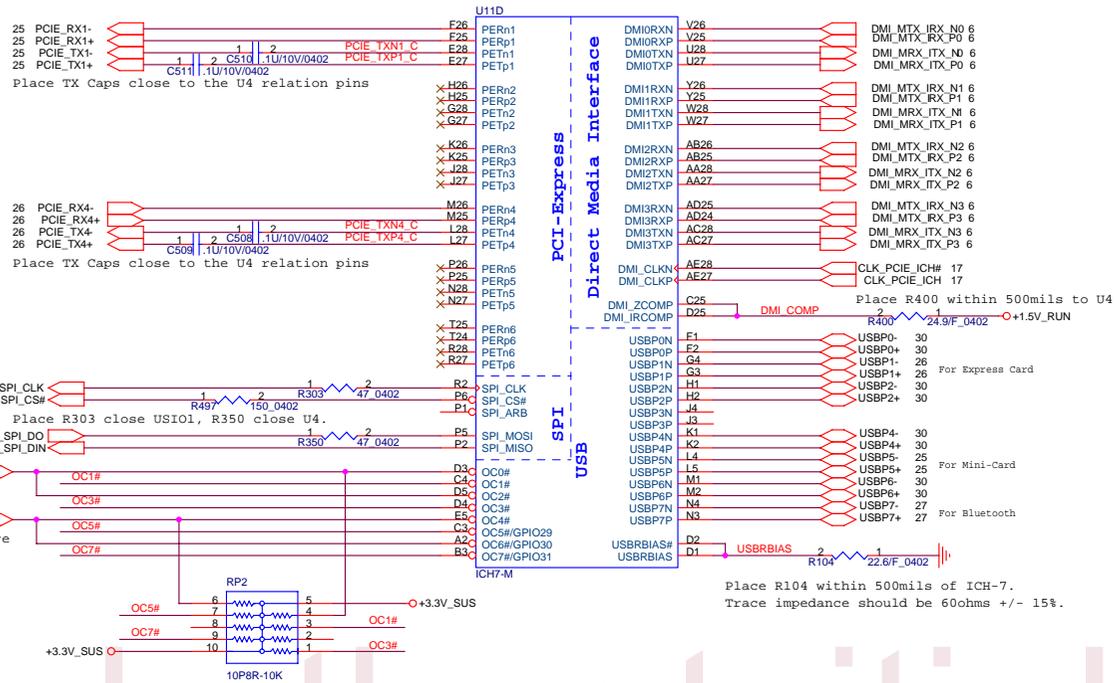
www.kyathuathitech.com

**QUANTA COMPUTER**

Title: Callistoga (VSS,NCTF)

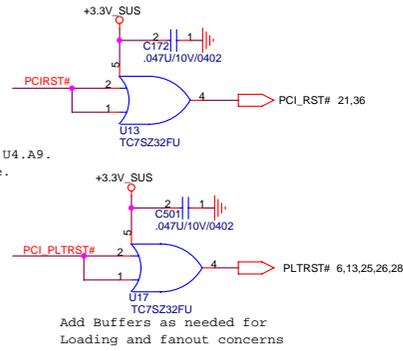
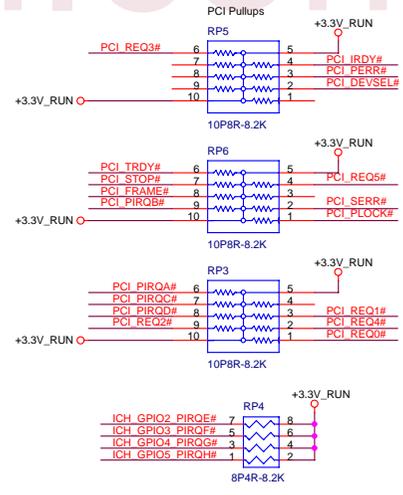
Size: Document Number FM1	Rev: 3A
Date: Tuesday, January 10, 2006	Sheet: 10 of 51





Resister pop options to boot from various sources

	GNT5#	GNT4#
LPC	11	Not Stuff
PCI	10	Not Stuff
SPI	01	Stuff



**QUANTA COMPUTER**

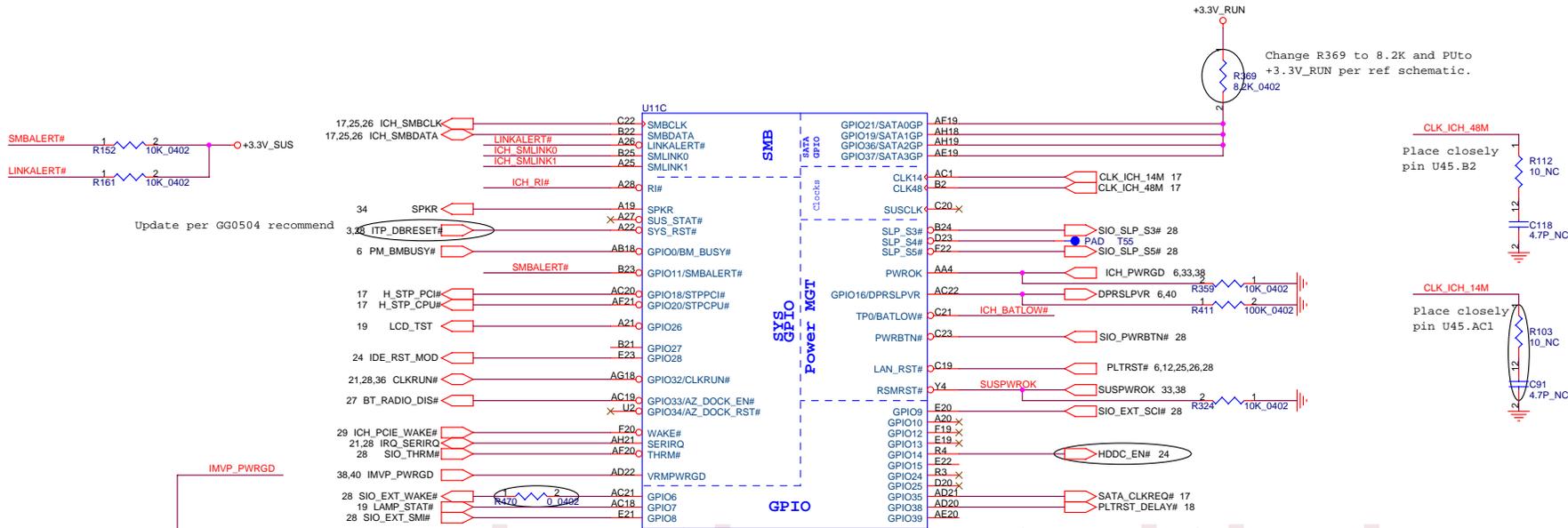
Title: ICH7-M (USB,DMI,PCIE,PCI)

Size: Document Number FM1

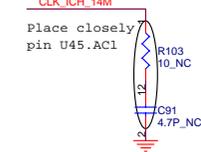
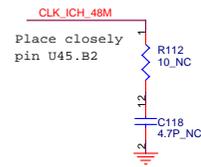
Date: Tuesday, January 10, 2006

Sheet: 12 of 51

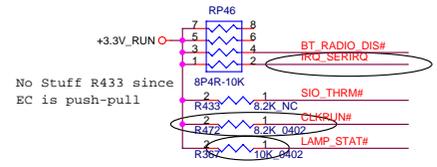
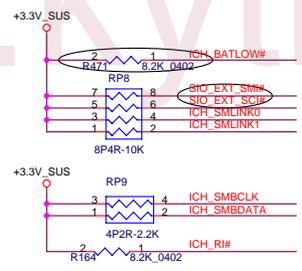
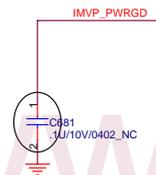
Rev: 3A



+3.3V\_RUN  
 R369 8.2K\_0402  
 Change R369 to 8.2K and PUTO +3.3V\_RUN per ref schematic.

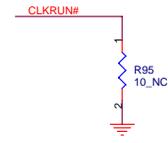


Update per GG0504 recommend



No Stuff R433 since EC is push-pull

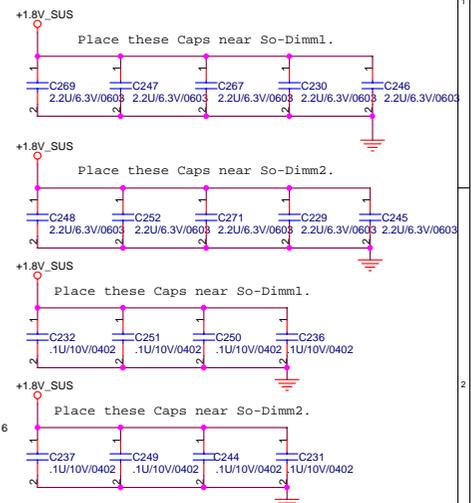
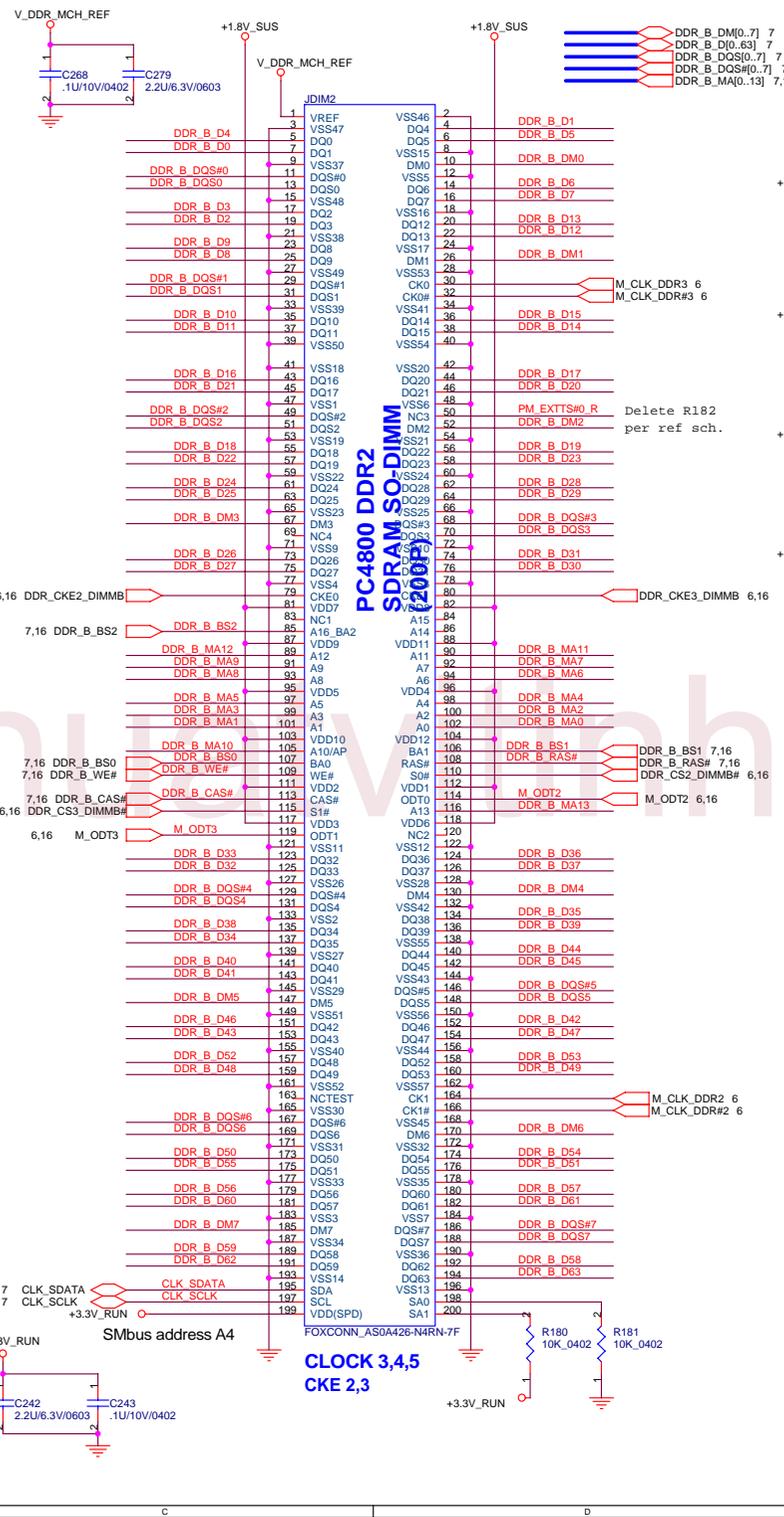
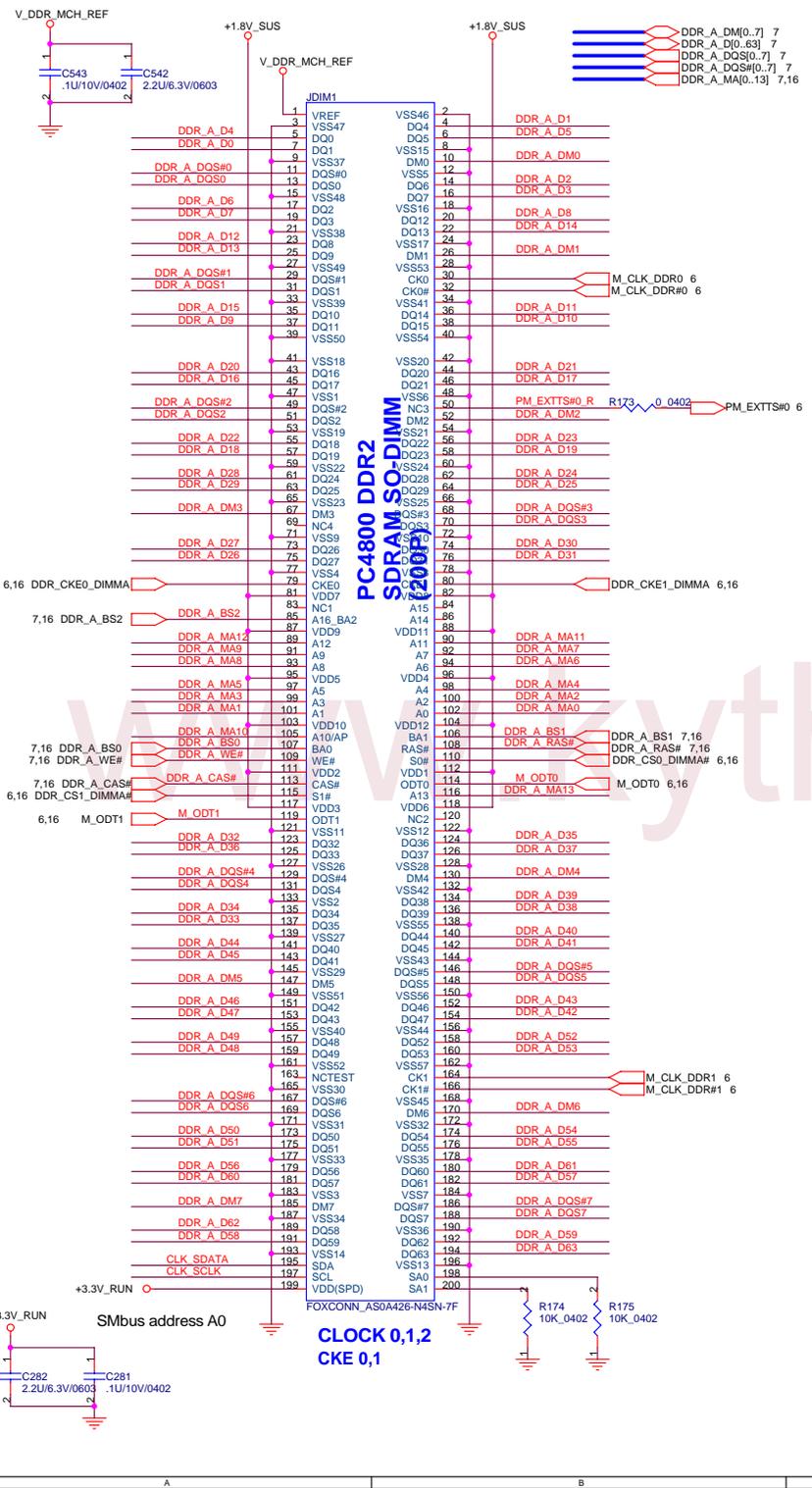
Change R367 from 8.2K to 10K per ref schematic.



Option to "Disable" clkrun. Pulling it down will keep the clks running

www.kythuatvithinh.com





**QUANTA COMPUTER**

Title: System DRAM Expansion (200P-DDR\_SODIMM X 2)

Size: Document Number FM1

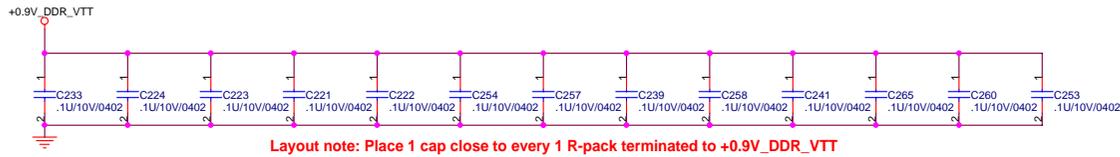
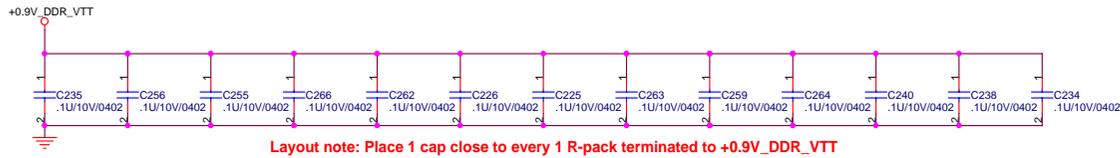
Date: Tuesday, January 10, 2006

Sheet: 15 of 51

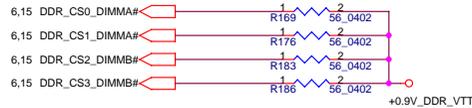
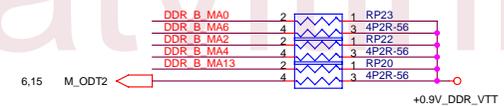
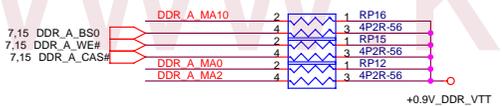
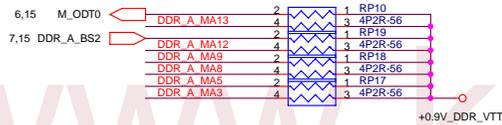
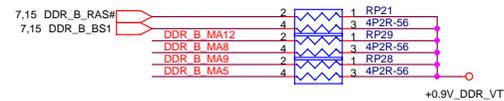
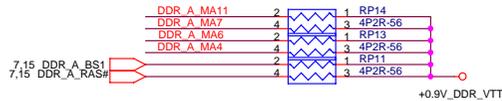
Rev: 3A

DDR\_A\_MA[0..13] 7,15

DDR\_B\_MA[0..13] 7,15



**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9V\_DDR\_VTT

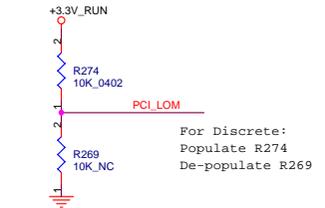
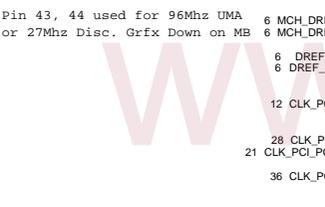
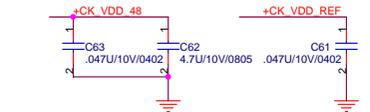


**QUANTA  
COMPUTER**

Title: DDR RES.ARRAY		
Size: FM1	Document Number:	Rev: 3A
Date: Tuesday, January 10, 2006	Sheet: 16	of 51

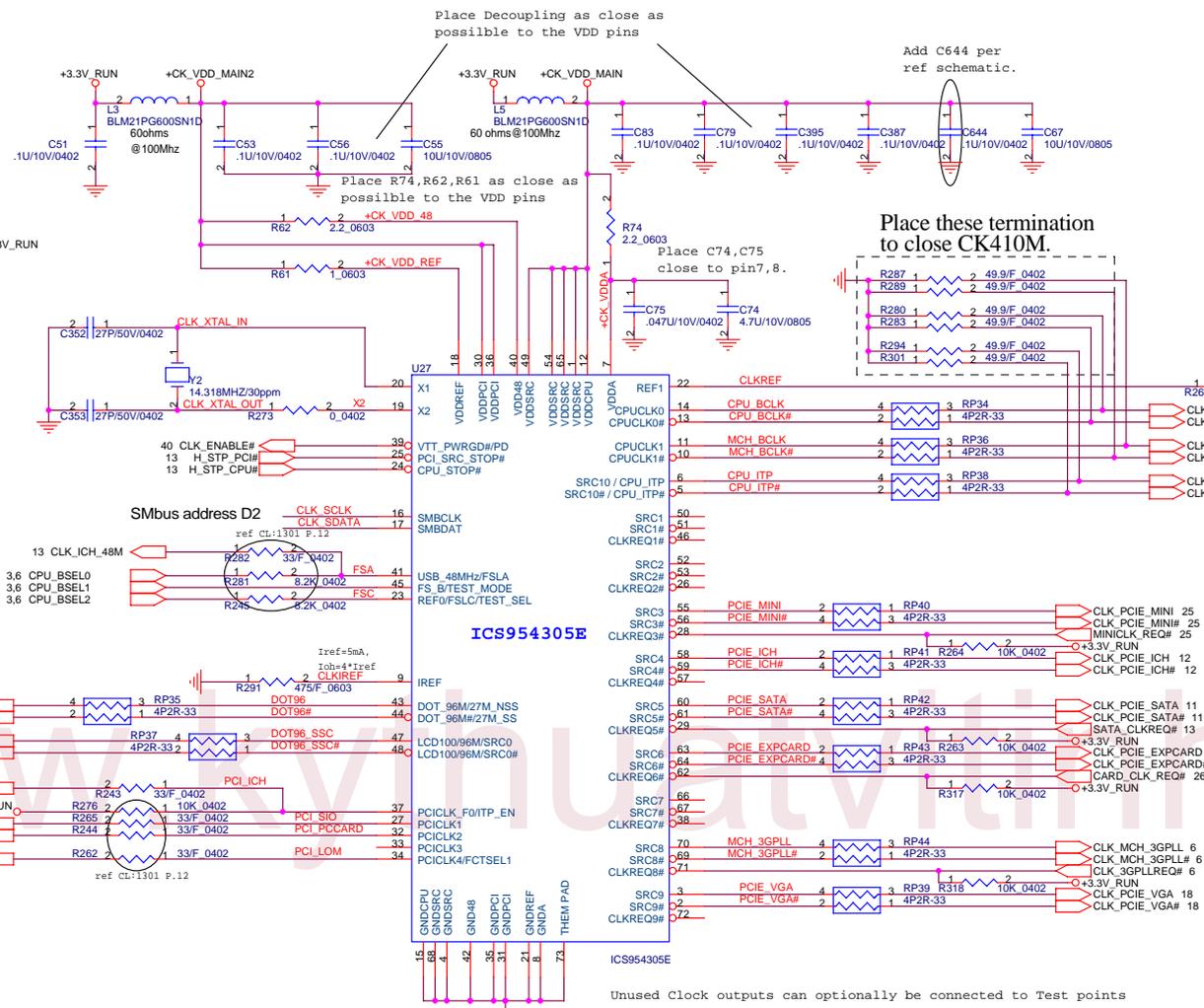
Frequency	BSEL0/FSA	BSEL2/FSC	BSEL1/FSB
100	1	0	1
133	0	0	1
166	0	1	1
200	0	1	0

Trace length between R277, R278 to UJ42 = <=50mils

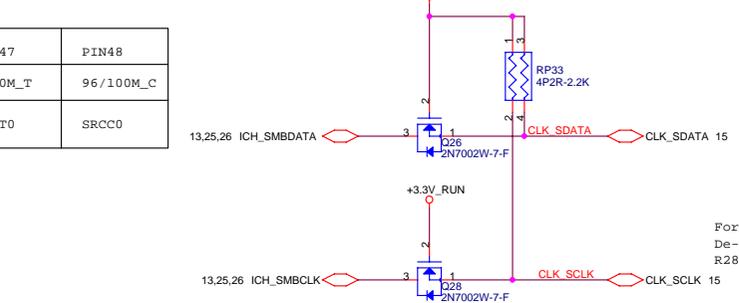


PCI\_LOM = FCTSELL1

FCTSELL1 (PIN34)	PIN43	PIN44	PIN47	PIN48
0 = UMA	DOT96T	DOT96C	96/100M_T	96/100M_C
1 = Disc. GRFX down	27Mout	27MSSout	SRC70	SRCC0



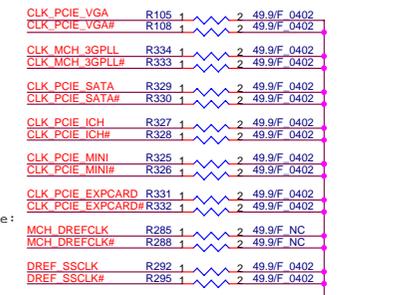
Unused Clock outputs can optionally be connected to Test points



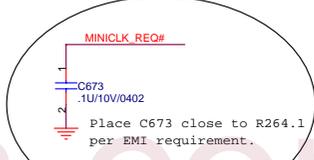
For Discrete: De-populate R285, R288

These are for backdrive issue

Place pull-down termination close to series R per Design Guide



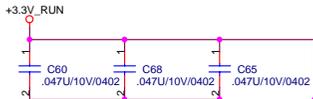
Place these termination to close CK410M.



Populate JVD01 for discrete.

YPRPB\_DET: SIGNAL FROM SVIDEO CONNECTOR, TO SWITCH TO COMPONENT OUT.

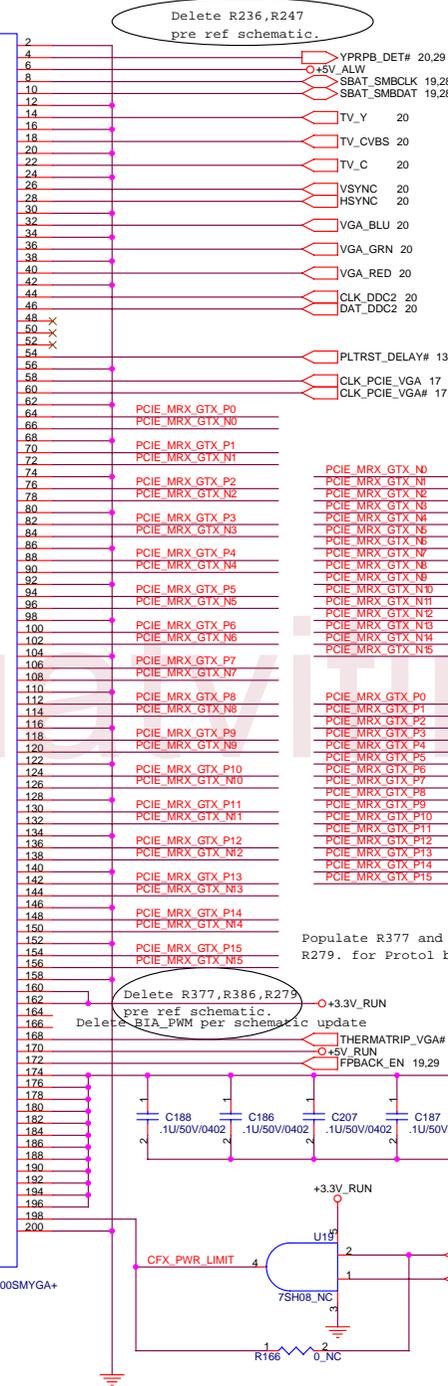
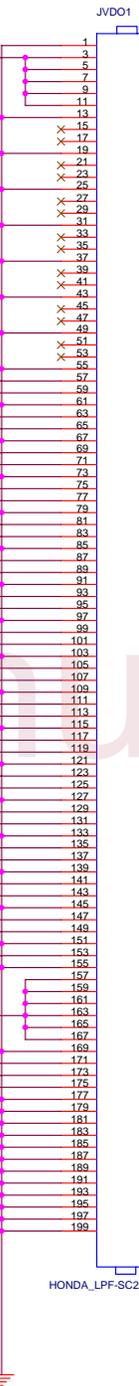
Delete R236,R247 pre ref schematic.



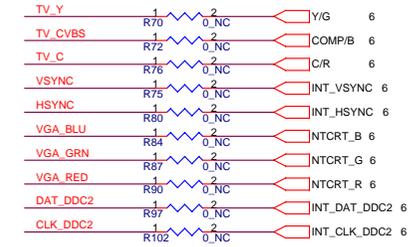
For Discrete: Populate C60,C68,C65

For Discrete: Populate C89,C98,C100,C103,C102,C106,C108,C112,C111,C115,C120,C124,C126,C128,C130,C133,C138,C140,C142,C144,C145,C148,C151,C152,C157,C161,C162,C165,C167,C168,C170,C175

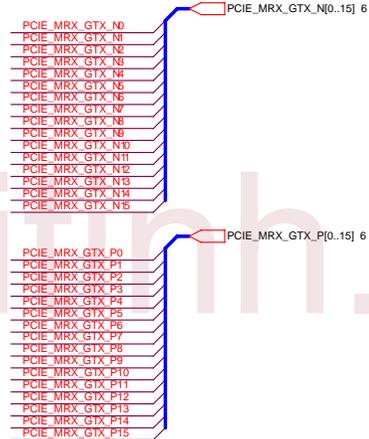
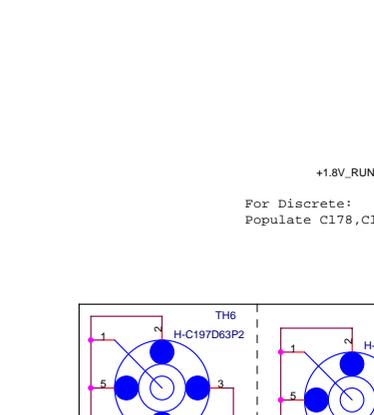
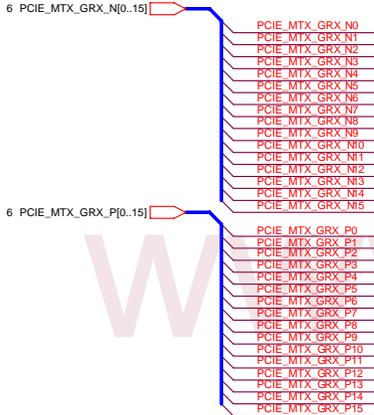
Table listing component values for various PCI Express lanes (e.g., C89, C98, C100, C103, C102, C106, C108, C112, C111, C115, C120, C124, C126, C128, C130, C133, C138, C140, C142, C144, C145, C148, C151, C152, C157, C161, C162, C165, C167, C168, C170, C175).



YPRPB\_DET# 20,29 +5V\_ALW SBAT\_SMBCLK 19,28 SMBUS Address 58 for Inverter. SBAT\_SMBDAT 19,28 SMBUS Address 98 for Temp.sensor.

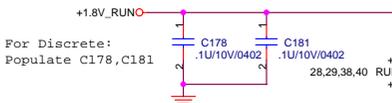


For Discrete: De-populate R70,R72,R76,R75,R80,R84,R87,R90,R97,R02



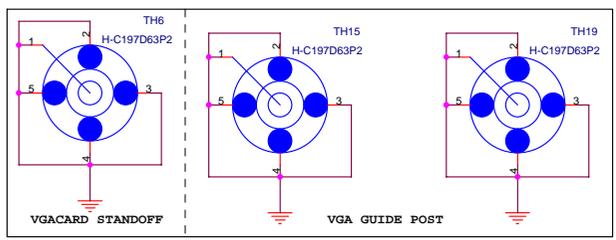
Populate R377 and De-populate R386, R279. for Protol build(old VGA card)

Delete R377,R386,R279 pre ref schematic. Delete BIA\_PWM per schematic update

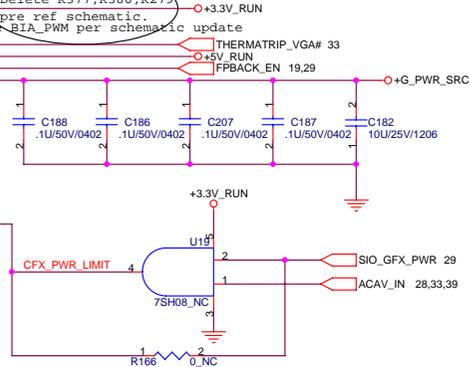


For Discrete: Populate C178,C181

+15V\_SUS RUNPWROK +2.5V\_RUN



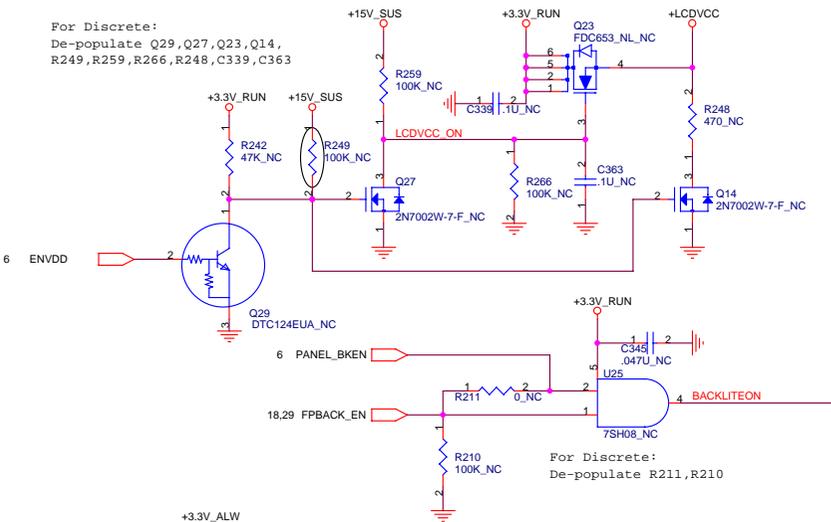
For Discrete: Populate TH6,TH15,TH19 TOP Side



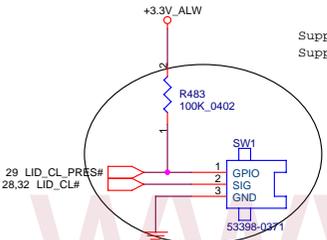
For Discrete: Populate C188,C186,C207,C187,C182,U19



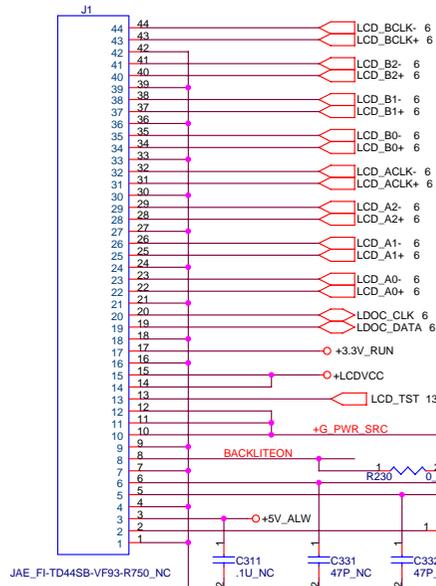
For Discrete:  
De-populate Q29, Q27, Q23, Q14,  
R249, R259, R266, R248, C339, C363



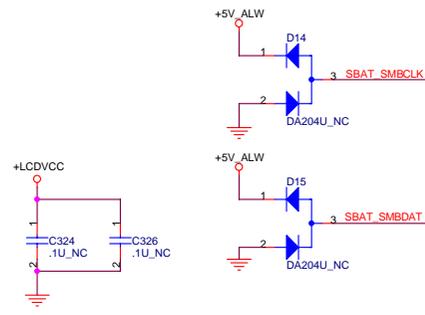
Support M07-Inverter: Populate R230, R211 and Depopulate U8, C345.  
Support D05-Inverter: Depopulate R230, R211 and Populate U8, C345.



Change LID SW to 3 Pins connector.

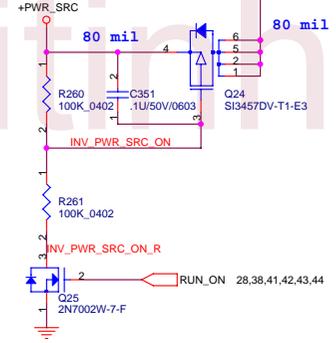


For Discrete:  
De-populate J1, R230, C311, C331, C332,  
D16, C341, C324, C326

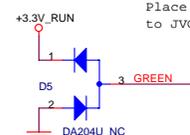
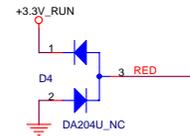
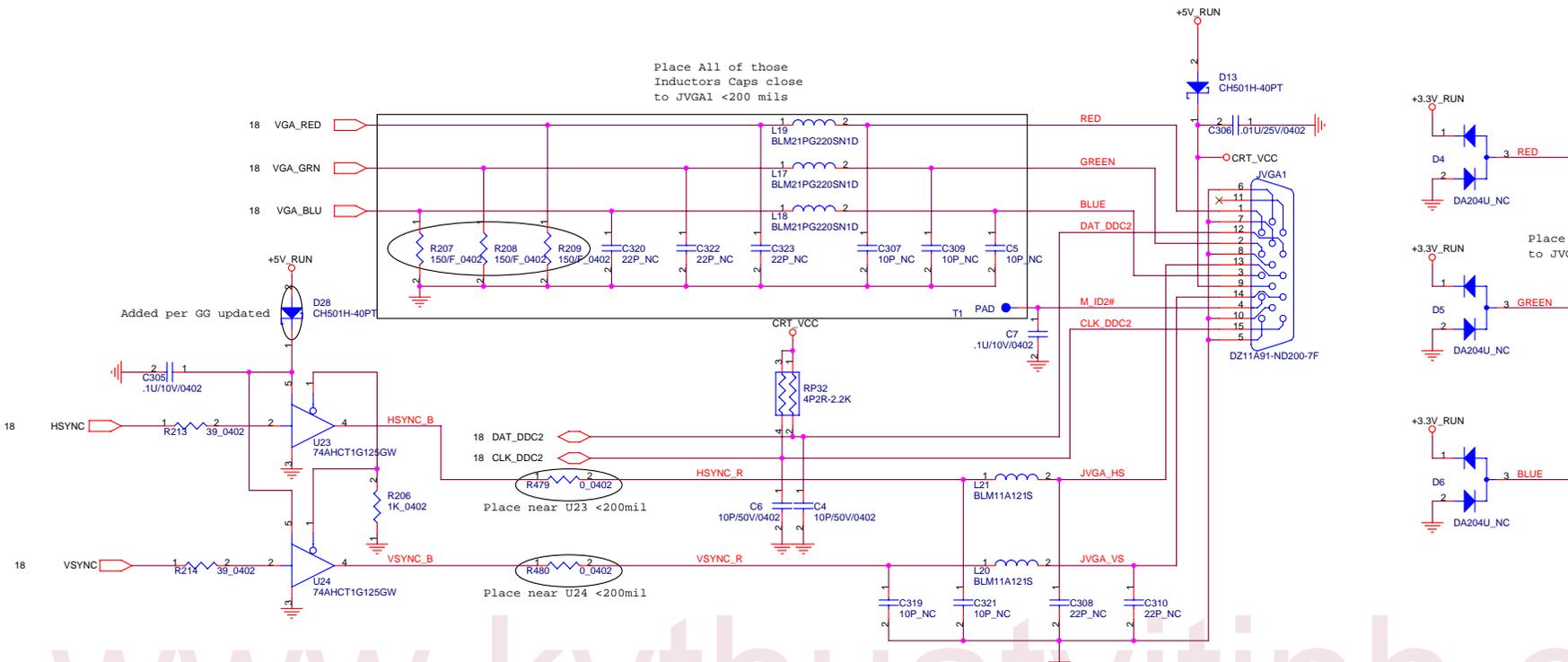


Address : A9H -Contrast  
AAH -Backlight

M'07 inverter support - De-populate D16.  
D'05 inverter support - Populate D16



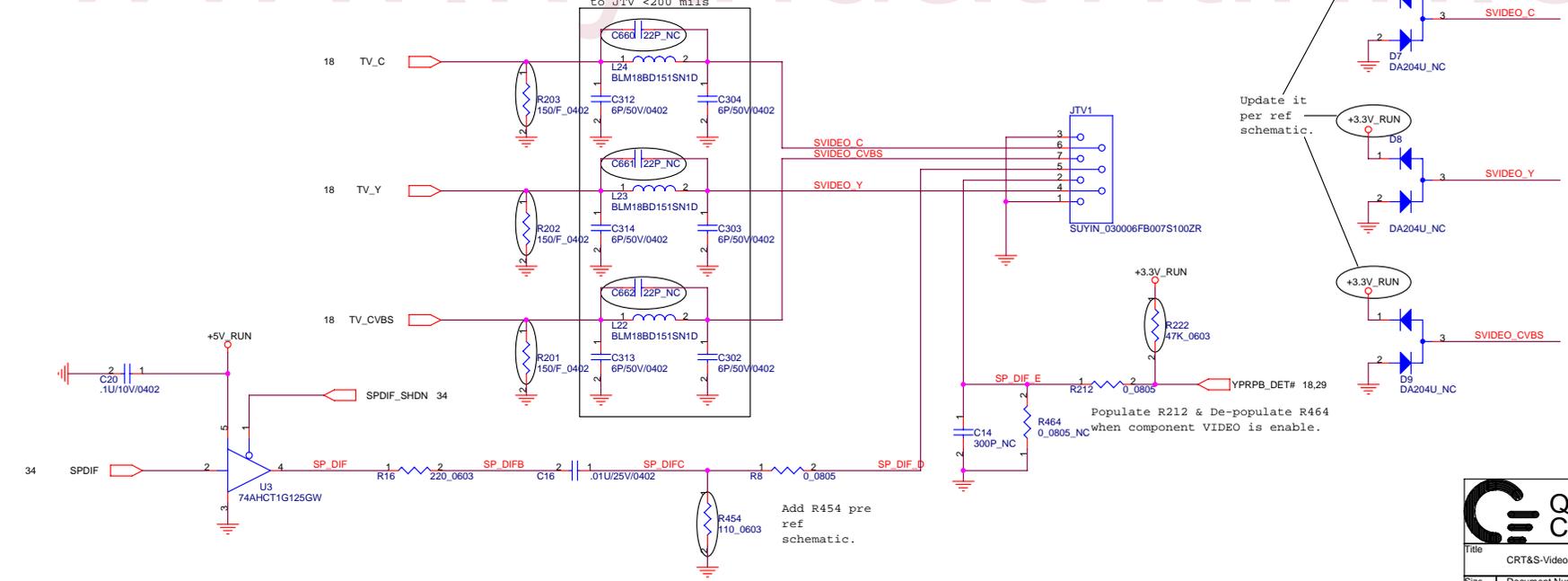
Place All of those Inductors Caps close to JVGA1 <200 mils



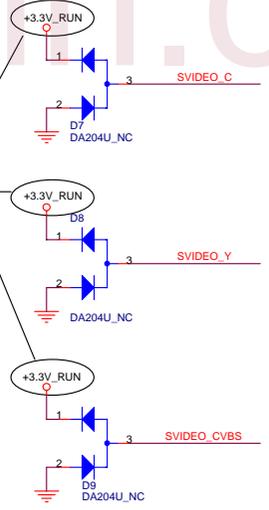
Place D4,D5,D6 close to JVGA1 <200 mils

Place L20,L21,C319,C321,C308,C310 close to JVGA1 <200 mils

Place All of those Inductors Caps close to JTV <200 mils

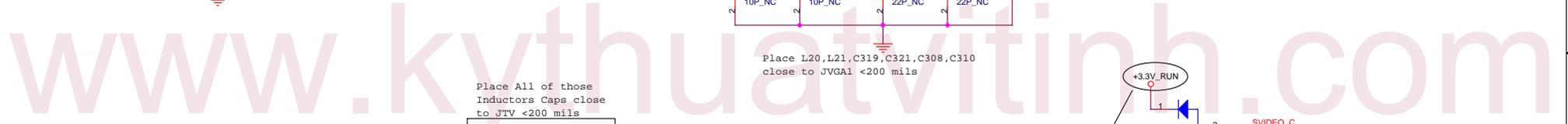


Update it per ref schematic.

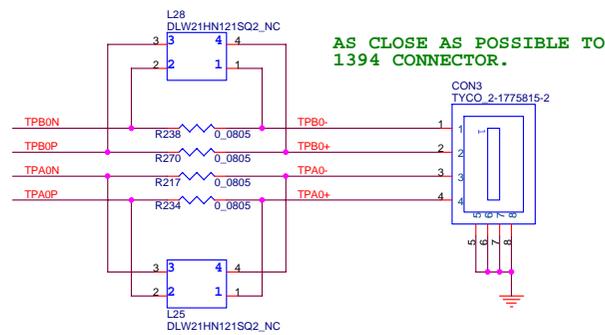
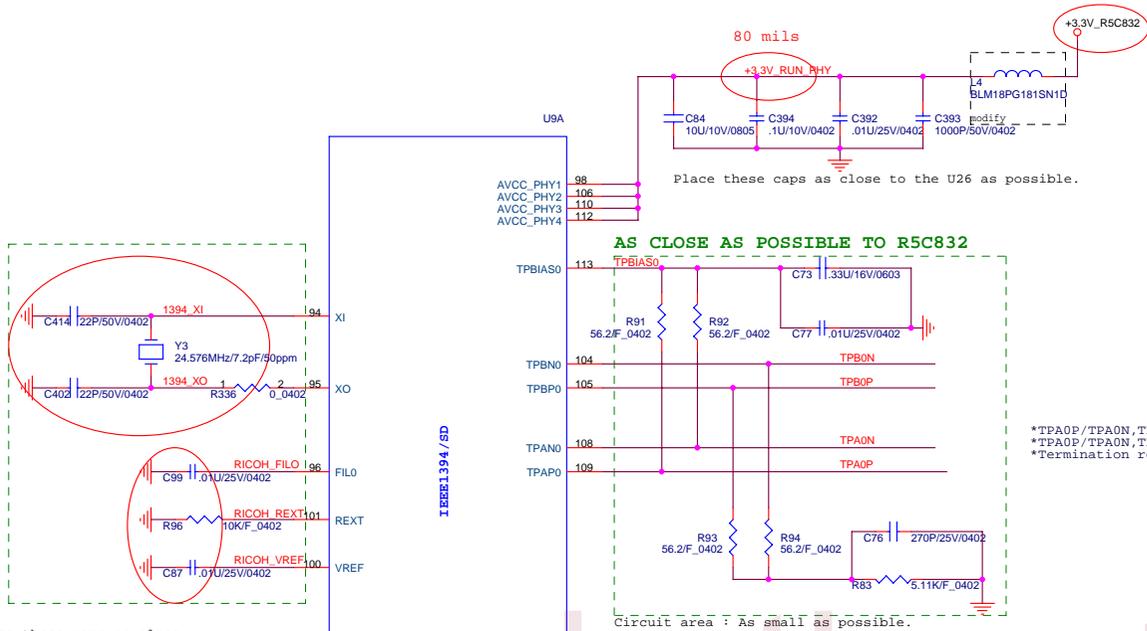


Populate R212 & De-populate R464 when component VIDEO is enable.

Add R454 pre ref schematic.



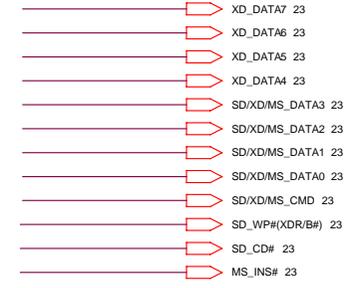
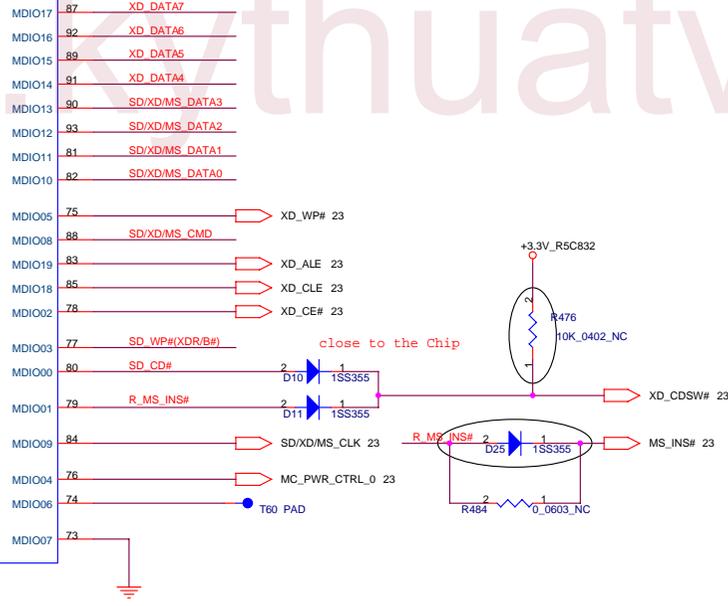




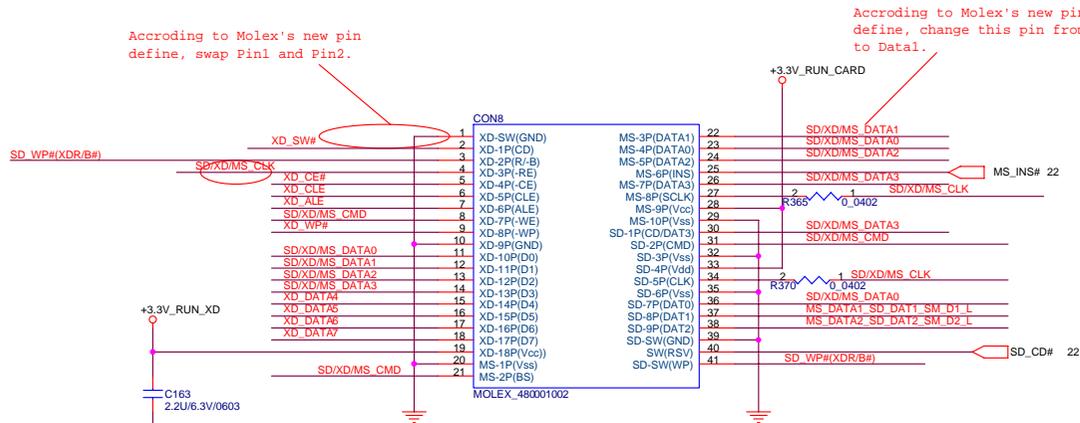
\*TPA0P/TPA0N, TPB0P/TPB0N pair trace : As close as possible.  
 \*TPA0P/TPA0N, TPB0P/TPB0N pair trace : Same length electrically.  
 \*Termination resistor for TPA+/- TPB+/- : As close as possible to its cable driver (device pin out).

Place these caps as close to the U26 as possible.

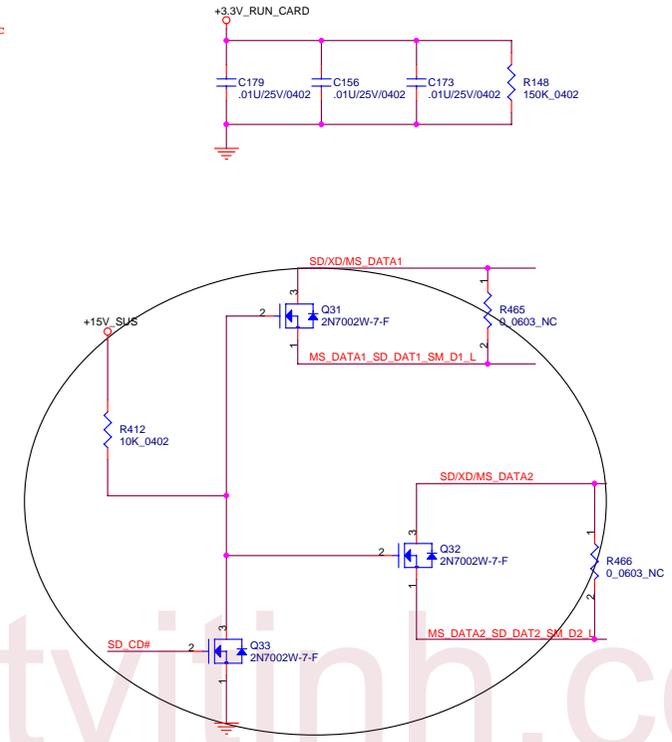
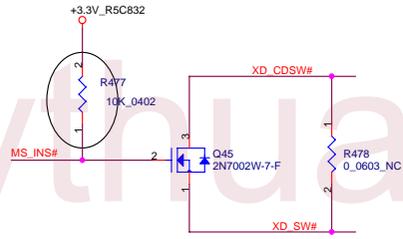
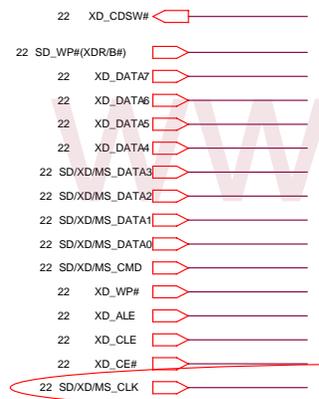
Circuit area : As small as possible.



**DO NOT INSERT SD/MMC, MEMORYSTICK AND XD SIMULTANEOUSLY.**

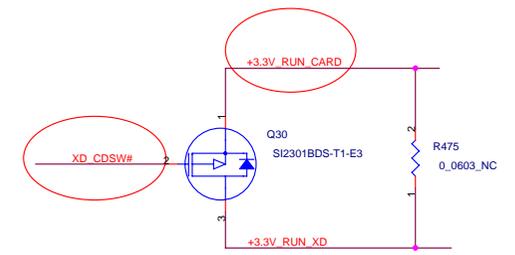
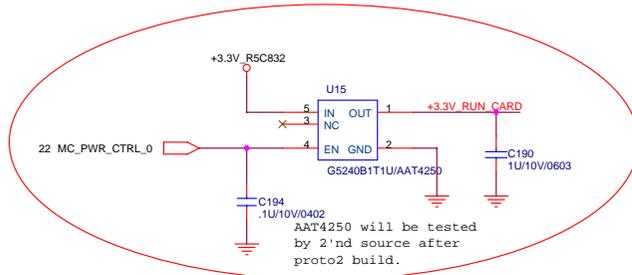


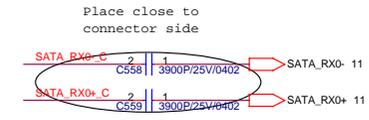
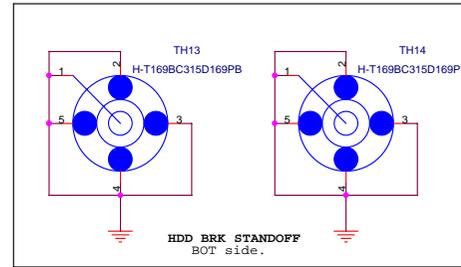
## 5 IN1 CARD READER



For SD/MS power

For XD power

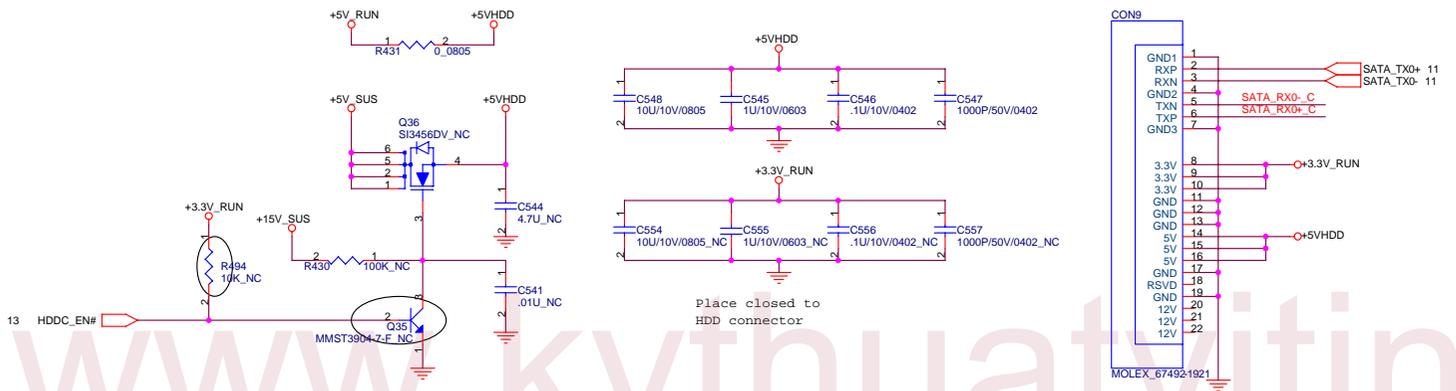




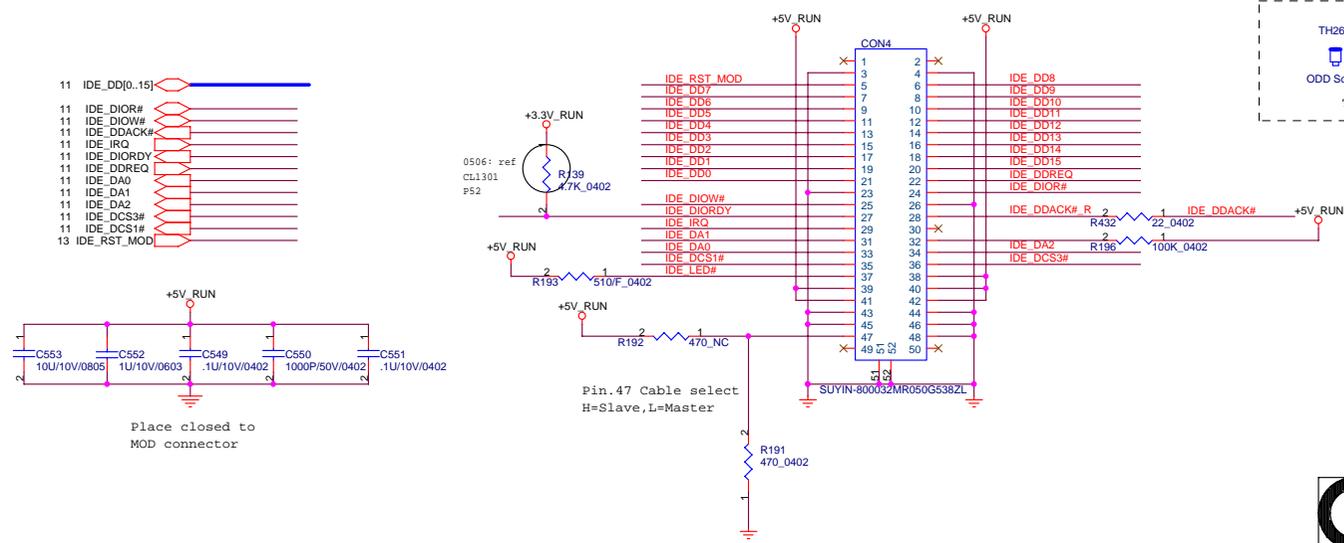
Place close to connector side  
Locate caps C558, C559 near HDD Conn.  
Length match SATA\_C\_RX0- & SATA\_C\_RX0+ within 20mils.

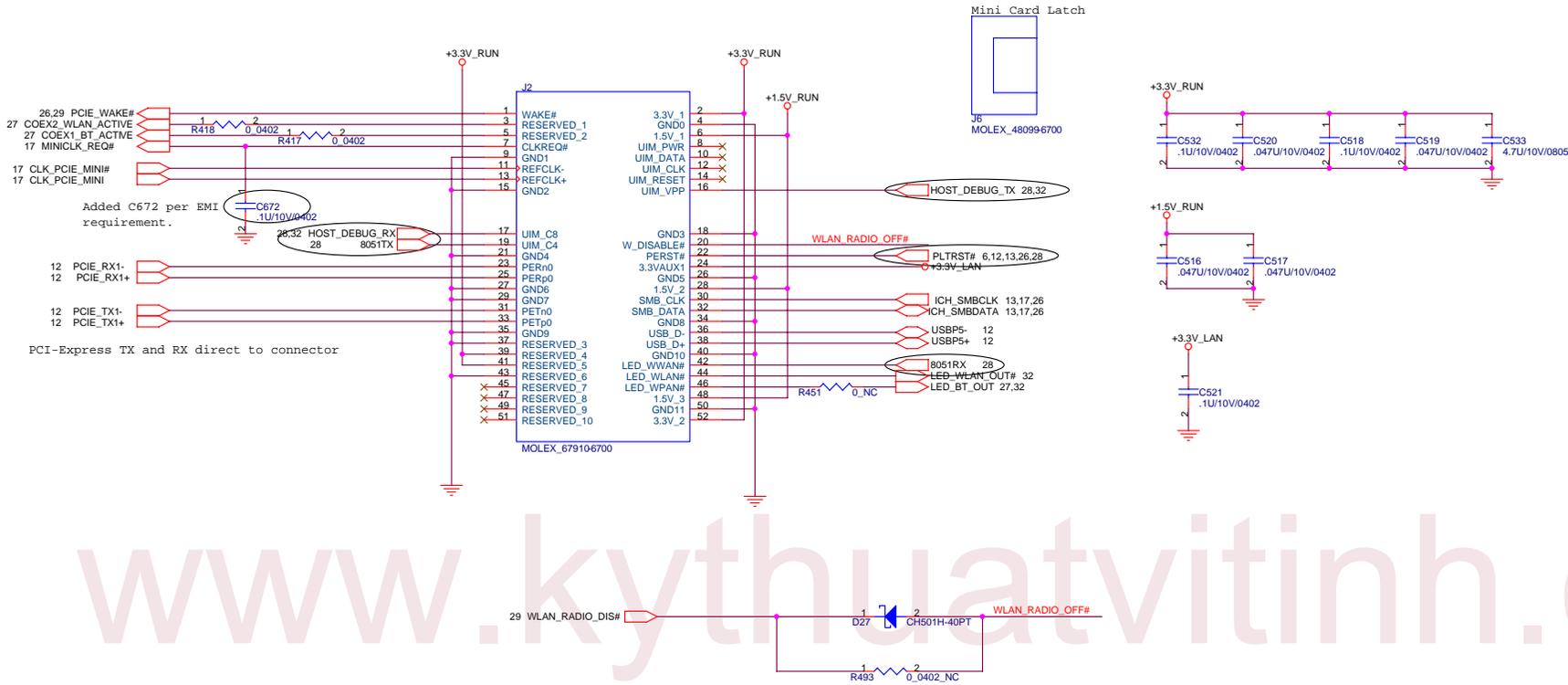
SATA drive vendors will use only 5V supply from the system and will derive 3.3V on the drive. If drive power goals are not achieved, drive vendors will use both 5V and 3.3V supplies from the system. Initial power saving using 3.3V from system is less than 5%.

Power Estimate:  
SATA drive power consumption estimate at MobileMark is 1.1W. An additional 150mW can be saved using Intel's IMST driver.

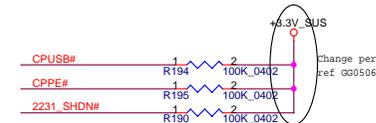
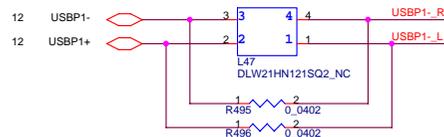
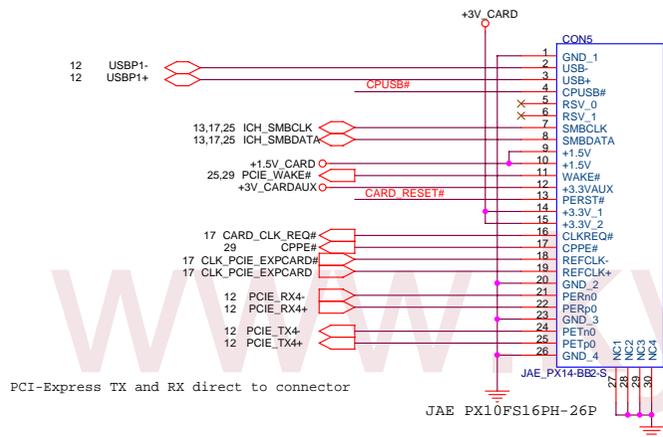
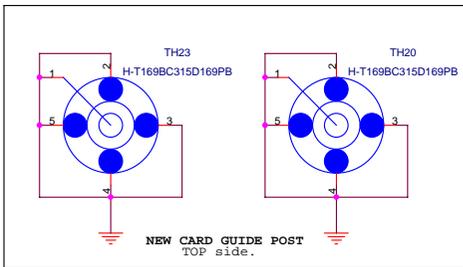


www.kythuatvithinh.com

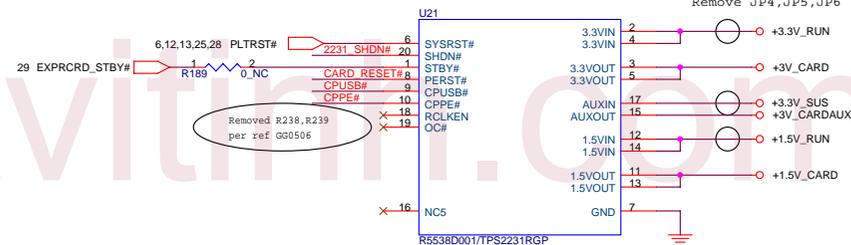




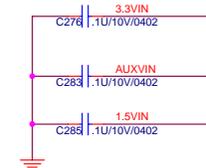
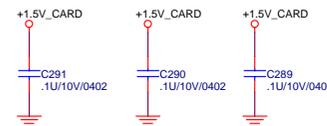
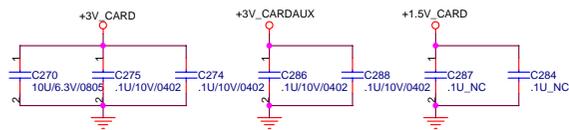
www.kythatvithinh.com



+1.5V\_CARD Max. 650mA, Average 500mA  
 +3V\_CARD Max. 1300mA, Average 1000mA

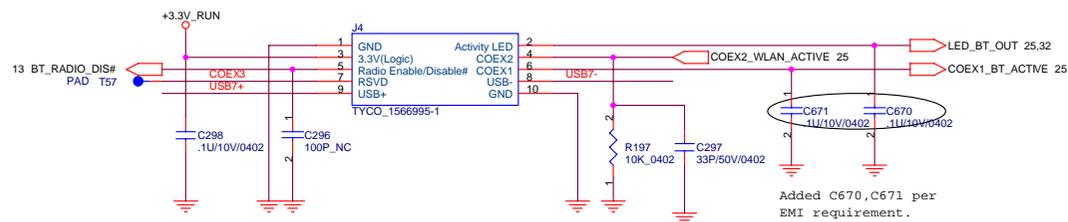
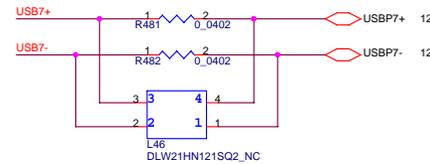
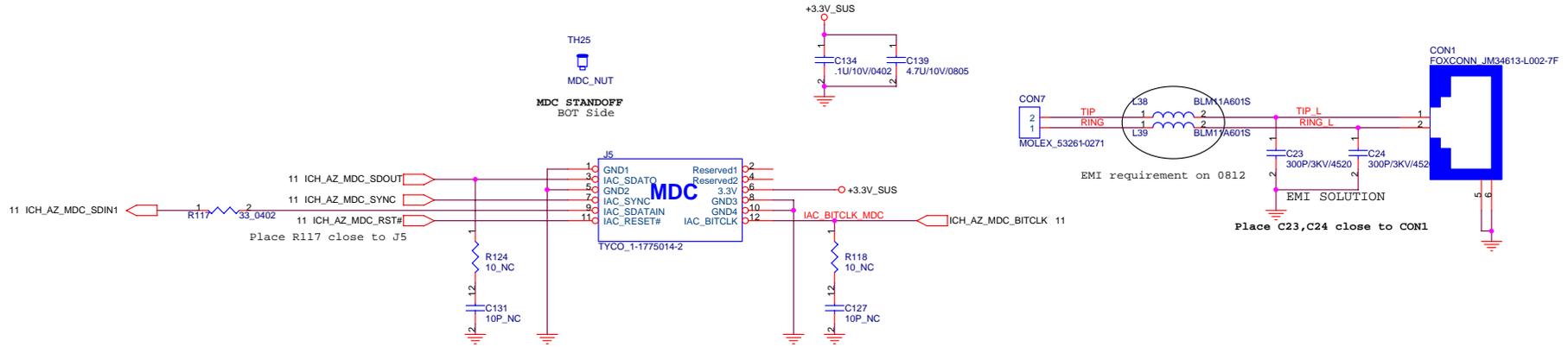


+1.5V\_CARD Max. 650mA, Average 500mA  
 +3V\_CARD Max. 1300mA, Average 1000mA

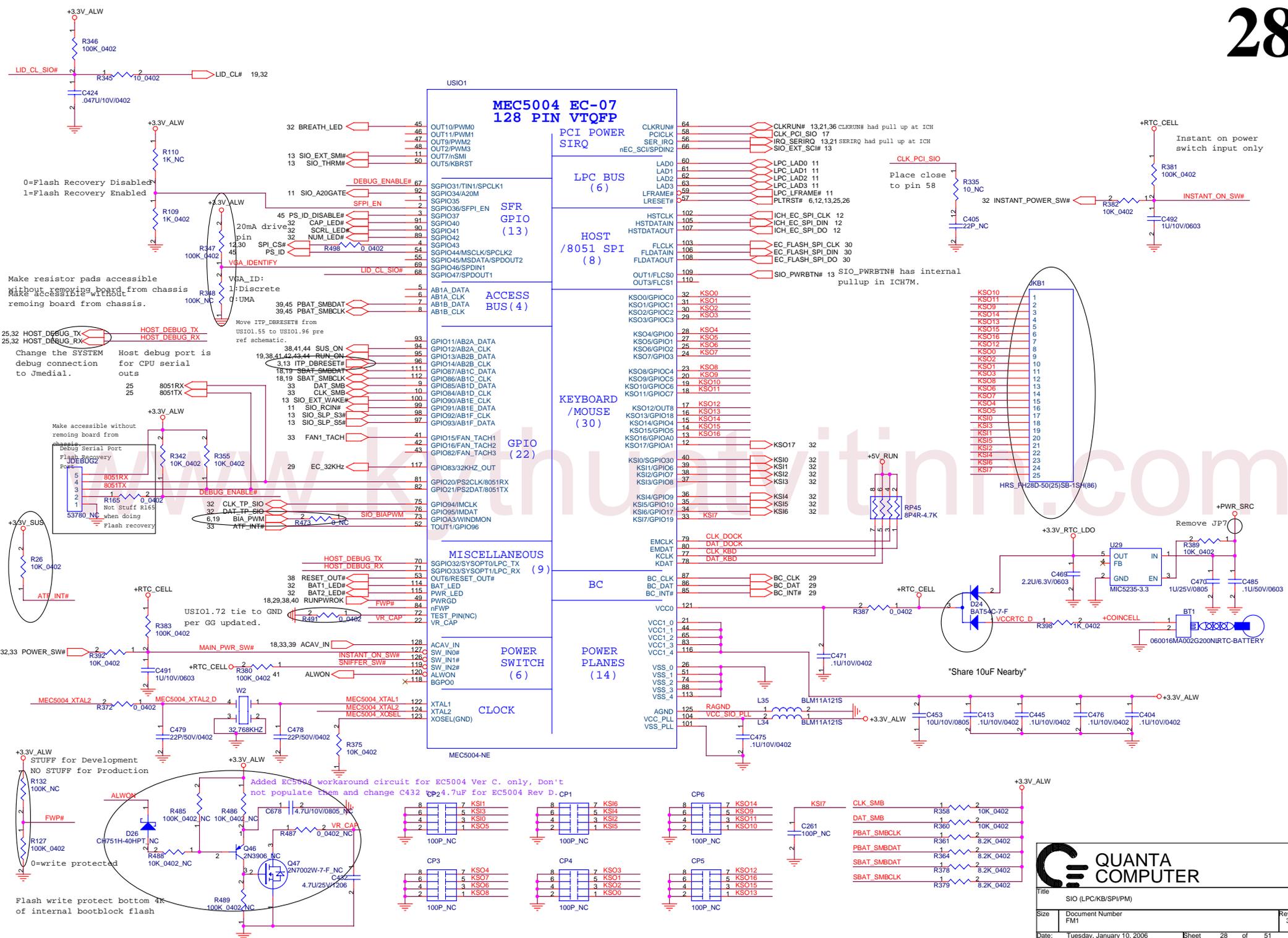


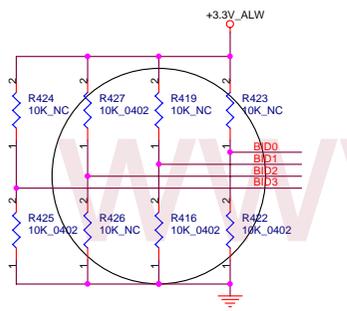
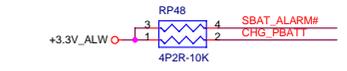
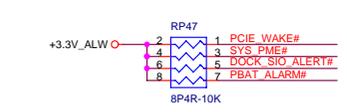
## MDC Layout Notes

1. Tip and Ring trace width = 25 mils
2. Spacing between Tip and Ring = 25 mils
3. Tip and Ring connector pitch = 25 mils
4. Keep out area from Tip and Ring to other signals = 100 mils
5. Power and Ground minimum trace width to connector = 20 mils
6. Route Tip and Ring on one layer only (top or bottom)
7. Modem internal cable wire size = 26 AWG  
(stranded or twisted pair wire)

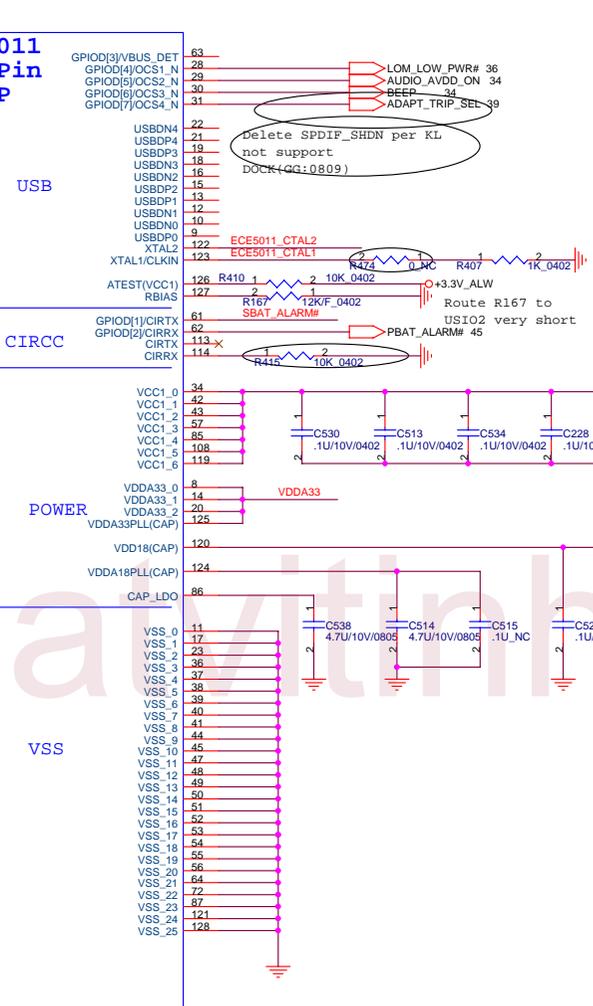
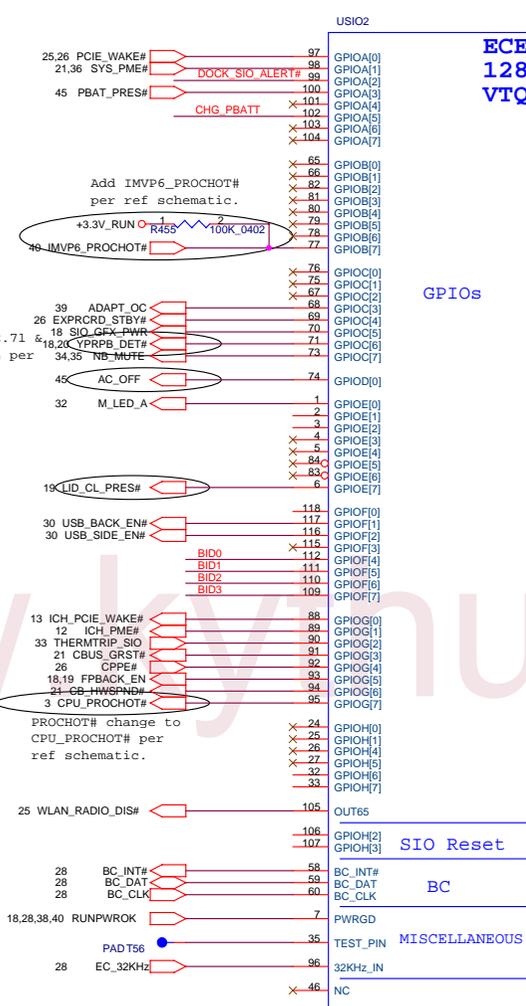


www.kythuativinh.com

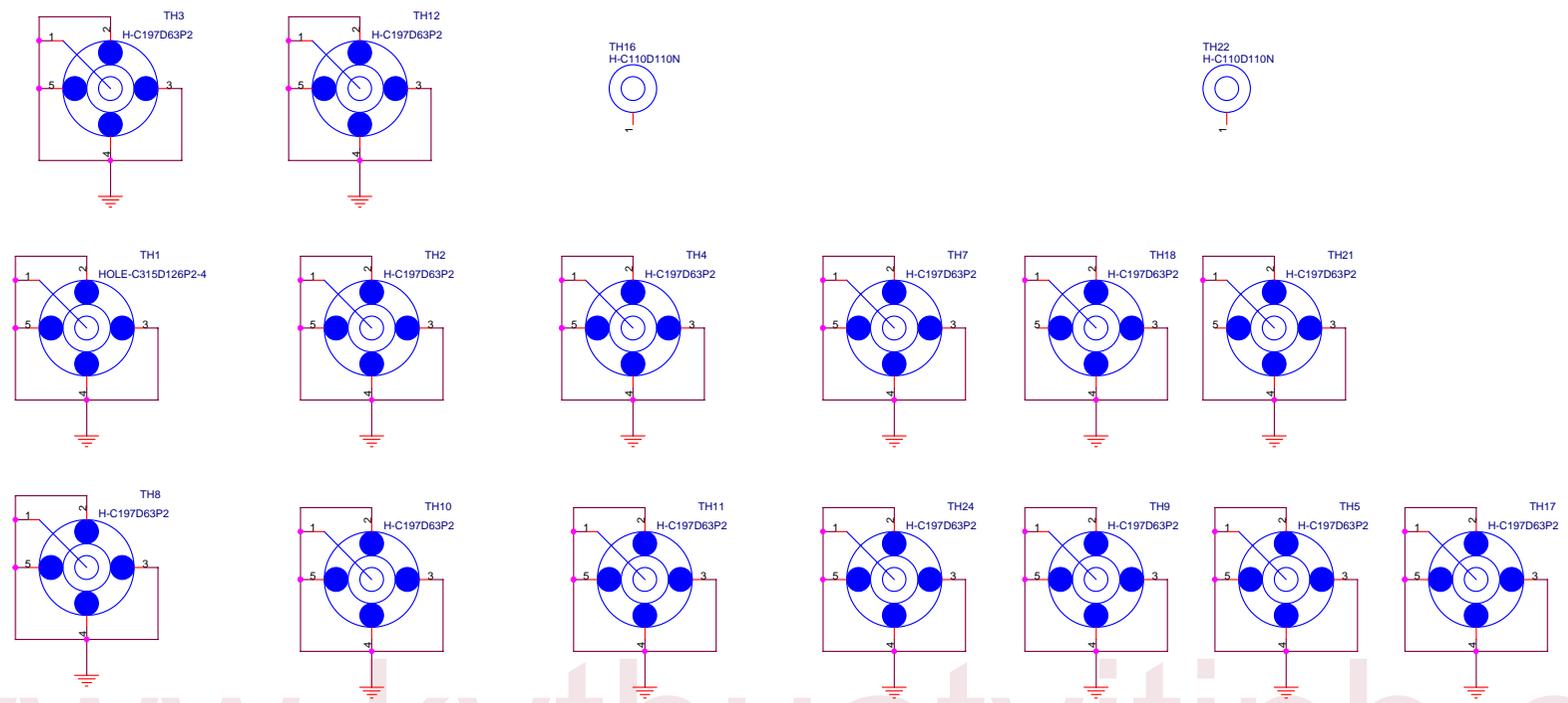




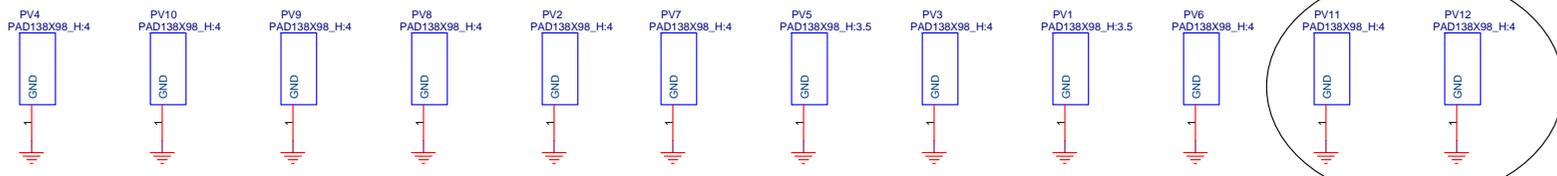
BID3	BID2	BID1	BID0	Board Revision
0	0	0	0	SST (X03)
0	0	0	1	PT (X01)
0	0	1	0	Pre-ST (X02)
0	0	1	1	ST (X02)
0	1	0	0	QT (A05)



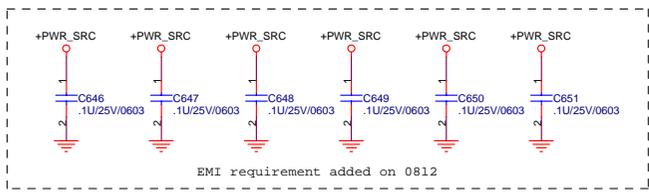
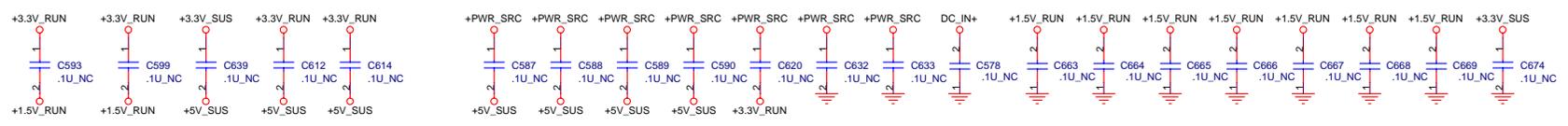




www.kythuativinh.com

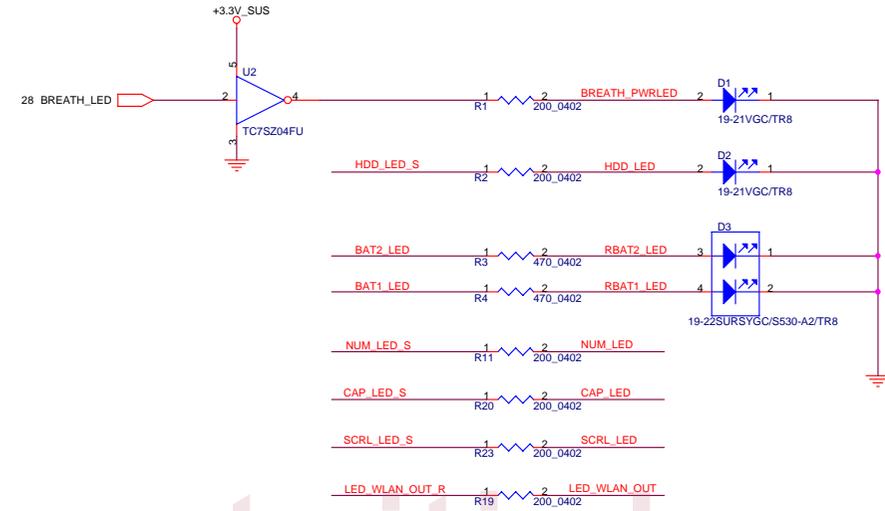
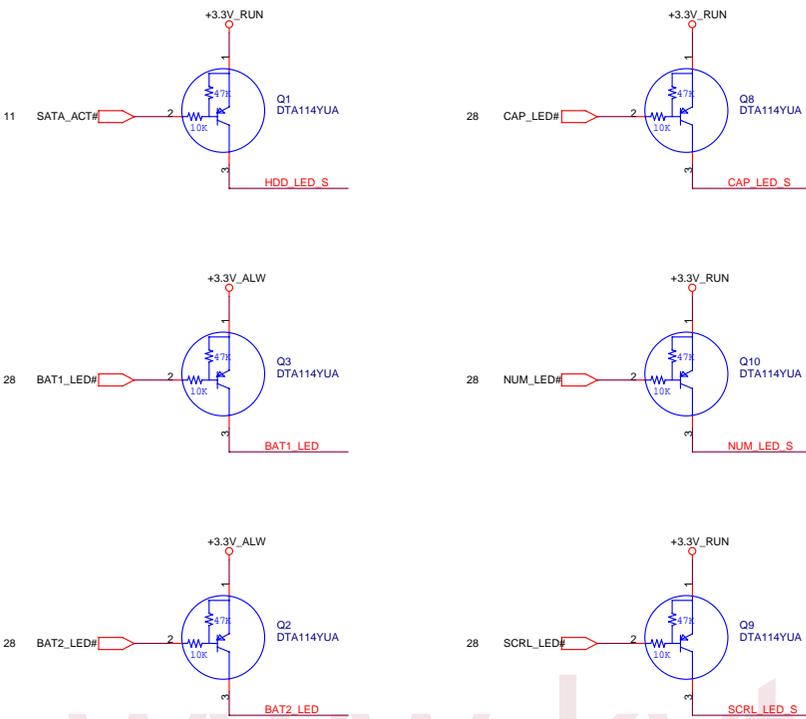


EMI requirement added on 0812

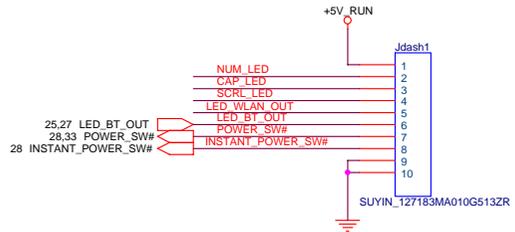
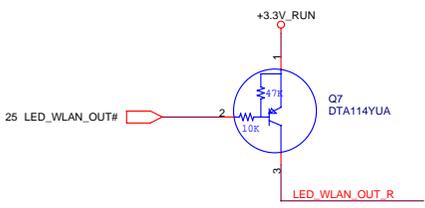
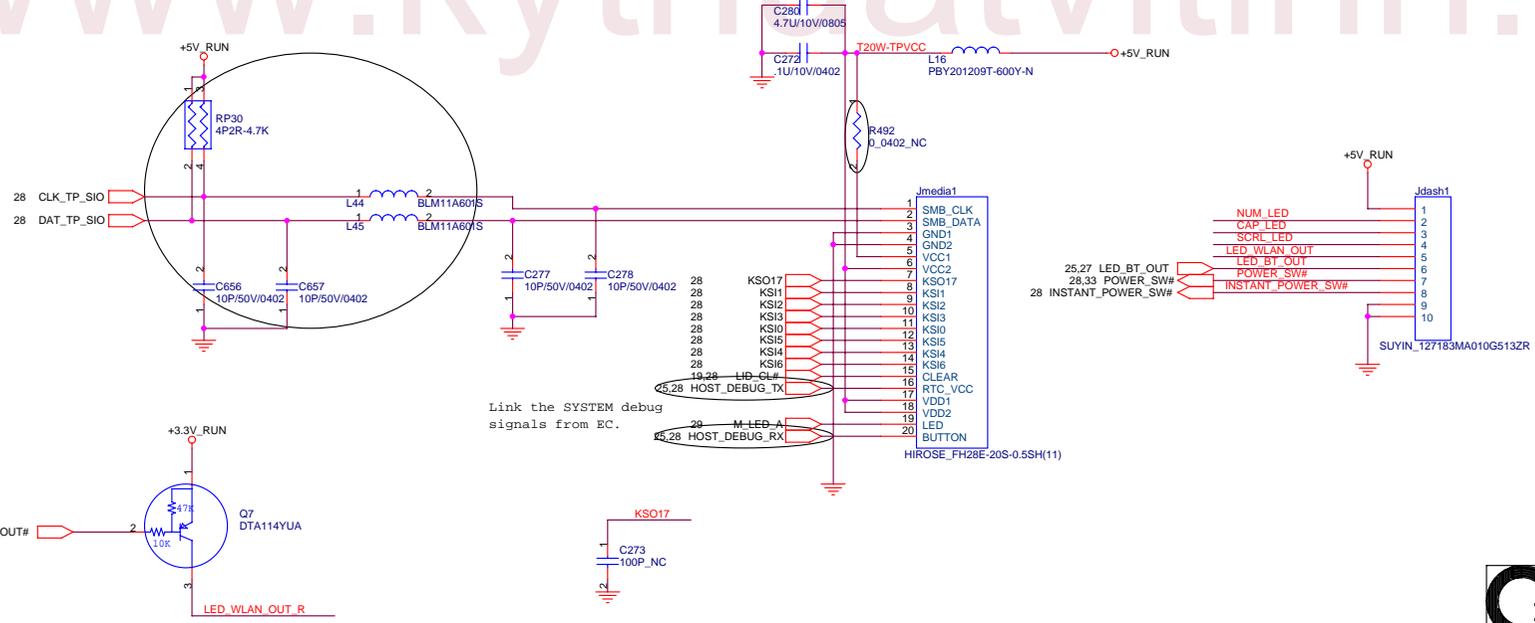


**QUANTA COMPUTER**

Title EMI & Screw hole		
Size	Document Number FM1	Rev 3A
Date: Tuesday, January 10, 2006	Sheet 31	of 51



www.kythuatvith.com



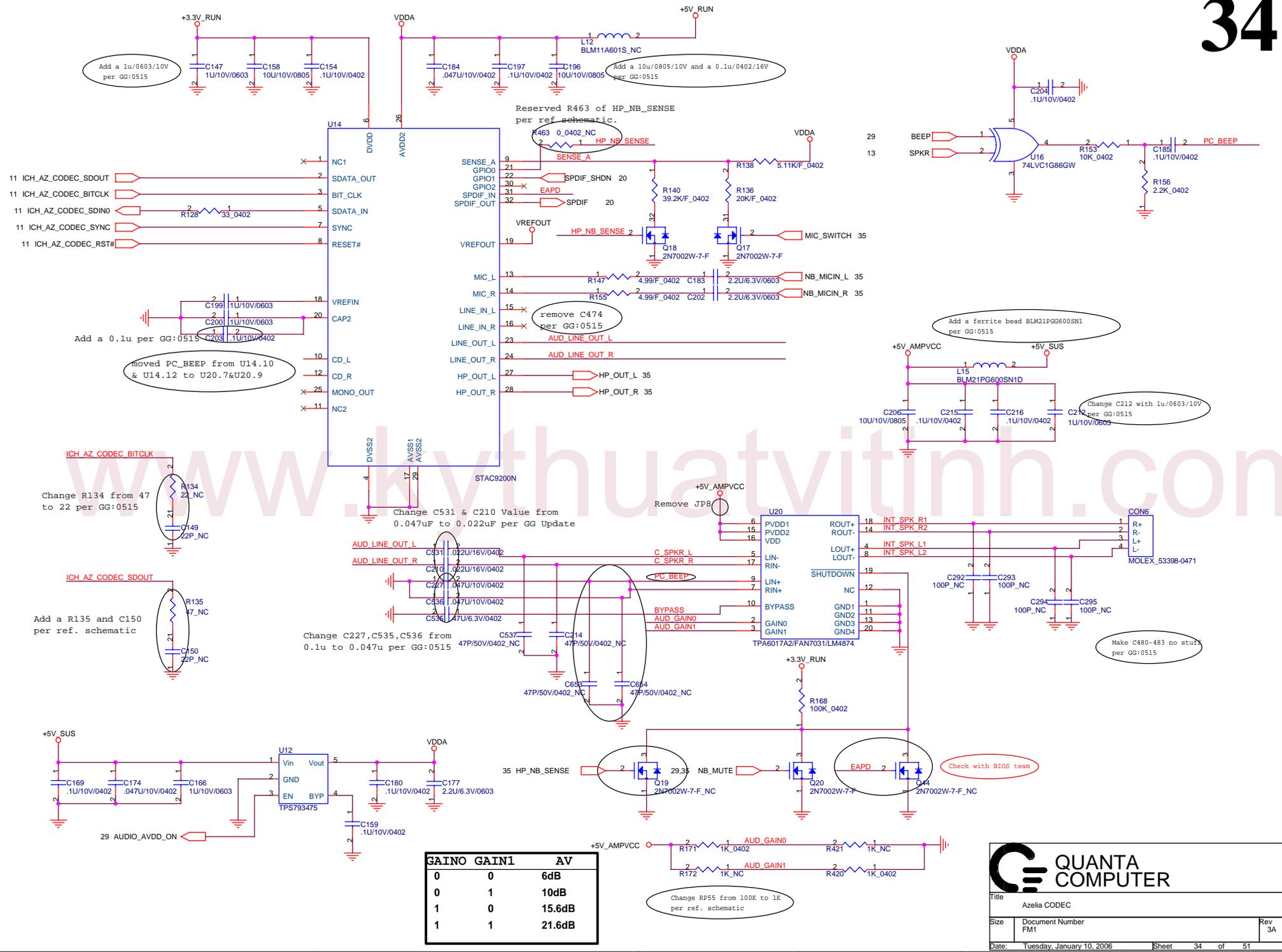
**QUANTA COMPUTER**

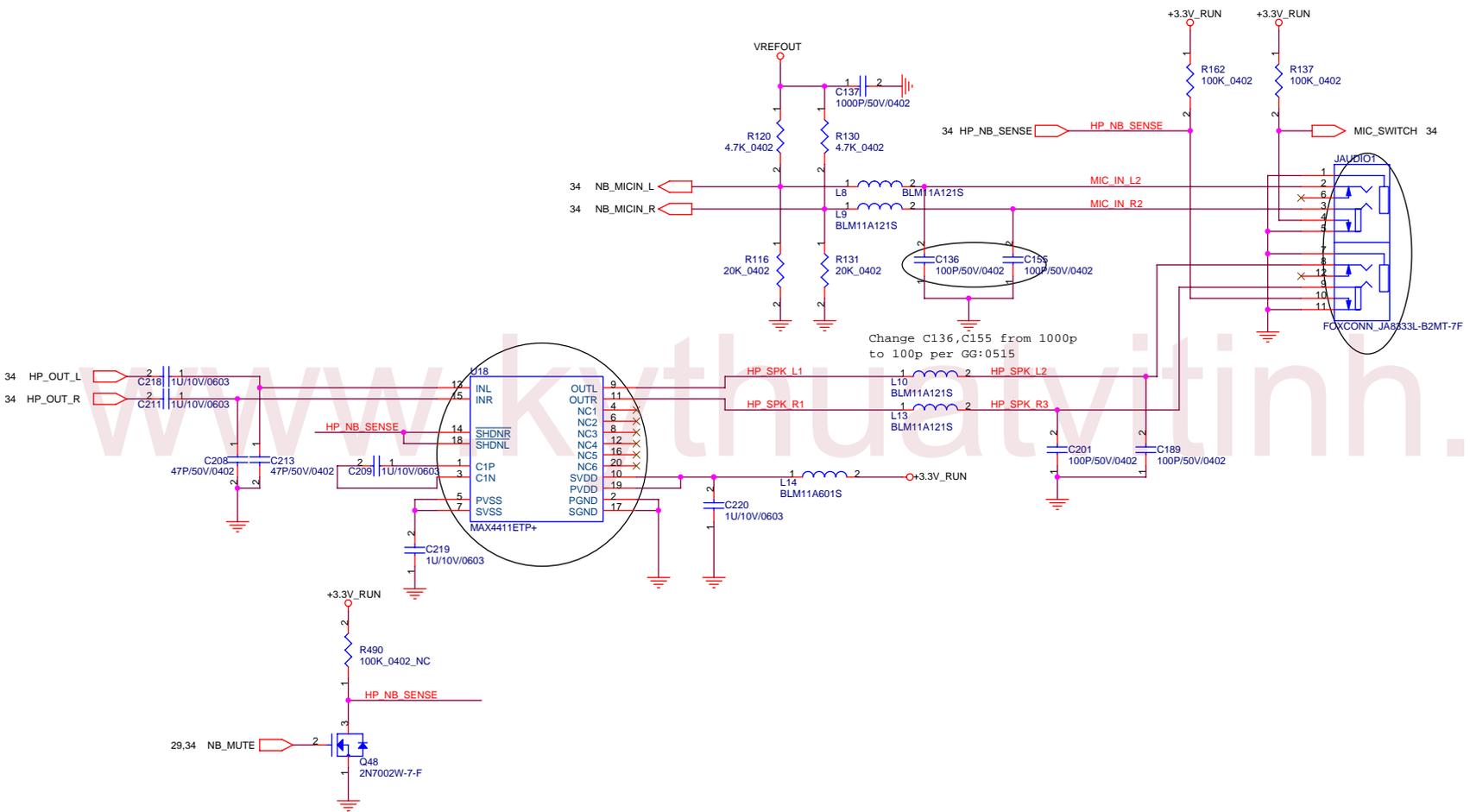
Title: SWITCH & LED

Size	Document Number	Rev
	FM1	3A

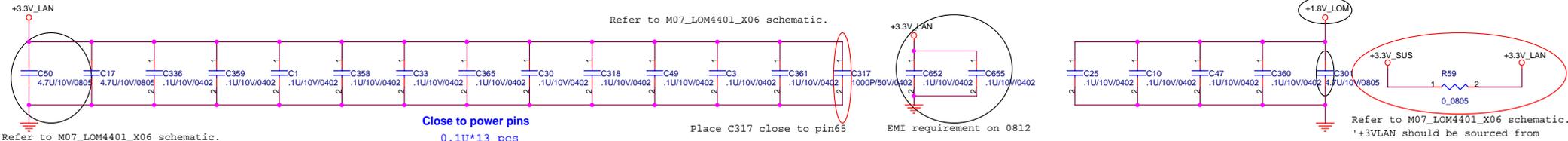
Date: Tuesday, January 10, 2006 Sheet 32 of 51



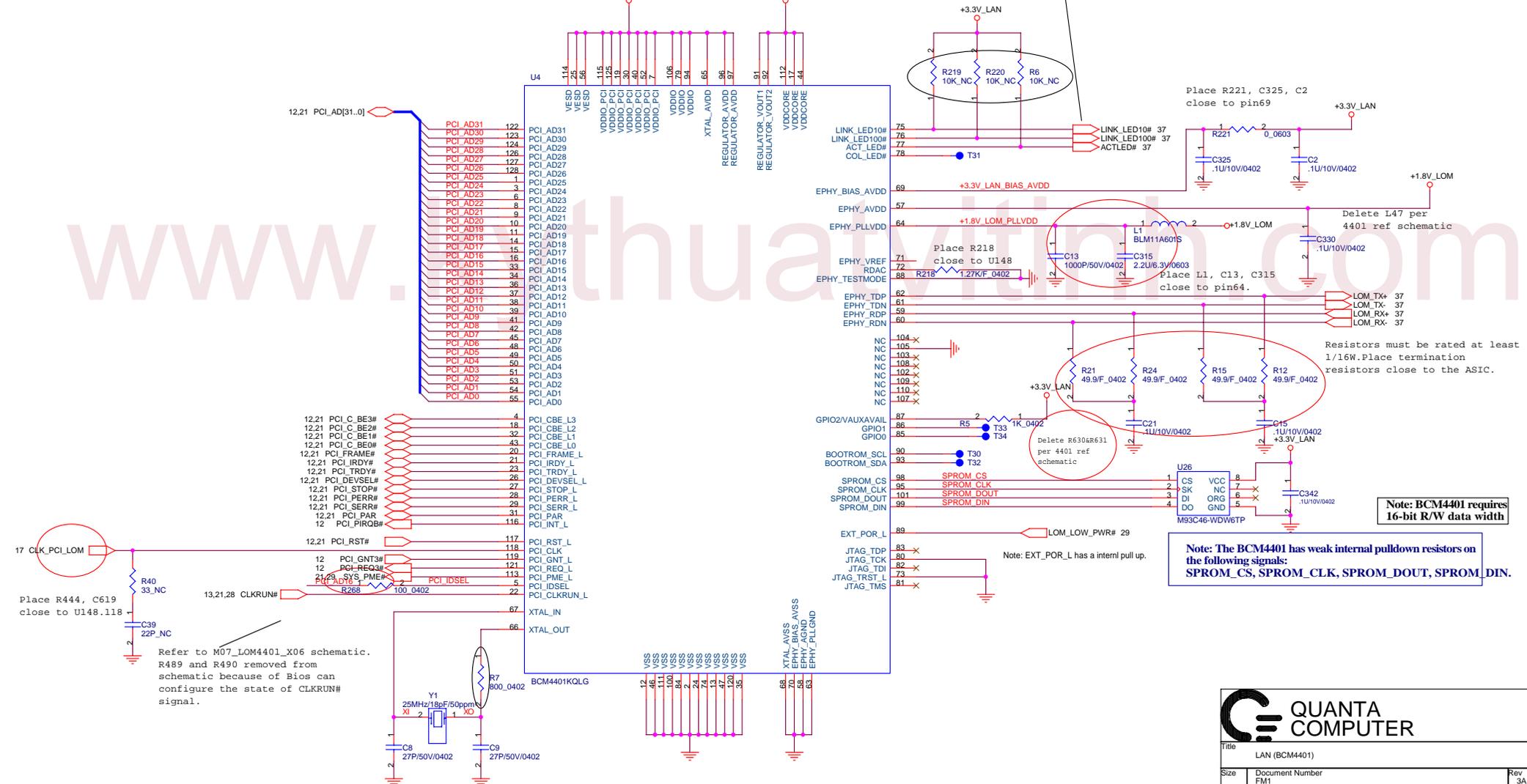




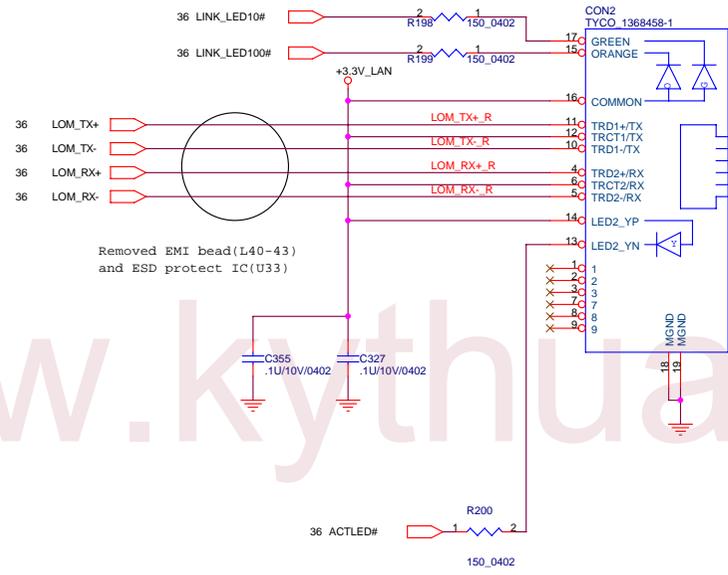
Title			AUDIO CONN		
Size	Document Number			Rev	
	FM1			3A	
Date:	Tuesday, January 10, 2006	Sheet	35	of	51



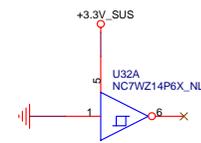
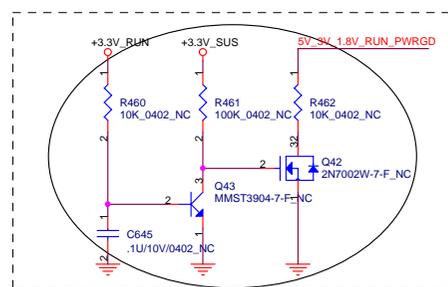
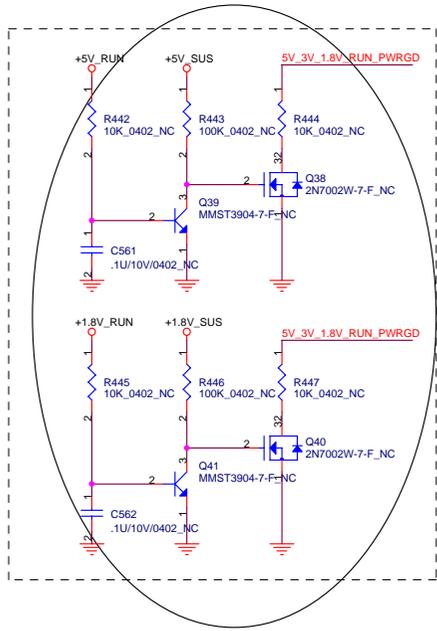
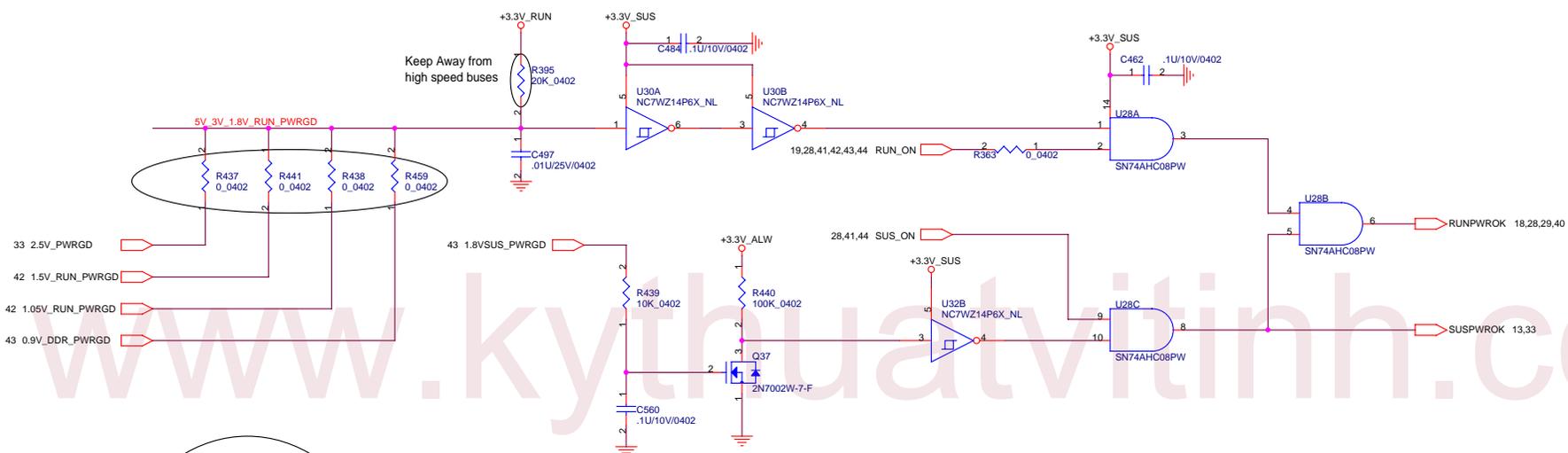
These three pin  
LINK\_LED10#,  
LINK\_LED100#,  
ACT\_LED are  
open-drain type.



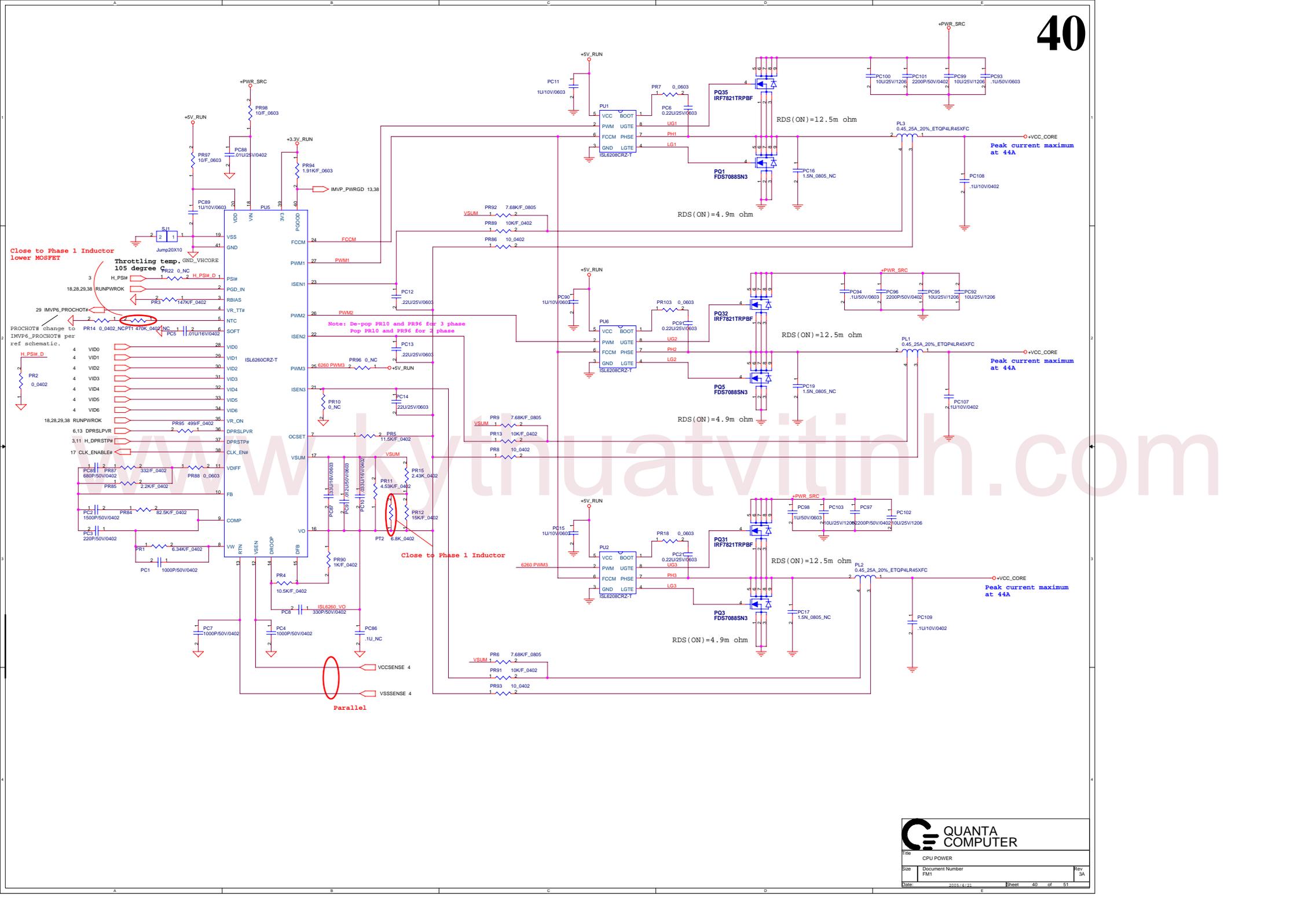
www.thuath.com



www.kyathuatvithinh.com







Close to Phase 1 Inductor lower MOSFET

PROCHOT# change to IMVP6\_PROCHOT# per ref schematic.

H\_PSM\_D

PR2 0.0402

18.28.29.38 RUNPWROK

6.13 DPRSLPVR

3.11 H\_DPRSTPM

17 CLK\_ENABLE#

PC1 1000P/50V/0402

PC7 1000P/50V/0402

PC8 1000P/50V/0402

PC4 1000P/50V/0402

PC6 1000P/50V/0402

PC86 .1u\_NC

PC4 1000P/50V/0402

PC8 1000P/50V/0402

PC86 .1u\_NC

PC4 1000P/50V/0402

PC8 1000P/50V/0402

PC86 .1u\_NC

PC4 1000P/50V/0402

PC8 1000P/50V/0402

PC86 .1u\_NC

Throttling temp. 105 degree

PR22 0\_NC

PR14 0.0402\_NCP147K\_0402

PR15 159K\_0402

PR16 159K\_0402

PR17 159K\_0402

PR18 159K\_0402

PR19 159K\_0402

PR20 159K\_0402

PR21 159K\_0402

PR22 0\_NC

PR23 0\_NC

PR24 0\_NC

PR25 0\_NC

PR26 0\_NC

PR27 0\_NC

PR28 0\_NC

PR29 0\_NC

PR30 0\_NC

PR31 0\_NC

PR32 0\_NC

PR33 0\_NC

PR34 0\_NC

PR35 0\_NC

PR36 0\_NC

Note: de-pop PR10 and PR96 for 3 phase Pop PR10 and PR96 for 2 phase

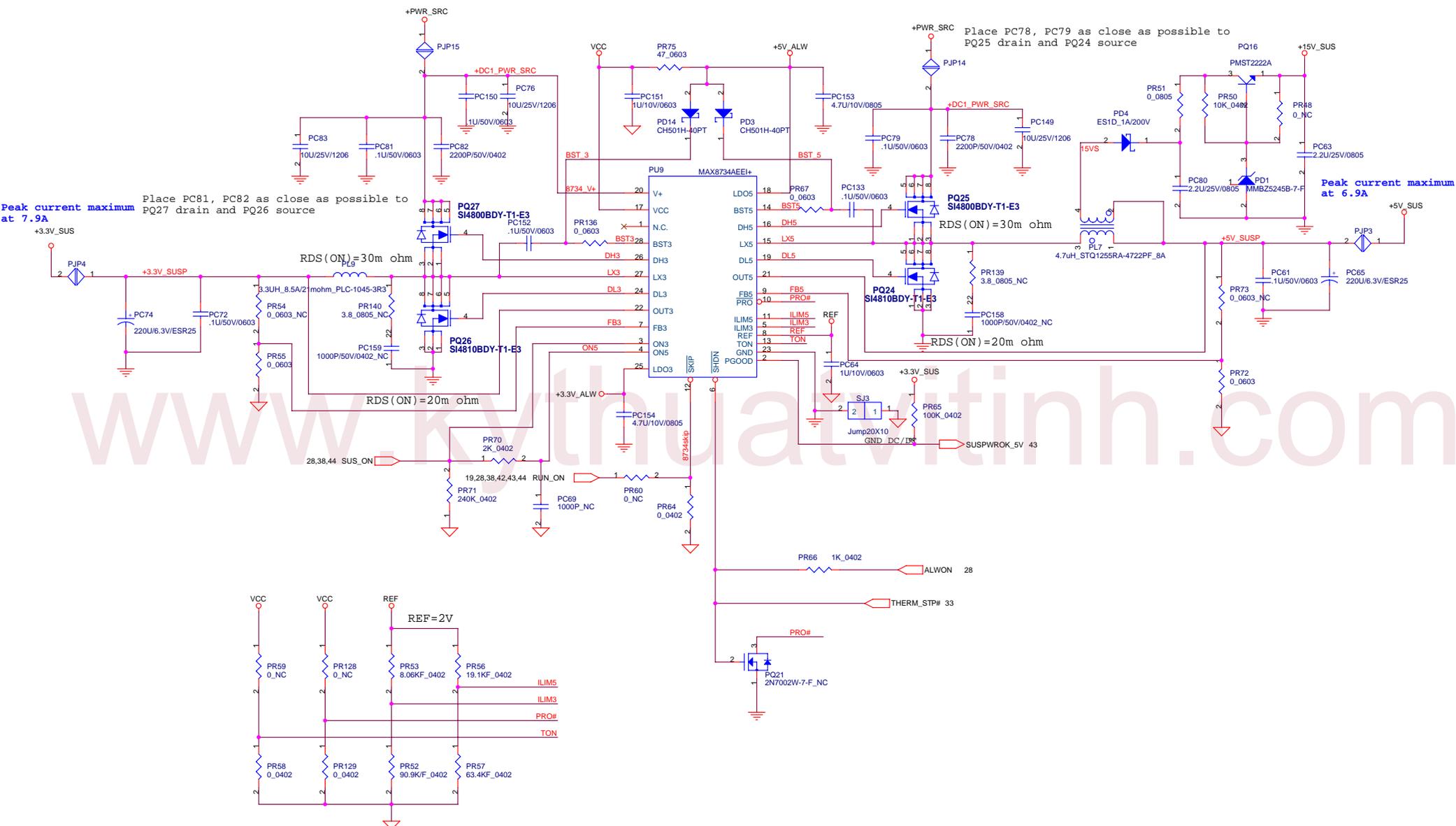
Close to Phase 1 Inductor

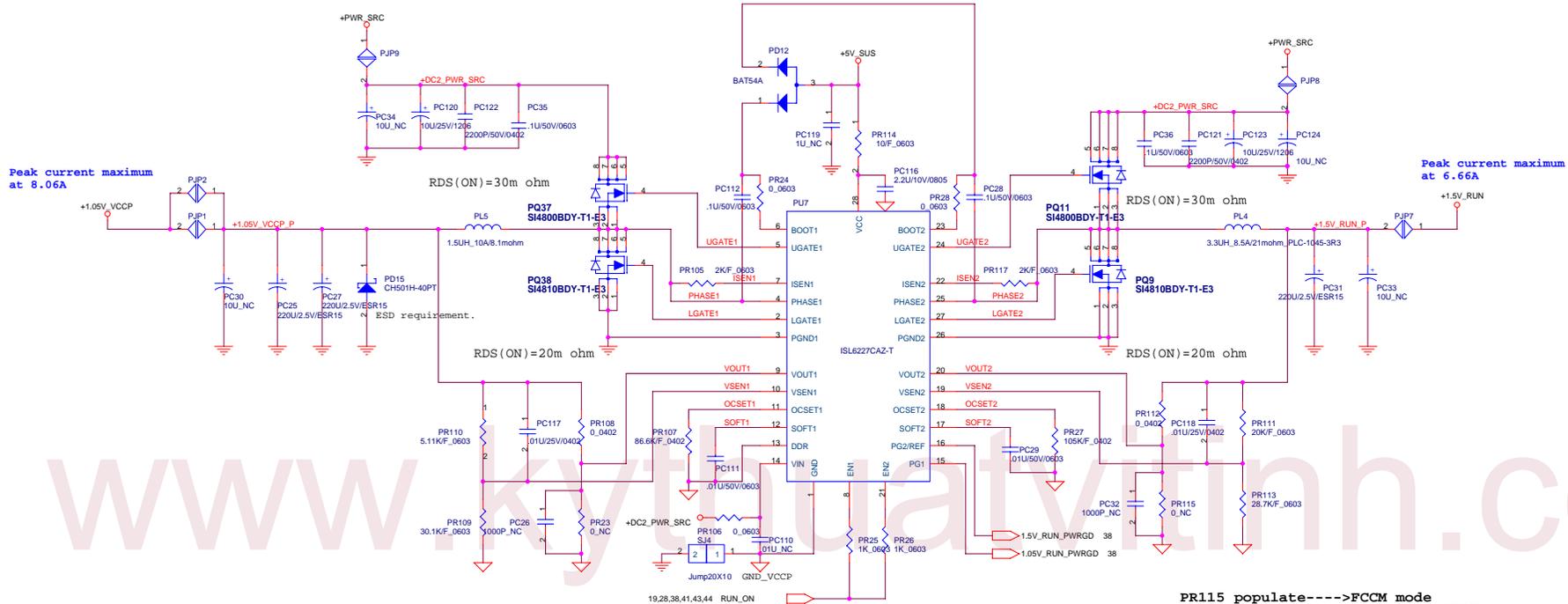
Parallel

Peak current maximum at 44A

Peak current maximum at 44A

Peak current maximum at 44A





Peak current maximum at 8.06A

Peak current maximum at 6.66A

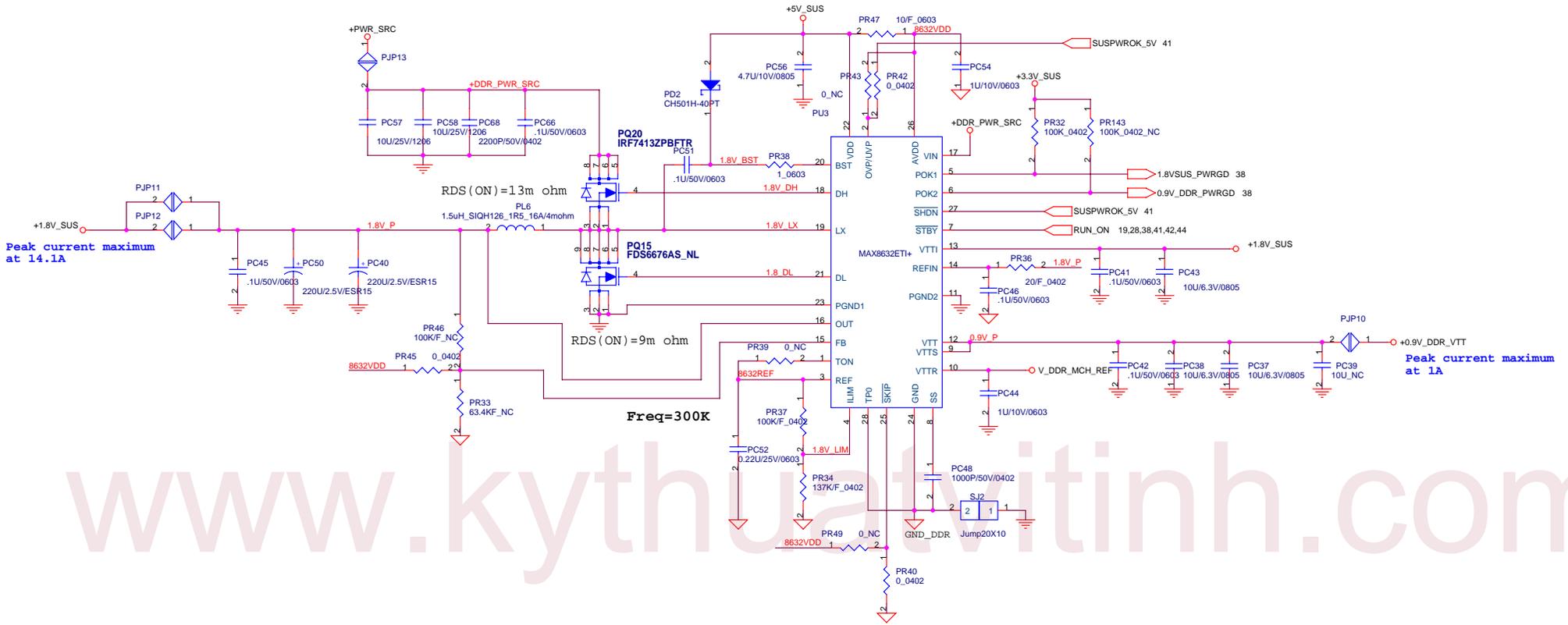
PR23 populate---->FCCM mode  
 PR108 populate---->Hysteretic/FCCM mode.

PR115 populate---->FCCM mode  
 PR112 populate---->Hysteretic/FCCM mode.

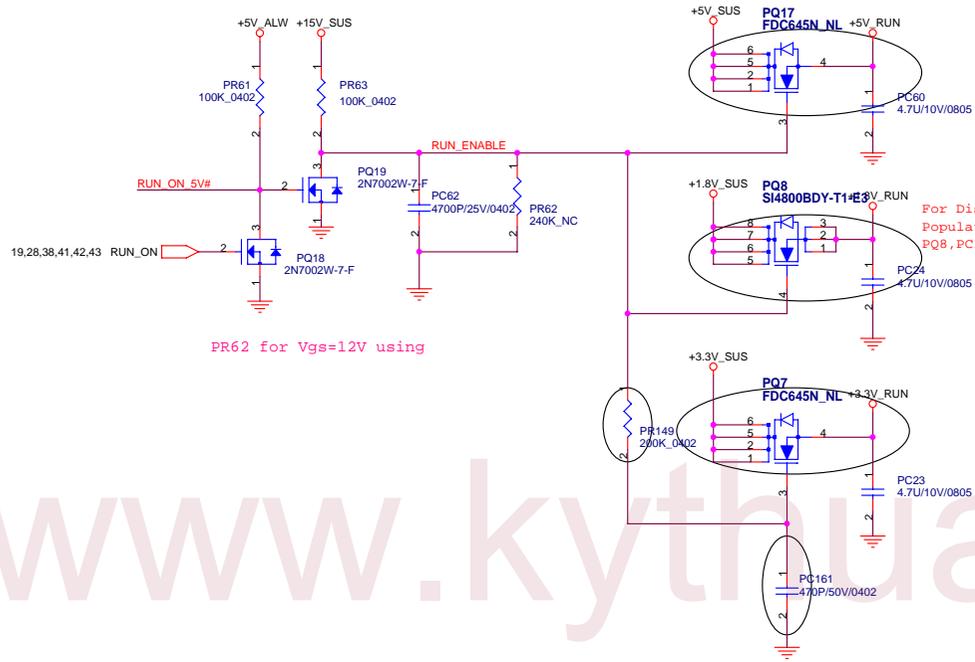
www.kyubatek.vn



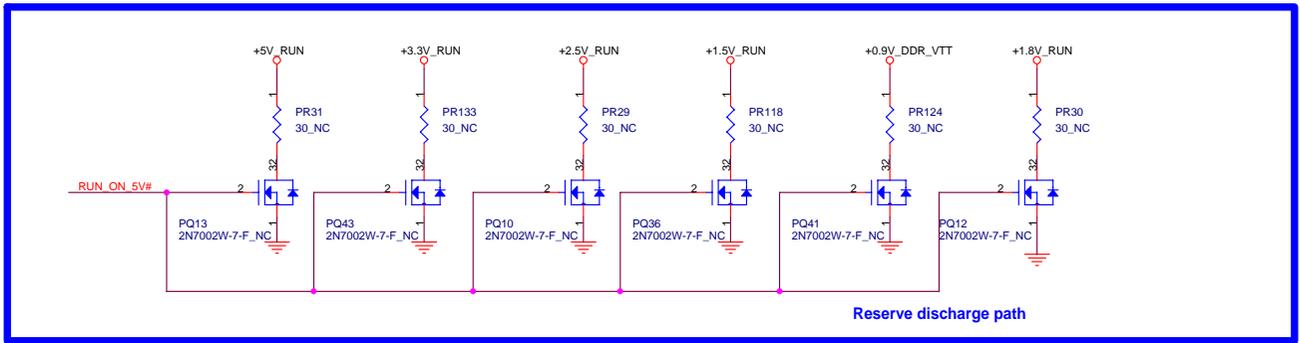
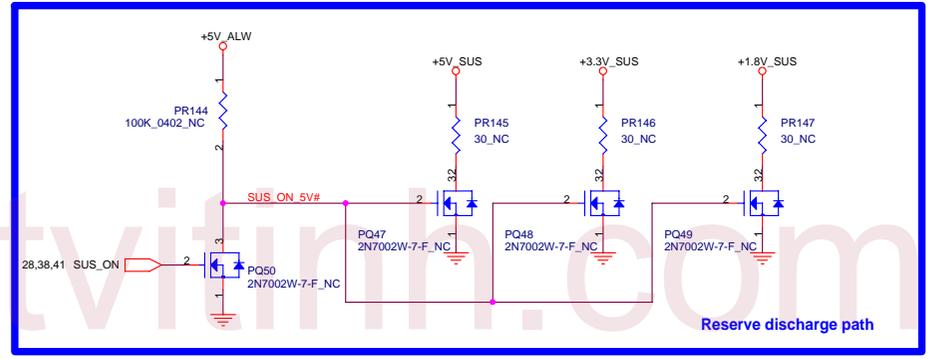
File			VCCP
Size	Document Number	Rev	
	FM1	3A	
Date	2005/4/21	Sheet	42 of 51



www.kythuraitinh.com

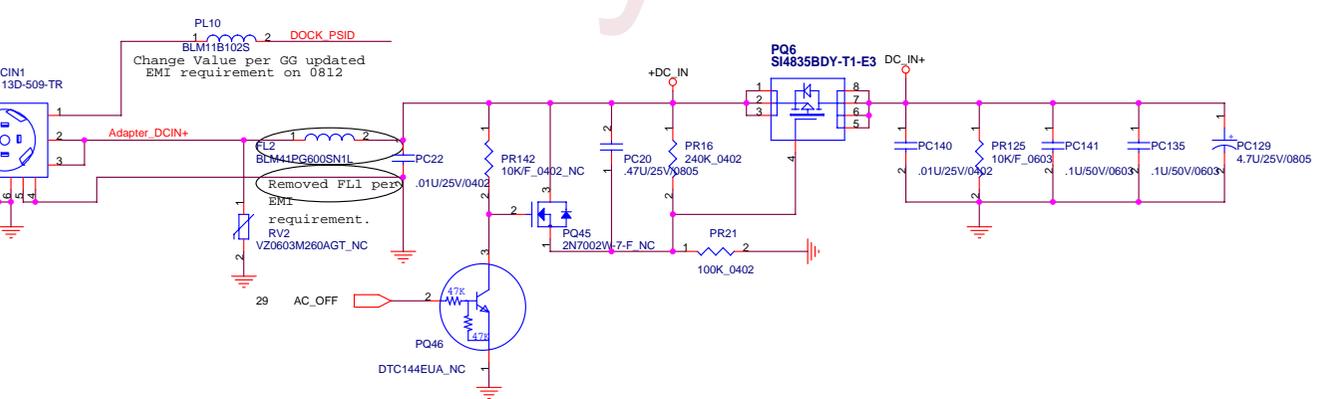
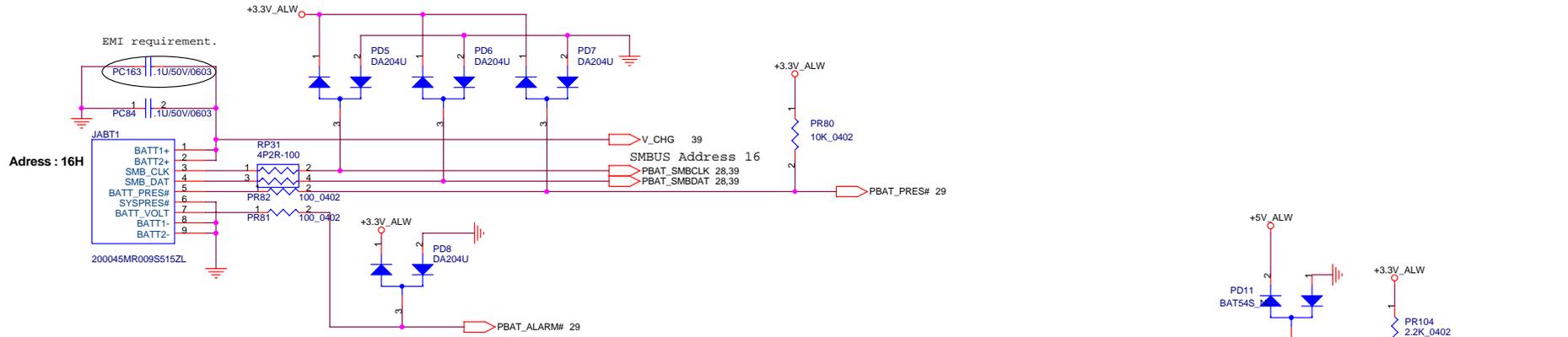


For Discrete:  
Populate  
PQ8, PC24



**QUANTA  
COMPUTER**

Title	RUN POWER SW	
Size	Document Number FM1	Rev 3A
Date:	2005/4/21	Sheet 44 of 51



www.kythuatvietnh.com

**QUANTA COMPUTER**

Title: DCIN,BATT CONNECTOR

Size: Document Number FM1 Rev 3A

Date: 2005/4/21 Sheet 45 of 51