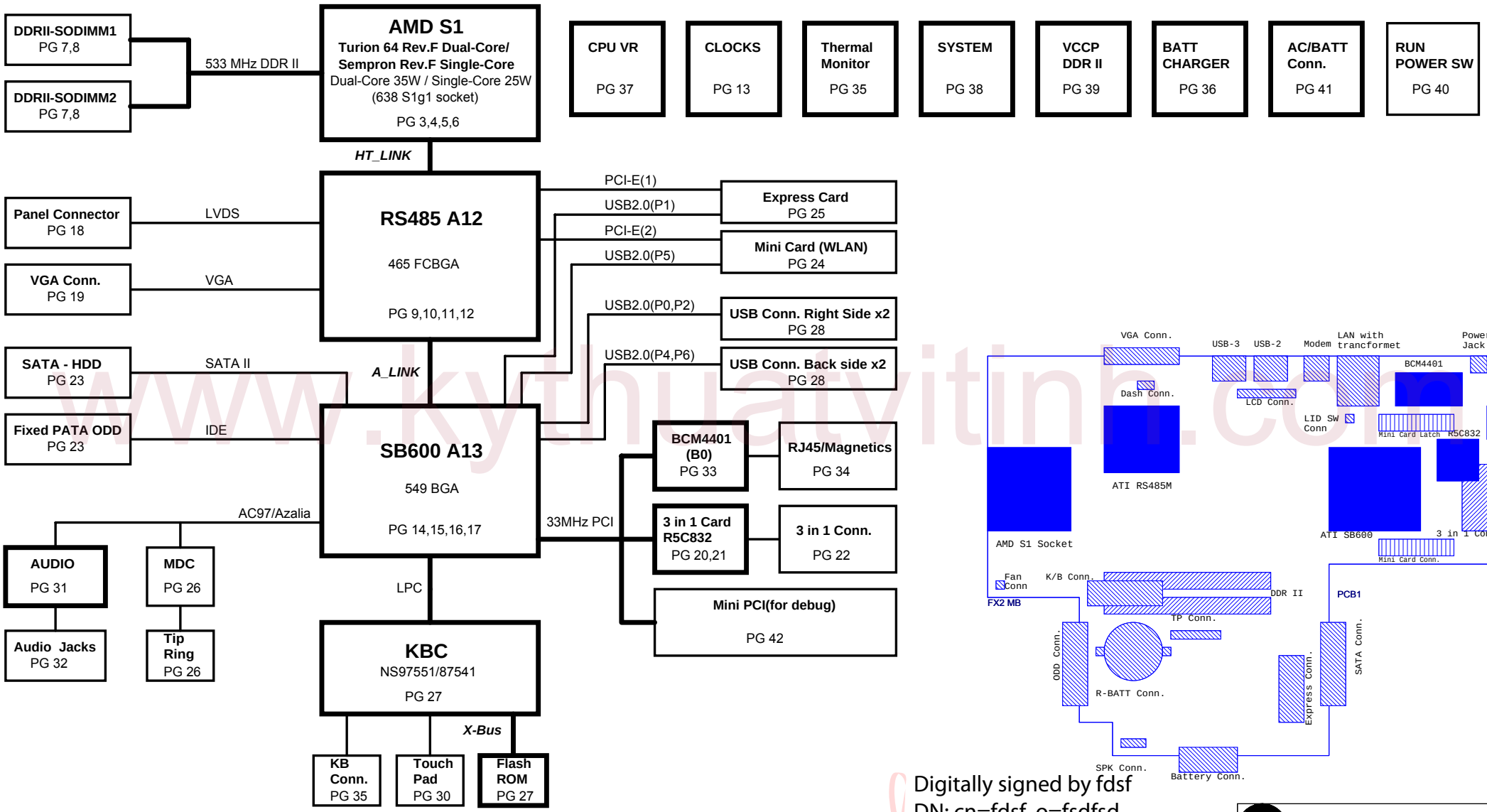
Kirin (FX2 with NS) VER : 1A



QUANTA COMPUTER

Title	BLOCK DIAGRAM	
Size	Document Number FX2	Rev 1A
Date: Friday, May 05, 2006	Sheet 1 of 47	

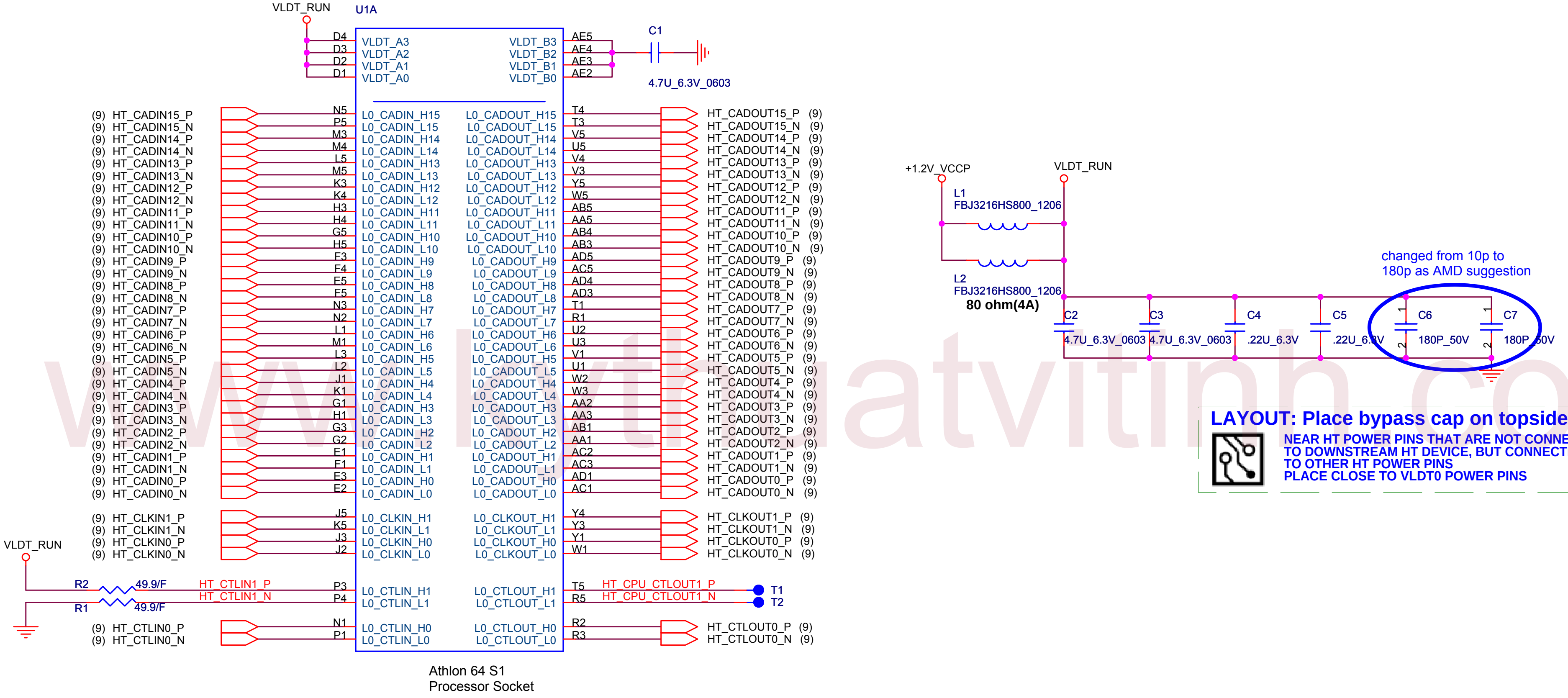
INDEX

QUANTA COMPUTER

Title	FRONT PAGE	
Size	Document Number FX2	Rev 1A
Date: Thursday, May 04, 2006	Sheet 2 of 47	

PROCESSOR HYPERTRANSPORT INTERFACE

VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



LAYOUT: Place bypass cap on topside of board

NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
PLACE CLOSE TO VLDT0 POWER PINS

QUANTA COMPUTER

Title	ATHLON64 HT I/F	
Size	Document Number FX2	Rev 1A
Date:	Friday, May 05, 2006	Sheet 3 of 47

Processor DDR2 Memory Interface

VDD_VTT_SUS_CPU IS CONNECTED TO THE VDD_VTT_SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

PLACE THEM CLOSE TO CPU WITHIN 1"

for +0.9V_DDR_VTT feedback

+1.8V_SUS

+0.9V_DDR_VTT

CPU_M_VREF

VTT_SENSE

R3 2K/F

R4 2K/F

C8 .1U_10V

C9 1000p_50V

C677 470P_50V

R6 39.2/F

R5 39.2/F

R566 0

U1B

MEMVREF

VTT_SENSE

MEMZN

MEMZP

M_ZN

M_ZP

MA0_CS_L3 MA0_CS_L2 MA0_CS_L1 MA0_CS_L0

MB0_CS_L3 MB0_CS_L2 MB0_CS_L1 MB0_CS_L0

MA0_CLK_H2 MA0_CLK_L2 MA0_CLK_H1 MA0_CLK_L1

MB0_CLK_H2 MB0_CLK_L2 MB0_CLK_H1 MB0_CLK_L1

M_CLKOUT1 (7) M_CLKOUT1# (7) M_CLKOUT0 (7) M_CLKOUT0# (7)

M_CLKOUT4 (7) M_CLKOUT4# (7) M_CLKOUT3 (7) M_CLKOUT3# (7)

M_CKE3 M_CKE2 M_CKE1 M_CKE0

MB_CKE1 MB_CKE0 MA_CKE1 MA_CKE0

MB0_ODT1 MB0_ODT0 MA0_ODT1 MA0_ODT0

M_ODT3 (7,8) M_ODT2 (7,8) M_ODT1 (7,8) M_ODT0 (7,8)

M_A_A[0..15]

MA_ADD15 MA_ADD14 MA_ADD13 MA_ADD12 MA_ADD11 MA_ADD10 MA_ADD9 MA_ADD8 MA_ADD7 MA_ADD6 MA_ADD5 MA_ADD4 MA_ADD3 MA_ADD2 MA_ADD1 MA_ADD0

MB_ADD15 MB_ADD14 MB_ADD13 MB_ADD12 MB_ADD11 MB_ADD10 MB_ADD9 MB_ADD8 MB_ADD7 MB_ADD6 MB_ADD5 MB_ADD4 MB_ADD3 MB_ADD2 MB_ADD1 MB_ADD0

M_B_A[0..15] (7,8)

M_A_BS#2 M_A_BS#1 M_A_BS#0

MA_BANK2 MA_BANK1 MA_BANK0

MB_BANK2 MB_BANK1 MB_BANK0

M_B_BS#2 (7,8) M_B_BS#1 (7,8) M_B_BS#0 (7,8)

M_A_RAS# M_A_CAS# M_A_WE#

MA_RAS_L MA_CAS_L MA_WE_L

MB_RAS_L MB_CAS_L MB_WE_L

M_B_RAS# (7,8) M_B_CAS# (7,8) M_B_WE# (7,8)

DDR II: CMD/CTRL/CLK

Athlon 64 S1
Processor Socket

U1C

(7) M_B_DQ[0..63]

M_B_DQ63 M_B_DQ62 M_B_DQ61 M_B_DQ60 M_B_DQ59 M_B_DQ58 M_B_DQ57 M_B_DQ56 M_B_DQ55 M_B_DQ54 M_B_DQ53 M_B_DQ52 M_B_DQ51 M_B_DQ50 M_B_DQ49 M_B_DQ48 M_B_DQ47 M_B_DQ46 M_B_DQ45 M_B_DQ44 M_B_DQ43 M_B_DQ42 M_B_DQ41 M_B_DQ40 M_B_DQ39 M_B_DQ38 M_B_DQ37 M_B_DQ36 M_B_DQ35 M_B_DQ34 M_B_DQ33 M_B_DQ32 M_B_DQ31 M_B_DQ30 M_B_DQ29 M_B_DQ28 M_B_DQ27 M_B_DQ26 M_B_DQ25 M_B_DQ24 M_B_DQ23 M_B_DQ22 M_B_DQ21 M_B_DQ20 M_B_DQ19 M_B_DQ18 M_B_DQ17 M_B_DQ16 M_B_DQ15 M_B_DQ14 M_B_DQ13 M_B_DQ12 M_B_DQ11 M_B_DQ10 M_B_DQ9 M_B_DQ8 M_B_DQ7 M_B_DQ6 M_B_DQ5 M_B_DQ4 M_B_DQ3 M_B_DQ2 M_B_DQ1 M_B_DQ0

MB_DATA63 MB_DATA62 MB_DATA61 MB_DATA60 MB_DATA59 MB_DATA58 MB_DATA57 MB_DATA56 MB_DATA55 MB_DATA54 MB_DATA53 MB_DATA52 MB_DATA51 MB_DATA50 MB_DATA49 MB_DATA48 MB_DATA47 MB_DATA46 MB_DATA45 MB_DATA44 MB_DATA43 MB_DATA42 MB_DATA41 MB_DATA40 MB_DATA39 MB_DATA38 MB_DATA37 MB_DATA36 MB_DATA35 MB_DATA34 MB_DATA33 MB_DATA32 MB_DATA31 MB_DATA30 MB_DATA29 MB_DATA28 MB_DATA27 MB_DATA26 MB_DATA25 MB_DATA24 MB_DATA23 MB_DATA22 MB_DATA21 MB_DATA20 MB_DATA19 MB_DATA18 MB_DATA17 MB_DATA16 MB_DATA15 MB_DATA14 MB_DATA13 MB_DATA12 MB_DATA11 MB_DATA10 MB_DATA9 MB_DATA8 MB_DATA7 MB_DATA6 MB_DATA5 MB_DATA4 MB_DATA3 MB_DATA2 MB_DATA1 MB_DATA0

MA_DATA63 MA_DATA62 MA_DATA61 MA_DATA60 MA_DATA59 MA_DATA58 MA_DATA57 MA_DATA56 MA_DATA55 MA_DATA54 MA_DATA53 MA_DATA52 MA_DATA51 MA_DATA50 MA_DATA49 MA_DATA48 MA_DATA47 MA_DATA46 MA_DATA45 MA_DATA44 MA_DATA43 MA_DATA42 MA_DATA41 MA_DATA40 MA_DATA39 MA_DATA38 MA_DATA37 MA_DATA36 MA_DATA35 MA_DATA34 MA_DATA33 MA_DATA32 MA_DATA31 MA_DATA30 MA_DATA29 MA_DATA28 MA_DATA27 MA_DATA26 MA_DATA25 MA_DATA24 MA_DATA23 MA_DATA22 MA_DATA21 MA_DATA20 MA_DATA19 MA_DATA18 MA_DATA17 MA_DATA16 MA_DATA15 MA_DATA14 MA_DATA13 MA_DATA12 MA_DATA11 MA_DATA10 MA_DATA9 MA_DATA8 MA_DATA7 MA_DATA6 MA_DATA5 MA_DATA4 MA_DATA3 MA_DATA2 MA_DATA1 MA_DATA0

M_A_DQ[0..63] (7)

M_A_DQ63 M_A_DQ62 M_A_DQ61 M_A_DQ60 M_A_DQ59 M_A_DQ58 M_A_DQ57 M_A_DQ56 M_A_DQ55 M_A_DQ54 M_A_DQ53 M_A_DQ52 M_A_DQ51 M_A_DQ50 M_A_DQ49 M_A_DQ48 M_A_DQ47 M_A_DQ46 M_A_DQ45 M_A_DQ44 M_A_DQ43 M_A_DQ42 M_A_DQ41 M_A_DQ40 M_A_DQ39 M_A_DQ38 M_A_DQ37 M_A_DQ36 M_A_DQ35 M_A_DQ34 M_A_DQ33 M_A_DQ32 M_A_DQ31 M_A_DQ30 M_A_DQ29 M_A_DQ28 M_A_DQ27 M_A_DQ26 M_A_DQ25 M_A_DQ24 M_A_DQ23 M_A_DQ22 M_A_DQ21 M_A_DQ20 M_A_DQ19 M_A_DQ18 M_A_DQ17 M_A_DQ16 M_A_DQ15 M_A_DQ14 M_A_DQ13 M_A_DQ12 M_A_DQ11 M_A_DQ10 M_A_DQ9 M_A_DQ8 M_A_DQ7 M_A_DQ6 M_A_DQ5 M_A_DQ4 M_A_DQ3 M_A_DQ2 M_A_DQ1 M_A_DQ0

To SODIMM socket B (Far)

To SODIMM socket A (near)

(7) M_B_DM[0..7]

M_B_DM7 M_B_DM6 M_B_DM5 M_B_DM4 M_B_DM3 M_B_DM2 M_B_DM1 M_B_DM0

MB_DM7 MB_DM6 MB_DM5 MB_DM4 MB_DM3 MB_DM2 MB_DM1 MB_DM0

MA_DM7 MA_DM6 MA_DM5 MA_DM4 MA_DM3 MA_DM2 MA_DM1 MA_DM0

M_A_DM7 M_A_DM6 M_A_DM5 M_A_DM4 M_A_DM3 M_A_DM2 M_A_DM1 M_A_DM0

M_A_DM[0..7] (7)

M_B_DQS7 M_B_DQS#7 M_B_DQS6 M_B_DQS#6 M_B_DQS5 M_B_DQS#5 M_B_DQS4 M_B_DQS#4 M_B_DQS3 M_B_DQS#3 M_B_DQS2 M_B_DQS#2 M_B_DQS1 M_B_DQS#1 M_B_DQS0 M_B_DQS#0

MB_DQS_H7 MB_DQS_L7 MB_DQS_H6 MB_DQS_L6 MB_DQS_H5 MB_DQS_L5 MB_DQS_H4 MB_DQS_L4 MB_DQS_H3 MB_DQS_L3 MB_DQS_H2 MB_DQS_L2 MB_DQS_H1 MB_DQS_L1 MB_DQS_H0 MB_DQS_L0

MA_DQS_H7 MA_DQS_L7 MA_DQS_H6 MA_DQS_L6 MA_DQS_H5 MA_DQS_L5 MA_DQS_H4 MA_DQS_L4 MA_DQS_H3 MA_DQS_L3 MA_DQS_H2 MA_DQS_L2 MA_DQS_H1 MA_DQS_L1 MA_DQS_H0 MA_DQS_L0

M_A_DQS7 M_A_DQS#7 M_A_DQS6 M_A_DQS#6 M_A_DQS5 M_A_DQS#5 M_A_DQS4 M_A_DQS#4 M_A_DQS3 M_A_DQS#3 M_A_DQS2 M_A_DQS#2 M_A_DQS1 M_A_DQS#1 M_A_DQS0 M_A_DQS#0

(7) M_B_DQS[0..7]

M_B_DQS0 M_B_DQS1 M_B_DQS2 M_B_DQS3 M_B_DQS4 M_B_DQS5 M_B_DQS6 M_B_DQS7

(7) M_B_DQS#[0..7]

M_B_DQS#0 M_B_DQS#1 M_B_DQS#2 M_B_DQS#3 M_B_DQS#4 M_B_DQS#5 M_B_DQS#6 M_B_DQS#7

(7) M_A_DQS[0..7]

M_A_DQS0 M_A_DQS1 M_A_DQS2 M_A_DQS3 M_A_DQS4 M_A_DQS5 M_A_DQS6 M_A_DQS7

(7) M_A_DQS#[0..7]

M_A_DQS#0 M_A_DQS#1 M_A_DQS#2 M_A_DQS#3 M_A_DQS#4 M_A_DQS#5 M_A_DQS#6 M_A_DQS#7

DDR: DATA

Athlon 64 S1
Processor Socket

+0.9V_DDR_VTT

C10 4.7U_6.3V_0603 C11 4.7U_6.3V_0603 C12 4.7U_6.3V_0603 C13 4.7U_6.3V_0603 C14 .22U_6.3V C15 .22U_6.3V C16 .22U_6.3V C17 .22U_6.3V

+0.9V_DDR_VTT

C18 1000p_50V C19 1000p_50V C20 1000p_50V C21 1000p_50V C22 180P_50V C23 180P_50V C24 180P_50V C25 180P_50V

QUANTA COMPUTER

Title: ATHLON64 DDRII MEMORY

Size: | Document Number: FX2 | Rev: 1A

Date: Friday, May 05, 2006 | Sheet 4 of 47

ATHLON Control and Debug

LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

CPU_VDDA_RUN

+2.5V_RUN
BLM18PG330SN1D_0603
L3
CPU_VDDA_RUN
C26 4.7U_6.3V_0603
C27 .22U_6.3V
C28 3900p_25V
C29 100U_6.3V_3528

(13) CPUCLK — C30 3900p_25V — CPU_CLKIN_SC_P
R14 169/F_0603
(13) CPUCLK# — C31 3900p_25V — CPU_CLKIN_SC_N

R14 close U1 within 600 mil , C30 & C31 close U1 within 1250 mil

If AMD SI is not used, the SID pin can be left unconnected and SIC should have a 300-Ω (±5%) pulldown to VSS.

+1.8V_SUS
R7 *300_NC
R9 *300_NC
R10 300
(14) CPU_SIC — R523 *0_NC
(14) CPU_SID — R524 *0_NC
CPU_SIC_R
CPU_SID_R

for CPU rev.F , if for rev.G , populate R7,R9,R523,R524 and depopulate R10

VLDT_RUN
place them to CPU within 1"
R13 44.2/F
R12 44.2/F
CPU_HTREF1
CPU_HTREF0

To Power
(37) COREFB+V
(37) COREFB-
(39) VDDIO_FB_H
VDDIO_FB_H
R567 0
C678 *
470P_50V
CPU_CLKIN_SC_P
CPU_CLKIN_SC_N

for +1.8V_SUS feedback

+1.8V_SUS
R551 300
R8 300
H_THERMTRIP# (35)

U1D
CPU_VDDA_RUN
VDDA2
VDDA1
THERMTRIP_L
PROCHOT_L
AF6 H_THERMTRIP#
AC7 H_PROCHOT#

T6 CPU_HT_RESET#
T5 CPU_ALL_PWROK
T7 CPU_LDTSTOP#
RESET_L
PWROK
LDTSTOP_L

CPU_SIC_R
CPU_SID_R
SIC
SID
HT_REF1
HT_REF0
VDD_FB_H
VDD_FB_L
VDDIO_FB_H
VDDIO_FB_L
CLKIN_H
CLKIN_L

VID5 (37)
VID4 (37)
VID3 (37)
VID2 (37)
VID1 (37)
VID0 (37)

CPU_PRESENT_L
AC6 CPU_PRESENT#
PSI_L
A3 PSI# (37)
T11

PSI_L is a Power Status Indicator signal. This signal is asserted when the processor is in a low powerstate. PSI_L should be connected to the power supply controller, if the controller supports "skipmode, or diode emulation mode". PSI_L is asserted by the processor during the C3 and S1 states.

CPU_DBRDY
DBRDY
CPU_TMS
CPU_TCK
CPU_TRST#
CPU_TDI
TMS
TCK
TRST_L
TDI
DBREQ_L
E10 CPU_DBREQ#
TDO
AF9 CPU_TDO

C9 CPU_TEST29_H_FBCLKOUT_P
C8 CPU_TEST29_L_FBCLKOUT_N
R16 80.6/F
ROUTE AS 80 Ohm DIFFERENTIAL PAIR PLACE IT CLOSE TO CPU WITHIN 1"

CPU_TEST25_H_BYPASSCLK_H
CPU_TEST25_L_BYPASSCLK_L
CPU_TEST19_PLLTEST0
CPU_TEST18_PLLTEST1
CPU_TEST17_BP3
CPU_TEST16_BP2
CPU_TEST07_ANALOG_T
CPU_TEST6_DIECRACKMON
CPU_TEST5_THERMDC
CPU_TEST4_THERMDA
CPU_TEST3_GATE0
CPU_TEST2_DRAIN0
TEST25_H
TEST25_L
TEST19
TEST18
TEST13
TEST9
TEST17
TEST16
TEST15
TEST14
TEST12
TEST7
TEST6
TEST5
TEST4
TEST3
TEST2
TEST29_H
TEST29_L
TEST24
TEST23
TEST22
TEST21
TEST20
TEST28_H
TEST28_L
TEST27
TEST26
TEST10
TEST8
CPU_TEST23_TSTUPD T14
CPU_TEST21_SCANEN
CPU_TEST28_H_PLLCHRZ_P T18
CPU_TEST28_L_PLLCHRZ_N T17
CPU_TEST26_BURNIN# T20
CPU_TEST10_ANALOGOUT T22
CPU_TEST08_DIG_T

(35) CPU_TEST5_THERMDC
(35) CPU_TEST4_THERMDA
add port to Page 35 U36 Thermal IC

RSVD0
RSVD1
RSVD2
RSVD3
RSVD4
RSVD5
RSVD6
RSVD7
RSVD8
RSVD9
RSVD10
RSVD11
RSVD12
RSVD13
RSVD14
RSVD15
RSVD16
RSVD17
RSVD18
RSVD19
RSVD20
CPU_MA_RESET# T25
CPU_MB_RESET# T27
CPU_RSVD_VIDSTRB1 T30
CPU_RSVD_VIDSTRB0 T29
CPU_RSVD_VDDNB_FB_P T31
CPU_RSVD_VDDNB_FB_N T32
CPU_RSVD_CORE_TYPE T33
MISC

AMD NPT S1 SOCKET
Processor Socket

change TEST 12/14/15/20/22/24/27 to be NC pin without pull up or pull down

(14,15) CPU_PWRGD — R19 0 — CPU_ALL_PWROK
R525 10K
(11,14) LDT_STOP# — R20 0 — CPU_LDTSTOP#
R526 10K
(14) LDT_RST# — R527 0 — CPU_HT_RESET#
R528 10K

change for SB600 from SB460

R527 can be used for EMI verifing, place close to CPU

+1.8V_RUN
+1.8V_SUS
R24 *10K_NC
R27 300
Q2 *MMBT3904_NC
H_PROCHOT#
CPU_EC_PROCHOT# (27)
CPU_PROCHOT# (15)
*MMBT3904_NC Q49

0428 : depopulate R24 & Q2 , because AMD Errata 141 "PROCHOT_L should not be used as an output from the processor"

SB this pin is 3.3V,need it level-shift.

delete ED5 H_THERMTRIP# circuit

CPU_TEST26_BURNIN# R22 300
CPU_PRESENT# R25 1K/F
CPU_TEST25_H_BYPASSCLK_H R26 510/F
CPU_TEST21_SCANEN R32 300
CPU_TEST25_L_BYPASSCLK_L R44 510/F
CPU_TEST19_PLLTEST0 R45 300
CPU_TEST18_PLLTEST1 R46 300
If no use which Net need pull-up or down

add HDT connector for debug convenience

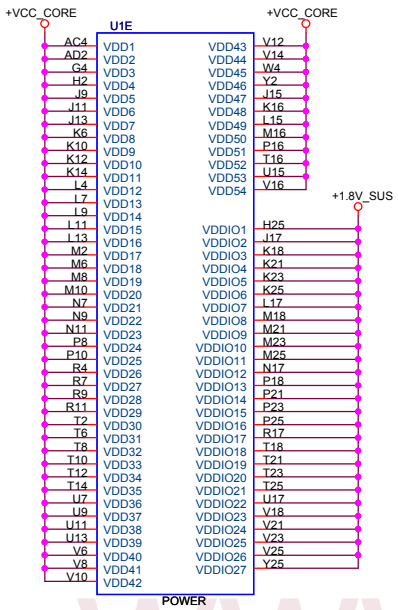
HDT CONNECTOR

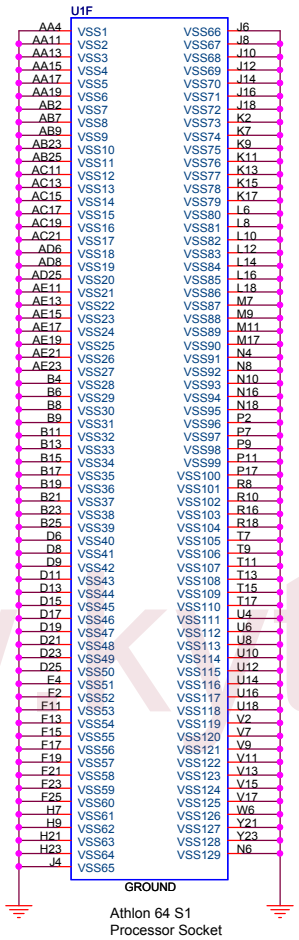
JHDT1
GND
Resreved
DBREQ_L
DBRDY
TCK
TMS
TDI
TRST_L
TDO
VDDIO
RESET_L
CPU_DBREQ#
CPU_DBRDY
CPU_TCK
CPU_TMS
CPU_TDI
CPU_TRST#
CPU_TDO
*HDT conn_NC
+3.3V_SUS
R580 *10K_NC
R581 *10K_NC
Q55 *MMBT3904_NC
CPU_RESET#
CPU_HT_RESET#

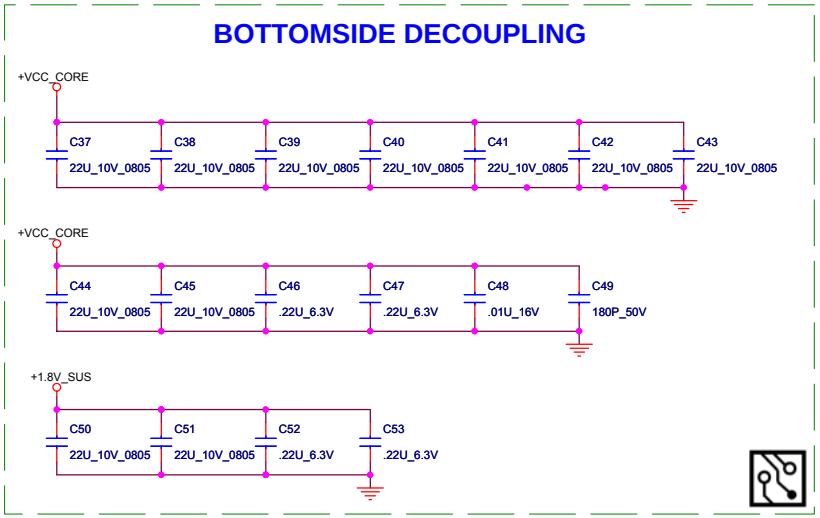
delete ED5 thermal sensor

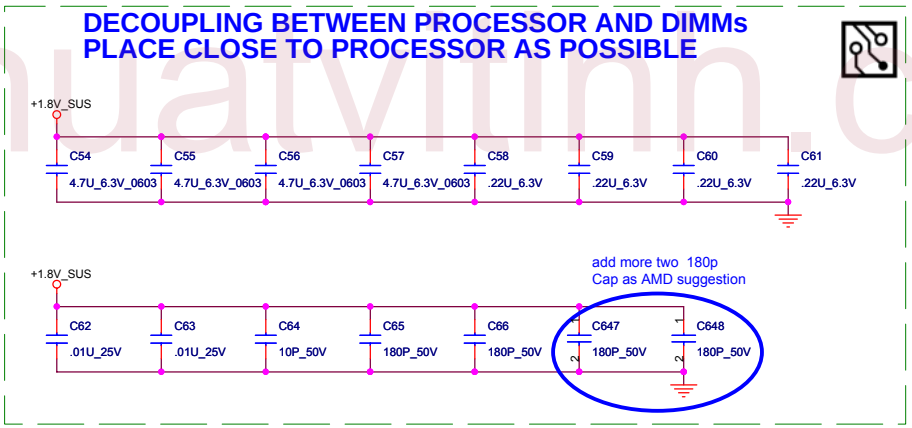
QUANTA COMPUTER

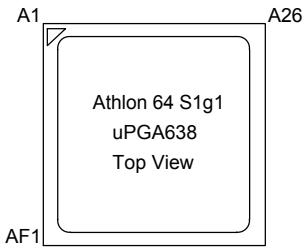
Title	ATHLON64 CTRL & DEBUG	
Size	Document Number FX2	Rev 1A
Date: Friday, May 05, 2006	Sheet 5 of 47	







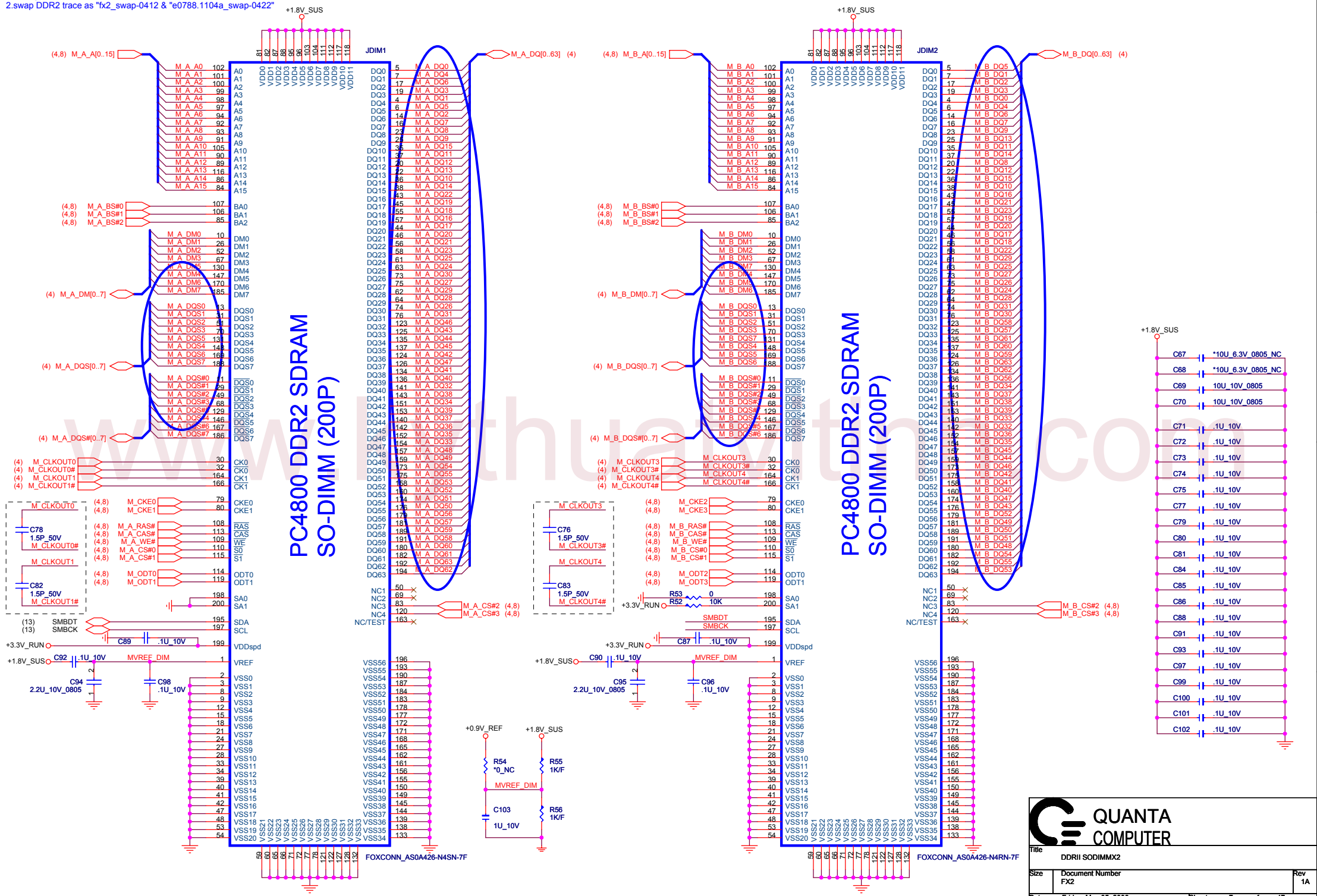




PROCESSOR POWER AND GROUND

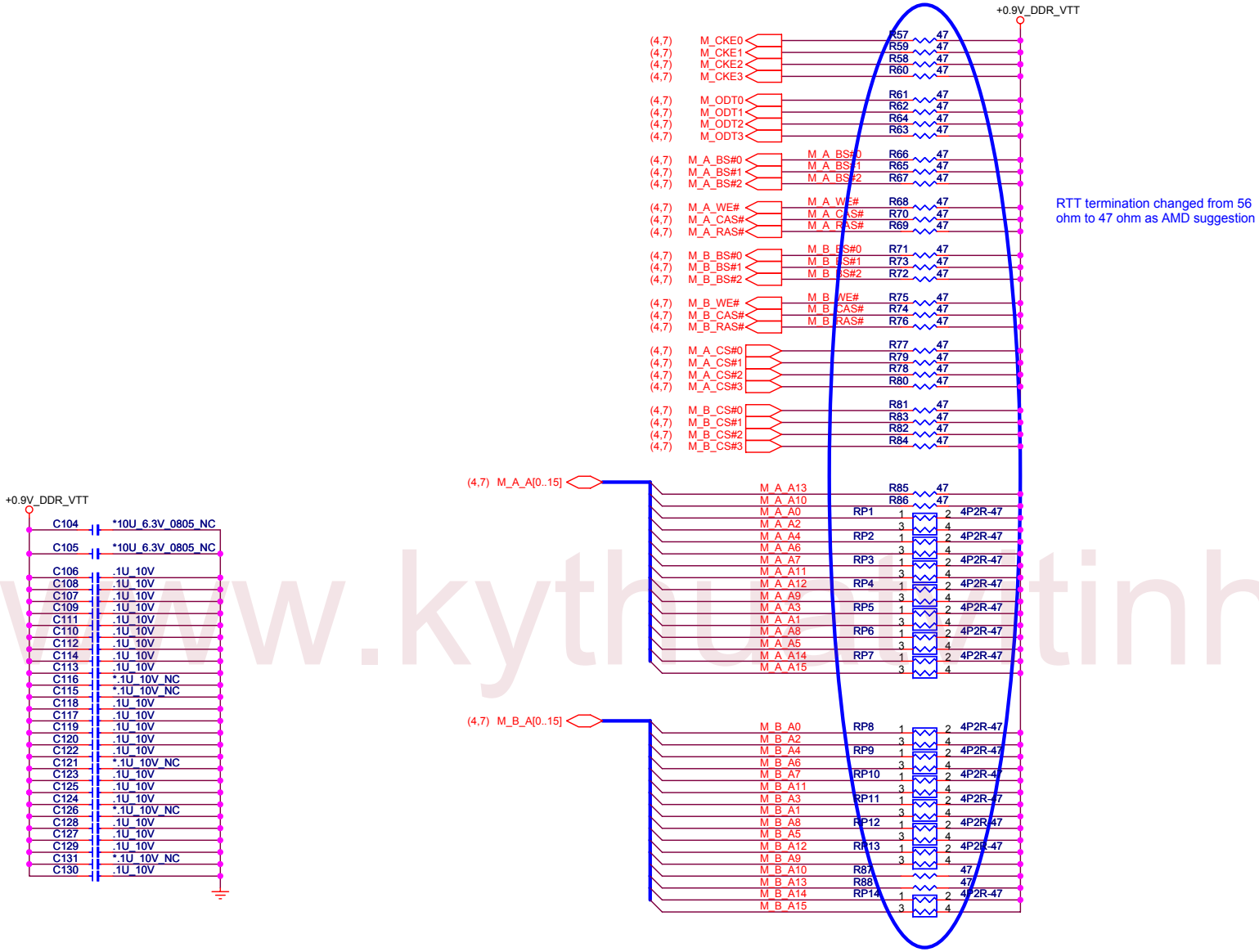
QUANTA COMPUTER		
Title: ATHLON64 PWR & GND		
Size	Document Number: FX2	Rev: 1A
Date: Thursday, May 04, 2006	Sheet 6 of 47	

1.Change DDR2 socket(P/N, Description, footprint, part reference, value)
2.swap DDR2 trace as "fx2_swap-0412 & "e0788.1104a_swap-0422"



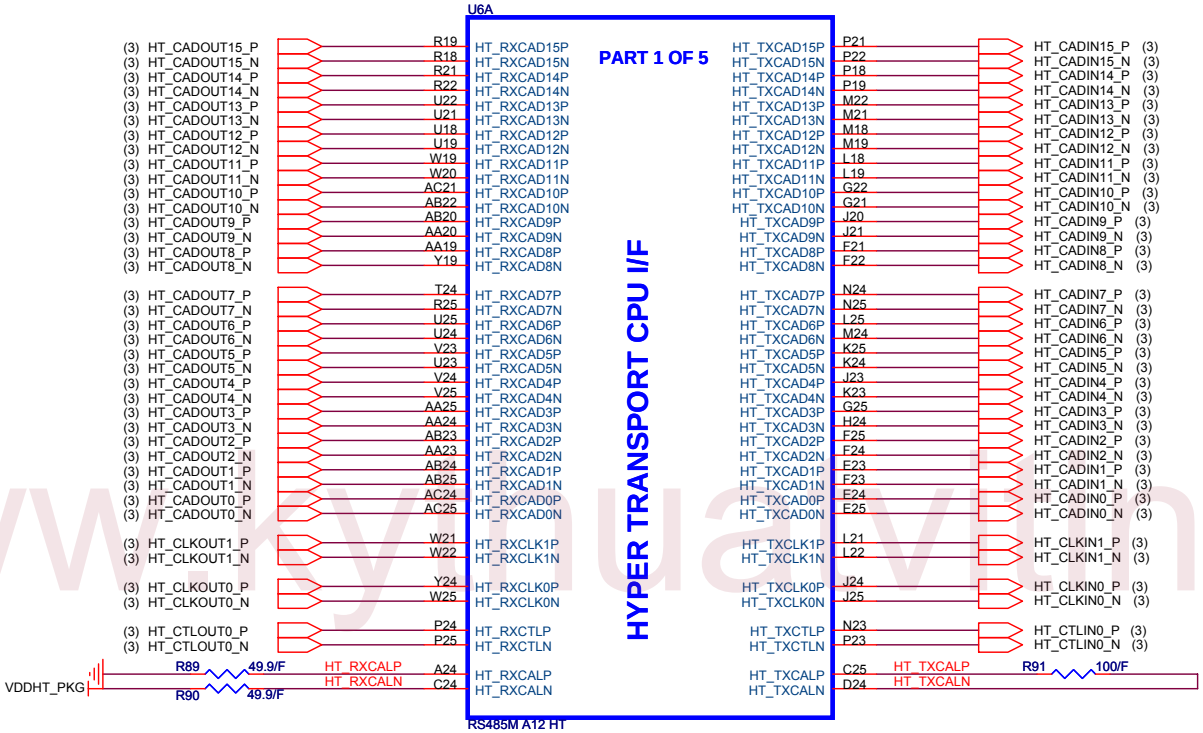
QUANTA COMPUTER

Title	DDRII SODIMMX2	
Size	Document Number FX2	Rev 1A
Date: Friday, May 05, 2006	Sheet 7 of 47	



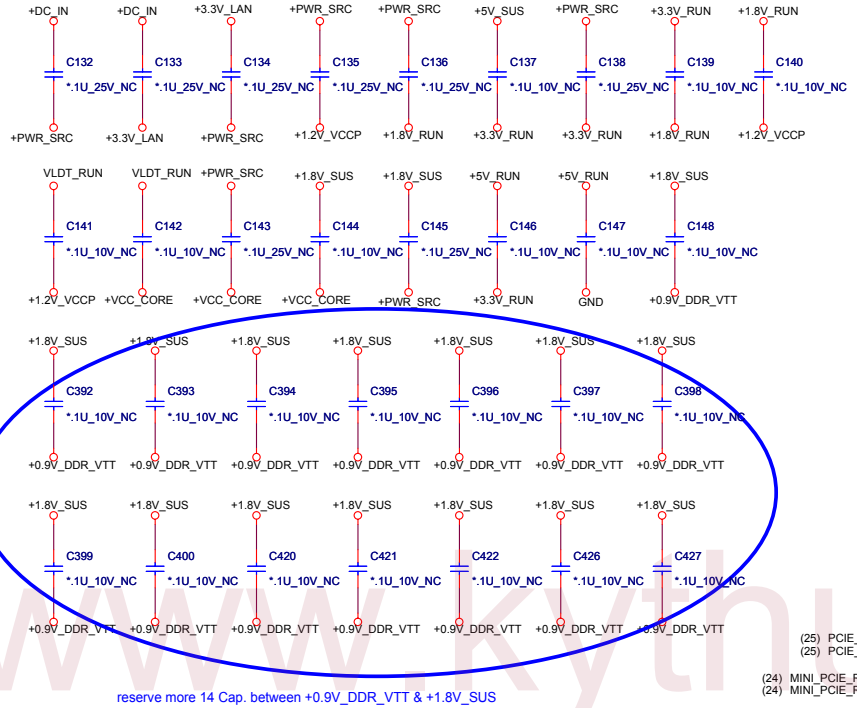
QUANTA COMPUTER

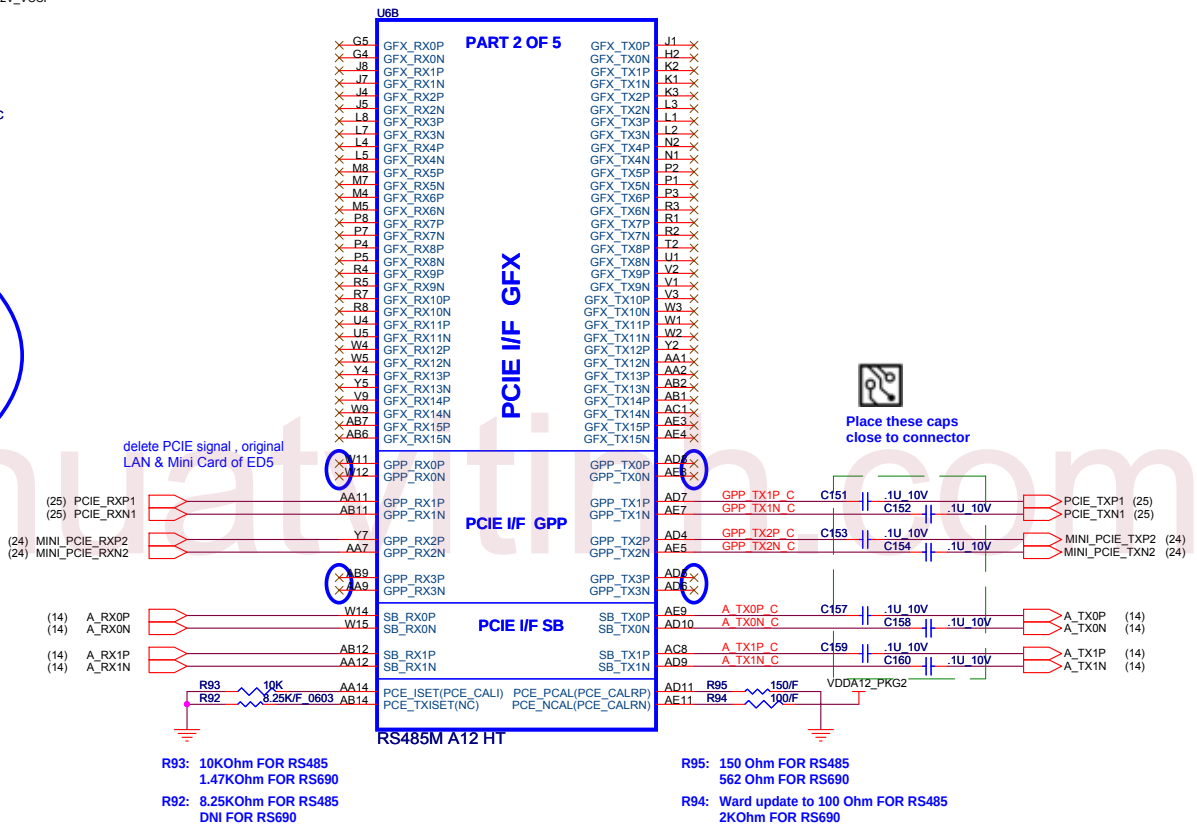
Title	DDRII TERMINATION	
Size	Document Number FX2	Rev 1A
Date: Friday, May 05, 2006	Sheet 8 of 47	



QUANTA COMPUTER

Title	RS485-HT LINK0 I/F		
Size	Document Number FX2		Rev 1A
Date: Friday, May 05, 2006		Sheet 9 of 47	





R93: 10KOhm FOR RS485
1.47KOhm FOR RS690

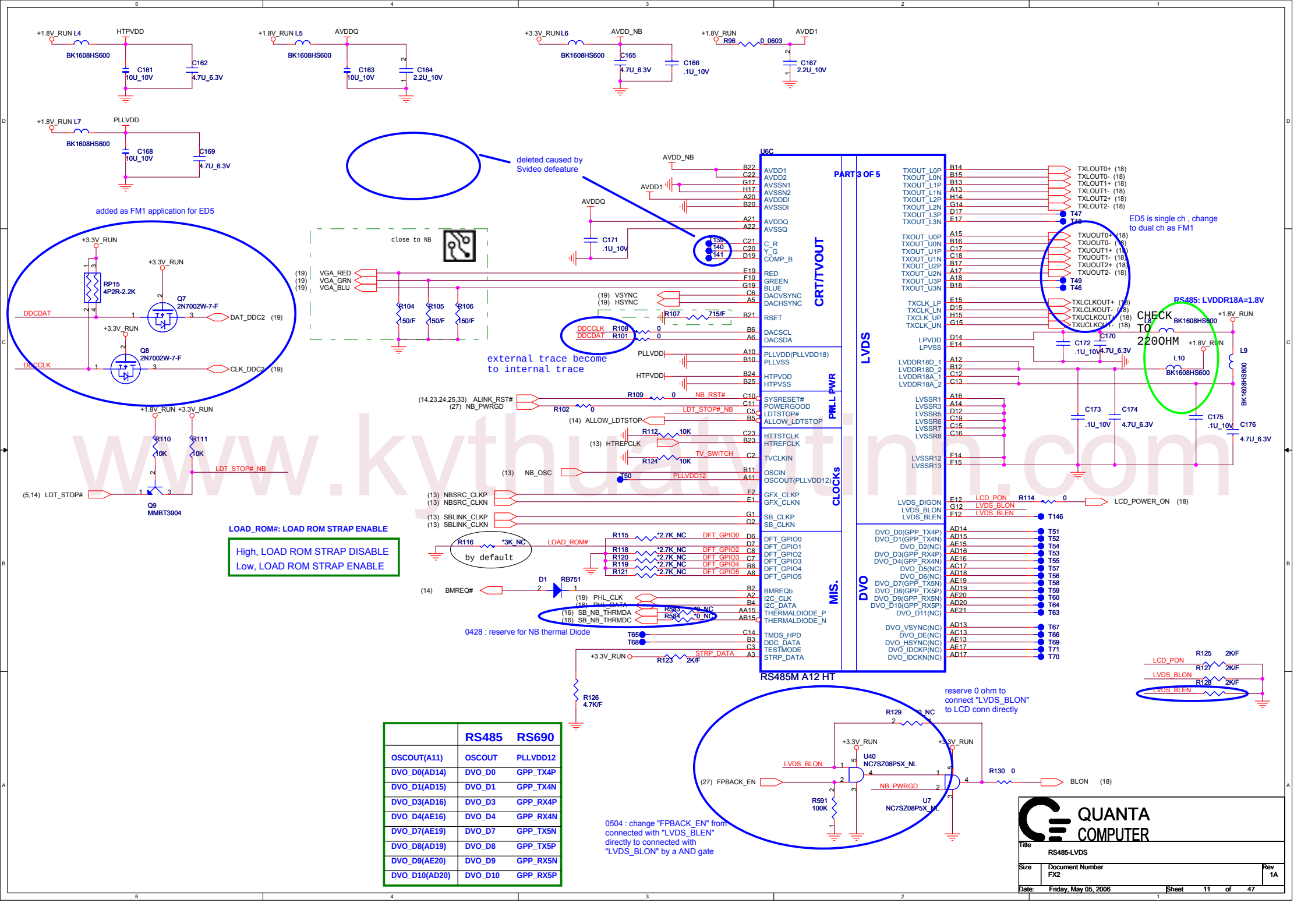
R92: 8.25KOhm FOR RS485
DNI FOR RS690

R95: 150 Ohm FOR RS485
562 Ohm FOR RS690

R94: Ward update to 100 Ohm FOR RS485
2KOhm FOR RS690

QUANTA COMPUTER

Title	RS485-PCIE LINK I/F	
Size	Document Number FX2	Rev 1A
Date: Friday, May 05, 2006	Sheet 10 of 47	

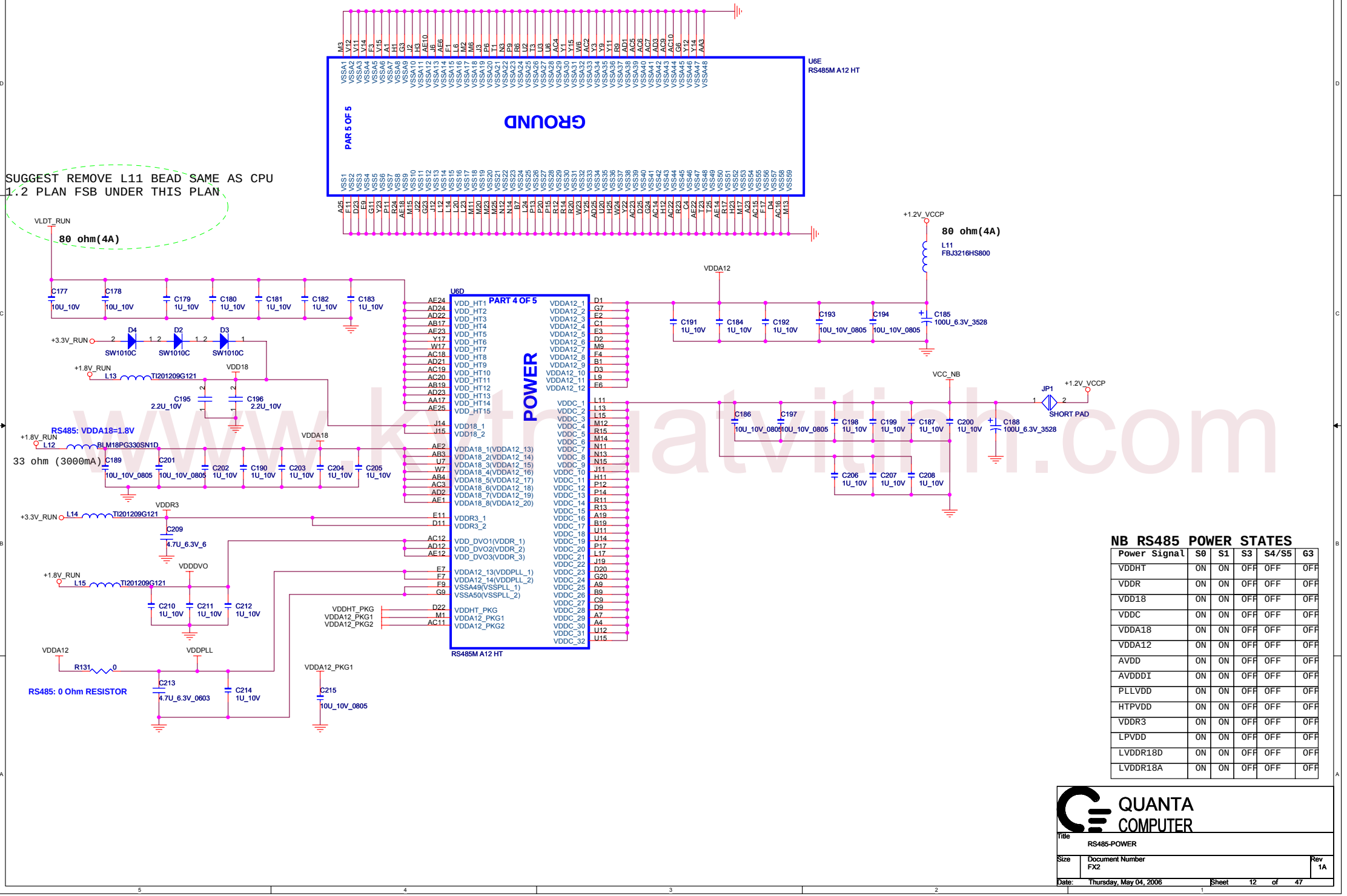


	RS485	RS690
OSCOUT(A11)	OSCOUT	PLLVDD12
DVO_D0(AD14)	DVO_D0	GPP_TX4P
DVO_D1(AD15)	DVO_D1	GPP_TX4N
DVO_D3(AD16)	DVO_D3	GPP_RX4P
DVO_D4(AE16)	DVO_D4	GPP_RX4N
DVO_D7(AE19)	DVO_D7	GPP_TX5N
DVO_D8(AD19)	DVO_D8	GPP_TX5P
DVO_D9(AE20)	DVO_D9	GPP_RX5N
DVO_D10(AD20)	DVO_D10	GPP_RX5P

QUANTA COMPUTER

Title	RS485-LVDS	
Size	Document Number FX2	Rev 1A
Date: Friday, May 05, 2006	Sheet 11 of 47	

SUGGEST REMOVE L11 BEAD SAME AS CPU
1.2 PLAN FSB UNDER THIS PLAN

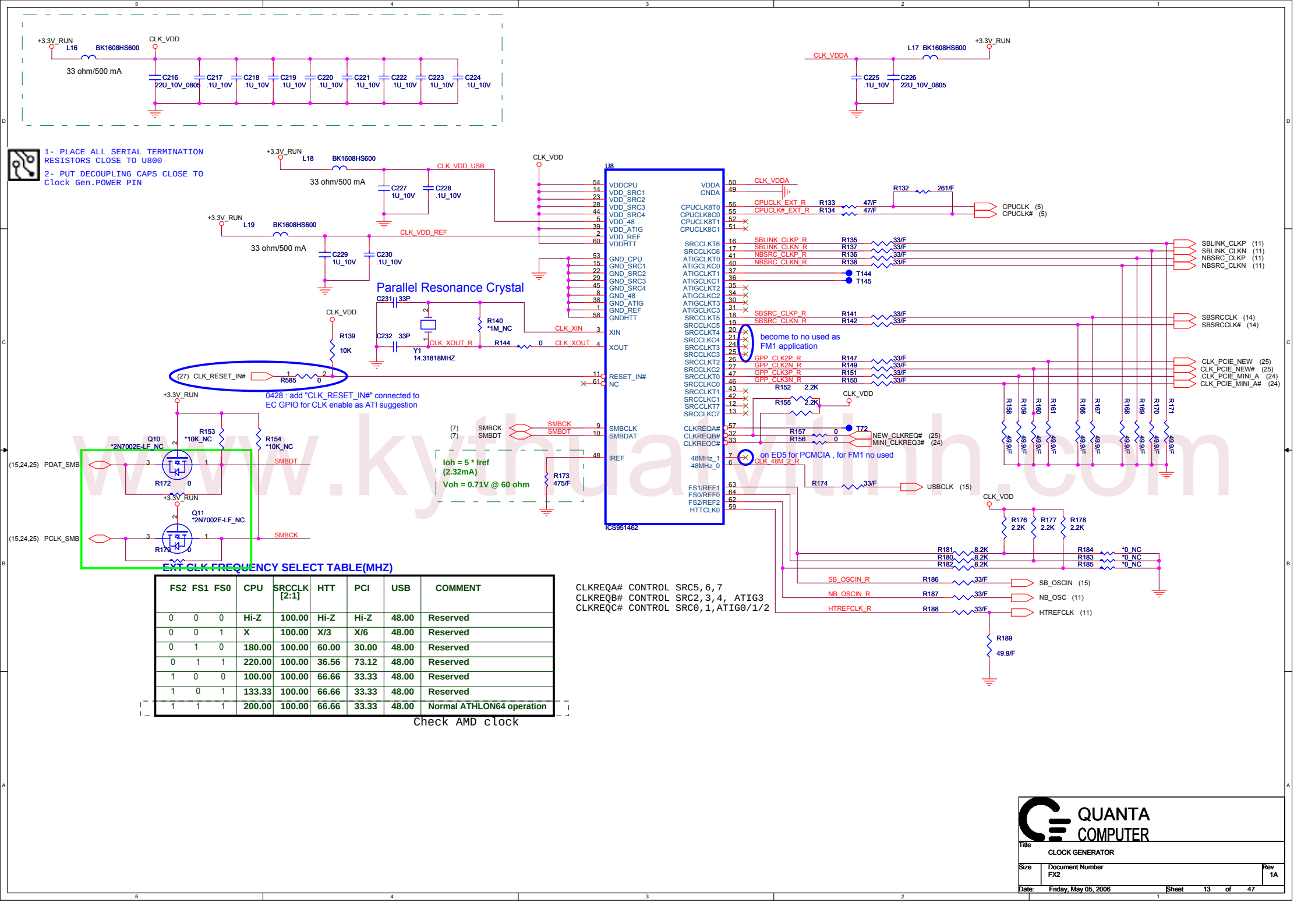


NB RS485 POWER STATES

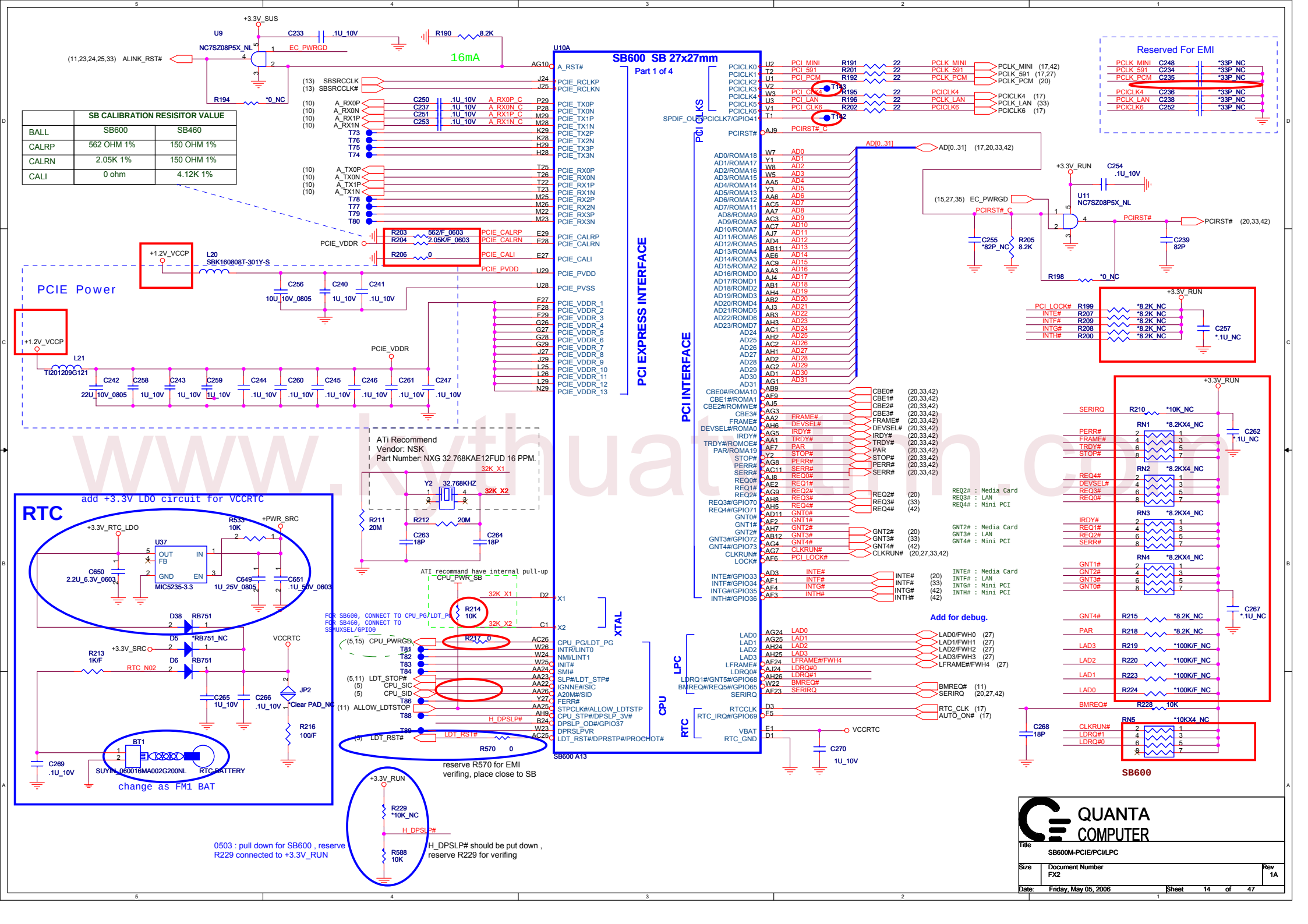
Power Signal	S0	S1	S3	S4/S5	G3
VDDHT	ON	ON	OFF	OFF	OFF
VDDR	ON	ON	OFF	OFF	OFF
VDD18	ON	ON	OFF	OFF	OFF
VDDC	ON	ON	OFF	OFF	OFF
VDDA18	ON	ON	OFF	OFF	OFF
VDDA12	ON	ON	OFF	OFF	OFF
AVDD	ON	ON	OFF	OFF	OFF
AVDDDI	ON	ON	OFF	OFF	OFF
PLLVDD	ON	ON	OFF	OFF	OFF
HTPVDD	ON	ON	OFF	OFF	OFF
VDDR3	ON	ON	OFF	OFF	OFF
LPVDD	ON	ON	OFF	OFF	OFF
LVDDR18D	ON	ON	OFF	OFF	OFF
LVDDR18A	ON	ON	OFF	OFF	OFF

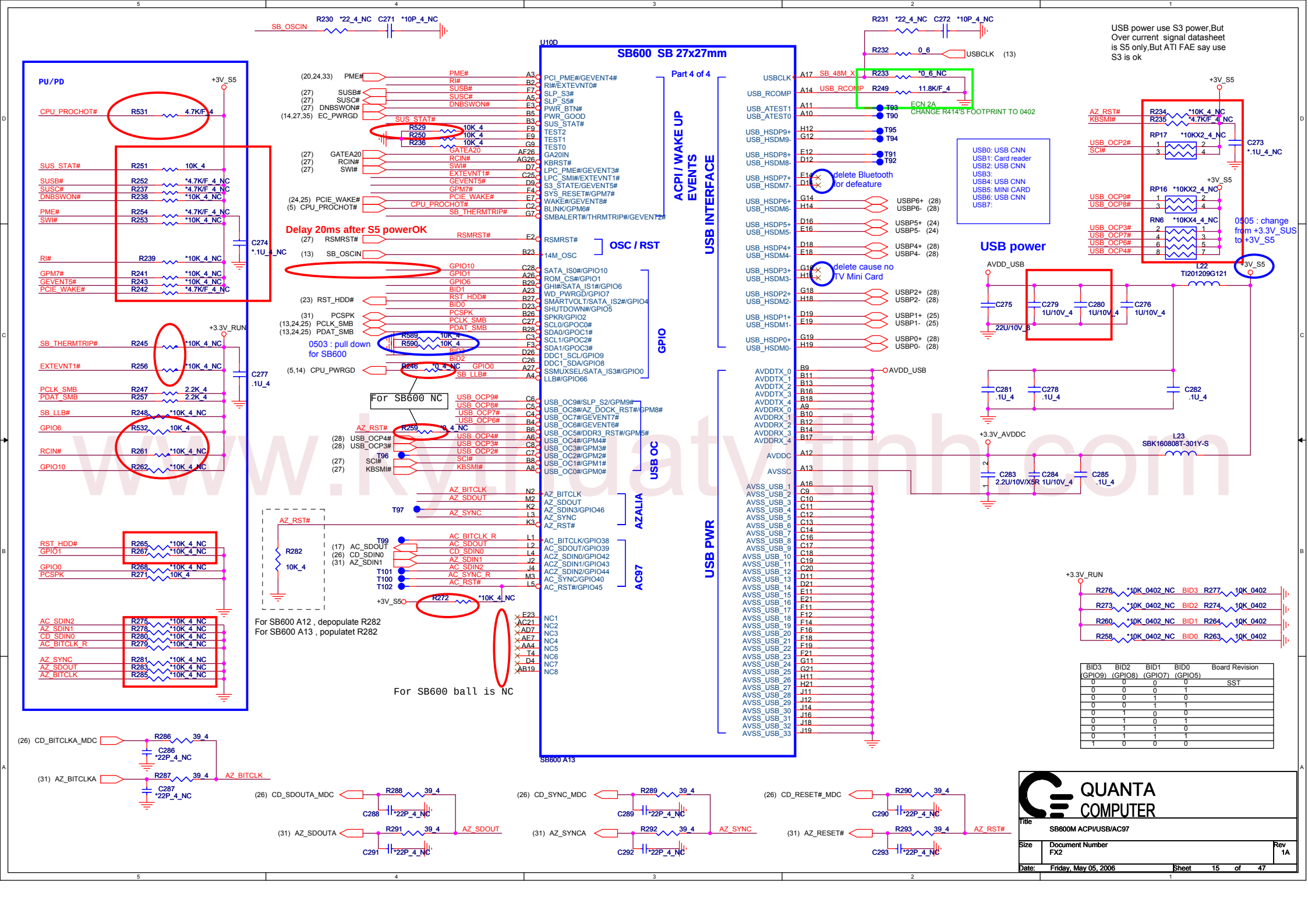
QUANTA COMPUTER

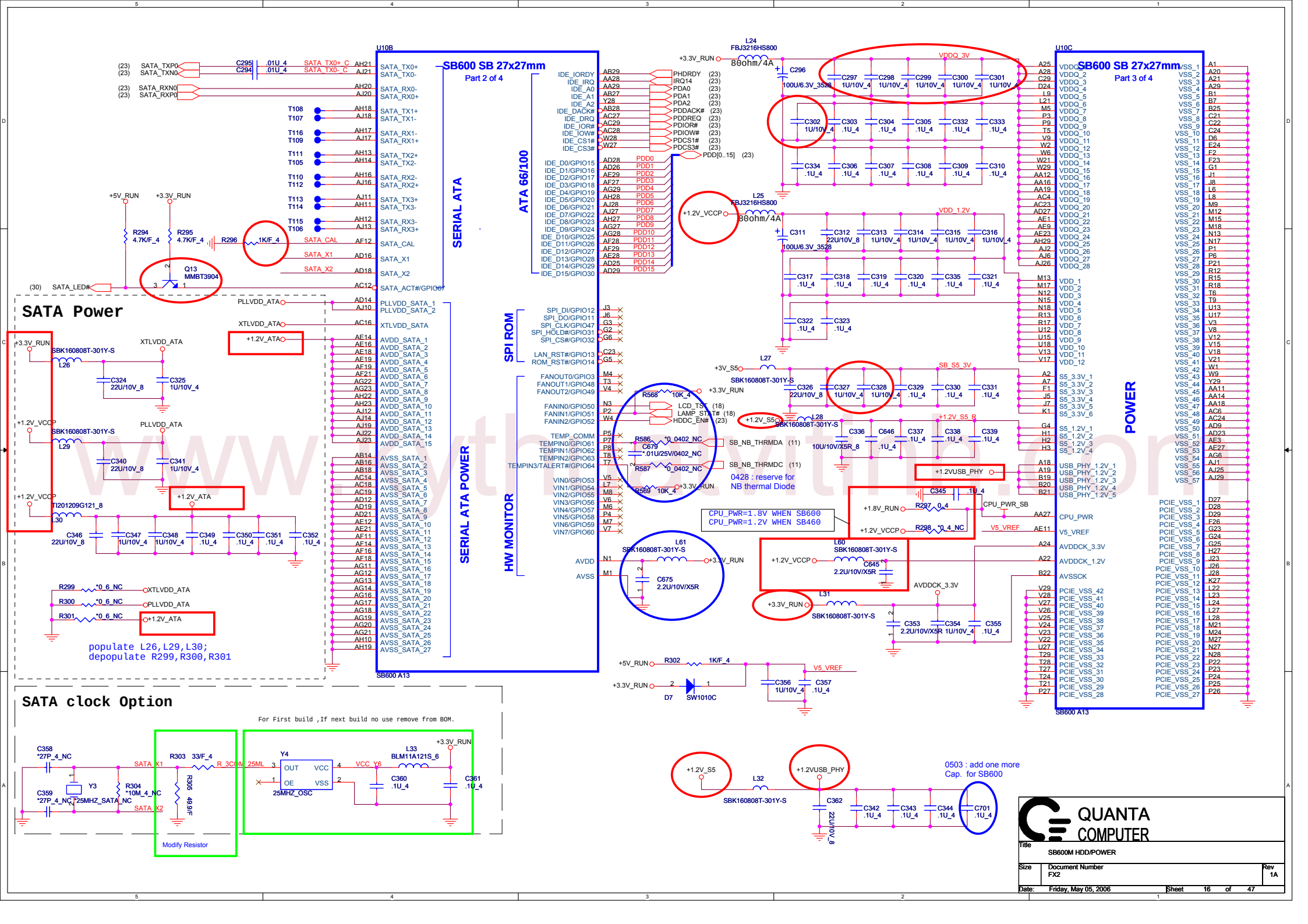
Title	RS485-POWER	
Size	Document Number FX2	Rev 1A
Date: Thursday, May 04, 2006	Sheet 12 of 47	



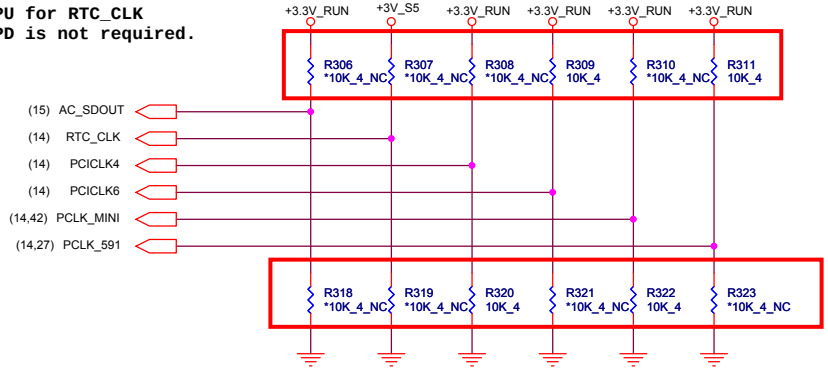
FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation


SB600 SB 27x27mm
Part 1 of 4
SB600 A13
PCI EXPRESS INTERFACE
PCI INTERFACE
PCI CLKS
XTAL
CPU
LPC
RTC
SB600
PCIE Power
RTC
add +3.3V LDO circuit for VCCRTC
change as FM1 BAT
ATi Recommend
Vendor: NSK
Part Number: NXG 32.768KAE12FUD 16 PPM.
ATI recommand have internal pull-up
reserve R570 for EMI
verifing, place close to SB
0503 : pull down for SB600 , reserve
R229 connected to +3.3V_RUN
H_DPSLP# should be put down ,
reserve R229 for verifing
Add for debug.
Reserved For EMI
16mA
SB CALIBRATION RESISITOR VALUE
BALL | SB600 | SB460
CALRP | 562 OHM 1% | 150 OHM 1%
CALRN | 2.05K 1% | 150 OHM 1%
CALI | 0 ohm | 4.12K 1%
QUANTA COMPUTER
Title: SB600M-PCIE/PCI/LPC
Size: Document Number: FX2
Rev: 1A
Date: Friday, May 05, 2006
Sheet 14 of 47


SB600 SB 27x27mm
U10D
Part 4 of 4
SB600 A13
PU/PD
ACPI / WAKE UP EVENTS
USB INTERFACE
OSC / RST
GPIO
USB OC
AZALIA
AC97
USB PWR
USB power
Delay 20ms after S5 powerOK
For SB600 NC
For SB600 A12 , depopulate R282
For SB600 A13 , populatet R282
For SB600 ball is NC
0503 : pull down for SB600
delete Bluetooth for defeature
delete cause no TV Mini Card
USB power use S3 power,But Over current signal datasheet is S5 only,But ATI FAE say use S3 is ok
USB0: USB CNN
USB1: Card reader
USB2: USB CNN
USB3:
USB4: USB CNN
USB5: MINI CARD
USB6: USB CNN
USB7:
ECN 2A
CHANGE R414'S FOOTPRINT TO 0402
0505 : change from +3.3V_SUS to +3V_S5
QUANTA COMPUTER
SB600M ACPI/USB/AC97
FX2
1A
Friday, May 05, 2006
15 of 47


SB600 SB 27x27mm
Part 2 of 4
SB600 SB 27x27mm
Part 3 of 4
SERIAL ATA
ATA 66/100
SPI ROM
HW MONITOR
SERIAL ATA POWER
POWER
SATA Power
SATA clock Option
populate L26,L29,L30;
depopulate R299,R300,R301
CPU_PWR=1.8V WHEN SB600
CPU_PWR=1.2V WHEN SB460
0428 : reserve for
NB thermal Diode
0503 : add one more
Cap. for SB600
For First build ,If next build no use remove from BOM.
Modify Resistor
SB600 A13
QUANTA
COMPUTER
SB600M HDD/POWER
Friday, May 05, 2006
16 of 47

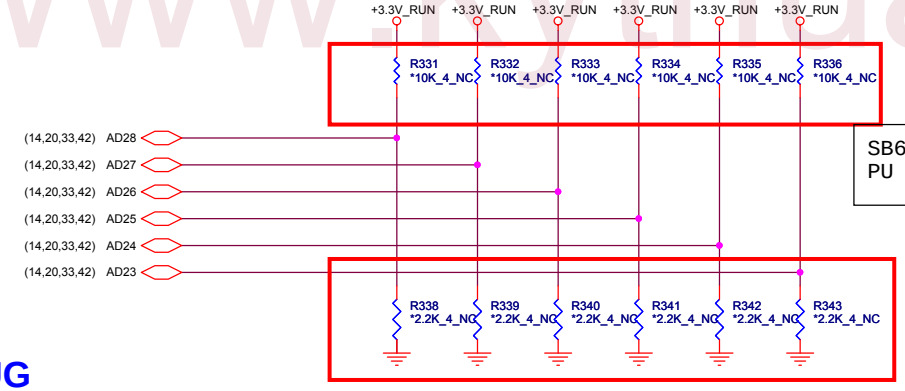
SB600 has 15K internal PD for AC_SDOUT
15K internal PU for RTC_CLK
,External PU/PD is not required.



delete SB460 setting

REQUIRED STRAPS

	AC_SDOUT	RTC_CLK	PCI_CLK4	PCI_CLK6	PCLK_MINI PCLK_591 PCI_CLK0 PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48 DEFAULT	CPU IF=K8 DEFAULT	H, H = PCI ROM H, L = SPI ROM
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ	CPU IF=P4	L, H = LPC ROM DEFAULT L, L = FWH ROM



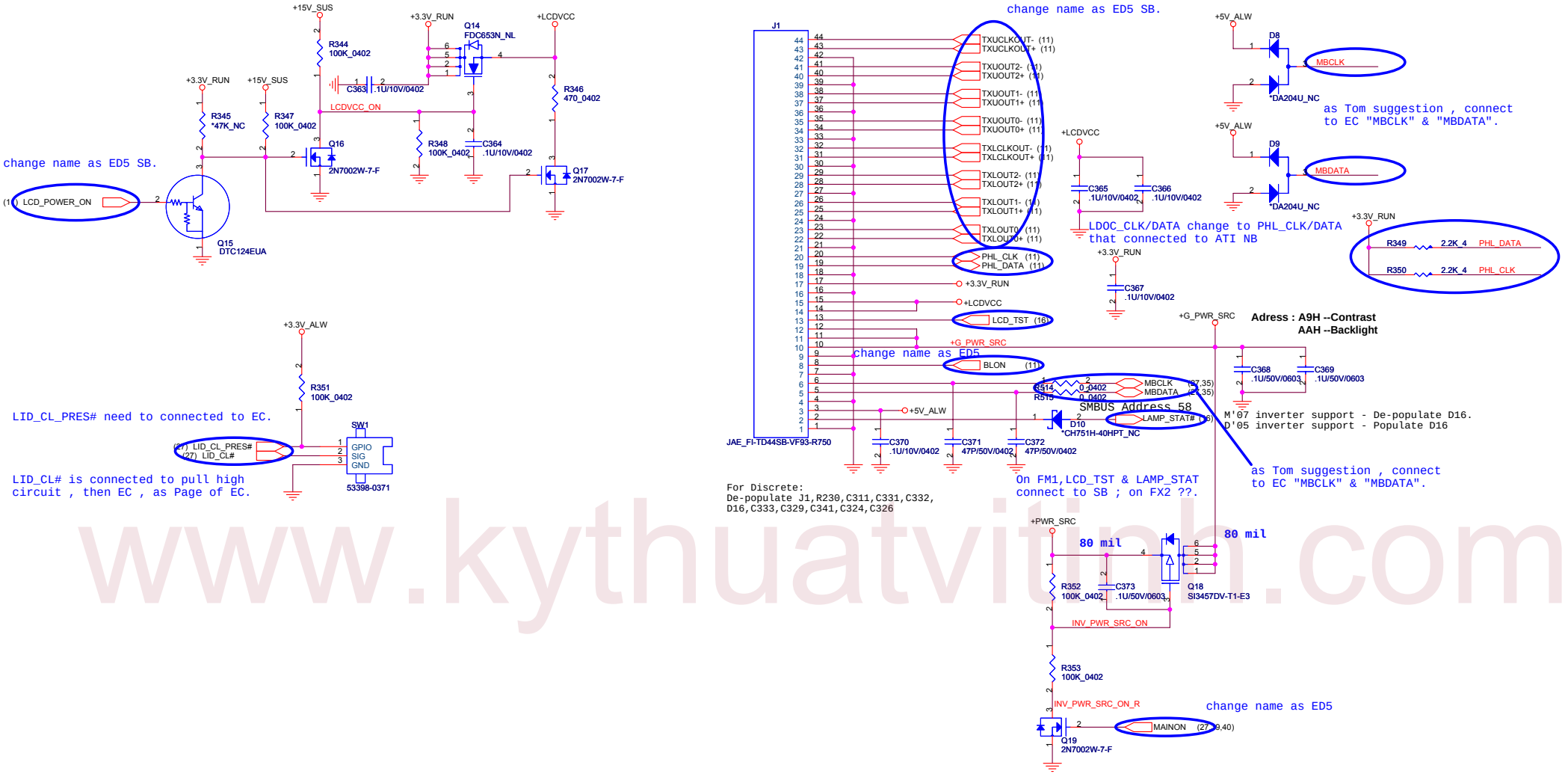
SB600 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

DEBUG STRAPS

	PDACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	Use Long Reset DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	boot fail time disabled DEFAULT
PULL LOW	USE SHORT RESET	Use Short Reset	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	boot fail time enabled
	SB460 Only	SB600 Only					SB600 Only

QUANTA COMPUTER

Title	SB600M STRAPS	
Size	Document Number FX2	Rev 1A
Date: Friday, May 05, 2006	Sheet 17 of 47	

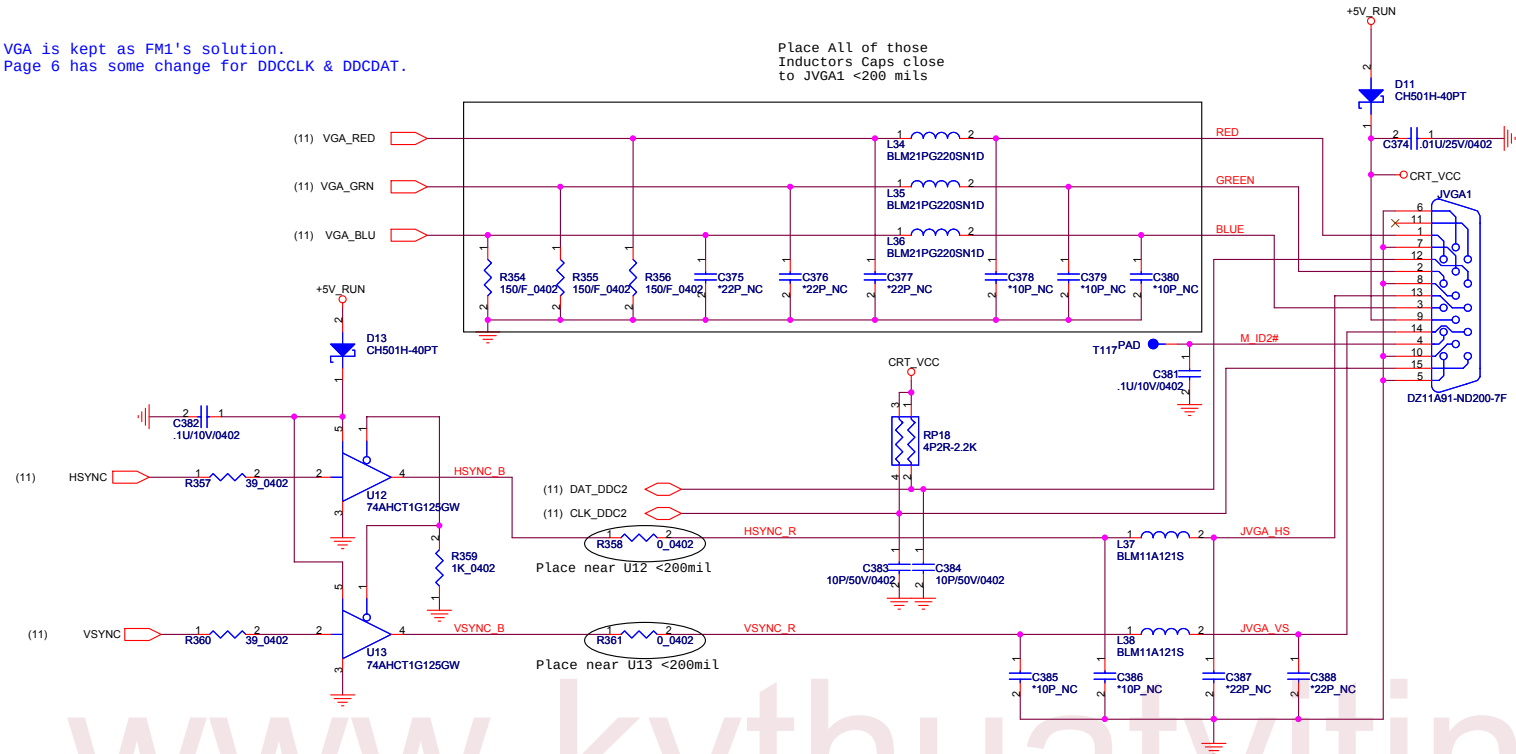


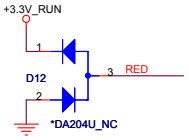
QUANTA COMPUTER

Title	LCD CONN	
Size	Document Number FX2	Rev 1A
Date: Friday, May 05, 2006	Sheet 18 of 47	

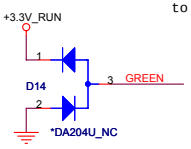
VGA is kept as FM1's solution.
Page 6 has some change for DDCCLK & DDCDAT.

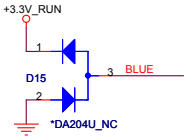
Place All of those
Inductors Caps close
to JVGA1 <200 mils



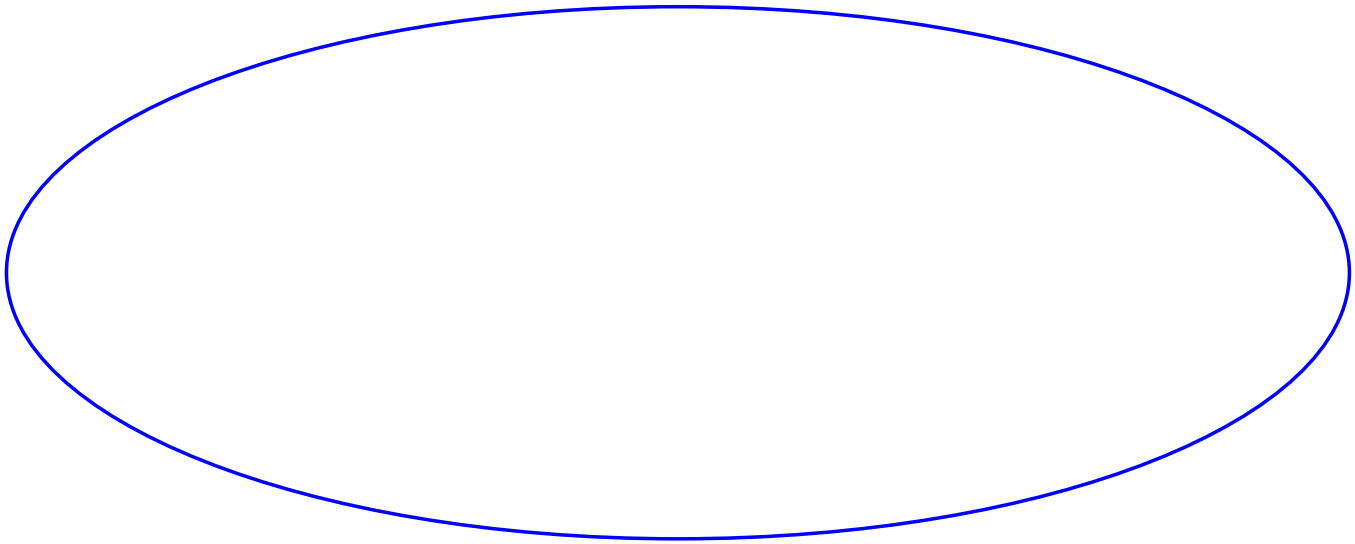


Place D4,D5,D6 close
to JVGA1 <200 mils





delete Svideo for defeature



QUANTA COMPUTER		
Title: CRT		
Size	Document Number: FX2	Rev: 1A
Date: Friday, May 05, 2006	Sheet 19 of 47	

change name for ED5
copy ED5 to FX2
Waiting to check

+3.3V_R5C832
C401 10U/10V/0805
C402 .01U/25V/0402
C403 .01U/25V/0402
C404 .01U/25V/0402
C405 .01U/25V/0402
C406 .01U/25V/0402
C407 10U/10V/0805
C408 .01U/25V/0402
C409 .1U/10V/0402
C410 .01U/25V/0402
Place the power caps close to the relation pins.
C413 .01U/25V/0402
C414 .01U/25V/0402
C415 .47U/10V/0603
C416 .47U/10V/0603
U15B
VCC_PCI1 10
VCC_PCI2 20
VCC_PCI3 27
VCC_PCI4 32
VCC_PCI5 41
VCC_PCI6 128
VCC_RIN 61
VCC_ROUT1 16
VCC_ROUT2 34
VCC_ROUT3 64
VCC_ROUT4 114
VCC_ROUT5 120
VCC_3V 67
VCC_MD 86
Place the power caps close to the relation pins.
C411 .01U/25V/0402
C412 10U/10V/0805
+3.3V_RUN
R371 0_0805
(14,17,33,42) AD[0..31]
PCI Bus
PowerOnReset for VccCore
Route GBRST# to GPIOG3 (pin 91) of the SIO companion chip ECE5011, and name the signal CBUS_GRST#. If CBUS_GRST# is controlled by the sysem, then C850 does not need to apply.
If R374 is populated, both C417 and R372 can be depop.
(27) CBUS_GRST#
R372 100K_0402
R374 *0_NC
C417 1U/10V/0603
GBRST# should be asserted only when system power supply is on.
AD31 125
AD30 126
AD29 127
AD28 1
AD27 2
AD26 3
AD25 5
AD24 6
AD23 9
AD22 11
AD21 12
AD20 14
AD19 15
AD18 17
AD17 18
AD16 19
AD15 36
AD14 37
AD13 38
AD12 39
AD11 40
AD10 42
AD9 43
AD8 44
AD7 46
AD6 47
AD5 48
AD4 49
AD3 50
AD2 51
AD1 52
AD0 53
PAR 33
C/BE3# 7
C/BE2# 21
C/BE1# 35
C/BE0# 45
IDSEL 8
PCI / OTHER
GND1 4
GND2 13
GND3 22
GND4 28
GND5 54
GND6 62
GND7 63
GND8 68
GND9 118
GND10 122
AGND1 99
AGND2 102
AGND3 103
AGND4 107
AGND5 111
+3.3V_R5C832
R373 10K_0402
Route to GPIOG6 (pin 94) on the SIO companion chip ECE5011, with the signal named CB_HWSPND#
HWSPND# 69
R375 *0_NC
CB_HWSPND# (27)
R517 10K_0402
pull down to disable MS & XD
MSEN 58
XDEN 55
UDIO5 57
UDIO3 65
UDIO4 59
UDIO2 56
UDIO1 60
UDIO0/SRIRQ# 72
SERIRQ (14,27,42)
R376 10K_0402
R377 100K_0402
Memory Stick disable
XD Card disable
Serial ROM disable
SD Card Enable
MMC Card Enable
Waiting to check LINK SB460 SERIRQ PIN PCLK_PCM
PCI Bus
R559 10K_0402
INTA# 115
INTB# 116
INTE# (14)
1394 Interrupt
Media card Interrupt
Waiting to check LINK SB460 PCI CLKS PIN PCLK_PCM
(14,33,42) PAR
(14,33,42) CBE3#
(14,33,42) CBE2#
(14,33,42) CBE1#
(14,33,42) CBE0#
AD17
R378 100_0402
(14) REQ2#
(14) GNT2#
(14,33,42) FRAME#
(14,33,42) IRDY#
(14,33,42) TRDY#
(14,33,42) DEVSEL#
(14,33,42) STOP#
(14,33,42) PERR#
(14,33,42) SERR#
REQ# 124
GNT# 123
FRAME# 23
IRDY# 24
TRDY# 25
DEVSEL# 26
STOP# 29
PERR# 30
SERR# 31
(14,33,42) PCIRST#
GBRST# 71
PCIRST# 119
(14) PCLK_PCM
PCICLK 121
as ED5 application
+3.3V_RUN
Q43 *DTC144EUA_NC
(15,24,33) PME#
R379 *0_NC
PME# 70
(14,27,33,42) CLKRUN#
CLKRUN# 117
CoreLogic CLOCKRUN#
The ICH schematics need to include a pull-up resistor to implement CLKRUN#, and the ICH schematics must have a pull-down, or constantly drive thesignal low, in order to disable CLKRUN#.
TEST 66
T118 PAD
R380 100K_0402
R5C832T_V00
PCLK_PCM
R381 *10_NC
C418 *10P_NC
Refer to DELL M07 schematic X06

QUANTA COMPUTER
Title: 5C832/PCI
Size: Document Number: FX2
Rev: 1A
Date: Friday, May 05, 2006
Sheet 20 of 47

deleted 1394 for defeature

3.AVCC_PHY3V, connection with +3.3V_R5C832 power
4.AVCC_PHY3V, Inductor Required between +3.3V_R5C832 and AVCC_PHY

80 mils

+3.3V_R5C832

+3.3V_RUN_PHY

C423 10U/10V/0805

C424 .1U/10V/0402

C419 .01U/25V/0402

C425 1000P/50V/0402

L43 BLM18PG181SN1D

modify

U15A

Place these caps as close to the U15 as possible.

AVCC_PHY1 98
AVCC_PHY2 106
AVCC_PHY3 110
AVCC_PHY4 112

TPBIAS0 113

94 XI
95 XO
96 FIL0
101 REXT
100 VREF

5.TPBN1 & TPBP1, Short to GND
if the 1394 Port Is Not Used

TPBN0 104
TPBP0 105

TPAN0 108
TPAP0 109

IEEE1394/SD

MDIO17 87
MDIO16 92
MDIO15 89
MDIO14 91

MDIO13 90 SD/XD/MS_DATA3 SD/XD/MS_DATA3 (22)
MDIO12 93 SD/XD/MS_DATA2 SD/XD/MS_DATA2 (22)
MDIO11 81 SD/XD/MS_DATA1 SD/XD/MS_DATA1 (22)
MDIO10 82 SD/XD/MS_DATA0 SD/XD/MS_DATA0 (22)

MDIO05 75
MDIO08 88 SD/XD/MS_CMD SD/XD/MS_CMD (22)
MDIO19 83
MDIO18 85
MDIO02 78

changed for SD/MMC/SDIO only

MDIO03 77 SD_WP#(XDR/B#) SD_WP#(XDR/B#) (22)
MDIO00 80 SD_CD# SD_CD# (22)

MDIO01 79

MDIO09 84 SD/XD/MS_CLK (22)

MDIO04 76 MC_PWR_CTRL_0 (22)
MDIO06 74 T119 PAD

97 RSV

MDIO07 73

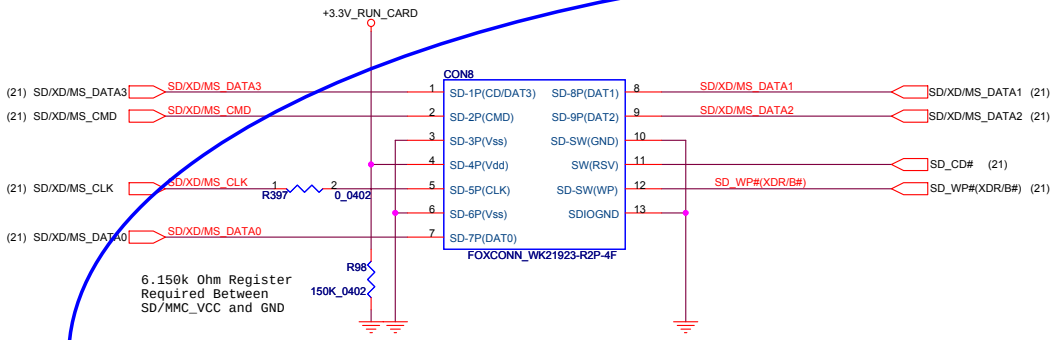
R5C832T_V00

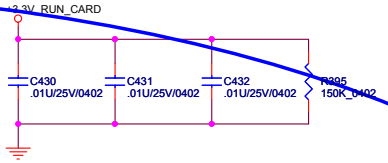
QUANTA COMPUTER

Title	CARD READER	
Size	Document Number FX2	Rev 1A
Date: Friday, May 05, 2006	Sheet 21 of 47	

DO NOT INSERT SD/MMC SIMULTANEOUSLY.

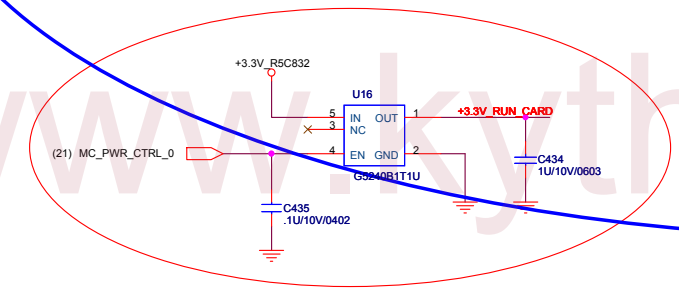
changed for SD/MMC/SDIO only





3 IN 1 CARD READER

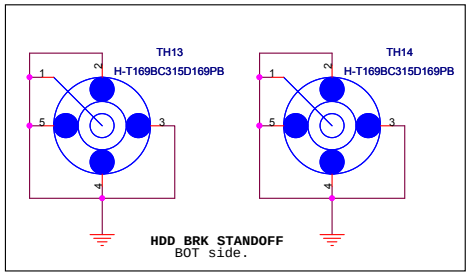
For SD/MS power



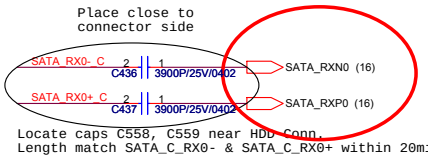
QUANTA COMPUTER

Title	CARD READER CONN	
Size	Document Number FX2	Rev 1A
Date: Friday, May 05, 2006	Sheet 22 of 47	

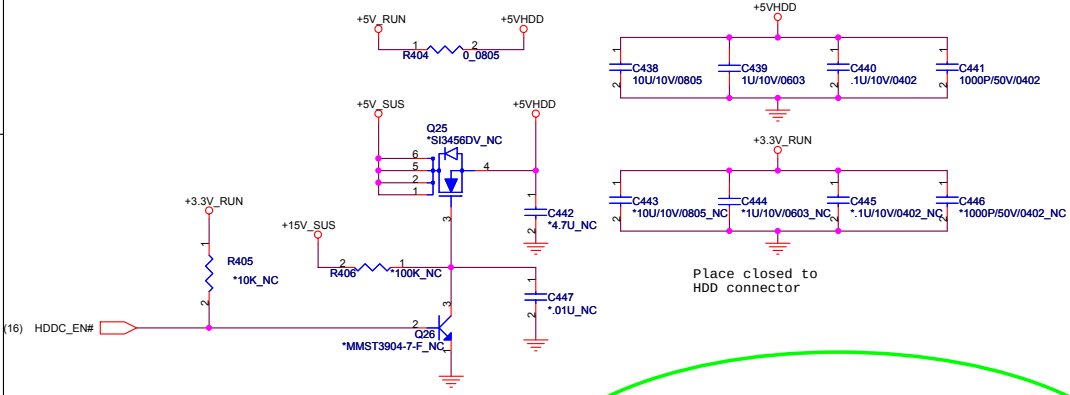
SATA HDD



Place close to connector side



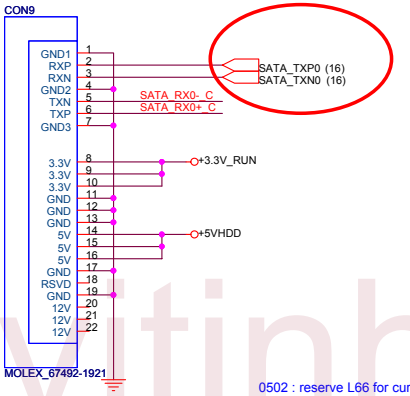
Locate caps C558, C559 near HDD Conn.
Length match SATA_C_RX0- & SATA_C_RX0+ within 20mils.



Place closed to HDD connector

SATA drive vendors will use only 5V supply from the system and will derive 3.3V on the drive. If drive power goals are not achieved, drive vendors will use both 5V and 3.3V supplies from the system. Initial power saving using 3.3V from system is less than 5%.

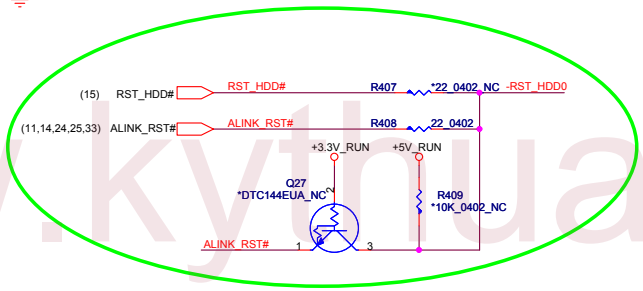
Power Estimate:
SATA drive power consumption estimate at MobileMark is 1.1W. An additional 150mW can be saved using Intel's IMST driver.



change name for ED5

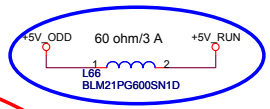
copy ED5 to FX2

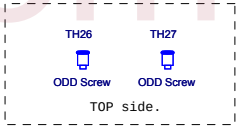
Waiting to check

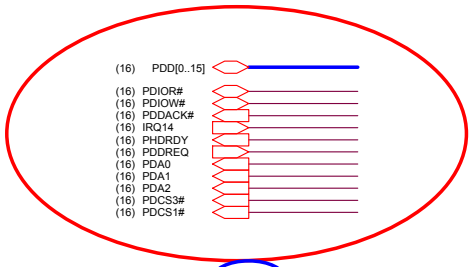


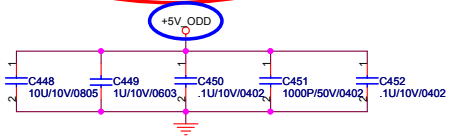
PATA ODD

0502 : reserve L66 for current measurement , can be removed and short directly after RTS ; and change +5V_RUN to +5V_ODD for ODD side power

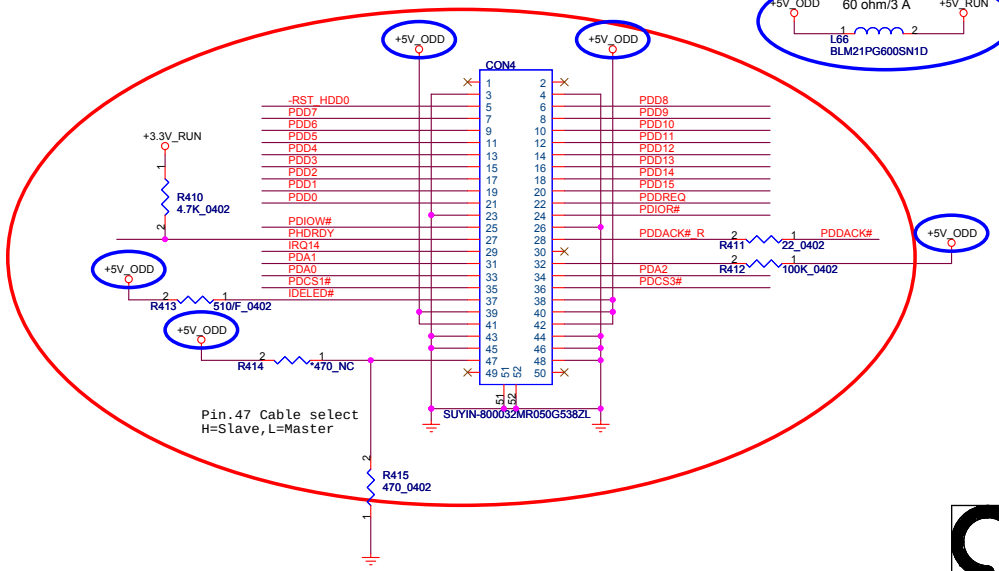








Place closed to MOD connector

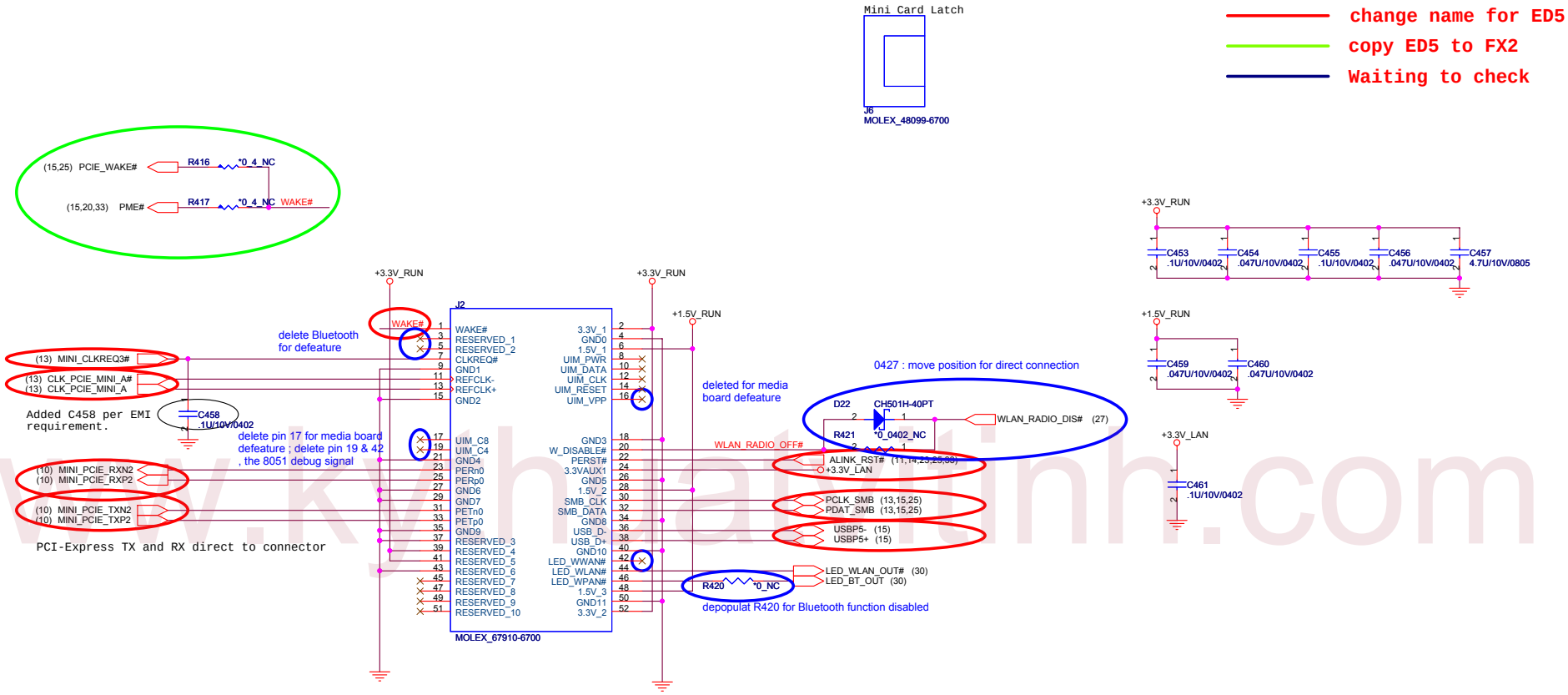


Pin.47 Cable select
H=Slave,L=Master

QUANTA COMPUTER

Title	SATA HDD & PATA ODD	
Size	Document Number FX2	Rev 1A
Date: Friday, May 05, 2006	Sheet 23 of 47	

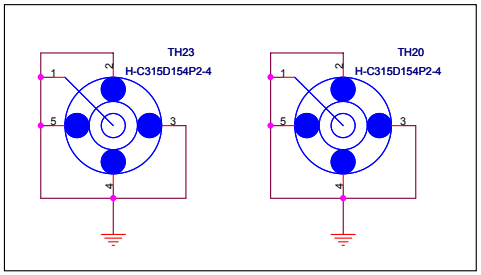
MINI CARD



QUANTA COMPUTER

Title	MINI Card	
Size	Document Number FX2	Rev 1A
Date: Friday, May 05, 2006	Sheet 24 of 47	

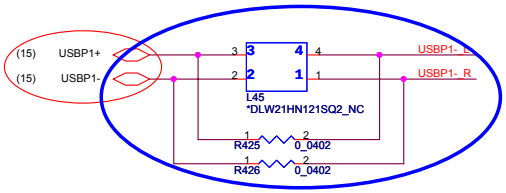
Express Card

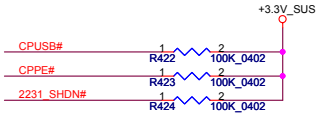


change name for ED5
copy ED5 to FX2
Waiting to check

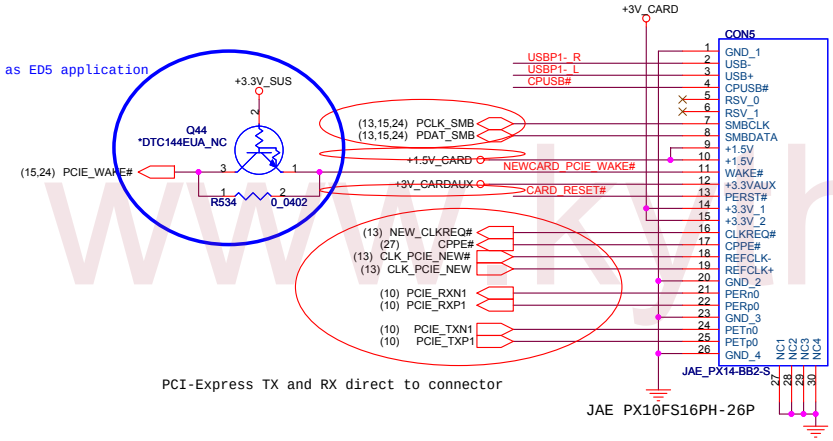
NEW CARD GUIDE POST
TOP side.

swap traces as "fx2_swap-0412"





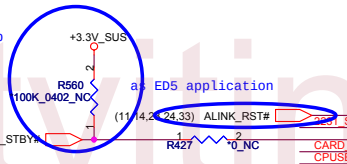
as ED5 application



PCI-Express TX and RX direct to connector

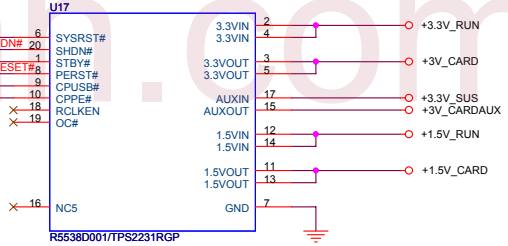
JAE PX10FS16PH-26P

reserve for pull up

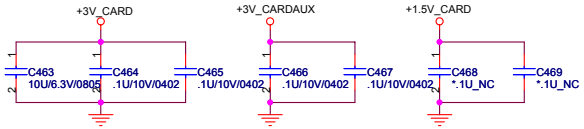


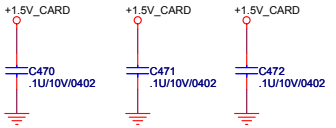
as ED5 application

+1.5V_CARD Max. 650mA, Average 500mA
+3V_CARD Max. 1300mA, Average 1000mA

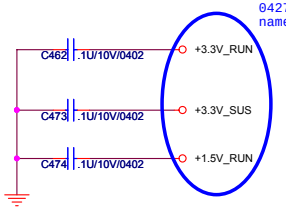


+1.5V_CARD Max. 650mA, Average 500mA
+3V_CARD Max. 1300mA, Average 1000mA





0427 : change from only net name to symbol "power point"



QUANTA COMPUTER

Title	Express Card	
Size	Document Number FX2	Rev 1A
Date: Friday, May 05, 2006	Sheet 25 of 47	

MDC INTERFACE

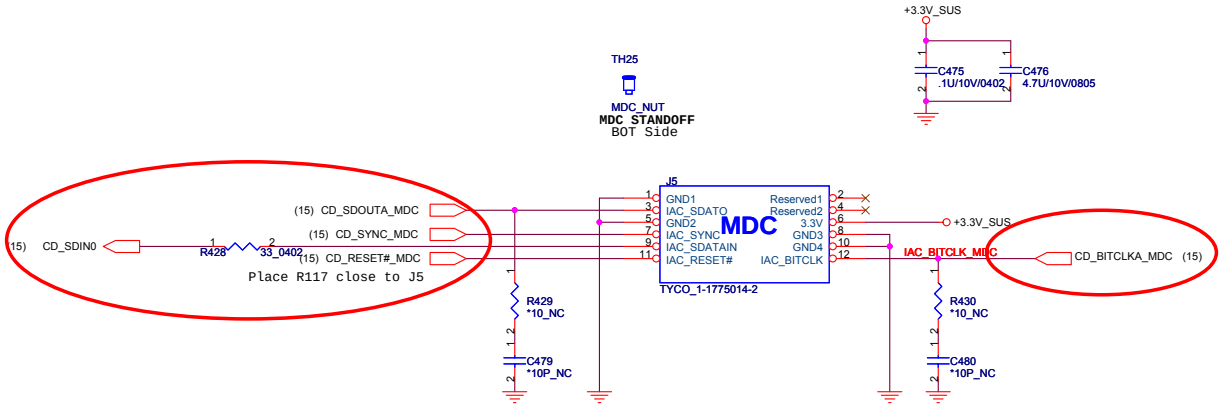
MDC Layout Notes

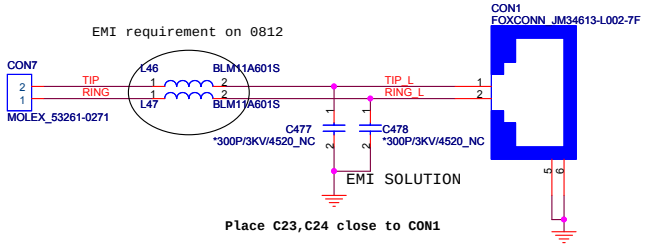
1. Tip and Ring trace width = 25 mils
2. Spacing between Tip and Ring = 25 mils
3. Tip and Ring connector pitch = 25 mils
4. Keep out area from Tip and Ring to other signals = 100 mils
5. Power and Ground minimum trace width to connector = 20 mils
6. Route Tip and Ring on one layer only (top or bottom)
7. Modem internal cable wire size = 26 AWG
(stranded or twisted pair wire)

change name for ED5

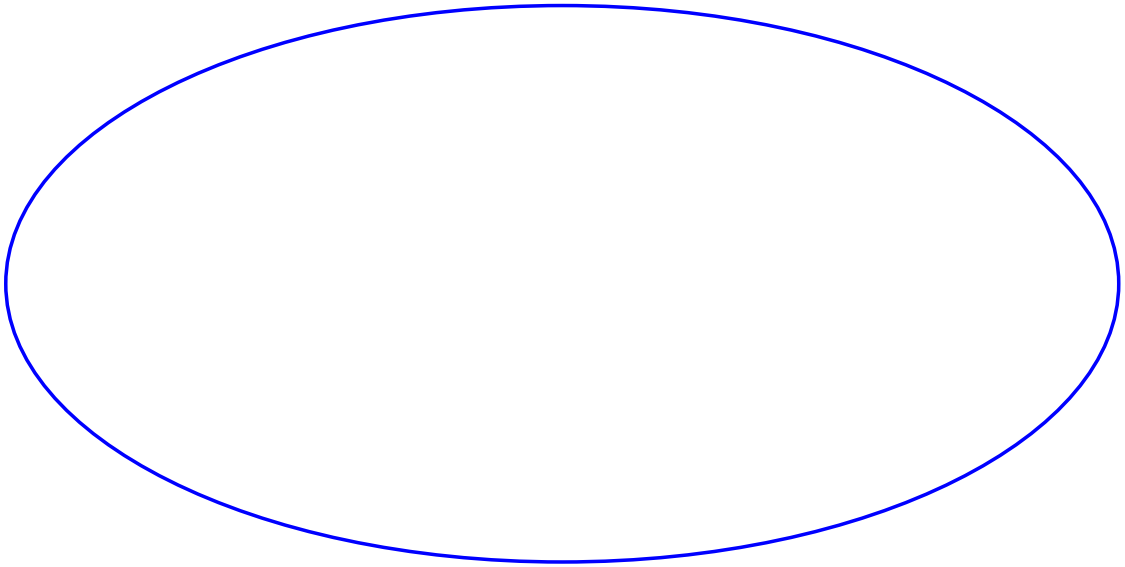
copy ED5 to FX2

Waiting to check





delete Bluetooth
for defeature



QUANTA COMPUTER

Title	MDC CONN	
Size	Document Number FX2	Rev 1A
Date: Friday, May 05, 2006	Sheet 26 of 47	

EC pin updated as "FX2 KBC GPIO define v14"

add R468 for +3.3_SRC & R516 connected to +3.3V_ALW as power concern about the leakage; create +3.3V_97551.

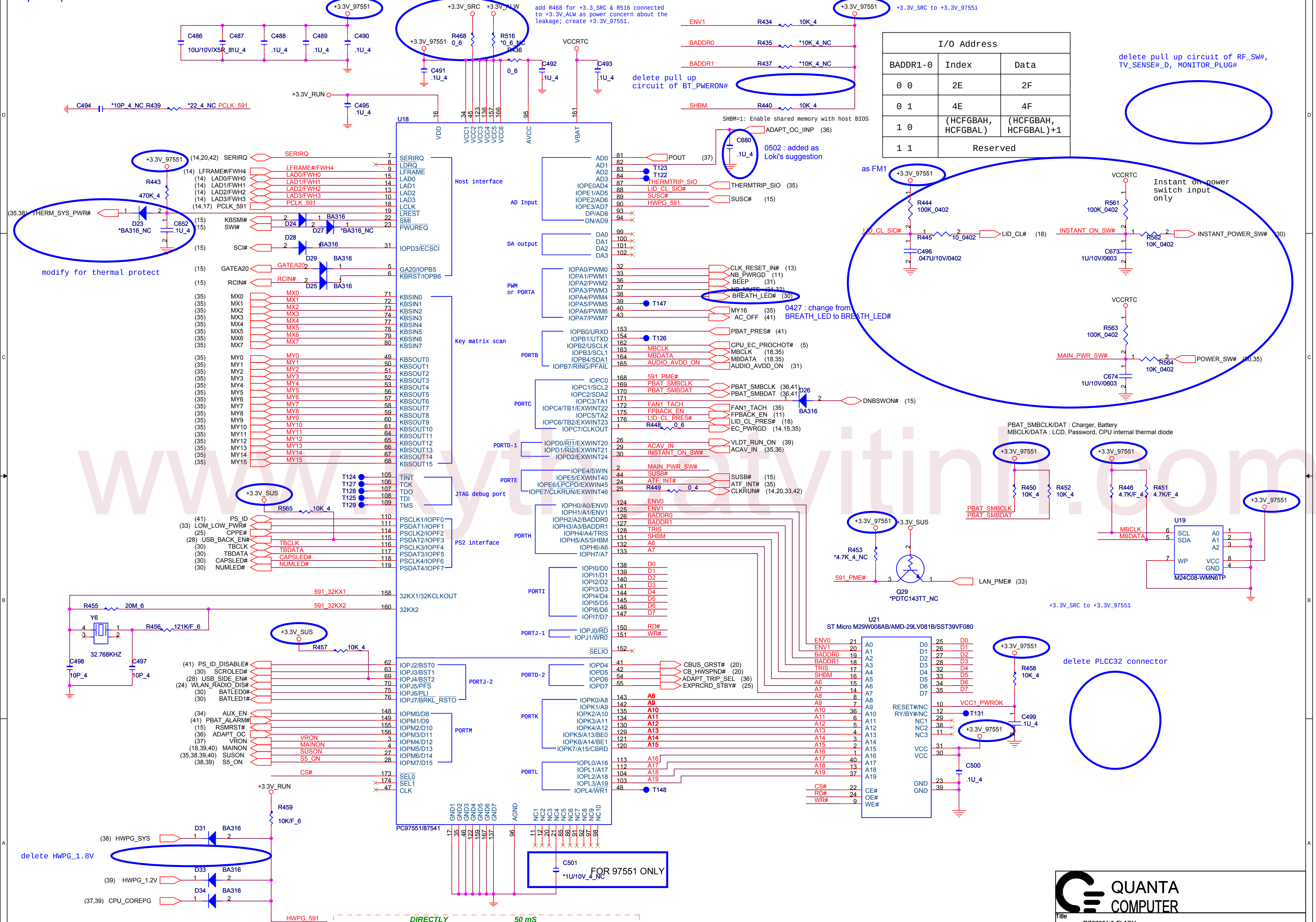
+3.3V_SRC to +3.3V_97551

delete pull up circuit of RF_SW#, TV_SENSE#_D, MONITOR_PLUG#

delete pull up circuit of BT_PWERON#

SHBM=1: Enable shared memory with host BIOS

I/O Address		
BADDR1-0	Index	Data
0 0	2E	2F
0 1	4E	4F
1 0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
1 1	Reserved	



EC & FALSH ROM

QUANTA COMPUTER

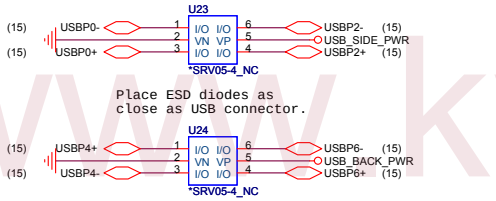
Title	PC97551 & FLASH	
Size	Document Number FX2	Rev 1A
Date:	Friday, May 05, 2006	Sheet 27 of 47

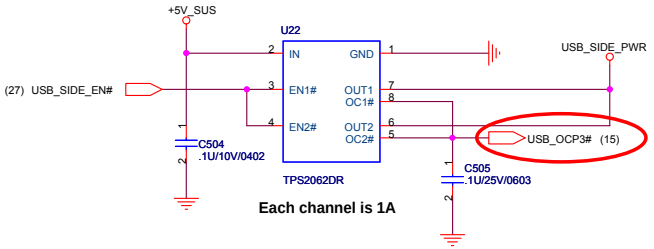
change name for ED5

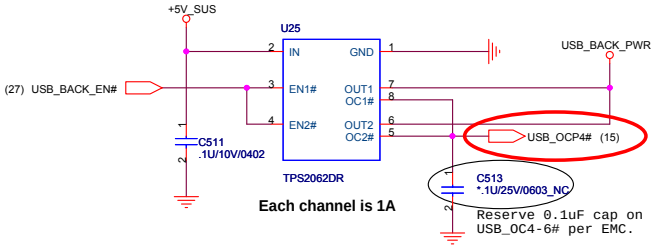
copy ED5 to FX2

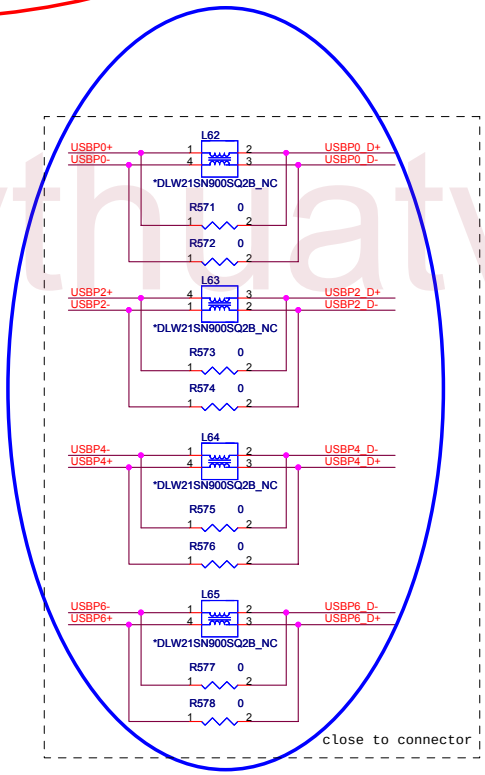
Waiting to check

8Mbit (1M Byte), SPI

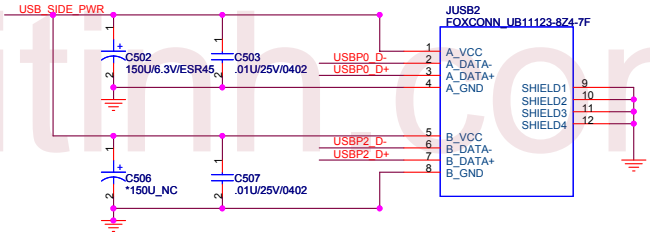


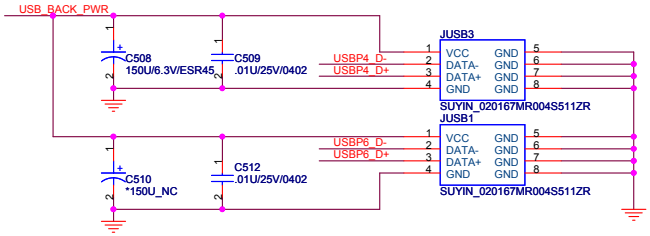






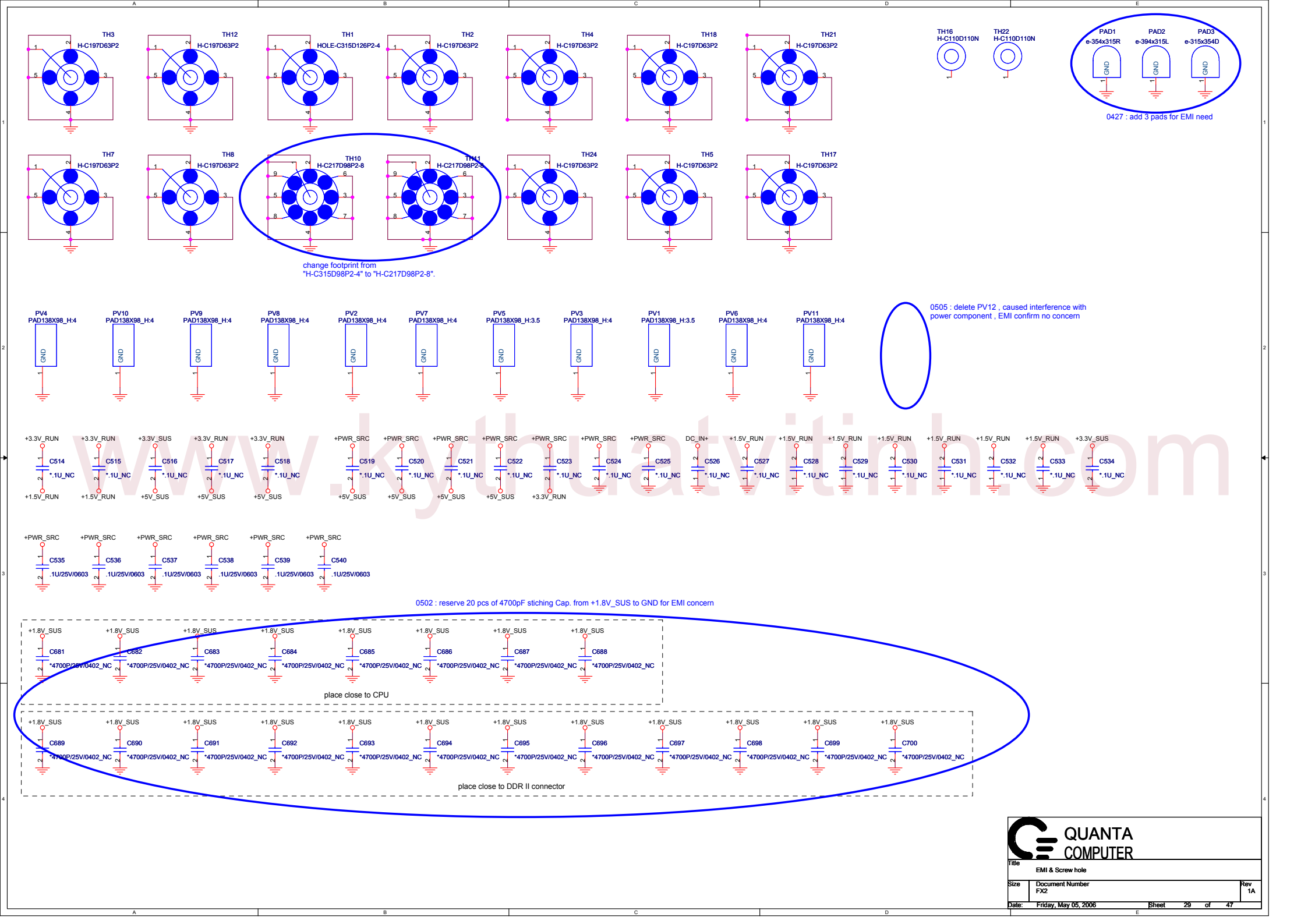
add for EMI suggestion ,
0502 : swap P0/P2 traces as "fx2-swap-0502"





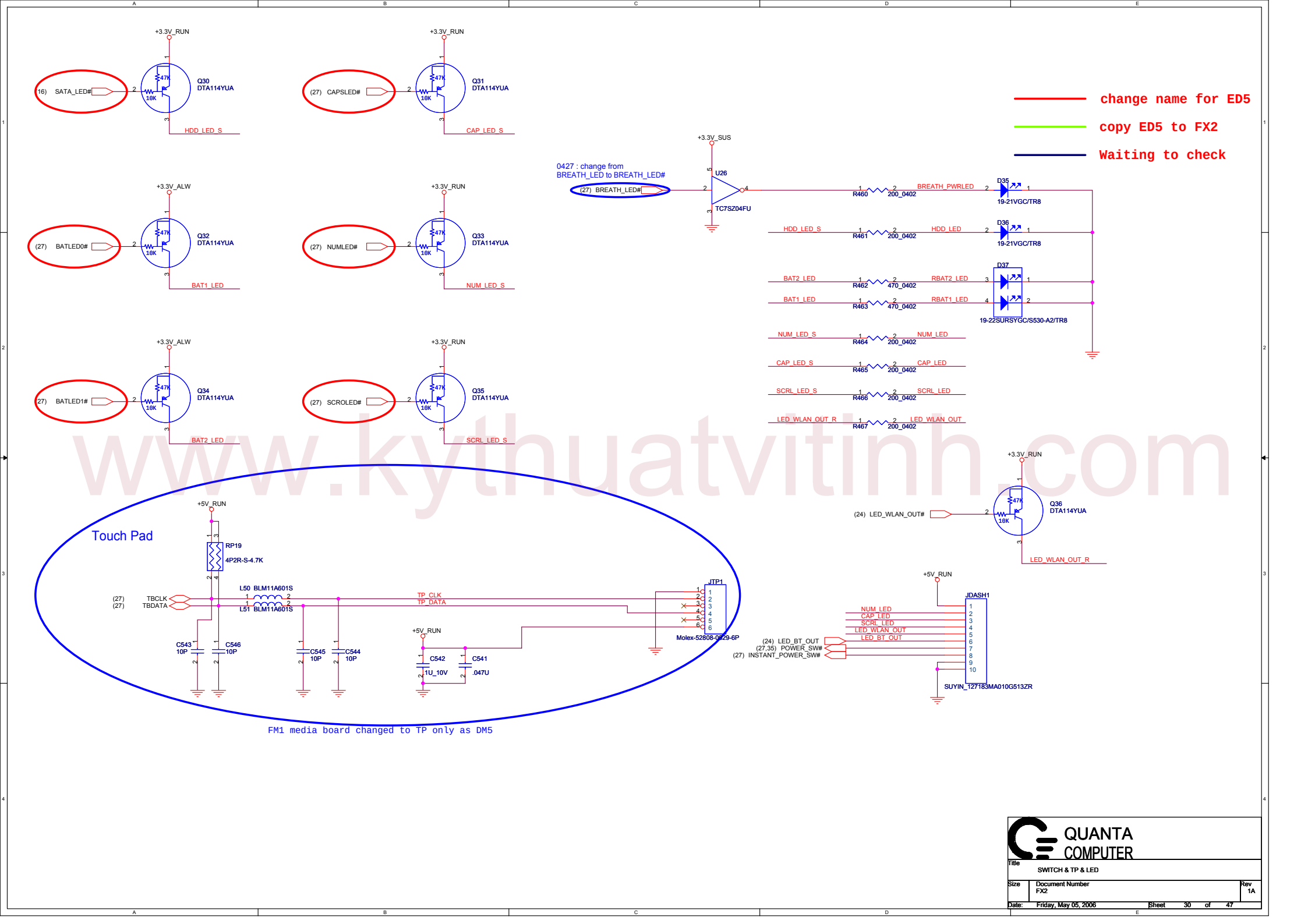
QUANTA COMPUTER

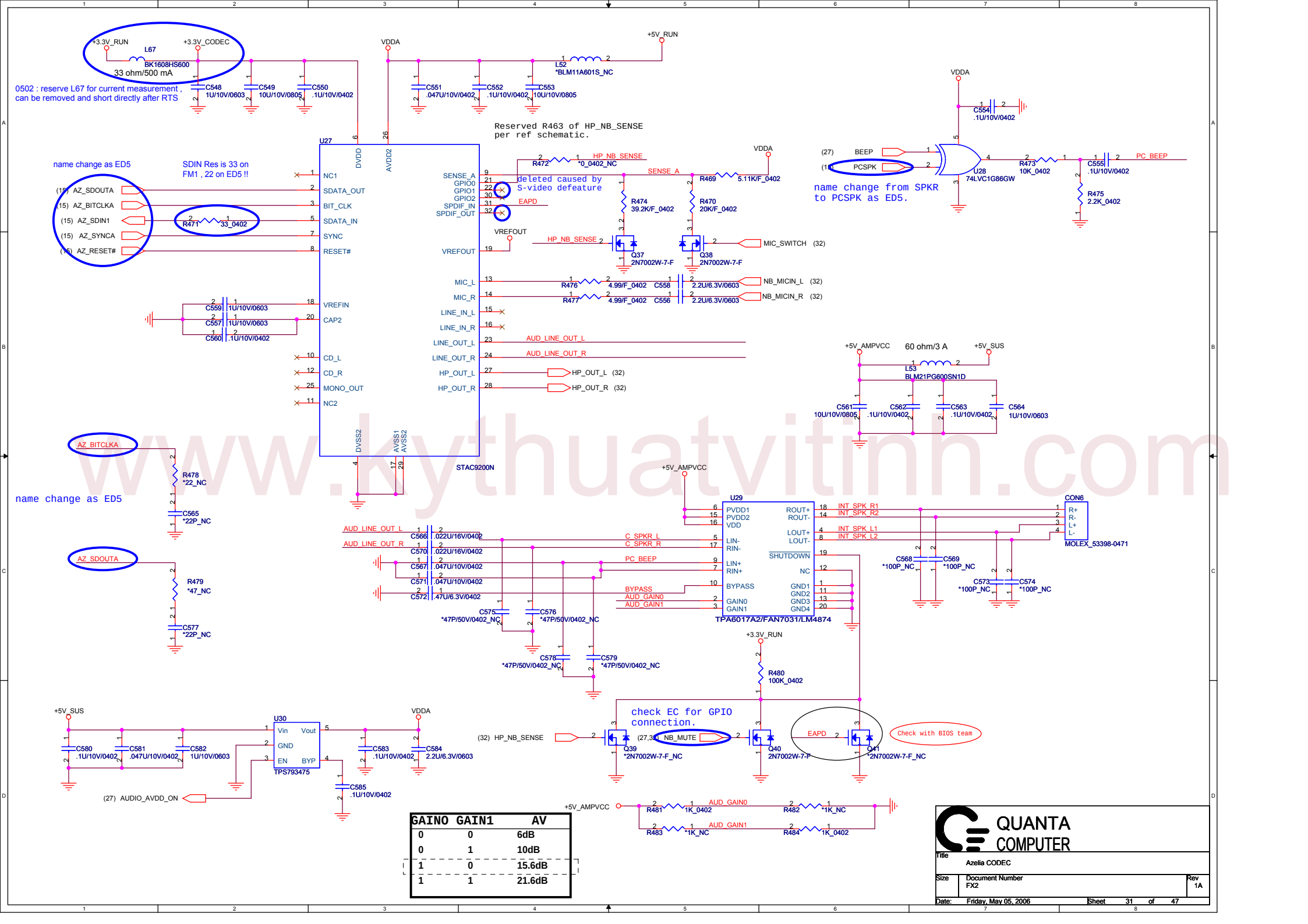
Title	USB	
Size	Document Number FX2	Rev 1A
Date: Friday, May 05, 2006	Sheet 28 of 47	



QUANTA COMPUTER

Title	EMI & Screw hole	
Size	Document Number FX2	Rev 1A
Date: Friday, May 05, 2006	Sheet 29 of 47	

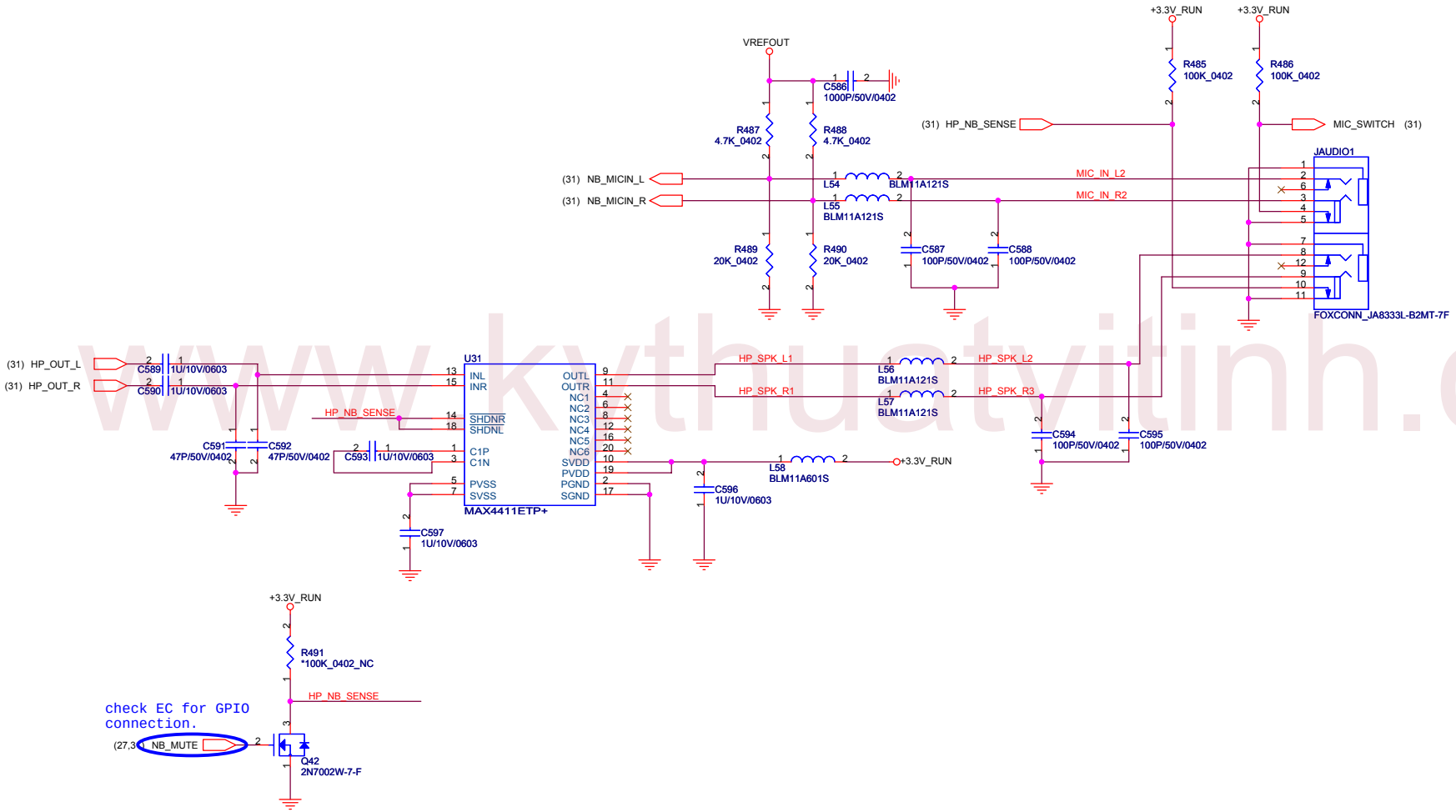




GAIN0	GAIN1	AV
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

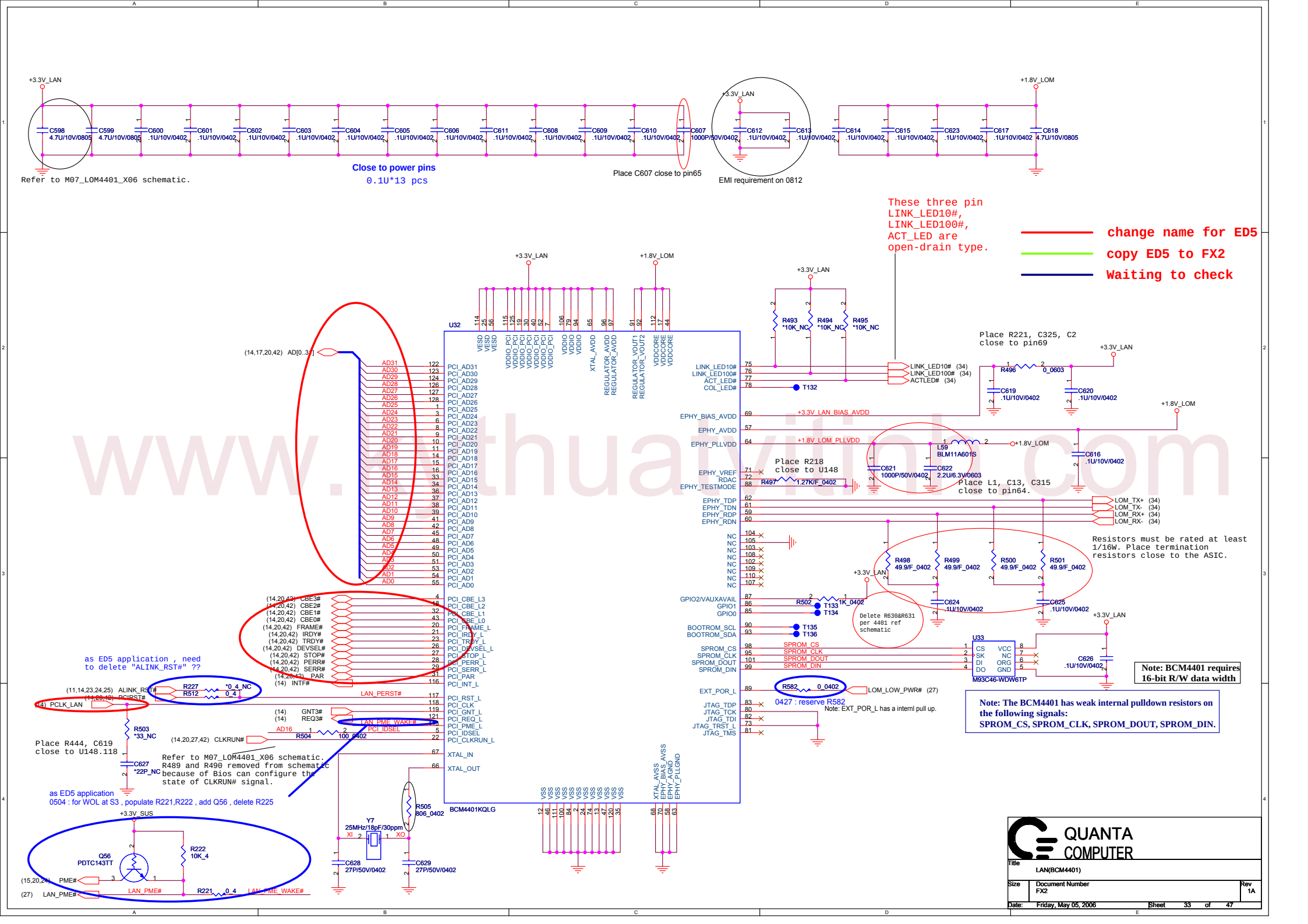
QUANTA COMPUTER

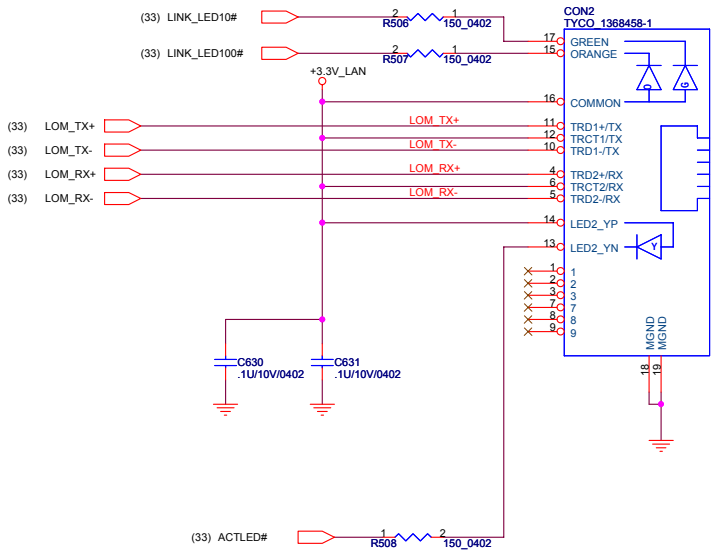
Title	Azelia CODEC	
Size	Document Number FX2	Rev 1A
Date: Friday, May 05, 2006	Sheet 31 of 47	



QUANTA COMPUTER

Title	AUDIO CONN	
Size	Document Number FX2	Rev 1A
Date: Friday, May 05, 2006	Sheet 32 of 47	


+3.3V_LAN
C598 4.7U/10V/0805
C599 4.7U/10V/0805
C600 .1U/10V/0402
C601 .1U/10V/0402
C602 .1U/10V/0402
C603 .1U/10V/0402
C604 .1U/10V/0402
C605 .1U/10V/0402
C606 .1U/10V/0402
C611 .1U/10V/0402
C608 .1U/10V/0402
C609 .1U/10V/0402
C610 .1U/10V/0402
C607 1000P/50V/0402
Refer to M07_LOM4401_X06 schematic.
Close to power pins
0.1U*13 pcs
Place C607 close to pin65
C612 .1U/10V/0402
C613 .1U/10V/0402
EMI requirement on 0812
+1.8V_LOM
C614 .1U/10V/0402
C615 .1U/10V/0402
C623 .1U/10V/0402
C617 .1U/10V/0402
C618 4.7U/10V/0805
These three pin LINK_LED10#, LINK_LED100#, ACT_LED are open-drain type.
change name for ED5
copy ED5 to FX2
Waiting to check
U32
BCM4401KQLG
R493 *10K_NC
R494 *10K_NC
R495 *10K_NC
Place R221, C325, C2 close to pin69
R496 0_0603
C619 .1U/10V/0402
C620 .1U/10V/0402
Place R218 close to U148
R497 1.27K/F_0402
C621 1000P/50V/0402
C622 2.2U/6.3V/0603
L59 BLM11A601S
C616 .1U/10V/0402
Place L1, C13, C315 close to pin64.
Resistors must be rated at least 1/16W. Place termination resistors close to the ASIC.
R498 49.9/F_0402
R499 49.9/F_0402
R500 49.9/F_0402
R501 49.9/F_0402
C624 .1U/10V/0402
C625 .1U/10V/0402
R502 1K_0402
Delete R630&R631 per 4401 ref schematic
U33
M93C46-WDW6TP
C626 .1U/10V/0402
Note: BCM4401 requires 16-bit R/W data width
Note: The BCM4401 has weak internal pulldown resistors on the following signals:
SPROM_CS, SPROM_CLK, SPROM_DOUT, SPROM_DIN.
R582 0_0402
0427 : reserve R582
Note: EXT_POR_L has a internl pull up.
as ED5 application , need to delete "ALINK_RST#" ??
R227 *0_4_NC
R512 0_4
R503 *33_NC
C627 *22P_NC
Place R444, C619 close to U148.118
Refer to M07_LOM4401_X06 schematic. R489 and R490 removed from schematic because of Bios can configure the state of CLKRUN# signal.
R504 100_0402
as ED5 application
0504 : for WOL at S3 , populate R221,R222 , add Q56 , delete R225
+3.3V_SUS
Q56 PDTC143TT
R222 10K_4
R221 0_4
LAN_PME#
LAN_PME_WAKE#
Y7 25MHz/18pF/30ppm
C628 27P/50V/0402
C629 27P/50V/0402
R505 806_0402
Title LAN(BCM4401)
Size Document Number FX2
Rev 1A
Date: Friday, May 05, 2006
Sheet 33 of 47

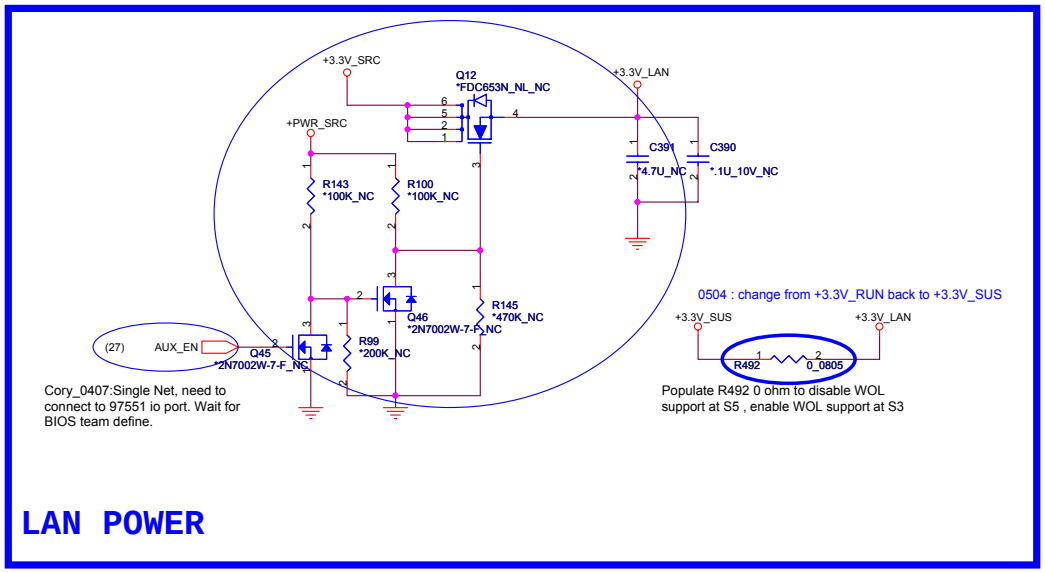


change name for ED5

copy ED5 to FX2

Waiting to check

copy DM5 to FX2



QUANTA COMPUTER

Title	LAN JACK	
Size	Document Number FX2	Rev 1A
Date: Friday, May 05, 2006	Sheet 34 of 47	

add Thermal IC as FM1

H_THERMDA&h_THERMDC
trace routing = W:10/S:10

(5) CPU_TEST4_THERMDA
(5) CPU_TEST5_THERMDC

Place C653 close to U36

C653 2200P/50V/0402

U36 EMC4000

+3.3V_SUS
R536 7.5K/F_0402
(18,27) MBDATA
(18,27) MBCLK
SMDATA
SMBCLK
LDO_SHDN#_ADDR
DP2
DN2
+3V_SUS
VSUS_PWRGD
+RTC_PWR3V
+3V_PWROK#
POWER_SW#
THERMTRIP1#
THERMTRIP2#
THERMTRIP3#
VSET
HW_LOCK#
VSS
FAN_DAC
FAN_OUT
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5

ATF_INT#
VCP1
VCP2
LDO_POK
DN1
DP1
THERMTRIP_SIO
ACAvail_Clr
SYS_SHDN#
VDD_5V
LDO_OUT
LDO_OUT
LDO_IN
LDO_IN
DP3
DN3
LDO_SET

+3.3V_SUS
R552 10K_0402
ATF_INT# (27)

delete single net "VCP1" & "VCP2"

R55310K_0402
+3.3V_RUN

+3.3V_SUS
R537 49.9/F_0402
+3VSUS_THRM
C655 .1U/10V/0402
VCCRTC
C658 .1U/10V/0402
SUSPWROK
R539 1K_0402
EC_PWRGD#
R540 1K_0402
(27,30) POWER_SW#
THERMTRIP1#

Place Q50 at bottom of CPU

REM_DIODE1_N & REM_DIODE1_P
trace routing = W:10/S:10

REM_DIODE1_N
REM_DIODE1_P
Place C656 close to the pins as possible.
C656 2200P/50/0402
Q50 MMST3904-7-F
C657 *2200P_NC
Place C657 close to the Q50

R541 10K_0402
+3.3V_ALW
THERMTRIP_SIO (27)
ACAV_IN (27,36)
THERM_SYS_PWR# (27,38)
R555 *10K_0402_NC
VCCRTC
+5V_RUN
+2.5V_RUN

+3.3V_SUS
R554 10K_0402
C663 .1U/10V/0402
R542 147K/F_0402
R543 41.2K_0402
C664 2200P/50V/0402
VSET
HW_LOCK#
R544 1K_0402
FAN1_VOUT

+3.3V_RUN
R535 10K_0402
FAN1_TACH (27)
R538 0_0402
FAN1
J3
FAN1_VOUT
FAN1_TACH_FB
VCC
SIG
GND
MOLEX_53398-0371
D39 *CH751H-40HPT_NC
C654 22U/10V/1206

+5V_RUN
C659 10U/10V/0805
C660 .1U/10V/0402
+2.5V_RUN
C661 10U/10V/0805
C662 .1U/10V/0402
Place C659~C662, C665~C667, close to U36

+3.3V_RUN_IN
C665 1U/10V/0603
C666 .1U/10V/0402
C667 *10U_NC

+3.3V_RUN_IN
R545 0_1210
+3.3V_RUN
REM_DIODE3_N & REM_DIODE3_P trace routing = W:10/S:10
REM_DIODE3_P
REM_DIODE3_N
LDO_SET
C668 2200P/50V/0402
Q51 MMST3904-7-F
C669 *2200P_NC
Place C669 close to Q51
Place C668 close to U36
Place Q51 Near the SO-DIMM.

+2.5V_RUN
R548 *31.5K_NC
LDO_SET
R550 1K_0603
Voltage margining circuit for LDO output.
For Vmargin, stuff R548 and R550=30K.
R550=1K for production

Notes:
Vset=(Tp-70)/21
3.3*(R543/R542+R543)=(Tp-70)/21
Where Tp=70 to 101 degree C
Set trip point=85 degree C
Vset = (85-75)/16= 0.625 V
Guardian II temp-tolerance= +/-3 degree C

+3.3V_SUS
R546 100K_0402
EC_PWRGD#
(14,15,27) EC_PWRGD
Q52 2N7002W-7-F

VLDT_RUN
R549 2.2K_0402
+3.3V_SUS
R547 8.2K_0402
THERMTRIP1#
Q53 MMST3904-7-F
C670 .1U/10V/0402
(5) H_THERMTRIP#
C670 needs to be placed near Guardian IC.

as FM1 keyboard matrix & "e0788.1104a_swap-0422"

JKB1
HRS_FH28D-50(25)SB-1SH(86)
(27) MY9 MY10 MY8 MY13 MY12 MY14 MY15 MY11 MY0 MY2 MY1 MY3 MY7 MY5 MY6 MY4 MY16 MX7 MX4 MX6 MX2 MX5 MX3 MX1 MX0

+3.3V_SUS
RP20 10KX8 MX0 MX1 MX3 MX5 MX7 MX4 MX6 MX2
RP21 10KX8 MY16 MY4 MY6 MY5 MY2 MY1 MY3 MY7
RP22 10KX8 MY0 MY11 MY15 MY14 MY10 MY8 MY13 MY12

CA1 *220PX4_NC MX0 MX1 MX3 MX5 MX7 MX4 MX6 MX2
CA2 *220PX4_NC
CA3 *220PX4_NC MY16 MY4 MY6 MY5 MY7 MY1 MY2 MY3
CA4 *220PX4_NC
CA5 *220PX4_NC MY0 MY11 MY15 MY14 MY10 MY8 MY13 MY12
CA6 *220PX4_NC

+3.3V_SUS
R513 10K_0402
MY9
C638 *220P/50V/0402_NC

wait to discuss !!

(27,38,39,40) SUSON
+1.8V_SUS
+3.3V_ALW
+3.3V_SUS
+3.3V_SUS
R557 10K_0402
R556 100K_0402
U38 TC7SZ04FU
C671 *.047U_NC
U39 TC7SZ08FU
SUSPWROK
Q54 3904
C672 1U/50V/0603

0427 : change Q54 from 2N7002W-7-F to 3904 ; C672 from .1U/10V/0402 to .1U/50V/0603 as voltage level & timing concern

KBC

QUANTA COMPUTER

Title	KB & THERMAL & FAN	
Size	Document Number FX2	Rev 1A
Date: Friday, May 05, 2006	Sheet 35 of 47	

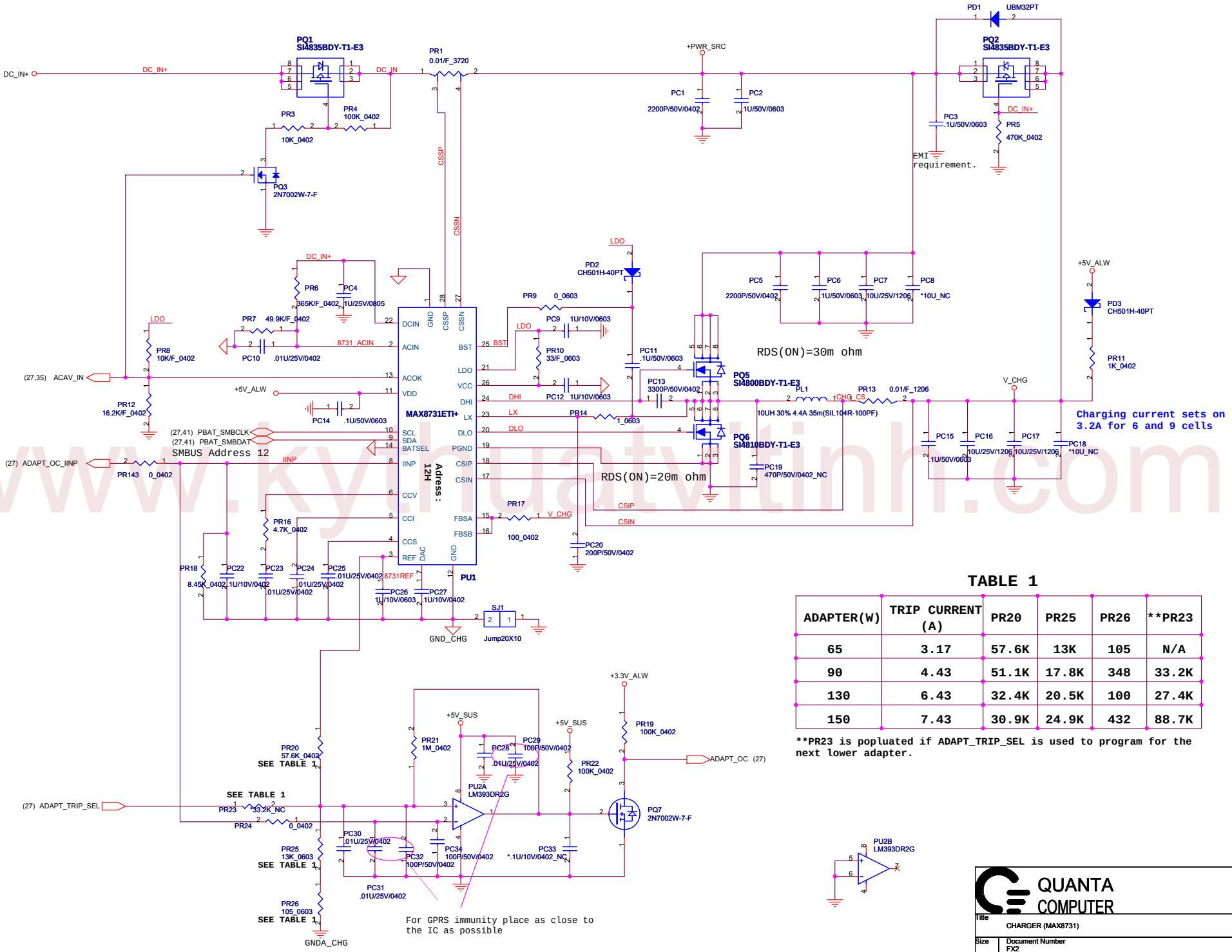


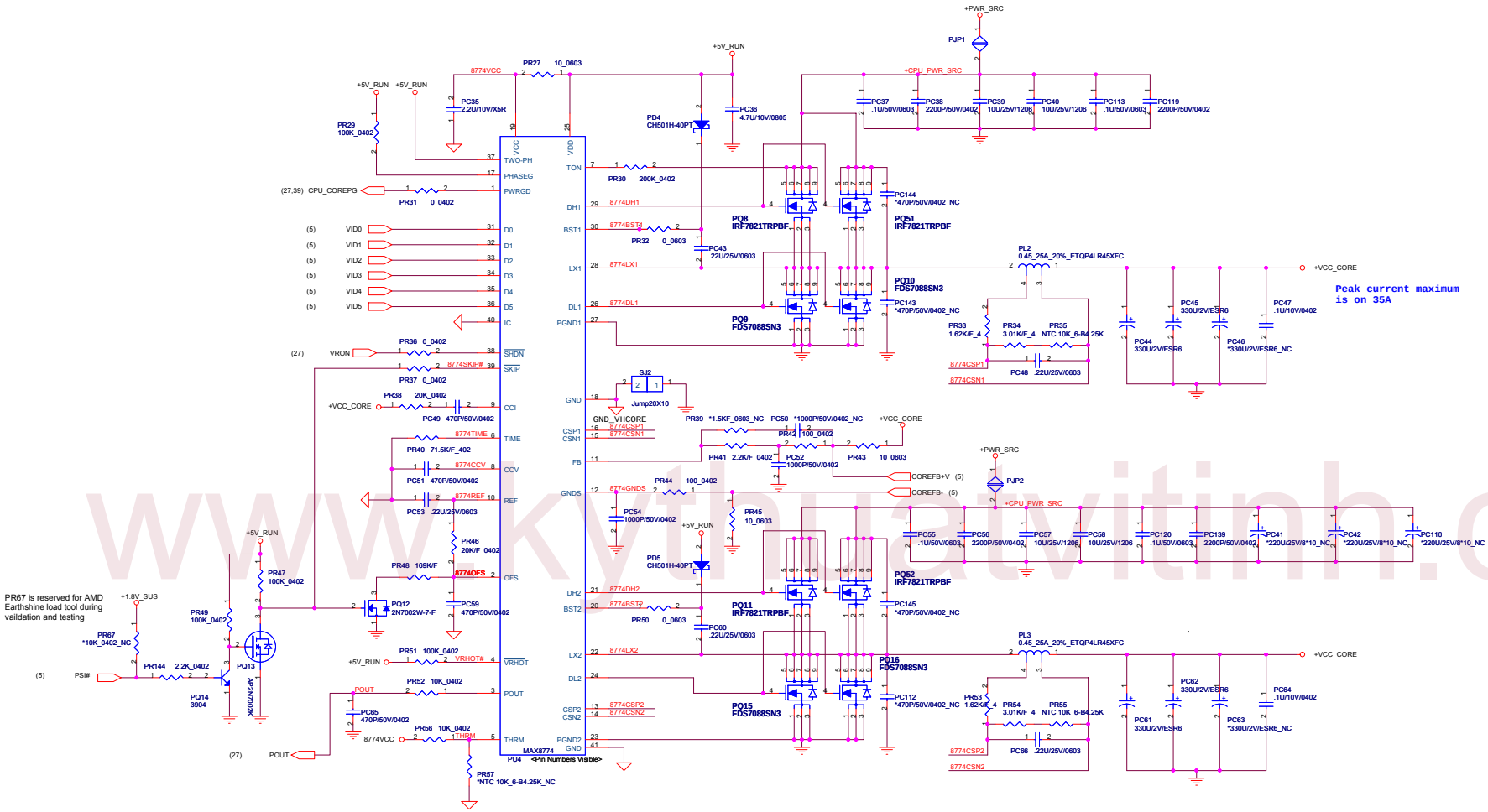
TABLE 1

ADAPTER(W)	TRIP CURRENT (A)	PR20	PR25	PR26	**PR23
65	3.17	57.6K	13K	105	N/A
90	4.43	51.1K	17.8K	348	33.2K
130	6.43	32.4K	20.5K	100	27.4K
150	7.43	30.9K	24.9K	432	88.7K

**PR23 is popluated if ADAPT_TRIP_SEL is used to program for the next lower adapter.

QUANTA COMPUTER

Title	CHARGER (MAX8731)	
Size	Document Number FX2	Rev 1A
Date: 2005/4/21	Sheet 36 of 47	

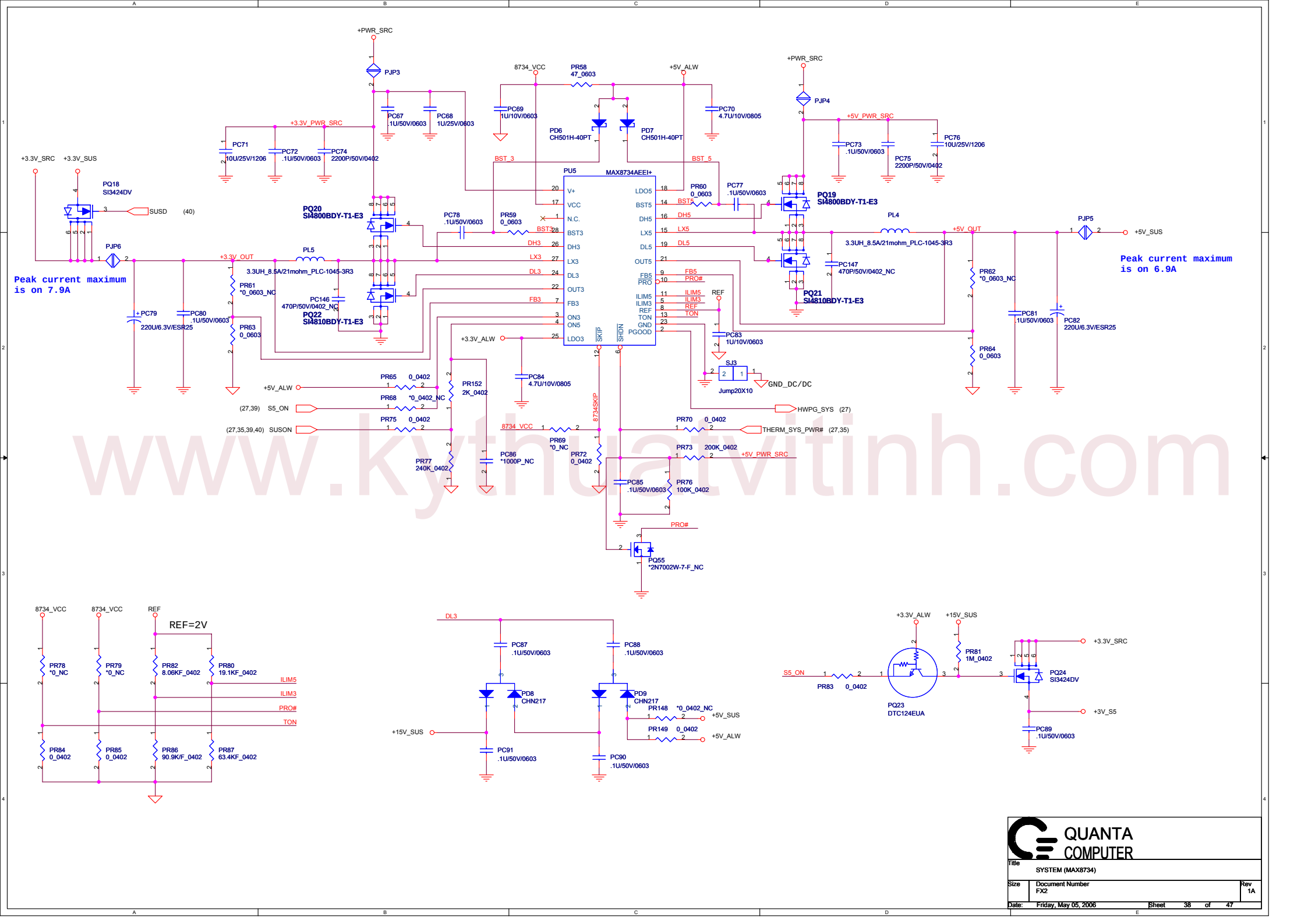


D5	D4	D3	D2	D1	D0	Output
0	0	0	0	0	0	1.5500V
0	0	0	0	0	1	1.5250V
0	0	0	0	1	0	1.5000V
0	0	0	0	1	1	1.4750V
0	0	0	1	0	0	1.4500V
0	0	0	1	0	1	1.4250V
0	0	0	1	1	0	1.4000V
0	0	0	1	1	1	1.3750V
0	0	1	0	0	0	1.3500V
0	0	1	0	0	1	1.3250V
0	0	1	0	1	0	1.3000V
0	0	1	0	1	1	1.2750V
0	0	1	1	0	0	1.2500V
0	0	1	1	0	1	1.2250V
0	0	1	1	1	0	1.2000V
0	0	1	1	1	1	1.1750V
0	1	0	0	0	0	1.1500V
0	1	0	0	0	1	1.1250V
0	1	0	0	1	0	1.1000V
0	1	0	0	1	1	1.0750V
0	1	0	1	0	0	1.0500V
0	1	0	1	0	1	1.0250V
0	1	0	1	1	0	1.0000V
0	1	0	1	1	1	0.9750V
0	1	1	0	0	0	0.9500V
0	1	1	0	0	1	0.9250V
0	1	1	0	1	0	0.9000V
0	1	1	0	1	1	0.8750V
0	1	1	1	0	0	0.8500V
0	1	1	1	0	1	0.8250V
0	1	1	1	1	0	0.8000V
0	1	1	1	1	1	0.7750V

D5	D4	D3	D2	D1	D0	Output
1	0	0	0	0	0	0.7625V
1	0	0	0	0	1	0.7500V
1	0	0	0	1	0	0.7375V
1	0	0	0	1	1	0.7250V
1	0	0	1	0	0	0.7125V
1	0	0	1	0	1	0.7000V
1	0	0	1	1	0	0.6875V
1	0	0	1	1	1	0.6750V
1	0	1	0	0	0	0.6625V
1	0	1	0	0	1	0.6500V
1	0	1	0	1	0	0.6375V
1	0	1	0	1	1	0.6250V
1	0	1	1	0	0	0.6125V
1	0	1	1	0	1	0.6000V
1	0	1	1	1	0	0.5875V
1	0	1	1	1	1	0.5750V
1	1	0	0	0	0	0.5625V
1	1	0	0	0	1	0.5500V
1	1	0	0	1	0	0.5375V
1	1	0	0	1	1	0.5250V
1	1	0	1	0	0	0.5125V
1	1	0	1	0	1	0.5000V
1	1	0	1	1	0	0.4875V
1	1	0	1	1	1	0.4750V
1	1	1	0	0	0	0.4625V
1	1	1	0	0	1	0.4500V
1	1	1	0	1	0	0.4375V
1	1	1	0	1	1	0.4250V
1	1	1	1	0	0	0.4125V
1	1	1	1	0	1	0.4000V
1	1	1	1	1	0	0.3875V
1	1	1	1	1	1	0.3750V

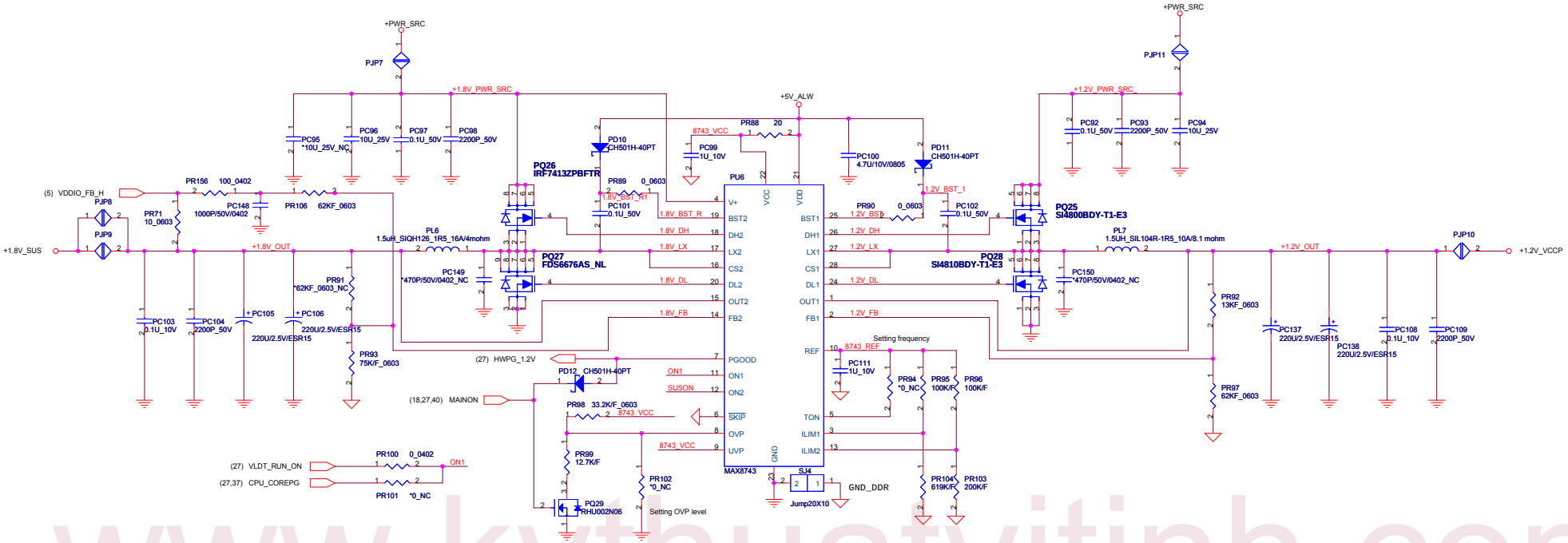
QUANTA COMPUTER

Title	VHCORE (MAX8774)	
Size	Document Number FX2	Rev 1A
Date: Friday, May 05, 2006	Sheet 37 of 47	

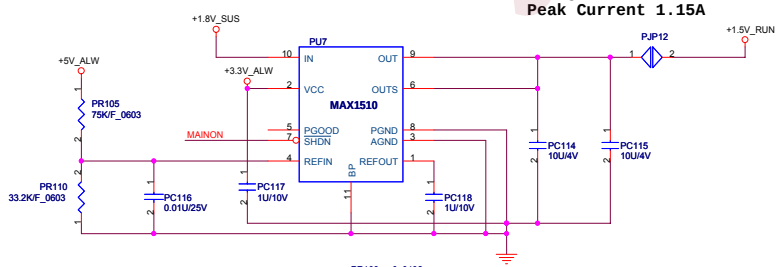


QUANTA COMPUTER

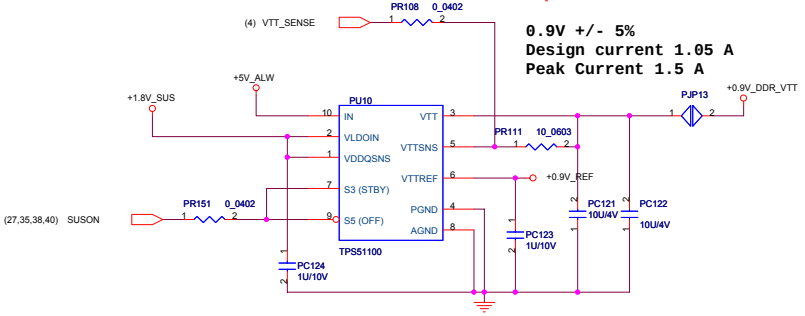
Title	SYSTEM (MAX8734)	
Size	Document Number FX2	Rev 1A
Date: Friday, May 05, 2006	Sheet 38 of 47	

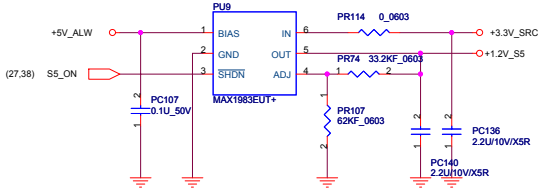


1.5 Volt +/- 5%
Design current 0.7A
Peak Current 1.15A



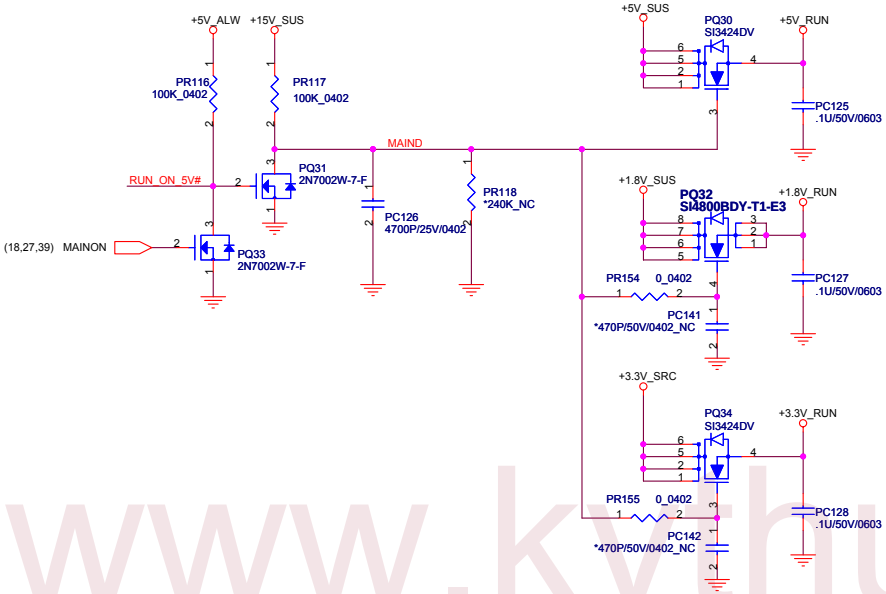
0.9V +/- 5%
Design current 1.05 A
Peak Current 1.5 A

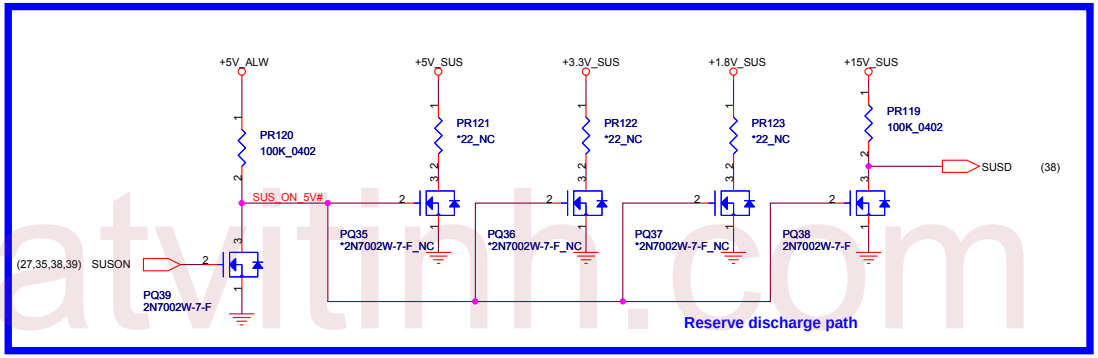


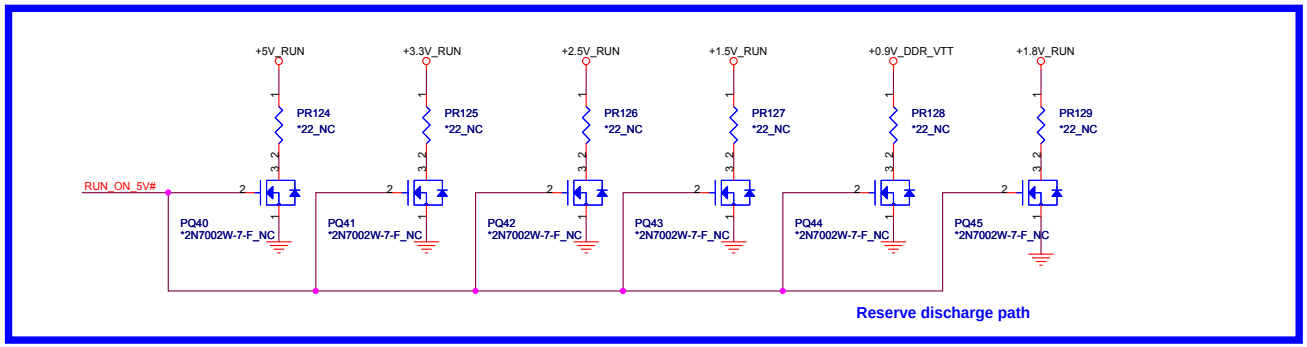


QUANTA COMPUTER

Title	VCCP	
Size	Document Number FX2	Rev 1A
Date: 2005/4/21	Sheet 39 of 47	

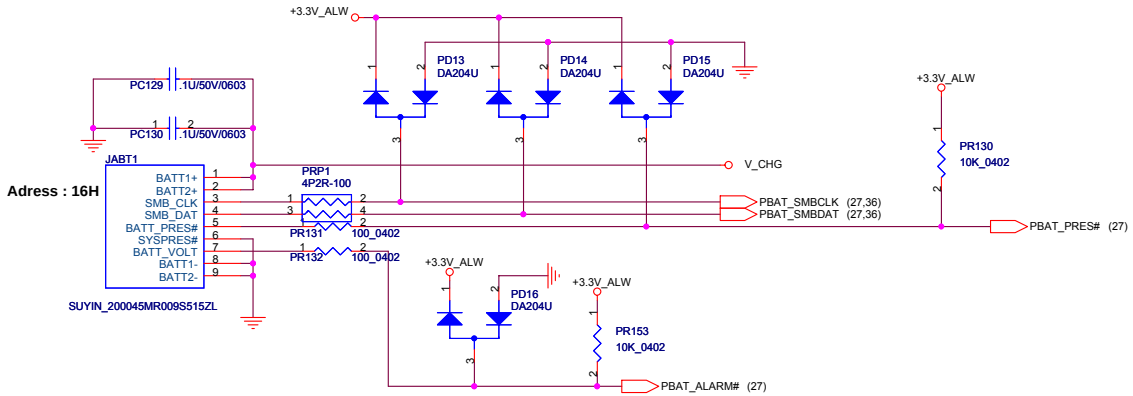


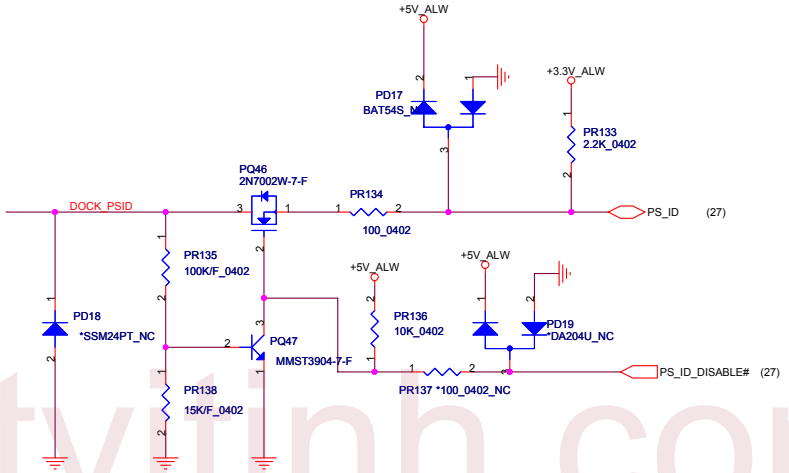


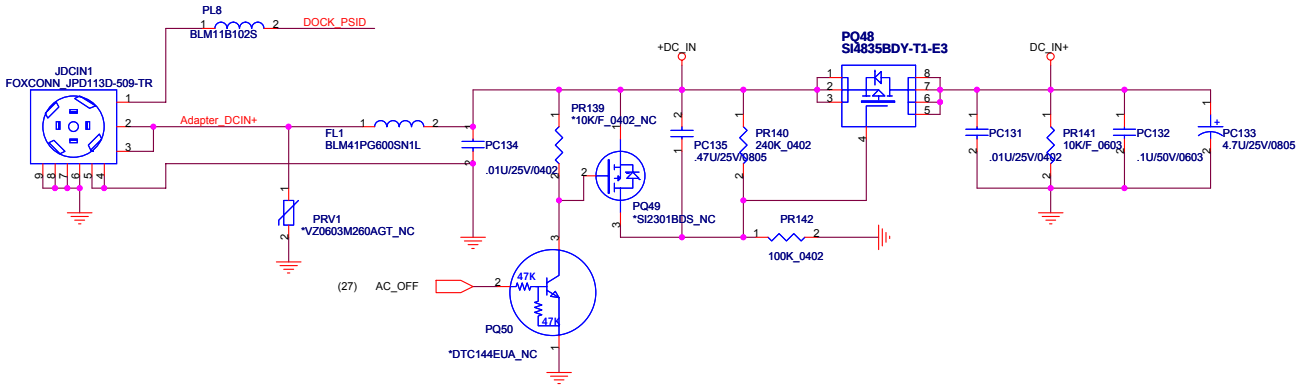


QUANTA COMPUTER

Title	RUN POWER SW	
Size	Document Number FX2	Rev 1A
Date: Friday, May 05, 2006	Sheet 40 of 47	





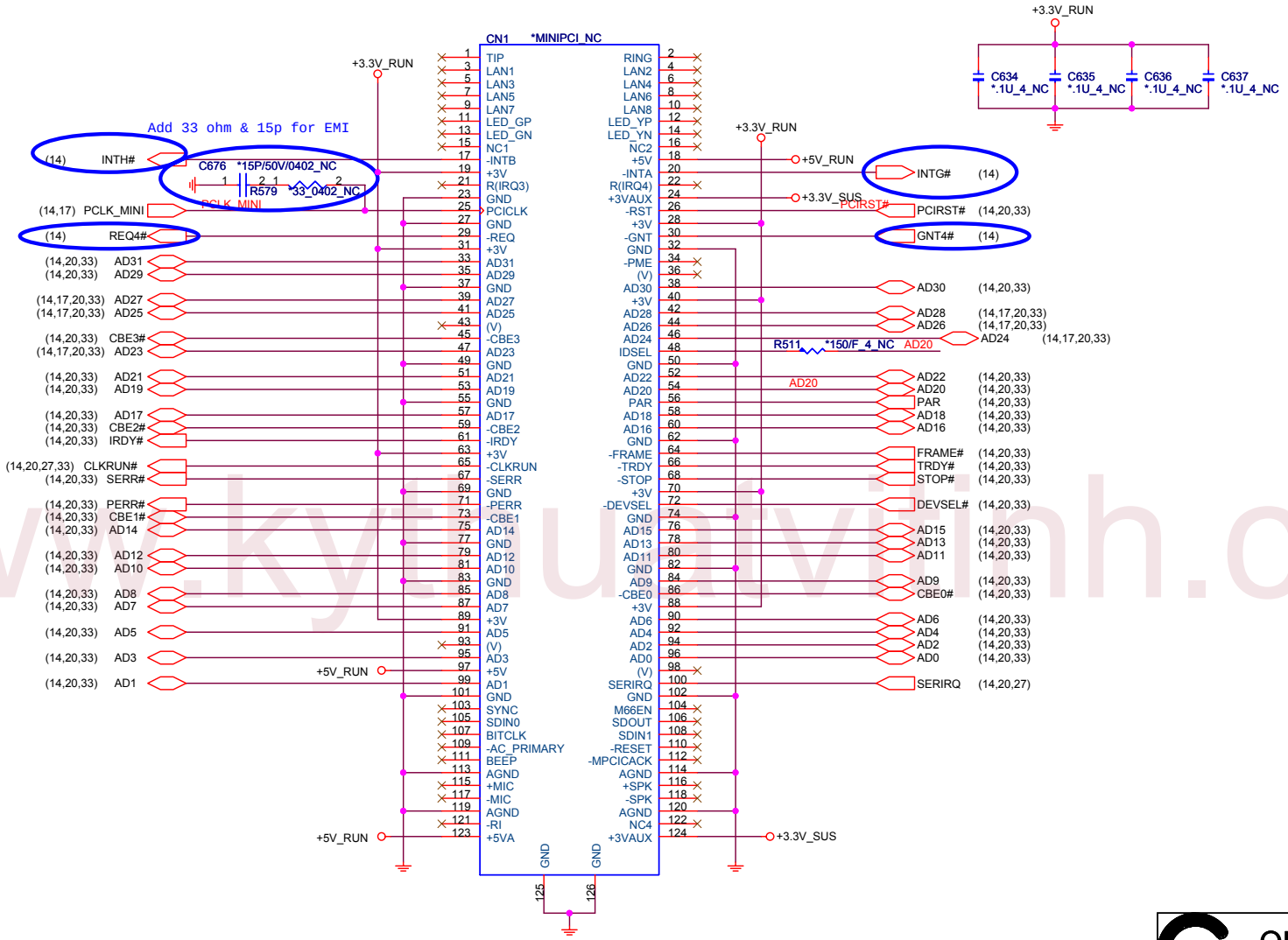


QUANTA COMPUTER

Title	DCIN,Batt	
Size	Document Number FX2	Rev 1A
Date: Friday, May 05, 2006	Sheet 41 of 47	

ID Select : AD20
Interrupt Pin : INTG# , INTH#
Request Indicate : REQ4#
Grant Indicate : GNT4#

DEBUG PURPOSE ONLY

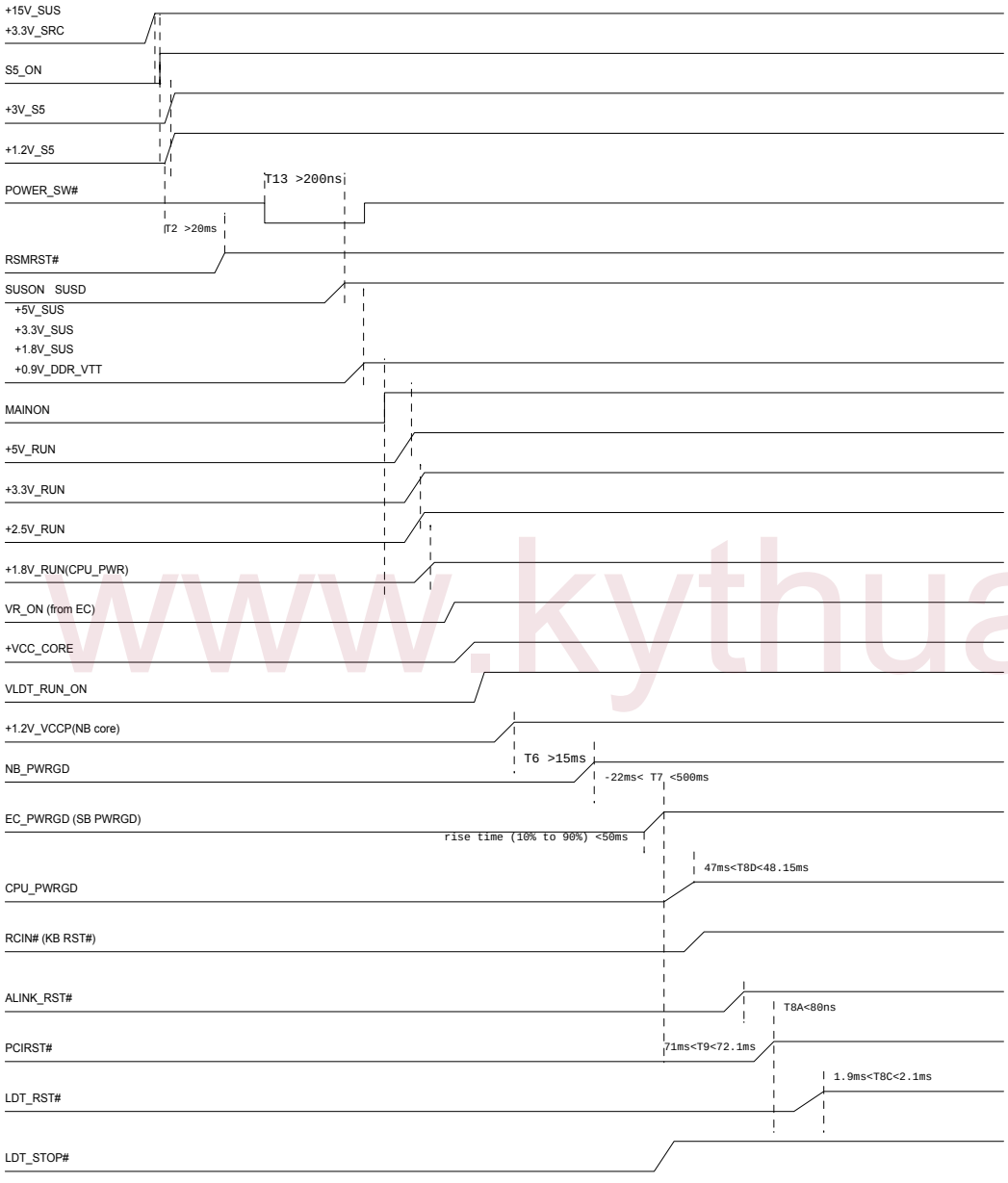


MPC

QUANTA COMPUTER

Title	MINI PCI(for debug)	
Size	Document Number FX2	Rev 1A
Date: Friday, May 05, 2006	Sheet 42 of 47	

Power On Sequence

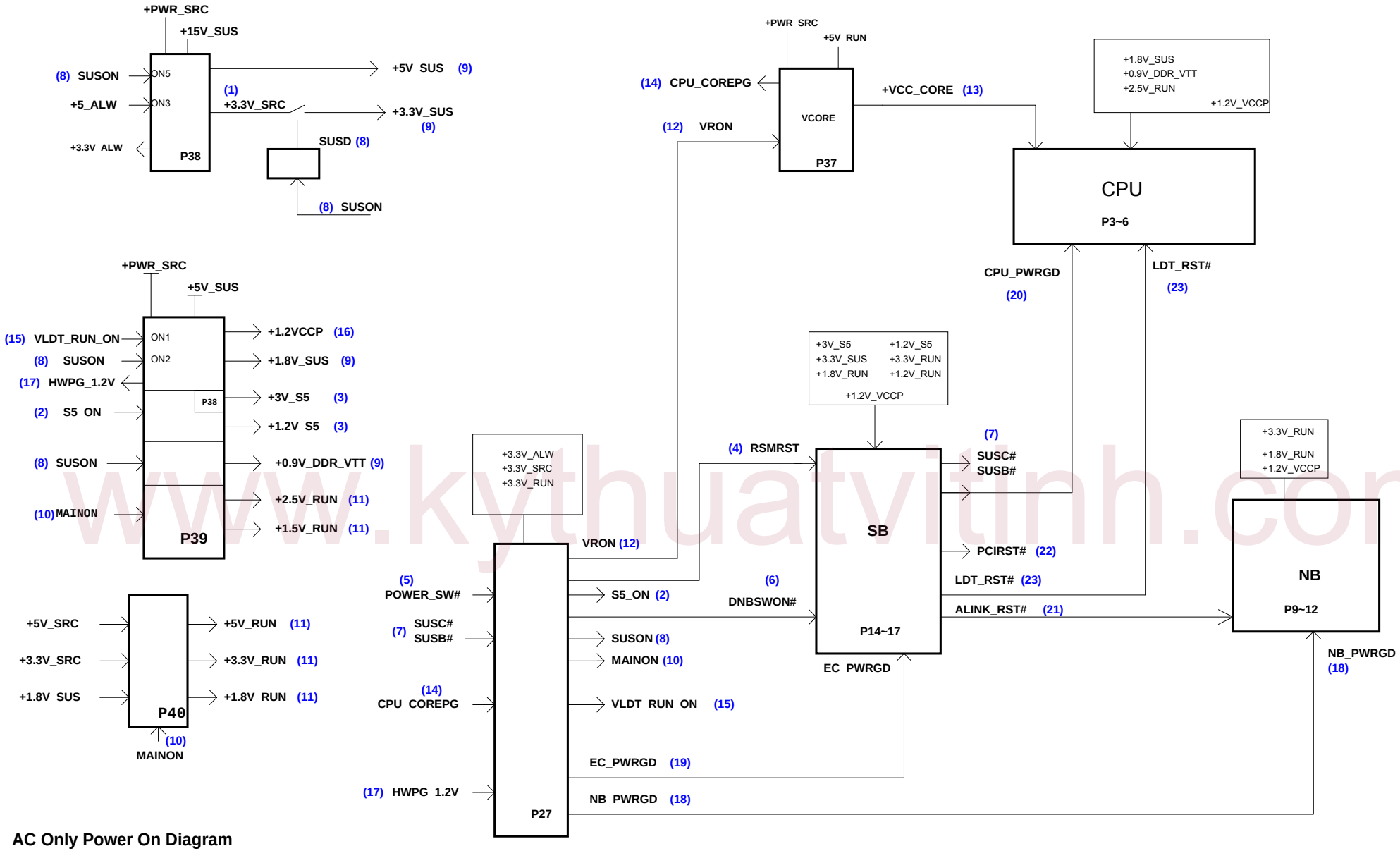


T6: NB core voltage to NB_PWRGD
T7: NB_PWRGD to SB_PWRGD
T8D: SB_PWRGD to CPU_PWRGD

T8A: ALINK_RST# to PCIRST#
T9: SB_PWRGD to PCIRST#
T8C: PCIRST# to LDT_RST#

QUANTA COMPUTER

Title	Power On Sequence	
Size	Document Number FX2	Rev 1A
Date: Wednesday, May 10, 2006	Sheet 43 of 47	

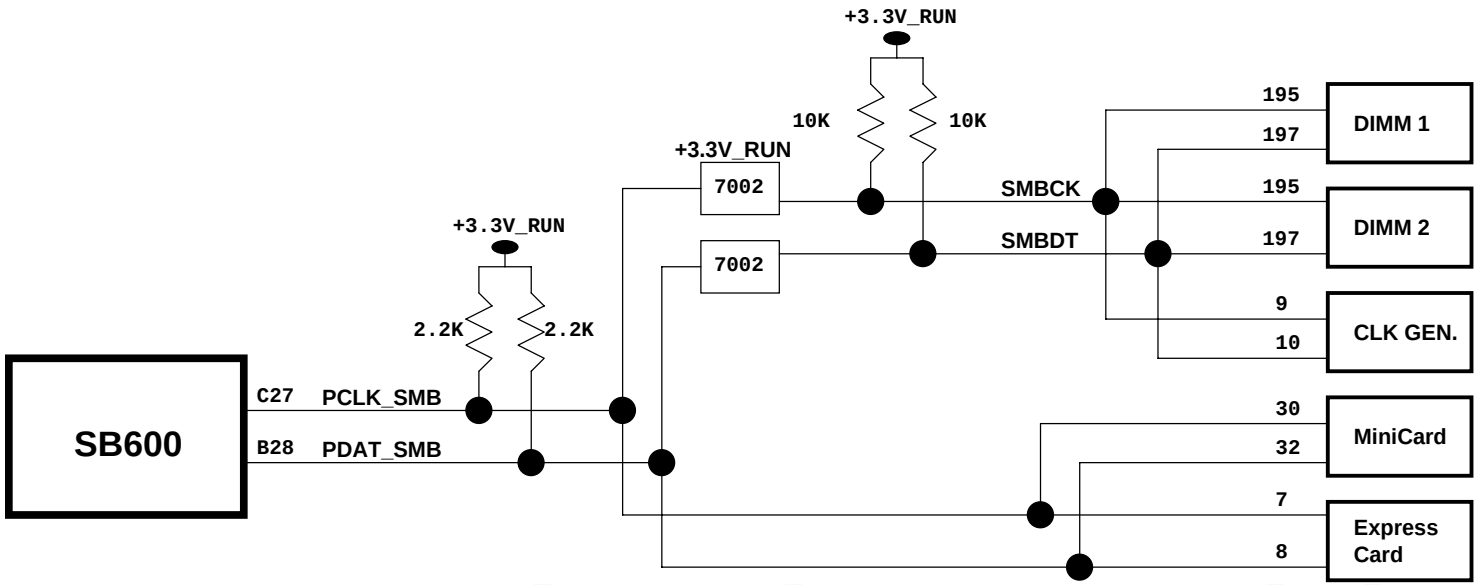


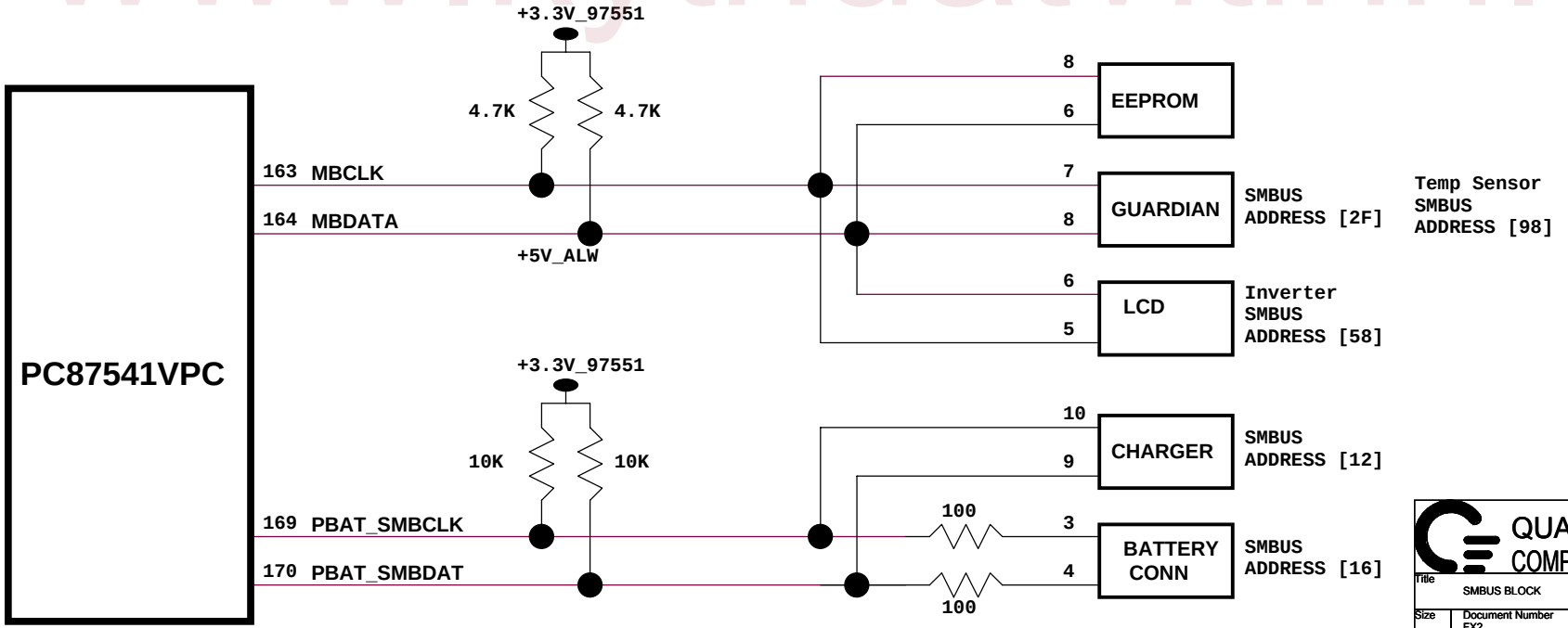
AC Only Power On Diagram

(1) +3.3V_SRC
(2) S5_ON
(3) +3V_S5, +1.2V_S5
(4) RSMRST
(5) POWER_SW#
(6) DNBSWON#
(7) SUSC#, SUSB#
(8) SUSON, SUSD
(9) +5V_SUS
+0.9V_DDR_VTT, +3.3V_SUS, +1.8V_SUS
(10) MAINON
(11) +5V_RUN, +3.3V_RUN
+2.5V_RUN, +1.8V_RUN, +1.5V_RUN
(12) VRON
(13) +VCC_CORE
(14) CPU_COREPG
(15) VLDT_RUN_ON
(16) +1.2_VCCP
(17) HWPG_1.2V
(18) NB_PWRGD
(19) EC_PWRGD
(20) CPU_PWRGD
(21) ALINK_RST#
(22) PCI_RST#
(23) LDT_RST#

QUANTA COMPUTER

Title	Power On Diagram	
Size	Document Number FX2	Rev 1A
Date: Thursday, May 04, 2006	Sheet 44 of 47	





QUANTA COMPUTER

Title	SMBUS BLOCK	
Size	Document Number FX2	Rev 1A
Date: Friday, May 05, 2006	Sheet 45 of 47	