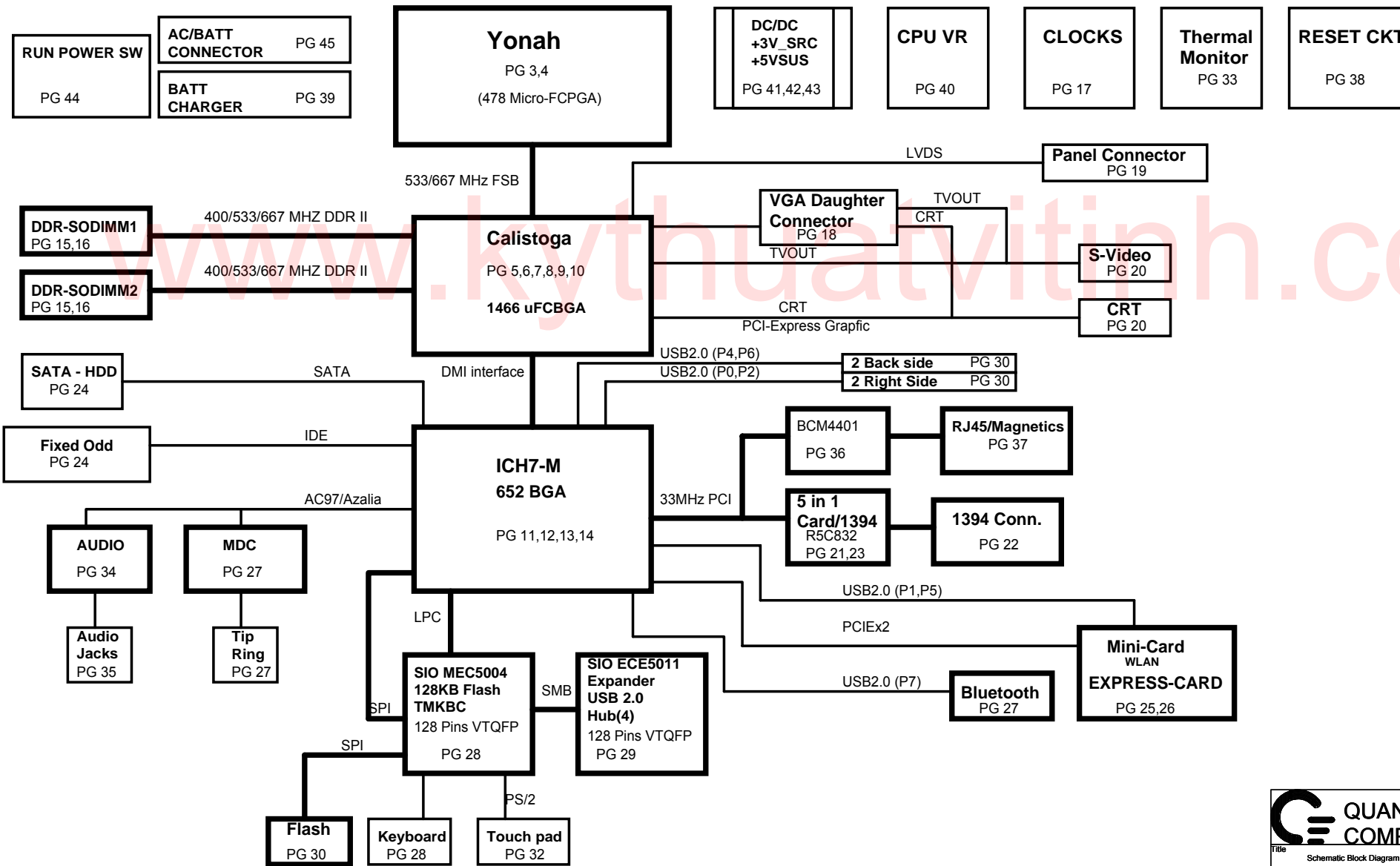


KEYLARGO-Integrate






VER : 2A

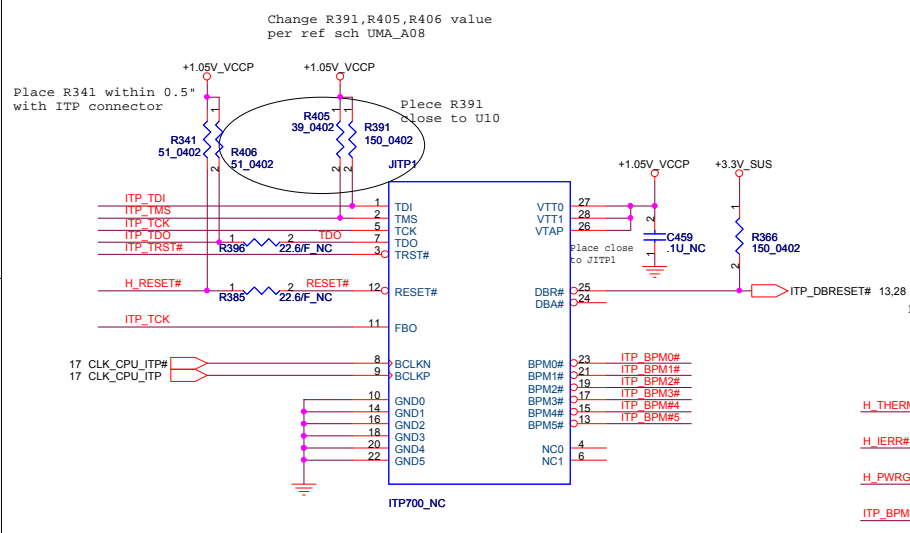
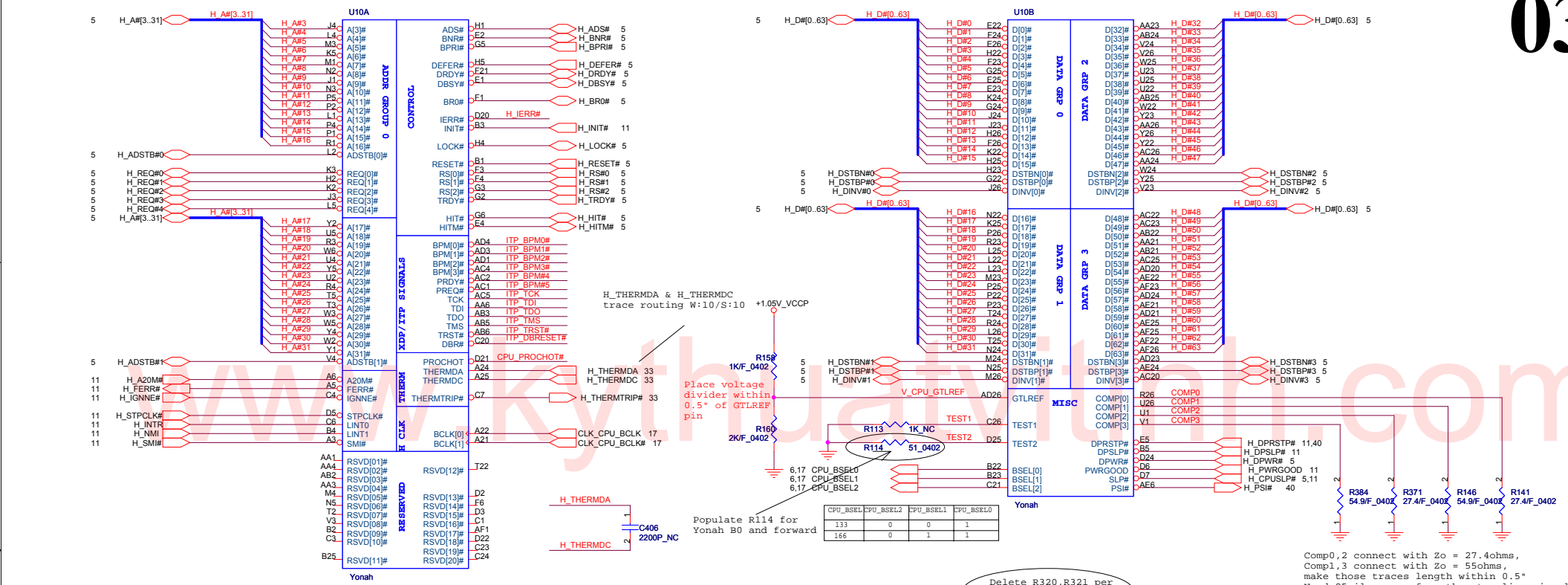


INDEX

Pg#	Description	DNI LIST
1	Schematic Block Diagram 1	
2	Blank Page	
3	Front Page	
4-5	Dothan	
6-10	Alviso	
11-13	ICH6	
14-15	DDRII SO-DIMM(200P)	
16	Clock Generator	
17	CH7306/7	
18-19	Blank Pages	
20	LCD Conn. & SSP	
21	CRT & TV Conn.	
22	SATA & IDE Conn.	
23	Screw Hole	
24	TI PIC6515	
25	Mini PCI Conn.	
26	MDC Conn.	
27-28	SIO (LPC47N354)	
29	SERIAL PORT & USB	
30	PARALLEL CONN.	
31	Flash ROM	
32	TOUCH PAD & BLUE TOOTH	
33	Switch Board Conn. & LED	
34	FAN & Thermal	
35-36	Audio CODEC (STAC9751) & Phone Jack	
37-38	LOM (BCM5751), Switch	
39	FIR	
40-41	Docking Conn. & Q-Switch	
42	Power Good	
43-44	Battery Selector & Charger	
45	CPU Power	
46	1.8V,0.9V,1.5V,1.05V	
47	3VALW/5V/3V/Power ON	
48	RUN Power Switch	
49	VGA DC/DC	
50	DCIN/Batt Conn.	

Power & Ground

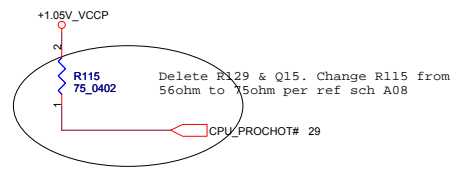
Label	Pg#	Description	Control Signal
DC_IN+		AC ADAPTER (20V)	
PBATT+		MAIN BATTERY + (10~17V)	
PWR_SRC		MAIN POWER (10~20V)	
RTC_PWR3_3V		RTC & PCL POWER (3_3V)	
+12V		+12V	DRUNPWROK
VHCORE		CPU CORE POWER (1.25/1.15V)	RUNPWROK
V1_2RUN		AGTL+ POWER (1.2V)	RUNPWROK
+3VRUN		SLP_S3# CTRLD POWER	RUN_ON
+3VSUS		SLP_S5# CTRLD POWER	SUS_ON
+5VALW		8051 POWER (5V)	
+5VRUN		SLP_S3# CTRLD POWER	RUN_ON
+5VSUS		SLP_S5# CTRLD POWER	SUS_ON
+5VHDD		HDD POWER (5V)	HDDC_EN#
+5VMOD		MODULE POWER (5V)	MODC_EN#
STRB#5V		EXTERNAL FDD POWER (5V)	FDD/LPT#
+5VFAN1, +5VFAN2		FAN POWER (5V)	FAN_OFF/ON#
VDDA		AUDIO ANALOG POWER (5V)	RUN_ON
1_8VSUS		RESUME WELL IN ICH	
1_8VRUN		SLP_S3# CTRLD POWER	
+3VALW		8051 POWER (3V)	
V1_5RUN		AGP I/O POWER	
 GND	ALL PAGES	DIGITAL GROUND	
 GNDDP		CPU POWER GND	
 CGNDP		CHARGER GND	
 DGNDP		DC/DC POWER GND	
 LANGND		COMBO CONN GND	



ITP disable guidelines

Signal	Resistor Value	Connect To	Resistor Placement
ITP_TDI	150 ohm +/- 5%	+1.05V_VCCP	Within 2.0" of the CPU
ITP_TMS	39 ohm +/- 5%	+1.05V_VCCP	Within 2.0" of the CPU
ITP_TRST#	680 ohm +/- 5%	GND	Within 2.0" of the CPU
ITP_TCK	27 ohm +/- 5%	GND	Within 2.0" of the CPU
TDO	Open	N/A	Within 2.0" of the CPU

Note: Populate R396, R385, C459 and R450 when ITP connector is populated.



QUANTA COMPUTER

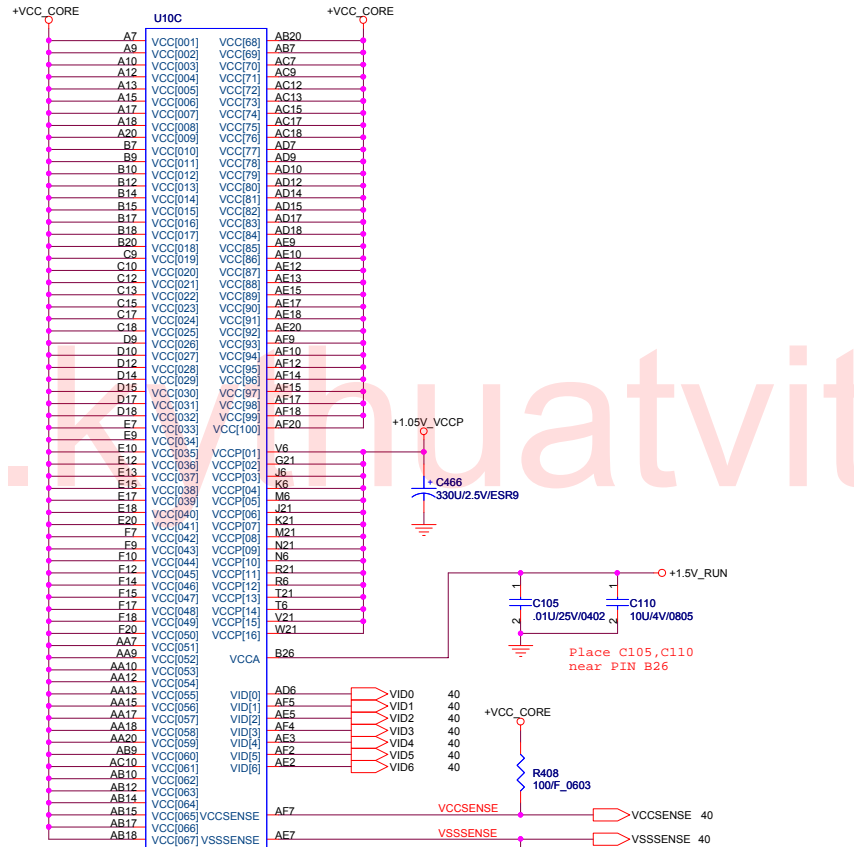
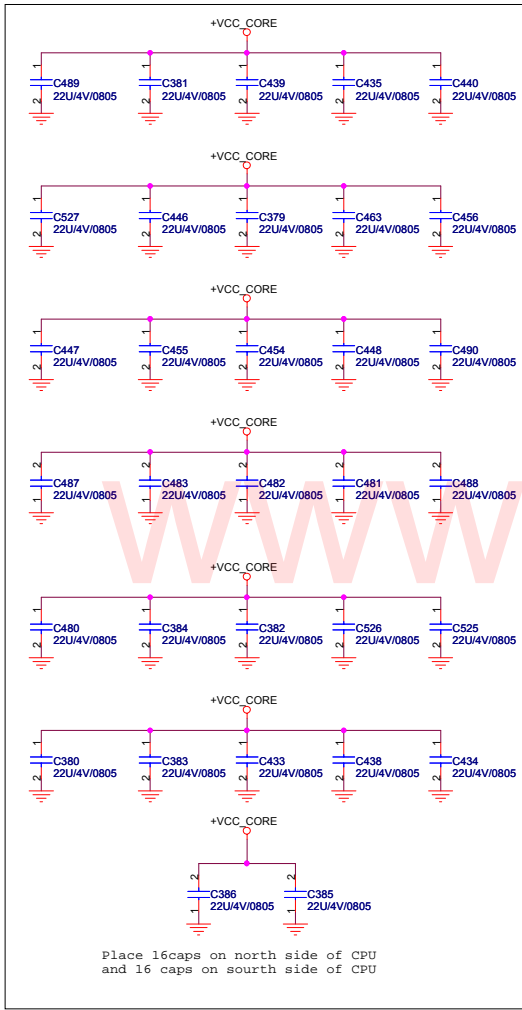
Title: Yonah Processor (HOST)

Size: Document Number FM1

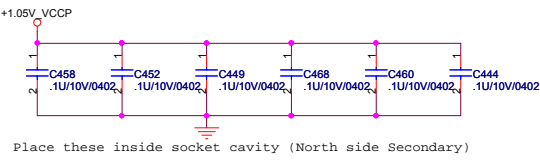
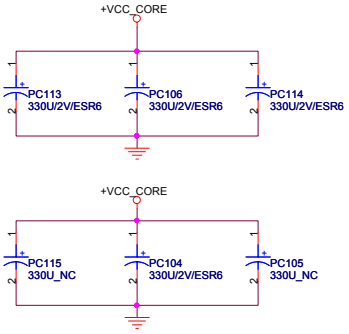
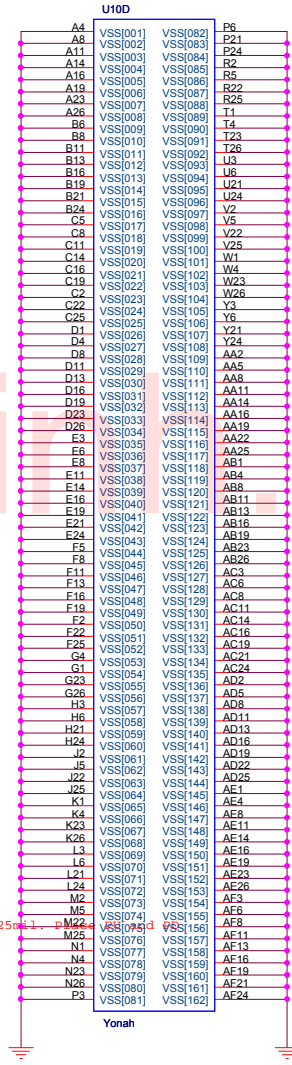
Date: Tuesday, September 06, 2005

Sheet: 3 of 51

Rev: 2A



Route VCCSENSE and VSSSENSE traces at 27.4ohms with 10mil spacing and for other signals keep 10mil spacing 25mil and length match within 25mil. Place R401, R408, R401 close to U10 within 0.5"

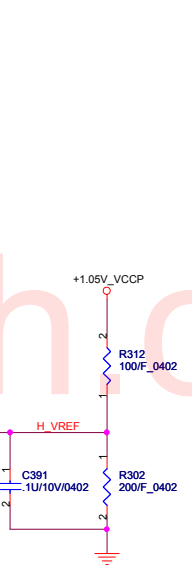
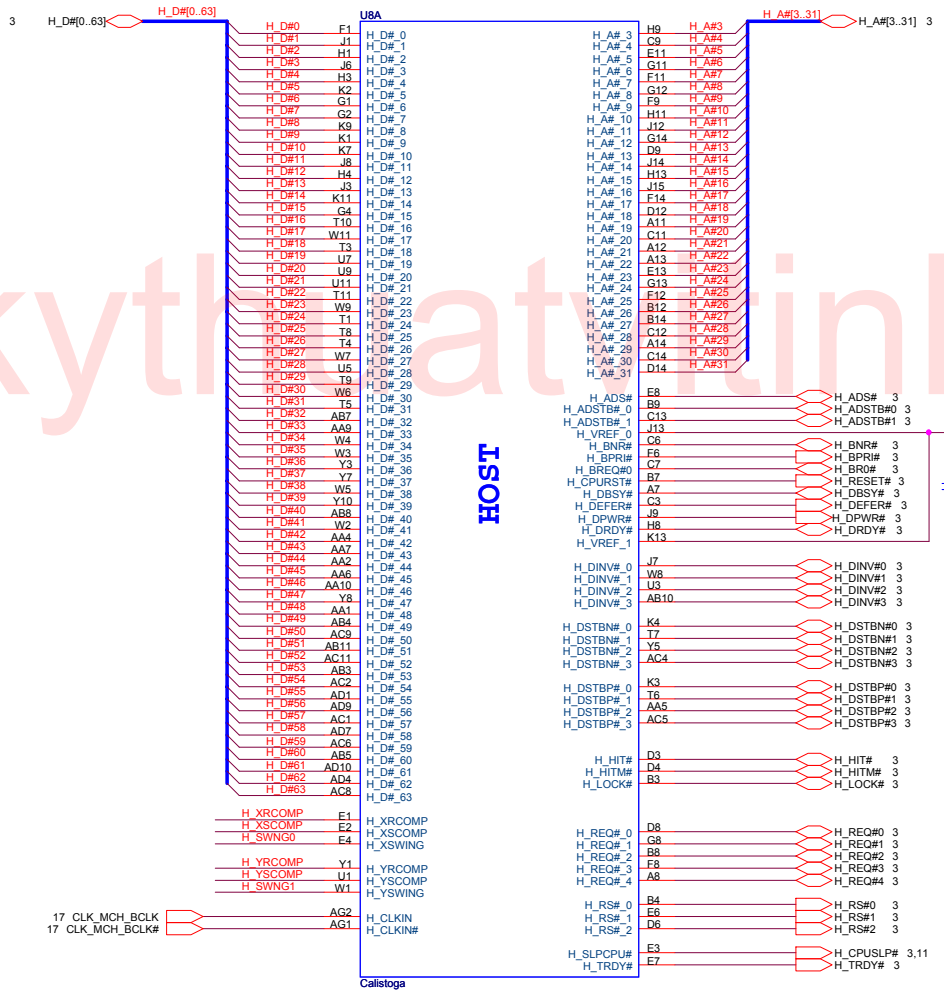
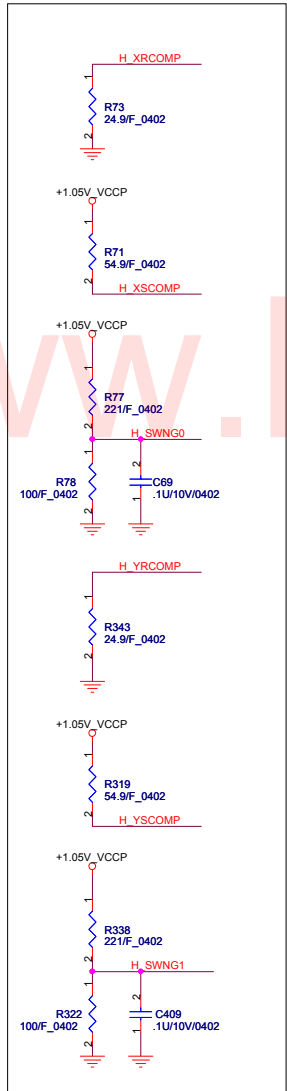


Total caps = 2684 uF
ESR = 6m ohm/4 // 3m ohm/32

QUANTA COMPUTER

Title: Yonah Processor (POWER)

Size: FM1	Document Number: FM1	Rev: 2A
Date: Tuesday, September 06, 2005	Sheet: 4	of 51



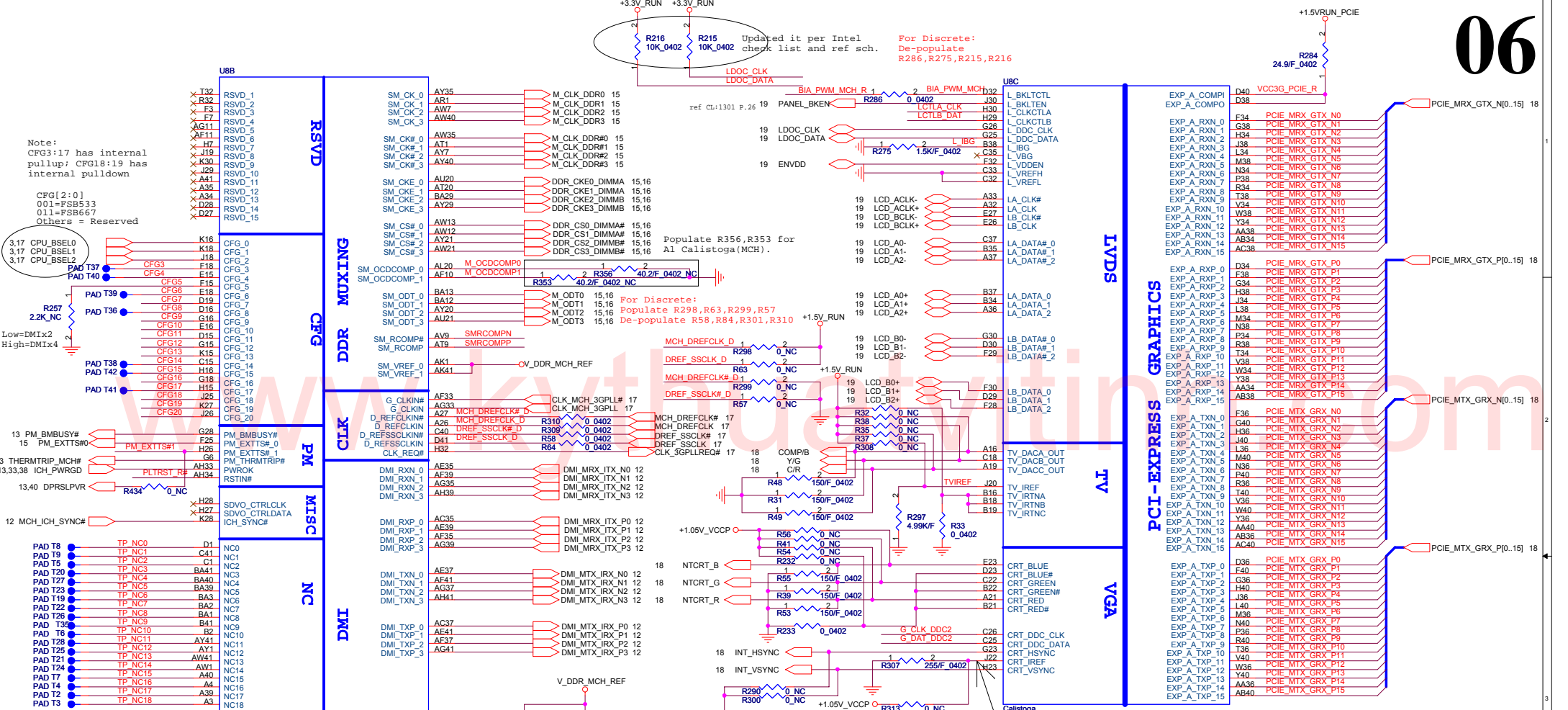
H_XRCOMP, H_XSCOMP, H_YRCOMP, H_YSCOMP,
 H_SWNG0, H_SWNG1 used W:10/S:20 mil.
 R & C of HXRCOMP, HXSCOMP, HYRCOMP, HYSCOMP,
 H_SWNG0, H_SWNG1 trace length less 0.5" from
 U3

QUANTA COMPUTER

Title: Callistoga (Host)

Size: FM1 | Document Number: FM1 | Rev: 2A

Date: Tuesday, September 06, 2005 | Sheet: 5 of 51



Note: CFG3:17 has internal pullup; CFG18:19 has internal pulldown

CFG[2:0] 001=FSB533 011=FSB667 Others = Reserved

3.17 CPU_BSEL0 3.17 CPU_BSEL1 3.17 CPU_BSEL2

Low=DMiX2 High=DMiX4

13 PM_BMBUSY# 15 PM_EXTTSS#

33 THERMTRIP_MCH# 13.3338 ICH_PWRGD

13.40 DPRSLPVR

12 MCH_I0H_SYNC#

SDVO_CTRLCLK SDVO_CTRLDATA ICH_SYNC#

SDVO_CTRL & SDVO_DATA Low = No SDVO Device Present High = SDVO Device Present

Calistoga

+1.8V_SUS

SMRCOMPEN SMRCOMPMP

CPU_Strap Low=RSVD High=Mobile CPU

PCIE Graphics Lane Low = Reverse Lane High = Normal operation

12.13.26.28 PLTRST#

Host PLL VCC Select Low=Reserved High=Mobility

PSB 4X CLK Enable Low=Calistoga High=Reserved

PSB Dynamic ODT Low=Dynamic ODT Disable High=Dynamic ODT Enable

Place C442, C176 close to U3.AK1 & U3.AK41

VCC Select Low=1.05V High=1.5V

DMI Lane Reversal Low=Normal High=Lane Reversed

Added BIA_PWM converted I/F gate per GG list

For Discrete: De-populate R223, R224, RP1, Q4, Q5, U40

Calistoga VGA_IREF Nets should be Routed 20 mils away from any Signals. Per Intel

For Discrete: De-populate R223, R224, RP1, Q4, Q5, U40

For Discrete: De-populate R223, R224, RP1, Q4, Q5, U40

For Discrete: De-populate R223, R224, RP1, Q4, Q5, U40

For Discrete: De-populate R223, R224, RP1, Q4, Q5, U40

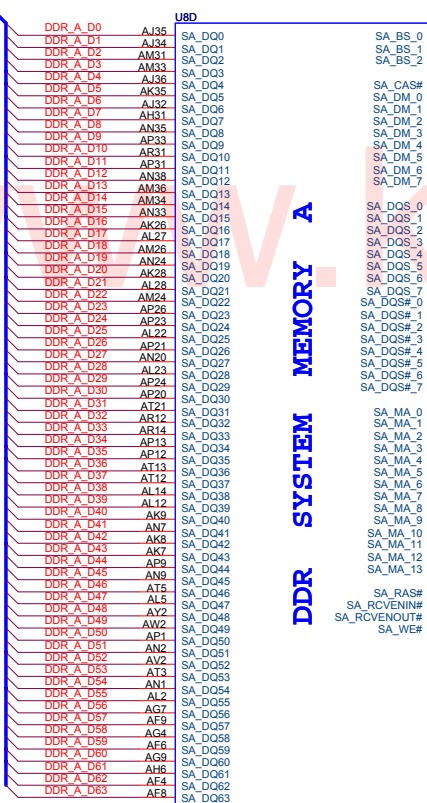
QUANTA COMPUTER

Title: Calistoga (VGA,DMI)

Size	Document Number	Rev
FM1		2A

Date: Tuesday, September 06, 2005 Sheet 6 of 51

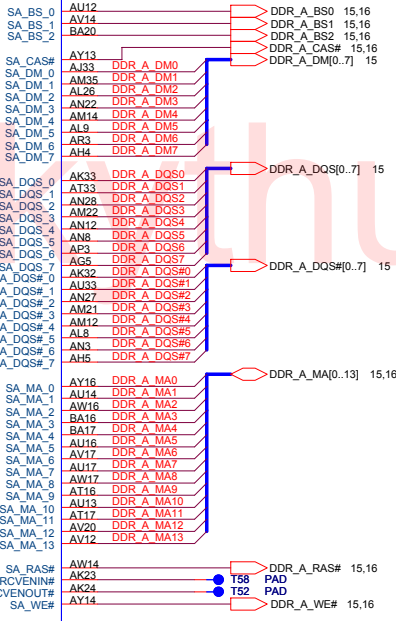
15 DDR_A_D[0..63]



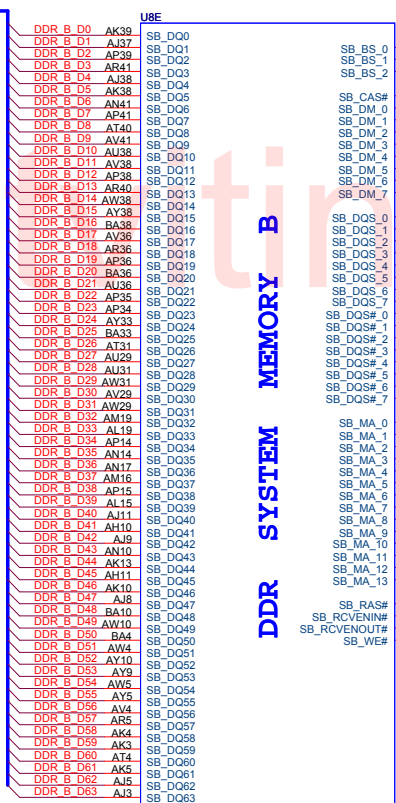
UBD

DDR SYSTEM MEMORY A

Calistoga



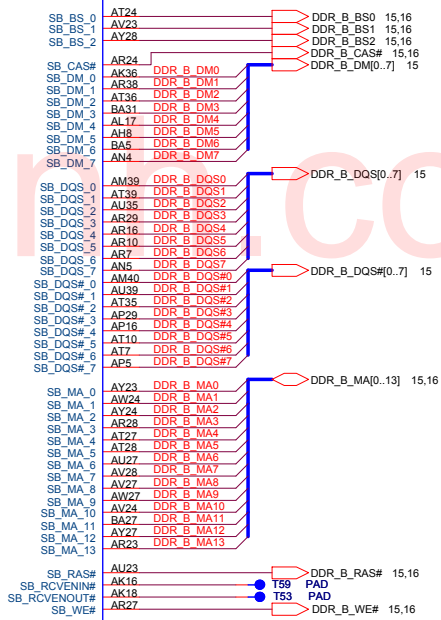
15 DDR_B_D[0..63]



UBE

DDR SYSTEM MEMORY B

Calistoga

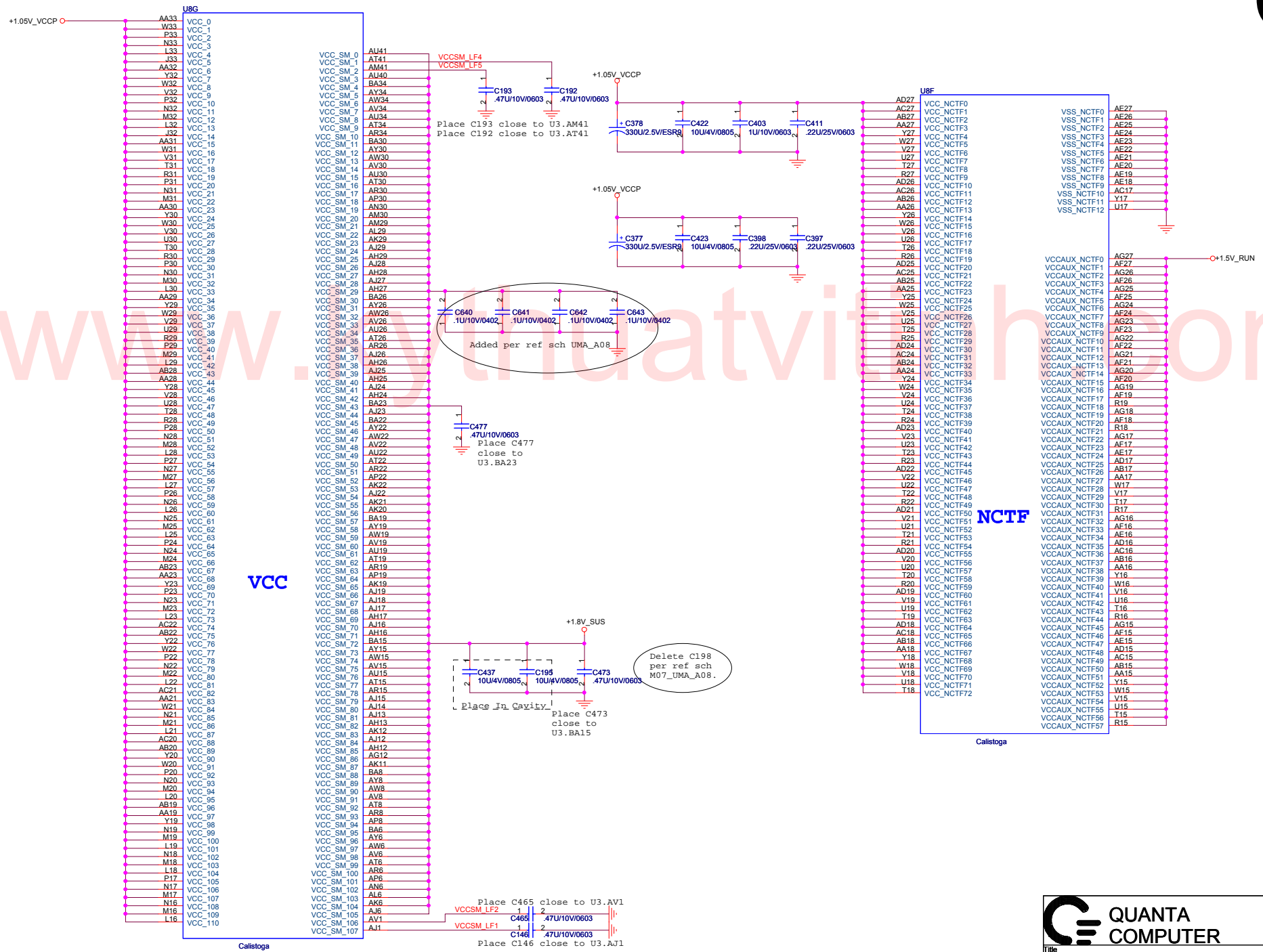


QUANTA COMPUTER

Title: Calistoga (DDR2)

Size	Document Number	Rev
FM1		2A

Date: Tuesday, September 06, 2005 Sheet 7 of 51

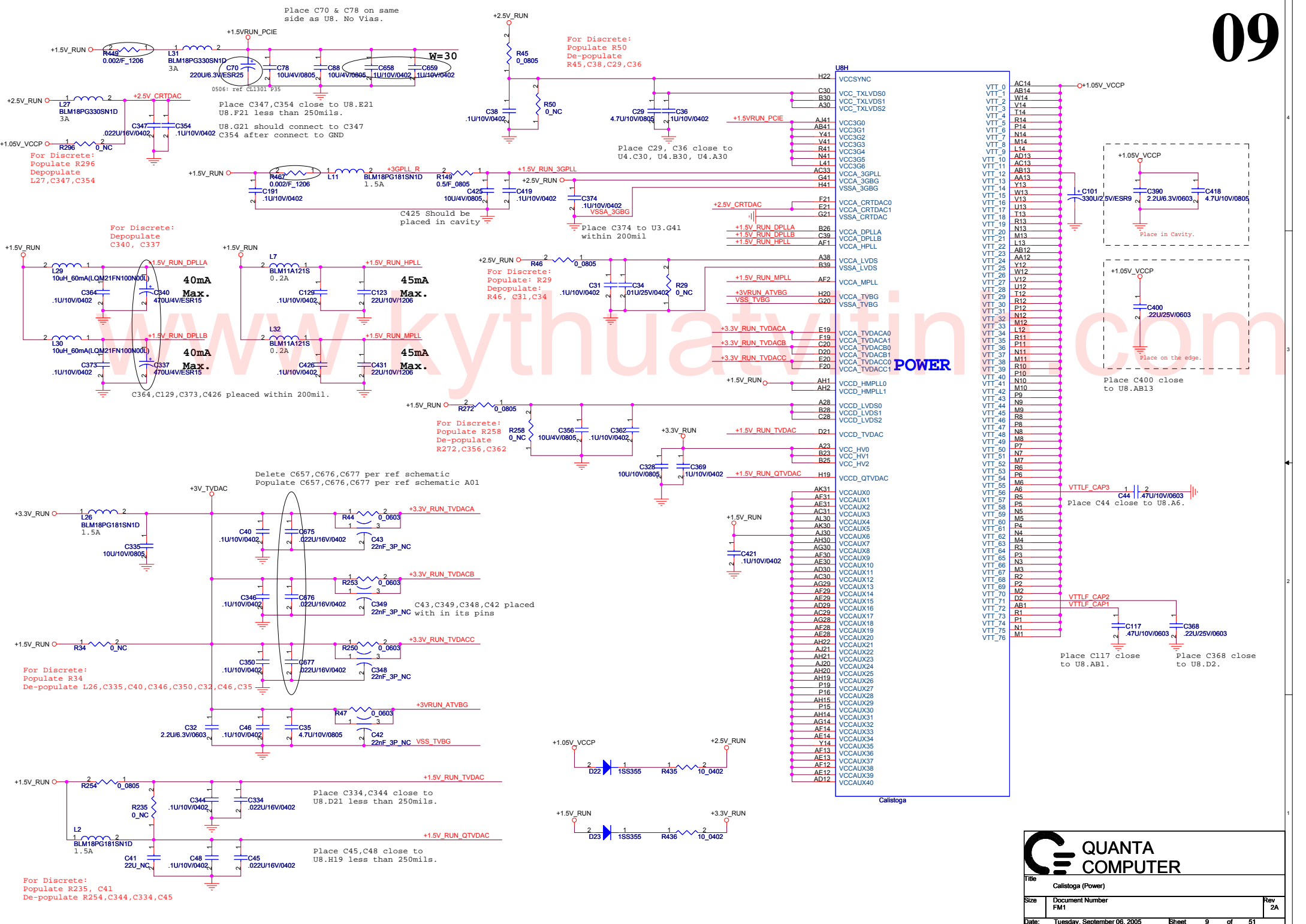


QUANTA COMPUTER

Title: Callistoga (VCC, NCTF)

Size	Document Number	Rev
FM1		2A

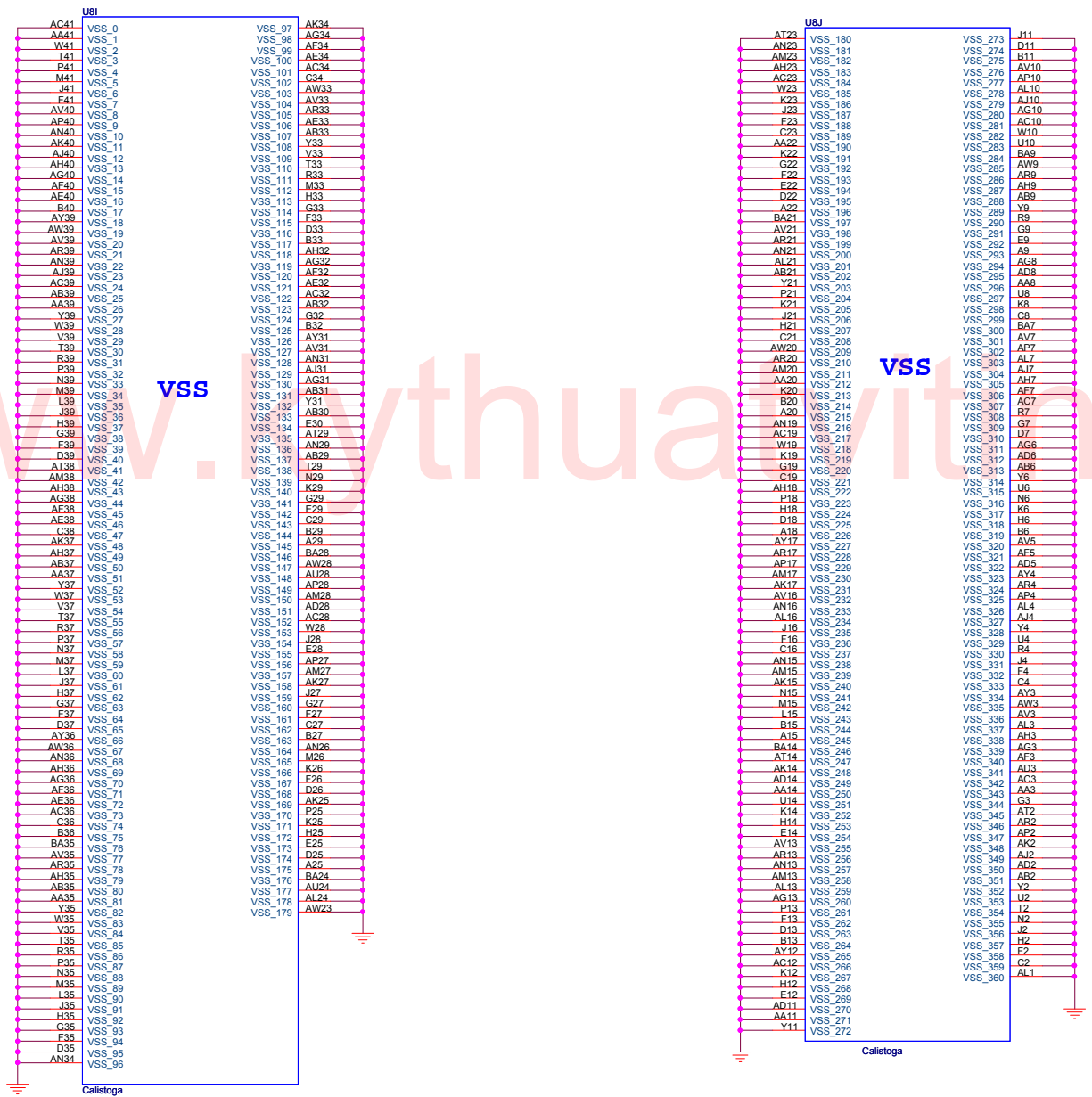
Date: Tuesday, September 06, 2005 Sheet 8 of 51



QUANTA COMPUTER

Title: Calistoga (Power)

Size: Document Number FM1	Rev: 2A
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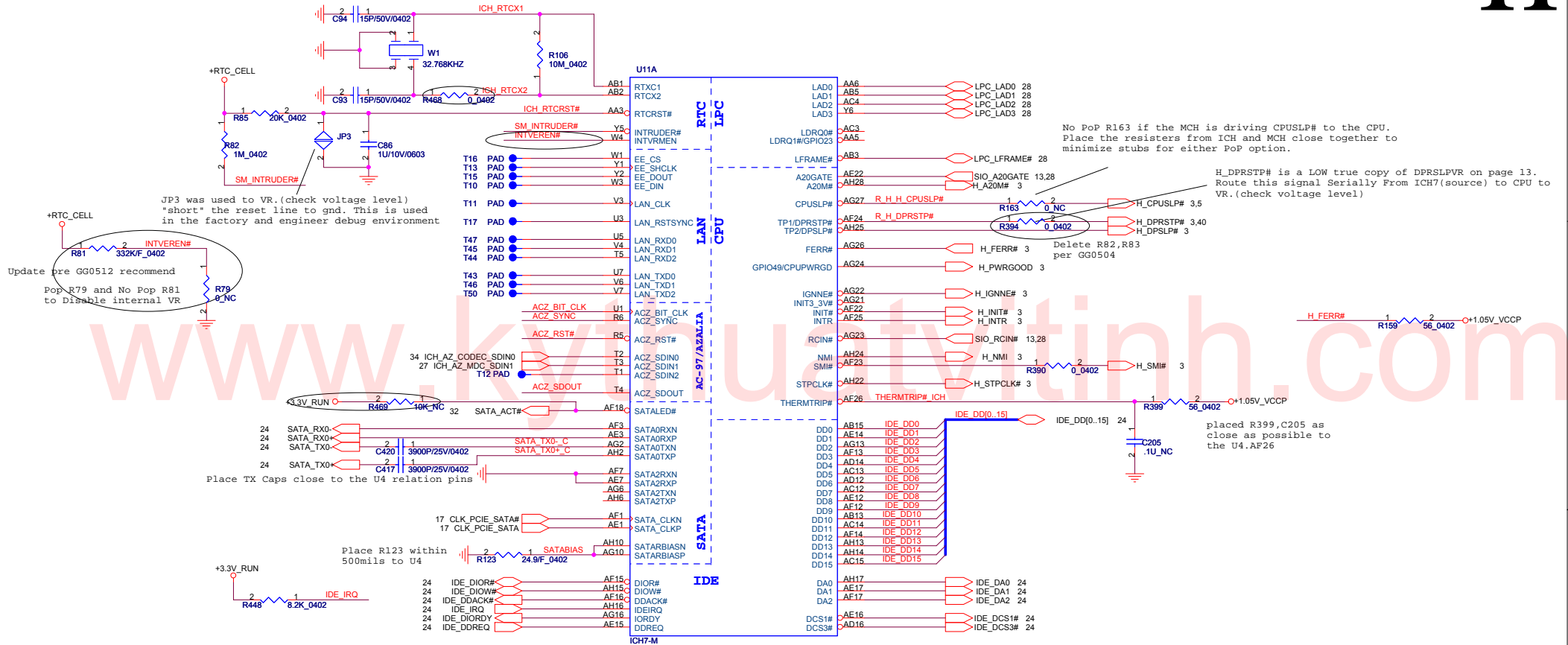


QUANTA COMPUTER

Title: Callistoga (VSS,NCTF)

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JP3 was used to VR.(check voltage level)
"short" the reset line to gnd. This is used
in the factory and engineer debug environment

Update pre GG0512 recommend
Pop R79 and No Pop R81
to Disable internal VR

Place TX Caps close to the U4 relation pins

Place R123 within
500mils to U4

X1,X2 Docking

IAC_SYNC	Port X Line	R126
1	1X2, 2X1	STUFF
0	4X1	UNSTUFF

All resistors of termination used
of "T" type routing need tuned
equal and close to the source.

No PoP R163 if the MCH is driving CPUSLP# to the CPU.
Place the resistors from ICH and MCH close together to
minimize stubs for either PoP option.

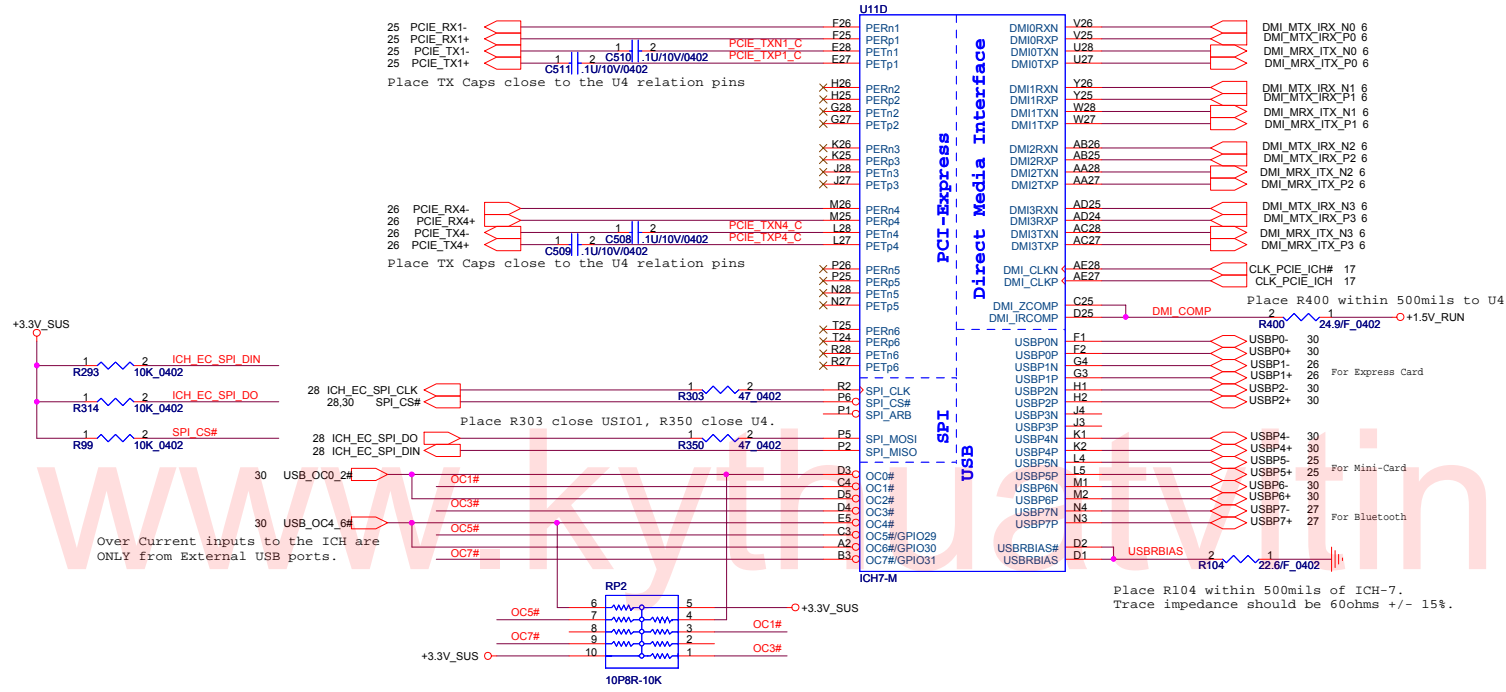
H_DPRSTP# is a LOW true copy of DPRSLPVR on page 13.
Route this signal Serially From ICH7(source) to CPU to
VR.(check voltage level)

Delete R82,R83
per GG0504

placed R399,C205 as
close as possible to
the U4.AF26

QUANTA
COMPUTER

Title ICH7-M (CPU,IDE,SATA,LPC,AC97)		
Size FM1	Document Number	Rev 2A
Date: Tuesday, September 06, 2005	Sheet 11	of 51



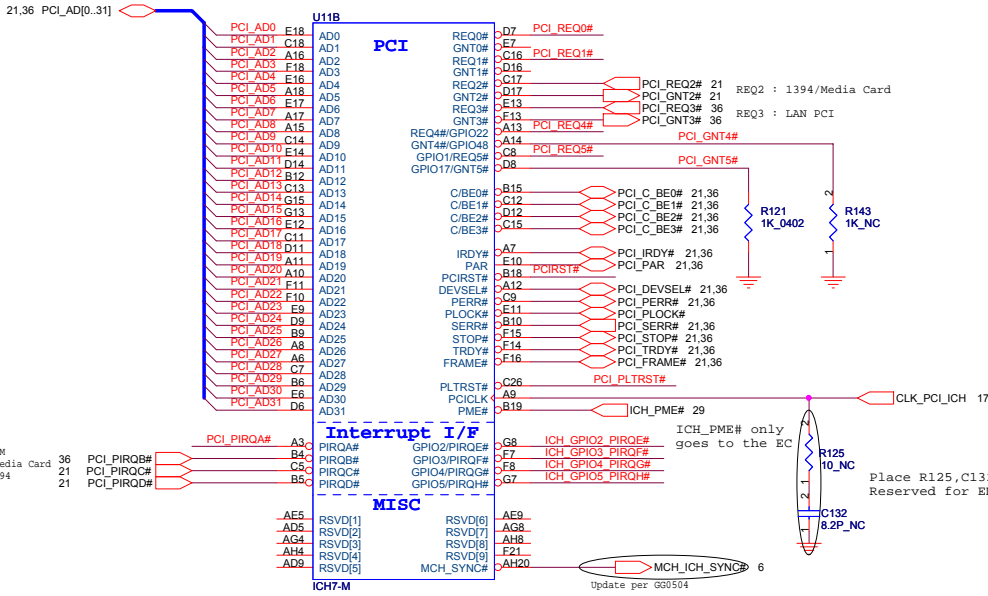
Place TX Caps close to the U4 relation pins

Place TX Caps close to the U4 relation pins

Place R303 close USI01, R350 close U4.

Over Current inputs to the ICH are ONLY from External USB ports.

Place R104 within 500mils of ICH-7. Trace impedance should be 60ohms +/- 15%.

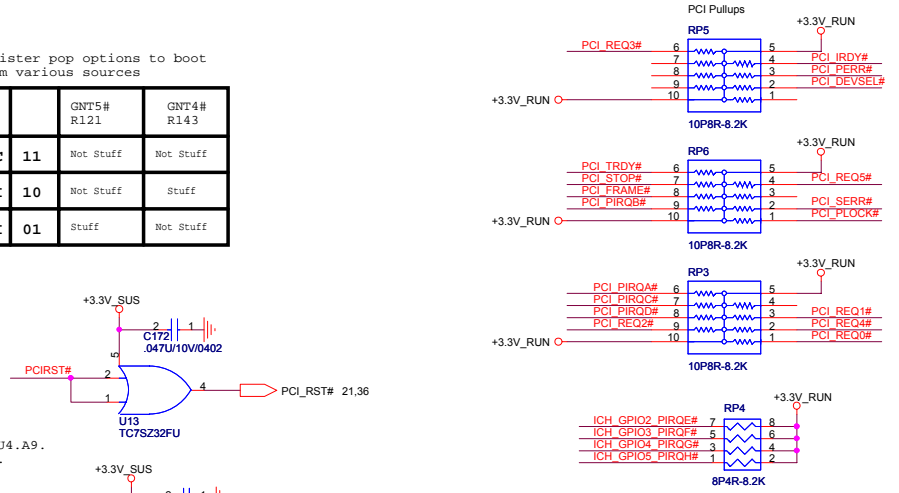


ICH_PME# only goes to the EC

Place R125, C132 close to U4.A9. Reserved for EMI fine tune.

Register pop options to boot from various sources

		GNT5# R121	GNT4# R143
LPC	11	Not Stuff	Not Stuff
PCI	10	Not Stuff	Stuff
SPI	01	Stuff	Not Stuff



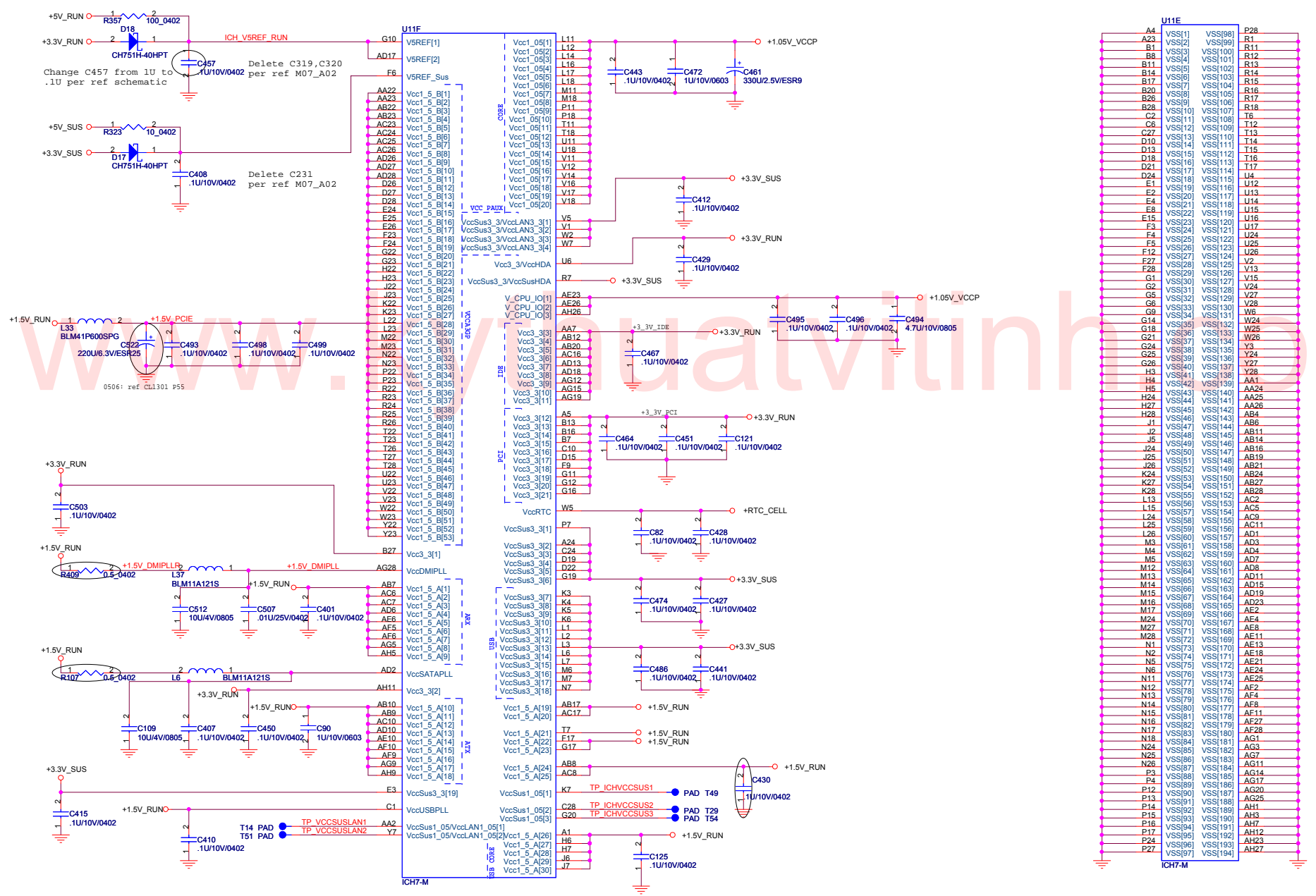
Add Buffers as needed for Loading and fanout concerns

QUANTA COMPUTER

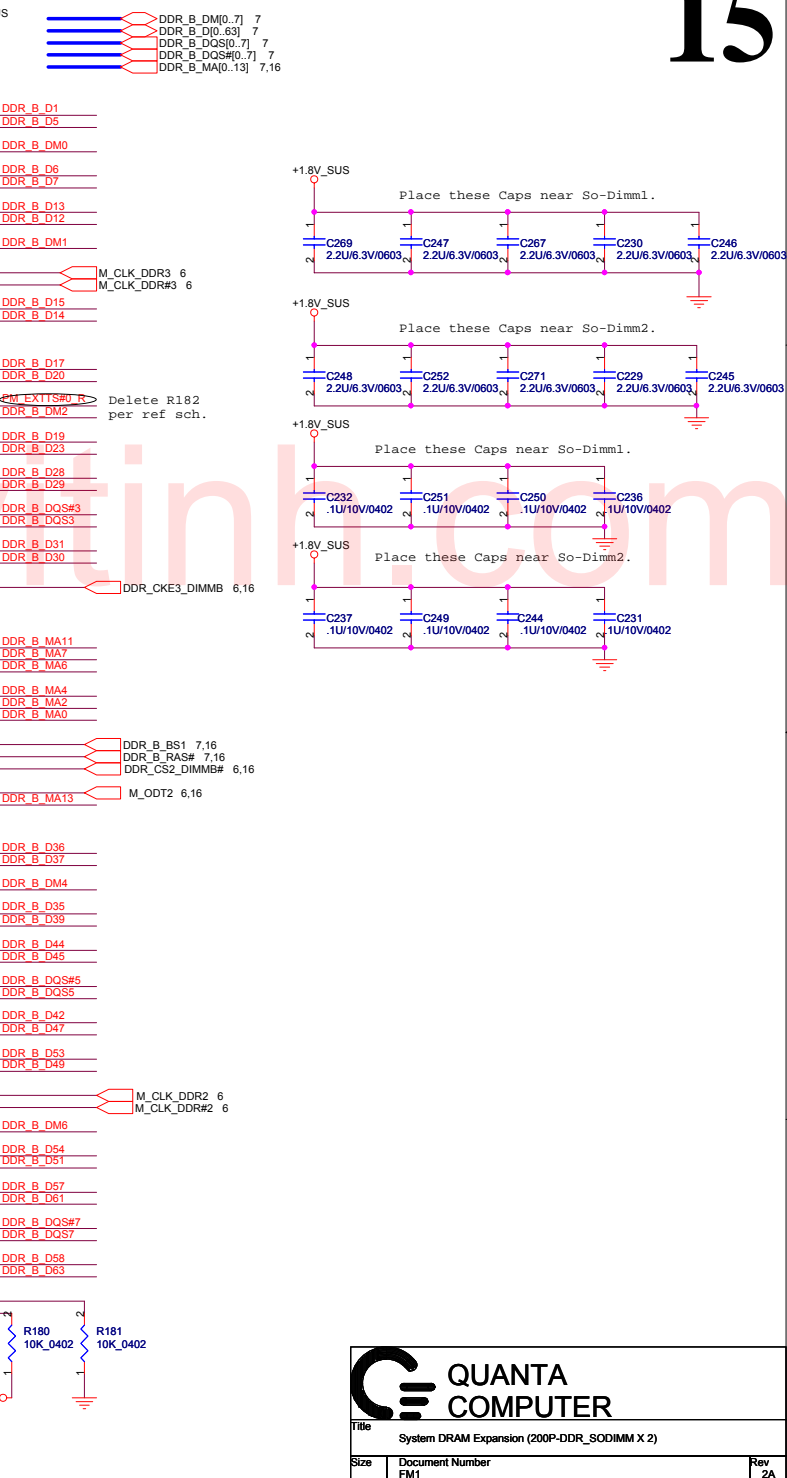
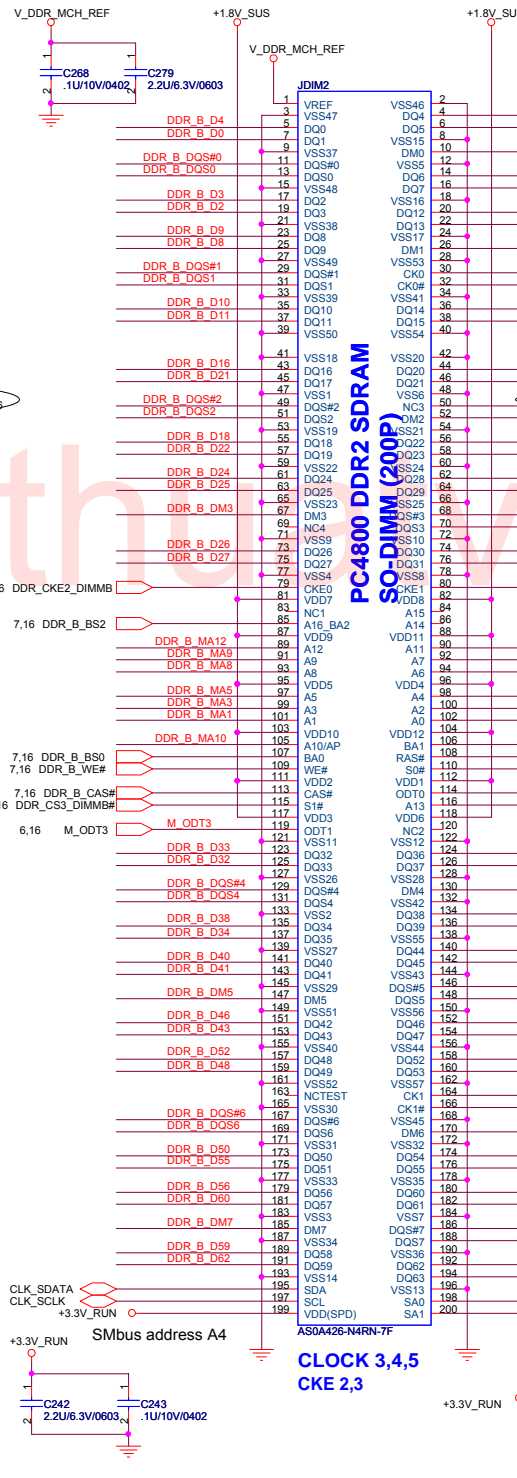
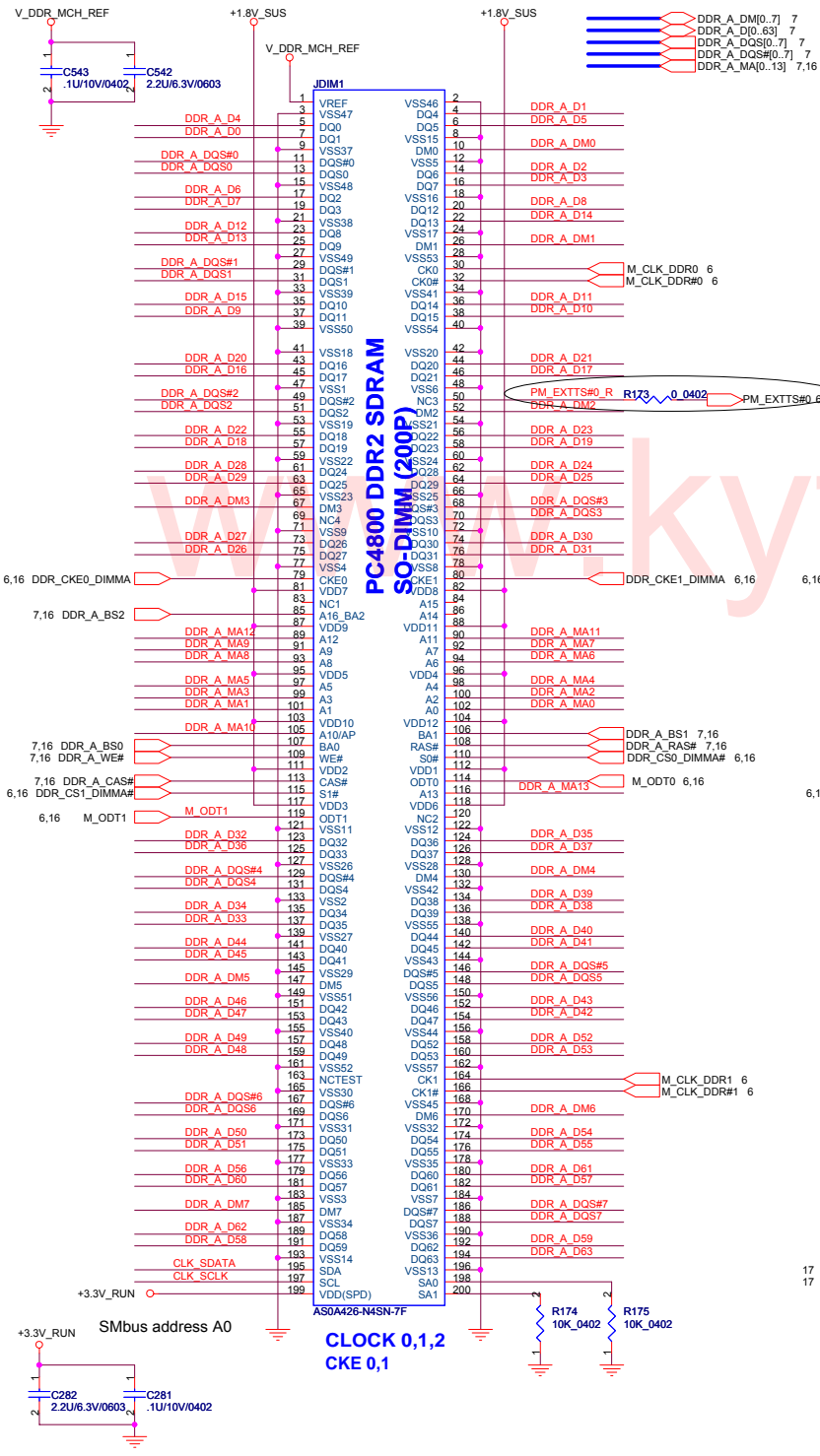
Title: ICH7-M (USB,DMI,PCIe,PCI)

Size	Document Number	Rev
	FM1	2A

Date: Tuesday, September 06, 2005 Sheet 12 of 51



U11E		P28
A4	VSS[1]	VSS[98]
A23	VSS[2]	VSS[99]
B1	VSS[3]	VSS[100]
B8	VSS[4]	VSS[101]
B14	VSS[5]	VSS[102]
B17	VSS[6]	VSS[103]
B20	VSS[7]	VSS[104]
B26	VSS[8]	VSS[105]
B28	VSS[9]	VSS[106]
C2	VSS[10]	VSS[107]
C6	VSS[11]	VSS[108]
C27	VSS[12]	VSS[109]
D10	VSS[13]	VSS[110]
D13	VSS[14]	VSS[111]
D18	VSS[15]	VSS[112]
D21	VSS[16]	VSS[113]
D24	VSS[17]	VSS[114]
E1	VSS[18]	VSS[115]
E2	VSS[19]	VSS[116]
E4	VSS[20]	VSS[117]
E8	VSS[21]	VSS[118]
E15	VSS[22]	VSS[119]
F3	VSS[23]	VSS[120]
F4	VSS[24]	VSS[121]
F5	VSS[25]	VSS[122]
F12	VSS[26]	VSS[123]
F27	VSS[27]	VSS[124]
F28	VSS[28]	VSS[125]
G1	VSS[29]	VSS[126]
G2	VSS[30]	VSS[127]
G5	VSS[31]	VSS[128]
G6	VSS[32]	VSS[129]
G9	VSS[33]	VSS[130]
G14	VSS[34]	VSS[131]
G18	VSS[35]	VSS[132]
G21	VSS[36]	VSS[133]
G24	VSS[37]	VSS[134]
G25	VSS[38]	VSS[135]
G26	VSS[39]	VSS[136]
H3	VSS[40]	VSS[137]
H4	VSS[41]	VSS[138]
H4	VSS[42]	VSS[139]
H5	VSS[43]	VSS[140]
H24	VSS[44]	VSS[141]
H27	VSS[45]	VSS[142]
H28	VSS[46]	VSS[143]
J1	VSS[47]	VSS[144]
J5	VSS[48]	VSS[145]
J4	VSS[49]	VSS[146]
J5	VSS[50]	VSS[147]
J25	VSS[51]	VSS[148]
K2	VSS[52]	VSS[149]
K27	VSS[53]	VSS[150]
K28	VSS[54]	VSS[151]
K28	VSS[55]	VSS[152]
L13	VSS[56]	VSS[153]
L15	VSS[57]	VSS[154]
L24	VSS[58]	VSS[155]
L25	VSS[59]	VSS[156]
L26	VSS[60]	VSS[157]
M3	VSS[61]	VSS[158]
M4	VSS[62]	VSS[159]
M5	VSS[63]	VSS[160]
M12	VSS[64]	VSS[161]
M13	VSS[65]	VSS[162]
M14	VSS[66]	VSS[163]
M15	VSS[67]	VSS[164]
M16	VSS[68]	VSS[165]
M17	VSS[69]	VSS[166]
M24	VSS[70]	VSS[167]
M27	VSS[71]	VSS[168]
M28	VSS[72]	VSS[169]
N1	VSS[73]	VSS[170]
N2	VSS[74]	VSS[171]
N5	VSS[75]	VSS[172]
N6	VSS[76]	VSS[173]
N11	VSS[77]	VSS[174]
N12	VSS[78]	VSS[175]
N13	VSS[79]	VSS[176]
N14	VSS[80]	VSS[177]
N15	VSS[81]	VSS[178]
N16	VSS[82]	VSS[179]
N17	VSS[83]	VSS[180]
N18	VSS[84]	VSS[181]
N24	VSS[85]	VSS[182]
N25	VSS[86]	VSS[183]
P3	VSS[87]	VSS[184]
P3	VSS[88]	VSS[185]
P4	VSS[89]	VSS[186]
P12	VSS[90]	VSS[187]
P13	VSS[91]	VSS[188]
P14	VSS[92]	VSS[189]
P15	VSS[93]	VSS[190]
P16	VSS[94]	VSS[191]
P24	VSS[95]	VSS[192]
P27	VSS[96]	VSS[193]
P27	VSS[97]	VSS[194]



QUANTA COMPUTER

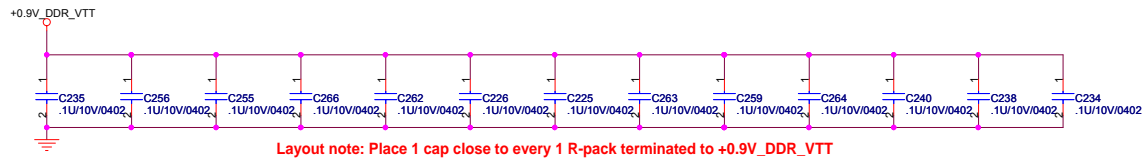
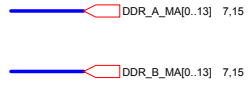
Title: System DRAM Expansion (200P-DDR_SODIMM X 2)

Size: Document Number FM1

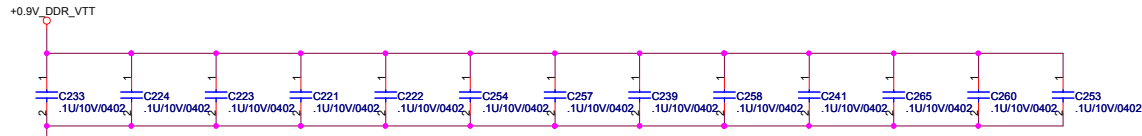
Date: Tuesday, September 06, 2005

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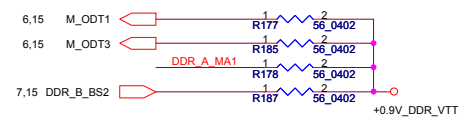
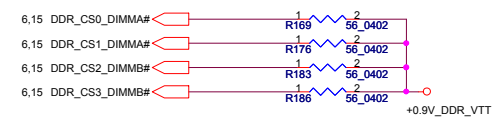
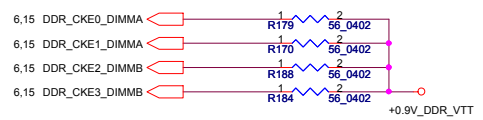
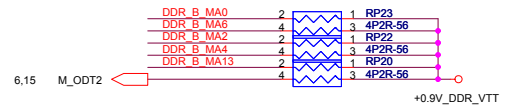
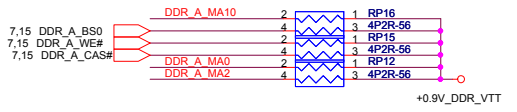
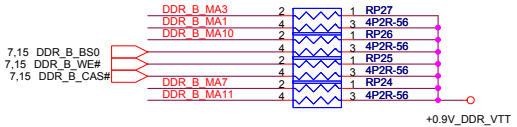
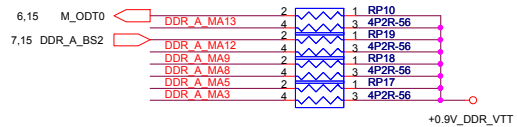
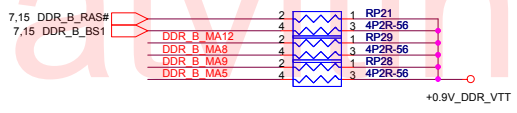
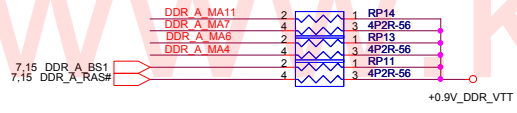
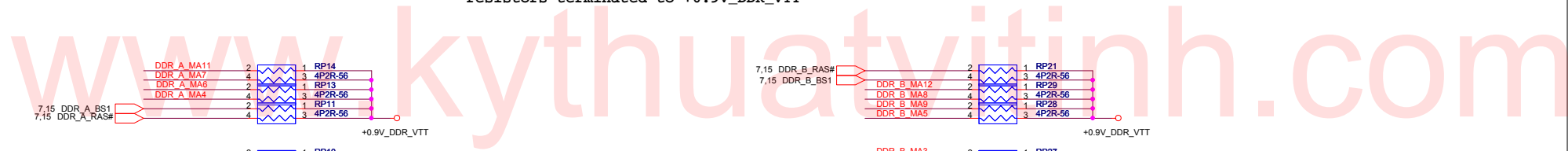


Layout note: Place 1 cap close to every 1 R-pack terminated to +0.9V_DDR_VTT



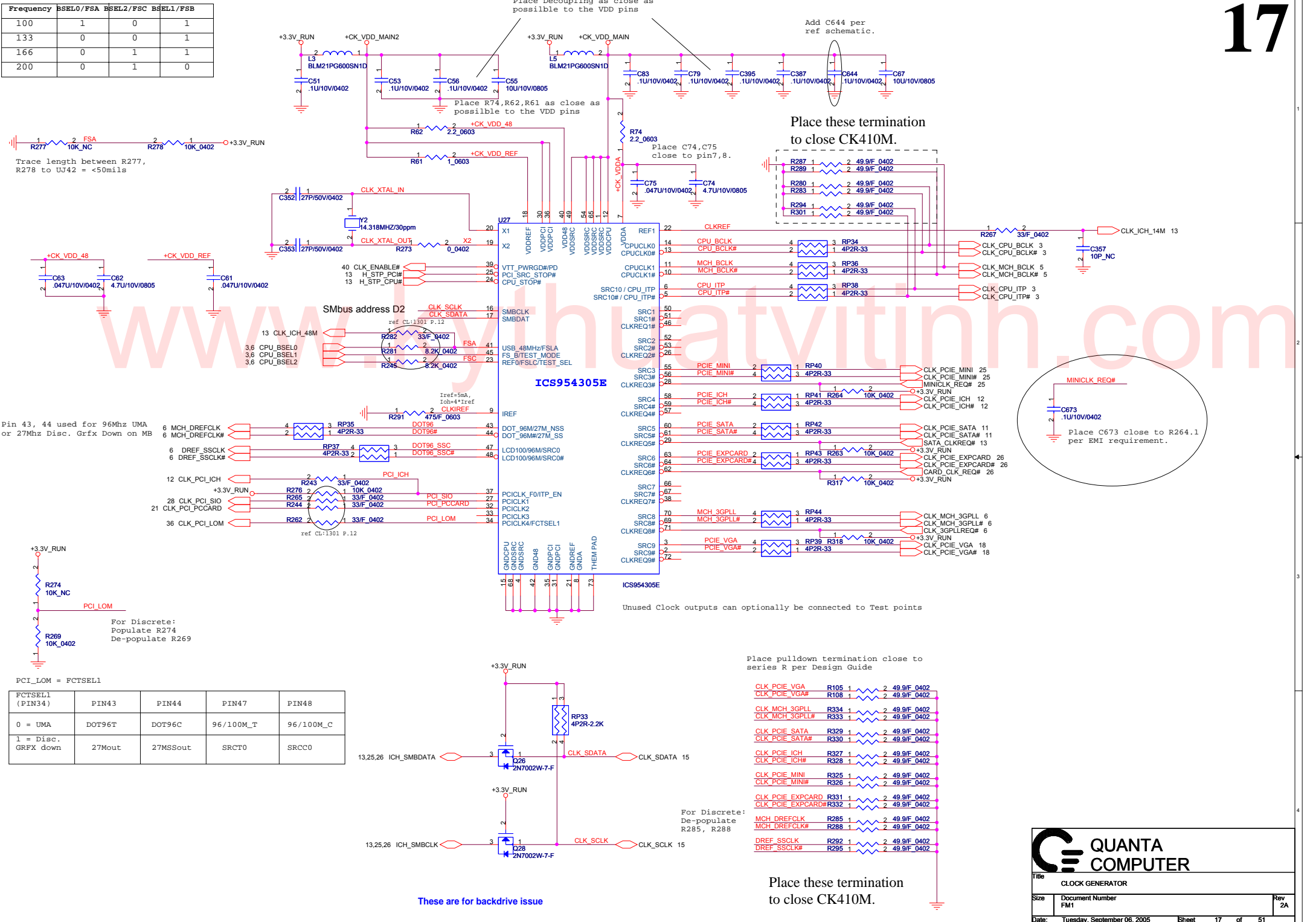
Layout note: Place 1 cap close to every 1 R-pack terminated to +0.9V_DDR_VTT

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V_DDR_VTT



Frequency	bSEL0/FSA	bSEL2/FSC	bSEL1/FSB
100	1	0	1
133	0	0	1
166	0	1	1
200	0	1	0

Trace length between R277, R278 to UJ42 = <50mils

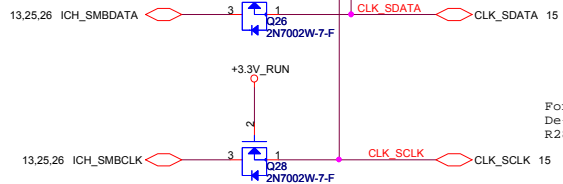


Pin 43, 44 used for 96Mhz UMA or 27Mhz Disc. Gfx Down on MB

For Discrete: Populate R274 De-populate R269

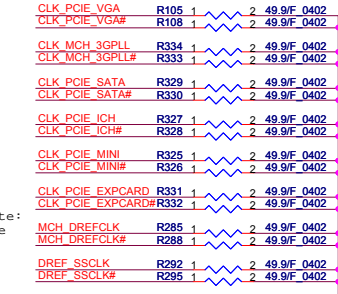
PCI_LOM = FCTSEL1

FCTSEL1 (PIN34)	PIN43	PIN44	PIN47	PIN48
0 = UMA	DOT96T	DOT96C	96/100M_T	96/100M_C
1 = Disc. GFRX down	27Mout	27MSSout	SRCT0	SRCC0



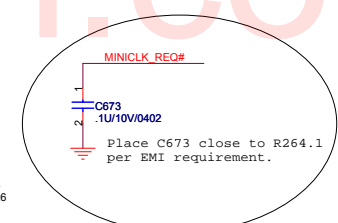
These are for backdrive issue

Place pull-down termination close to series R per Design Guide



For Discrete: De-populate R285, R288

Place these termination to close CK410M.

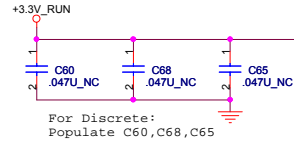


Place C673 close to R264.1 per EMI requirement.

**QUANTA
COMPUTER**

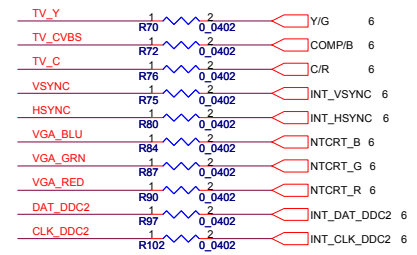
Title: CLOCK GENERATOR		
Size: FM1	Document Number: FM1	Rev: 2A
Date: Tuesday, September 06, 2005	Sheet: 17	of 51

Populate JVD01 for discrete. YPRPB_DET: SIGNAL FROM SVIDEO CONNECTOR, TO SWITCH TO COMPONENT OUT.

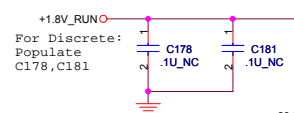
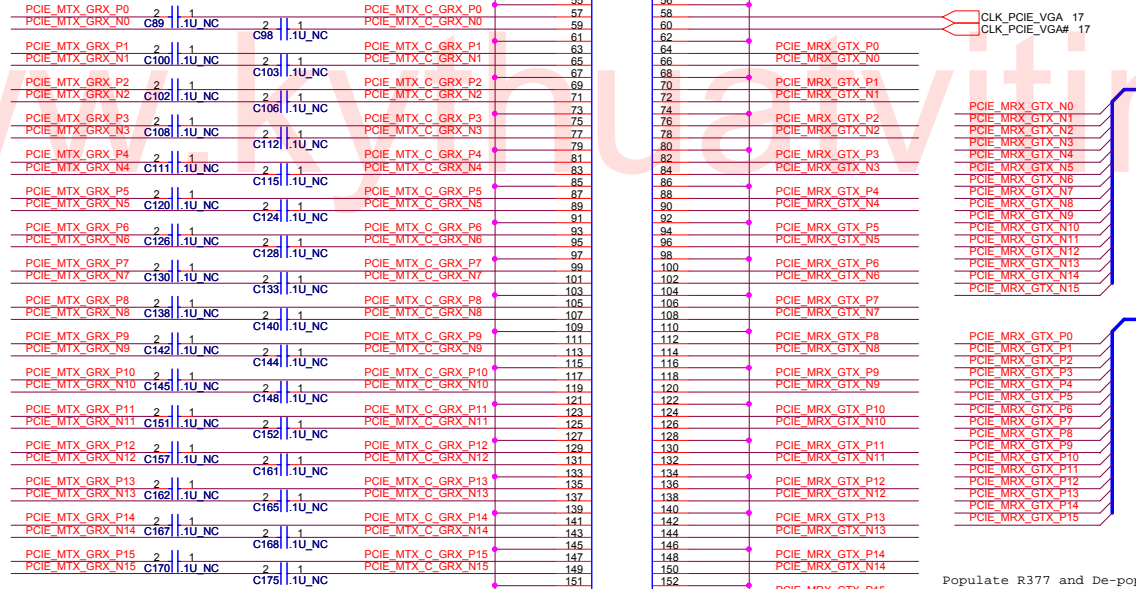
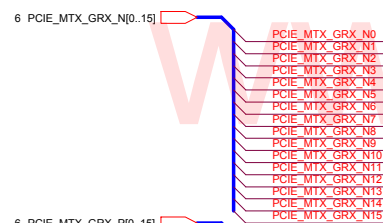


For Discrete: Populate C89,C98,C100,C103,C102,C106,C108,C112, C111,C115,C120,C124,C126,C128,C130,C133, C138,C140,C142,C144,C145,C148,C151,C152, C157,C161,C162,C165,C167,C168,C170,C175

Delete R236,R247 pre ref schematic.



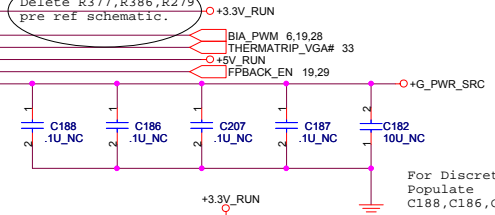
For Discrete: De-populate R70,R72,R76,R75,R80,R84,R87,R90,R97,R02



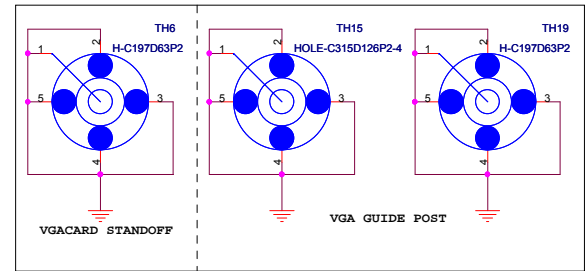
For Discrete: Populate C178,C181

Delete R377,R386,R279 pre ref schematic.

Populate R377 and De-populate R386, R279. for Protol build(old VGA card)



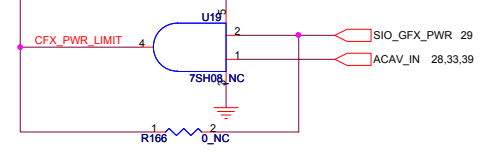
For Discrete: Populate C188,C186,C207,C187,C182,U19



For Discrete: Populate TH6,TH15,TH19

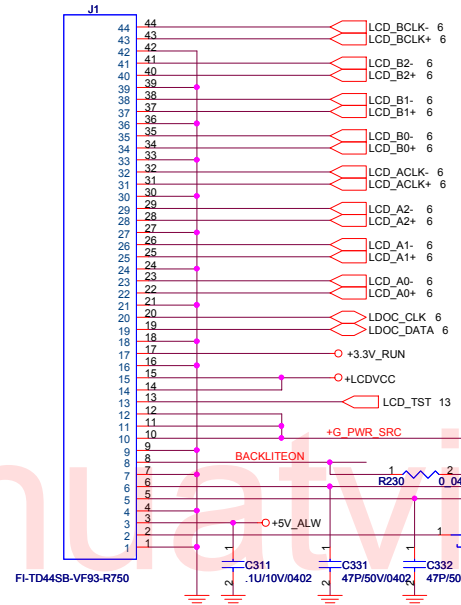
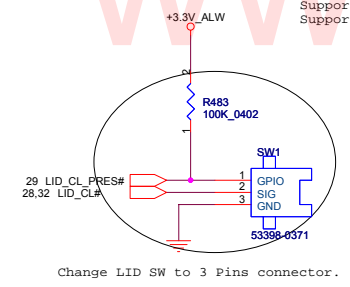
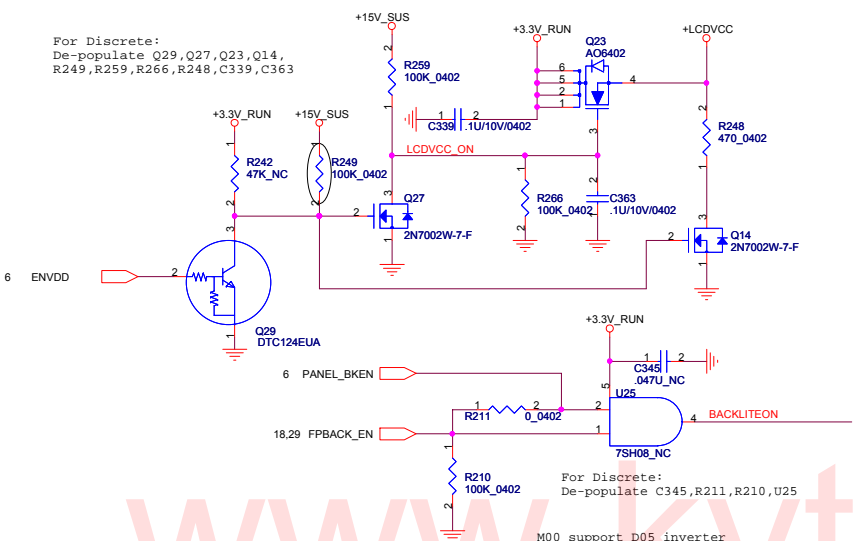
TOP Side

HONDA LFP-SC200SMYGA*_NC

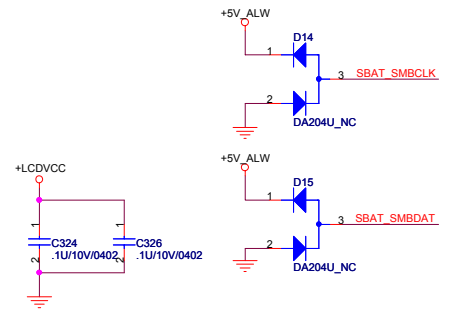


QUANTA COMPUTER logo and title block containing: Title: DDR RES.ARRAY, Size: FM1, Document Number: FM1, Rev: 2A, Date: Tuesday, September 06, 2005, Sheet: 18 of 51

For Discrete:
De-populate Q29, Q27, Q23, Q14,
R249, R259, R266, R248, C339, C363

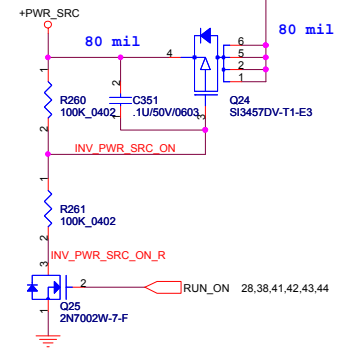


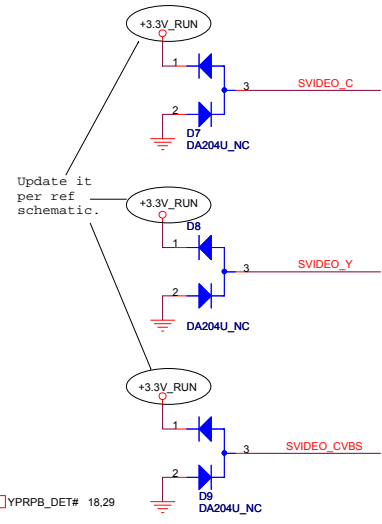
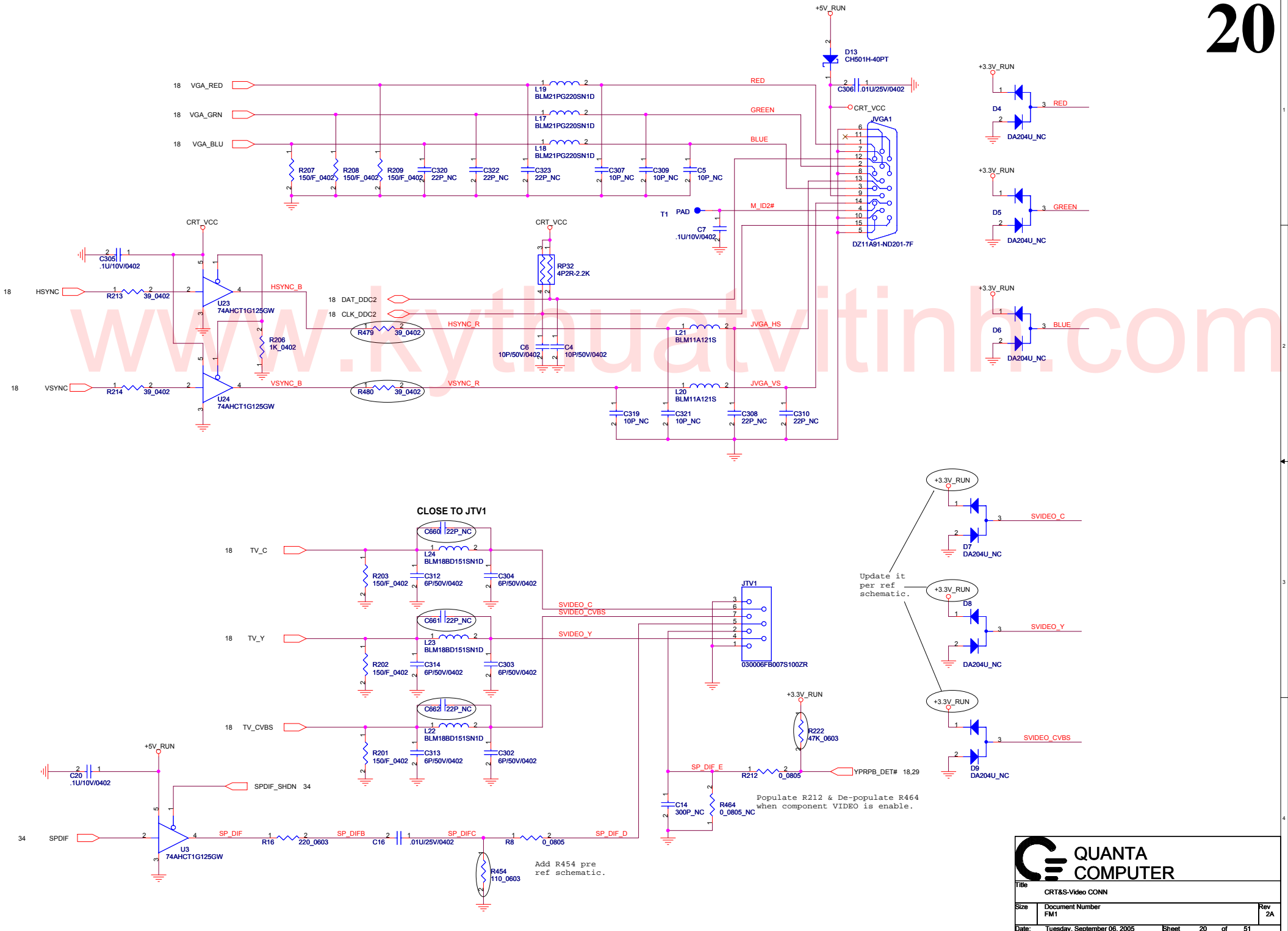
For Discrete:
De-populate J1, R230, C311, C331, C332, D16, C333, C329, C341, C324, C326



Adress : A9H --Contrast
AAH --Backlight

M'07 inverter support - De-populate D16.
D'05 inverter support - Populate D16

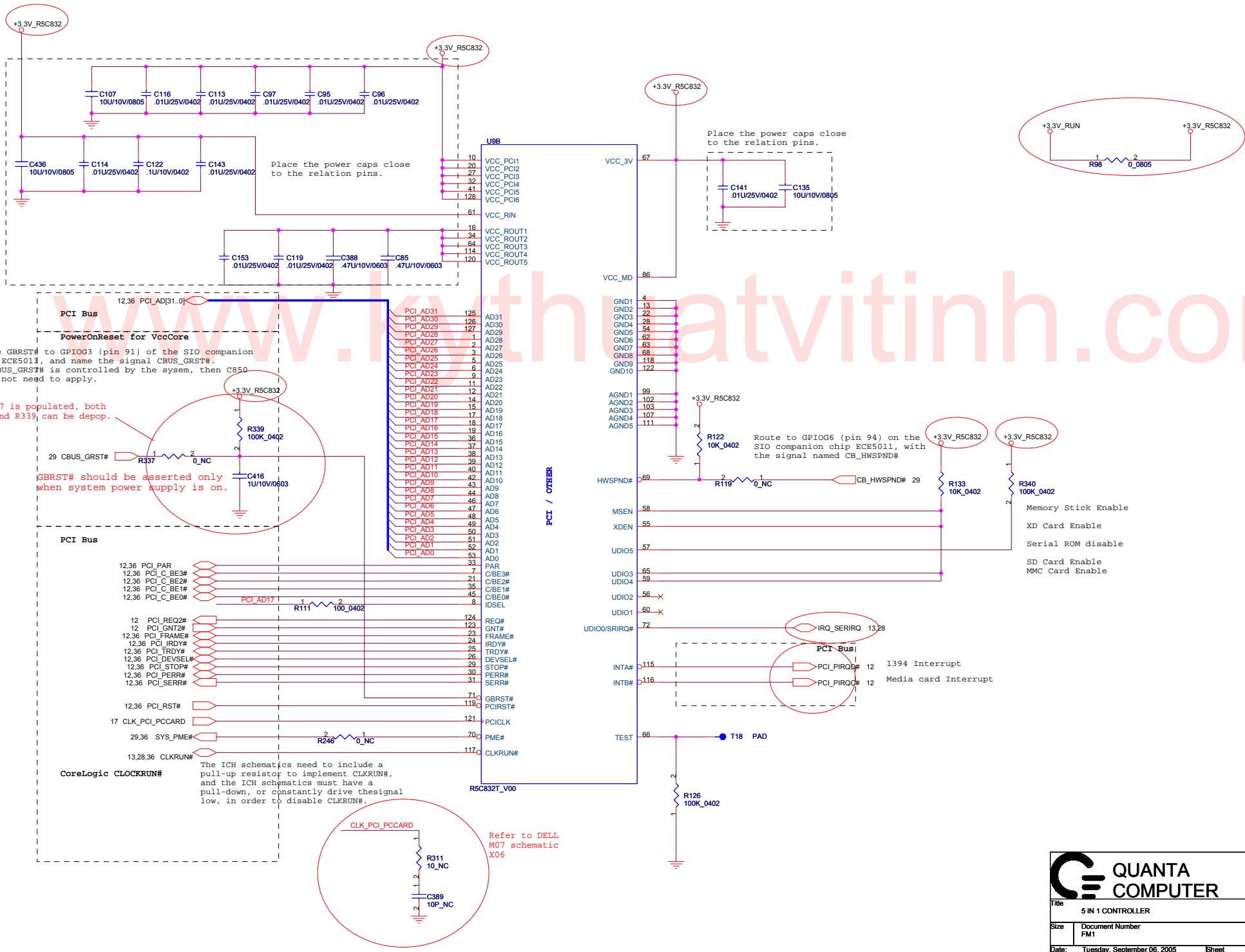




Update it per ref schematic.

Populate R212 & De-populate R464 when component VIDEO is enable.

Add R454 pre ref schematic.



Route GBRST# to GPIO3 (pin 91) of the SIO companion chip ECE5011, and name the signal CBUS_GRST#. If CBUS_GRST# is controlled by the system, then C850 does not need to apply.

If R337 is populated, both C416 and R339, can be depop.

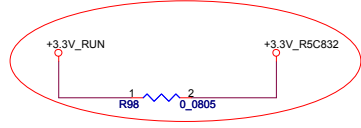
GBRST# should be asserted only when system power supply is on.

The ICH schematics need to include a pull-up resistor to implement CLKRUN#, and the ICH schematics must have a pull-down, or constantly drive the signal low, in order to disable CLKRUN#.

Place the power caps close to the relation pins.

Route to GPIO6 (pin 94) on the SIO companion chip ECE5011, with the signal named CB_HWSPND#

Refer to DELL M07 schematic X06

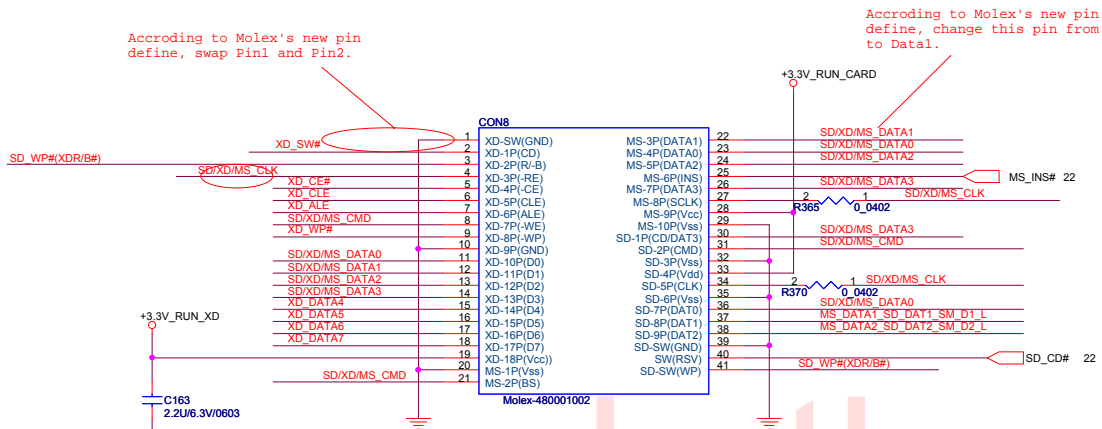


QUANTA COMPUTER

Title: 5 IN 1 CONTROLLER

Size	Document Number	Rev
	FM1	2A

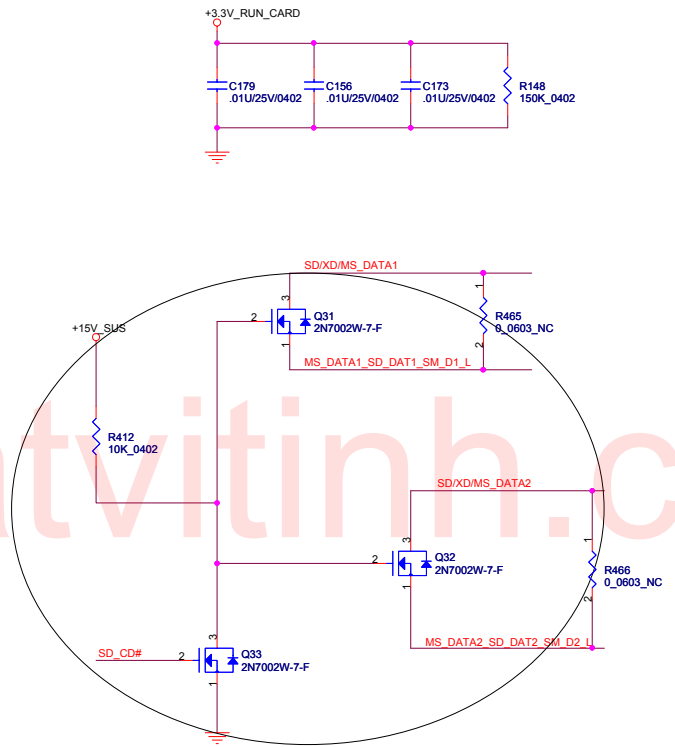
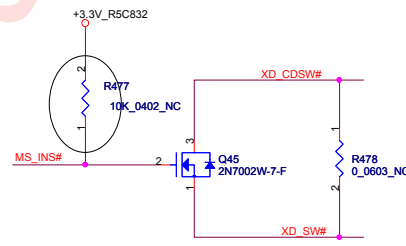
Date: Tuesday, September 06, 2005 Sheet 21 of 51



5 IN1 CARD READER

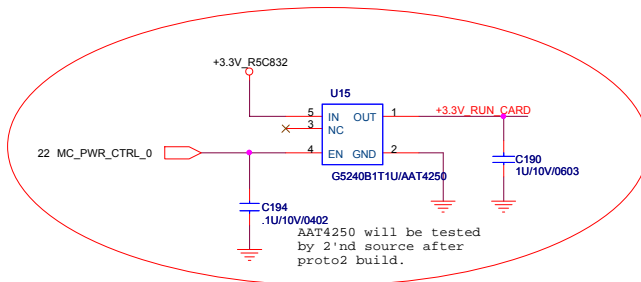
Refer to M07, connect C163 to +3VRUN_XD.

- 22 XD_CDSW#
- 22 SD_WP#(XDR/B#)
- 22 XD_DATA7
- 22 XD_DATA6
- 22 XD_DATA5
- 22 XD_DATA4
- 22 SD_XD/MS_DATA3
- 22 SD_XD/MS_DATA2
- 22 SD_XD/MS_DATA1
- 22 SD_XD/MS_DATA0
- 22 SD_XD/MS_CMD
- 22 XD_WP#
- 22 XD_ALE
- 22 XD_CLE
- 22 XD_CE#
- 22 SD_XD/MS_CLK

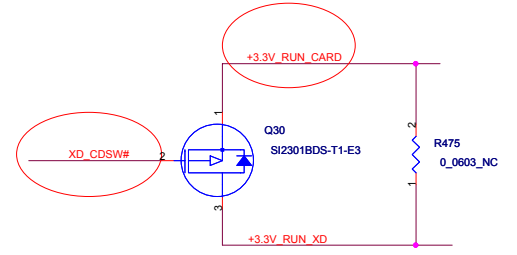


For SD/MS power

For XD power



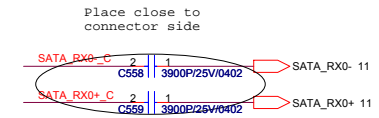
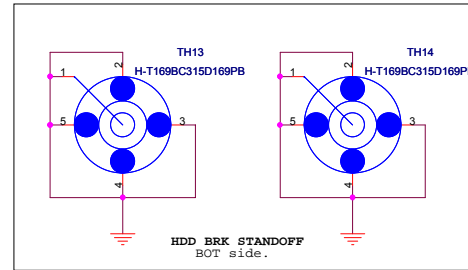
AAT4250 will be tested by 2'nd source after proto2 build.



QUANTA COMPUTER

Title: CARD READER CONN

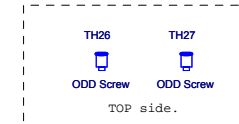
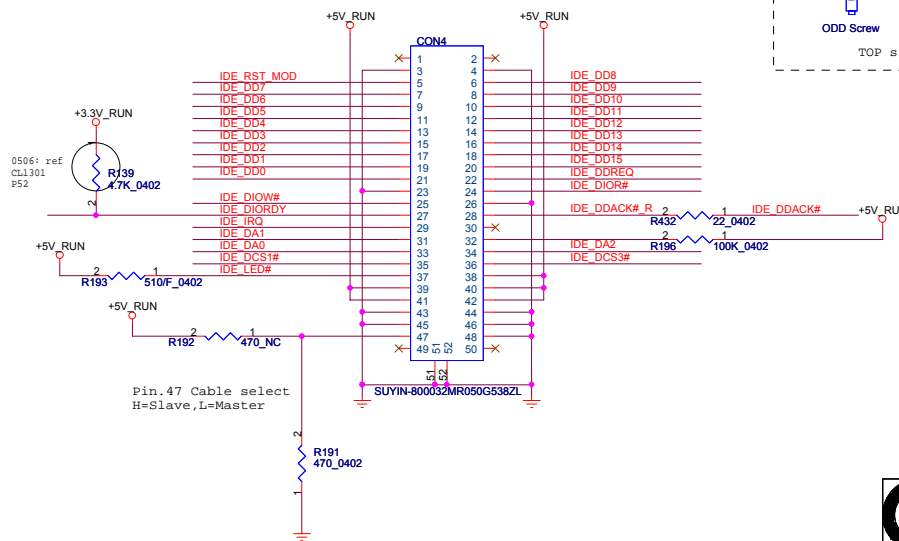
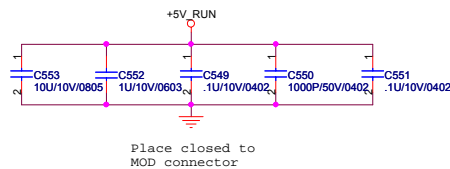
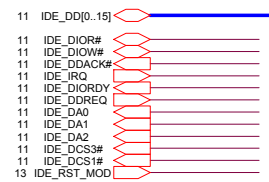
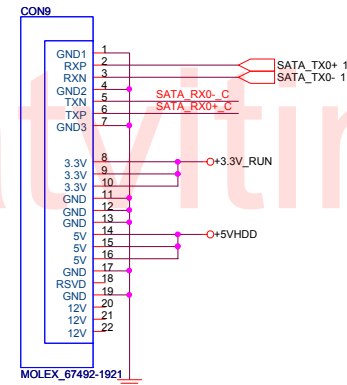
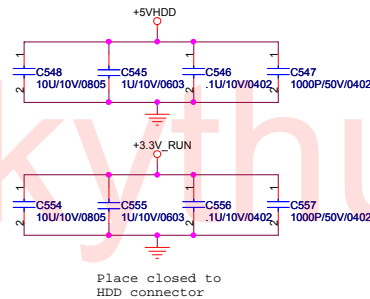
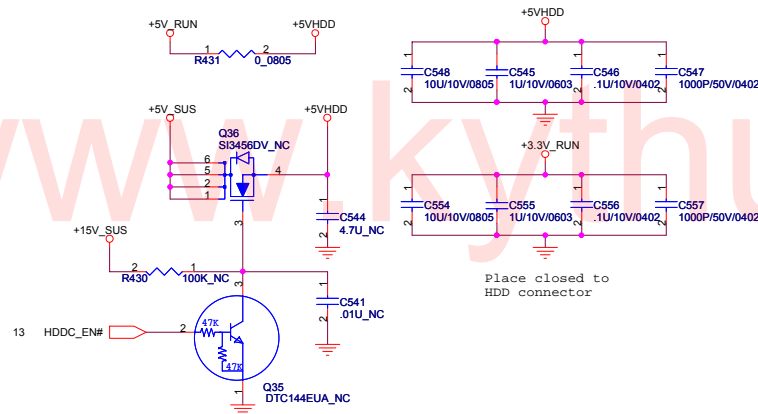
Size: CM1	Document Number: CM1	Rev: 2A
Date: Tuesday, September 06, 2005	Sheet: 23	of 51



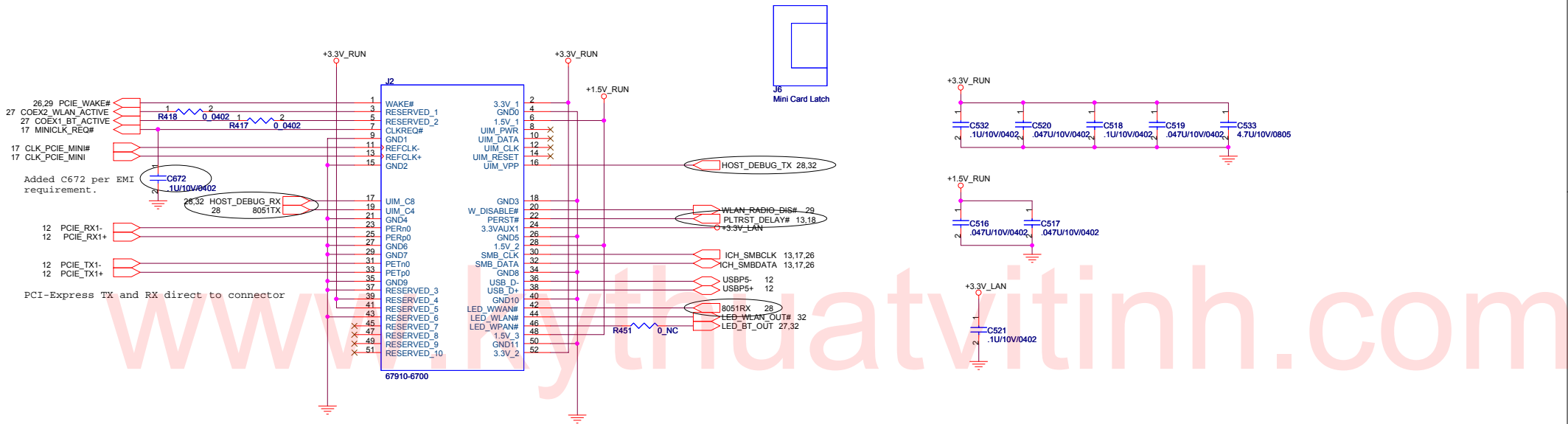
Locate caps C558, C559 near HDD Conn.
Length match SATA_C_RX0- & SATA_C_RX0+ within 20mils.

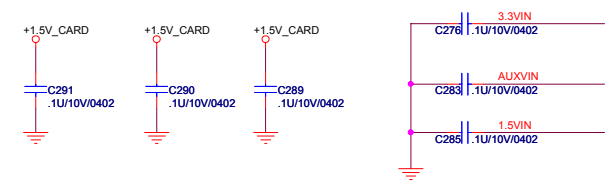
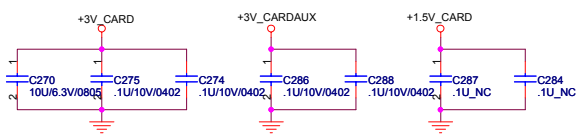
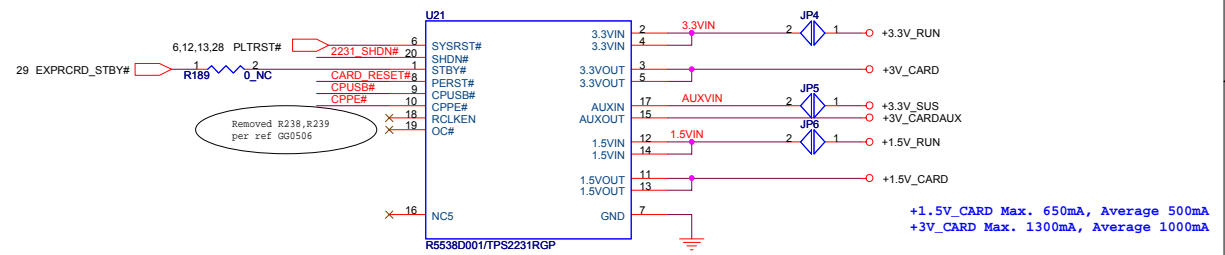
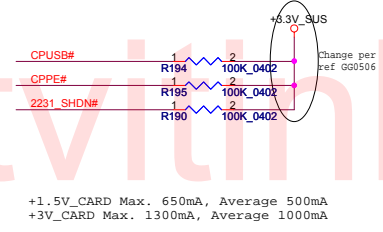
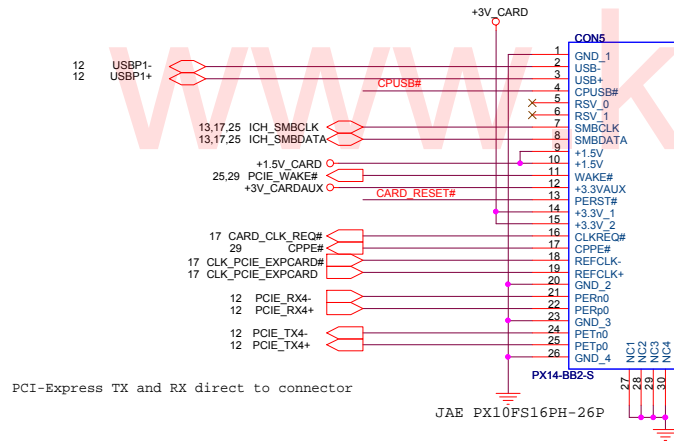
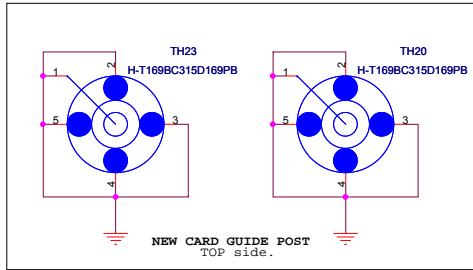
SATA drive vendors will use only 5V supply from the system and will derive 3.3V on the drive. If drive power goals are not achieved, drive vendors will use both 5V and 3.3V supplies from the system. Initial power saving using 3.3V from system is less than 5%.

Power Estimate:
SATA drive power consumption estimate at MobileMark is 1.1W. An additional 150mW can be saved using Intel's IMST driver.



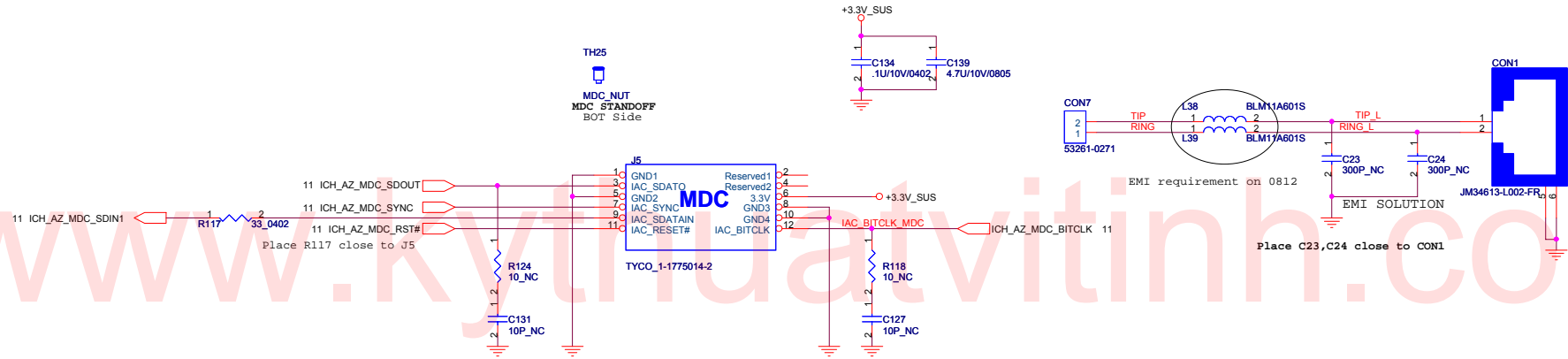
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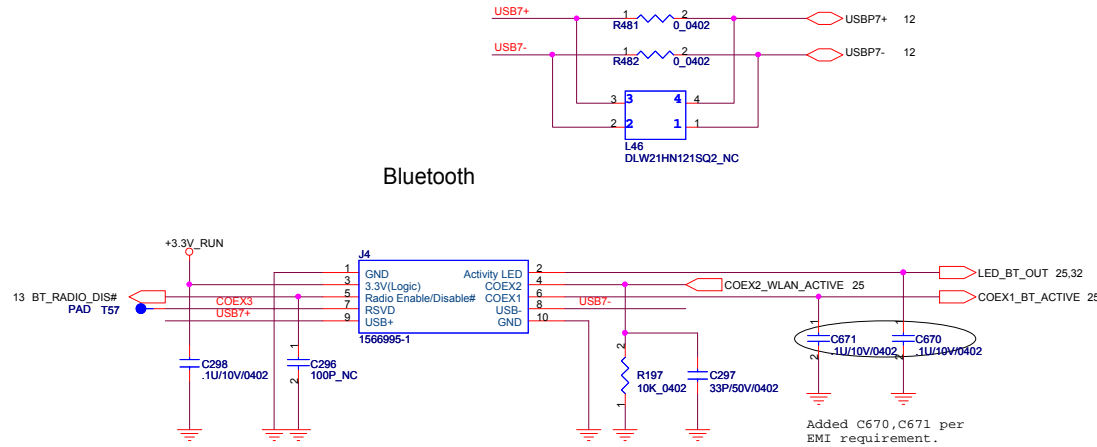


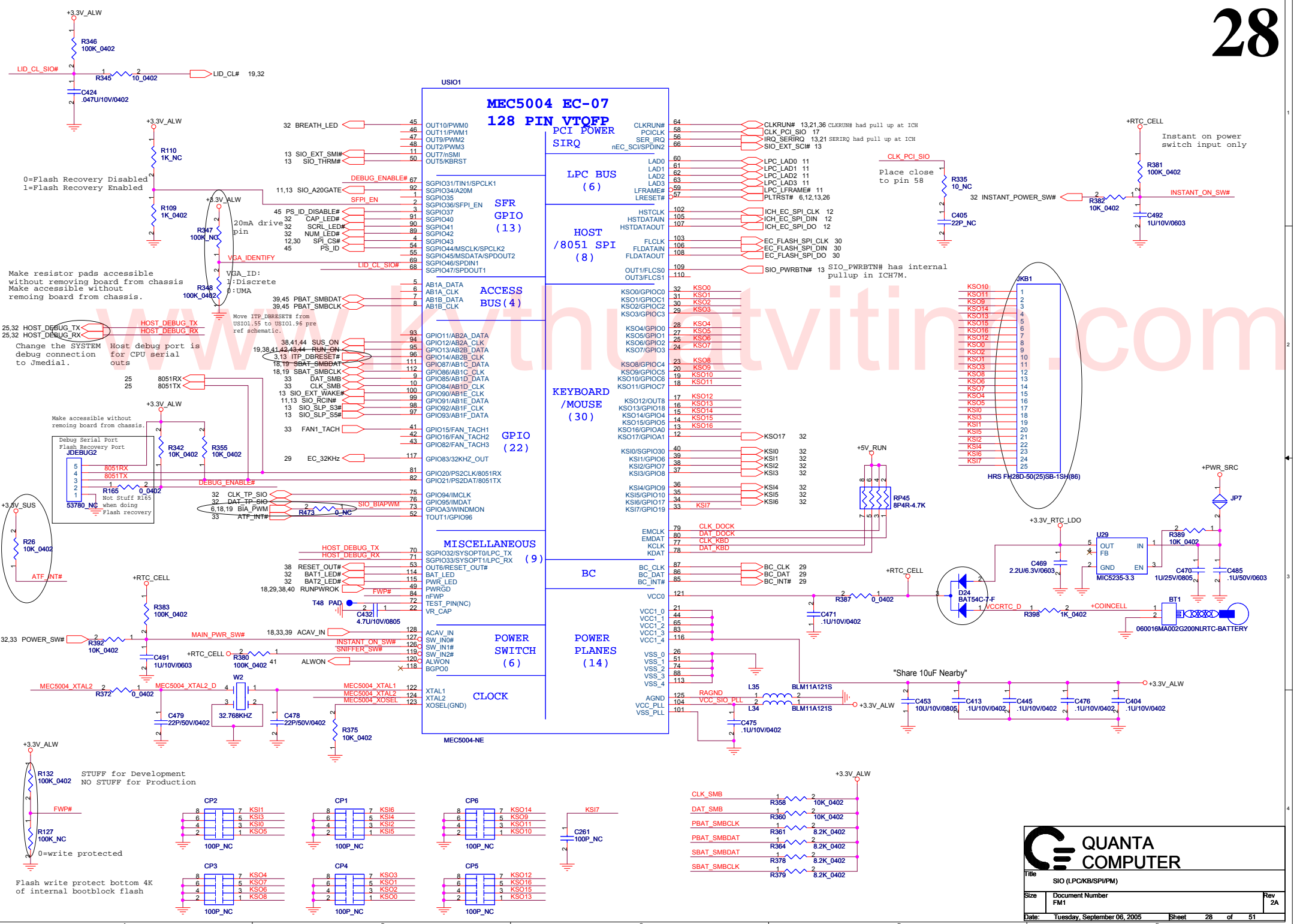
MDC Layout Notes

1. Tip and Ring trace width = 25 mils
2. Spacing between Tip and Ring = 25 mils
3. Tip and Ring connector pitch = 25 mils
4. Keep out area from Tip and Ring to other signals = 100 mils
5. Power and Ground minimum trace width to connector = 20 mils
6. Route Tip and Ring on one layer only (top or bottom)
7. Modem internal cable wire size = 26 AWG (stranded or twisted pair wire)



Bluetooth





MEC5004 EC-07
128 PIN VTOFP
PCI POWER SIRQ

LPC BUS (6)

HOST /8051 SPI (8)

ACCESS BUS (4)

KEYBOARD /MOUSE (30)

GPIO (22)

MISCELLANEOUS (9)

BC

POWER SWITCH (6)

POWER PLANES (14)

CLOCK

0=Flash Recovery Disabled
 1=Flash Recovery Enabled

Make resistor pads accessible without removing board from chassis
 Make accessible without removing board from chassis.

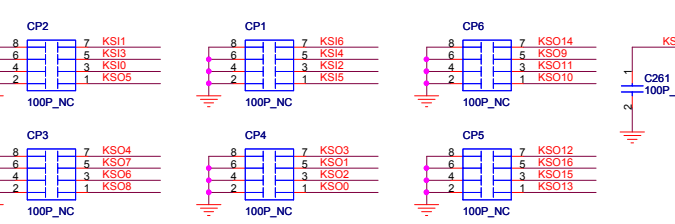
Change the SYSTEM Host debug port is debug connection for CPU serial to Jmedial.

Make accessible without removing board from chassis.

Not Stuff R165 when doing Flash recovery

STUFF for Development
 NO STUFF for Production

Flash write protect bottom 4K of internal bootblock flash

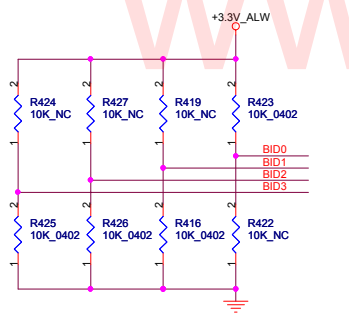
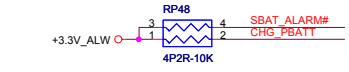
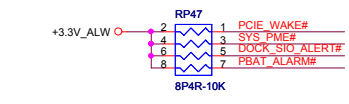


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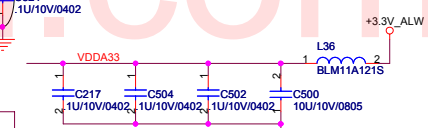
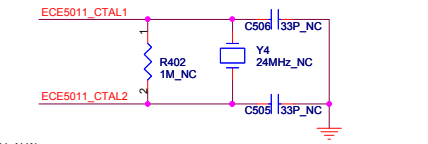
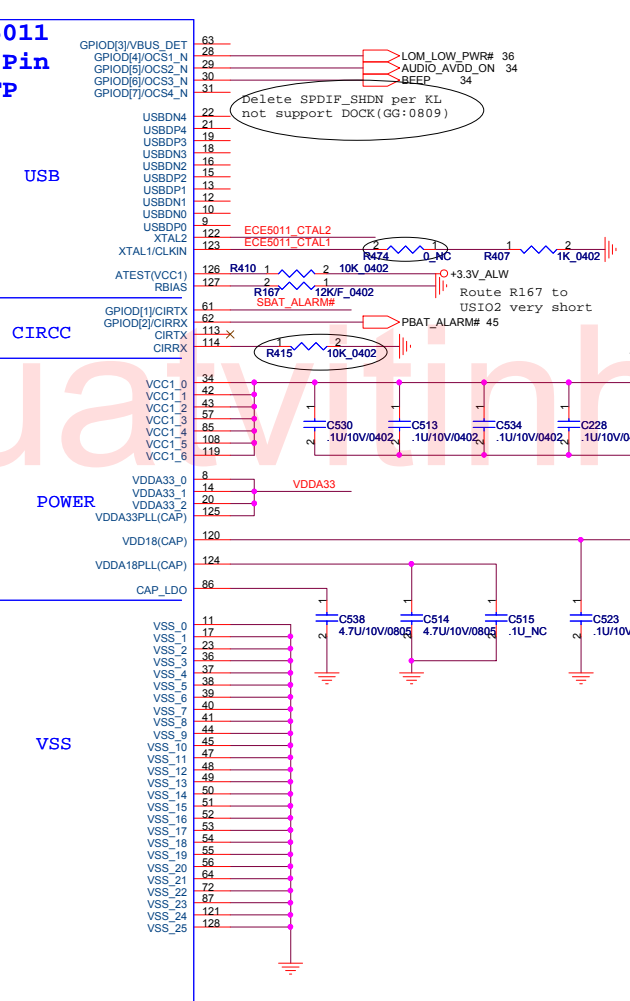
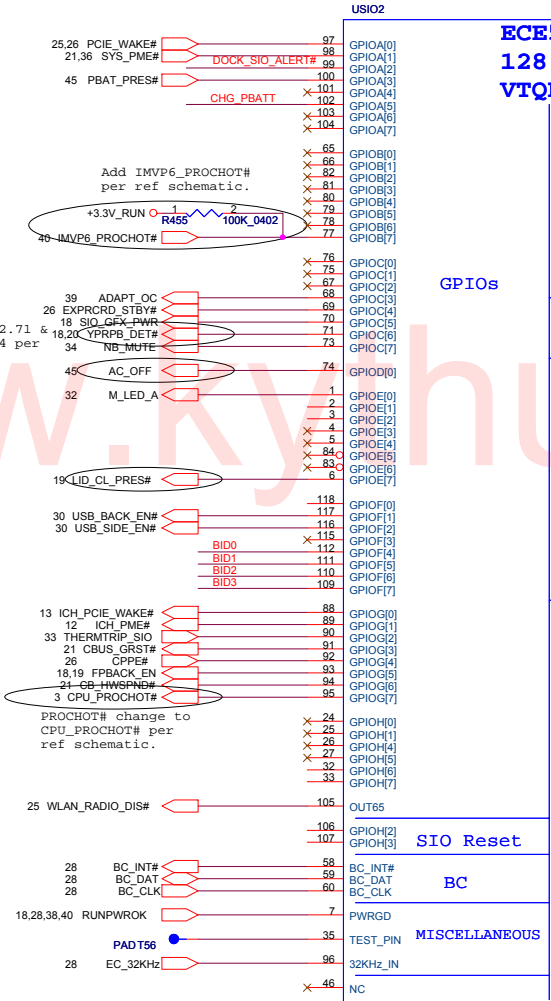
Title: SIO (LPC/KB/SPI/PM)

Size: FM1	Document Number: FM1	Rev: 2A
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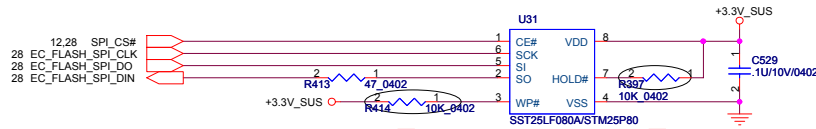
Date: Tuesday, September 06, 2005 Sheet: 28 of 51



BID3	BID2	BID1	BID0	Board Revision
0	0	0	0	PROTO1 (X00)
0	0	0	1	PROTO2 (X01)
0	0	1	0	PROTO3 (X02)
0	0	1	1	QT(X03)
0	1	0	0	A00 PWB/A01 PWA

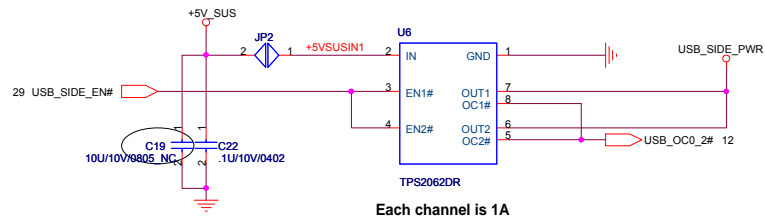


8Mbit (1M Byte), SPI

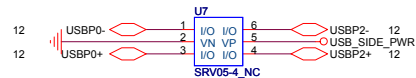
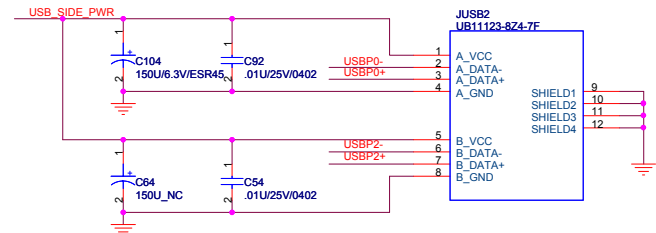


Delete UPW1, C434-436, RP53 per GG0524 item 135.

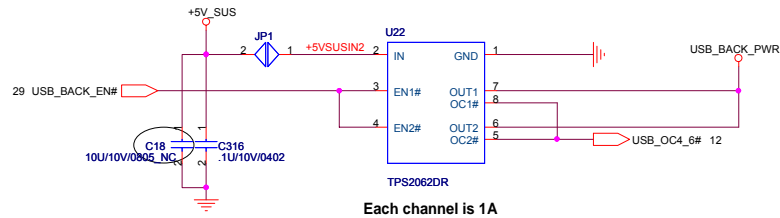
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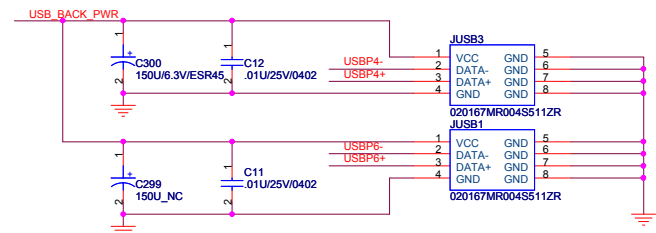
Each channel is 1A

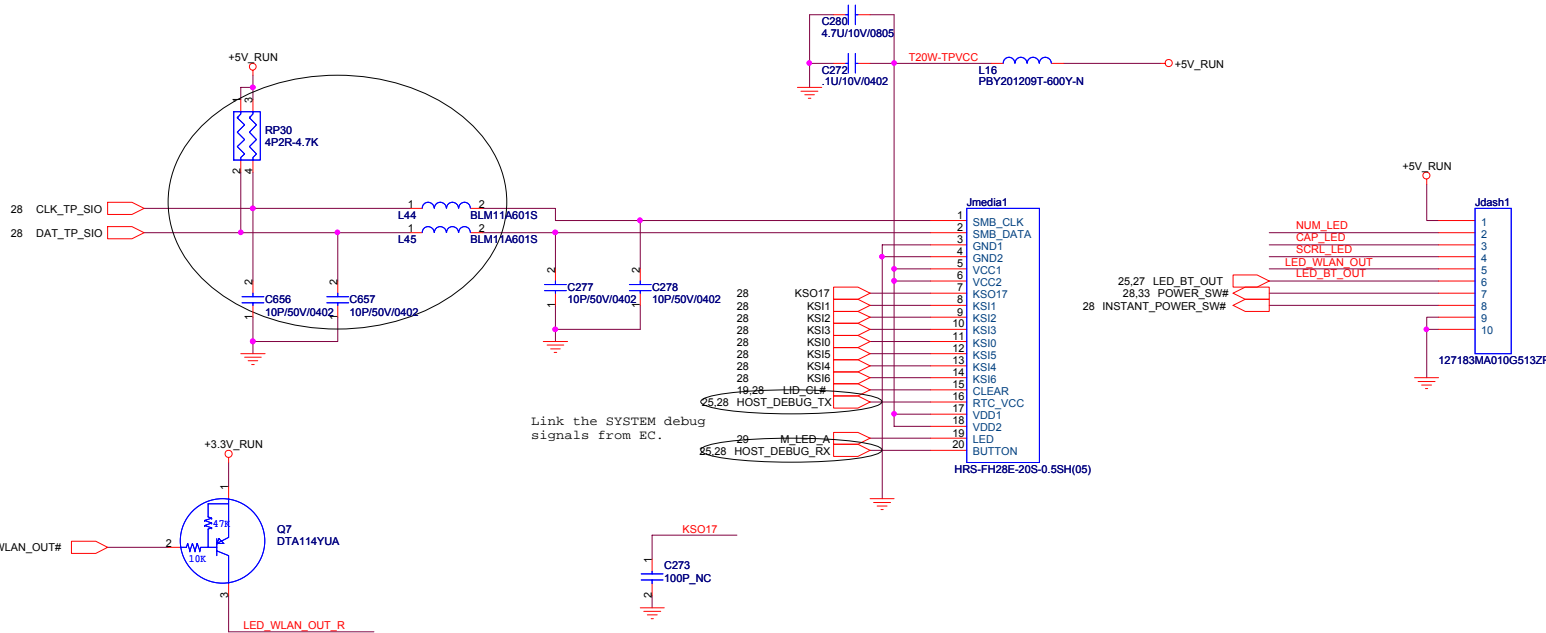
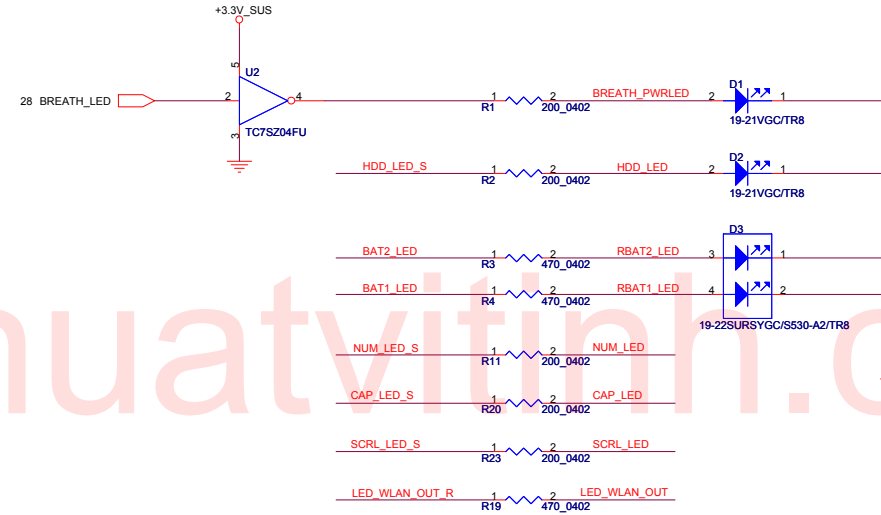
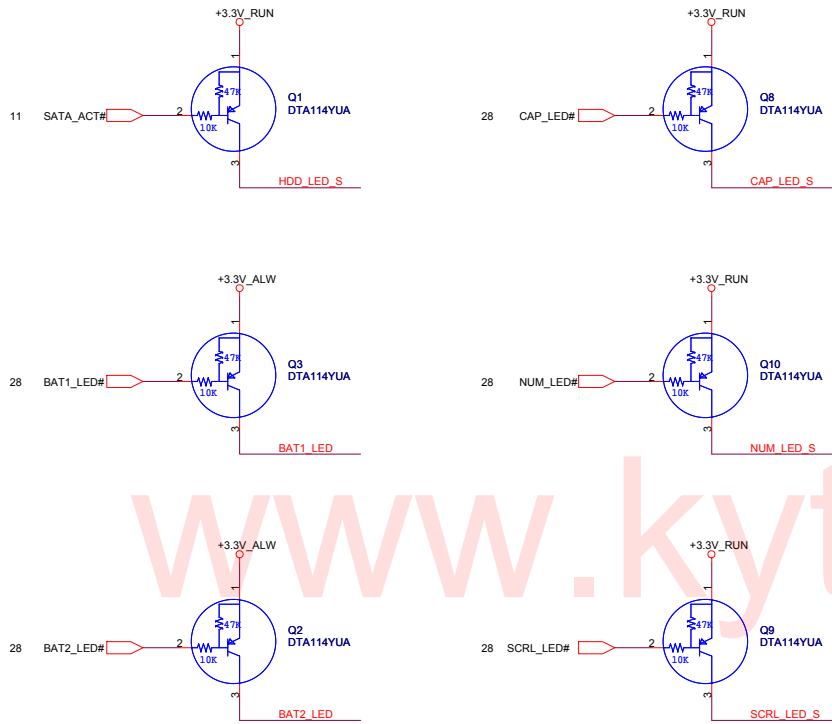


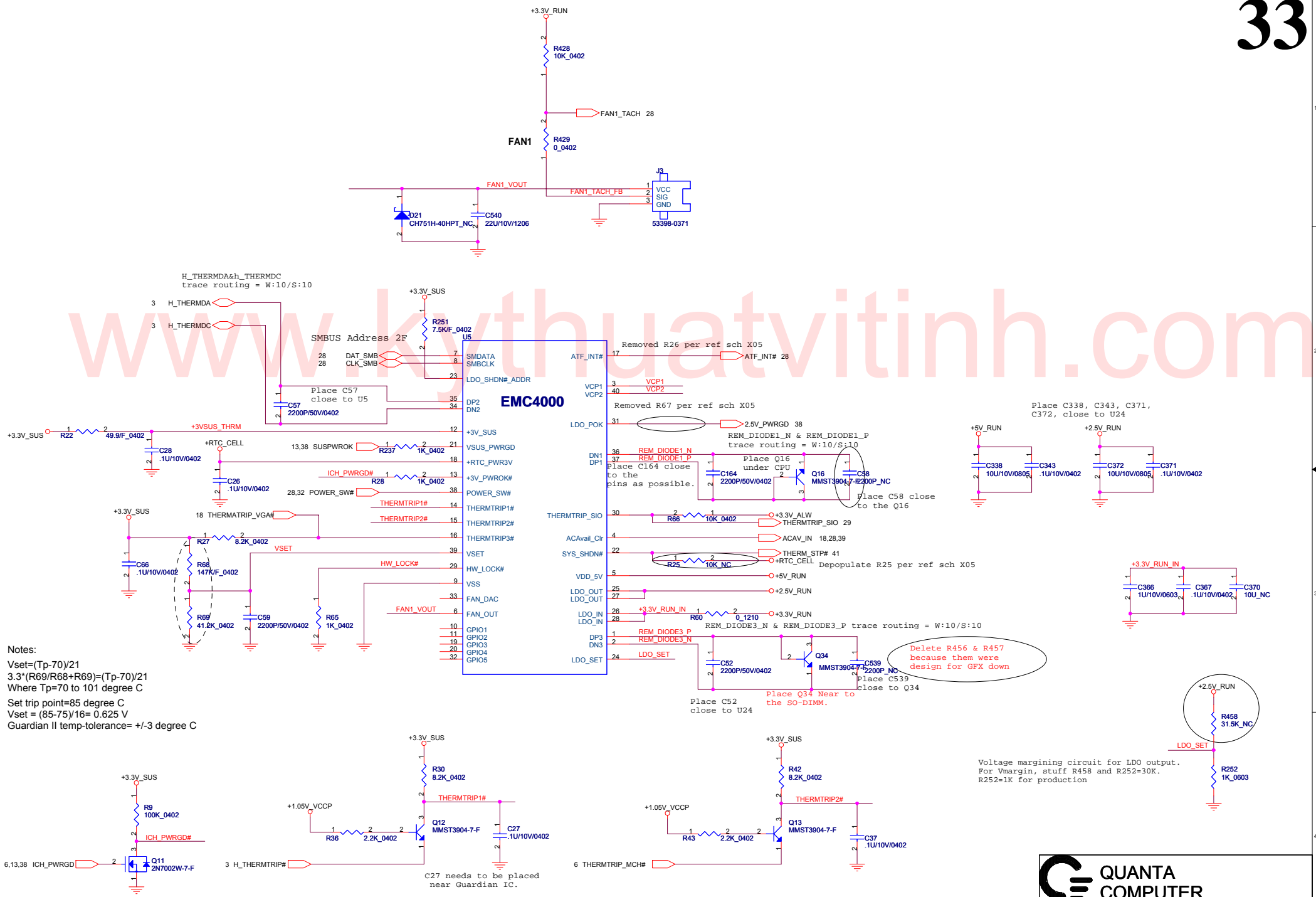
Place ESD diodes as close as possible to USB connector.



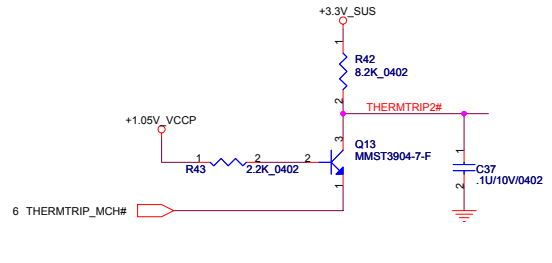
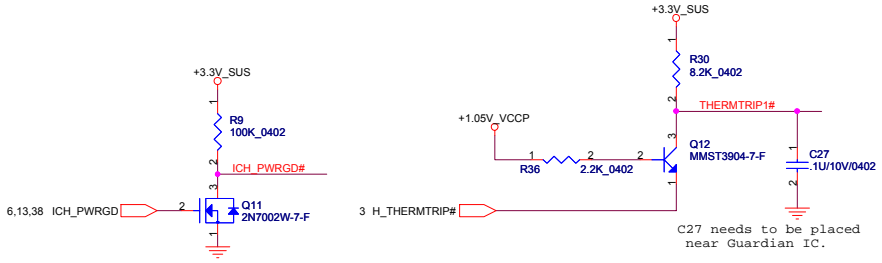
Each channel is 1A



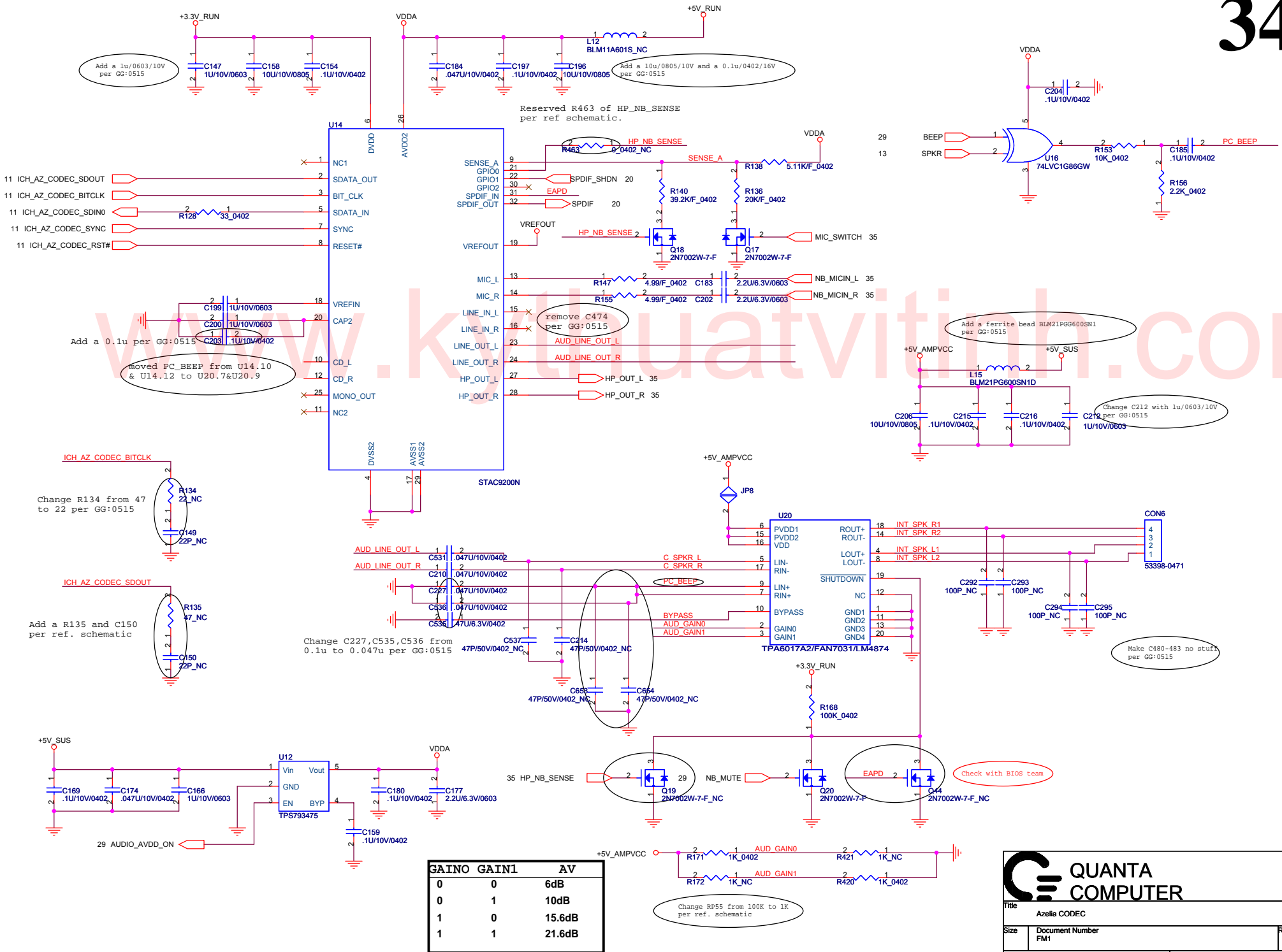




Notes:
 $V_{set} = (T_p - 70) / 21$
 $3.3 \cdot (R_{69} / R_{68} + R_{69}) = (T_p - 70) / 21$
 Where $T_p = 70$ to 101 degree C
 Set trip point = 85 degree C
 $V_{set} = (85 - 75) / 16 = 0.625$ V
 Guardian II temp-tolerance = ± 3 degree C



Voltage margining circuit for LDO output.
 For Vmargin, stuff R458 and R252=30K.
 R252=1K for production



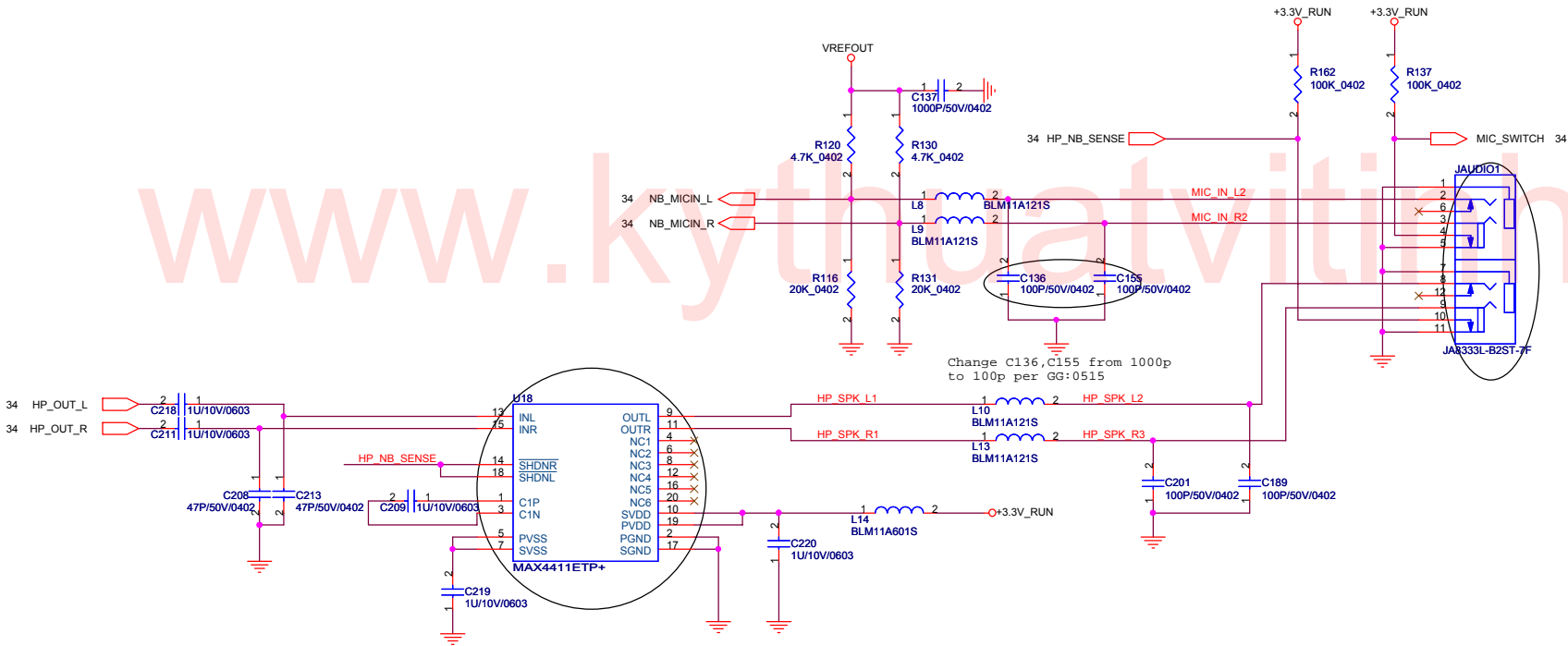
GAIN0	GAIN1	AV
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

QUANTA COMPUTER


Title: Azelia CODEC

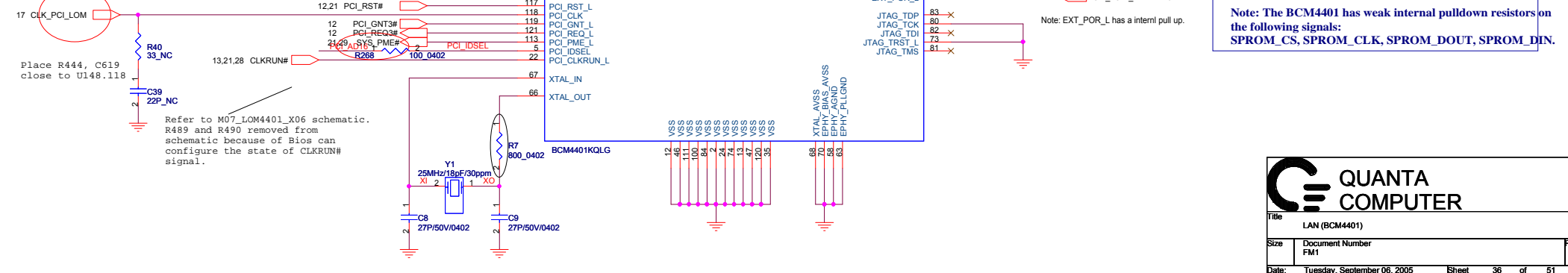
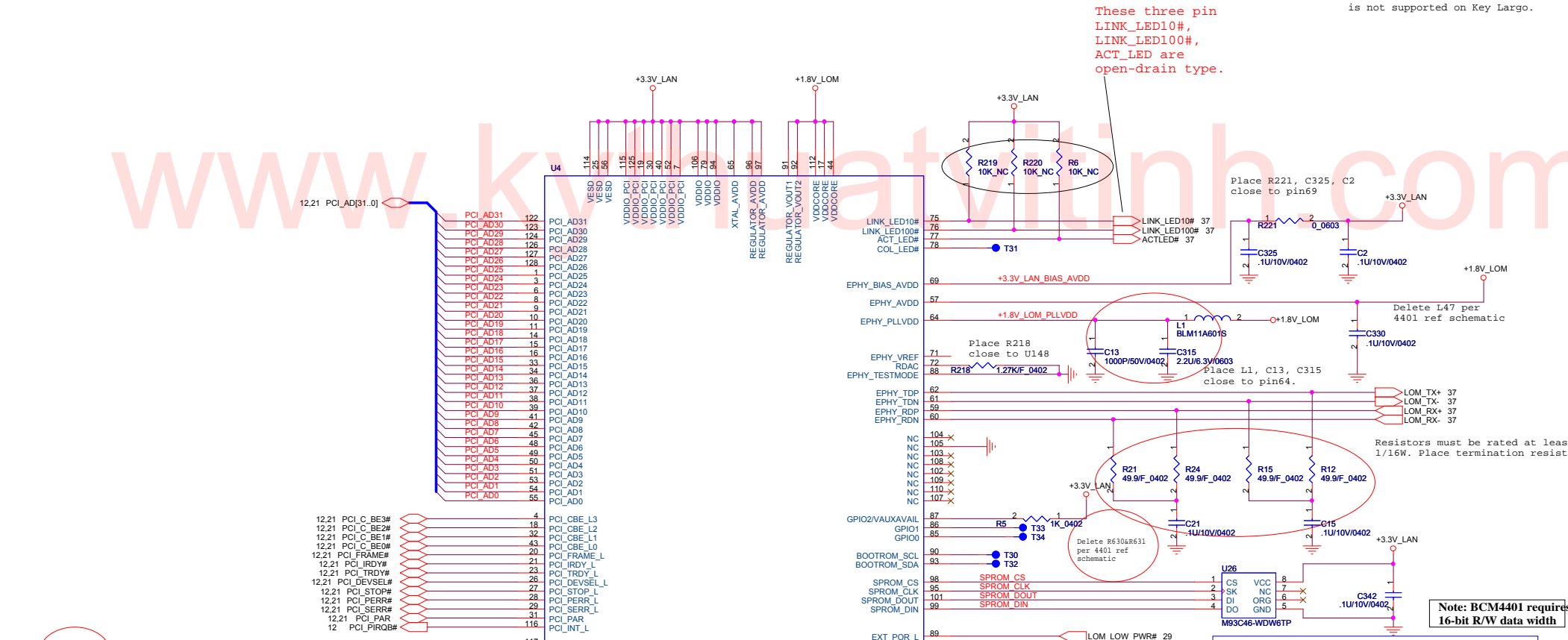
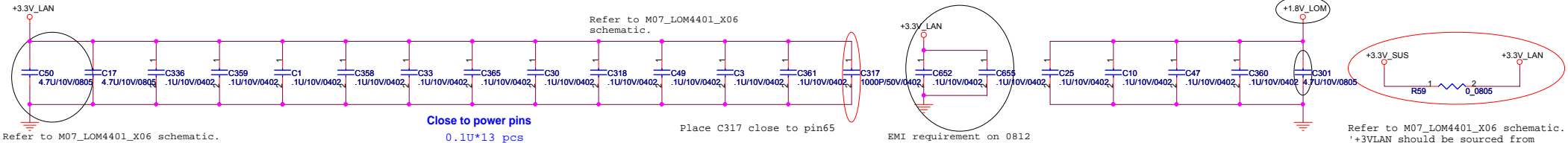
Size: Document Number FM1 Rev 2A

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 QUANTA COMPUTER		
Title: AUDIO CONN		
Size: FM1	Document Number: FM1	Rev: 2A
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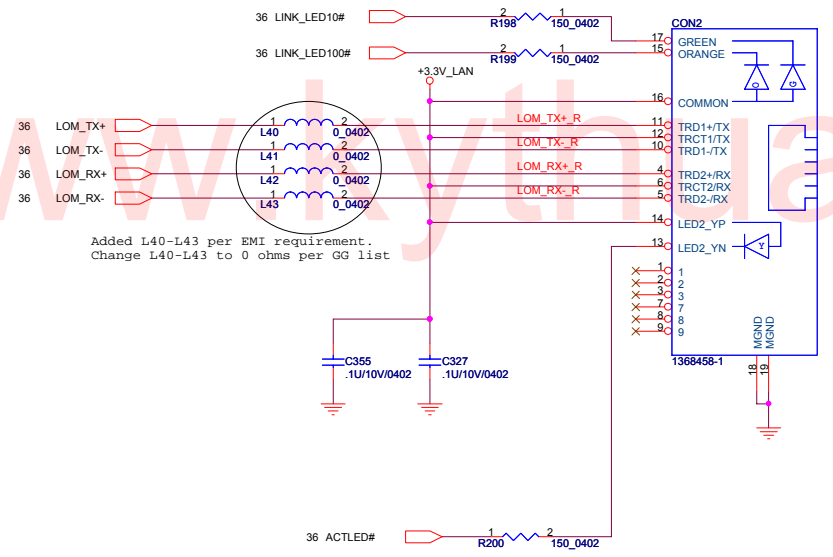
QUANTA COMPUTER

Title: LAN (BCM4401)

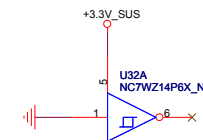
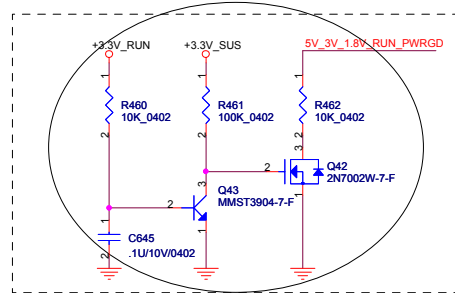
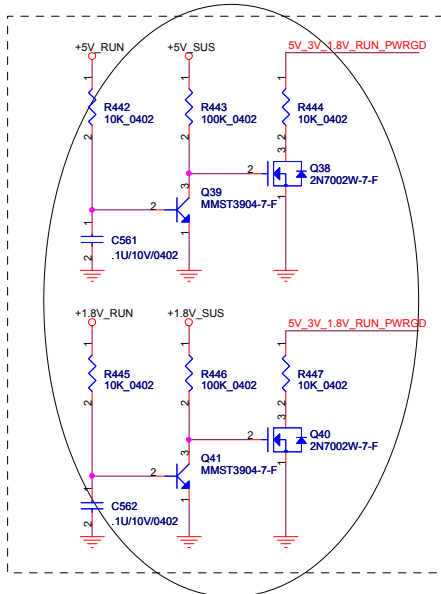
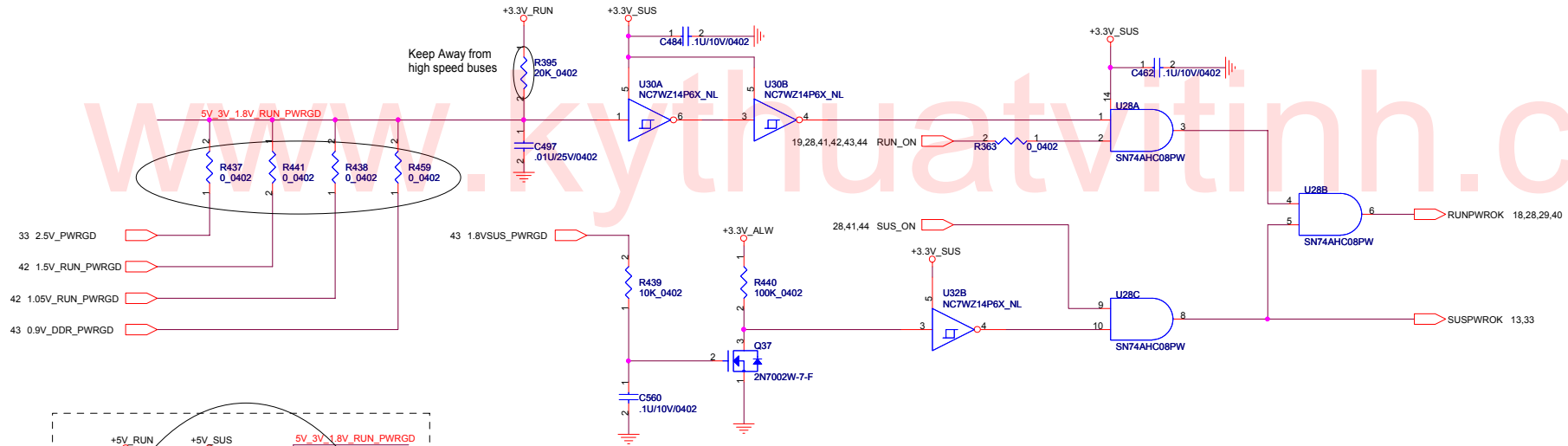
Size: Document Number FM1 Rev 2A

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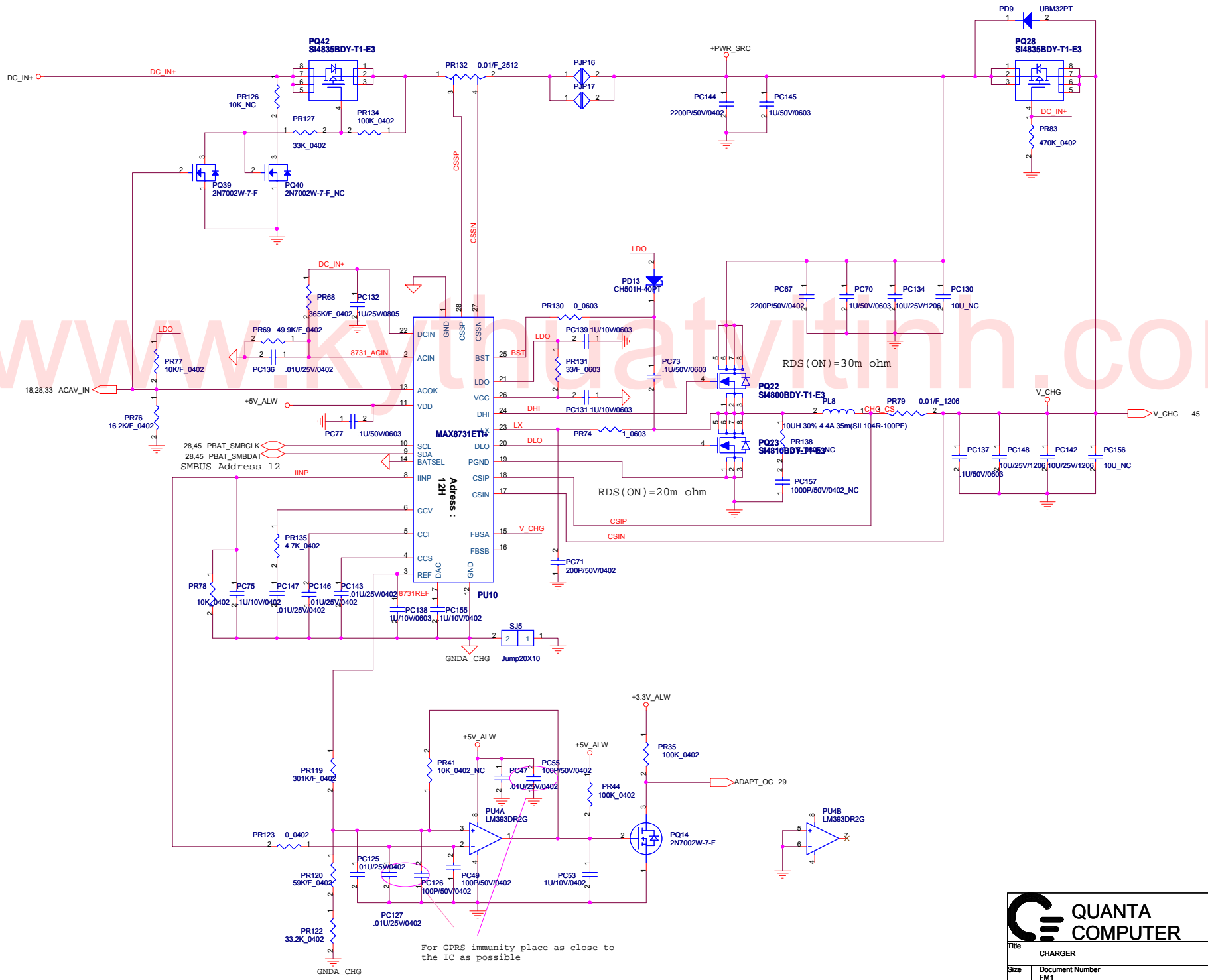
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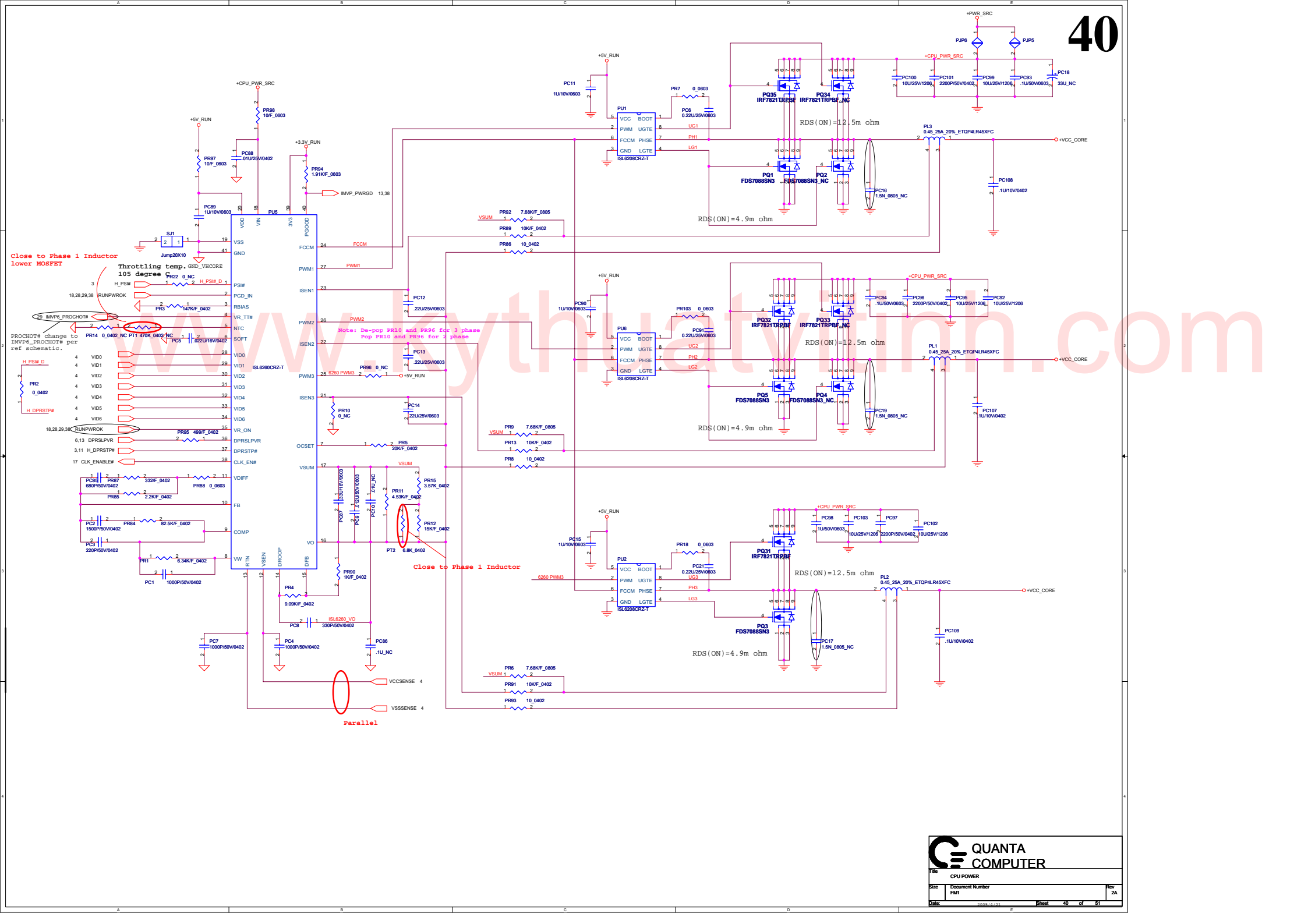
Added L40-L43 per EMI requirement.
Change L40-L43 to 0 ohms per GG list



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Close to Phase 1 Inductor
lower MOSFET

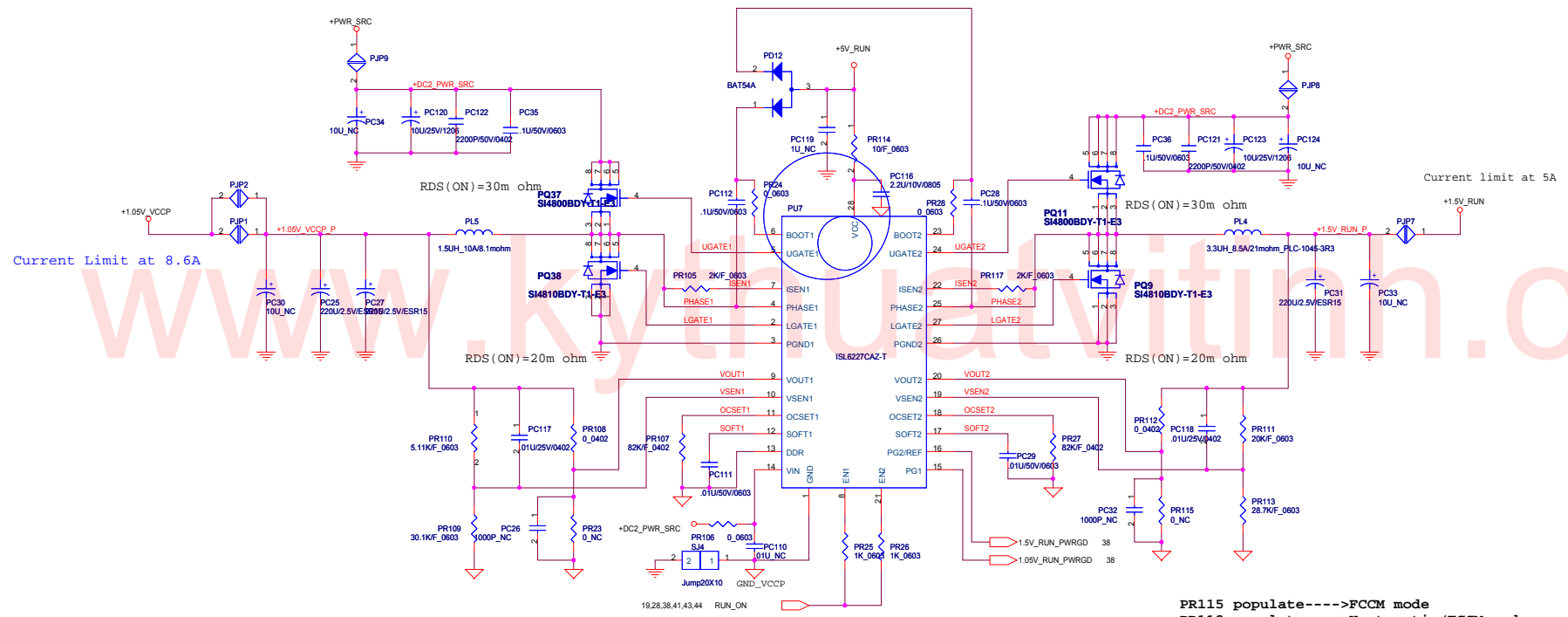
Throttling temp. 105 degree

PROCHOT# change to IMVP6_PROCHOT# per ref schematic.

Note: De-pop PR10 and PR96 for 3 phase
Pop PR10 and PR96 for 2 phase

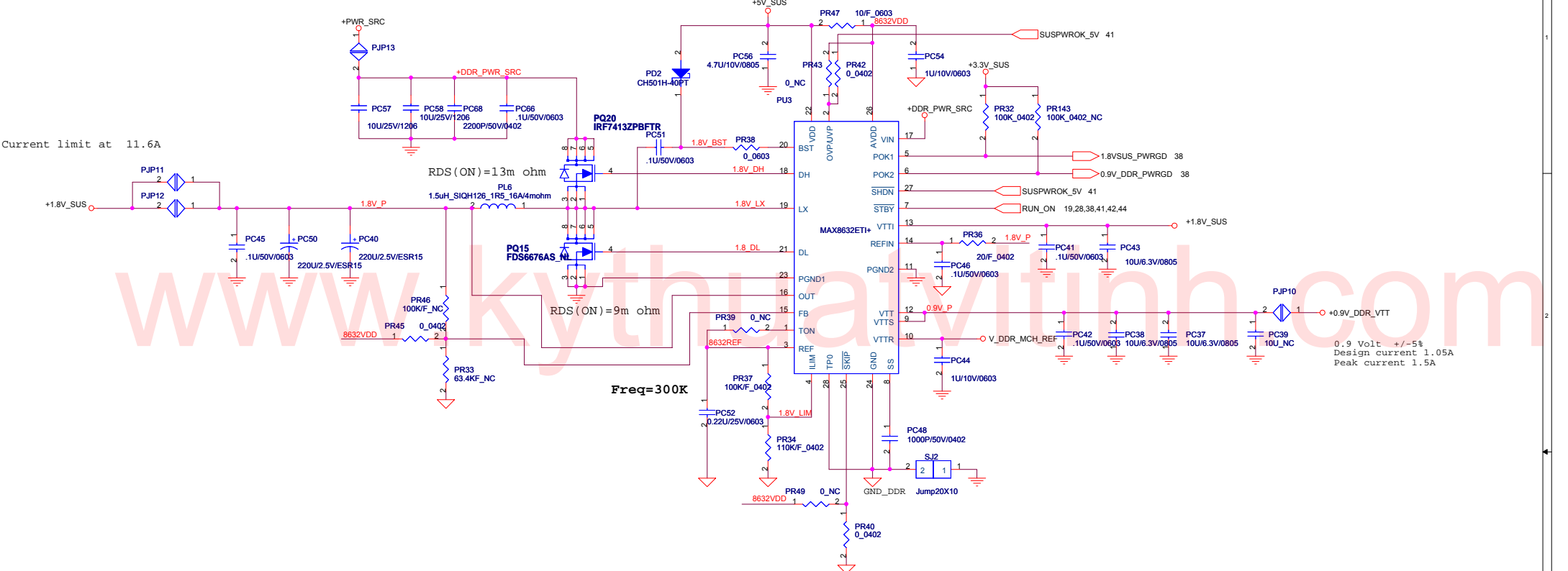
Close to Phase 1 Inductor

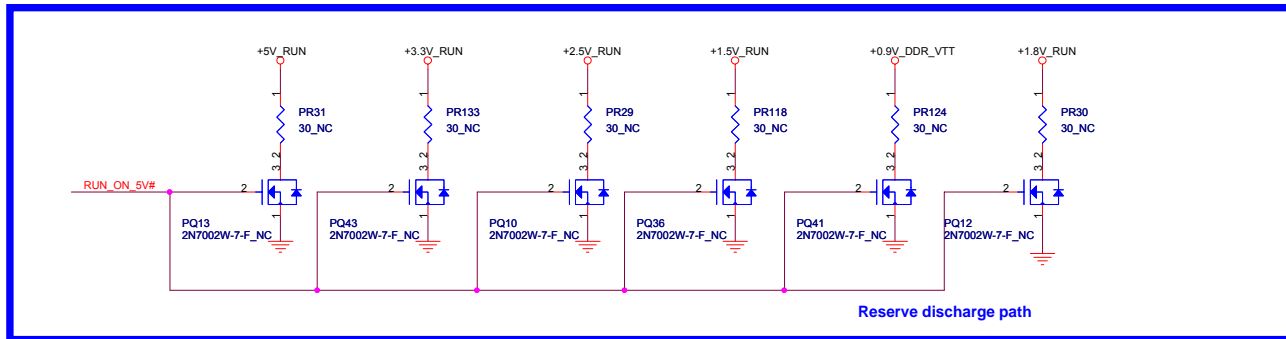
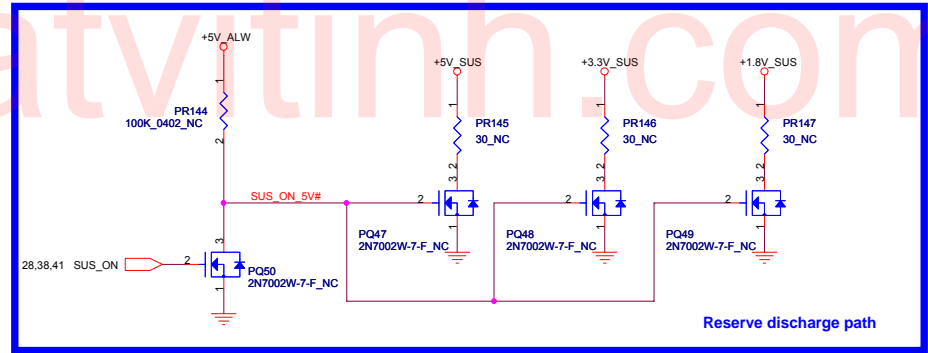
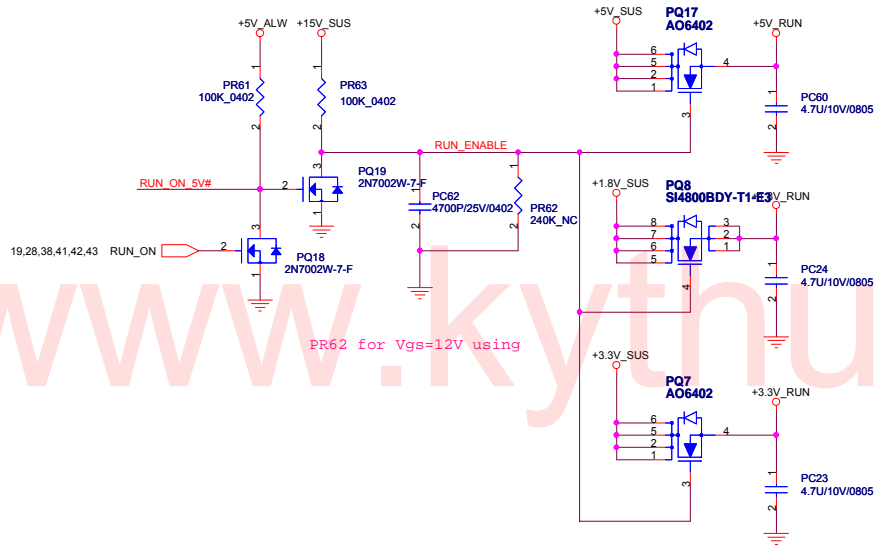
Parallel



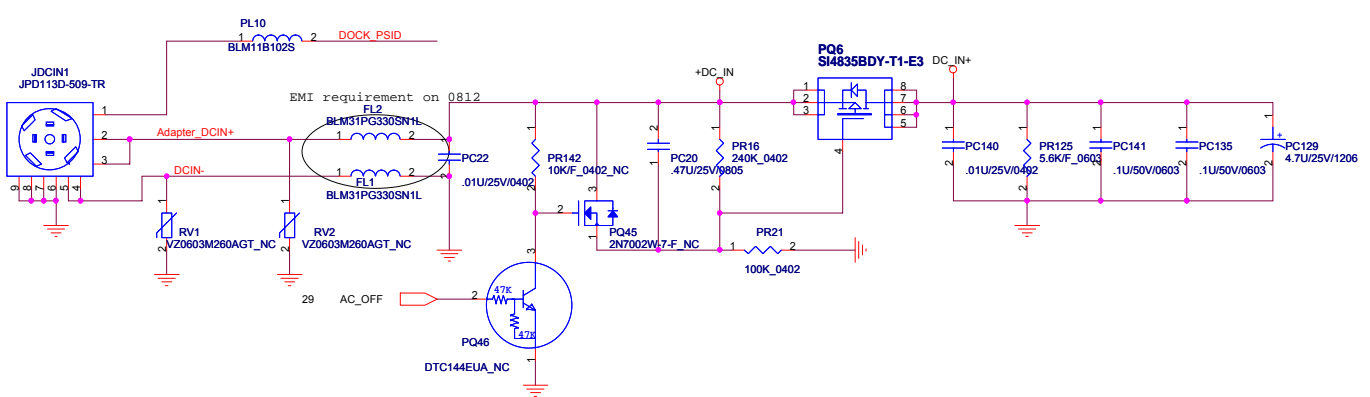
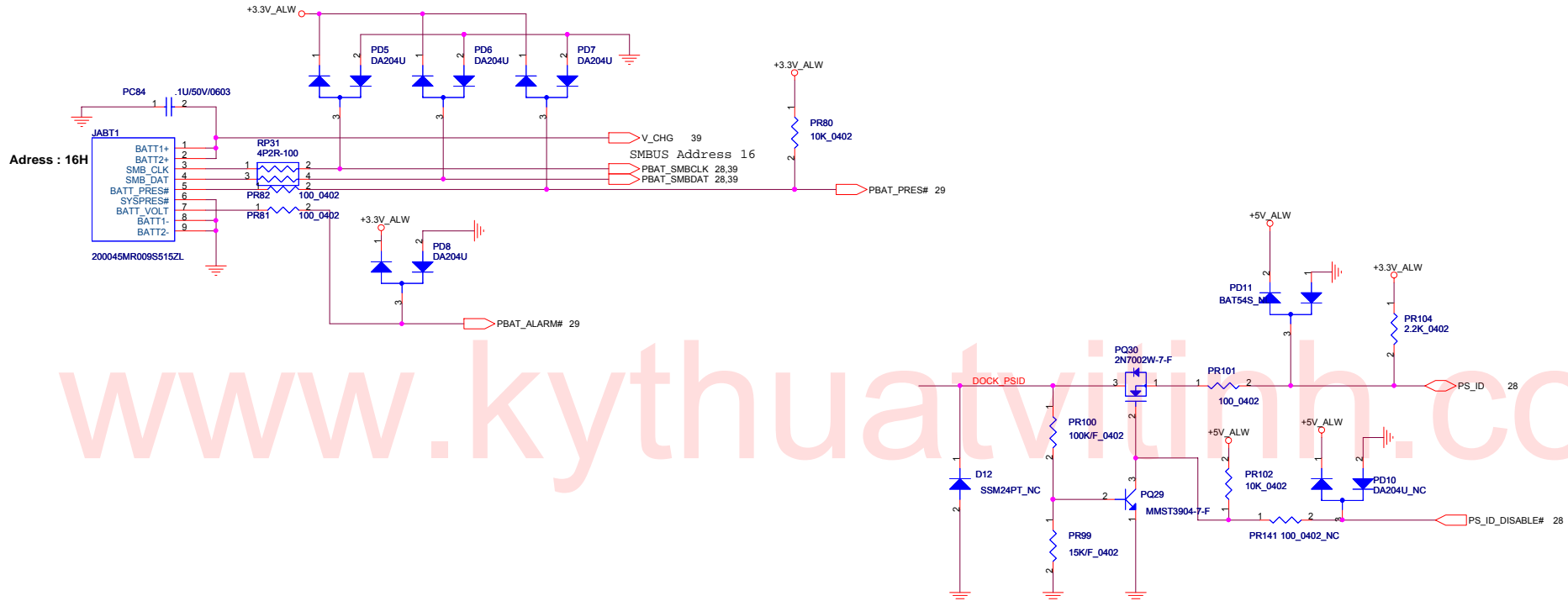
PR23 populate---->FCCM mode
PR108 populate---->Hysteretic/FCCM mode.

PR115 populate---->FCCM mode
PR112 populate---->Hysteretic/FCCM mode.





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Title: DCIN,BATT CONNECTOR

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