

COMPAL CONFIDENTIAL

MODEL NAME : *NAL22/23/24*

PCB NO : *LA-5573P (DAA00001G00)*

BOM P/N : *43177531LXX*

M10 Margaux DIS/ASICS rPGA Auburndale/Clarksville +FCBGA PCH IBEXPEAK-M + N10M-NS-B/N10P-GLM/N10P-GLM4

2010-01-21

REV : 1.0(A00)

@ : Nopop Component

7@ : N10P-GLM VID

8@ : N10M-NS-B & N10P-GLM4 VID

9@ : N10P-GLM4 only

MB Type	BOM P/N	Asics DIS N10P		Margaux DIS N10M		TCM		TPM		BOM CONFIG
		1@	2@	W(3@)	W/O(4@)	W(5@)	W/O(6@)			
Margaux DIS, TPM EN,TCM DIS	43177531L01		*		*	*				2@, 4@, 5@, 8@
Margaux DIS, TCM EN,TPM DIS	43177531L02		*	*			*			2@, 3@, 6@, 8@
Margaux DIS, ALL TPM DISABLE	43177531L03		*		*		*			2@, 4@, 6@, 8@
Asics GLM, TPM EN,TCM DIS	43177531L11	*			*	*				1@, 4@, 5@, 7@
Asics GLM, TCM EN,TPM DIS	43177531L12	*		*			*			1@, 3@, 6@, 7@
Asics GLM, ALL TPM DISABLE	43177531L13	*			*		*			1@, 4@, 6@, 7@
Asics GLM4, TPM EN,TCM DIS	43177531L21	*			*	*				1@, 4@, 5@, 8@, 9@
Asics GLM4, TCM EN,TPM DIS	43177531L22	*		*			*			1@, 3@, 6@, 8@, 9@
Asics GLM4, ALL TPM DISABLE	43177531L23	*			*		*			1@, 4@, 6@, 8@, 9@

MB PCB	
Part Number	Description
DAA00001G00	PCB 0AH LA-5573P REV0 M/B DIS

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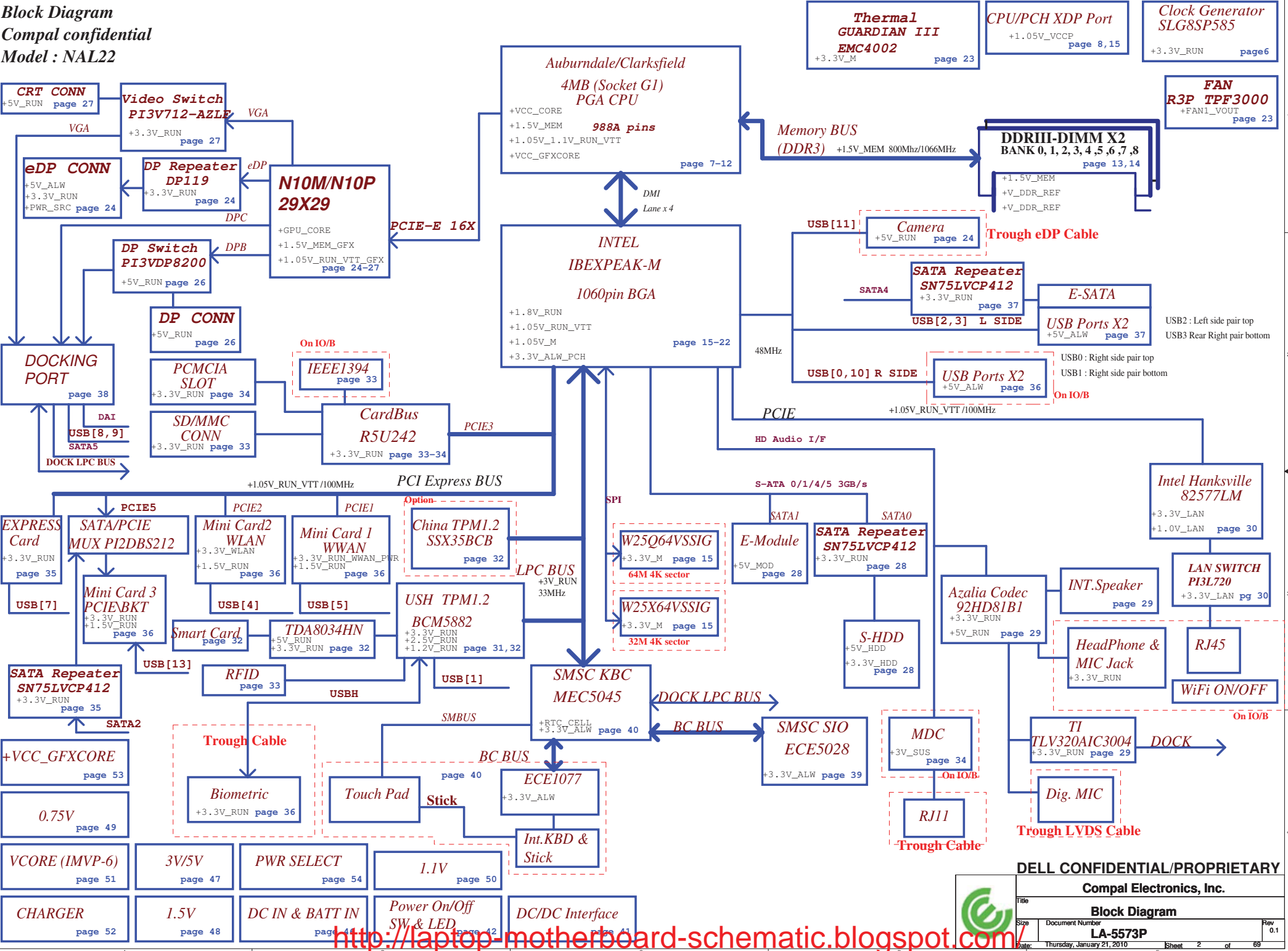
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Block Diagram
 Compal confidential
 Model : NAL22



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Block Diagram

LA-5573P

POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M1	LOW	LOW	HIGH	LOW	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M1	LOW	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State \ power plane	+15V_ALW +5V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_CORE +1.05V_RUN_VTT +1.05V_RUN	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

PCH	USB PORT#	DESTINATION
	0	JUSB1 (Ext Right Side Bottom)
	1	JUSB1 (Ext Right Side Top)
	2	JESA1 (Ext Left Side Top)
	3	JESA1 (Ext Left Side Bottom)
	4	WLAN
	5	WWAN
	6	Bluetooth
	7	USH->BIO
	8	DOCKING
	9	DOCKING
	10	Express card
	11	Camera
	12	NA
13	WPAN/NVMHCI	

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	Card Bus
Lane 4	EXPRESS CARD
Lane 5	MINI CARD-3 PCIE/BKT
Lane 6	10/100/1G LAN
Lane 7	None
Lane 8	None

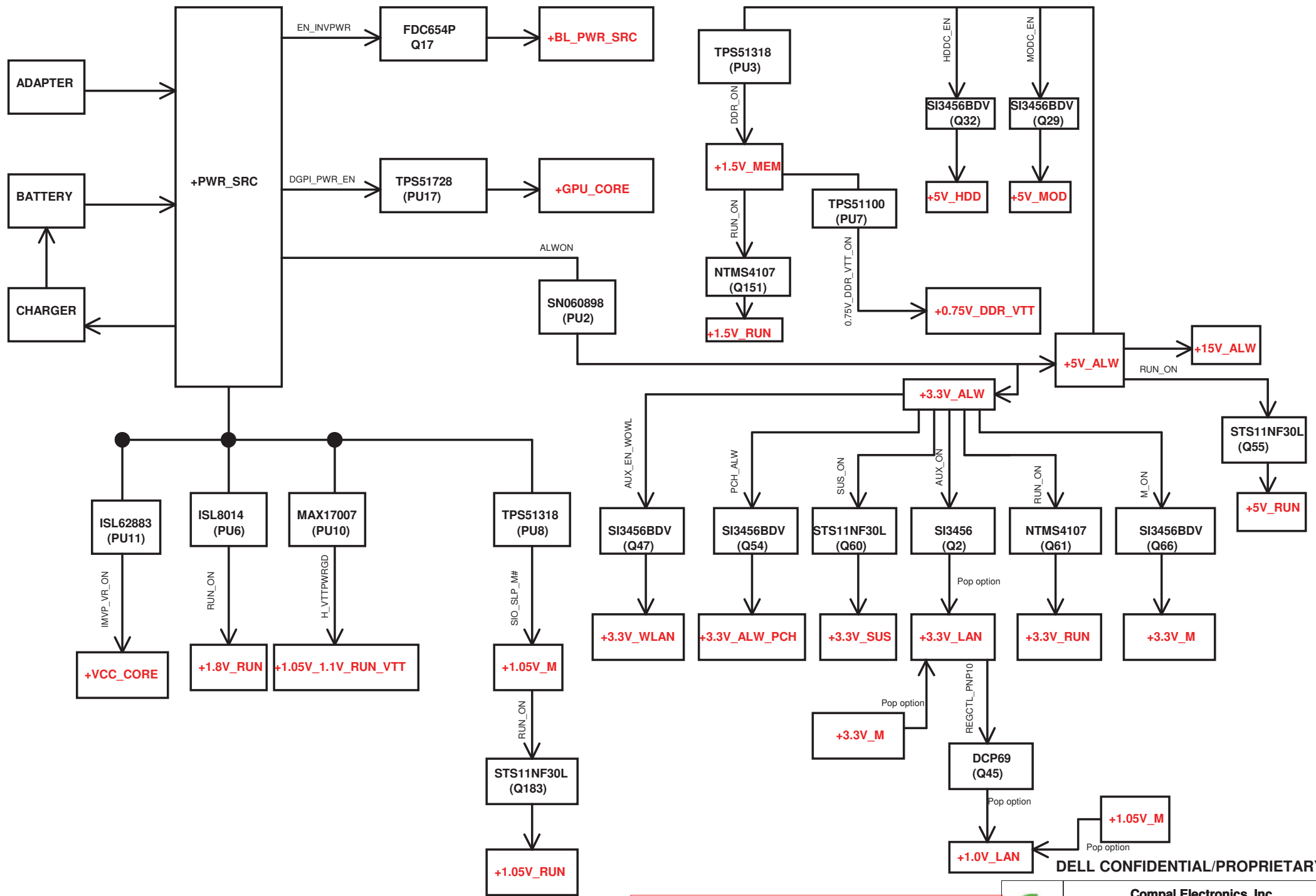
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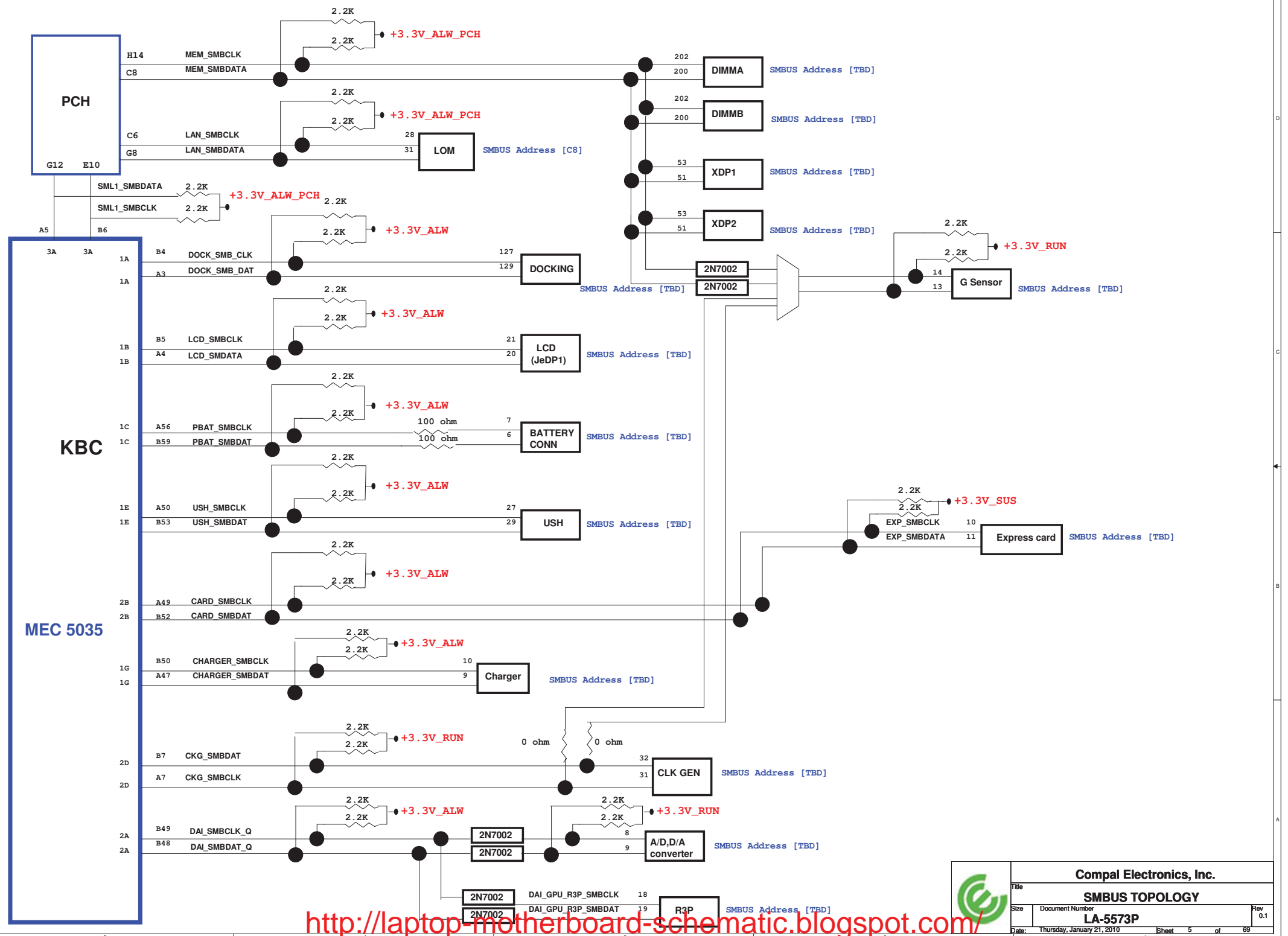
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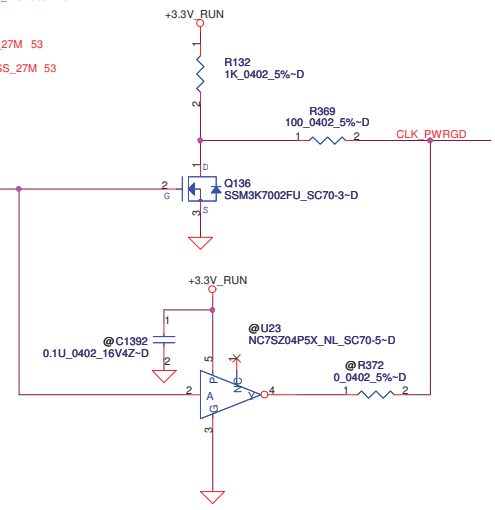
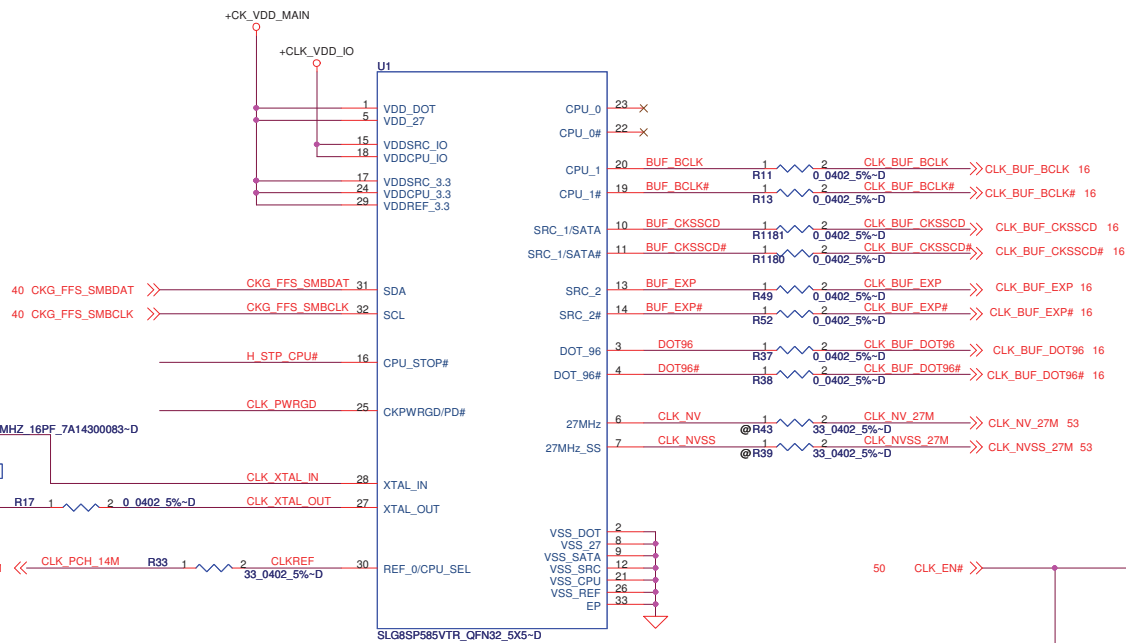
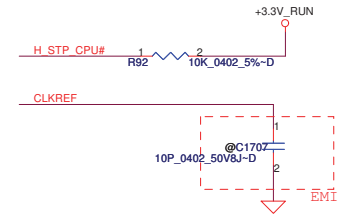
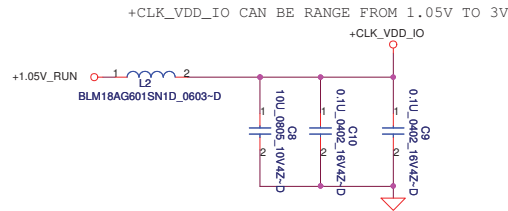
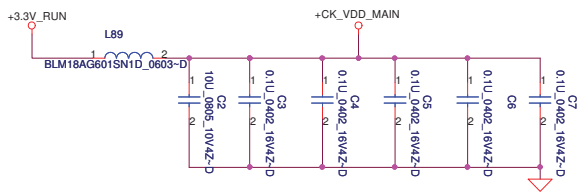


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Power Rail			
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PIN 30	CPU0	CPU1
1 (0.7~1.5v)	100MHz	100MHz
0 (DEFAULT)	133MHz	133MHz

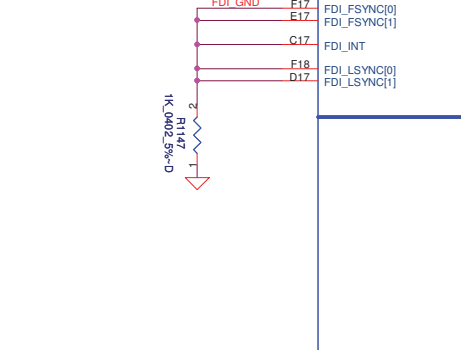
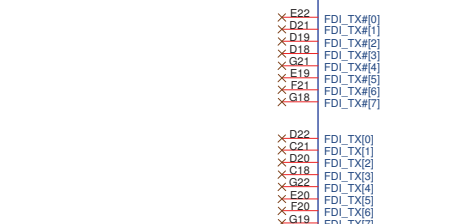
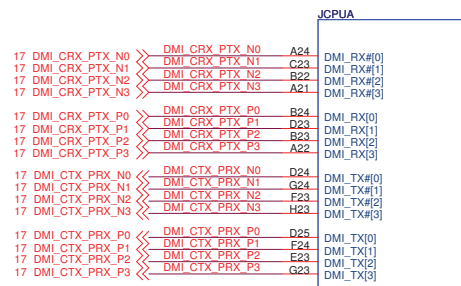
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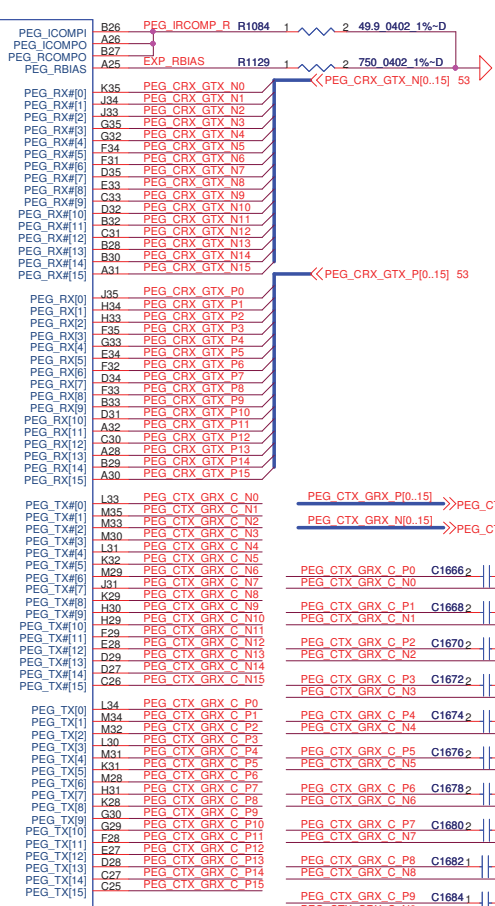
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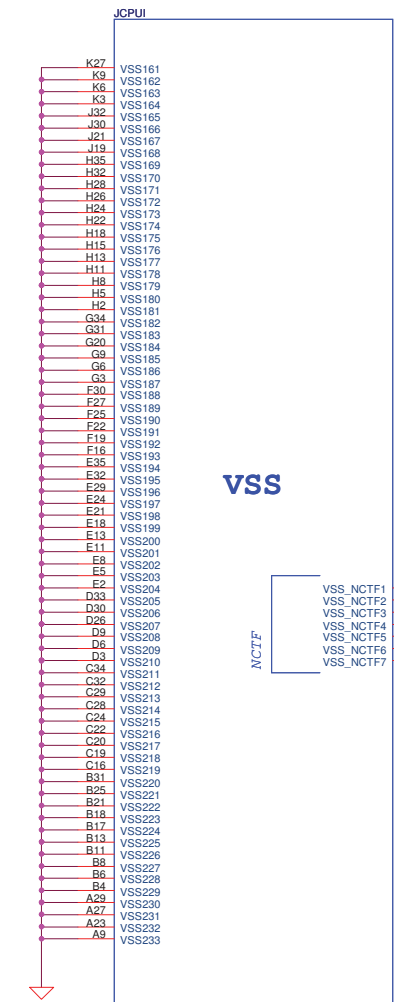


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GRAPHICS

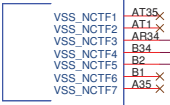


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PEG_TX#2	M30	PEG CTX GRX C N2	PEG CTX GRX P1	C1668	2	0.1U 0402 10V7K-D	PEG CTX GRX P1
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VSS

NCTF



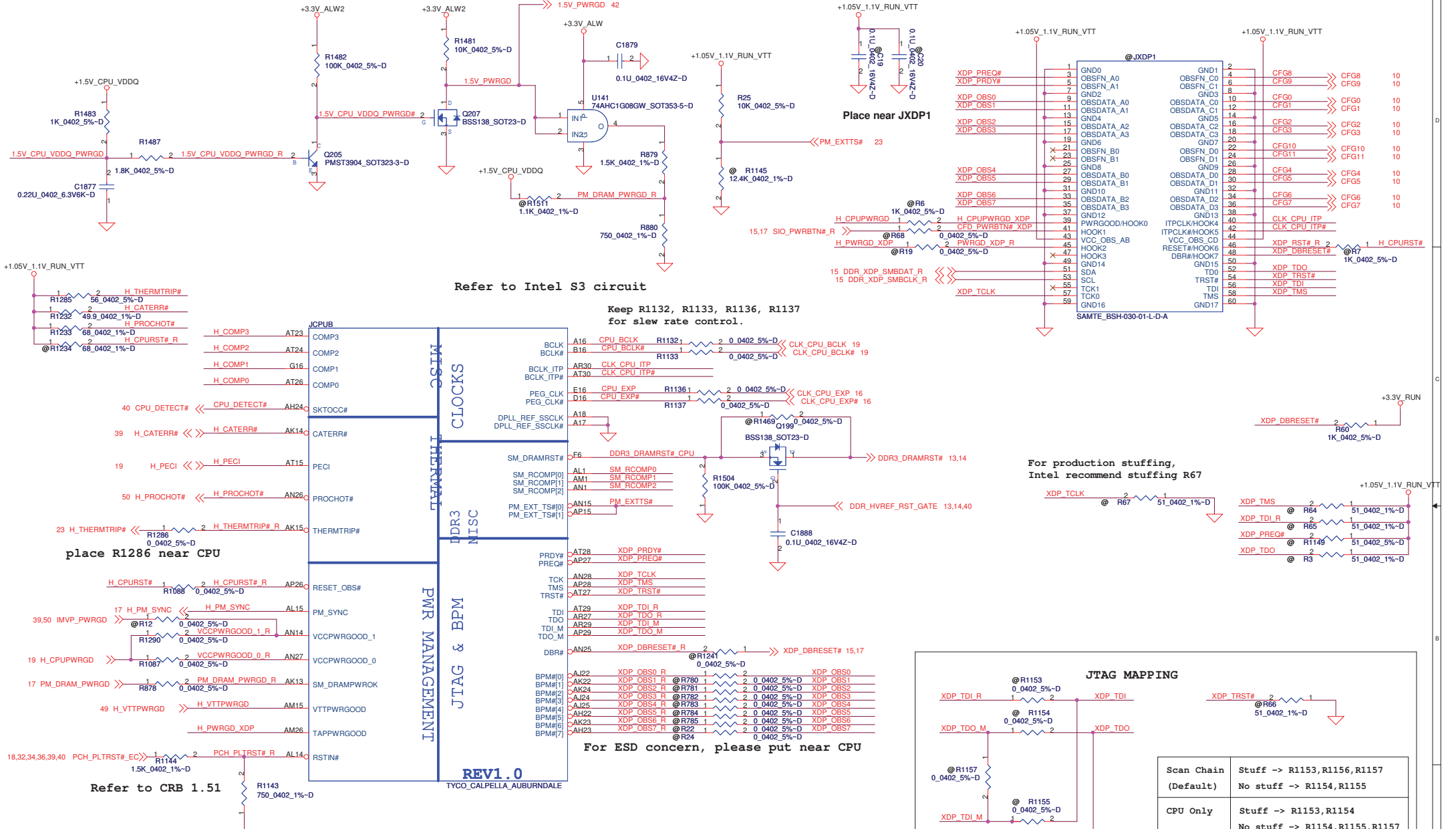
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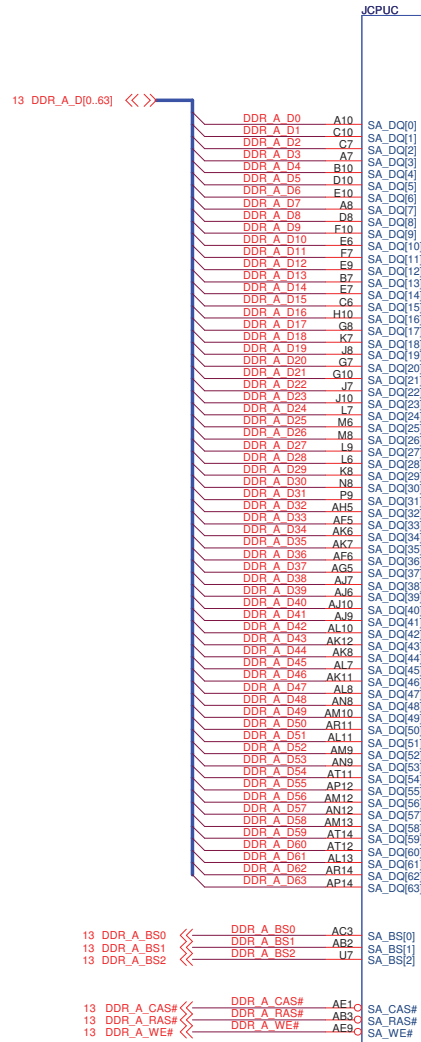
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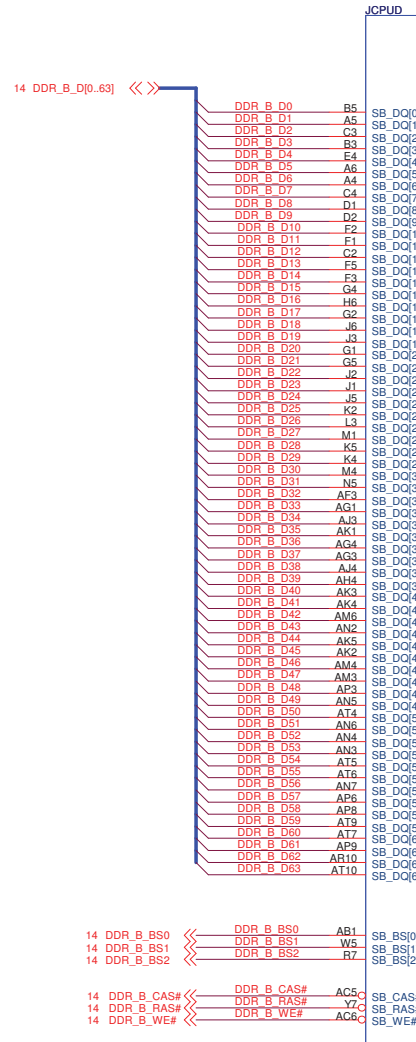
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 Burndale (2/6)
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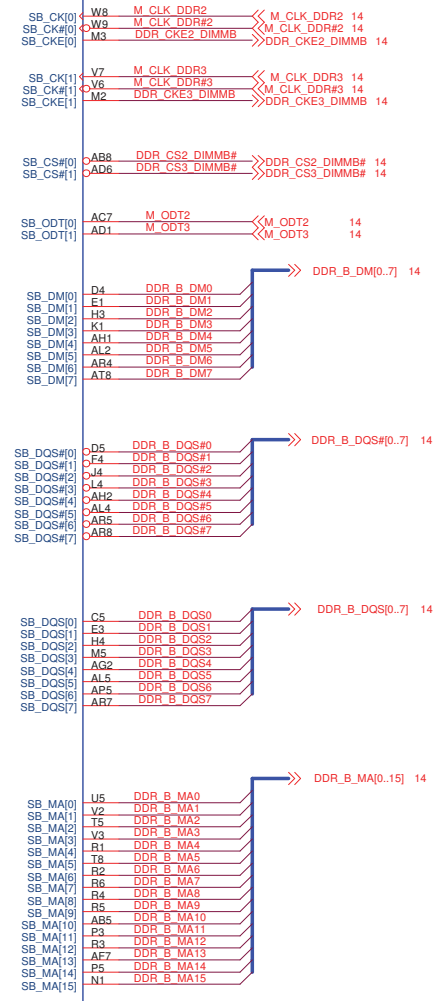
DDR SYSTEM MEMORY A

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DDR SYSTEM MEMORY - B

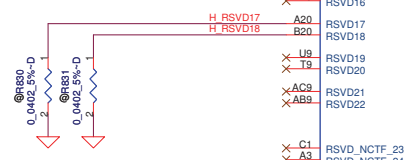
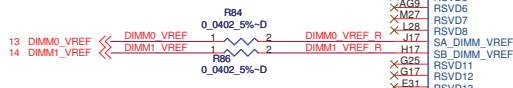
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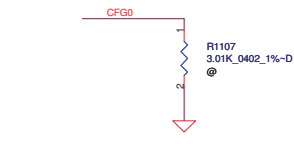


Populate R84,R86 for Intel DDR3 VREFDQ multiple methods M3

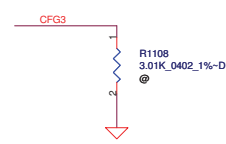


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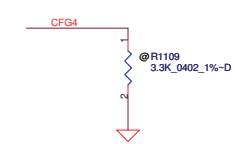
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PCI-Express Configuration Select	
CFG0	1 : Single PEG 0 : Bifurcation enable



PCI-Express Static Lane Reversal	
CFG3	1 : Normal Operation 0 : Lane Number Reversed 15->0, 14->1 ...



Display Port Presence	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

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Auburndale (4/6)

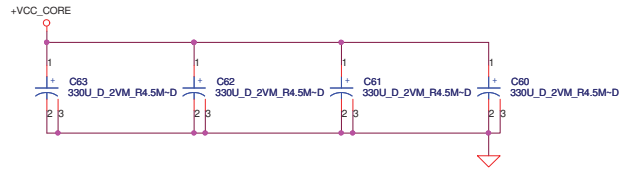
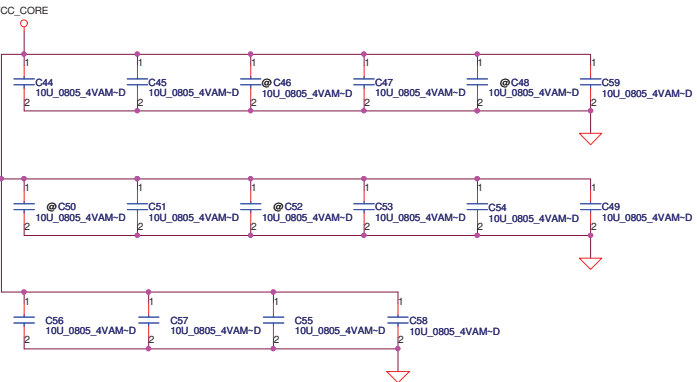
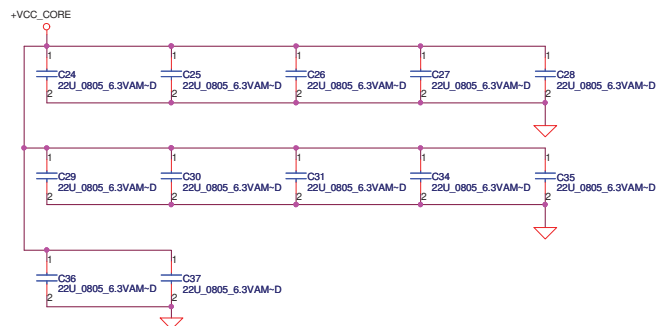
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A-5572P

Rev
0.1



Margaux DIS-->330uFx4 (C60-C63)
Asics/Asics II-->330uFx5 (C60-C63,C66)

JCPUIF

AG35	VCC1
AG34	VCC2
AG33	VCC3
AG32	VCC4
AG31	VCC5
AG30	VCC6
AG29	VCC7
AG28	VCC8
AG27	VCC9
AG26	VCC10
AF35	VCC11
AF34	VCC12
AF33	VCC13
AF32	VCC14
AF31	VCC15
AF30	VCC16
AF29	VCC17
AF28	VCC18
AF27	VCC19
AF26	VCC20
AD35	VCC21
AD34	VCC22
AD33	VCC23
AD32	VCC24
AD31	VCC25
AD30	VCC26
AD29	VCC27
AD28	VCC28
AD27	VCC29
AD26	VCC30
AC35	VCC31
AC34	VCC32
AC33	VCC33
AC32	VCC34
AC31	VCC35
AC30	VCC36
AC29	VCC37
AC28	VCC38
AC27	VCC39
AC26	VCC40
AC25	VCC41
AA35	VCC42
AA34	VCC43
AA33	VCC44
AA32	VCC45
AA31	VCC46
AA30	VCC47
AA29	VCC48
AA28	VCC49
AA27	VCC50
Y35	VCC51
Y34	VCC52
Y33	VCC53
Y32	VCC54
Y31	VCC55
Y30	VCC56
Y29	VCC57
Y28	VCC58
Y27	VCC59
Y26	VCC60
V35	VCC61
V34	VCC62
V33	VCC63
V32	VCC64
V31	VCC65
V30	VCC66
V29	VCC67
V28	VCC68
V27	VCC69
V26	VCC70
U35	VCC71
U34	VCC72
U33	VCC73
U32	VCC74
U31	VCC75
U30	VCC76
U29	VCC77
U28	VCC78
U27	VCC79
U26	VCC80
R35	VCC81
R34	VCC82
R33	VCC83
R32	VCC84
R31	VCC85
R30	VCC86
R29	VCC87
R28	VCC88
R27	VCC89
R26	VCC90
P35	VCC91
P34	VCC92
P33	VCC93
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P26	VCC100

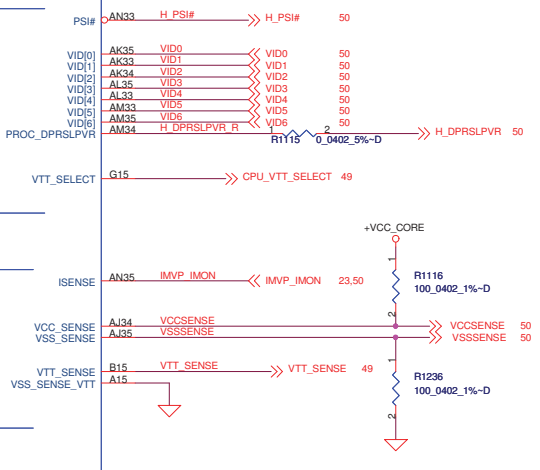
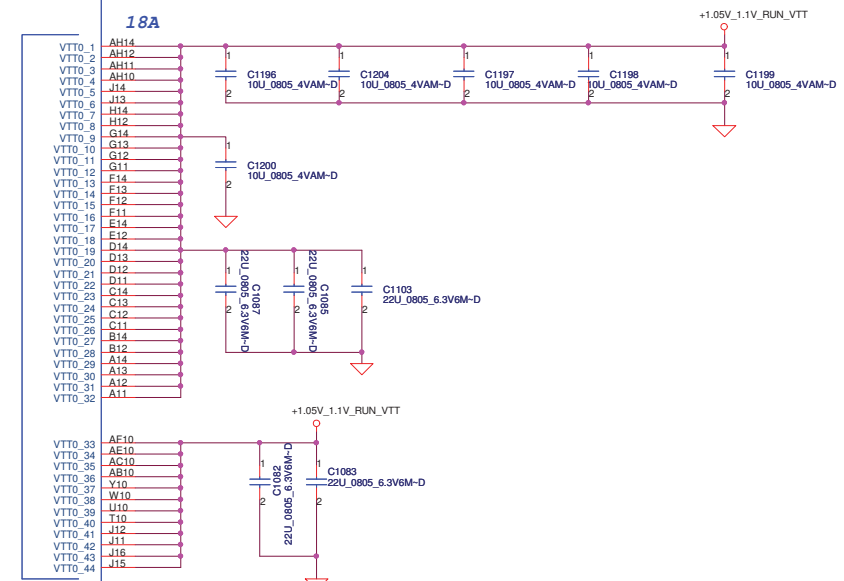
I.1V RAIL POWER

CPU CORE SUPPLY

POWER

CPU VIDS

SENSE LINES



VTT_SELECT = low, 1.1V
VTT_SELECT = high, 1.05V

Place R1116 and R1117 near CPU
Route VCCSENSE and VSSSENSE trace at 27.4 ohms, 7 mils spacing

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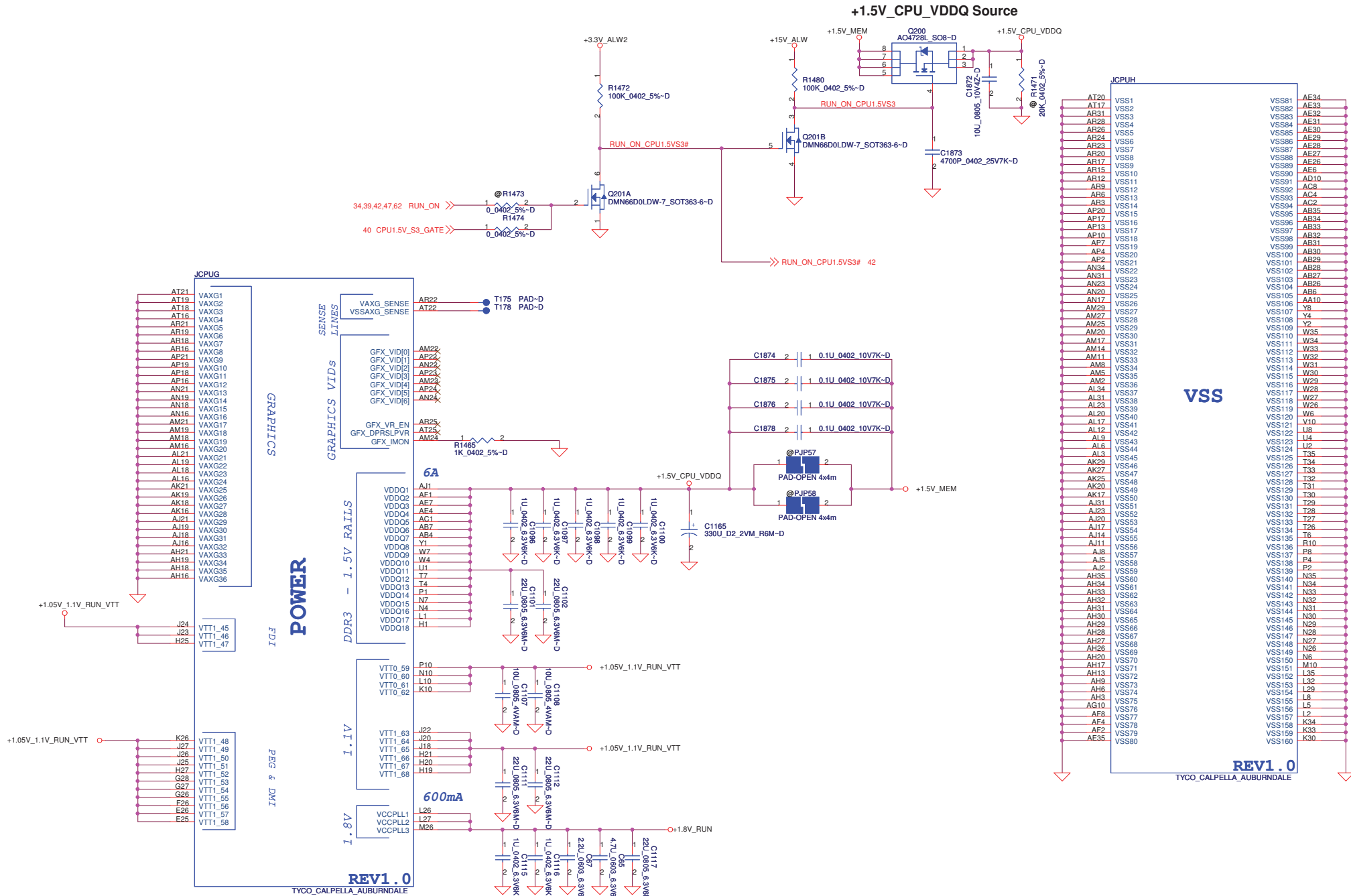
Compal Electronics, Inc.

File	Auburndale (5/6)
Document Number	IA-5573P
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Auburndale (6/6)

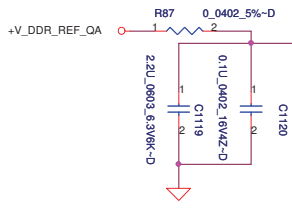
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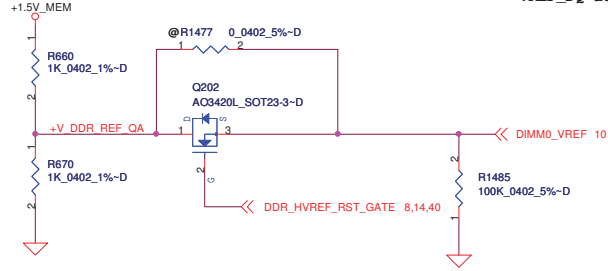
<http://laptop-motherboard-schematic.blogspot.com/>

- 9 DDR_A_DQS#0[0..7] <<>>
- 9 DDR_A_D[0..63] <<>>
- 9 DDR_A_DM[0..7] <<>>
- 9 DDR_A_DQS[0..7] <<>>
- 9 DDR_A_MA[0..15] <<>>

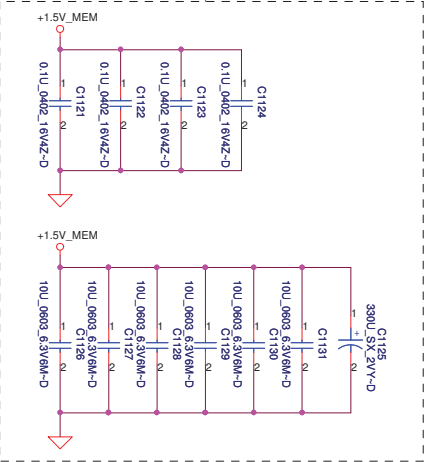
Populate R87 for Intel DDR3 VREFDQ multiple methods M1



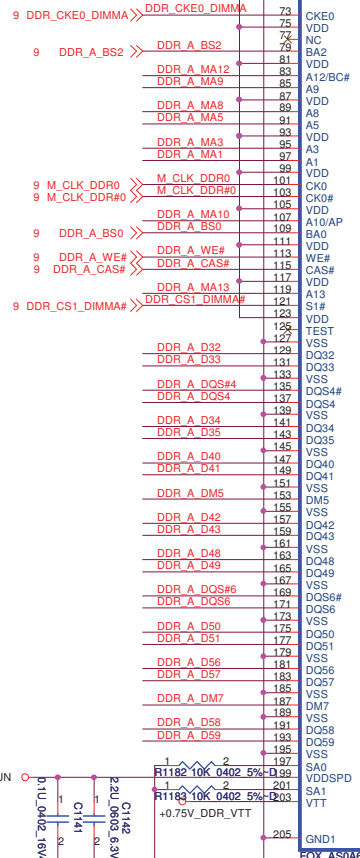
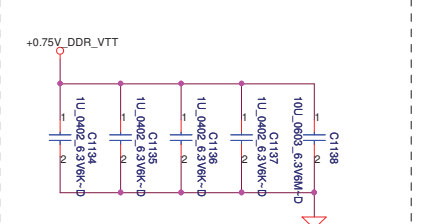
Note:
Check voltage tolerance of VREF_DQ at the DIMM socket



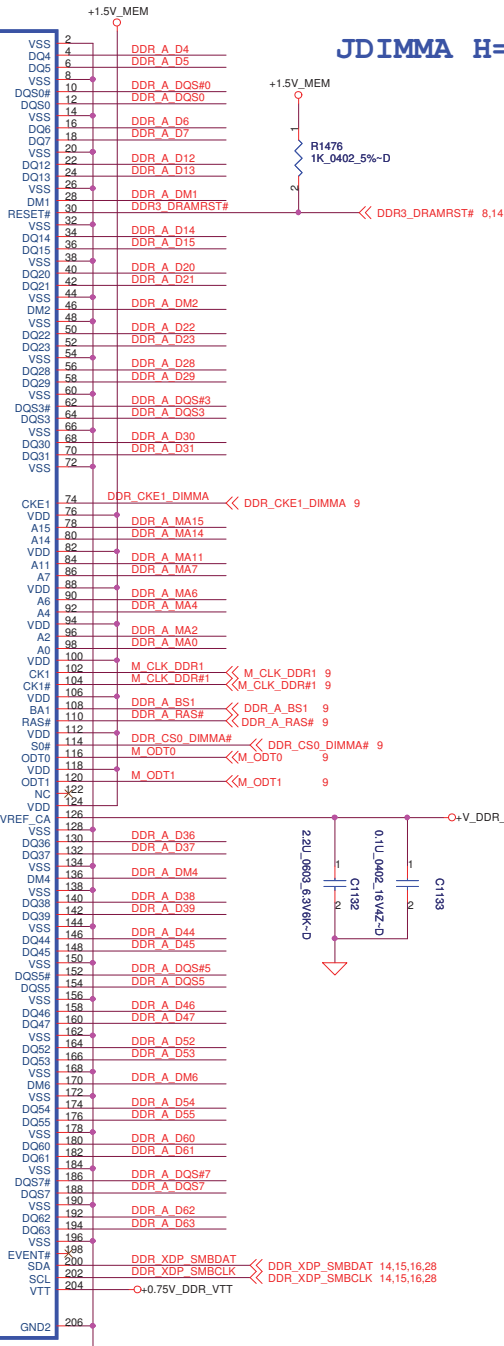
Layout Note:
Place near JDIMMA



Layout Note:
Place near JDIMMA.203,204



JDIMMA H=5.2



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DDRIII-SODIMM SLOT1

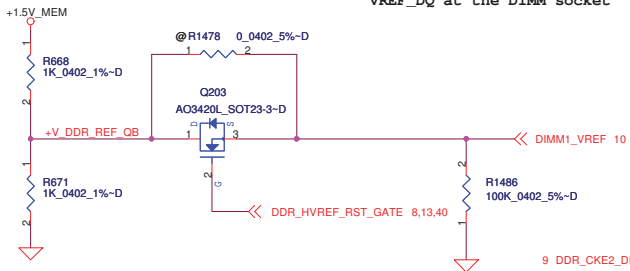
LA-5573P

File: _____
Size: _____ Document Number: _____ Rev: 0.1
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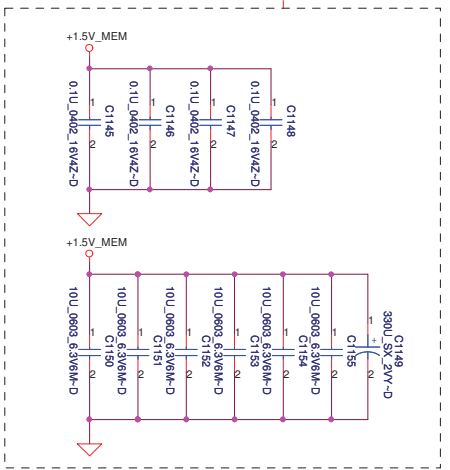
- 9 DDR_B_DQS#(0..7) <<>
- 9 DDR_B_D[0..63] <<>
- 9 DDR_B_DM(0..7) <<>
- 9 DDR_B_DQS(0..7) <<>
- 9 DDR_B_MA(0..15) <<>

Populate R88 for Intel DDR3 VREFDQ multiple methods M1

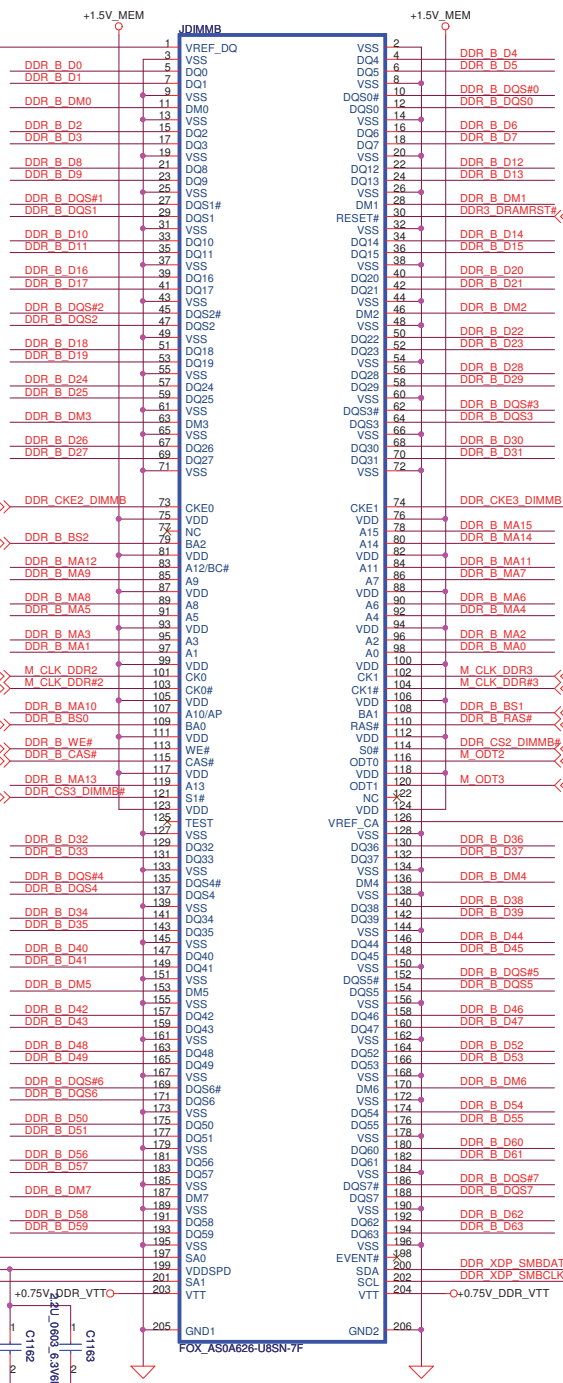
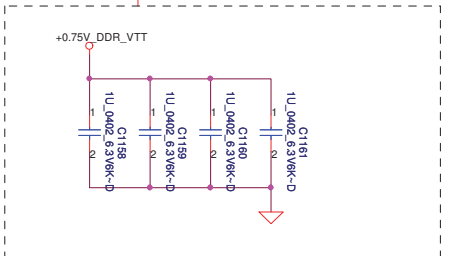
Note: Check voltage tolerance of VREF_DQ at the DIMM socket



Layout Note: Place near JDIMMB



Layout Note: Place near JDIMMB.203, 204



JDIMMB H=9.2

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Title DDRIII-SODIMM SLOT2		
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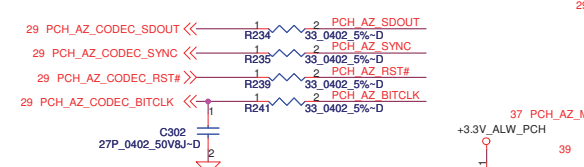
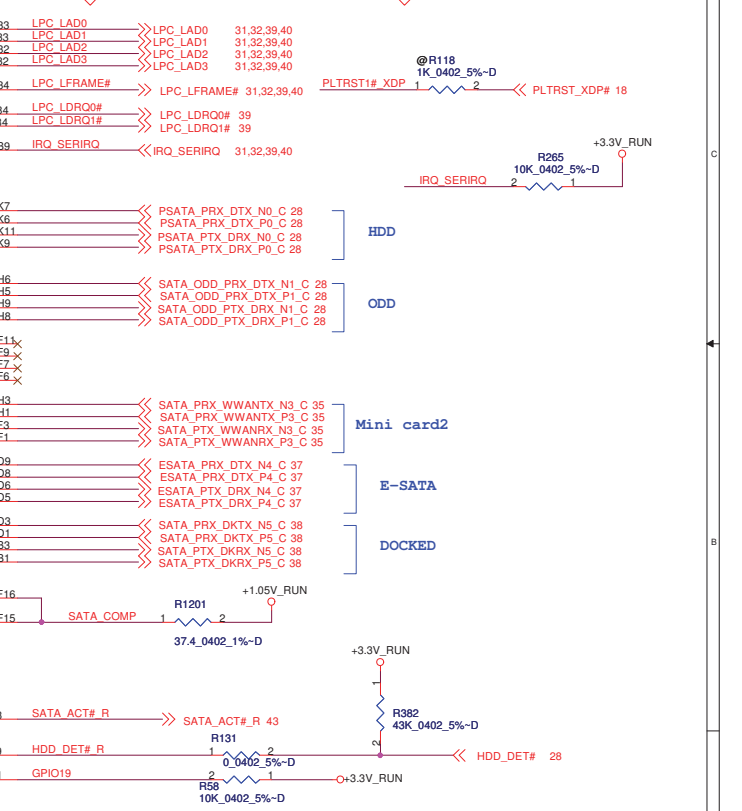
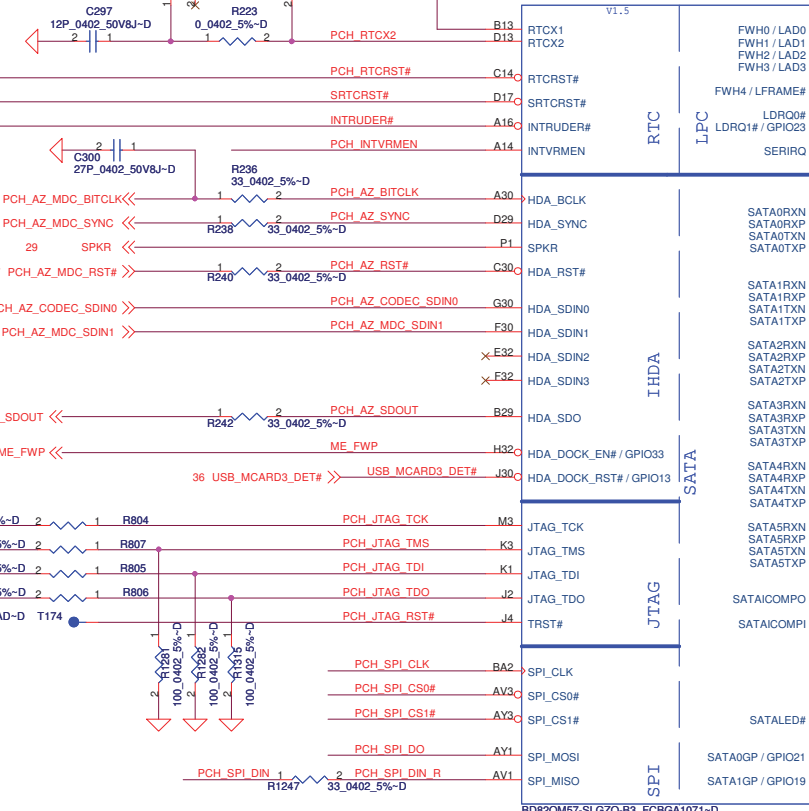
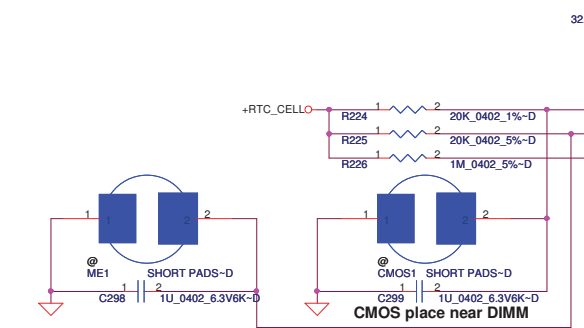
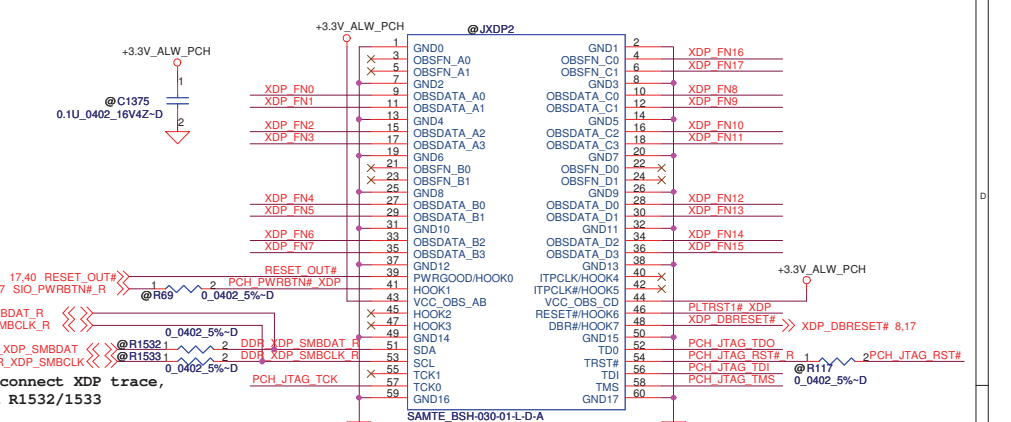
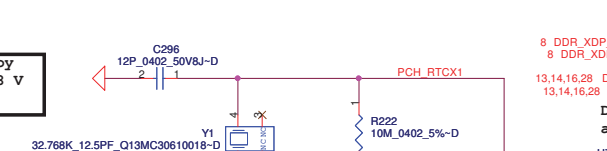
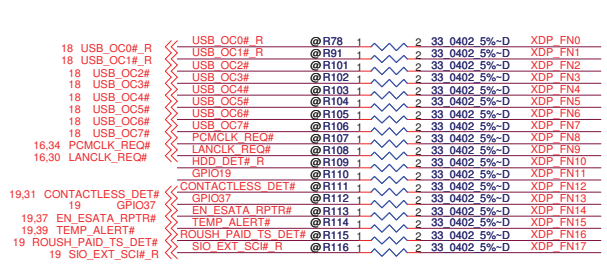
CMOS CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

ME CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

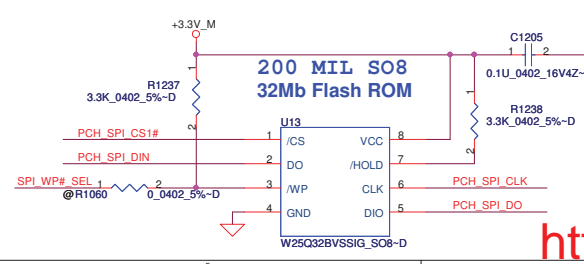
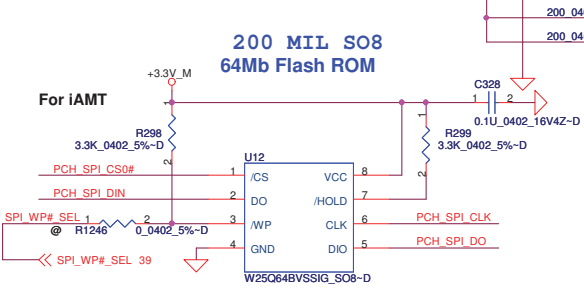


INTVRMEN - Integrated SUS
 1.1V VRM Enable
 High - Enable Internal VRs

On Die PLL VR is supplied by 1.5V when sampled high, 1.8 V when sampled low



Stuff R128, no stuff R123 when production



PCH Pin	Ref.	PCH JTAG Enable		PCH JTAG Disable		Production
		ES1	ES2	ES1	ES2	
TDO	R806	No Stuff	200 ohm	No Stuff	No Stuff	No Stuff
TMS	R1315	No Stuff	100 ohm	No Stuff	No Stuff	No Stuff
TMS	R807	200 ohm	200 ohm	No Stuff	No Stuff	No Stuff
TDI	R1281	100 ohm	100 ohm	No Stuff	No Stuff	No Stuff
TDI	R805	200 ohm	200 ohm	20K ohm	No Stuff	No Stuff
TCK	R1282	100 ohm	100 ohm	10K ohm	No Stuff	No Stuff
TCK	R804	51 ohm	51 ohm	51 ohm	51 ohm	No Stuff
TRST#	R808	20K ohm	20K ohm	No Stuff	No Stuff	No Stuff
TRST#	R1286	10K ohm	10K ohm	No Stuff	No Stuff	No Stuff

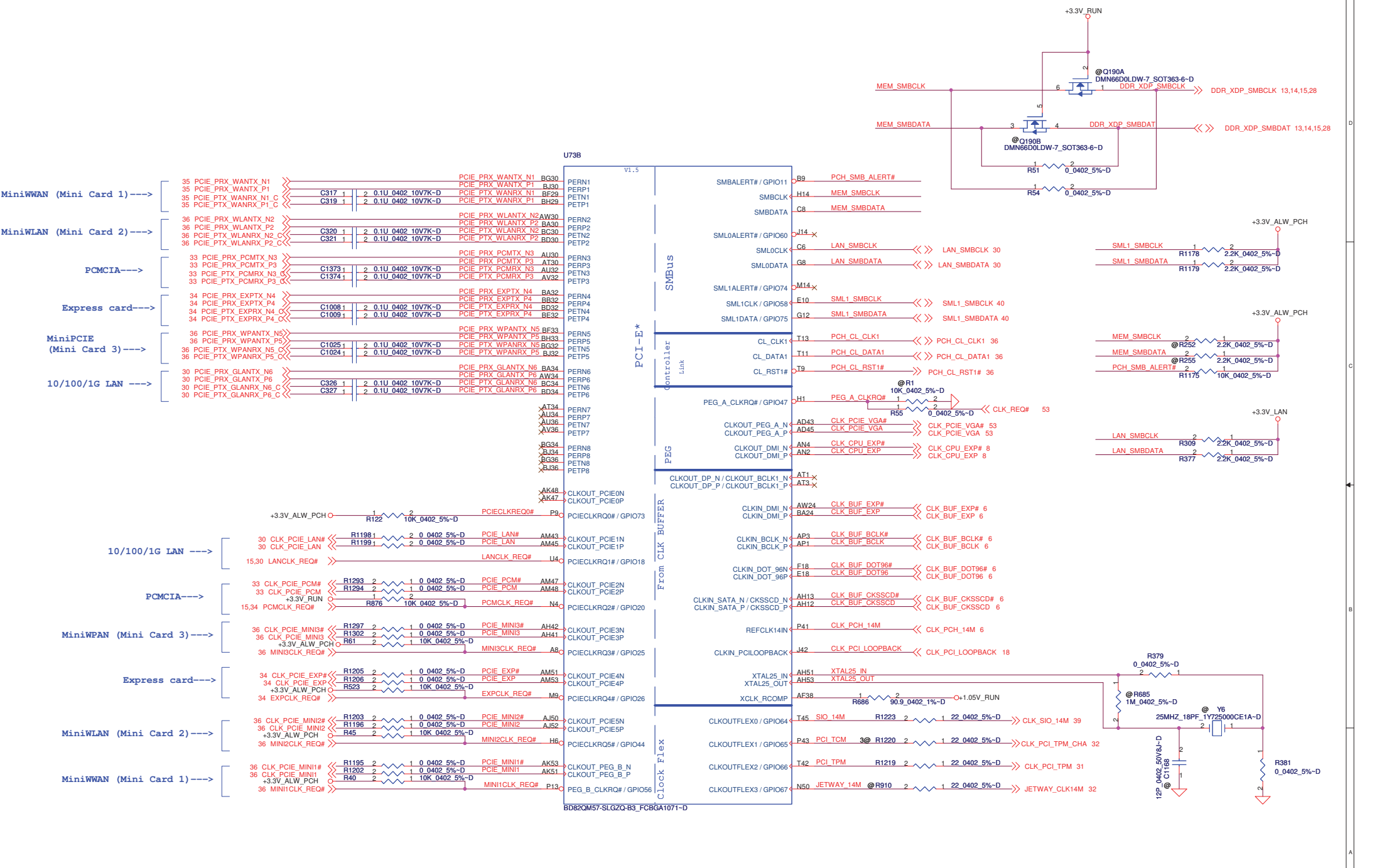
No Reboot Strap
 Low = Default
 High = No Reboot

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PCH (1/8)

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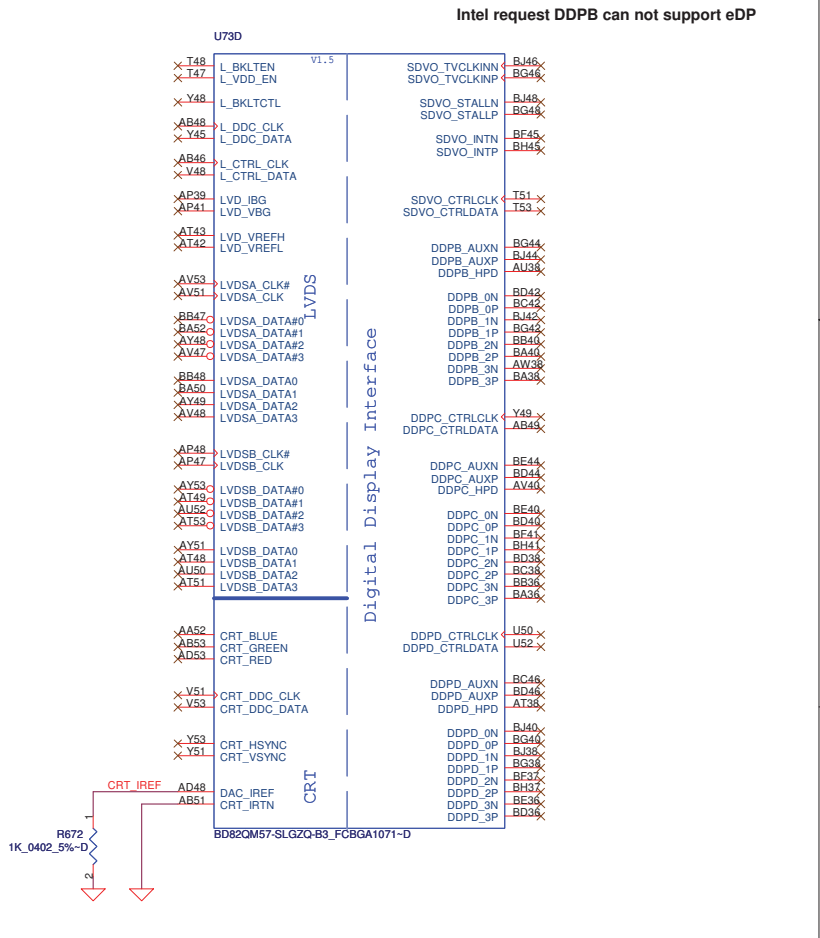
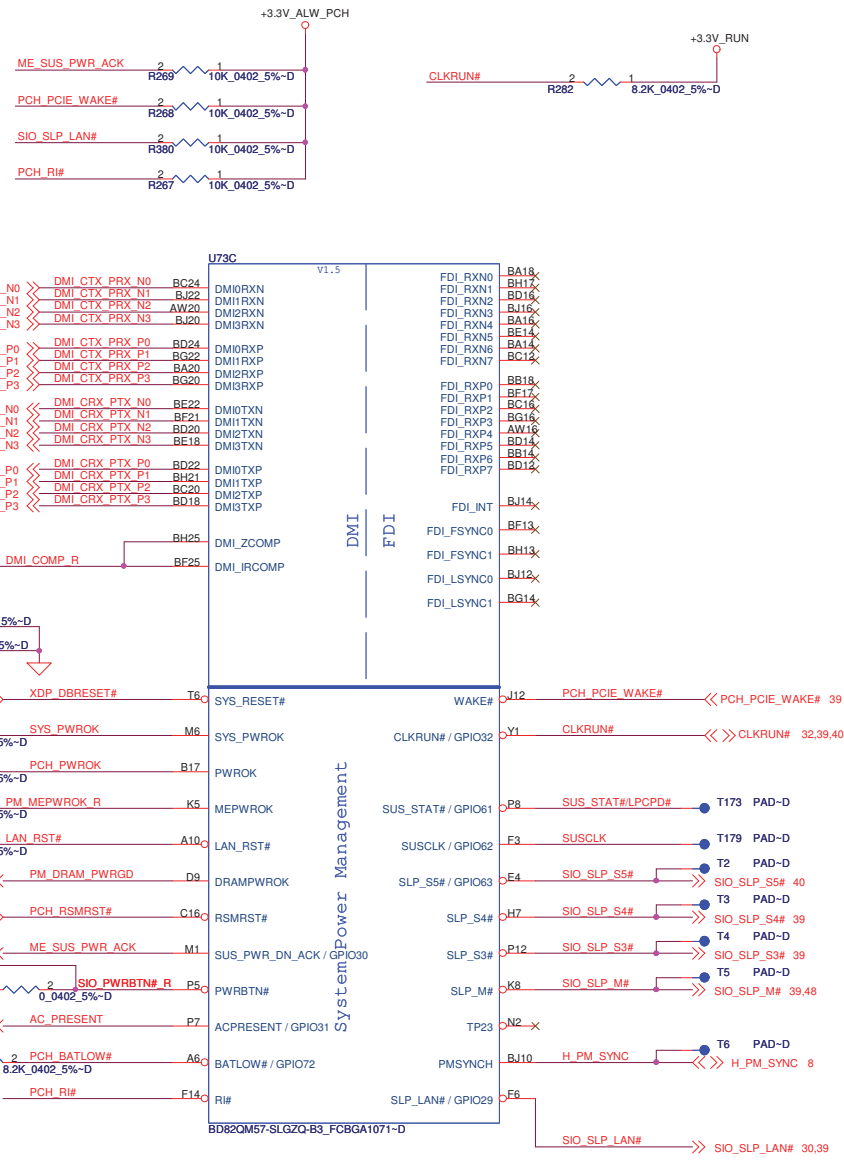
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Intel request DDPB can not support eDP

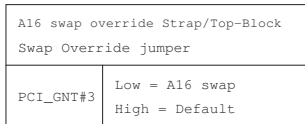
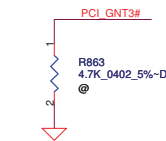
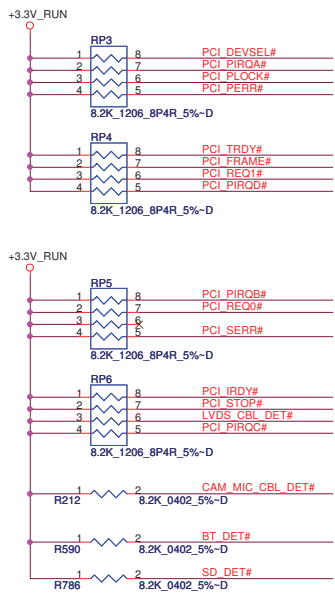
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PCH (3/8)

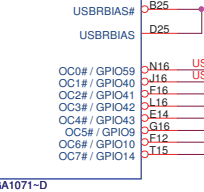
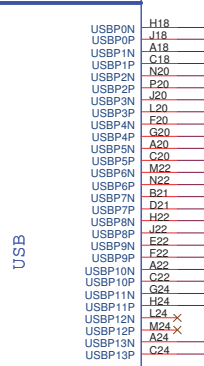
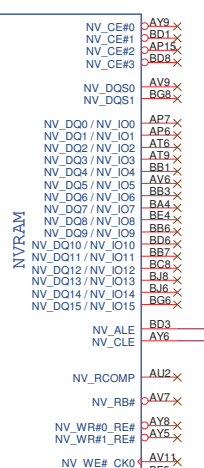
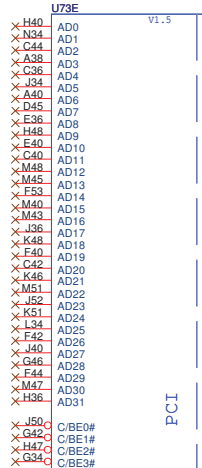
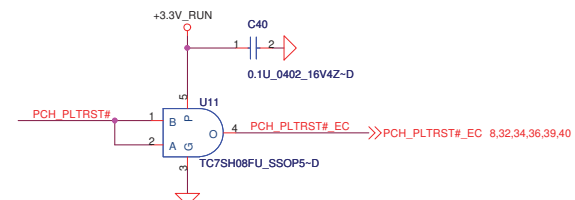
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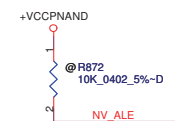


Al6 swap override Strap/Top-Block
Swap Override jumper

PCI_GNT#3	Low = Al6 swap
	High = Default

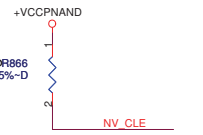


PCH XDP ENABLE	Stuff: R78,R89,R101-R116
	No Stuff: R71,R77,RP1,RP2,R45,R40,R131,R58,R1242,R1243,R1244,R1245,R74,R130
PCH XDP DISABLE	Stuff: R71,R77,RP1,RP2,R45,R40,R131,R58,R1242,R1243,R1244,R1245,R74,R130
	No Stuff: R78,R89,R101-R116



Danbury Technology Enabled

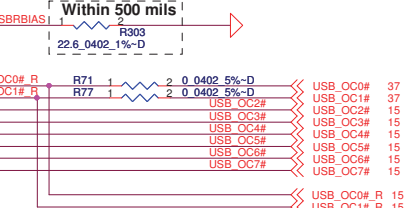
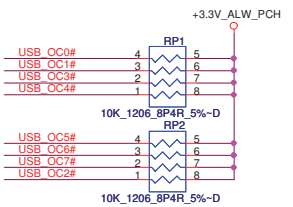
NV_ALE	High = Enabled (Default)
	Low = Disabled



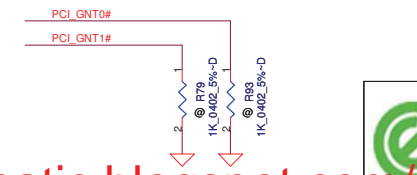
DMI Termination Voltage

NV_CLE	Set to Vss when LOW
	Set to Vcc when HIGH

- >Right Side Bottom
- >Right Side Top
- >Left Side Top
- >Left Side Bottom
- >WLAN
- >WWAN
- >Blue Tooth
- >BIO
- >DOCK
- >Express Card
- >Camera
- >PCIE/BKT



PCI_GNT#1	PCI_GNT#0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI



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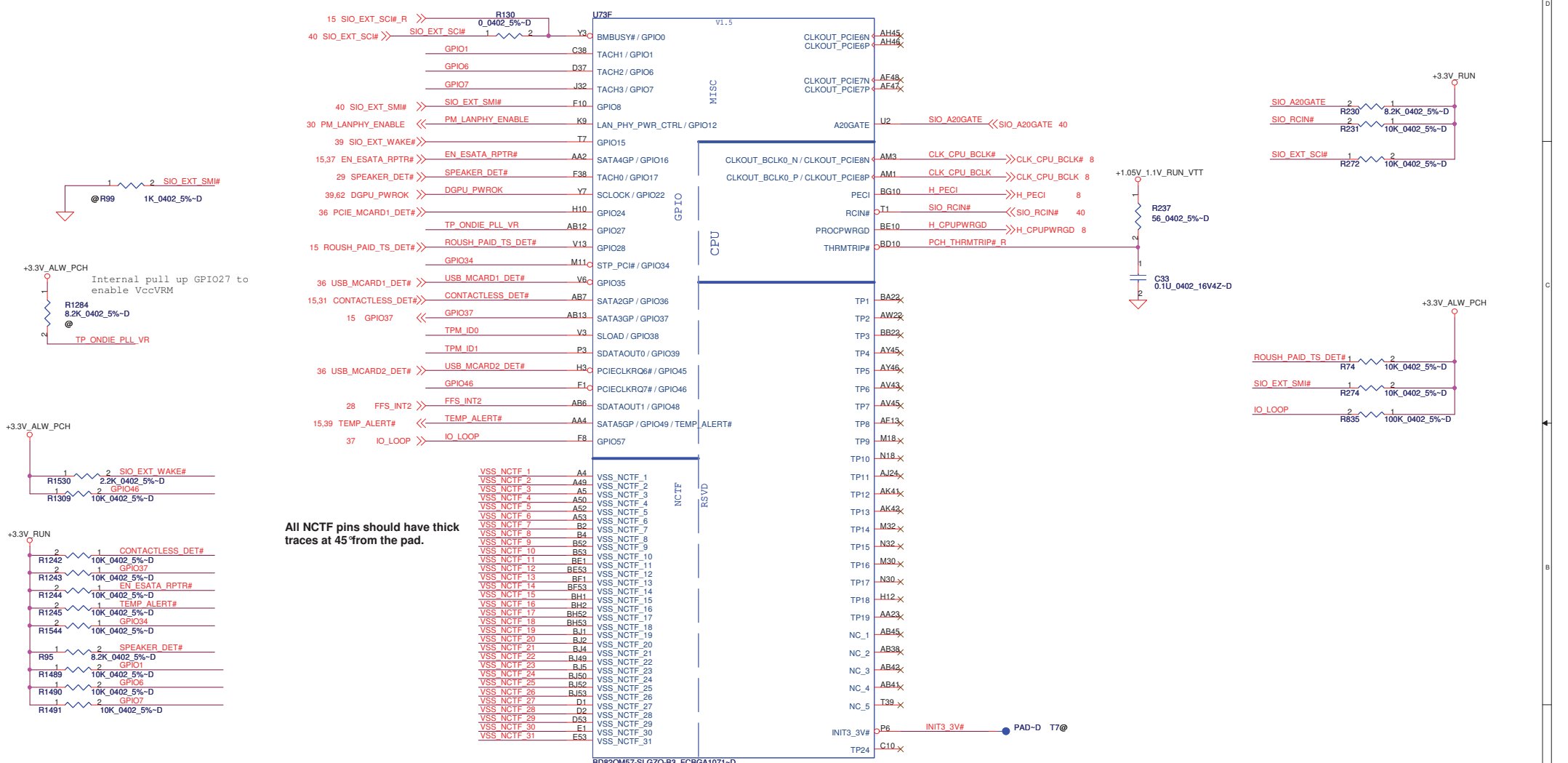
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Title

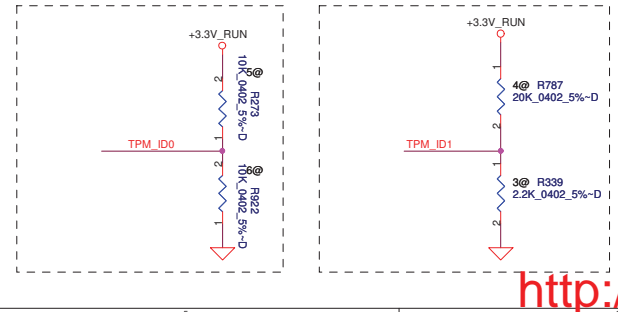
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All NCTF pins should have thick traces at 45° from the pad.



	TPM_ID0	TPM_ID1
China TPM	0	0
No TPM, No China TPM	0	1
USH1.0 (For SSI)	1	0
USH2.0	1	1

----- will use MEMO control pop R339 & de-pop R787 when USH1.0 enable for SSI build only

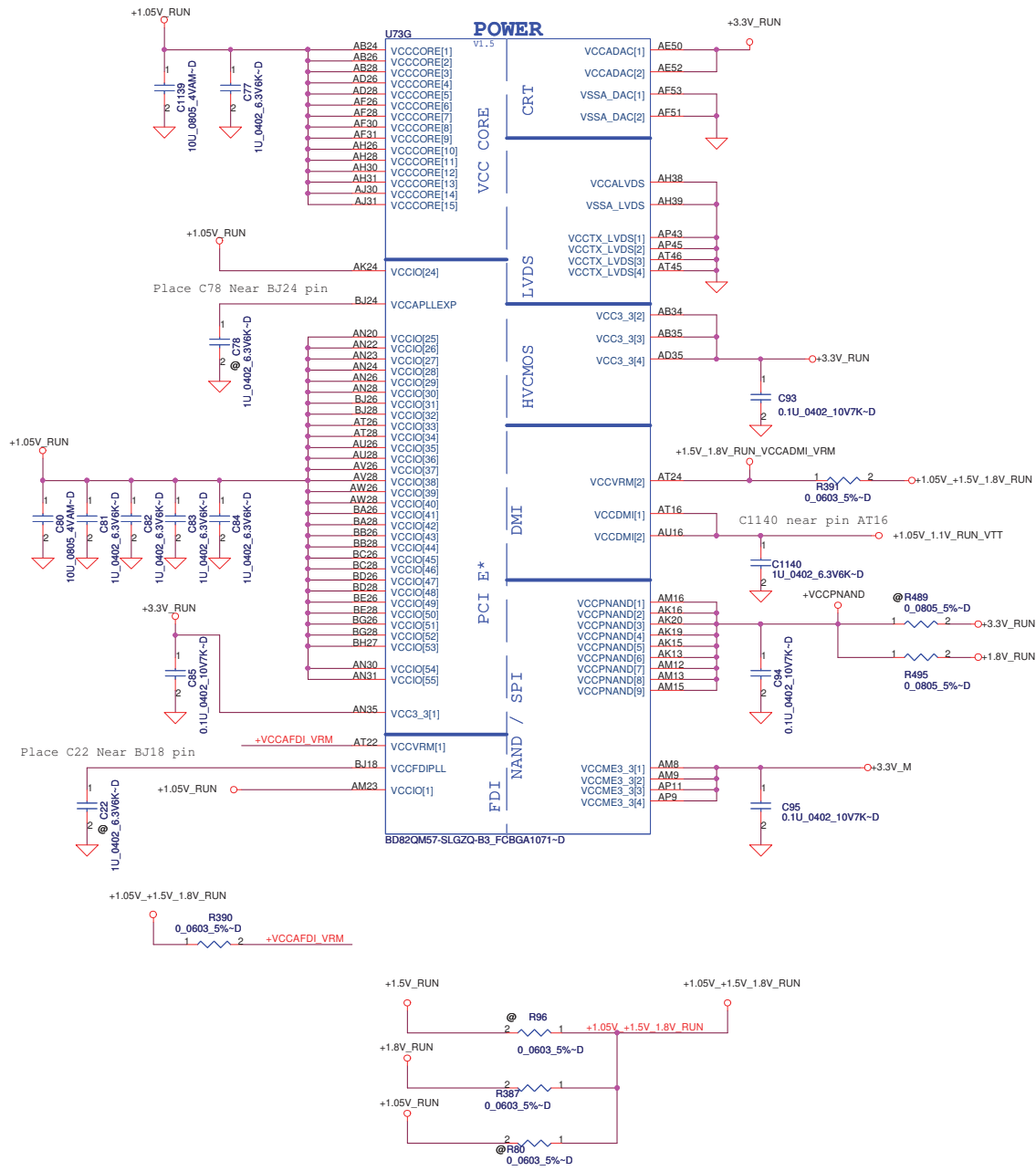
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PCH (5/8)

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PCH Power Rail Table		
Voltage Rail	Voltage	SO Iccmax Current (A)
V_CPU_IO	1.1/1.05	< 1 (mA)
V5REF	5	< 1 (mA)
V5REF_Sus	5	< 1 (mA)
Vcc3_3	3.3	0.357
VccAClk	1.1	0.052
VccADAC	3.3	0.069
VccADPLLA	1.1	0.068
VccADPLLB	1.1	0.069
Vccap11EXP	1.1	0.04
VccCore	1.1	1.432
VccDMI	1.1	0.058
VccDMI	1.1	0.061
VccFDIPLL	1.1	0.037
VccIO	1.1	3.062
VccLAN	1.1	0.32
VccME	1.1	1.849
VccME3_3	3.3	0.085
VccpNAND	1.8	0.156
VccRTC	3.3	2 (mA)
VccSATAPLL	1.1	0.031
VccSus3_3	3.3	0.163
VccSusHDA	3.3	0.006
VccVRM	1.8 / 1.5	0.196
VccALVDS	3.3	< 1 (mA)
VccTX_LVDS	1.8	0.059

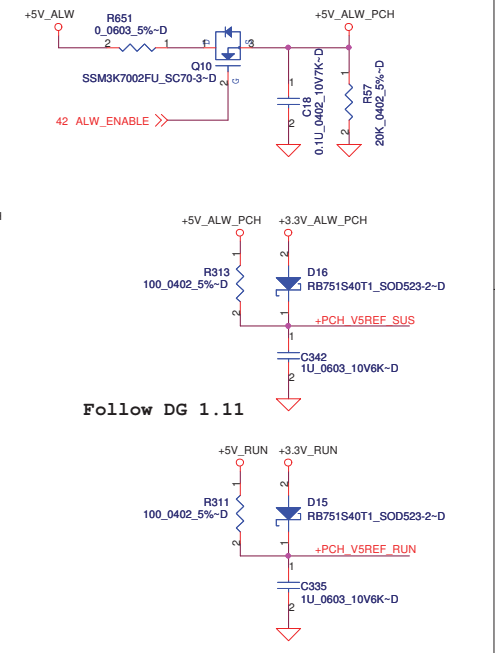
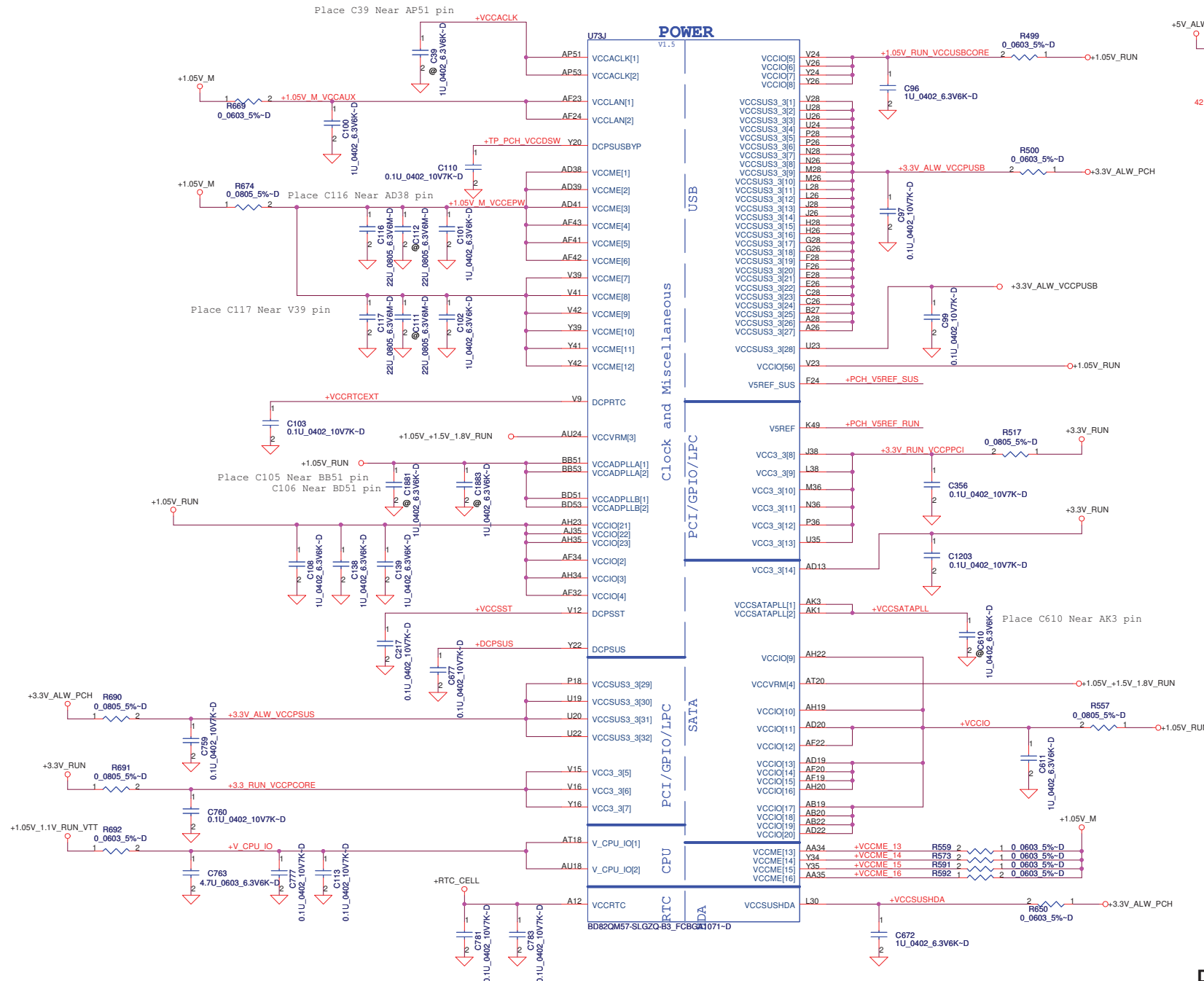
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Title: **PCH (6/8)**

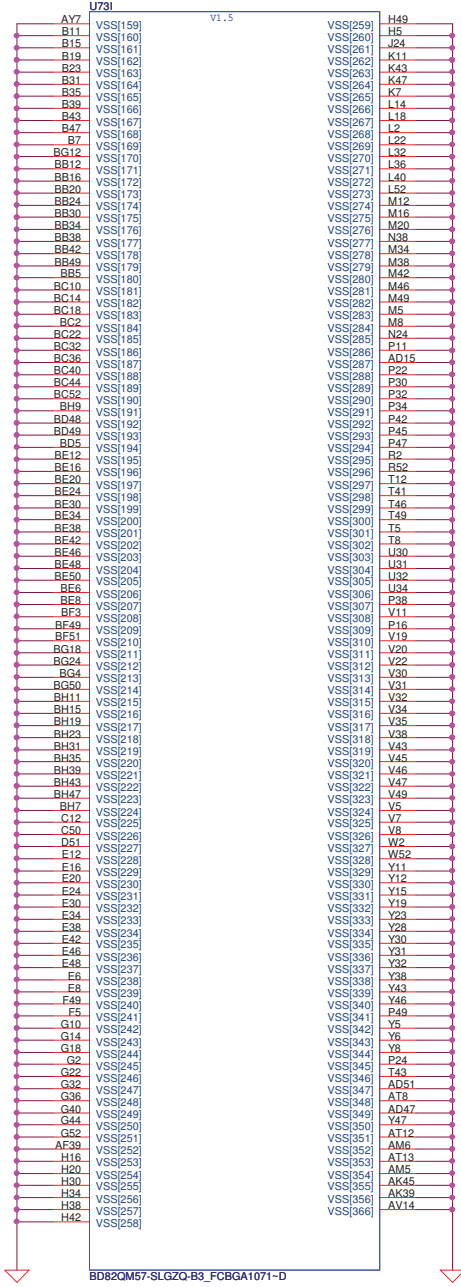
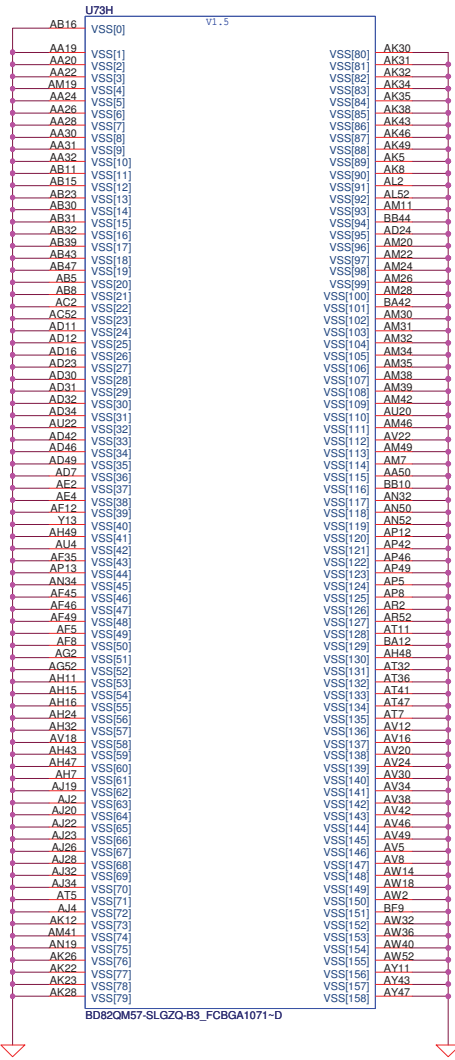
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Follow DG 1.11

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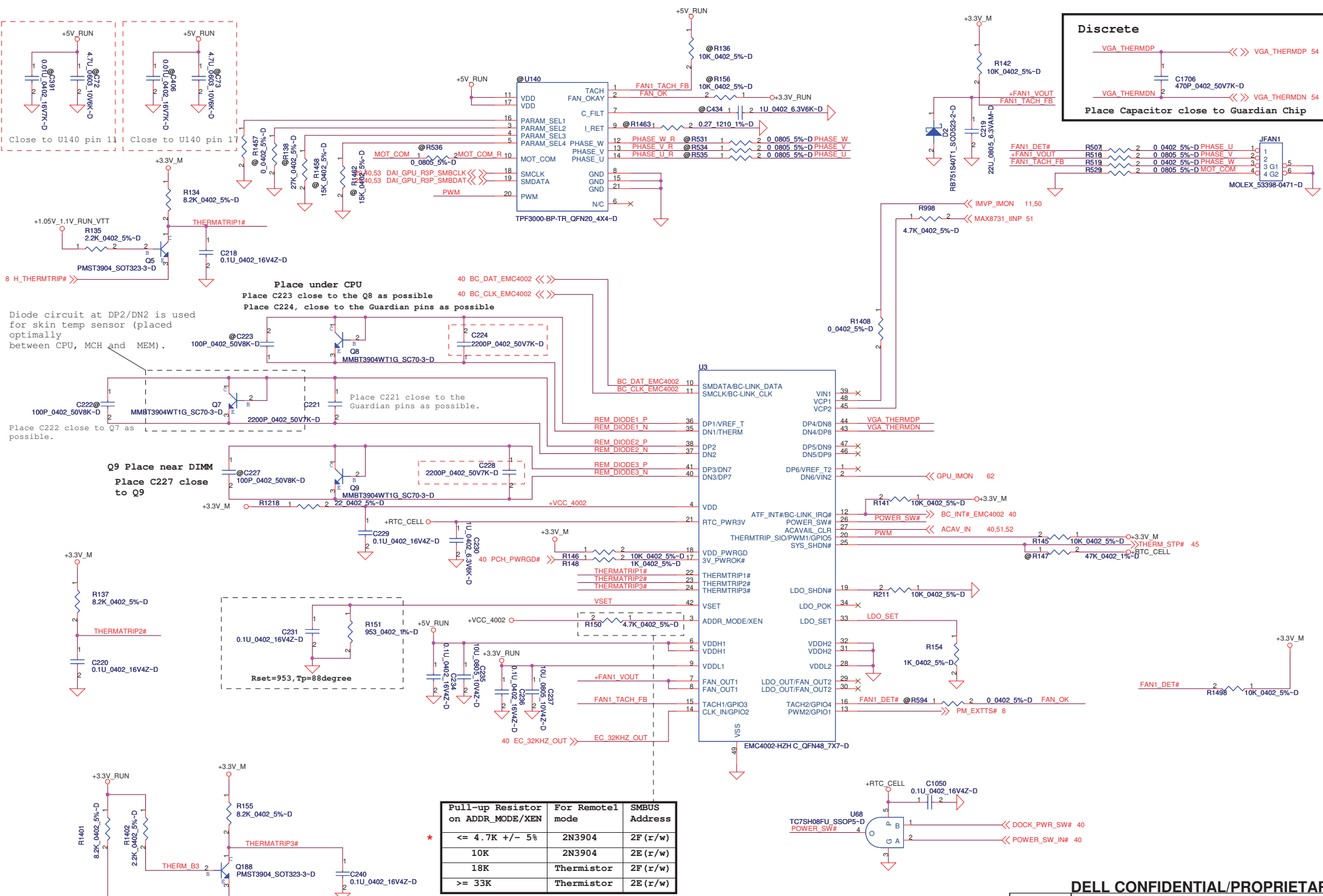


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Title: PCH (8/8)

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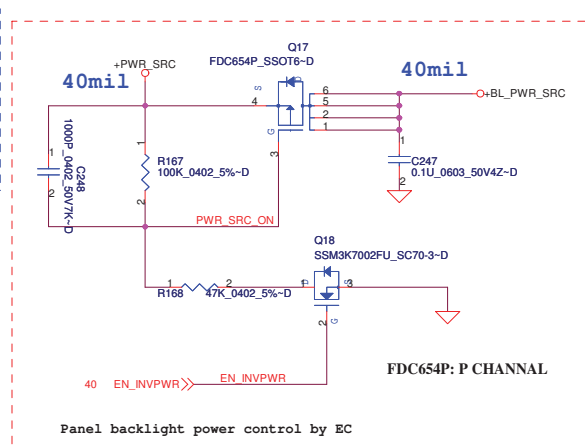
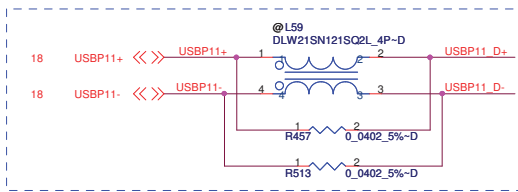
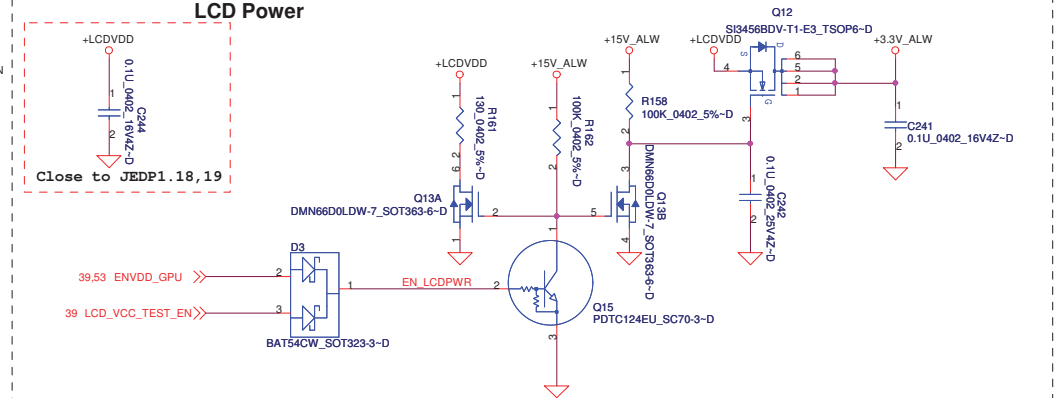
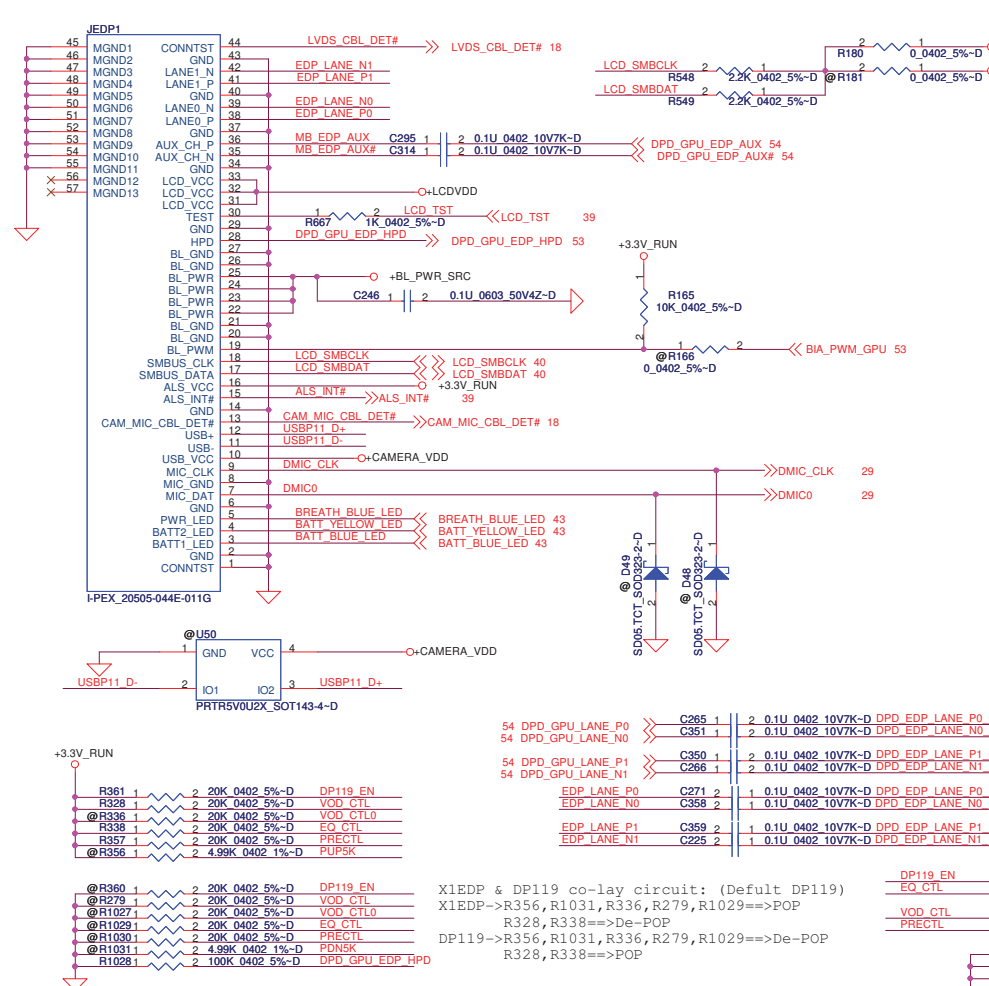
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FAN & Thermal Sensor

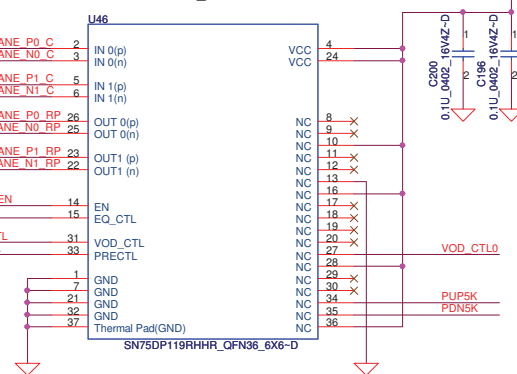
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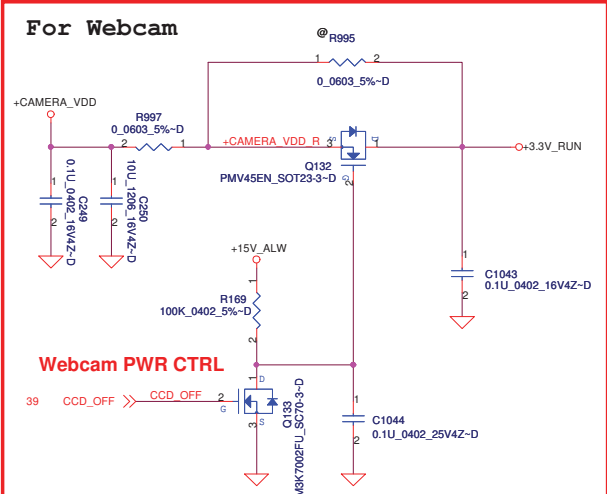
eDP Repeater



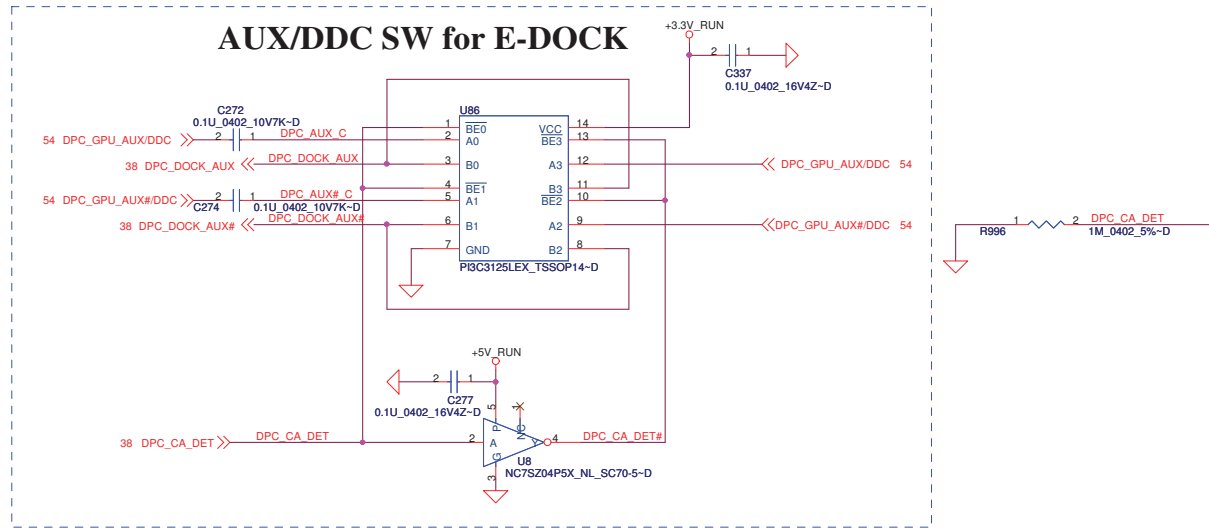
Refer to SN75DP119RHHR rev. 0P35

VOD (mV)	PRE (dB)	PRECTL	VOD_CTL	EQ gain (dB)	EQ_CTL
300	2.5	0	0	0	0
	6	VCC/2	0	3	VCC/2
	8.5	1	0	6	1
400	0	0	VCC/2	*	*
	3.5	VCC/2	VCC/2		
600	0	0	1		
	2	VCC/2	1		
800	0	1	1		

MODE	DP119_EN
PWR Down	0
OUT2 DIS	VCC/2
OUT1 OUT2 EN	1



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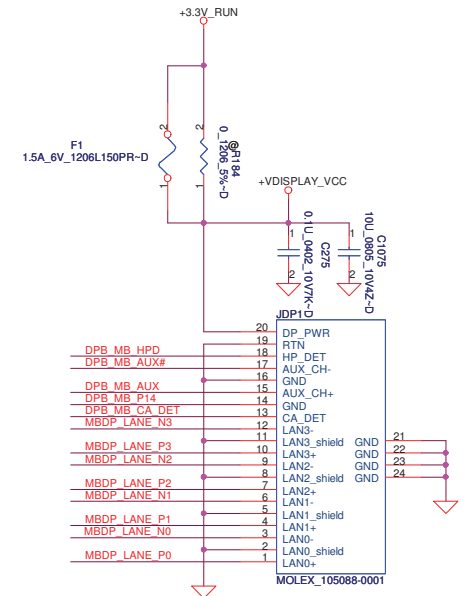
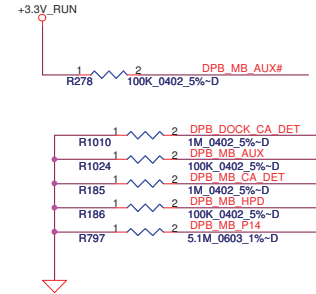
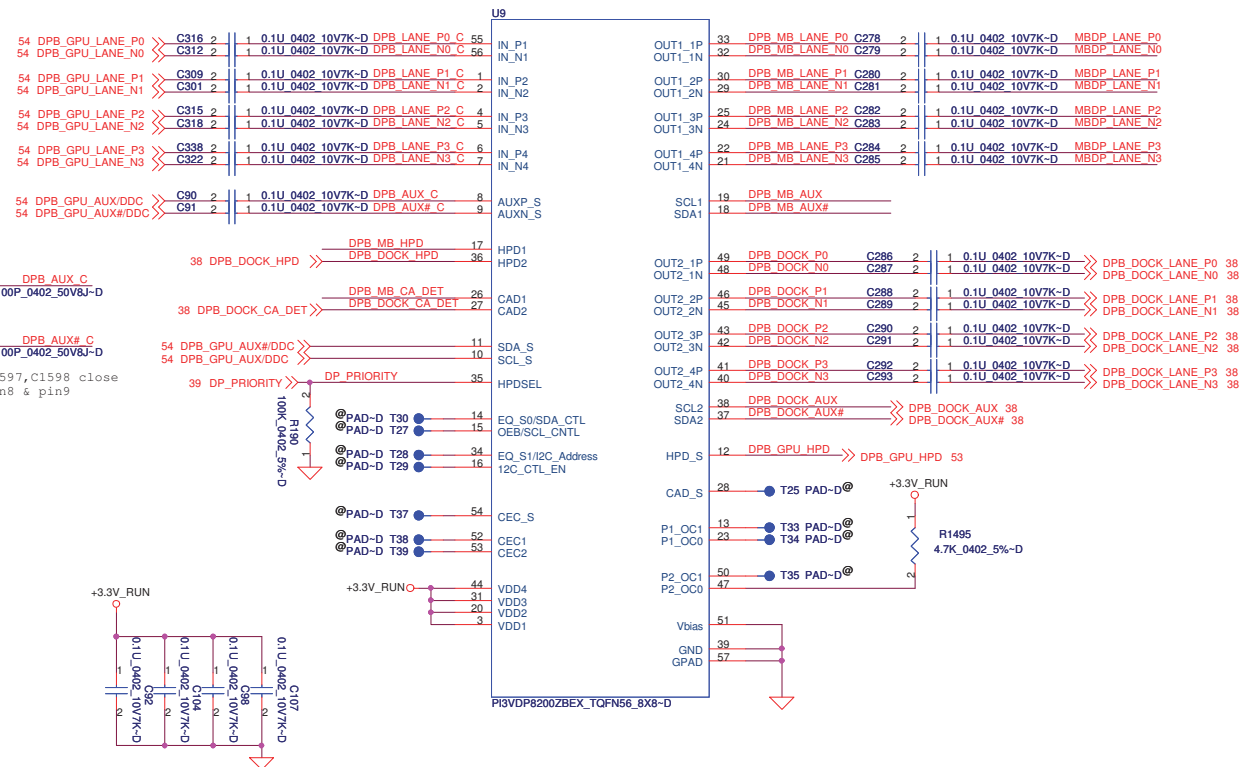


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DPB SW for MB & DOCK

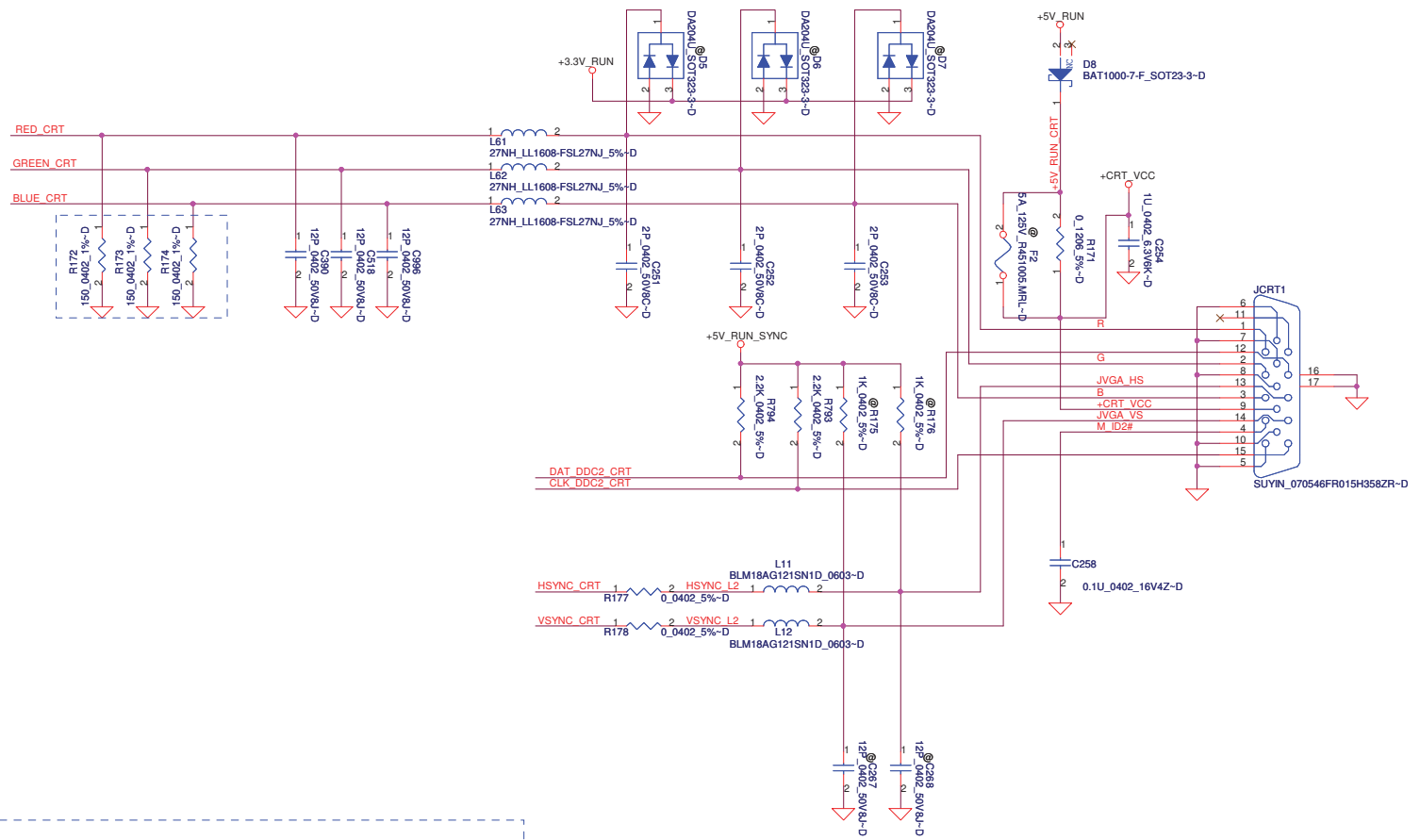


Place C1597, C1598 close to U9 pin8 & pin9

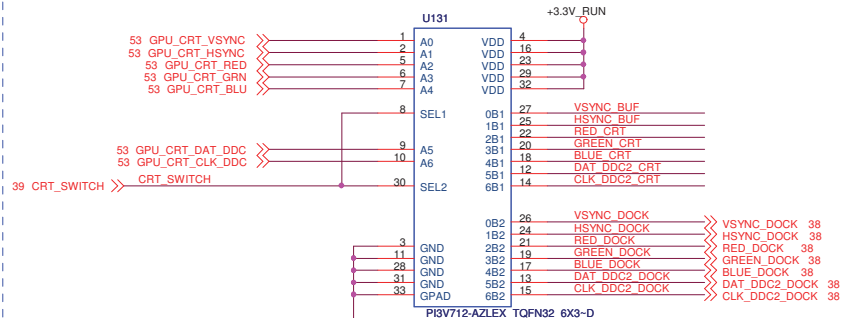
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Compal Electronics, Inc.			
Title: Display port			
Size	Document Number	Rev	
	LA-5573P	0.1	
Date:	Thursday, January 21, 2010	Sheet	26 of 69

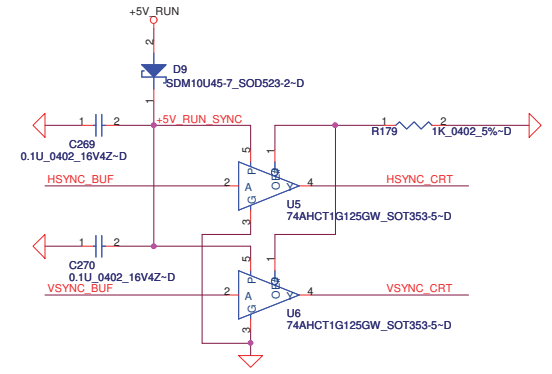
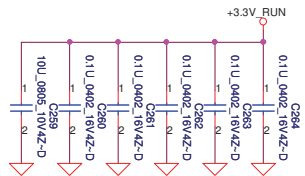
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VGA SW for MB/DOCK



SEL1/SEL2	Chanel	Source
0	A=B1	MB
1	A=B2	APR/SPR

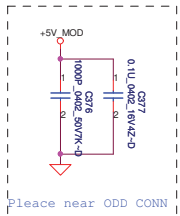


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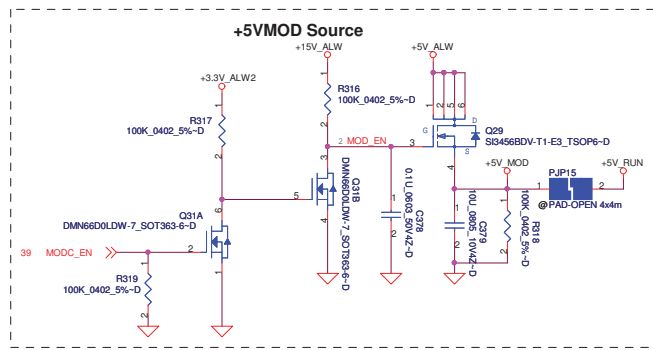
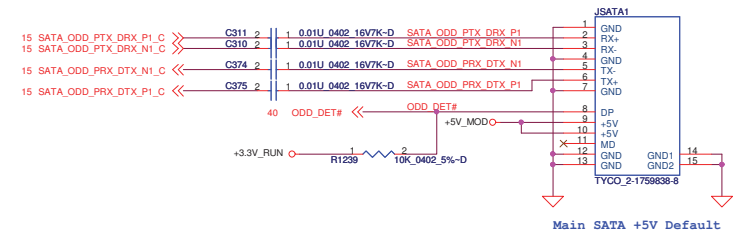
Compal Electronics, Inc.			
CRT/Video switch			
Size	Document Number	Rev	
	LA-5573P	0.1	
Date:	Thursday, January 21, 2010	Sheet	27 of 69

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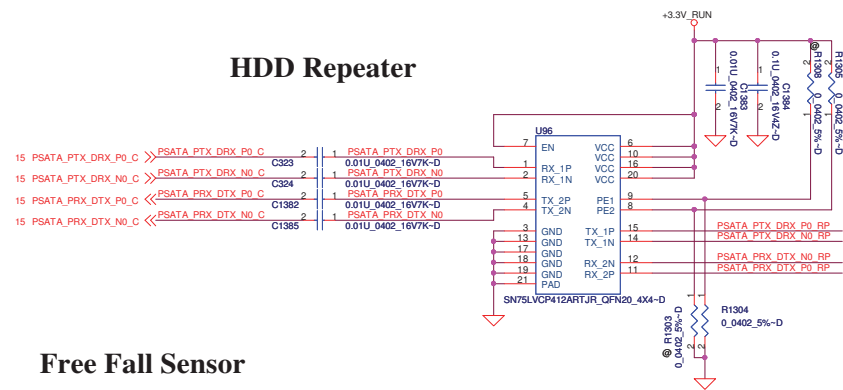
<http://laptop-motherboard-schematic.blogspot.com/>



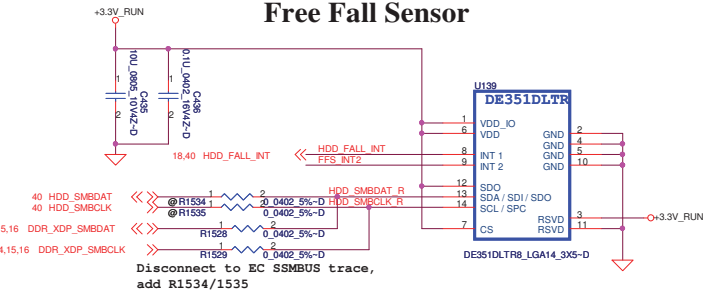
For ODD



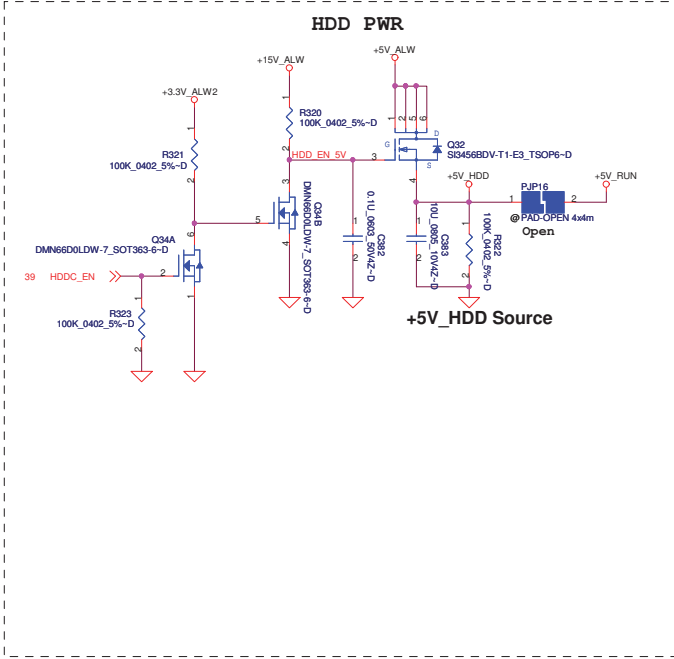
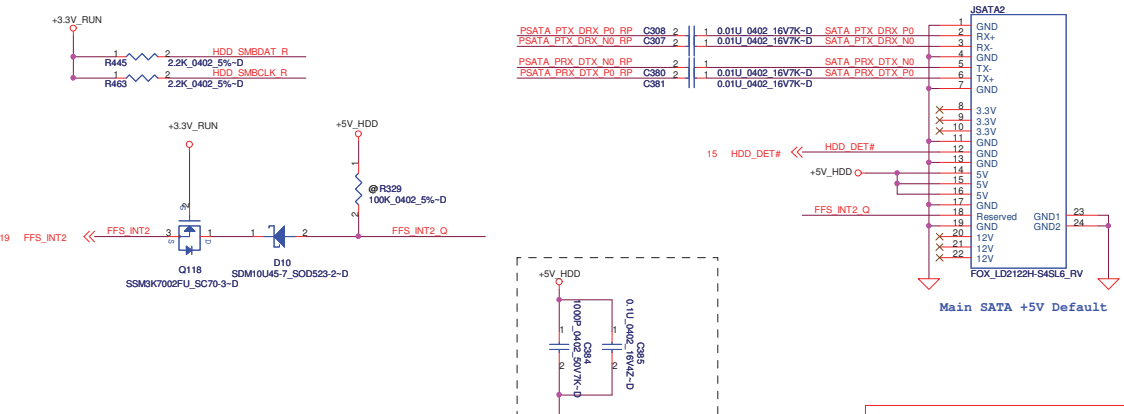
HDD Repeater



Free Fall Sensor



For HDD Temp.



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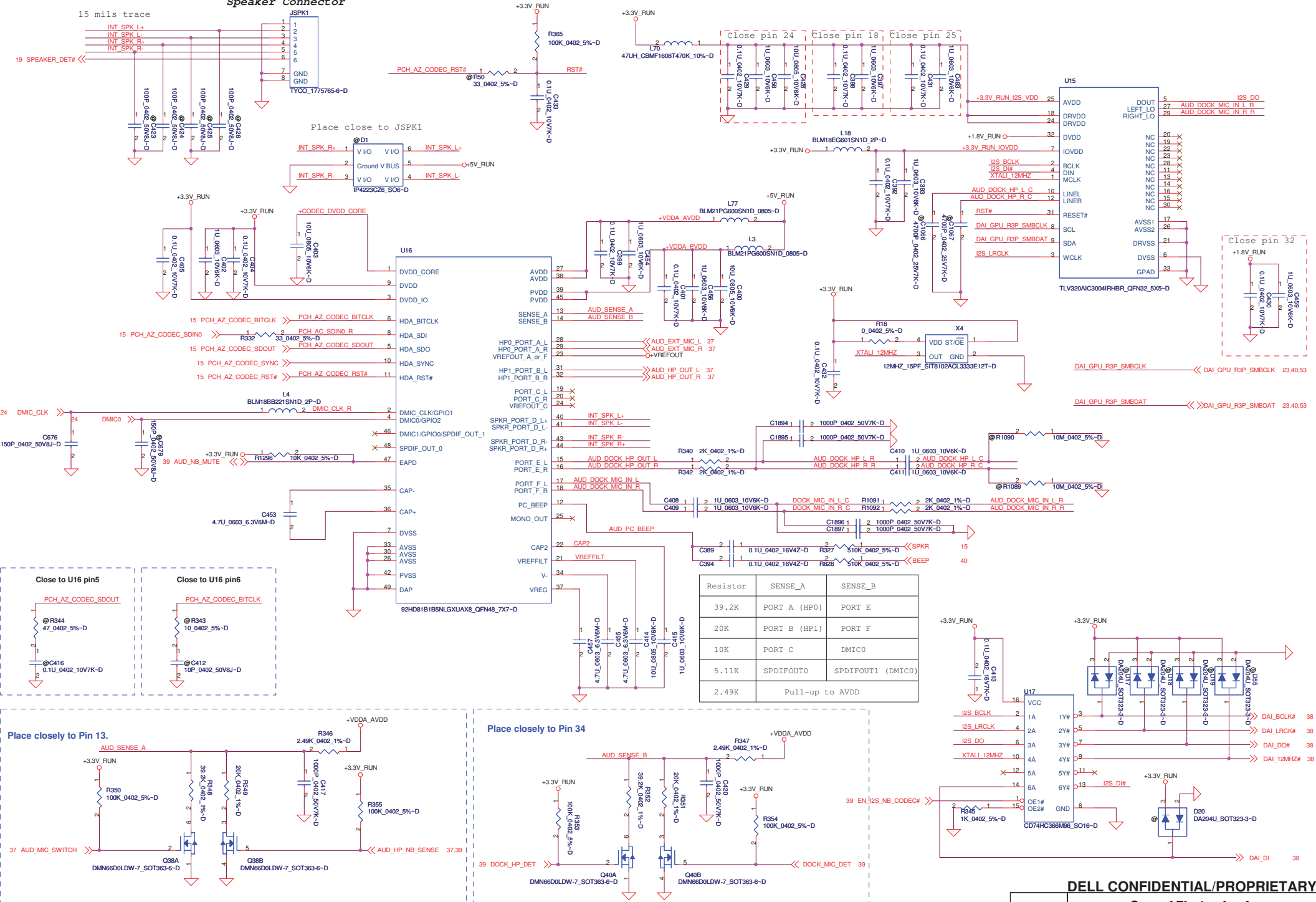
Compal Electronics, Inc.

File		ODD/HDD CONNECTOR	
Doc No		LA-5573P	
Date	Thursday, January 21, 2010	Sheet	28 of 69

<http://laptop-motherboard-schematic.blogspot.com/>

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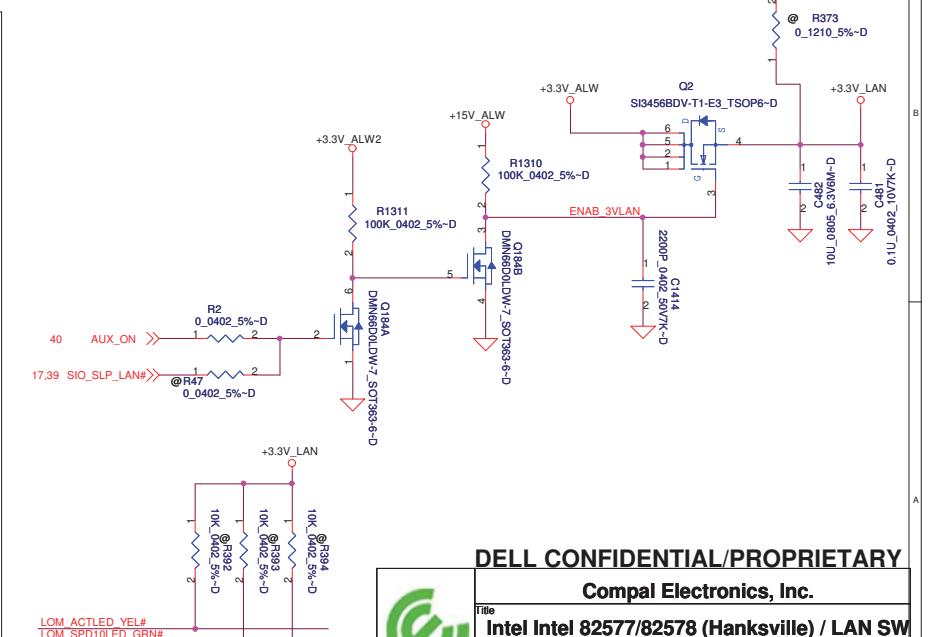
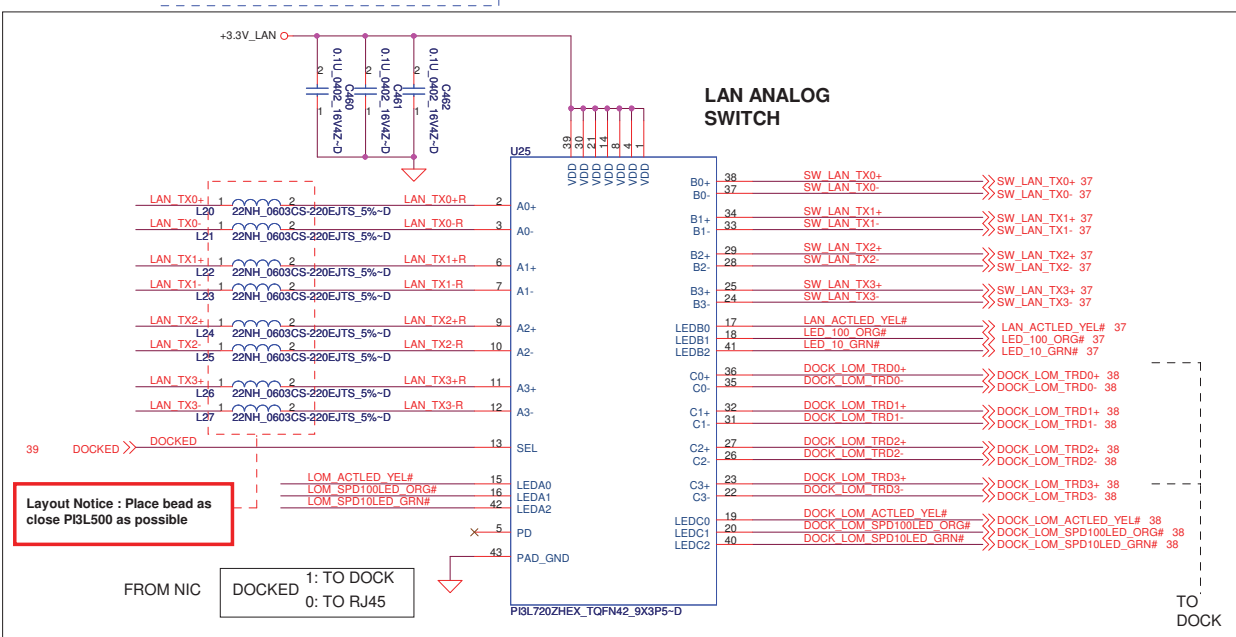
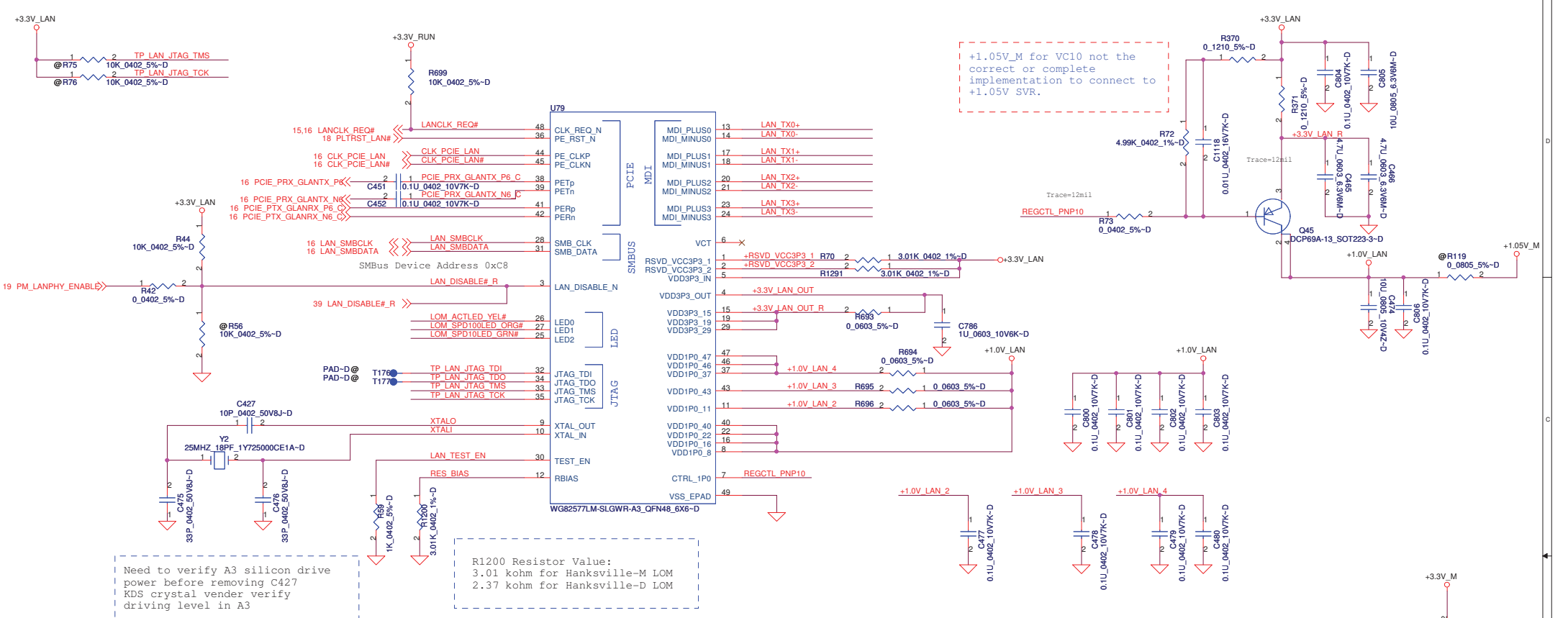
Speaker Connector

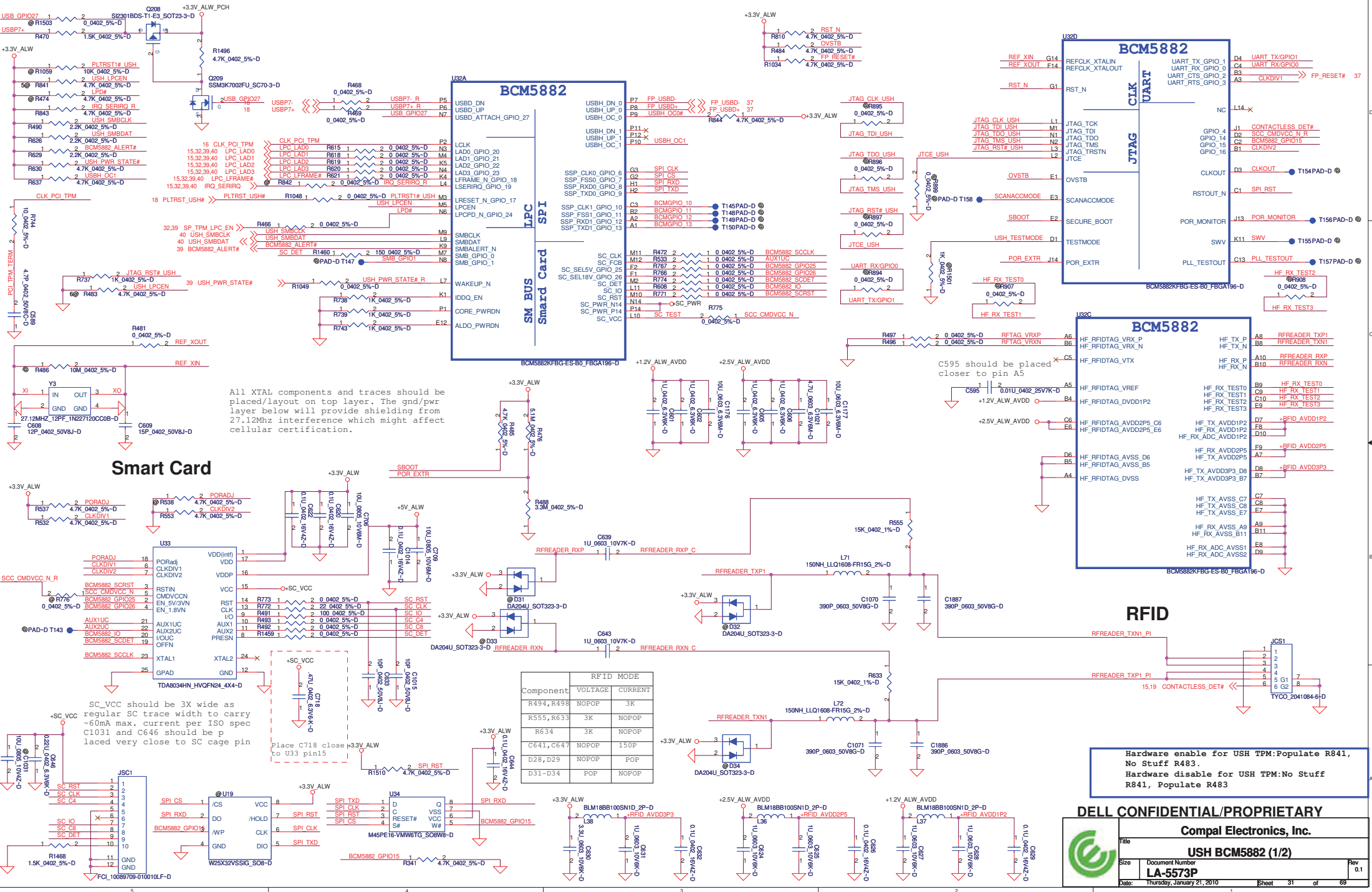


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Compal Electronics, Inc.			
Title: Azalia (HD) Codec			
Size:	Document Number:	Rev: 0.1	
Date: Thursday, January 21, 2010		Sheet: 29	of: 69

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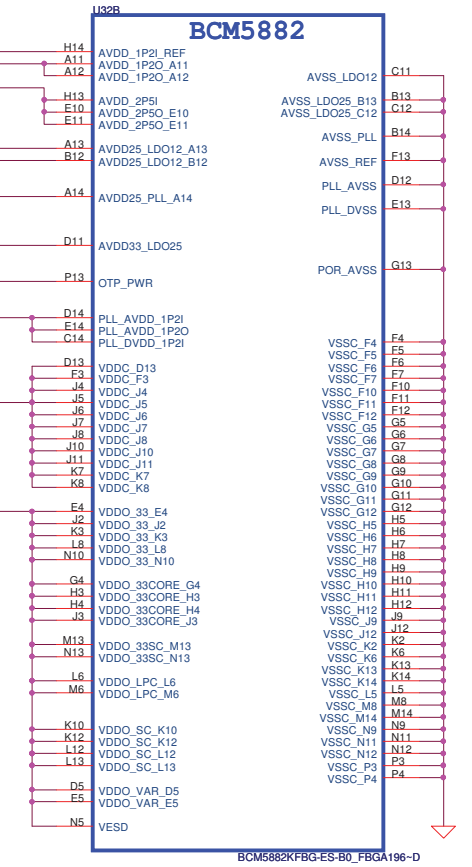
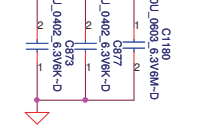
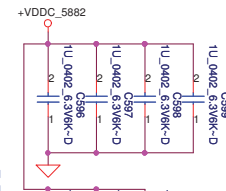
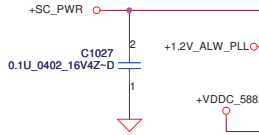
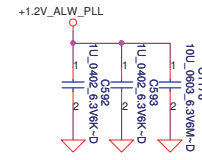
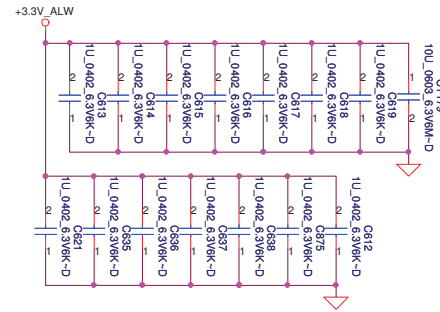
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Compal Electronics, Inc.

USH BCM5882 (1/2)

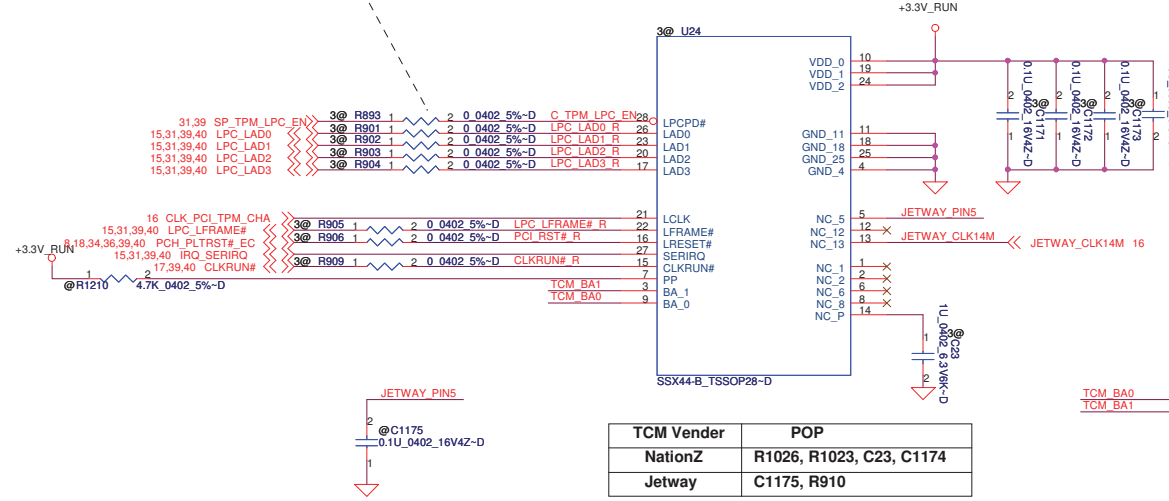
File: _____
 Size: _____ Document Number: **LA-5573P** Rev: 0.1
 Date: Thursday, January 21, 2010 Sheet 31 of 69

USH BCM5882 and China TCM Z8H172T Option				
PART/PIN	Ref Des	TCM Enable	TPM Enable	ALL TPM/TCM Disable
TCM circuit	All 3@	POP	@	@
USH_LPCEN	PU R841	@	POP	@
PD R483	POP	@	@	@
SIO 5028 ->SP_TPM_LPC_EN	PU R788	@	@	@
PCH GPIO39 ->TPM_ID1	PU R787	@	@	POP
PD R339	POP	POP	POP	@
PCH GPIO38 ->TPM_ID0	PU R273	POP	POP	@
PD R922	@	@	@	POP



LOW:Power Down Mode
High:Working Mode

China TCM: NationZ & Jetway co-lay



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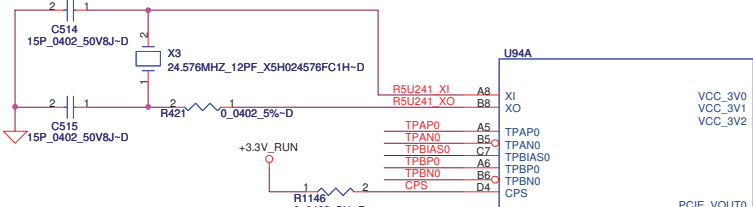
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LA-573P

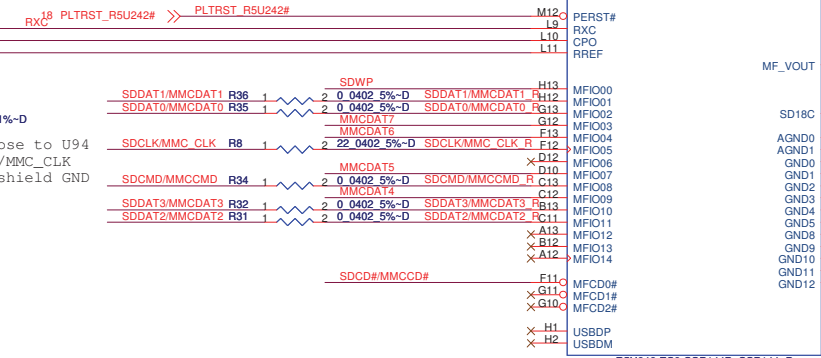
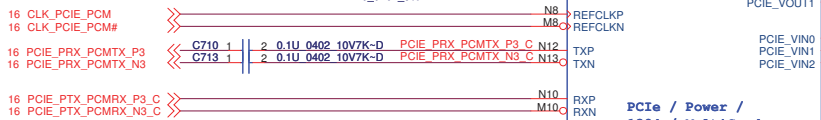
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Crystal close to U94



C710, C713 as close as possible to U94

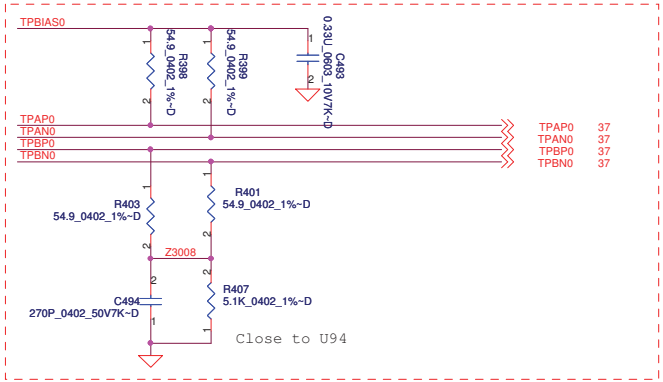
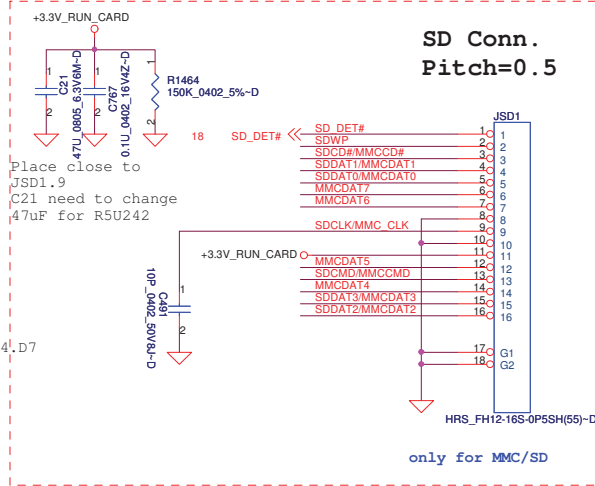
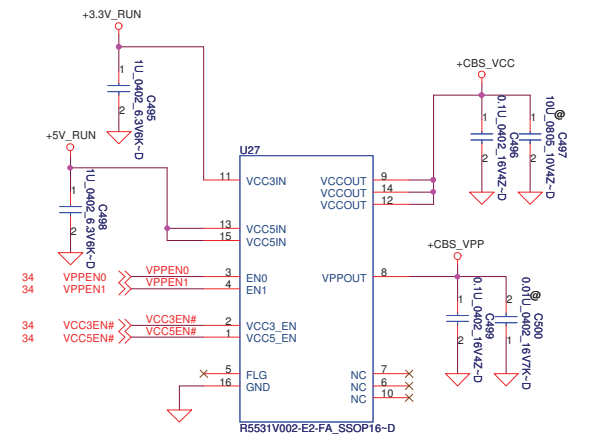
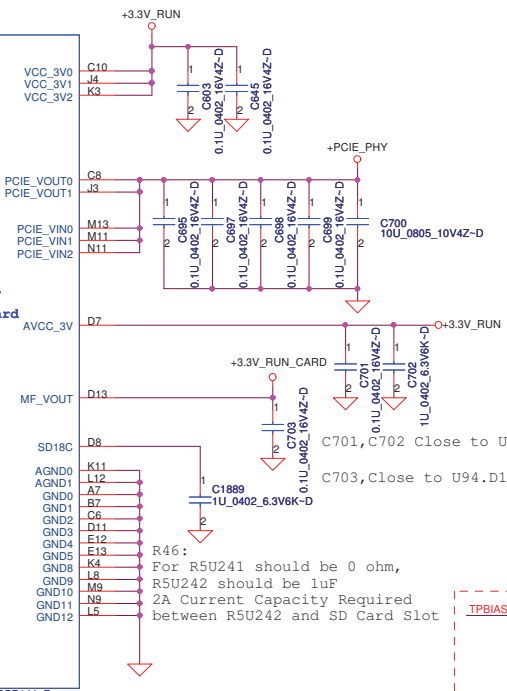


C707, C705, R1148 as close as possible to U94

MFIO Pin Assignment Table

MFIO	SD8	XD	MS8
00	WP	D7	BS
01	D1	D6	-
02	D0	D5	D1
03	D7	D4	-
04	D6	D3	D5
05	CLK	D2	D0
06	-	D1	-
07	D5	D0	D4
08	CMD	WP#	D2
09	D4	WE#	D6
10	D3	ALE	D3
11	D2	CLE	-
12	-	CE#	-
13	-	RE#	D7
14	-	R/B#	CLK

C645, Close to U94.C10
 C603, Close to U94.J4/K3
 C695, Close to U94.M13
 C697, Close to U94.M11/N11
 C698, Close to U94.J3
 C699, Close to U94.C8



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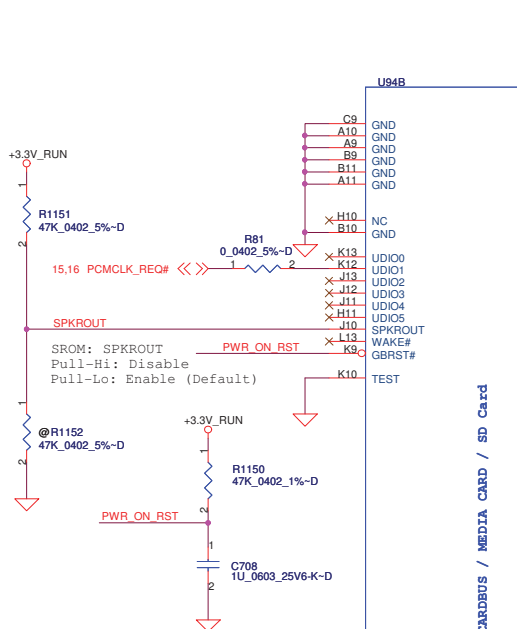
Document Number R5U242 (1/2)

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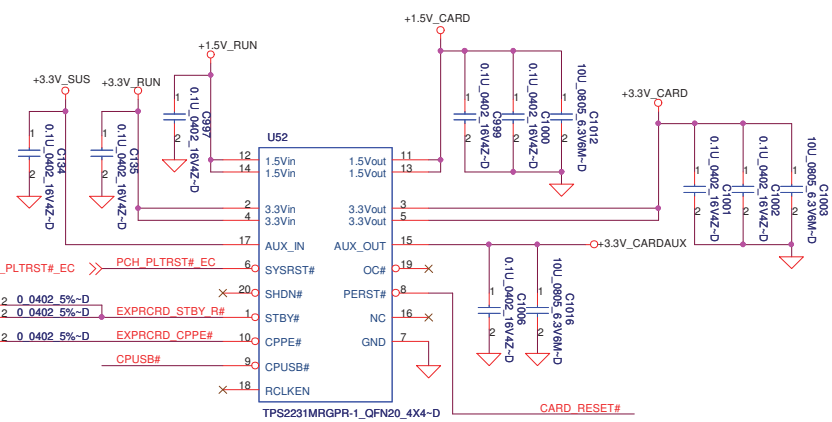
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CADR25	L2	CBS CAD19
CADR24	K2	CBS CAD17
CADR23	H4	CBS CFRAME#
CADR22	J1	CBS CTRDY#
CADR21	G3	CBS CDEVSEL#
CADR20	F3	CBS CSTOP#
CADR19	G2	CBS CBLOCK#
CADR18	F2	CBS DATA18
CADR17	E2	CBS CAD16
CADR16	H3	CBS CO/BE1#
CADR15	J2	CBS CIRDY#
CADR14	G1	CBS CPERR#
CADR13	F1	CBS CPAR#
CADR12	K1	CBS CO/BE2#
CADR11	C2	CBS CAD12
CADR10	C3	CBS CAD9
CADR9	D2	CBS CAD14
CADR8	E3	CBS CO/BE1#
CADR7	M1	CBS CAD20
CADR6	M2	CBS CAD21
CADR5	L3	CBS CAD22
CADR4	N3	CBS CAD23
CADR3	N4	CBS CAD25
CADR2	M4	CBS CAD26
CADR1	M4	CBS CAD26
CADR0	M4	CBS CAD26

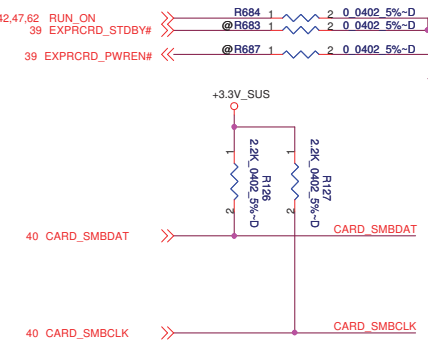
R410 Close to U94, CBS_CCLK need shield GND



Express Card BTB Conn.

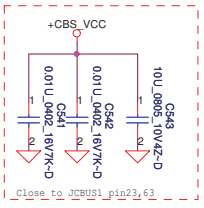
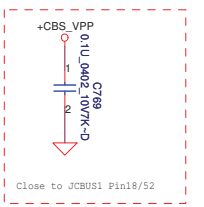
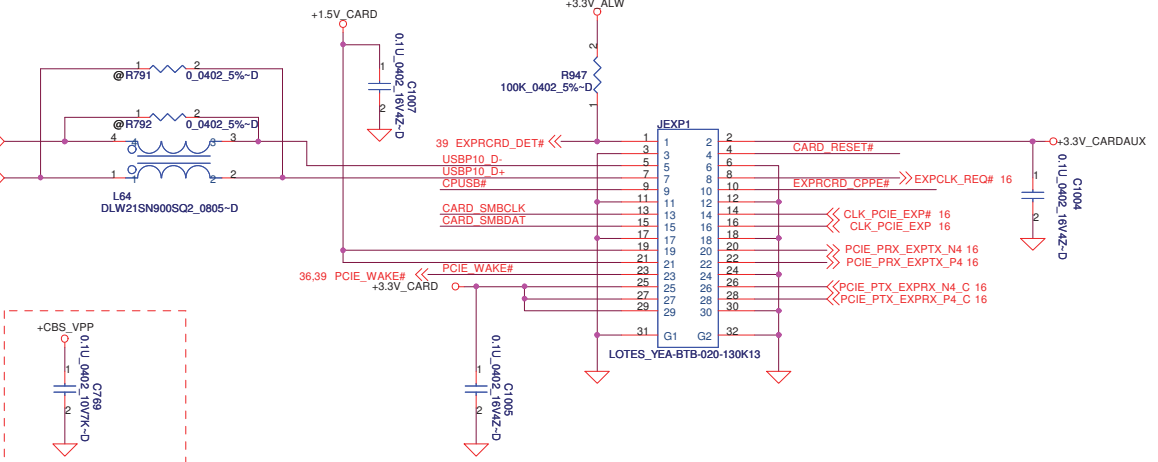
+1.5V_CARD: Max. 650mA, Average 500mA
+3.3V_CARD: Max. 1300mA, Average 1000mA

Power-On-Reset: GBRST# (Global Reset)
 Note: De-asserted BEFORE PERST# de-assertion



33	VPPEN1	VPPEN1	D9	VPPEN1
33	VPPEN0	VPPEN0	F10	VPPEN0
33	VCC3EN#	VCC3EN#	E11	VCC3EN#
33	VCC5EN#	VCC5EN#	E11	VCC5EN#

CE#	C1	CBS CAD11
WE#	F4	CBS CGNT#
D3	D3	CBS CAD10
CE2#	D5	CBS CO/BE0#
CE1#	L4	CBS CO/BE3#
RES#	N1	CBS CRST#
RESET	N2	CBS CSERR#
WAIT#	L7	CBS COLKRUN#
WPN#/IOIS16#	G4	CBS CINT#
RDY#/REC#	L6	CBS AUDIO
BVD1	K7	CBS CSTSCHNG
BVD2	K2	CBS CVS2
VS2#	E4	CBS CVS1
VS1#	K8	CBS CCD2#
CD#	D6	CBS CCD1#
INPACK#	K6	CBS CAD18
IODR#	D1	CBS CAD13
IOWR#	E1	CBS CAD15

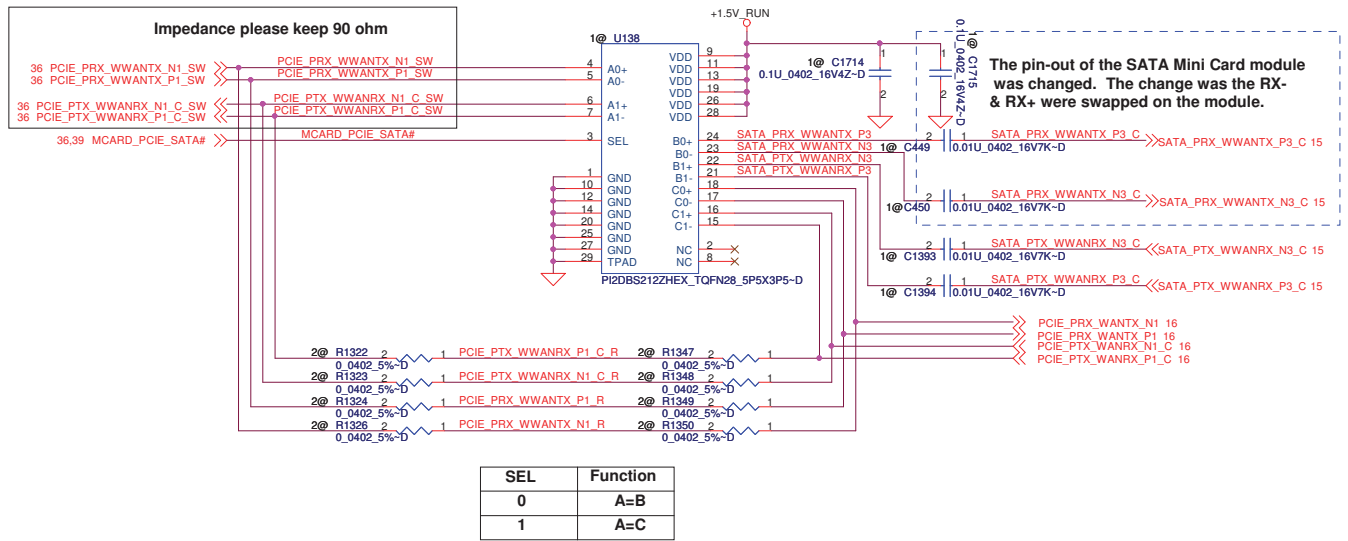


CBS CAD0	1	GND1	35	GND3	35	CBS COD1#
CBS CAD1	2	CAD0	36	CCD1#	37	CBS CAD2
CBS CAD3	3	CAD1	37	CAD2	38	CBS CAD4
CBS CAD5	4	CAD3	38	CAD4	39	CBS CAD6
CBS CAD7	5	CAD5	39	CAD6	40	CBS DATA14
CBS CC/BE0#	6	CAD7	40	CB_D14	41	CBS CAD8
CBS CAD9	7	CAD9	41	CAD8	42	CBS CAD10
CBS CAD11	8	CAD11	42	CVS1	43	CBS CVS1
CBS CAD12	9	CAD12	43	CVS2	44	CBS CAD13
CBS CAD14	10	CAD14	44	CAD13	45	CBS CAD15
CBS CC/BE1#	11	CAD14	45	CAD15	46	CBS CAD18
CBS CPAR#	12	CCBE1#	46	CAD16	47	CBS DATA18
CBS CPERR#	13	CPAR	47	CB_D18	48	CBS CBLOCK#
CBS CGNT#	14	CPERR#	48	CBLCK#	49	CBS CSTOP#
CBS CINT#	15	CGNT#	49	CSTOP#	50	CBS CDEVSEL#
VCC	16	CINT#	50	CDEVSEL#	51	
+CBS_VCC	17	VCC	51	VCC	52	
+CBS_VPP	18	VPP1	52	VPP2	53	CBS CTRDY#
CBS_CCLK	19	CCLK	53	CTRDY#	54	CBS CFRAME#
CBS CIRDY#	20	CIRDY#	54	CFRAME#	55	CBS CAD17
CBS CO/BE2#	21	CCBE2#	55	CAD17	56	CBS CAD19
CBS CAD18	22	CAD18	56	CAD19	57	CBS CVS2
CBS CAD20	23	CAD20	57	CVS2	58	CBS CRST#
CBS CAD21	24	CAD21	58	CRST#	59	CBS CSERR#
CBS CAD22	25	CAD22	59	CSERR#	60	CBS CREQ#
CBS CAD23	26	CAD23	60	CREQ#	61	CBS CO/BE3#
CBS CAD24	27	CAD24	61	CO/BE3#	62	CBS AUDIO
CBS CAD25	28	CAD25	62	AUDIO	63	CBS CSTSCHNG
CBS CAD26	29	CAD26	63	CSTSCHNG	64	CBS CAD18
CBS CAD27	30	CAD27	64	CBS CAD8	65	CBS CAD8
CBS CAD29	31	CAD29	65	CBS CAD30	66	CBS CAD31
CBS DATA2	32	CAD29	66	CB_D2	67	CBS CAD2#
CBS_CCLKRUN#	33	CCLKRUN#	67	CAD31	68	
	34	GND2	68	GND4	69	
	69	GND5	71	GND7	71	
	70	GND6	72	GND8	72	



For Asics placement estimate

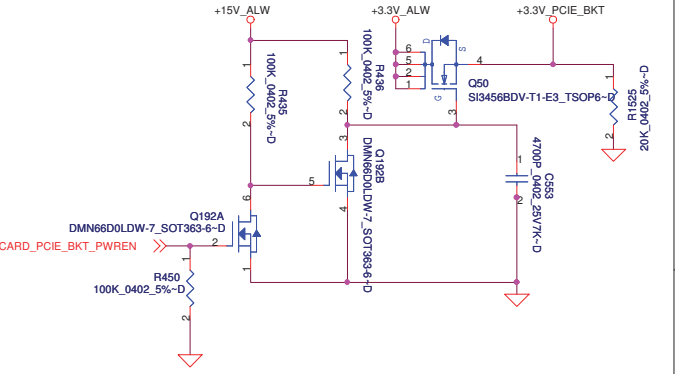
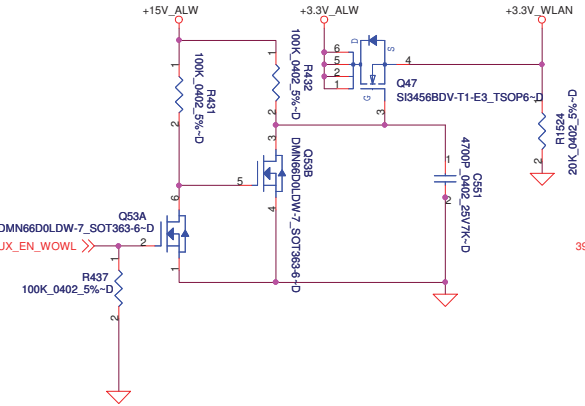
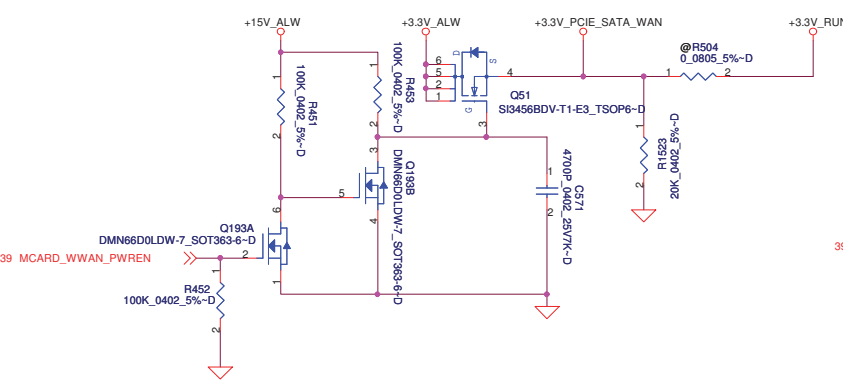
PCIE/SATA SW for Mini card1



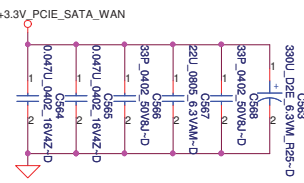
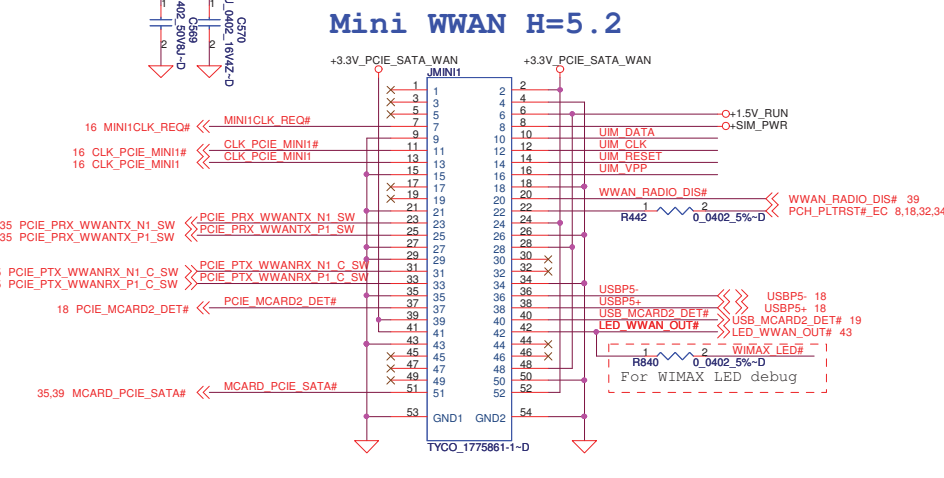
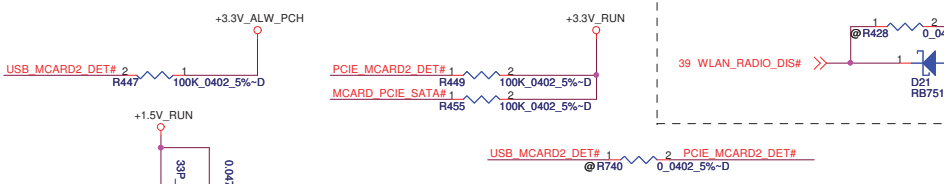
Power Control for Mini card1

Power Control for Mini card2

Power Control for Mini card3

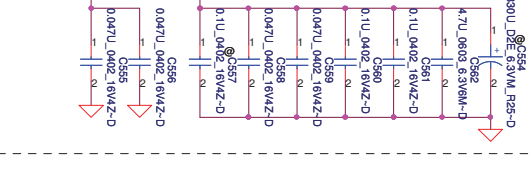
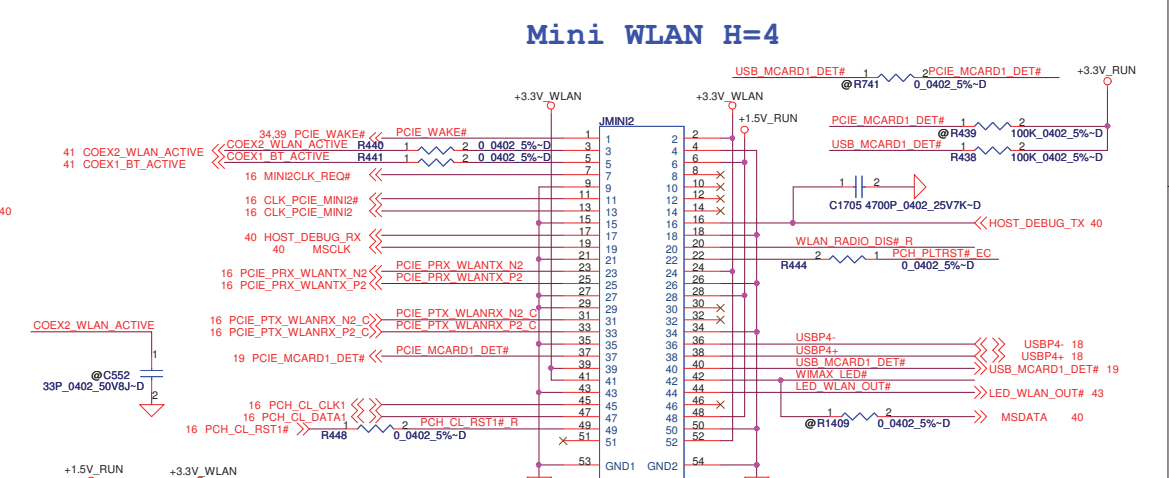
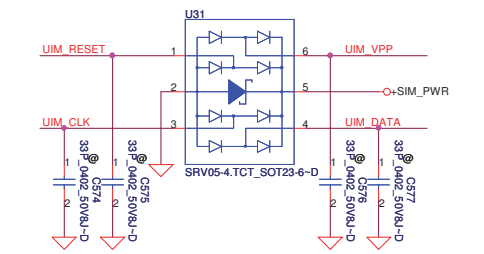
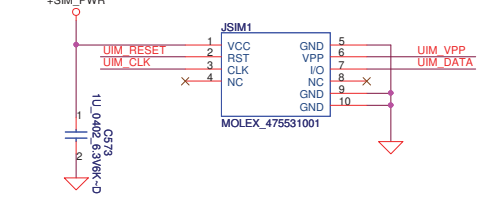


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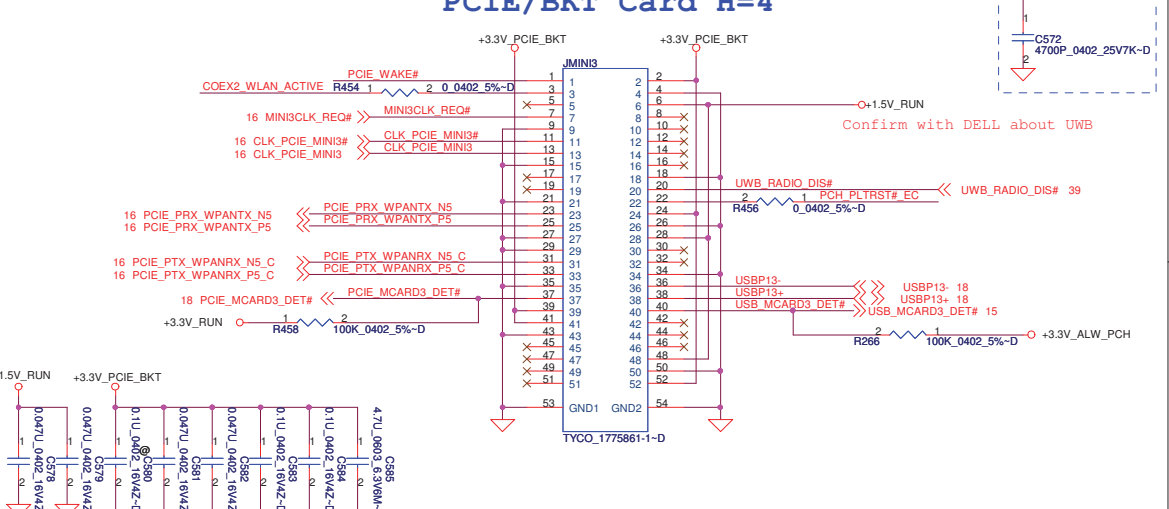


PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+~9%	1000	750	
+3.3Vaux	+~9%	330	250	250 (Wake enable) 5 (Not wake enable)
+1.5V	+~5%	500	375	NA

SIM Card Push-Push



PCIE/BKT Card H=4



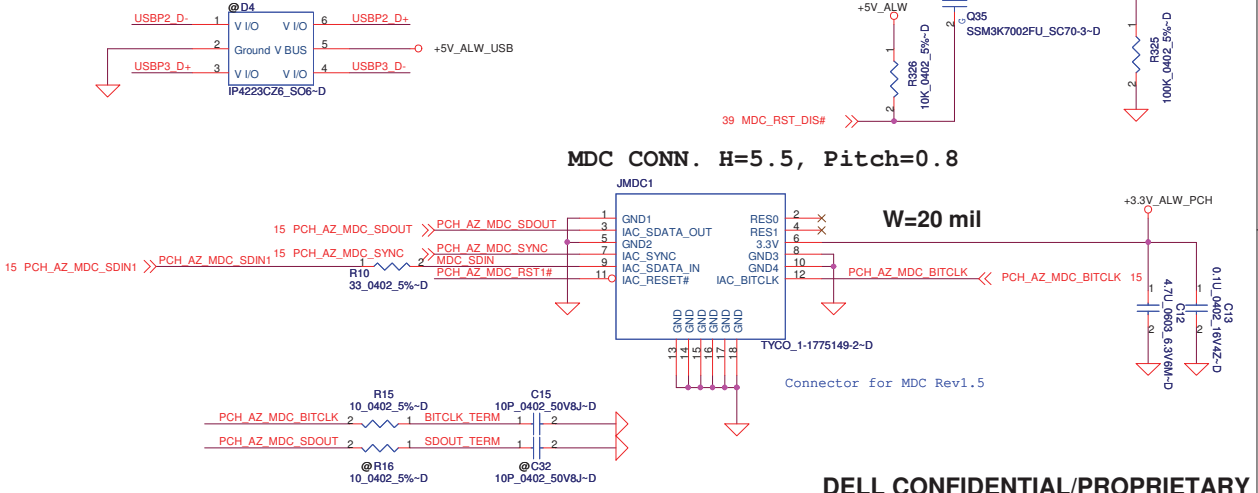
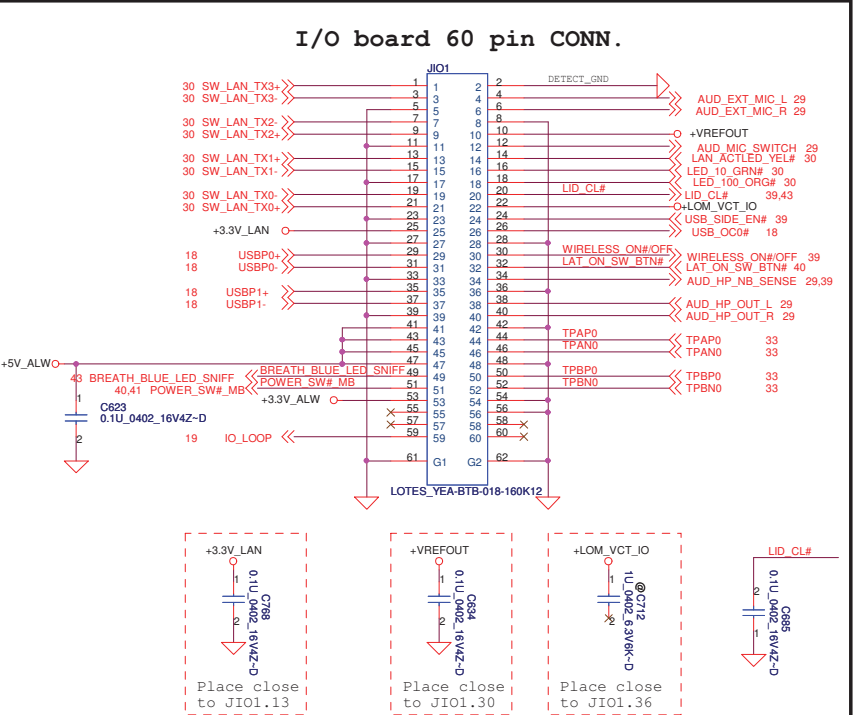
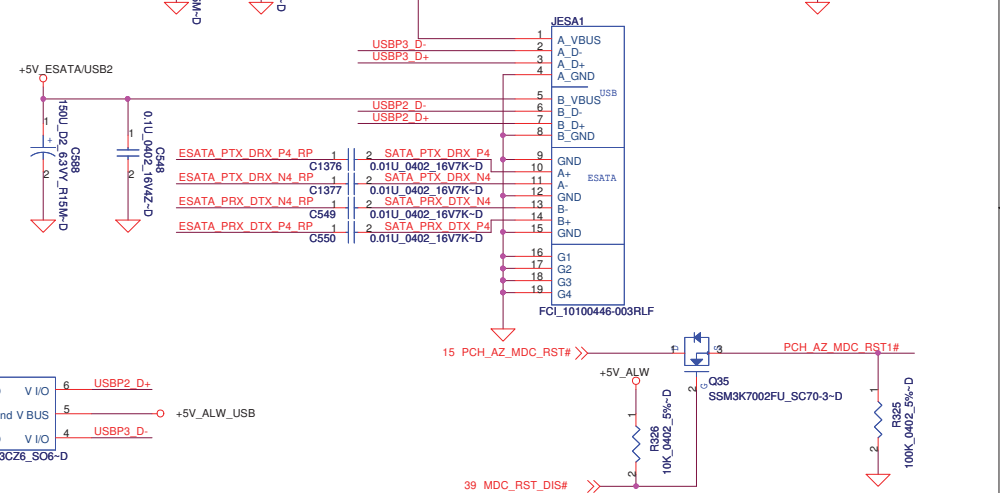
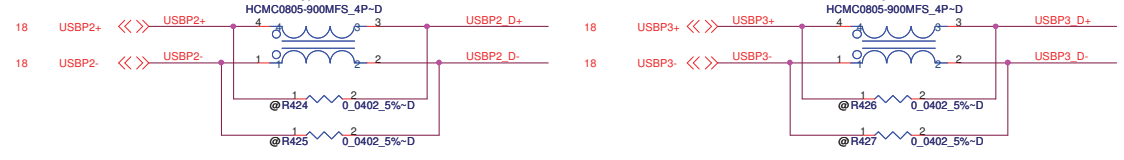
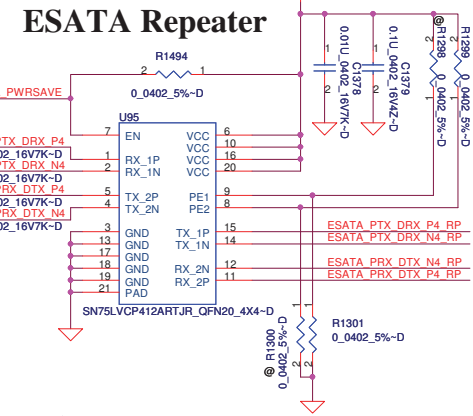
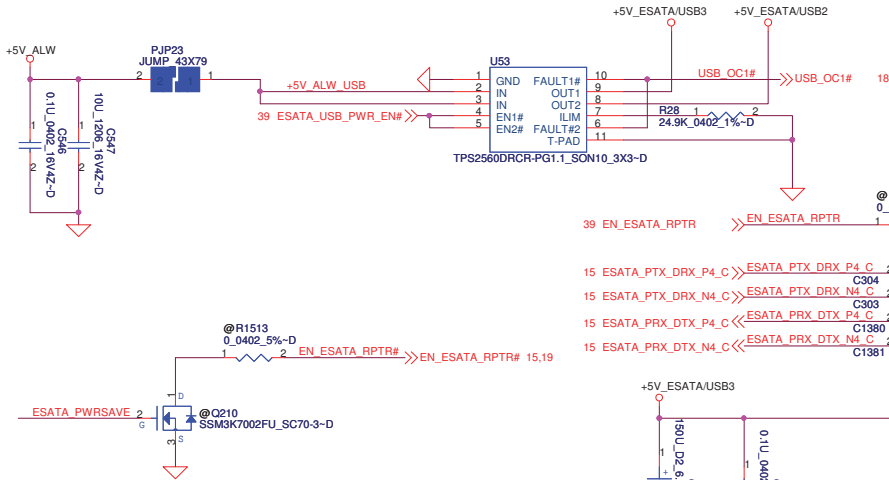
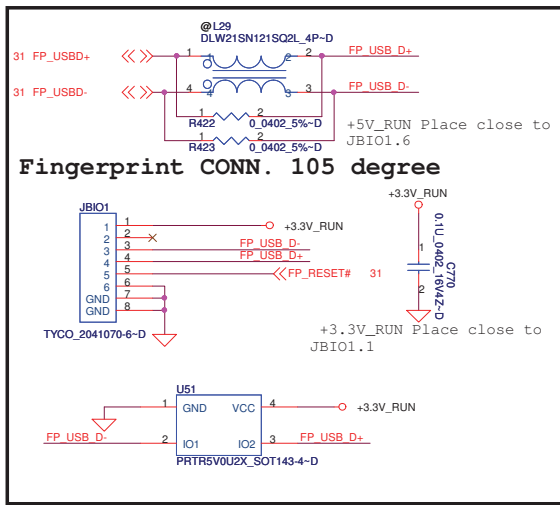
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Title: Mini Card			
Size	Document Number	Rev	
	LA-5573P	0.1	
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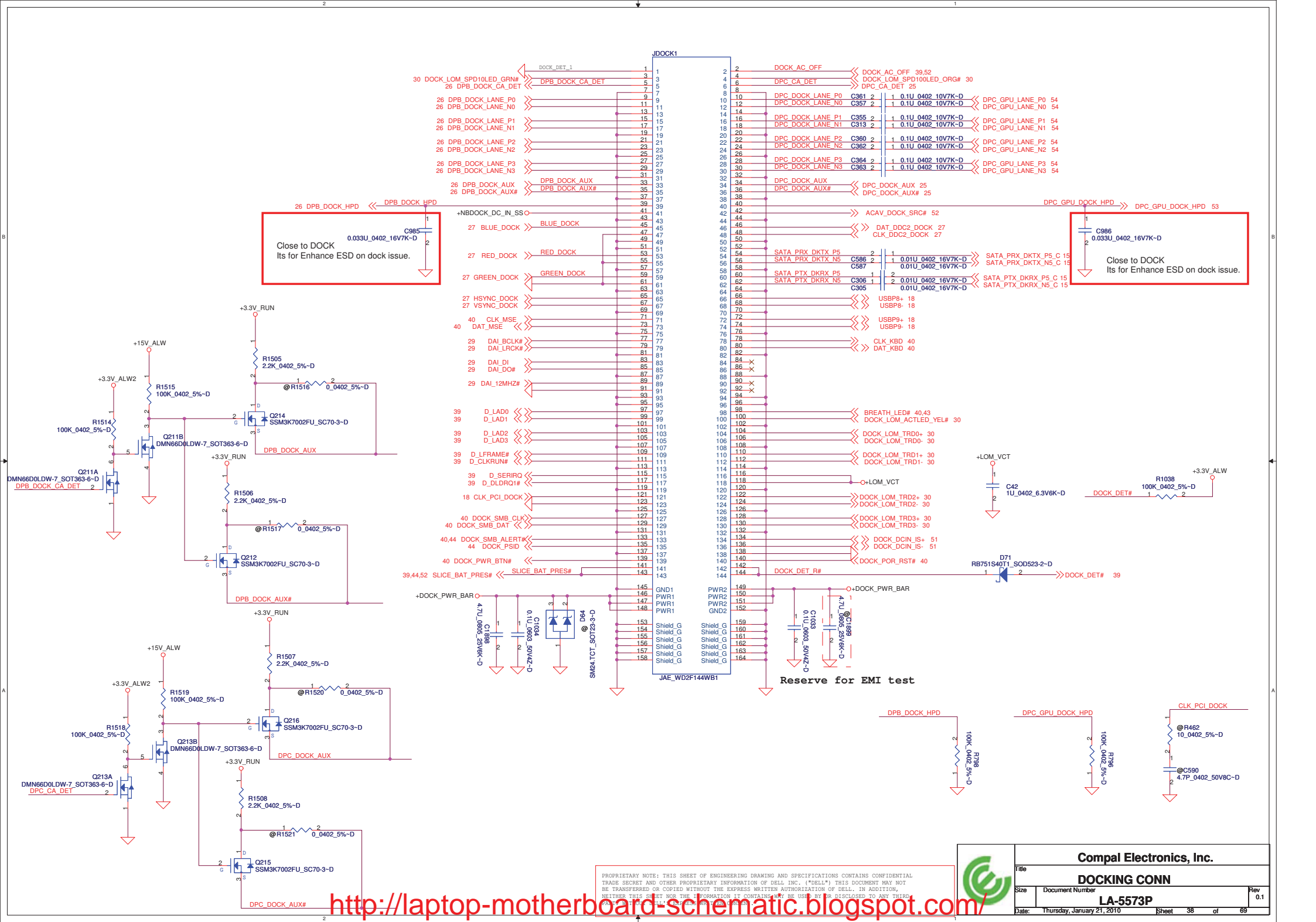
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USB 2.0 PORT

Document Number: **LA-5573P**

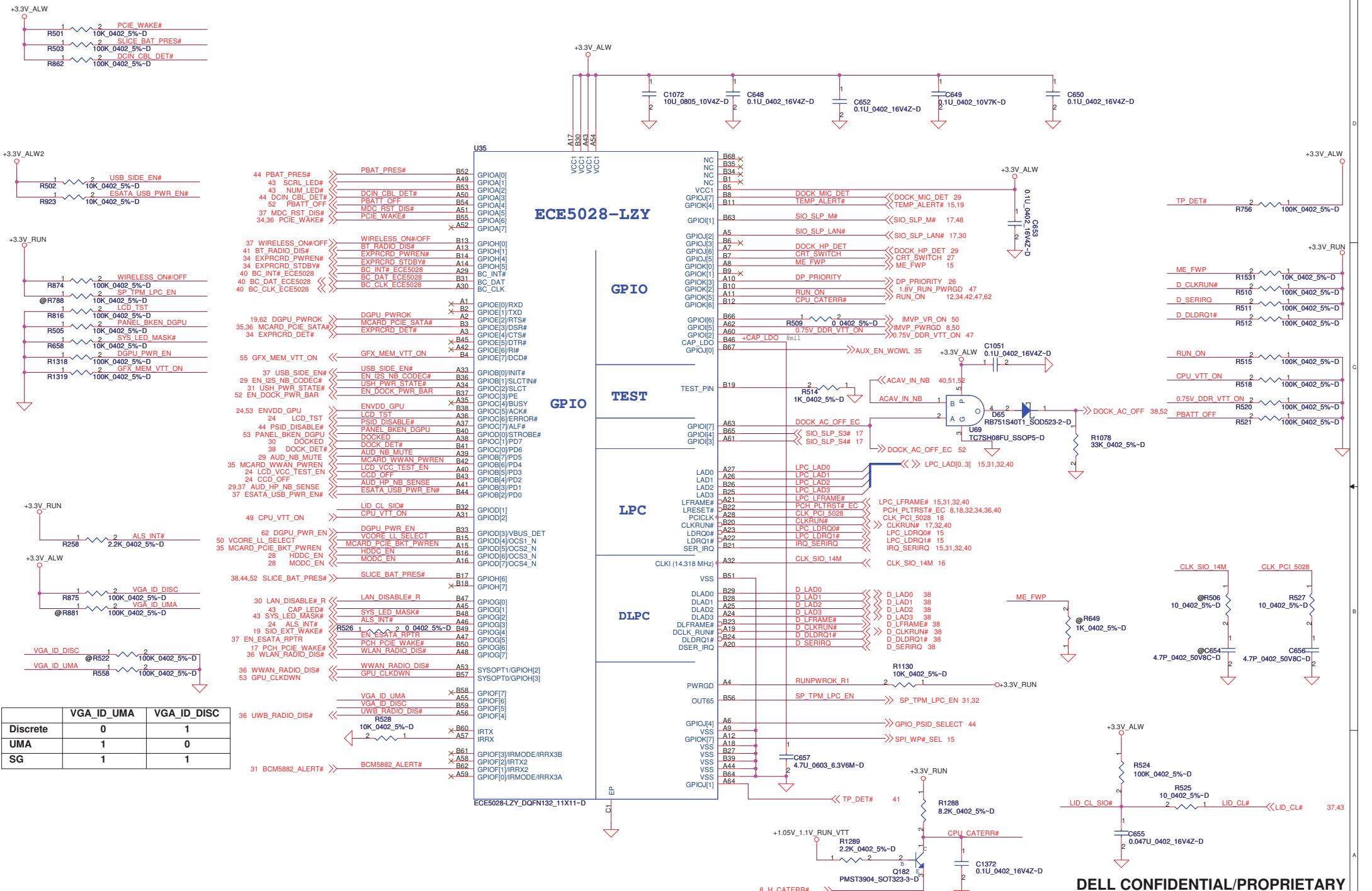
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	VGA_ID_UMA	VGA_ID_DISC
Discrete	0	1
UMA	1	0
SG	1	1

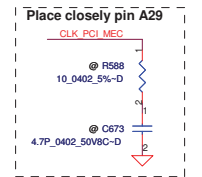
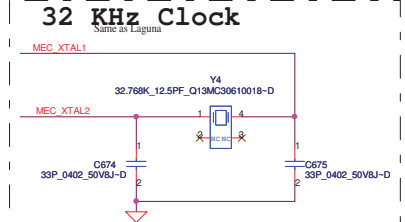
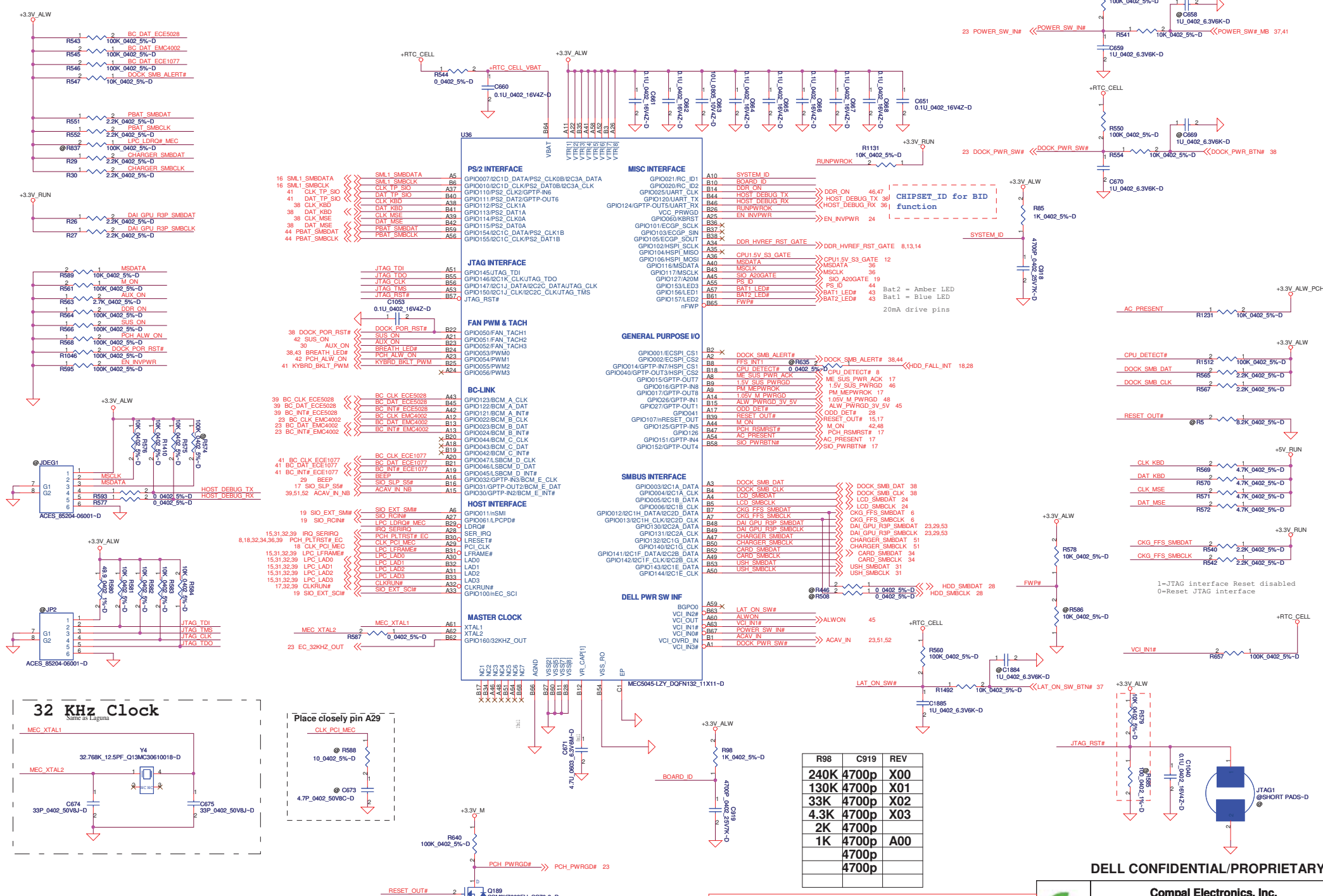
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ECE5028		
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R98	C919	REV
240K	4700p	X00
130K	4700p	X01
33K	4700p	X02
4.3K	4700p	X03
2K	4700p	A00
1K	4700p	A00
4700p		
4700p		

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Compal Electronics, Inc.

File: **EMC5045**

Size: **Document Number**

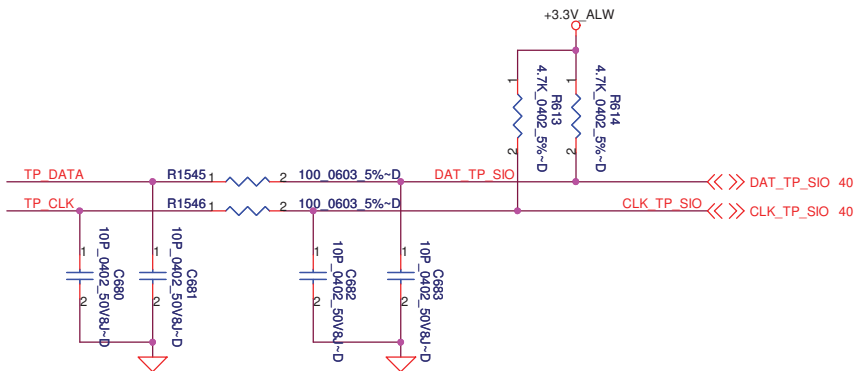
Part Number: **LA-5573P**

Rev: **0.1**

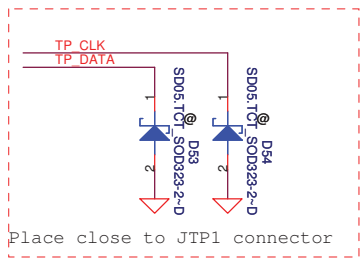
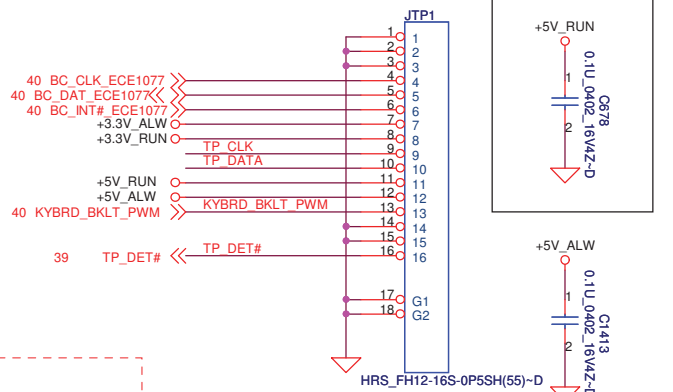
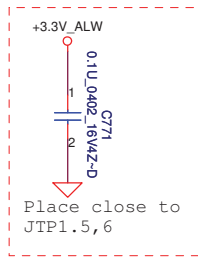
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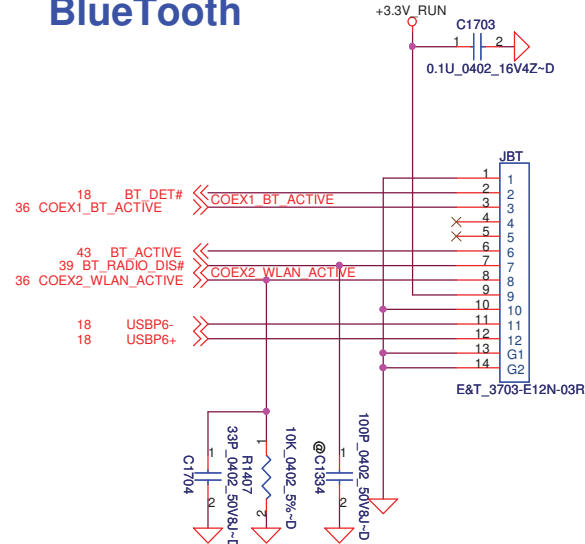
Touch Pad



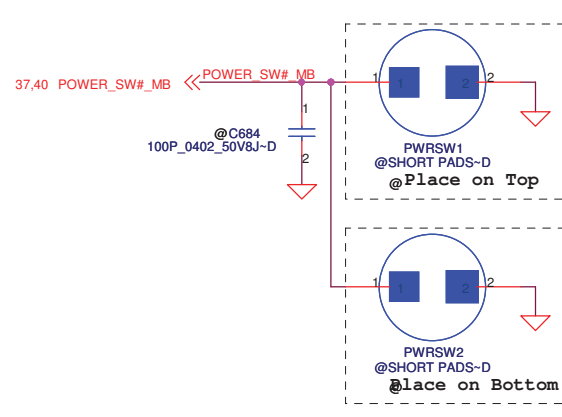
Touch Pad Conn. Pitch=0.5



BlueTooth



Power Switch for debug



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Title		Touch PAD/Int KB/LID	
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@ FAN

Part Number	Description
DC28A000800	FAN SET DAQ20 DC5V AB7405HB-HB3 ADDA

@ Speak

Part Number	Description
PK230003Q0L	SPK PACK ZJX 2.0W 4 OHM FG

@SM CARD BODY

Part Number	Description
SP070007V0L	S SOCKET TYCO 1770551-1 10P H5.9 SMART

@PCMCIA BODY

Part Number	Description
DC000001Q0L	PCMCIA TYCO 1759096-1

@ MDC wire set cable

Part Number	Description
DC02000CS0L	H-CONN SET ZGX MB-MDC

@ T/P wire set cable

Part Number	Description
DC02000840L	H-CONN SET ZJX MB-B/T-TP-FP

@ LVDS cable

Part Number	Description
DC020003Y0L	H-CONN SET ZJX MB-LCD 14 WXGA+ (-1ch)

@ LVDS cable

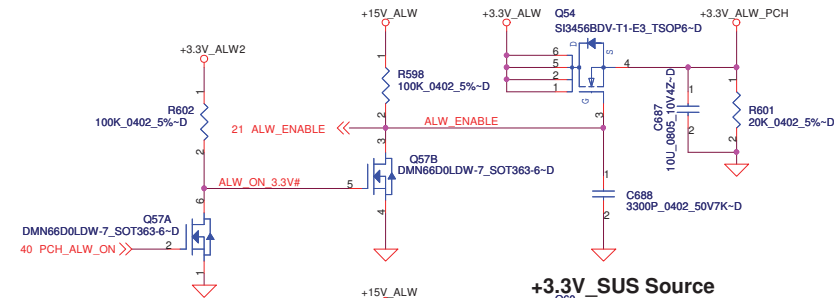
Part Number	Description
DC02000870L	H-CONN SET ZJX MB-LCD 14 WXGA+ (-2ch)

@ RTC BATT

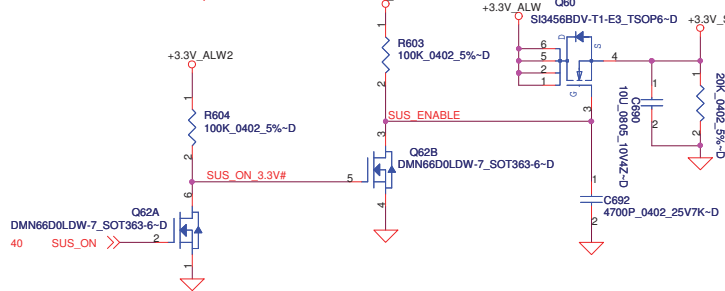
Part Number	Description
GC20323MX00	BATT CR2032 3V 220MAH MAXELL

DC/DC Interface

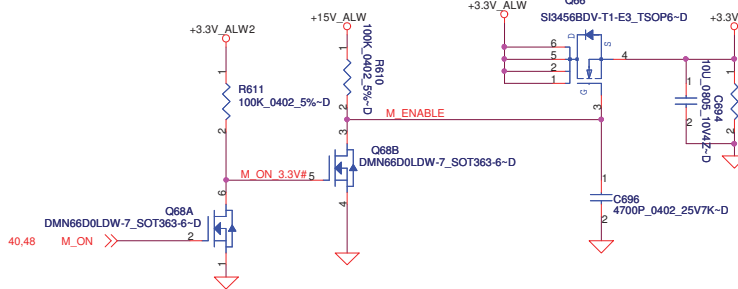
+3.3V_ALW_PCH Source



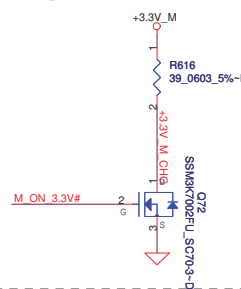
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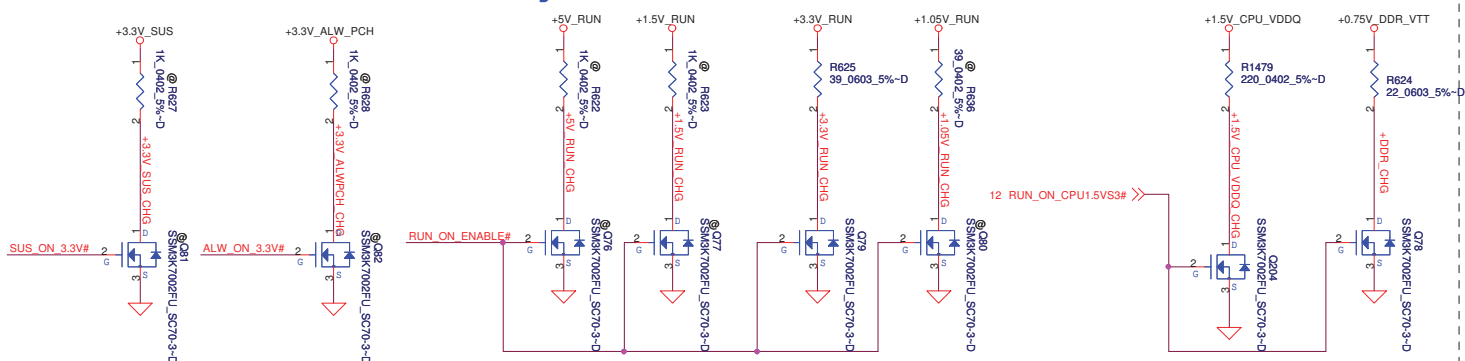
+3.3VM Source



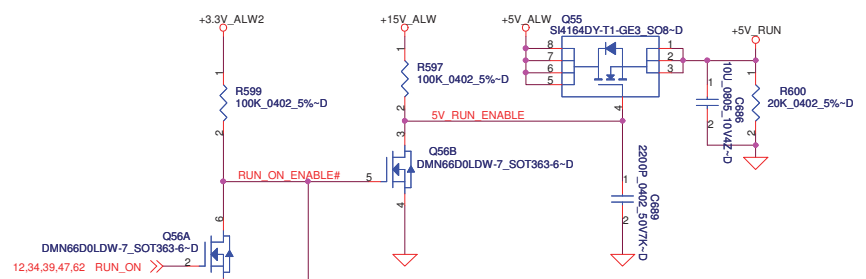
Discharg Circuit



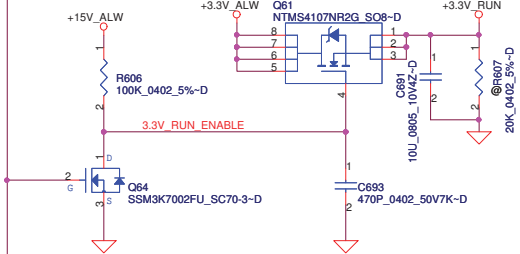
Discharg Circuit



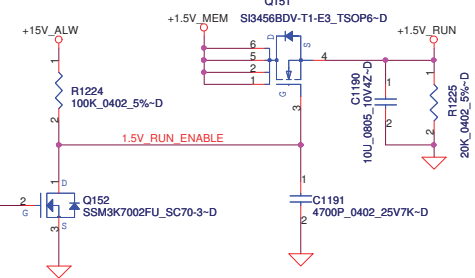
+5VRUN Source



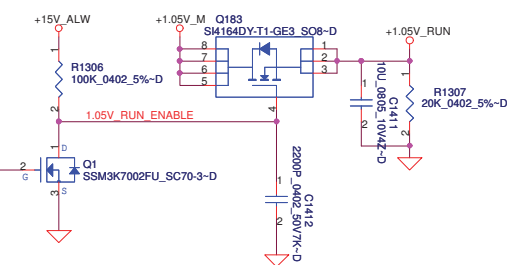
+3.3V_RUN Source



+1.5V_RUN Source



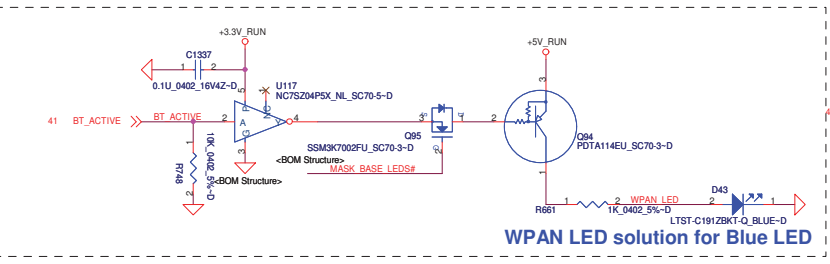
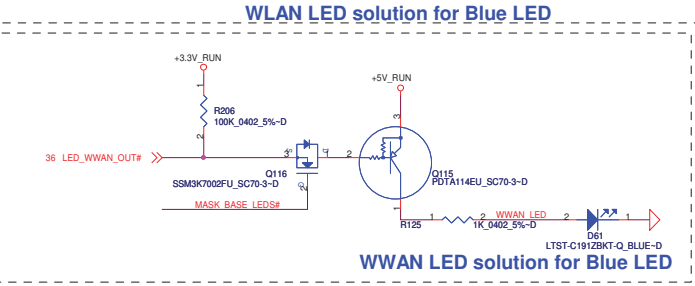
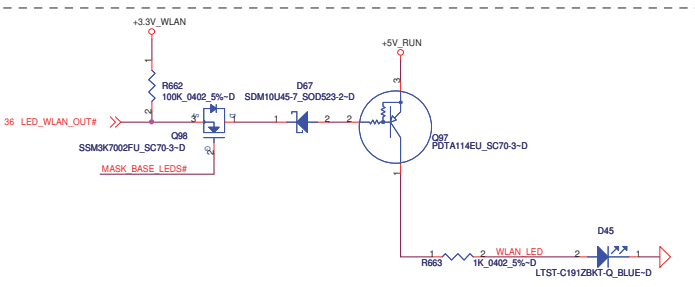
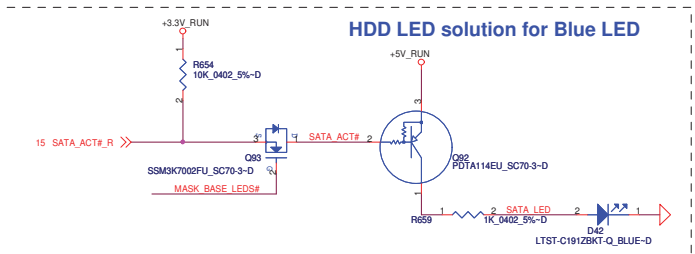
+1.05V_RUN Source



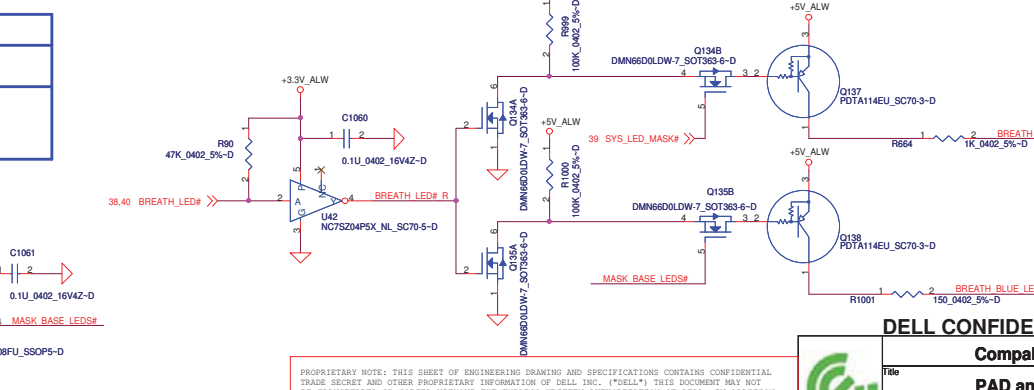
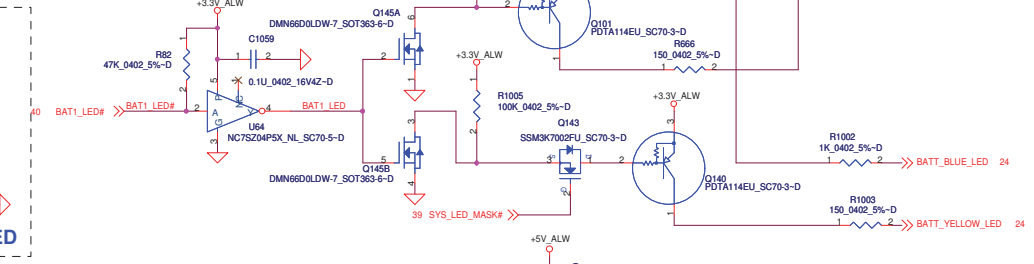
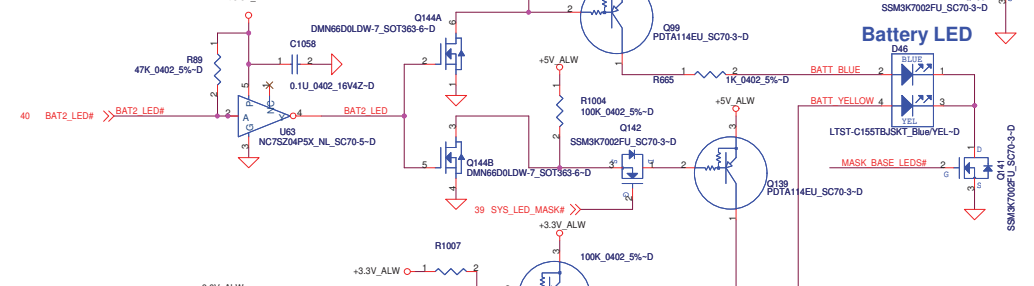
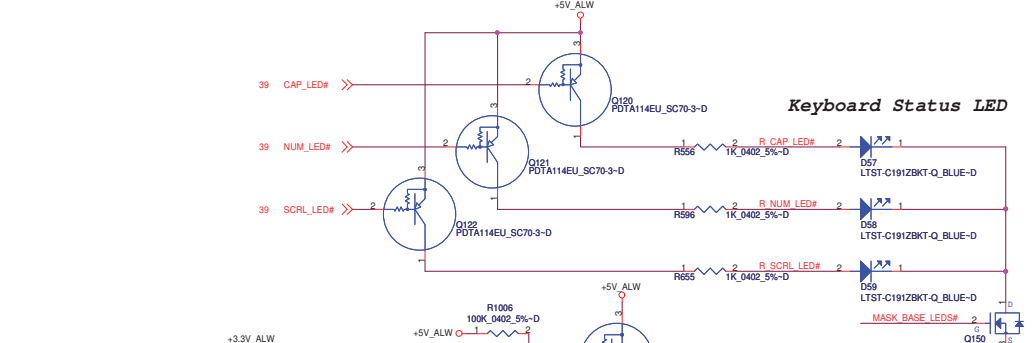
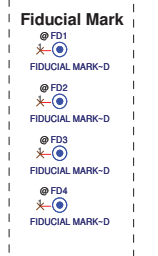
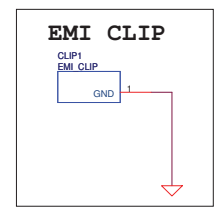
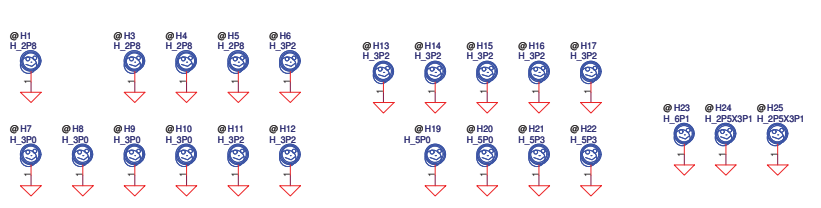
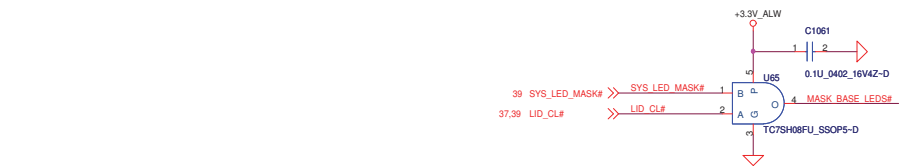
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Title		
POWER CONTROL		
Size	Document Number	Rev
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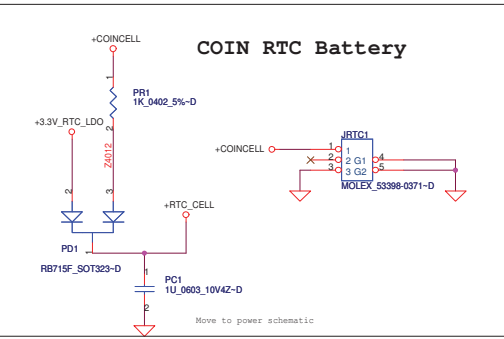
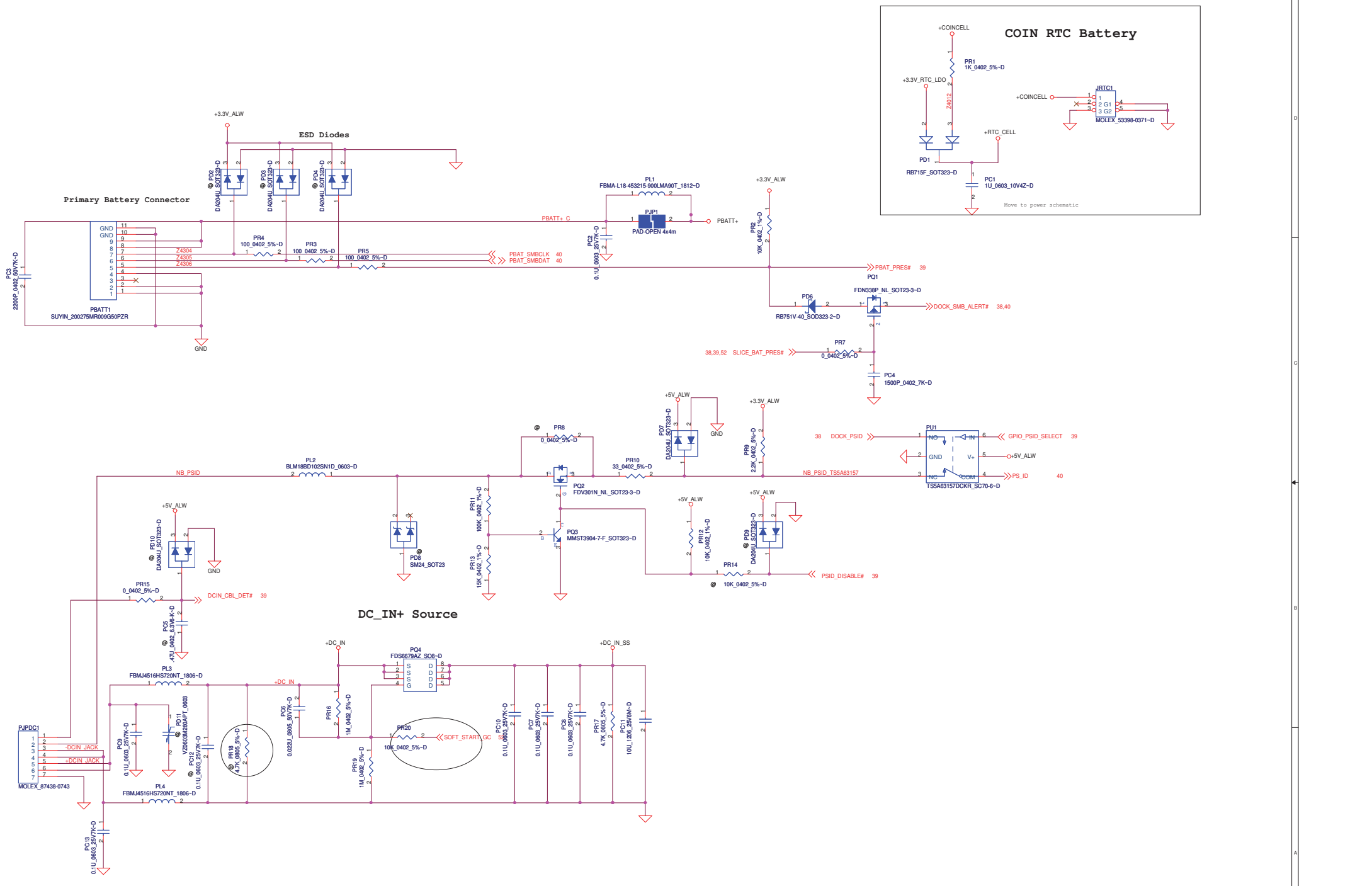


	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



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Title: PAD and Standoff	
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+DCIN

File	+DCIN		
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+3.3V_ALWP / +5V_ALWP / +5V_ALW2 / +15V_ALWP / +3.3V_RTC_LDO

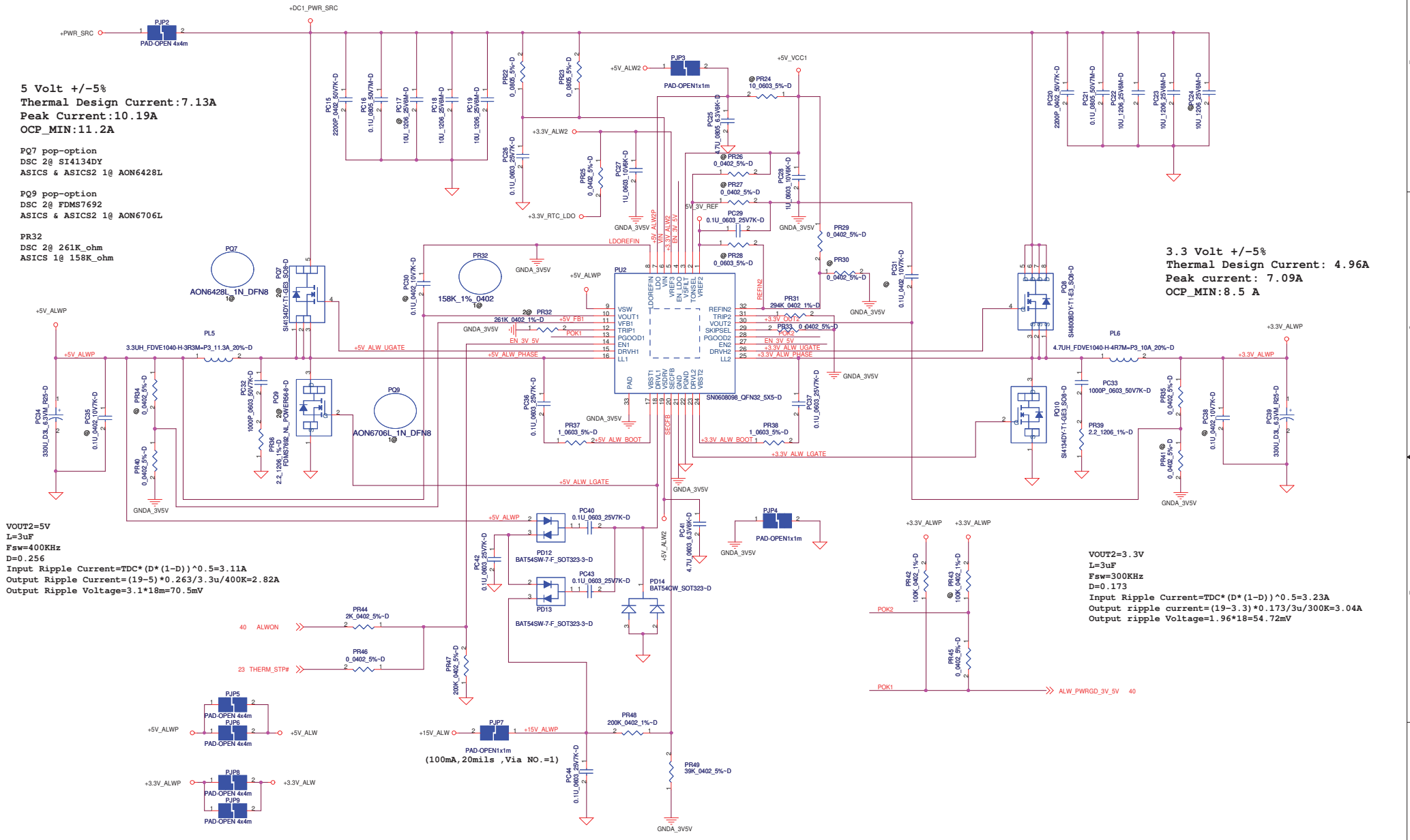
5 Volt +/-5%
 Thermal Design Current: 7.13A
 Peak Current: 10.19A
 OCP_MIN: 11.2A

PQ7 pop-option
 DSC 2@ SI4134DY
 ASICS & ASICS2 1@ AON6428L

PQ9 pop-option
 DSC 2@ FDM57692
 ASICS 1@ ASICS2 1@ AON6706L

PR32
 DSC 2@ 261K_ohm
 ASICS 1@ 158K_ohm

3.3 Volt +/-5%
 Thermal Design Current: 4.96A
 Peak current: 7.09A
 OCP_MIN: 8.5 A



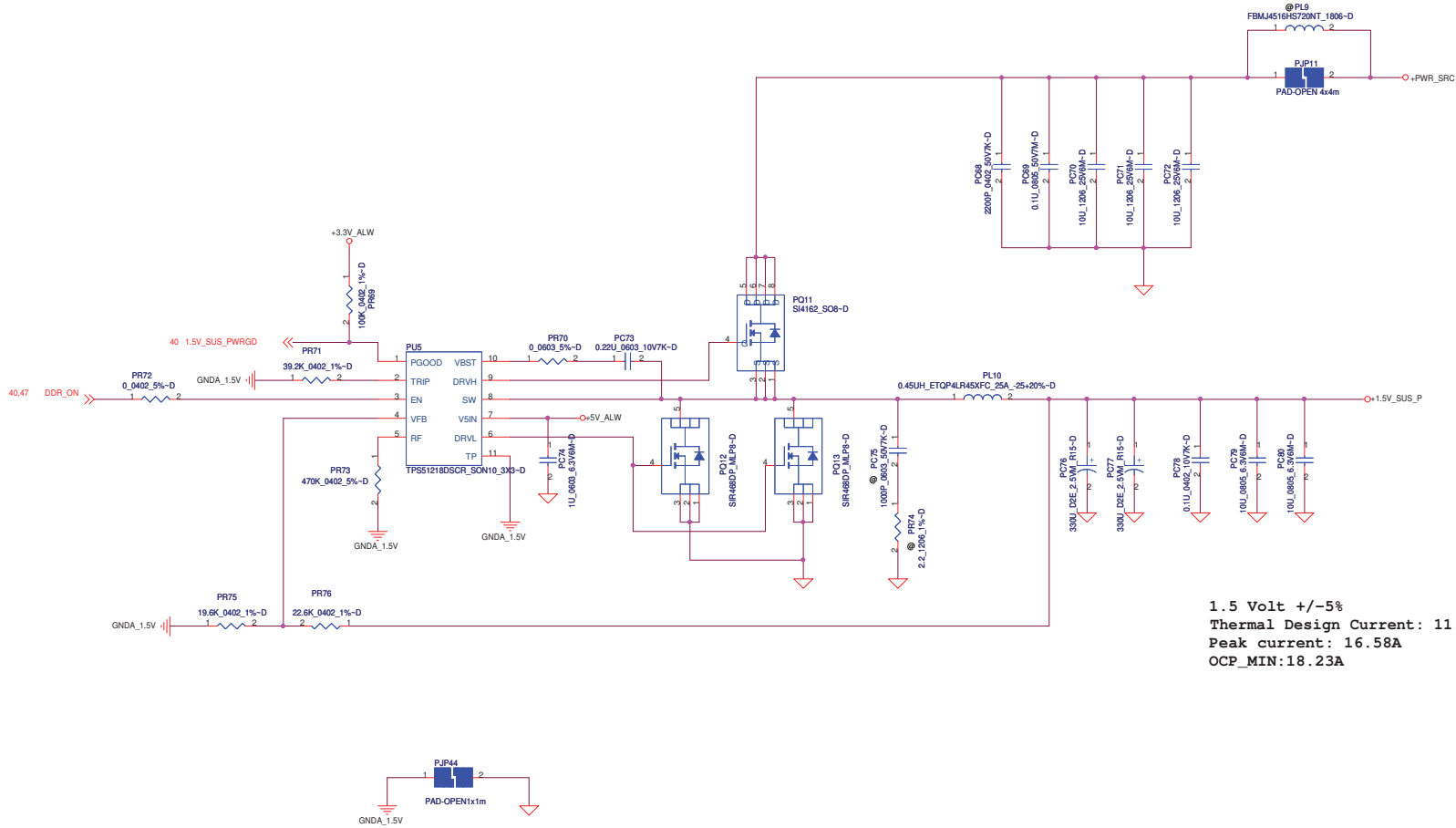
VOUT2=5V
 L=3uF
 Fsw=400KHz
 D=0.256
 Input Ripple Current=TDC*(D*(1-D))^0.5=3.11A
 Output Ripple Current=(19-5)*0.263/3.3u/400K=2.82A
 Output Ripple Voltage=3.1*18=70.5mV

VOUT2=3.3V
 L=3uF
 Fsw=300KHz
 D=0.173
 Input Ripple Current=TDC*(D*(1-D))^0.5=3.23A
 Output ripple current=(19-3.3)*0.173/3u/300K=3.04A
 Output ripple Voltage=1.96*18=54.72mV

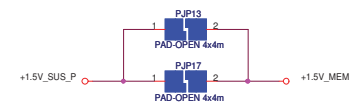
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Title		DC/DC +3V/ +5V	
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1.5 Volt +/-5%
 Thermal Design Current: 11.6A
 Peak current: 16.58A
 OCP_MIN: 18.23A



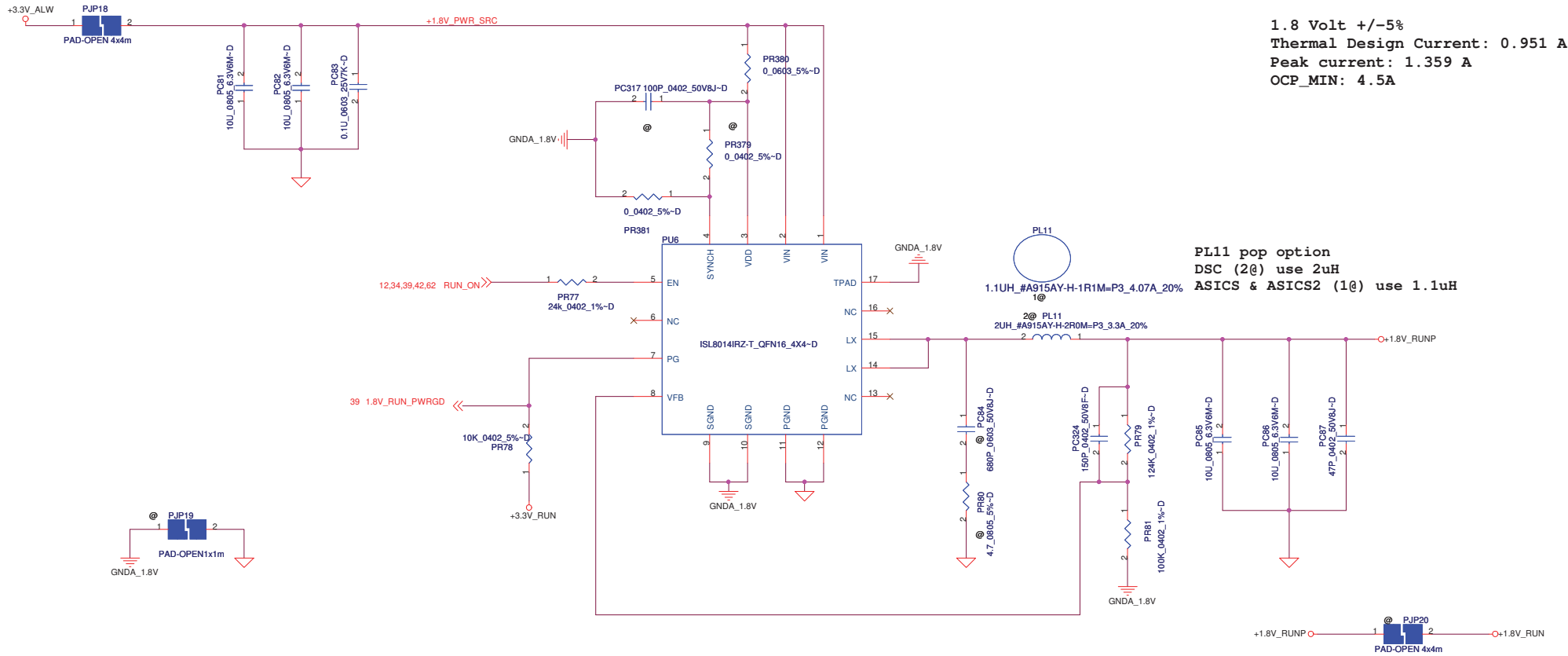
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Title +1.5V MEM			
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+1.8V_RUNP

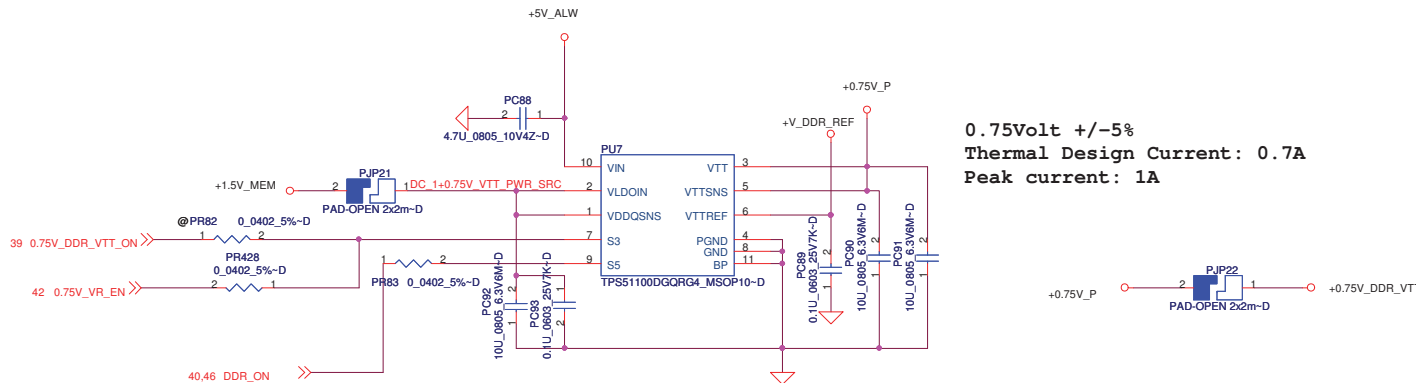


1.8 Volt +/-5%
 Thermal Design Current: 0.951 A
 Peak current: 1.359 A
 OCP_MIN: 4.5A

PL11 pop option
 DSC (2@) use 2uH
 ASICS & ASICS2 (1@) use 1.1uH

VOUT=1.8V
 L=3.3uF
 Fsw=290KHz
 D=0.092
 Input Ripple Current=TDC*(D*(1-D))^0.5=0.884A
 Output Ripple Current=1.707A
 Output Ripple Voltage=1.707*15m=20.5mV

+0.75V_DDR_VTT DDR3 Termination



0.75Volt +/-5%
 Thermal Design Current: 0.7A
 Peak current: 1A

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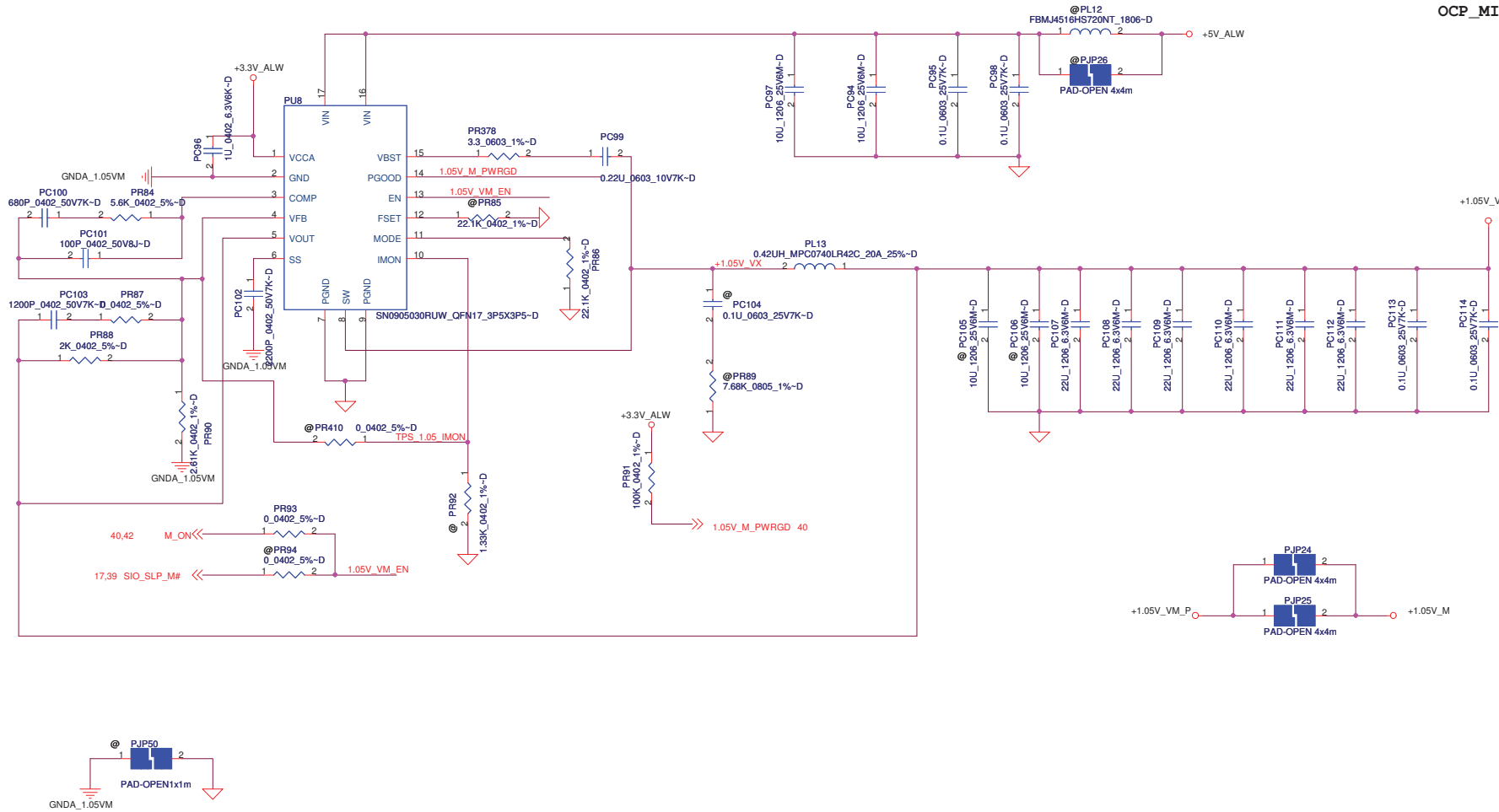
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Title			
+0.75V DDR VT/+1.8V RUN			
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+1.05V_M_P

1.05 Volt +/-5%
 Thermal Design Current: 7.6A
 Peak current: 10.9A
 OCP_MIN: 11.9A



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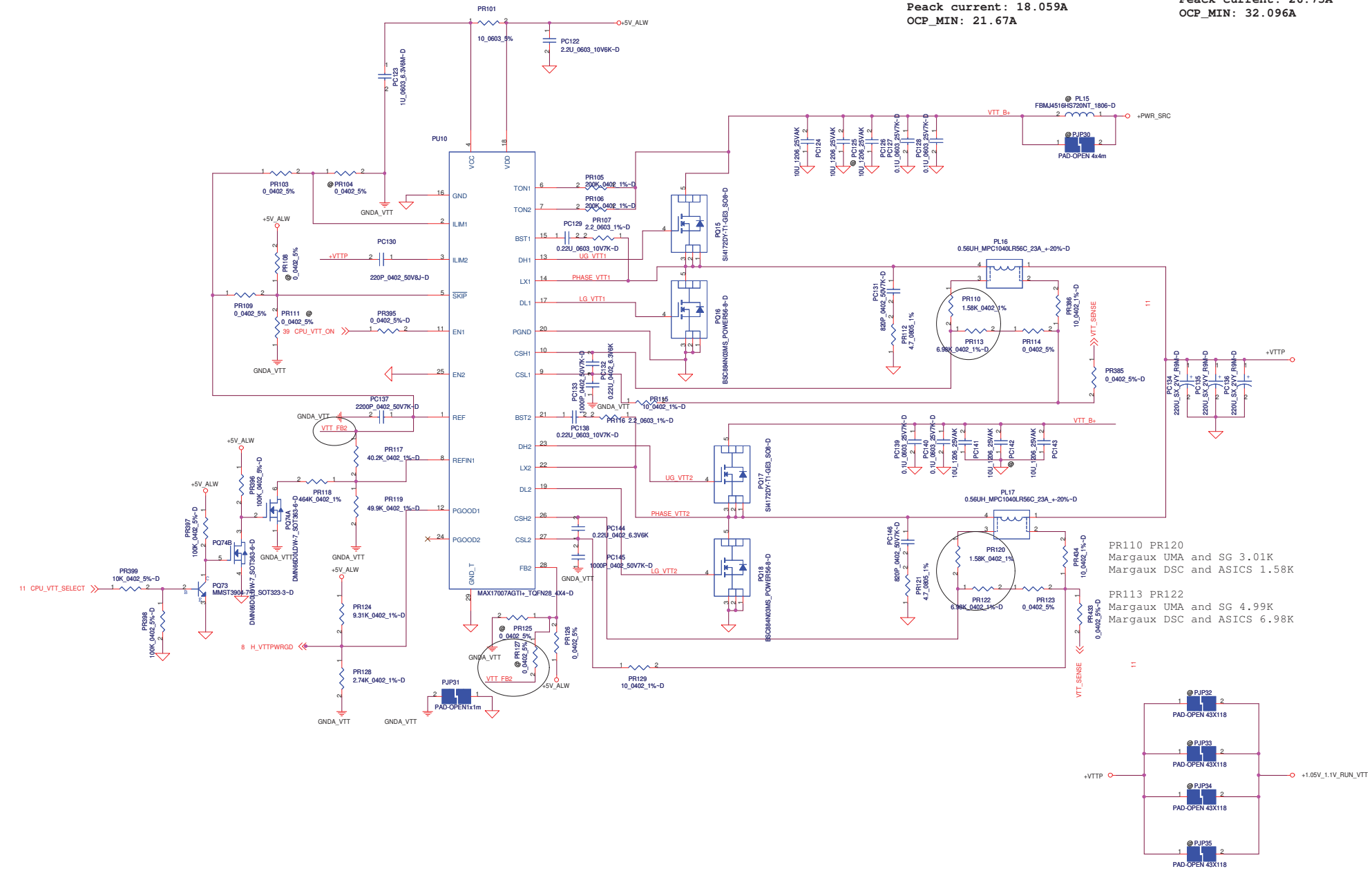
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1.1 Volt +/-5%
 Thermal Design Current: 12.641A
 Peak current: 18.059A
 OCP_MIN: 21.67A

1.05 Volt +/-5%
 Thermal Design Current: 18.72A
 Peak current: 26.75A
 OCP_MIN: 32.096A



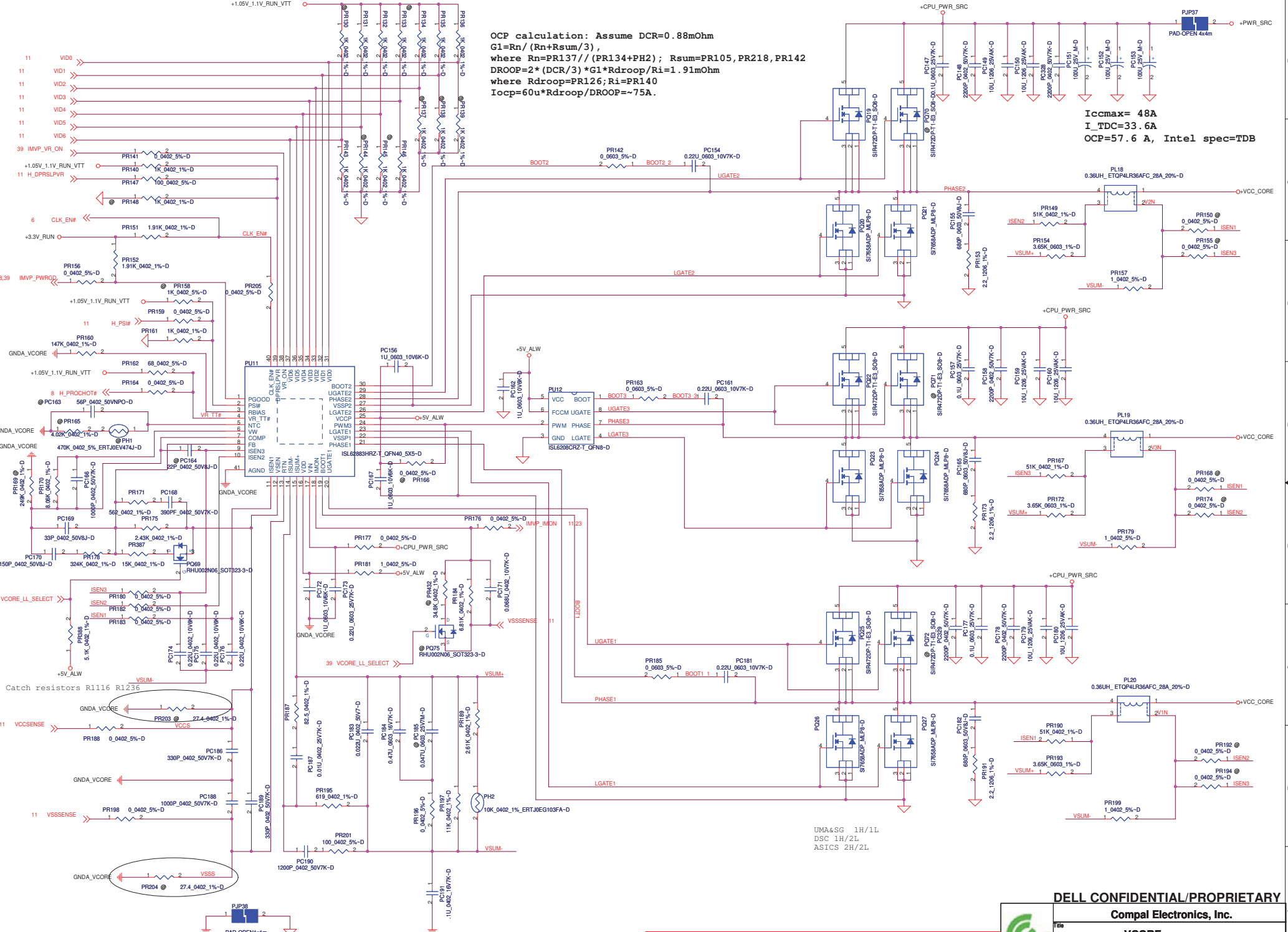
PR110 PR120
 Margaux UMA and SG 3.01K
 Margaux DSC and ASICS 1.58K

PR113 PR122
 Margaux UMA and SG 4.99K
 Margaux DSC and ASICS 6.98K

Title			<Title>
Size	Document Number	Rev	
C	LA-5772P	1A	
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OCP calculation: Assume DCR=0.88mOhm
 $G1=Rn/(Rn+Rsum/3)$,
 where $Rn=PR137//((PR134+PH2)$; $Rsum=PR105, PR218, PR142$
 $DROOP=2*(DCR/3)*G1*Rdroop/Ri=1.91mOhm$
 where $Rdroop=PR126$; $Ri=PR140$
 $Iocp=60u*Rdroop/DROOP\sim 75A$.

$I_{ccmax} = 48A$
 $I_{TDC} = 33.6A$
 $OCP = 57.6A$, Intel spec=TDB



Catch resistors R116 R1236

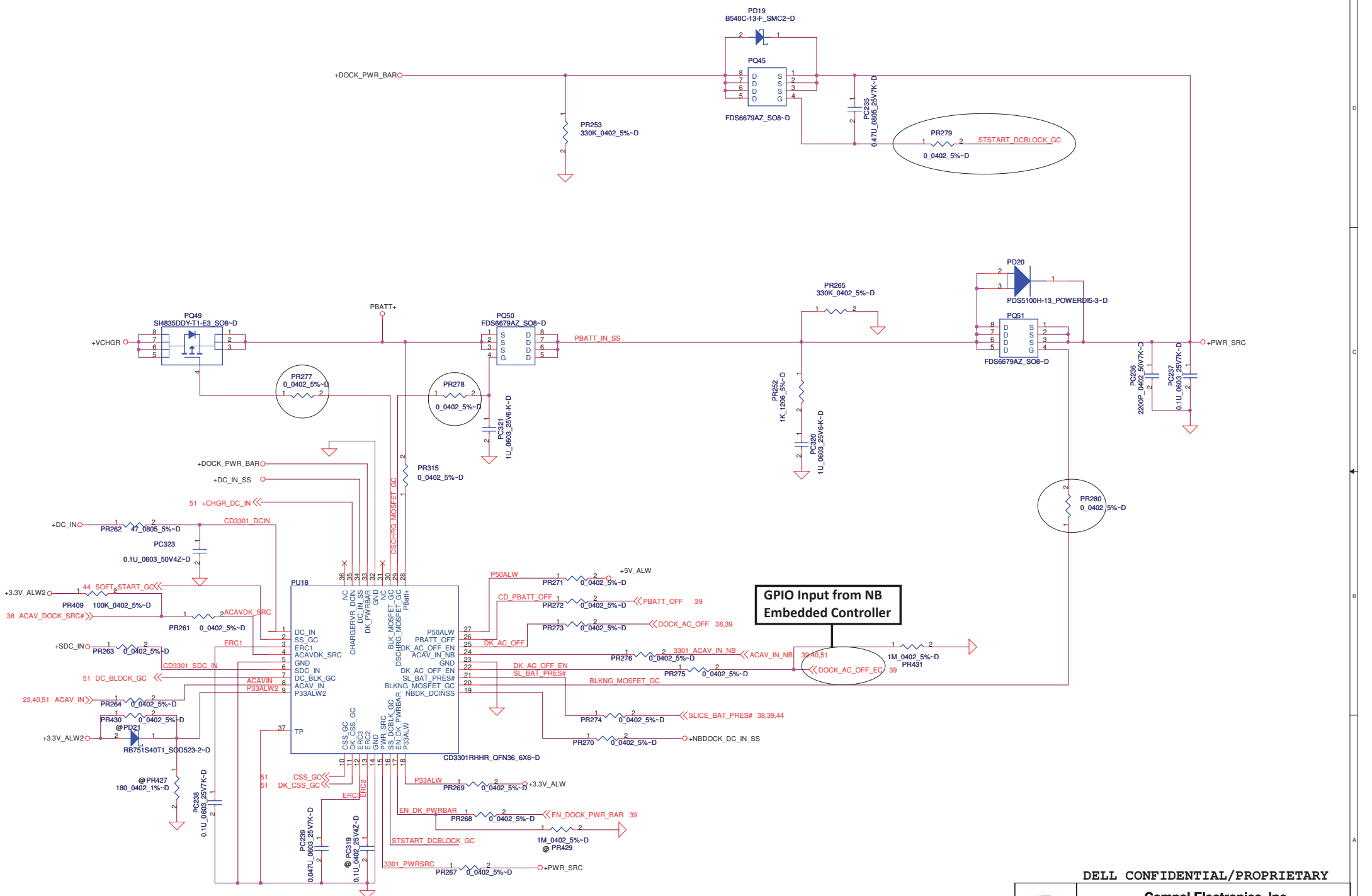
UMA&SG 1H/1L
 DSC 1H/2L
 ASICS 2H/2L

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Compal Electronics, Inc.	
+VCORE	
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GPIO Input from NB Embedded Controller

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Selector

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7 PEG_CTX_GRX_P0..15] >> PEG_CTX_GRX_P0..15]
 7 PEG_CTX_GRX_N0..15] >> PEG_CTX_GRX_N0..15]
 7 PEG_CRX_GTX_P0..15] >> PEG_CRX_GTX_P0..15]
 7 PEG_CRX_GTX_N0..15] >> PEG_CRX_GTX_N0..15]

PEG_CRX_GTX_P0	C1439	2	1	0.1U	0402	10V7K-D	PEG_CRX_GTX_C_P0
PEG_CRX_GTX_N0	C1440	2	1	0.1U	0402	10V7K-D	PEG_CRX_GTX_C_N0
PEG_CRX_GTX_P1	C1441	2	1	0.1U	0402	10V7K-D	PEG_CRX_GTX_C_P1
PEG_CRX_GTX_N1	C1442	2	1	0.1U	0402	10V7K-D	PEG_CRX_GTX_C_N1
PEG_CRX_GTX_P2	C1443	2	1	0.1U	0402	10V7K-D	PEG_CRX_GTX_C_P2
PEG_CRX_GTX_N2	C1444	2	1	0.1U	0402	10V7K-D	PEG_CRX_GTX_C_N2
PEG_CRX_GTX_P3	C1446	2	1	0.1U	0402	10V7K-D	PEG_CRX_GTX_C_P3
PEG_CRX_GTX_N3	C1447	2	1	0.1U	0402	10V7K-D	PEG_CRX_GTX_C_N3
PEG_CRX_GTX_P4	C1448	2	1	0.1U	0402	10V7K-D	PEG_CRX_GTX_C_P4
PEG_CRX_GTX_N4	C1449	2	1	0.1U	0402	10V7K-D	PEG_CRX_GTX_C_N4
PEG_CRX_GTX_P5	C1450	2	1	0.1U	0402	10V7K-D	PEG_CRX_GTX_C_P5
PEG_CRX_GTX_N5	C1451	2	1	0.1U	0402	10V7K-D	PEG_CRX_GTX_C_N5
PEG_CRX_GTX_P6	C1452	2	1	0.1U	0402	10V7K-D	PEG_CRX_GTX_C_P6
PEG_CRX_GTX_N6	C1453	2	1	0.1U	0402	10V7K-D	PEG_CRX_GTX_C_N6
PEG_CRX_GTX_P7	C1454	2	1	0.1U	0402	10V7K-D	PEG_CRX_GTX_C_P7
PEG_CRX_GTX_N7	C1455	2	1	0.1U	0402	10V7K-D	PEG_CRX_GTX_C_N7
PEG_CRX_GTX_P8	C1457	2	1	0.1U	0402	10V7K-D	PEG_CRX_GTX_C_P8
PEG_CRX_GTX_N8	C1458	2	1	0.1U	0402	10V7K-D	PEG_CRX_GTX_C_N8
PEG_CRX_GTX_P9	C1459	2	1	0.1U	0402	10V7K-D	PEG_CRX_GTX_C_P9
PEG_CRX_GTX_N9	C1460	2	1	0.1U	0402	10V7K-D	PEG_CRX_GTX_C_N9
PEG_CRX_GTX_P10	C1461	2	1	0.1U	0402	10V7K-D	PEG_CRX_GTX_C_P10
PEG_CRX_GTX_N10	C1462	2	1	0.1U	0402	10V7K-D	PEG_CRX_GTX_C_N10
PEG_CRX_GTX_P11	C1463	2	1	0.1U	0402	10V7K-D	PEG_CRX_GTX_C_P11
PEG_CRX_GTX_N11	C1464	2	1	0.1U	0402	10V7K-D	PEG_CRX_GTX_C_N11
PEG_CRX_GTX_P12	C1465	2	1	0.1U	0402	10V7K-D	PEG_CRX_GTX_C_P12
PEG_CRX_GTX_N12	C1466	2	1	0.1U	0402	10V7K-D	PEG_CRX_GTX_C_N12
PEG_CRX_GTX_P13	C1468	2	1	0.1U	0402	10V7K-D	PEG_CRX_GTX_C_P13
PEG_CRX_GTX_N13	C1469	2	1	0.1U	0402	10V7K-D	PEG_CRX_GTX_C_N13
PEG_CRX_GTX_P14	C1470	2	1	0.1U	0402	10V7K-D	PEG_CRX_GTX_C_P14
PEG_CRX_GTX_N14	C1471	2	1	0.1U	0402	10V7K-D	PEG_CRX_GTX_C_N14
PEG_CRX_GTX_P15	C1472	2	1	0.1U	0402	10V7K-D	PEG_CRX_GTX_C_P15
PEG_CRX_GTX_N15	C1473	2	1	0.1U	0402	10V7K-D	PEG_CRX_GTX_C_N15

U106A Part 1 of 7

PEG_CTX_GRX_P0	AP17	PEG_RX0
PEG_CTX_GRX_N0	AN17C	PEG_RX0_N
PEG_CTX_GRX_P1	AP19	PEG_RX1
PEG_CTX_GRX_N1	AN19	PEG_RX1_N
PEG_CTX_GRX_P2	AP19A	PEG_RX1_N
PEG_CTX_GRX_P3	AR20	PEG_RX2
PEG_CTX_GRX_N3	AN20	PEG_RX2_N
PEG_CTX_GRX_P4	AN22	PEG_RX3
PEG_CTX_GRX_N4	AP22C	PEG_RX3_N
PEG_CTX_GRX_P5	AR22C	PEG_RX4
PEG_CTX_GRX_N5	AN22C	PEG_RX4_N
PEG_CTX_GRX_P6	AP23	PEG_RX5
PEG_CTX_GRX_N6	AN23	PEG_RX5_N
PEG_CTX_GRX_P7	AN23C	PEG_RX6
PEG_CTX_GRX_N7	AP23C	PEG_RX6_N
PEG_CTX_GRX_P8	AR25	PEG_RX7
PEG_CTX_GRX_N8	AN26C	PEG_RX8
PEG_CTX_GRX_P9	AP26	PEG_RX8_N
PEG_CTX_GRX_N9	AN26	PEG_RX9
PEG_CTX_GRX_P10	AN28	PEG_RX9_N
PEG_CTX_GRX_N10	AP28C	PEG_RX10
PEG_CTX_GRX_P11	AR28	PEG_RX10_N
PEG_CTX_GRX_N11	AN28	PEG_RX11
PEG_CTX_GRX_P12	AP29	PEG_RX11_N
PEG_CTX_GRX_N12	AN29C	PEG_RX12
PEG_CTX_GRX_P13	AN31	PEG_RX13
PEG_CTX_GRX_N13	AP31C	PEG_RX13_N
PEG_CTX_GRX_P14	AR32C	PEG_RX14
PEG_CTX_GRX_N14	AN32	PEG_RX14_N
PEG_CTX_GRX_P15	AR34	PEG_RX15
PEG_CTX_GRX_N15	AP34C	PEG_RX15_N

GPIO

PCI EXPRESS

DVO

CLK

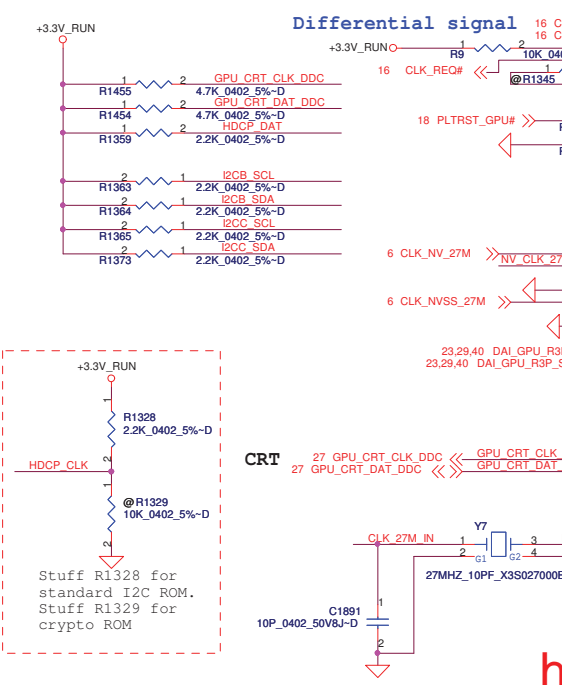
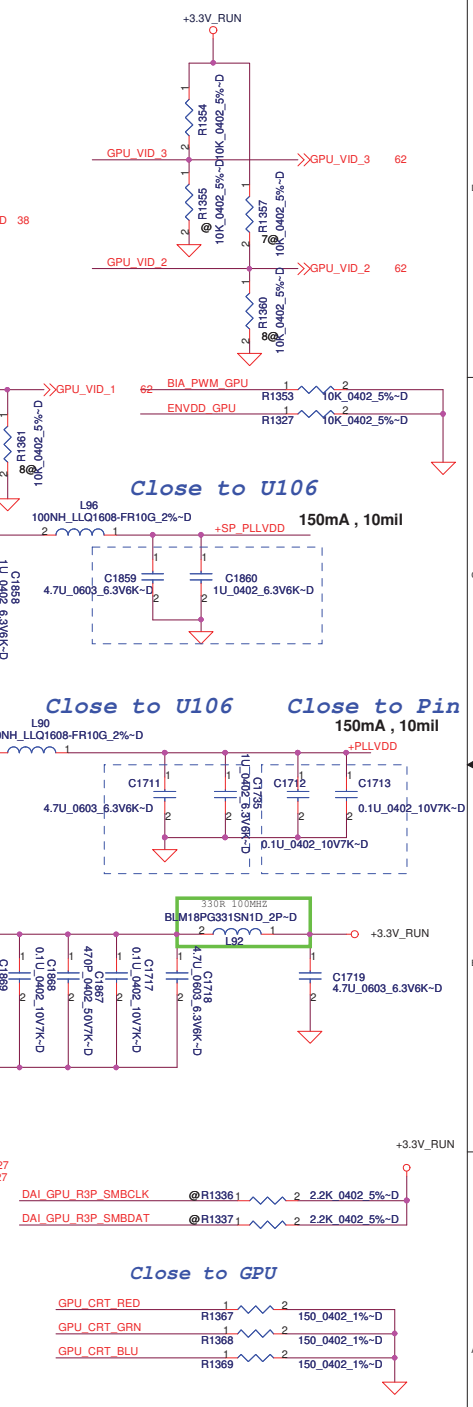
I2C

DACS

GPIO0	K1	GPU VID 1
GPIO1	K2	DPB GPU HPD
GPIO2	K3	BIA_PWM_GPU
GPIO3	H3	ENVDD_GPU
GPIO4	H2	PANEL_BKEN_DGPU
GPIO5	H1	GPU VID 2
GPIO6	H4	GPU VID 3
GPIO7	H5	GPU VID 4
GPIO8	H6	THERMTRIP_VGA#
GPIO9	J7	
GPIO10	K4	
GPIO11	K5	GPU_CLKDOWN
GPIO12	J4	
GPIO13	J6	
GPIO14	L2	DPC_GPU_DOCK_HPD
GPIO15	L2	
GPIO16	L4	
GPIO17	M4	DPD_GPU_EDP_HPD
GPIO18	L7	
GPIO19	L5	
GPIO20	K6	
GPIO21	L6	
GPIO22	M6	
GPIO23	M6	

MIOA_D0	N1	
MIOA_D1	P4	
MIOA_D2	P2	
MIOA_D3	P2	
MIOA_D4	P3	
MIOA_D5	T3	
MIOA_D6	T1	
MIOA_D7	U4	
MIOA_D8	U1	
MIOA_D9	U1	
MIOA_D10	U3	
MIOA_D11	U3	
MIOA_D12	R6	
MIOA_D13	T6	
MIOA_D14	N6	
MIOB_D0	Y1	
MIOB_D1	Y2	
MIOB_D2	Y3	
MIOB_D3	AB1	
MIOB_D4	AB2	
MIOB_D5	AB2	
MIOB_D6	AC4	
MIOB_D7	AC2	
MIOB_D8	AC3	
MIOB_D9	AE3	
MIOB_D10	AE3	
MIOB_D11	W6	
MIOB_D12	W6	
MIOB_D13	W6	
MIOB_D14	Y6	
MIOA_HSVMC	N3	
MIOA_VSYNC	L3	
MIOB_HSVMC	W1	
MIOB_VSYNC	W2	
MIOA_DE	N2	
MIOA_CTL3	N5	
MIOA_VREF	N5	
MIOB_DE	Y5	
MIOB_CTL3	W3	
MIOB_VREF	AF1	
MIOA_CLKIN	N4	
MIOA_CLKOUT	R4	
MIOB_CLKIN	AE1	
MIOB_CLKOUT	V4	
MIOA_CLKOUT_N	T4	
MIOB_CLKOUT_N	W4	
MIOA_CAL_PD_VDDO	U5	
MIOA_CAL_PU_GND	T5	
MIOB_CAL_PD_VDDO	AA7	
MIOB_CAL_PU_GND	AA6	

DACA_RED	AM15	GPU CRT RED
DACA_GREEN	AM14	GPU CRT GRN
DACA_BLUE	AL14	GPU CRT BLU
DACA_HSVMC	AM13	GPU CRT HSVMC
DACA_VSYNC	AL13	GPU CRT VSYNC
DACA_VDD	AJ12	+DACA VDD
DACA_VREF	AK12	-DACA VREF
DACA_RSET	AK13	
I2CC_SCL	E3	I2CC_SCL
I2CC_SDA	E4	I2CC_SDA
I2CB_SCL	G3	I2CB_SCL
I2CB_SDA	G2	I2CB_SDA
DACB_VDD	AK4	
DACB_GREEN	AL4	
DACB_BLUE	AJ4	
DACB_HSVMC	AM1	
DACB_VSYNC	AM2	
DACB_VDD	AG7	+DACB VDD
DACB_VREF	AK6	
DACB_RSET	AH7	



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N10P_PCIE,GPIO,CLK,I2C

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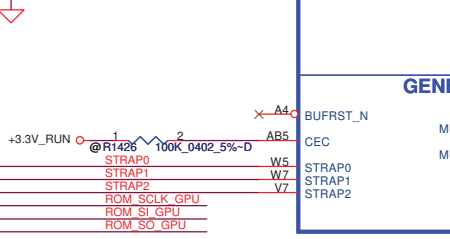
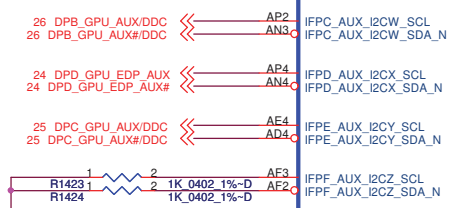
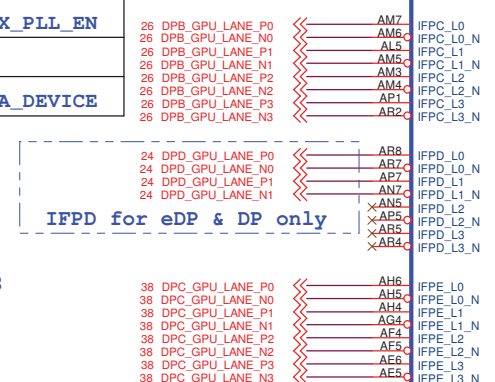
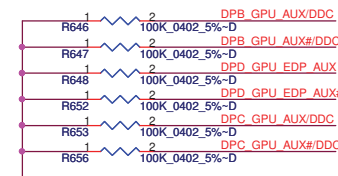
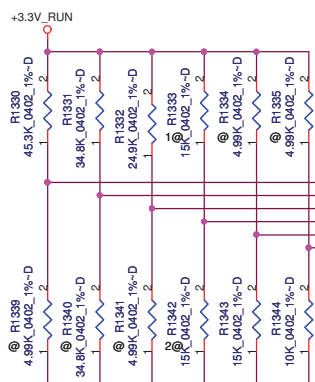
STRAP0	USER[3:0]
STRAP1	3GIO_PADCFG_LUT_ADR[3:0]
STRAP2	PCI_DEVID[3:0]

ROM_SCLK	PCIDEVID_EXT, SUB_VENDOR, SLOT_CLK, PEX_PLL_EN
ROM_SI	RAM_CFG[3:0]
ROM_SO	XCLK_417, FB_0_BAR_SIZE, ALT_ADOOR, VGA_DEVICE

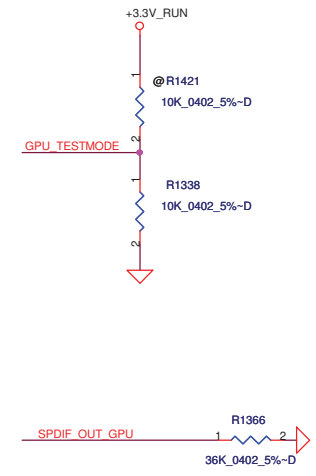
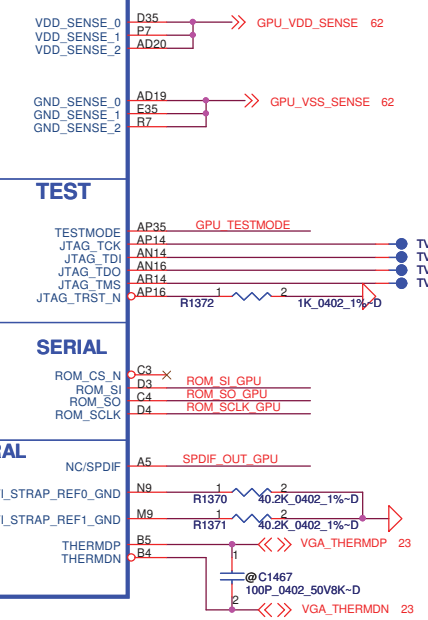
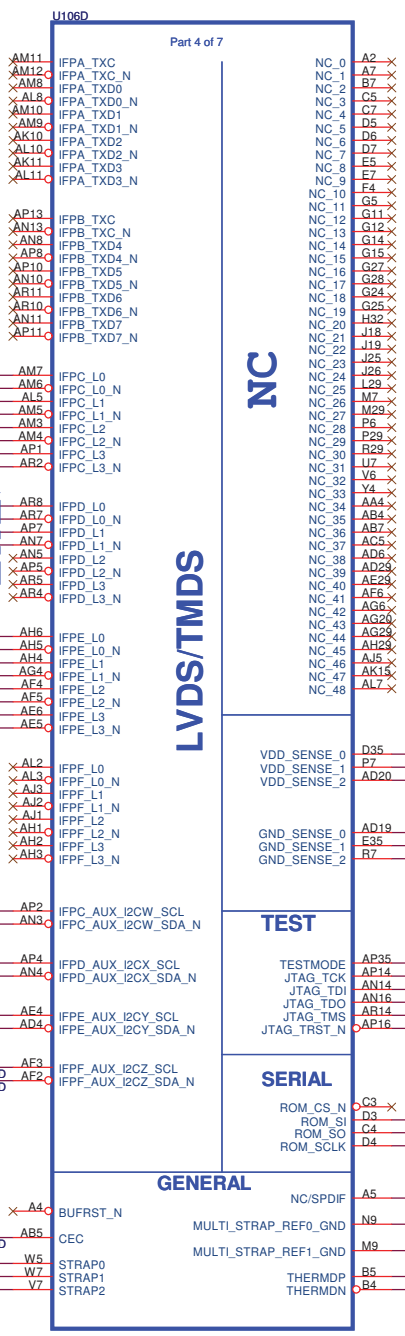
	R1332	R1341	R1342	R1333	
Asics	10K	depop	15K	depop	N10P-GS
Margaux					

Resistor Values	PU/PD	Bit3-Bit0	
STRAP0	PU	1111	45K
STRAP1	PD	0110	35K
STRAP2	PU	1100	25K
ROM_SCLK	PD	0010	15K
ROM_SI	PD	0011	20K
ROM_SO	PD	0001	10K

For Samsung 64Mx16 DDR3 part stuff R1343=20K
 For Hynix 64Mx16 DDR3 part stuff R1343=15K
 Hynix H5TQ1G63BFR-12C SA00003240L



N10P-GLM-A3_BGA969-D
 Hynix H5TQ1G63BFR-12C SA00003240L
 For Samsung 64Mx16 DDR3 part stuff R1343=20K
 For Hynix 64Mx16 DDR3 part stuff R1343=15K



Compal Electronics, Inc.

N10P DP, STRAP

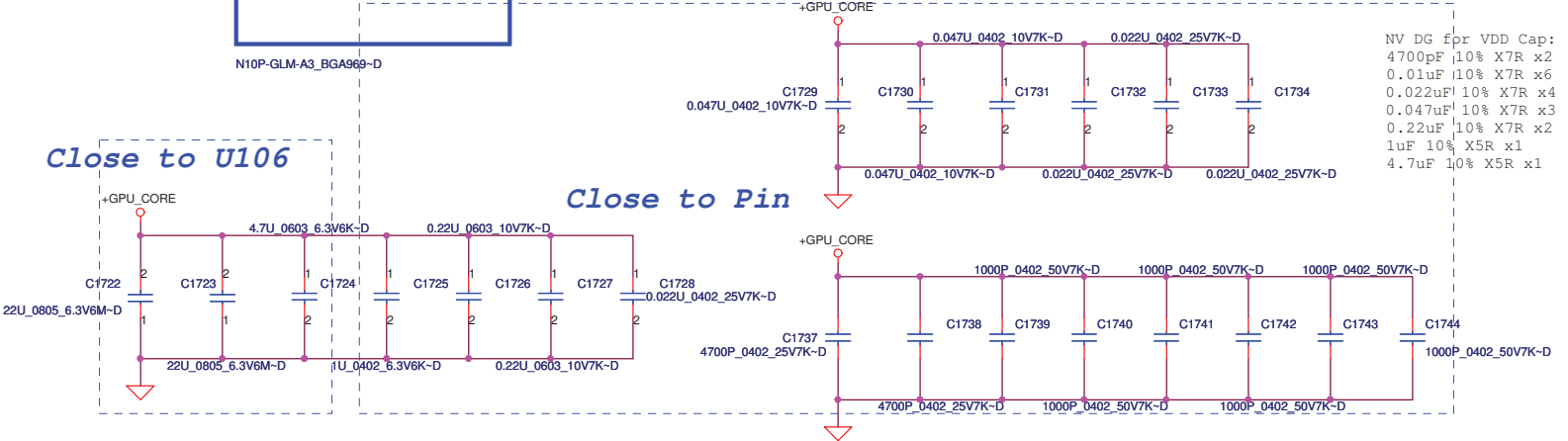
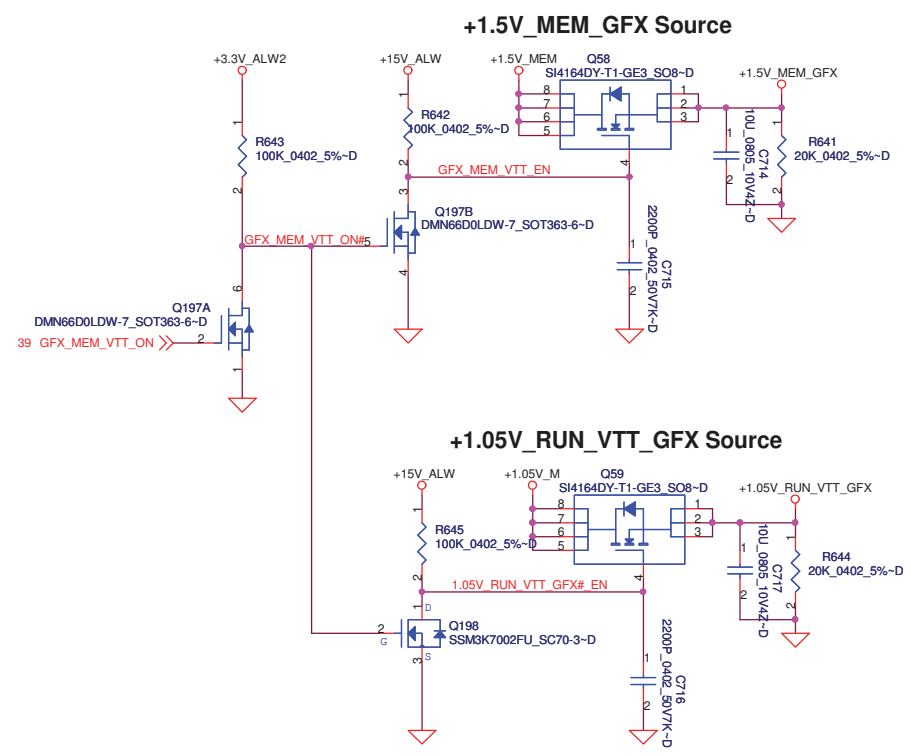
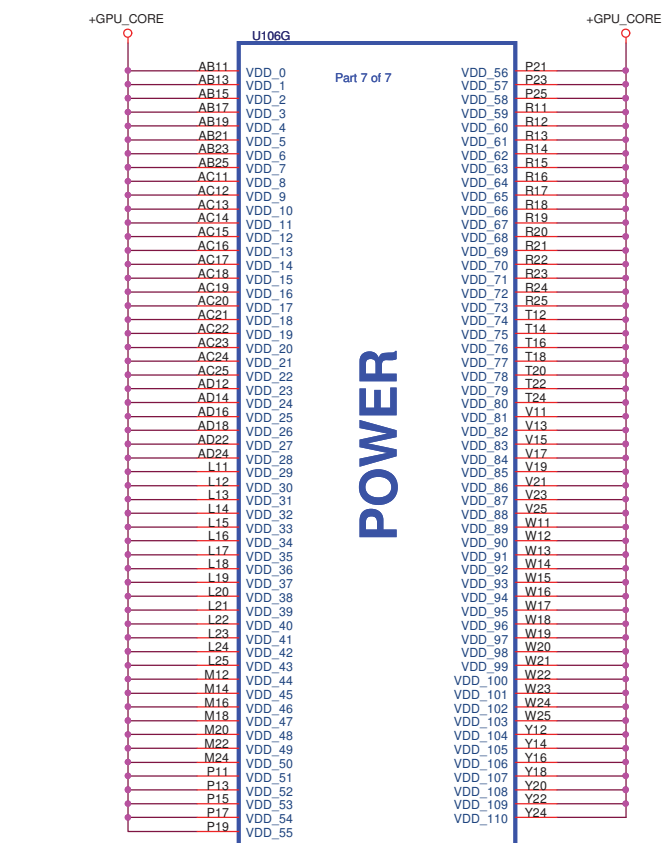
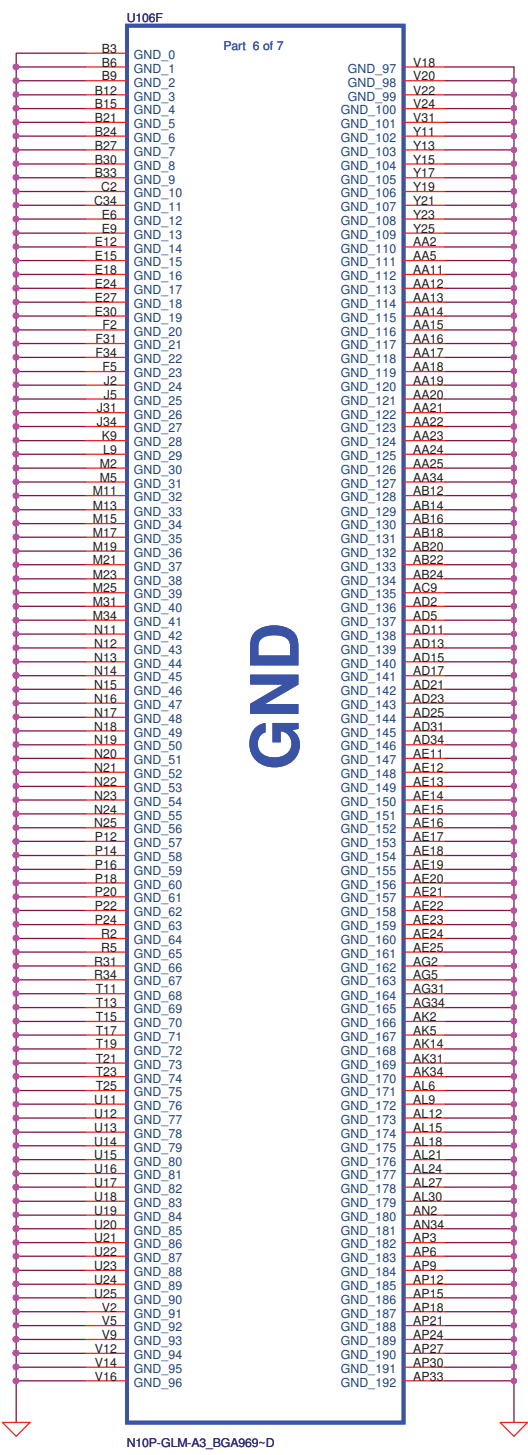
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Rev 3.0

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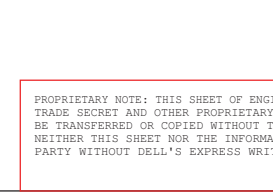
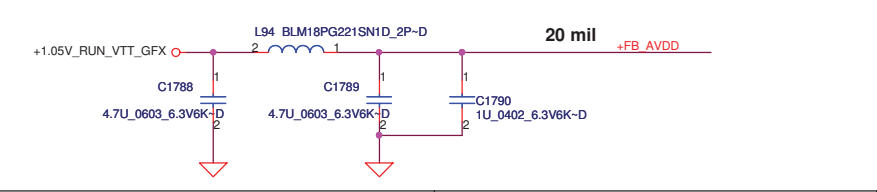
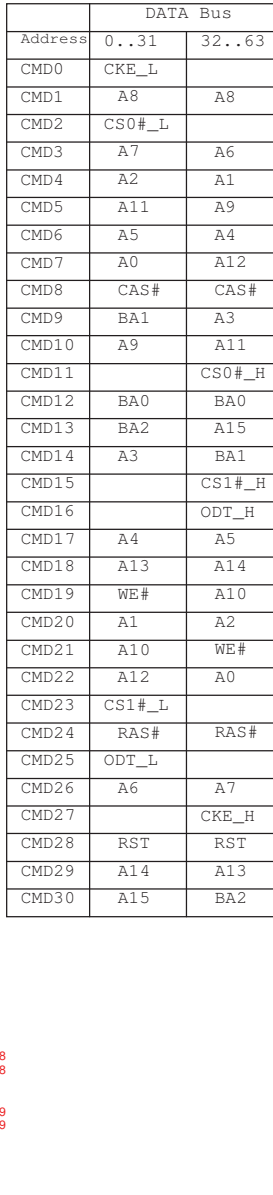
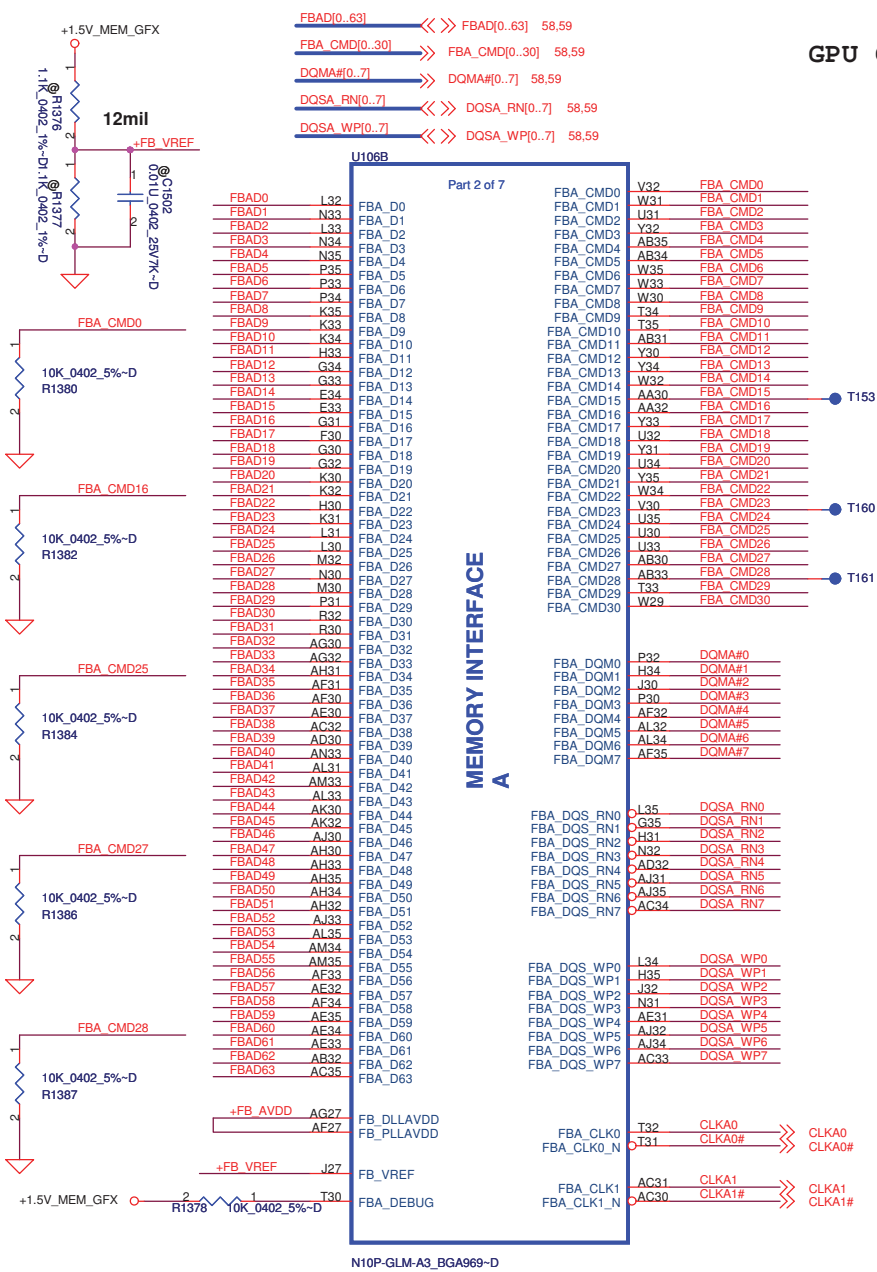
NV DG for VDD Cap:
 4700pF 10% X7R x2
 0.01uF 10% X7R x6
 0.022uF 10% X7R x4
 0.047uF 10% X7R x3
 0.22uF 10% X7R x2
 1uF 10% X5R x1
 4.7uF 10% X5R x1

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		Compal Electronics, Inc.	
		Title: N10P GPU CORE, GND	
Size	Document Number	Rev	
	LA-5573P	3.0	
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GPU CMD - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	BA0
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2



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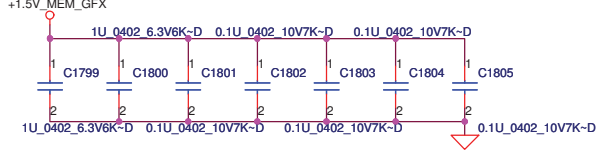
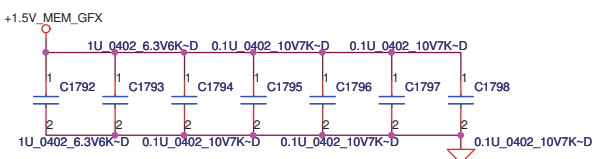
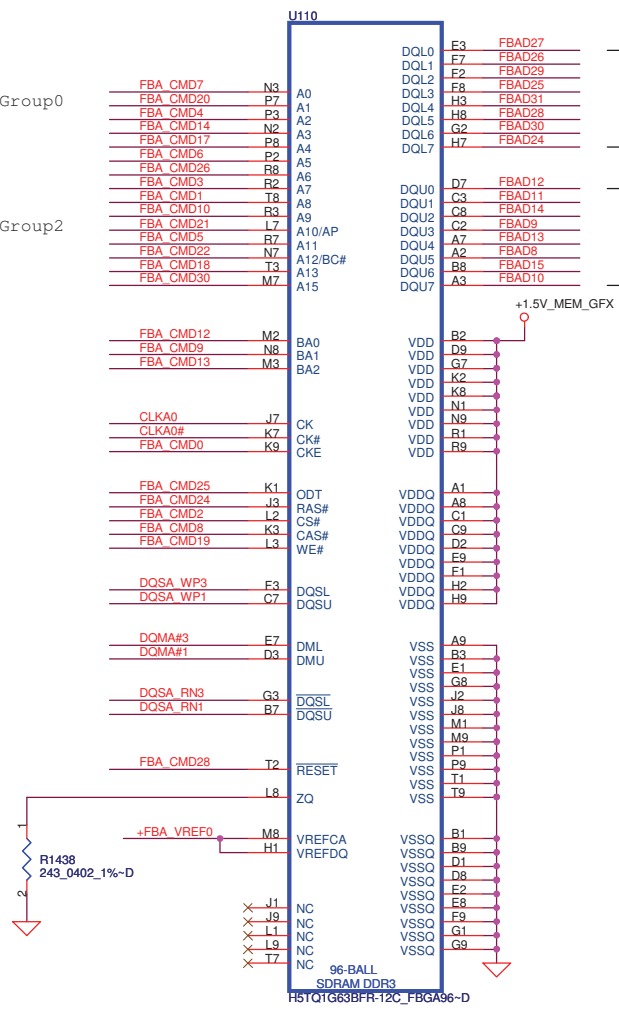
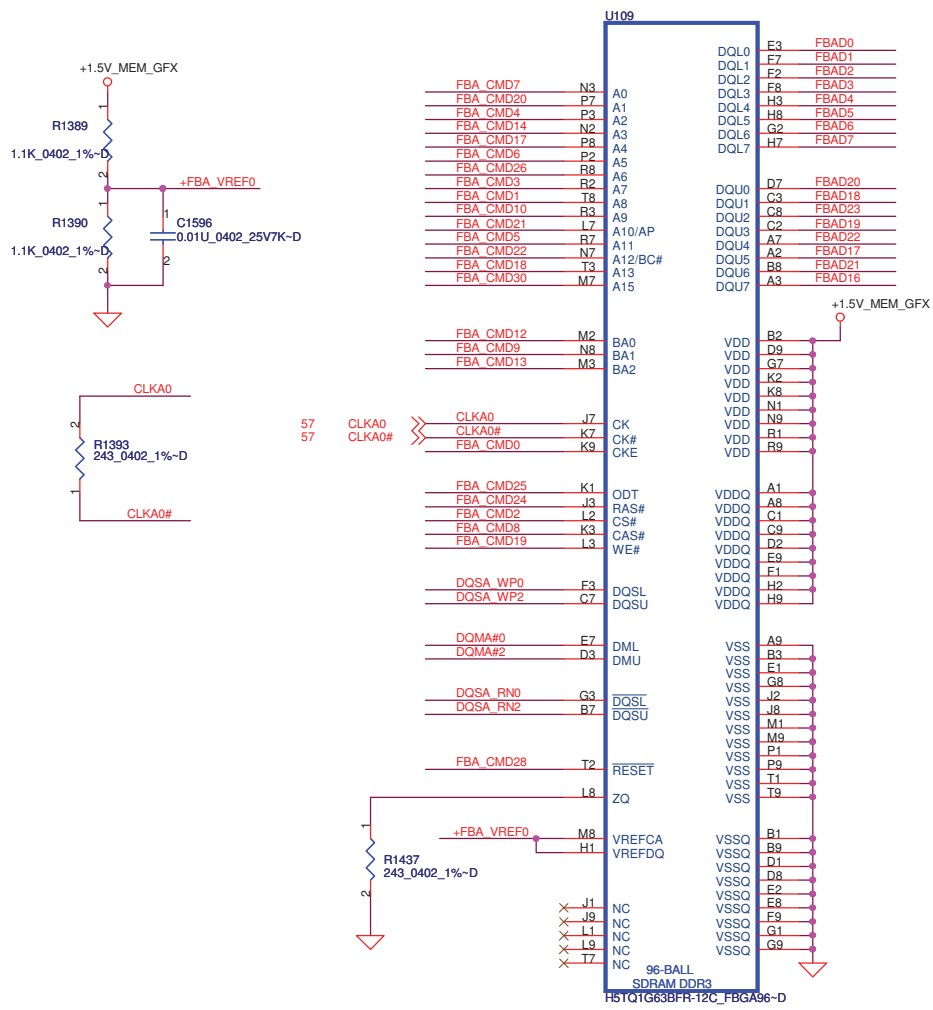
N10P Memory

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Memory Partition A - Lower 32 bits

- FBA_CMD[0..30] <<< FBA_CMD[0..30] 57,59
- FBAD[0..63] <<<>> FBAD[0..63] 57,59
- DQMA#[0..7] <<< DQMA#[0..7] 57,59
- DQSA_RN[0..7] <<<>> DQSA_RN[0..7] 57,59
- DQSA_WP[0..7] <<<>> DQSA_WP[0..7] 57,59

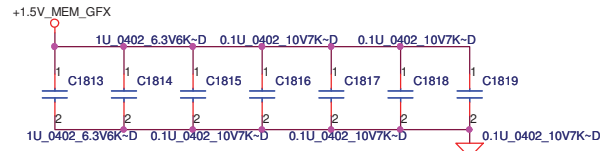
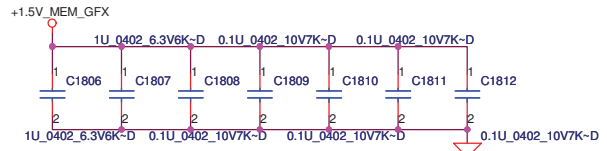
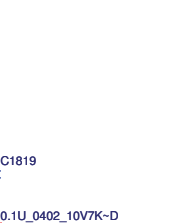
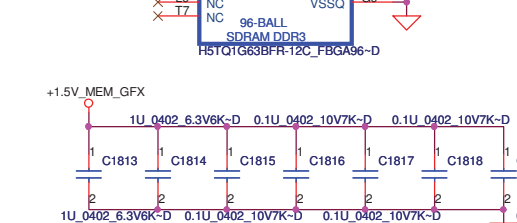
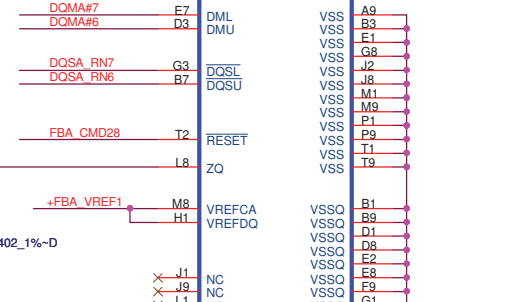
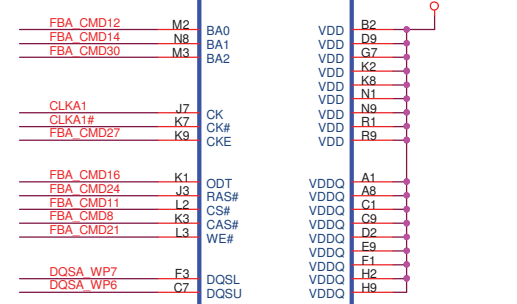
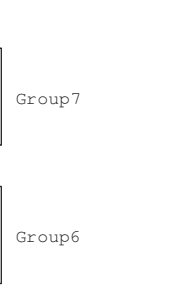
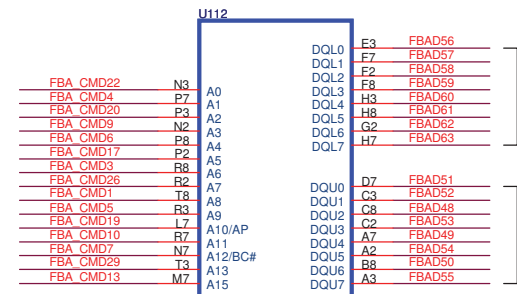
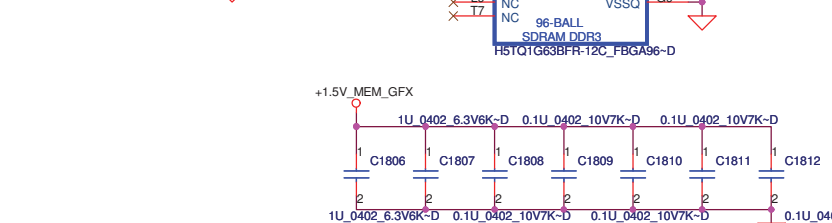
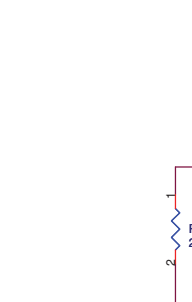
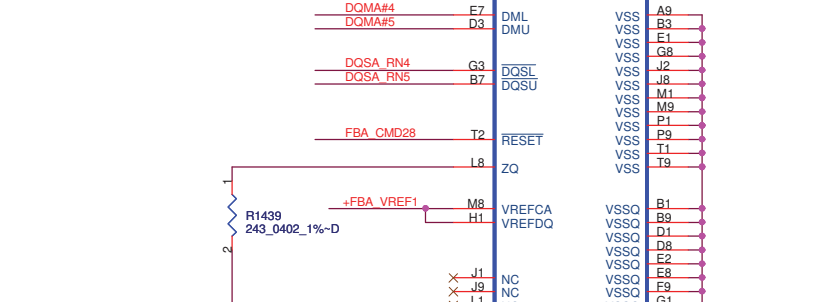
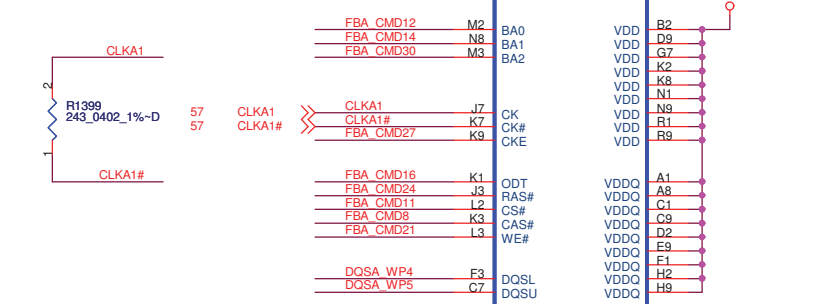
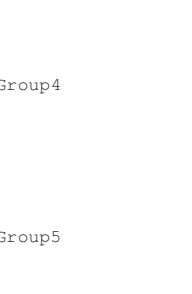
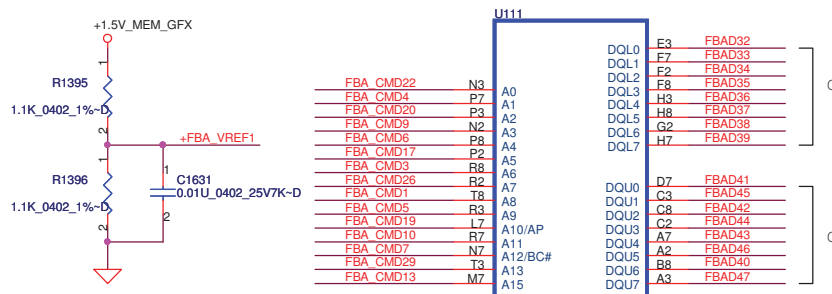


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Memory Partition A - Upper 32 bits

FBA_CMD[0..30] <<< FBA_CMD[0..30] 57,58
 FBAD[0..63] <<<>> FBAD[0..63] 57,58
 DQMA#[0..7] <<< DQMA#[0..7] 57,58
 DQSA_RN[0..7] <<<>> DQSA_RN[0..7] 57,58
 DQSA_WP[0..7] <<<>> DQSA_WP[0..7] 57,58

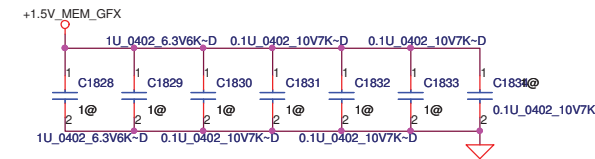
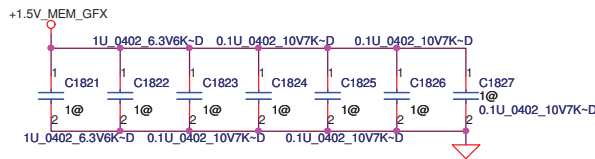
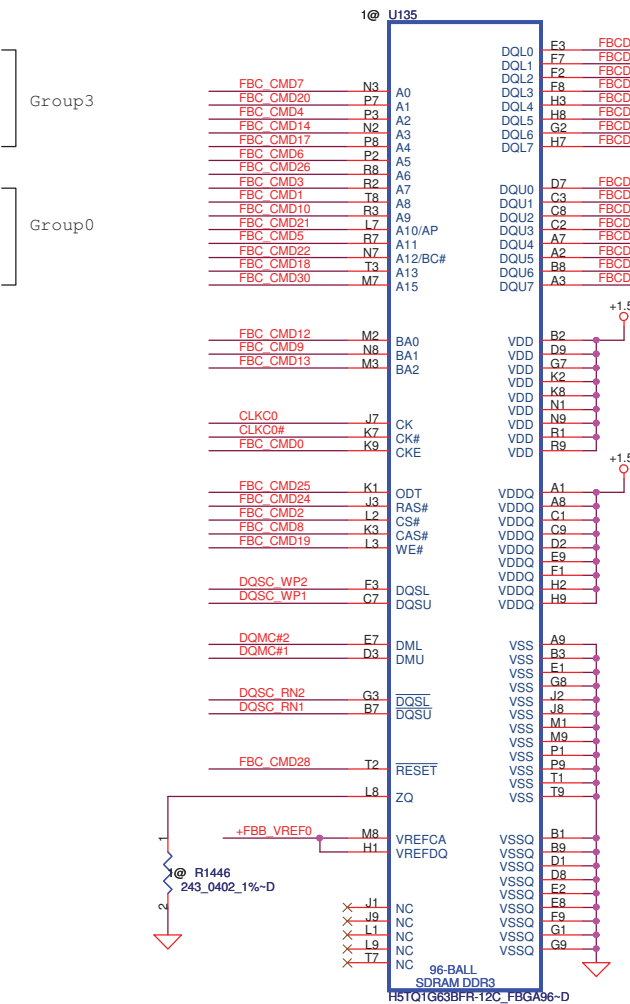
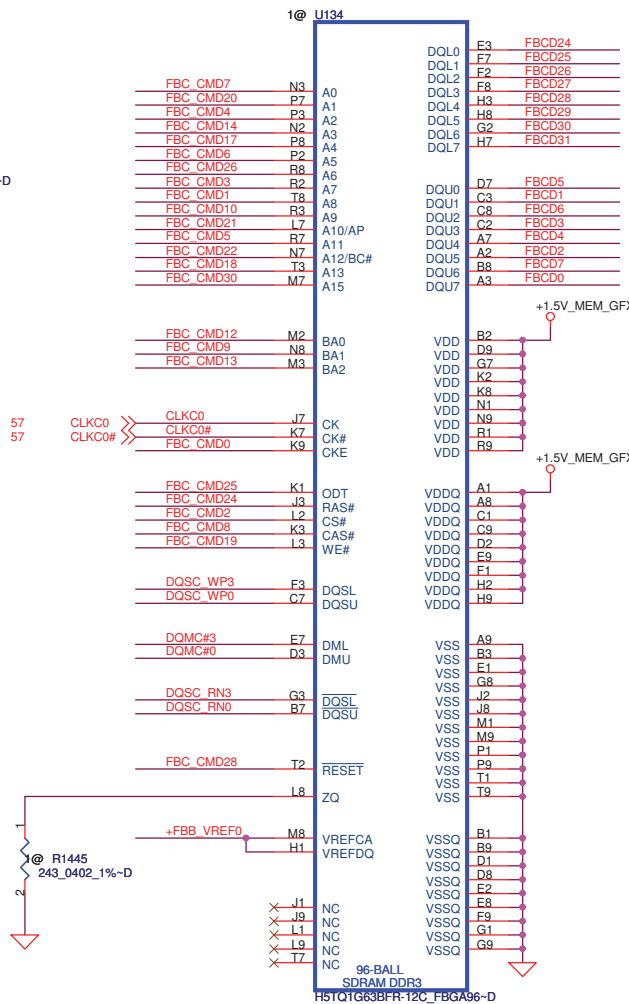
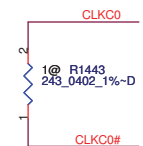
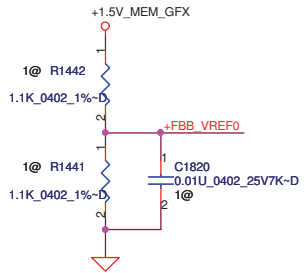


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Memory Partition C - Lower 32 bits

FB CD[0..63] <<>> FB CD[0..63] 57,61
 FBC_CMD[0..30] <<>> FBC_CMD[0..30] 57,61
 DQMC#[0..7] <<>> DQMC#[0..7] 57,61
 DQSC RN[0..7] <<>> DQSC RN[0..7] 57,61
 DQSC WP[0..7] <<>> DQSC_WP[0..7] 57,61



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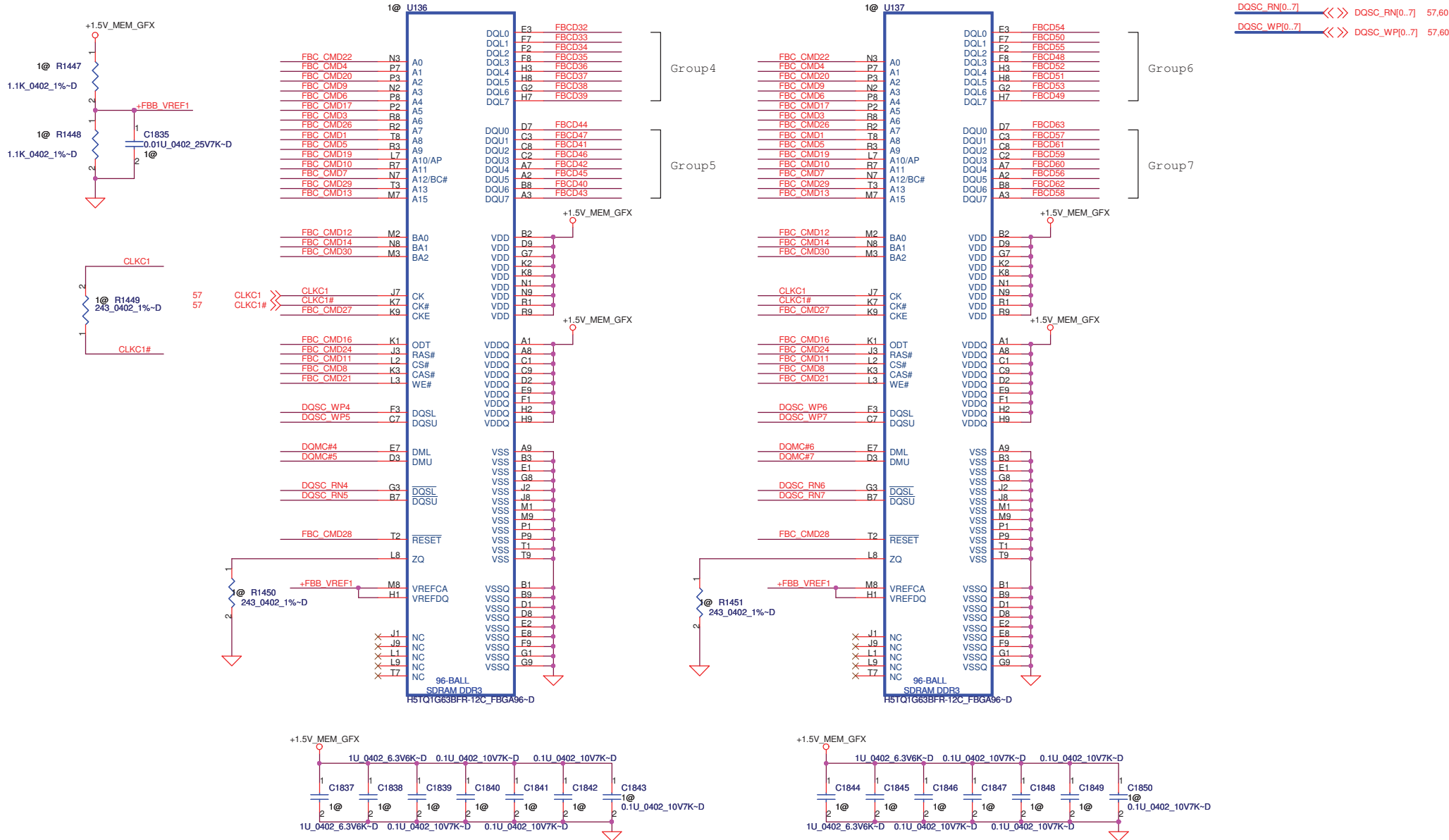
VRAM C Lower

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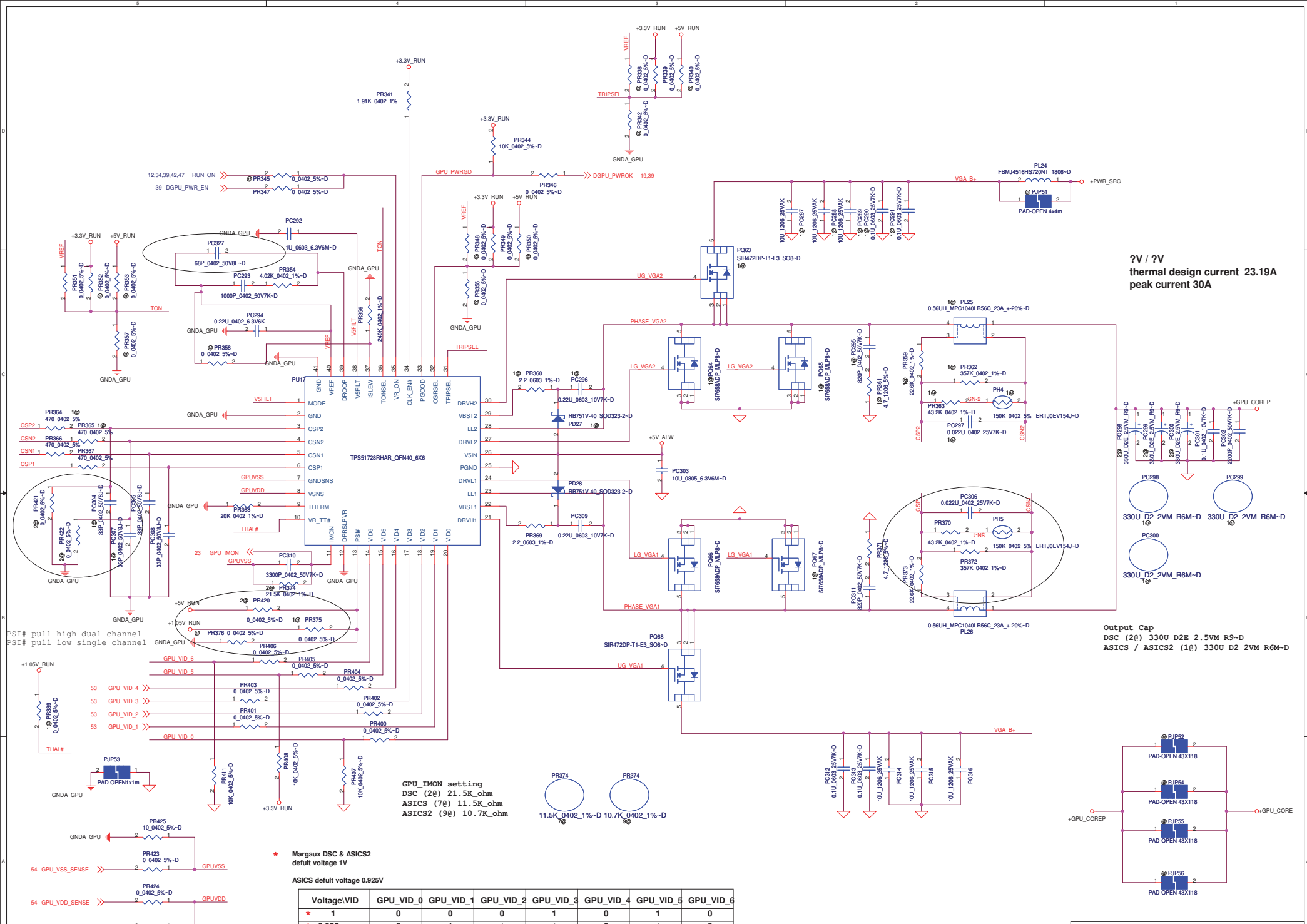
Memory Partition C - Upper 32 bits

FB CD[0..63] <<> FB CD[0..63] 57,60
 FBC_CMD[0..30] <<> FBC_CMD[0..30] 57,60
 DOMC#[0..7] <<> DOMC#[0..7] 57,60
 DQSC_RN[0..7] <<> DQSC_RN[0..7] 57,60
 DQSC_WP[0..7] <<> DQSC_WP[0..7] 57,60

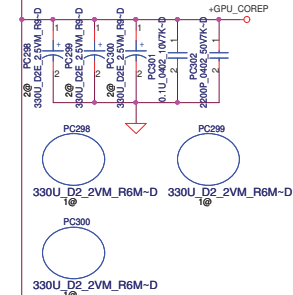


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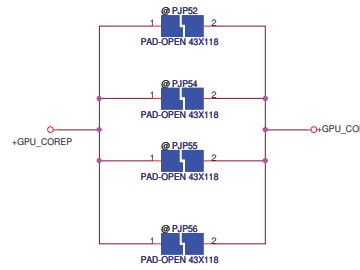
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?V / ?V
 thermal design current 23.19A
 peak current 30A



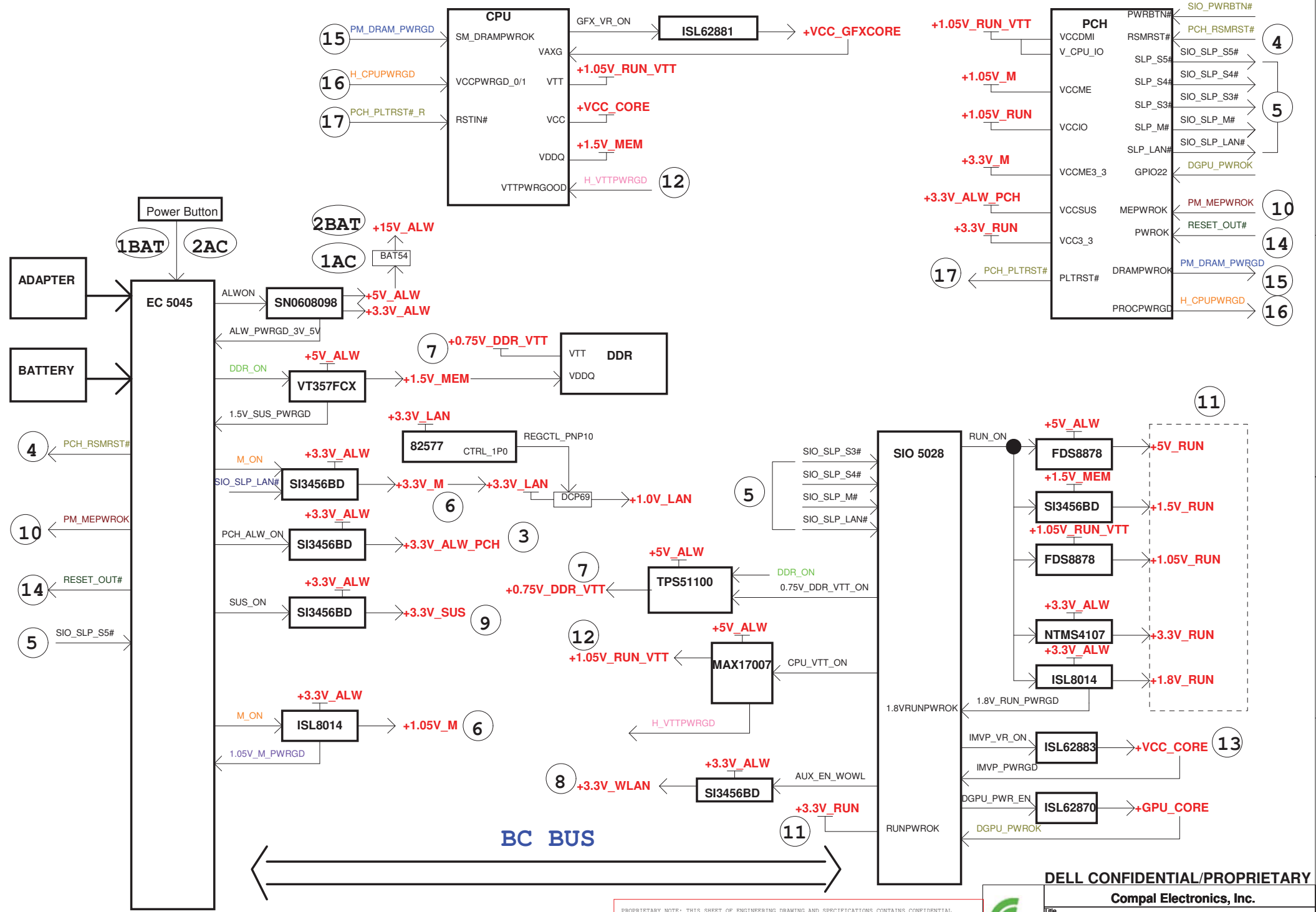
Output Cap
 DSC (2@) 330U_D2E_2.5VM_R9-D
 ASICS / ASICS2 (1@) 330U_D2_2VM_R6M-D



GPU_IMON setting
 DSC (2@) 21.5K_ohm
 ASICS (7@) 11.5K_ohm
 ASICS2 (9@) 10.7K_ohm

* Margaux DSC & ASICS2
 default voltage 1V
 ASICS default voltage 0.925V

Voltage/VID	GPU_VID_0	GPU_VID_1	GPU_VID_2	GPU_VID_3	GPU_VID_4	GPU_VID_5	GPU_VID_6
* 1	0	0	0	1	0	1	0
* 0.925	0	1	1	1	0	1	0
0.85	0	0	1	0	1	1	0
0.8	0	0	0	1	1	1	0



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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	8, 12, 13, 14, 42	HW	6/30/2009	Intel	Intel S3 reduction circuit.	Add R1469, R1471-R1480, C1872-C1877, Q199-Q204, change R624 to 27 ohm, pop Q78, add net DDR_HVREF_RST_GATE from U36.B36, CPU1.5V_S3_GATE from U36.B37, change CPU VDDQ net name to +1.5V_CPU_VDDQ	X01
2	40	HW	6/30/2009	COMPAL	Board ID	R98 change to 130k ohm	X01
3	43	HW	6/30/2009	COMPAL	for derating concern	Change R1001 from 82 to 150 ohm	X00
4	8	HW	6/30/2009	Intel	Follow CRB by Intel request	R1286 needs to change to 0-ohm	X00
5	39, 40	HW	6/30/2009	COMPAL	MEMO implementation	de-pop R1319, R595	X00
6	8	HW	7/01/2009	Intel	Intel S3 reduction circuit.	Change R879 to 2k, R880 to 1.1k, add U141	X01
7	55	HW	7/01/2009	COMPAL	Rdson concern by ADC	Change Q55/Q58/Q59/Q183 to SI4164	X01
8	8, 42, 47	HW	7/02/2009	Intel	Intel S3 reduction circuit.	Add R1481-R1484, Q205, Q206, Q207, C1877, PR428, change R879 to 1.5k, R880 to 750 ohm, change net DDR_HVREF_RST_GATE to U36.A34, CPU1.5V_S3_GATE to U36.A36	X01
9	30	HW	7/03/2009	COMPAL	+3.3V_LAN enable control follow M09	De-pop R47	X01
10	12	HW	7/03/2009	DELL	Intel S3 reduction circuit.	De-pop R1473, separated +V_DDR_REF_Q for each SO-DIMM, The dividers should use 1% part replacement for 5% as well	X01
11	8, 12, 13, 14, 42	HW	7/08/2009	DELL Intel	Intel S3 reduction circuit.	Add C1879, PJP57, PJP58, R1485, R1486, change Q205 to PMST3904, Q200 to AO4728L, R624 to 22 ohm, connect RUN_ON_CPU1.5VS3# to Q78.2 Q204.2,	X01
12	8	HW	7/09/2009	COMPAL	Intel S3 reduction circuit.	Add R1487	X01
13	24	HW	7/14/2009	COMPAL	Nvidia BIA PWM implementation	POP R165, de-pop R166	X01
14	8, 15	HW	7/14/2009	COMPAL	Depop all related components where are located at 0 Z-hight area	Depop JXDP1, JXDP2, JDEG1, JP2 circuit	X02
15	24	HW	7/14/2009	DELL	ENVDD_PCH connection	Remove D91 and connect ENVDD_GPU to 5028.pin B38	X02
16	19	HW	7/14/2009	Intel	GPIO1,6,7 PU if not being used	Add R1489-R1491	X02
17	24	HW	7/14/2009	COMPAL	Camera need to be changed from 7 to 8 pin	Change JEDP1 pin definition	X02
18	37	HW	7/16/2009	COMPAL	JTP1, JBI01 power gnd pins redefined	Change JTP1, JBI01 pin definition	X02
19	37, 40	HW	7/16/2009	SMSC	LAT_ON_SW# needs to be added a 1uF cap	Add @C1884, C1885, R1492, change R560 to 100K, JIO.32 change to LAT_ON_SW_BTN#	X02
20	23	HW	7/16/2009	SMSC	R594 has to be a group with R3P circuit	De-pop R594 for M09 fan solution	X02
21	31	HW	7/17/2009	Braodcom	Found both PD R898 and PU R485 pop	depopulate R898 for normal operation	X02
22	40	HW	7/17/2009	COMPAL	Board ID	Change R98 to 62K ohm.	X02
23	31	HW	7/17/2009	Braodcom	RFID disable circuit remove	Remove R1062-R1065	X02
24	28, 37	HW	7/17/2009	TI	Please reserve 1 resistor and connect connector (Pin1 or 7) to MAX4951	Add R1493 & R1494 at pin 18 of U95 & U96 for power saving	X02
25	31	HW	7/17/2009	Braodcom	+SC VCC Capacitor (C718) Value Change	Broadcom has recommended changing the value of C718 from .47uF to 220nF	X02
26	42	HW	7/17/2009	COMPAL	Backdrive EA Failure on Margaux/ASICS	Pop R625 and Q79	X02
27	24	HW	7/17/2009	DELL	eDP repeater change to SN75DP119.	update U46 circuit for eDP repeater	X02
28	23	HW	7/17/2009	COMPAL	R3P circuit by SMSC request	R536 depop for 3P FAN, R1457 change to 0 ohm, R138 change to 27K ohm	X02
29	21	HW	7/17/2009	Intel	The PLLs aren't used in a DIS system	De-pop C105 & C106	X02
30	33	HW	7/17/2009	TXC	EA result	C514, C515 have to change to 22pF	X02
31	36, 39	HW	7/22/2009	DELL	Reconnect the signal UWB_RADIO_DIS#	connect UWB_RADIO_DIS# from EC5028.A56 to MINI3.20	X02
32	23	HW	7/22/2009	DELL	Change FAN solution to M09	De-pop R3P circuit component & pop M09 solution	X02
33	42	HW	7/23/2009	COMPAL	de-rating result fail	Change Q61 from AO4456 to NTMS4107	X02
34	26	HW	7/23/2009	PERICOM	Pericom 8200 SW issue DVI can not work	Add R1495 to pull up U9 pin 23 (P1_OC0) of Pericom 8200 SW with a 4.7K ohm resistor to 3.3 RUN	X02
35	24	HW	7/23/2009	TI	eDP repeater DP119 vender review request	reserve pop option for X1EDP & DP119, change PU/PD to 20K.	X02
36	28	HW	7/23/2009	DELL	We will never disable the power to HDD redriver, go back connected in SSI	Remove R1493 & delete SATA_PWRSAVE	X02
37	18, 28, 40	HW	7/23/2009	DELL	There has been some confusion due to the net name showing active low	change net name HDD_FALL_INT1# to HDD_FALL_INT to show correct polarity	X02

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
38	29	HW	7/24/2009	DELL	use the SiTimes part due to the cost savings	change X4 from TXC to SiTimes.	X02
39	31	HW	7/24/2009	Broadcom	connect pin-L10 of U32 to pin-5 of U33, and disconnect pin-D2 from pin-5 of U33	pop R775, de-pop R776	X02
40	33	HW	7/24/2009	COMPAL	fixed SD/MMC Clock overshoot and undershoot	Changing R8 dumping from 0-ohm to 10-ohm	X02
41	31	HW	7/24/2009	Broadcom	BCM5880 Leakage Issue on Margaux	Add Q208,Q209,R1496 circuit to fix.	X02
42	37, 39	HW	7/27/2009	DELL	ESATA repeater power saving	Add a 0 ohm jumper between EN pin and VDD, but no-pop it. Then connect the EN pin to 5028.A47 with a 0 ohm jumper that is popped.	X02
43	39	HW	7/27/2009	DELL	Sometimes VGA_ID_DISC and VGA_ID_UMA both read as low	Change R875 and R881 to +3.3V_ALW rail.	X02
44	23	HW	7/27/2009	SMSC	SMSC review feedback	The pull-up source of the R150 should be changed to +VCC_4002	X02
45	31	HW	7/27/2009	NXP	Better for decoupling noise	Change C1015 ,C633 to 10pf	X02
46	36	HW	7/27/2009	DELL	For PCH GPIOs rail.	PCIE_MCARD3_DET# & USB_MCARD1_DET# pull-ups (R458 & R438) need to change from +3.3V_ALW_PCH rail to +3.3V_RUN rail	X02
47	11	HW	7/27/2009	Intel	The VCC_Core de-coupling requirements for Clarksfield XE processor	C60-64, C66 change to 470uF/4mOhm, C44-C59 change to 22uF(0805)	X02
48	23, 40	HW	7/29/2009	SMSC	per SMSC 5045 AN 19.6, 4002 AN 16.11	R541, R554, R1492 should be 10K, R147 should be populate, Add R1498	X02
49	35	HW	7/29/2009	DELL	Braidwood has been removed from IbeX Peak platforms	De-pop JBW1 & R1453	X02
50	39	HW	7/29/2009	DELL	GPIO MAP update	change net name from RESERVED FOR ESATA to EN_ESATA_RPTR	X02
51	42	HW	7/29/2009	Compal	By Intel S3 timing concern	reserve R1500 & @R1499 0 ohm for Q206.2 from RUN_ON_CPU1.5VS3# & RUN_ON_ENABLE#	X02
52	37	HW	7/30/2009	Intel	Intel continues to recommend that all pre-production and production motherboards include common mode choke footprints to enable a stuffing option in case a choke is required to pass EMI testing	Add @L30, @L31, R424-R427	X02
53	31	HW	7/30/2009	Broadcom	Broadcom schematic review request	pop R537; Remove C647, C641,R634, R498, R898; Add @C1886 & @C1887; Remove L73, R631, C1026, R494, Short net RFREADER_TXN1_PI_R to RFREADER_RXP_C; Remove C642, C640, change R487, R496 to 0 ohm; Add @R1501; de-pop R496 & R497; JCS1 pin2 & pin3 and pin4 & pin5 should be short to carry higher current.	X02
54	31	HW	7/30/2009	Compal	Solve smart card cage vender reverse pin definition.	Reverse JCS1 pin definition	X02
55	31	HW	7/31/2009	Broadcom	Broadcom schematic review request	The pin1 of R497 and R496 should be connected to GND	X02
56	15, 40	HW	7/31/2009	KDS	KDS crystal EA result	change DIS C296 & C297 to 12pF, C674, C675 to 33pF	X02
57	8, 15	HW	7/31/2009	Intel	For XDP debug concern	Populate all the resistors and leave out the connector	X02
58	27	HW	8/03/2009	Compal	CRB EA result	C251-C253 to 4.7pF; L61-L63 to 10-Ohm Bead ; De-pop C996, C518, C390	X02
59	23	HW	8/03/2009	Compal	If populate R147 PU resistor for THERM_STP#, it will impact ALWON signal at MEC 5045	De-pop R147	X02
60	15, 40	HW	8/04/2009	KDS	KDS crystal EA result	change DIS C427 change to 200 ohm, C514, C515 back to 15P and change X3 from CL=16pF to CL=12pF	X02
61	8	HW	8/05/2009	DELL	fix the Intel S3 power up timing	change C1877 from 0.01uF to 0.22uF 0402 cap.	X02
62	28, 37	HW	8/06/2009	Compal	Per ESATA/SATA EA result	pop R1301, R1304, de-pop R1298, R1308	X02
63	28	HW	8/06/2009	Compal	ODD_DET# PU from +5V_MOD to +3.3V_RUN	connect R1239.1 to +3.3V_RUN & pop R1239	X02
64	42	HW	8/06/2009	SMSC	Watch dog timer may not be resetED when 4002 VDD_PWRGD is not completely at Logic Low	Pop R616 to 39 & pop Q72	X02
65	30	HW	8/10/2009	Intel	Remove the VCT trace	Remove @R562, @C41	X02
66	35	HW	8/10/2009	DELL	Braidwood Removal on RAM	Remove @JBW1, @C1851, @R1452, @R1453, @C1852, R1411	X02
67	31	HW	8/11/2009	Broadcom	Broadcom review request	Remove @R1061, Change C718 value to 470pF, change C646 value to 220pF. pin2 of R470 should have a 0ohm but de-pop resistor to USB_GPIO27 net.	X02

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
68	8	HW	8/11/2009	Intel	Intel review request	add @R1504 for DDR3_DRAMRST# CPU PD & add C1888 for PM_DRAMRST# to slow down gate of FET	X02
69	33	HW	8/11/2009	Richo	Change pop option for R5U242	Change C21 from 10U to 47U, change R46 to C1889 (1uF)	X02
70	38	HW	8/11/2009	Compal	For DVI DOCK issue	Add R1505-R1508	X02
71	21	HW	8/12/2009	Intel	Follow CRB rev 1.6 schematic	No stuff C111 and C112	X02
72	31	HW	8/12/2009	Broadcom	Per Broadcom request	pop R496 & R497 (0 ohm)	X02
73	31	HW	8/12/2009	Compal	Smart card EA result	change R772 to 47 Ohm for resolving SC_CLK Rise/Fail timing issue	X02
74	8	HW	8/12/2009	Intel	Follow Intel S3 white paper rev0.9	pop R1504 & change C1888 to 470pF	X02
75	37	HW	8/12/2009	DELL	add a pull-up to +3.3V_ALW for IO_LOOP	change R835.1 from +3.3V_ALW_PCH to +3.3V_ALW	X02
76	37	HW	8/12/2009	Compal	disconnect IO & DOCK VCT	rename IO VCT to +LOM_VCT_IO & reserve C712 pad for test.	X02
77	31	HW	8/13/2009	Broadcom	Per Broadcom request	need to have 4.7K pull-up to 3.3V_ALW for BCM5882 pin-C1 "RSTOUT_N"	X02
78	8	HW	8/13/2009	DELL	Avoid a glitch for DDR_HVREF_RST_GATE, please add a 1.1K 1% no-stuff pull-up to +1.5V_CPU_VDDQ rail on the PM_DRAM_PWRGD_R signal for a back-up option	change C1888 to 0.1u, add @R1511 for PM_DRAM_PWRGD_R	X02
79	8,45	HW	8/13/2009	DELL	CPU detection since the edge diode has been removed from M'09	Add R1512 for CPU_DETECT# and connect JCPU.AH24 to U36.B18	X02
80	37	HW	8/14/2009	DELL	Invert the EN_ESATA_RPTR signal and connect this to SATAGP4/GPIO16	Add @R1513 & @Q210, pop R1494 and de-pop R1497, change net name from GPIO16 to EN_ESATA_RPTR#	X02
81	33	HW	8/14/2009	Compal	Solve 1394 impedance issue	Change R399, R400, R401, R403 to 54.9 ohm.	X02
82	37	HW	8/14/2009	Compal	EMI solution	pop L30 & L31, de-pop R424-R427	X02
83	38	HW	8/17/2009	NV	Solve DIV issue	Add Q211-Q216, R1514-R1521 for SW DDC PU.	X02
84	11	HW	8/17/2009	Compal	PWR team request	de-pop C66, C64, change C60-C63 to 330uF, C44-C59 to 10uF, can meet Intel spec.	X02
85	55	HW	8/18/2009	NV	Reserve crystal for 27M.	add @R1522, @y7, @C1890, @C1891	X02
86	26	HW	8/19/2009	Pericom	8200 pin 8,9 add cpas to minimize noise	Add C1597 & C1598	X02
87	29	HW	8/19/2009	COMPAL	EMI solution	C676 to 150pF and R1295 to L4 (220 ohm), POP C1121-C1124, C1145-C1148	X02
88	33,34	HW	8/20/2009	COMPAL	EMI solution for SD CLOCK & EXP card USB	R8 change to 22 ohm, pop L64 & depop R791, R792	X02
89	11	HW	9/11/2009	DELL	To meet Intel spec	C60-C63, Margaux DIS-->330uF, Asics/Asics II-->470uF	X02
90	55	HW	9/11/2009	DELL	27M crystal for NV	add Y7, C1890, C1891, R1522, R1417, de-pop R617, R1317, R43, R39	X02
91	21	HW	9/11/2009	Intel	Intel request	de-pop C39, C610	X02
92	31	HW	9/11/2009	Broadcom	Broadcom review feedback	change C718 from 470p to .47u, C646 from 220p to .22u	X02
93	30	HW	9/11/2009	Intel	Follow Intel document request	change R1502 to C427 10pF, C475, C476 to 33pF	X02
94	35	HW	9/11/2009	Compal	Add PD 10k for Minicard PWR	Add R1523-R1525	X03
95	31	HW	10/23/2009	Compal	Smart card connector DFM issue	change JSC1 type (the same with Rothschild)	X03
96	54	HW	10/23/2009	NV	JTAG TRST#: Populate R1372 with 1K resistor.	Change R1372 to 1K and pop	X03
97	40	HW	10/23/2009	COMPAL	Board ID	Change R98 to 4.3K ohm.	X03
98	17	HW	10/23/2009	Intel	Intel schematic check list 2.0 request	R268 change from 1k ohm to 10k ohm, R672 change from 0.5% to 5%	X03
99	40	HW	10/23/2009	SMSC	SMSC review feed back	R561 and R1046 are too large it is recommend that no PU/PD be larger than 100K	X03
100	12,42	HW	10/23/2009	COMPAL	avoid double bleed off	+3.3V_M, +3.3V_RUN, +1.5V_CPU_VDDQ power plane discharge circuit have been pop, de-pop R612, R607, R1471.	X03
101	36	HW	10/23/2009	DELL	support WiMax LED status	Need to populate R840	X03
102	16,32	HW	10/25/2009	COMPAL	Change R910 placement	Please put R910 close to PCH not TCM chip	X03
103	41	HW	10/25/2009	COMPAL	Touch Pad PU need to move from 5V to 3V	R613, R614 change power rail from +5V_ALW to +3.3V_ALW	X03
104	31	HW	10/28/2009	Broadcom	For 5882-B0 request	L71, L72 68nH, 2%, 400mA; C1070, C1071 1500pF, 2%, 50V; C1886, C1887 150pF, 2%, 50V	X03
105	29	HW	10/28/2009	IDT	create a low pass filter with the pole set at 36kHz to filter out of band noise	de-pop C1066 & C1067, R1090, R1089 ; R340 & R342, R1091 & R1092 change to 2k, add C1894-C1897 1000pF.	X03
110	29	HW	10/28/2009	COMPAL	ME request for JSPK1 swap	JSPK1 Pin 2 and pin 4 swap, pin 3 and pin 5 swap	X03

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111	8, 12, 13, 15, 16, 28	HW	10/29/2009	DELL	MEM SMBus design needs to change	Move Q190 connection, add R1528,R1529, add net name DDR_XDP_CLK/DAT	X03
112	31	HW	10/29/2009	DELL	smart card clock resistor	Change R772 from 47 ohm to 22 ohm	X03
113	37	HW	10/29/2009	COMPAL	EMI concern	pop R15 with 10 ohm and C15 with 10pF	X03
114	36	HW	10/29/2009	COMPAL	USB MCARD2_DET# change to +3.3V_ALW_PCH	R447 pull up should change to +3.3V_ALW_PCH	X03
115	40	HW	10/29/2009	COMPAL	avoid RESET_OUT# double PD	de-pop R5	X03
116	15	HW	11/02/2009	COMPAL	EMI, RF team concern	pop C300, C302	X03
117	24	HW	11/04/2009	COMPAL	LCD power sequencing issue	change R161 from 470 to 130 ohm .	X03
118	37	HW	11/05/2009	COMPAL	EMI concern	Change choke vender from Murata to Delta on L30,L31	X03
119	29	HW	11/05/2009	COMPAL	RF team concern	X4 change from Sitime to TXC	X03
120	15	HW	11/05/2009	COMPAL	RTC issue	Y1 & Y4 change from 30ppm to 10ppm.	X03
121	15	HW	11/05/2009	COMPAL	For flash ROM EOL issue	U13 change from W25X32 to W25Q32	X03
122	19	HW	11/09/2009	DELL	PCH driving the siganl low at GPIO15 initial	add R1530 2.2K PU resistor to +3.3V_ALW_PCH on the SIO_EXT_WAKE# signal.	X03
123	55	HW	11/10/2009	COMPAL	By power team request	Please pop 22u*2 at original reserved location C1722 and C1723.	X03
124	39	HW	11/10/2009	DELL	add a 10K 5% PU to +3.3V_RUN on ME_FWP	Add R1531	X03
125	24, 53	HW	11/11/2009	NV	By NV review request	pop R180, de-pop R181; change GPU booting voltage setting, GPU_VID1: @Q4, 7@R1374, 8@R1361, GPU_VID4:pop R1379, GPU VID2: 7@R1357, 8@R1360, GPU_VID3: pop R1354	X03
126	15, 28	HW	11/13/2009	COMPAL	To cut redundant trace for SMBUS	Add @R1532/R1533/R1534/R1535	X03
127	19	HW	11/17/2009	Intel	By Intel check list request	Add R1544 for PCH GPIO34	X03
128	41	HW	12/24/2009	Compal	To solve touch pad ESD issue	Change L41 and L42 to R1545 & R1546 with 100 ohm.	X03
129	29	HW	12/24/2009	Compal	RF noise issue concern	change Sitime 12MHz oscillator X4 to driver strength 1x	X03
130	15	HW	12/24/2009	Intel	Follow Intel check list rev2.0	Change R224 to tolerance from 5% to 1%	X03
131	36	HW	12/24/2009	DELL	Wimax LED abnormal operation.	de-pop R1409	X03
132	11	HW	12/24/2009	Compal	PWR team request	Change C60-C63, add C66 to 330uF for Ascis/AsicsII	X03
133	38	HW	12/24/2009	Compal	Simplo battery slice EMI issue	Add C1898 and C1899(Depop, reserve for EMI test)	A00
134	31	HW	12/24/2009	Braodcom	By Broadcom request	Change L71,L72 from 68nH to 150nH, C1070,C1071 from 1500pF to 390pF.C1887, C1888 from 150pF to 390pF.	A00
135	40	HW	12/30/2009	DELL	Board ID	Change R98 from 4.3K to 1K for A00	A00
136	33, 34	HW	12/30/2009	COMPAL	Change R5U242 to rev ES3	Change U94 from ES2 to ES3	A00
137	8, 15	HW	12/30/2009	Intel	De-pop XDP & JTAG resistor	de-pop C19,C20,R6,R7,R68,R19,R3,R1153,R1156,R1157,R66,R1241,R780-R785, R22,R24,R78,R91,R101-R116,C1375,R69,R118,R123,R804,R807,R805,R806,R1281, R1282,R1315	A00
138	28, 37	HW	01/15/2010	COMPAL	Change Esata repeater for power save	Change U95 U96 from 412 to 412A	A00
139	27	HW	01/15/2010	COMPAL	EMI concern	Change L61-L63 to 27nH, C251-C253 to 2P, pop C390, C518, C996	A00
140	11	HW	01/18/2010	COMPAL	No stuff MLCC caps to fix Acoustic noise	de-pop C46, C48, C50, C52	A00
141	15	HW	01/21/2010	COMPAL	For factory to do JTAG test	Pop R123, R804-R807, R1281, R1282, R1315	A00

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1	50	+VCORE_DSC	6/12	Dell	Adjust Vimon	ASICS and ASICS2 Change PR184 to 7.5K	
2	62	Graphic ASICS	6/19	TI	Adjust compensation	DSC Change PR370 to 43.2K, PR372 to 357K, PR373 to 22.6K, PC 306 to 0.022uF ASICS/ASICS2 Change PR370&PR363 to 43.2K, PR372&PR362 to 357K, PR373&PR359 to 22.6K, PC306&PC297 to 0.022uF	
3	62	Graphic ASICS	6/19	TI	Droop circuit add cap for filtering the noise	DSC, ASICS and ASICS2 Change PD26 to PC327 68pF	
4	62	Graphic ASICS	6/19	TI	Adjust to operate single phase	DSC PR364,PR365,PC304,PC307 unpop and add PR421&PR422 0_ohm to avoid PIN3,4 floating Add PR420 0_ohm connect +5V_RUN to control PSI# for Single phase	
5	62	Graphic ASICS	6/30	TI	add 0_ohm for cut power rail to debug	Add PR423 PR424 PR425 PR426	
6	62	Graphic ASICS	7/01	TI	CSS GC logic wrong issue	Add PR427 180_ohm to GND	
7	62	Graphic ASICS	7/2	ADC Guangyong 090612	Change PR374 and PC310 reference GND to GPUVSS	connect PR374 and PC310 pin1 to GPUVSS	
8	50	+VCORE	7/14	Dell / intersil	change Cisense GND to VSUM-	PC174 PC175 PC176 pin2 connect to VSUM-	
9	52	Selector	7/16	Compal	Add 1M_ohm pull down to fix ACAV_IN_NB oscillation when battery mode S5	Add PR429	
10	52	Selector	7/22	TI	new version CD3301 (PG2.1) dont need PD21	un-pop PD21 add PR430	
11	53	Selector	7/22	TI	DOCK_AC_OFF_EC floating issue	add PR431	
12	62	Graphic ASICS	8/3	TI	Pin38 V5FILT is output pin. don't need to connect to power rail.	Delete connection to +5V_RUN	
13	45 / 49 50 / 51	+5V/+3.3V +1.1VTT +Vcore charger	8/11	Compal / EMC	solve EMI issue	pop PC32 PC33 PR36 PR39 PL15 PC155 PC165 PC182 PR153 PR173 PR191 PL24 add PL27	
14	50	+VCORE	8/13	Intersil	Adjust Imon and Load line	PR195 change to 619, PR175 change to 2.43K, PR387 change to 15K PR184 change to 8.45K, add PR432 34.8K and PQ75 (PR432 and PQ75 un-pop Merle 0820) PC171 change to 0.068uF, PC183 add 0.022uF	
15	49	+1.1VTT	8/13	DELL	Improve ESD	PQ74 change SB57002528L to SB00000DH0L	
16	51	Charger	8/13	Dell / TI	change PU13 to BQ24747 to improve IC ESD to change strong	change PU13 from SA00001RK0L to SA00003KX0L	
17	48	+1.05V_VM_DSC	8/13	TI	change from TPS51318 to SN0905030	change PU8 to SN0905030	
18	45	+5V/+3.3V	8/17	TI/Compal	adjust OCP setting	Change PR31 from 243K to 294K, PR32 from 232K to 261K(DSC) 158K(ASICS)	
19	46	+1.5V_MEM_DSC	8/17	TI/Compal	adjust OCP setting	Change PR71 from 61.9K to 39.2K	
20	50	+VCORE	0820	Dell EMC	Add 2 2200pF caps. (jerry lin 0820)	Add PC328 PC329	

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21	44	+DCIN	10/23	TI/Compal	slow soft star to fast issue	Change PR20 from 0_ohm to 10K.	
22	49	+1.1VTT	10/23	Intel	VTT power good voltage level change	Change PR124 from 28.7K to 9.31K. Change PR128 from 10K to 2.74K.	
23	51	Charger	10/23	Compal EMI	EMI solution	pop PC214 1000pF, PR234 4.7_ohm	
24	49	+1.1VTT	10/23	Maxim	fix VTT drop issue	ILIM = 30mV, un-pop PR104, PR103=0_ohm, PC130=220pF PR110, PR120=1.58K_ohm ; PR113, PR122=6.98K_ohm ; PR114, PR123=0_ohm Ceq PC132, PC144 =0.22uF ; Filter PC133, PC145=un-pop ; PR115, PR129=0_ohm REF capacitor PC137 change to 2.2nF ; REFIN PR117, PR118 and PR119 increase by 10x Add PR432, PR433 for dual remote sense	
25	51	Charger	10/23	TI	Reduce CD3301 pin34 pin 35 peak current	Change PR392 to 0805 size.	
26	51	Charger	11/10	Compal	ACAV_IN_NB level adjust. (10/29)	Change PR246 from 21.5K to 22.6K	
27	50	+Vcore	11/17	Compal	pop PC190 PR201 for improve 2nd source FDIM	pop PC190 PR201	
28	49	+1.1VTT	01/20	Maxim	fix dual pulse issue	pop filter PC133, PC145=1000p ; PR115, PR129=10_ohm	
29	51	Charger	01/20	Compal	reduce surge current. (for CD3301)	Change PR392 form 0_ohm to lohm change PC199 from 1uF to 0.1uF	
30	51	Charger	01/20	Compal	EMI can pass without this bead. remove for cost saving.	un-pop PL27	
31	62	Graphic ASICS	8/3	Compal	RF boardband issue	pop PC295 PC311 820pF , pop PR361 PR371 4.7ohm.	
32	49	+1.1VTT	01/20	Compal RF/EMI	fix RF boardband issue	change PC131 PC146 from 680pF to 820pF	