

COMPAL CONFIDENTIAL

MODEL NAME : *JAL20*

PCB NO : *LA-4043P (DA80000CV0L)*

BOM NO : *43164831L01(TPM)*

43XXXXXXXX (Non TPM)

M09 Maybach UMA uFCPGA Mobile Penryn Intel Cantiga GM + ICH9M

2008-10-22

REV : 0.1(X00)

@ : Nopop Component
3@ : disable TPM
4@ : enable TPM

Fix Function Field

MB PCB

Part Number	Description
DA80000CV0L	PCB 03N LA-4043P REV0 M/B LOW COST

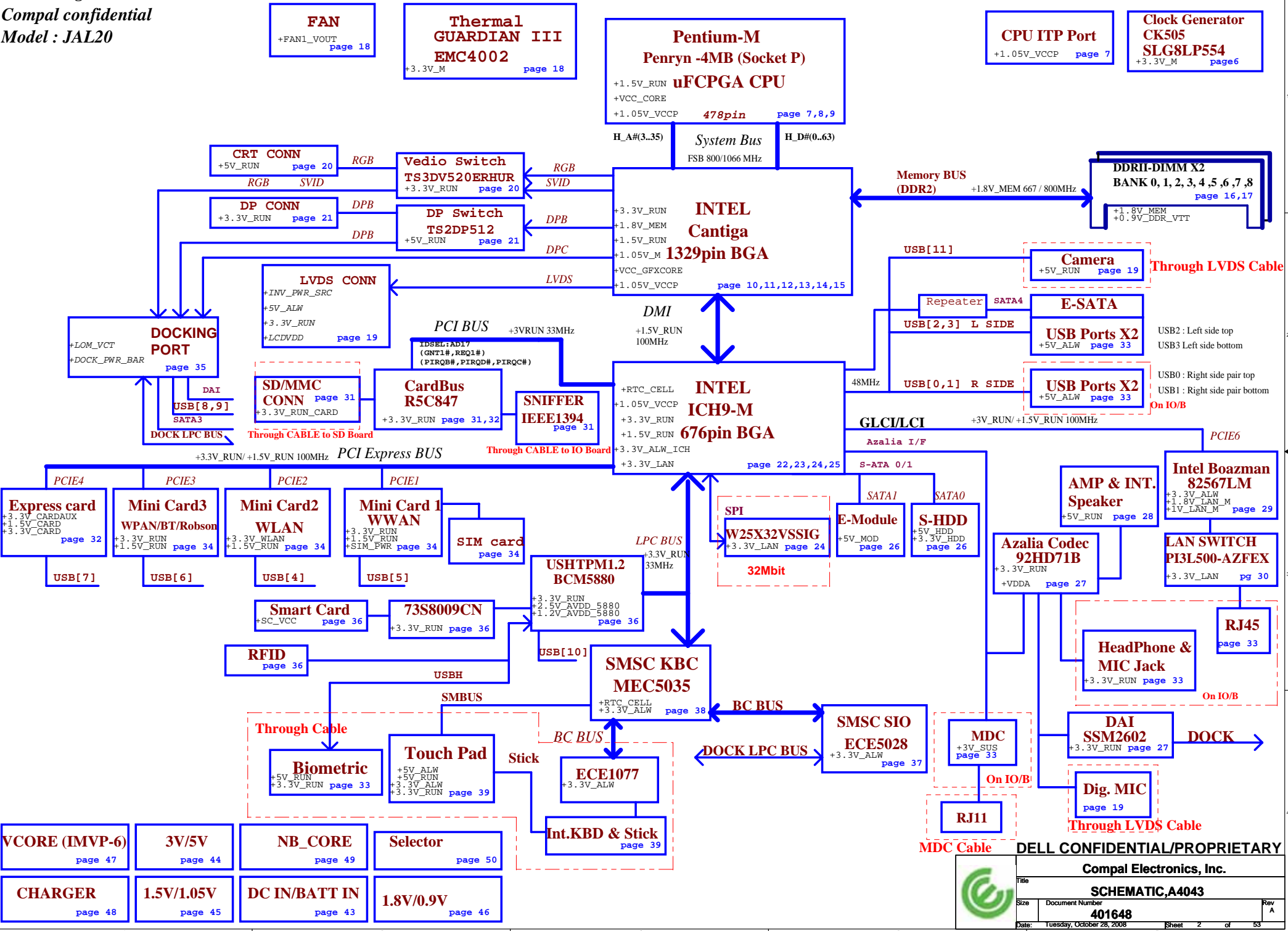
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POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	ON
S4 (Suspend to DISK) / M1	LOW	HIGH	HIGH	LOW	HIGH	ON	ON	ON	OFF	ON
S5 (SOFT OFF) / M1	LOW	HIGH	LOW	LOW	HIGH	ON	ON	ON	OFF	ON
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State \ power plane	+15V_ALW +5V_ALW +3.3V_ALW_ICH +3.3V_RTC_LDO	+3.3V_SUS +1.8V_MEM	+5V_RUN +3.3V_RUN +2.5V_RUN +1.5V_RUN +0.9V_DDR_VTT +VCC_GFXCORE +VCC_CORE +1.05V_VCCP	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
R5C847	AD17	REQ#1 / GNT#1	PIRQ[B..D]

ICH9-M	USB PORT#	DESTINATION
	0	JUSB1 (Ext Right Side Top)
	1	JUSB1 (Ext Right Side Bottom)
	2	JESA1 (Ext Left Side Top)
	3	JESA1 (Ext Left Side Bottom)
	4	WLAN
	5	WWAN
	6	WPAN
	7	Card Bus/Express card
	8	DOCKING
	9	DOCKING
	10	USH->BIO
11	Camera	

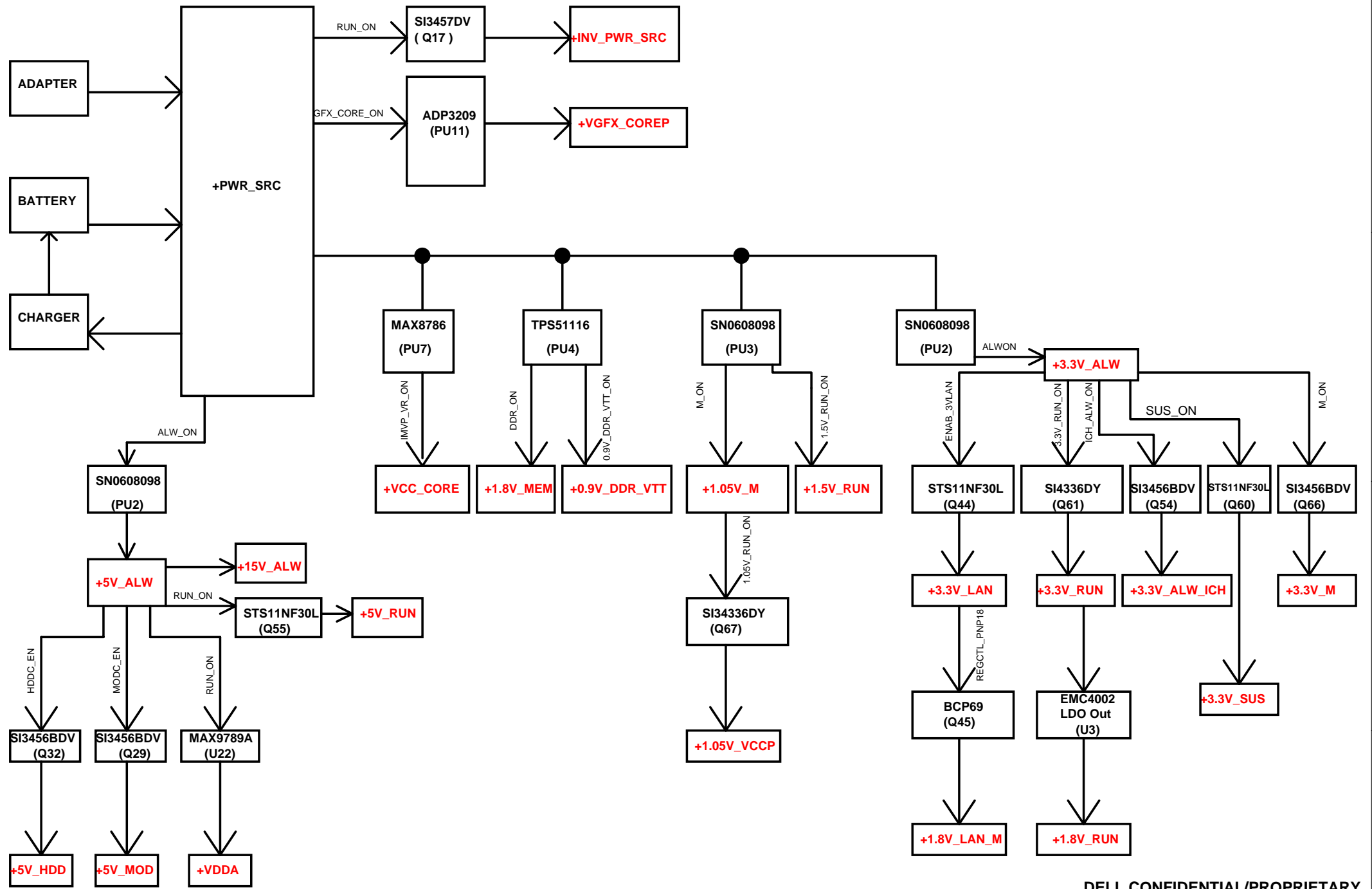
PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	MINI CARD-3 BT/UWB
Lane 4	EXPRESS CARD
Lane 5	None
Lane 6	10/100/1G LAN

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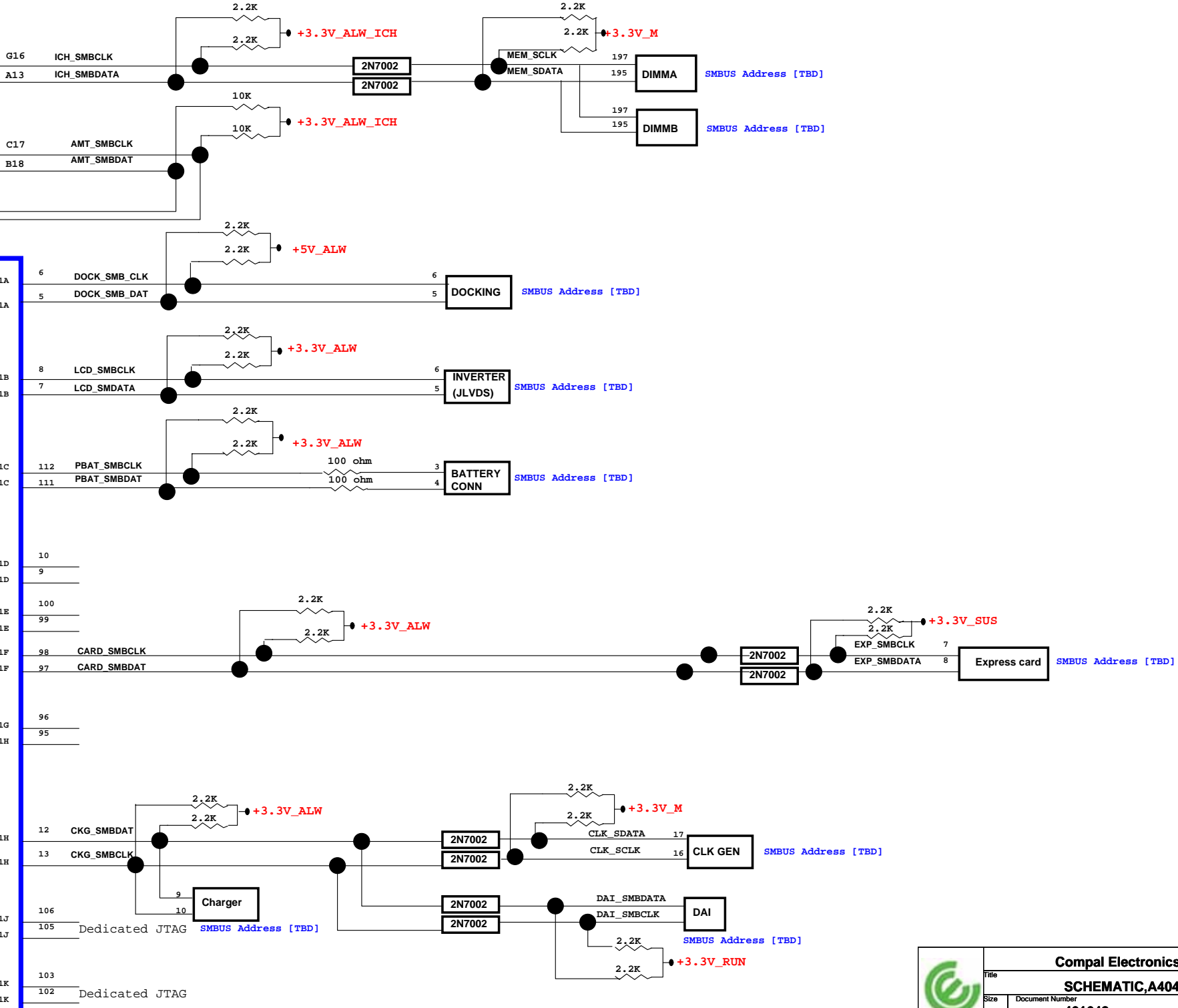
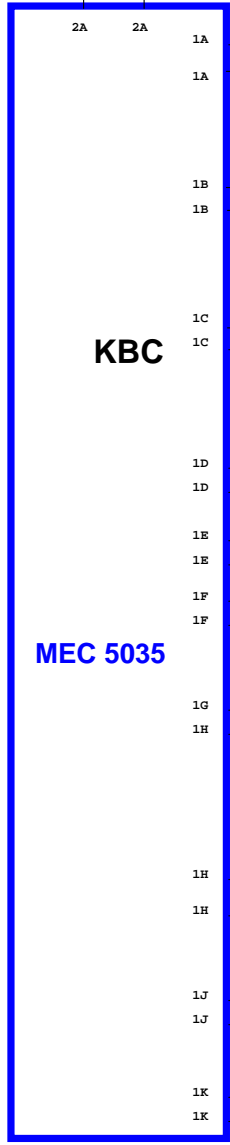
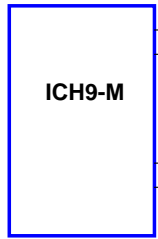
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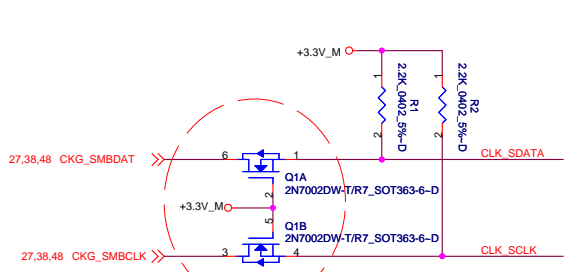


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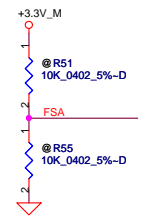
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FSC	CLKSEL2	FSB	CLKSEL1	FSA	CLKSEL0	CPU	MHz	SRC	MHz	PCI	MHz
0	0	0	0	266	100	33.3					
0	0	1	133	100	33.3						
0	1	0	200	100	33.3						
0	1	1	166	100	33.3						
1	0	0	333	100	33.3						
1	0	1	100	100	33.3						
1	1	0	400	100	33.3						



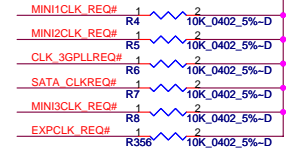
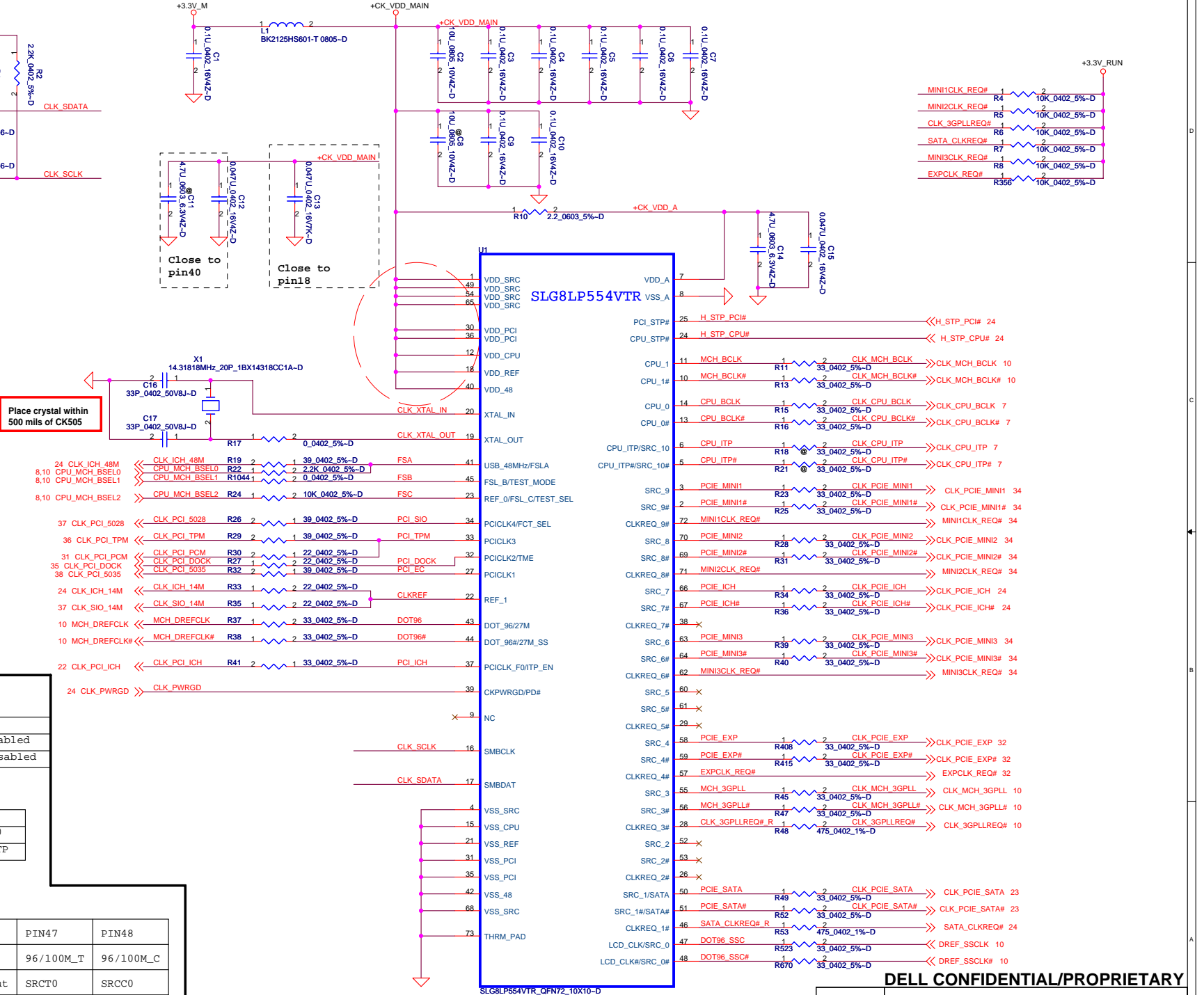
R1124 modify for G3 issues, cut in at A01

TMB	PIN 32
0	overclocking enabled
1	overclocking disabled

ITP_EN	PIN 37
0	Pin 5/6 as SRC_10
1	Pin 5/6 as CPU_ITP

FCTSEL1	PIN43	PIN44	PIN47	PIN48
0=UMA	DOT96T	DOT96C	96/100M_T	96/100M_C
1=DIS	27M_out	27M SSout	SRCT0	SRCC0

0=UMA
1=Disc. GRFX down



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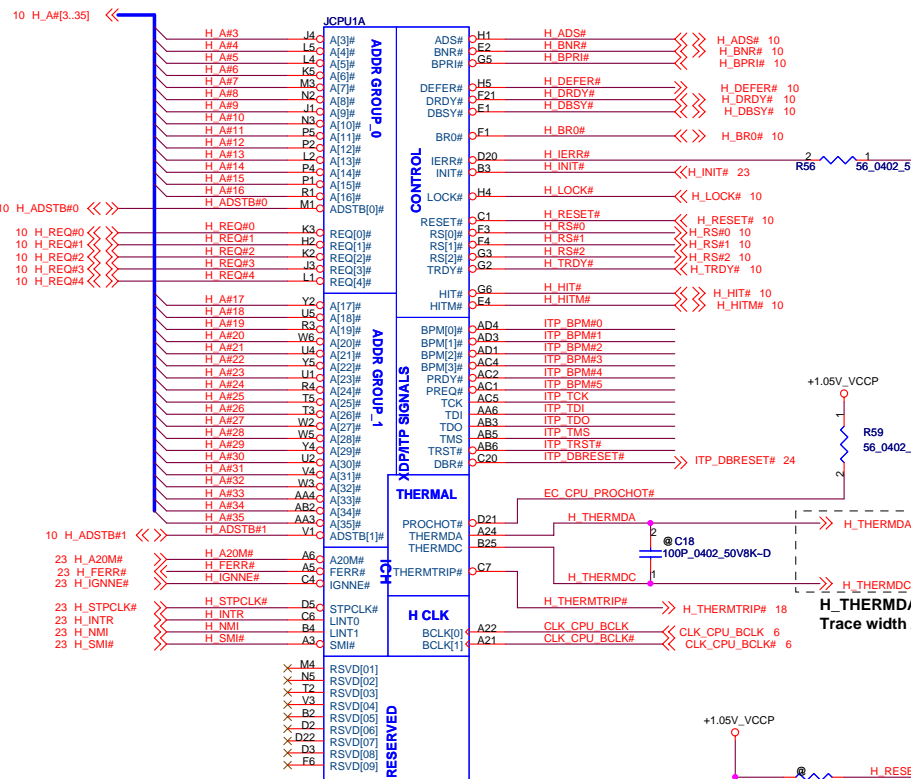
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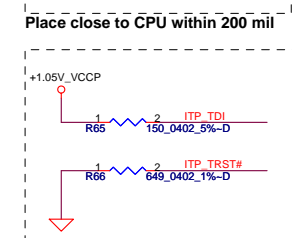
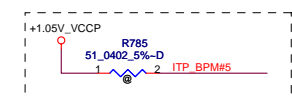
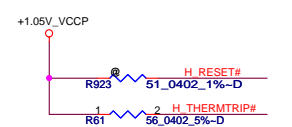
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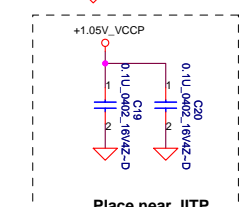


Depop R57 & R930 for Enhance ESD on dock issue

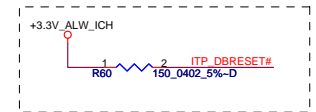
H_THERMDA, H_THERMDC routing together, Trace width / Spacing = 10 / 10 mil



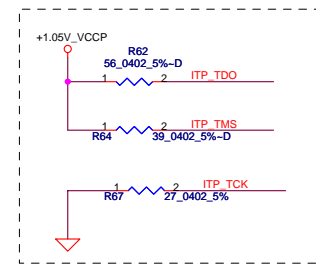
Place close to CPU within 200ps = 1000 mil



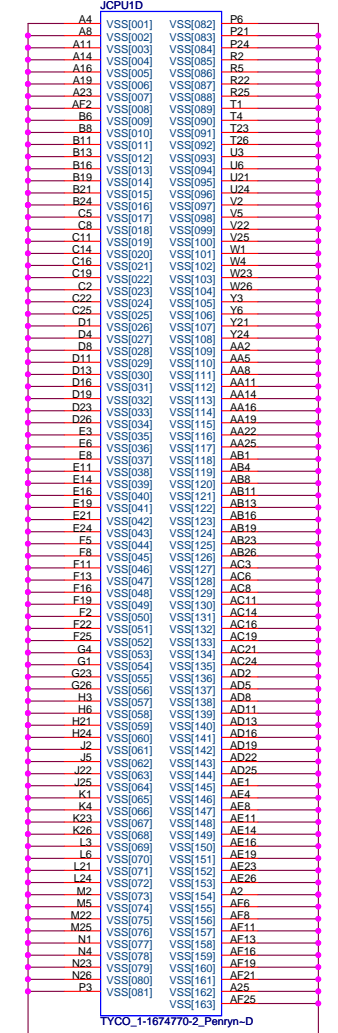
Place near JITP



Place close to JITP within 1ns = 5000 mil



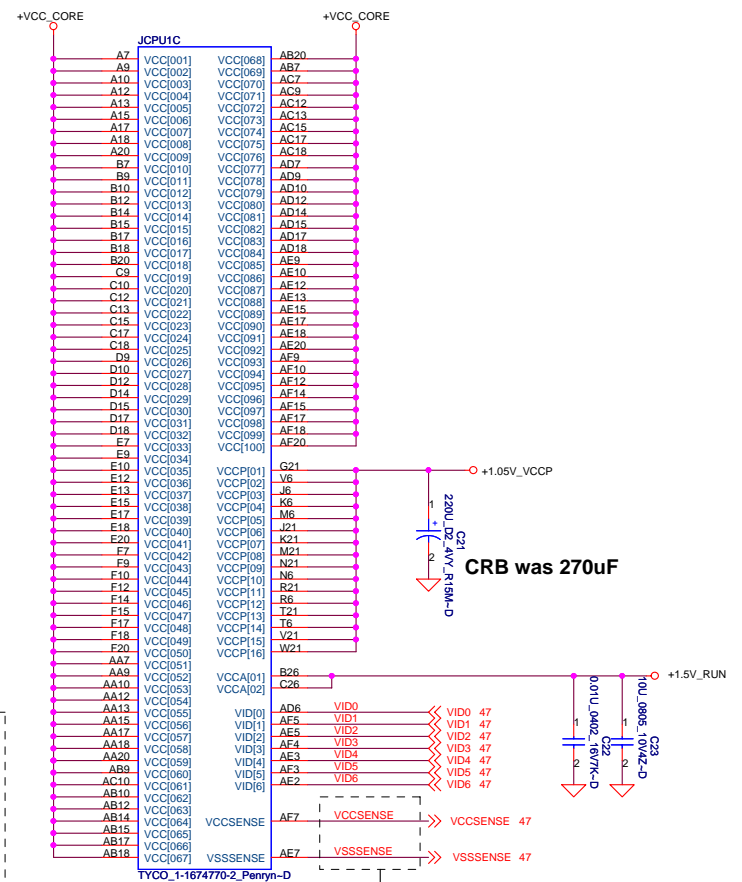
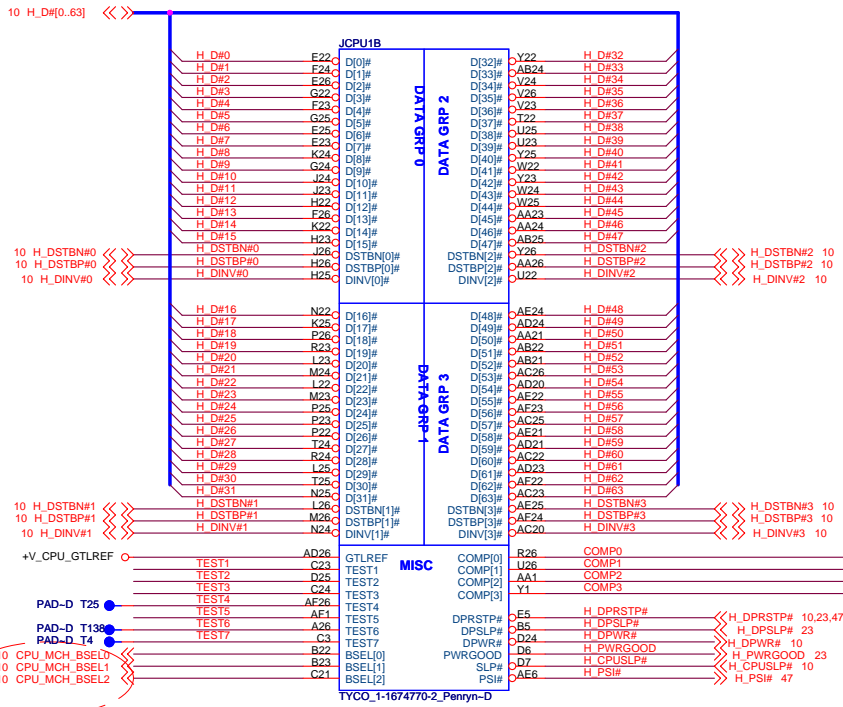
Place close to JITP within 200ps = 1000 mil



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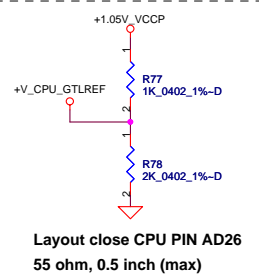
Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP0, COMP2 trace should be 27.4 ohm. COMP1, COMP3 should be 55 ohm.

Length match within 25 mils, Z0=27.4 ohm

Place R75 and R76 near CPU

Route VCCSENSE and VSSSENSE trace at 27.4 ohms, 7 mils spacing and the placement should be within 1 inch (max)

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0

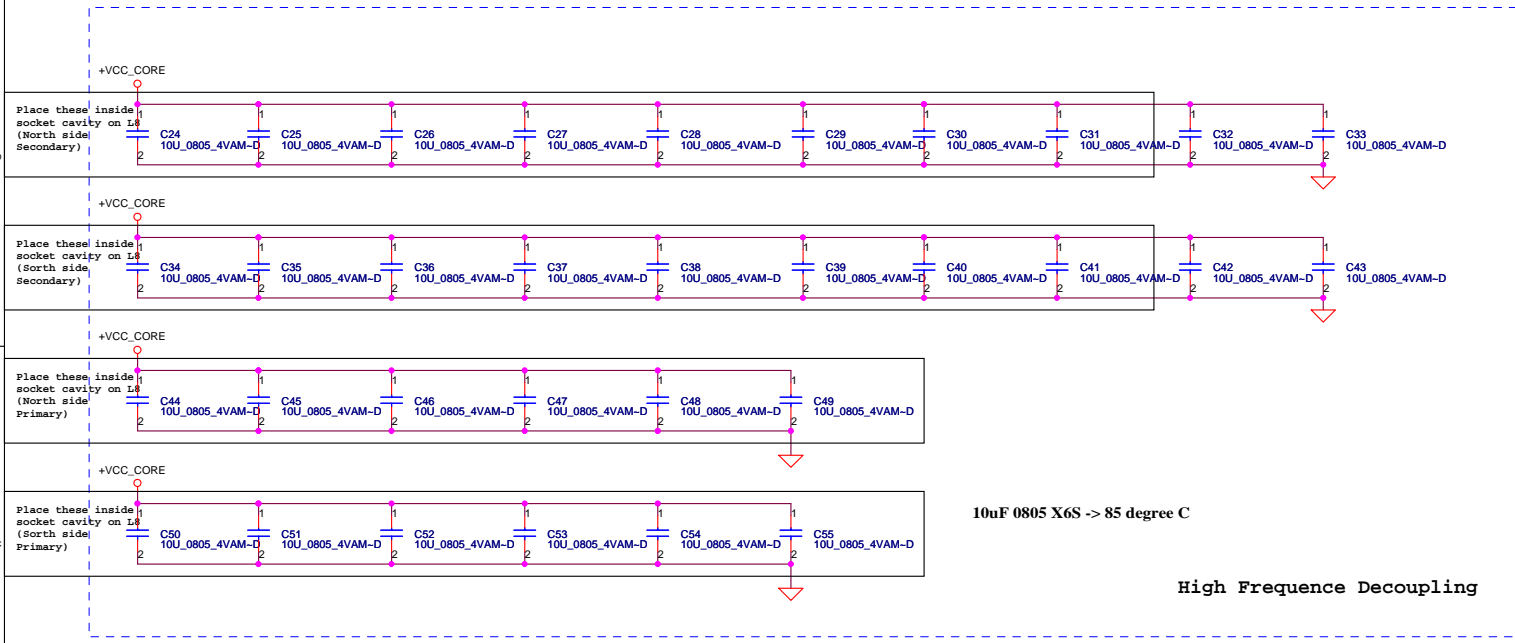


Layout close CPU PIN AD26
55 ohm, 0.5 inch (max)

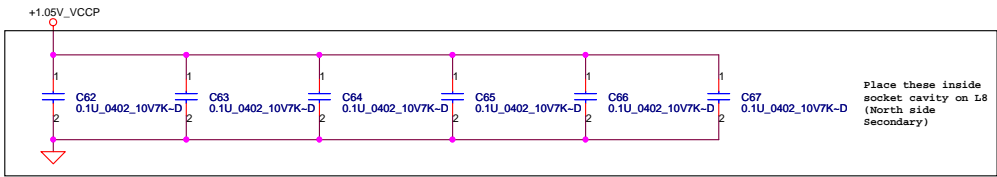
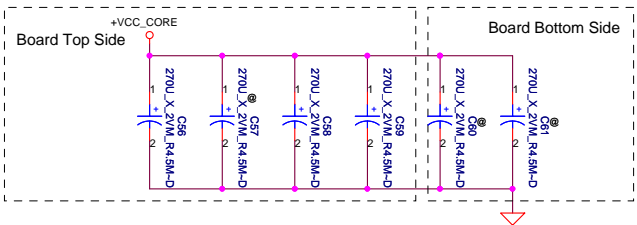
For the purpose of testability, route these signals through a ground referenced Z0 = 55ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

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Near VCORE regulator.



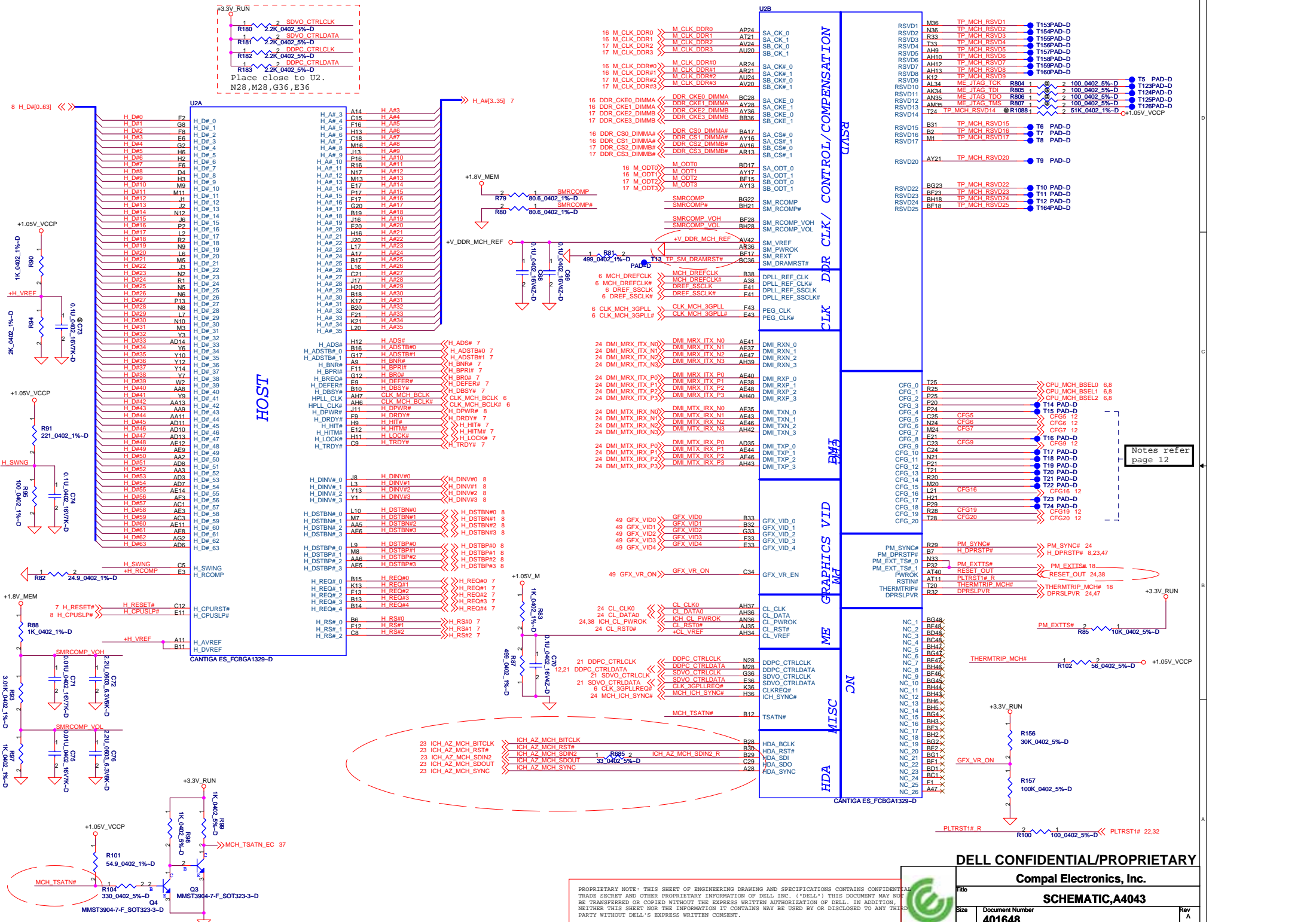
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+3.3V RUN
 R180 2.2K 0402 5%-D SDVO_CTRLCLK
 R181 2.2K 0402 5%-D SDVO_CTRLDATA
 R182 2.2K 0402 5%-D DDPC_CTRLCLK
 R183 2.2K 0402 5%-D DDPC_CTRLDATA
 Place close to U2.
 N28, M28, G36, E36

U2A

HOST

CANTIGA ES_FCBGA1329-D

+3.3V RUN

MMS13904-7-F_SOT323-3-D

16 M_CLK_DDR0 M_CLK_DDR0 AP24
 16 M_CLK_DDR1 M_CLK_DDR1 AT21
 17 M_CLK_DDR2 M_CLK_DDR2 AV24
 17 M_CLK_DDR3 M_CLK_DDR3 AU20
 16 M_CLK_DDR#0 M_CLK_DDR#0 AR24
 16 M_CLK_DDR#1 M_CLK_DDR#1 AR21
 17 M_CLK_DDR#2 M_CLK_DDR#2 AV20
 17 M_CLK_DDR#3 M_CLK_DDR#3 AU20
 16 DDR_CKE0_DIMM# M_CLK_DDR0#0 BC28
 16 DDR_CKE1_DIMM# M_CLK_DDR1#1 BC28
 17 DDR_CKE2_DIMM# M_CLK_DDR2#2 AV36
 17 DDR_CKE3_DIMM# M_CLK_DDR3#3 BC36
 16 DDR_CS0_DIMM# M_CLK_DDR#0#0 BA17
 16 DDR_CS1_DIMM# M_CLK_DDR#1#1 AV16
 17 DDR_CS2_DIMM# M_CLK_DDR#2#2 AV16
 17 DDR_CS3_DIMM# M_CLK_DDR#3#3 AR13
 16 M_ODT0 M_ODT0 B017
 16 M_ODT1 M_ODT1 AV28
 17 M_ODT2 M_ODT2 BF15
 17 M_ODT3 M_ODT3 AV13
 SMRCOMP SMRCOMP# B222
 SMRCOMP# SMRCOMP# BF21
 SMRCOMP_VOH SMRCOMP_VOH BF28
 SMRCOMP_VOL SMRCOMP_VOL BF28
 +V_DDR_MCH_REF +V_DDR_MCH_REF AV42
 SM_VREF SM_VREF AV36
 SM_PWROK SM_PWROK BF12
 SM_DRAMRST# SM_DRAMRST# BC36

U2B

CLK/DDR/CONTROL/COMPENSATION

GRAPHICS VID

ME

MISC

HDA

CANTIGA ES_FCBGA1329-D

RSV1D1 M36 TP MCH RSV1D1 T153PAD-D
 RSV1D2 A38 TP MCH RSV1D2 T154PAD-D
 RSV1D3 R33 TP MCH RSV1D3 T155PAD-D
 RSV1D4 T33 TP MCH RSV1D4 T156PAD-D
 RSV1D5 AH9 TP MCH RSV1D5 T157PAD-D
 RSV1D6 AH10 TP MCH RSV1D6 T158PAD-D
 RSV1D7 AH12 TP MCH RSV1D7 T159PAD-D
 RSV1D8 AH13 TP MCH RSV1D8 T160PAD-D
 RSV1D9 AK4 ME JTAG TCK R804 1 2 100 0402 5%-D T5 PAD-D
 RSV1D10 AK4 ME JTAG TDI R805 1 2 100 0402 5%-D T122PAD-D
 RSV1D11 AK34 ME JTAG TDI R805 1 2 100 0402 5%-D T124PAD-D
 RSV1D12 AN35 ME JTAG TMS R807 1 2 100 0402 5%-D T125PAD-D
 RSV1D13 AM05 ME JTAG TMS R807 1 2 100 0402 5%-D T126PAD-D
 RSV1D14 T24 TP MCH RSV1D14 R1088 1 2 51K 0402 1%-D T105_VCCP
 RSV1D15 B31 TP MCH RSV1D15 T6 PAD-D
 RSV1D16 B2 TP MCH RSV1D16 T6 PAD-D
 RSV1D17 M1 TP MCH RSV1D17 T8 PAD-D
 RSV1D18 AY21 TP MCH RSV1D20 T9 PAD-D
 RSV1D19 BG23 TP MCH RSV1D22 T10 PAD-D
 RSV1D20 BF23 TP MCH RSV1D23 T11 PAD-D
 RSV1D21 BH18 TP MCH RSV1D24 T12 PAD-D
 RSV1D22 BE18 TP MCH RSV1D25 T16PAD-D
 CFG0 0 T25 CPU_MCH_BSEL0 6.8
 CFG1 1 P25 CPU_MCH_BSEL1 6.8
 CFG2 2 P25 CPU_MCH_BSEL2 6.8
 CFG3 3 P20 T14 PAD-D
 CFG4 4 C25 CFG5 T15 PAD-D
 CFG5 5 N24 CFG6 CFG6 12
 CFG6 6 M24 CFG7 CFG7 12
 CFG7 7 E21 CFG8 12
 CFG8 8 C23 CFG9 T16 PAD-D
 CFG9 9 C24 T17 PAD-D
 CFG10 10 N21 T18 PAD-D
 CFG11 11 P21 T19 PAD-D
 CFG12 12 R20 T20 PAD-D
 CFG13 13 M20 T21 PAD-D
 CFG14 14 L21 CFG16 CFG16 12
 CFG15 15 L21 T22 PAD-D
 CFG16 16 L21 T23 PAD-D
 CFG17 17 P23 CFG19 12
 CFG18 18 R28 CFG19 12
 CFG19 19 T28 CFG20 CFG20 12
 R20 PM_SYNC# PM_SYNC# 24
 R37 H_DPRSTP# H_DPRSTP# 8.23,47
 N33 PM_EXTTSP# PM_EXTTSP# 18
 AT40 RESET_OUT RESET_OUT 24.38
 AT11 PLTRST# R PLTRST# R
 T20 THERMTRIP_MCH# THERMTRIP_MCH# 18
 R32 DPRSLPVR DPRSLPVR 24.47
 NC1 BC48
 NC2 BD48
 NC3 BC48
 NC4 BH47
 NC5 BG47
 NC6 BE47
 NC7 BE47
 NC8 BE46
 NC9 BG45
 NC10 BH44
 NC11 BH44
 NC12 BH45
 NC13 BH5
 NC14 BH5
 NC15 BG4
 NC16 BH4
 NC17 BF3
 NC18 BH2
 NC19 BE2
 NC20 BF1
 NC21 BG1
 NC22 BF1
 NC23 BC1
 NC24 E1
 NC25 E1
 NC26 A27

U2C

CLK/DDR/CONTROL/COMPENSATION

GRAPHICS VID

ME

MISC

HDA

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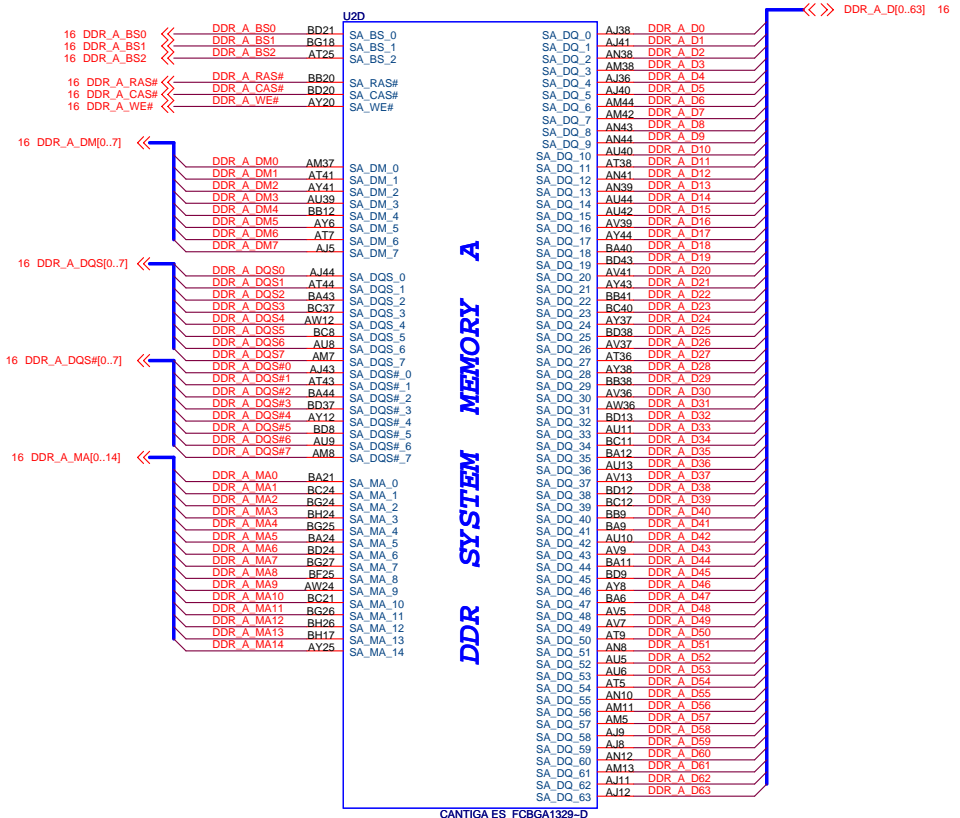
Notes refer page 12

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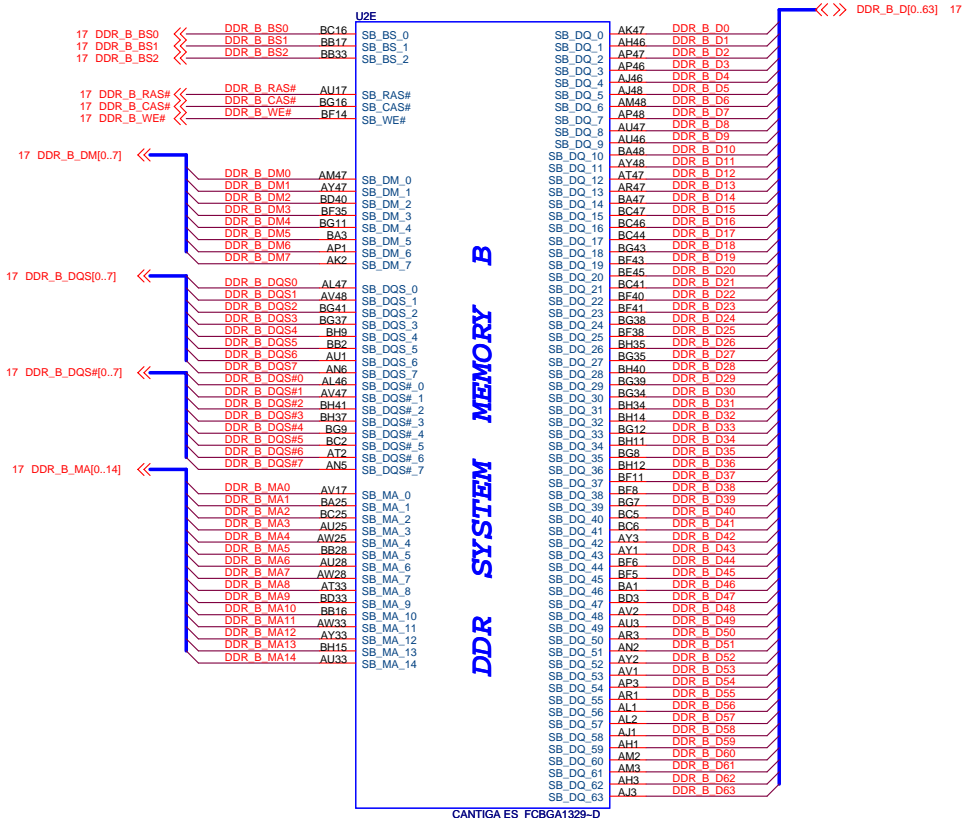
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CANTIGA ES_FCBGA1329-D



CANTIGA ES_FCBGA1329-D

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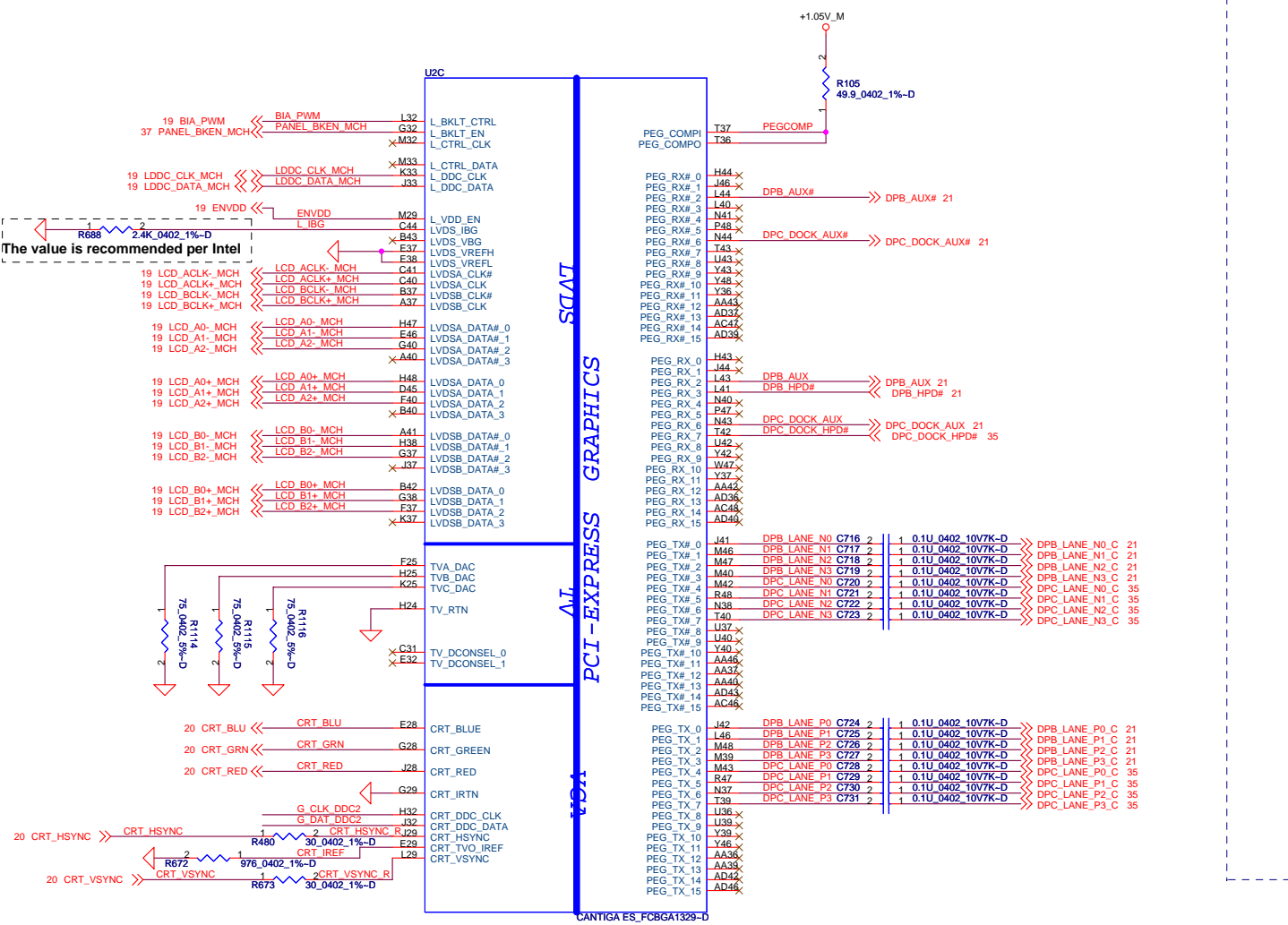
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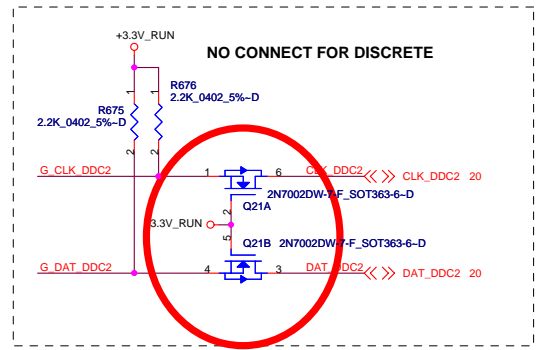
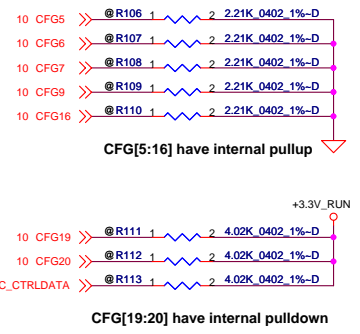
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Strap Pin Table		
CFG5	DMI X2 Select	Low = DMI x 2 High = DMI x 4 (Default)
CFG6	iTPM Host Interface	Low = iTPM enable High = iTPM disable(Default)
CFG7	Management Engine Crypto Strap	Low = TLS cipher suite with no confidentiality High = TLS cipher suite with confidentiality(Default)
CFG9	PCI Express Graphic Lane	Low = Reverse Lane High = Normal Operation(Default)
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable(default)
CFG19	DMI Lane Reversal	Low=Normal (default) High=Lane Reversed
CFG20	SDVO/PCIE Concurrent Operation	Low=Only SDVO or PCIe1 is operational (default) High=SDVO and PCIe1 are operating simultaneously via PEG port
SDVO_CTRL_DATA		Low=No SDVO Device Present (default) High=SDVO Device Present
DDPC_CTRLDATA		Low=DisplayPort disabled (default) High=DisplayPort device present



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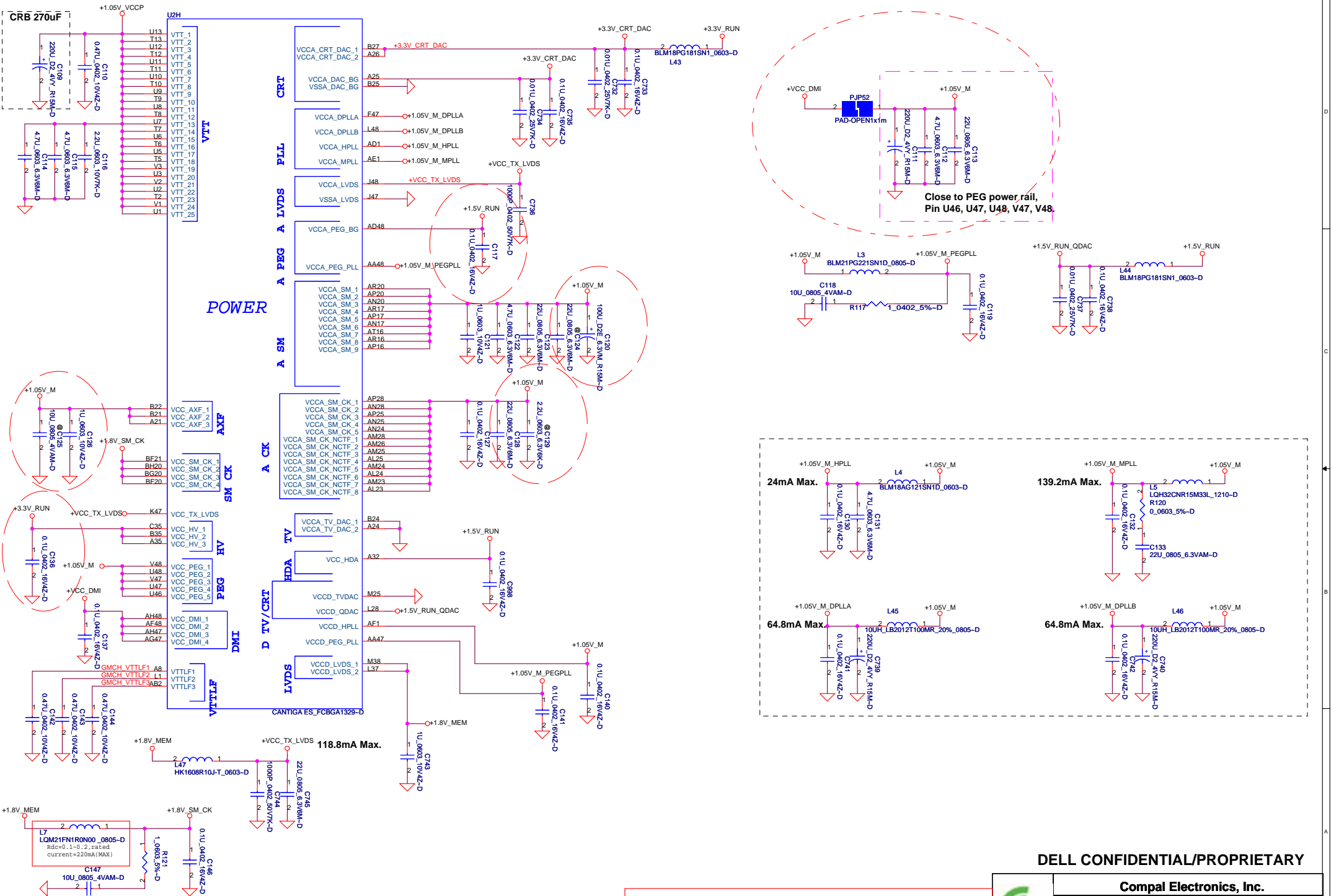
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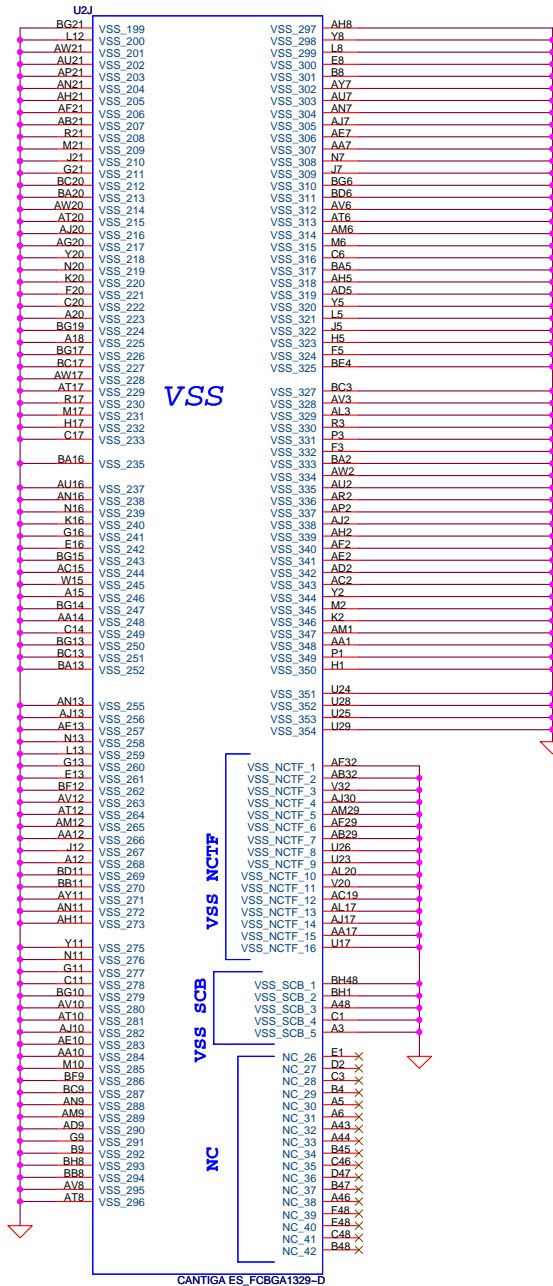
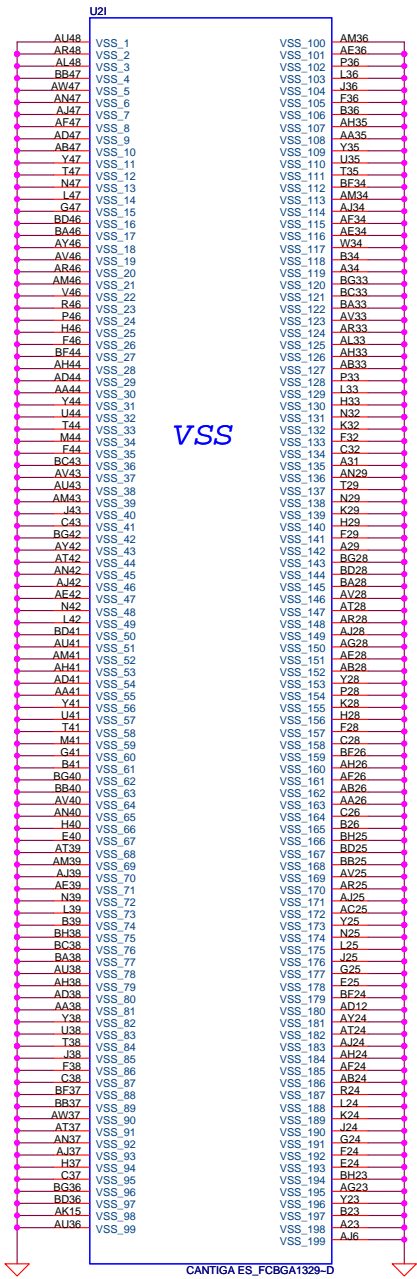
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Size	Document Number	Rev
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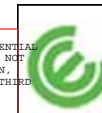


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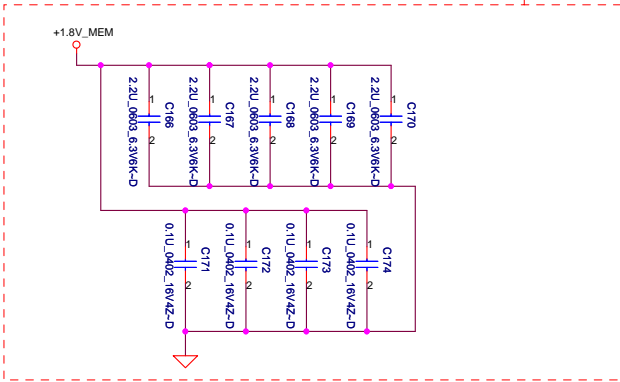
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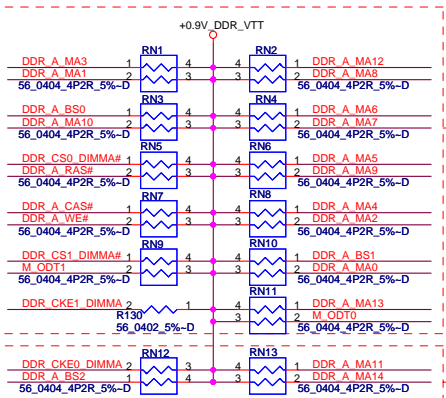
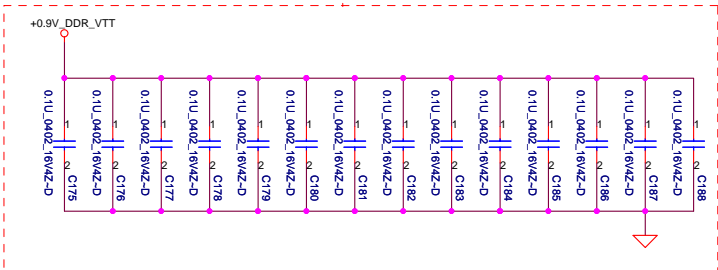


- 11 DDR_A_DQS#[0..7] <<>>
- 11 DDR_A_D[0..63] <<>>
- 11 DDR_A_DM[0..7] <<>>
- 11 DDR_A_DQS[0..7] <<>>
- 11 DDR_A_MA[0..14] <<>>

Layout Note:
Place near JDIMMA

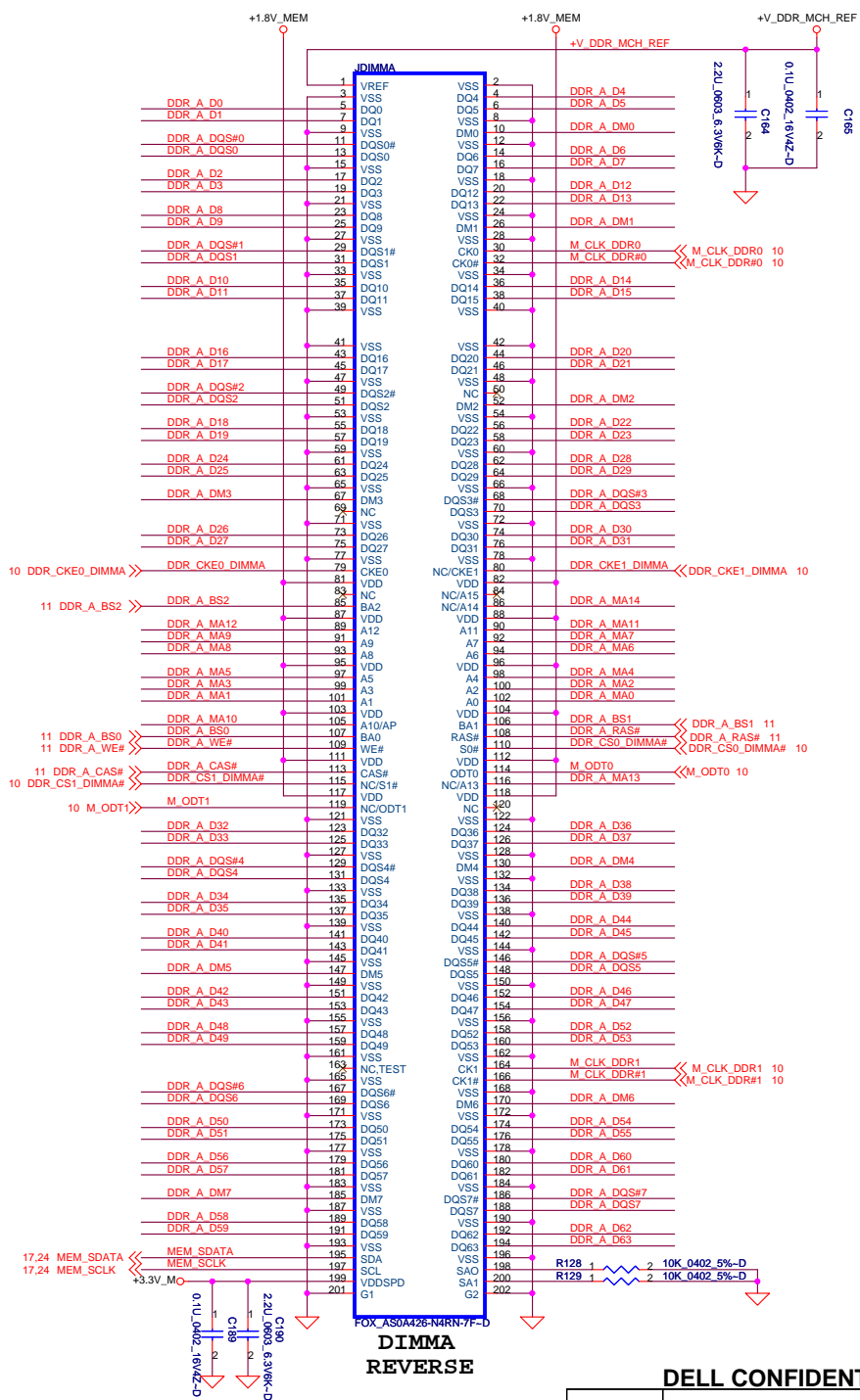


Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V_DDR_VTT



Layout Note:
Place these resistor closely JDIMMA, all trace length < 750 mil

Layout Note:
Place these resistor closely JDIMMA, all trace length Max=1.3"



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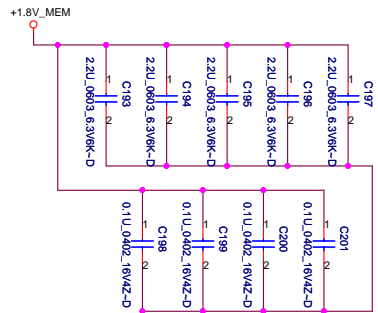
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Size: Document Number **401648** Rev A

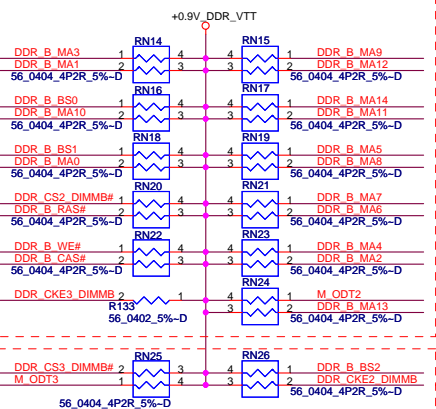
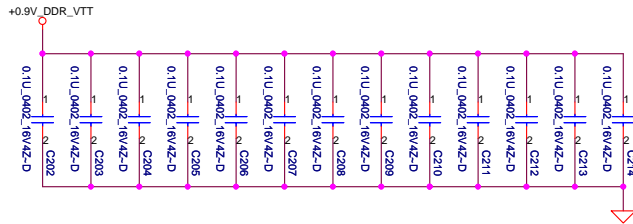
Date: Tuesday, October 28, 2008 Sheet 16 of 53



Layout Note:
Place near JDIMMB

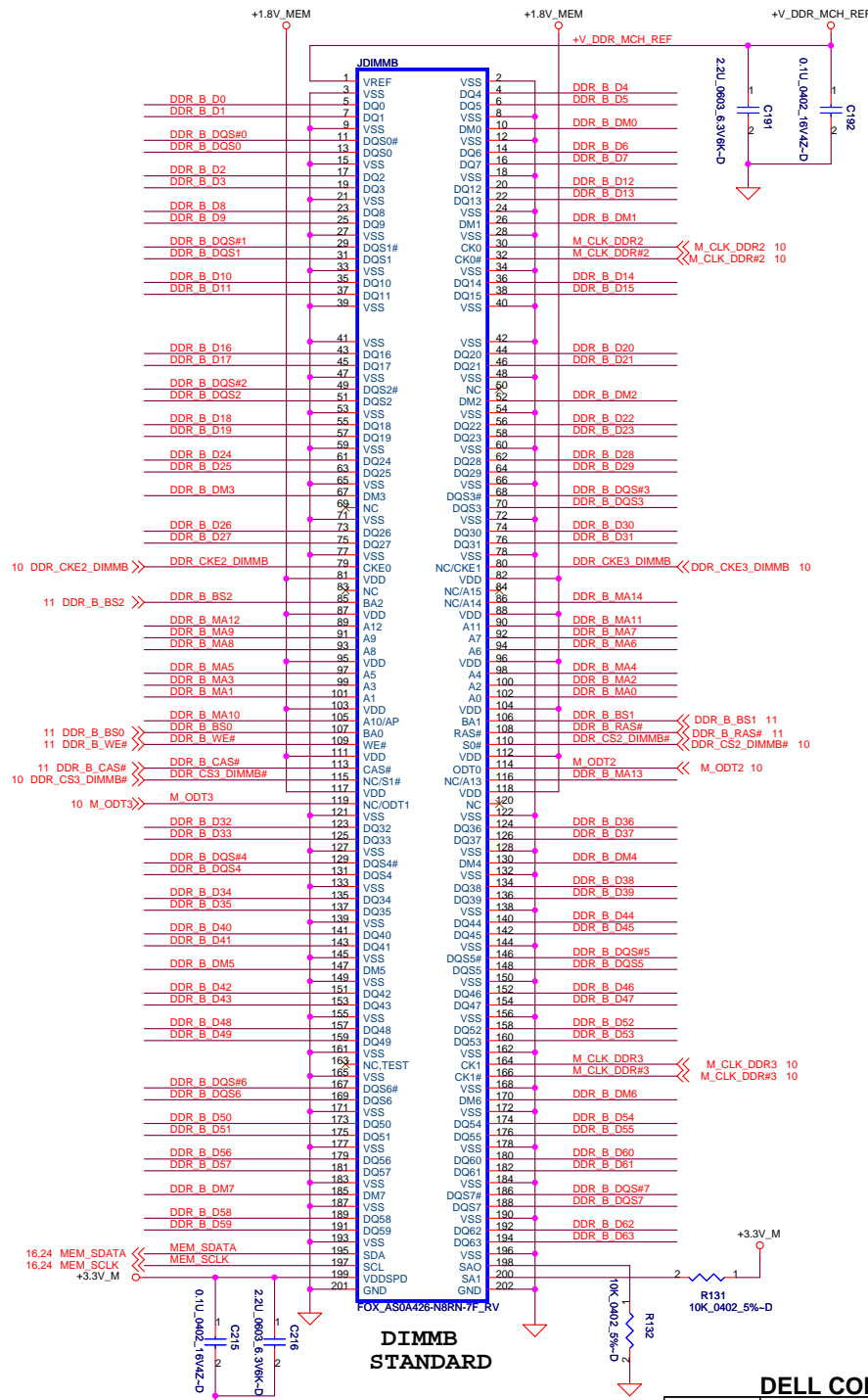


Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V_DDR_VTT



Layout Note:
Place these resistor closely JDIMMB, all trace length < 750 mil

Layout Note:
Place these resistor closely JDIMMB, all trace length Max=1.3"



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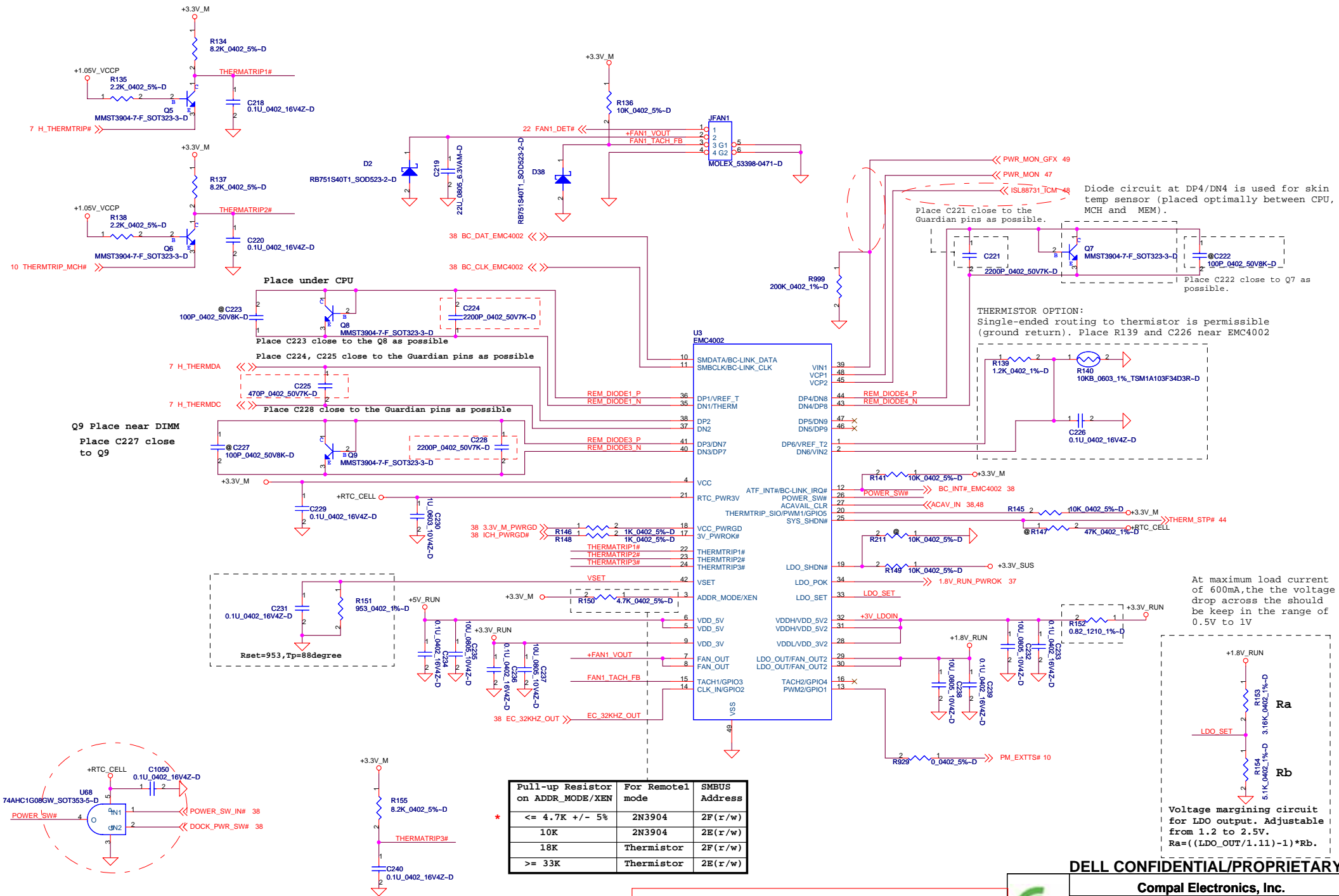
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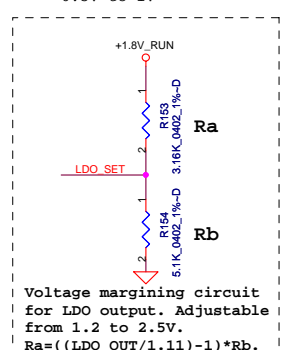


Diode circuit at DP4/DN4 is used for skin temp sensor (placed optimally between CPU, MCH and MEM).
Place C221 close to the Guardian pins as possible.
Place C222 close to Q7 as possible.

THERMISTOR OPTION:
Single-ended routing to thermistor is permissible (ground return). Place R139 and C226 near EMC4002

At maximum load current of 600mA, the the voltage drop across the should be keep in the range of 0.5V to 1V

Pull-up Resistor on ADDR_MODE/XEN	For Remotel mode	SMBUS Address
<= 4.7K +/- 5%	2N3904	2F(r/w)
10K	2N3904	2E(r/w)
18K	Thermistor	2F(r/w)
>= 33K	Thermistor	2E(r/w)



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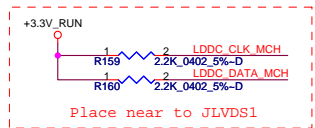
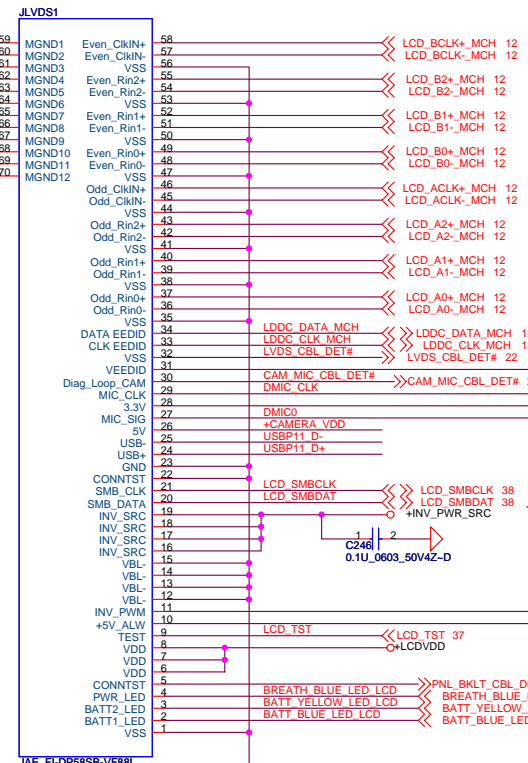
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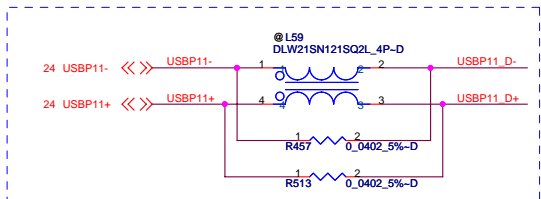
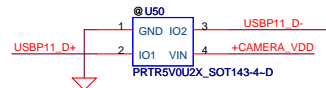
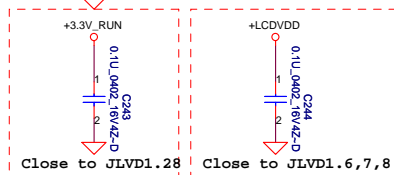
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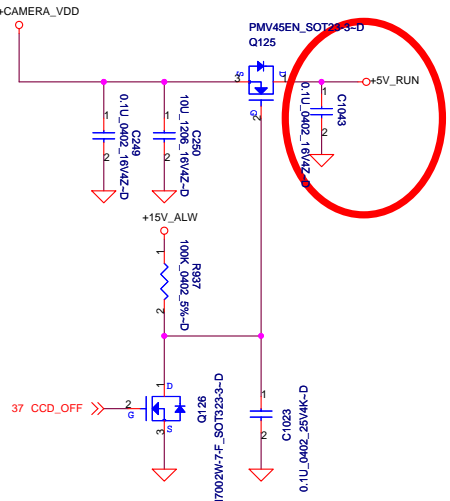
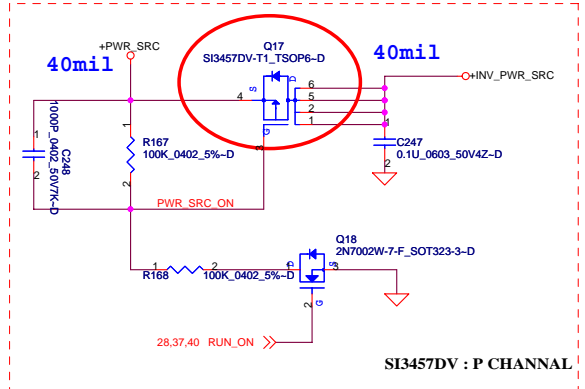
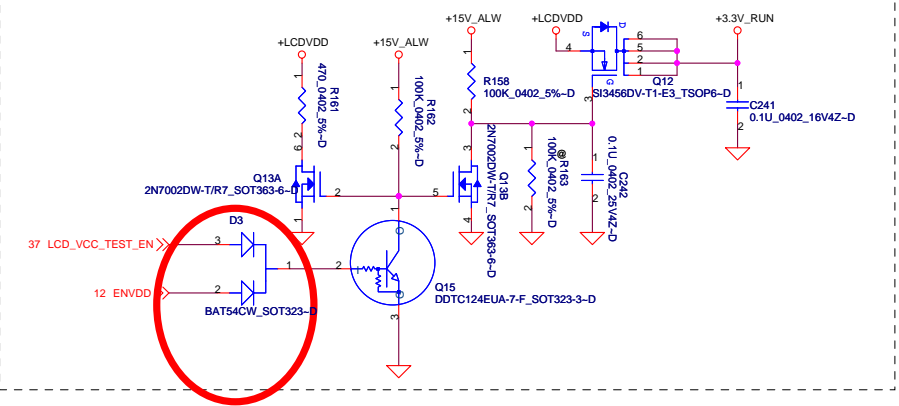
@ LVDS CABLE

Part Number	Description
DA30000341L	PCB 03P LA-4051P REV0 M/B

Pin28 3.3VRUN is for Mic PWR



LCD Power

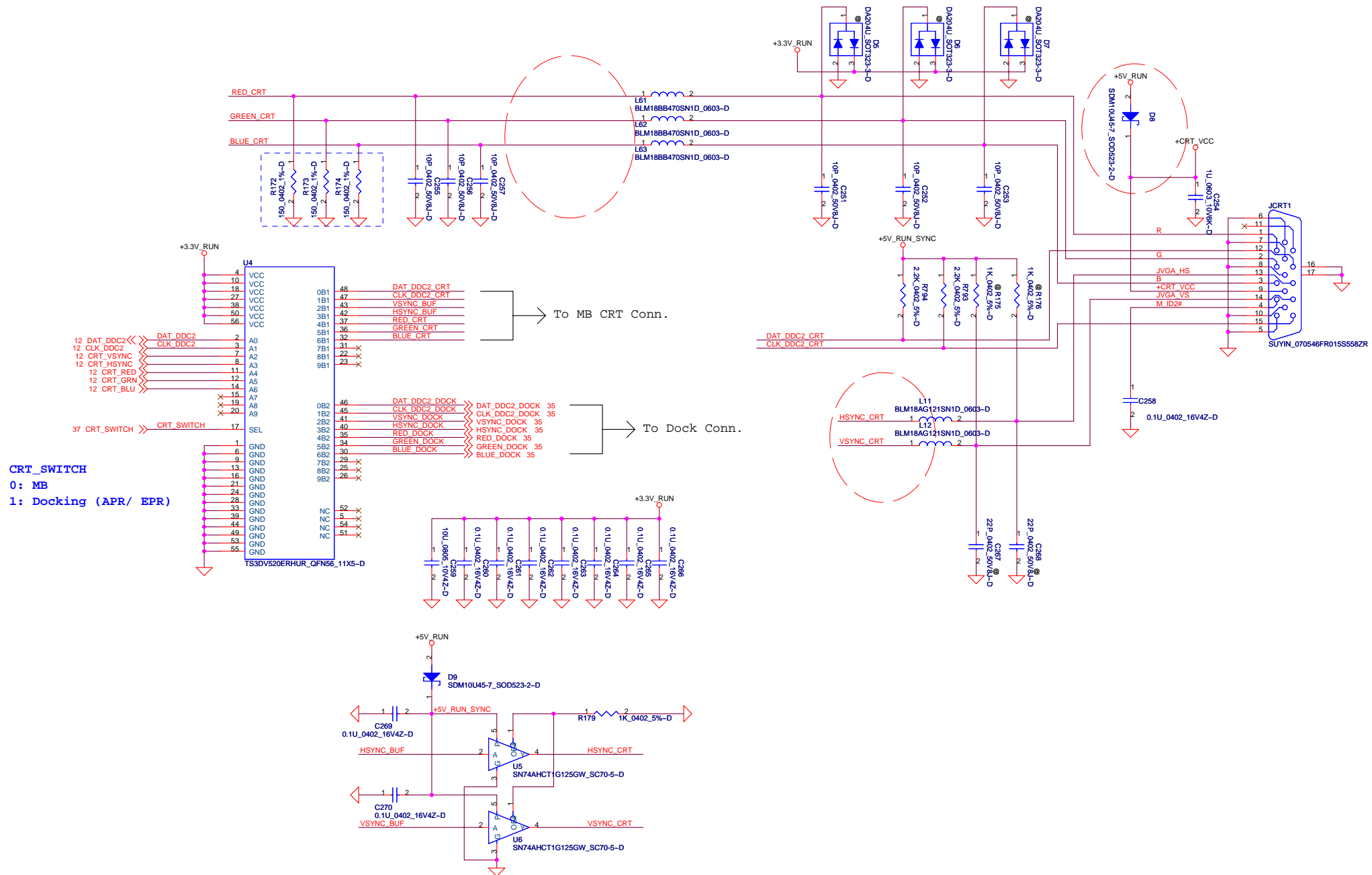


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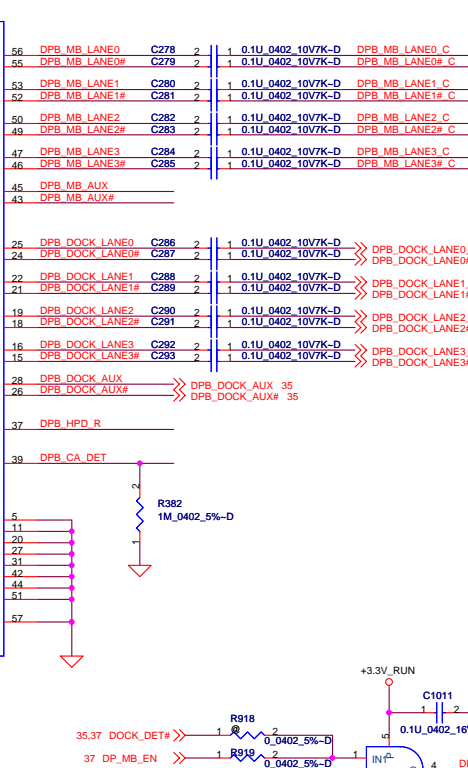
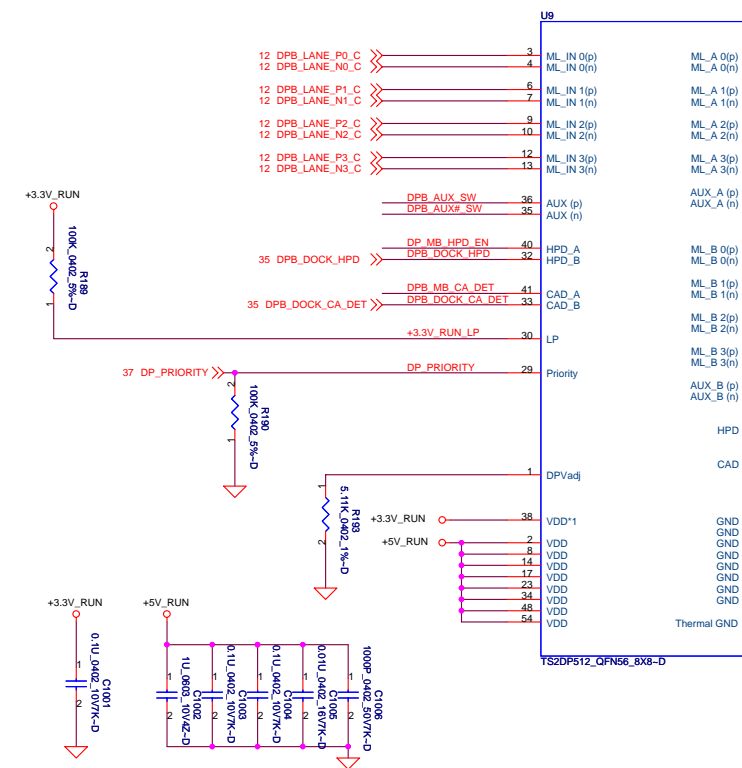
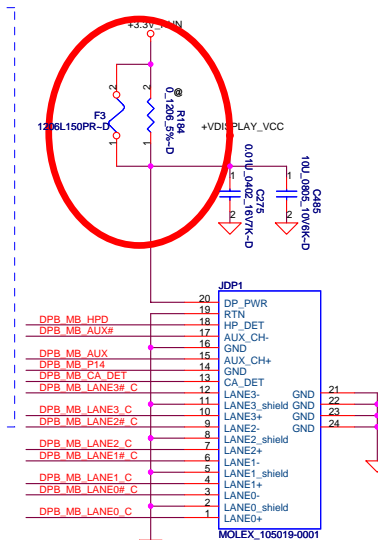
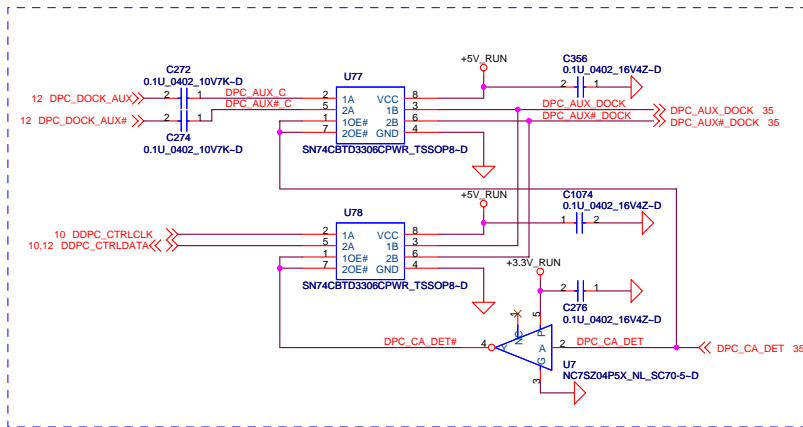
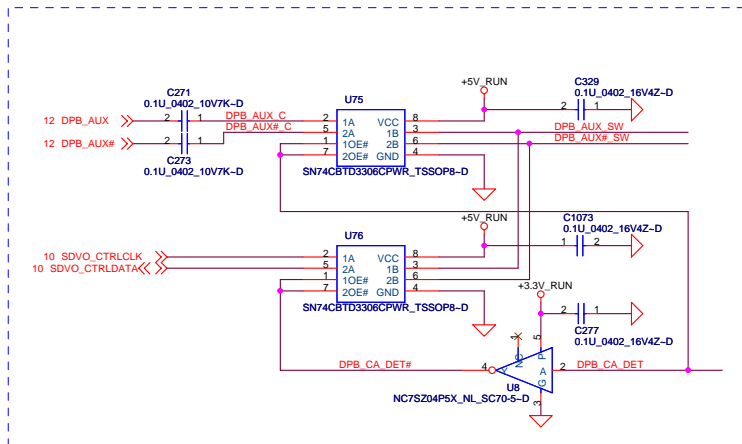
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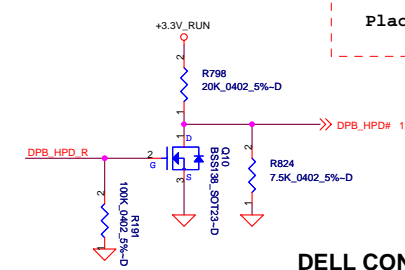
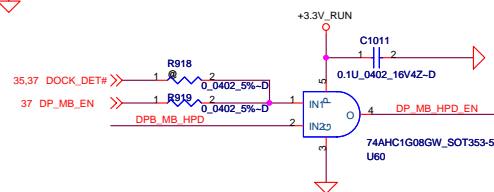
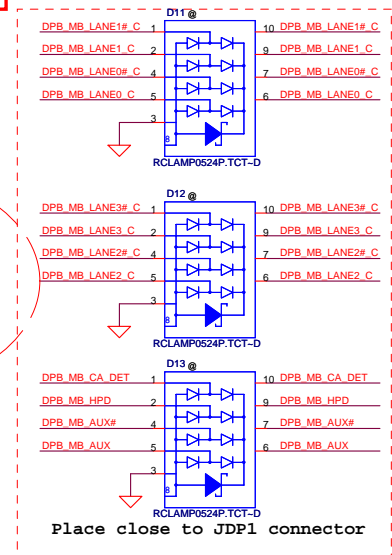
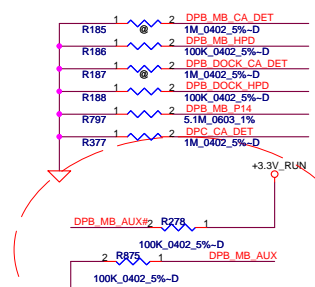
SW for MB side

SW for eDOCK side

Display port Connector



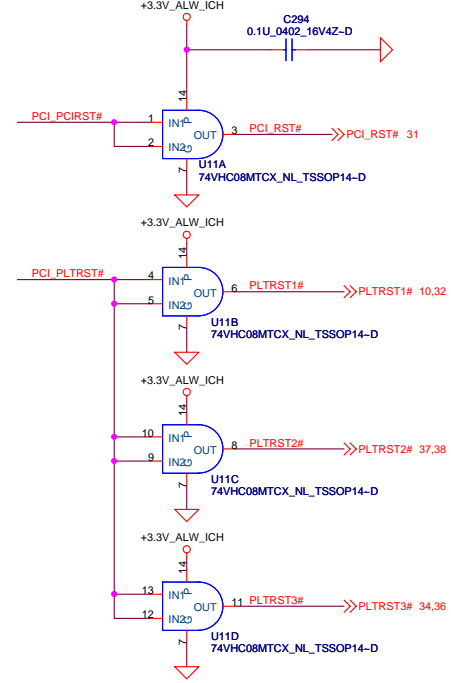
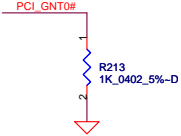
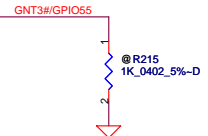
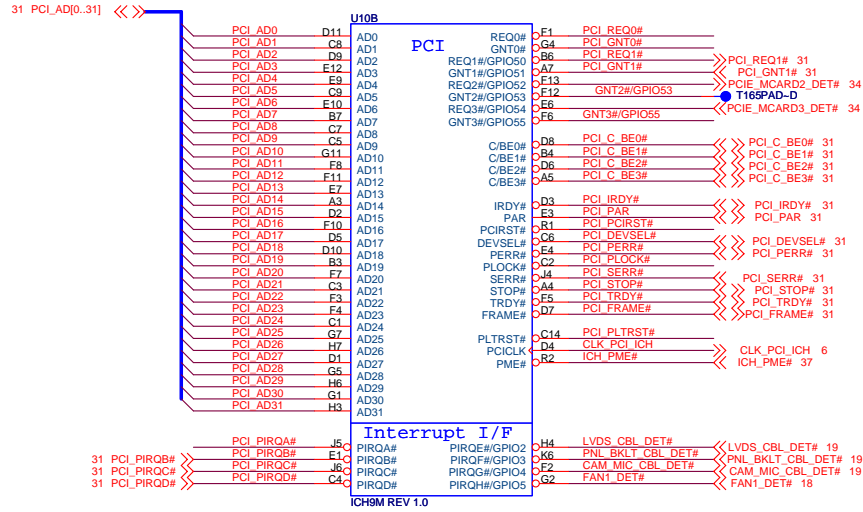
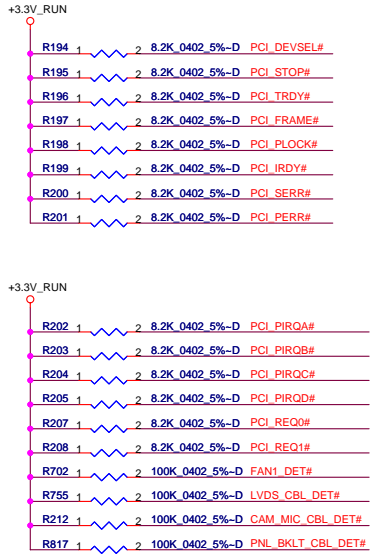
C884
0.033U_0402_16V4Z-D
DPB_DOCK_HPDP
Close to R188
Its for Enhance ESD on dock issue.



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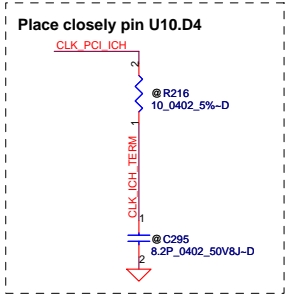


A16 away override strap.

GNT3#/GPIO55	Low = A16 swap override enabled. High = Default.
--------------	---

Boot BIOS Strap

PCI_GNT0#	SPI_CS1#	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC



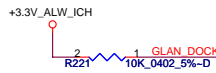
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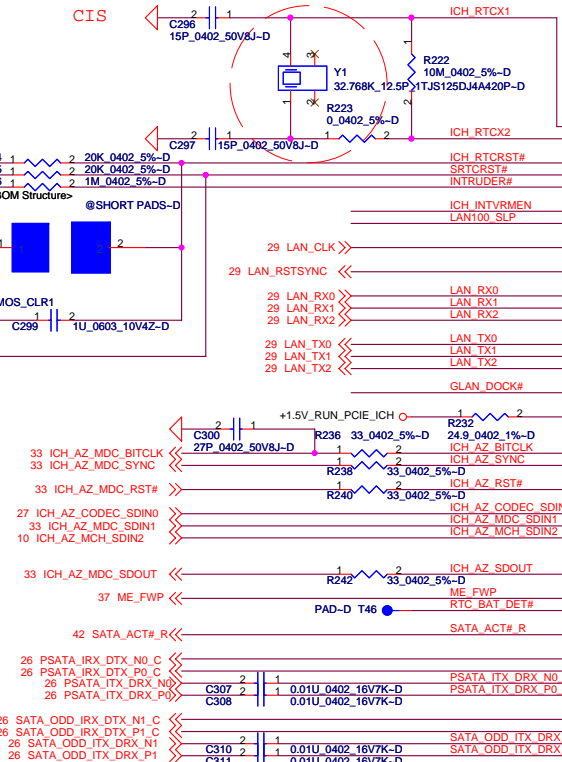
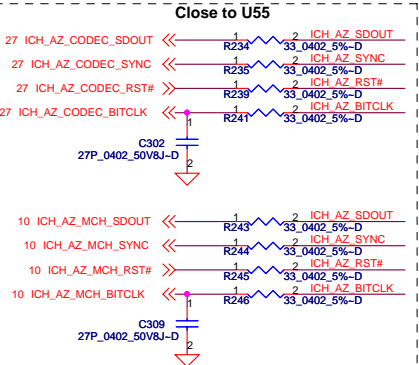
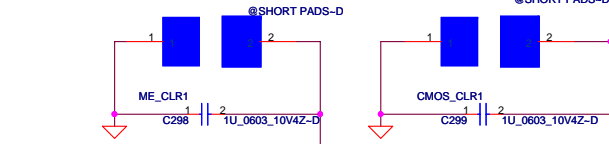
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Package
9.6X4.06 mm

CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

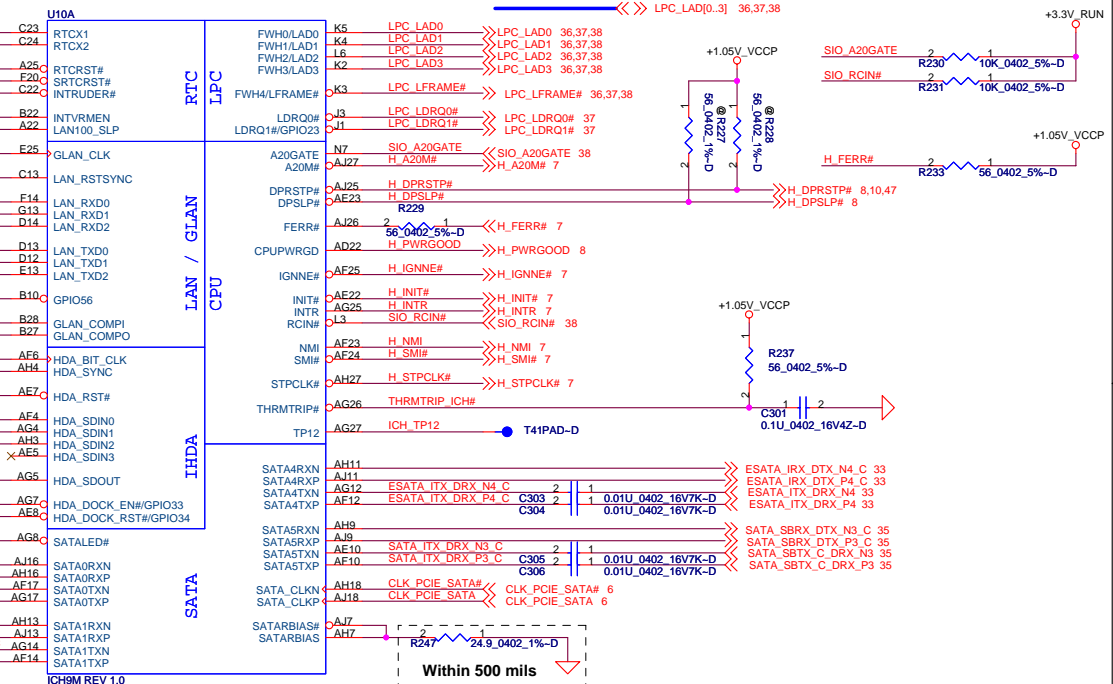


ICH9M Internal VR Enable Strap
(Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)

ICH_INTRVSMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)
---------------	---

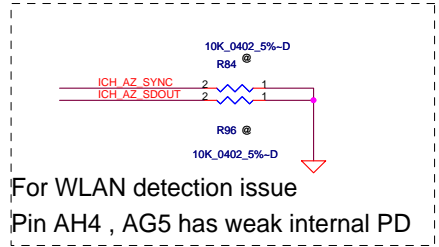
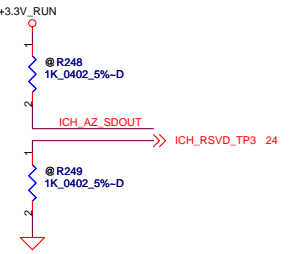
ICH9M LAN100 SLP Strap
(Internal VR for VccLAN1.05 and VccCL1.05)

ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)
----------------	---



XOR Chain Entrance Strap

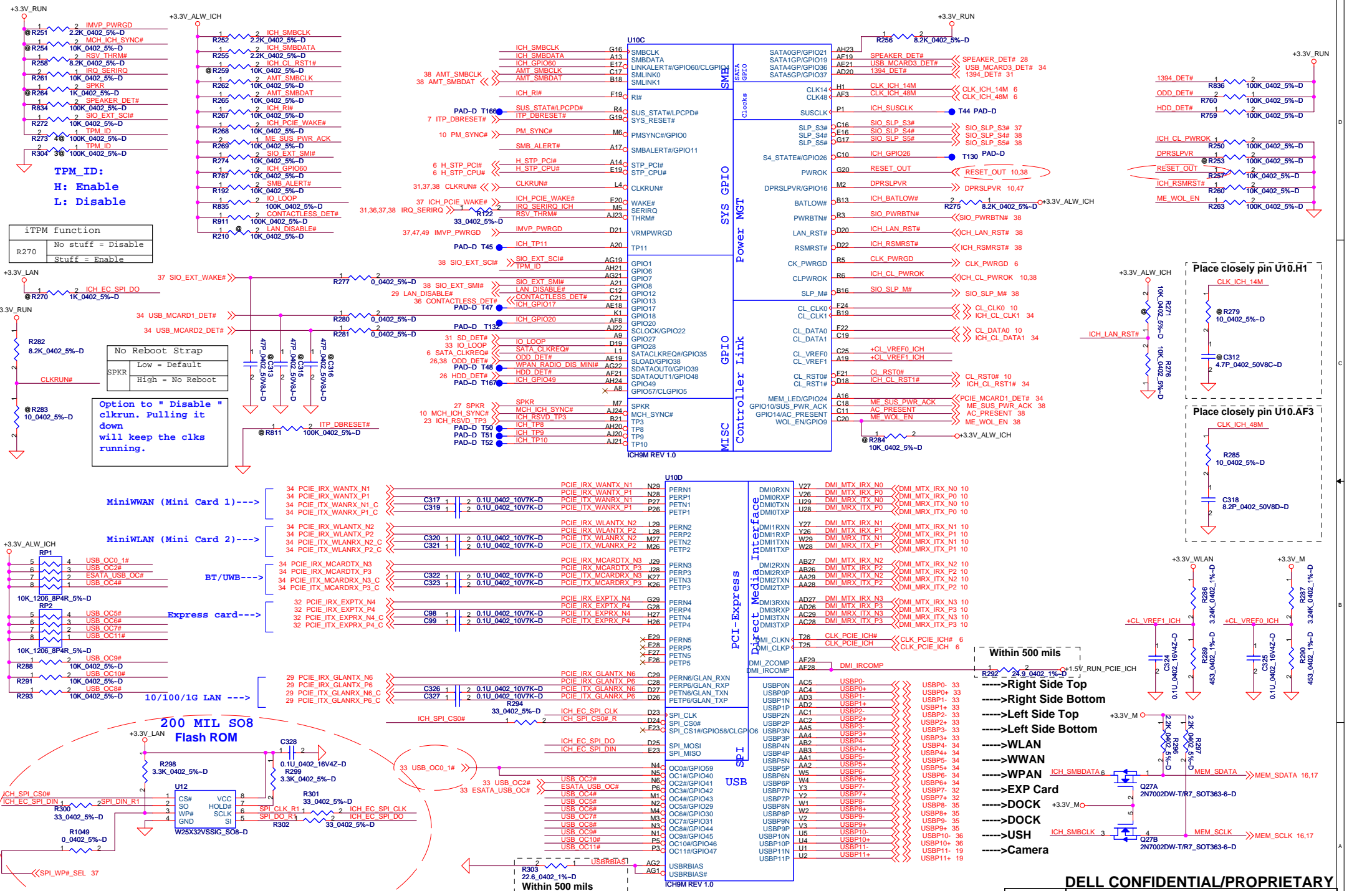
ICH_RSVD_TP3	HDA SDOOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1



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TPM ID:
H: Enable
L: Disable

iTPM function	
R270	No stuff = Disable
	Stuff = Enable

No Reboot Strap
Low = Default
High = No Reboot

Option to "Disable" clkrun. Pulling it down will keep the clks running.

MiniWWAN (Mini Card 1)---->

MiniWLAN (Mini Card 2)---->

BT/UWB---->

Express card---->

10/100/1G LAN ---->

200 MIL SOB Flash ROM

U12
R298 3.3K_0402_5%-D
R299 0.1U_0402_16V4Z-D
R301 33_0402_5%-D
R302 33_0402_5%-D
R300 33_0402_5%-D
R1049 0.0402_5%-D
W25X32V55IG_S08-D

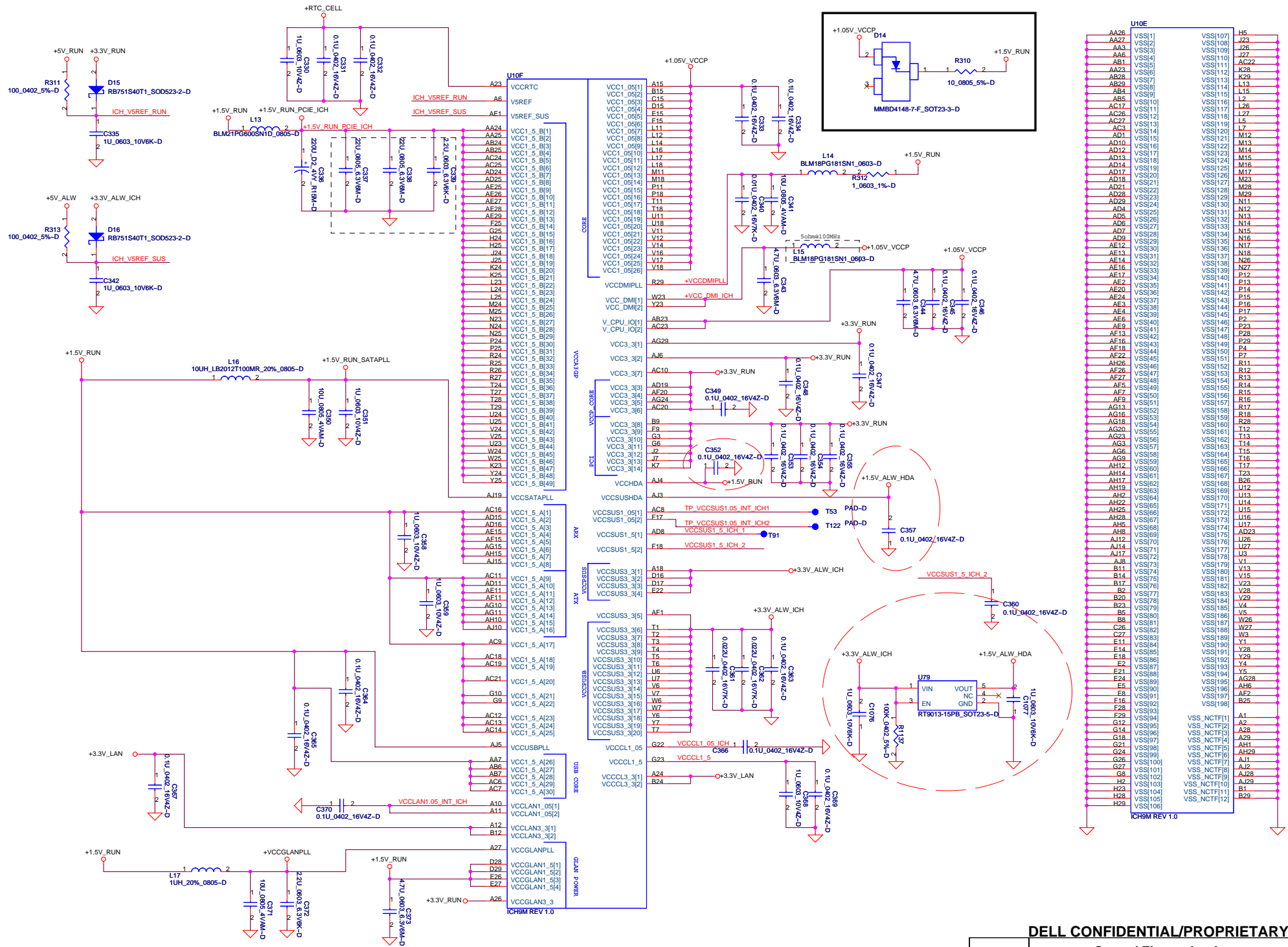
- Within 500 mils
- Right Side Top
- Right Side Bottom
- Left Side Top
- Left Side Bottom
- WLAN
- WWAN
- WPAN
- EXP Card
- DOCK
- DOCK
- USH
- Camera

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SCHMATIC,A4043

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Size: _____ Document Number: **401648**
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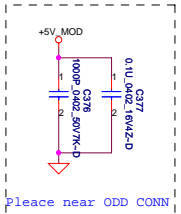


U10E		
AA26	VSS[1]	H5
AA27	VSS[2]	J23
AA3	VSS[3]	J26
AA6	VSS[10]	L2
AB1	VSS[11]	AC22
AA23	VSS[5]	K28
AB28	VSS[7]	VSS[13]
AB29	VSS[8]	K29
AB4	VSS[9]	VSS[14]
AB5	VSS[10]	VSS[15]
AC17	VSS[11]	L26
AC26	VSS[12]	L27
AC27	VSS[12]	VSS[18]
AC3	VSS[13]	VSS[19]
AD1	VSS[14]	M12
AD10	VSS[15]	VSS[21]
AD12	VSS[16]	M13
AD13	VSS[17]	M14
AD14	VSS[18]	M15
AD17	VSS[19]	M16
AD18	VSS[20]	M17
AD21	VSS[21]	M23
AD22	VSS[22]	M28
AD26	VSS[23]	M29
AD29	VSS[24]	VSS[30]
AD4	VSS[25]	N11
AD6	VSS[26]	N12
AD7	VSS[27]	N13
AD9	VSS[28]	N14
AE12	VSS[29]	N15
AE13	VSS[30]	N17
AE14	VSS[32]	N26
AE16	VSS[33]	N27
AE17	VSS[33]	P12
AE2	VSS[35]	P13
AE20	VSS[36]	P14
AE24	VSS[36]	P15
AE3	VSS[37]	P16
AE4	VSS[38]	P17
AE6	VSS[39]	P2
AE9	VSS[40]	P23
AE13	VSS[41]	P28
AE16	VSS[43]	P4
AE18	VSS[44]	R1
AE22	VSS[45]	R11
AH26	VSS[46]	R12
AH27	VSS[47]	R13
AH28	VSS[48]	R14
AH3	VSS[49]	R15
AH7	VSS[50]	R16
AH9	VSS[51]	R17
AG13	VSS[52]	R18
AG16	VSS[53]	R19
AG18	VSS[54]	R2
AG20	VSS[54]	T12
AG23	VSS[55]	T13
AG3	VSS[56]	T14
AG6	VSS[57]	T15
AG9	VSS[58]	T16
AG10	VSS[59]	T17
AH12	VSS[60]	T2
AH14	VSS[61]	T23
AH17	VSS[62]	B26
AH19	VSS[63]	L12
AH2	VSS[64]	L13
AH22	VSS[65]	L14
AH25	VSS[65]	L15
AH28	VSS[67]	L16
AH5	VSS[69]	L17
AH8	VSS[68]	AD23
AH12	VSS[70]	J26
AH17	VSS[71]	U3
AH18	VSS[72]	V1
AH19	VSS[73]	V19
B11	VSS[74]	V13
B14	VSS[75]	V15
B17	VSS[75]	V23
B18	VSS[76]	V29
B2	VSS[77]	V28
B20	VSS[78]	V4
B23	VSS[78]	V29
B5	VSS[80]	V5
B8	VSS[81]	V26
C26	VSS[82]	W27
C27	VSS[82]	W3
E14	VSS[83]	Y28
E11	VSS[84]	Y1
E18	VSS[85]	Y2
E2	VSS[86]	Y4
E21	VSS[88]	Y28
E24	VSS[89]	AG28
E5	VSS[89]	AH6
E8	VSS[90]	AF2
F16	VSS[91]	AH2
F28	VSS[92]	VSS[198]
F29	VSS[94]	VSS_NCTF[1]
G12	VSS[95]	VSS_NCTF[2]
G14	VSS[96]	VSS_NCTF[3]
G18	VSS[97]	VSS_NCTF[4]
G21	VSS[98]	VSS_NCTF[5]
G24	VSS[99]	VSS_NCTF[6]
G26	VSS[99]	VSS_NCTF[8]
G27	VSS[101]	VSS_NCTF[7]
G8	VSS[102]	VSS_NCTF[9]
H2	VSS[103]	VSS_NCTF[10]
H23	VSS[104]	VSS_NCTF[11]
H28	VSS[105]	VSS_NCTF[12]
H29	VSS[106]	VSS[106]

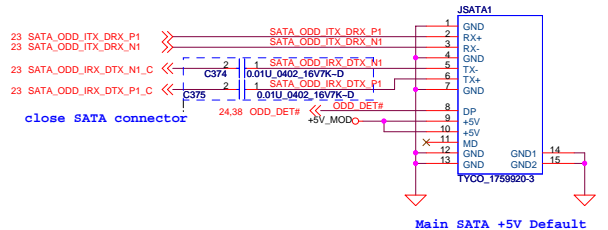
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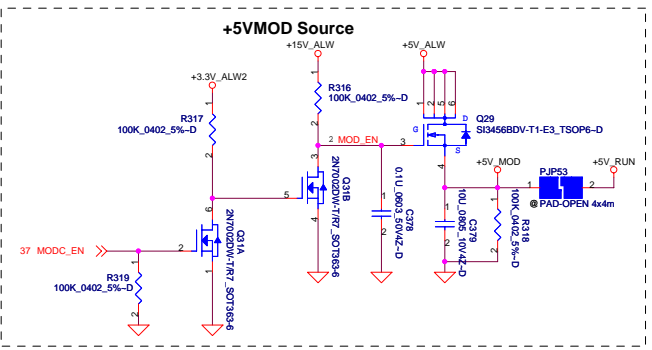
Title		SCHEMATIC_A4043	
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Date:	Tuesday, October 28, 2008	Sheet	25 of 53



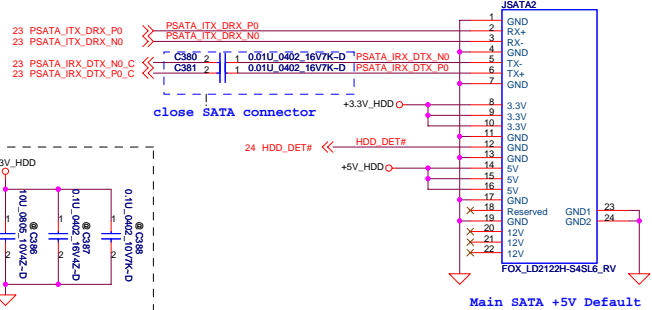
For ODD



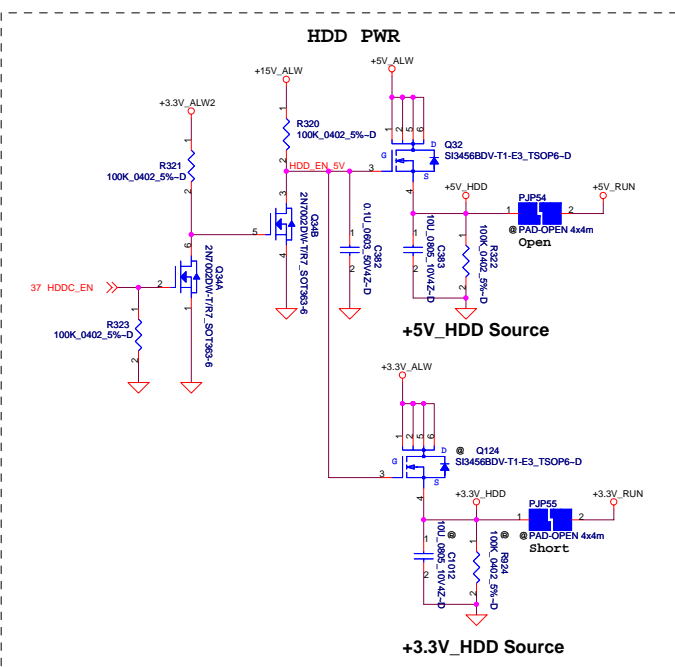
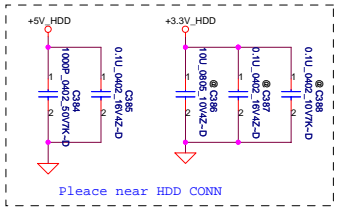
Main SATA +5V Default



For HDD



Main SATA +5V Default

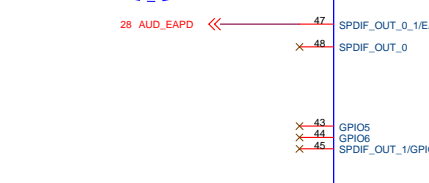
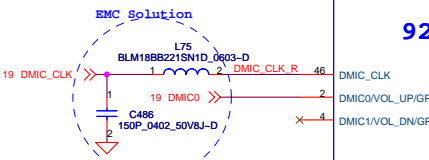
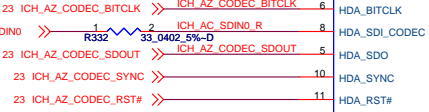
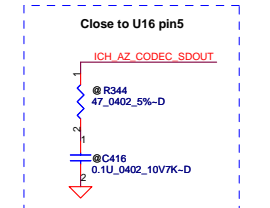
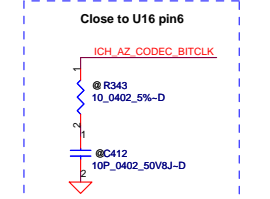
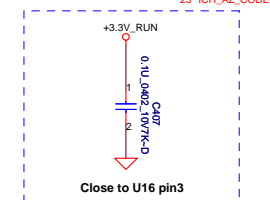
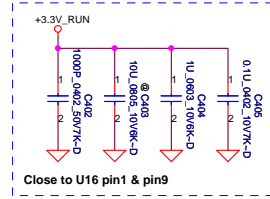
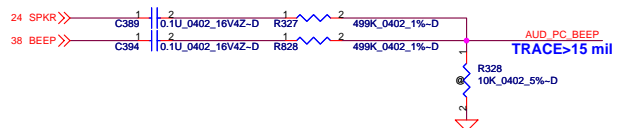


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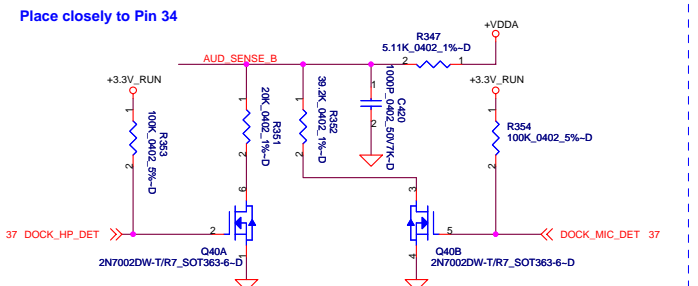
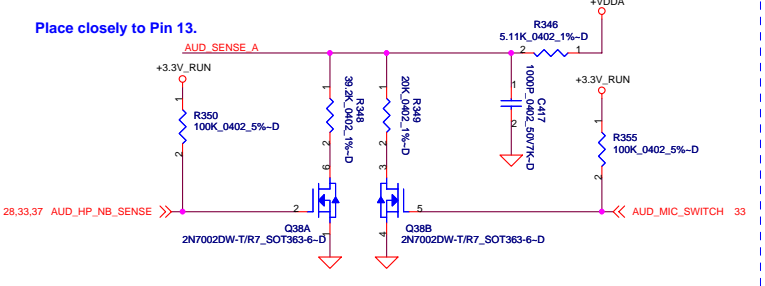
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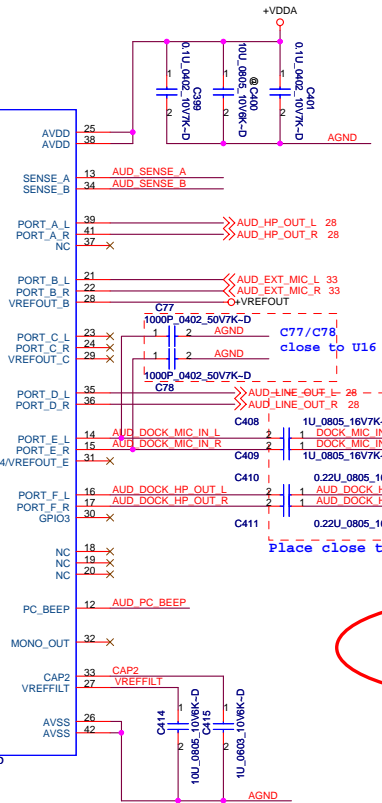
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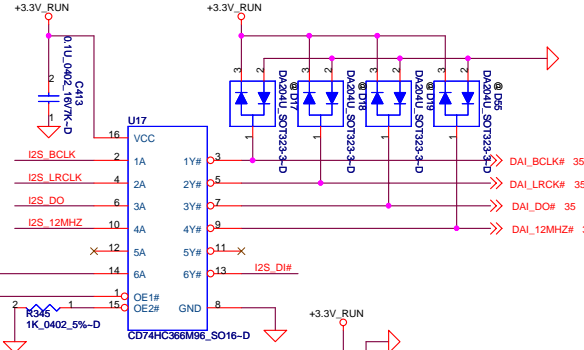
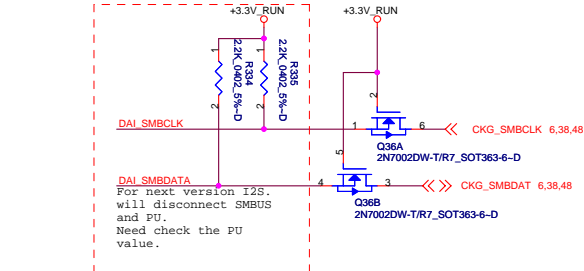
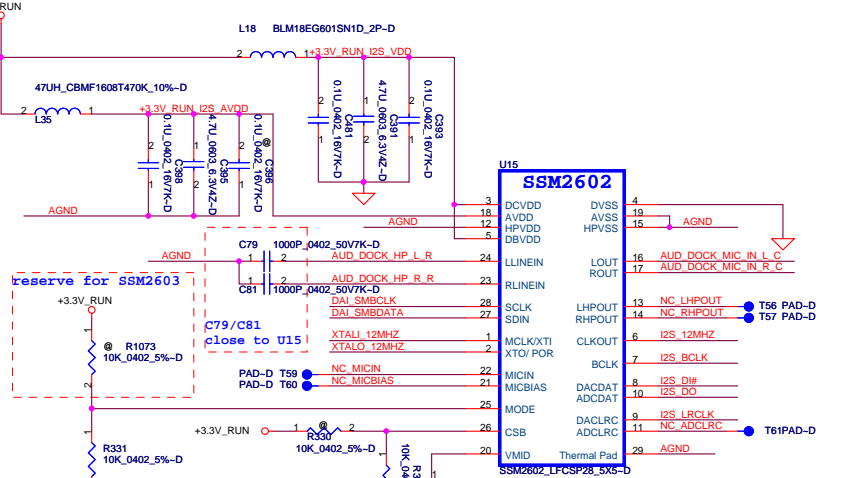
@ SPEAKER SET	
Part Number	Description
DA30000341L	PCB 03P LA-4051P REV0 M/B



92HD71B



Layout Skill
AGND short to GND



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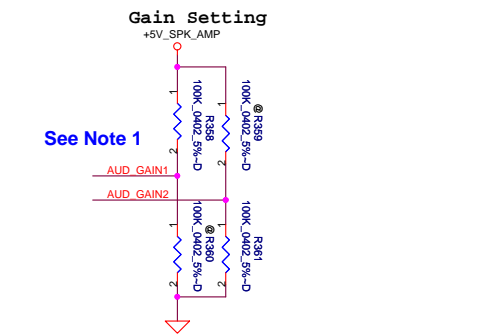
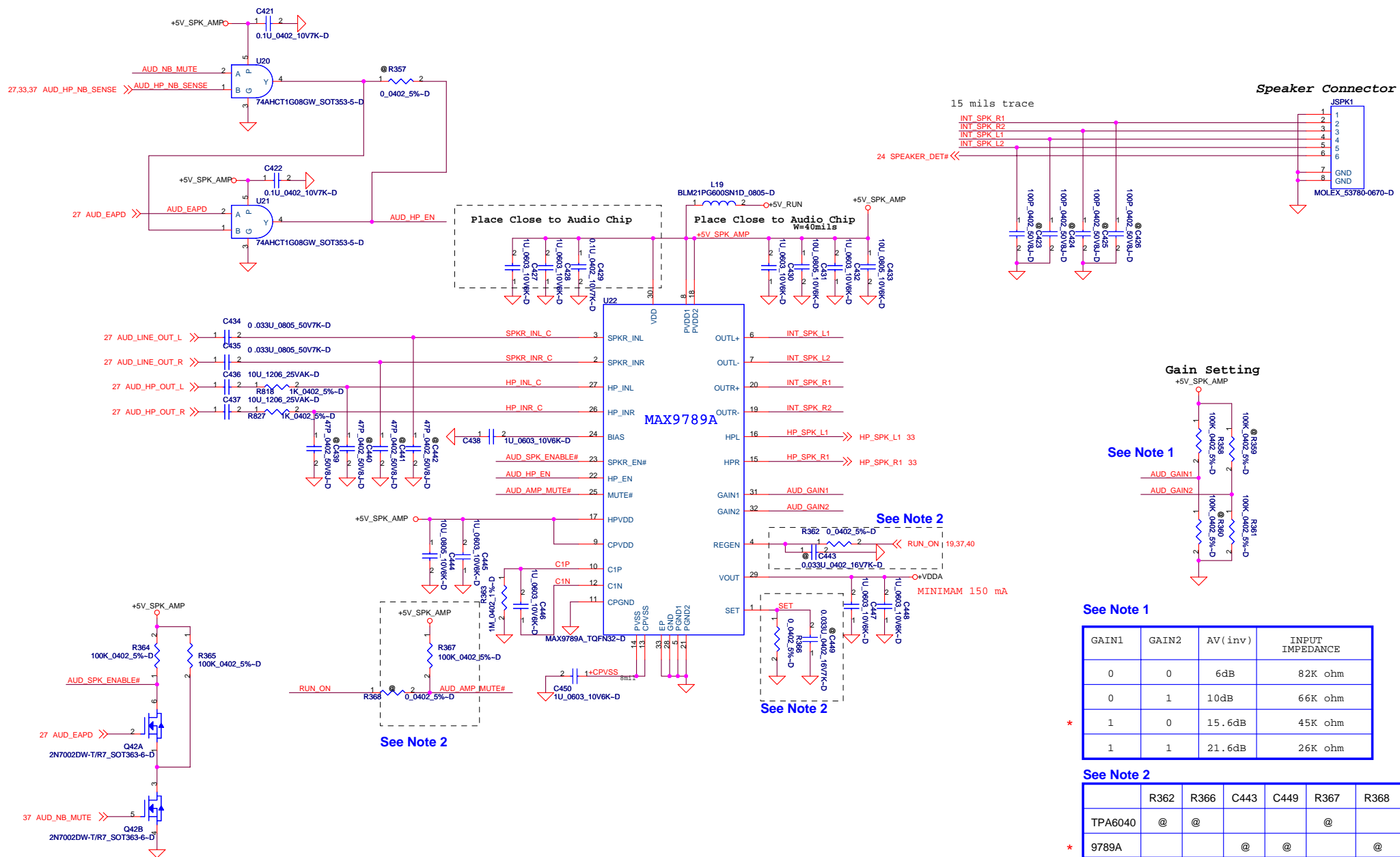
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Size: _____ Document Number: **401648**

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See Note 1

GAIN1	GAIN2	AV (inv)	INPUT IMPEDANCE
0	0	6dB	82K ohm
0	1	10dB	66K ohm
1	0	15.6dB	45K ohm
1	1	21.6dB	26K ohm

See Note 2

	R362	R366	C443	C449	R367	R368
TPA6040	@	@		@	@	
9789A			@	@		@

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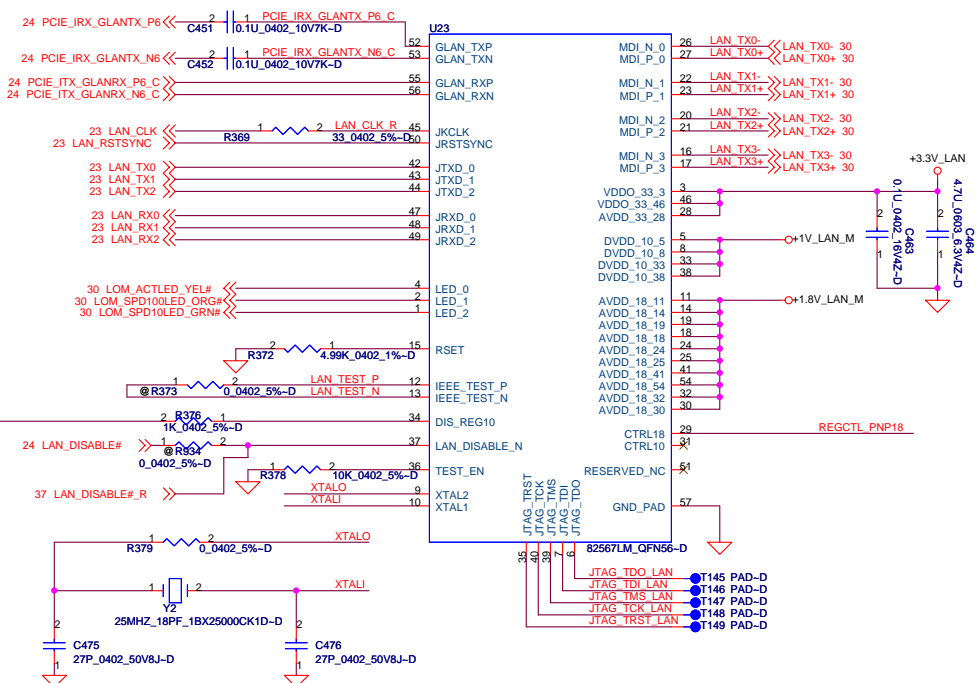
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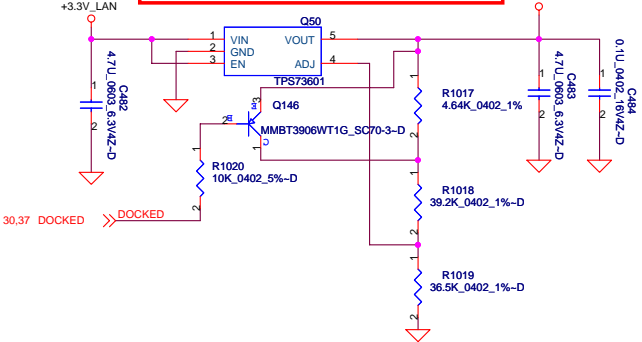
Date: Tuesday, October 28, 2008 Sheet 28 of 53



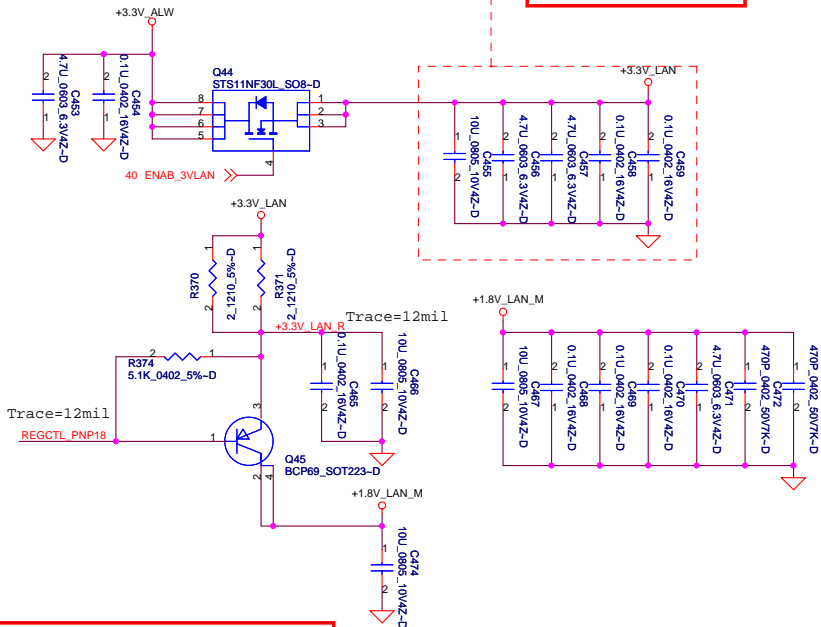
Need to ensure crystal at least 300uW max power drive-level

MA use internal 1V, NOT external solutions.
82567LM:
B0 version: 1.05V
A1 version: 1V

+LOM_VCT = 2.5V (WO/Docking)
= 2.65V (W/Docking)
 $V_{OUT} = 1.204 (1+R1/R2)$,
where R1 = R1017 + R1018, R2 = R1019



Layout Notice : Place as close chip as possible.



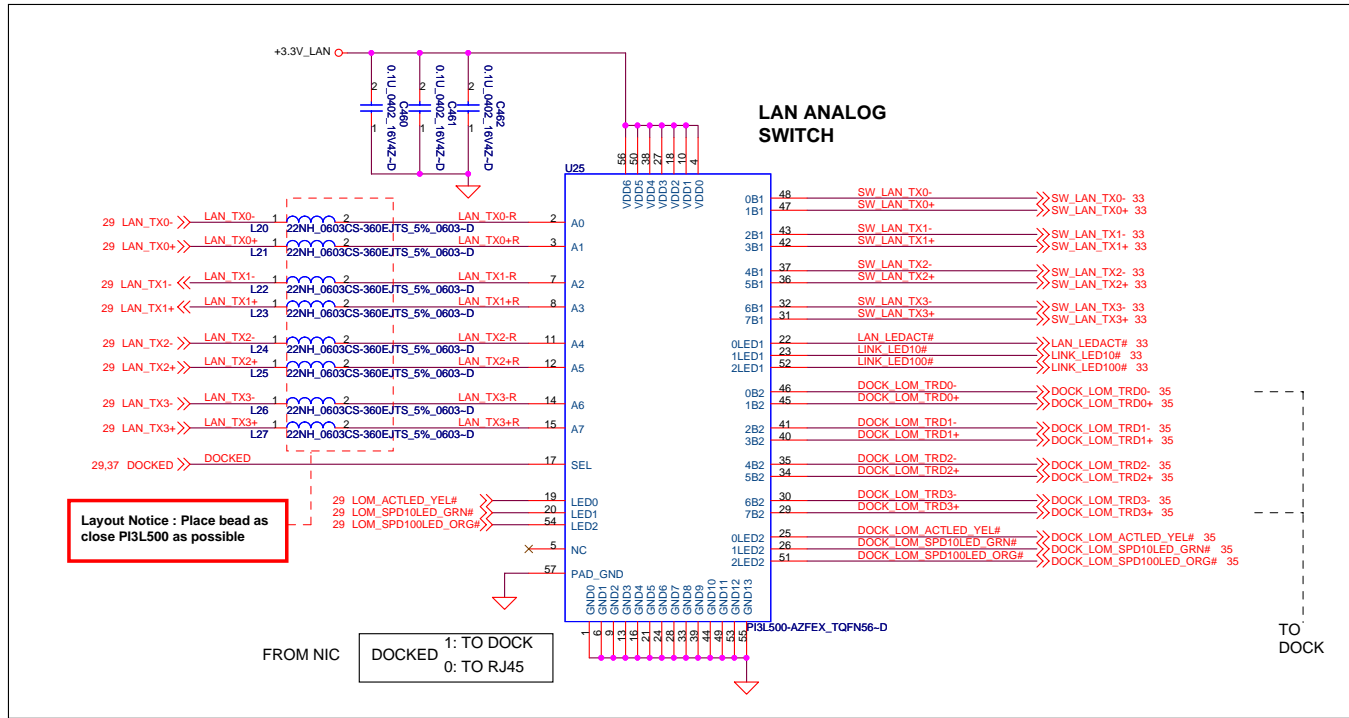
Follow 82567 schematic chiplist that VCC_1.0 for external use 10uF XR5 *2 and 0.1uF *2 for internal use 4.7uF X5R *2 and 0.1uF *3

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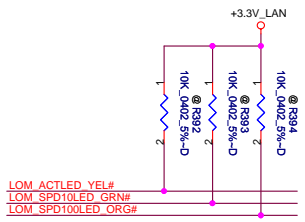
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SCHEMATIC_A4043			
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Layout Notice : Place bead as close P13L500 as possible



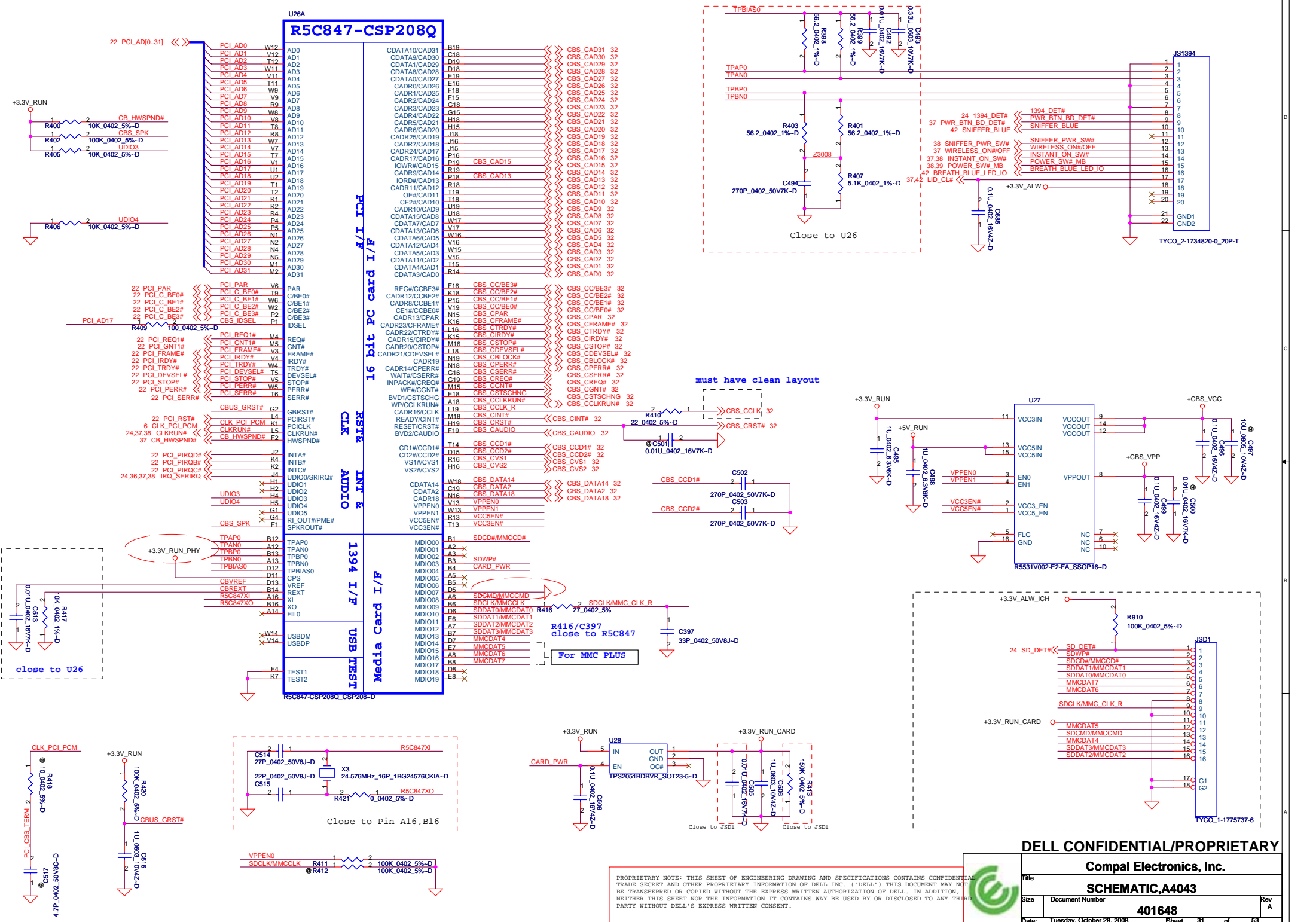
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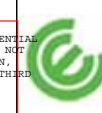
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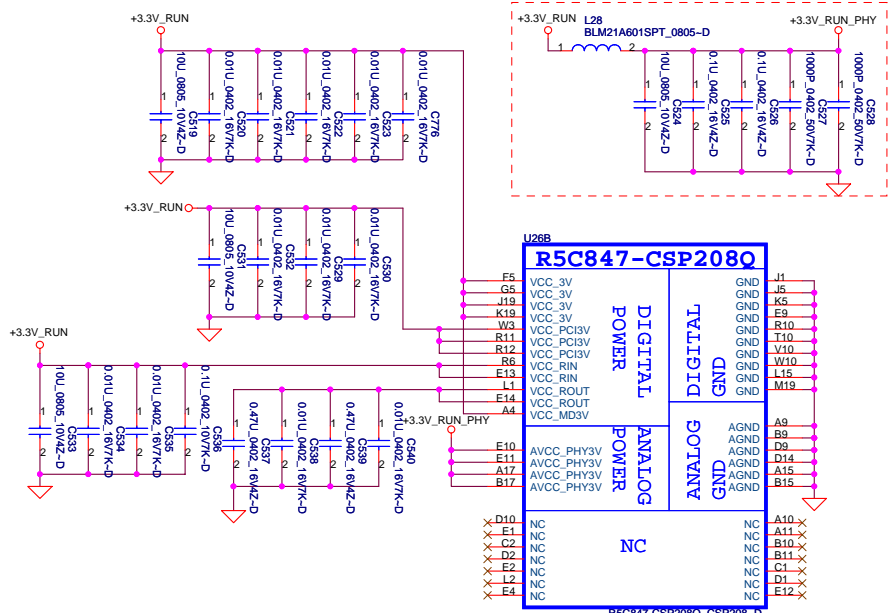
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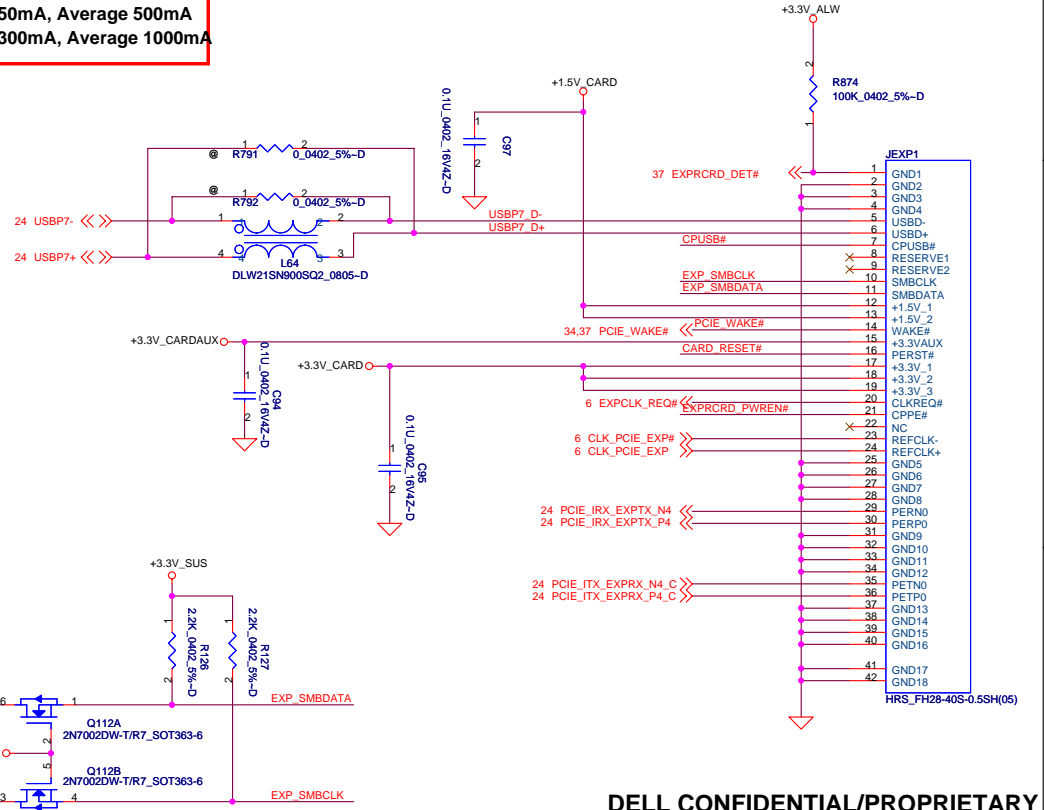
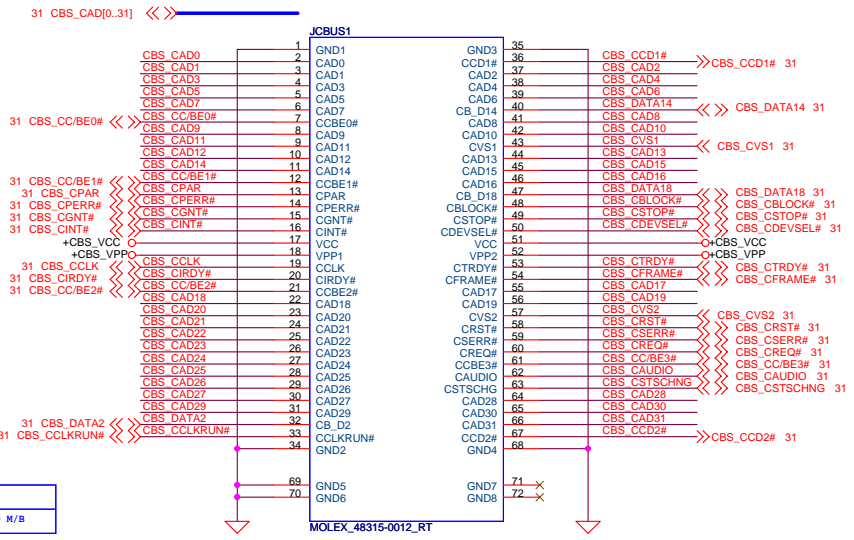
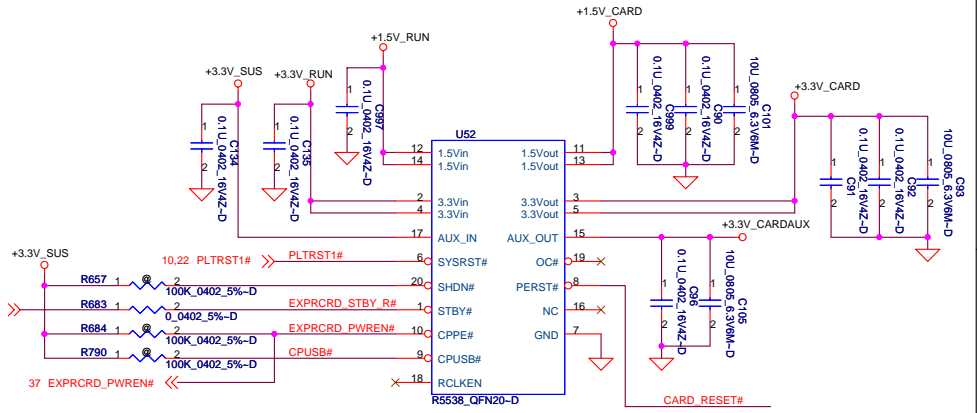
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Express Card

+1.5V_CARD: Max. 650mA, Average 500mA
+3.3V_CARD: Max. 1300mA, Average 1000mA

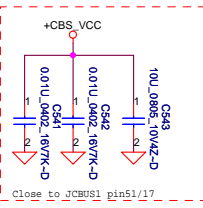
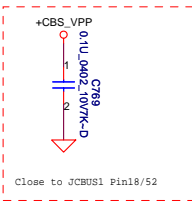


Part Number	Description
DA30000341L	PCB 03P LA-4051P REV0 M/B

Part Number	Description
DA30000341L	PCB 03P LA-4051P REV0 M/B

Part Number	Description
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Part Number	Description
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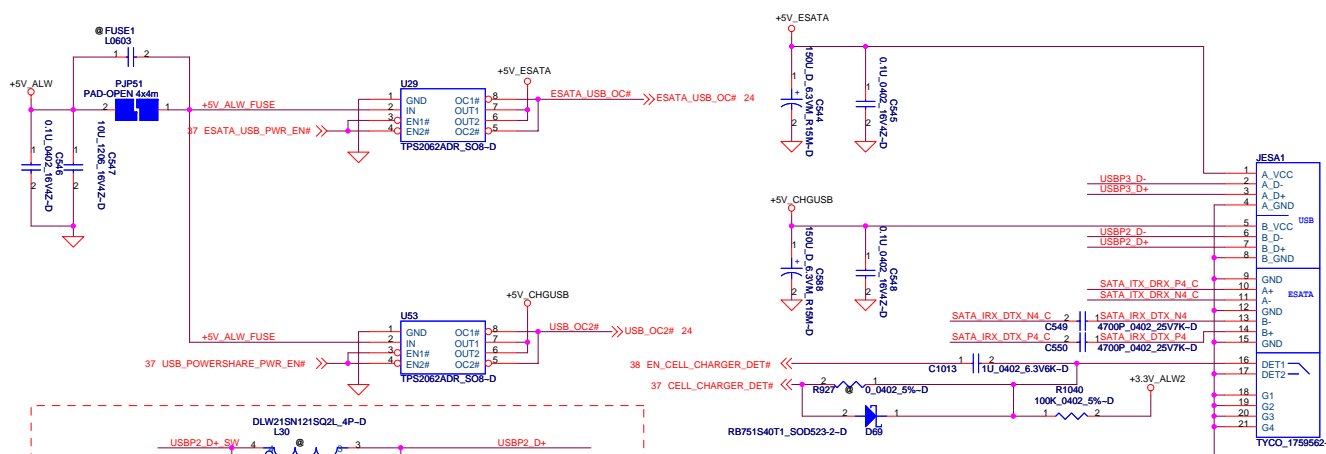
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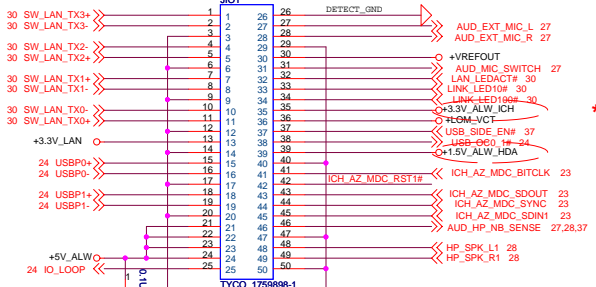
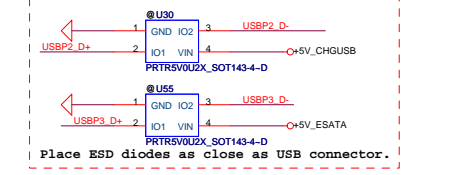
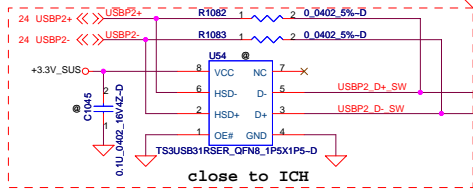
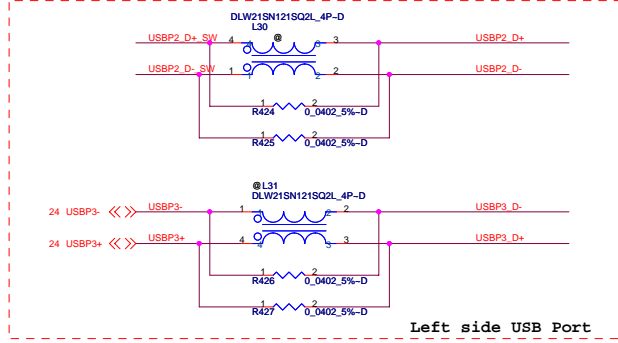
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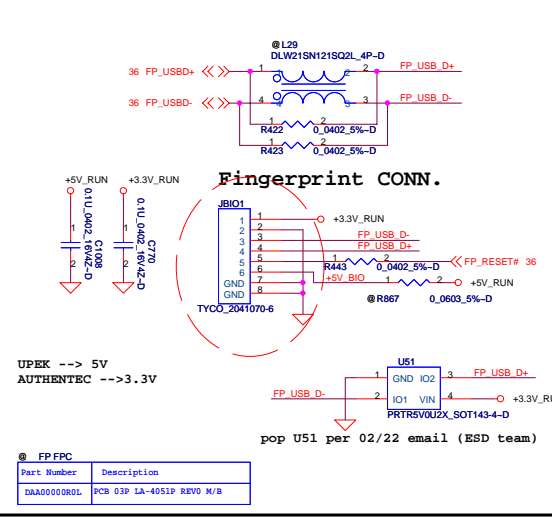
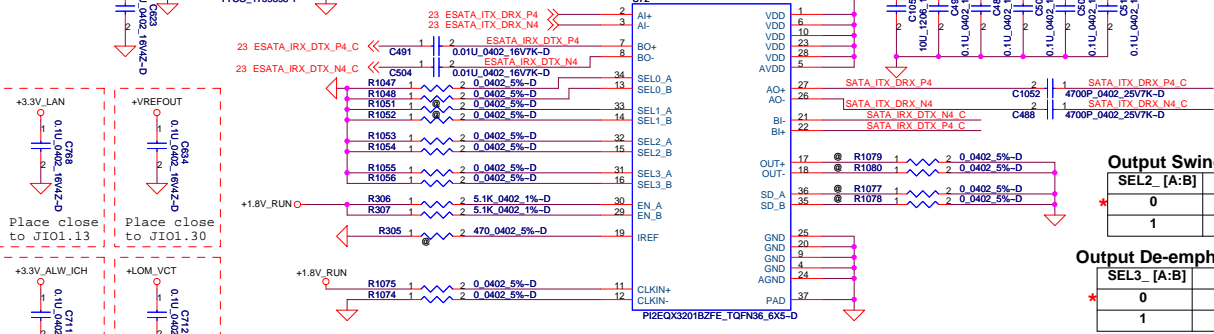


USB PORT#	DESTINATION
0	JUSB1 (Ext Right Side Top)
1	JUSB1 (Ext Right Side Bottom)
2	JESA1 (Ext Left Side Top)
3	JESA1 (Ext Left Side Bottom)
4	WLAN
5	WWAN
6	WPAN
7	Express card
8	DOCKING
9	DOCKING
10	USH->BIO
11	Camera



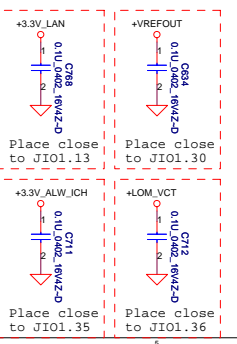
Equalizer Selection

SEL0_ [A:B]	SEL1_ [A:B]	Compliance Channel
0	0	no equalization
0	1	[0:2.5dB] @ 1.6 GHz
1	0	[2.5:4.5dB] @ 1.6 GHz
1	1	[4.5:6.5dB] @ 1.6 GHz



FP FPC

Part Number	Description
DA0A0000R0L	PCB 03P LA-4051P REV0 M/B

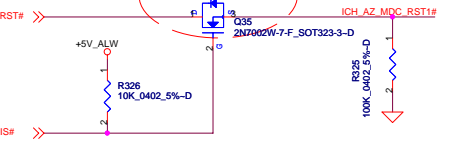


Output Swing Control

SEL2_ [A:B]	Swing
0	1x
1	1.2x

Output De-emphasis Adjustment

SEL3_ [A:B]	De-emphasis
0	0dB
1	-3.5dB



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Part Number: DA0A0000R0L, Description: PCB 03P LA-4051P REV0 M/B

Part Number: DA0A0000R0L, Description: PCB 03P LA-4051P REV0 M/B

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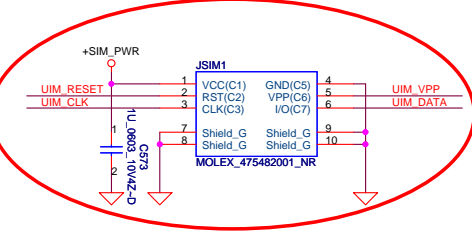
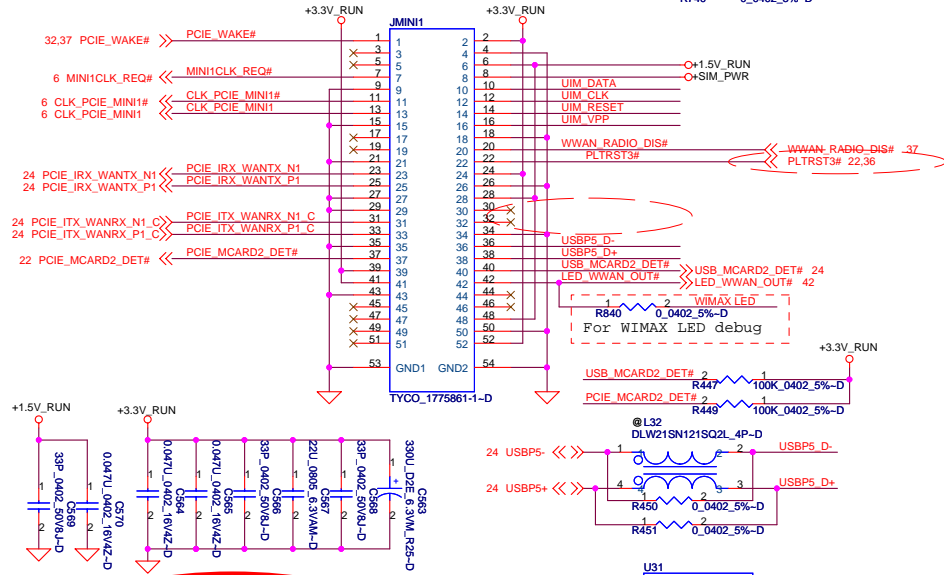
Date: Tuesday, October 28, 2008

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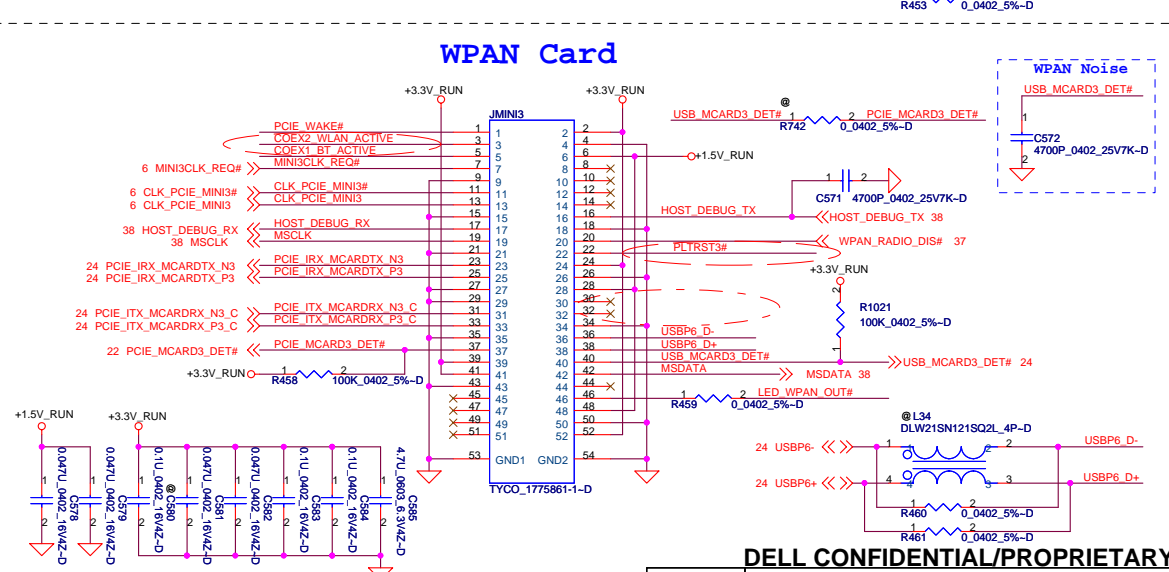
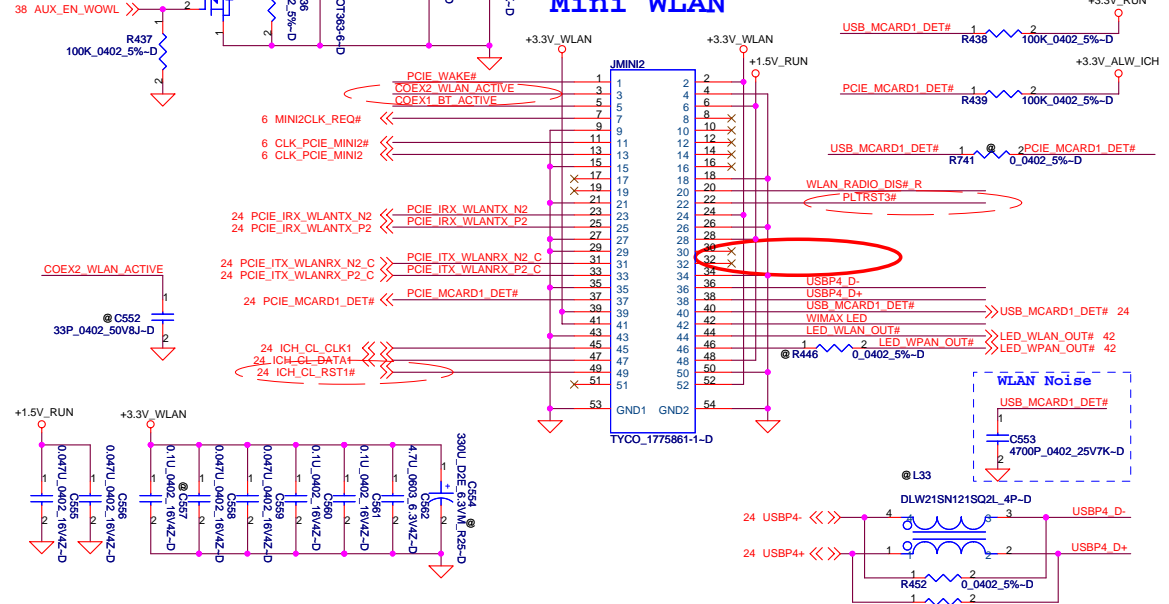
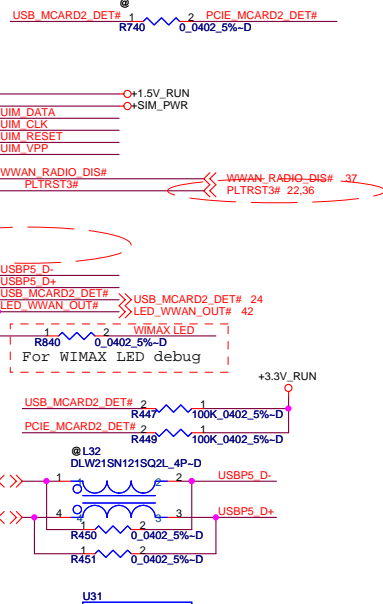
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Delete SM bus

Mini WWAN



PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+-9%	1000	750	
+3.3Vaux	+-9%	330	250	250 (Wake enable) 5 (Not wake enable)
+1.5V	+-5%	500	375	NA



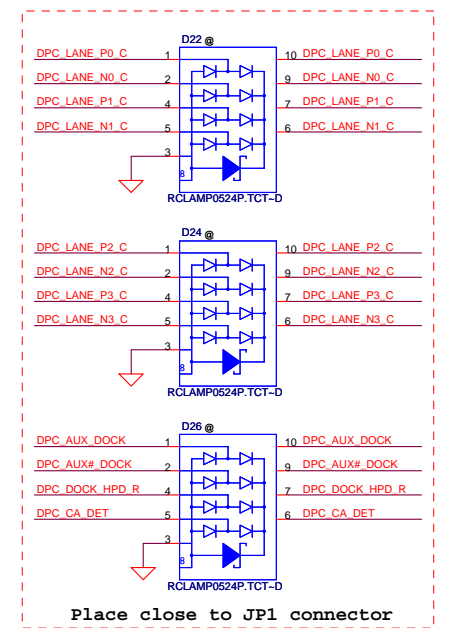
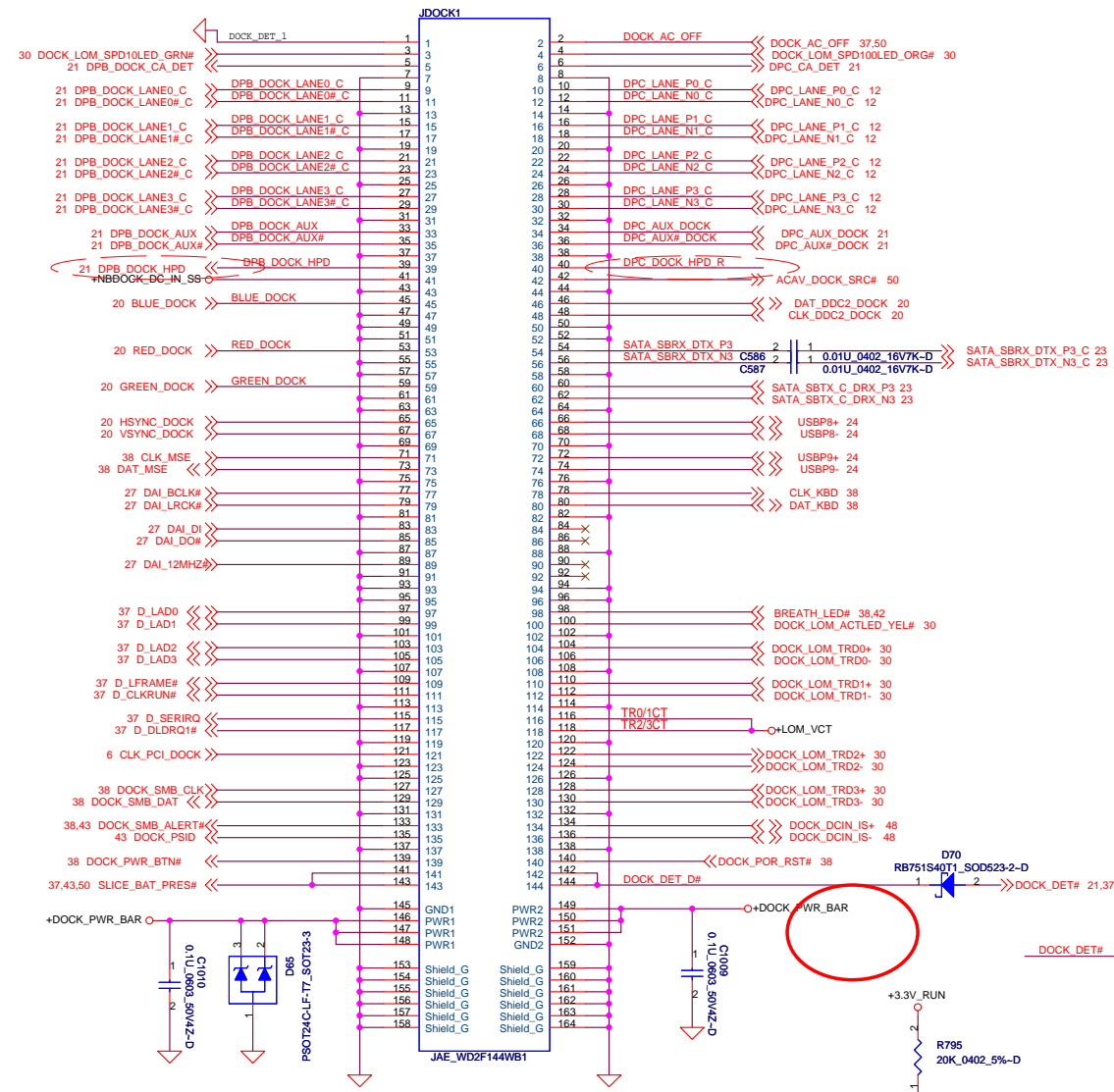
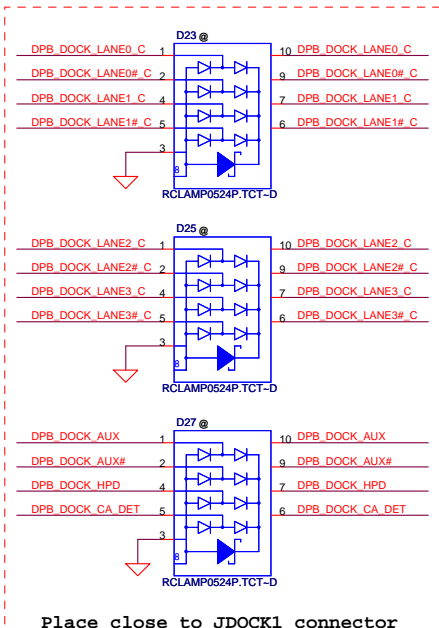
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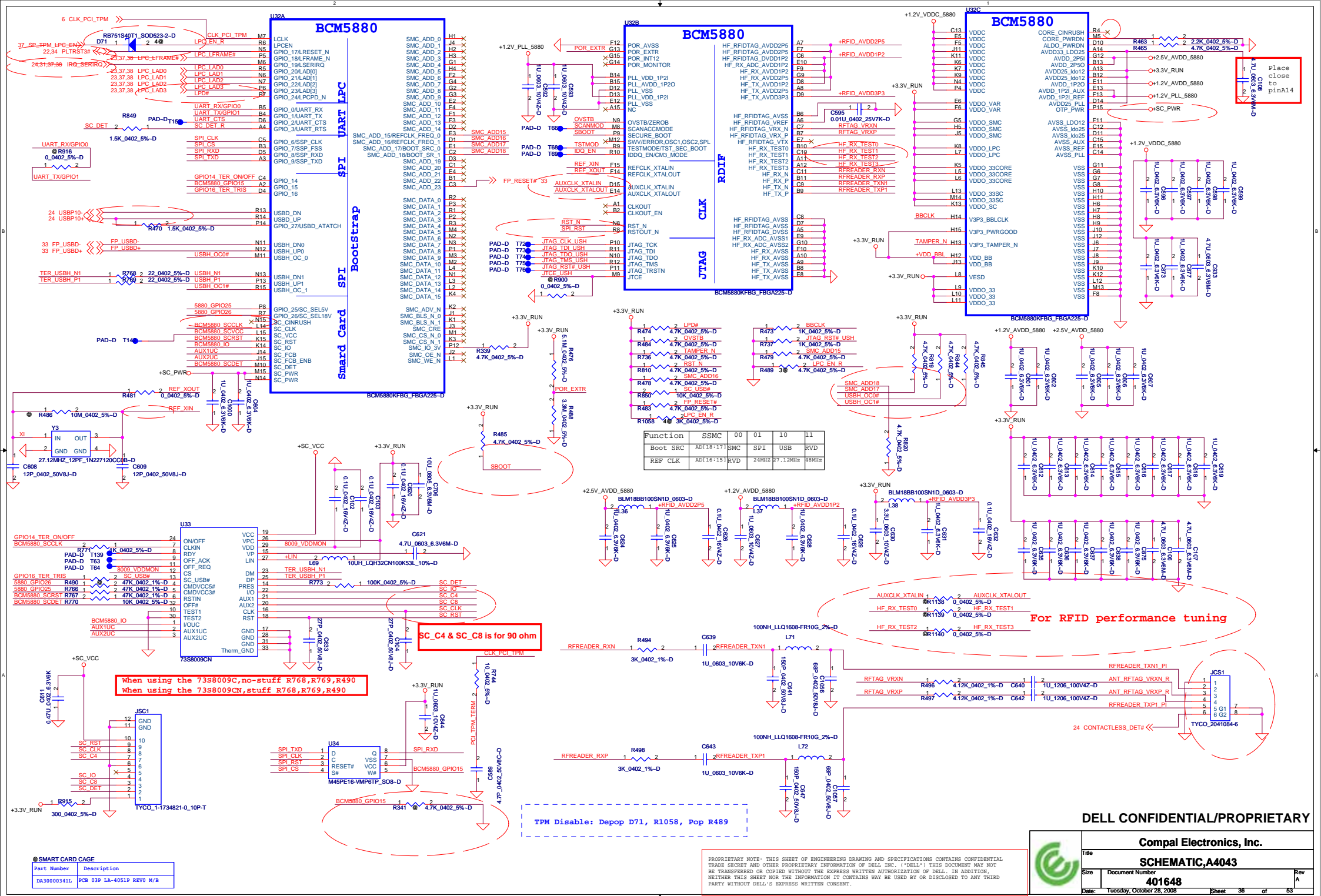
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Close to R796
Its Enhance ESD on dock issue.

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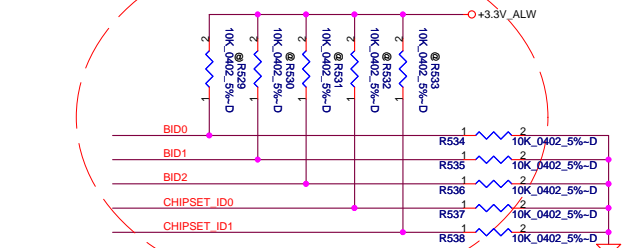
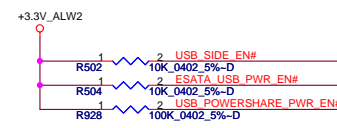
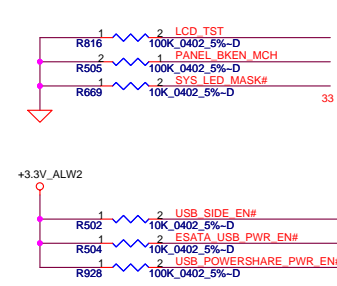
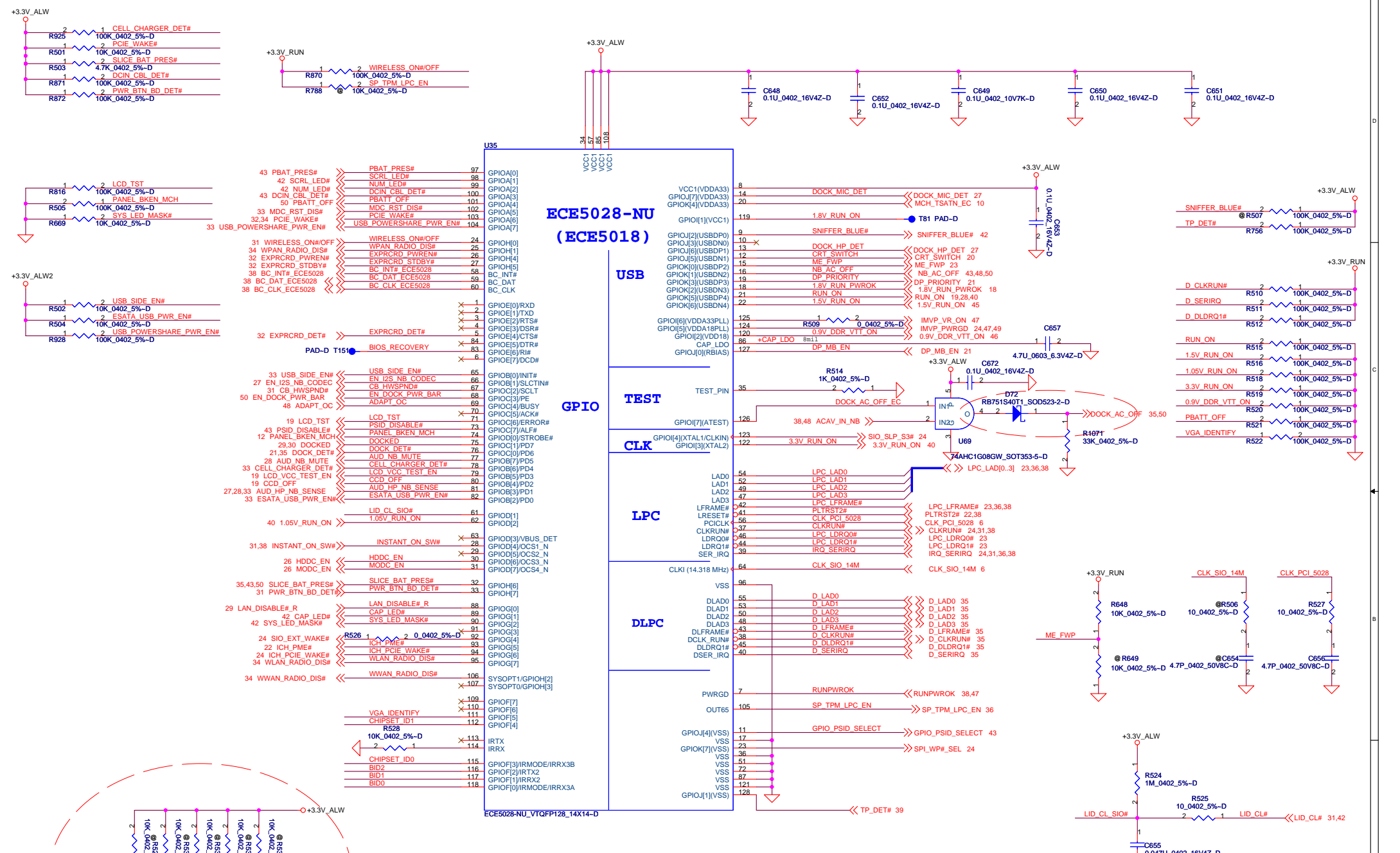
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@SMART CARD CAGE

Part Number	Description
DA3000034LL	PCB 03P LA-4051P REV0 M/B



CHIPSET_ID0	CHIPSET_ID1	Note
0	0	
0	0	

BID2	BID1	BID0	REV
0	0	0	X00

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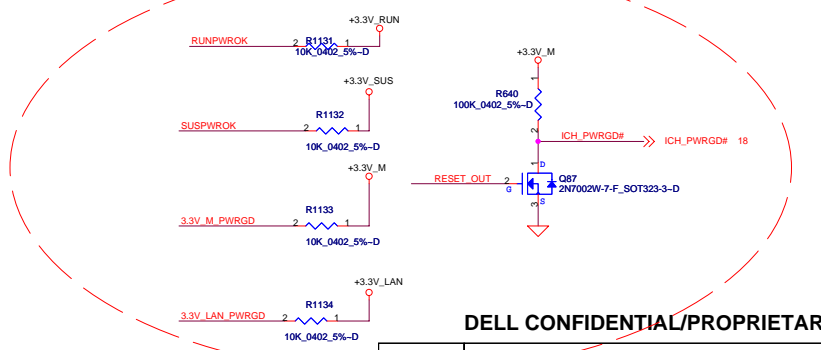
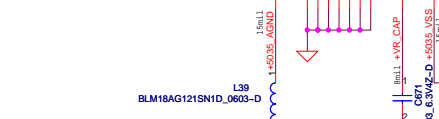
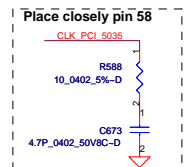
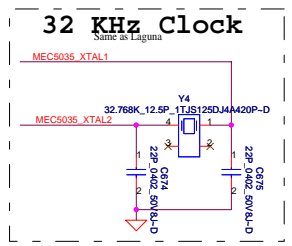
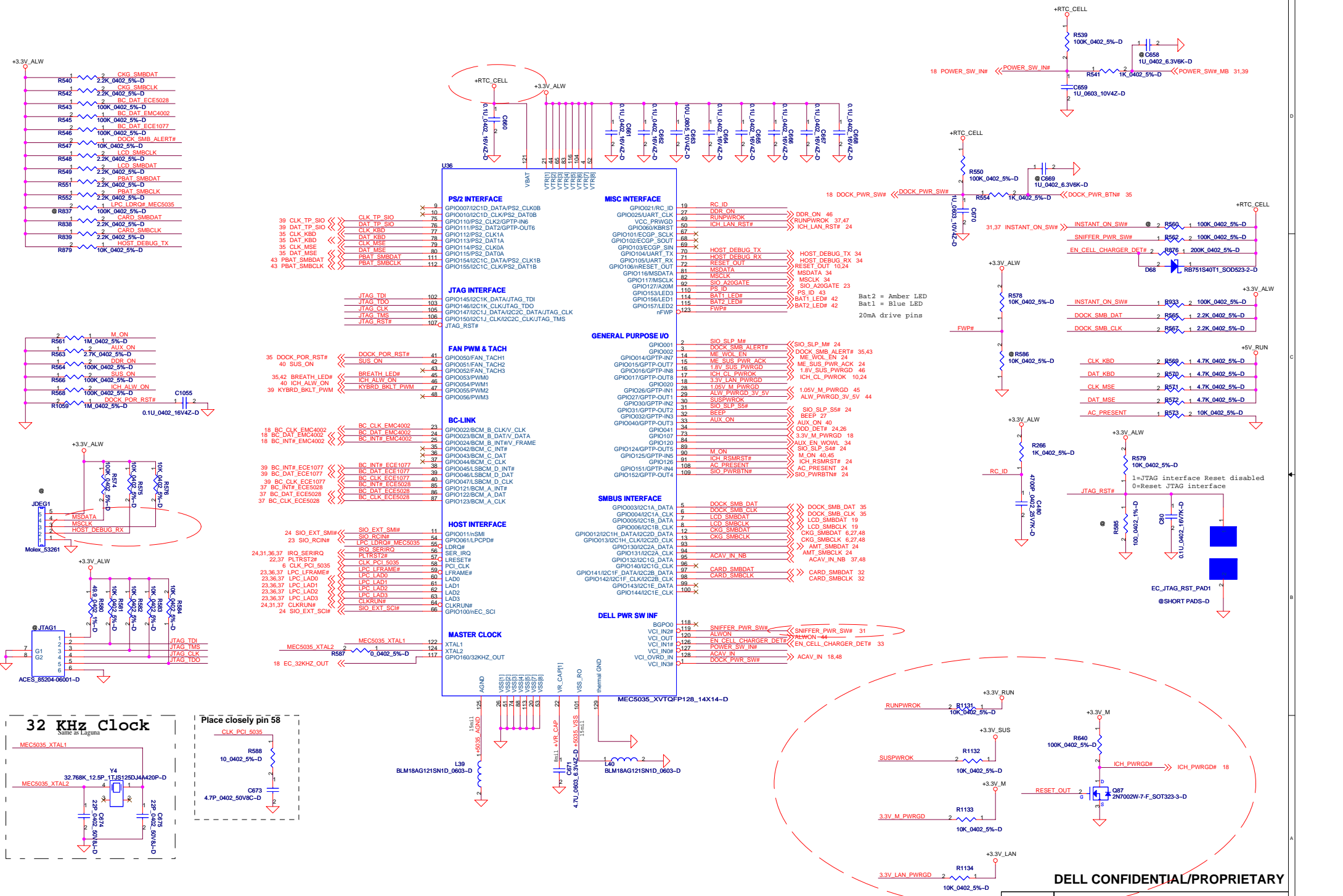
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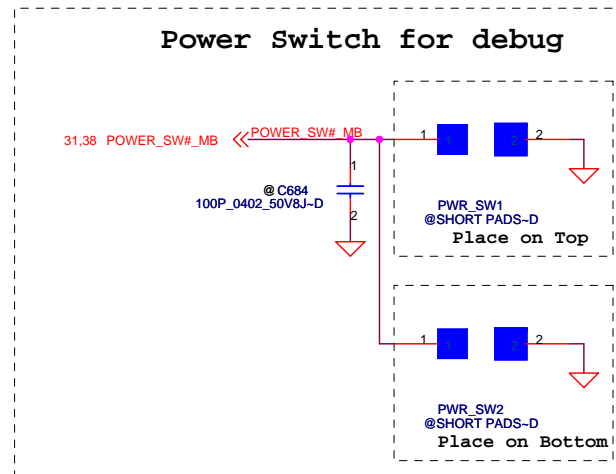
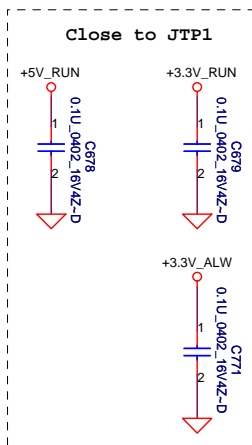
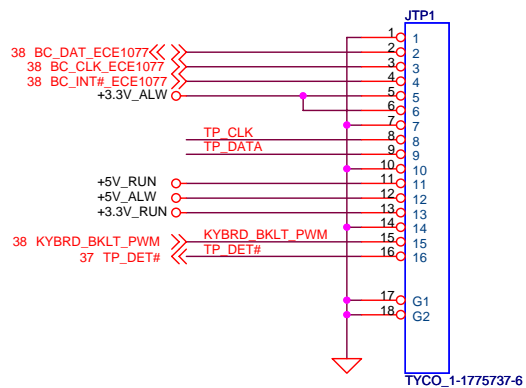
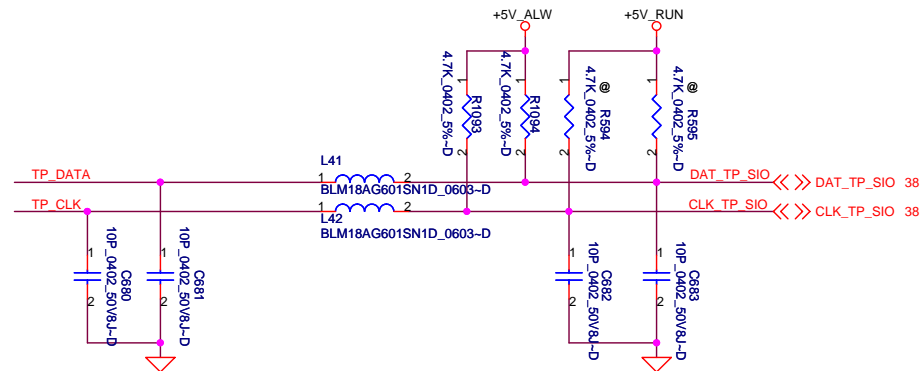
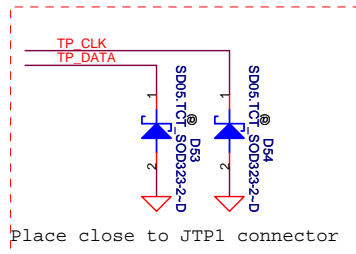
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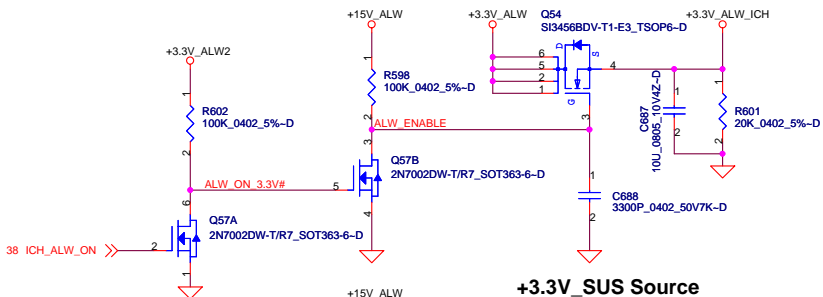
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Size	Document Number	
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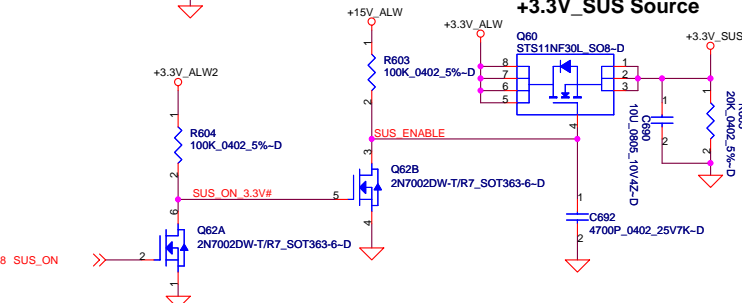


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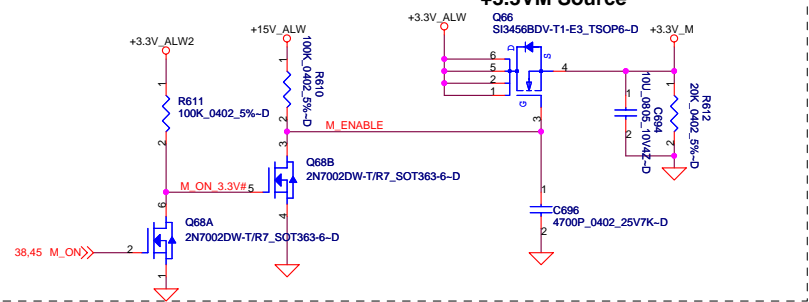
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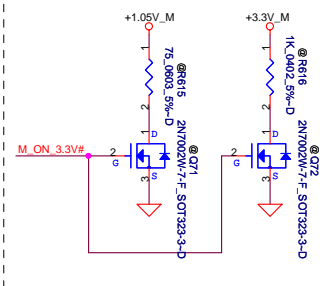
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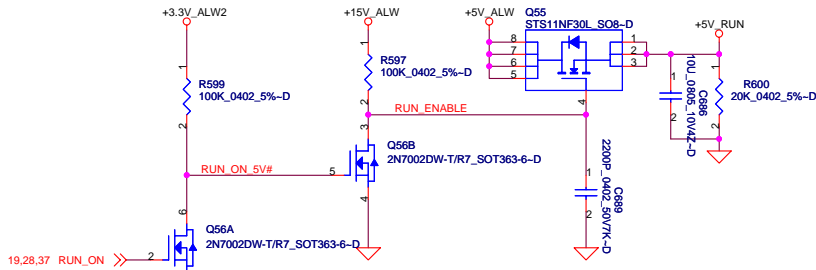
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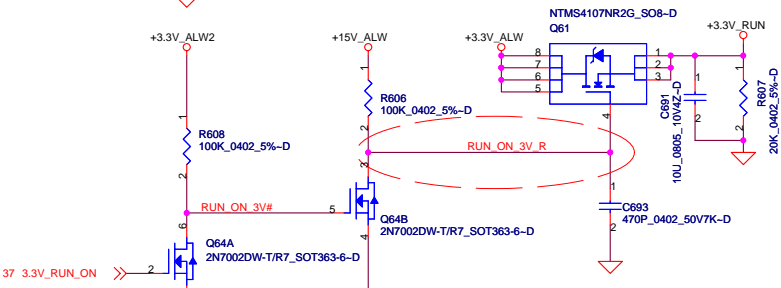
Discharge Circuit



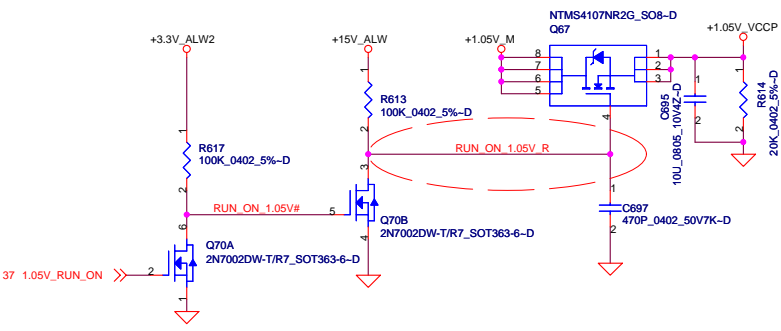
+5VRUN Source



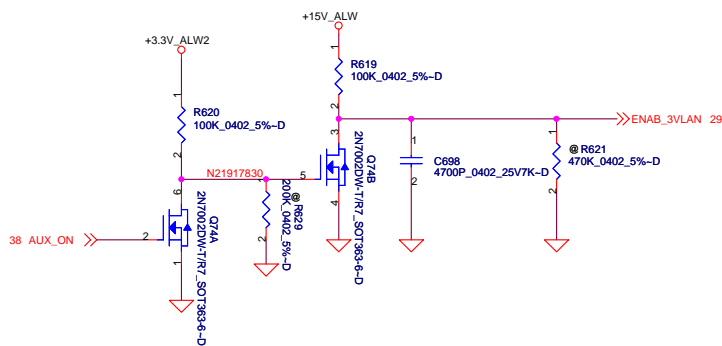
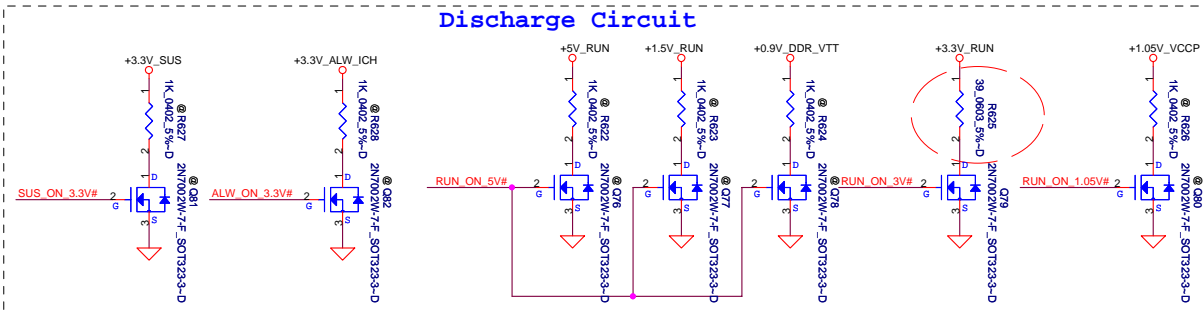
+3.3V_RUN Source



+1.05V_VCCP Source



Discharge Circuit



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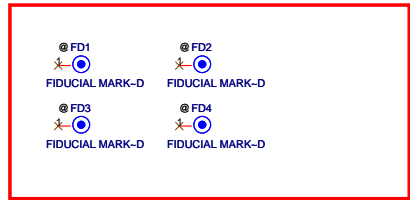
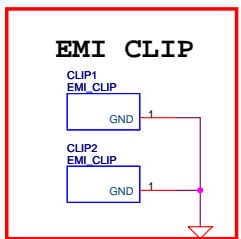
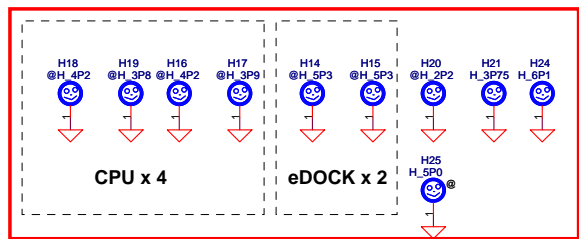
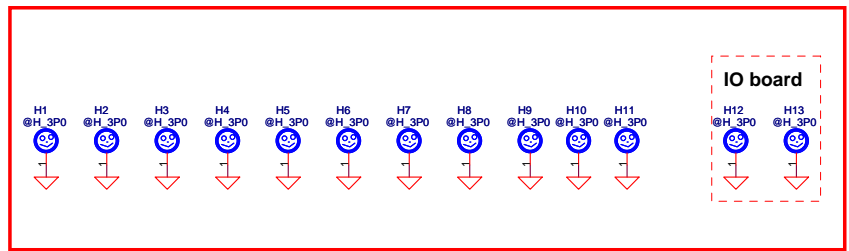
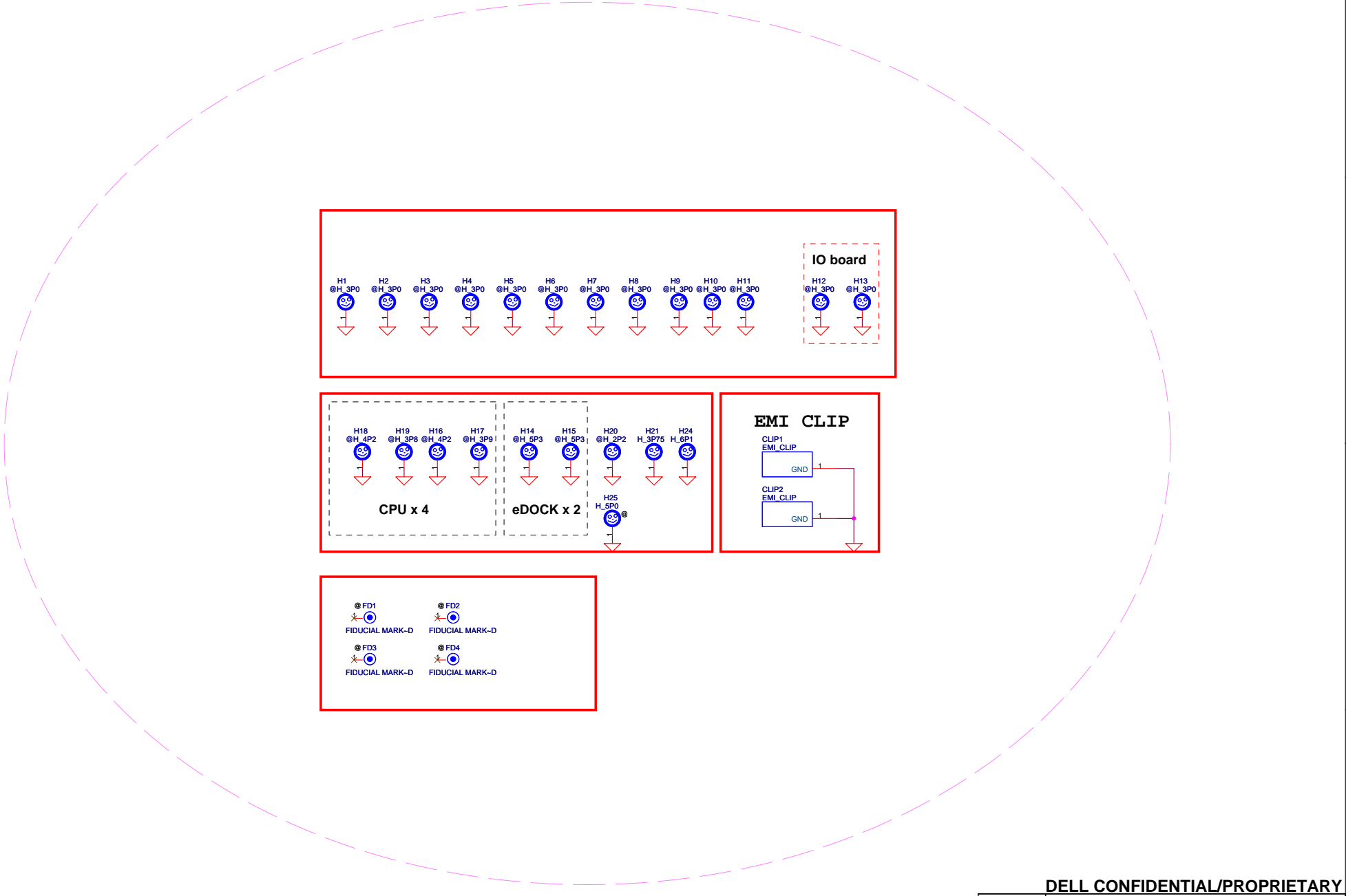
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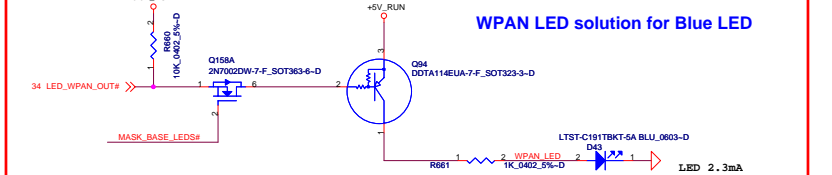
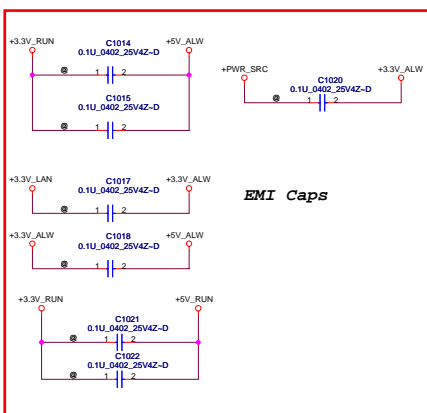
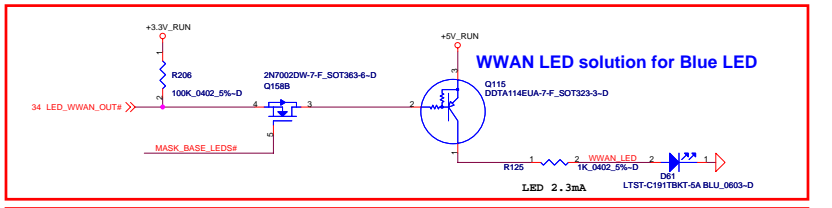
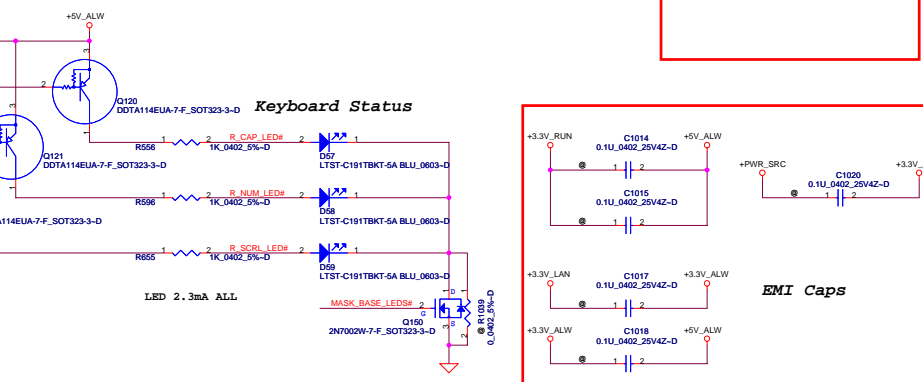
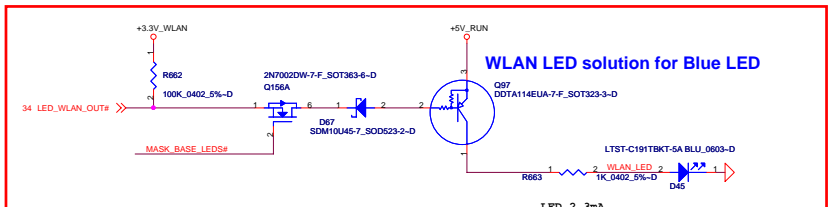
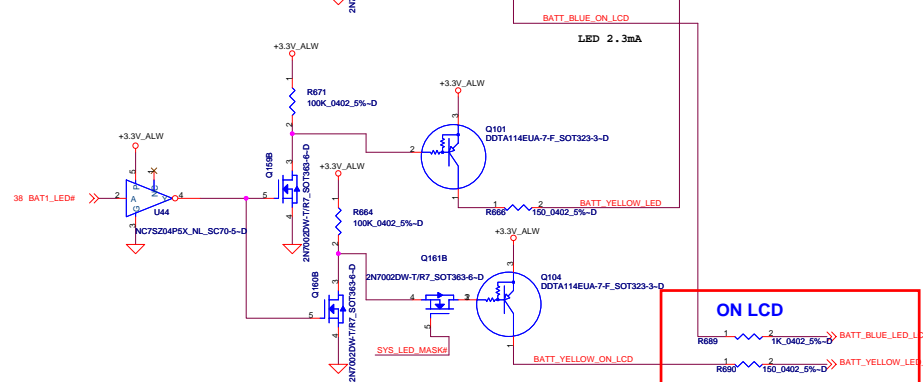
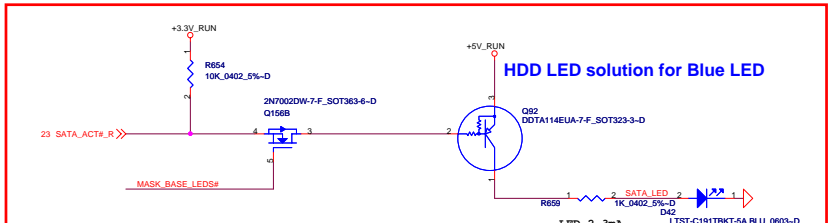
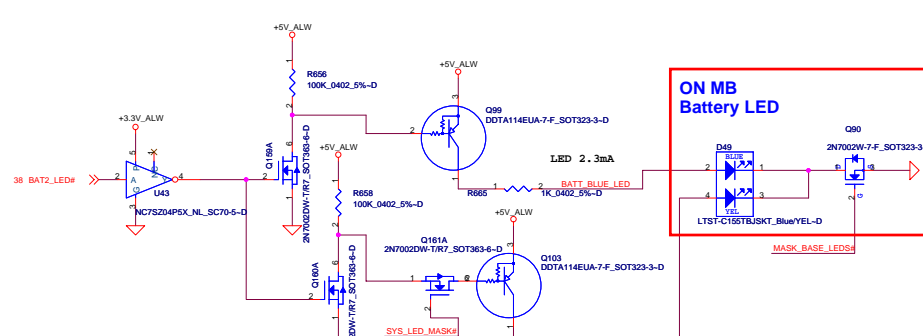
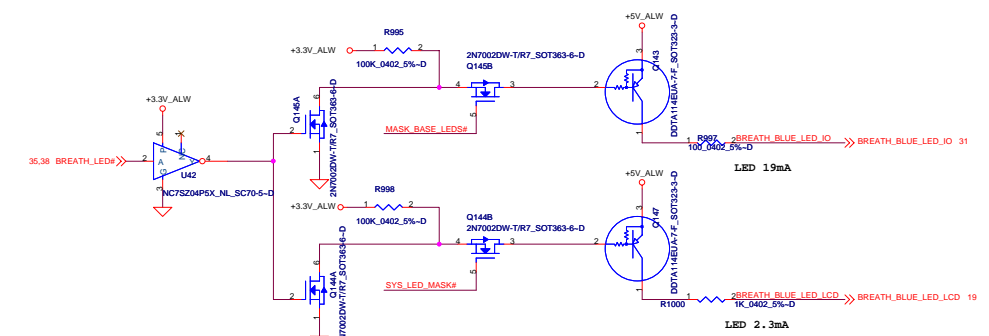
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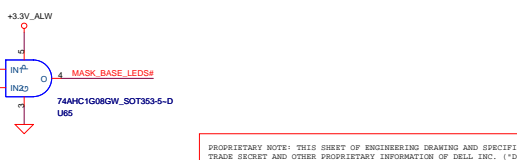
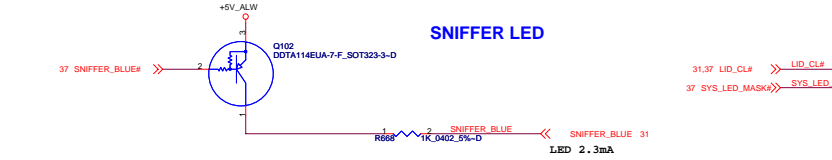
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LED Circuit Control Table

	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



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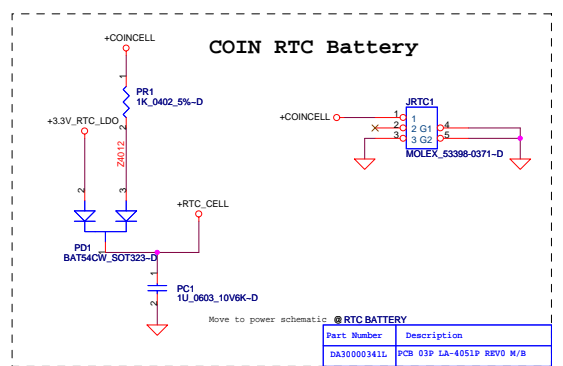
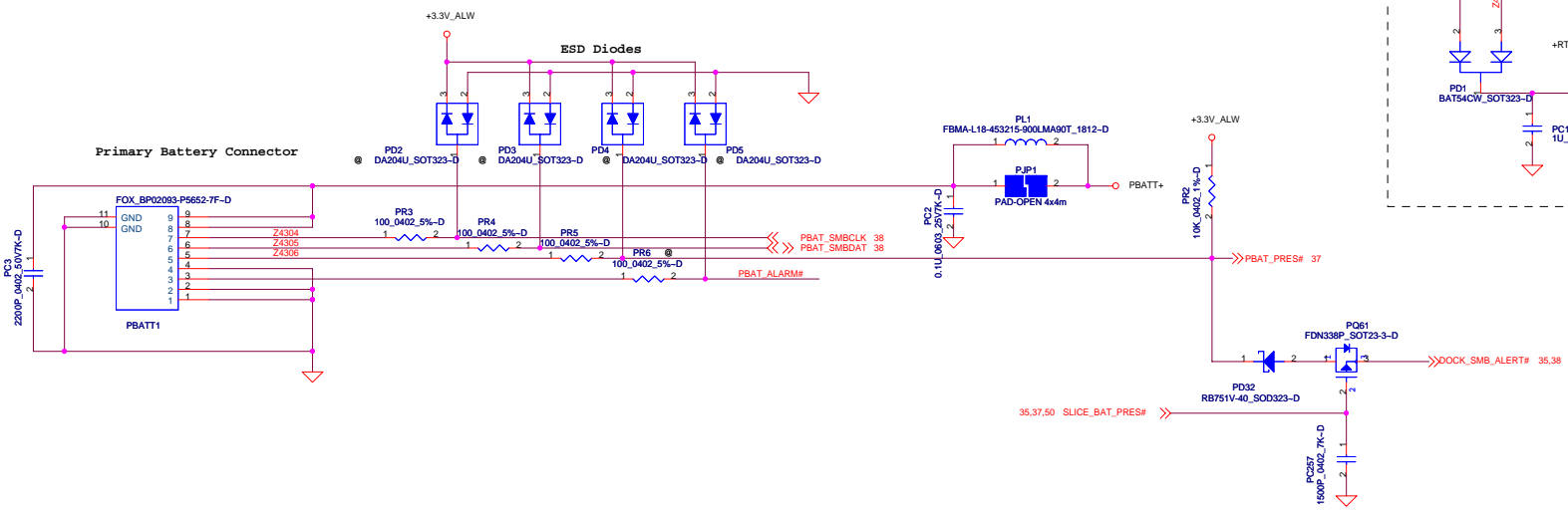
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Issue: 1/06/2009, October 23, 2008

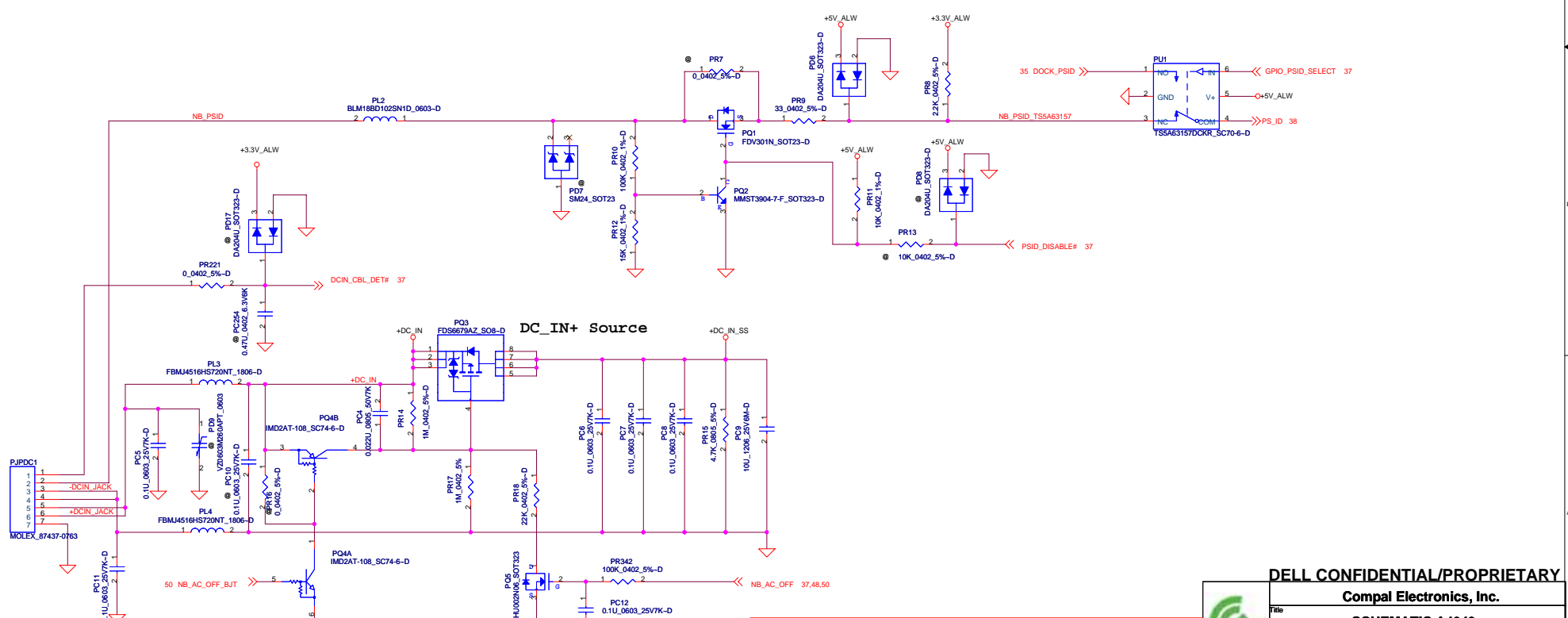
Rev: **A**

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@ RTC BATTERY	
Part Number	Description
DA30000341L	PCB 03P LA-4051P REV0 M/B



@ DC-IN cable	
Part Number	Description
DC3100380L	CONN SHR 03N 10CA2CK-NB
	NMDC-DC3A1201-DP

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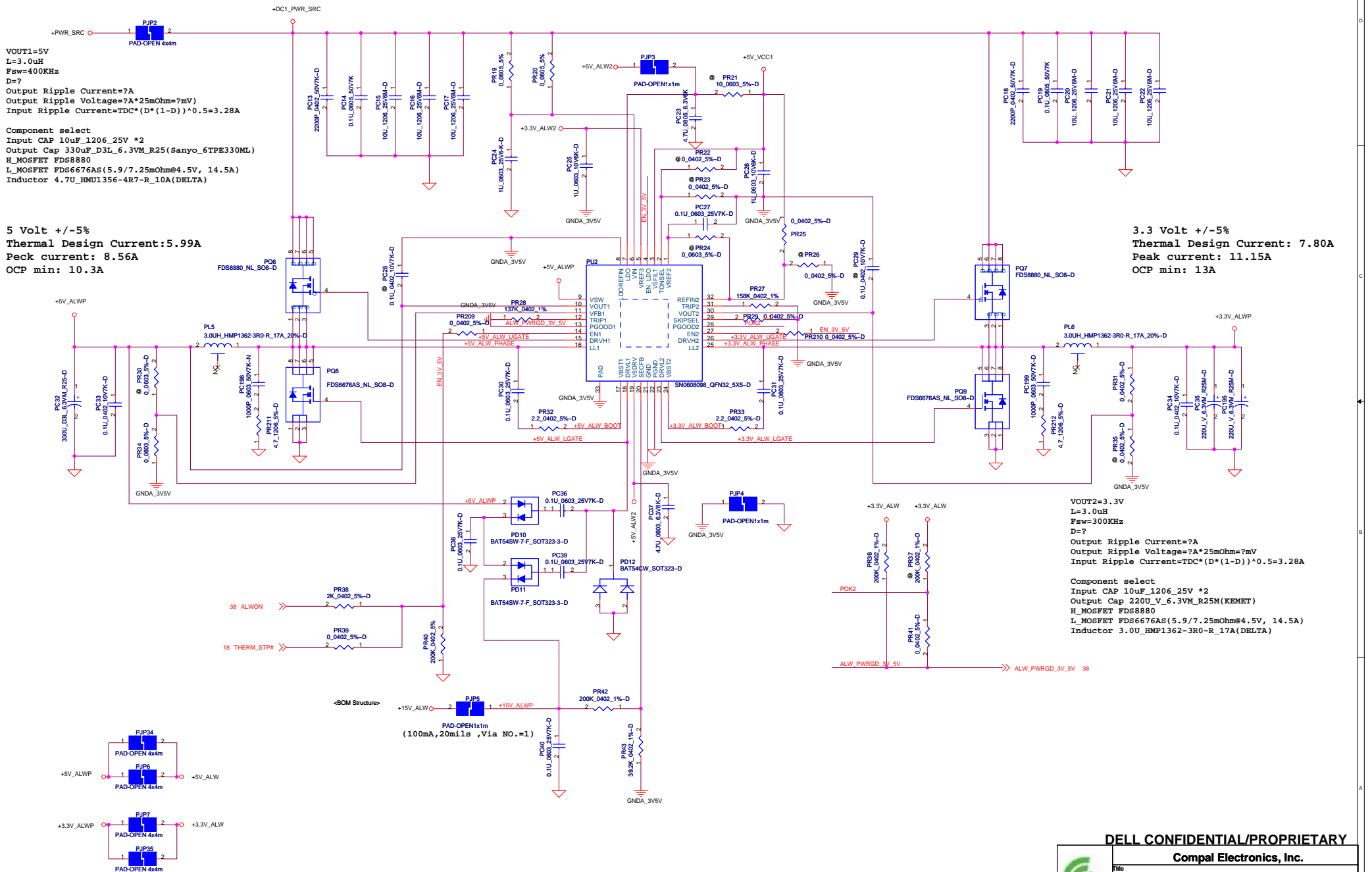
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+3.3V_ALWP/ +5V_ALWP/ +5V_ALW2 / +15V_ALWP



VOUT1=5V
L=3.0uH
Fsw=400KHz
D=?
Output Ripple Current=?A
Output Ripple Voltage=?A*25mOhm=?mV
Input Ripple Current=TDC*(D*(1-D))^0.5=3.28A

Component select
Input CAP 10uF_1206_25V *2
Output Cap 330uF_D3L_6.3VM_R25(Sanyo_6TPE330ML)
H_MOSFET FDS8880
L_MOSFET FDS6676AS(5.9/7.25mOhm@4.5V, 14.5A)
Inductor 4.7U_HMU1356-4R7-R_10A(DELTA)

5 Volt +/-5%
Thermal Design Current:5.99A
Peck current: 8.56A
OCP min: 10.3A

3.3 Volt +/-5%
Thermal Design Current: 7.80A
Peak current: 11.15A
OCP min: 13A

VOUT2=3.3V
L=3.0uH
Fsw=300KHz
D=?
Output Ripple Current=?A
Output Ripple Voltage=?A*25mOhm=?mV
Input Ripple Current=TDC*(D*(1-D))^0.5=3.28A

Component select
Input CAP 10uF_1206_25V *2
Output Cap 220U_V_6.3VM_R25(KEMET)
H_MOSFET FDS8880
L_MOSFET FDS6676AS(5.9/7.25mOhm@4.5V, 14.5A)
Inductor 3.0U_HMP1362-3R0-R_17A(DELTA)

<BOM Structure>
+15V_ALW1
PJP5
PAD-OPEN1x1m
(100mA, 20mils, Via NO.=1)

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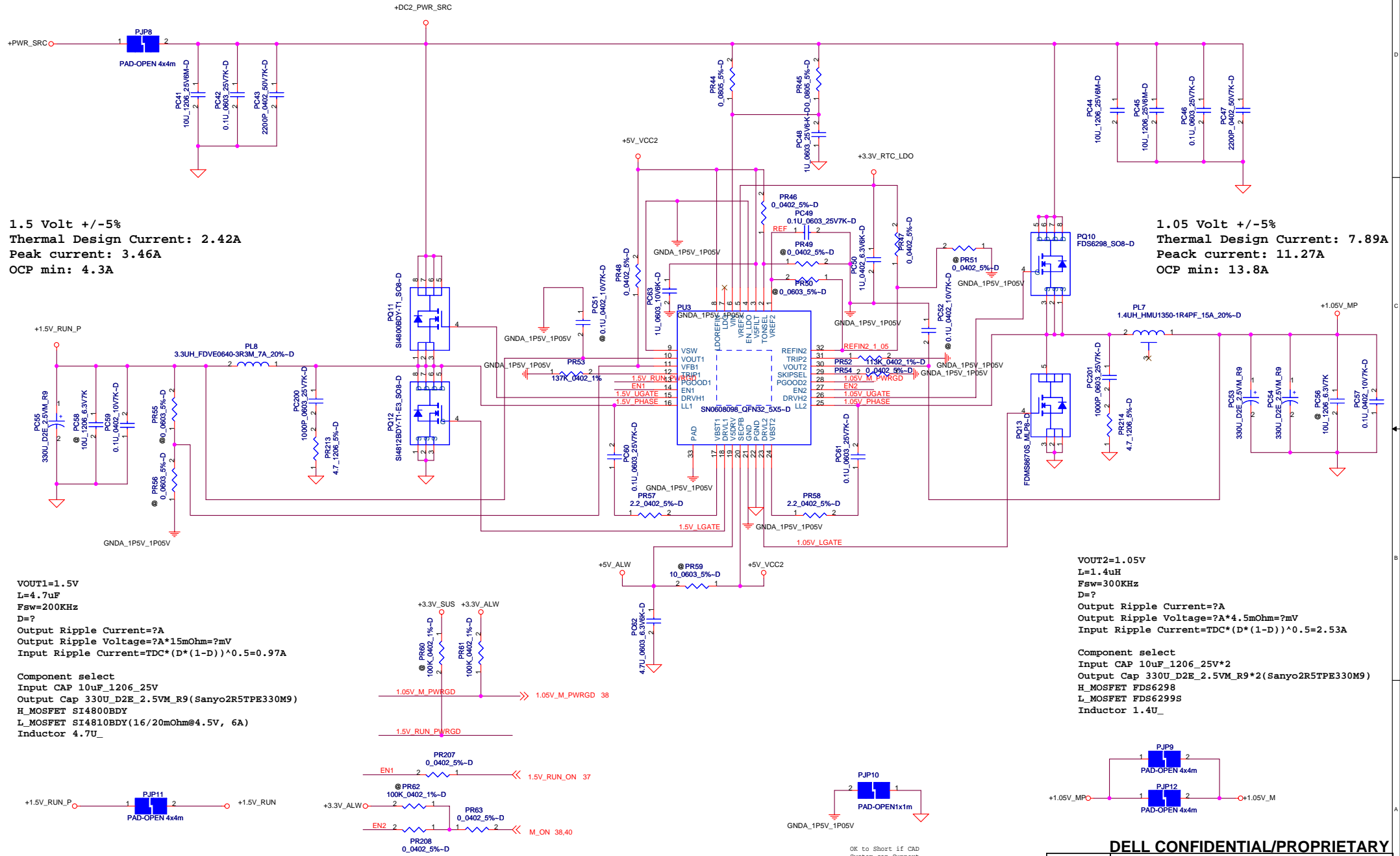
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+1.5V_RUN / +1.05V_M / +3.3V_RTC_LDO



1.5 Volt +/-5%
 Thermal Design Current: 2.42A
 Peak current: 3.46A
 OCP min: 4.3A

1.05 Volt +/-5%
 Thermal Design Current: 7.89A
 Peak current: 11.27A
 OCP min: 13.8A

VOUT1=1.5V
 L=4.7uF
 Fsw=200KHz
 D=?
 Output Ripple Current=?A
 Output Ripple Voltage=?A*15mOhm=?mV
 Input Ripple Current=TDC*(D*(1-D))^0.5=0.97A

Component select
 Input CAP 10uF_1206_25V
 Output Cap 330U_D2E_2.5VM_R9 (Sanyo2R5TPE330M9)
 H_MOSFET SI4800BDY
 L_MOSFET SI4810BDY(16/20mOhm@4.5V, 6A)
 Inductor 4.7U

VOUT2=1.05V
 L=1.4uH
 Fsw=300KHz
 D=?
 Output Ripple Current=?A
 Output Ripple Voltage=?A*4.5mOhm=?mV
 Input Ripple Current=TDC*(D*(1-D))^0.5=2.53A

Component select
 Input CAP 10uF_1206_25V*2
 Output Cap 330U_D2E_2.5VM_R9*2 (Sanyo2R5TPE330M9)
 H_MOSFET FDS6298
 L_MOSFET FDS6299S
 Inductor 1.4U

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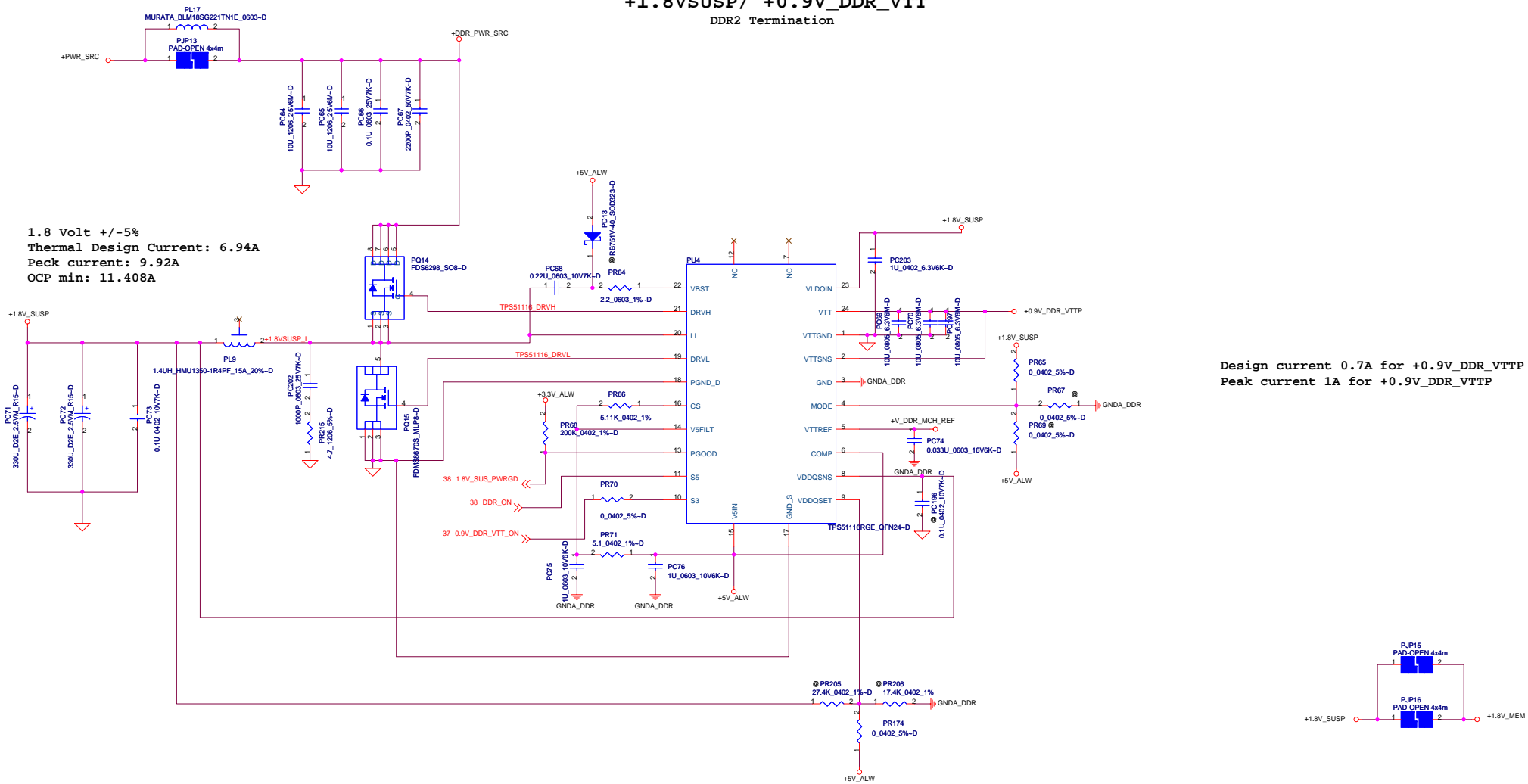
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+1.8VSUSP/ +0.9V_DDR_VTT
DDR2 Termination

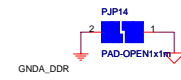
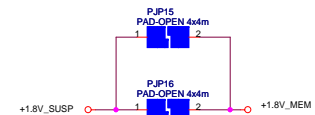


1.8 Volt +/-5%
 Thermal Design Current: 6.94A
 Peck current: 9.92A
 OCP min: 11.408A

Design current 0.7A for +0.9V_DDR_VTTP
 Peak current 1A for +0.9V_DDR_VTTP

VOUT1=1.8V
 L=1.4uH
 Fsw=400KHz
 D=?
 Output Ripple Current=?A
 Output Ripple Voltage=?A*15mOhm=7mV
 Input Ripple Current=I_{DC}*(D*(1-D))*0.5=0.97A

Component select
 Input CAP 10uF_1206_25V
 Output Cap 330U_D2E_2.5VM_R9*2(Sanyo2R5TPE330M9)
 H_MOSFET FDS6298
 L_MOSFET FDS6299S
 Inductor 1.4U_



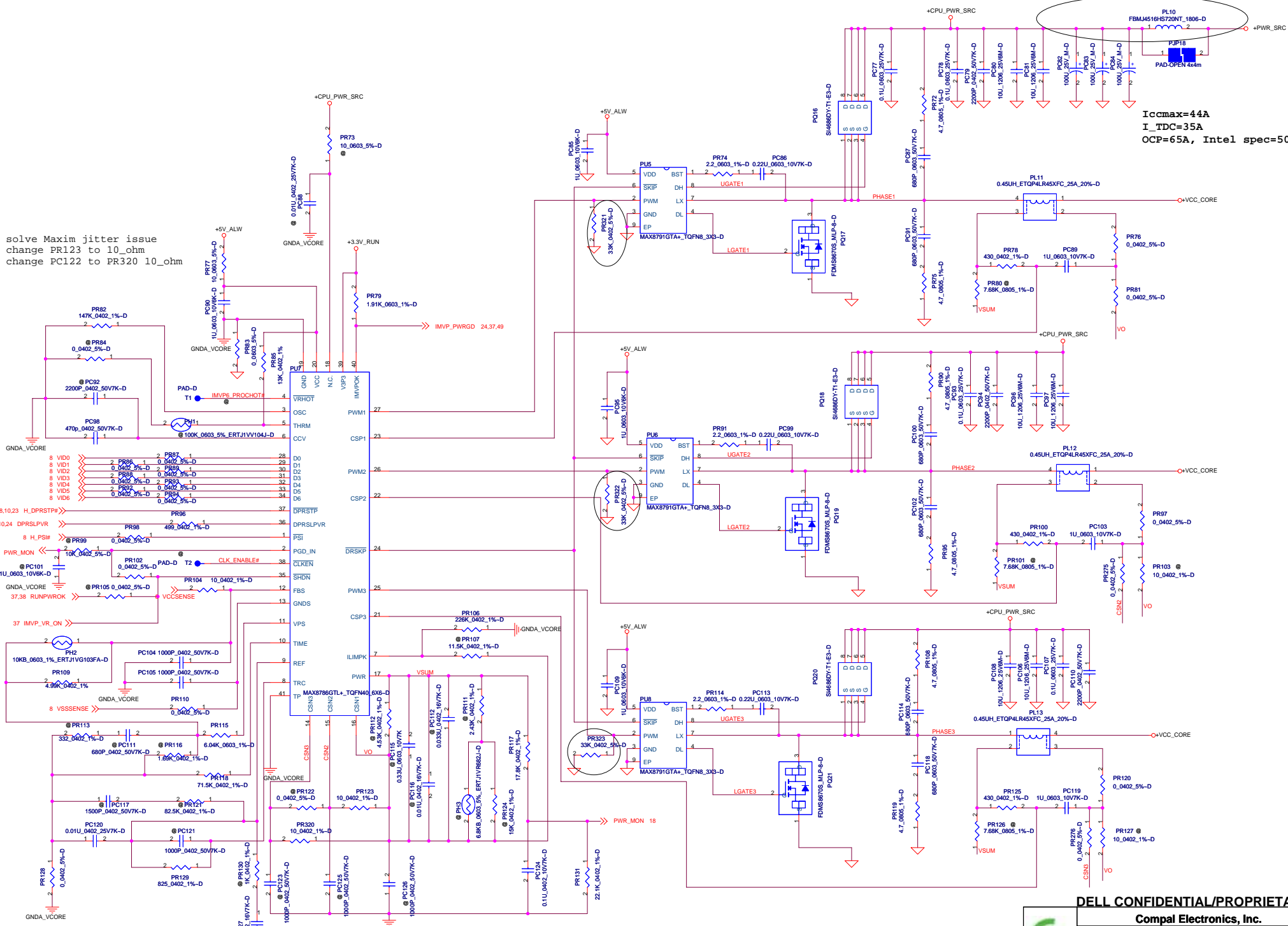
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solve Maxim jitter issue
change PR123 to 10_ohm
change PC122 to PR320 10_ohm



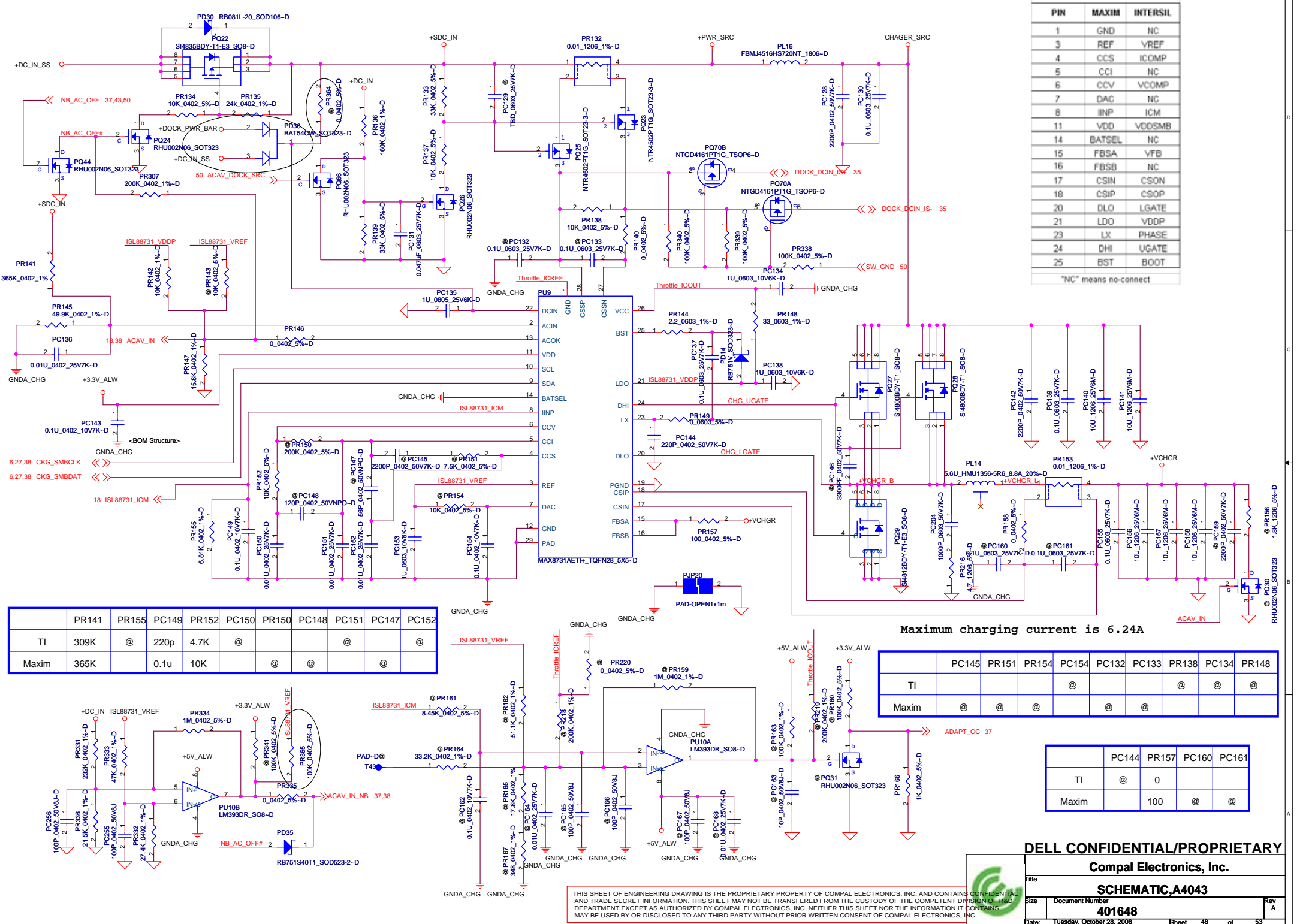
Iccmax=44A
I_TDC=35A
OCP=65A, Intel spec=50A

- 8 VID0
- 8 VID1
- 8 VID2
- 8 VID3
- 8 VID4
- 8 VID5
- 8 VID6
- 8.10.23 H_DPRSTP#
- 10.24 DPRSLPVR
- 8 H_PSI#
- 18 PWR_MON
- 1U_0603_10V8K-D
- 37.38 RUNPWROK
- 37 IMVP_VR_ON
- 8 VSSSENSE
- PR113
- PCV11
- PR116
- PR117
- PC117
- PR118
- PR119
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TABLE 3. PIN NAME DIFFERENCES

PIN	MAXIM	INTERSIL
1	GND	NC
3	REF	VREF
4	CCS	ICOMP
5	CCI	NC
6	CCV	VCOMP
7	DAC	NC
8	IINP	ICM
11	VDD	VDDSMR
14	BATSEL	NC
15	FBSA	VFB
16	FBSB	NC
17	CSIN	CSOP
18	CSIP	CSOP
20	DLO	LGATE
21	LDO	VDDP
23	LX	PHASE
24	DHI	UGATE
25	BST	BOOT

"NC" means no-connect



	PR141	PR155	PC149	PR152	PC150	PR150	PC148	PC151	PC147	PC152
TI	309K	@	220p	4.7K	@	@	@	@	@	@
Maxim	365K		0.1u	10K						

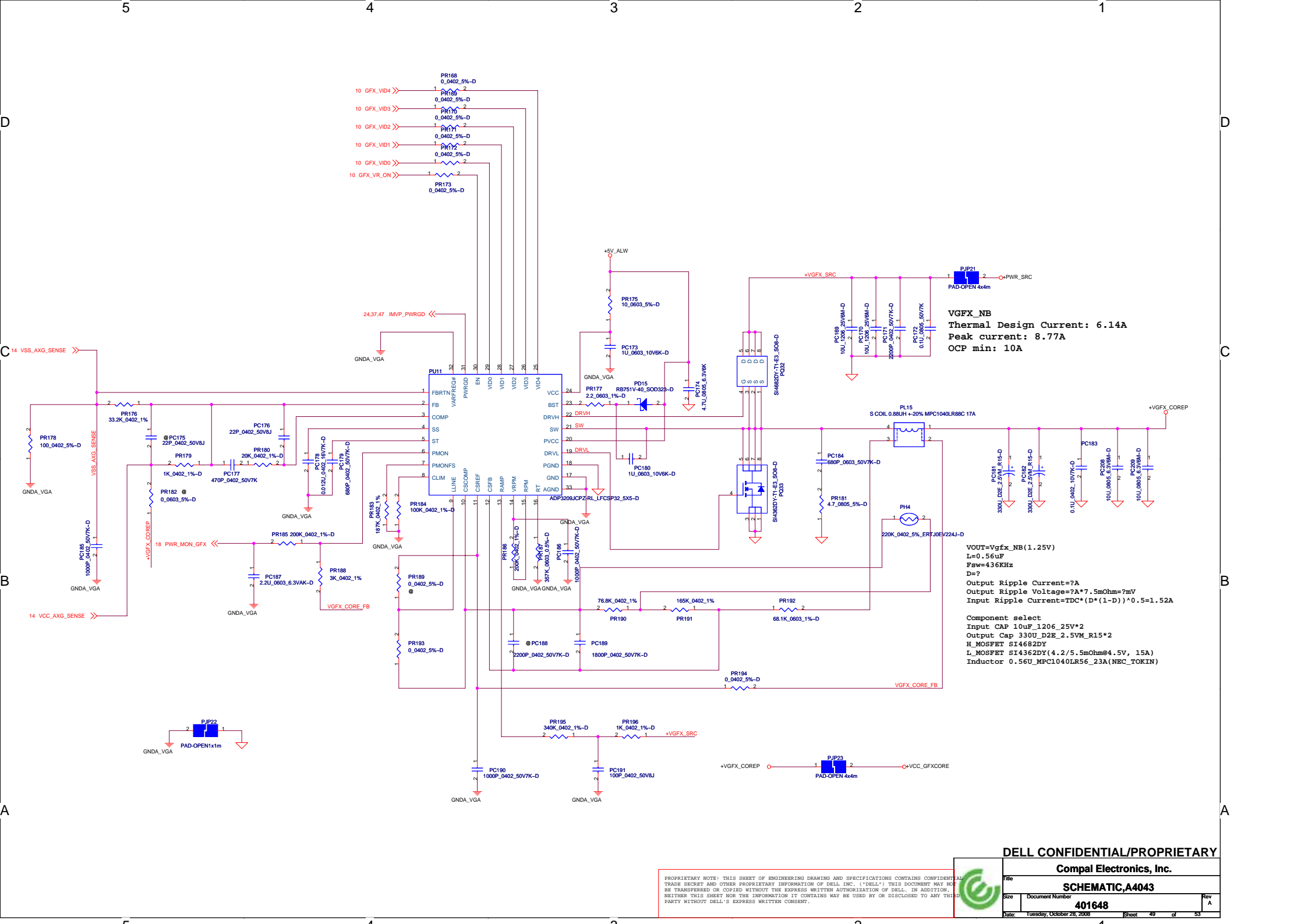
Maximum charging current is 6.24A

	PC145	PR151	PR154	PC154	PC132	PC133	PR138	PC134	PR148
TI	@	@	@	@	@	@	@	@	@
Maxim	@	@	@	@	@	@	@	@	@

	PC144	PR157	PC160	PC161
TI	@	0	@	@
Maxim	100	@	@	@

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VGFX_NB
 Thermal Design Current: 6.14A
 Peak current: 8.77A
 OCP min: 10A

VOUT=Vgfx_NB(1.25V)
 L=0.56uF
 Fsw=436KHz
 D=?
 Output Ripple Current=?A
 Output Ripple Voltage=?A*7.5mOhm=?mV
 Input Ripple Current=TDC*(D*(1-D))^0.5=1.52A

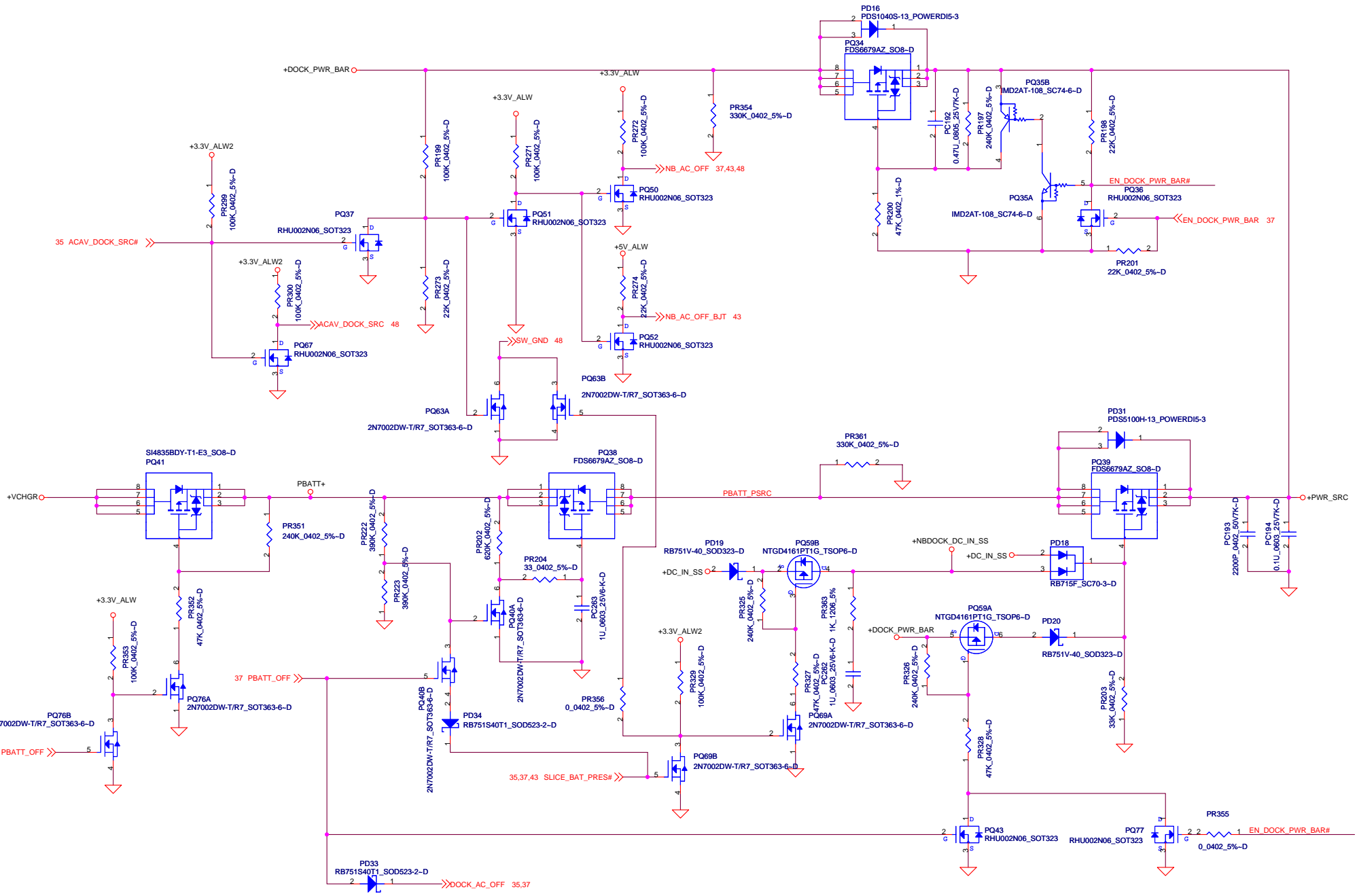
Component select
 Input CAP 10uF_1206_25V*2
 Output Cap 330U_D2E_2.5VM_R15*2
 H_MOSFET SI4682DY
 L_MOSFET SI4362DY(4.2/5.5mOhm@4.5V, 15A)
 Inductor 0.56U_MPC1040LR56_23A(NBC_TOKIN)

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	10	MCH HDA	09/23/2008	Compal	Support 1.5V MDC module. Delete bi-derectional level shift circuit.	Delete U67 and enable circuit, delete R42, R44, R686, R687 and change R685 to 33ohm.	X00
2	10	MCH	09/23/2008	Compal	Eliminate Power Sequence circuit, ICH_PWRGD change to RESET_OUT	Change U2.AT40 (Cantiga PWROK) to RESET_OUT	X00
3	18	Thermal	09/23/2008	Compal	Eliminate 2.5V_RUN_PWRGD. System do not use +2.5V_RUN power plan.	Delete U3 Pin 34 (4002 LDO_POK).	X00
4	24	ICH	09/23/2008	Compal	Eliminate Power Sequence circuit, ICH_PWRGD change to RESET_OUT	Change U10.G20 (ICH9M PWROK) to RESET_OUT	X00
5	25	MDC	09/23/2008	Compal	Support 1.5V MDC module. Delete bi-derectional level shift circuit.	Delete R314 R315, change +3.3V/1.5V_RUN_HDA to +1.5V_RUN, add U79 RICHTEK RT9013-15PB SOT23-5 to transfer +3.3V_ALW to +1.5V_ALW_HDA	X00
6	38	EC	09/23/2008	Compal	Eliminate Power Sequence circuit. RUNPWROK, SUSPWROK, 3.3V_M_PWRGD,3.3V_LAN_PWRGD become floating.	RUNPWROK add R1131 10K and pull high to +3.3V_RUN SUSPWROK add R1132 10K and pull high to +3.3V_SUS 3.3V_M_PWRGD add R1133 10K and pull high to +3.3V_M 3.3V_LAN_PWRGD add R1134 10K and pull high to +3.3V_LAN	X00
7	37	SIO	09/23/2008	Compal	Delete sniffer yellow circuit	Delete U35 Pin 10 sniffer yellow since don't used yellow LED.	X00
8	37	SIO	09/23/2008	Compal	Eliminate Power Sequence circuit, 2.5V_RUN_PWRGD change to 1.8V_RUN_PWRGD.	Change U3.34 (LDO_POK) and U35.18 to 1.8V_RUN_PWRGD.	X00
9	34	Mini Card	09/25/2008	Dell	By Dell comment , remove SM bus circuit of Mini card.To reach cost down.	Remove R429 R430 Q48 R433 R434 Q49.	X00
10	21	Display Port	09/25/2008	Compal	Change DP switch to Pericom PI2VDP8100.	Change U9 to PI2VDP8100, delete switch on mother board side (U75, U76 and circuit around).	X00
11	33	ESATA	09/25/2008	Compal	For cost down consideration.Change cheaper ESATA reapter.	Change ESATA reapter from SA00002D80L to SA00002YQ0L.	X00
12	38	EC	09/25/2008	Compal	Follow MINICOOPER named RESET_OUT# as RESET_OUT	Rename RESET_OUT# to RESET_OUT	X00
13	27	Codec	09/25/2008	Compal	Support 1.5V MDC module. Delete bi-derectional level shift circuit.	Change U16 Pin3 (DVDD_IO) from +3.3V_RUN to +1.5V_RUN.	X00
14	25	ICH	09/26/2008	Compal	Change +1.5V_ALW_HDA source plane.	Change U79 Pin1 to +3.3V_ALW_ICH.	X00
15	33	MDC	09/26/2008	Compal	Support 1.5V MDC module.	Change JI01 Pin 35 from +3.3V_SUS to +3.3V_ALW_ICH. Add Pin 39 +1.5V_ALW_HDA.	X00
16	24	Flash ROM	10/02/2008	Compal	Depop 2nd SPI flash ROM	Depop R214,R387,R386,R1060,R375,R383,C392,R384,U13	X00
17	23	SB	10/02/2008	Compal	For low cost consideration, change Y1 for cheaper crystal.	Change Y1 form 32.768KHZ 12.5PF 1TJE125DP1 to 32.768KHZ 12.5PF 1TJS125DJ2A07	X00
18	36	USH I/F	10/03/2008	Compal	By Broadcom require to reserve location for RFID performance tuning.	Add R1138, R1139,R1140 but depop.	X00
19	33 37	BIO RFID	10/07/2008	Compal	Change connector type	Change JBI01 to TYCO_2041070-6_6P-T. Chnage JCS1 to TYCO_2041084-6_6P-T	X00
20	34	SIM CARD	09/23/2008	Compal	Change SIM card slot.	Change JSIM1 to cost down SIM slot LTCX000EZ0L (TEMP: SP070711300)	X00

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	43	+DC_IN	11/17	leverage Roush	Battery slice need detect NB battery is insert or not.	Add PQ61 NTR4502PT1G, and PD32 RB751_SOD323 Connect to DOCK_SMB_ALERT# and SLICE_BAT_PRES#	X01
2	43	+DC_IN	11/17	leverage Roush	DCIN_CBL_DET# damage ECE5028	Add ESD diode PD17 DA204U_SOT323 at DCIN_CBL_DET# Series PR221 1K_0402_5% between PJPDC1, PIN1 and DCIN_CBL_DET# Parallel PC254 0.47uF_0402_6.3V on DCIN_CBL_DET#	X01
3	43	+DC_IN	11/17	leverage Roush	Roush component and rework changes for Dcoking test	PC4 change form 0.47uF_0805_25V to 0.1uF_0805_25V PR14 change form 240K_0402_5% to 1M_0402_5% PR17 change form 47K_0402_1% to 220K_0402_5% PR18 change form 47K_0402_1% to 22K_0402_5% PR342 change form 0_0402_1% to 100K_0402_5%	X01
4	48	Charger	11/17	leverage Roush	NB DC blocking MOSFET won't turn off when Dock AC insert.	Add PQ44 RHU002N06 control NB DC blocking MOSFET. Control signal is NB_AC_OFF Series PR284 200K_0402_1% between PQ44 PIN1 and ACAV_IN Add PD30 B540C parallel PQ34	X01
5	48	Charger	11/17	leverage Roush	Charger of ISL88731 will turn off When ACIN is no power	Add LM393 to replace ISL88731 ACOK function(PU11B)	X01
6	48 50	Charger Selector	11/17	leverage Roush	+PWR_SRC exist on Docking connector through the DOCK_DCIN_IS+ and -	Add PQ62 NTGD4161PT1G series DOCK_DCIN_IS+ and - Add PQ63 RHU002N06 to control PQ62 on/off	X01
7	48 50	Charger Selector	11/17	leverage Roush	A global signal name change for all notebooks	From "ACAV_IN_DOCK" to "ACAV_DOCK_SRC" From "ACAV_IN_DOCK#" to "ACAV_DOCK_SRC#"	X01
8	48	Charger	11/17	leverage Roush	SCH165050: Validate EMC4002 VIN1/VCP1/VCP2 for UMA & Discrete for PT1 SMT	Depop UL circuit.	X01
9	50	Selector	11/17	leverage Roush	PBATT DC blocking MOSFET won't turn off when Docking AC insert. It will cause Battery or adapter protect.	Add PD18 RB715F_SOT323, PD20 and PD19 RB751V_SOD323, PR329 100K_0402_5% PR328 and PR327 47K_0402_5%, PR326 and PR325 240K_0402_5% PQ69 2N7002DW-7-F_SOT363-6, PQ59 NTG6161PT1G_TSOP6 Extra net name add +NBDock_DC_IN_SS from Docking connector	X01
10	43	+DCIN	11/20	EE / SCH165224	follow HW change	To delete the RTC detection circuit	X01
11	48 50	Selector charger	11/30	Dell	for slice function implement	change charger output to FB pin15 net name from PBATT+ to +VCHGR Add PQ41 PQ70 PR351 PR352 PR353 between +VCHGR and PBATT+	X01
12	43	+DCIN	12/17	Dell	change DCIN connector for ESD issue of "DCIN_CBL_DET#"	from Molex_87437_0663 to MOLEX_87437-0763	X02
13	50	Selector	12/28	leverage Roush	follow Roush	change PQ63 from RHU002N06 to 2N7002DW ADD PD33 RB751V ADD PR354 ADD PQ77 RHU002N06 and PR355 0 ohm	X02
14	48	Charger	12/28	leverage Roush	follow Roush	Change PC131 from TBD to 0.047uF	X02

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
15	47	+Vcore	02/18	Dell / Maxim	Reduce Ring-backwithin 20mV when change bulk caps from 4*220uF to 3*270uF	PR129 change from 909 ohm to 825 ohm	
16	50	Selector	02/18	Merle DELL	Fix BITS CR196131 and CR196130	Add PR363 1K_1206 and PC262 1U_0603_25V from +NBDOCK_DC_IN_SS to ground Add PD35 RB751S40T1_SOD523-2 from NB_AC_OFF# to ACAV_IN_NB	
17	47	+Vcore	02/18	Maxim	Fix Jitter issue	change PR123 to 10_ohm change PC122 to PR320 10_ohm	
18	48/50	charger / selector	02/26	Compal	location change for Charger 2nd source X76 BOM control	change PR141 to PR217 change PR217 to PR141 change PR228 to PR218 change PR218 to PR351 change PR230 to PR219 change PR219 to PR352 change PR229 to PR220 change PR220 to PR353 change PR284 to PR307 change PQ62 to PQ70 change PQ70 to PQ76	
19	48	Charger	03/06	Compal	Delete non-use circuit	delete +DC_IN_SS to PR217 and PR217.	
20	50	Selector	03/06	Compal	For slice battery hot docking issue	Change PQ40 from IMD2AT to 2N7002DW change PR202 from240K_ohm ot 620k_ohm change PR204 from 47K_ohm to 33_ohm add PR222 390K_ohm and PR223 390K_ohm add PD34 RB751S40T1	
21	47	+Vcore	03/11	Maxim	For driver IC power down issue	Add PR321 PR322 PR323 from IC pin 2 to GND	
22	44-50	All	03/19	Compal	EMI solution	Change PR32 PR33 PR57 PR58 PR64 PR74 PR91 PR144 PR177 to 2.2_ohm Add PC198 PR211 PC199 PR212 PC200 PR213 PC201 PR214 PC202 PR215 PC87 PR72 PC91 PR75 PC100 PR90 PC102 PR95 PC114 PR108 PC118 PR119 PC204 PR216 PC184 PR181 PC128 PC130	
23	45	1.5V/1.05v	4/23	Compal	change non-lead free part to lead free part	PR47 change from SD03415830L to SD03415838L	
24	47	Vcore	4/23	Maxim	Driver IC power down issue need change resistor value	change PR321 PR322 PR323 to 33K	
25	49	ADP3209	4/23	Intel Compal	Follow Roush VGFY DC load line slope change to -7.5mOhm	Change PR192 from 75K_0603 to 68.1K_0603	
26	43	DC-IN	6/3	Compal	Glitch issue on SLICE_BAT_PRES#	Add PC257:SE074152K8L(S CER CAP 1500P 50V +-10% X7R 0402) between pin2 of PQ61 and GND.	
27	50	Selector	6/4	Compal	Reserve a pull high resistor between +3.3V_ALW2 and SLICE_BAT_PRES#	Add un-pop PR330:SD02847018L(S RES 1/16W 4.7K +-5% 0402) between +3.3V_ALW2 and PQ40B.5.	
28	48	Charger	9/11	Dell	reduce charger IC power consumption when battery mode	Add location PD36, PR364, PR365. Pop PD36 PR365. Un-pop PR364	
29	48	Charger	9/11	Dell / Compal	De-pop UL circuit	De-pop PR161 PR162 PR220 PR159 PR163 PR160 PC162 PR165 PR167 PC164 PC165 PC166 PC167 PC168 PC163 PQ31 Pop PR166	
30	48	Charger	10/22	Dell	using Guardian for UL compliance need to change PR155	change PR155 from 8.45K to 6.81K	