COMPAL CONFIDENTIAL

MODEL NAME : *NCL01*

PCB NO : *LA-5472P (DAA00001I00)*

E2 Rothschild DSC

rPGA Arrandale +
FCBGA PCH IBEXPEAK-M
+ N10M-NS-S

2010-01-20

REV : 1.0(A00)

@ : Nopop Component

MB Type	BOM P/N	PCMCIA	Express	TCM		TPM				ATG	BOM CONFIG
		1@	2@	W(3@)	W/O(4@)	W(5@)	W/O(6@)	7@	8@	9@	
EXPRESS CARD ,Enble TPM ,Disable TCM	43177831L01		*		*	*					2@,4@,5@
EXPRESS CARD ,Disable TPM ,Enble TCM	43177831L02		*	*			*				2@,3@,6@
EXPRESS CARD ,Disable TPM ,Disable TCM	43177831L03		*		*		*				2@,4@,6@
PCMCIA CARD ,Enble TPM ,Disable TCM	43177831L04	*			*	*					1@,4@,5@
PCMCIA CARD ,Disable TPM ,Enble TCM	43177831L05	*		*			*				1@,3@,6@
PCMCIA CARD ,Disable TPM ,Disable TCM	43177831L06	*			*		*				1@,4@,6@

MB PCB

Part Number	Description
DAZ0AZ00100	PCB NCL01 LA-5472P LS-5471P/5473P/5574P

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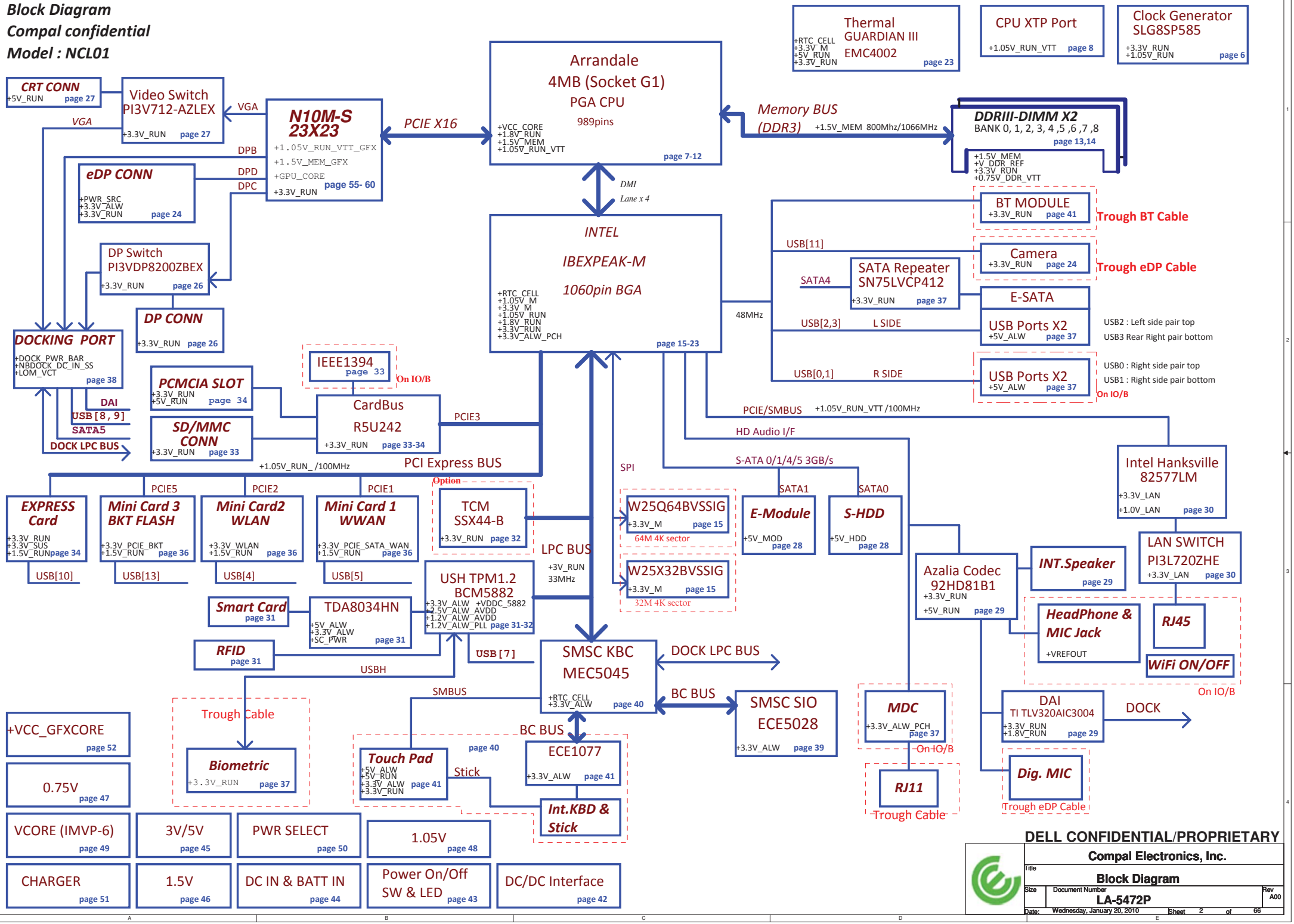
Compal Electronics, Inc.

Title: Cover Sheet

Size | Document Number: LA-5472P | Rev: A00

Date: Wednesday, January 20, 2010 | Sheet 1 of 66

Block Diagram
Compal confidential
Model : NCL01



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Title	Block Diagram	
Size	Document Number LA-5472P	Rev A00
Date: Wednesday, January 20, 2010	Sheet 2 of 66	

POWER STATES

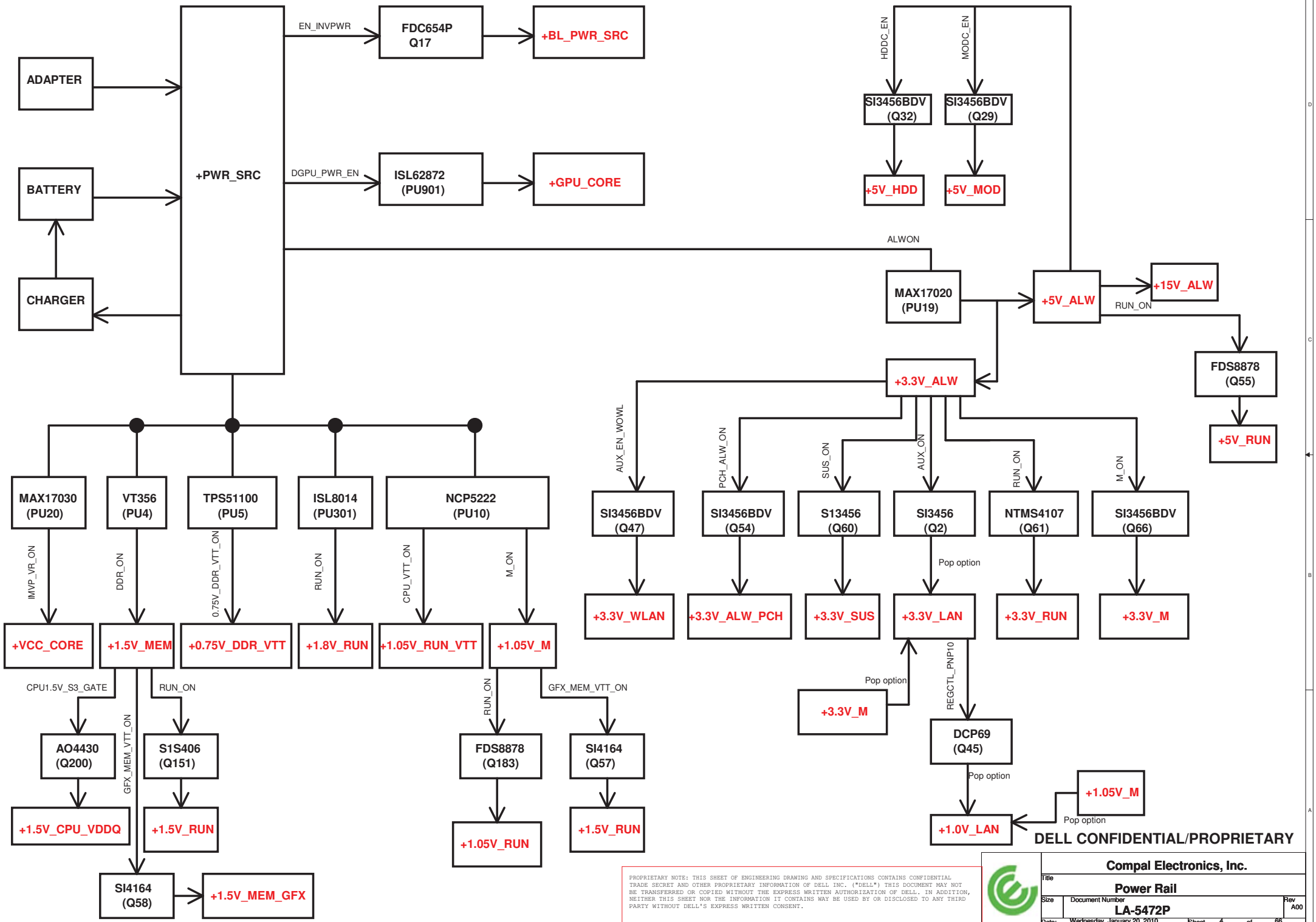
State \ Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M1	LOW	LOW	HIGH	LOW	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M1	LOW	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State \ power plane	+15V_ALW +5V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_CORE +1.05V_RUN_VTT +1.05V_RUN	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

PCH	USB PORT#	DESTINATION
	0	JUSB1 (Ext Right Side Top)
	1	JUSB1 (Ext Right Side Bottom)
	2	JESA1 (Ext Left Side Top)
	3	JESA1 (Ext Left Side Bottom)
	4	WLAN
	5	WWAN
	6	Bluetooth
	7	USH->BIO
	8	DOCKING
	9	DOCKING
	10	Express card
	11	Camera
	12	none
	13	JMINI3(PCIE/BKT CARD)

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	PCMCIA
Lane 4	EXPRESS CARD
Lane 5	MINI CARD-3 PCIE/BKT
Lane 6	10/100/1G LAN
Lane 7	None
Lane 8	None



Compal Electronics, Inc.

Title: Power Rail

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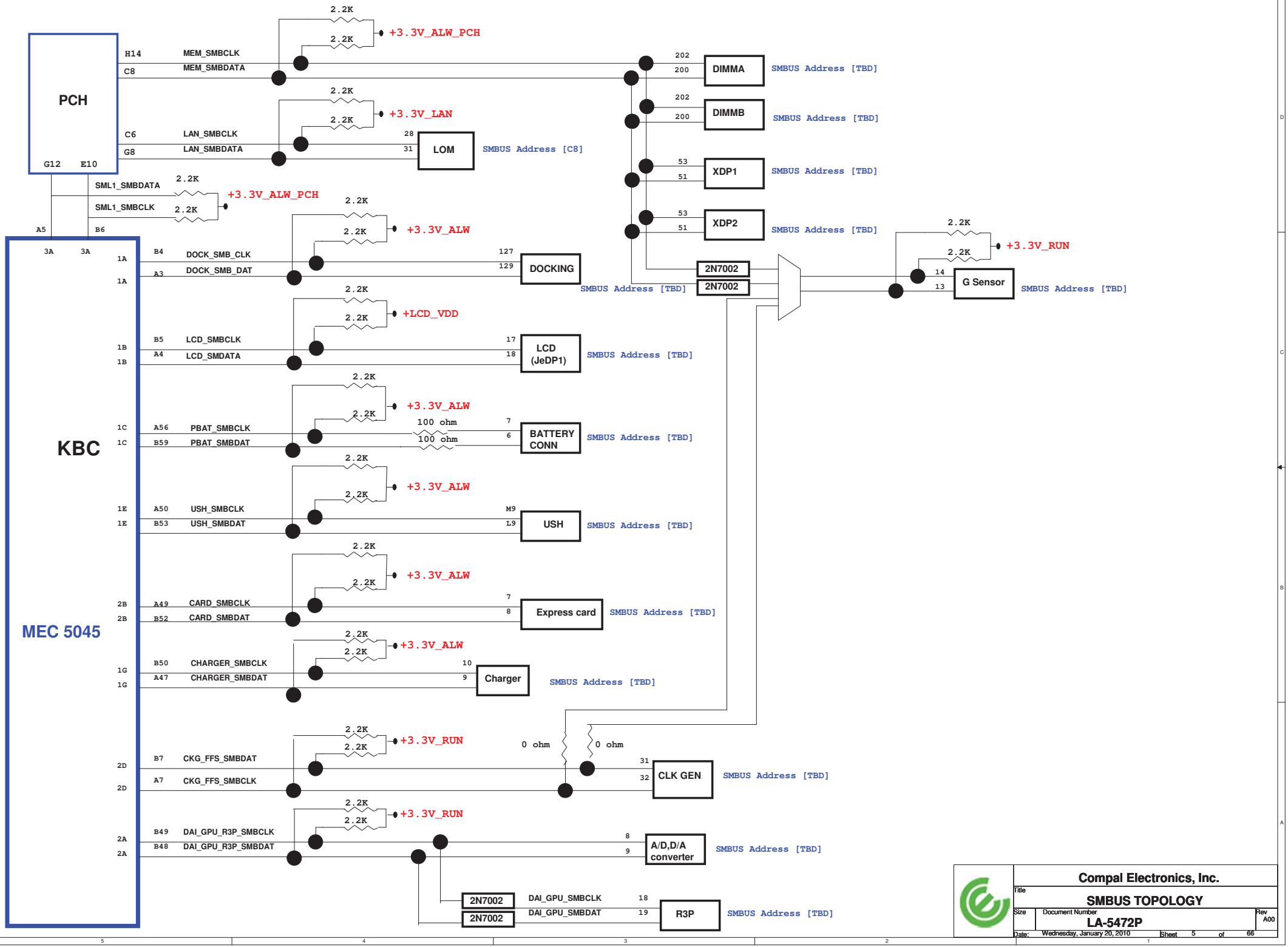
Date: Wednesday, January 20, 2010 | Sheet 4 of 66



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Title	SMBUS TOPOLOGY
Size	Document Number: LA-5472P
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Date:	Wednesday, January 20, 2010
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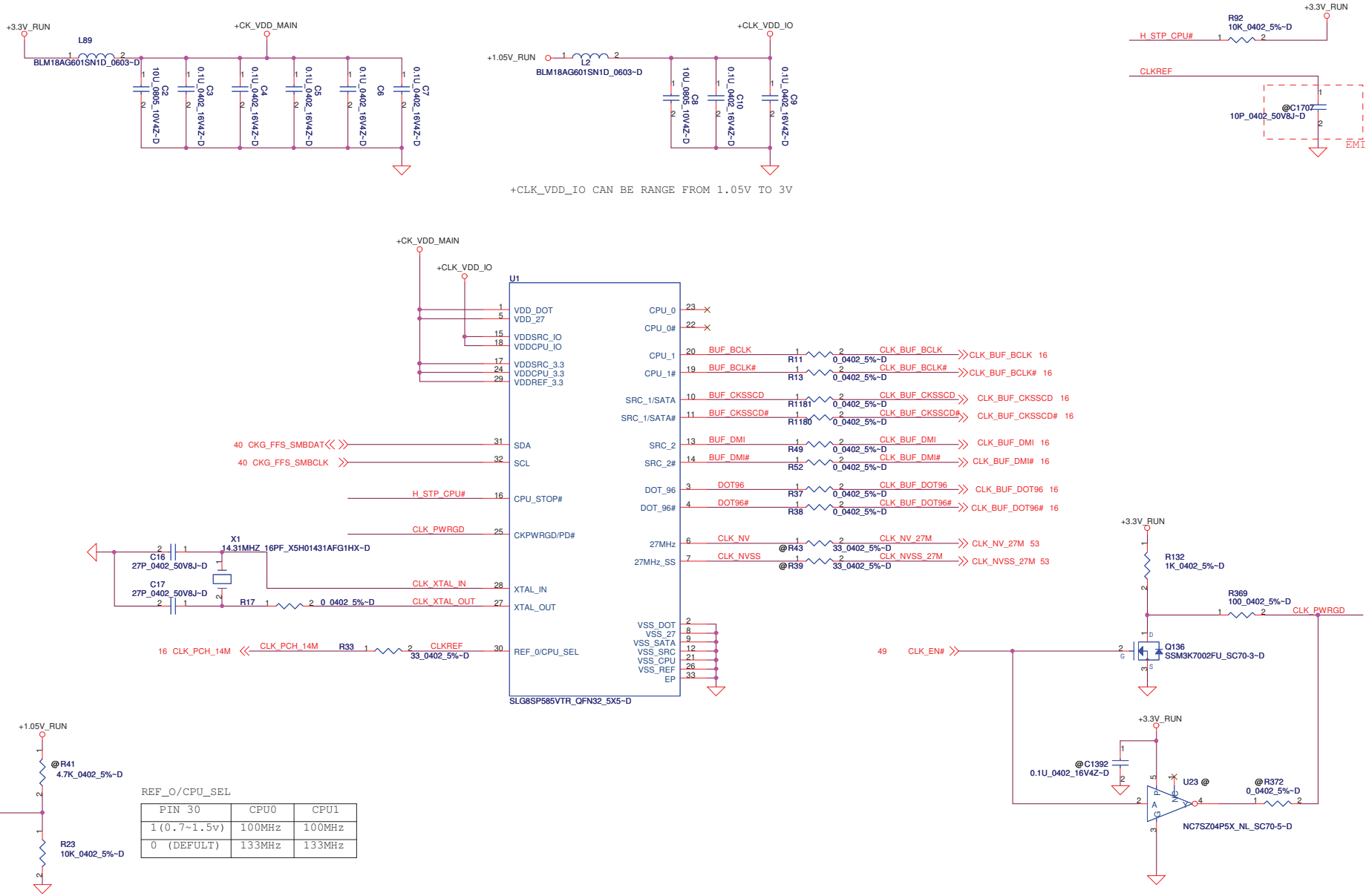

REF_O/CPU_SEL

PIN 30	CPU0	CPU1
1(0.7~1.5v)	100MHz	100MHz
0 (DEFULT)	133MHz	133MHz

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Title: Clock Generator

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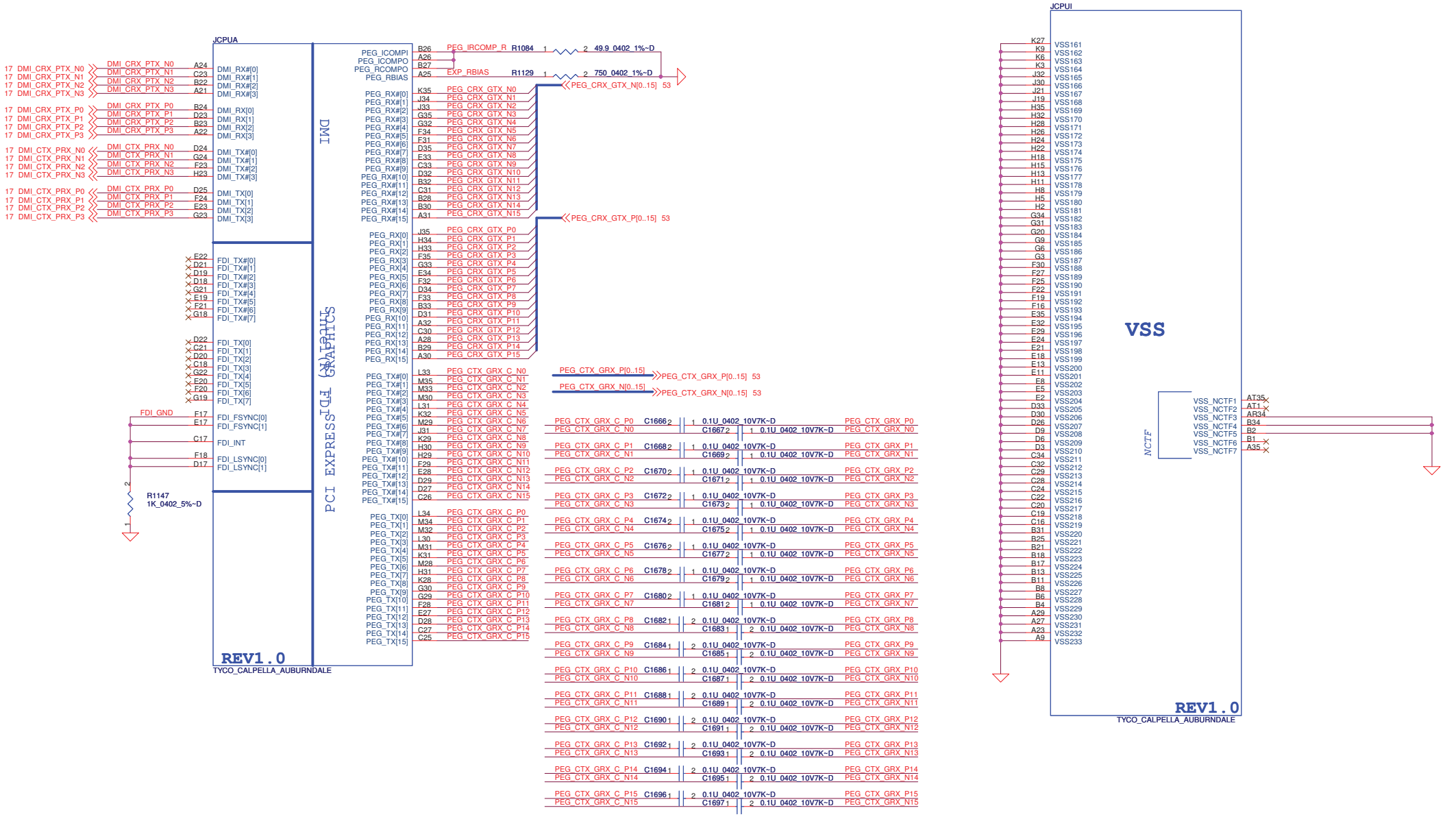
Date: Wednesday, January 20, 2010 | Sheet 6 of 66



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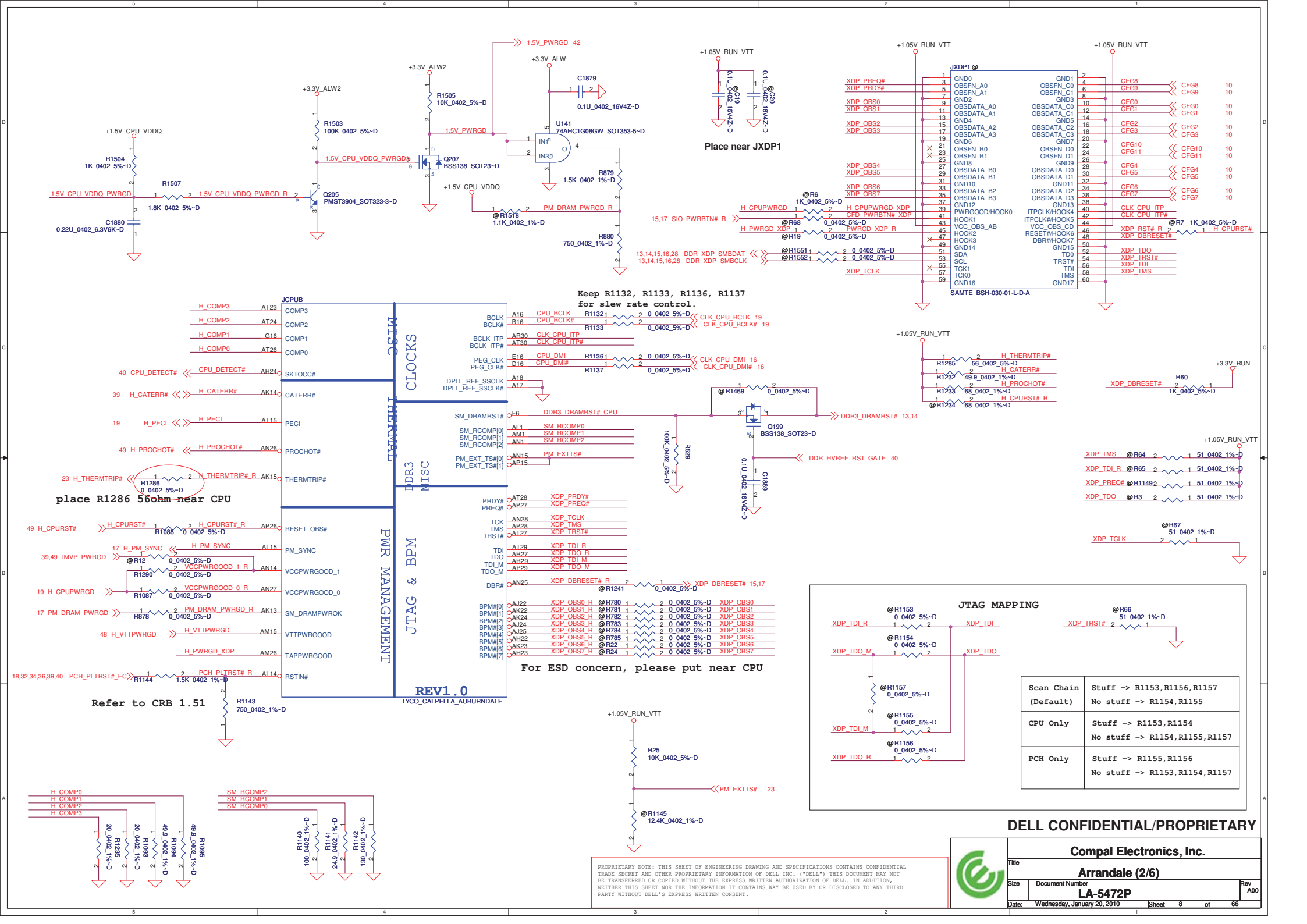
Title: Arrandale (1/6)

Size: | Document Number: LA-5472P | Rev: A00

Date: Wednesday, January 20, 2010 | Sheet 7 of 66


Keep R1132, R1133, R1136, R1137
for slew rate control.
place R1286 56ohm near CPU
Refer to CRB 1.51
For ESD concern, please put near CPU
Place near JXDP1
JTAG MAPPING
Scan Chain (Default) | Stuff -> R1153,R1156,R1157 | No stuff -> R1154,R1155
CPU Only | Stuff -> R1153,R1154 | No stuff -> R1154,R1155,R1157
PCH Only | Stuff -> R1155,R1156 | No stuff -> R1153,R1154,R1157
REV1.0
TYCO_CALPELLA_AUBURNDALE
JCPUB
JXDP1@
SAMTE_BSH-030-01-L-D-A
MISC
THERMAL
CLOCKS
DDR3
MISC
JTAG & BPM
PWR MANAGEMENT
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Title
Arrandale (2/6)
Size
Document Number
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A00
Date: Wednesday, January 20, 2010
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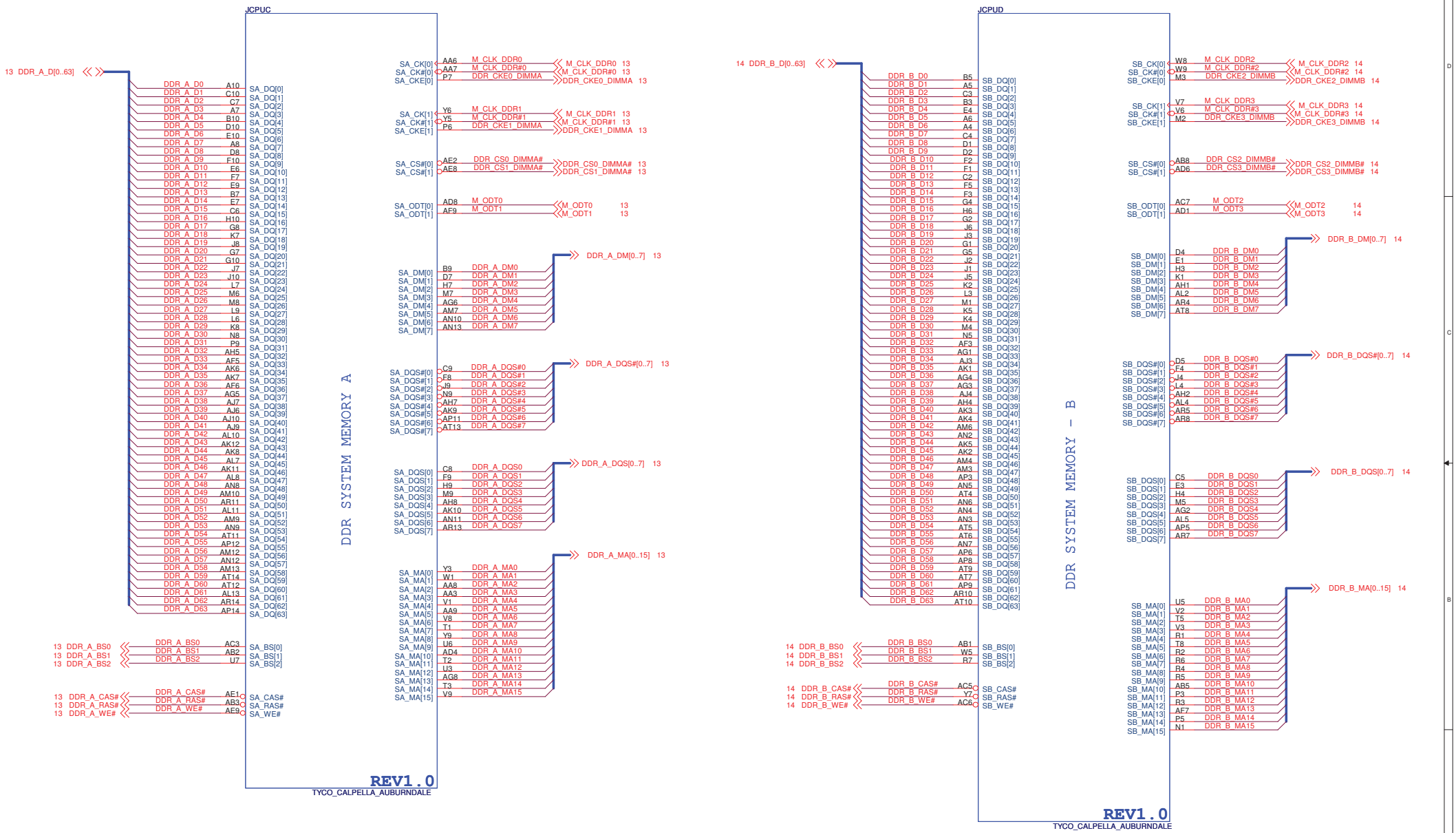

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Title	Arrandale (3/6)
Size	Document Number: LA-5472P
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Date:	Wednesday, January 20, 2010
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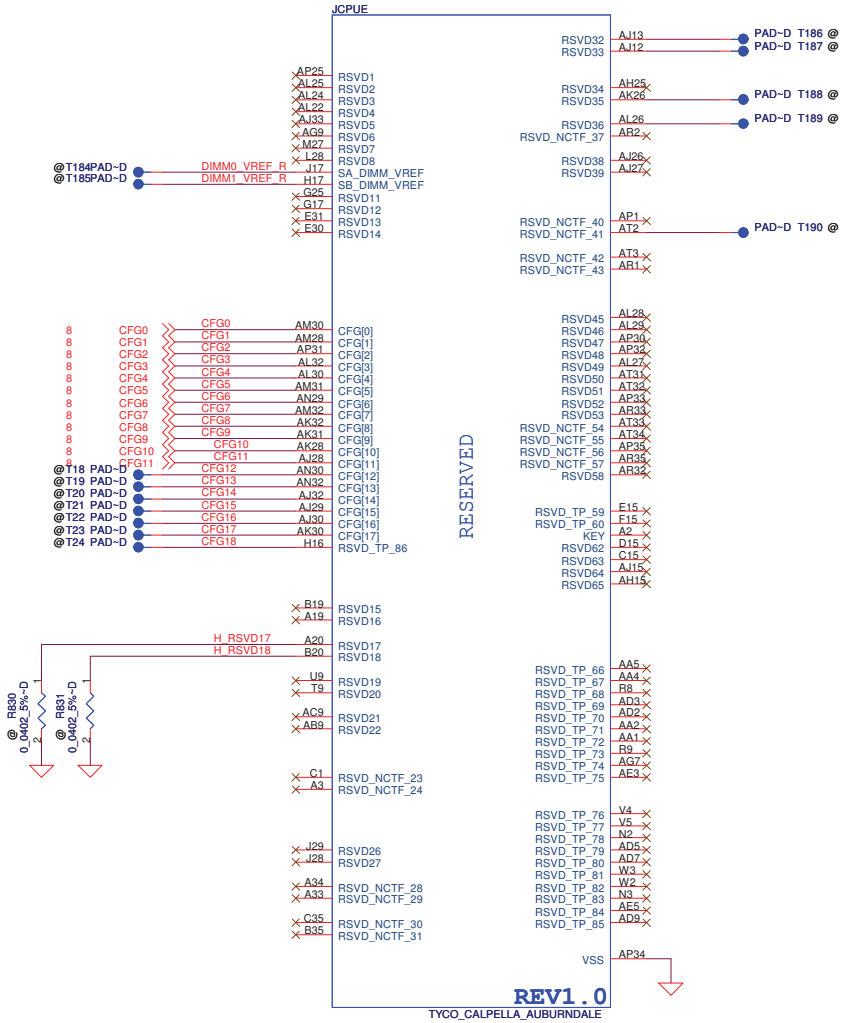
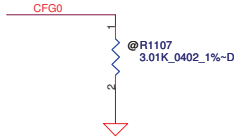
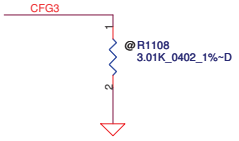
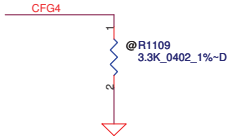




PCI-Express Configuration Select	
CFG0	1 : Single PEG 0 : Bifurcation enable



PCI-Express Static Lane Reversal	
CFG3	1 : Normal Operation 0 : Lane Number Reversed 15->0, 14->1 ...



Display Port Presence	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

Compal Electronics, Inc.

Title: Arrandale (4/6)

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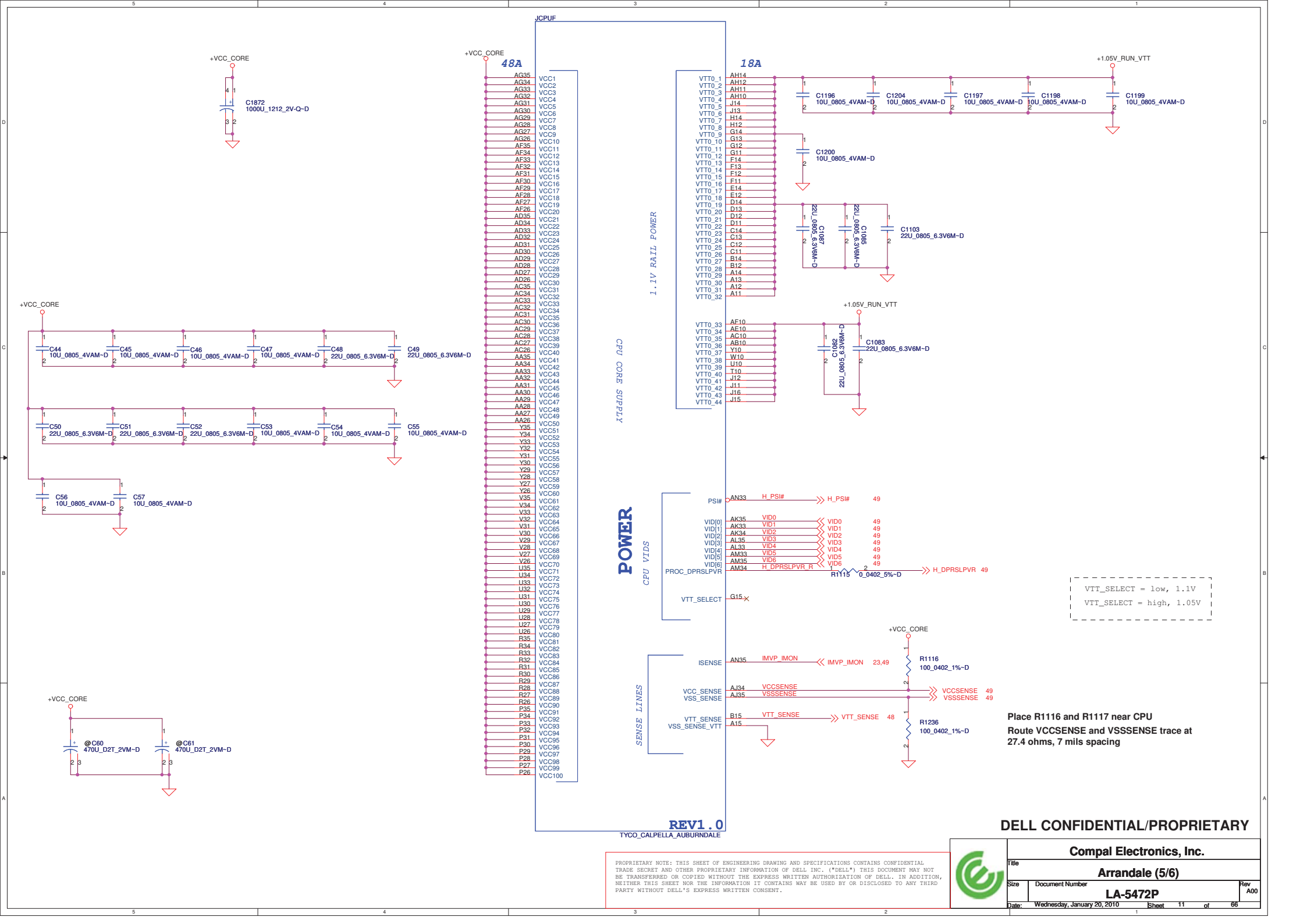
Date: Wednesday, January 20, 2010 | Sheet 10 of 66



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Title: Arrandale (5/6)

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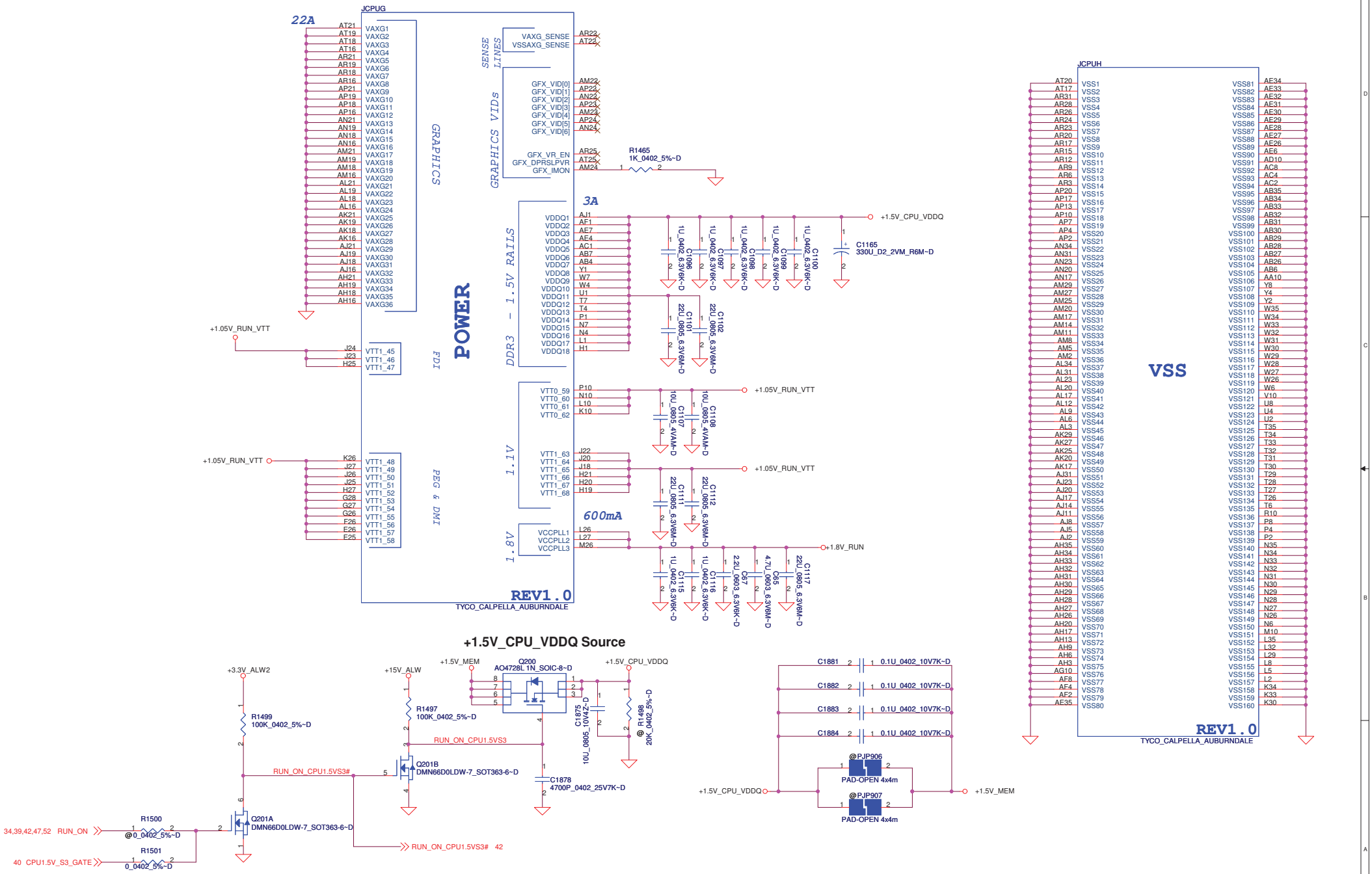
Date: Wednesday, January 20, 2010 | Sheet 11 of 66



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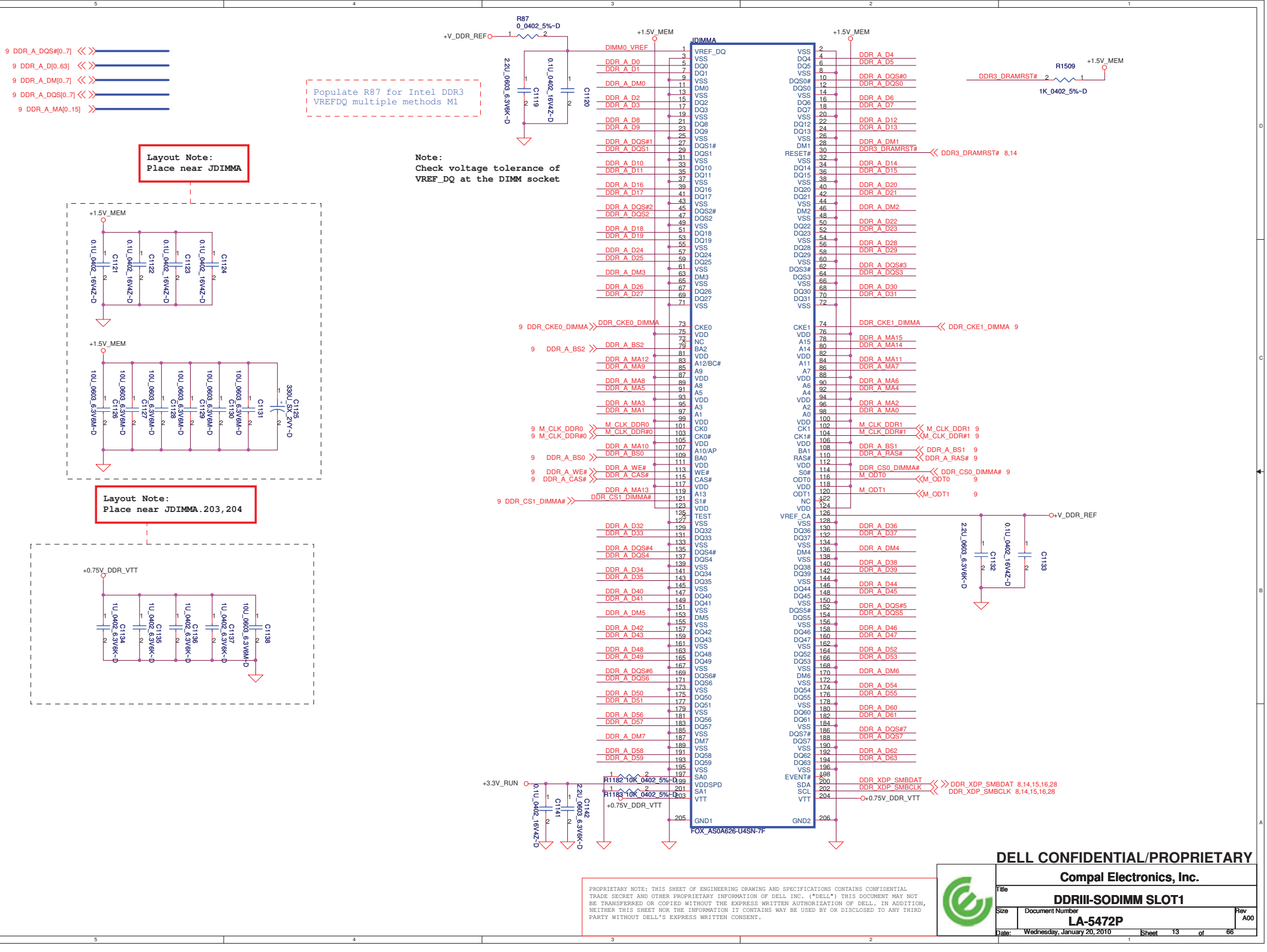
Title: Arrandale (6/6)			
Size	Document Number: LA-5472P		Rev: A00
Date: Wednesday, January 20, 2010	Sheet 12 of 66		

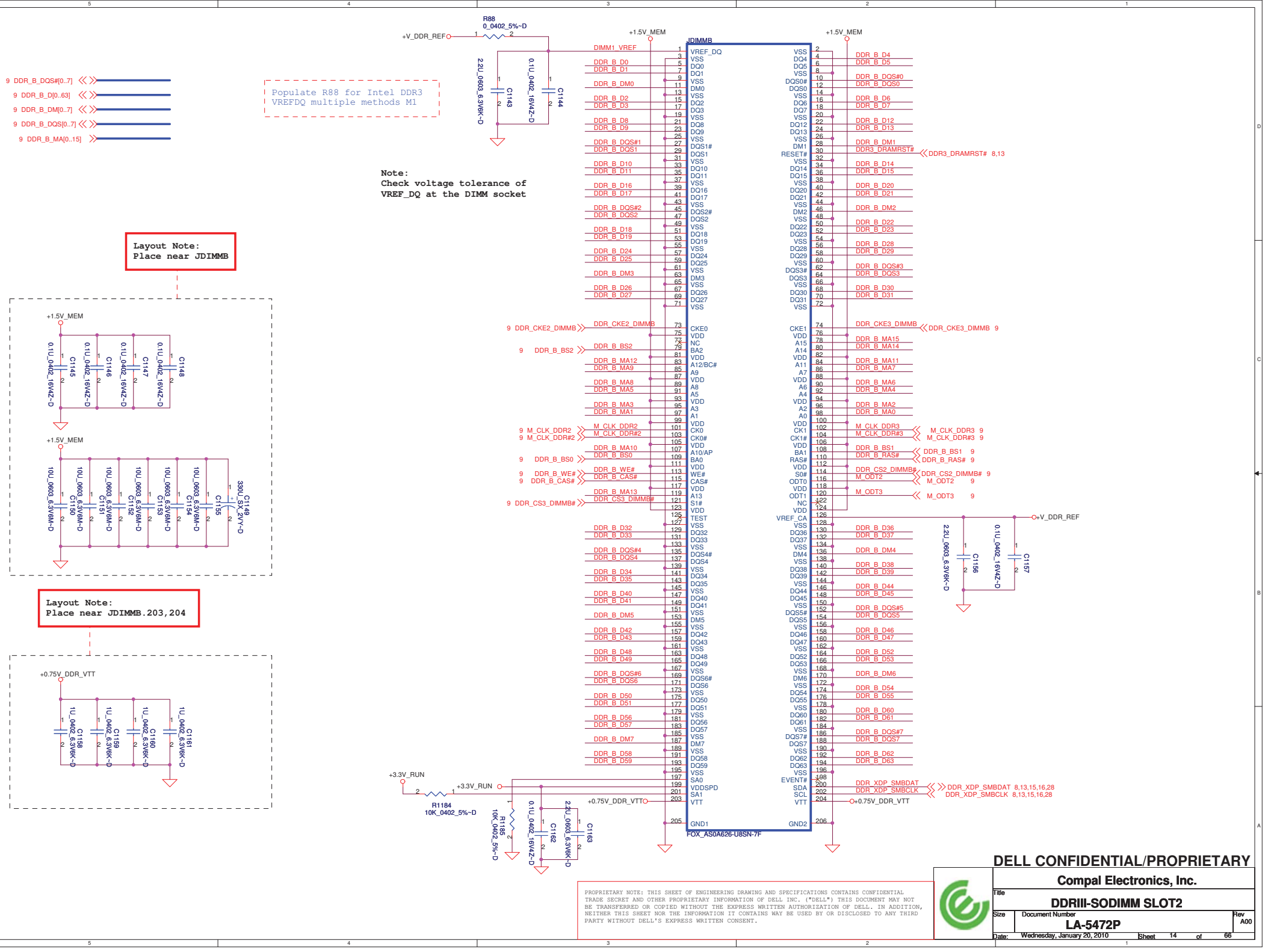


Compal Electronics, Inc.

Title: DDRIII-SODIMM SLOT1

Size | Document Number: LA-5472P | Rev: A00

Date: Wednesday, January 20, 2010 | Sheet 13 of 66



Compal Electronics, Inc.

Title: DDRIII-SODIMM SLOT2

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Date: Wednesday, January 20, 2010 | Sheet 14 of 66

CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

On Die PLL VR is supplied by 1.5V when sampled high, 1.8 V when sampled low

CMOS place near DIMM

200 MIL SO8
64Mb Flash ROM
For iAMT

200 MIL SO8
32Mb Flash ROM

		PCH JTAG Enable		PCH JTAG Disable		Production
PCH Pin	Ref.	ES1	ES2	ES1	ES2	All
TDO	R806	No Stuff	200 ohm	No Stuff	No Stuff	200 ohm
	R1315	No Stuff	100 ohm	No Stuff	No Stuff	100 ohm
TMS	R807	200 ohm	200 ohm	No Stuff	No Stuff	200 ohm
	R1281	100 ohm	100 ohm	No Stuff	No Stuff	100 ohm
TDI	R805	200 ohm	200 ohm	20K ohm	No Stuff	200 ohm
	R1282	100 ohm	100 ohm	10K ohm	No Stuff	100 ohm
TCK	R804	4.7K ohm	4.7K ohm	4.7K ohm	4.7K ohm	51 ohm
TRST#	R808	20K ohm	No Stuff	No Stuff	No Stuff	No Stuff
	R1316	10K ohm	No Stuff	No Stuff	No Stuff	No Stuff

No Reboot Strap	
SPKR	Low = Default
	High = No Reboot

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Title: PCH (1/8)

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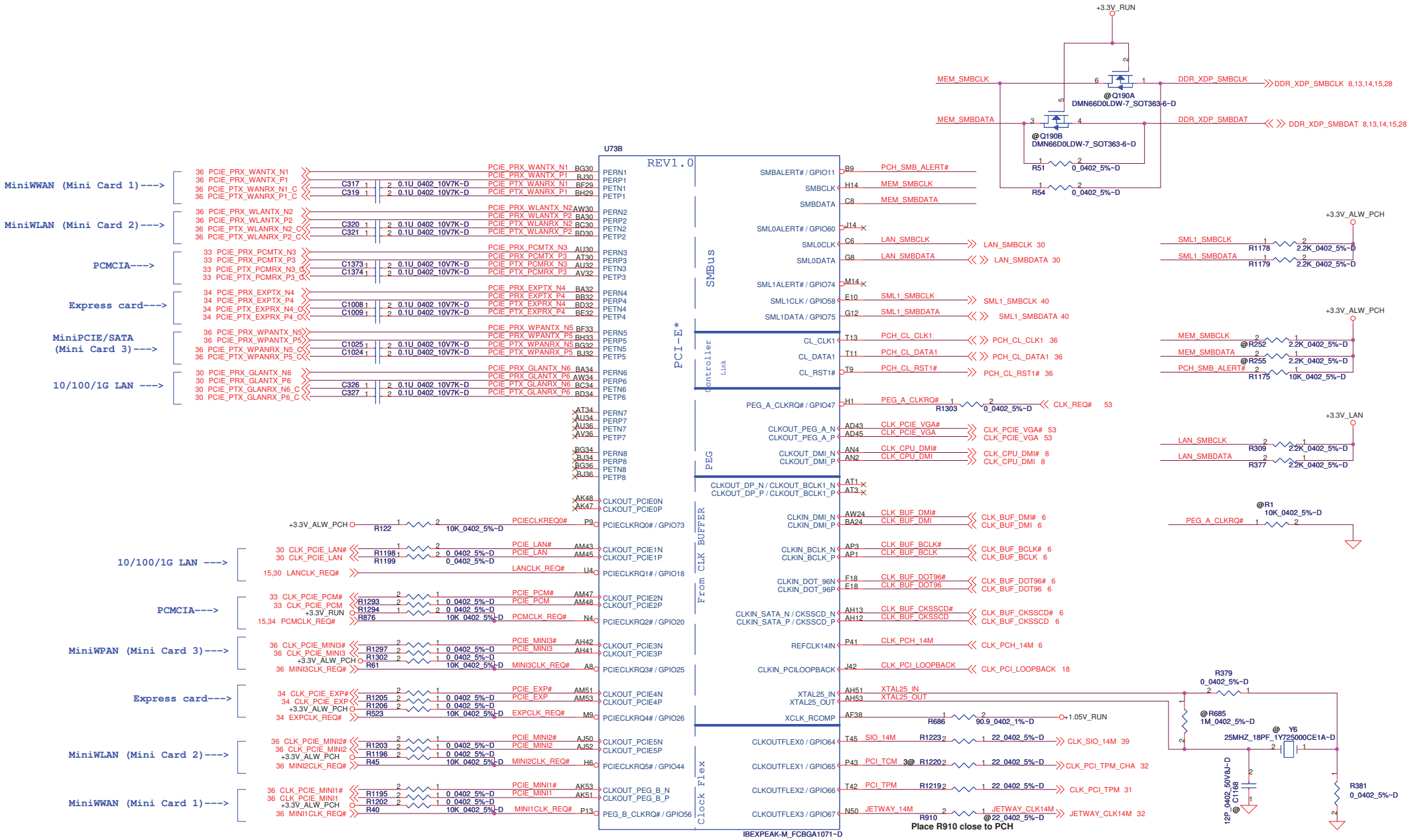

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Title	PCH (2/8)	
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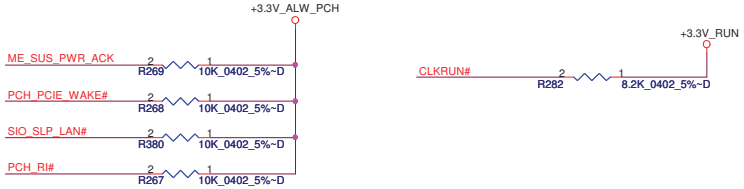
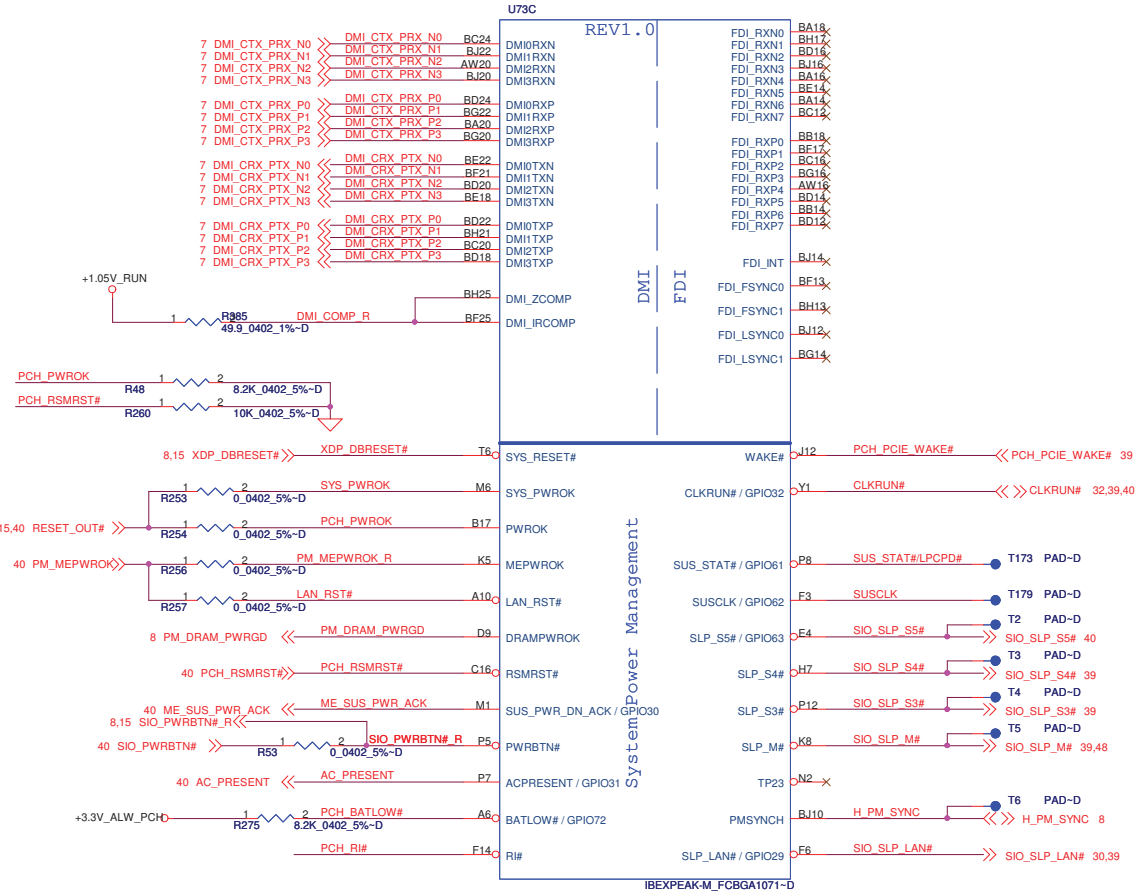
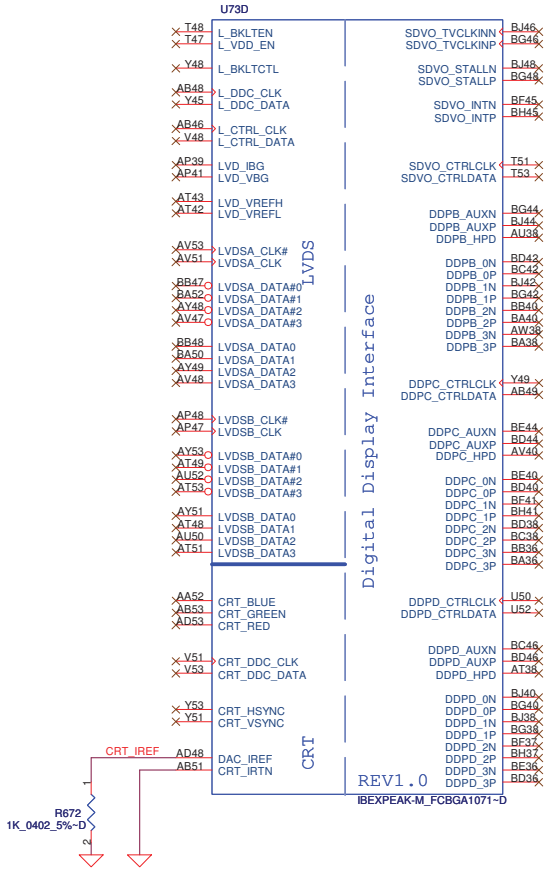
Intel WW18 Strapping option

PORT	STRAP	ENABLE	DISABLE
LVDS	L_DDC_DATA	PU to 3.3V thoough 2.2Kohm	NC
PORT B	SDVO_CTRLDATA	PU to 3.3V thoough 2.2Kohm	NC
PORT B	DDPC_CTRLDATA	PU to 3.3V thoough 2.2Kohm	NC
PORT B	DDPD_CTRLDATA	PU to 3.3V thoough 2.2Kohm	NC
eDP on CPU	CFG[4] (at CPU)	PD to GND thoough 3.3Kohm	NC





Intel request DDPB can not support eDP



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Title: PCH (3/8)

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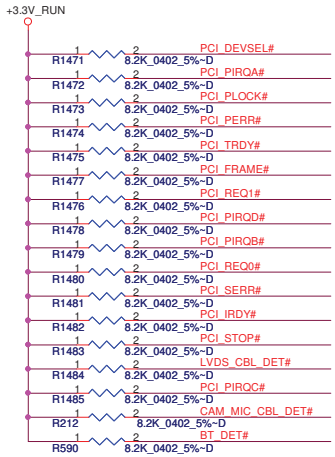
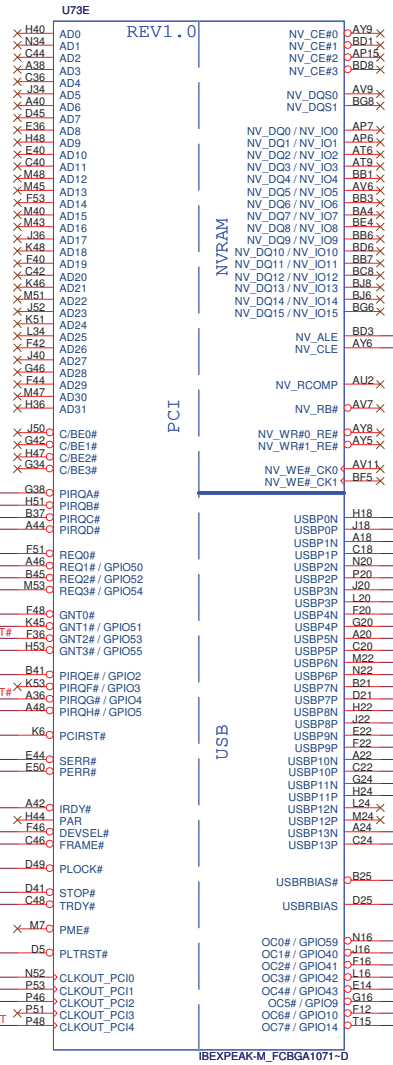
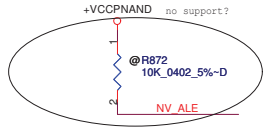
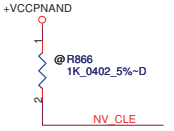
PCH XDP ENABLE	Stuff: R78,R89,R101~R116
	No Stuff: R71,R77,RP1,RP2,R45,R40,R131,R58,R1242,R1243,R1244,R1245,R74,R130
PCH XDP DISABLE	Stuff: R71,R77,RP1,RP2,R45,R40,R131,R58,R1242,R1243,R1244,R1245,R74,R130
	No Stuff: R78,R89,R101~R116







Danbury Technology Enabled	
NV_ALE	High = Enabled (Default) Low = Disabled



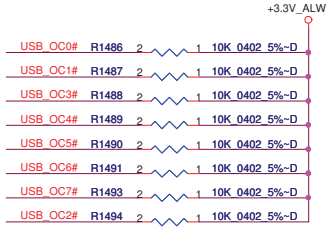
DMI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

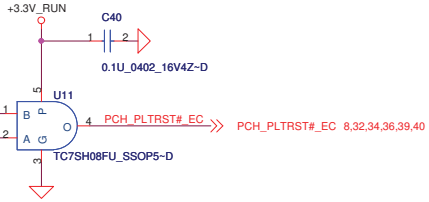
A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap High = Default

----->Right Side Top
----->Right Side Bottom
----->Left Side Top
----->Left Side Bottom
----->WLAN
----->WWAN
----->Blue Tooth
----->BIO_USH
----->DOCK
----->DOCK
----->Express Card
----->Camera

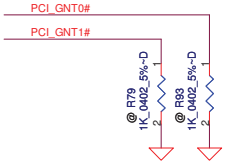
----->WPAN

change base on Rothschild layout concern.





Boot BIOS Strap		
PCI_GNT#1	PCI_GNT#0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI



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Title: PCH (4/8)

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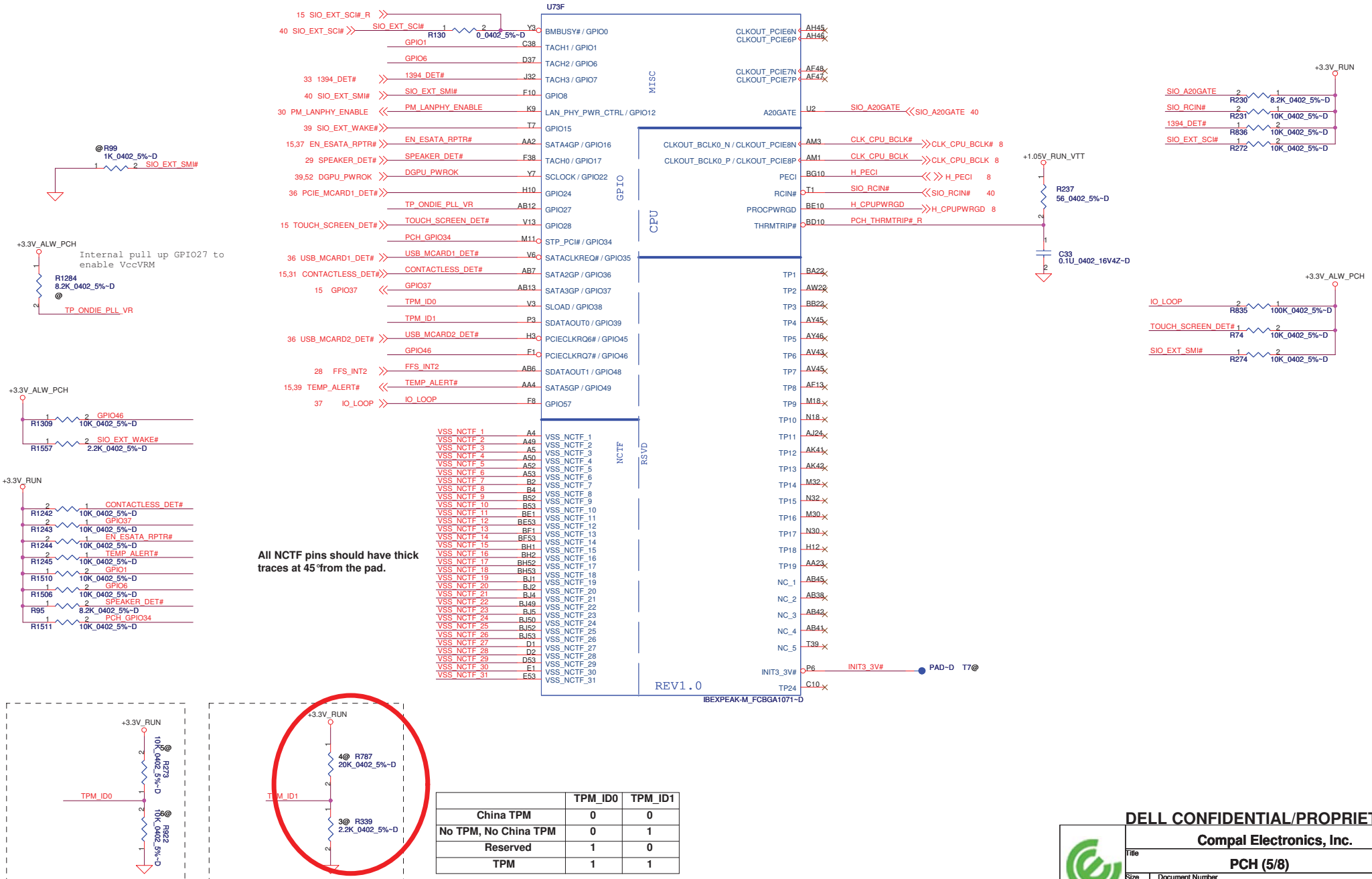

	TPM_ID0	TPM_ID1
China TPM	0	0
No TPM, No China TPM	0	1
Reserved	1	0
TPM	1	1

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Compal Electronics, Inc.

Title: PCH (5/8)

Size | Document Number: LA-5472P | Rev: A00

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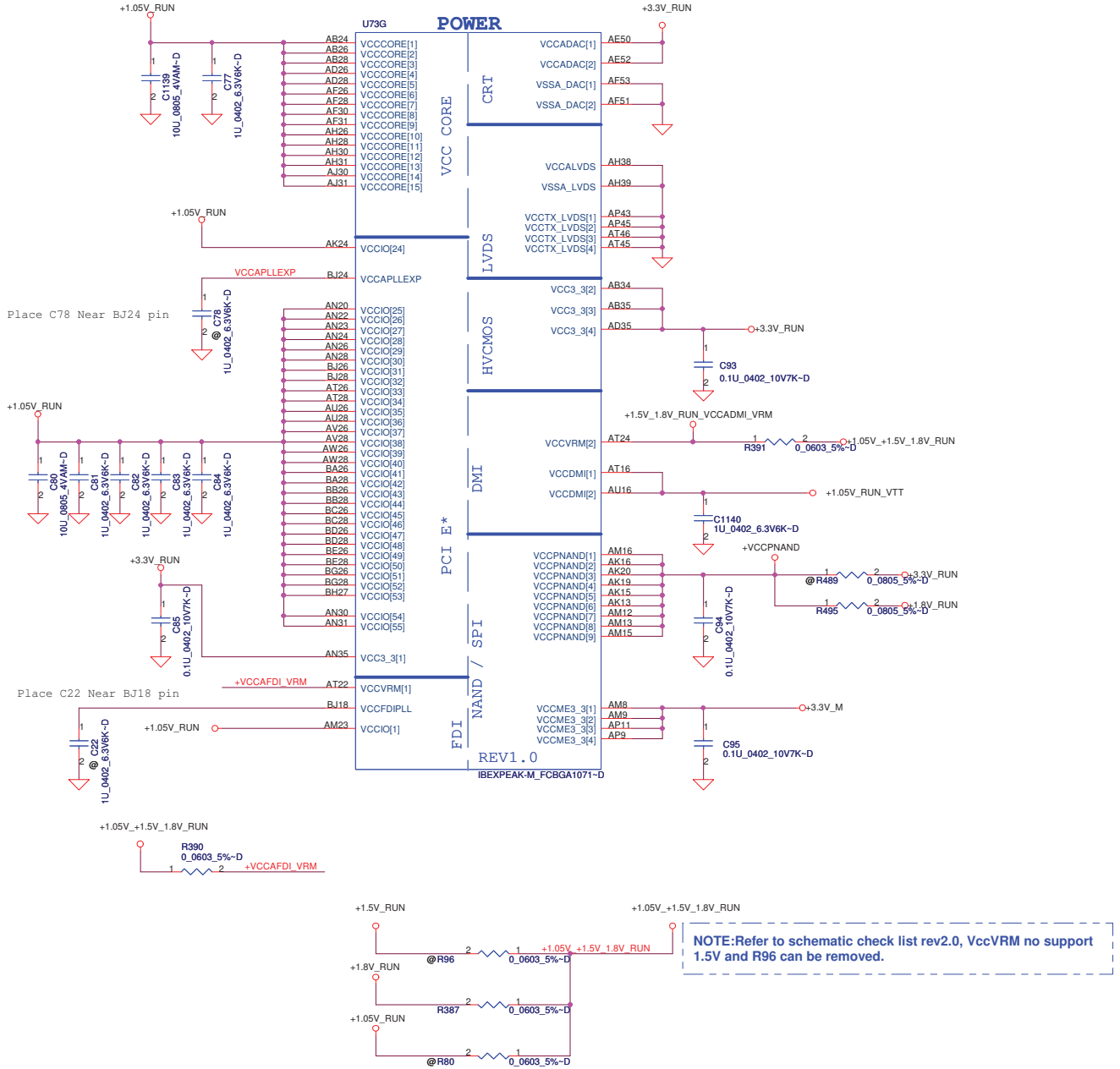

PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_CPU_IO	1.1/1.05	< 1 (mA)
V5REF	5	< 1 (mA)
V5REF_Sus	5	< 1 (mA)
Vcc3_3	3.3	0.357
VccAClk	1.1	0.052
VccADAC	3.3	0.069
VccADPLLA	1.1	0.068
VccADPLLB	1.1	0.069
VccapllEXP	1.1	0.04
VccCore	1.1	1.432
VccDMI	1.1	0.058
VccDMI	1.1	0.061
VccFDIPLL	1.1	0.037
VccIO	1.1	3.062
VccLAN	1.1	0.32
VccME	1.1	1.849
VccME3_3	3.3	0.085
VccpNAND	1.8	0.156
VccRTC	3.3	2 (mA)
VccSATAPLL	1.1	0.031
VccSus3_3	3.3	0.163
VccSusHDA	3.3	0.006
VccVRM	1.8 / 1.5	0.196
VccVRM	1.05	< 1 (mA)
VccALVDS	3.3	< 1 (mA)
VccTX_LVDS	1.8	0.059

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Title: PCH (6/8)

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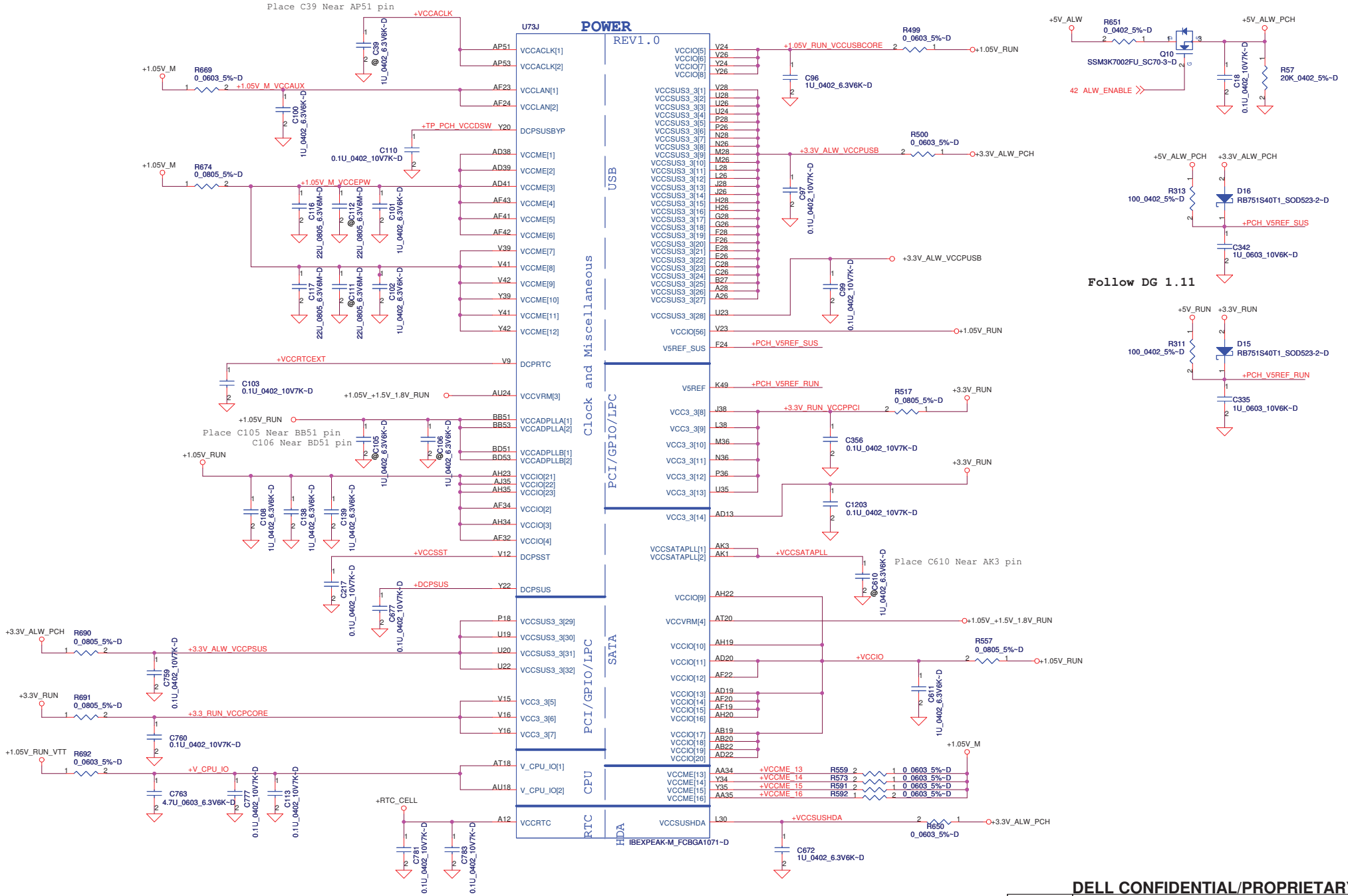

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Title: PCH (7/8)

Size: | Document Number: LA-5472P | Rev: A00

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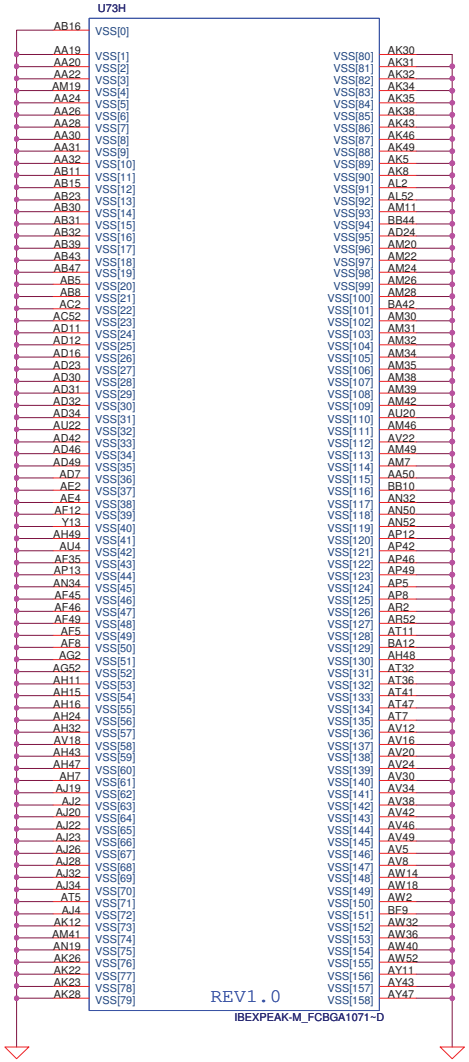

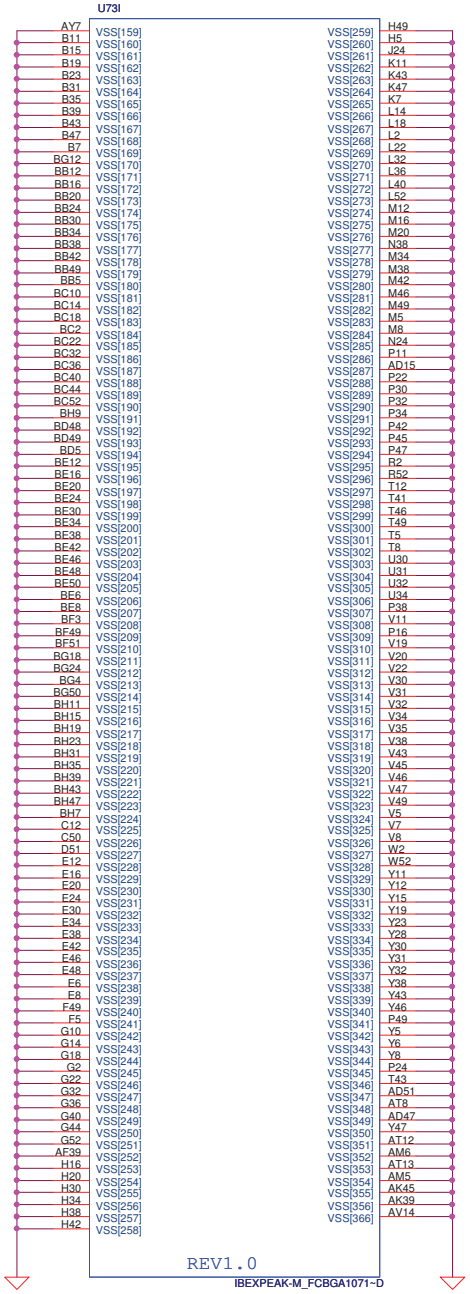

Compal Electronics, Inc.

Title: PCH (8/8)

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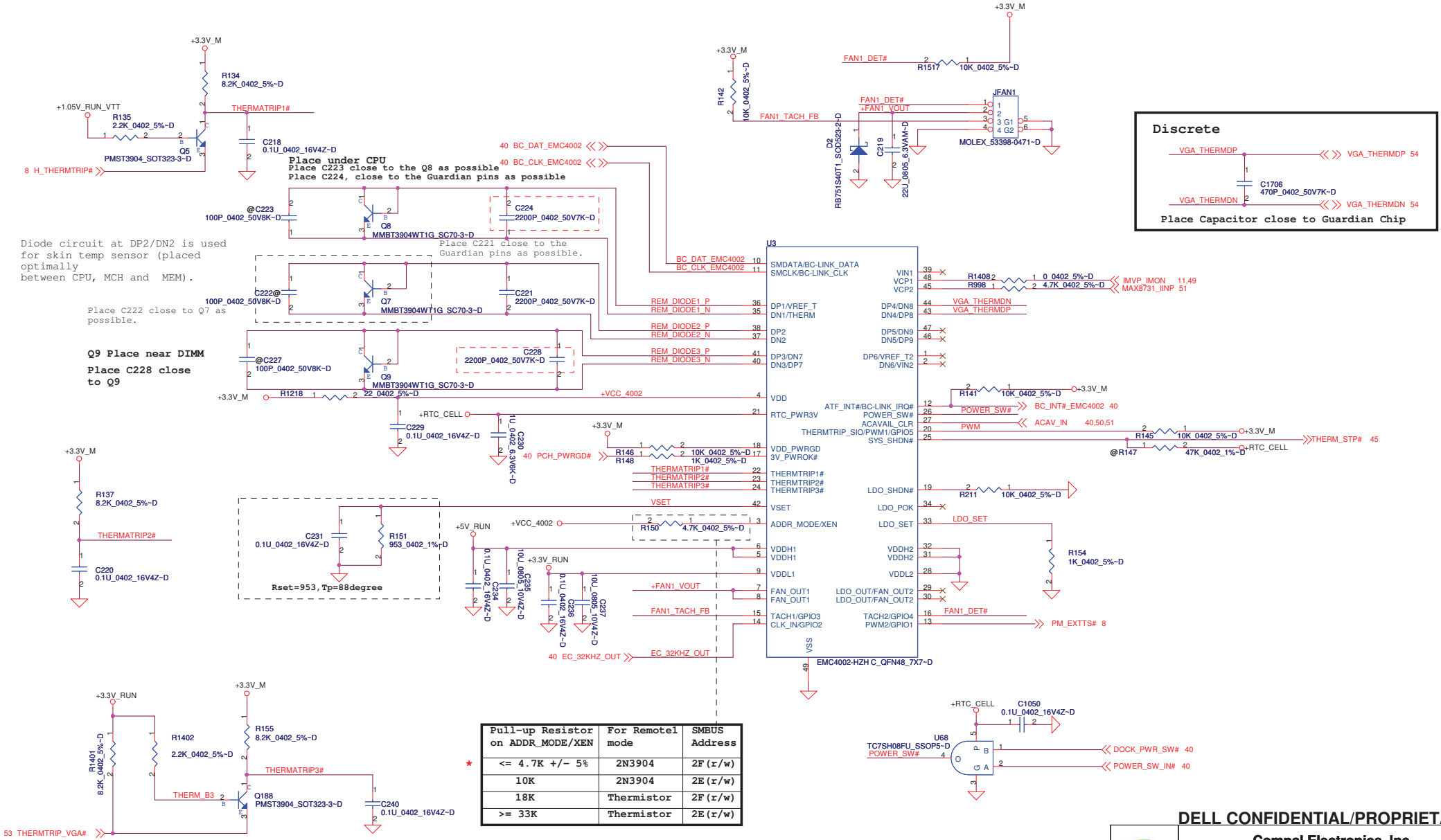

Pull-up Resistor on ADDR_MODE/XEN	For Remote1 mode	SMBUS Address
<= 4.7K +/- 5%	2N3904	2F(r/w)
10K	2N3904	2E(r/w)
18K	Thermistor	2F(r/w)
>= 33K	Thermistor	2E(r/w)

Compal Electronics, Inc.

Title: FAN & Thermal Sensor

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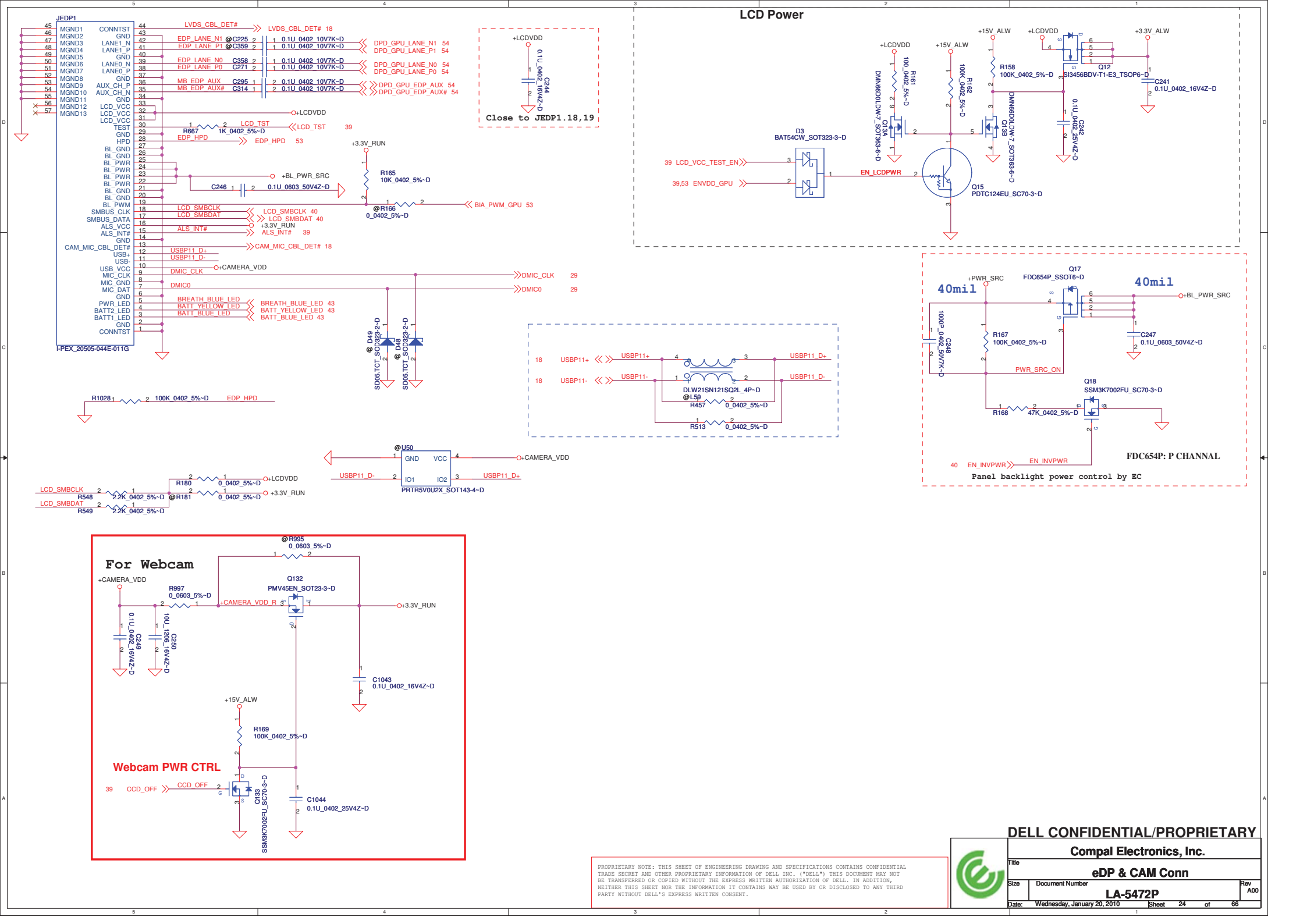
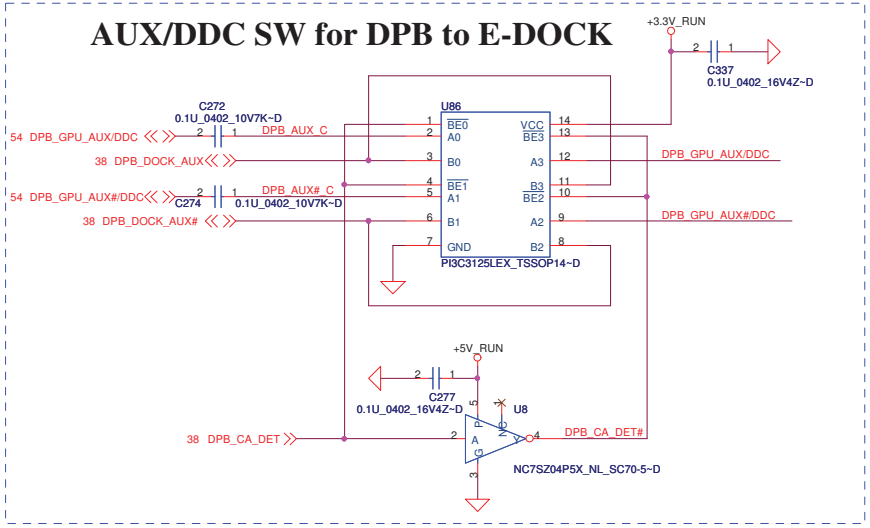


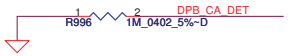
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title	eDP & CAM Conn	
Size	Document Number: LA-5472P	Rev: A00
Date: Wednesday, January 20, 2010	Sheet 24 of 66	

AUX/DDC SW for DPB to E-DOCK





Compal Electronics, Inc.

Title: DPB AUX SW for DOCK

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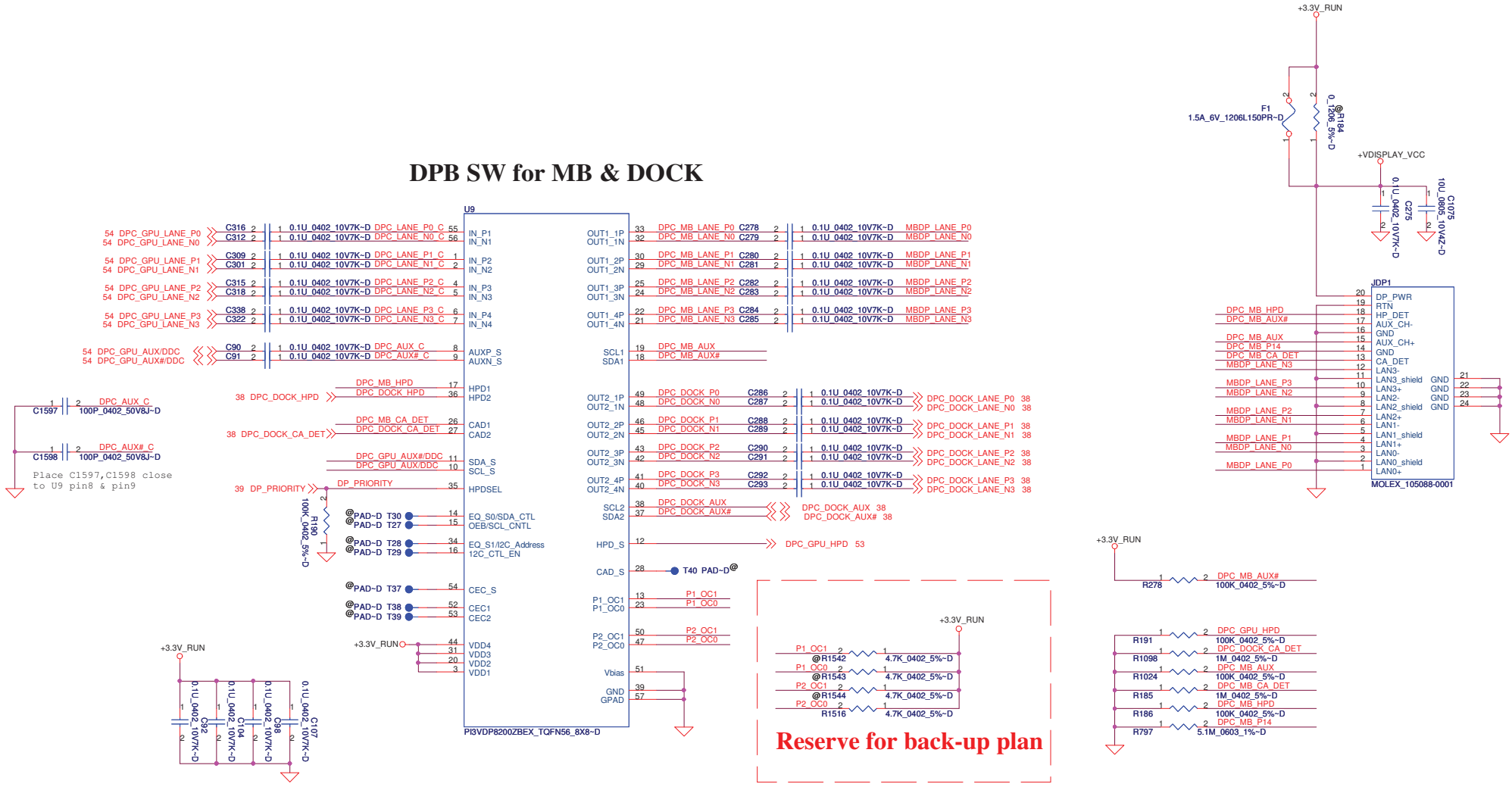
Display port Connector



Compal Electronics, Inc.

Title: Display port

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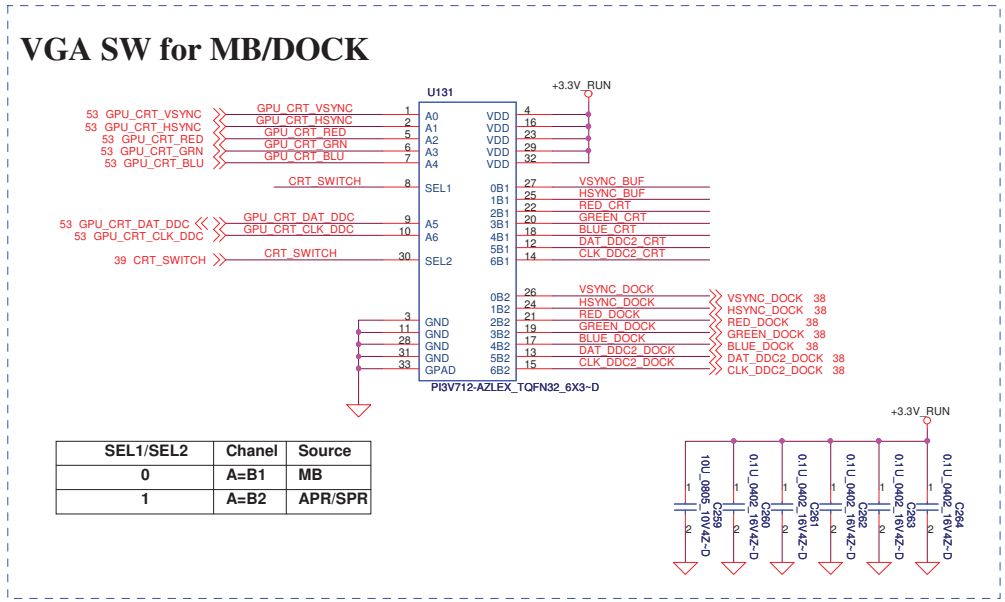
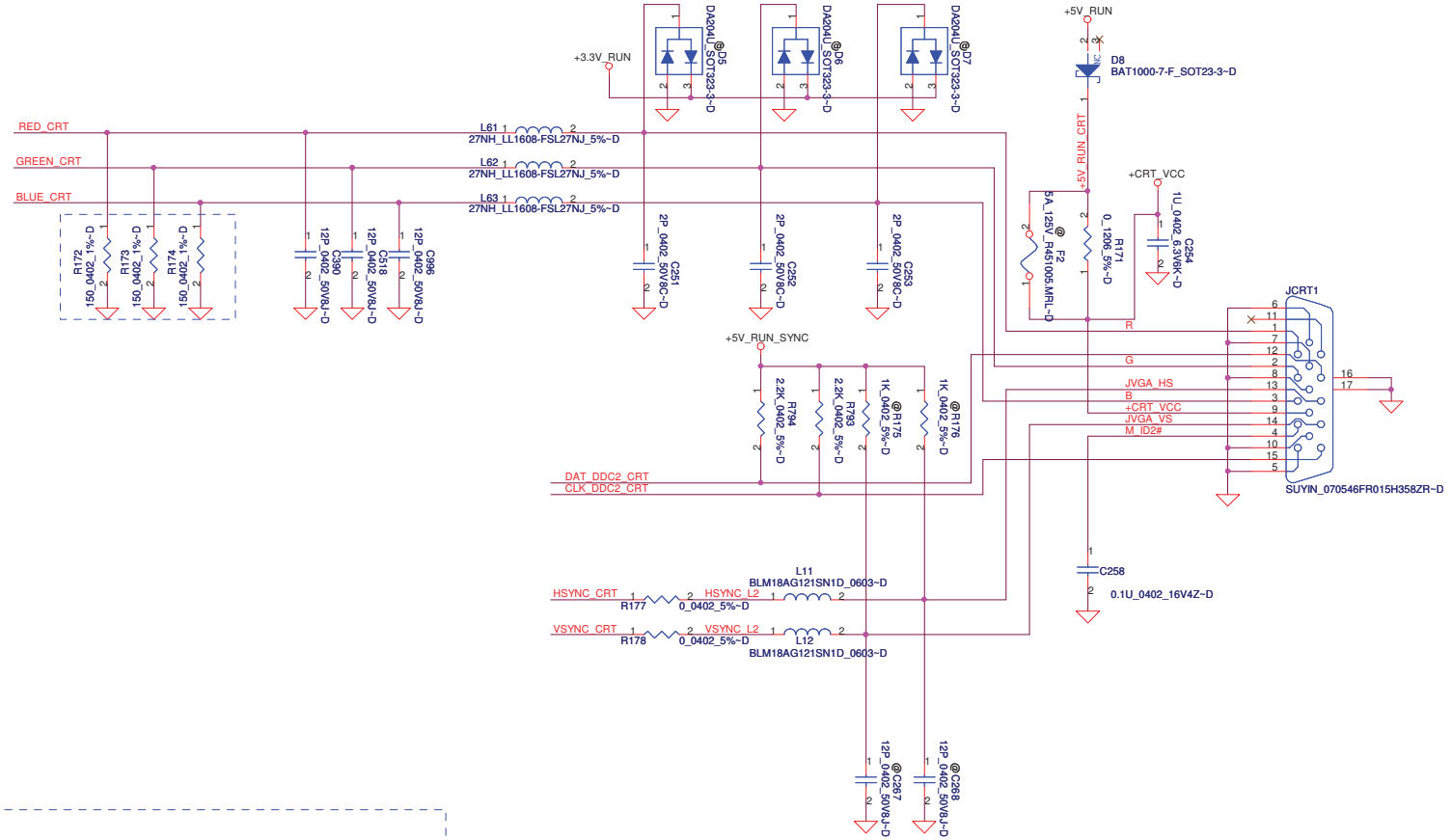
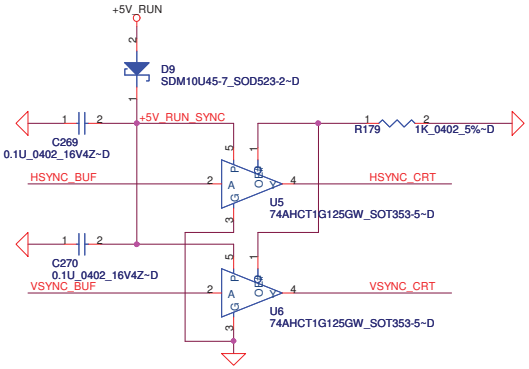
Date: Wednesday, January 20, 2010 | Sheet 26 of 66







Compal Electronics, Inc.

Title: CRT/Video switch

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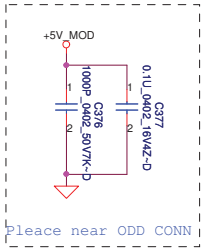
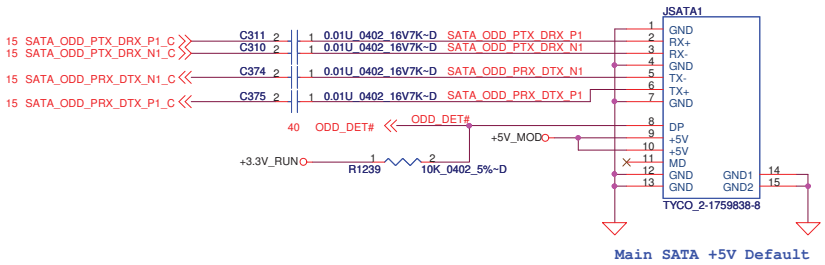
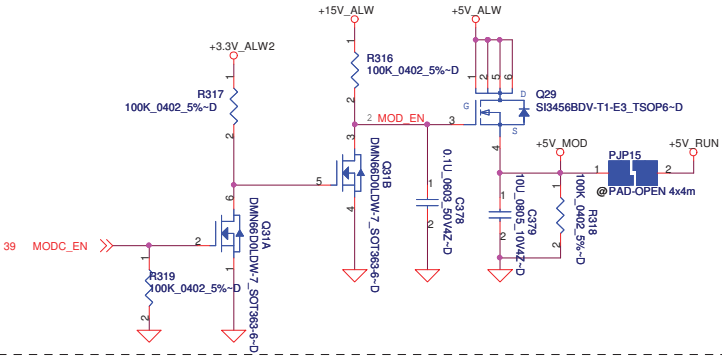
Date: Wednesday, January 20, 2010 | Sheet 27 of 66



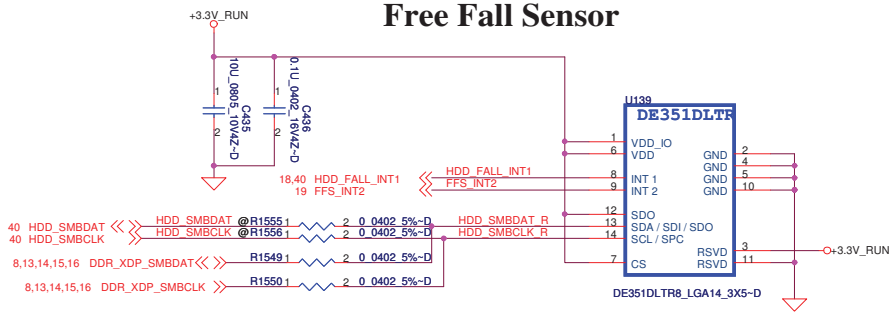
For ODD



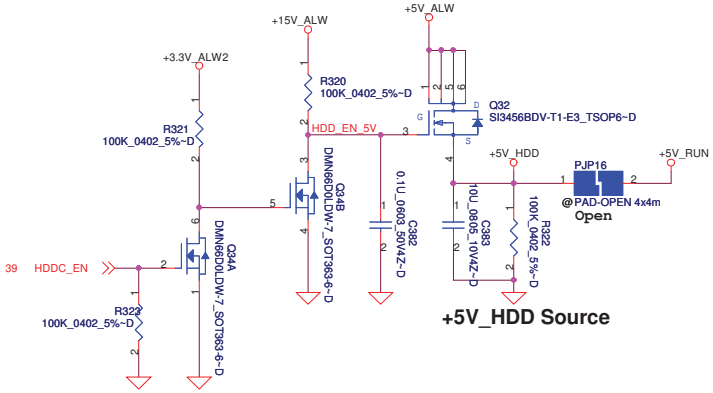
+5VMOD Source

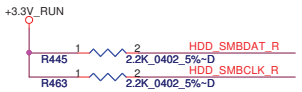


Free Fall Sensor

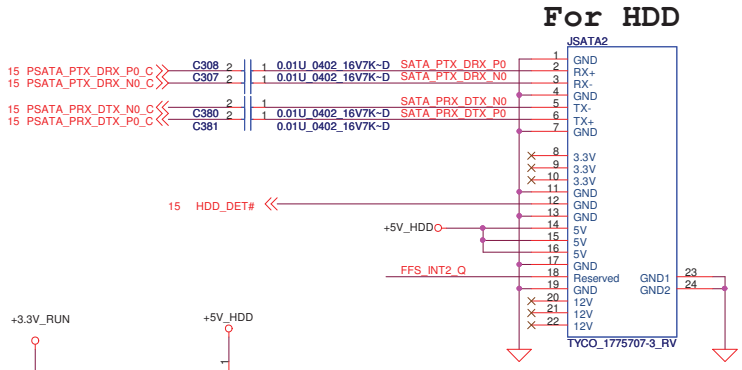


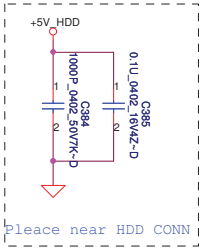
HDD PWR

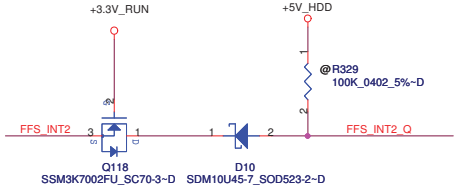




For HDD







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Compal Electronics, Inc.

Title: ODD/HDD CONNECTOR

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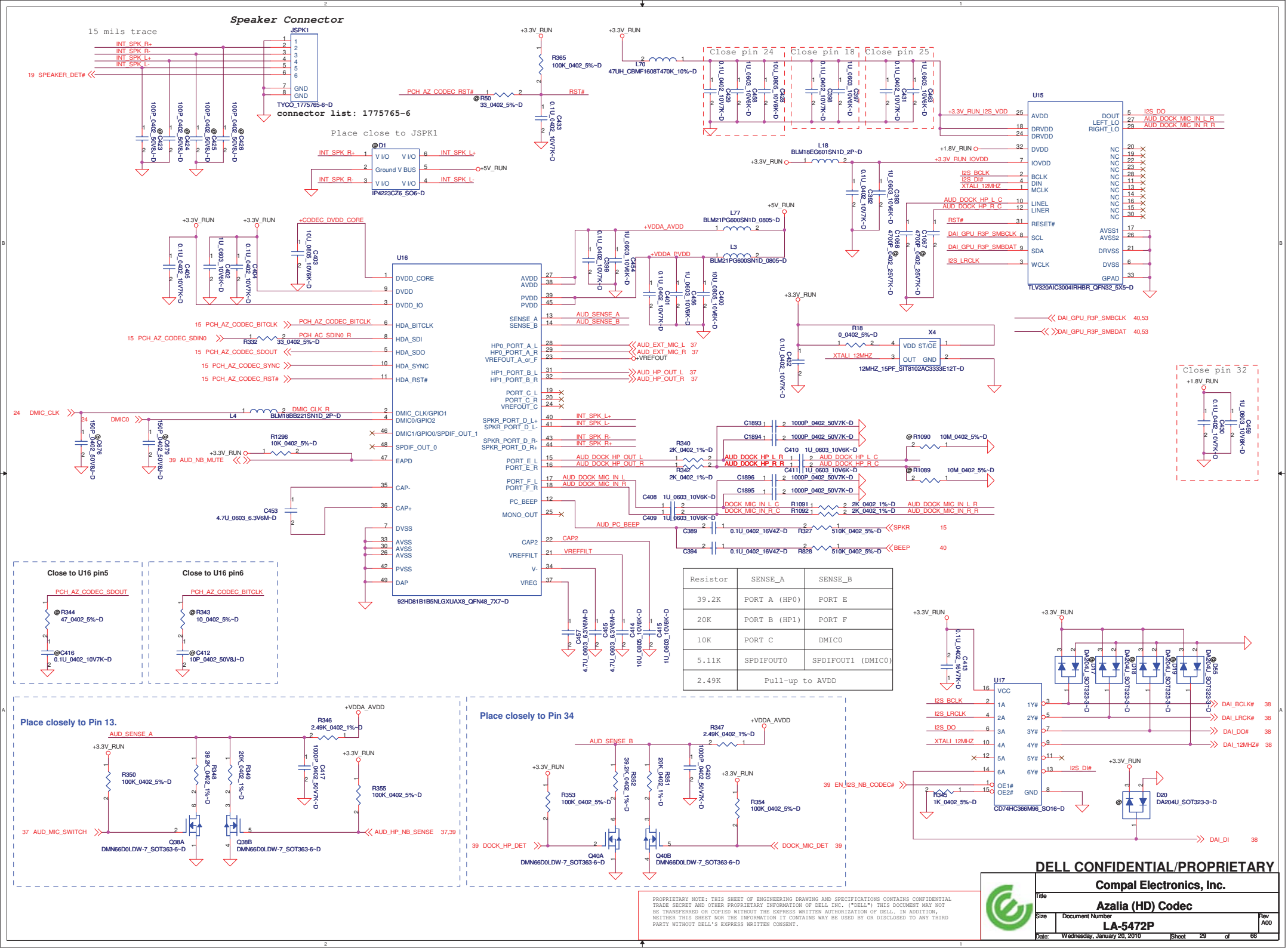

Resistor	SENSE_A	SENSE_B
39.2K	PORT A (HP0)	PORT E
20K	PORT B (HP1)	PORT F
10K	PORT C	DMIC0
5.11K	SPDIFOUT0	SPDIFOUT1 (DMIC0)
2.49K	Pull-up to AVDD	

Compal Electronics, Inc.

Title: Azalia (HD) Codec

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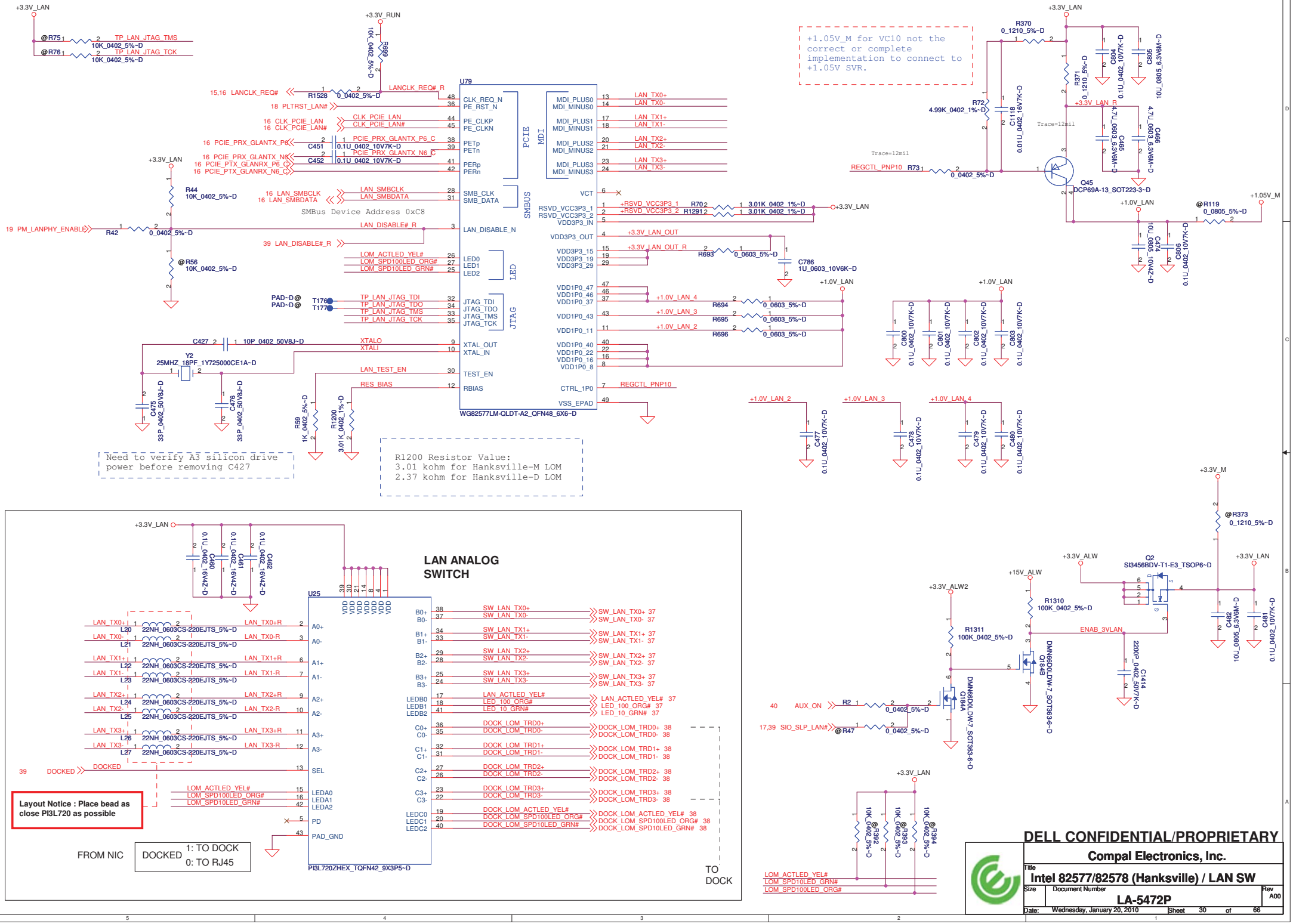
+1.05V_M for VC10 not the correct or complete implementation to connect to +1.05V SVR.
U79
WG82577LM-QLDT-A2_QFN48_6X6~D
SMBus Device Address 0xC8
Need to verify A3 silicon drive power before removing C427
R1200 Resistor Value:
3.01 kohm for Hanksville-M LOM
2.37 kohm for Hanksville-D LOM
LAN ANALOG SWITCH
U25
PI3L720ZHEX_TQFN42_9X3P5~D
Layout Notice : Place bead as close PI3L720 as possible
FROM NIC
DOCKED 1: TO DOCK 0: TO RJ45
TO DOCK
Q45 DCP69A-13_SOT223-3~D
Q2 SI3456BDV-T1-E3_TSOP6~D
DMN66D0LDW-7_SOT363-6~D
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Compal Electronics, Inc.
Intel 82577/82578 (Hanksville) / LAN SW
LA-5472P
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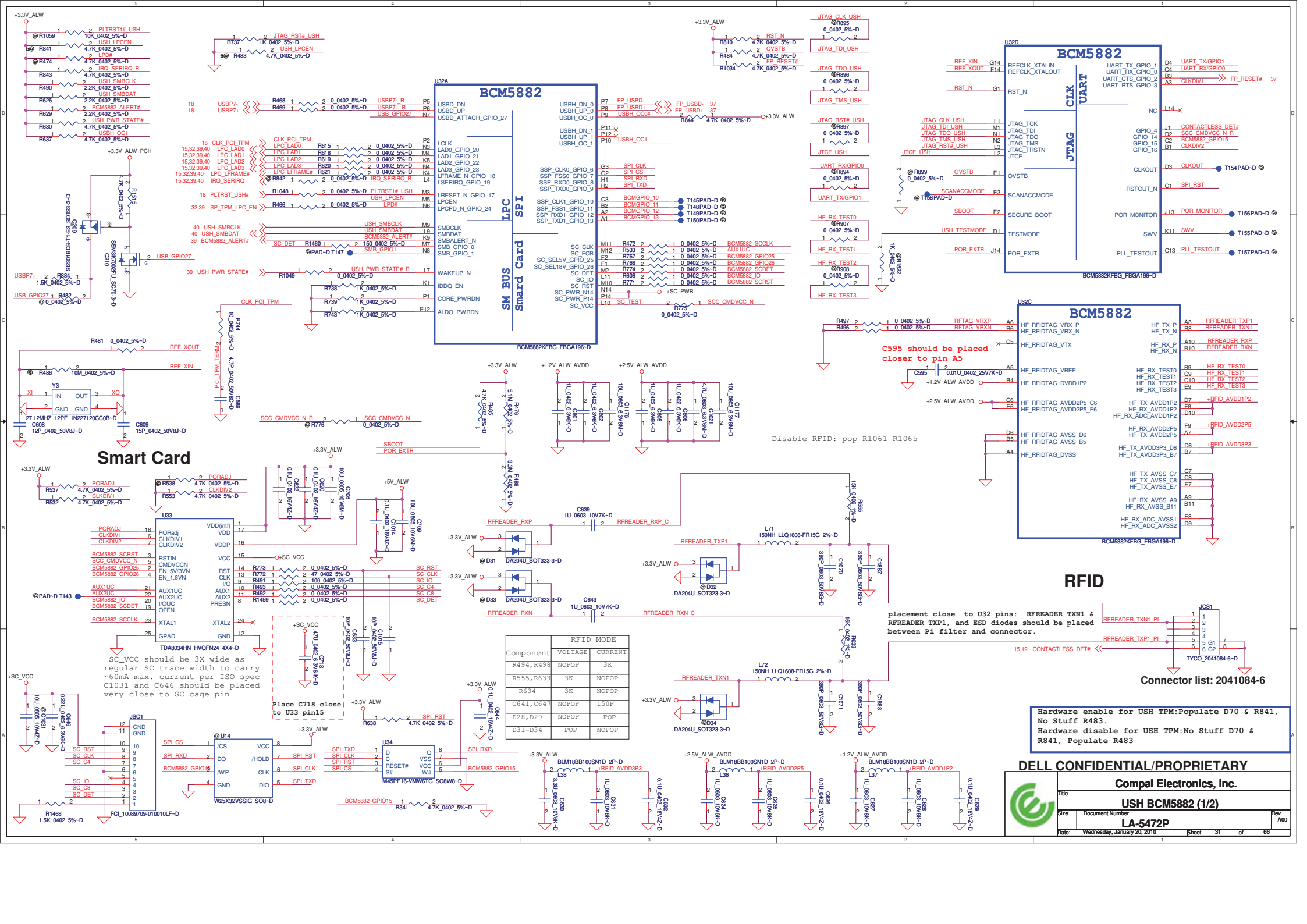
Smart Card
RFID
U32A
BCM5882
U32D
U32C
U33
TDA8034HN_HVQFN24_4X4~D
U34
M45PE16-VMW6TG_SO8W8~D
W25X32VSSIG_SO8~D
JSC1
FCI_10089709-010010LF~D
JCS1
TYCO_2041084-6~D
Connector list: 2041084-6
SC_VCC should be 3X wide as regular SC trace width to carry ~60mA max. current per ISO spec C1031 and C646 should be placed very close to SC cage pin
Place C718 close to U33 pin15
C595 should be placed closer to pin A5
Disable RFID: pop R1061~R1065
placement close to U32 pins: RFREADER_TXN1 & RFREADER_TXP1, and ESD diodes should be placed between Pi filter and connector.
Hardware enable for USH TPM:Populate D70 & R841, No Stuff R483.
Hardware disable for USH TPM:No Stuff D70 & R841, Populate R483
RFID MODE
Component | VOLTAGE | CURRENT
R494,R498 | NOPOP | 3K
R555,R633 | 3K | NOPOP
R634 | 3K | NOPOP
C641,C647 | NOPOP | 150P
D28,D29 | NOPOP | POP
D31~D34 | POP | NOPOP
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Compal Electronics, Inc.
USH BCM5882 (1/2)
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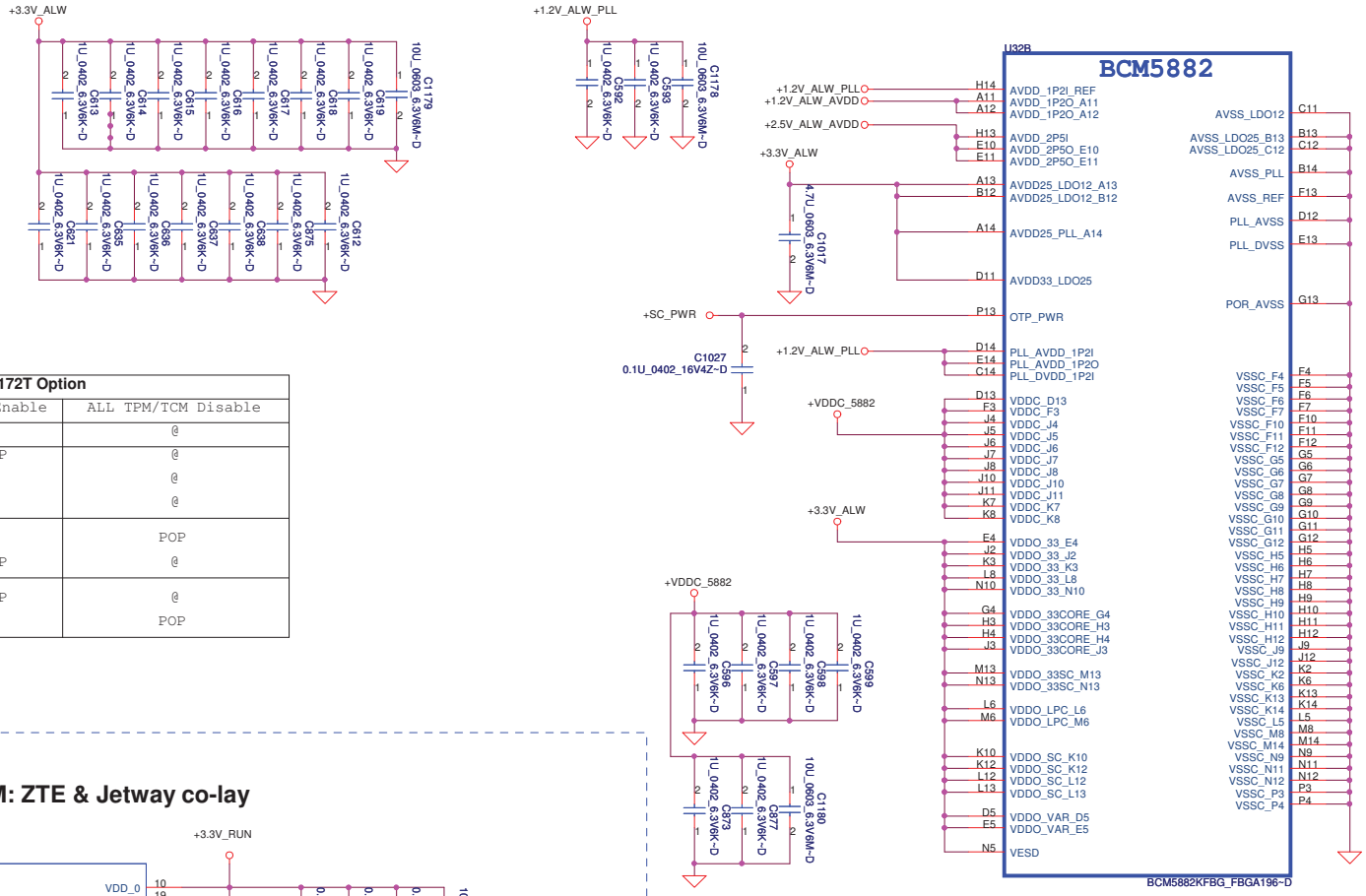
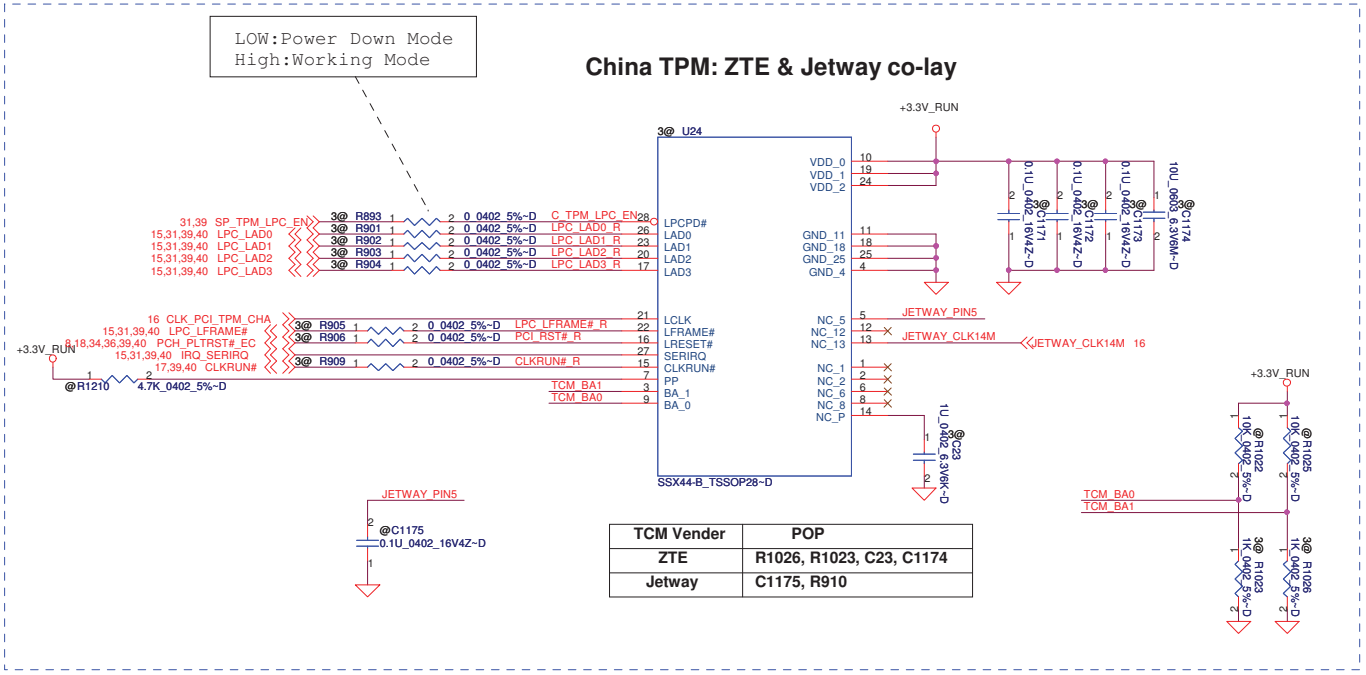


USH BCM5882 and China TPM Z8H172T Option				
PART/PIN	Ref Des	TCM Enable	TPM Enable	ALL TPM/TCM Disable
TCM circuit	All 3@	POP	@	@
SIO 5028 ->SP_TPM_LPC_EN	PU R841	@	POP	@
	PD R483	POP	@	@
	PU R788	@	@	@
PCH GPIO39 ->TPM_ID1	PU R787	@	@	POP
	PD R339	POP	POP	@
PCH GPIO38 ->TPM_ID0	PU R273	POP	POP	@
	PD R922	@	@	POP



TCM Vender	POP
ZTE	R1026, R1023, C23, C1174
Jetway	C1175, R910

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Compal Electronics, Inc.

Title: USH BCM5882 (2/2)

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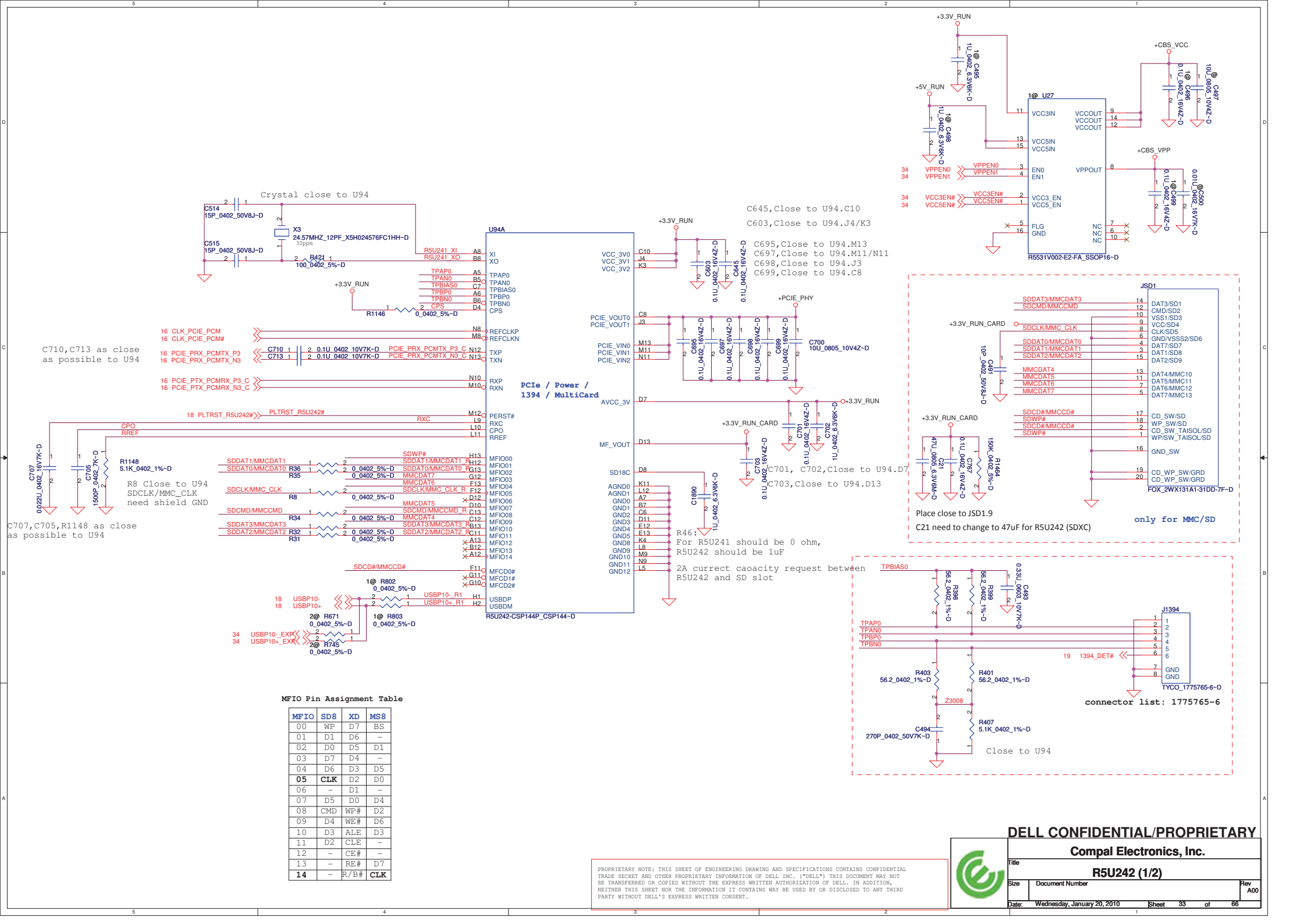

MFIO Pin Assignment Table

MFIO	SD8	XD	MS8
00	WP	D7	BS
01	D1	D6	–
02	D0	D5	D1
03	D7	D4	–
04	D6	D3	D5
05	**CLK**	D2	D0
06	–	D1	–
07	D5	D0	D4
08	CMD	WP#	D2
09	D4	WE#	D6
10	D3	ALE	D3
11	D2	CLE	–
12	–	CE#	–
13	–	RE#	D7
14	–	R/B#	**CLK**

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Compal Electronics, Inc.

Title: R5U242 (1/2)

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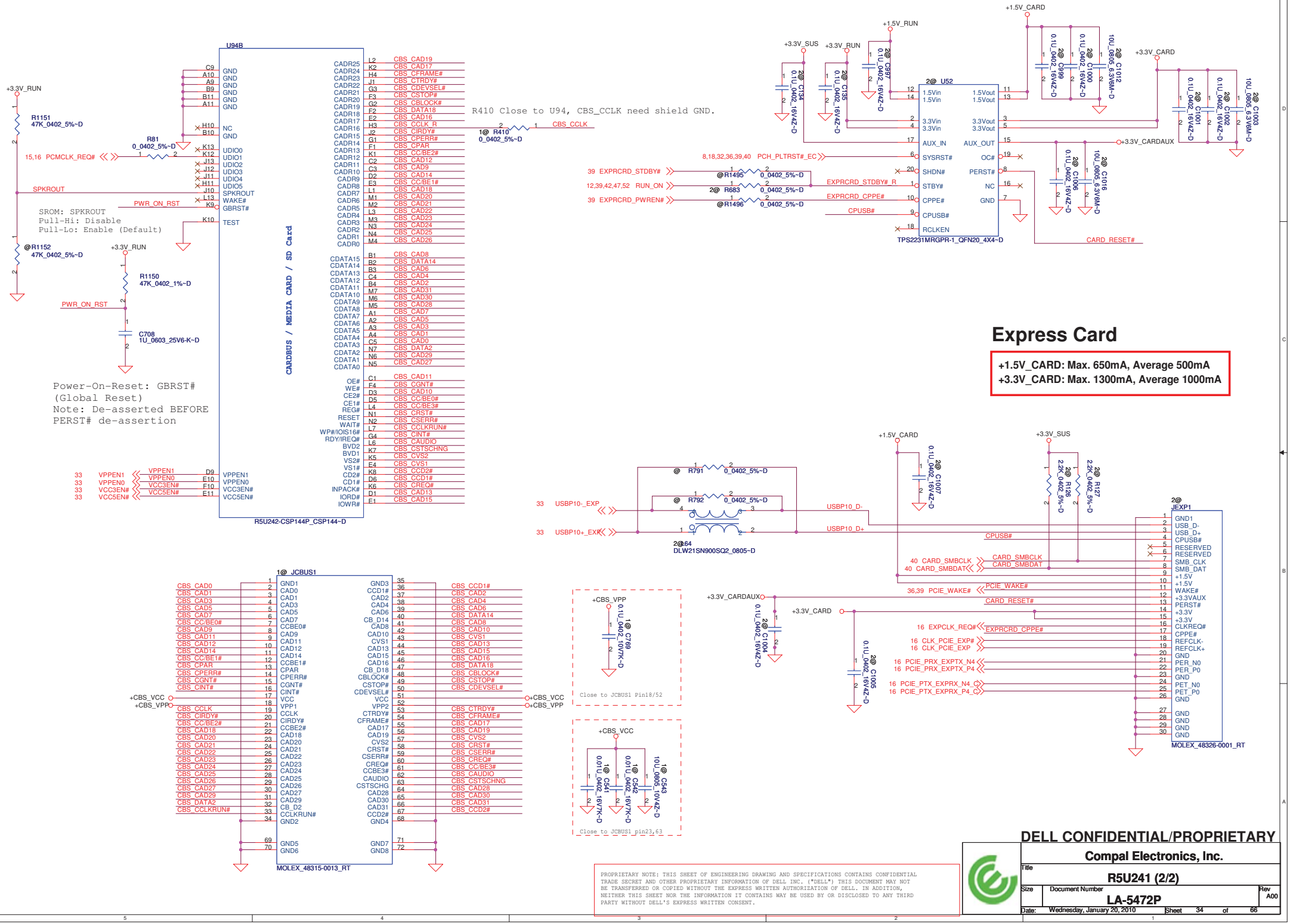
U94B
CARDBUS / MEDIA CARD / SD Card
R5U242-CSP144P_CSP144-D
R410 Close to U94, CBS_CCLK need shield GND.
SROM: SPKROUT
Pull-Hi: Disable
Pull-Lo: Enable (Default)
Power-On-Reset: GBRST#
(Global Reset)
Note: De-asserted BEFORE
PERST# de-assertion
2@ U52
TPS2231MRGPR-1_QFN20_4X4~D
Express Card
+1.5V_CARD: Max. 650mA, Average 500mA
+3.3V_CARD: Max. 1300mA, Average 1000mA
2@64
DLW21SN900SQ2_0805~D
2@
JEXP1
MOLEX_48326-0001_RT
1@ JCBUS1
MOLEX_48315-0013_RT
Close to JCBUS1 Pin18/52
Close to JCBUS1 pin23,63
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R5U241 (2/2)
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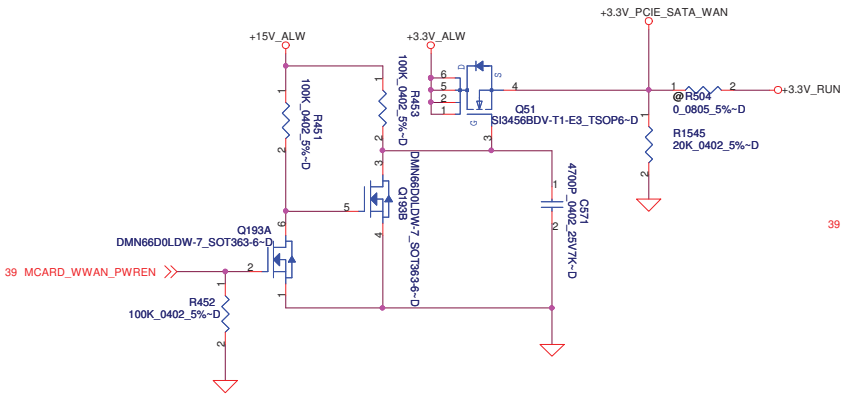
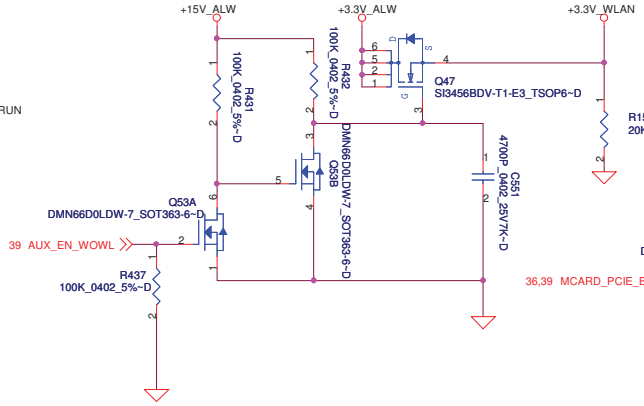
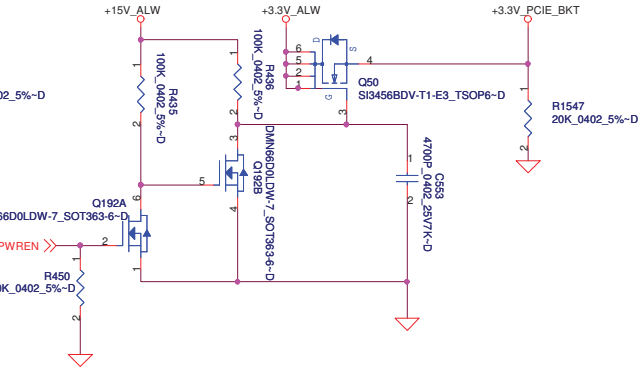
Power Control for Mini card1



Power Control for Mini card2



Power Control for Mini card3



Compal Electronics, Inc.

Title	PCIE PWR	
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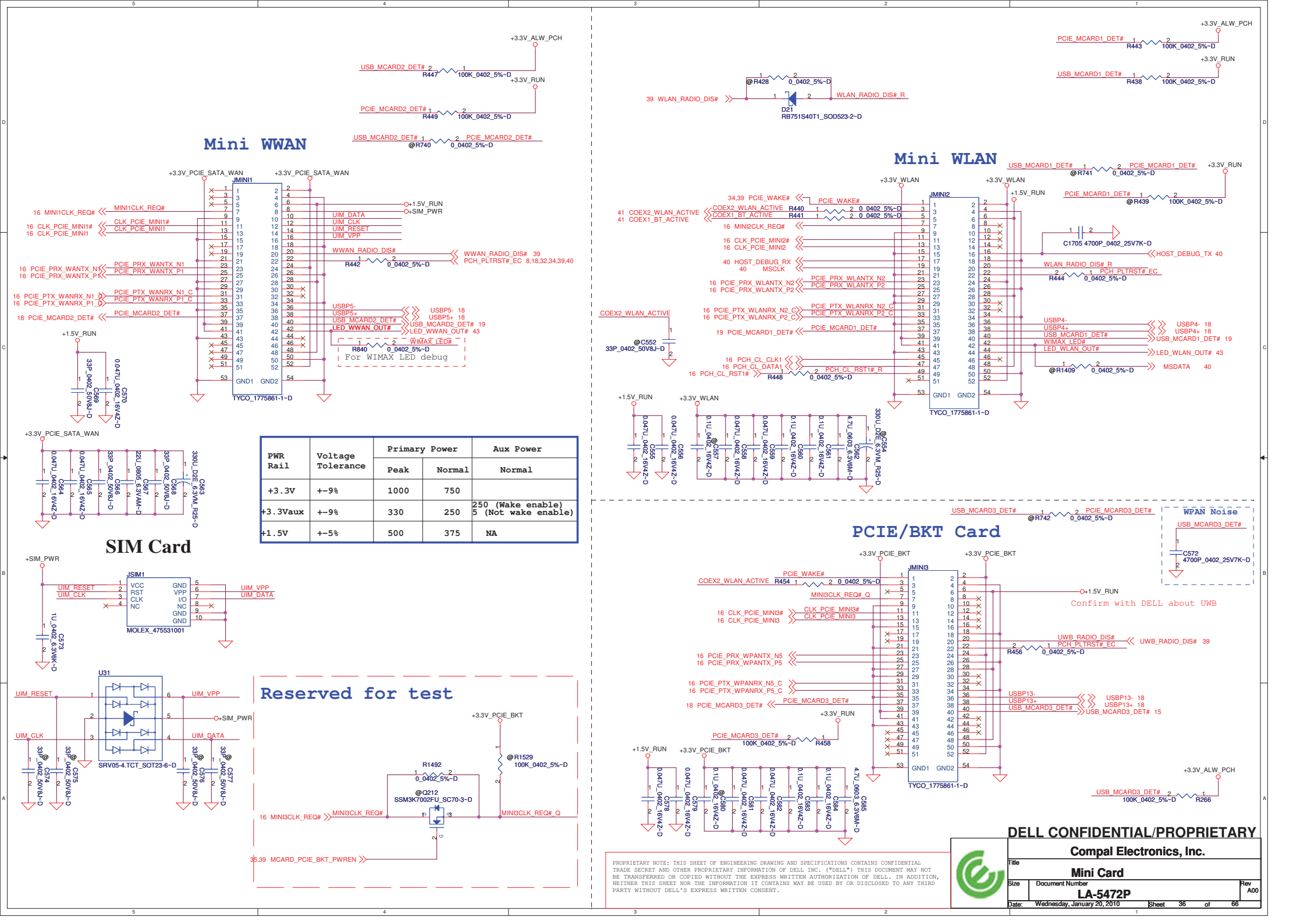

PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+-9%	1000	750	
+3.3Vaux	+-9%	330	250	250 (Wake enable) 5 (Not wake enable)
+1.5V	+-5%	500	375	NA

Compal Electronics, Inc.

Title: Mini Card

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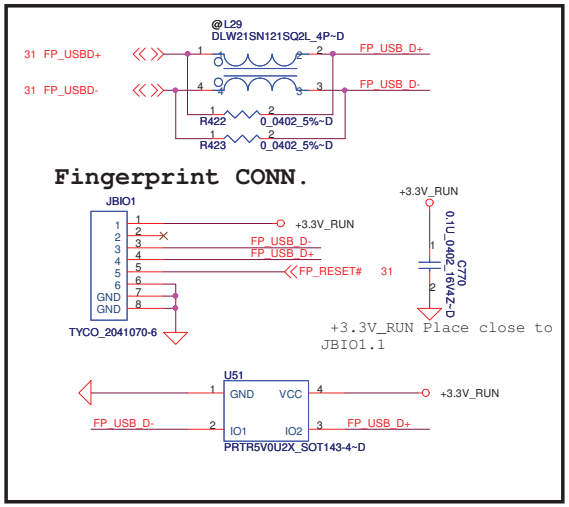
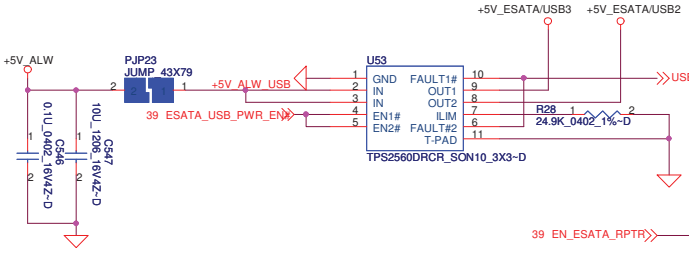
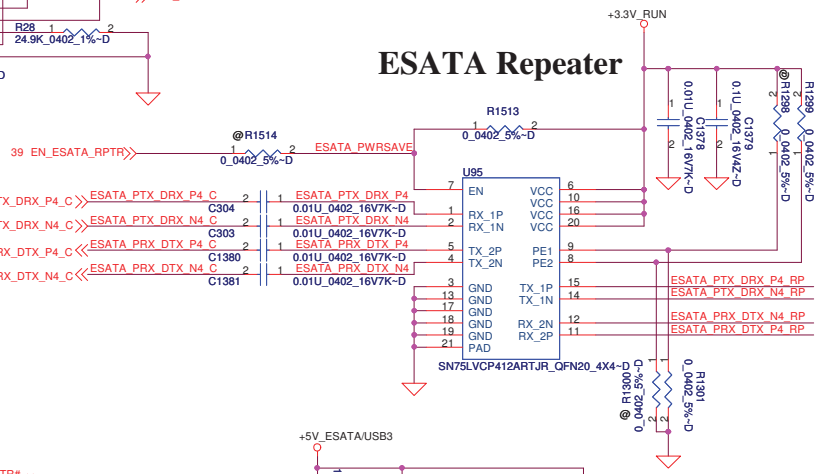
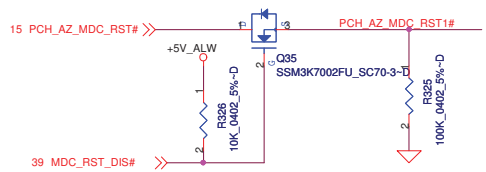
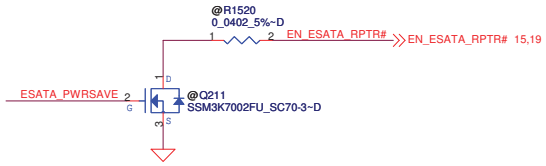
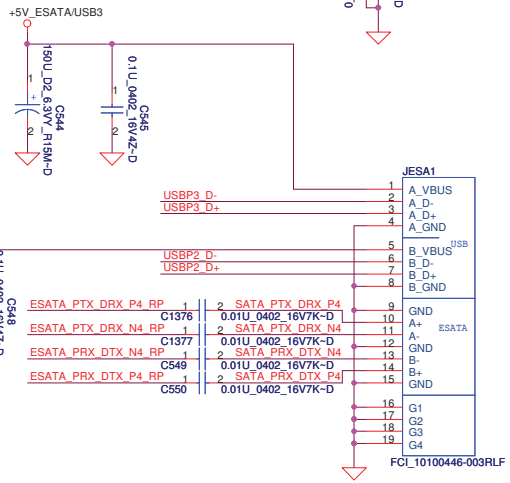




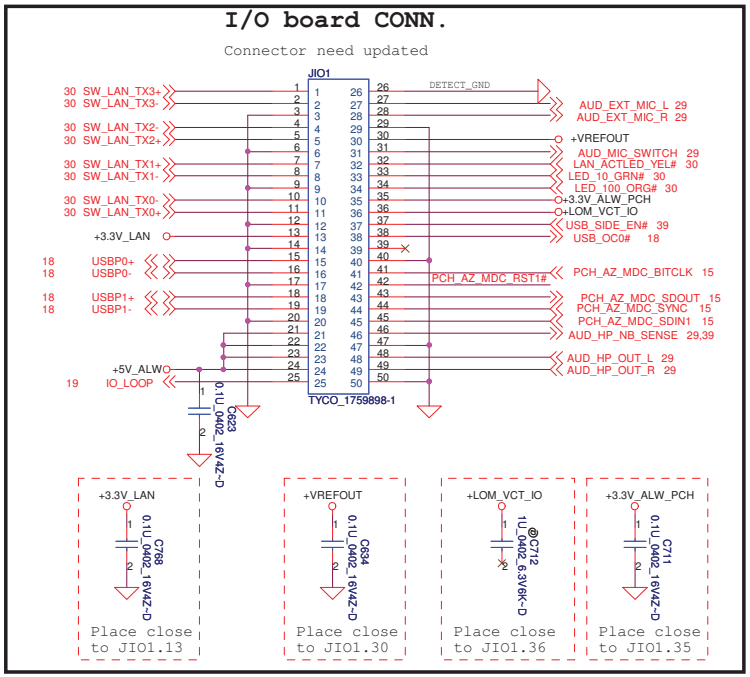


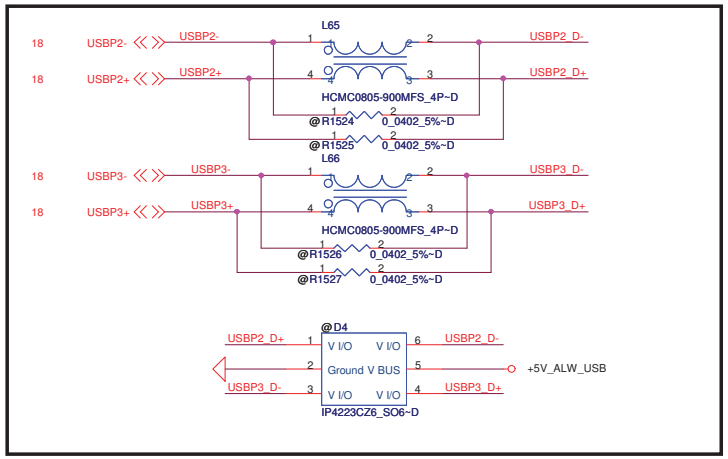






double check pin define with IO board.





Compal Electronics, Inc.

Title: USB 2.0 PORT

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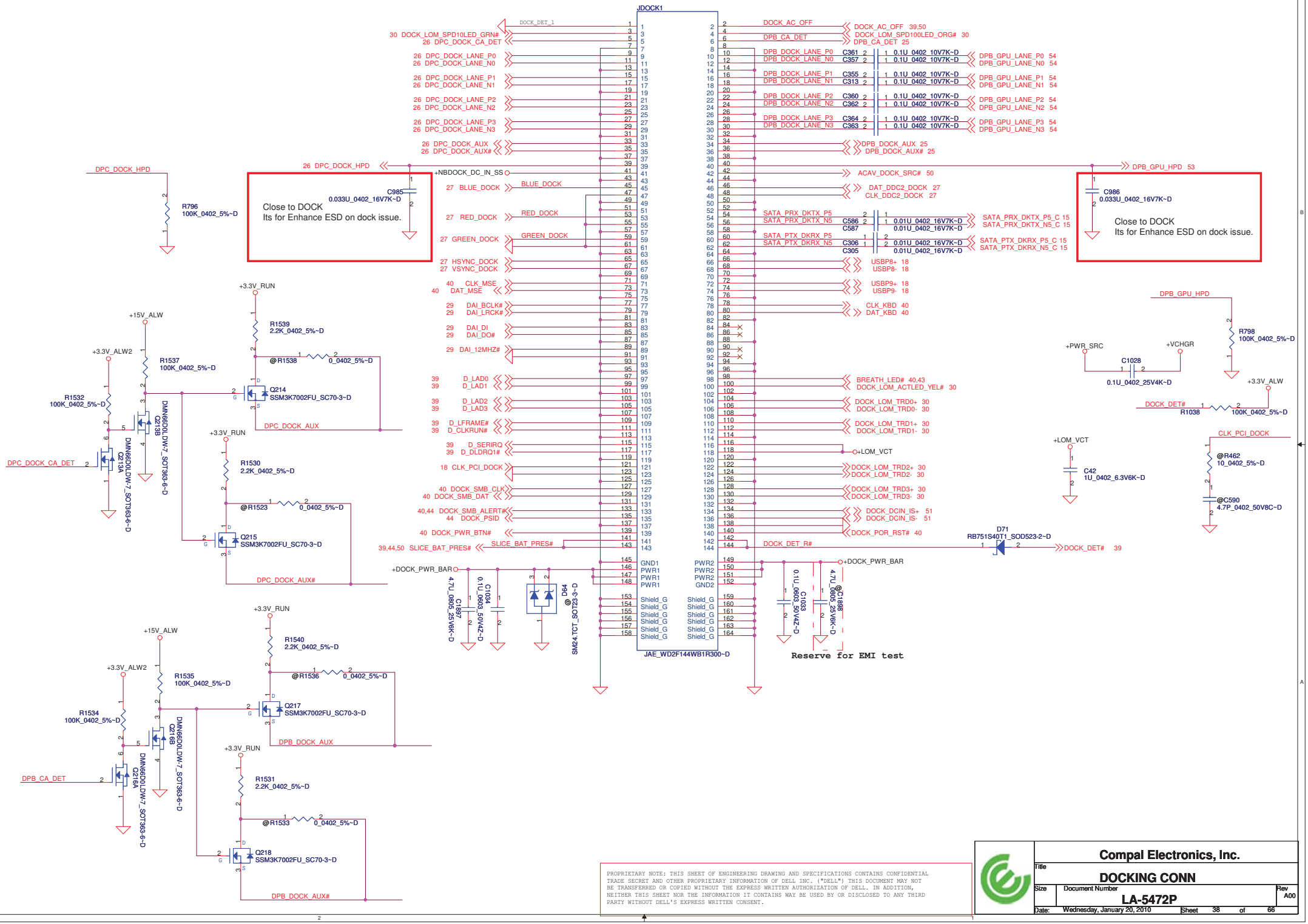

Compal Electronics, Inc.

Title: DOCKING CONN

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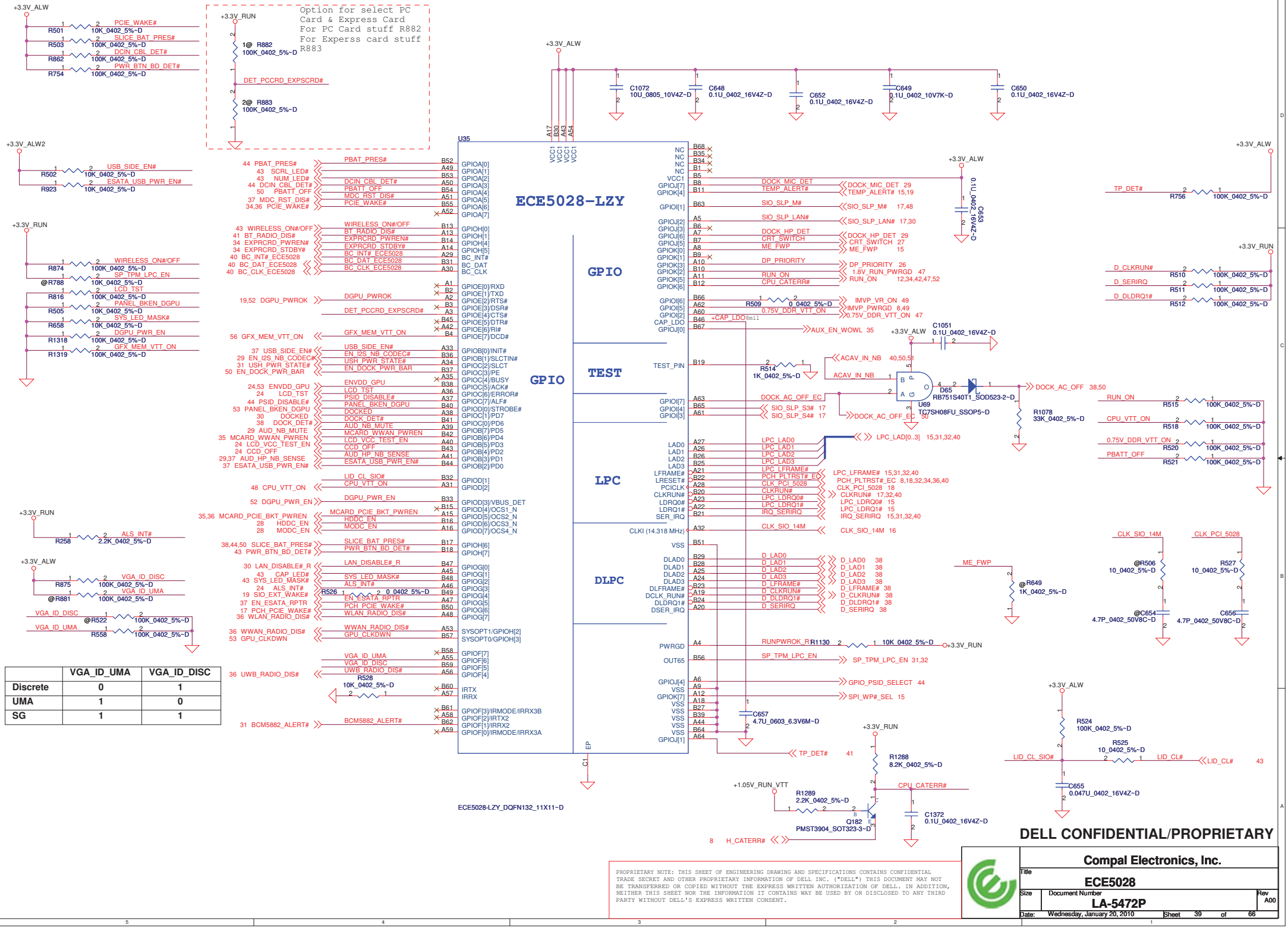
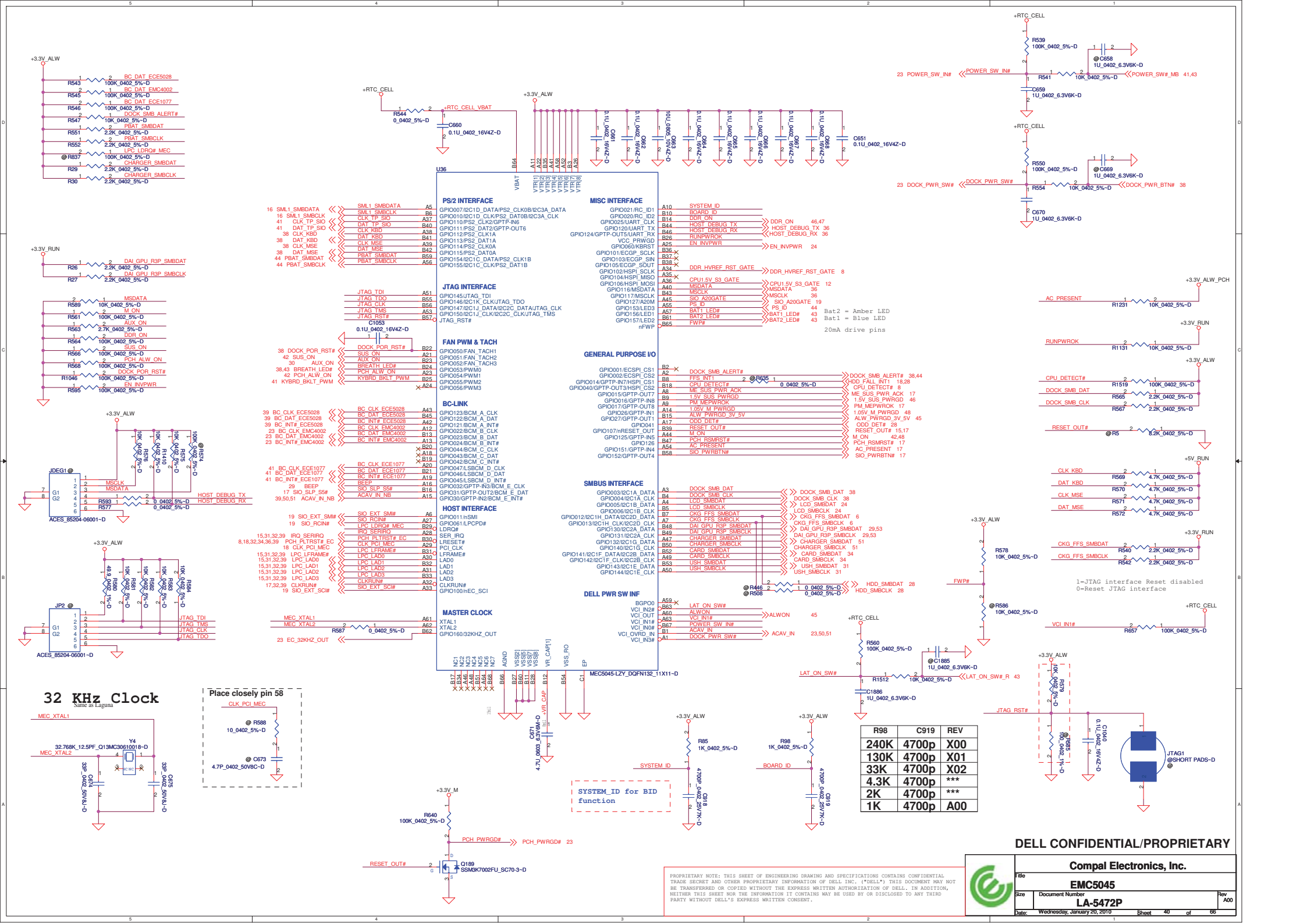
Date: Wednesday, January 20, 2010 | Sheet 38 of 66

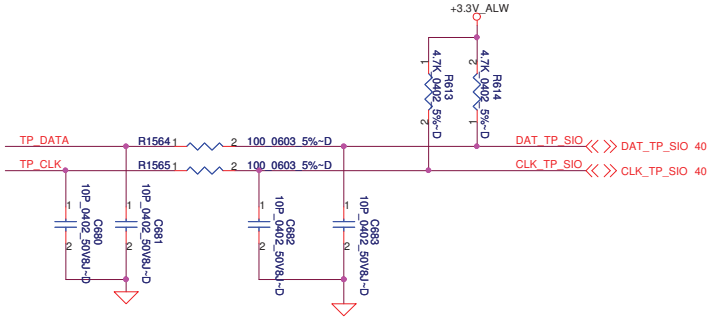


	VGA_ID_UMA	VGA_ID_DISC
Discrete	0	1
UMA	1	0
SG	1	1

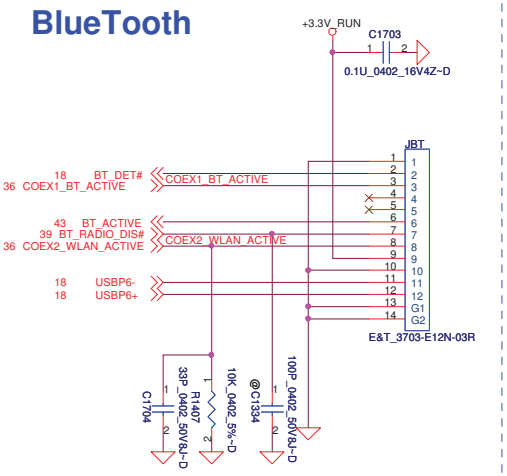


R98	C919	REV
240K	4700p	X00
130K	4700p	X01
33K	4700p	X02
4.3K	4700p	***
2K	4700p	***
1K	4700p	A00

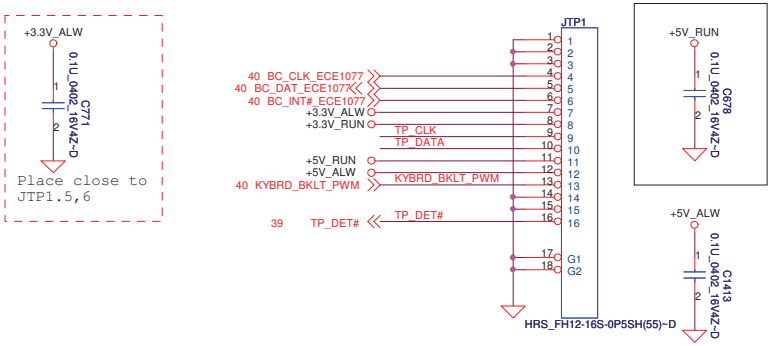
Touch Pad



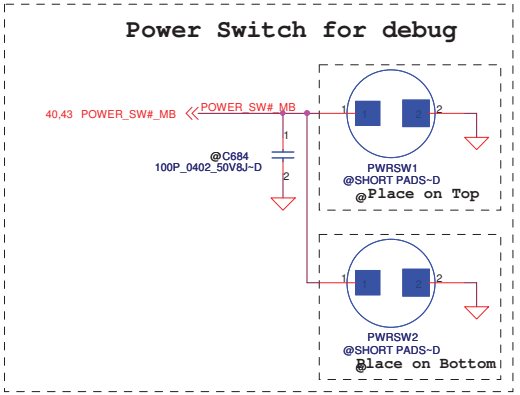
BlueTooth

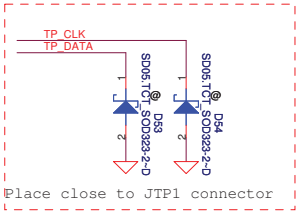


Touch Pad Conn. Pitch=0.5



Power Switch for debug





@FAN

Part Number	Description
DC28A000800	FAN SET DAQ20 DC5V AB7405HB-HB3 ADDA

@Speak

Part Number	Description
PK230003Q0L	SPK PACK ZJX 2.0W 4 OHM FG

@SM CARD BODY

Part Number	Description
SP070007V0L	S SOCKET TYCO 1770551-1 10P H5.9 SMART

@PCMCIA BODY

Part Number	Description
DC000001Q0L	PCMCIA TYCO 1759096-1

@MDC wire set cable

Part Number	Description
DC02000CS0L	H-CONN SET ZGX MB-MDC

@T/P wire set cable

Part Number	Description
DC02000840L	H-CONN SET ZJX MB-B/T-TP-FP

@LVDS cable

Part Number	Description
DC020003Y0L	H-CONN SET ZJX MB-LCD 14 WXGA+(-1ch)

@LVDS cable

Part Number	Description
DC02000870L	H-CONN SET ZJX MB-LCD 14 WXGA+(-2ch)

@RTC BATT

Part Number	Description
GC20323MX00	BATT CR2032 3V 220MAH MAXELL

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: Touch PAD/Int KB/LID

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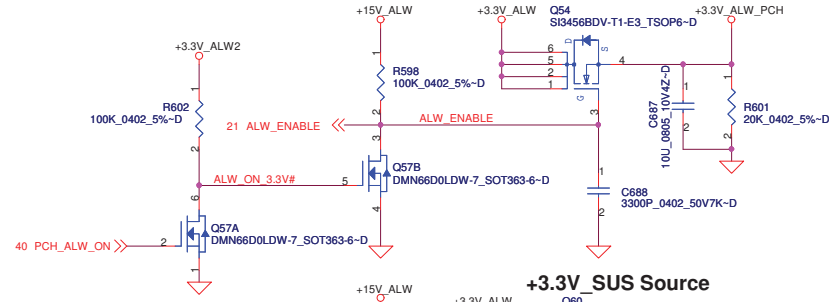
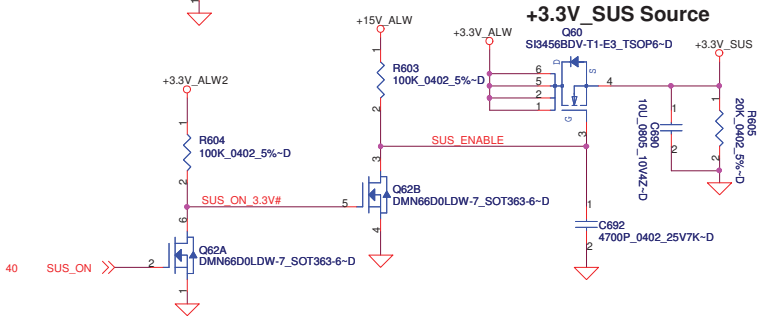
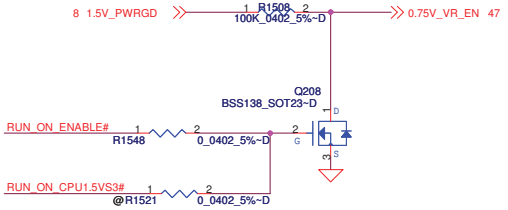
DC/DC Interface

+3.3V_ALW_PCH Source

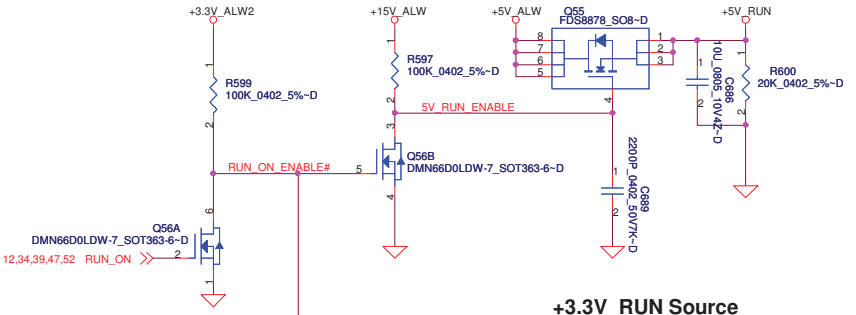


+3.3V_SUS Source

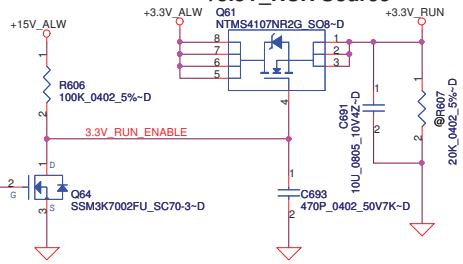




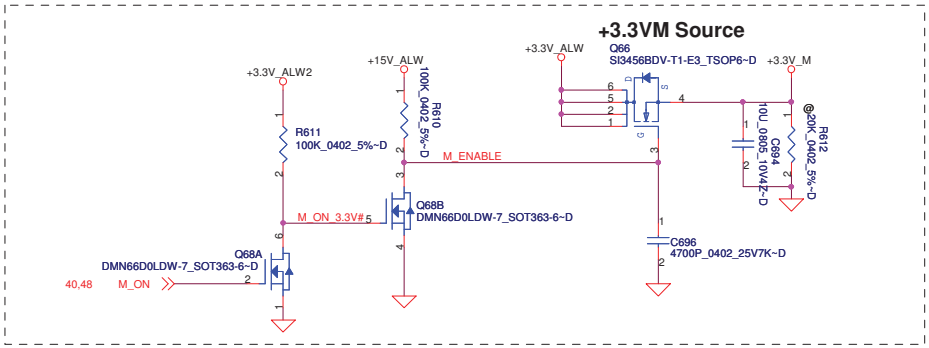
+5VRUN Source



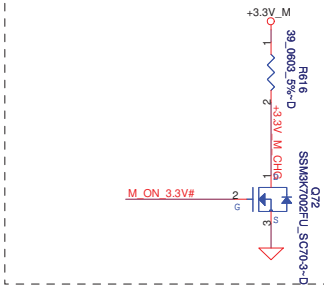
+3.3V_RUN Source



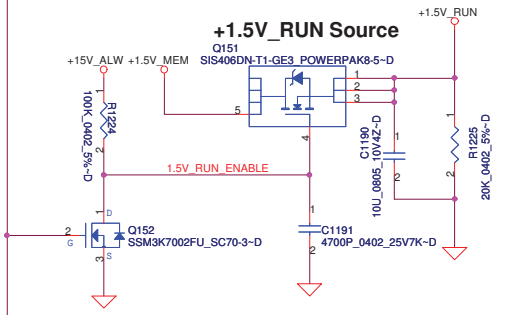
+3.3VM Source



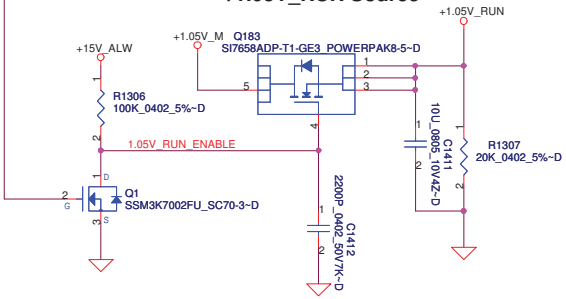
Discharg Circuit



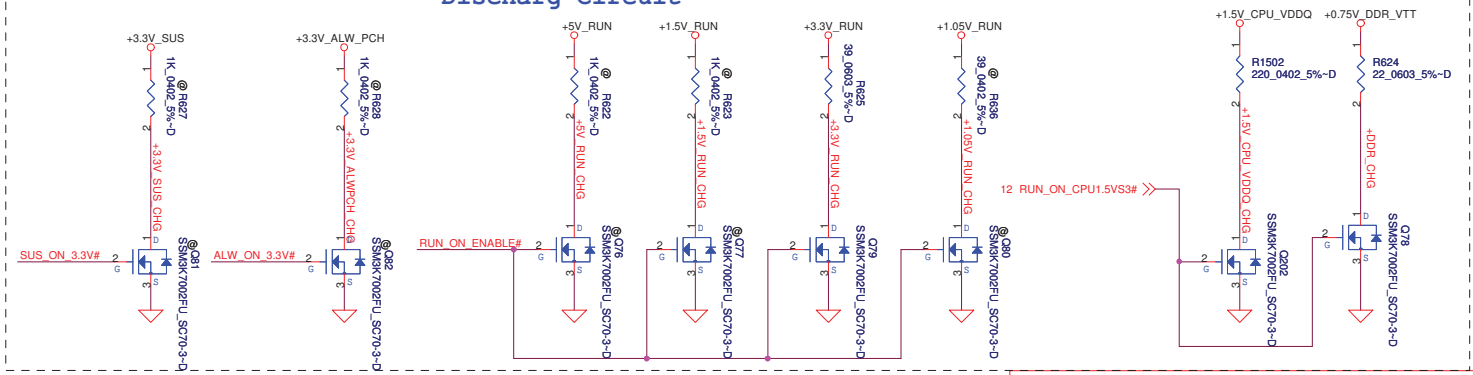
+1.5V_RUN Source



+1.05V_RUN Source



Discharg Circuit



Compal Electronics, Inc.

Title: POWER CONTROL

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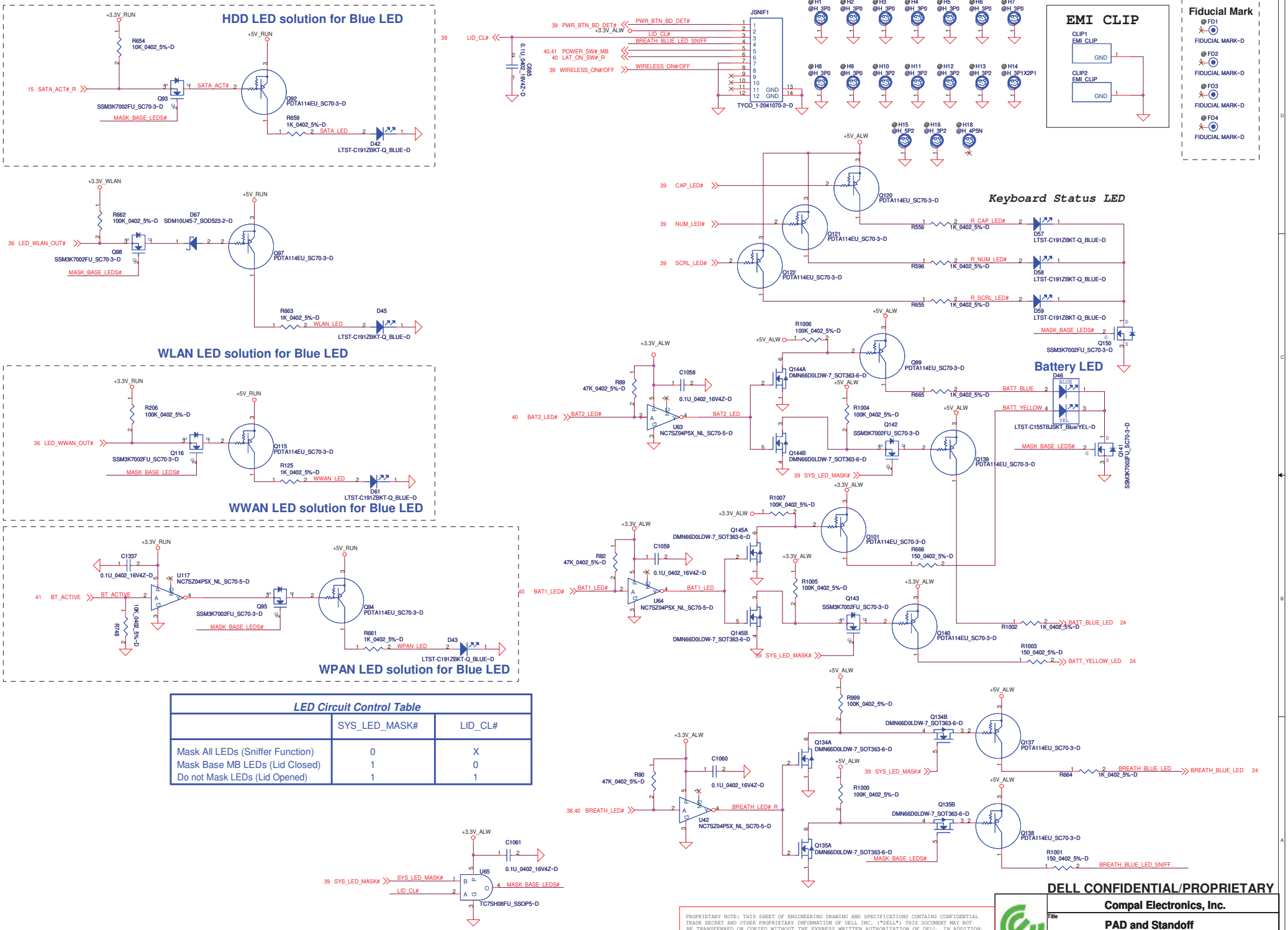
HDD LED solution for Blue LED
WLAN LED solution for Blue LED
WWAN LED solution for Blue LED
WPAN LED solution for Blue LED
EMI CLIP
Fiducial Mark
Keyboard Status LED
Battery LED
LED Circuit Control Table
SYS_LED_MASK#
LID_CL#
Mask All LEDs (Sniffer Function) 0 X
Mask Base MB LEDs (Lid Closed) 1 0
Do not Mask LEDs (Lid Opened) 1 1
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
PAD and Standoff
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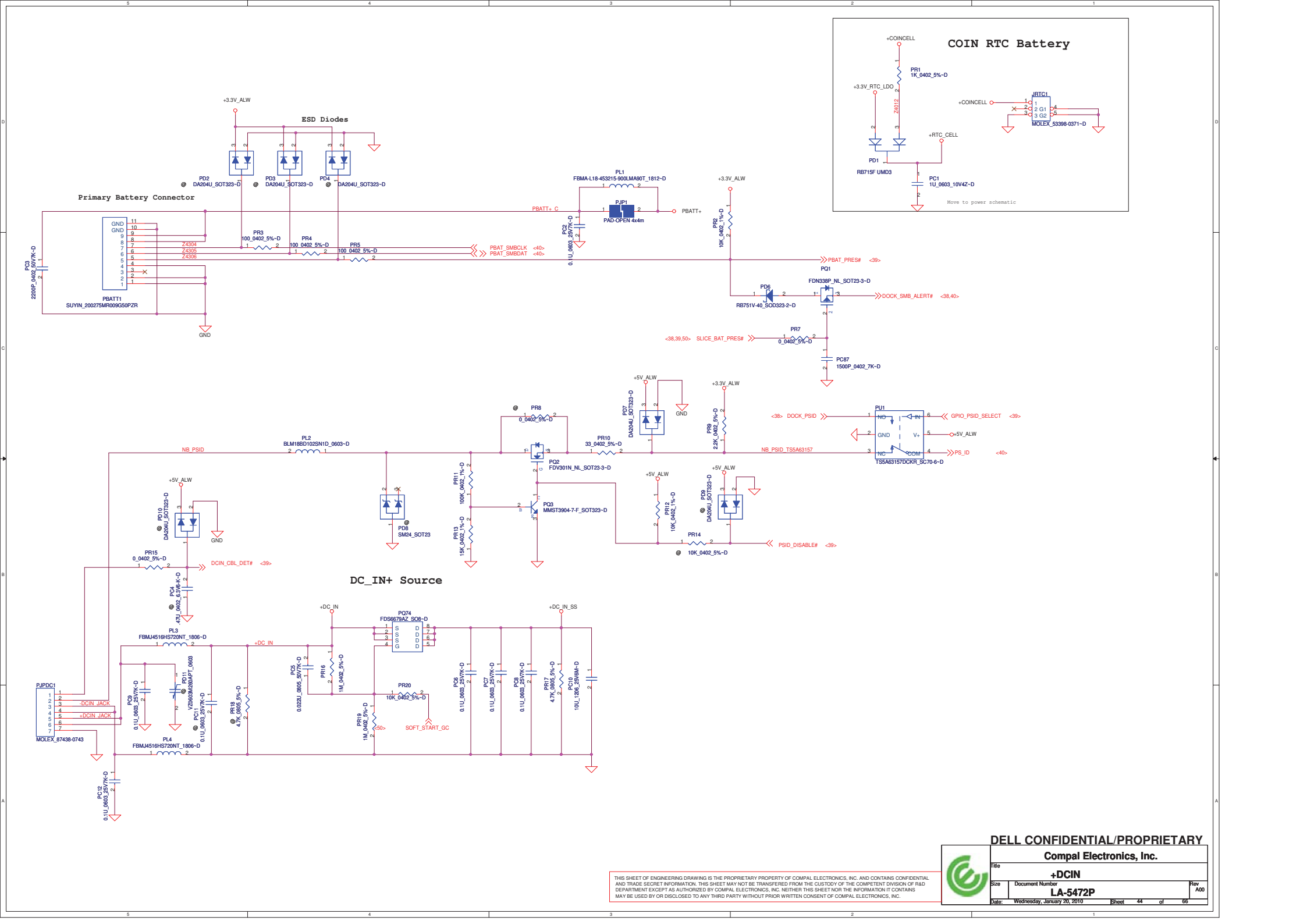

Compal Electronics, Inc.

Title: +DCIN

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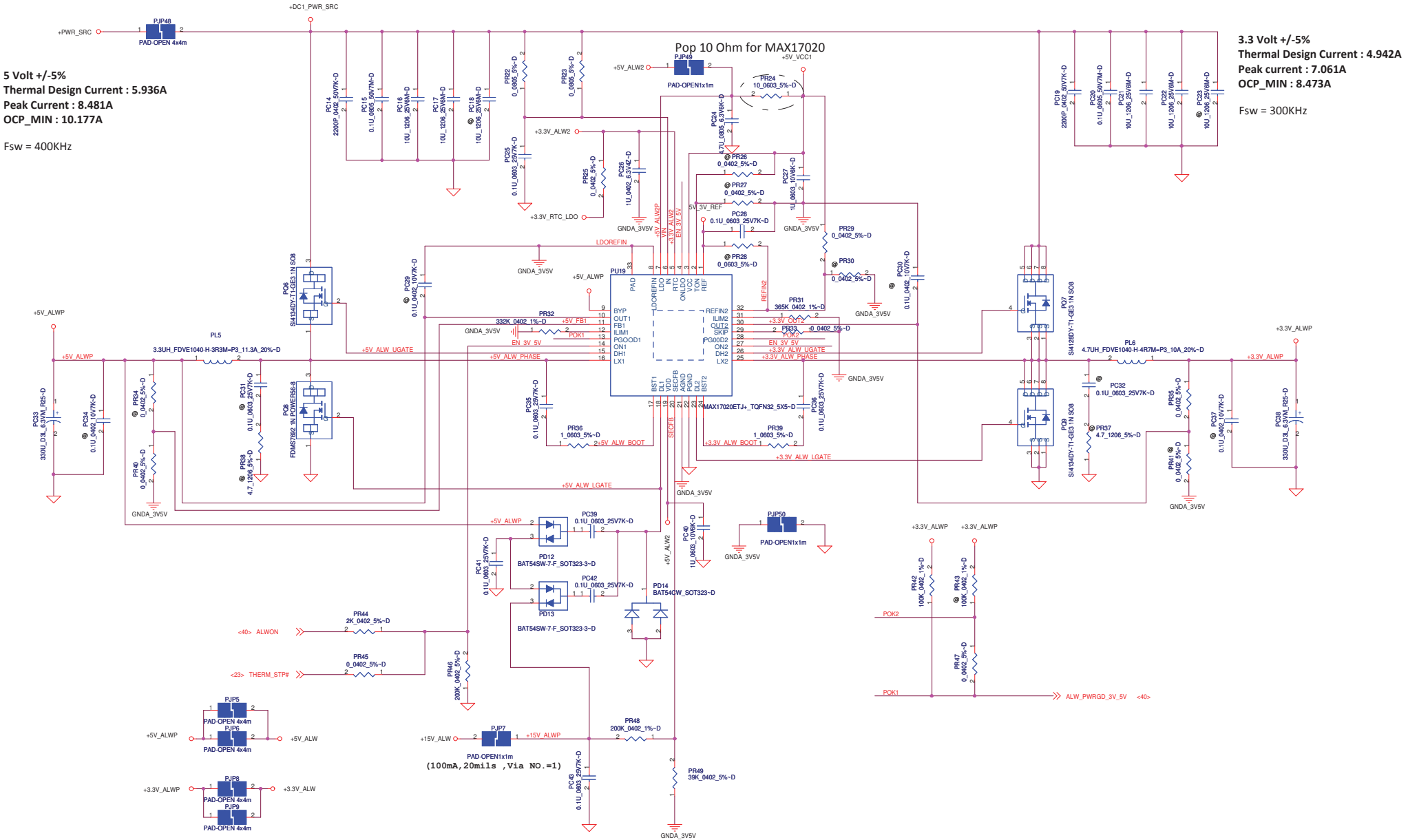
+3.3V_ALWP/ +5V_ALWP/ +5V_ALW2 / +15V_ALWP/ +3.3V_RTC_LDO



Compal Electronics, Inc.		
Title: DC/DC +3V/ +5V		
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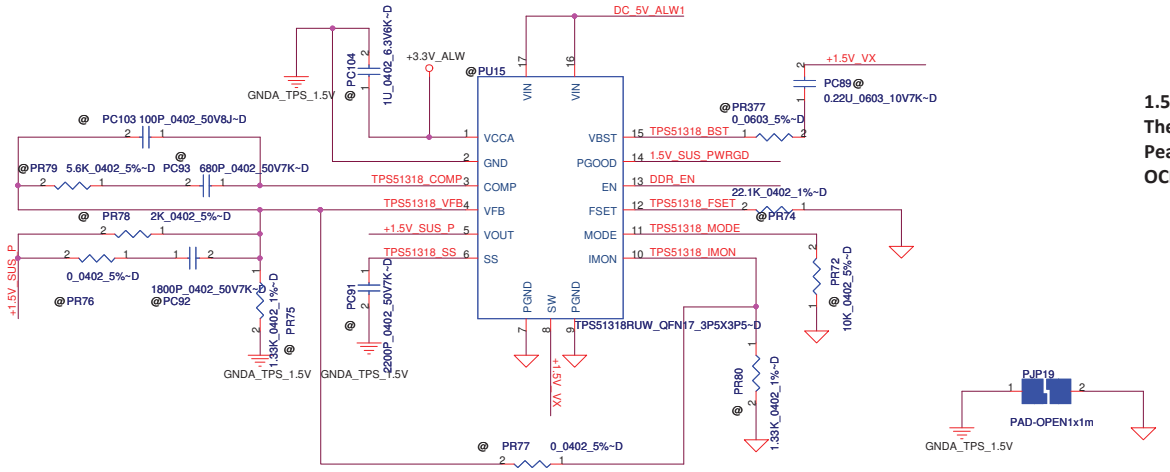
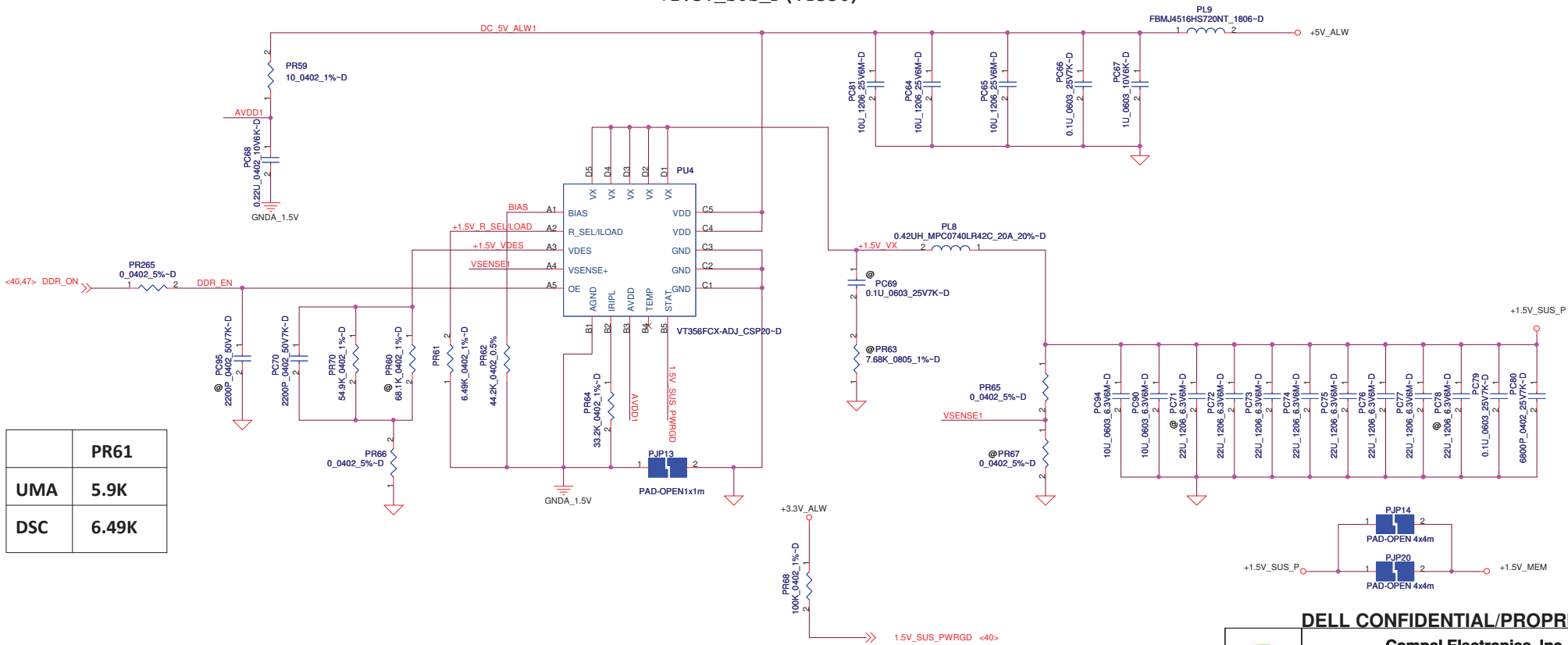
+1.5V_SUS_P (TPS51318)



1.5 Volt +/-5%
Thermal Design Current : 7.876A
Peak current : 11.251A
OCP_MIN : 13.501A

+1.5V_SUS_P (VT356)



	PR61
UMA	5.9K
DSC	6.49K

Compal Electronics, Inc.

Title	+1.5V_MEM	
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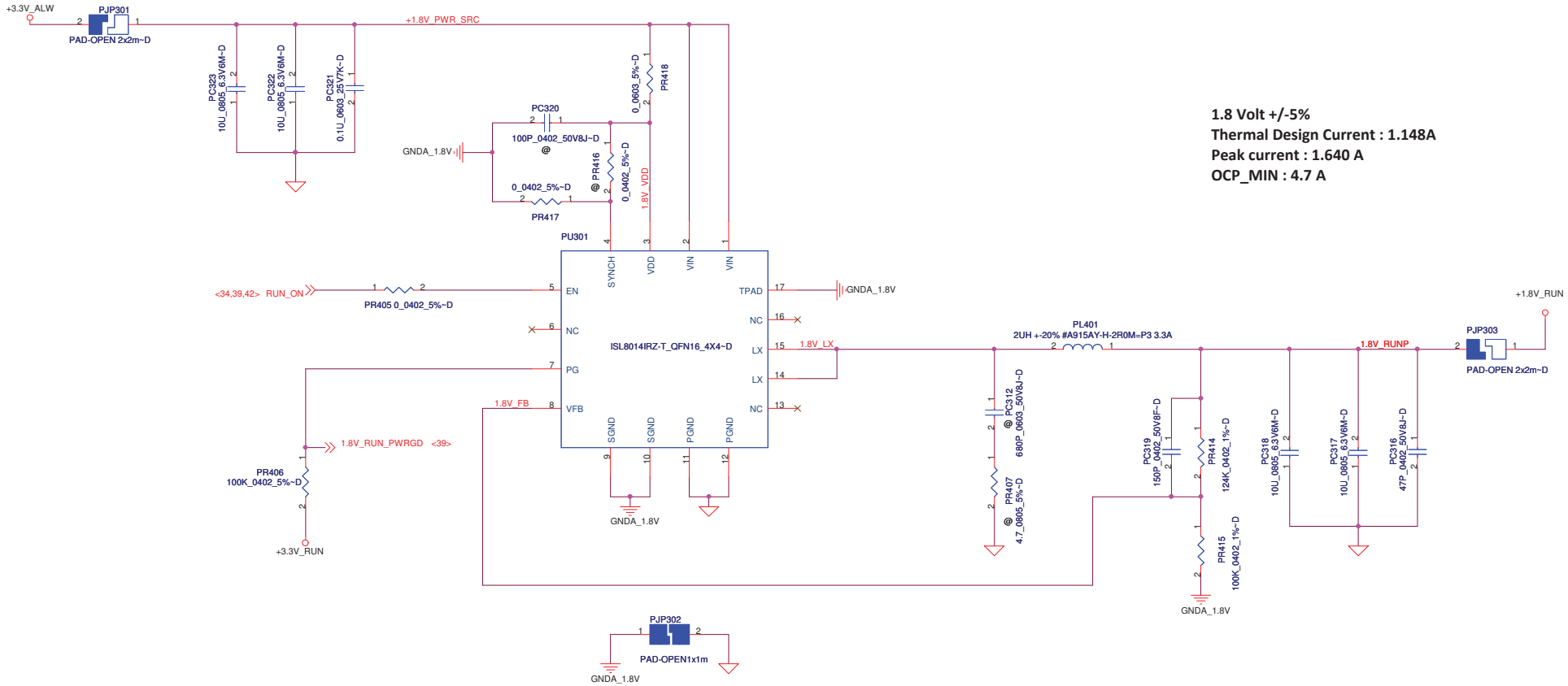
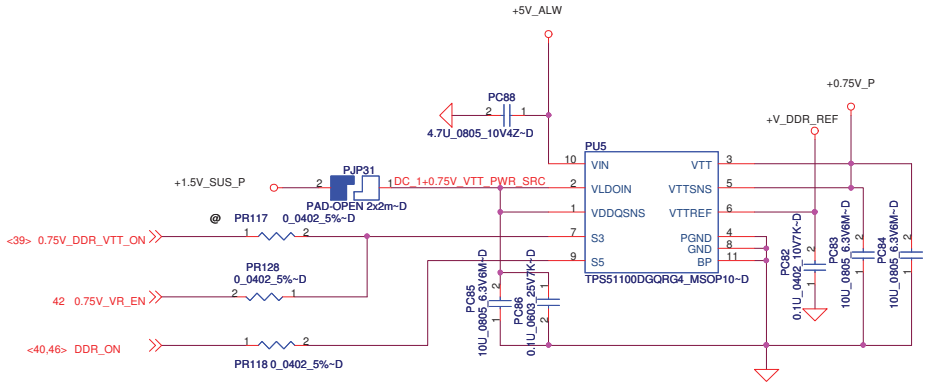
+1.8V_RUN



1.8 Volt +/-5%
Thermal Design Current : 1.148A
Peak current : 1.640 A
OCP_MIN : 4.7 A

+0.75V_DDR_VTT

DDR3 Termination



0.75Volt +/-5%
Thermal Design Current: 0.525A
Peak current: 0.750A
OCP mini: 0.900A

Compal Electronics, Inc.

Title: +0.75V_DDR_VT/+1.8V_RUN

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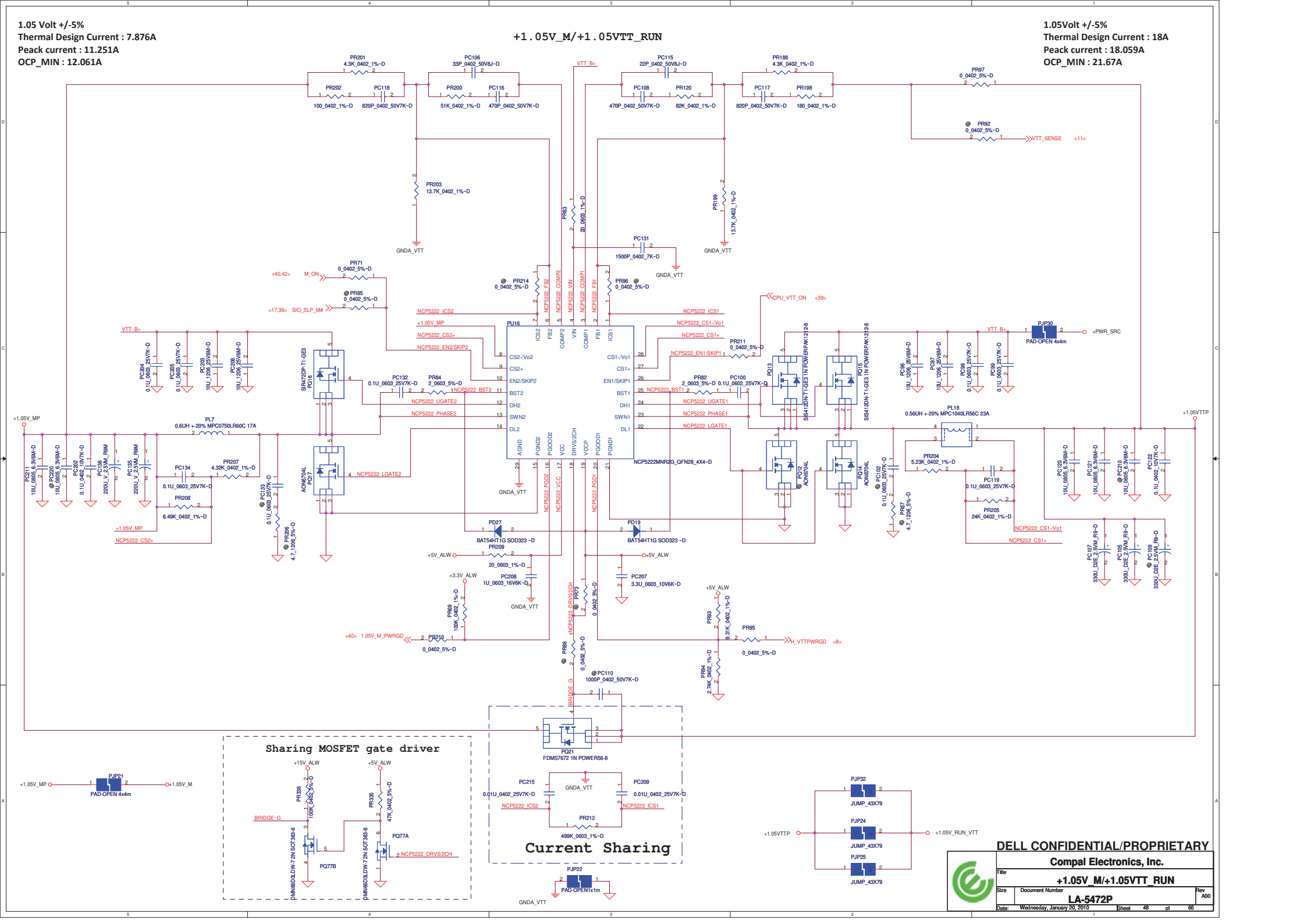
1.05 Volt +/-5%
Thermal Design Current : 7.876A
Peack current : 11.251A
OCP_MIN : 12.061A

+1.05V_M/+1.05VTT_RUN

1.05Volt +/-5%
Thermal Design Current : 18A
Peack current : 18.059A
OCP_MIN : 21.67A



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Compal Electronics, Inc.

Title	+1.05V_M/+1.05VTT_RUN	
Size	Document Number	Rev
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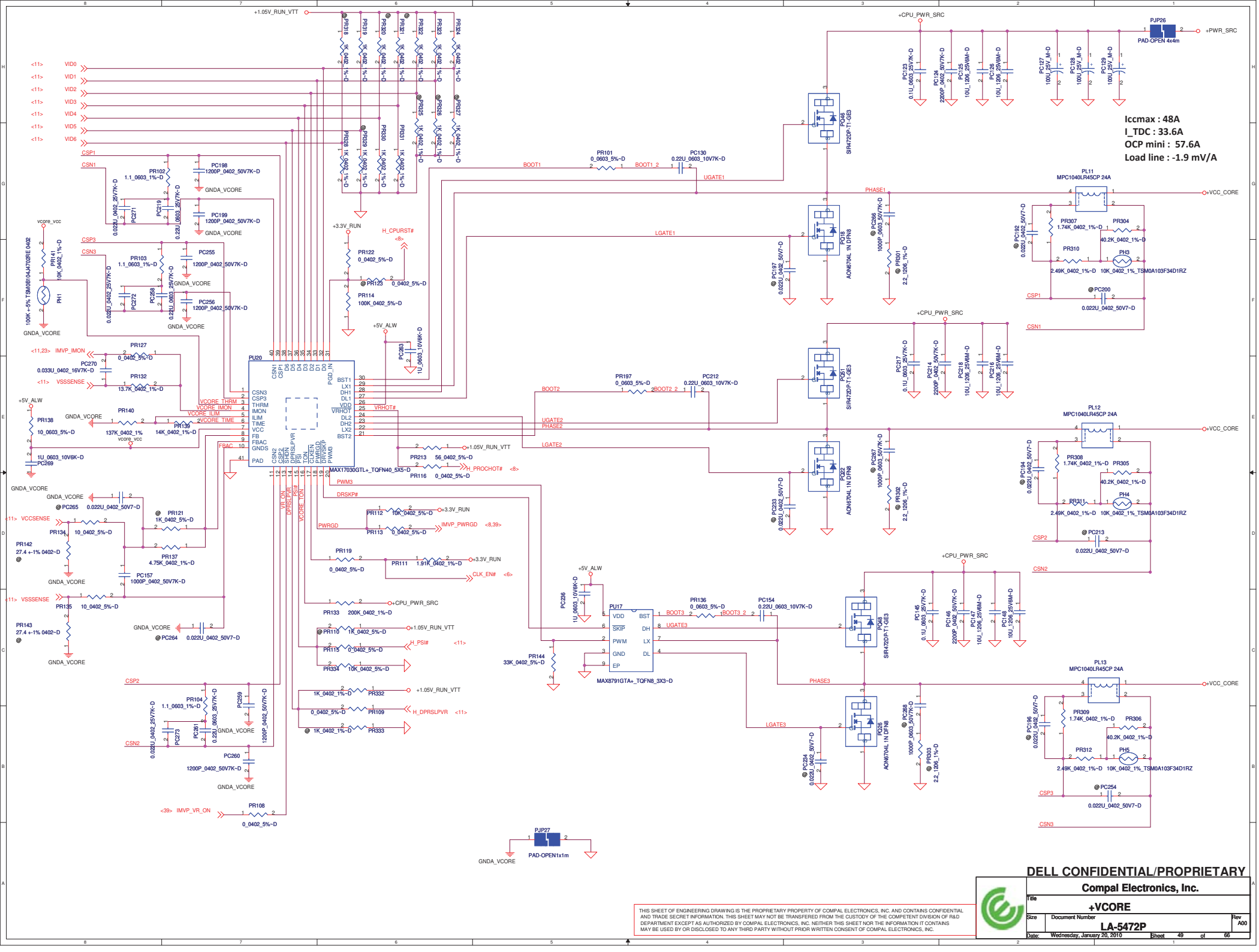

Compal Electronics, Inc.

Title: +VCORE

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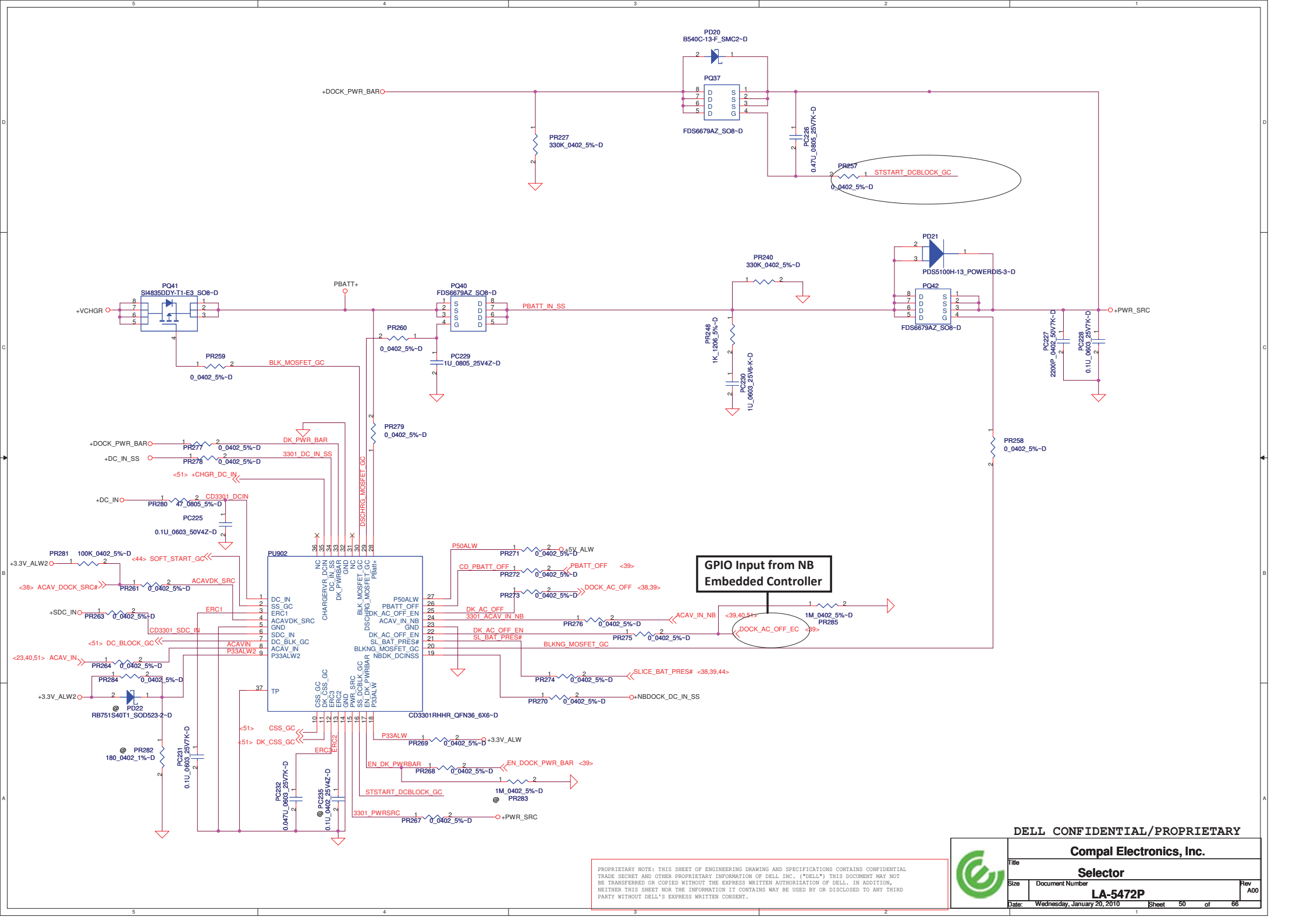

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Compal Electronics, Inc.	
Title	Selector
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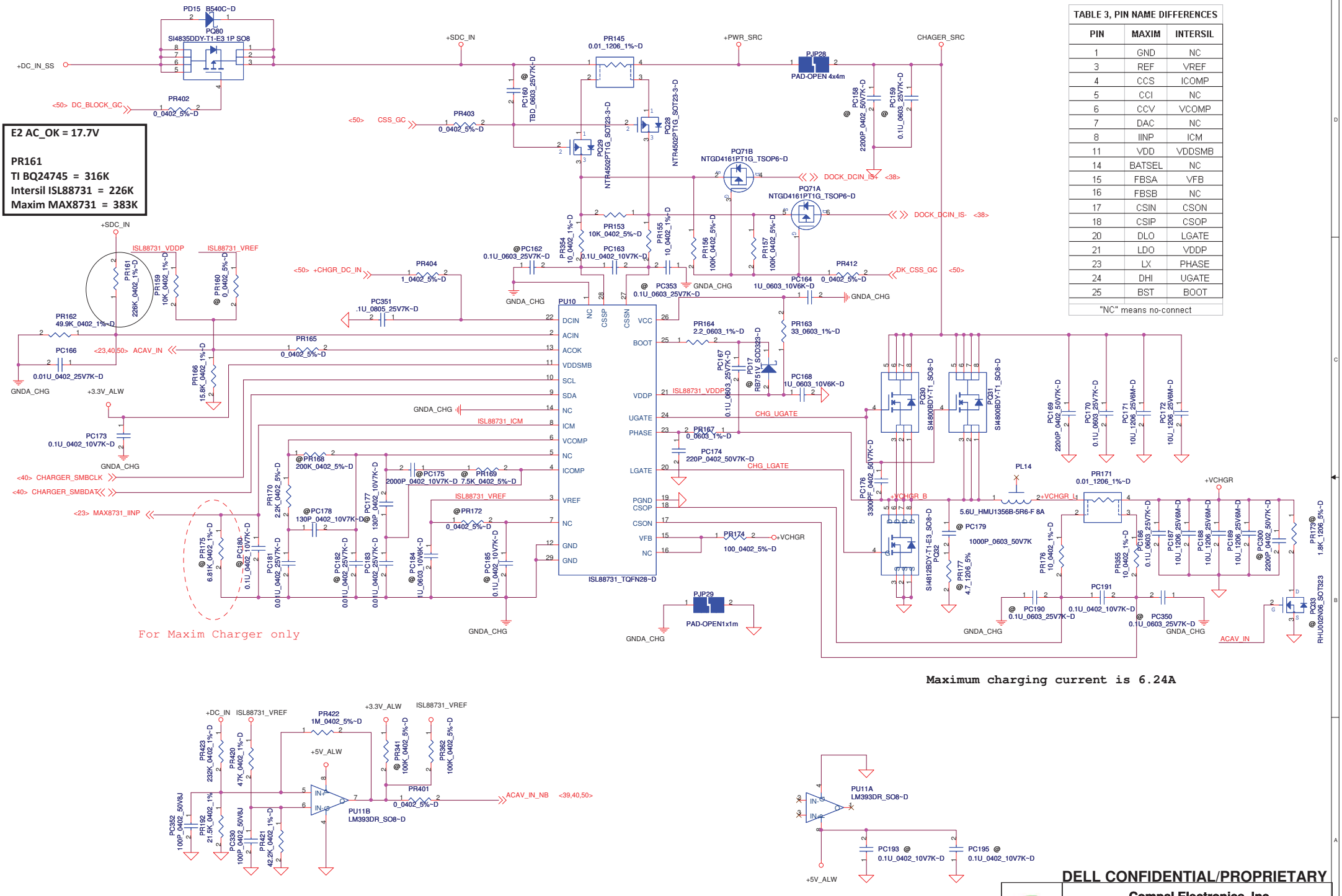
E2 AC_OK = 17.7V
PR161
TI BQ24745 = 316K
Intersil ISL88731 = 226K
Maxim MAX8731 = 383K
TABLE 3, PIN NAME DIFFERENCES
PIN | MAXIM | INTERSIL
1 | GND | NC
3 | REF | VREF
4 | CCS | ICOMP
5 | CCI | NC
6 | CCV | VCOMP
7 | DAC | NC
8 | IINP | ICM
11 | VDD | VDDSMB
14 | BATSEL | NC
15 | FBSA | VFB
16 | FBSB | NC
17 | CSIN | CSON
18 | CSIP | CSOP
20 | DLO | LGATE
21 | LDO | VDDP
23 | LX | PHASE
24 | DHI | UGATE
25 | BST | BOOT
"NC" means no-connect
For Maxim Charger only
Maximum charging current is 6.24A
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
Charger
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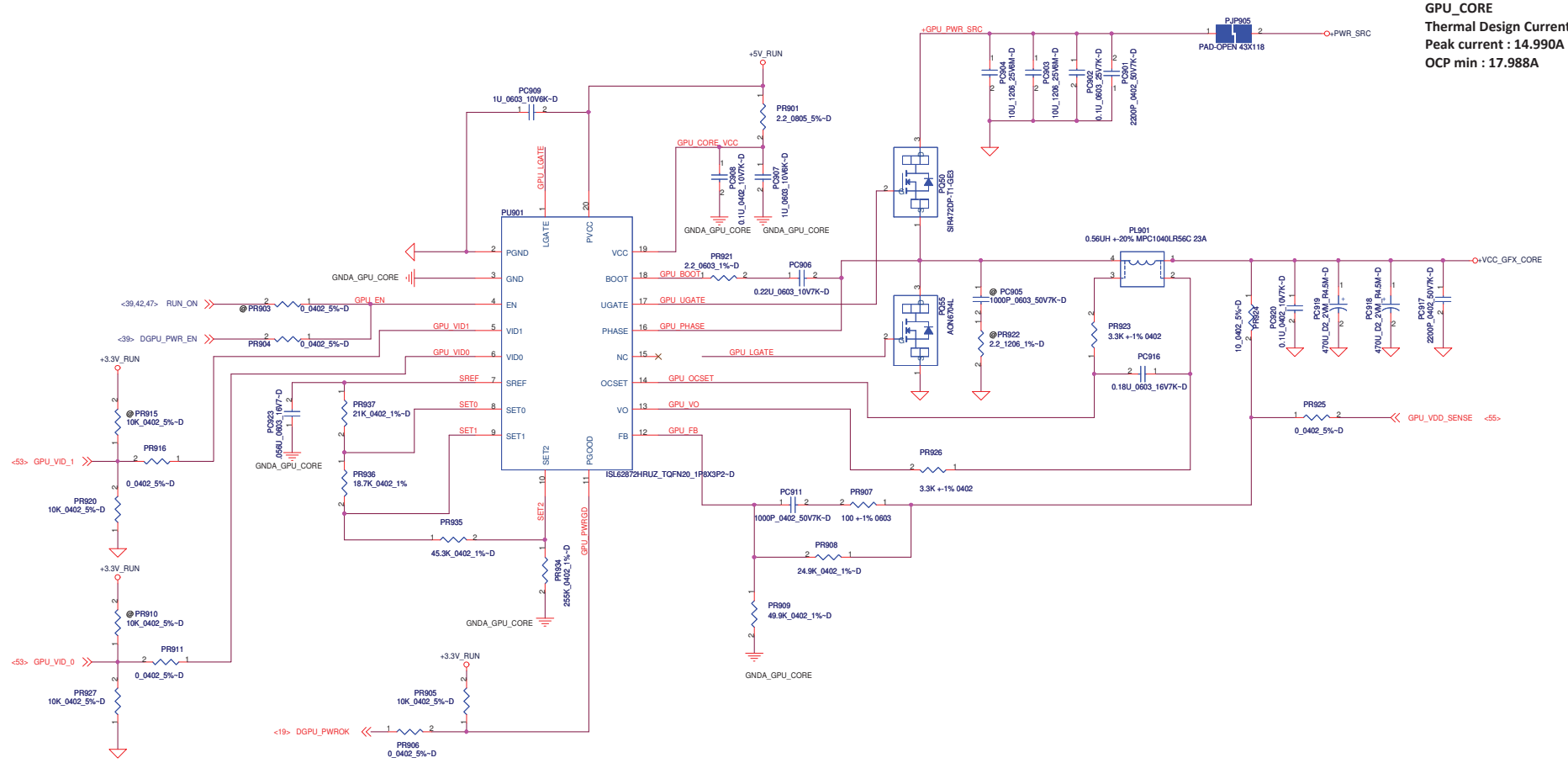

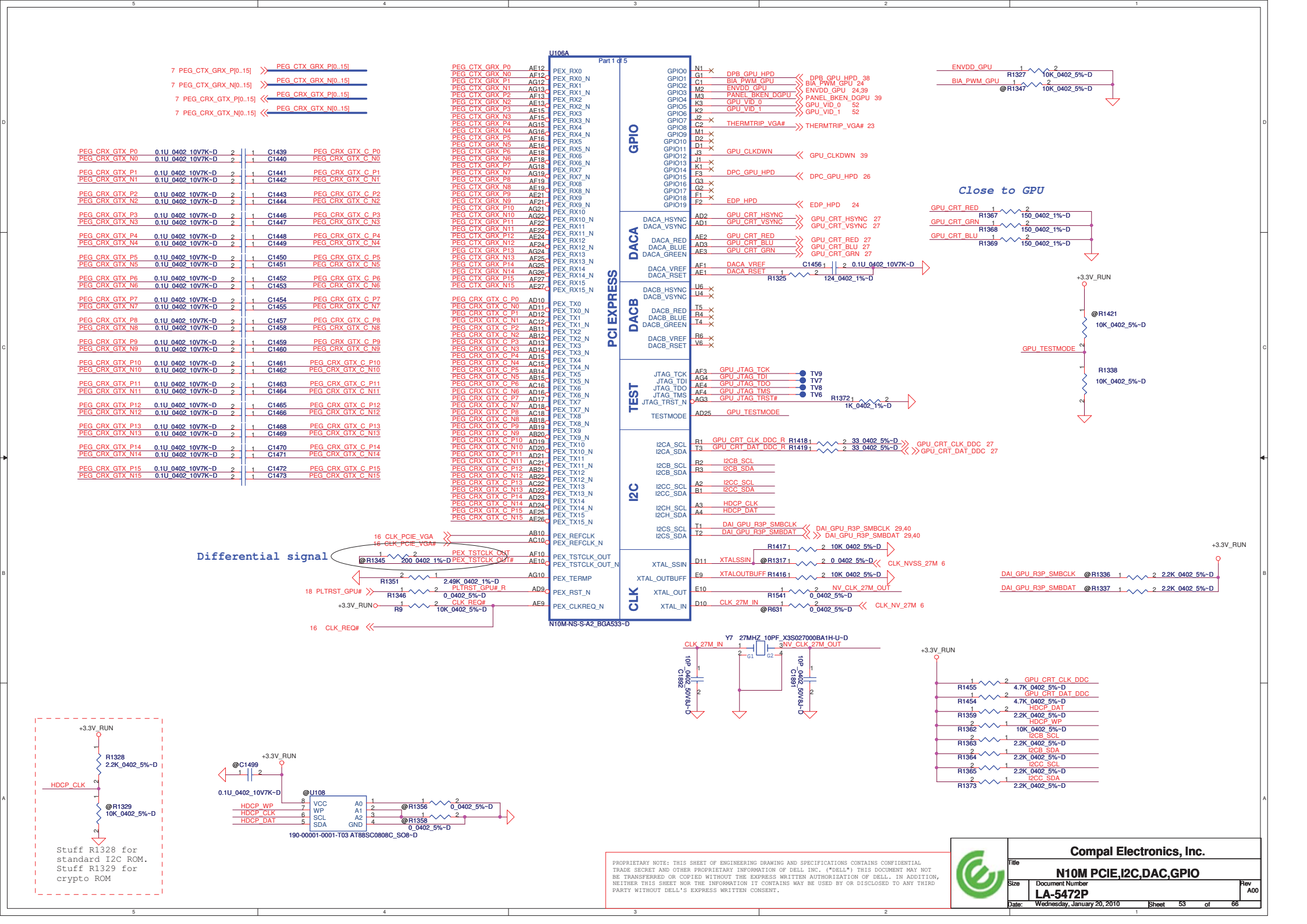

Compal Electronics, Inc.

Title: N10M PCIE,I2C,DAC,GPIO

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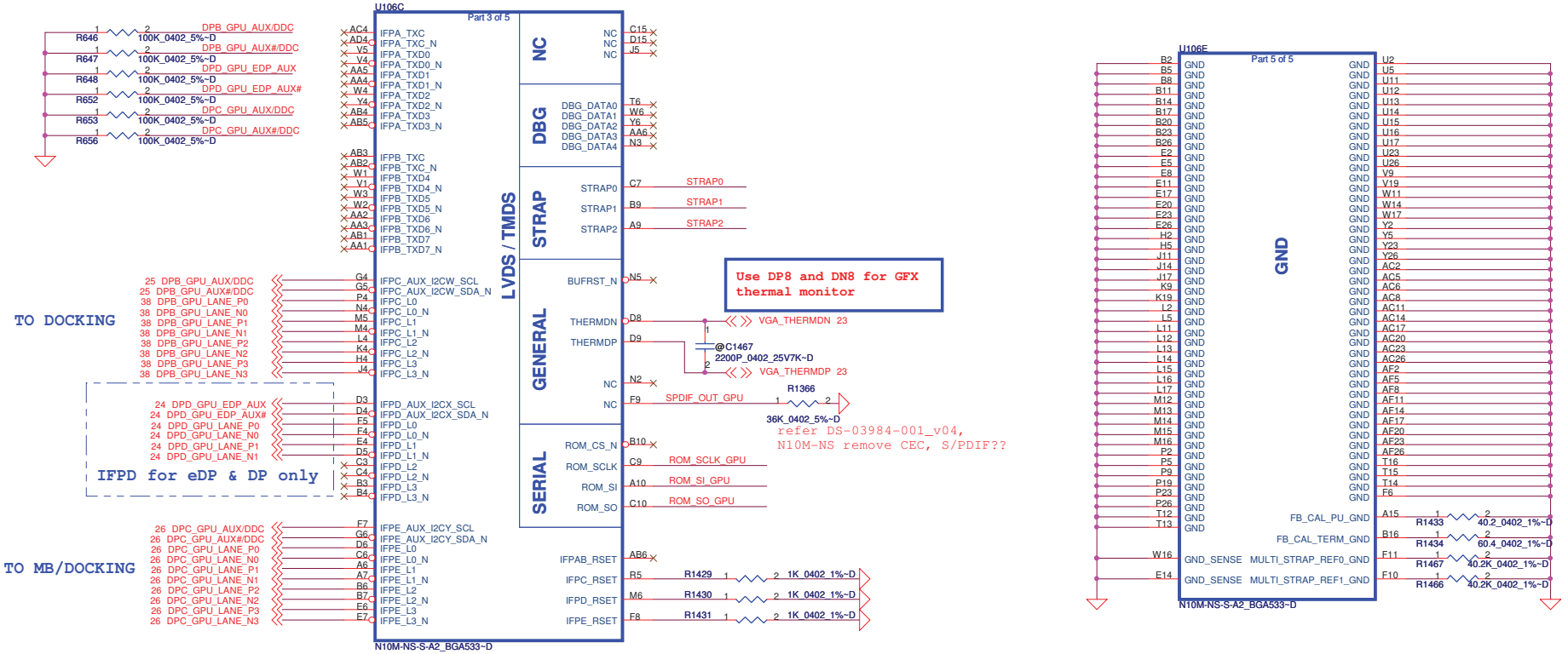

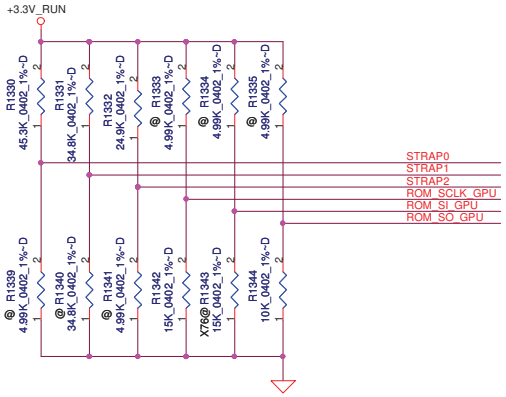

Resistor Values	Pull-up to +3V	Pull-down to Gnd
5K	01111	11111
10K	01110	11110
15K	01011	11011
20K	01001	11001
25K	00111	10111
30K	00110	10110
35K	00011	10011
45K	00000	100000

X7620431001:for Hynix 64Mx16 DDR3 part stuff R1343=15K
X7620431002:For Samsung 64Mx16 DDR3 part stuff R1343=20K

STRAP0	USER[3:0]
STRAP1	3GIO_PADCFG_LUT_ADR[3:0]
STRAP2	PCI_DEVID[3:0]

ROM_SCLK	PCIDEVID_EXT, SUB_VENDOR, SLOT_CLK, PEX_PLL_EN
ROM_SI	RAM_CFG[3:0]
ROM_SO	XCLK_417, FB_0_BAR_SIZE, ALT_ADOOR, VGA_DEVICE

Compal Electronics, Inc.

Title: N10M DP, STRAP, GND

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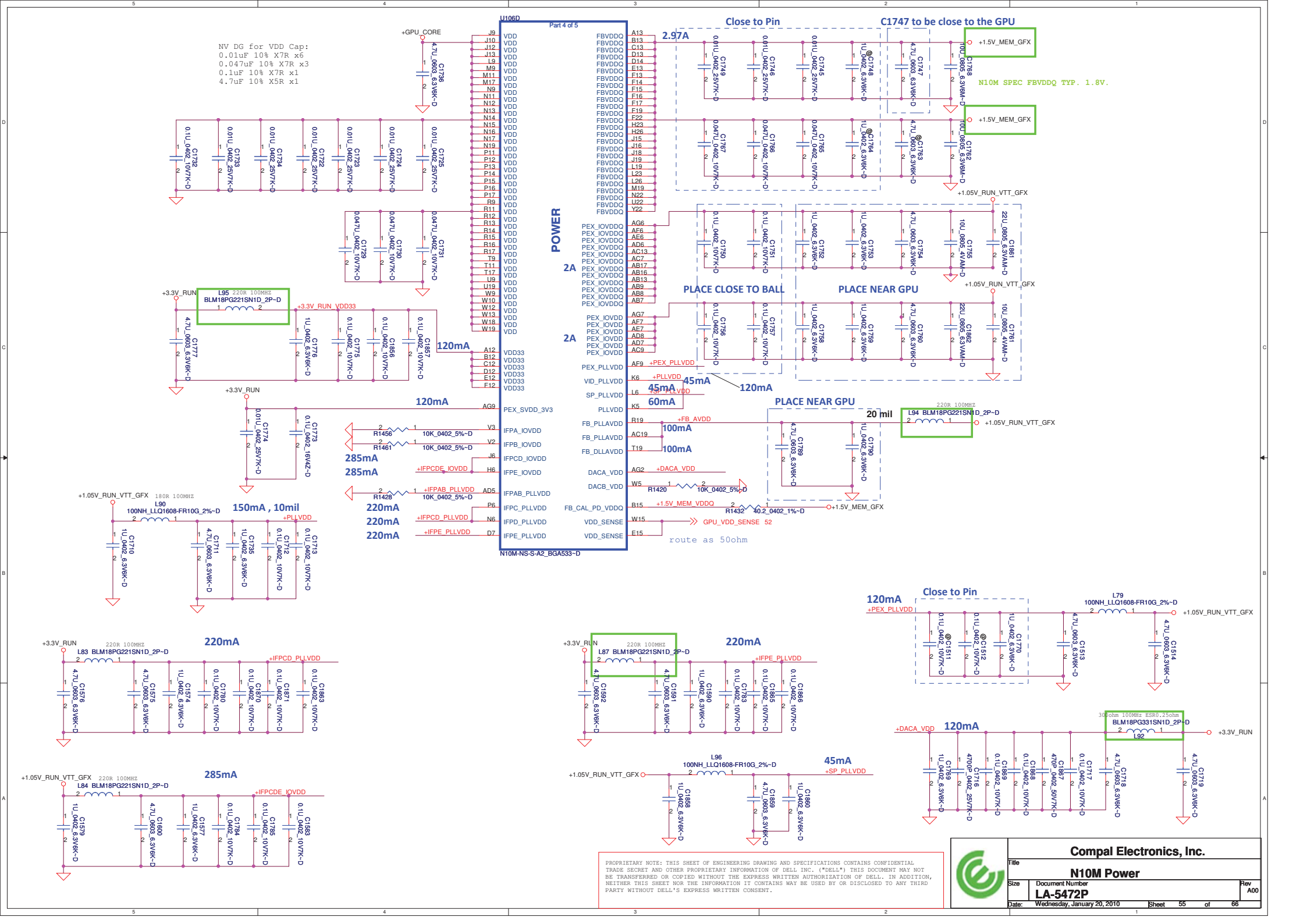
NV DG for VDD Cap:
0.01uF 10% X7R x6
0.047uF 10% X7R x3
0.1uF 10% X7R x1
4.7uF 10% X5R x1
U106D
Part 4 of 5
POWER
N10M-NS-S-A2_BGA533~D
+GPU_CORE
2.97A
Close to Pin
C1747 to be close to the GPU
+1.5V_MEM_GFX
N10M SPEC FBVDDQ TYP. 1.8V.
+1.05V_RUN_VTT_GFX
PLACE CLOSE TO BALL
PLACE NEAR GPU
2A
+3.3V_RUN
+3.3V_RUN_VDD33
120mA
+PEX_PLLVDD
+PLLVDD
45mA
60mA
+FB_AVDD
100mA
+DACA_VDD
+1.5V_MEM_VDDQ
GPU_VDD_SENSE 52
route as 50ohm
285mA
220mA
150mA , 10mil
+1.05V_RUN_VTT_GFX 180R 100MHZ
L90 100NH_LLQ1608-FR10G_2%~D
+IFPCDE_IOVDD
+IFPAB_PLLVDD
+IFPCD_PLLVDD
+IFPE_PLLVDD
+SP_PLLVDD
L94 BLM18PG221SN1D_2P~D
20 mil
+3.3V_RUN 220R 100MHZ
L83 BLM18PG221SN1D_2P~D
L87 BLM18PG221SN1D_2P~D
+1.05V_RUN_VTT_GFX 220R 100MHZ
L84 BLM18PG221SN1D_2P~D
L96 100NH_LLQ1608-FR10G_2%~D
L79 100NH_LLQ1608-FR10G_2%~D
300ohm 100MHz ESR0.25ohm
BLM18PG331SN1D_2P~D
L92
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Compal Electronics, Inc.
Title
N10M Power
Size
Document Number
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Rev
A00
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FBAD[0..63] FBAD[0..63] 57,58
FBA_CMD[0..30] FBA_CMD[0..30] 57,58
DQMA#[0..7] DQMA#[0..7] 57,58
DQSA_RN[0..7] DQSA_RN[0..7] 57,58
DQSA_WP[0..7] DQSA_WP[0..7] 57,58

FBA_CMD0 — 10K_0402_5%~D R1380
FBA_CMD16 — 10K_0402_5%~D R1382
FBA_CMD25 — 10K_0402_5%~D R1384
FBA_CMD27 — 10K_0402_5%~D R1386
FBA_CMD28 — 10K_0402_5%~D R1387

+1.5V_MEM_GFX — 1.1K_0402_1%~D @R1378 — 16mil — +FB_VREF — 1.1K_0402_1%~D @R1377 — @C1502 0.01U_0402_25V7K~D

U106B
Part 2 of 5
MEMORY INTERFACE
N10M-NS-S-A2_BGA533~D

FBAD0	D22	FBA_D0	FBA_CMD0	F26	FBA_CMD0
FBAD1	E24	FBA_D1	FBA_CMD1	J24	FBA_CMD1
FBAD2	E22	FBA_D2	FBA_CMD2	F25	FBA_CMD2
FBAD3	D24	FBA_D3	FBA_CMD3	M23	FBA_CMD3
FBAD4	D26	FBA_D4	FBA_CMD4	N27	FBA_CMD4
FBAD5	D27	FBA_D5	FBA_CMD5	M27	FBA_CMD5
FBAD6	C27	FBA_D6	FBA_CMD6	K26	FBA_CMD6
FBAD7	B27	FBA_D7	FBA_CMD7	J25	FBA_CMD7
FBAD8	A21	FBA_D8	FBA_CMD8	J27	FBA_CMD8
FBAD9	B21	FBA_D9	FBA_CMD9	G23	FBA_CMD9
FBAD10	C21	FBA_D10	FBA_CMD10	G26	FBA_CMD10
FBAD11	C19	FBA_D11	FBA_CMD11	J23	FBA_CMD11
FBAD12	C18	FBA_D12	FBA_CMD12	M25	FBA_CMD12
FBAD13	D18	FBA_D13	FBA_CMD13	K27	FBA_CMD13
FBAD14	B18	FBA_D14	FBA_CMD14	G25	FBA_CMD14
FBAD15	C16	FBA_D15	FBA_CMD15	L24	FBA_CMD15
FBAD16	E21	FBA_D16	FBA_CMD16	K23	FBA_CMD16
FBAD17	F21	FBA_D17	FBA_CMD17	K24	FBA_CMD17
FBAD18	D20	FBA_D18	FBA_CMD18	G22	FBA_CMD18
FBAD19	F20	FBA_D19	FBA_CMD19	K25	FBA_CMD19
FBAD20	D17	FBA_D20	FBA_CMD20	H22	FBA_CMD20
FBAD21	F18	FBA_D21	FBA_CMD21	M26	FBA_CMD21
FBAD22	D16	FBA_D22	FBA_CMD22	H24	FBA_CMD22
FBAD23	E16	FBA_D23	FBA_CMD23	F27	FBA_CMD23
FBAD24	A22	FBA_D24	FBA_CMD24	J26	FBA_CMD24
FBAD25	C24	FBA_D25	FBA_CMD25	G24	FBA_CMD25
FBAD26	D21	FBA_D26	FBA_CMD26	G27	FBA_CMD26
FBAD27	B22	FBA_D27	FBA_CMD27	M24	FBA_CMD27
FBAD28	C22	FBA_D28	FBA_CMD28	K22	FBA_CMD28
FBAD29	A25	FBA_D29	FBA_CMD29	J22	FBA_CMD29
FBAD30	B25	FBA_D30	FBA_CMD30	L22	FBA_CMD30
FBAD31	A26	FBA_D31			
FBAD32	U24	FBA_D32	FBA_DQM0	C26	DQMA#0
FBAD33	V24	FBA_D33	FBA_DQM1	B19	DQMA#1
FBAD34	V23	FBA_D34	FBA_DQM2	D19	DQMA#2
FBAD35	R24	FBA_D35	FBA_DQM3	D23	DQMA#3
FBAD36	T23	FBA_D36	FBA_DQM4	T24	DQMA#4
FBAD37	R23	FBA_D37	FBA_DQM5	AA23	DQMA#5
FBAD38	P24	FBA_D38	FBA_DQM6	AB27	DQMA#6
FBAD39	P22	FBA_D39	FBA_DQM7	T26	DQMA#7
FBAD40	AC24	FBA_D40			
FBAD41	AB23	FBA_D41	FBA_DQS_RN0	D25	DQSA_RN0
FBAD42	AB24	FBA_D42	FBA_DQS_RN1	A18	DQSA_RN1
FBAD43	W24	FBA_D43	FBA_DQS_RN2	E18	DQSA_RN2
FBAD44	AA22	FBA_D44	FBA_DQS_RN3	B24	DQSA_RN3
FBAD45	W23	FBA_D45	FBA_DQS_RN4	R22	DQSA_RN4
FBAD46	W22	FBA_D46	FBA_DQS_RN5	Y24	DQSA_RN5
FBAD47	V22	FBA_D47	FBA_DQS_RN6	AA27	DQSA_RN6
FBAD48	AA25	FBA_D48	FBA_DQS_RN7	R27	DQSA_RN7
FBAD49	W27	FBA_D49			
FBAD50	W26	FBA_D50	FBA_DQS_WP0	C25	DQSA_WP0
FBAD51	W25	FBA_D51	FBA_DQS_WP1	A19	DQSA_WP1
FBAD52	AB25	FBA_D52	FBA_DQS_WP2	E19	DQSA_WP2
FBAD53	AB26	FBA_D53	FBA_DQS_WP3	A24	DQSA_WP3
FBAD54	AD26	FBA_D54	FBA_DQS_WP4	T22	DQSA_WP4
FBAD55	AD27	FBA_D55	FBA_DQS_WP5	AA24	DQSA_WP5
FBAD56	V25	FBA_D56	FBA_DQS_WP6	AA26	DQSA_WP6
FBAD57	R25	FBA_D57	FBA_DQS_WP7	T27	DQSA_WP7
FBAD58	V26	FBA_D58			
FBAD59	V27	FBA_D59	FB_VREF	A16	+FB_VREF
FBAD60	R26	FBA_D60			
FBAD61	T25	FBA_D61	FBA_CLK0	F24	CLKA0 57
FBAD62	N25	FBA_D62	FBA_CLK0_N	F23	CLKA0# 57
FBAD63	N26	FBA_D63			
			FBA_CLK1	N24	CLKA1 58
			FBA_CLK1_N	N23	CLKA1# 58
			FBA_DEBUG	M22	R1378 1 2 10K_0402_5%~D +1.5V_MEM_GFX

PAD~D T32@
PAD~D T31@

Mode C – Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	BA0
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2

+1.5V_MEM_GFX Source

+3.3V_ALW2 — R643 100K_0402_5%~D — GFX_MEM_VTT_ON# 5 — Q197A DMN66D0LDW-7_SOT363-6~D — 39 GFX_MEM_VTT_ON
+15V_ALW — R642 100K_0402_5%~D — Q197B DMN66D0LDW-7_SOT363-6~D — GFX_MEM_VTT_EN
+1.5V_MEM — Q58 SI4164DY-T1-GE3_SO8~D — 2200P_0402_50V7K~D C715
+1.5V_MEM_GFX — 10U_0805_10V4Z~D C714 — 20K_0402_5%~D R641

+1.05V_RUN_VTT_GFX Source

+15V_ALW — R645 100K_0402_5%~D — Q198 SSM3K7002FU_SC70-3~D — 1.05V_RUN_VTT_GFX# EN
+1.05V_M — Q59 SI4164DY-T1-GE3_SO8~D — 2200P_0402_50V7K~D C716
+1.05V_RUN_VTT_GFX — 10U_0805_10V4Z~D C717 — 20K_0402_5%~D R644

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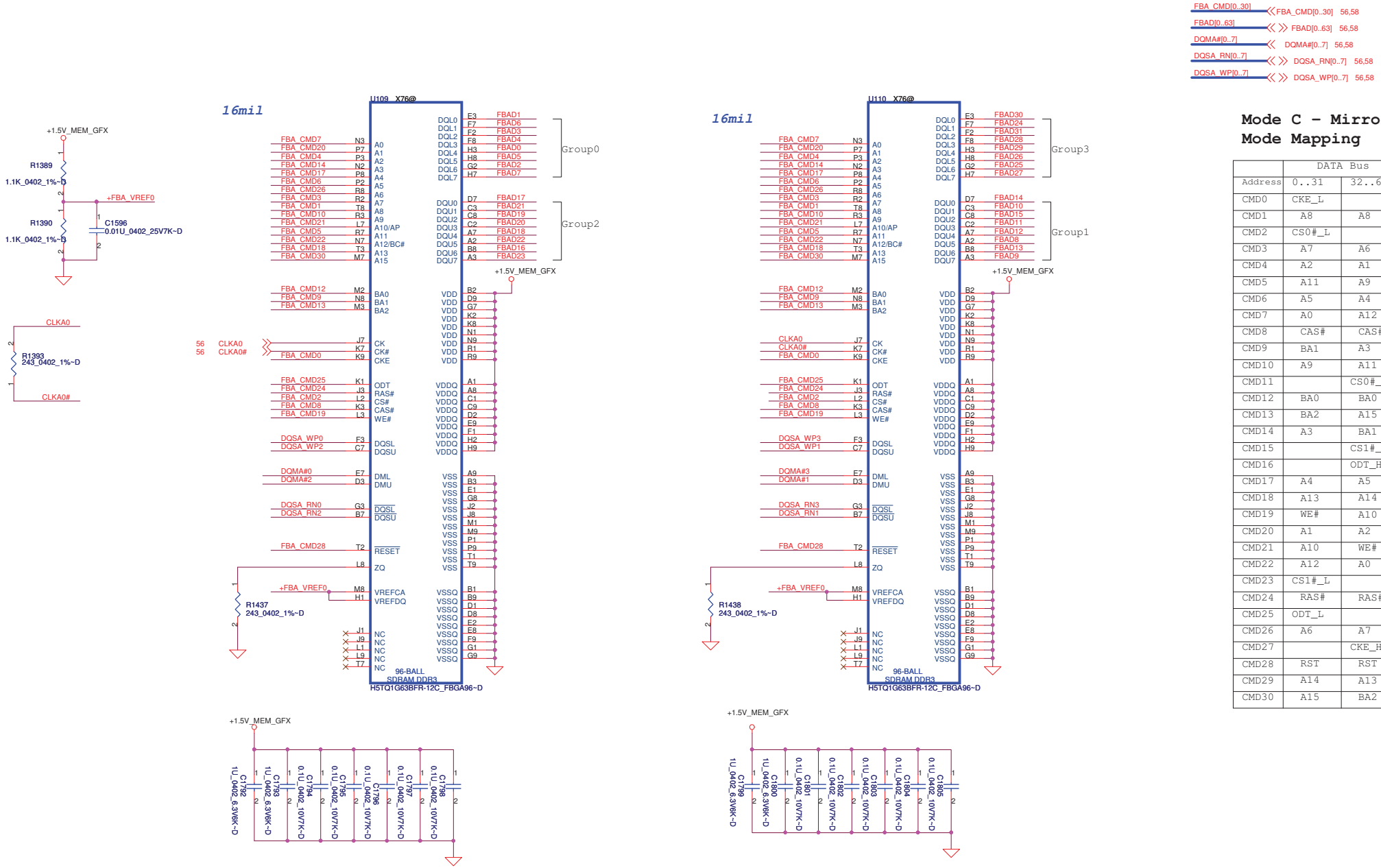
Memory Partition A – Lower 32 bits



Mode C – Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	BA0
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2

Compal Electronics, Inc.
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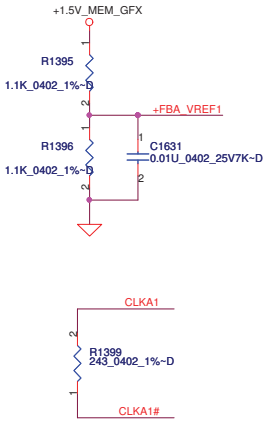
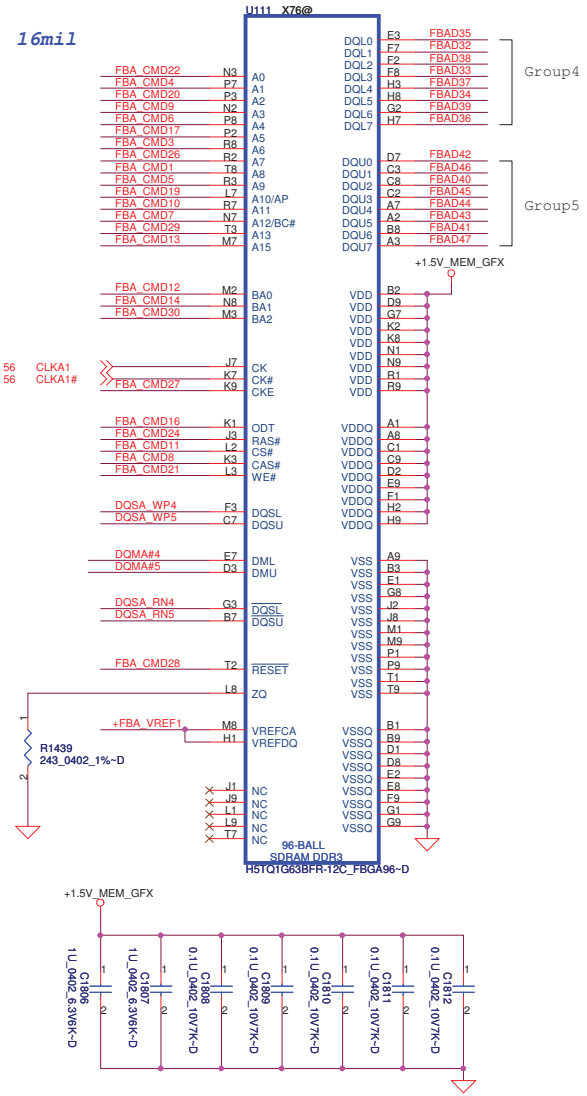
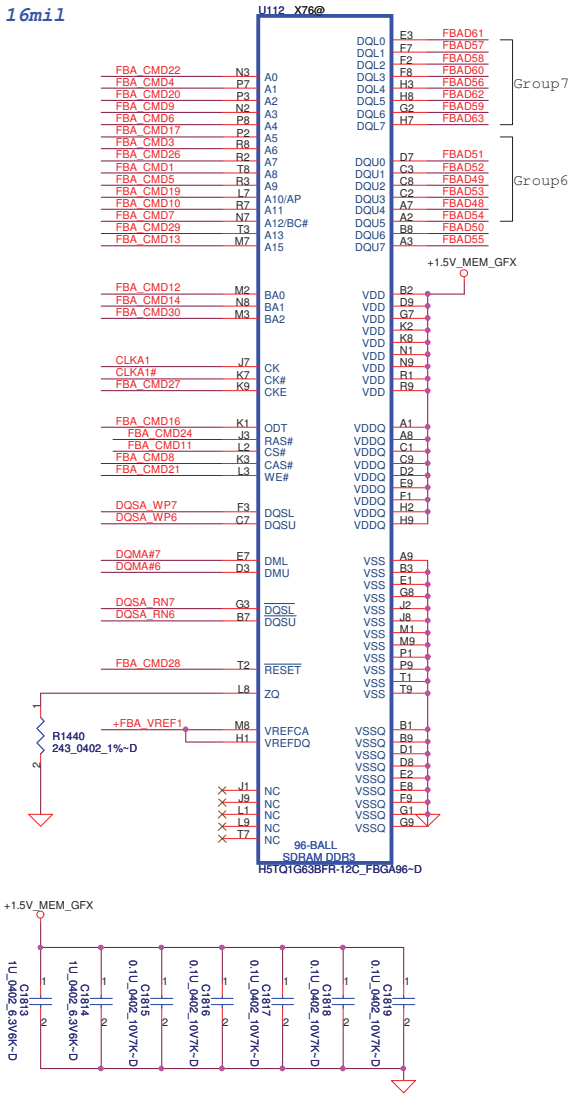
Memory Partition A - Upper 32 bits







FBAD[0..63] FBAD[0..63] 56,57
FBA_CMD[0..30] FBA_CMD[0..30] 56,57
DQMA#[0..7] DQMA#[0..7] 56,57
DQSA_RN[0..7] DQSA_RN[0..7] 56,57
DQSA_WP[0..7] DQSA_WP[0..7] 56,57

Mode C - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	BA0
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2

Compal Electronics, Inc.
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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	40	HW	7/13/2009	COMPAL	Board ID	R98 change to 130k ohm	X01
2	30	HW	7/13/2009	COMPAL	follow M09 +3.3V_LAN enable control circuit	Depop R47	X01
3	8, 12, 13, 42	HW	7/13/2009	Intel	Intel S3 reduction circuit.	Add R1469, R1497~R1505, R1507~R1509, C1875, C1878~C1884, Q199~Q202, Q205, Q207, Q208 , U141, PJP906, PJP907, change R879 to 1.5K, R880 to 750ohm, R624 to 22 ohm, change CPU CDDQ power source from +1.5V_MEM to +1.5V_CPU_VDDQ, change +.075_DDR_VTT discharge gate from RUN_ON_ENABLE# to RUN_ON_CPU1.5VS3#, add +1.5V_CPU_VDDQ discharge circuit, add net "DDR_HVREF_RST_GATE" from U36.A34 to Q119.2, "CPU1.5V_S3_GATE" from U36.A36 to R1501	X01
4	31	HW	7/23/2009	Broadcom	Change C718 value	Change C718 from .47uF to .22uF	X01
5	23	HW	7/23/2009	DELL	Follow DELL request to remove R3P circuit	Delete U140, R136, R138, R156,R507, R516, R519, R529, R531, R534~R536, R594, R1457, R1458, R1462, R1463, C434, C72, C73, C391, C406, pop R142, D2, C219	X01
6	41,37	HW	7/23/2009	Compal	Per M09 lesson learn request	Re-define JTP1, JBIO1	X01
7	19	HW	7/23/2009	Intel	GPIO1, 6, 7 need to PU if no used.	Add R1506, R1510	X01
8	40 43	HW	7/23/2009	Compal	Follow SMSC5045 spec	Add R1512, @C1885, C1886, change R560 to 100Kohm, add net name LAT_ON_SW#_R	X01
9	31	HW	7/23/2009	Broadcom	Remove RFID disable circuit	Remove R1062~R1065	X01
10	24	HW	7/23/2009	Compal	CAM Module change from 7 pin to 8 pin	Change pin define for JEDP1	X01
11	31	HW	7/23/2009	Broadcom	R898 and R485 pop at the same time	Depop R898	X01
12	24	HW	7/29/2009	Compal	NVidia BIA_PWM implementation	POP R165, de-pop R166	X01
13	8,15	HW	7/29/2009	Compal	Depop all related components where are located at 0 Z-hight area	Depop JXDP1, JXDP2, JDEG1, JP2 connector	X01
14	42	HW	7/29/2009	Compal	For load switches Vout over 5% range concern by power team .	Change Q151 to SIS406D,Q183 to SI7658ADP,Q58 to SI4164DY	X01
15	42	HW	7/29/2009	Compal	Backdrive EA Failure on RAM	Pop R625 and Q79, change R625 to 0603 size.	X01
16	21	HW	7/29/2009	Intel	The PLLs aren't used in a DIS system	De-pop C105 & C106	X01
17	36,39	HW	7/29/2009	DELL	Reconnect the signal UWB_RADIO_DIS#	Connect UWB_RADIO_DIS# from EC5028.A56 to MINI3.20	X01
18	24	HW	7/29/2009	PERICOM	Pericom 8200 SW issue DVI can not work	Add R1516 to pull up U9 pin 23 (P1_OC0) of Pericom 8200 SW with a 4.7K ohm resistor to +3.3_RUN	X01
19	29	HW	7/29/2009	Compal	EMI solution.	Change R1295 to L4 (220ohm) and R1217 from 22ohm to 47ohm.	X01
20	42	HW	7/29/2009	Compal	Base on de-rating report.	Change Q61 from AO4456 to NTMS4107.	X01
21	37, 39	HW	7/29/2009	Compal	GPIO MAP update	Add reserved R1513 between U95.18 and +3.3V_RUN, add R1514 between U95.18 and 5028.A47 named EN_ESATA_RPTR.	X01

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
22	31	HW	7/29/2009	Broadcom	Resolve 5882 leackage issue	Add R884, R1515, Q209, Q210	X01
23	31	HW	7/29/2009	Broadcom	Resolve smart cart can't work problem.	pop R775, R537, depop R776.	X01
24	36	HW	7/29/2009	Compal	Change PU power rail for USB_MCARD1_DET#	Change USB_MCARD1_DET# PU power rail to +3.3V_RUN	X01
25	31	HW	7/29/2009	Compal	Remove R1061 to avoid double PU and provide back-drive path.	Remove R1061	X01
26	21	HW	7/29/2009	Compal	Follow the pop option on CRB1.6 to depop C39 for +VCCACLK, C610 for +SATAPLL, C111 and C112 for +1.05V_M_VCCEPW	Depop C610, C39, C111, C112	X01
27	15	HW	7/29/2009	Compal	Base on crystal EA result.	Change external Load Capacitor Value C296 and C297 to 12 pF of Y1.	X01
28	30	HW	7/29/2009	Compal	Base on crystal EA result.	Change external Load Capacitor Value C476 to 33 pF and C427 change to 200 ohm (R808) of Y2.	X01
29	40	HW	7/29/2009	Compal	Base on crystal EA result.	Change external Load Capacitor Value C674 and C675 to 33 pF of Y4.	X01
30	33	HW	7/29/2009	Compal	Base on crystal EA result.	Change external Load Capacitor Value C514 and C515 to 22 pF of X3.	X01
31	29	HW	7/29/2009	Compal	EMI solution.	Change R1215 from 22ohm to 47ohm.	X01
32	29	HW	7/29/2009	Compal	Prevent floating of PCH_GPIO34	Add R1511 10K PD.	X01
33	38	HW	7/29/2009	Compal	Based on DFX team request	Change docking connector from SP030000F0L(JAE_WD2F144WB1_144P-T) to SP030000F0L(JAE_WD2F144WB1R300_144P).	X01
34	36	HW	7/29/2009	Compal	Change PU power rail for PCIE_MCARD3_DET#	Change PCIE_MCARD3_DET# PU power rail to +3.3V_RUN	X01
35	18 35	HW	05/08/2009	Compal	Remove Braidwood circuit.	Delete R1411,R1453,JBW1	X01
36	36	HW	05/08/2009	Compal	Base on SATA EA result, need to trun off Pre-emphasis 0.	Depop R1298,pop R1301.	X01
37	33	HW	10/08/2009	Compal	Base on crystal EA result.	Change C514 C514 to 15pF and R421 to 100 ohm.	X01
38	38	HW	11/08/2009	Compal	Change VGA_ID_DISC & VGA_ID_UMA PU power rail	Change VGA_ID_DISC & VGA_ID_UMA PU power rail from +3.3V_RUN to +3.3V_ALW	X01
39	38	HW	11/08/2009	Compal	Change ODD_DET# PU power rail.	Change ODD_DET# PU power rail to +3.3V_RUN	X01
40	41	HW	11/08/2009	SMSC	Watch dog timer may not be reseted when EMC4002 VDD_PWRGD is not completely at Logic Low.	Add discharge circuit for +3.3V_M	X01
41	23	HW	11/08/2009	SMSC	SMSC review feedback	The pull-up source of the R150 should be changed to +VCC_4002	X01
42	39	HW	11/08/2009	SMSC	per SMSC 5045 AN 19.6, 4002 AN 16.11	R541, R554, R1512 should be 10K.	X01
43	23	HW	11/08/2009	Compal	FAN1_DET# should have 10K PU to +3.3V_M	Add R1517	X01
44	31	HW	11/08/2009	Broadcom	Follow Broadcom request	Delete T159, R494, R498, R631, R634, R898, C640, C641, C642 C647, C1026, L73, add R1522, C1887, C1888, change connection for R496, R497 to GND, change connection for JCS1pin3 and pin4	X01

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
45	8	HW	11/08/2009	DELL	Fix the Intel S3 power up timing	Change C1880 from 0.01uF to 0.22uF 0402 cap.	X01
46	31	HW	11/08/2009	Broadcom	Follow Broadcom request	Change C646 to 220nF that was placed near the JSC1 pin 10 (+SC_VCC).And 470nF should be at C718 near U3 (TDA8034)	X01
47	31	HW	12/08/2009	Broadcom	Follow Broadcom request	Change R497 & R496 to 0 ohm, but depop	X01
48	27	HW	12/08/2009	Compal	RGB EA result	C251-C253 to 8.2pF; L61-L63 to 10-Ohm Bead ; De-pop C390,C518,C996	X01
49	29	HW	12/08/2009	DELL	Use the SiTimes part due to the cost savings	Change X4 from TXC to SiTimes SIT8102AC3333E12T	X01
50	8	HW	12/08/2009	Intel	Intel review schematic feedback	Add R529 and C1889	X01
51	33	HW	12/08/2009	Richo	Change pop option for R5U242	Change C21 from 10U to 47U, change R46 to C1889 (1uF)	X01
52	31	HW	12/08/2009	Broadcom	BCM5882 pin-C1 "RSTOUT_N" is an open drain I/O type, we need to have 4.7K pull-up to 3.3V_ALW	Add R638	X01
53	30 36	HW	13/08/2009	Compal	Disconnect IO & DOCK VCT	Delete R652 & C41,Rename IO VCT to +LOM_VCT_IO & reserve C712 pad for test.	X01
54	31	HW	13/08/2009	Compal	Broadcom review request	USB_GPIO27 Should have a 0ohm but de-pop resistor.	X01
55	39	HW	14/08/2009	SMSC	SMSC review	Change R561 and R1046 from 1M ohm to 100K ohm.	X01
~~56~~	~~39~~	~~HW~~	~~14/08/2009~~	~~SMSC~~	~~SMSC review~~	~~Remove R587, base on crystal EA result that only need to change caps value.~~	~~X01~~
57	10	HW	14/08/2009	Intel	Follow Intel recommand to add debug TP.	Add T186~T190	X01
58	31	HW	14/08/2009	Compal	Smart card EA result	Change R772 to 47 Ohm and C1015 to 10pF for resolving SC_CLK Rise/Fail timing issue and also change C633 to 10pF.	X01
59	31	HW	14/08/2009	DELL	Avoid a glitch for DDR_HVREF_RST_GATE, please add a 1.1K 1% no-stuff pull-up to +1.5V_CPU_VDDQ rail on the PM_DRAM_PWRGD_R signal for a back-up option	Change C1889 to 0.1u, add R1518 for PM_DRAM_PWRGD_R but depop.	X01
60	8 45	HW	14/08/2009	DELL	CPU detection since the edge diode has been removed from M'09	Delete T1 and add R1519 for CPU_DETECT# and connect JCPU.AH24 to U36.B18	X01
61	15 19 36	HW	14/08/2009	DELL	Invert the EN_ESATA_RPTR signal and connect this to SATAGP4/GPIO16	Add Q211 and R1520 but depop,pop R1513 and de-pop R1514 , change net name from GPIO16 to EN_ESATA_RPTR#	X01
62	34	HW	14/08/2009	Compal	By EMI request,pop common choke	Change Pop otion for express card, pop L64, depop R791 R792.For USB2,3 pop L65,L66 and reserve R1524,R1525,R1526 and R1527.	X01
63	30	HW	14/08/2009	Intel	By Intel request	Add R1528 for LAN_REQ#	X01
64	37	HW	17/08/2009	Intel	Adding stitching caps near the DOCK_LOM traces where it crosses over plane splits.	Add C1028	X01

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
65	38	HW	8/19/2009	NV	Solve DVI issue	Add Q213-Q218,R1523,R1530~R1540	X01
66	26	HW	8/19/2009	Pericom	8200 pin 8,9 add caps to minimize noise	Add C1597 & C1598	X01
67	53	HW	8/19/2009	NV	Reserve crystal for 27M.	Add @R1541,@Y7, @C1891, @C1892	X01
68	24	HW	8/20/2009	Compal	Follow Marguax schematic	Depop R279,R1027	X01
69	53	HW	8/20/2009	Compal	Add PU/PD resistor for 8200 back-up plan	Add R1542~R1544, but depop.	X01
70	35	HW	8/24/2009	Compal	Add PD resistor for back-drive issue	Add R1545~R1547	X01
71	24	HW	8/25/2009	Compal	No need PD/PU resistors at EDP AUX channel	Delete R279 & R1027	X01
~~72~~	~~21~~	~~HW~~	~~8/25/2009~~	~~Compal~~	~~Add by pass caps~~	~~populate C39 & C610~~	~~X01~~
73	42	HW	8/25/2009	Compal	Un-populate pop option for double discharge path	Un-populate R612,R607 and R1498	X01
74	11	HW	8/25/2009	Compal	Base on power team FDIM test	Change C48,C49,C50,C51,and C52 to 22uF.	X01
75	30	HW	8/26/2009	Intel	Follow Intel WW35 `09	Change R808 to C427 10pF and change C475 to 33pF	X01
76	53	HW	8/27/2009	Compal	Follow Marguax to populate 27MHz crystal for PT build.	Populate Y7,C1891,C1892,R1541 and de-pop R631	X01
77	6,53	HW	9/28/2009	Compal	Populate 27MHz crystal.	Depop R43,R39,R1317, pop R1417	X02
78	17	HW	9/28/2009	Intel	Follow Intel DG 1.62	Change R672 to 1K_0402_5%.	X02
79	15,18	HW	9/28/2009	Compal	Depop XDP circuit component	Depop R118,R94	X02
80	53	HW	9/29/2009	NV	GPU_JTAG_TRST# should be pull down	Pop R1372 and cahnge to 1K 0hm.	X02
81	40	HW	10/20/2009	Compal	Depop R5	Depop R5 for double pull down	X02
82	33	HW	10/20/2009	Compal	Follow DFX recommendation change JSD1 footprint to modify screw hole.	Chnage FOX_2WX131A1-31DD-7F_20P-T to FOX_2WX131A1-31DD-7F_18P.	X02
83	36	HW	10/20/2009	Compal	Correct USB_MCARD2_DET# PU power rail	Chnage power rail from +3.3V_RUN to +3.3V_ALW_PCH	X02
84	17	HW	10/20/2009	Compal	Follow schematic check list 2.0, change resistor value	Chnage R268 from 1K to 10K	X02
85	16	HW	10/20/2009	Compal	Change R910 value and placement	Change R910 form 0 ohm to 22 ohm and place near PCH side.	X02
86	37	HW	10/26/2009	Compal	Chnage USB common choke by EMI request	Change L95 L96 from DLW21SN900SQ2_0805~D to HCMC0805-900MFS_4P~D	X02
~~87~~	~~23~~	~~HW~~	~~10/26/2009~~	~~Compal~~	~~Change OTP temperature~~	~~change R151 from 953ohm to 1.82Kohm~~	~~X02~~
88	53	HW	10/27/2009	Compal	To solve 27 Mhz noise issue	Connect Y7 pin 2 and 4 to GND.	X02
89	31	HW	10/27/2009	Broadcom	For 5882-B0 request	L71, L72 68nH, 2%, 400mA; C1070, C1071 1500pF, 2%, 50V; C1886, C1887 150pF, 2%, 50V	X02
90	15	HW	10/29/2009	Compal	Change flash ROM part number	Due to W25X32VSSIG will be EOL, change part number to W25Q32BVSSIG.	X02

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
91	16	HW	10/29/2009	Dell	MEM SMBus design needs to change	Move Q190 connection, add R1549,R1550, add net name DDR_XDP_CLK/DAT	X02
92	29	HW	10/29/2009	Compal	Create a low pass filter with the pole set at 36kHz to filter out of band noise	De-pop C1066 & C1067, R1090, R1089 ; R340 & R342, R1091 & R1092 change to 2k, add C1893-C1896 1000pF.	X02
93	40	HW	11/02/2009	Compal	Change BID	Change R98 form 130K ohm to 33K ohm.	X02
94	8,15	HW	11/02/2009	Compal	To avoid stub for SM bus EA quality XDP is not use.	Add R1551~R1556 but depop	X02
95	36	HW	11/02/2009	DELL	Support WiMax LED status	Need to populate R840	X02
96	43	HW	11/05/2009	Compal	To avoid golden finger was scraped on FFC.	Change sniffer connector from TYCO_1-1734820-2 to TYCO_1-2041070-2.	X02
97	41	HW	11/05/2009	Compal	Chnage TP_SMbus_PU power rail.	Change power rail from +5V_ALW to +3.3V_ALW	X02
~~98~~	~~31~~	~~HW~~	~~11/05/2009~~	~~BRCM~~	~~Delete 2nd ROM for BRCM5882~~	~~By BRCM review result ,delete U14.~~	~~X02~~
99	24	HW	11/10/2009	Compal	LCD power sequencing issue	change R161 from 470 to 100 ohm .	X02
100	19	HW	11/11/2009	DELL	PCH driving the siganl low at GPIO15 initial.	Add R1557 2.2K PU resistor to +3.3V_ALW_PCH on the SIO_EXT_WAKE# signal.	X02
101	15	HW	11/11/2009	DELL	To change the pin on the EC side to OD and add a pull-up to PCH's core well	Add R1558 10K PU resistor to +3.3V_RUN on the ME_FWP signal.	X02
102	15,40	HW	11/11/2009	Compal	RTC timing issue	Y1 & Y4 change from 1TJS125DJ4A420P to Q13MC30610018.Opreating temperature should -40~+85 degree to meet test requirement.	X02
103	19	HW	11/17/2009	Compal	Chnage GPIO34 of PCH from PD to PU	Change from PD to PU +3.3V_RUN	X02
~~104~~	~~31~~	~~HW~~	~~11/17/2009~~	~~Compal~~	~~Follow Marguax schmatic and it also could pass smart card EA.~~	~~To change R772 from 47 ohm to 22 ohm~~	~~X02~~
105	31	HW	11/17/2009	Compal	To solve touch pad ESD issue	Change L41 and L42 to 100 ohm (R1564 & R1565)	X02
106	15	HW	11/19/2009	Compal	Follow Intel check list rev2.0	Change R2244 to tolerance from 5% to 1%	X02
~~107~~	~~15~~	~~HW~~	~~11/19/2009~~	~~Compal~~	~~Follow DCU 414044 Rev2.0~~	~~Depop R123 ,R804-807 and R1281,R1282 R1315.~~	~~X02~~
108	38	HW	12/22/2009	Compal	Simplo battery slice EMI issue	Add C1897 and C1898(Depop,reserve for EMI test)	A00
109	37	HW	12/22/2009	Compal	DFB issue ,finger printer connector will easy shift during reflow process.	Change finger printer connector from TYCO_1734242-6_6P-T to TYCO_2041070-6_6P-T	A00
110	31	HW	12/22/2009	Compal	By Broadcom recommend	Change L71,L72 from 68nH to 150nH, C1070,C1071 from 1500pF to 390pF.C1887,C1888 from 150pF to 390pF.	A00
111	32	HW	12/22/2009	Compal	Change TCM to T1 version	Change TCM from SSX44B-D-T to SSX44-D-T1	A00
112	40	HW	12/22/2009	Compal	Change BID	Change R98 form 33K ohm to 1K ohm.	A00
113	08	HW	12/22/2009	Compal	Depop CPU XDP and JTAG circuit for for production systems	Depop C19,C20,R6,R68,R19,R7,R3, R780~R785,R22,R24,R1153,R1156,R66,R1241,R1257	A00
~~114~~	~~15~~	~~HW~~	~~12/22/2009~~	~~Compal~~	~~Depop PCH JTAG circuit for for production systems~~	~~Depop R123, R804-R807,R1281,R1282,R1315~~	~~A00~~

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115	33,34	HW	01/07/2010	Compal	Change R5U2542 form ES2 to ES3	Change part number from SA00003C21L to SA00003C22L	A00
116	27	HW	01/14/2010	Compal	RGB EMI issue	Change L61,L62,L63 from 10nH to 27nH, C251,C252,C253 from 8.2pF to 2pF and pop C390,C518,C996	A00
117	37	HW	01/15/2010	Compal	Change SATA repeater part to power saving part	Change U95 to SA00003P10L	A00
118	26	HW	01/19/2010	Pericom	Pericom DP SW DP8200 has new silicon W version in stead of Y version	Change U9 to SA00003CD2L	A00

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1	50	Selector	7/20	TI	CSS GC logic wrong issue	Add PR282 180_ohm to GND	X01
2	46	1.5V_MEM	7/20	Compal ADC Guangyong	Add droop resistor for TI solution	Add PR77	X01
3	45	+3.3V/+5V	8/17	Compal ADC Guangyong	Change 3V/5V choke for cost down	change PL5 from SH00000H90L to SH00000FN0L change PL6 from SH00000HB0L to SH00000HR0L	X01
4	50	Selector	8/17	Compal	Add 1M_ohm pull down to fix ACAV_IN_NB oscillation when battery mode S5	Add PR283	X01
5	50	Selector	8/17	TI	new version CD3301 (PG2.1) don't need PD22 and PR282	depop PD22 add PR282, pop PR430	X01
6	50	Selector	8/17	TI	DOCK_AC_OFF_EC floating issue	add PR285	X01
7	52	ISL62872_GPU	8/17	Dell / intersil	change PU901 to ISL62872 to support NV VID fixture	change PU901 to ISL62872 from ISL62870 and support circuit.	X01
8	49	+VCORE MAX17030	8/17	Compal	change thermistor package from 0603 to 0402 for cost down	Change PH3,PH4 and PH5 from SL200000B0L to SL200000W0L	X01
~~9~~	~~47~~	~~1.8V_RUN~~	~~8/18~~	~~MAXIM~~	~~Output ripple voltage unstable issue~~	~~Change PC314 from SE00000868L(22u/0805) to SE00000O00L(100u/1206)~~ ~~Change PR409 from SD03480618L (8.06k) to SD03460418L (6.04k)~~ ~~Change PR410 from SD03440218L(4.02k) to SD03430118L(3.01k)~~ ~~Change PR408 from SD014402A8L(40.2 Ohm) to SD000008H8L(51 Ohm)~~ ~~Change PC315 from SE000003W8L(820pF) to SE076333K8L (3300pF)~~ ~~Change PR411from SD00000268L(6.98K) to SD03445318L(4.53K)~~ ~~Change PC310 from SE074102K8L(1000P) to SE074472K8L(4700pF)~~ ~~Change PC309 from SE071330J8L (33pF) to SE071560J8L (56pF)~~ ~~Change PC311 from SE042104K8L(.1u/0603/25V) to SE076104K8L(.1u/0402/16V)~~ ~~Add PR413 SD02800008L (0 Ohm)~~	~~X01~~
10	49	+VCORE MAX17030	8/20	Maxim	Vcore FDIM issue	Change PR102, PR103 and PR104 from SD013220B8L(2.2) to SD00000V98L(1.1) Change PR310, PR311 and PR312 from SD03430118L(3.01k) to SD03424918L(2.49k) Change PR307, PR308 and PR309 from SD03422118L(2.21k) to SD03417418L(1.74k) Change PR137 from SD03449910L(4.99k) to SD03447518L(4.75k) Add PC271,PC272 and PC273 SE075223K8L(0.022uF)	X01
11	48	+1.05VM/ +1.05VTT	8/20	ON	Fine tune DC accurcay	Change PR188 and PR201 from SD03451018L(5.1k) to SD00000U28L (4.3k) Change PR199 and PR203 from SD03416228L(16.2k) to SD03413728L(13.7k) Change PR198 from SD03468008L(680 Ohm) to SD03418008L(180 Ohm) Change PR202 from SD03468008L(680 Ohm) to SD03410008L(100 Ohm) Change PC108 and PC116 from SE074331K8L(330p) to SE074471K8L(470p) Change PR200 from SD00000DM0L(200k) to SD03451028L(51k) Change PC115 from SE071300J0L(SE071300J0L) to SE071220J8L(22P) Change PC106 from SE071300J0L(30P) to SE071330J8L(33P) Change PR204 from SD03447518L(4.75K) to SD03452318L(5.23K) Change PR205 from SD03444228L(44.2K) to SD03424028L(24K) Change PR207 from SD00000LZ0L(3.83K) to SD00000J20L(4.32K) Change PR208 from SD03482518L(8.25k) to SD03464918L(6.49k)	X01
12	47	1.8V_RUN	8/25	DELL	1.8V transient 0.1A ~ 1.6A output voltage over spec	Change PU301 from SA00003B10L(MAX15050) to SA00003CG0L (ISL8014) and support circuit	X01

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13	49	Vcore	8/25	MAXIM	Improve DC accuracy	Change exposed pad to PGND from AGND	X01
14	49	Vcore	8/25	MAXIM	Vender recommend PSI# pull down 10k	Change PR334 from SD03410018L (1k) to SD02810028L(10k)	X01
15	51	Charger	8/25	Compal ADC Guangyong	Improve charger choke saturation current at 100 degree C	Change PL14 from SH04856AM8L (5.6u) to SH00000I60L (5.6u)	X01
16	44	DCIN	8/25	Compal	3.3V_ALW2 black driver issue with RTC battery only	Change PD1 from SC100000Q0L(BAT54CW) to SCSB715F08L (RB715F)	X01
17	49	Vcore	8/27	Compal	Reseve resistor pad for debug	Add PR122 and PR123	X01
18	52	GPU_Core	9/01	Intersil	PR916 and PR911 for debug change to O Ohm	Change PR916 from SD02810018L(1K) to SD02800008L(0 Ohm) Change PR911 from SD02810018L(1K) to SD02800008L(0 Ohm)	X01
19	49	Vcore	9/01	MAXIM	Fine tune Imon time constant meet Intel SPEC 300uS~500uS	Change PC270 from SE075223K8L (0.022U) to SE076333K8L (.033U)	X01
20	49	Vcore	9/01	MAXIM	Make sure DPRSLPVE low level under 0.33V	Change PR109 from SD03449908L (499 Ohm) to SD02800008L (0 Ohm)	X01
21	52	GPU_Core	10/06	NV	GPU_CORE defult setting should be 1V for faster to boot to system and short warm up time for GPU	Depop PR910 and POP PR927	X02
22	44	DC_IN	10/13	TI	High inrush current on DC_IN when AC adapter plug in	Change PR20 from SD02800008L(0 Ohm) to SD02810028L(10k)	X02
23	49	Vcore	10/20	MAXIM	3 phase overlap issue with 2nd source MOSFET	Add PC198, PC199, PC255, PC256, PC259 and PC260 SE074122K8L (1200pF)	X02
24	48	+1.05VTT	10/28	INTEL	Fine tune H_VTTPWRGD voltage level meet Vih(min) = 0.75 * Vtt	Change PR94 from SD03410028L (10k) to SD03427418L (2.74K) Change PR93 from SD03428728L (28.7k) to SD03493118L (9.31K)	X02
25	49	+VCORE	11/03	Compal	change thermistor package from 0603 to 0402 for cost down	Change PH1 from SL20000068L (100K 0603) to SL20000160L (100K 0402)	X02
26	52	GPU_Core	11/12	Compal	For NVIDIA output voltage +/- 30mV criteria	Change PC918 from SGA19331D1L (330u/9m Ohm) to SGA0000420L (470u/4.5m Ohm)	X02
27	48	+1.05VTT/ +1.05VM	11/16	ON	Bost diode over stress	Change PD19 and PD27 from SC1B751V08L(RB751V) to SCS00003M0L(BAT54HT1)	X02
28	51	Charger	01/12	Compal	Reduce Pin33,34 and 35 of the CD3301 surge current	Change PC351 from SE00000130L (1u/0805) to SE043104M8L (0.1u/0805) Change PR404 from SD02800008L (0 Ohm) to SD028100B8L (1 Ohm)	A00

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