

COMPAL CONFIDENTIAL

MODEL NAME : **NCL01**

PCB NO : **LA-5472P (DAA00001I00)**

E2 Rothschild DSC

**rPGA Arrandale +
FCBGA PCH IBEXPEAK-M
+ N10M-NS-S**

2010-01-20

REV : 1.0(A00)

@ : Nopop Component

MB Type	BOM P/N	PCMCIA	Express	TCM		TPM		ATG		BOM CONFIG
		1@	2@	W(3@)	W/O(4@)	W(5@)	W/O(6@)	7@	8@	
EXPRESS CARD ,Enble TPM ,Disable TCM	43177831L01		*		*	*				2@,4@,5@
EXPRESS CARD ,Disable TPM ,Enble TCM	43177831L02		*	*			*			2@,3@,6@
EXPRESS CARD ,Disable TPM ,Disable TCM	43177831L03		*		*	*				2@,4@,6@
PCMCIA CARD ,Enble TPM ,Disable TCM	43177831L04	*			*	*				1@,4@,5@
PCMCIA CARD ,Disable TPM ,Enble TCM	43177831L05	*		*			*			1@,3@,6@
PCMCIA CARD ,Disable TPM ,Disable TCM	43177831L06	*			*		*			1@,4@,6@

MB PCB	
Part Number	Description
DAA0A200100	PCB NCL01 LA-5472P LS-5471P/5473P/5574P

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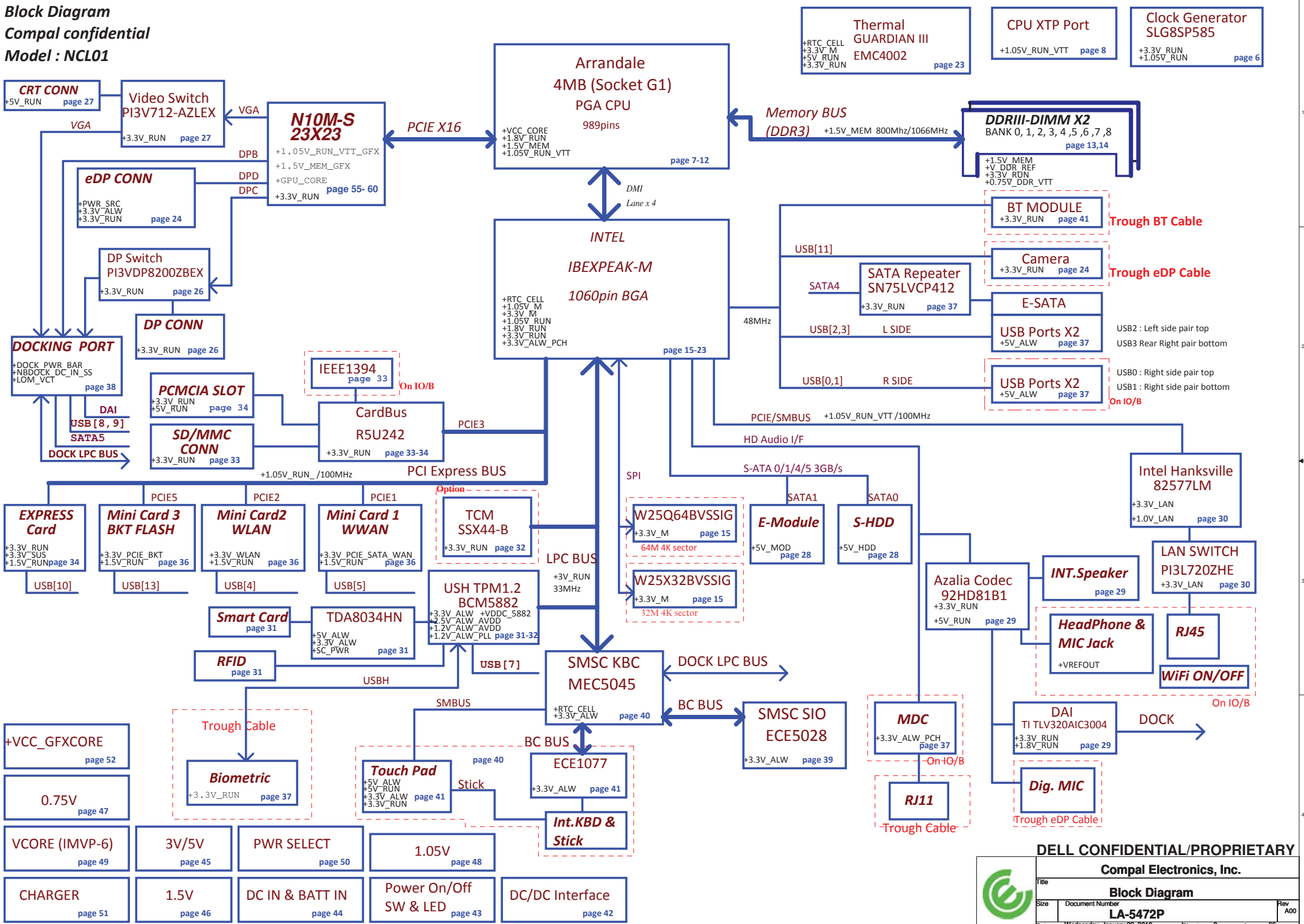


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Block Diagram
Compal confidential
Model : NCL01



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Block Diagram			
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POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M1	LOW	LOW	HIGH	LOW	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M1	LOW	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State \ power plane	+15V_ALW +5V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_CORE +1.05V_RUN_VTT +1.05V_RUN	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

PCH	USB PORT#	DESTINATION
	0	JUSB1 (Ext Right Side Top)
	1	JUSB1 (Ext Right Side Bottom)
	2	JESA1 (Ext Left Side Top)
	3	JESA1 (Ext Left Side Bottom)
	4	WLAN
	5	WWAN
	6	Bluetooth
	7	USH->BIO
	8	DOCKING
	9	DOCKING
	10	Express card
	11	Camera
	12	none
13	JMINI3(PCIE/BKT CARD)	

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	PCMCIA
Lane 4	EXPRESS CARD
Lane 5	MINI CARD-3 PCIE/BKT
Lane 6	10/100/1G LAN
Lane 7	None
Lane 8	None

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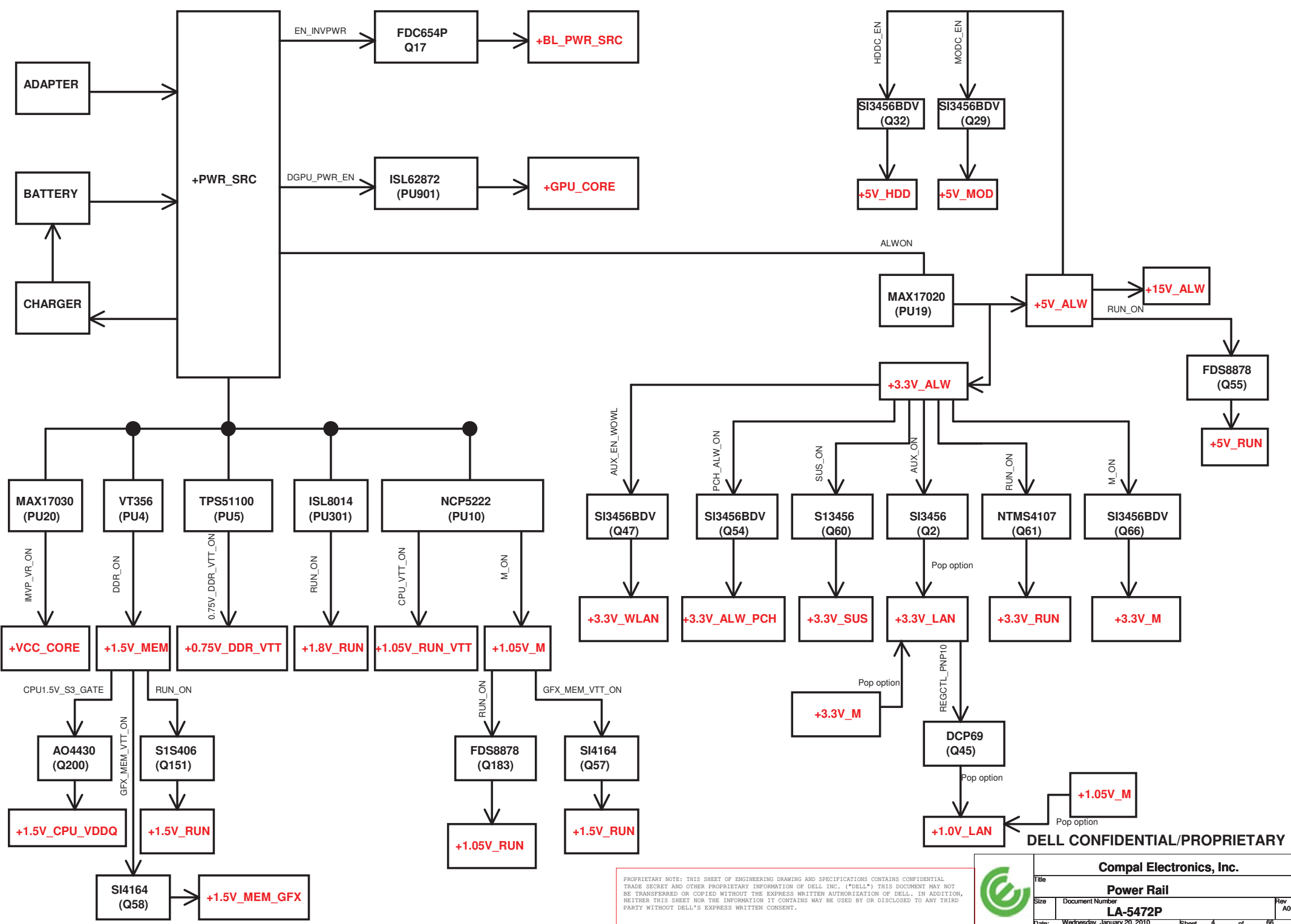
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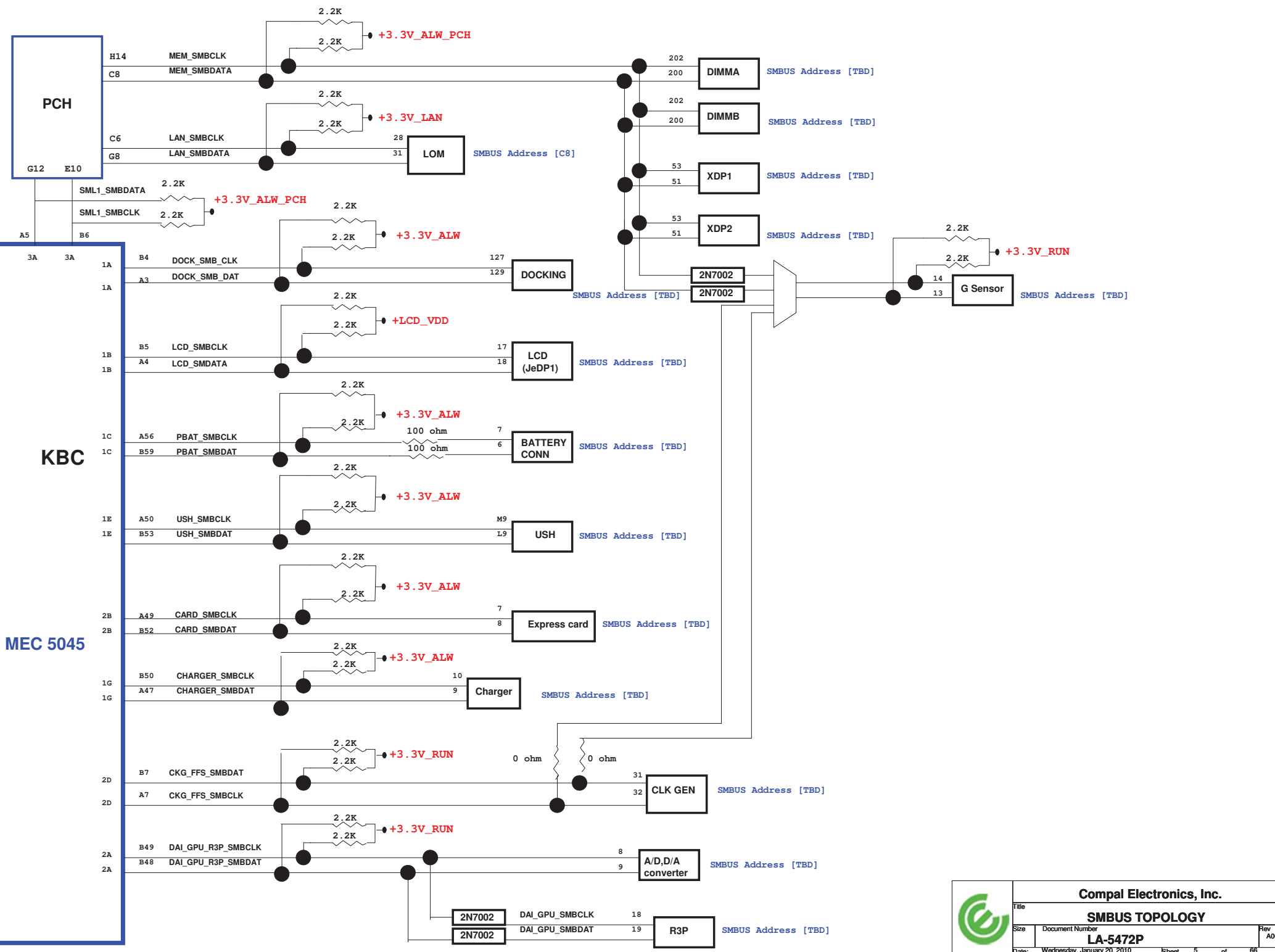


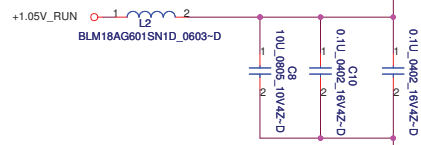
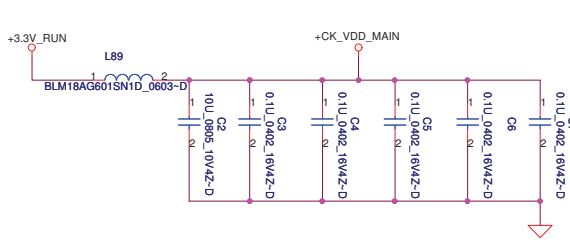
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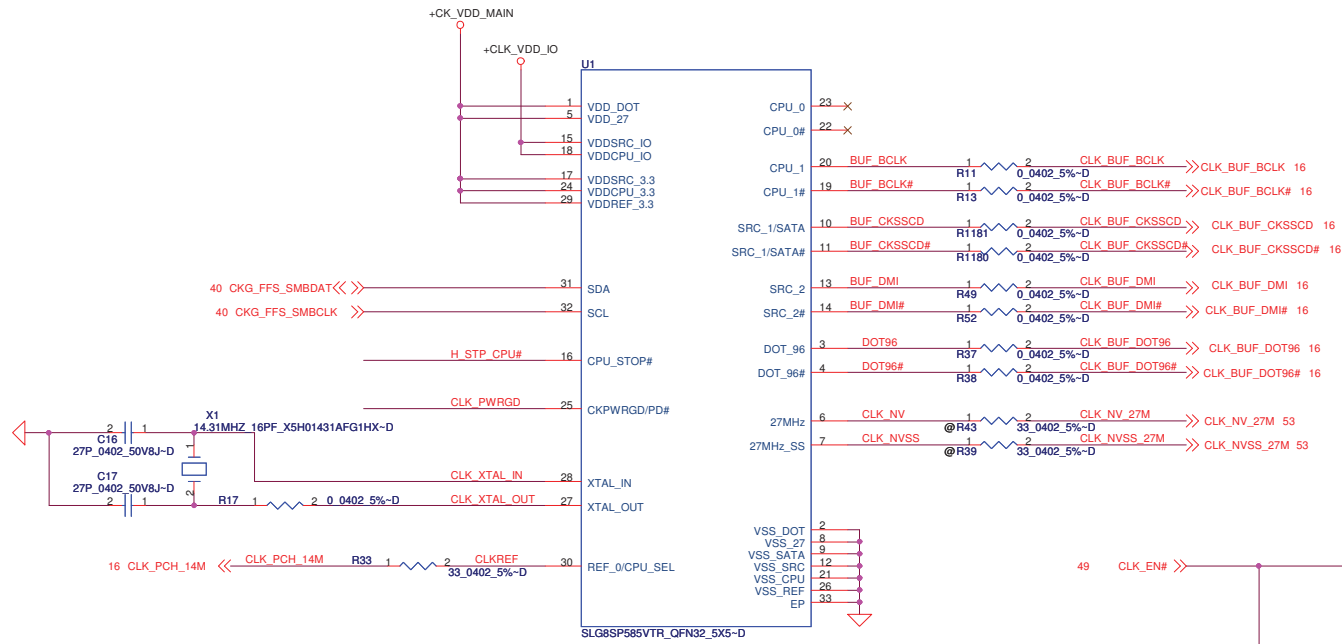
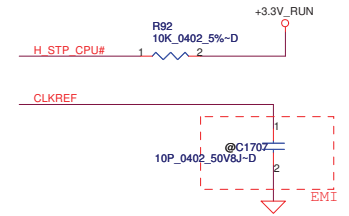
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Power Rail			
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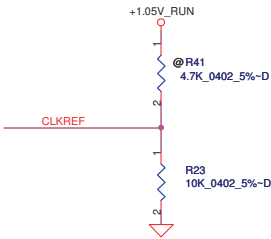
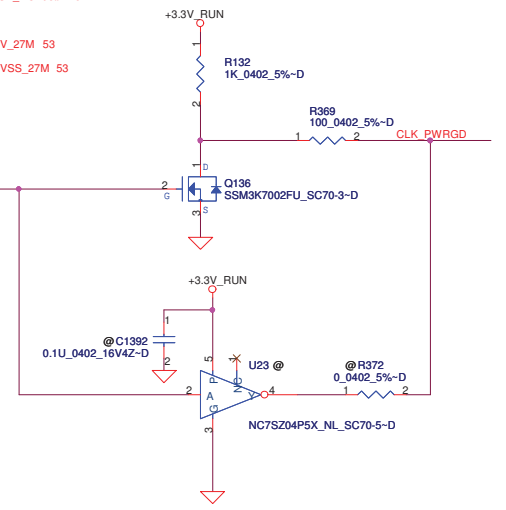


+CLK_VDD_IO CAN BE RANGE FROM 1.05V TO 3V



REF_0/CPU_SEL

PIN 30	CPU0	CPU1
1 (0.7~1.5v)	100MHz	100MHz
0 (DEFAULT)	133MHz	133MHz



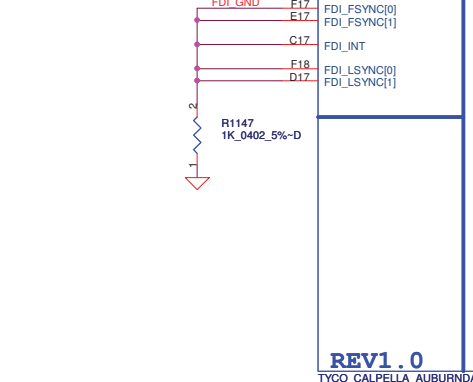
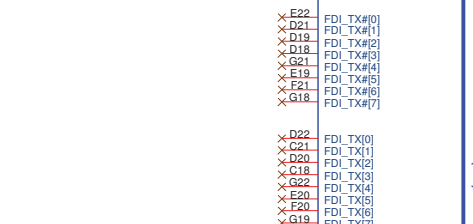
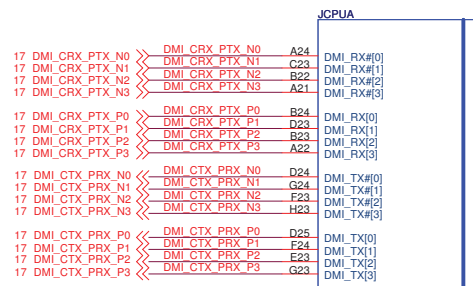
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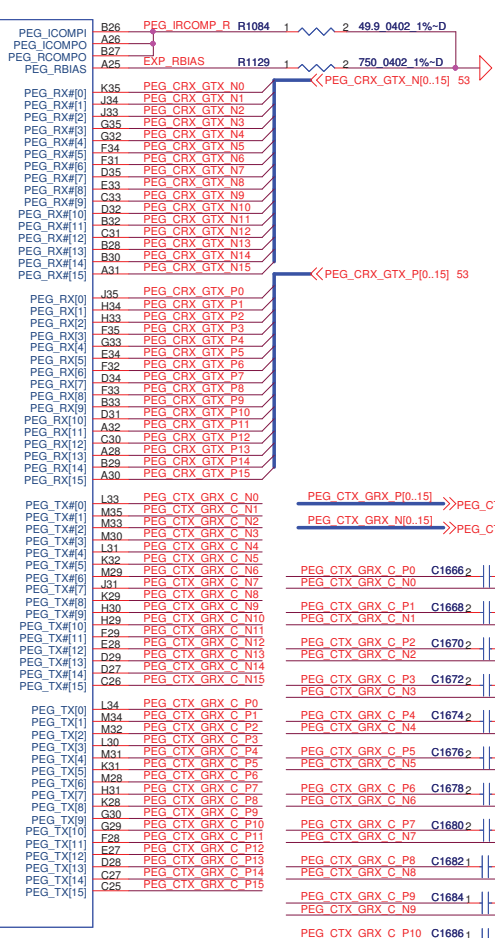
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Clock Generator			
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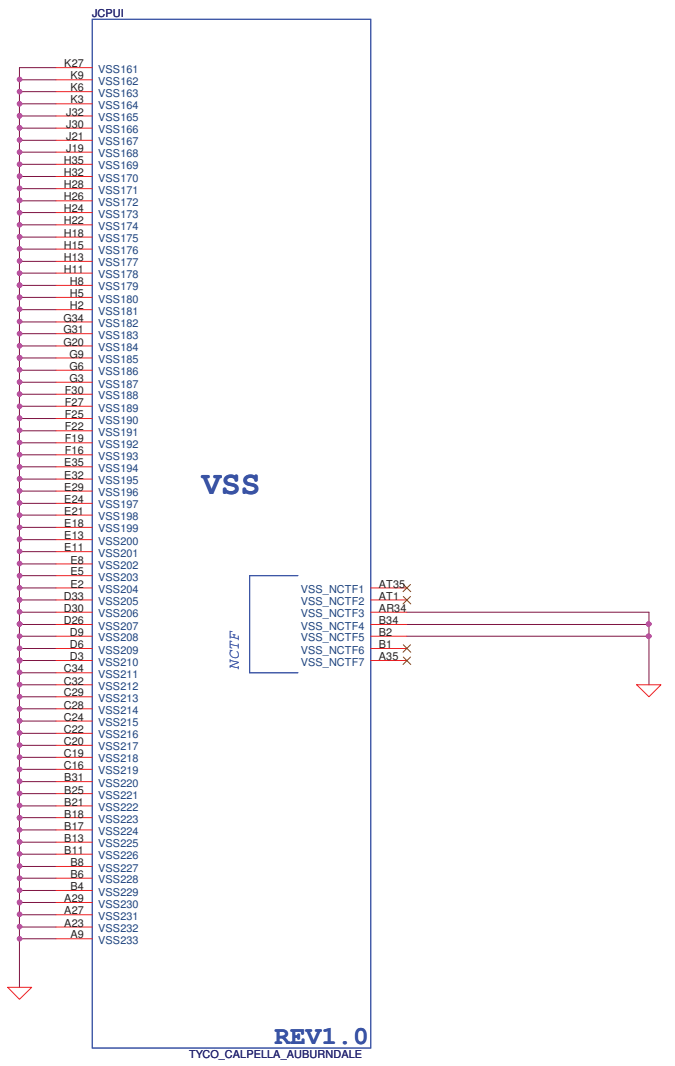


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PCI EXPRESS 4 GRAPHICS



PEG_TX#0	L33	PEG CTX GRX C N0	PEG CTX GRX C N0	C1666_2	1	0.1U_0402	10V7K-D	PEG CTX GRX P0
PEG_TX#1	M35	PEG CTX GRX C N1	PEG CTX GRX C N1	C1672_2	1	0.1U_0402	10V7K-D	PEG CTX GRX N0
PEG_TX#2	M30	PEG CTX GRX C N2	PEG CTX GRX C N2	C1668_2	1	0.1U_0402	10V7K-D	PEG CTX GRX P1
PEG_TX#3	M30	PEG CTX GRX C N3	PEG CTX GRX C N3	C1669_2	1	0.1U_0402	10V7K-D	PEG CTX GRX N1
PEG_TX#4	L31	PEG CTX GRX C N4	PEG CTX GRX C N4	C1670_2	1	0.1U_0402	10V7K-D	PEG CTX GRX P2
PEG_TX#5	K32	PEG CTX GRX C N5	PEG CTX GRX C N5	C1671_2	1	0.1U_0402	10V7K-D	PEG CTX GRX N2
PEG_TX#6	M29	PEG CTX GRX C N6	PEG CTX GRX C N6	C1672_2	1	0.1U_0402	10V7K-D	PEG CTX GRX P3
PEG_TX#7	J31	PEG CTX GRX C N7	PEG CTX GRX C N7	C1673_2	1	0.1U_0402	10V7K-D	PEG CTX GRX N3
PEG_TX#8	K29	PEG CTX GRX C N8	PEG CTX GRX C N8	C1674_2	1	0.1U_0402	10V7K-D	PEG CTX GRX P4
PEG_TX#9	H30	PEG CTX GRX C N9	PEG CTX GRX C N9	C1675_2	1	0.1U_0402	10V7K-D	PEG CTX GRX N4
PEG_TX#10	H29	PEG CTX GRX C N10	PEG CTX GRX C N10	C1676_2	1	0.1U_0402	10V7K-D	PEG CTX GRX P5
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PEG_TX#13	D27	PEG CTX GRX C N13	PEG CTX GRX C N13	C1679_2	1	0.1U_0402	10V7K-D	PEG CTX GRX N6
PEG_TX#14	C26	PEG CTX GRX C N14	PEG CTX GRX C N14	C1680_2	1	0.1U_0402	10V7K-D	PEG CTX GRX P7
PEG_TX#15	C26	PEG CTX GRX C N15	PEG CTX GRX C N15	C1681_2	1	0.1U_0402	10V7K-D	PEG CTX GRX N7
PEG_TX#0	L34	PEG CTX GRX C P0	PEG CTX GRX C P0	C1682_1	2	0.1U_0402	10V7K-D	PEG CTX GRX P8
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PEG_TX#2	M32	PEG CTX GRX C P2	PEG CTX GRX C P2	C1684_1	2	0.1U_0402	10V7K-D	PEG CTX GRX P9
PEG_TX#3	L30	PEG CTX GRX C P3	PEG CTX GRX C P3	C1685_1	2	0.1U_0402	10V7K-D	PEG CTX GRX N9
PEG_TX#4	M31	PEG CTX GRX C P4	PEG CTX GRX C P4	C1686_1	2	0.1U_0402	10V7K-D	PEG CTX GRX P10
PEG_TX#5	K31	PEG CTX GRX C P5	PEG CTX GRX C P5	C1687_1	2	0.1U_0402	10V7K-D	PEG CTX GRX N10
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PEG_TX#10	G29	PEG CTX GRX C P10	PEG CTX GRX C P10	C1692_1	2	0.1U_0402	10V7K-D	PEG CTX GRX P13
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PEG_TX#12	E27	PEG CTX GRX C P12	PEG CTX GRX C P12	C1694_1	2	0.1U_0402	10V7K-D	PEG CTX GRX P14
PEG_TX#13	D28	PEG CTX GRX C P13	PEG CTX GRX C P13	C1695_1	2	0.1U_0402	10V7K-D	PEG CTX GRX N14
PEG_TX#14	C27	PEG CTX GRX C P14	PEG CTX GRX C P14	C1696_1	2	0.1U_0402	10V7K-D	PEG CTX GRX P15
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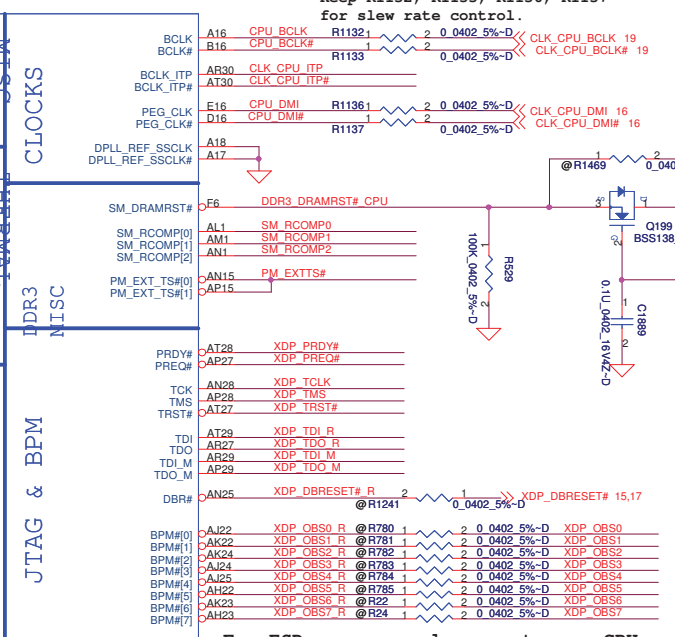
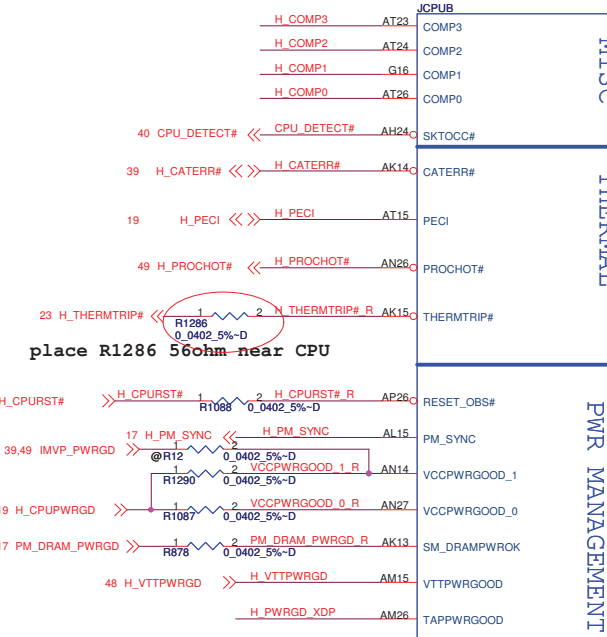
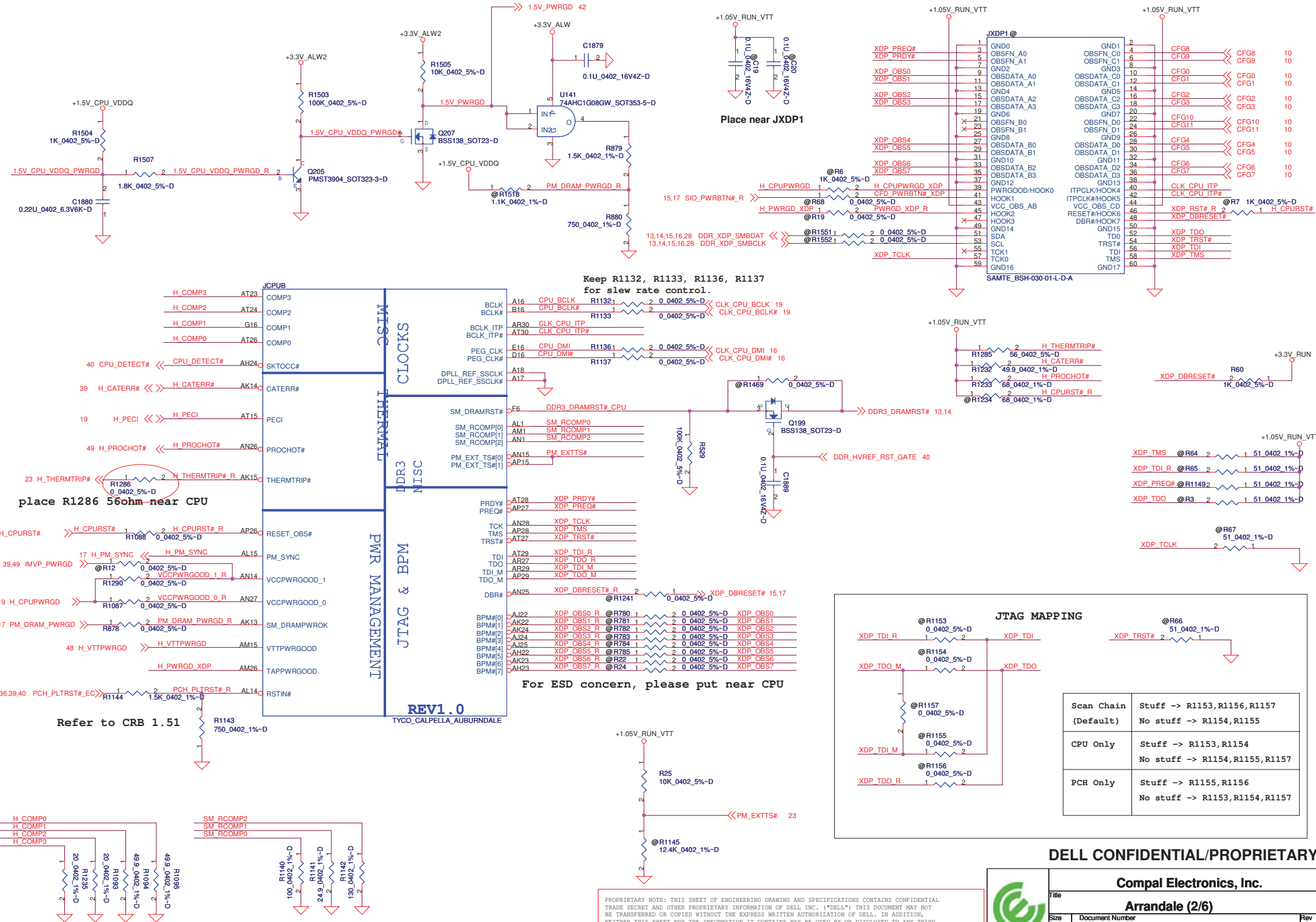


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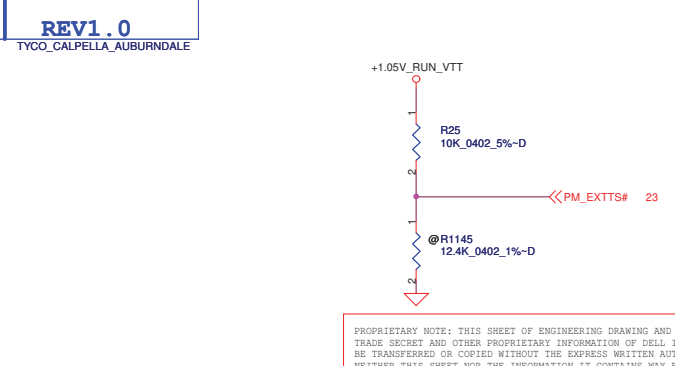
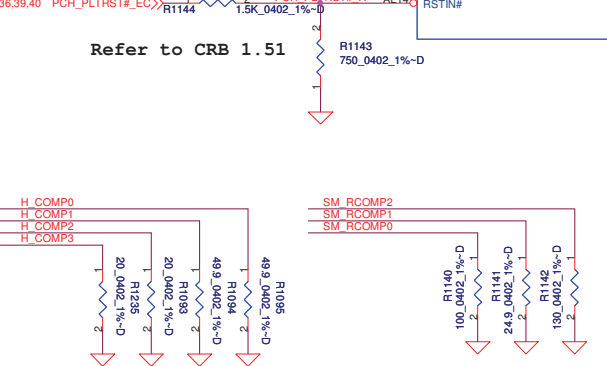
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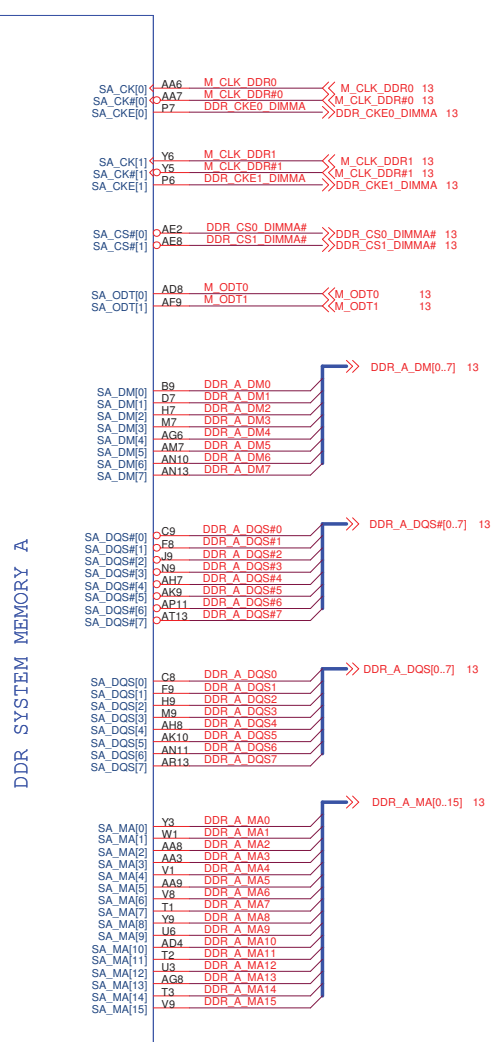
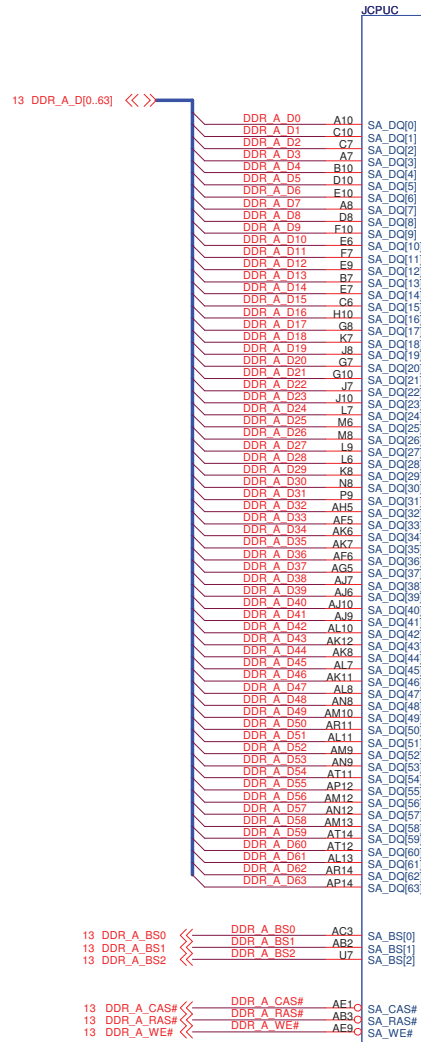
JTAG MAPPING

XDP TDI R	@R1153 0.0402_5%-D	XDP TDI	@R66 51.0402_1%-D
XDP TDI M	@R1155 0.0402_5%-D	XDP TDO	
XDP TDO M	@R1154 0.0402_5%-D	XDP TDO	
XDP TDO R	@R1156 0.0402_5%-D	XDP TDO	

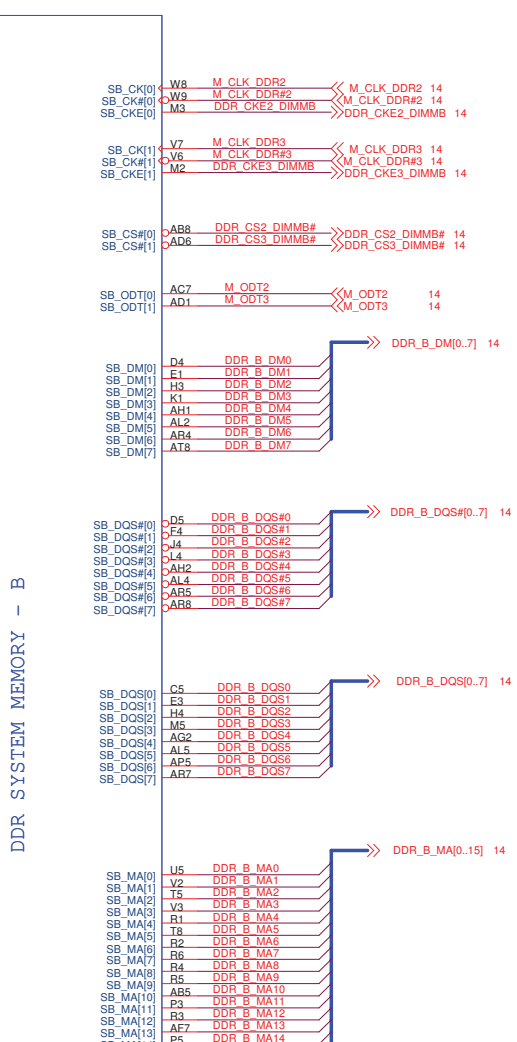
Scan Chain (Default)	Stuff -> R1153,R1156,R1157 No stuff -> R1154,R1155
CPU Only	Stuff -> R1153,R1154 No stuff -> R1154,R1155,R1157
PCH Only	Stuff -> R1155,R1156 No stuff -> R1153,R1154,R1157



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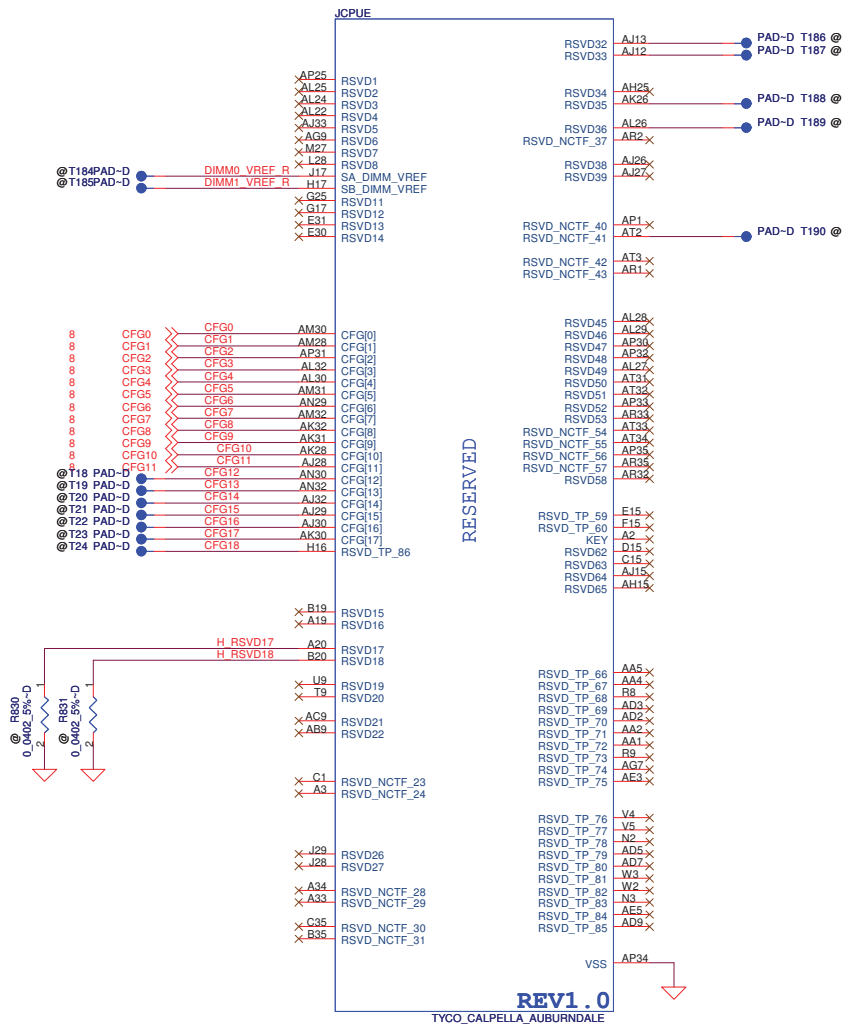
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PCI-Express Configuration Select

CFG0	1 : Single PEG 0 : Bifurcation enable
------	------------------------------------------

PCI-Express Static Lane Reversal

CFG3	1 : Normal Operation 0 : Lane Number Reversed 15->0, 14->1 ...
------	----------------------------------------------------------------------

Display Port Presence

CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port
------	--------------------------------------------------------------------------------------------------------------------------------------------------------------------

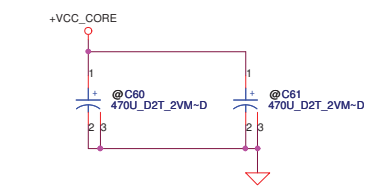
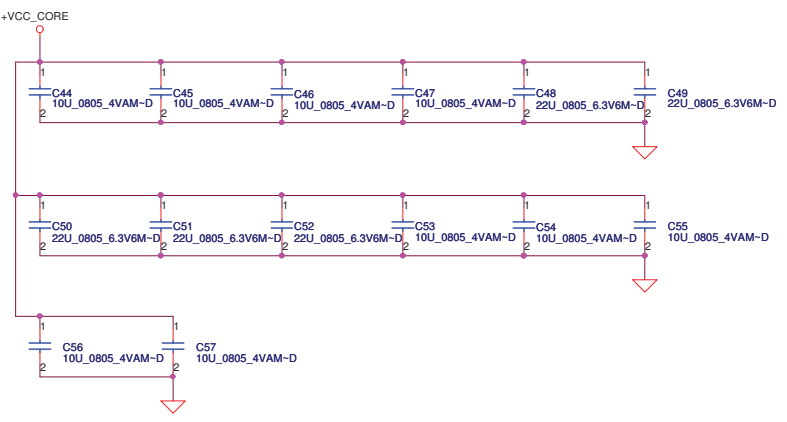
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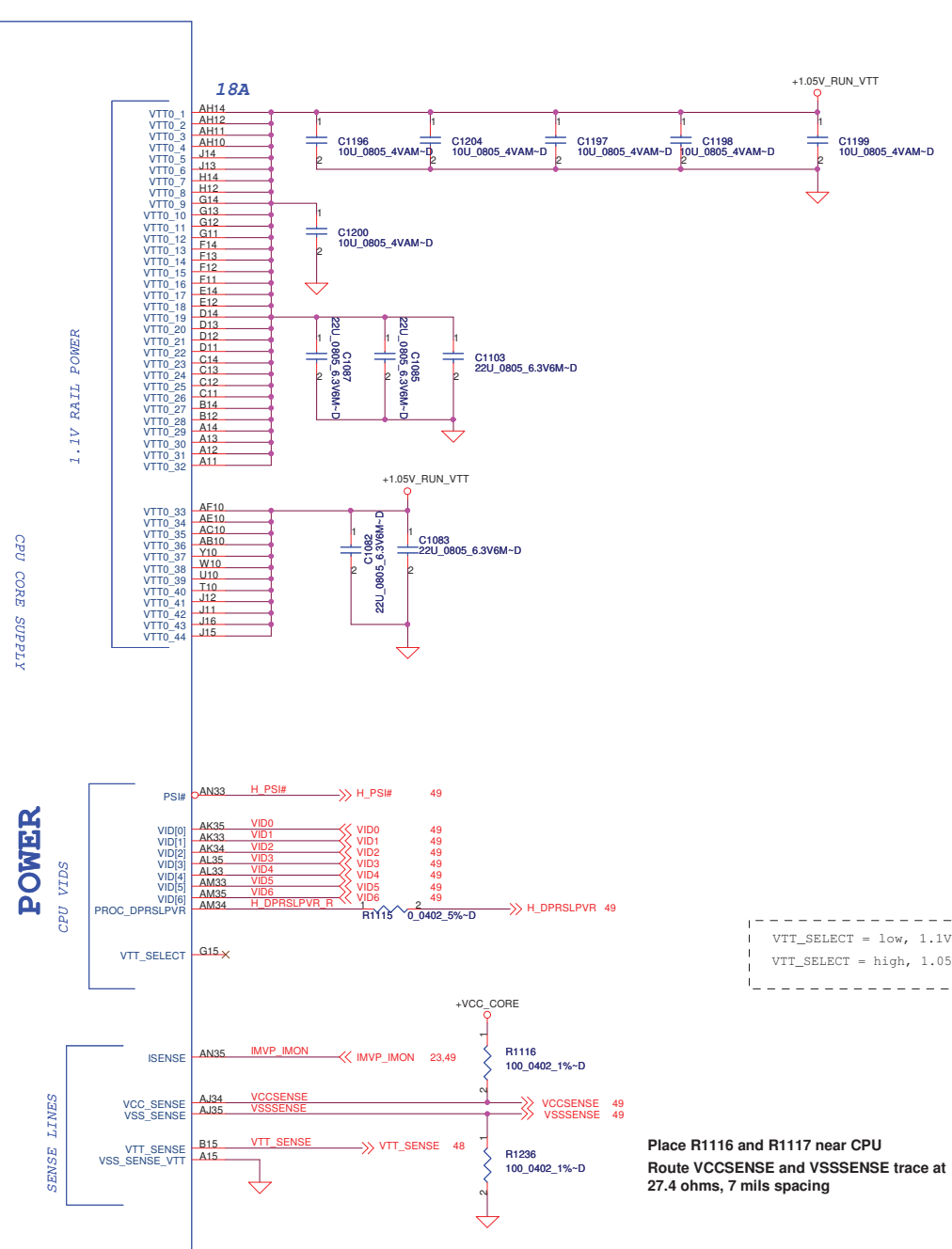
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JCPUF

+VCC_CORE	48A
AG35	VCC1
AG34	VCC2
AG33	VCC3
AG32	VCC4
AG31	VCC5
AG30	VCC6
AG29	VCC7
AG28	VCC8
AG27	VCC9
AG26	VCC10
AF35	VCC11
AF34	VCC12
AF33	VCC13
AF32	VCC14
AF31	VCC15
AF30	VCC16
AF29	VCC17
AF28	VCC18
AF27	VCC19
AF26	VCC20
AD35	VCC21
AD34	VCC22
AD33	VCC23
AD32	VCC24
AD31	VCC25
AD30	VCC26
AD29	VCC27
AD28	VCC28
AD27	VCC29
AD26	VCC30
AC35	VCC31
AC34	VCC32
AC33	VCC33
AC32	VCC34
AC31	VCC35
AC30	VCC36
AC29	VCC37
AC28	VCC38
AC27	VCC39
AC26	VCC40
AA35	VCC41
AA34	VCC42
AA33	VCC43
AA32	VCC44
AA31	VCC45
AA30	VCC46
AA29	VCC47
AA28	VCC48
AA27	VCC49
AA26	VCC50
Y35	VCC51
Y34	VCC52
Y33	VCC53
Y32	VCC54
Y31	VCC55
Y30	VCC56
Y29	VCC57
Y28	VCC58
Y27	VCC59
Y26	VCC60
Y25	VCC61
Y24	VCC62
Y23	VCC63
Y22	VCC64
Y21	VCC65
Y20	VCC66
Y19	VCC67
Y18	VCC68
Y17	VCC69
Y16	VCC70
U35	VCC71
U34	VCC72
U33	VCC73
U32	VCC74
U31	VCC75
U30	VCC76
U29	VCC77
U28	VCC78
U27	VCC79
U26	VCC80
R35	VCC81
R34	VCC82
R33	VCC83
R32	VCC84
R31	VCC85
R30	VCC86
R29	VCC87
R28	VCC88
R27	VCC89
R26	VCC90
P34	VCC91
P33	VCC92
P32	VCC93
P31	VCC94
P30	VCC95
P29	VCC96
P28	VCC97
P27	VCC98
P26	VCC99
P25	VCC100



REV1.0
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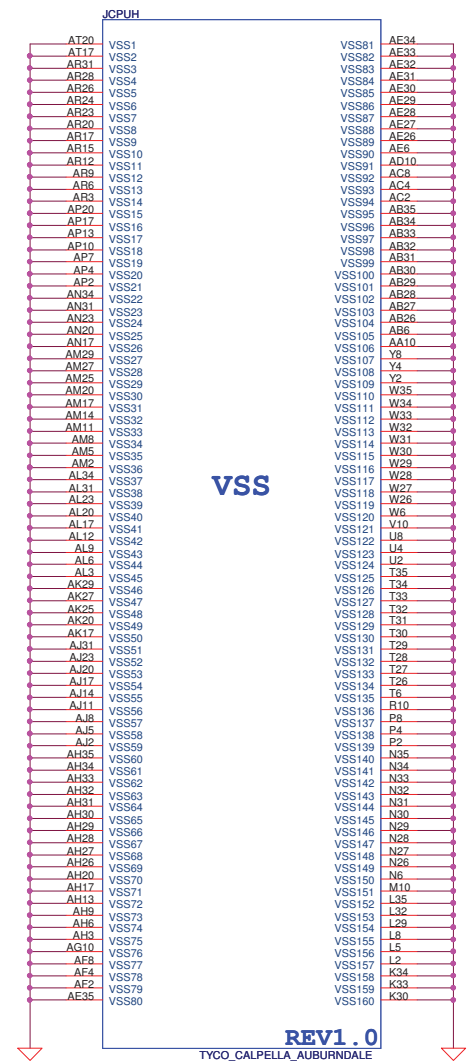
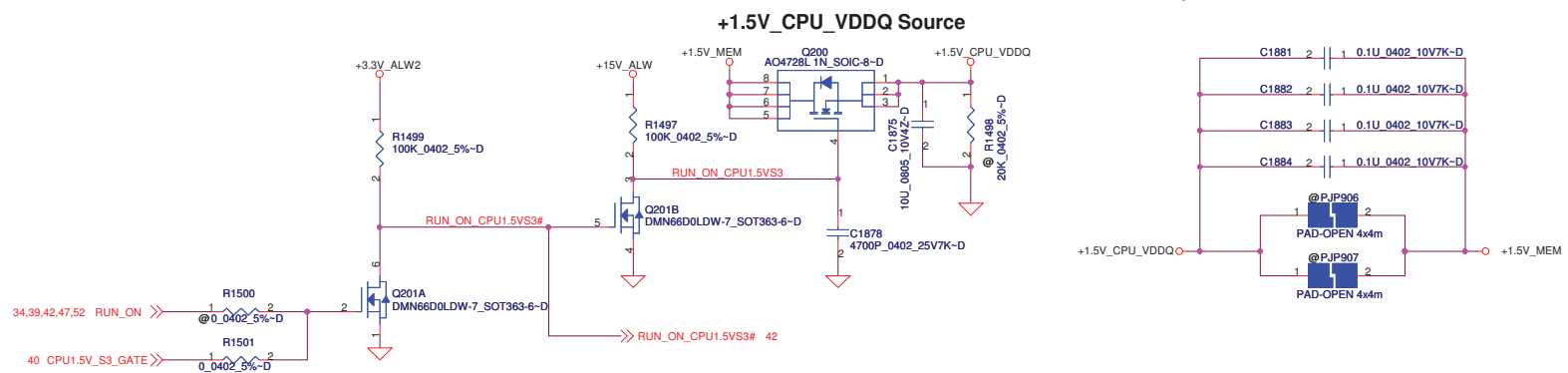
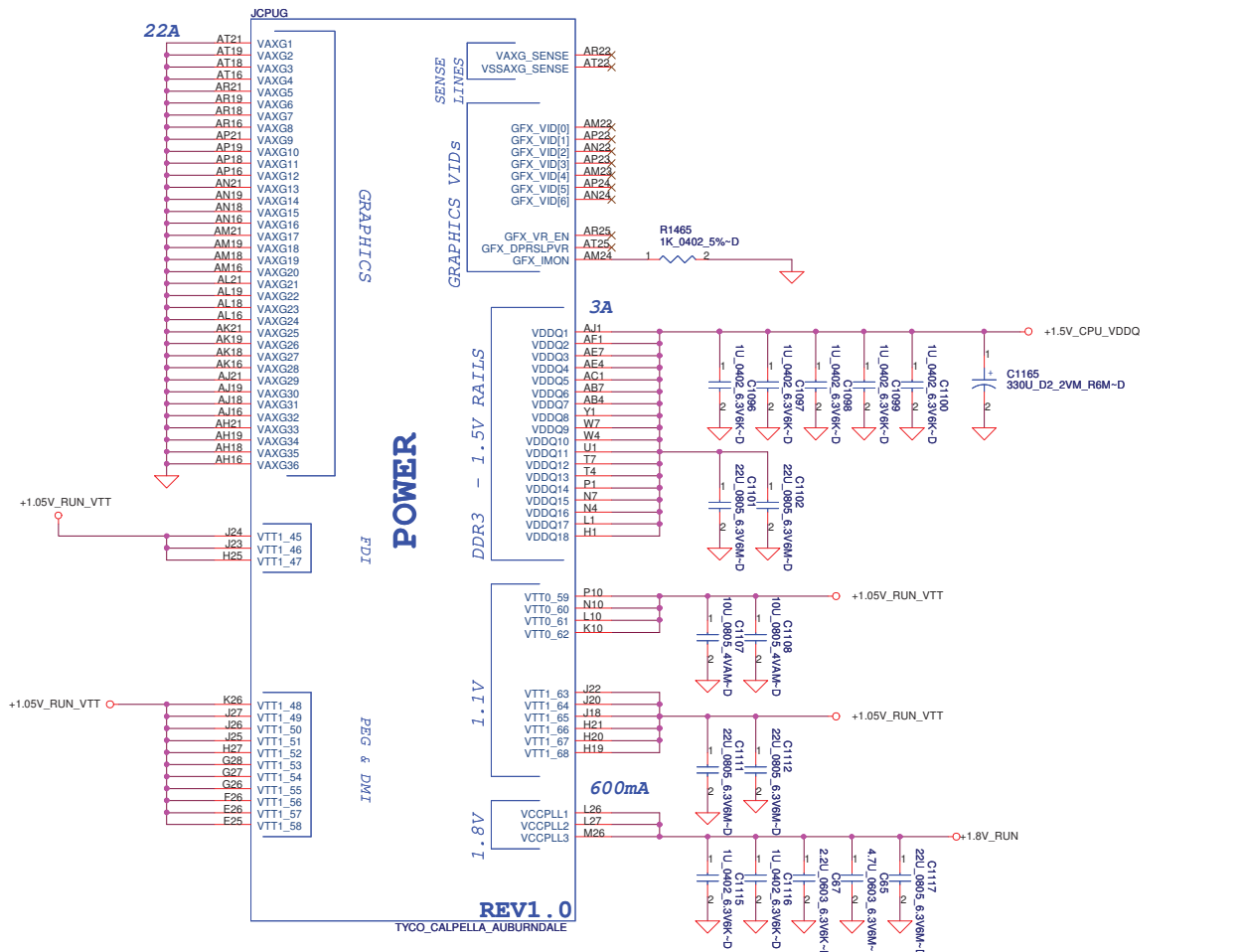
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VTT_SELECT = low, 1.1V
VTT_SELECT = high, 1.05V

Place R1116 and R1117 near CPU
Route VCCSENSE and VSSSENSE trace at 27.4 ohms, 7 mils spacing

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Arrandale (5/6)			
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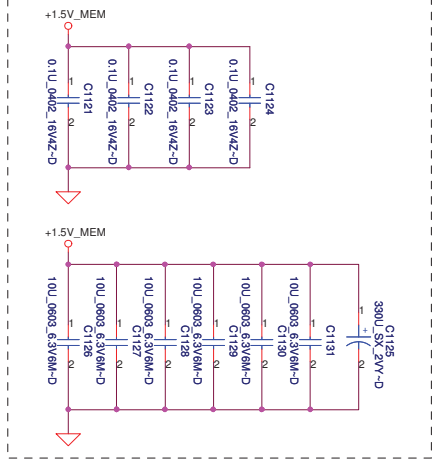
Compal Electronics, Inc.

Arrandale (6/6)

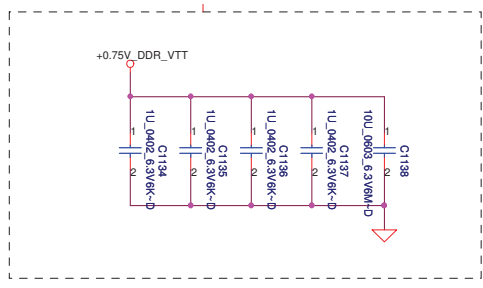
Title			
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- 9 DDR_A_DQS#[0..7] <<>
- 9 DDR_A_D[0..63] <<>
- 9 DDR_A_DM[0..7] <<>
- 9 DDR_A_DQS#[0..7] <<>
- 9 DDR_A_MA[0..15] <<>

Layout Note:
Place near JDIMMA

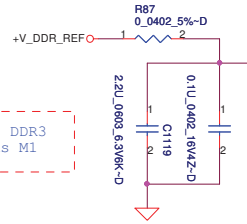


Layout Note:
Place near JDIMMA. 203, 204

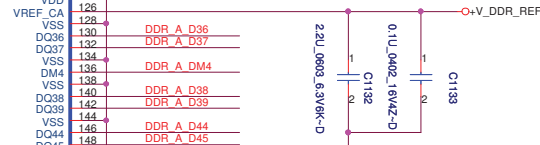
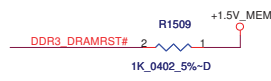
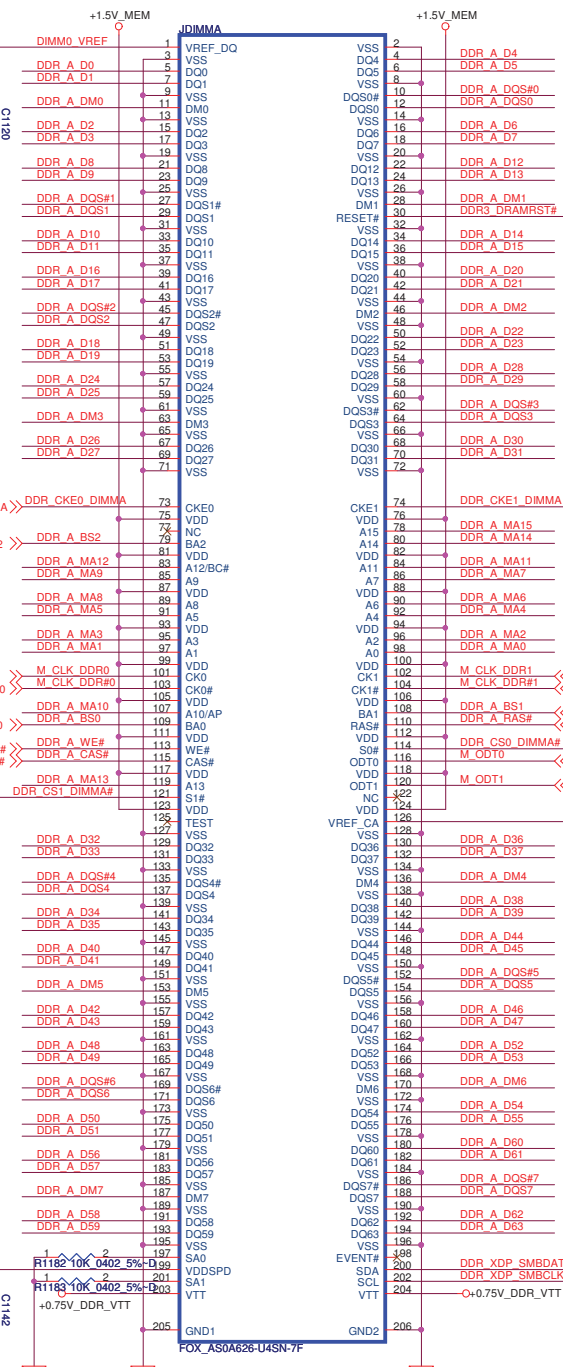
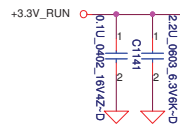


Populate R87 for Intel DDR3 VREFDQ multiple methods M1

Note:
Check voltage tolerance of VREF_DQ at the DIMM socket



- 9 DDR_CKE0_DIMMA >> DDR_CKE0_DIMMA
- 9 DDR_A_BS2 >> DDR_A_BS2
- 9 M_CLK_DDR0 >> M_CLK_DDR0
- 9 M_CLK_DDR#0 >> M_CLK_DDR#0
- 9 DDR_A_BS0 >> DDR_A_BS0
- 9 DDR_A_WE# >> DDR_A_WE#
- 9 DDR_A_CAS# >> DDR_A_CAS#
- 9 DDR_CS1_DIMMA# >> DDR_CS1_DIMMA#



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Title		DDRIII-SODIMM SLOT1	
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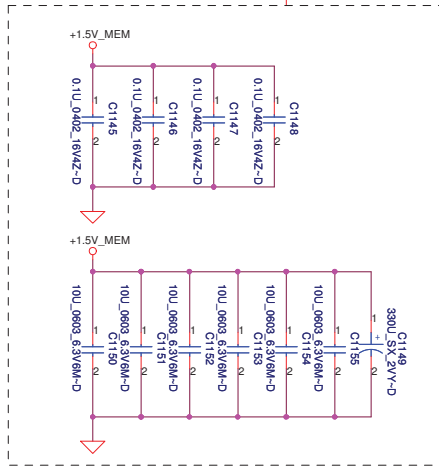
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- 9 DDR_B_DQS#(0.7) <<>
- 9 DDR_B_D[0..63] <<>
- 9 DDR_B_DM(0.7) <<>
- 9 DDR_B_DQS(0.7) <<>
- 9 DDR_B_MA[0..15] <>

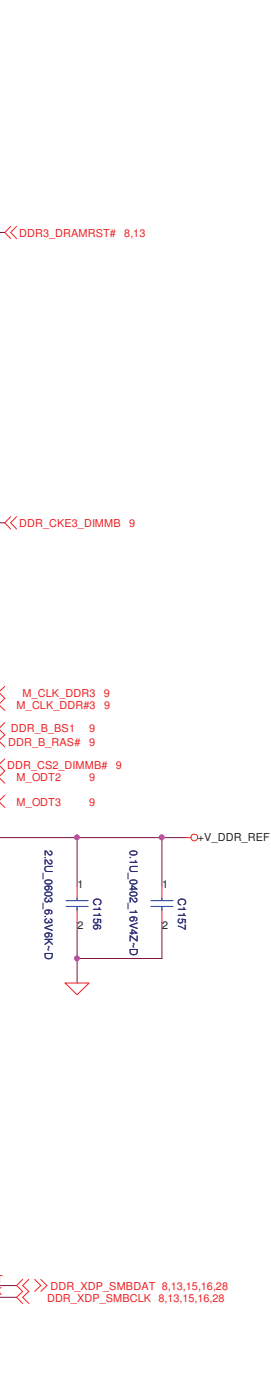
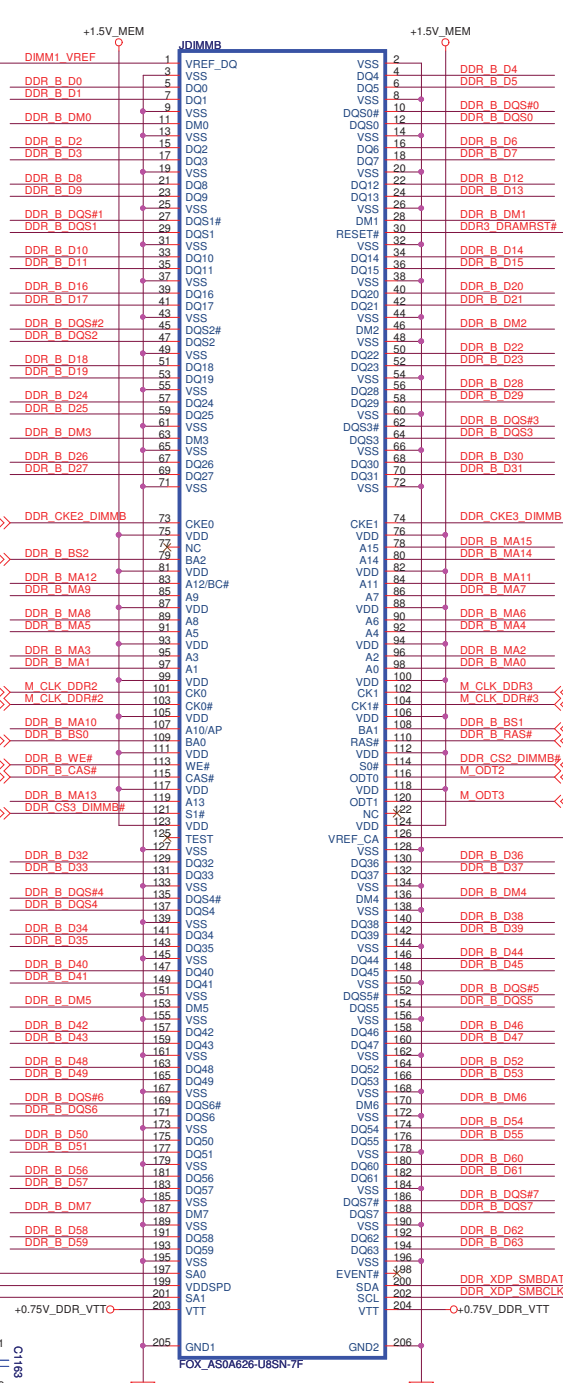
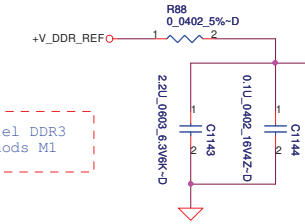
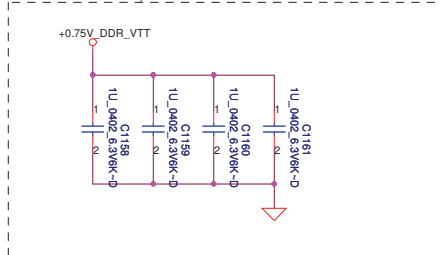
Populate R88 for Intel DDR3 VREFDQ multiple methods M1

Note:
Check voltage tolerance of VREF_DQ at the DIMM socket

Layout Note:
Place near JDIMMB



Layout Note:
Place near JDIMMB.203,204



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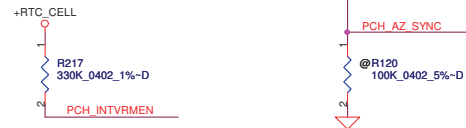


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DDRIII-SODIMM SLOT2		
File	Document Number	Rev
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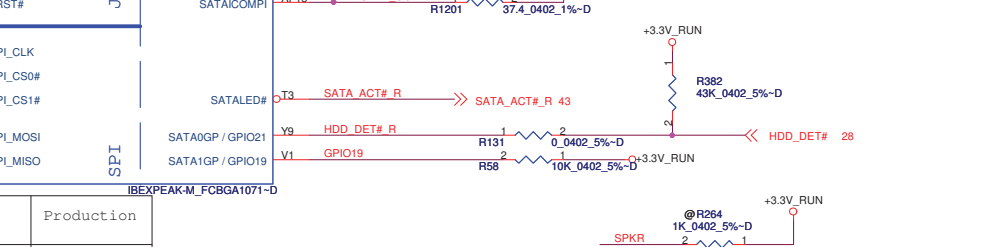
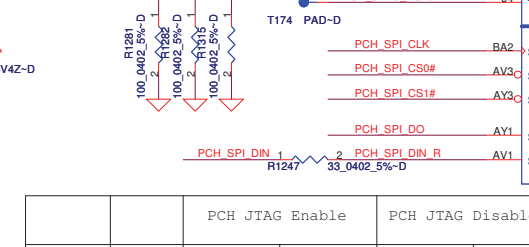
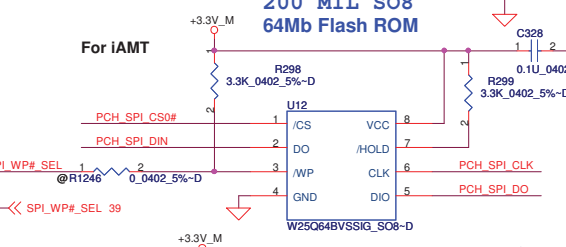
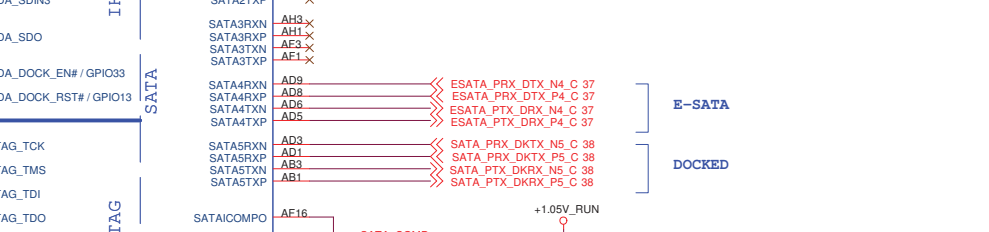
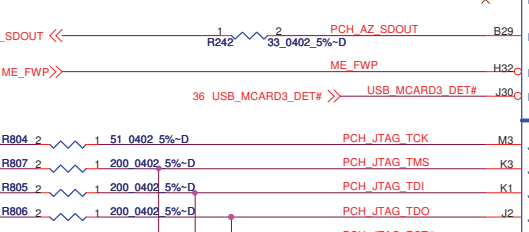
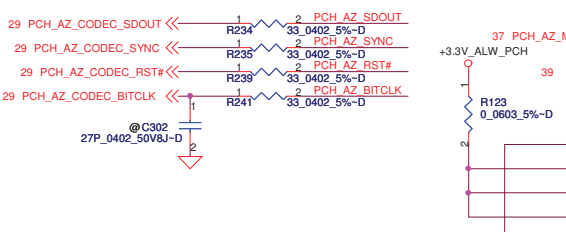
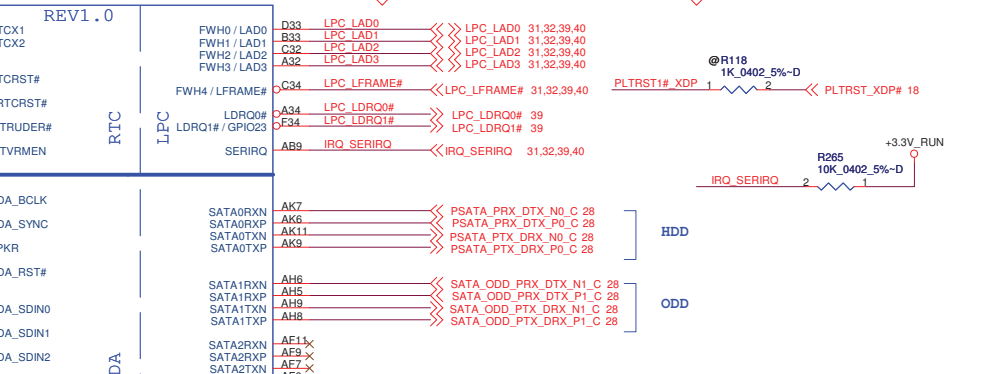
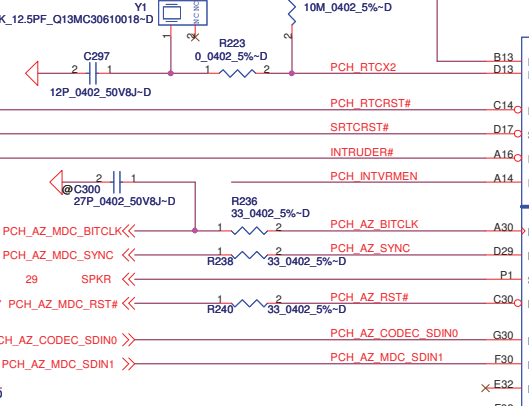
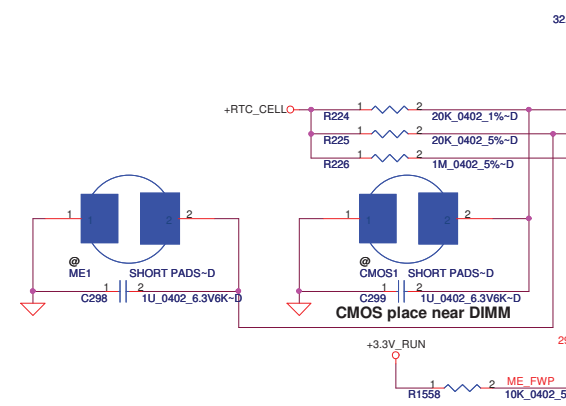
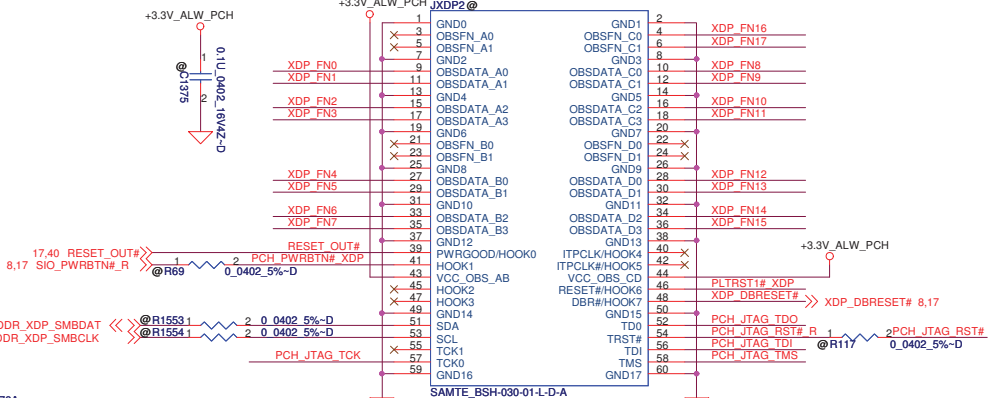
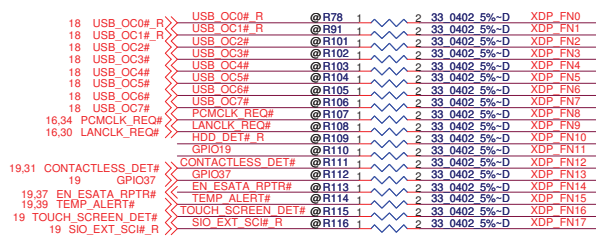
CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers



INTRVREN- Integrated SUS
 1.1V VRM Enable
 High - Enable Internal VRs

On Die PLL VR is supplied by
 1.5V when sampled high, 1.8 V
 when sampled low



PCH Pin	Ref.	PCH JTAG Enable		PCH JTAG Disable		Production
		ES1	ES2	ES1	ES2	
TDO	R806	No Stuff	200 ohm	No Stuff	No Stuff	200 ohm
	R1315	No Stuff	100 ohm	No Stuff	No Stuff	100 ohm
TMS	R807	200 ohm	200 ohm	No Stuff	No Stuff	200 ohm
	R1281	100 ohm	100 ohm	No Stuff	No Stuff	100 ohm
TDI	R805	200 ohm	200 ohm	20K ohm	No Stuff	200 ohm
	R1282	100 ohm	100 ohm	10K ohm	No Stuff	100 ohm
TCK	R804	4.7K ohm	4.7K ohm	4.7K ohm	4.7K ohm	51 ohm
TRST#	R808	20K ohm	No Stuff	No Stuff	No Stuff	No Stuff
	R1316	10K ohm	No Stuff	No Stuff	No Stuff	No Stuff

No Reboot Strap
SPKR
Low = Default
High = No Reboot

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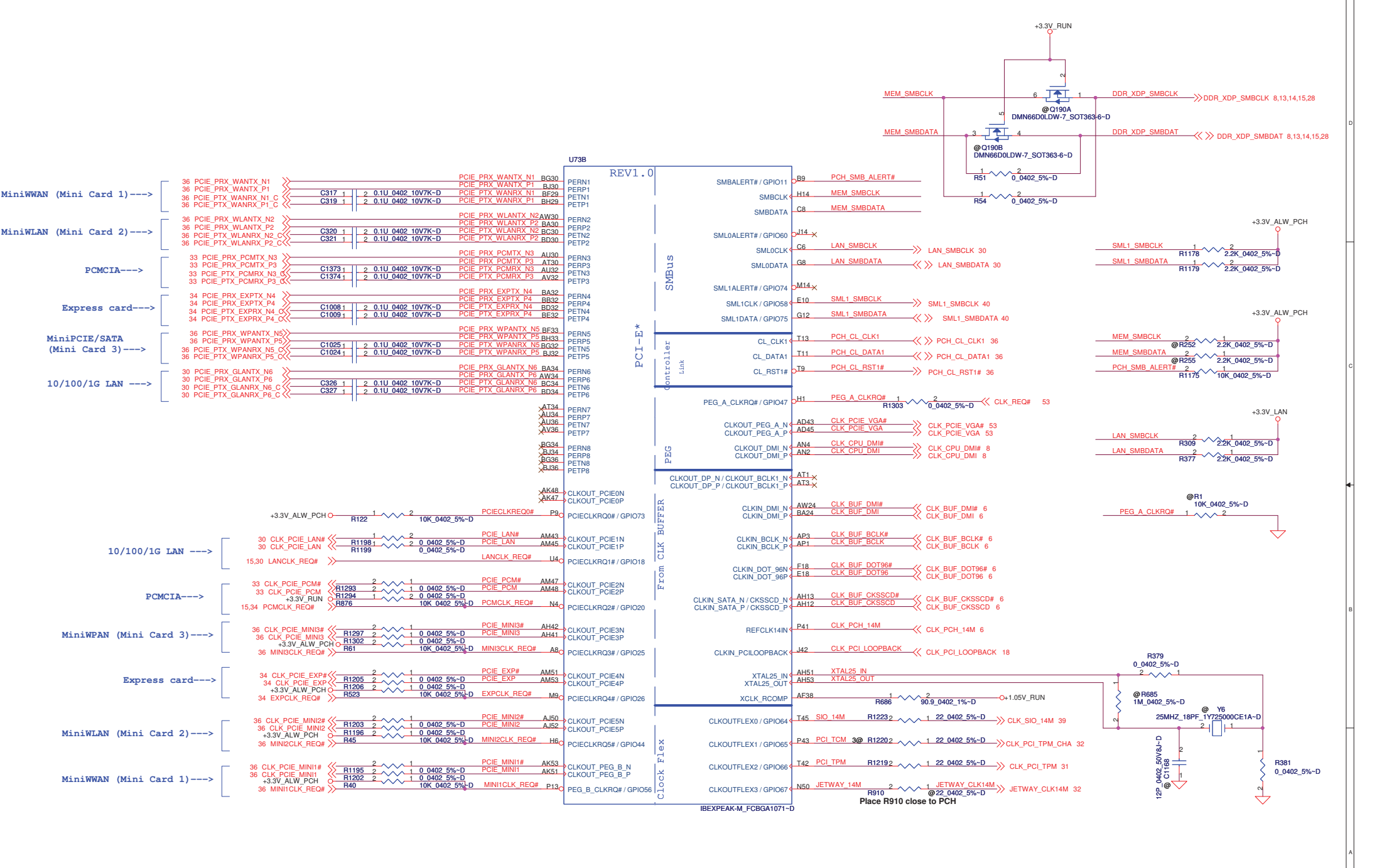
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PCH (1/8)

LA-5472P

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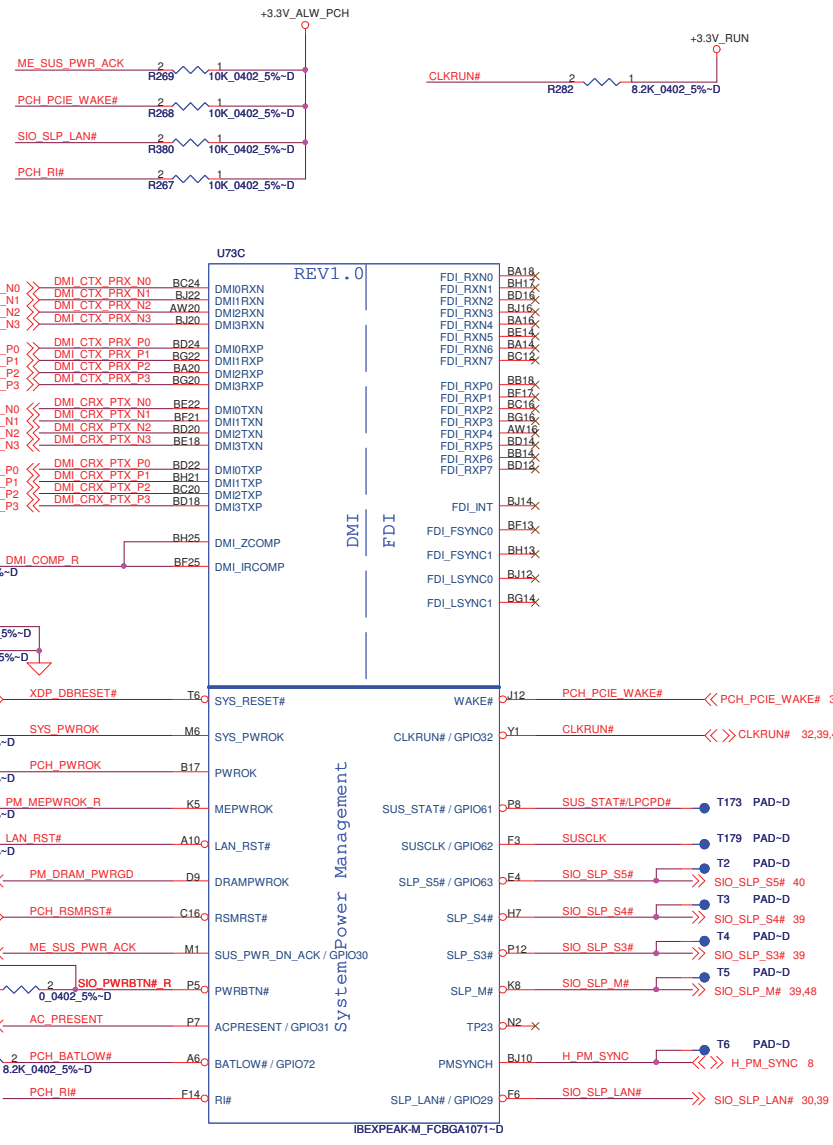
Compal Electronics, Inc.

PCH (2/8)

LA-5472P

Rev A00

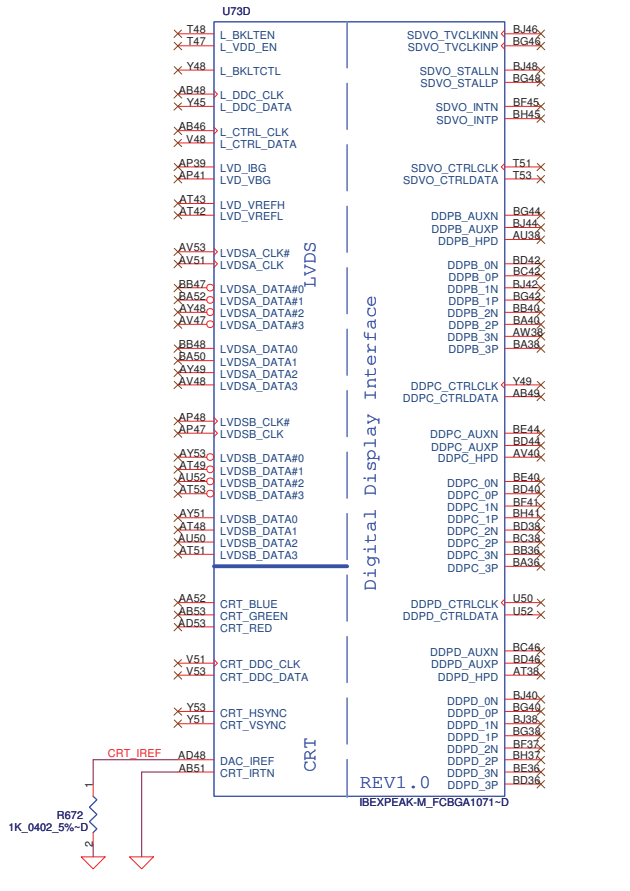
Date: Wednesday, January 20, 2010 Sheet 16 of 66



Intel WW18 Strapping option


PORT	STRAP	ENABLE	DISABLE
LVDS	L_DDC_DATA	PU to 3.3V through 2.2Kohm	NC
PORT B	SDVO_CTRLDATA	PU to 3.3V through 2.2Kohm	NC
PORT B	DDPC_CTRLDATA	PU to 3.3V through 2.2Kohm	NC
PORT B	DDPD_CTRLDATA	PU to 3.3V through 2.2Kohm	NC
eDP on CPU	CFG[4] (at CPU)	PD to GND through 3.3Kohm	NC

Intel request DDPB can not support eDP



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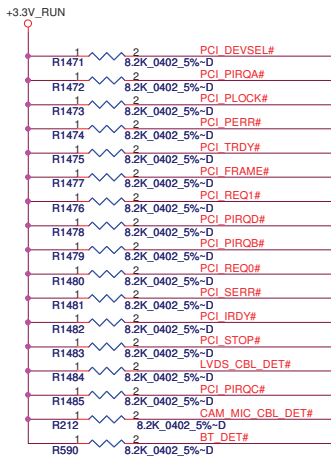


PCH (3/8)

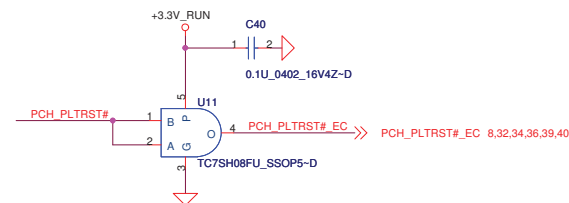
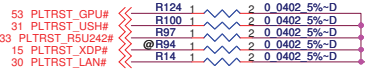
LA-5472P

Rev A00

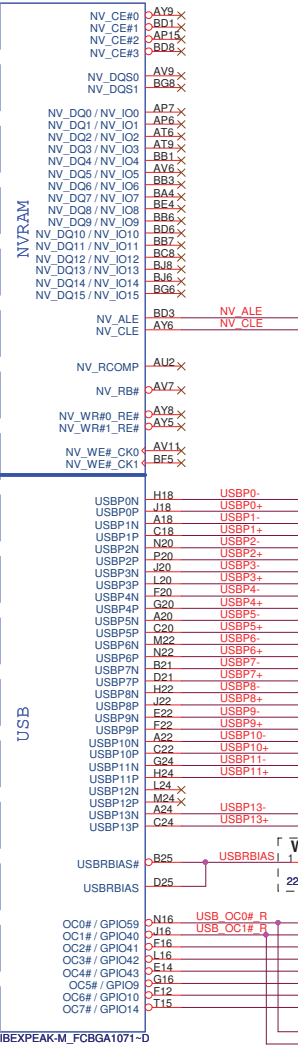
Title		PCH (3/8)	
Size	Document Number	Rev A00	
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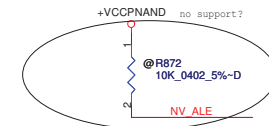
A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap High = Default



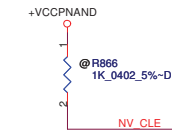
U73E
REV 1.0



PCH XDP ENABLE	Stuff: R78, R89, R101~R116
	No Stuff: R71, R77, RP1, RP2, R45, R40, R131, R58, R1242, R1243, R1244, R1245, R74, R130
PCH XDP DISABLE	Stuff: R71, R77, RP1, RP2, R45, R40, R131, R58, R1242, R1243, R1244, R1245, R74, R130
	No Stuff: R78, R89, R101~R116



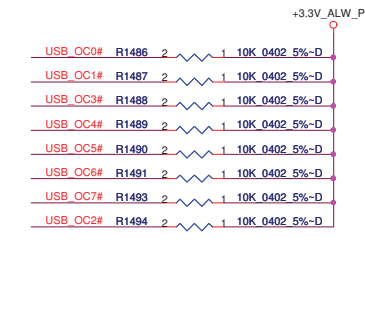
Danbury Technology Enabled	
NV_ALE	High = Enabled (Default) Low = Disabled



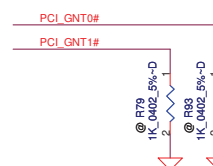
DMI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

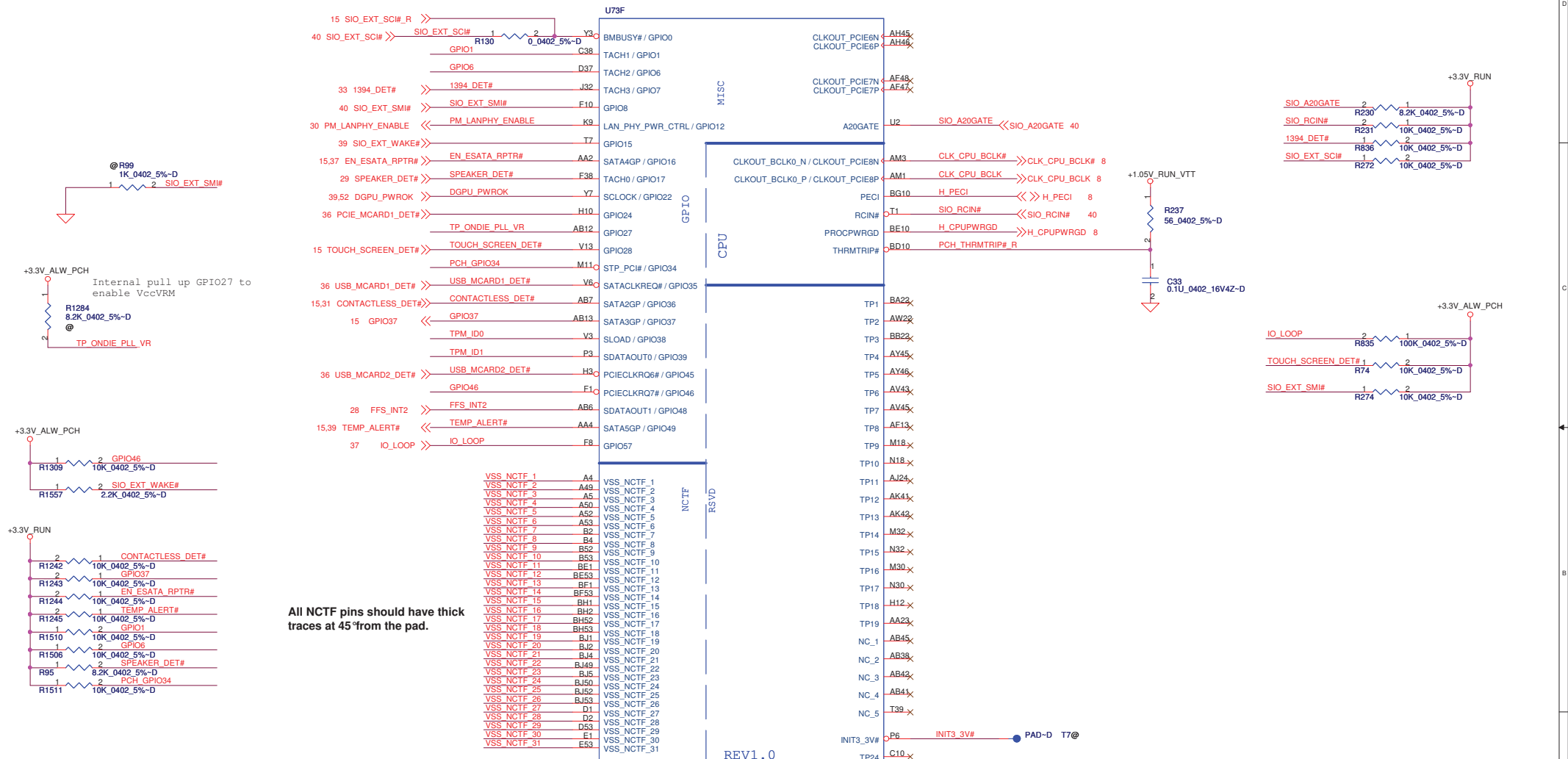
- >Right Side Top
- >Right Side Bottom
- >Left Side Top
- >Left Side Bottom
- >WLAN
- >WWAN
- >Blue Tooth
- >BIO_USH
- >DOCK
- >Express Card
- >Camera
- >WPAN

change base on Rothschild layout concern.



PCI_GNT#1	PCI_GNT#0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

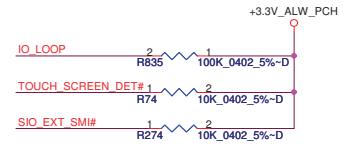
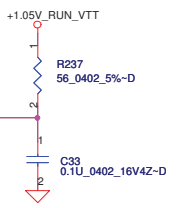
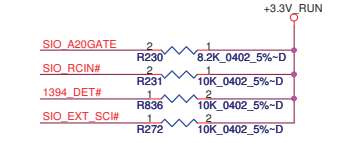
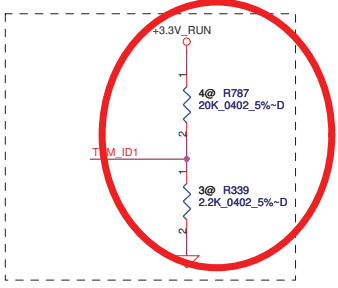
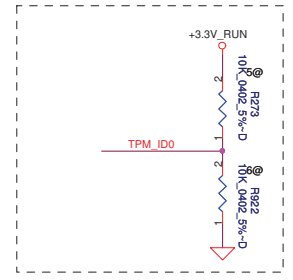
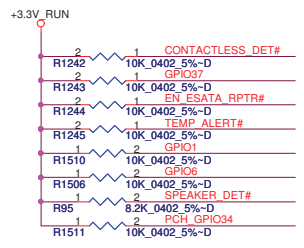
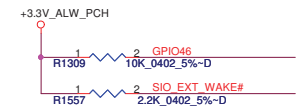
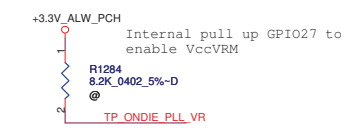
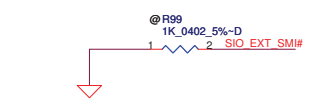




All NCTF pins should have thick traces at 45° from the pad.

- VSS_NCTF_1 A4
- VSS_NCTF_2 A49
- VSS_NCTF_3 A5
- VSS_NCTF_4 A50
- VSS_NCTF_5 A52
- VSS_NCTF_6 A53
- VSS_NCTF_7 B2
- VSS_NCTF_8 B4
- VSS_NCTF_9 B52
- VSS_NCTF_10 B53
- VSS_NCTF_11 BE1
- VSS_NCTF_12 BE53
- VSS_NCTF_13 BF1
- VSS_NCTF_14 BF53
- VSS_NCTF_15 BH1
- VSS_NCTF_16 BH2
- VSS_NCTF_17 BH52
- VSS_NCTF_18 BH53
- VSS_NCTF_19 BJ1
- VSS_NCTF_20 BJ2
- VSS_NCTF_21 BJ4
- VSS_NCTF_22 BJ49
- VSS_NCTF_23 BJ5
- VSS_NCTF_24 BJ50
- VSS_NCTF_25 BJ52
- VSS_NCTF_26 BJ53
- VSS_NCTF_27 D1
- VSS_NCTF_28 D2
- VSS_NCTF_29 D53
- VSS_NCTF_30 E1
- VSS_NCTF_31 E53

	TPM_ID0	TPM_ID1
China TPM	0	0
No TPM, No China TPM	0	1
Reserved	1	0
TPM	1	1

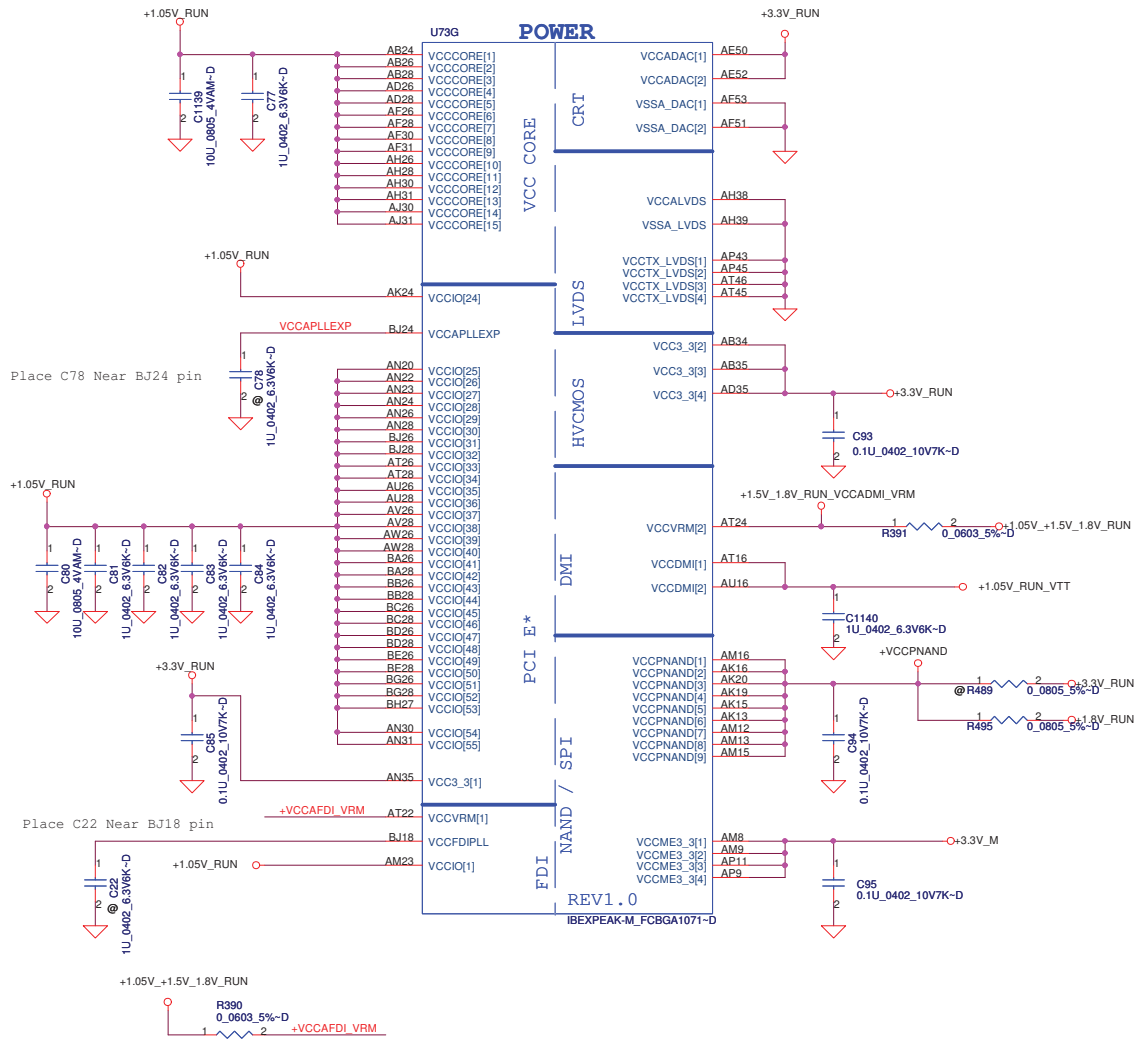


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PCH (5/8)

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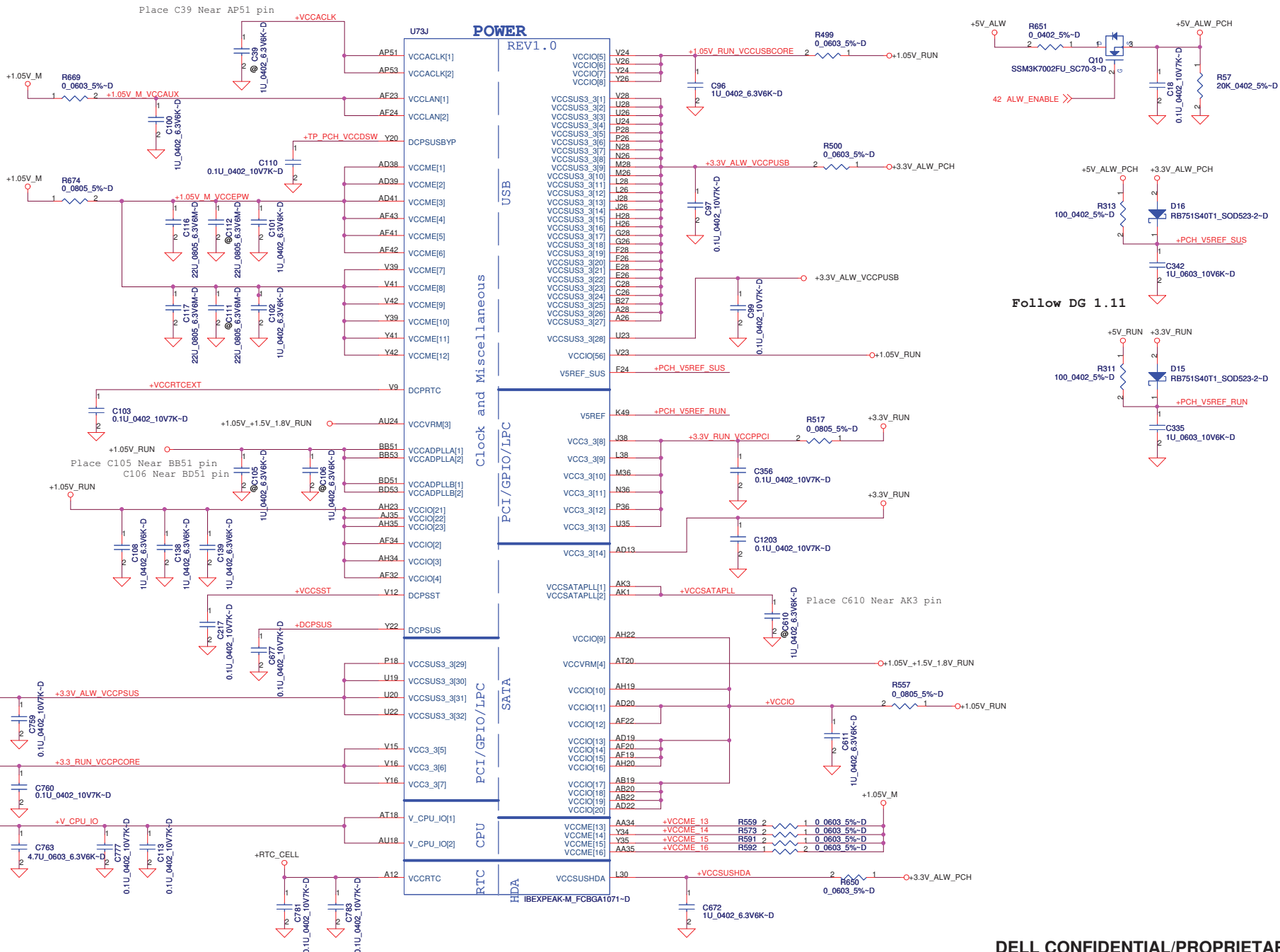
PCH Power Rail Table		
Voltage Rail	Voltage	SO Iccmax Current (A)
V_CPU_IO	1.1/1.05	< 1 (mA)
V5REF	5	< 1 (mA)
V5REF_Sus	5	< 1 (mA)
Vcc_3	3.3	0.357
VccAClk	1.1	0.052
VccADAC	3.3	0.069
VccADPLLA	1.1	0.068
VccADPLLB	1.1	0.069
Vccap11EXP	1.1	0.04
VccCore	1.1	1.432
VccDMI	1.1	0.058
VccDMI	1.1	0.061
VccFDIPLL	1.1	0.037
VccIO	1.1	3.062
VccLAN	1.1	0.32
VccME	1.1	1.849
VccME3_3	3.3	0.085
VccpNAND	1.8	0.156
VccRTC	3.3	2 (mA)
VccSATAPLL	1.1	0.031
VccSus_3_3	3.3	0.163
VccSusHDA	3.3	0.006
VccVRM	1.8 / 1.5	0.196
VccALVDS	3.3	< 1 (mA)
VccTX_LVDS	1.8	0.059



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Follow DG 1.11

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U73H		U73H	
AB16	VSS[0]		
AA19	VSS[1]	AK30	VSS[90]
AA20	VSS[2]	AK31	VSS[91]
AA22	VSS[3]	AK32	VSS[92]
AM19	VSS[4]	AK34	VSS[93]
AA24	VSS[5]	AK35	VSS[94]
AA26	VSS[6]	AK38	VSS[95]
AA28	VSS[7]	AK43	VSS[96]
AA30	VSS[8]	AK46	VSS[97]
AA31	VSS[9]	AK49	VSS[98]
AA32	VSS[10]	AK5	VSS[99]
AB11	VSS[11]	AK6	VSS[100]
AB15	VSS[12]	AL2	VSS[91]
AB23	VSS[13]	AL52	VSS[92]
AB30	VSS[14]	AM11	VSS[93]
AB31	VSS[15]	BB44	VSS[94]
AB32	VSS[16]	AD24	VSS[95]
AB39	VSS[17]	AM20	VSS[96]
AB43	VSS[18]	AM22	VSS[97]
AB47	VSS[19]	AM24	VSS[98]
AB5	VSS[20]	AM26	VSS[99]
AB8	VSS[21]	AM28	VSS[100]
AC2	VSS[22]	BA42	VSS[101]
AC52	VSS[23]	AM30	VSS[102]
AD11	VSS[24]	AM31	VSS[103]
AD12	VSS[25]	AM32	VSS[104]
AD16	VSS[26]	AM34	VSS[105]
AD23	VSS[27]	AM35	VSS[106]
AD30	VSS[28]	AM38	VSS[107]
AD31	VSS[29]	AM39	VSS[108]
AD32	VSS[30]	AM42	VSS[109]
AD34	VSS[31]	AU20	VSS[110]
AU22	VSS[32]	AM46	VSS[111]
AD42	VSS[33]	AV22	VSS[112]
AD46	VSS[34]	AM49	VSS[113]
AD49	VSS[35]	AM7	VSS[114]
AD7	VSS[36]	AA50	VSS[115]
AE2	VSS[37]	BB10	VSS[116]
AE4	VSS[38]	AN48	VSS[117]
AF12	VSS[39]	AN50	VSS[118]
Y13	VSS[40]	AN52	VSS[119]
AH49	VSS[41]	AP12	VSS[120]
AU4	VSS[42]	AP23	VSS[121]
AF35	VSS[43]	AP46	VSS[122]
AP13	VSS[44]	AP49	VSS[123]
AN34	VSS[45]	AP24	VSS[124]
AF45	VSS[46]	AP2	VSS[125]
AF46	VSS[47]	AR2	VSS[126]
AF49	VSS[48]	AR52	VSS[127]
AF5	VSS[49]	AT11	VSS[128]
AF9	VSS[50]	BA12	VSS[129]
AG2	VSS[51]	AH48	VSS[130]
AG52	VSS[52]	AT32	VSS[131]
AH11	VSS[53]	AT36	VSS[132]
AH15	VSS[54]	AT41	VSS[133]
AH16	VSS[55]	AT47	VSS[134]
AH24	VSS[56]	AT7	VSS[135]
AH32	VSS[57]	AV12	VSS[136]
AV18	VSS[58]	AV16	VSS[137]
AH43	VSS[59]	AV20	VSS[138]
AH7	VSS[60]	AV24	VSS[139]
AJ19	VSS[61]	AV30	VSS[140]
AJ2	VSS[62]	AV34	VSS[141]
AJ20	VSS[63]	AV42	VSS[142]
AJ22	VSS[64]	AV46	VSS[143]
AJ23	VSS[65]	AV49	VSS[144]
AJ26	VSS[66]	AV5	VSS[145]
AJ28	VSS[67]	AV8	VSS[146]
AJ32	VSS[68]	AW14	VSS[147]
AJ34	VSS[69]	AW18	VSS[148]
AT5	VSS[70]	AW2	VSS[149]
AJ4	VSS[71]	BF9	VSS[150]
AK12	VSS[72]	AW32	VSS[151]
AM41	VSS[73]	AW36	VSS[152]
AN19	VSS[74]	AW40	VSS[153]
AK26	VSS[75]	AW52	VSS[154]
AK22	VSS[76]	AY11	VSS[155]
AK23	VSS[77]	AY43	VSS[156]
VSS[78]		AY47	VSS[157]
AK28	VSS[79]		VSS[158]

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IBEXPEAK-M_FCBGA1071-D

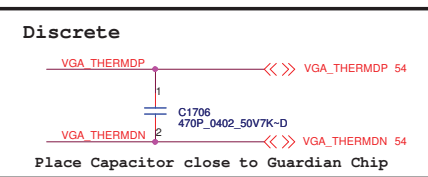
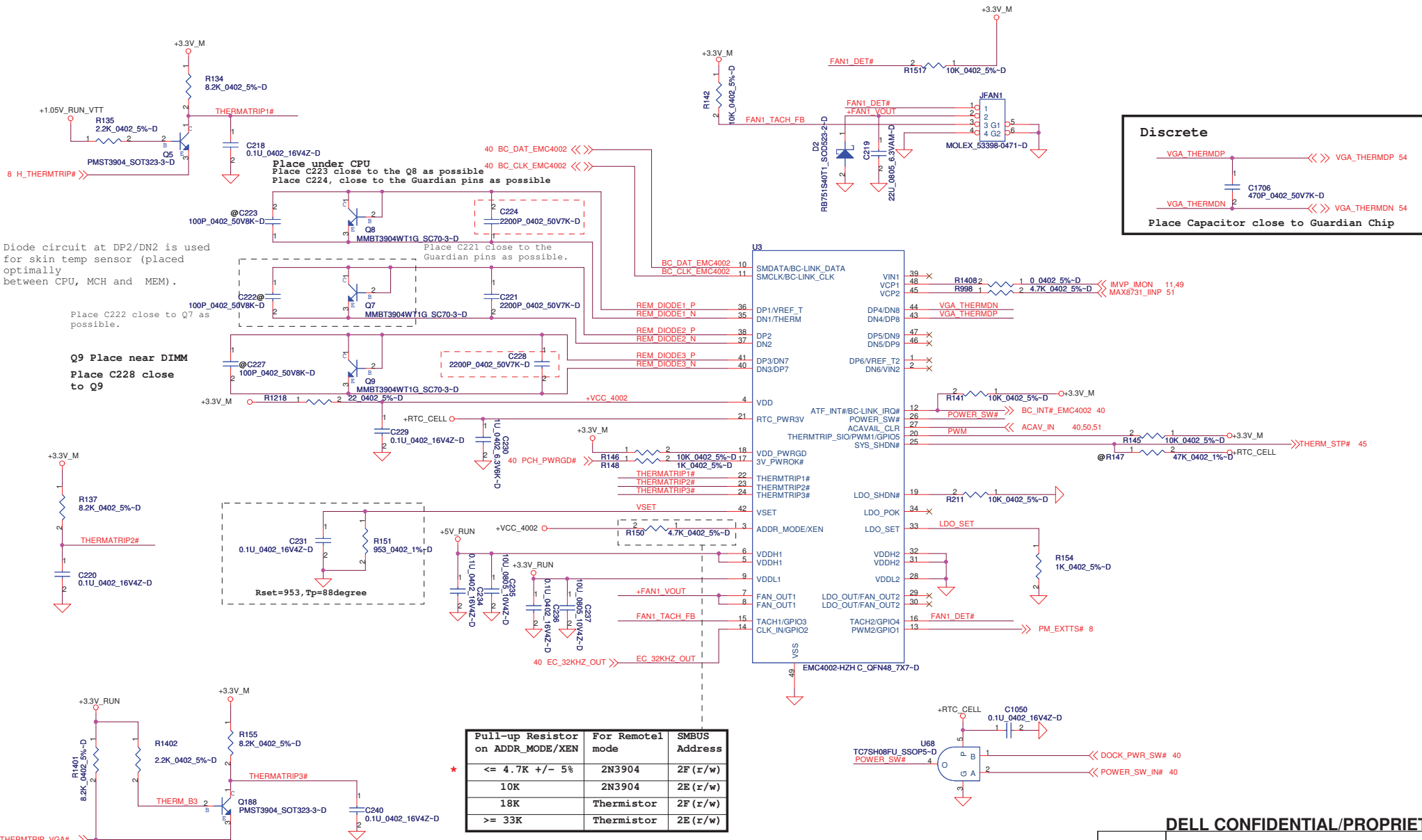
U73I		U73I	
AY7	VSS[159]	H49	VSS[258]
B11	VSS[160]	H5	VSS[260]
B15	VSS[161]	J24	VSS[261]
B19	VSS[162]	K11	VSS[262]
B23	VSS[163]	K43	VSS[263]
B31	VSS[164]	K47	VSS[264]
B35	VSS[165]	K7	VSS[265]
B39	VSS[166]	L14	VSS[266]
B43	VSS[167]	L18	VSS[267]
B47	VSS[168]	L2	VSS[268]
B7	VSS[169]	L22	VSS[269]
B12	VSS[170]	L36	VSS[270]
BB16	VSS[171]	L40	VSS[271]
BB20	VSS[172]	L52	VSS[272]
BB24	VSS[173]	M12	VSS[273]
BB30	VSS[174]	M16	VSS[274]
BB34	VSS[175]	M20	VSS[275]
BB38	VSS[176]	M38	VSS[276]
BB42	VSS[177]	M42	VSS[277]
BB49	VSS[178]	M44	VSS[278]
BBS	VSS[179]	M49	VSS[279]
BC10	VSS[180]	M5	VSS[280]
BC14	VSS[181]	M46	VSS[281]
BC18	VSS[182]	M49	VSS[282]
BC2	VSS[183]	M5	VSS[283]
BC22	VSS[184]	M8	VSS[284]
BC26	VSS[185]	M24	VSS[285]
BC32	VSS[186]	P11	VSS[286]
BC40	VSS[187]	AD15	VSS[287]
BC44	VSS[188]	P22	VSS[288]
BC52	VSS[189]	P30	VSS[289]
BD48	VSS[190]	P32	VSS[290]
BD49	VSS[191]	P4	VSS[291]
BD5	VSS[192]	P42	VSS[292]
BE12	VSS[193]	R2	VSS[293]
BE16	VSS[194]	R2	VSS[294]
BE20	VSS[195]	R52	VSS[295]
BE24	VSS[196]	T12	VSS[296]
BE30	VSS[197]	T41	VSS[297]
BE38	VSS[198]	T49	VSS[298]
BE42	VSS[199]	T46	VSS[299]
BE46	VSS[200]	T5	VSS[300]
BE49	VSS[201]	T8	VSS[301]
BE50	VSS[202]	U30	VSS[302]
BE52	VSS[203]	U31	VSS[303]
BE54	VSS[204]	U32	VSS[304]
BE56	VSS[205]	U34	VSS[305]
BE6	VSS[206]	P38	VSS[306]
BE8	VSS[207]	P16	VSS[307]
BE9	VSS[208]	P11	VSS[308]
BEF1	VSS[209]	V19	VSS[309]
BG18	VSS[210]	V20	VSS[310]
BG24	VSS[211]	V22	VSS[311]
BG50	VSS[212]	V30	VSS[312]
BH11	VSS[213]	V31	VSS[313]
BH15	VSS[214]	V32	VSS[314]
BH19	VSS[215]	V34	VSS[315]
BH23	VSS[216]	V36	VSS[316]
BH31	VSS[217]	V38	VSS[317]
BH35	VSS[218]	V43	VSS[318]
BH43	VSS[219]	V45	VSS[319]
BH47	VSS[220]	V46	VSS[320]
BH7	VSS[221]	V47	VSS[321]
C12	VSS[222]	V49	VSS[322]
C50	VSS[223]	V7	VSS[323]
D51	VSS[224]	V8	VSS[324]
E12	VSS[225]	W2	VSS[325]
E20	VSS[226]	W52	VSS[326]
E24	VSS[227]	Y11	VSS[327]
E34	VSS[228]	Y15	VSS[328]
E38	VSS[229]	Y19	VSS[329]
E42	VSS[230]	Y23	VSS[330]
E46	VSS[231]	Y28	VSS[331]
E48	VSS[232]	Y28	VSS[332]
E49	VSS[233]	Y31	VSS[333]
E8	VSS[234]	Y36	VSS[334]
F49	VSS[235]	Y38	VSS[335]
F5	VSS[236]	Y43	VSS[336]
G10	VSS[237]	Y46	VSS[337]
G14	VSS[238]	Y46	VSS[338]
G18	VSS[239]	Y46	VSS[339]
G2	VSS[240]	Y46	VSS[340]
G22	VSS[241]	Y49	VSS[341]
G32	VSS[242]	Y6	VSS[342]
G36	VSS[243]	Y8	VSS[343]
G40	VSS[244]	Y8	VSS[344]
G44	VSS[245]	P24	VSS[345]
G52	VSS[246]	T43	VSS[346]
AF39	VSS[247]	AD51	VSS[347]
H16	VSS[248]	AT8	VSS[348]
H20	VSS[249]	AD47	VSS[349]
H34	VSS[250]	Y47	VSS[350]
H38	VSS[251]	AT12	VSS[351]
H42	VSS[252]	AM6	VSS[352]
	VSS[253]	AT13	VSS[353]
	VSS[254]	AM5	VSS[354]
	VSS[255]	AK45	VSS[355]
	VSS[256]	AK39	VSS[356]
	VSS[257]	AV14	VSS[357]
	VSS[258]		

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Compal Electronics, Inc.		
PCH (8/8)		
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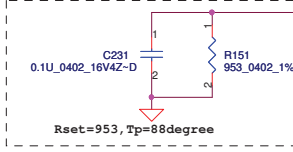
Diode circuit at DP2/DN2 is used for skin temp sensor (placed optimally between CPU, MCH and MEM).

Place C222 close to Q7 as possible.

Q9 Place near DIMM Place C228 close to Q9

Place C223 close to the Q8 as possible Place C224, close to the Guardian pins as possible

Place C221 close to the Guardian pins as possible.



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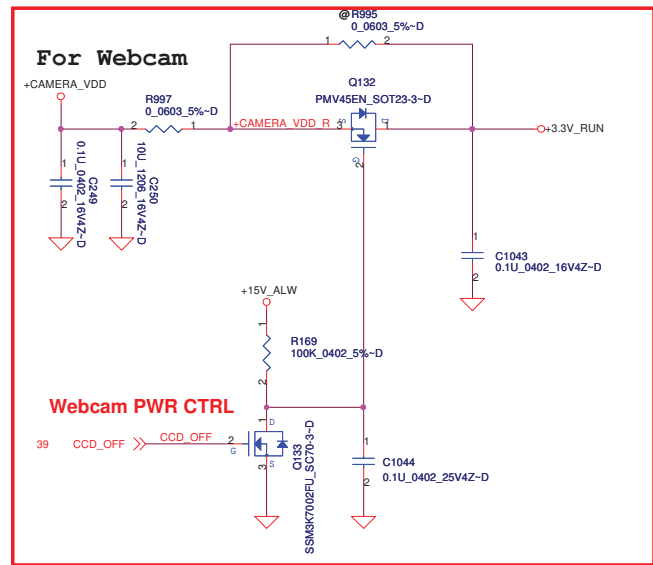
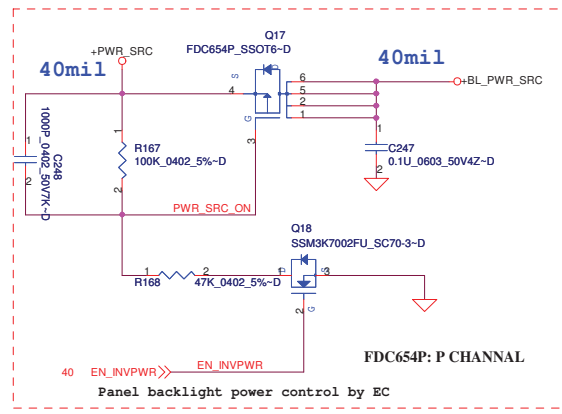
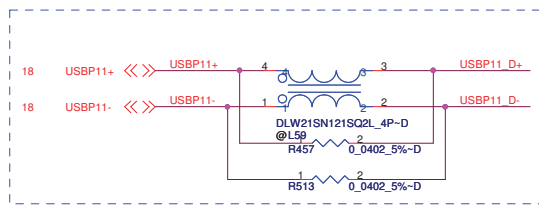
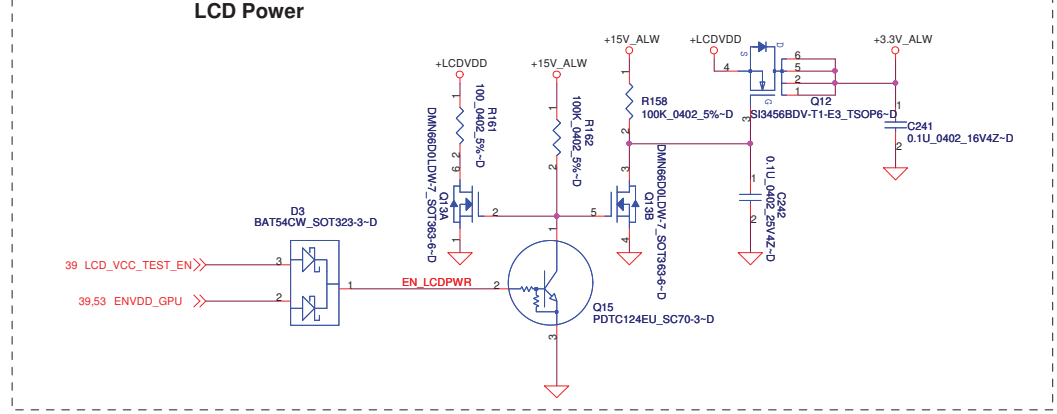
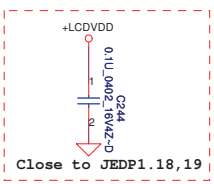
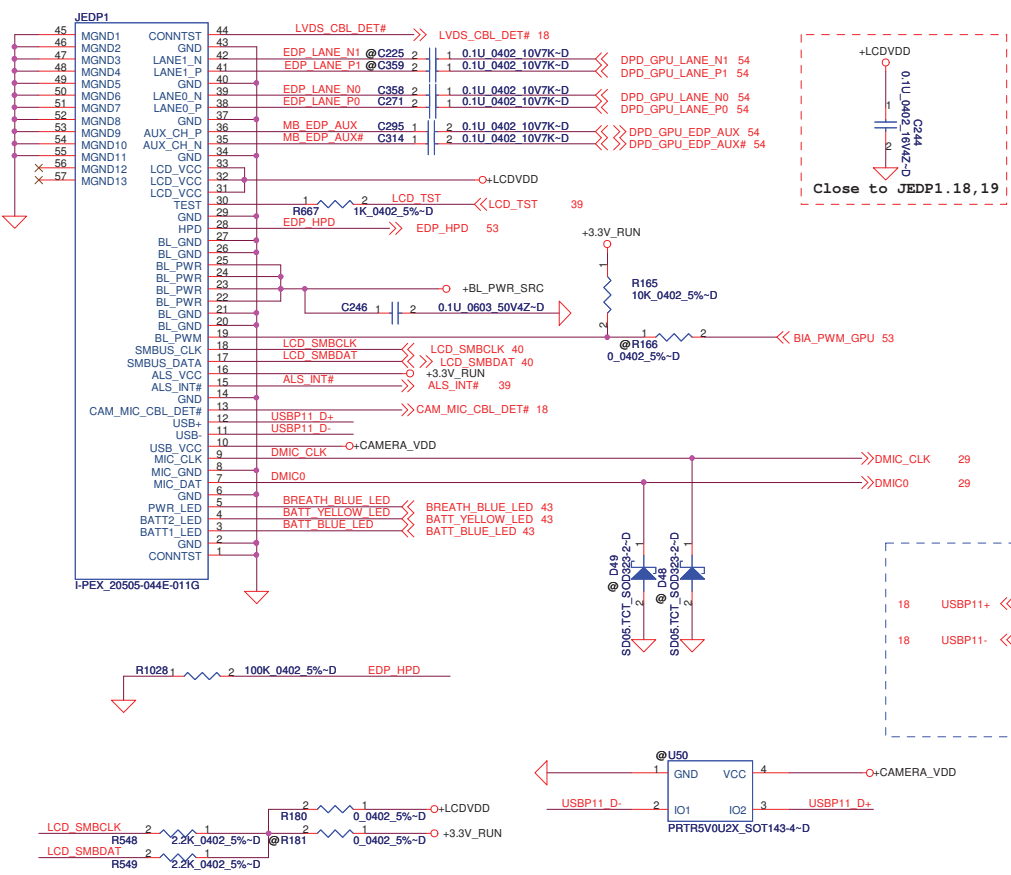
FAN & Thermal Sensor

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LCD Power



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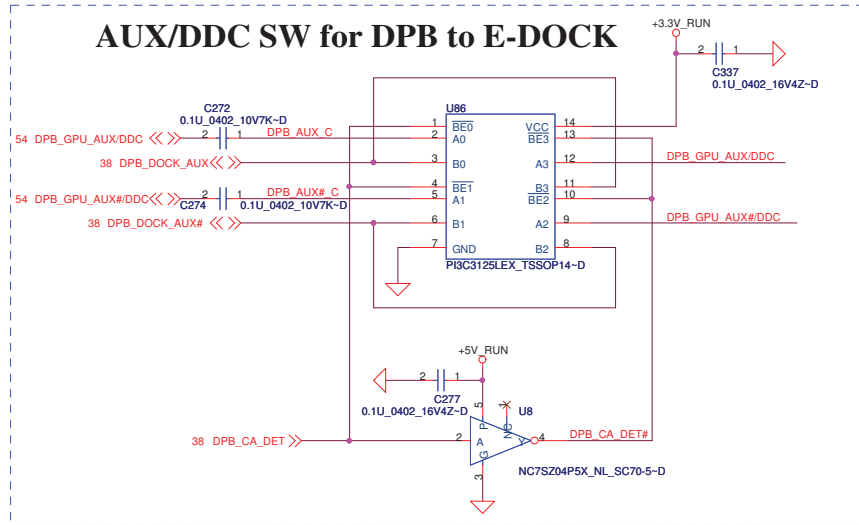
Compal Electronics, Inc.

Title: eDP & CAM Conn

Size: Document Number: LA-5472P

Date: Wednesday, January 20, 2010 Sheet 24 of 66

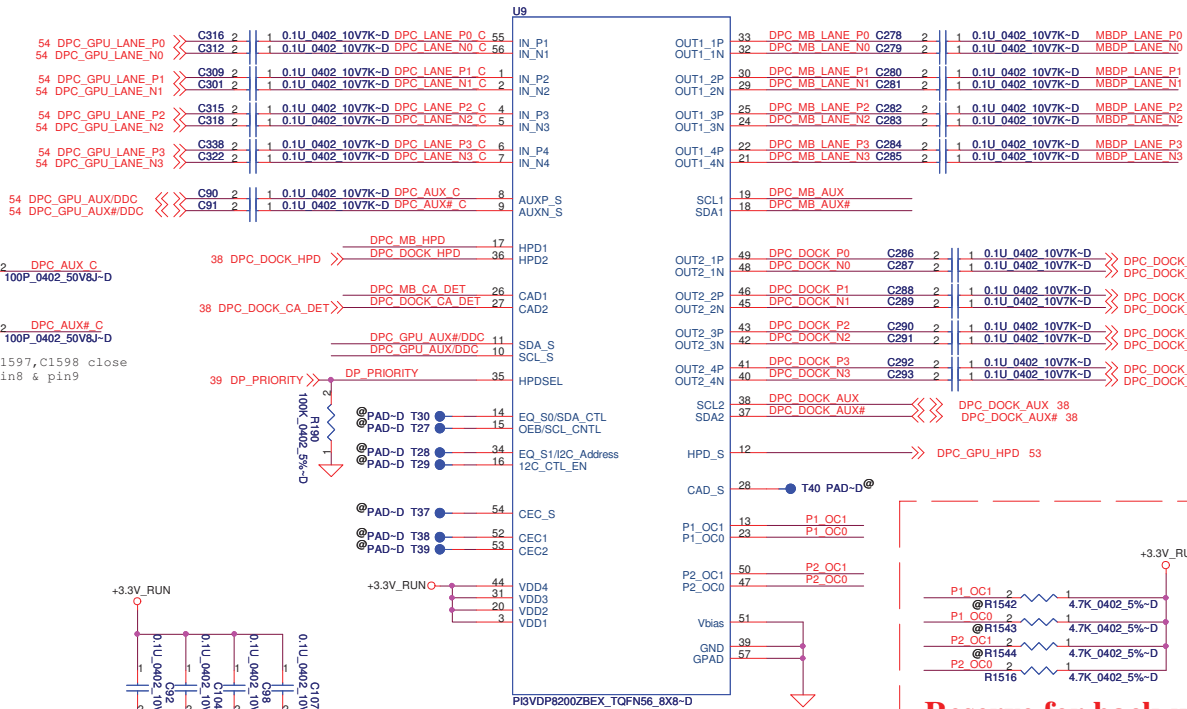
AUX/DDC SW for DPB to E-DOCK



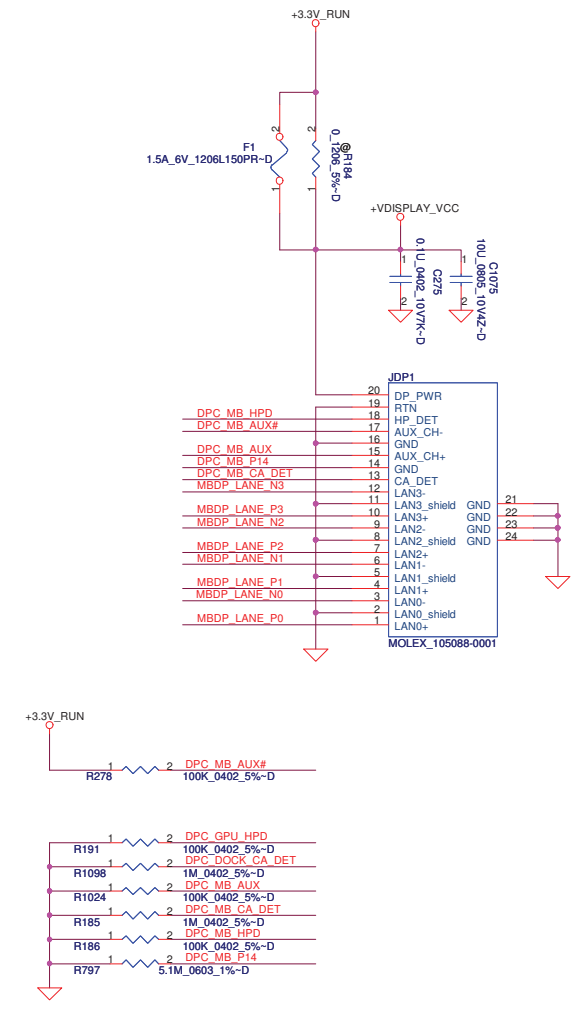
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Compal Electronics, Inc.			
DPB AUX SW for DOCK			
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DPB SW for MB & DOCK



Display port Connector



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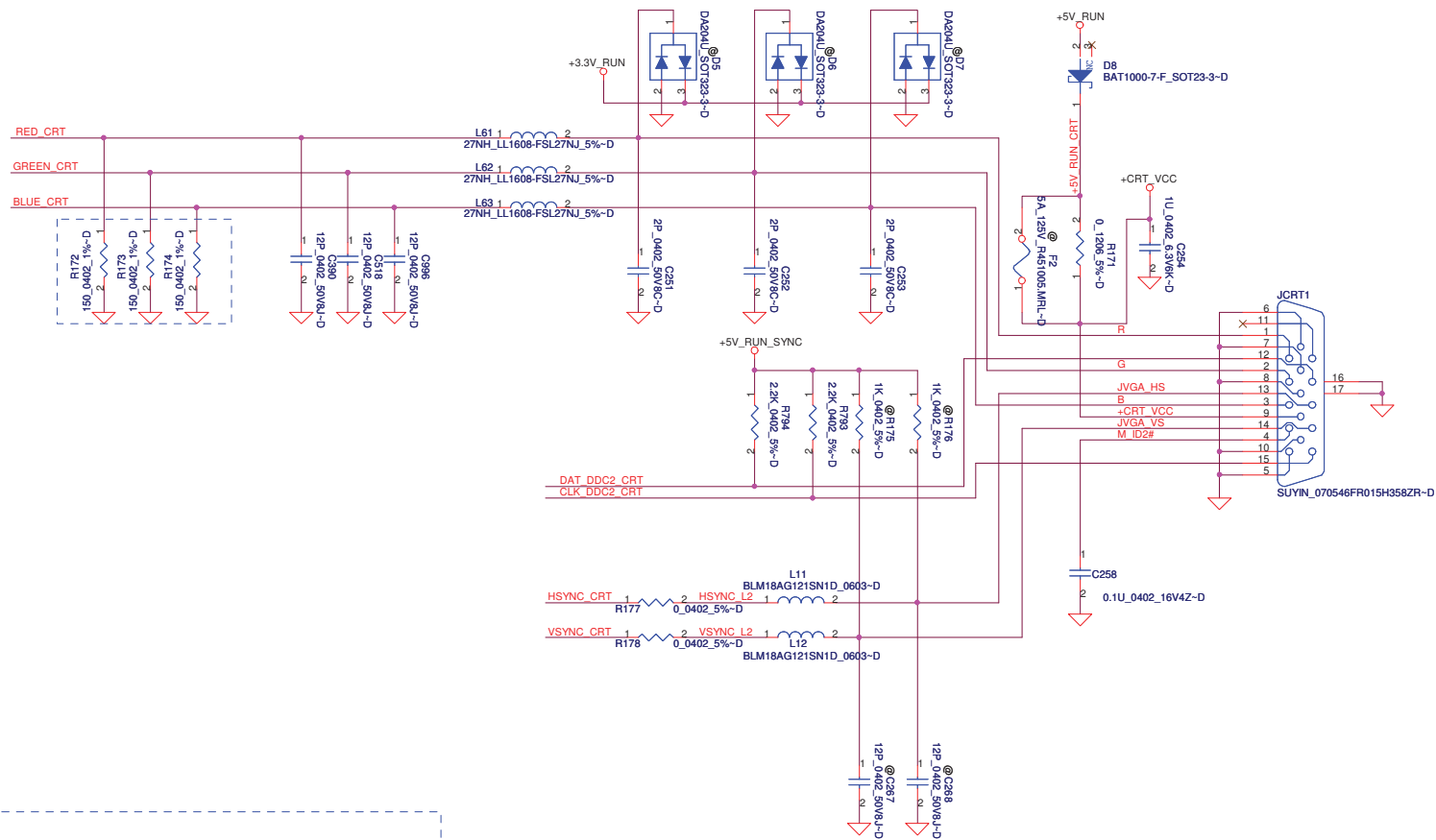
Compal Electronics, Inc.

Title: Display port

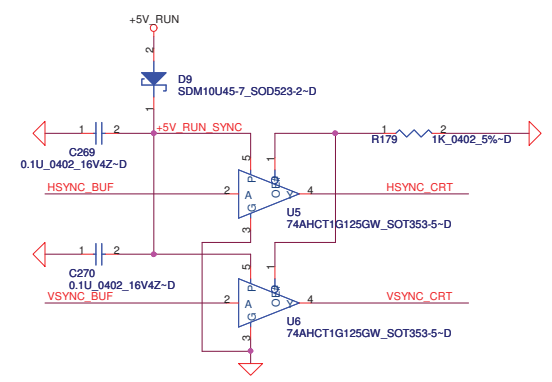
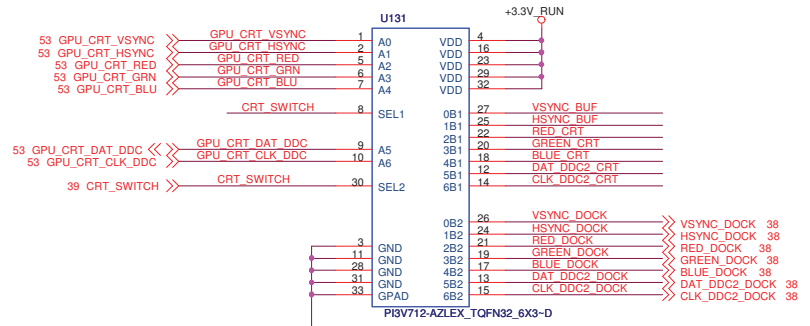
Size: Document Number LA-5472P

Date: Wednesday, January 20, 2010 Sheet 26 of 66

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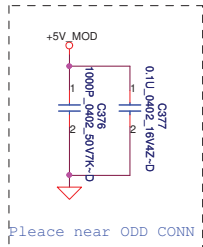
VGA SW for MB/DOCK



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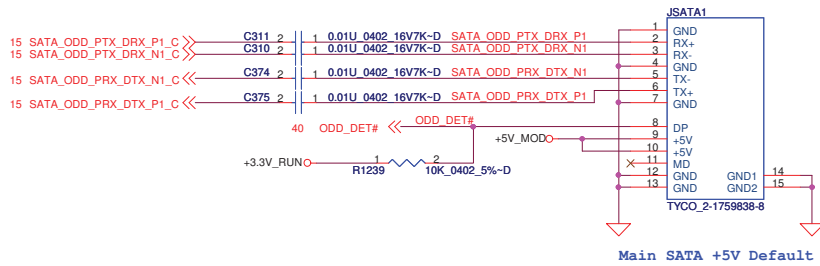
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	Compal Electronics, Inc.		
	CRT/Video switch		
	LA-5472P		
Size	Document Number	Rev	
Date	Wednesday, January 20, 2010	Sheet	27 of 66

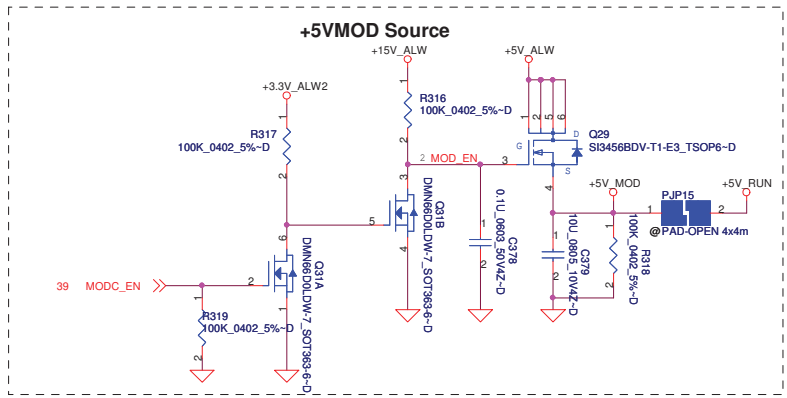


Please near ODD CONN

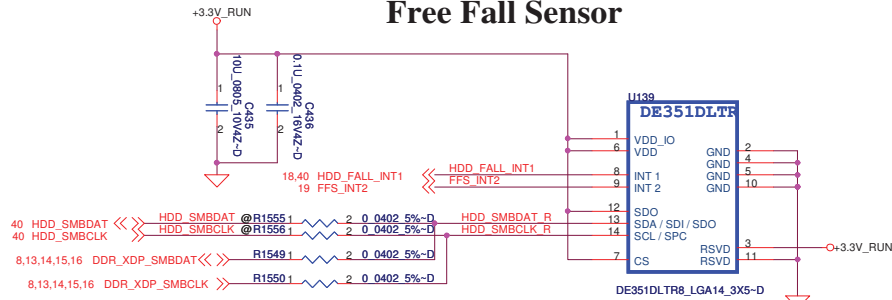
For ODD



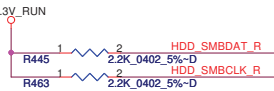
Main SATA +5V Default



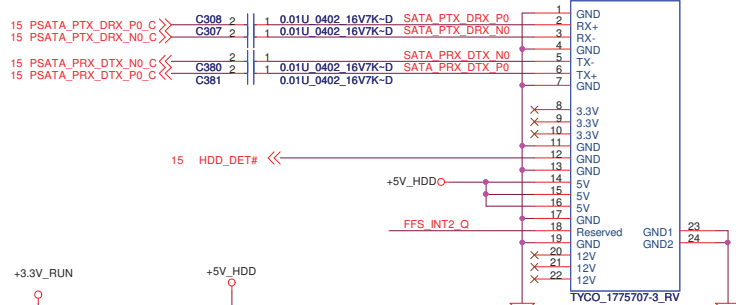
Free Fall Sensor



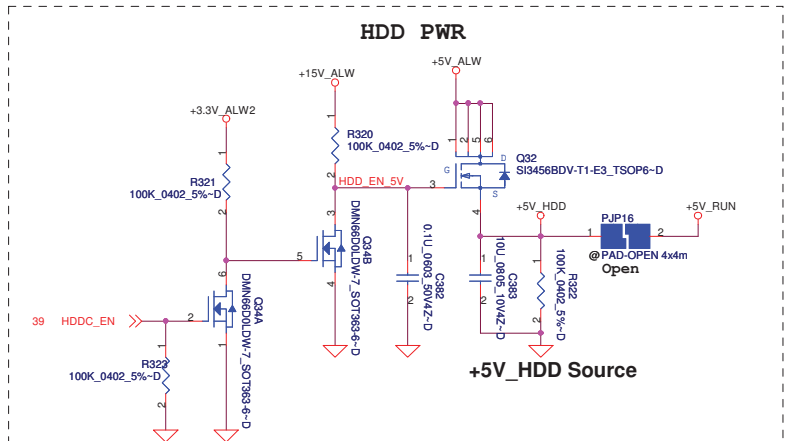
DE351DLTR8 LGA14_3X5-D



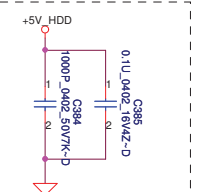
For HDD



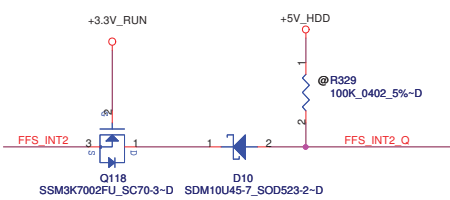
Main SATA +5V Default



+5V_HDD Source



Please near HDD CONN



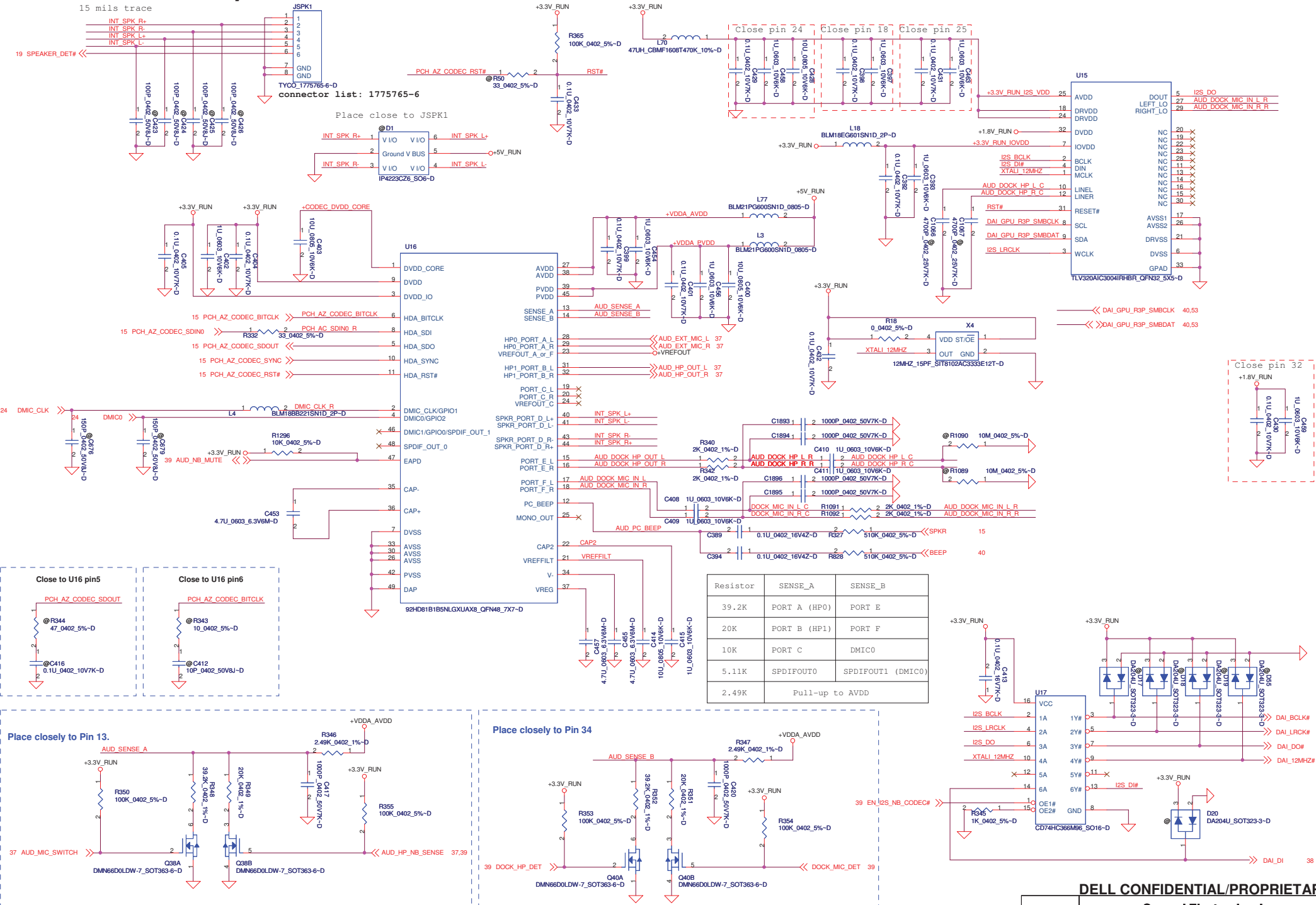
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Compal Electronics, Inc.

Title			
ODD/HDD CONNECTOR			
Size	Document Number	Rev	
	LA-5472P	A00	
Date:	Wednesday, January 20, 2010	Sheet	28 of 66

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Speaker Connector



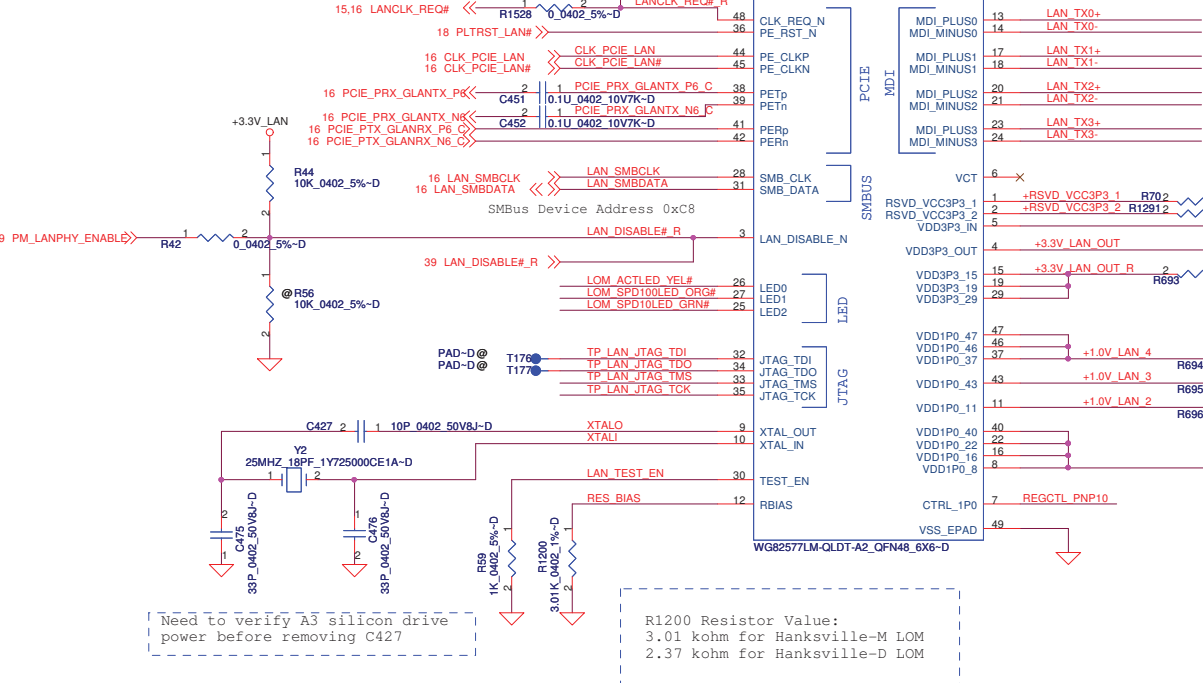
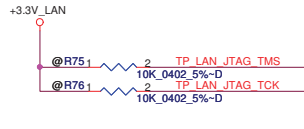
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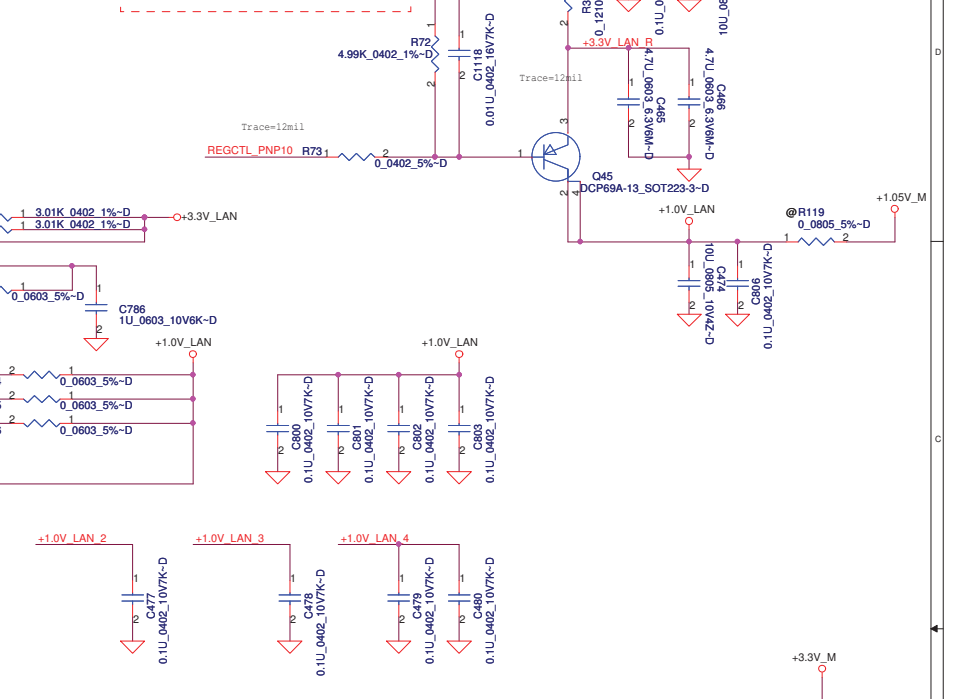


Title		Azalia (HD) Codec	
Size	Document Number	LA-5472P	
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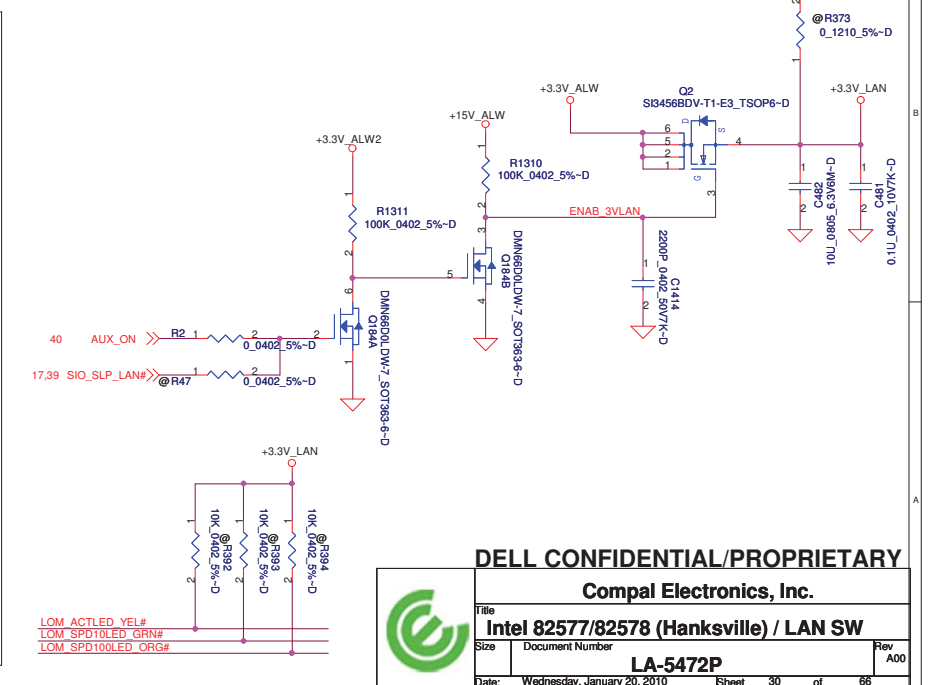
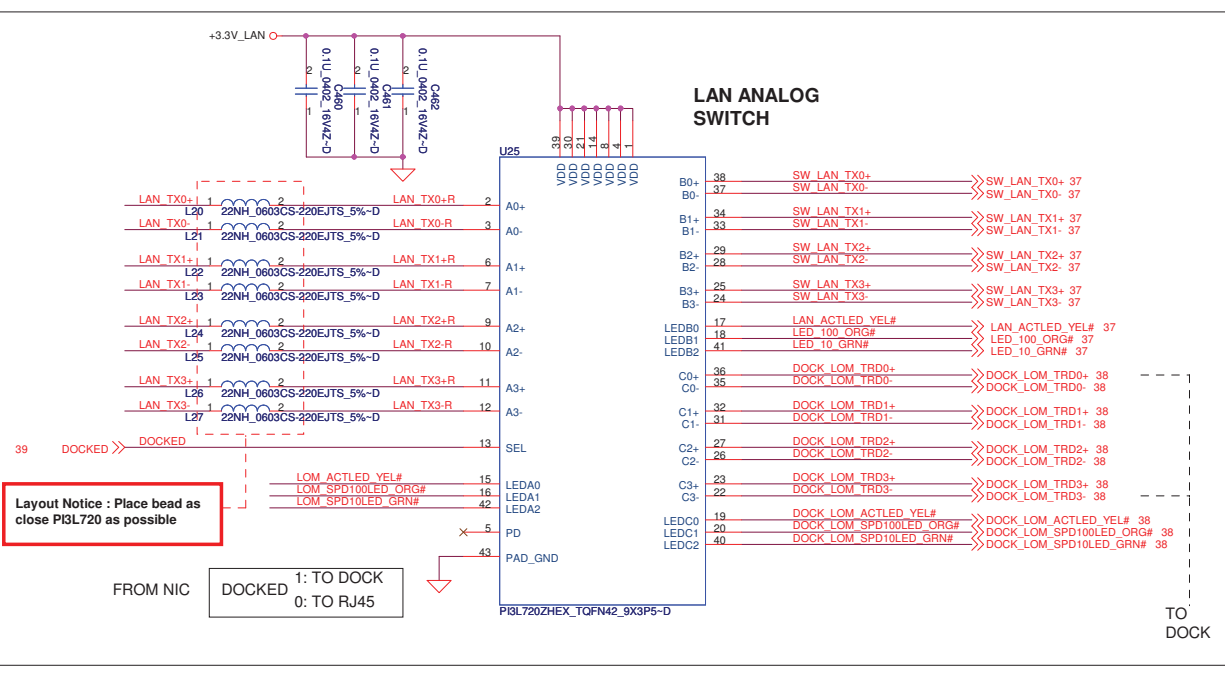


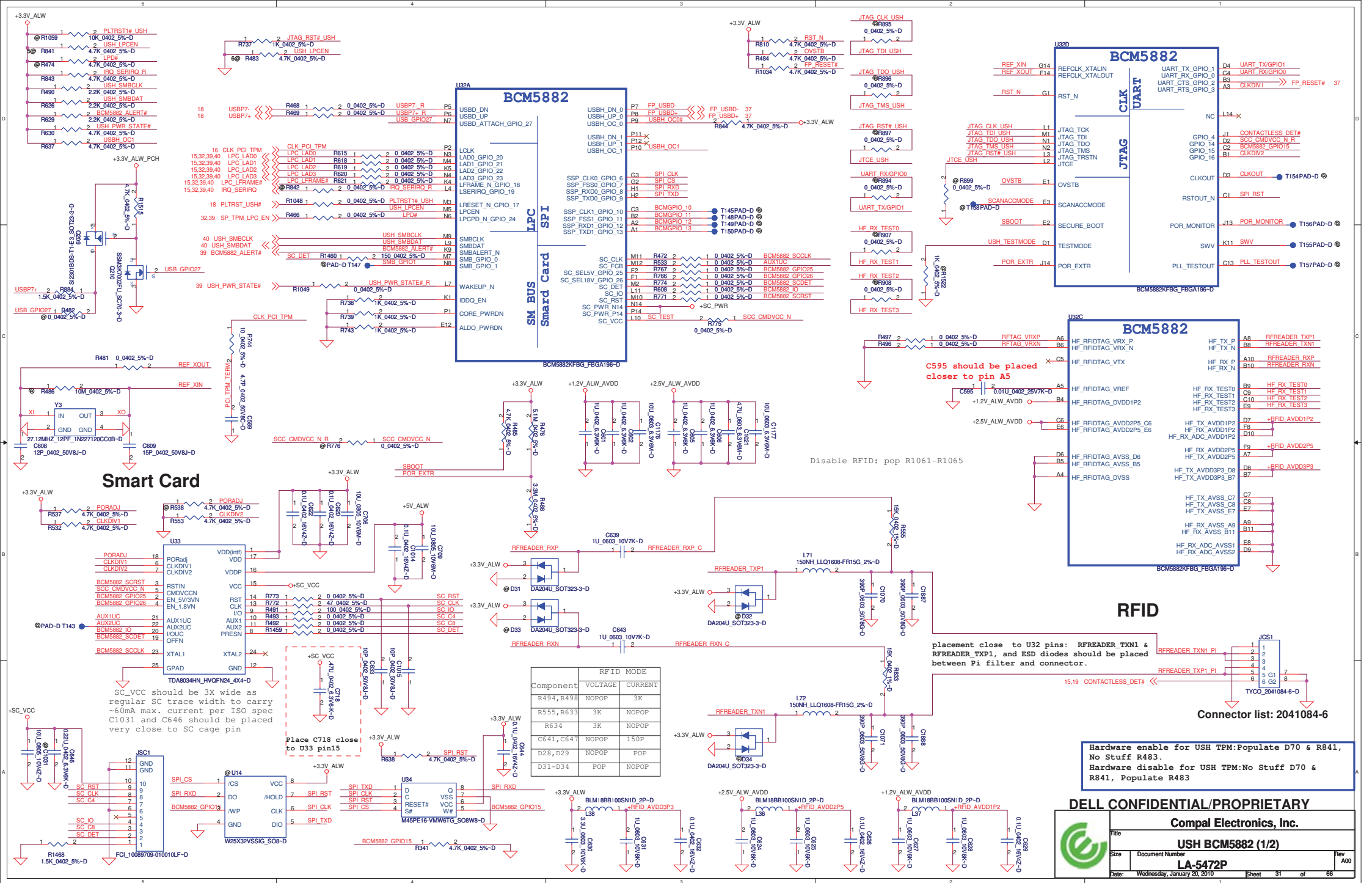
+1.05V_M for VC10 not the correct or complete implementation to connect to +1.05V_SVR.



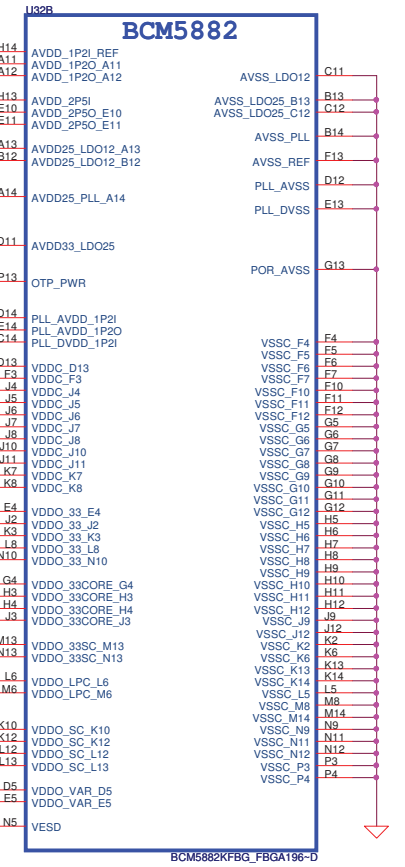
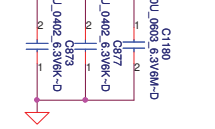
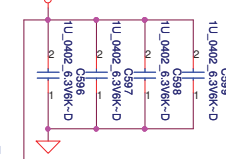
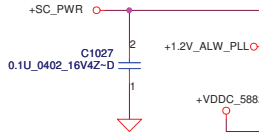
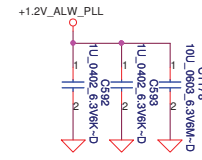
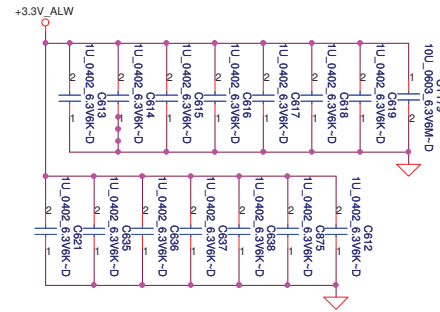
Need to verify A3 silicon drive power before removing C427

R1200 Resistor Value:
 3.01 kohm for Hanksville-M LOM
 2.37 kohm for Hanksville-D LOM



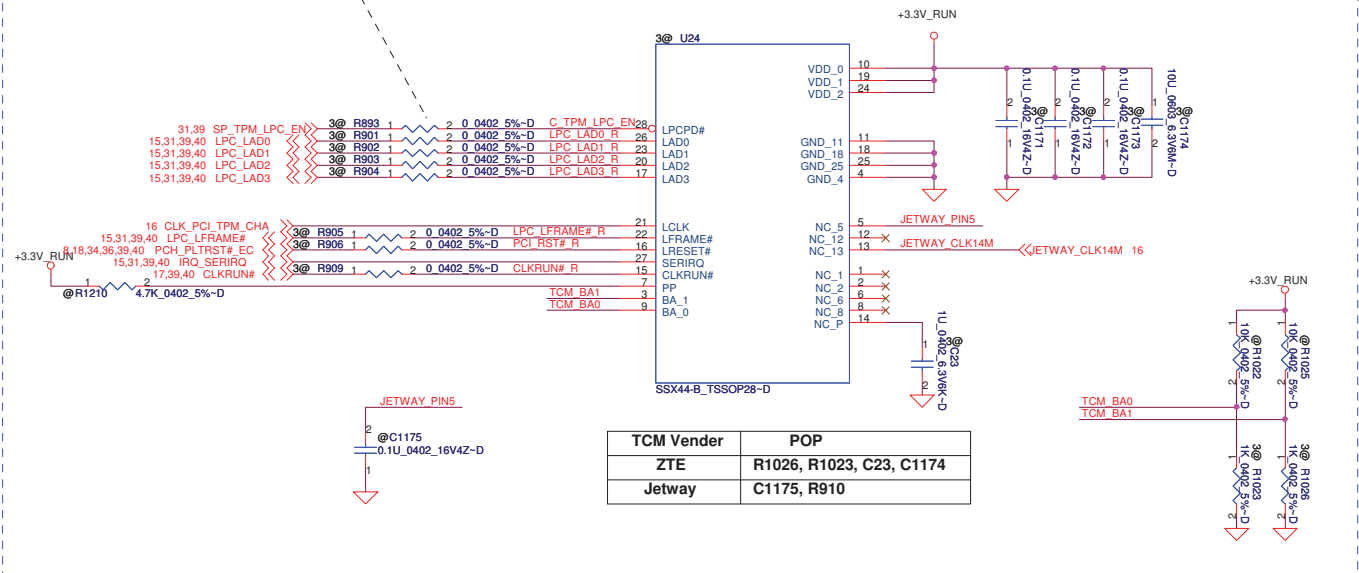


USH BCM5882 and China TPM Z8H172T Option				
PART/PIN	Ref Des	TCM Enable	TPM Enable	ALL TPM/TCM Disable
TCM circuit	All 3@	POP	@	@
STO 5028 ->SP_TPM_LPC_EN	PU R841	@	POP	@
	PD R483	POP	@	@
	PU R788	@	@	@
PCH GPIO39 ->TPM_ID1	PU R787	@	@	POP
	PD R339	POP	POP	@
PCH GPIO38 ->TPM_ID0	PU R273	POP	POP	@
	PD R922	@	@	POP



LOW: Power Down Mode
High: Working Mode

China TPM: ZTE & Jetway co-lay



TCM Vender	POP
ZTE	R1026, R1023, C23, C1174
Jetway	C1175, R910

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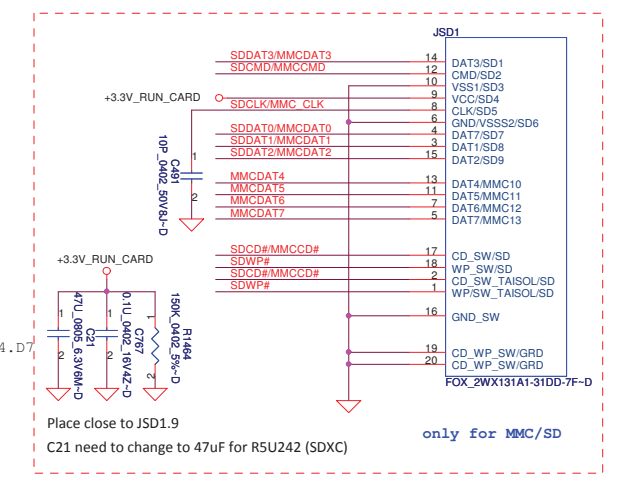
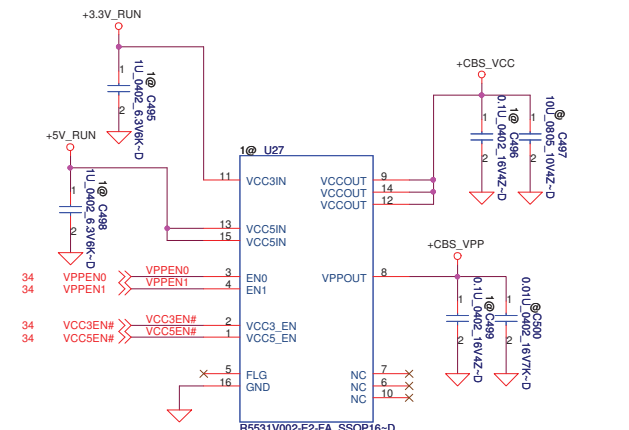
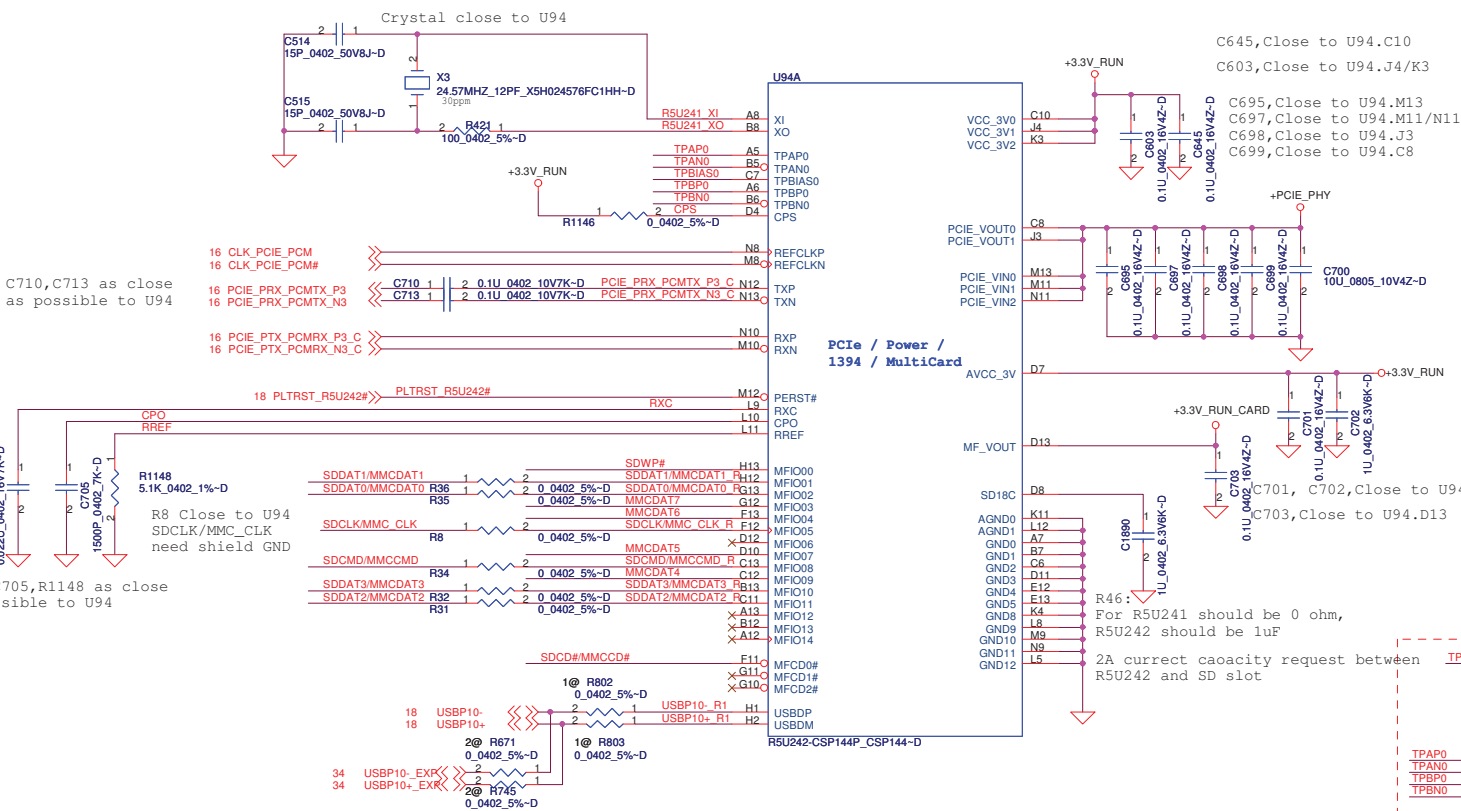
Compal Electronics, Inc.

USH BCM5882 (2/2)

LA-5472P



Title		Rev
USH BCM5882 (2/2)		A00
Size	Document Number	Rev
	LA-5472P	A00
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MFIO Pin Assignment Table

MFIO	SD8	XD	MS8
00	WP	D7	BS
01	D1	D6	-
02	D0	D5	D1
03	D7	D4	-
04	D6	D3	D5
05	CLK	D2	D0
06	-	D1	-
07	D5	D0	D4
08	CMD	WP#	D2
09	D4	WE#	D6
10	D3	ALE	D3
11	D2	CLE	-
12	-	CE#	-
13	-	RE#	D7
14	-	R/B#	CLK

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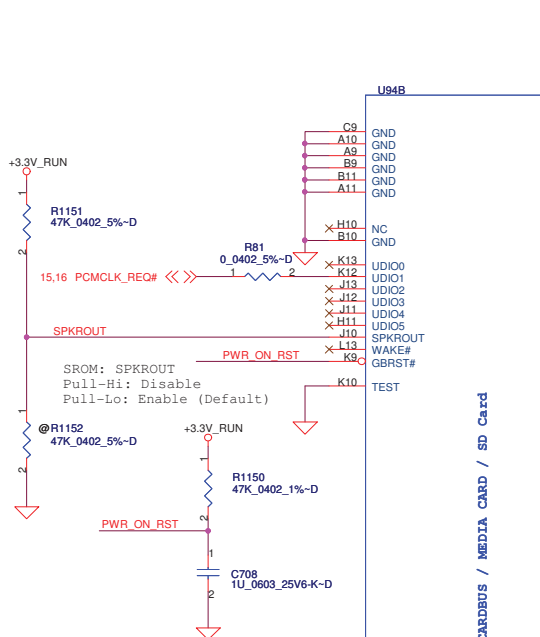
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Title: **RSU242 (1/2)**

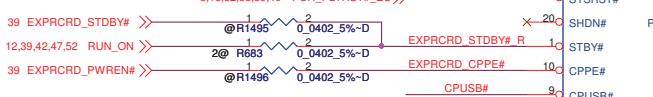
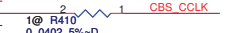
Size: _____ Document Number: _____ Rev: **A00**

Date: **Wednesday, January 20, 2010** Sheet **33** of **66**



CADR25	K2	CBS CAD17
CADR24	H4	CBS CFRAME#
CADR23	J1	CBS CTRDY#
CADR22	G3	CBS CDEVSEL#
CADR21	F3	CBS CSTOP#
CADR20	G2	CBS CBLOCK#
CADR19	F2	CBS DATA18
CADR18	E2	CBS CAD16
CADR17	H3	CBS CCB1E1#
CADR16	J2	CBS CIRDY#
CADR15	G1	CBS CPERR#
CADR14	F1	CBS CPAR#
CADR13	K1	CBS CCB2E2#
CADR12	C2	CBS CAD2
CADR11	C3	CBS CAD9
CADR10	D2	CBS CAD14
CADR9	E3	CBS CCB1E1#
CADR8	F3	CBS CAD18
CADR7	M1	CBS CAD20
CADR6	M2	CBS CAD21
CADR5	M3	CBS CAD22
CADR4	L3	CBS CAD23
CADR3	N3	CBS CAD24
CADR2	N4	CBS CAD25
CADR1	M4	CBS CAD26
CADR0	M4	CBS CAD26
CDATA15	B1	CBS CAD8
CDATA14	B2	CBS DATA14
CDATA13	B3	CBS CAD5
CDATA12	B4	CBS CAD2
CDATA11	M7	CBS CAD31
CDATA10	M6	CBS CAD30
CDATA9	M5	CBS CAD28
CDATA8	A1	CBS CAD7
CDATA7	A2	CBS CAD5
CDATA6	A3	CBS CAD3
CDATA4	A4	CBS CAD0
CDATA3	N7	CBS DATA2
CDATA2	N6	CBS CAD29
CDATA1	N5	CBS CAD27
CDATA0	N5	CBS CAD27

R410 Close to U94, CBS_CCLK need shield GND.



Express Card

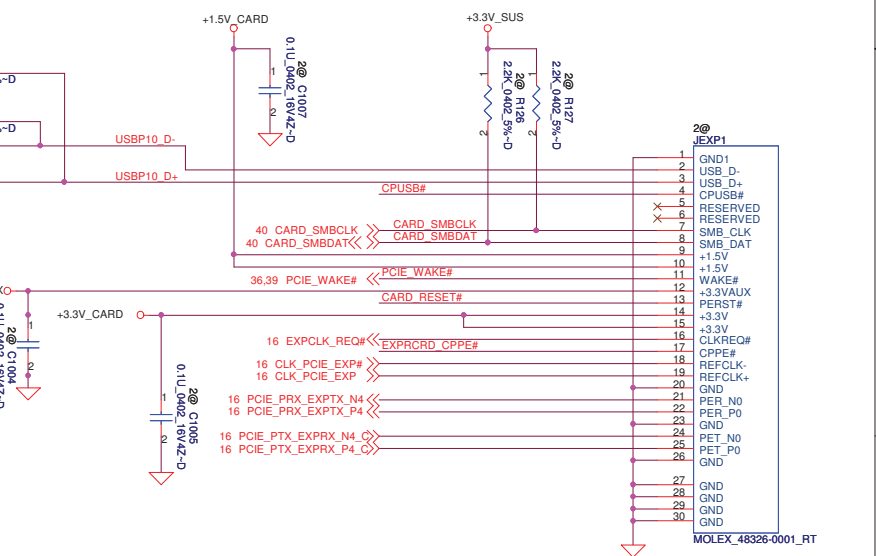
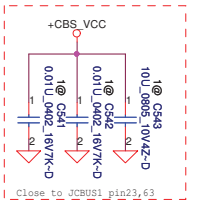
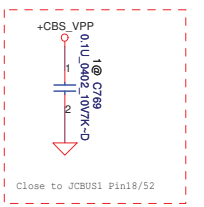
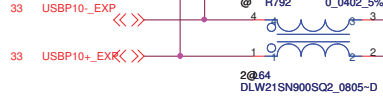
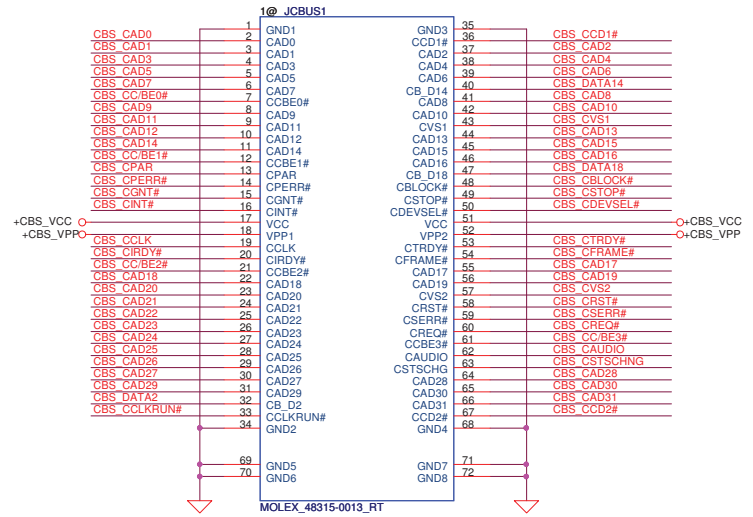
+1.5V_CARD: Max. 650mA, Average 500mA
+3.3V_CARD: Max. 1300mA, Average 1000mA

Power-On-Reset: GBRST#
 (Global Reset)
 Note: De-asserted BEFORE
 PERST# de-assertion

- 33 VPPEN1 <<< VPPEN1 D9 VPPEN1
- 33 VPPEN0 <<< VPPEN0 E10 VPPEN0
- 33 VCC3EN# <<< VCC3EN# F10 VCC3EN#
- 33 VCC5EN# <<< VCC5EN# E11 VCC5EN#

CE#	C1	CBS CAD11
WE#	F4	CBS CGNT#
D3#	D3	CBS CAD10
CE2#	D5	CBS CCB2E0#
CE1#	L4	CBS CCB3E3#
RES#	N1	CBS CRST#
RESET	N2	CBS CSERR#
WAIT#	L7	CBS COLKRUN#
WPN#/IOIS16#	G4	CBS CINT#
RDY#REQ#	L6	CBS AUDIO
BVD1	K7	CBS CSTSCHNG
BVD2	E4	CBS CVS1
VS2#	K8	CBS CCD2#
VS1#	D6	CBS CCD1#
CD1#	K6	CBS CAD18
INPACK#	D1	CBS CAD13
IORD#	E1	CBS CAD15
IOWR#	E1	CBS CAD15

RSU242-CSP144P_CSP144-D



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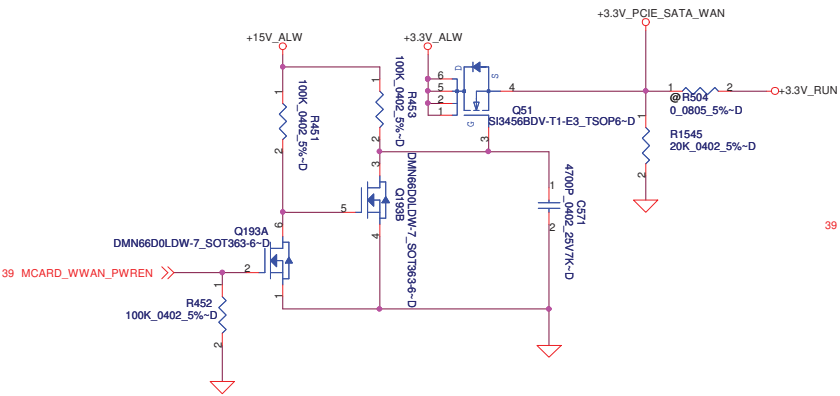
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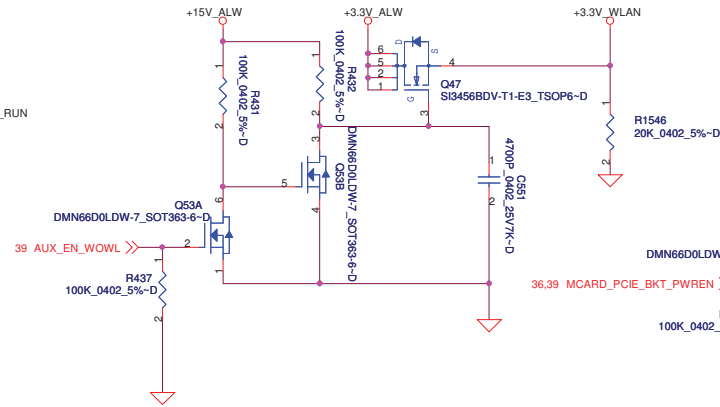
Size: **LA-5472P**

Date: **Wednesday, January 20, 2010** Sheet **34** of **66**

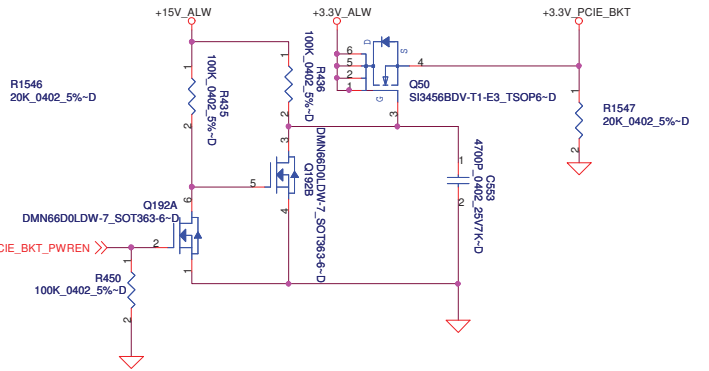
Power Control for Mini card1



Power Control for Mini card2



Power Control for Mini card3



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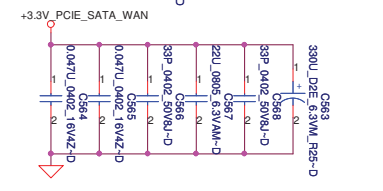
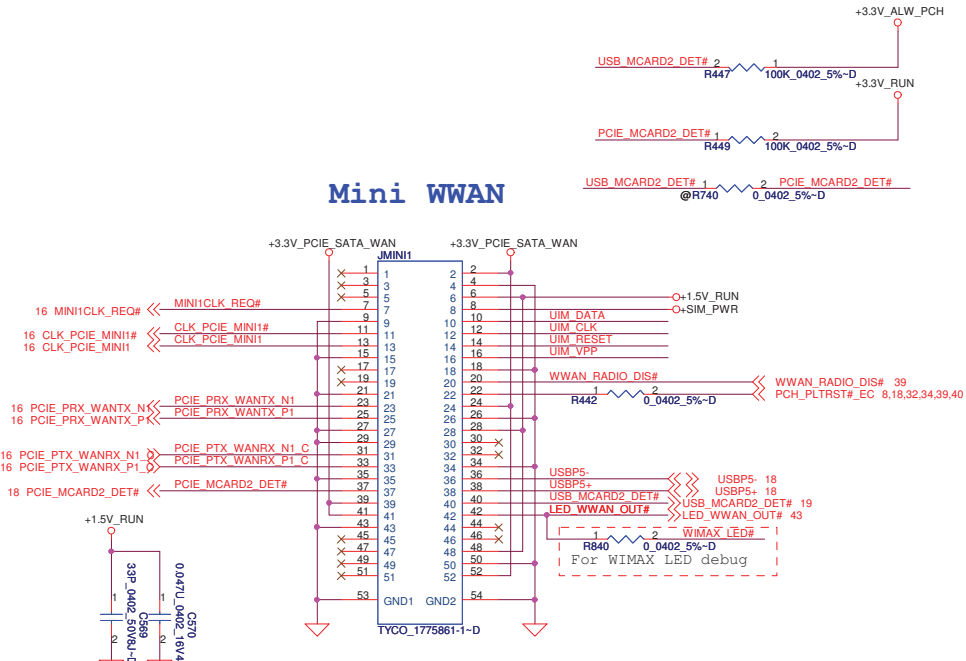


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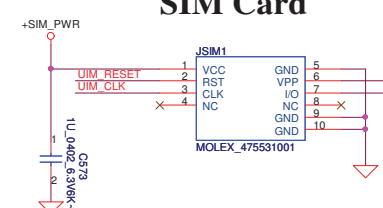
Compal Electronics, Inc.

Title PCIE PWR			Rev A00
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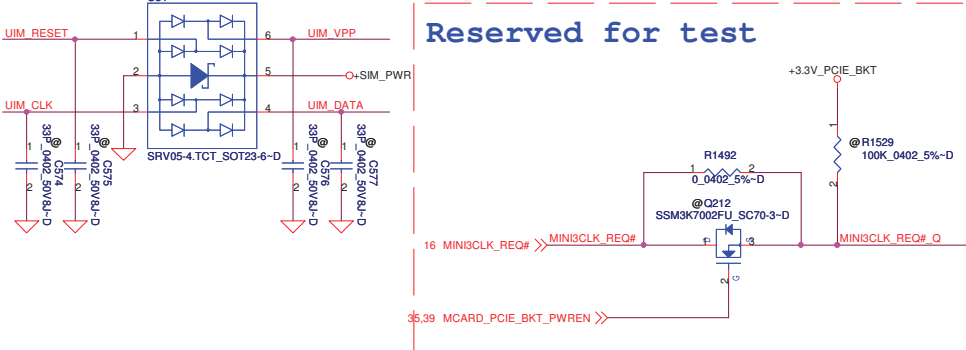
Mini WWAN



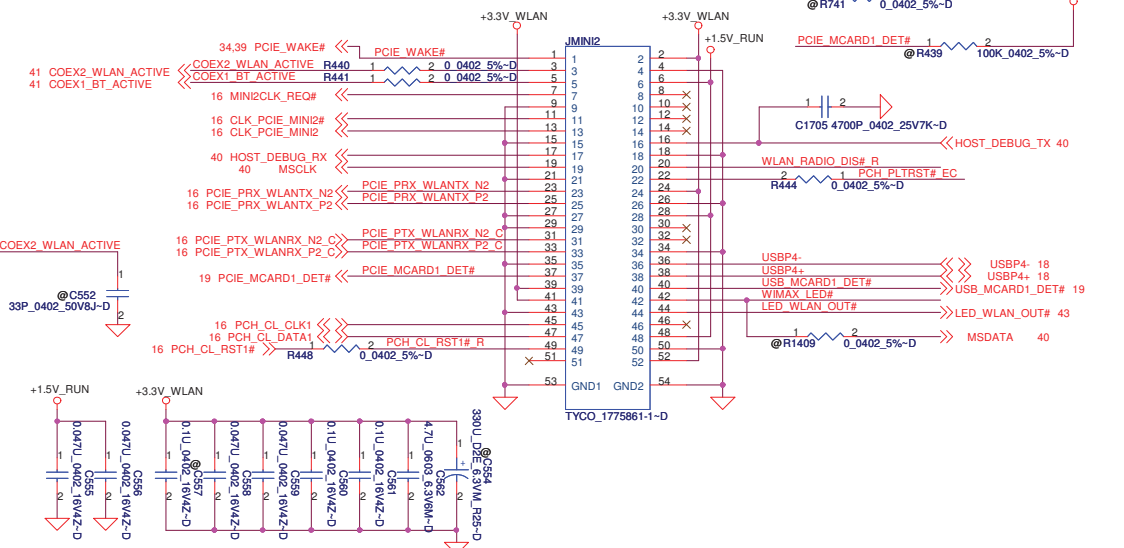
PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+9%	1000	750	
+3.3Vaux	+9%	330	250	250 (Wake enable) 5 (Not wake enable)
+1.5V	+5%	500	375	NA



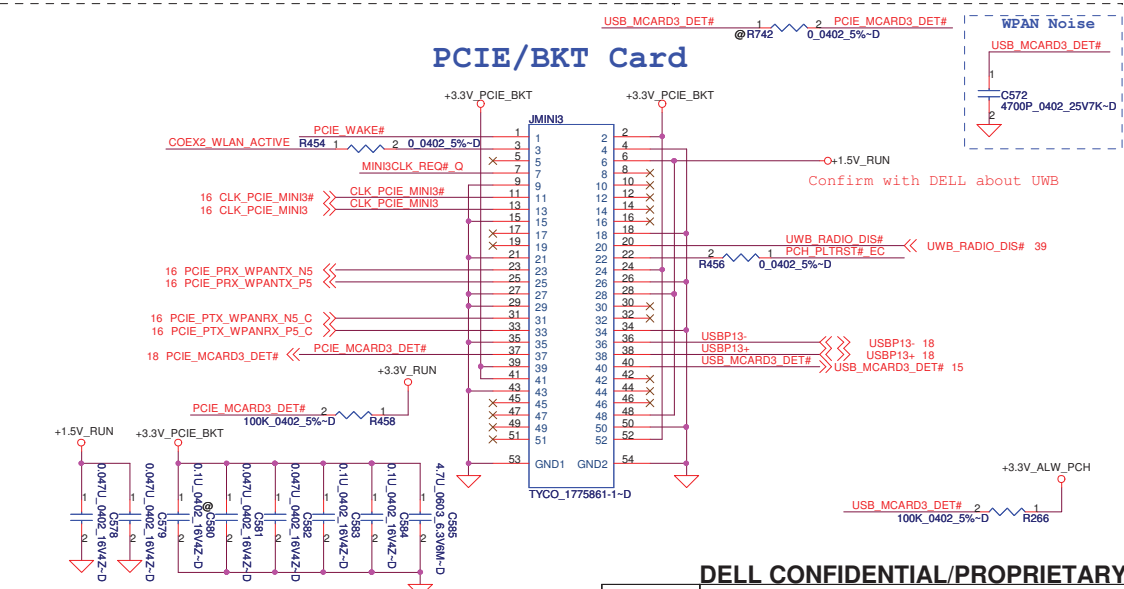
Reserved for test

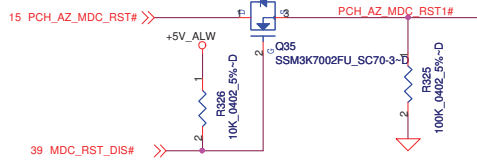
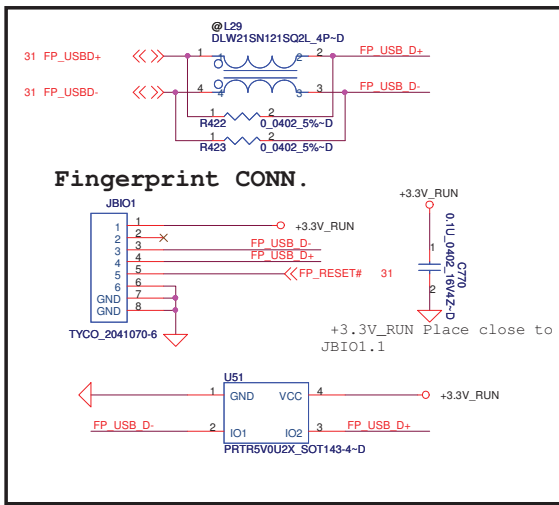


Mini WLAN

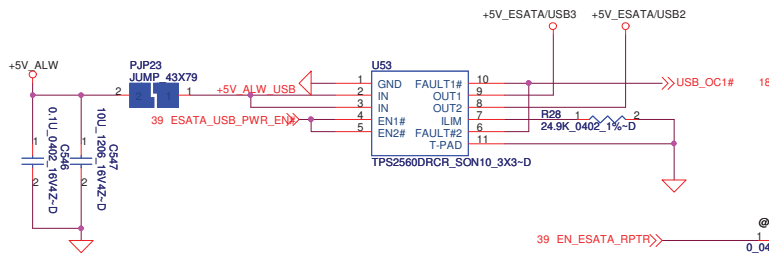
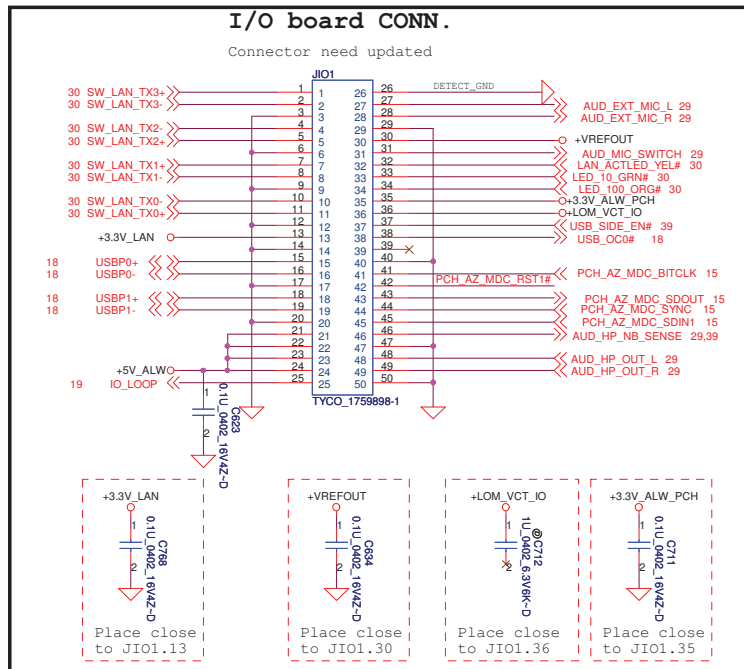


PCIE/BKT Card

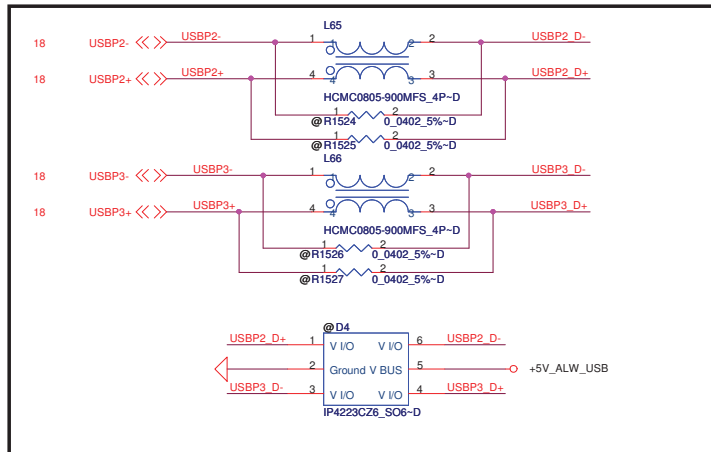
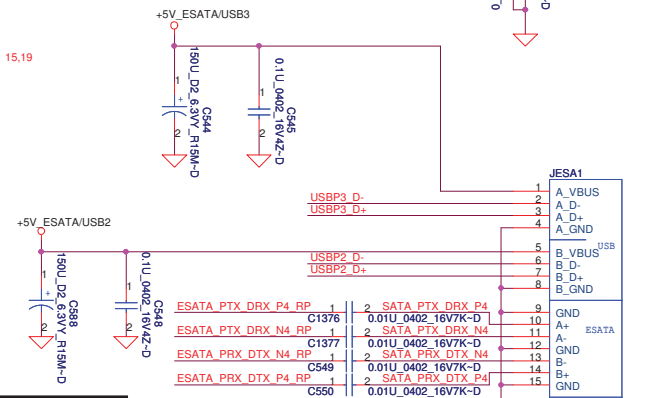
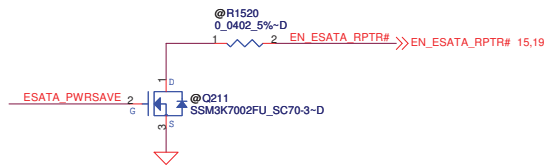
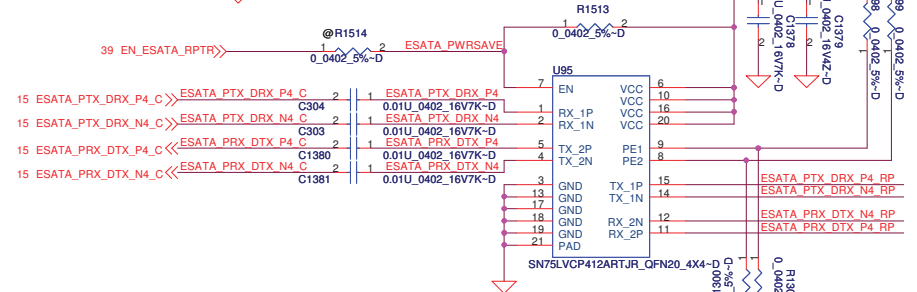




double check pin define with IO board.



ESATA Repeater



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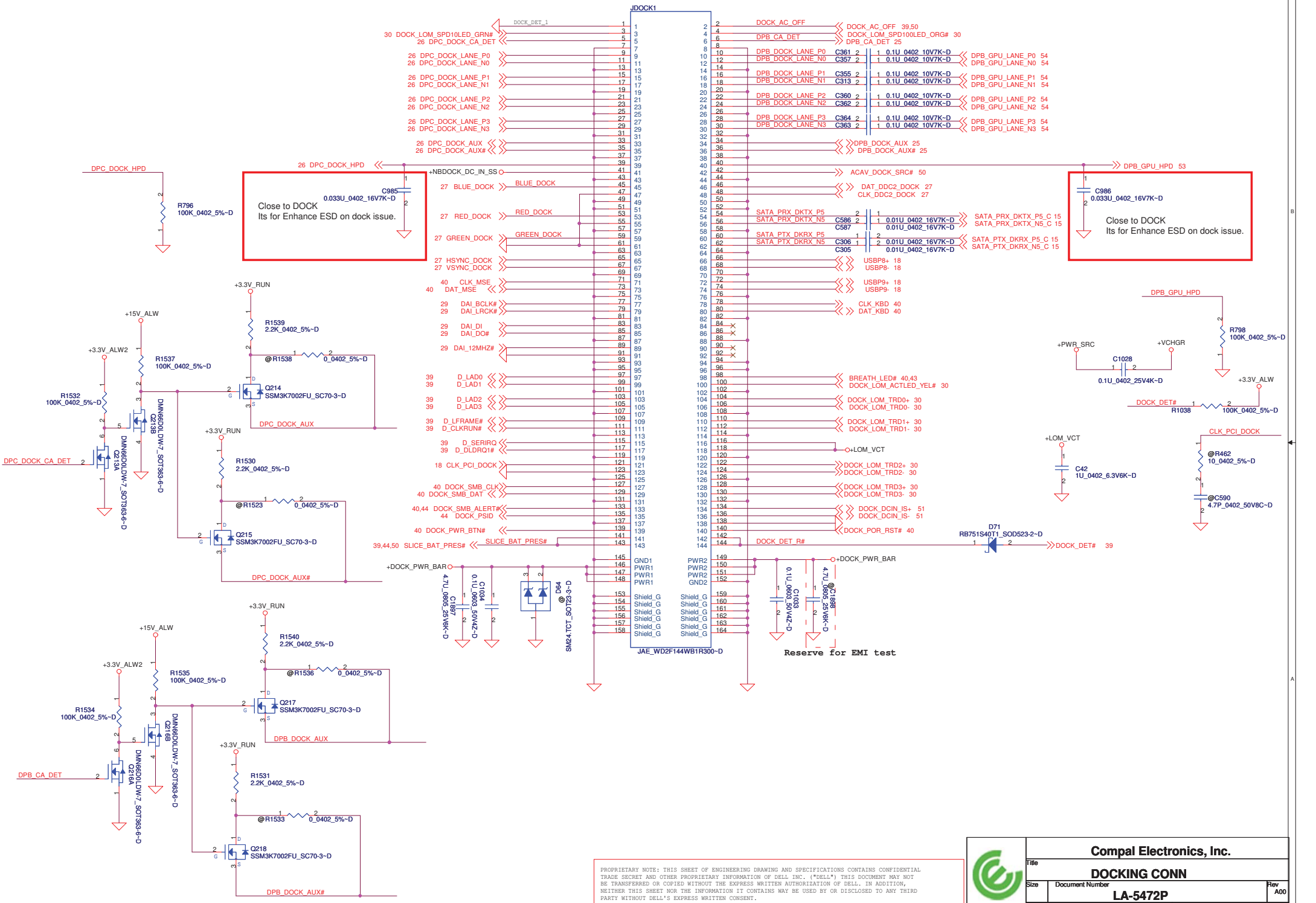
USB 2.0 PORT

LA-5472P

Document Number

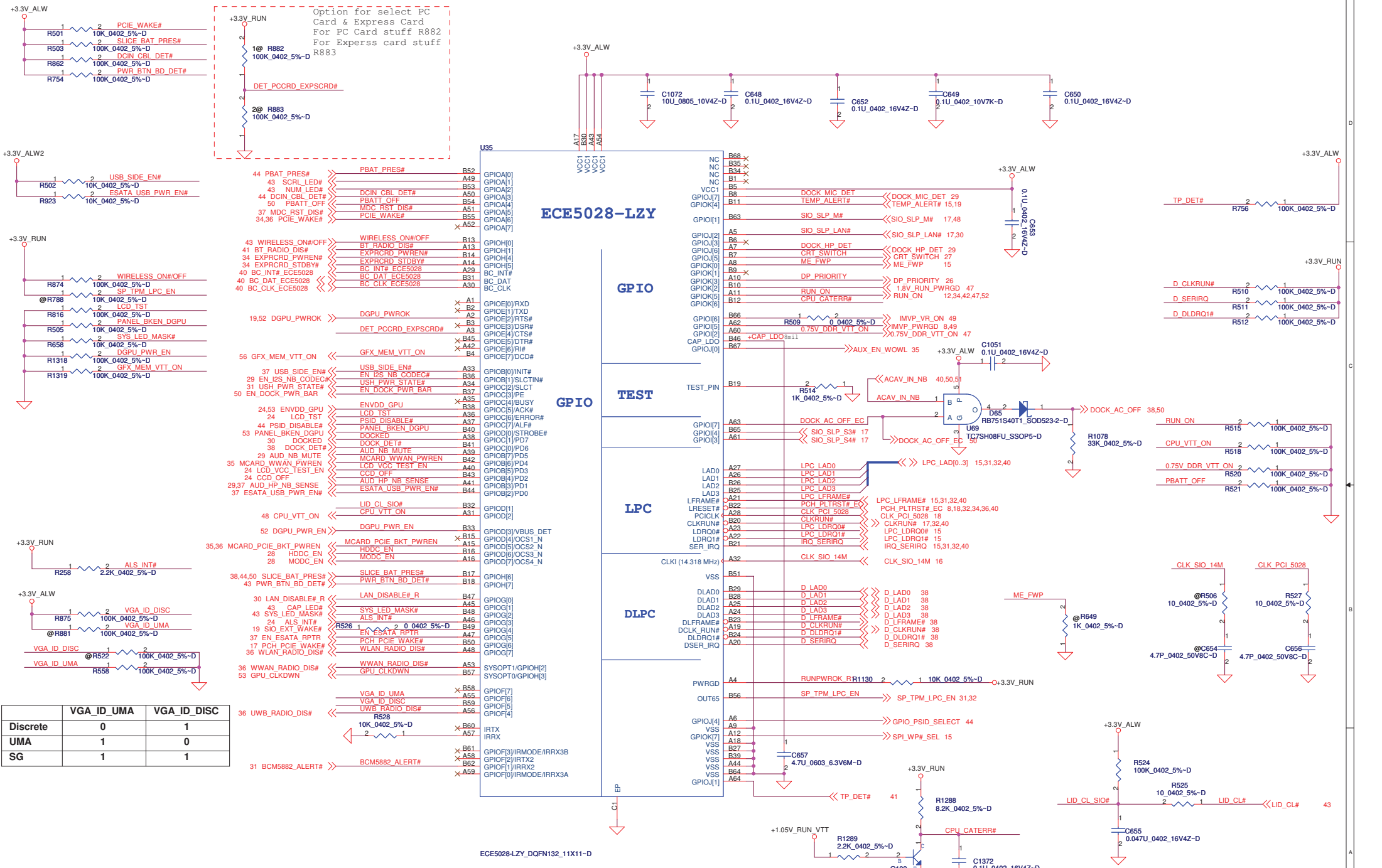
Wednesday, January 20, 2010

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DOCKING CONN			
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	VGA_ID_UMA	VGA_ID_DISC
Discrete	0	1
UMA	1	0
SG	1	1

ECE5028-LZY_DQFN132_11X11-D

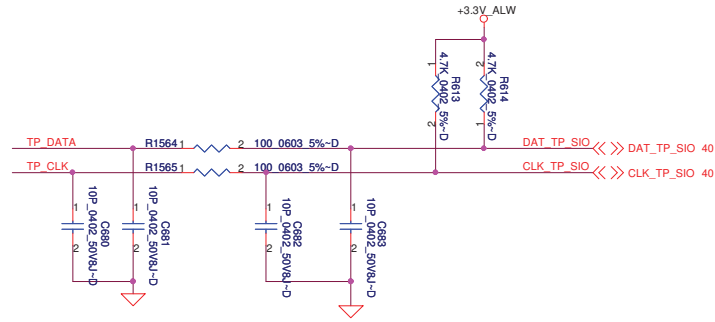
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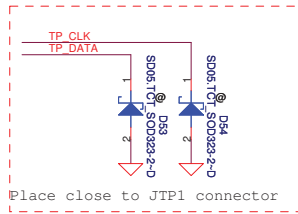
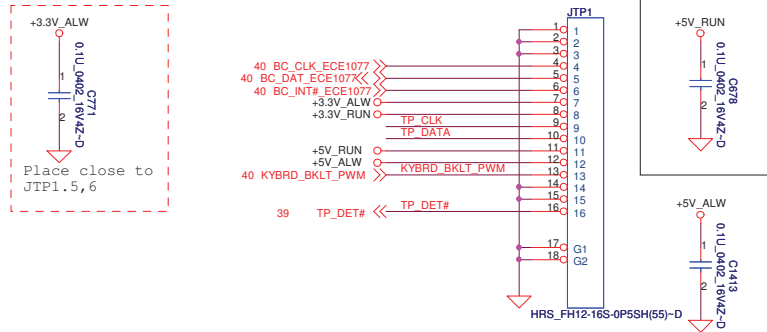


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<p>Date:</p> <p align="center">Wednesday, January 20, 2010</p>	<p>Sheet</p> <p align="center">39</p>	<p>of</p> <p align="right">66</p>	

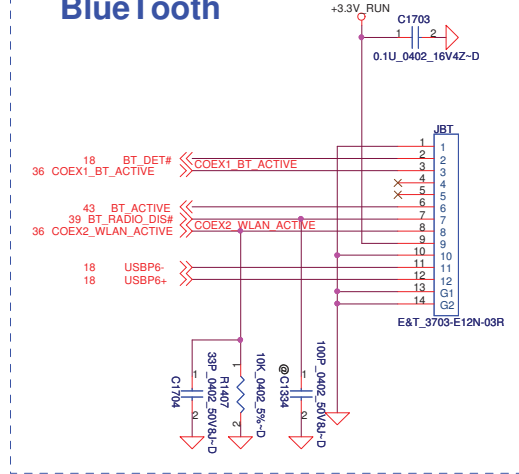
Touch Pad



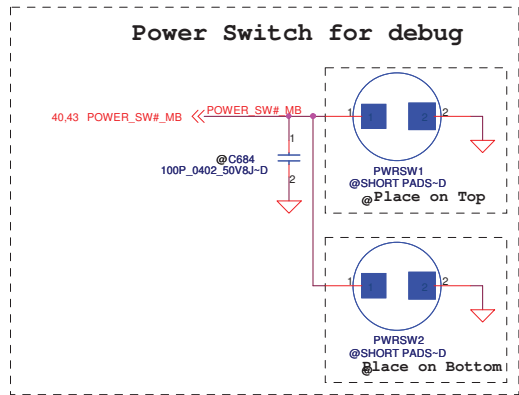
Touch Pad Conn. Pitch=0.5



BlueTooth



Power Switch for debug



Part Number	Description
DC28A000800	FAN SET DAQ20 DC5V AB7405HB-HB3 ADDA
PK230003Q0L	SPK PACK 2JX 2.0W 4 OHM FG
SP070007V0L	SOCKET TYCO I770551-1 10P H5.9 SWART
DC000001Q0L	PCMCIA TYCO 1759096-1
DC02000CS0L	H-CONN SET ZGX MB-MDC
DC02000840L	H-CONN SET ZJX MB-B/T-TP-FP
DC020003Y0L	H-CONN SET ZJX MB-LCD 14 WXGA+(-1ch)
DC02000870L	H-CONN SET ZJX MB-LCD 14 WXGA+(-2ch)
GC20323MX00	BATT CR2032 3V 220MAH MAXELL

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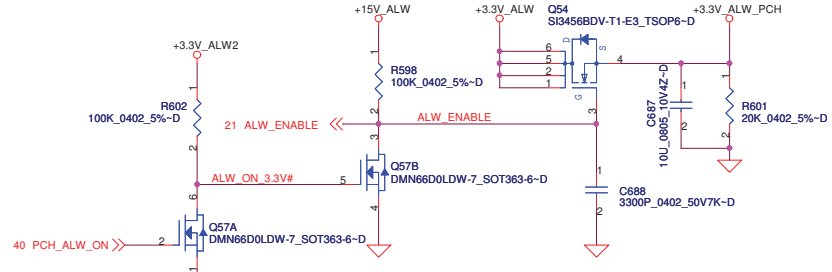
Compal Electronics, Inc.

Title			
Touch Pad/Int KB/LID			
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Date:	Wednesday, January 20, 2010	Sheet	41 of 66

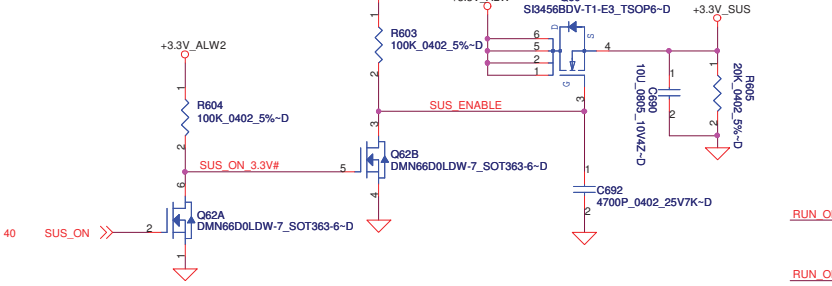
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DC/DC Interface

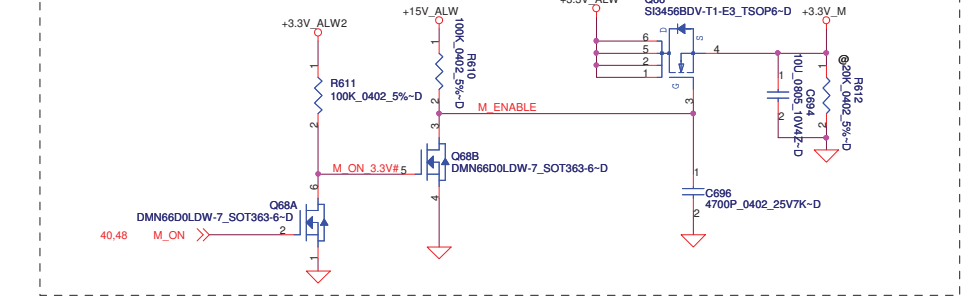
+3.3V_ALW_PCH Source



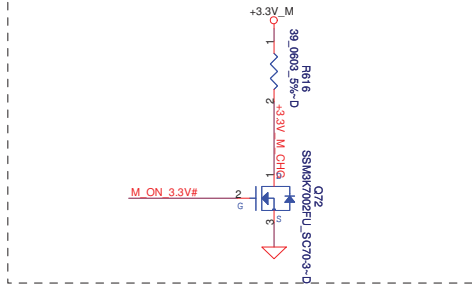
+3.3V_SUS Source



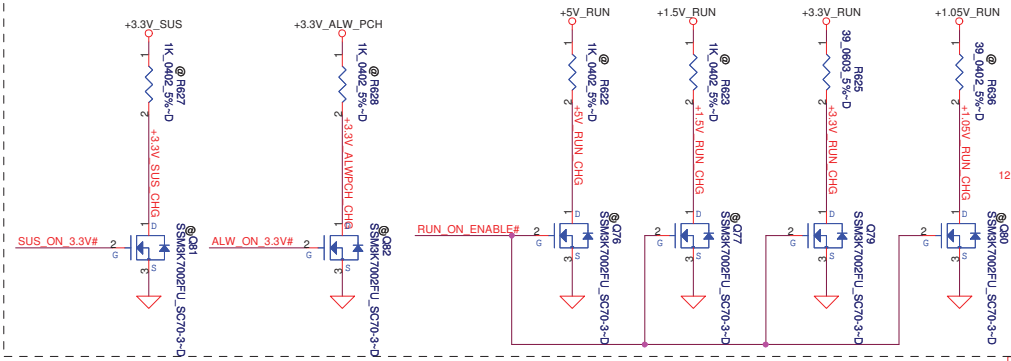
+3.3VM Source



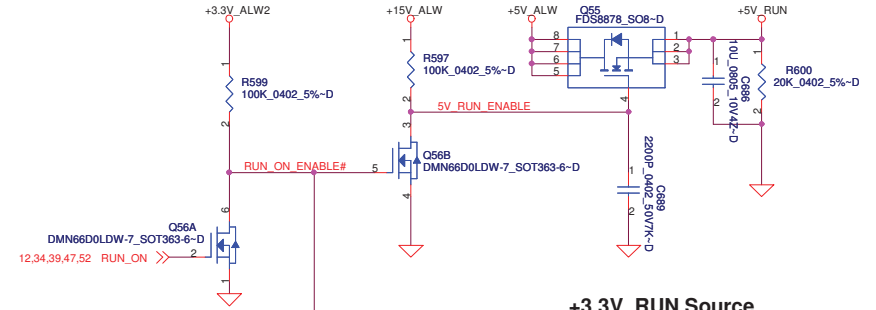
Discharg Circuit



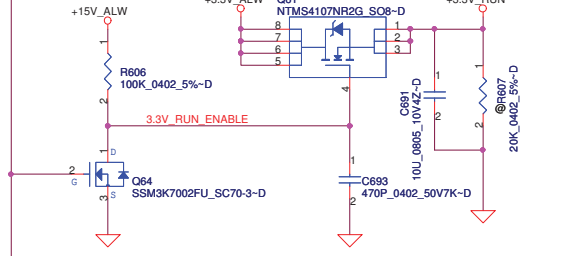
Discharg Circuit



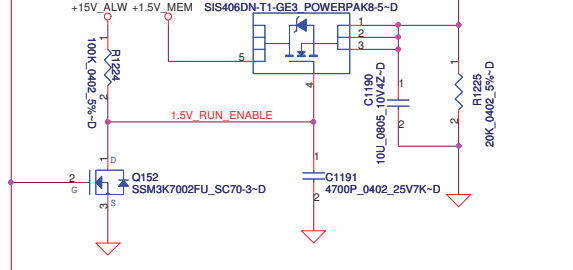
+5VRUN Source



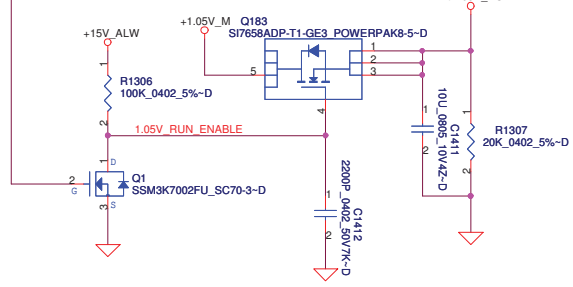
+3.3V_RUN Source



+1.5V_RUN Source



+1.05V_RUN Source



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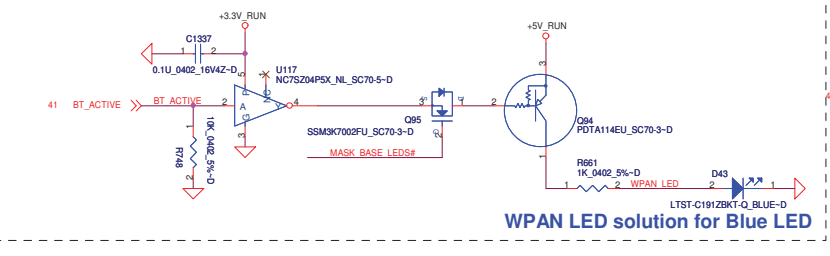
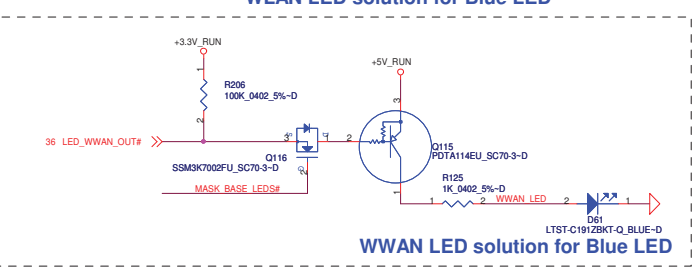
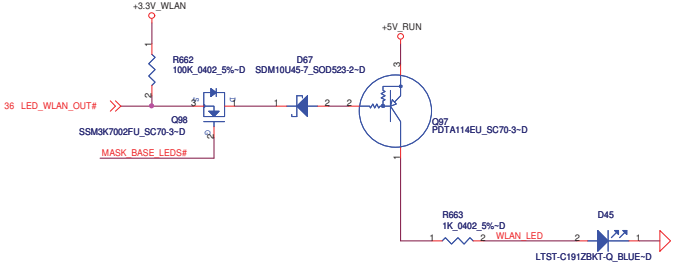
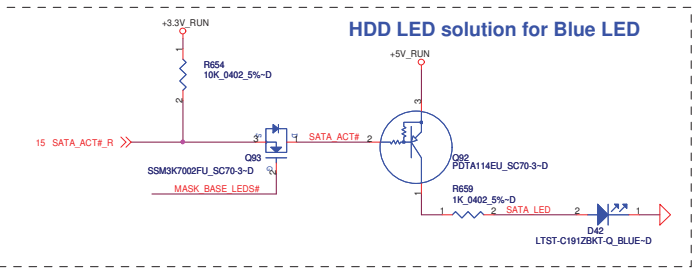
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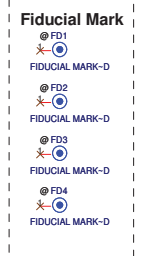
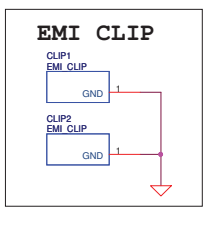
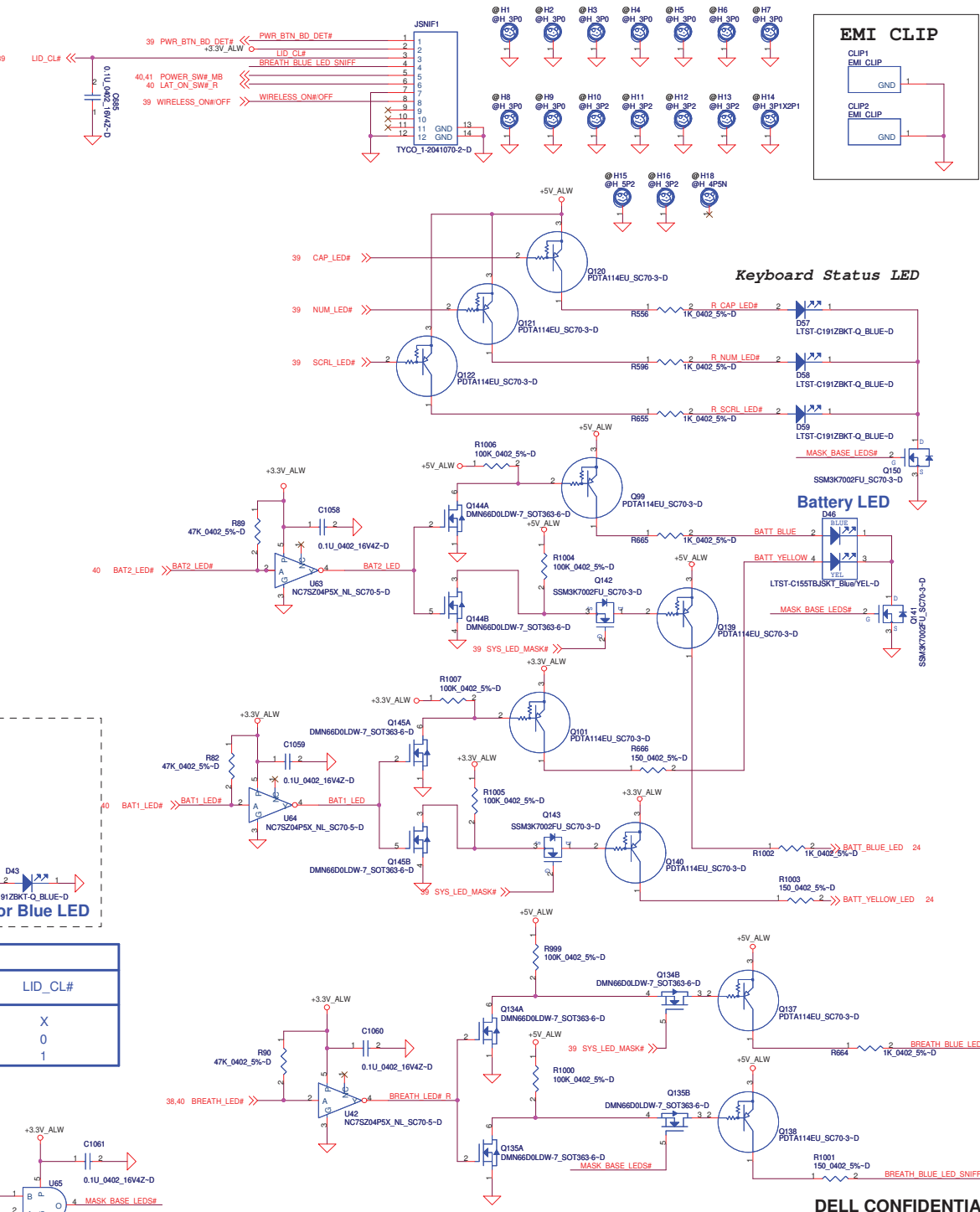
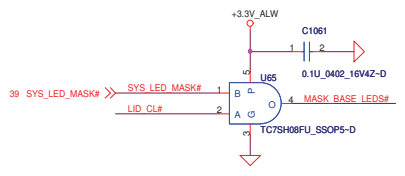
POWER CONTROL

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	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



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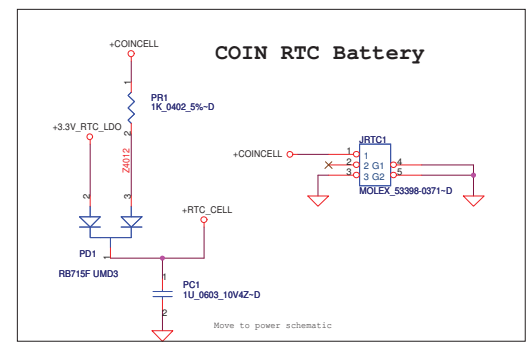
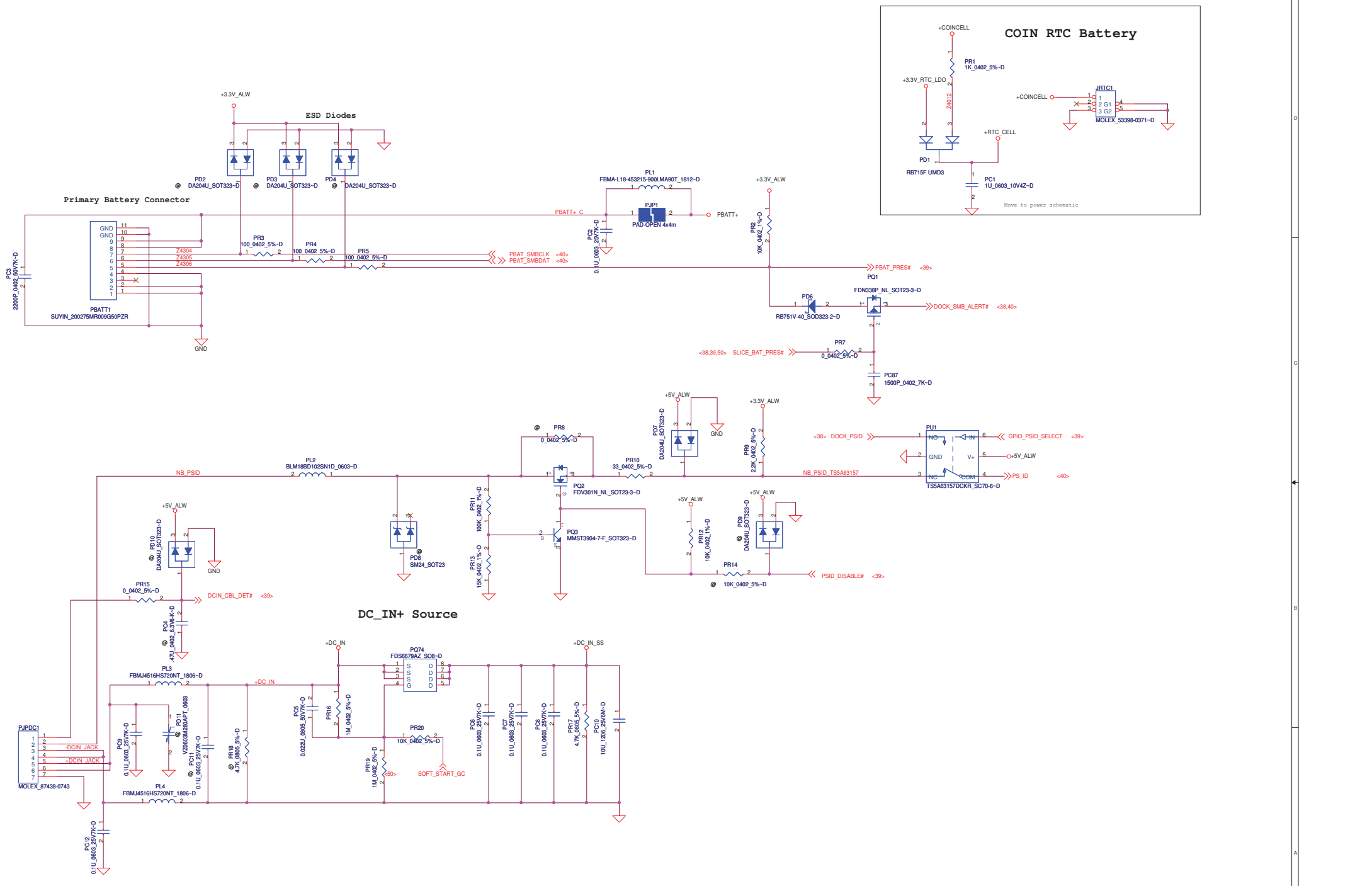
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PAD and Standoff

LA-5472P

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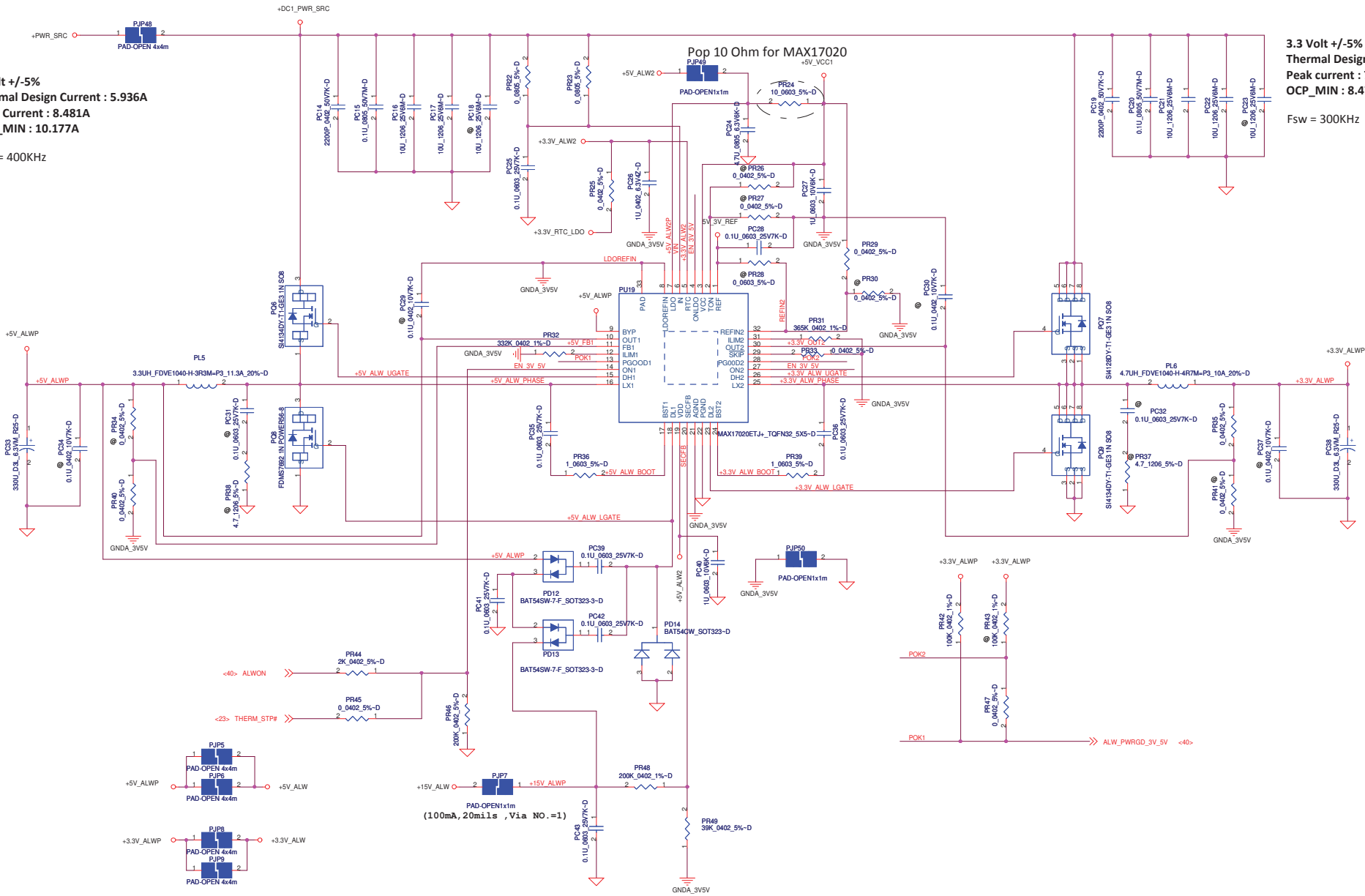
DELL CONFIDENTIAL/PROPRIETARY			
Compal Electronics, Inc.			
File	+DCIN		
Size	Document Number	Rev A00	
	LA-5472P		
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+3.3V_ALWP / +5V_ALWP / +5V_ALW2 / +15V_ALWP / +3.3V_RTC_LDO

5 Volt +/-5%
 Thermal Design Current : 5.936A
 Peak Current : 8.481A
 OCP_MIN : 10.177A

Fsw = 400KHz

3.3 Volt +/-5%
 Thermal Design Current : 4.942A
 Peak current : 7.061A
 OCP_MIN : 8.473A
 Fsw = 300KHz



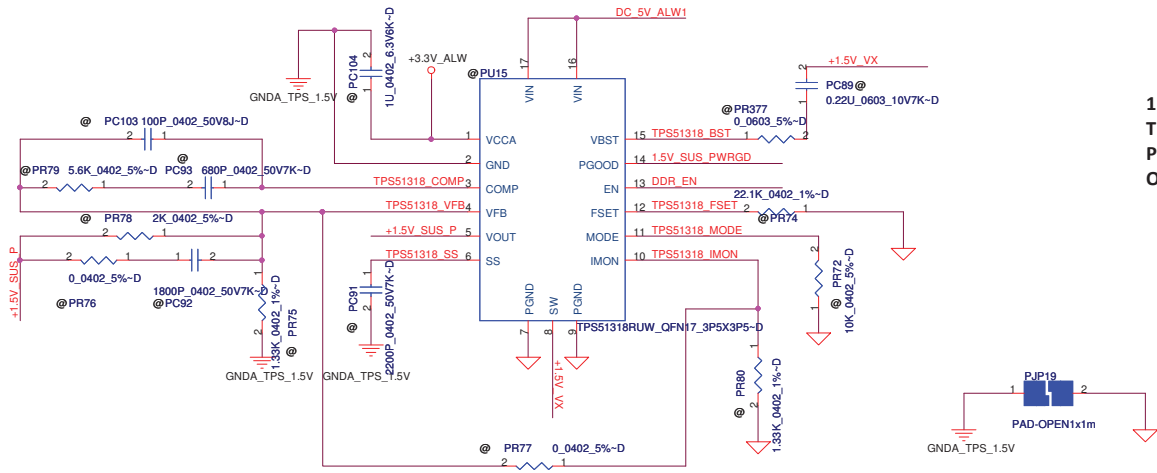
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Title		DC/DC +3V/ +5V	
Size	Document Number	LA-5472P	
Date:	Wednesday, January 20, 2010	Sheet	45 of 66

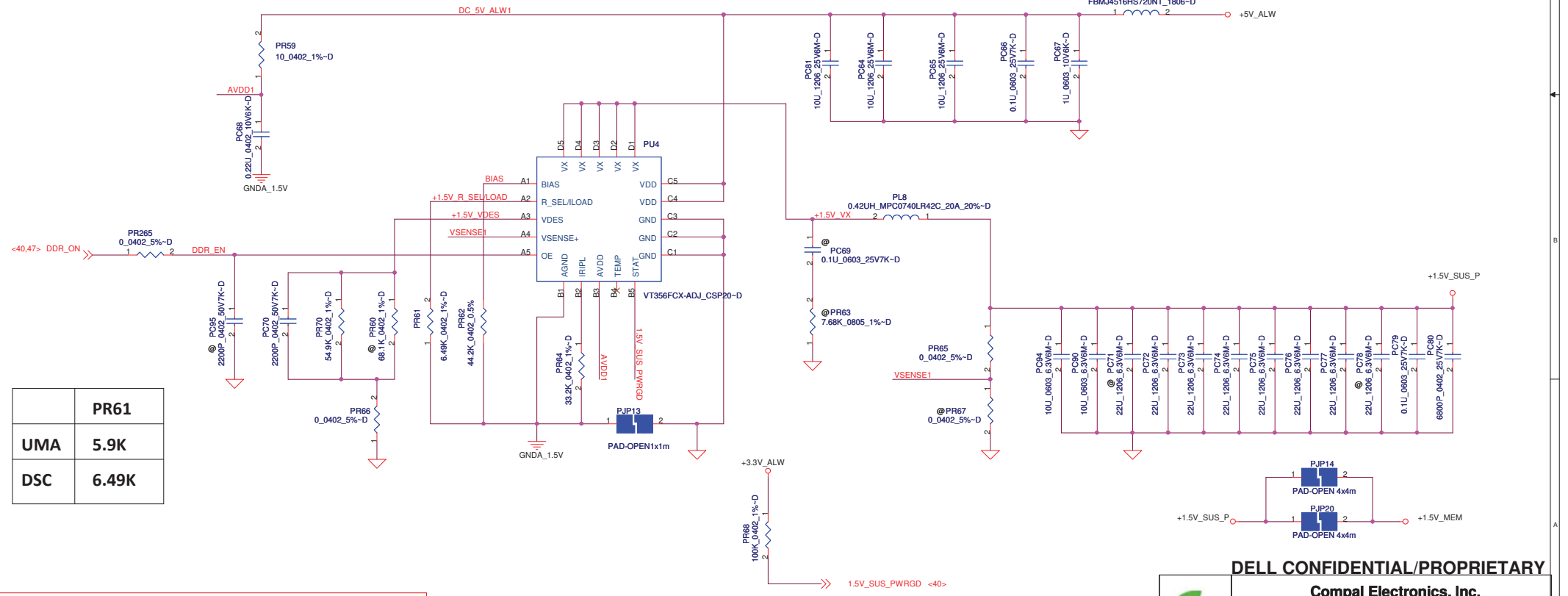
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+1.5V_SUS_P (TPS51318)



1.5 Volt +/-5%
Thermal Design Current : 7.876A
Peak current : 11.251A
OCP_MIN : 13.501A

+1.5V_SUS_P (VT356)



PR61	
UMA	5.9K
DSC	6.49K

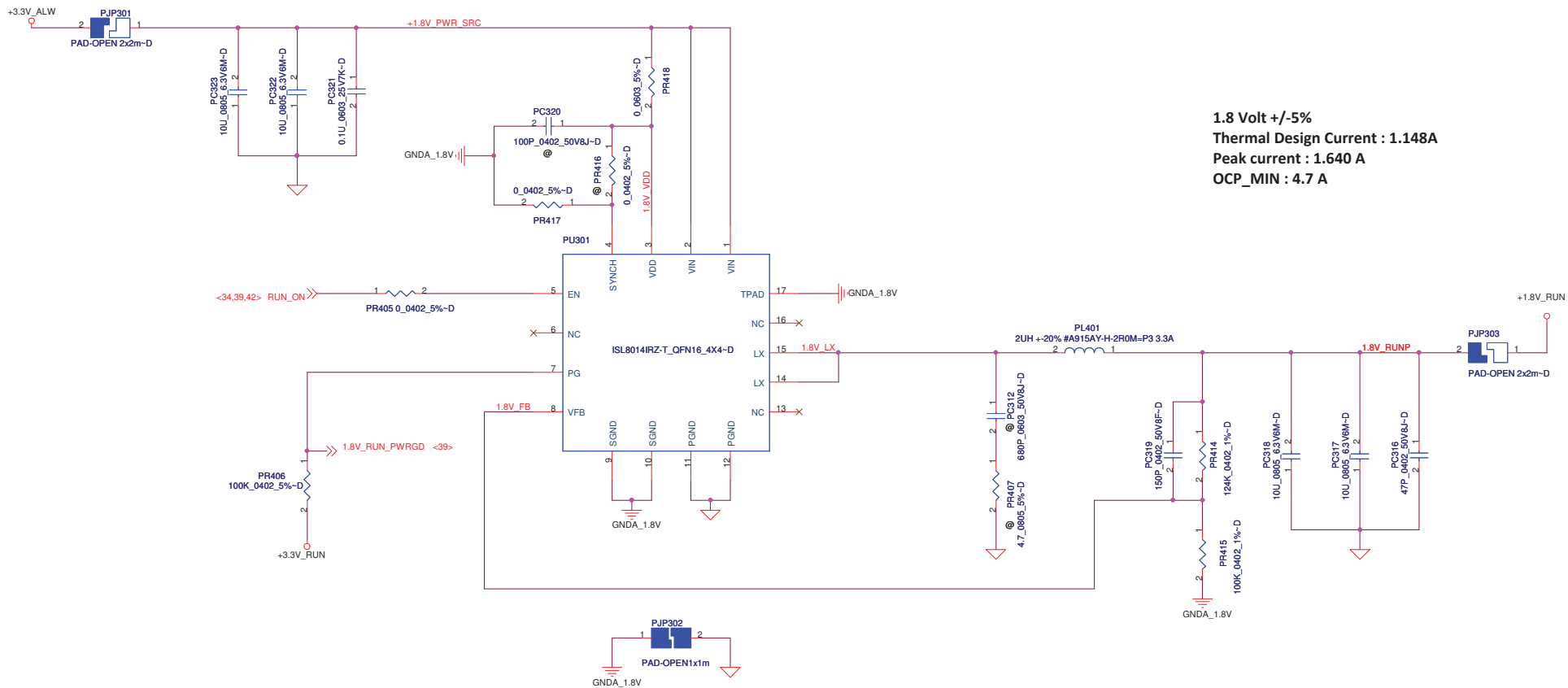
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Title: **+1.5V MEM**
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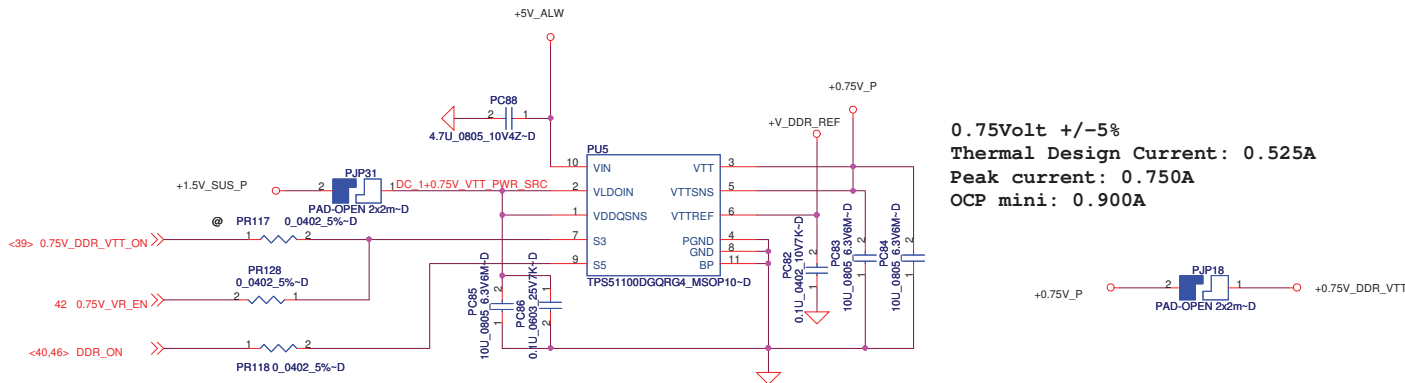
+1.8V_RUN



1.8 Volt +/-5%
 Thermal Design Current : 1.148A
 Peak current : 1.640 A
 OCP_MIN : 4.7 A

+0.75V_DDR_VTT

DDR3 Termination



0.75Volt +/-5%
 Thermal Design Current: 0.525A
 Peak current: 0.750A
 OCP mini: 0.900A

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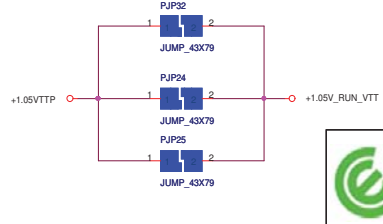
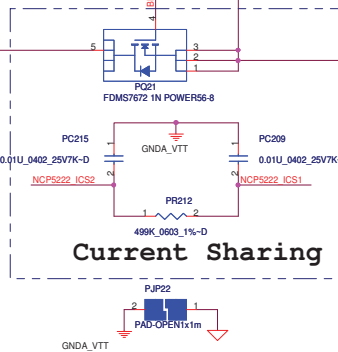
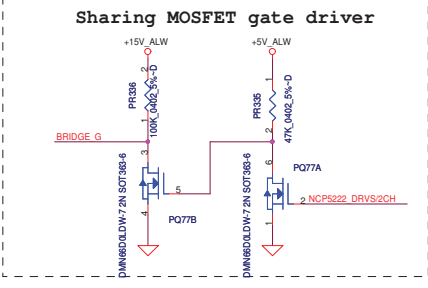
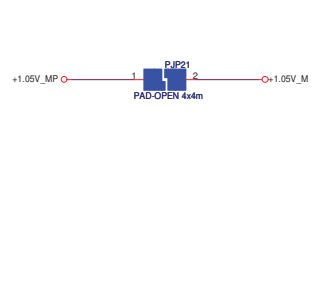
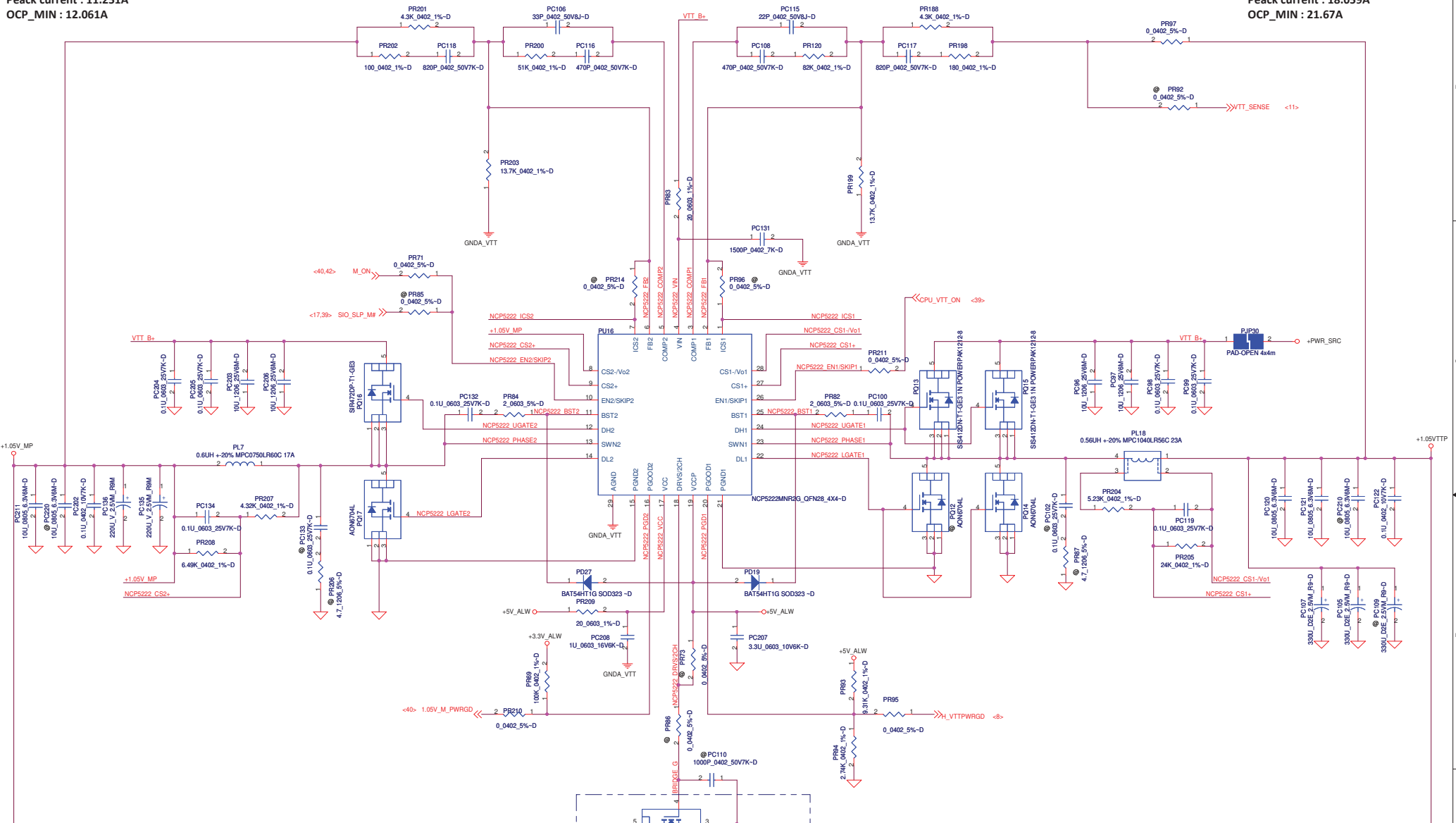
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+0.75V DDR VT/+1.8V RUN			
Size	Document Number	Rev	
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1.05 Volt +/-5%
 Thermal Design Current : 7.876A
 Peak current : 11.251A
 OCP_MIN : 12.061A

+1.05V_M/+1.05VTT_RUN

1.05Volt +/-5%
 Thermal Design Current : 18A
 Peak current : 18.059A
 OCP_MIN : 21.67A

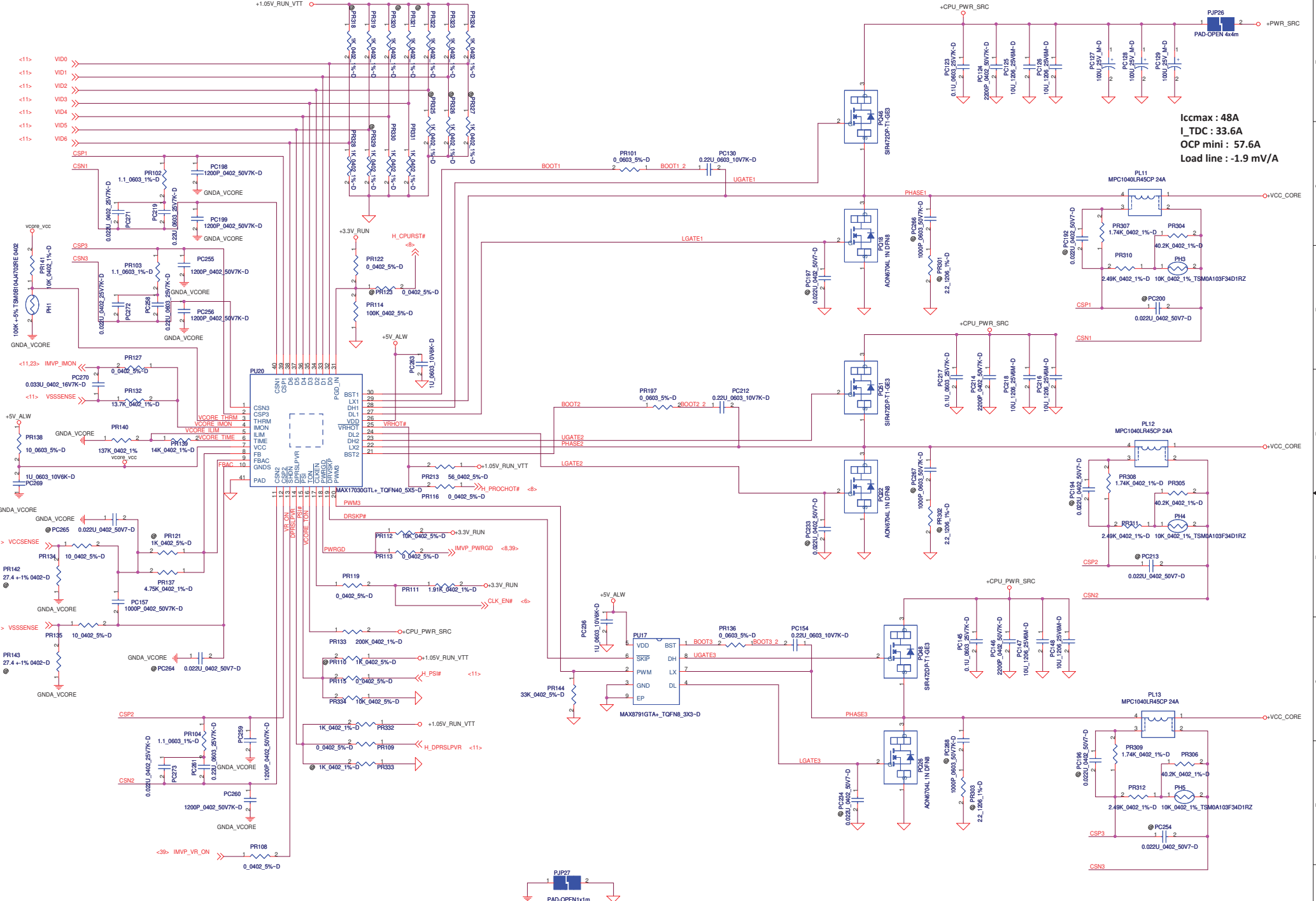


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+1.05V_M/+1.05VTT_RUN

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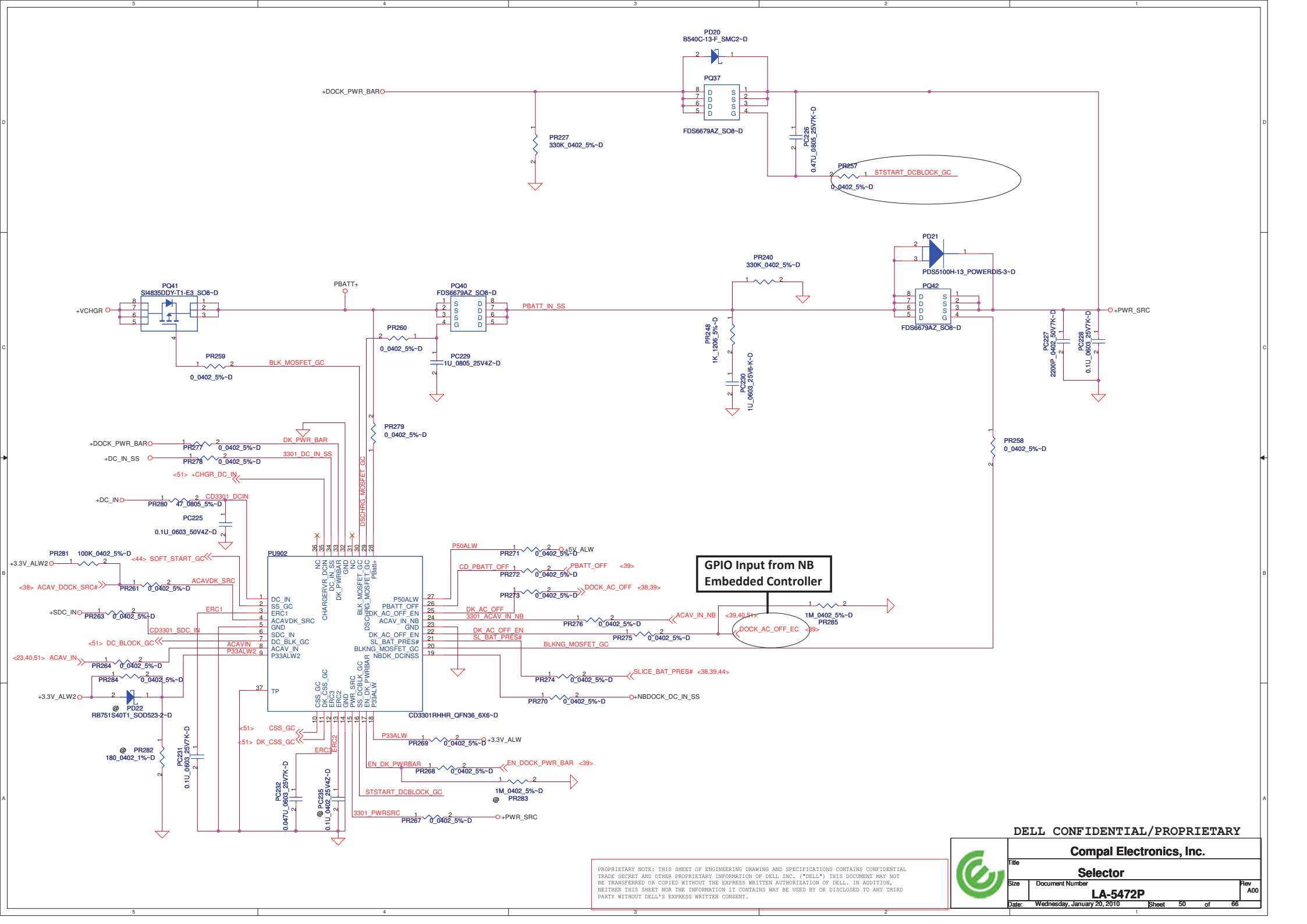


Iccmax : 48A
I_TDC : 33.6A
OCP mini : 57.6A
Load line : -1.9 mV/A

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		Compal Electronics, Inc.	
		+VCORE	
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Selector

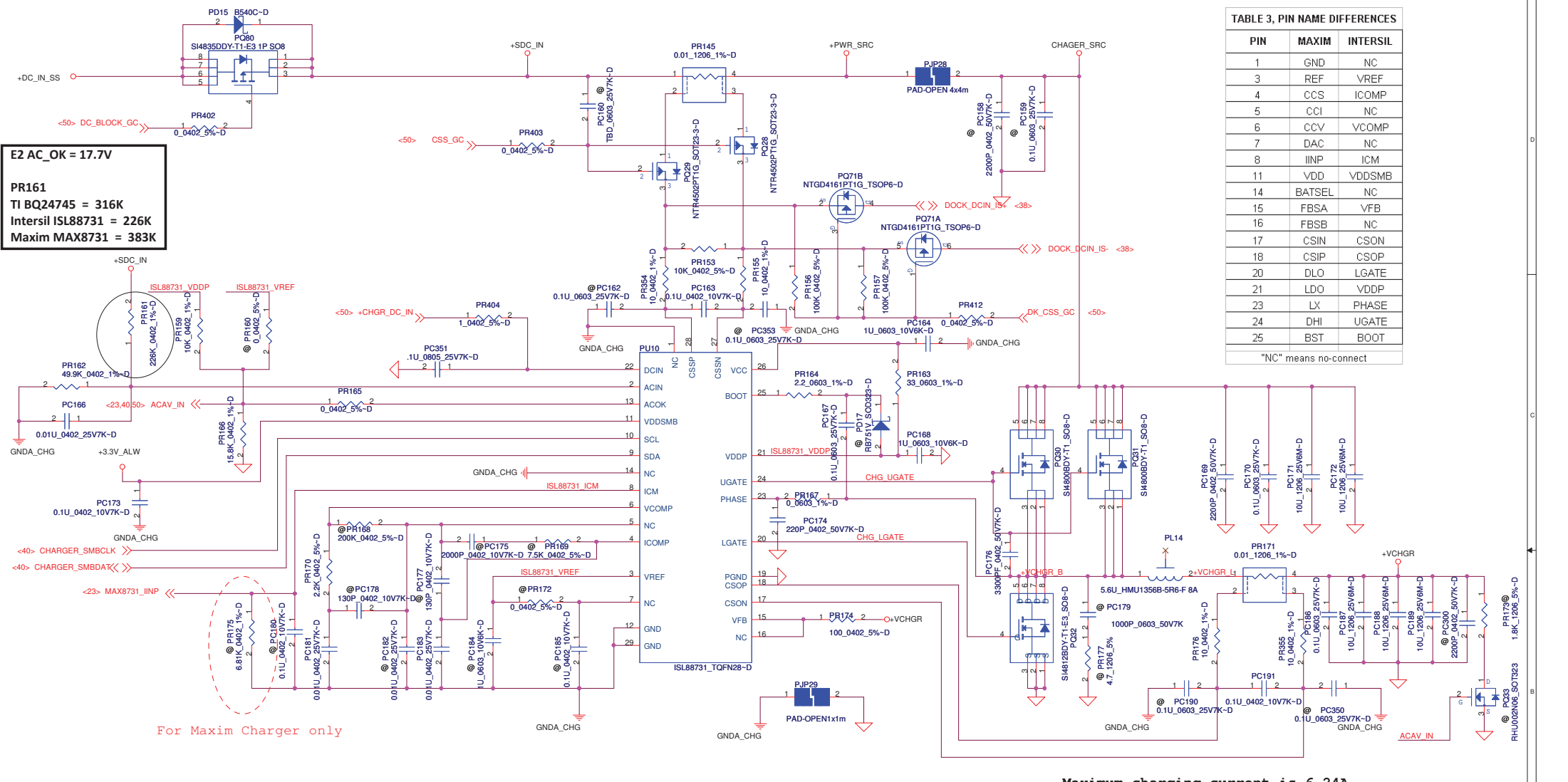
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PIN	MAXIM	INTERSIL
1	GND	NC
3	REF	VREF
4	CCS	ICOMP
5	CCI	NC
6	CCV	VCOMP
7	DAC	NC
8	IINP	ICM
11	VDD	VDDSMB
14	BATSEL	NC
15	FBSA	VFB
16	FBSB	NC
17	CSIN	CSOIN
18	CSIP	CSOP
20	DLO	LGATE
21	LDO	VDDP
23	LX	PHASE
24	DHI	UGATE
25	BST	BOOT

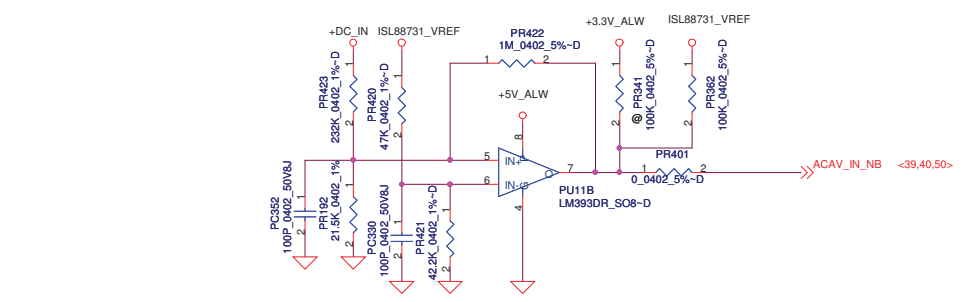
"NC" means no-connect

E2 AC_OK = 17.7V
 PR161
 TI BQ24745 = 316K
 Intersil ISL88731 = 226K
 Maxim MAX8731 = 383K



For Maxim Charger only

Maximum charging current is 6.24A

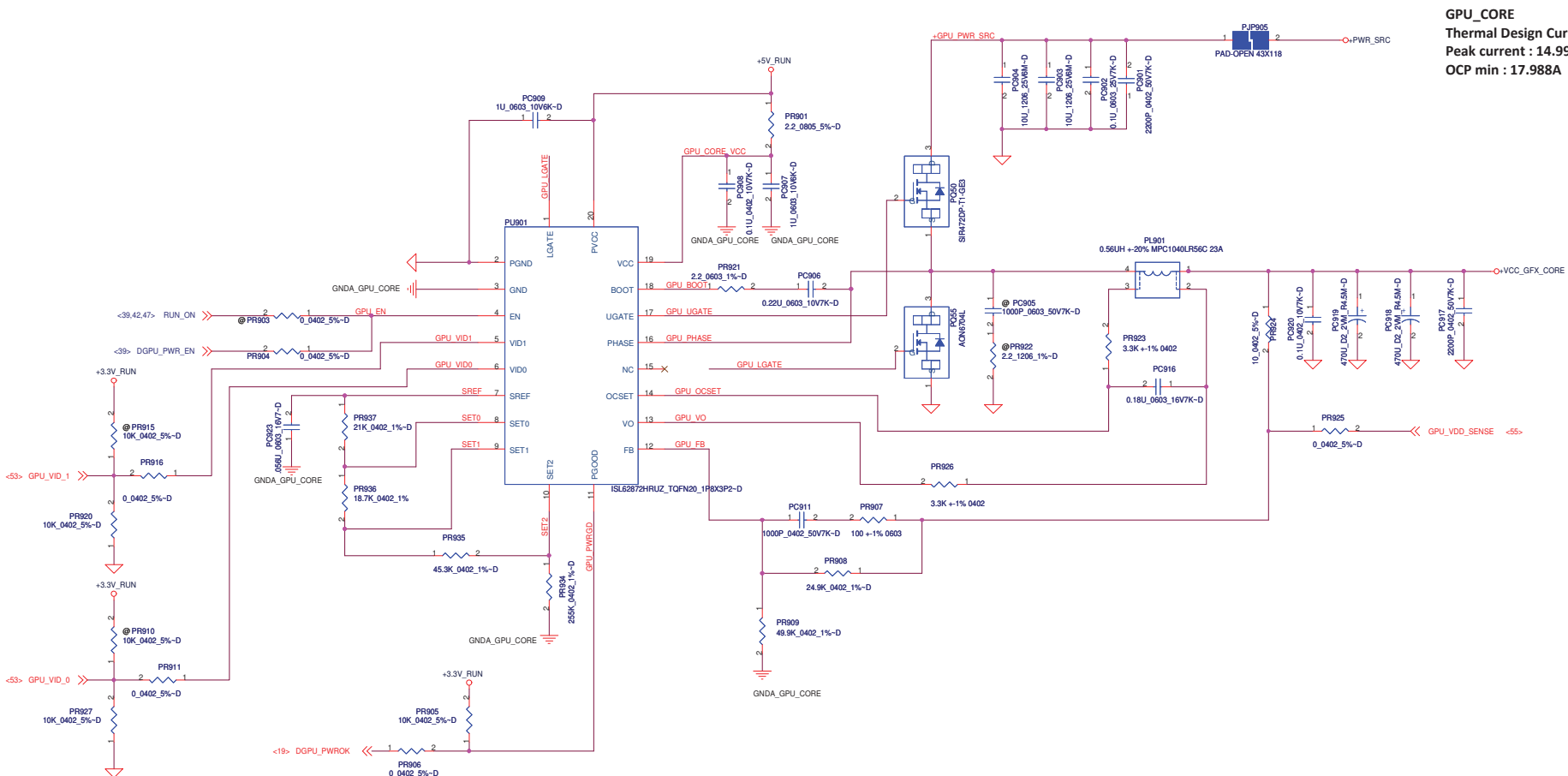


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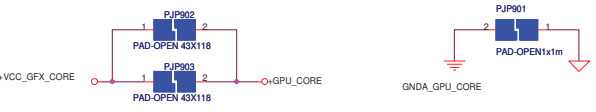


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Compal Electronics, Inc.		
Charger		
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GPU_CORE
 Thermal Design Current : 11.587A
 Peak current : 14.990A
 OCP min : 17.988A



	1.0V	0.85V	0.8V	0.75V
GPU_VID_0	0	1	0	1
GPU_VID_1	0	0	1	1

output voltage adjustable network

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ISL62870 GPU core

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Size: **LA-5472P**

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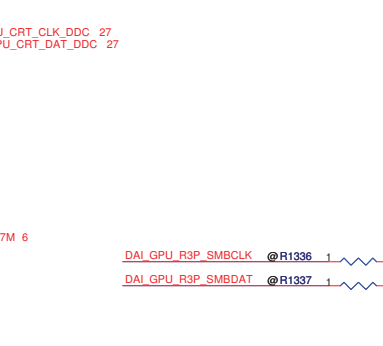
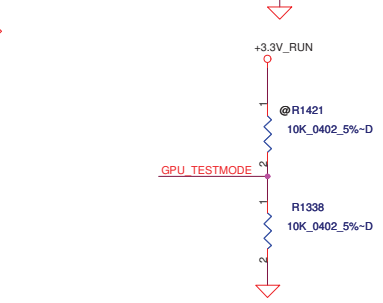
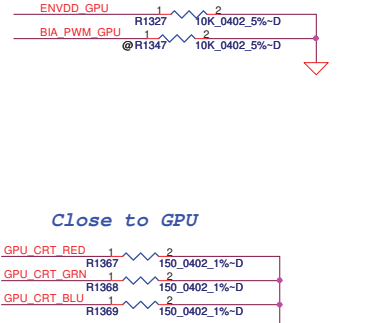
7 PEG_CTX_GRX_P0.[15] >> PEG_CTX_GRX_P0.[15]
 7 PEG_CTX_GRX_N0.[15] >> PEG_CTX_GRX_N0.[15]
 7 PEG_CRX_GTX_P0.[15] << PEG_CRX_GTX_P0.[15]
 7 PEG_CRX_GTX_N0.[15] << PEG_CRX_GTX_N0.[15]

PEG_CRX_GTX_P0	0.1U	0402	10V7K-D	2	1	C1439	PEG_CRX_GTX_C_P0
PEG_CRX_GTX_N0	0.1U	0402	10V7K-D	2	1	C1440	PEG_CRX_GTX_C_N0
PEG_CRX_GTX_P1	0.1U	0402	10V7K-D	2	1	C1441	PEG_CRX_GTX_C_P1
PEG_CRX_GTX_N1	0.1U	0402	10V7K-D	2	1	C1442	PEG_CRX_GTX_C_N1
PEG_CRX_GTX_P2	0.1U	0402	10V7K-D	2	1	C1443	PEG_CRX_GTX_C_P2
PEG_CRX_GTX_N2	0.1U	0402	10V7K-D	2	1	C1444	PEG_CRX_GTX_C_N2
PEG_CRX_GTX_P3	0.1U	0402	10V7K-D	2	1	C1446	PEG_CRX_GTX_C_P3
PEG_CRX_GTX_N3	0.1U	0402	10V7K-D	2	1	C1447	PEG_CRX_GTX_C_N3
PEG_CRX_GTX_P4	0.1U	0402	10V7K-D	2	1	C1448	PEG_CRX_GTX_C_P4
PEG_CRX_GTX_N4	0.1U	0402	10V7K-D	2	1	C1449	PEG_CRX_GTX_C_N4
PEG_CRX_GTX_P5	0.1U	0402	10V7K-D	2	1	C1450	PEG_CRX_GTX_C_P5
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PEG_CRX_GTX_P7	0.1U	0402	10V7K-D	2	1	C1454	PEG_CRX_GTX_C_P7
PEG_CRX_GTX_N7	0.1U	0402	10V7K-D	2	1	C1455	PEG_CRX_GTX_C_N7
PEG_CRX_GTX_P8	0.1U	0402	10V7K-D	2	1	C1457	PEG_CRX_GTX_C_P8
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PEG_CRX_GTX_N14	0.1U	0402	10V7K-D	2	1	C1471	PEG_CRX_GTX_C_N14
PEG_CRX_GTX_P15	0.1U	0402	10V7K-D	2	1	C1472	PEG_CRX_GTX_C_P15
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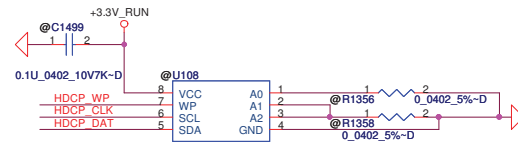
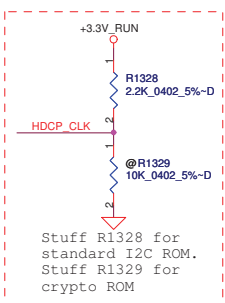
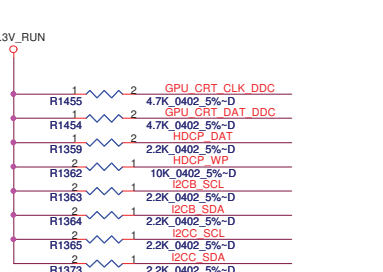
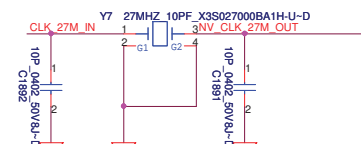
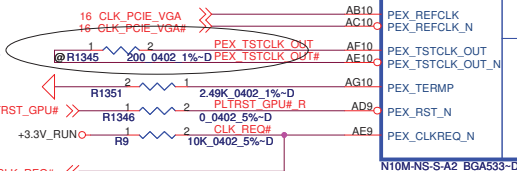
U106A Part 1 of 5

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PEG_CTX_GRX_P2	AE13	PEG_CTX_GRX_P3	AE13
PEG_CTX_GRX_N2	AE13	PEG_CTX_GRX_N3	AE15
PEG_CTX_GRX_P4	AG15	PEG_CTX_GRX_N4	AG16
PEG_CTX_GRX_P5	AE16	PEG_CTX_GRX_N5	AE16
PEG_CTX_GRX_P6	AE18	PEG_CTX_GRX_N6	AE18
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PEG_CTX_GRX_P13	AG24	PEG_CTX_GRX_N13	AG24
PEG_CTX_GRX_P14	AG25	PEG_CTX_GRX_N14	AG26
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PEG_CRX_GTX_C_P1	AD11	PEG_CRX_GTX_C_N1	AC12
PEG_CRX_GTX_C_P2	AB11	PEG_CRX_GTX_C_N2	AB12
PEG_CRX_GTX_C_P3	AD13	PEG_CRX_GTX_C_N3	AD14
PEG_CRX_GTX_C_P4	AD15	PEG_CRX_GTX_C_N4	AD16
PEG_CRX_GTX_C_P5	AB14	PEG_CRX_GTX_C_N5	AB15
PEG_CRX_GTX_C_P6	AC16	PEG_CRX_GTX_C_N6	AD16
PEG_CRX_GTX_C_P7	AD17	PEG_CRX_GTX_C_N7	AD18
PEG_CRX_GTX_C_P8	AC18	PEG_CRX_GTX_C_N8	AC18
PEG_CRX_GTX_C_P9	AB18	PEG_CRX_GTX_C_N9	AB19
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PEG_CRX_GTX_C_P11	AD20	PEG_CRX_GTX_C_N11	AD21
PEG_CRX_GTX_C_P12	AB21	PEG_CRX_GTX_C_N12	AB22
PEG_CRX_GTX_C_P13	AC22	PEG_CRX_GTX_C_N13	AD22
PEG_CRX_GTX_C_P14	AD22	PEG_CRX_GTX_C_N14	AD24
PEG_CRX_GTX_C_P15	AE25	PEG_CRX_GTX_C_N15	AE26

GPIO	N1 X	DPB_GPU_HPD	DPB_GPU_HPD_38
GPIO1	C1	BIA_PWM_GPU	BIA_PWM_GPU_24
GPIO2	M2	ENVDD_GPU	ENVDD_GPU_24,39
GPIO3	M3	PANEL_BKEN_DGPU	PANEL_BKEN_DGPU_39
GPIO4	K3	GPU_VID_0	GPU_VID_0_52
GPIO5	K2	GPU_VID_1	GPU_VID_1_52
GPIO6	J2 X		
GPIO7	C2 X	THERMTRIP_VGA#	THERMTRIP_VGA#_23
GPIO8	M1 X		
GPIO9	D2 X		
GPIO10	D1 X		
GPIO11	J3 X	GPU_CLKDWN	GPU_CLKDWN_39
GPIO12	J1 X		
GPIO13	F3 X	DPC_GPU_HPD	DPC_GPU_HPD_26
GPIO14	G3 X		
GPIO15	G2 X		
GPIO16	F1 X		
GPIO17	F2 X	EDP_HPD	EDP_HPD_24
GPIO18	F2 X		
GPIO19	F2 X		
DACA	AD2	GPU_CRT_HSYNC	GPU_CRT_HSYNC_27
DACA_VSYNC	AD1	GPU_CRT_VSYNC	GPU_CRT_VSYNC_27
DACA_RED	AE2	GPU_CRT_RED	GPU_CRT_RED_27
DACA_BLUE	AD3	GPU_CRT_BLU	GPU_CRT_BLU_27
DACA_GREEN	AE3	GPU_CRT_GRN	GPU_CRT_GRN_27
DACA_VREF	AF1	DACA_VREF	C1456 1 2 0.1U 0402 10V7K-D
DACA_RSET	AE1	DACA_RSET	R1325 2 124_0402_1%-D
DACB_HSsync	U6 X		
DACB_VSYNC	U4 X		
DACB_RED	T5 X		
DACB_BLUE	R4 X		
DACB_GREEN	T4 X		
DACB_VREF	R6 X		
DACB_RSET	V6 X		
TEST	AF3	GPU_JTAG_TCK	Tv9
JTAG_TCK	AG4	GPU_JTAG_TDI	Tv7
JTAG_TDO	AE4	GPU_JTAG_TDO	Tv8
JTAG_TMS	AF4	GPU_JTAG_TMS	Tv6
JTAG_TRST_N	AG3	GPU_JTAG_TRST#	R1372 1 2 1K_0402_1%-D
TESTMODE	AD25	GPU_TESTMODE	
I2C	R1	GPU_CRT_CLK_DDC R	R1418 2 33_0402_5%-D
I2CA_SCL	R2	GPU_CRT_DAT_DDC R	R1419 2 33_0402_5%-D
I2CA_SDA	T3		
I2CB_SCL	R3		
I2CB_SDA	R2		
I2CC_SCL	A2		
I2CC_SDA	B1		
I2CH_SCL	A3	HDCP_CLK	
I2CH_SDA	A4	HDCP_DAT	
I2CS_SCL	T1	DAI_GPU_R3P_SMBCLK	DAI_GPU_R3P_SMBCLK_29,40
I2CS_SDA	T2	DAI_GPU_R3P_SMBDAT	DAI_GPU_R3P_SMBDAT_29,40
XTAL_SSN	D11	XTALSSIN	@R1317 1 2 0_0402_5%-D
XTAL_OUTBUFF	E9	XTALOUTBUFF	R1416 1 2 10K_0402_5%-D
XTAL_OUT	E10		
XTAL_IN	D10	CLK_27M_IN	R1541 1 2 0_0402_5%-D
			@R631 1 2 0_0402_5%-D



Differential signal



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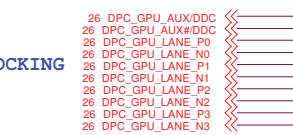
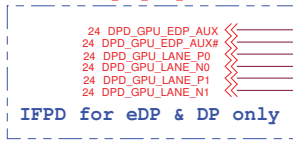
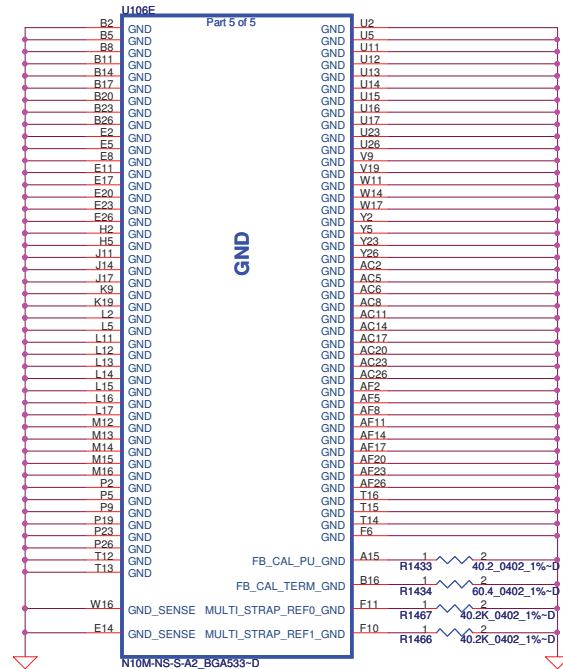
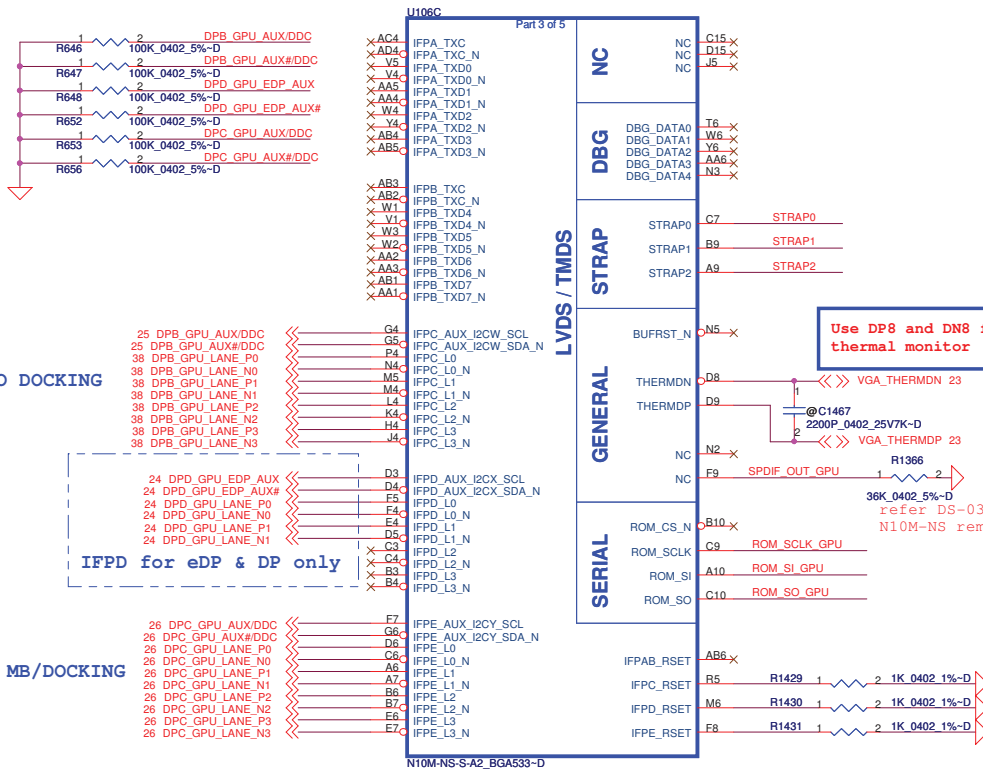
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Title: N10M PCIe,I2C,DAC,GPIO

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Stuff R1328 for standard I2C ROM.
 Stuff R1329 for crypto ROM



Resistor Values	Pull-up to +3V	Pull-down to Gnd
5K	01111	11111
10K	01110	11110
15K	01011	11011
20K	01001	11001
25K	00111	10111
30K	00110	10110
35K	00011	10011
45K	00000	10000

X7620431001:for Hynix 64Mx16 DDR3 part stuff R1343=15K
 X7620431002:For Samsung 64Mx16 DDR3 part stuff R1343=20K

STRAP0	USER[3:0]
STRAP1	3GIO_PADCFG_LUT_ADR[3:0]
STRAP2	PCI_DEVID[3:0]

ROM_SCLK	PCIDEVID_EXT, SUB_VENDOR, SLOT_CLK, PEX_PLL_EN
ROM_SI	RAM_CFG[3:0]
ROM_SO	XCLK_417, FB_0_BAR_SIZE, ALT_ADOOR, VGA_DEVICE

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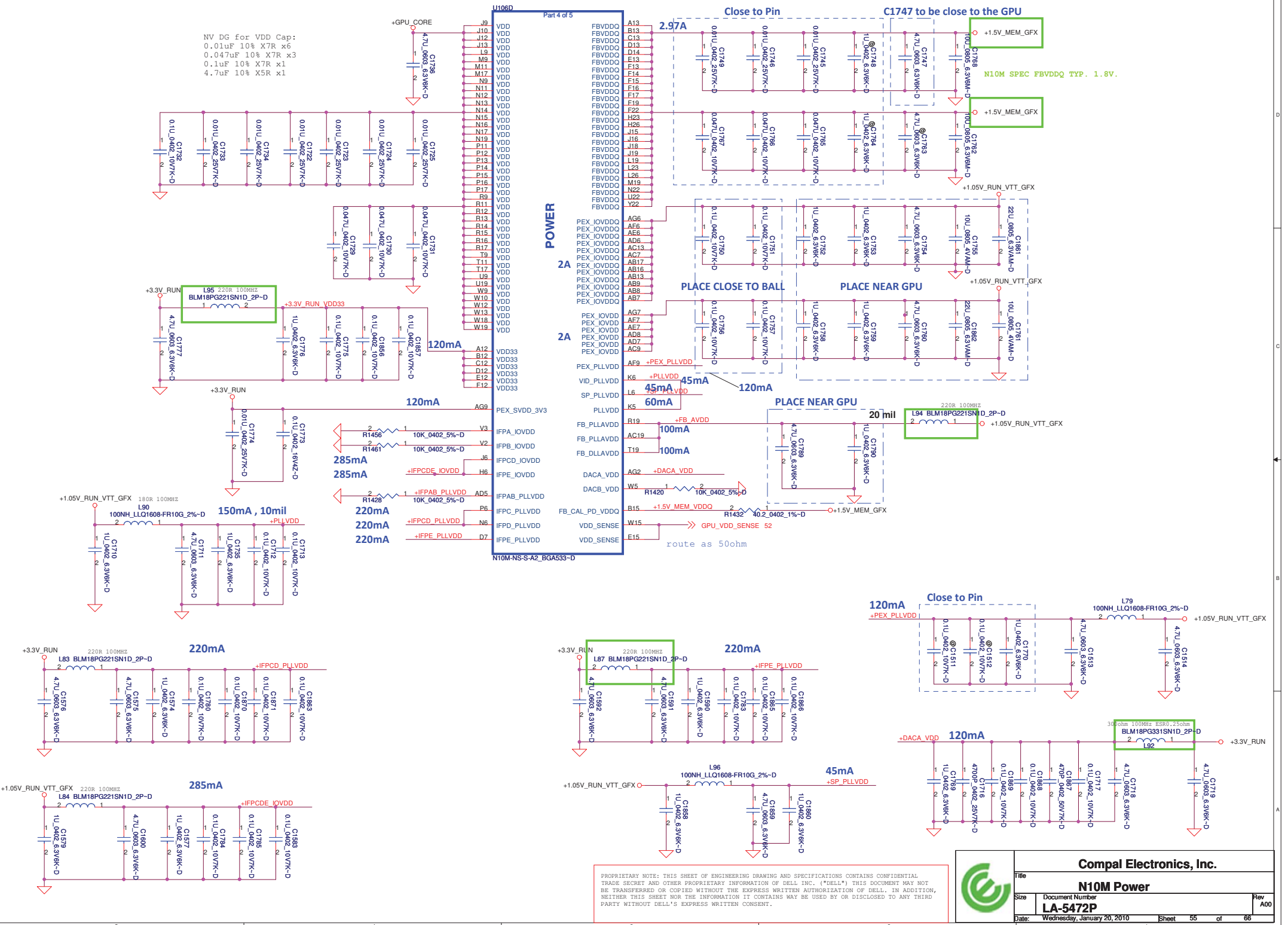
Compal Electronics, Inc.

N10M DP, STRAP, GND

LA-5472P

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NV DG for VDD Cap:
 0.01uF 10% X7R x6
 0.047uF 10% X7R x3
 0.1uF 10% X7R x1
 4.7uF 10% X5R x1



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Title: **N10M Power**

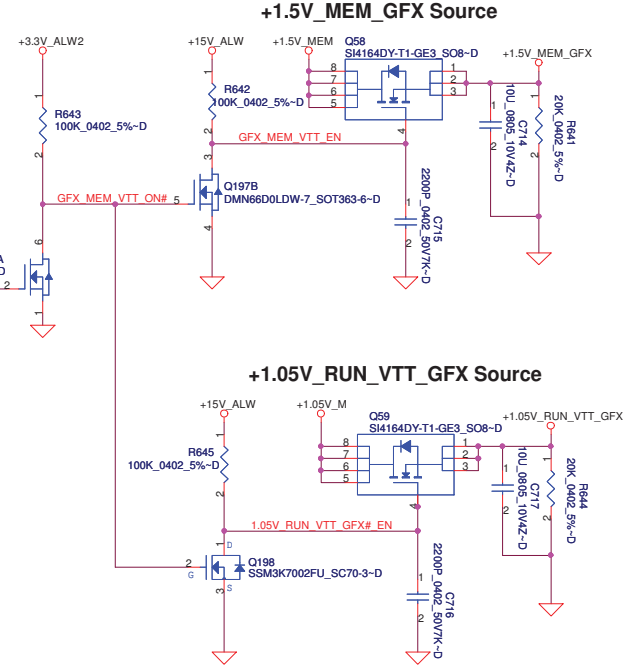
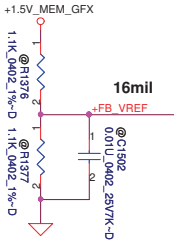
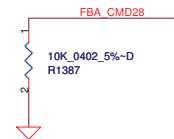
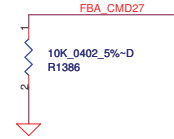
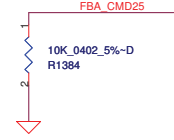
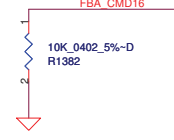
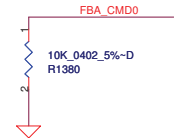
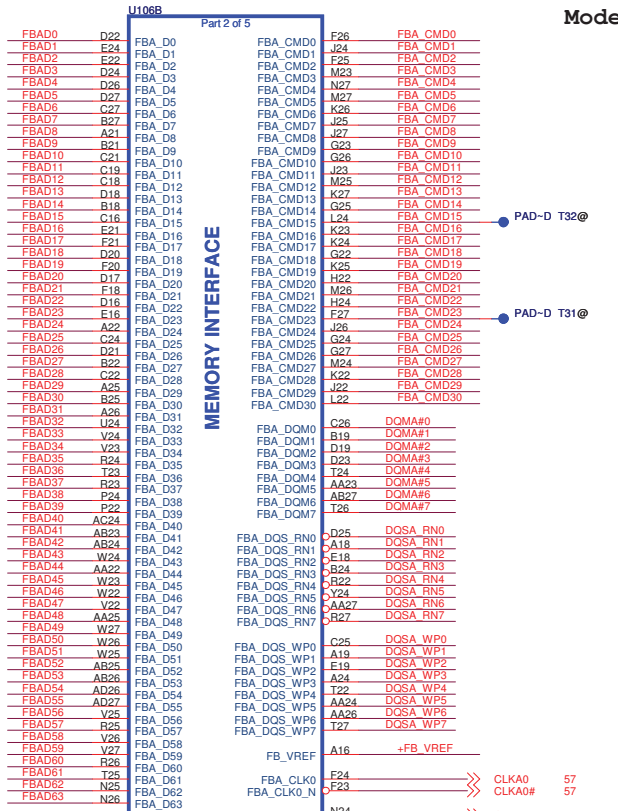
Size: **Document Number LA-5472P**

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FBAD[0..63] <<>> FBAD[0..63] 57.58
 FBA_CMD[0..30] <<>> FBA_CMD[0..30] 57.58
 DQMA#[0..7] <<>> DQMA#[0..7] 57.58
 DQSA_RN[0..7] <<>> DQSA_RN[0..7] 57.58
 DQSA_WP[0..7] <<>> DQSA_WP[0..7] 57.58

Mode C - Mirror Mode Mapping

DATA Bus	
Address	0..31 32..63
CMD0	CKE_L
CMD1	A8 A8
CMD2	CS0#_L
CMD3	A7 A6
CMD4	A2 A1
CMD5	A11 A9
CMD6	A5 A4
CMD7	A0 A12
CMD8	CAS# CAS#
CMD9	BA1 A3
CMD10	A9 A11
CMD11	CS0#_H
CMD12	BA0 BA0
CMD13	BA2 A15
CMD14	A3 BA1
CMD15	CS1#_H
CMD16	ODT_H
CMD17	A4 A5
CMD18	A13 A14
CMD19	WE# A10
CMD20	A1 A2
CMD21	A10 WE#
CMD22	A12 A0
CMD23	CS1#_L
CMD24	RAS# RAS#
CMD25	ODT_L
CMD26	A6 A7
CMD27	CKE_H
CMD28	RST RST
CMD29	A14 A13
CMD30	A15 BA2



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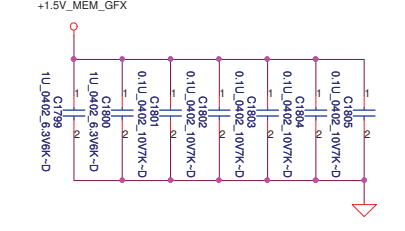
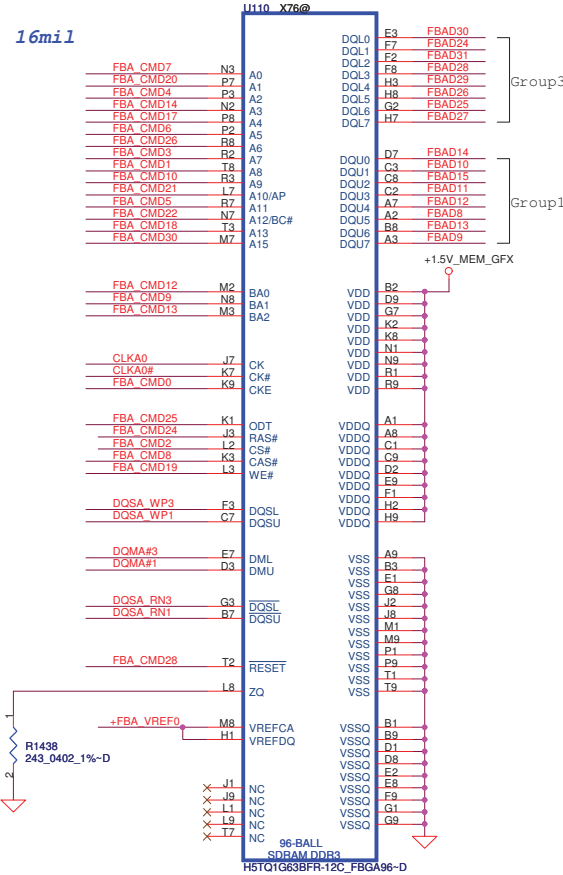
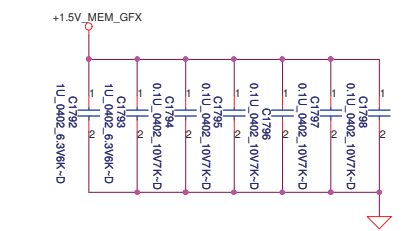
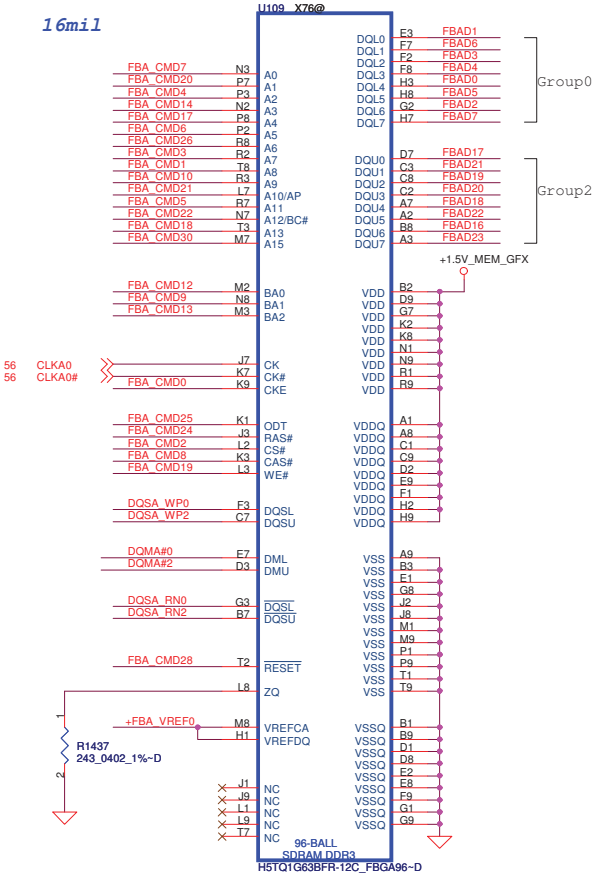
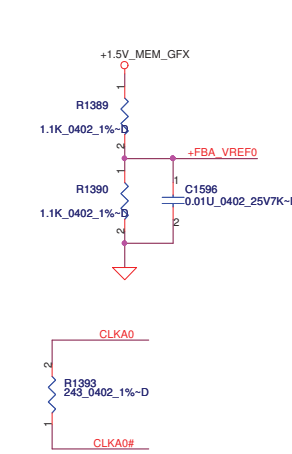
N10M Memory

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Memory Partition A - Lower 32 bits

- FBA_CMD[0..30] << FBA_CMD[0..30] 56.58
- FBAD[0..63] << FBAD[0..63] 56.58
- DQMA#[0..7] << DQMA#[0..7] 56.58
- DQSA_RN[0..7] << DQSA_RN[0..7] 56.58
- DQSA_WP[0..7] << DQSA_WP[0..7] 56.58



Mode C - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	BA0
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2



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Title: **VRAM A Lower**

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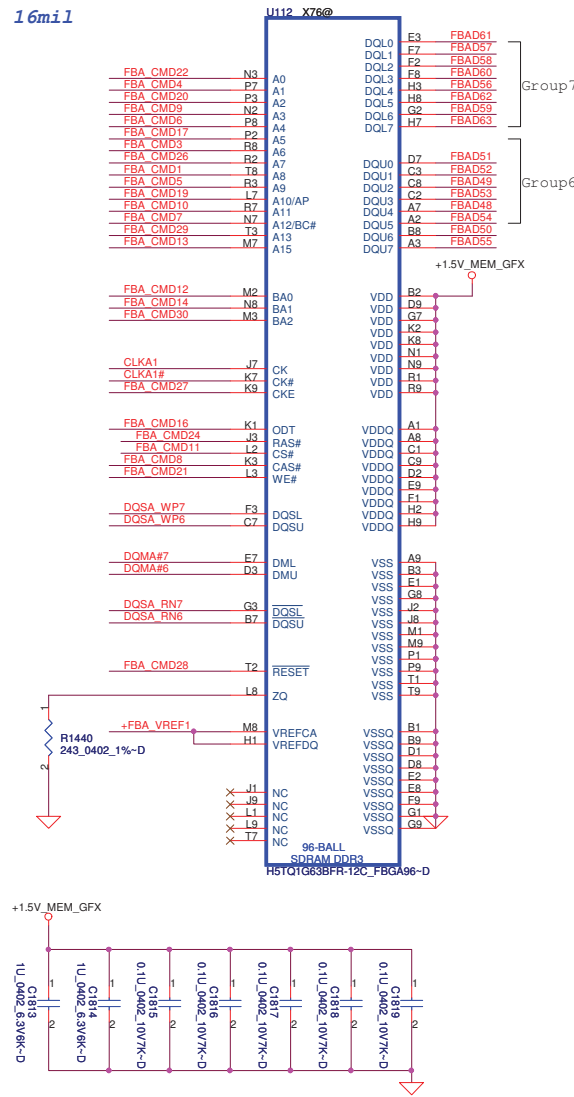
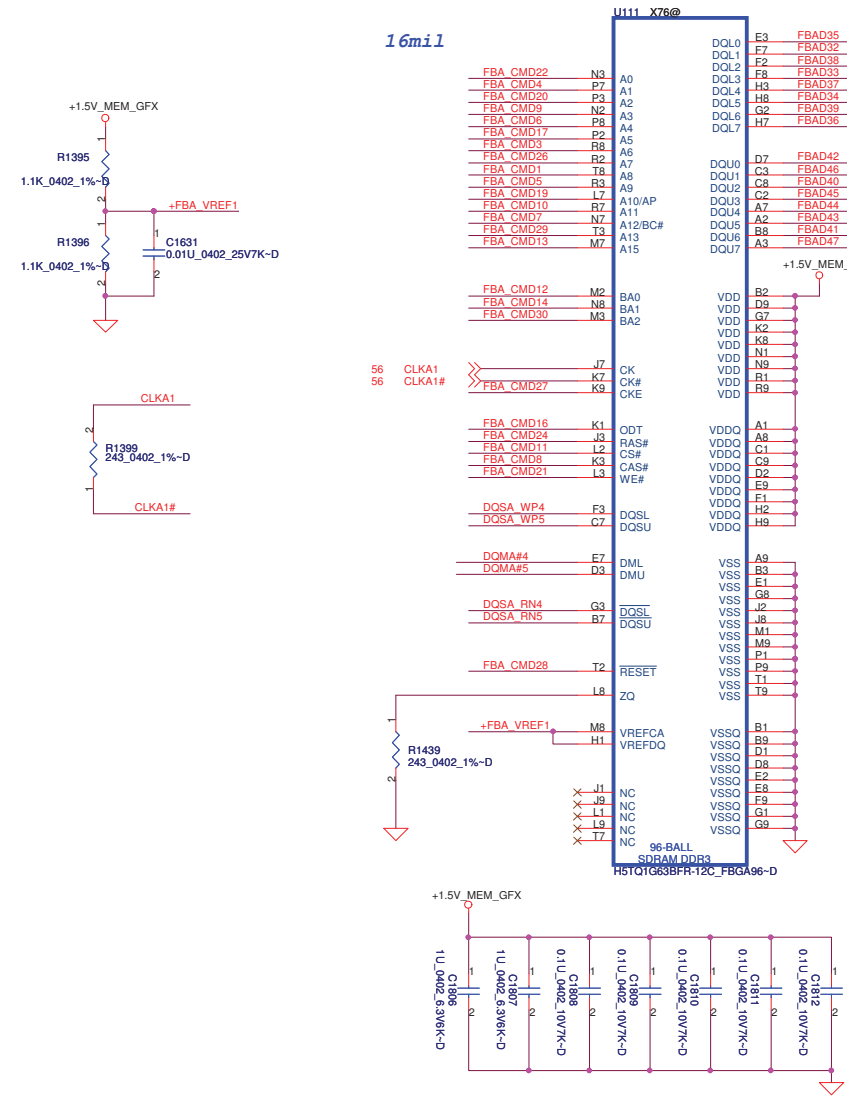
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Memory Partition A - Upper 32 bits

- FBAD[0..63] <<>> FBAD[0..63] 56..57
- FBA_CMD[0..30] <<>> FBA_CMD[0..30] 56..57
- DOMA#[0..7] <<>> DOMA#[0..7] 56..57
- DQSA_RN[0..7] <<>> DQSA_RN[0..7] 56..57
- DQSA_WP[0..7] <<>> DQSA_WP[0..7] 56..57



Mode C - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	BA0
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2

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VRAM A Upper

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	40	HW	7/13/2009	COMPAL	Board ID	R98 change to 130k ohm	X01
2	30	HW	7/13/2009	COMPAL	follow M09 +3.3V_LAN enable control circuit	Depop R47	X01
3	8, 12, 13, 42	HW	7/13/2009	Intel	Intel S3 reduction circuit.	Add R1469, R1497~R1505, R1507~R1509, C1875, C1878~C1884, Q199~Q202, Q205, Q207, Q208, U141, PJP906, PJP907, change R879 to 1.5K, R880 to 750ohm, R624 to 22 ohm, change CPU CDDQ power source from +1.5V_MEM to +1.5V_CPU_VDDQ, change +.075_DDR_VTT discharge gate from RUN_ON_ENABLE# to RUN_ON_CPU1.5VS3#, add +1.5V_CPU_VDDQ discharge circuit, add net "DDR_HVREF_RST_GATE" from U36.A34 to Q119.2, "CPU1.5V_S3_GATE" from U36.A36 to R1501	X01
4	31	HW	7/23/2009	Broadcom	Change C718 value	Change C718 from .47uF to .22uF	X01
5	23	HW	7/23/2009	DELL	Follow DELL request to remove R3P circuit	Delete U140, R136, R138, R156,R507, R516, R519, R529, R531, R534~R536, R594, R1457, R1458, R1462, R1463, C434, C72, C73, C391, C406, pop R142, D2, C219	X01
6	41,37	HW	7/23/2009	Compal	Per M09 lesson learn request	Re-define JTP1, JBI01	X01
7	19	HW	7/23/2009	Intel	GPIO1, 6, 7 need to PU if no used.	Add R1506, R1510	X01
8	40 43	HW	7/23/2009	Compal	Follow SMSC5045 spec	Add R1512, @C1885, C1886, change R560 to 100Kohm, add net name LAT_ON_SW#_R	X01
9	31	HW	7/23/2009	Broadcom	Remove RFID disable circuit	Remove R1062~R1065	X01
10	24	HW	7/23/2009	Compal	CAM Module change from 7 pin to 8 pin	Change pin define for JEDP1	X01
11	31	HW	7/23/2009	Broadcom	R898 and R485 pop at the same time	Depop R898	X01
12	24	HW	7/29/2009	Compal	Nvidia BIA_PWM implementation	POP R165, de-pop R166	X01
13	8,15	HW	7/29/2009	Compal	Depop all related components where are located at 0 Z-high area	Depop JXDP1, JXDP2, JDEG1, JP2 connector	X01
14	42	HW	7/29/2009	Compal	For load switches Vout over 5% range concern by power team.	Change Q151 to SIS406D,Q183 to SI7658ADP,Q58 to SI4164DY	X01
15	42	HW	7/29/2009	Compal	Backdrive EA Failure on RAM	Pop R625 and Q79, change R625 to 0603 size.	X01
16	21	HW	7/29/2009	Intel	The PLLs aren't used in a DIS system	De-pop C105 & C106	X01
17	36,39	HW	7/29/2009	DELL	Reconnect the signal UWB_RADIO_DIS#	Connect UWB_RADIO_DIS# from EC5028.A56 to MINI3.20	X01
18	24	HW	7/29/2009	PERICOM	Pericom 8200 SW issue DVI can not work	Add R1516 to pull up U9 pin 23 (P1_OC0) of Pericom 8200 SW with a 4.7K ohm resistor to +3.3_RUN	X01
19	29	HW	7/29/2009	Compal	EMI solution.	Change R1295 to L4 (220ohm) and R1217 from 22ohm to 47ohm.	X01
20	42	HW	7/29/2009	Compal	Base on de-rating report.	Change Q61 from AO4456 to NTMS4107.	X01
21	37, 39	HW	7/29/2009	Compal	GPIO MAP update	Add reserved R1513 between U95.18 and +3.3V_RUN, add R1514 between U95.18 and 5028.A47 named EN_ESATA_RPTR.	X01

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
22	31	HW	7/29/2009	Broadcom	Resolve 5882 leakage issue	Add R884, R1515, Q209, Q210	X01
23	31	HW	7/29/2009	Broadcom	Resolve smart cart can't work problem.	pop R775, R537, depop R776.	X01
24	36	HW	7/29/2009	Compal	Change PU power rail for USB_MCARD1_DET#	Change USB_MCARD1_DET# PU power rail to +3.3V_RUN	X01
25	31	HW	7/29/2009	Compal	Remove R1061 to avoid double PU and provide back-drive path.	Remove R1061	X01
26	21	HW	7/29/2009	Compal	Follow the pop option on CRB1.6 to depop C39 for +VCCACLK, C610 for +SATAPLL, C111 and C112 for +1.05V_M_VCEPW	Depop C610, C39, C111, C112	X01
27	15	HW	7/29/2009	Compal	Base on crystal EA result.	Change external Load Capacitor Value C296 and C297 to 12 pF of Y1.	X01
28	30	HW	7/29/2009	Compal	Base on crystal EA result.	Change external Load Capacitor Value C476 to 33 pF and C427 change to 200 ohm (R808) of Y2.	X01
29	40	HW	7/29/2009	Compal	Base on crystal EA result.	Change external Load Capacitor Value C674 and C675 to 33 pF of Y4.	X01
30	33	HW	7/29/2009	Compal	Base on crystal EA result.	Change external Load Capacitor Value C514 and C515 to 22 pF of X3.	X01
31	29	HW	7/29/2009	Compal	EMI solution.	Change R1215 from 22ohm to 47ohm.	X01
32	29	HW	7/29/2009	Compal	Prevent floating of PCH_GPIO34	Add R1511 10K PD.	X01
33	38	HW	7/29/2009	Compal	Based on DFX team request	Change docking connector from SP030000F0L(JAE_WD2F144WB1_144P-T) to SP030000F0L(JAE_WD2F144WB1R300_144P).	X01
34	36	HW	7/29/2009	Compal	Change PU power rail for PCIE_MCARD3_DET#	Change PCIE_MCARD3_DET# PU power rail to +3.3V_RUN	X01
35	18 35	HW	05/08/2009	Compal	Remove Braidwood circuit.	Delete R1411,R1453,JBW1	X01
36	36	HW	05/08/2009	Compal	Base on SATA EA result, need to trun off Pre-emphasis 0.	Depop R1298,pop R1301.	X01
37	33	HW	10/08/2009	Compal	Base on crystal EA result.	Change C514 C514 to 15pF and R421 to 100 ohm.	X01
38	38	HW	11/08/2009	Compal	Change VGA_ID_DISC & VGA_ID_UMA PU power rail	Change VGA_ID_DISC & VGA_ID_UMA PU power rail from +3.3V_RUN to +3.3V_ALW	X01
39	38	HW	11/08/2009	Compal	Change ODD_DET# PU power rail.	Change ODD_DET# PU power rail to +3.3V_RUN	X01
40	41	HW	11/08/2009	SMSC	Watch dog timer may not be reseted when EMC4002 VDD_PWRGD is not completely at Logic Low.	Add discharge circuit for +3.3V_M	X01
41	23	HW	11/08/2009	SMSC	SMSC review feedback	The pull-up source of the R150 should be changed to +VCC_4002	X01
42	39	HW	11/08/2009	SMSC	per SMSC 5045 AN 19.6, 4002 AN 16.11	R541, R554, R1512 should be 10K.	X01
43	23	HW	11/08/2009	Compal	FAN1_DET# should have 10K PU to +3.3V_M	Add R1517	X01
44	31	HW	11/08/2009	Broadcom	Follow Broadcom request	Delete T159, R494, R498, R631, R634, R898, C640, C641, C642 C647, C1026, L73, add R1522, C1887, C1888, change connection for R496, R497 to GND, change connection for JCS1pin3 and pin4	X01

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
45	8	HW	11/08/2009	DELL	Fix the Intel S3 power up timing	Change C1880 from 0.01uF to 0.22uF 0402 cap.	X01
46	31	HW	11/08/2009	Broadcom	Follow Broadcom request	Change C646 to 220nF that was placed near the JSC1 pin 10 (+SC_VCC). And 470nF should be at C718 near U3 (TDA8034)	X01
47	31	HW	12/08/2009	Broadcom	Follow Broadcom request	Change R497 & R496 to 0 ohm, but depop	X01
48	27	HW	12/08/2009	Compal	RGB EA result	C251-C253 to 8.2pF; L61-L63 to 10-Ohm Bead ; De-pop C390,C518,C996	X01
49	29	HW	12/08/2009	DELL	Use the SiTimes part due to the cost savings	Change X4 from TXC to SiTimes SIT8102AC3333E12T	X01
50	8	HW	12/08/2009	Intel	Intel review schematic feedback	Add R529 and C1889	X01
51	33	HW	12/08/2009	Richo	Change pop option for R5U242	Change C21 from 10U to 47U, change R46 to C1889 (1uF)	X01
52	31	HW	12/08/2009	Broadcom	BCM5882 pin-C1 "RSTOUT_N" is an open drain I/O type, we need to have 4.7K pull-up to 3.3V_ALW	Add R638	X01
53	30 36	HW	13/08/2009	Compal	Disconnect IO & DOCK VCT	Delete R652 & C41, Rename IO VCT to +LOM_VCT_IO & reserve C712 pad for test.	X01
54	31	HW	13/08/2009	Compal	Broadcom review request	USB_GPIO27 Should have a 0ohm but de-pop resistor.	X01
55	39	HW	14/08/2009	SMSC	SMSC review	Change R561 and R1046 from 1M ohm to 100K ohm.	X01
56	39	HW	14/08/2009	SMSC	SMSC review	Remove R587, base on crystal EA result that only need to change caps value.	X01
57	10	HW	14/08/2009	Intel	Follow Intel recommand to add debug TP.	Add T186~T190	X01
58	31	HW	14/08/2009	Compal	Smart card EA result	Change R772 to 47 Ohm and C1015 to 10pF for resolving SC_CLK Rise/Fail timing issue and also change C633 to 10pF.	X01
59	31	HW	14/08/2009	DELL	Avoid a glitch for DDR_HVREF_RST_GATE, please add a 1.1K 1% no-stuff pull-up to +1.5V_CPU_VDDQ rail on the PM_DRAM_PWRGD_R signal for a back-up option	Change C1889 to 0.1u, add R1518 for PM_DRAM_PWRGD_R but depop.	X01
60	8 45	HW	14/08/2009	DELL	CPU detection since the edge diode has been removed from M'09	Delete T1 and add R1519 for CPU_DETECT# and connect JCPU.AH24 to U36.B18	X01
61	15 19 36	HW	14/08/2009	DELL	Invert the EN_ESATA_RPTR signal and connect this to SATAGP4/GPIO16	Add Q211 and R1520 but depop, pop R1513 and de-pop R1514 , change net name from GPIO16 to EN_ESATA_RPTR#	X01
62	34	HW	14/08/2009	Compal	By EMI request, pop common choke	Change Pop otion for express card, pop L64, depop R791 R792. For USB2,3 pop L65,L66 and reserve R1524,R1525,R1526 and R1527.	X01
63	30	HW	14/08/2009	Intel	By Intel request	Add R1528 for LAN_REQ#	X01
64	37	HW	17/08/2009	Intel	Adding stitching caps near the DOCK_LOM traces where it crosses over plane splits.	Add C1028	X01

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65	38	HW	8/19/2009	NV	Solve DVI issue	Add Q213~Q218, R1523, R1530~R1540	X01
66	26	HW	8/19/2009	Pericom	8200 pin 8,9 add caps to minimize noise	Add C1597 & C1598	X01
67	53	HW	8/19/2009	NV	Reserve crystal for 27M.	Add @R1541,@Y7, @C1891, @C1892	X01
68	24	HW	8/20/2009	Compal	Follow Marguax schematic	Depop R279, R1027	X01
69	53	HW	8/20/2009	Compal	Add PU/PD resistor for 8200 back-up plan	Add R1542~R1544, but depop.	X01
70	35	HW	8/24/2009	Compal	Add PD resistor for back-drive issue	Add R1545~R1547	X01
71	24	HW	8/25/2009	Compal	No need PD/PU resistors at EDP AUX channel	Delete R279 & R1027	X01
72	21	HW	8/25/2009	Compal	Add by pass caps	populate C39 & C610	X01
73	42	HW	8/25/2009	Compal	Un-populate pop option for double discharge path	Un-populate R612, R607 and R1498	X01
74	11	HW	8/25/2009	Compal	Base on power team FDIM test	Change C48, C49, C50, C51, and C52 to 22uF.	X01
75	30	HW	8/26/2009	Intel	Follow Intel WW35 `09	Change R808 to C427 10pF and change C475 to 33pF	X01
76	53	HW	8/27/2009	Compal	Follow Marguax to populate 27MHz crystal for PT build.	Populate Y7, C1891, C1892, R1541 and de-pop R631	X01
77	6, 53	HW	9/28/2009	Compal	Populate 27MHz crystal.	Depop R43, R39, R1317, pop R1417	X02
78	17	HW	9/28/2009	Intel	Follow Intel DG 1.62	Change R672 to 1K_0402_5%.	X02
79	15, 18	HW	9/28/2009	Compal	Depop XDP circuit component	Depop R118, R94	X02
80	53	HW	9/29/2009	NV	GPU_JTAG_TRST# should be pull down	Pop R1372 and cahnge to 1K Ohm.	X02
81	40	HW	10/20/2009	Compal	Depop R5	Depop R5 for double pull down	X02
82	33	HW	10/20/2009	Compal	Follow DFX recommendation change JSD1 footprint to modify screw hole.	Chnage FOX_2WX131A1-31DD-7F_20P-T to FOX_2WX131A1-31DD-7F_18P.	X02
83	36	HW	10/20/2009	Compal	Correct USB_MCARD2_DET# PU power rail	Chnage power rail from +3.3V_RUN to +3.3V_ALW_PCH	X02
84	17	HW	10/20/2009	Compal	Follow schematic check list 2.0, change resistor value	Chnage R268 from 1K to 10K	X02
85	16	HW	10/20/2009	Compal	Change R910 value and placement	Change R910 form 0 ohm to 22 ohm and place near PCH side.	X02
86	37	HW	10/26/2009	Compal	Chnage USB common choke by EMI request	Change L95 L96 from DLW21SN900SQ2_0805~D to HCMC0805-900MFS_4P~D	X02
87	23	HW	10/26/2009	Compal	Change OTP temperature	change R151 from 953ohm to 1.02Kohm	X02
88	53	HW	10/27/2009	Compal	To solve 27 Mhz noise issue	Connect Y7 pin 2 and 4 to GND.	X02
89	31	HW	10/27/2009	Broadcom	For 5882-B0 request	L71, L72 68nH, 2%, 400mA; C1070, C1071 1500pF, 2%, 50V; C1886, C1887 150pF, 2%, 50V	X02
90	15	HW	10/29/2009	Compal	Change flash ROM part number	Due to W25X32VSSIG will be EOL, change part number to W25Q32BVSSIG.	X02

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91	16	HW	10/29/2009	Dell	MEM SMBus design needs to change	Move Q190 connection, add R1549,R1550, add net name DDR_XDP_CLK/DAT	X02
92	29	HW	10/29/2009	Compal	Create a low pass filter with the pole set at 36kHz to filter out of band noise	De-pop C1066 & C1067, R1090, R1089 ; R340 & R342, R1091 & R1092 change to 2k, add C1893-C1896 1000pF.	X02
93	40	HW	11/02/2009	Compal	Change BID	Change R98 form 130K ohm to 33K ohm.	X02
94	8, 15	HW	11/02/2009	Compal	To avoid stub for SM bus EA quality XDP is not use.	Add R1551~R1556 but depop	X02
95	36	HW	11/02/2009	DELL	Support WiMax LED status	Need to populate R840	X02
96	43	HW	11/05/2009	Compal	To avoid golden finger was scraped on FFC.	Change sniffer connector from TYCO_1-1734820-2 to TYCO_1-2041070-2.	X02
97	41	HW	11/05/2009	Compal	Chnagne TP SMBus PU power rail.	Change power rail from +5V_ALW to +3.3V_ALW	X02
98	31	HW	11/05/2009	BRCM	Delete 2nd ROM for BRCN5882	By BRCM review result, delete U14.	X02
99	24	HW	11/10/2009	Compal	LCD power sequencing issue	change R161 from 470 to 100 ohm .	X02
100	19	HW	11/11/2009	DELL	PCH driving the siganl low at GPIO15 initial.	Add R1557 2.2K PU resistor to +3.3V_ALW_PCH on the SIO_EXT_WAKE# signal.	X02
101	15	HW	11/11/2009	DELL	To change the pin on the EC side to OD and add a pull-up to PCH's core well	Add R1558 10K PU resistor to +3.3V_RUN on the ME_FWP signal.	X02
102	15, 40	HW	11/11/2009	Compal	RTC timing issue	Y1 & Y4 change from 1TJS125DJ4A420P to Q13MC30610018. Opreating temperature should -40~+85 degree to meet test requirement.	X02
103	19	HW	11/17/2009	Compal	Chnagne GPIO34 of PCH from PD to PU	Change from PD to PU +3.3V_RUN	X02
104	31	HW	11/17/2009	Compal	Follow Marguax schmatic and it also could pass smart card EA.	To change R772 from 47 ohm to 22 ohm	X02
105	31	HW	11/17/2009	Compal	To solve touch pad ESD issue	Change L41 and L42 to 100 ohm (R1564 & R1565)	X02
106	15	HW	11/19/2009	Compal	Follow Intel check list rev2.0	Change R2244 to tolerance from 5% to 1%	X02
107	15	HW	11/19/2009	Compal	Follow DCU 414044 Rev2.0	Depop R123, R804-R807 and R1281, R1282, R1315.	X02
108	38	HW	12/22/2009	Compal	Simplo battery slice EMI issue	Add C1897 and C1898 (Depop, reserve for EMI test)	A00
109	37	HW	12/22/2009	Compal	DFB issue, finger printer connector will easy shift during reflow process.	Change finger printer connector from TYCO_1734242-6_6P-T to TYCO_2041070-6_6P-T	A00
110	31	HW	12/22/2009	Compal	By Broadcom recommend	Change L71, L72 from 68nH to 150nH, C1070, C1071 from 1500pF to 390pF. C1887, C1888 from 150pF to 390pF.	A00
111	32	HW	12/22/2009	Compal	Change TCM to T1 version	Change TCM from SSX44B-D-T to SSX44-D-T1	A00
112	40	HW	12/22/2009	Compal	Change BID	Change R98 form 33K ohm to 1K ohm.	A00
113	08	HW	12/22/2009	Compal	Depop CPU XDP and JTAG circuit for for production systems	Depop C19, C20, R6, R68, R19, R7, R3, R780~R785, R22, R24, R1153, R1156, R66, R1241, R1257	A00
114	15	HW	12/22/2009	Compal	Depop PCH JTAG circuit for for production systems	Depop R123, R804-R807, R1281, R1282, R1315	X00

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115	33, 34	HW	01/07/2010	Compal	Change R5U2542 form ES2 to ES3	Change part number from SA00003C21L to SA00003C22L	A00
116	27	HW	01/14/2010	Compal	RGB EMI issue	Change L61,L62,L63 from 10nH to 27nH, C251,C252,C253 from 8.2pF to 2pF and pop C390,C518,C996	A00
117	37	HW	01/15/2010	Compal	Change SATA repeater part to power saving part	Change U95 to SA00003P10L	A00
118	26	HW	01/19/2010	Pericom	Pericom DP SW DP8200 has new silicon W version in stead of Y version	Change U9 to SA00003CD2L	A00

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1	50	Selector	7/20	TI	CSS GC logic wrong issue	Add PR282 180_ohm to GND	X01
2	46	1.5V_MEM	7/20	Compal ADC Guangyong	Add droop resistor for TI solution	Add PR77	X01
3	45	+3.3V/+5V	8/17	Compal ADC Guangyong	Change 3V/5V choke for cost down	change PL5 from SH00000H90L to SH00000FN0L change PL6 from SH00000HB0L to SH00000HR0L	X01
4	50	Selector	8/17	Compal	Add 1M_ohm pull down to fix ACAV_IN_NB oscillation when battery mode S5	Add PR283	X01
5	50	Selector	8/17	TI	new version CD3301 (PG2.1) don't need PD22 and PR282	depop PD22 add PR282, pop PR430	X01
6	50	Selector	8/17	TI	DOCK_AC_OFF_EC floating issue	add PR285	X01
7	52	ISL62872_GPU	8/17	Dell / intersil	change PU901 to ISL62872 to support NV VID fixture	change PU901 to ISL62872 from ISL62870 and support circuit.	X01
8	49	+VCORE MAX17030	8/17	Compal	change thermistor package from 0603 to 0402 for cost down	Change PH3,PH4 and PH5 from SL200000B0L to SL200000W0L	X01
9	47	1.8V_RUN	8/18	MAXIM	Output ripple voltage unstable issue	Change PC314 from SE00000868L(22u/0805) to SE00000000L(100u/1206) Change PR409 from SD03480618L(8.06k) to SD03460418L(6.04k) Change PR410 from SD03440218L(4.02k) to SD03430118L(3.01k) Change PR408 from SD014402A8L(40.2 Ohm) to SD0000008H8L(51 Ohm) Change PC315 from SE000003W8L(820pF) to SE076333K8L(3300pF) Change PR411 from SD00000268L(6.98k) to SD03445318L(4.53k) Change PC310 from SE074102K8L(1000P) to SE074472K8L(4700pF) Change PC309 from SE071330J8L(33pF) to SE071560J8L(56pF) Change PC311 from SE042104K8L(0.1u/0603/25V) to SE076104K8L(.1u/0402/16V) Add PR413 SD02800008L(0 Ohm)	X01
10	49	+VCORE MAX17030	8/20	Maxim	Vcore FDIM issue	Change PR102, PR103 and PR104 from SD013220B8L(2.2) to SD00000V98L(1.1) Change PR310, PR311 and PR312 from SD03430118L(3.01k) to SD03424918L(2.49k) Change PR307, PR308 and PR309 from SD03422118L(2.21k) to SD03417418L(1.74k) Change PR137 from SD03449910L(4.99k) to SD03447518L(4.75k) Add PC271,PC272 and PC273 SE075223K8L(0.022uF)	X01
11	48	+1.05VM/ +1.05VTT	8/20	ON	Fine tune DC accurcay	Change PR188 and PR201 from SD03451018L(5.1k) to SD00000U28L(4.3k) Change PR199 and PR203 from SD03416228L(16.2k) to SD03413728L(13.7k) Change PR198 from SD03468008L(680 Ohm) to SD03418008L(180 Ohm) Change PR202 from SD03468008L(680 Ohm) to SD03410008L(100 Ohm) Change PC108 and PC116 from SE074331K8L(330p) to SE074471K8L(470p) Change PR200 from SD00000DM0L(200k) to SD03451028L(51k) Change PC115 from SE071300J0L(SE071300J0L) to SE071220J8L(22P) Change PC106 from SE071300J0L(30P) to SE071330J8L(33P) Change PR204 from SD03447518L(4.75K) to SD03452318L(5.23K) Change PR205 from SD03444228L(44.2K) to SD03424028L(24K) Change PR207 from SD00000LZ0L(3.83K) to SD00000J20L(4.32K) Change PR208 from SD03482518L(8.25k) to SD03464918L(6.49k)	X01
12	47	1.8V_RUN	8/25	DELL	1.8V transient 0.1A ~ 1.6A output voltage over spec	Change PU301 from SA00003B10L(MAX15050) to SA00003CG0L (ISL8014) and support circuit	X01

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13	49	Vcore	8/25	MAXIM	Improve DC accuracy	Change exposed pad to PGND from AGND	X01
14	49	Vcore	8/25	MAXIM	Vender recommend PSI# pull down 10k	Change PR334 from SD03410018L (1k) to SD02810028L(10k)	X01
15	51	Charger	8/25	Compal ADC Guangyong	Improve charger choke saturation current at 100 degree C	Change PL14 from SH04856AM8L (5.6u) to SH00000I60L (5.6u)	X01
16	44	DCIN	8/25	Compal	3.3V_ALW2 black driver issue with RTC battery only	Change PD1 from SC100000Q0L(BAT54CW) to SCSB715F08L (RB715F)	X01
17	49	Vcore	8/27	Compal	Reserve resistor pad for debug	Add PR122 and PR123	X01
18	52	GPU_Core	9/01	Intersil	PR916 and PR911 for debug change to 0 Ohm	Change PR916 from SD02810018L(1K) to SD02800008L(0 Ohm) Change PR911 from SD02810018L(1K) to SD02800008L(0 Ohm)	X01
19	49	Vcore	9/01	MAXIM	Fine tune Imon time constant meet Intel SPEC 300uS~500uS	Change PC270 from SE075223K8L (0.022U) to SE076333K8L (.033U)	X01
20	49	Vcore	9/01	MAXIM	Make sure DPRSLPVE low level under 0.33V	Change PR109 from SD03449908L (499 Ohm) to SD02800008L (0 Ohm)	X01
21	52	GPU_Core	10/06	NV	GPU_CORE default setting should be 1V for faster to boot to system and short warm up time for GPU	Depop PR910 and POP PR927	X02
22	44	DC_IN	10/13	TI	High inrush current on DC_IN when AC adapter plug in	Change PR20 from SD02800008L(0 Ohm) to SD02810028L(10k)	X02
23	49	Vcore	10/20	MAXIM	3 phase overlap issue with 2nd source MOSFET	Add PC198, PC199, PC255, PC256, PC259 and PC260 SE074122K8L (1200pF)	X02
24	48	+1.05VTT	10/28	INTEL	Fine tune H_VTTPWRGD voltage level meet Vih(min) = 0.75 * Vtt	Change PR94 from SD03410028L (10k) to SD03427418L (2.74K) Change PR93 from SD03428728L (28.7k) to SD03493118L (9.31K)	X02
25	49	+VCORE	11/03	Compal	change thermistor package from 0603 to 0402 for cost down	Change PH1 from SL20000068L (100K 0603) to SL20000160L (100K 0402)	X02
26	52	GPU_Core	11/12	Compal	For NVIDIA output voltage +/- 30mV criteria	Change PC918 from SGA19331D1L (330u/9m Ohm) to SGA0000420L (470u/4.5m Ohm)	X02
27	48	+1.05VTT/ +1.05VM	11/16	ON	Boost diode over stress	Change PD19 and PD27 from SC1B751V08L(RB751V) to SCS00003M0L(BAT54HT1)	X02
28	51	Charger	01/12	Compal	Reduce Pin33,34 and 35 of the CD3301 surge current	Change PC351 from SE00000130L (1u/0805) to SE043104M8L (0.1u/0805) Change PR404 from SD02800008L (0 Ohm) to SD028100B8L (1 Ohm)	A00