

# COMPAL CONFIDENTIAL

MODEL NAME : *NAL60*

PCB NO : *LA-5691P (DAA00001K00)*

BOM P/N : *43178731L01/43178731L02*

## M10 Lafite

**BGA Arrandale (34 x 28 mm) +  
SFF IBEXPEAK-M**

**2009-07-07**

**REV : 0.1(X00)**

**@ : Nopop Component**

MB Type	BOM P/N	CPU	With BLT	Non BLT	TCM		TPM		BOM CONFIG
			1@	2@	W(3@)	W/O(4@)	W(5@)	W/O(6@)	
BLT EN, TPM EN	43178731L01	SV 2.4G	*			*	*		1@, 4@, 5@
BLT EN, TPM EN	43178731L02	SV 2.0G	*		*			*	1@, 3@, 6@
BLT DIS, TCM EN	43178731L03	LV 1.8G		*		*	*		2@, 4@, 5@

MB PCB	
Part Number	Description
DAA00001K00	PCB 0AW LA-5691P REV0 M/B

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### POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	ON
S4 (Suspend to DISK) / M1	LOW	LOW	HIGH	LOW	HIGH	ON	ON	OFF	OFF	ON
S5 (SOFT OFF) / M1	LOW	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	ON
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

### PM TABLE

State \ power plane	+15V_ALW +5V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_CORE +1.05V_RUN_VTT +1.05V_RUN	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

PCH	USB PORT#	DESTINATION
	0	USB Port (Ext Right Side)
	1	NA
	2	USB Port (Ext Left Side)
	3	NA
	4	WLAN
	5	WWAN
	6	Bloetooth
	7	USB->BIO
	8	DOCKING
	9	DOCKING
	10	Express Card
	11	Camera
	12	BKT
13	WPAN/NVMHCI	

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	Card Reader
Lane 4	EXPRESS CARD
Lane 5	MINI CARD-3 WPAN/NVMHCI
Lane 6	10/100/1G LAN
Lane 7	None
Lane 8	None

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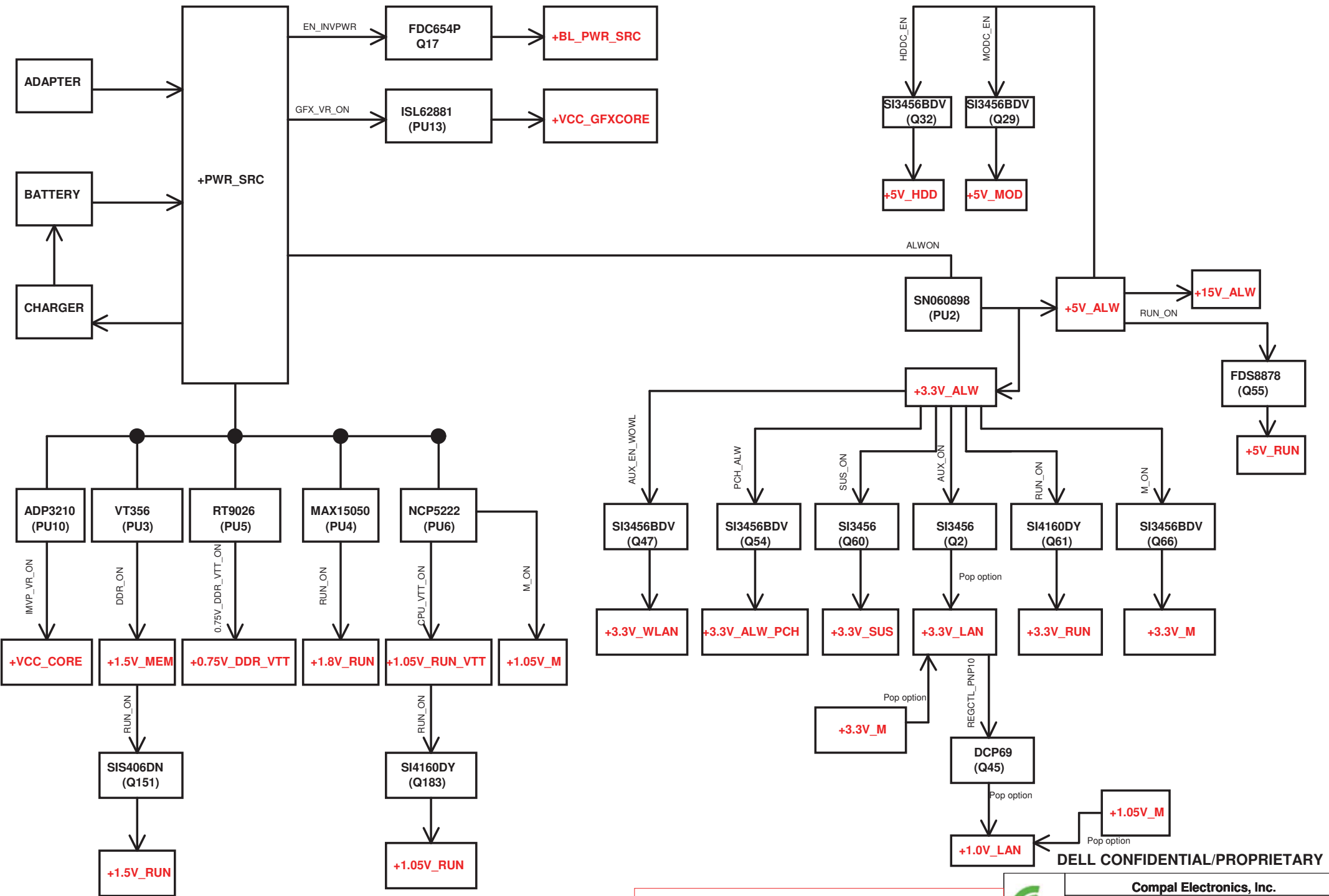
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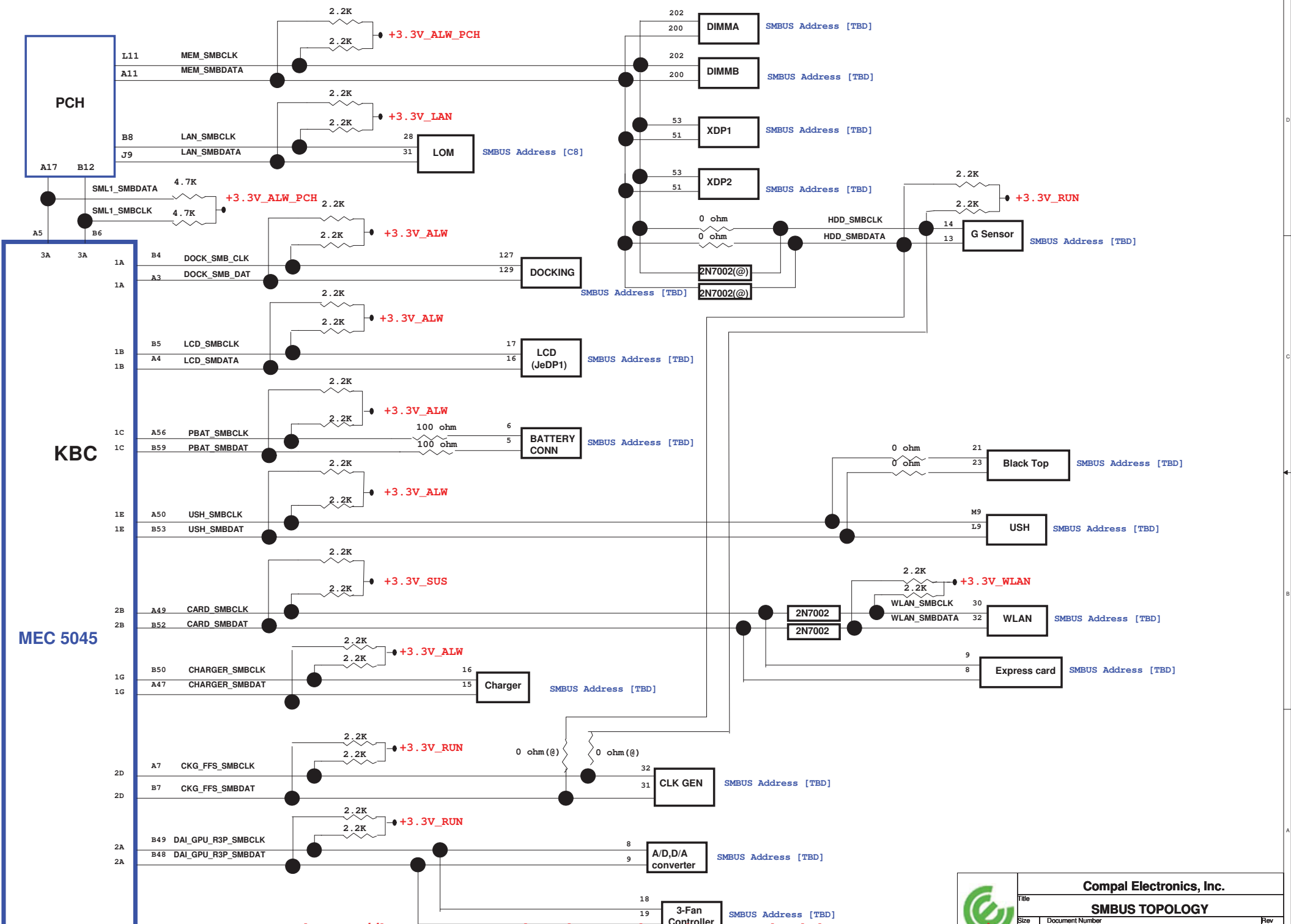
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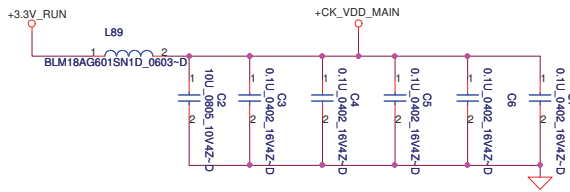
<b>Compal Electronics, Inc.</b>			
<b>Power Rail</b>			
<b>LA-5691P</b>			
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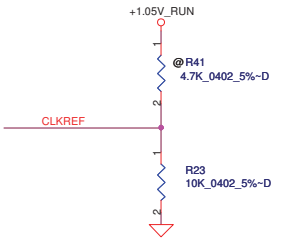
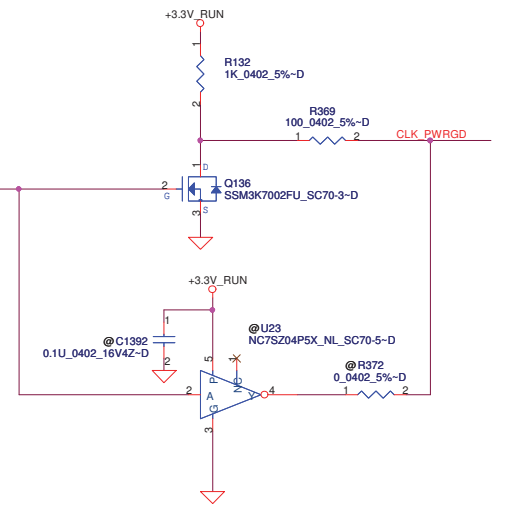
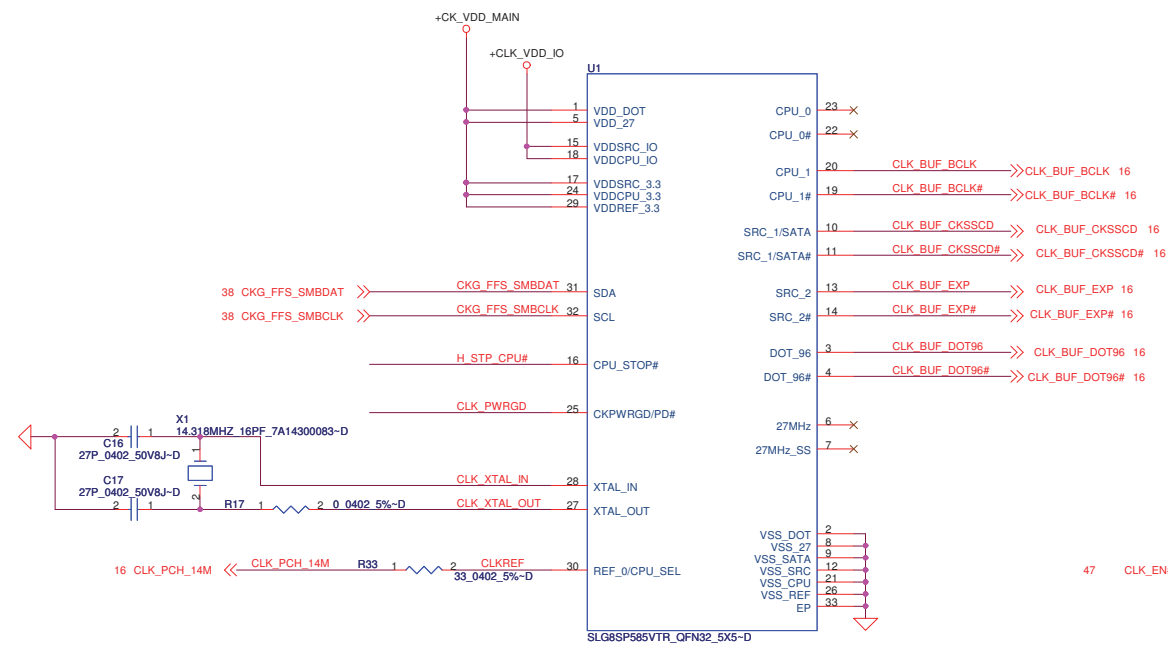
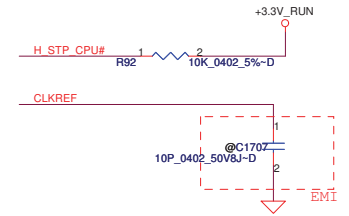
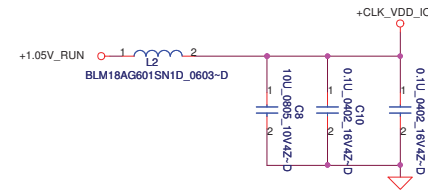


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+CLK\_VDD\_IO CAN BE RANGE FROM 1.05V TO 3V



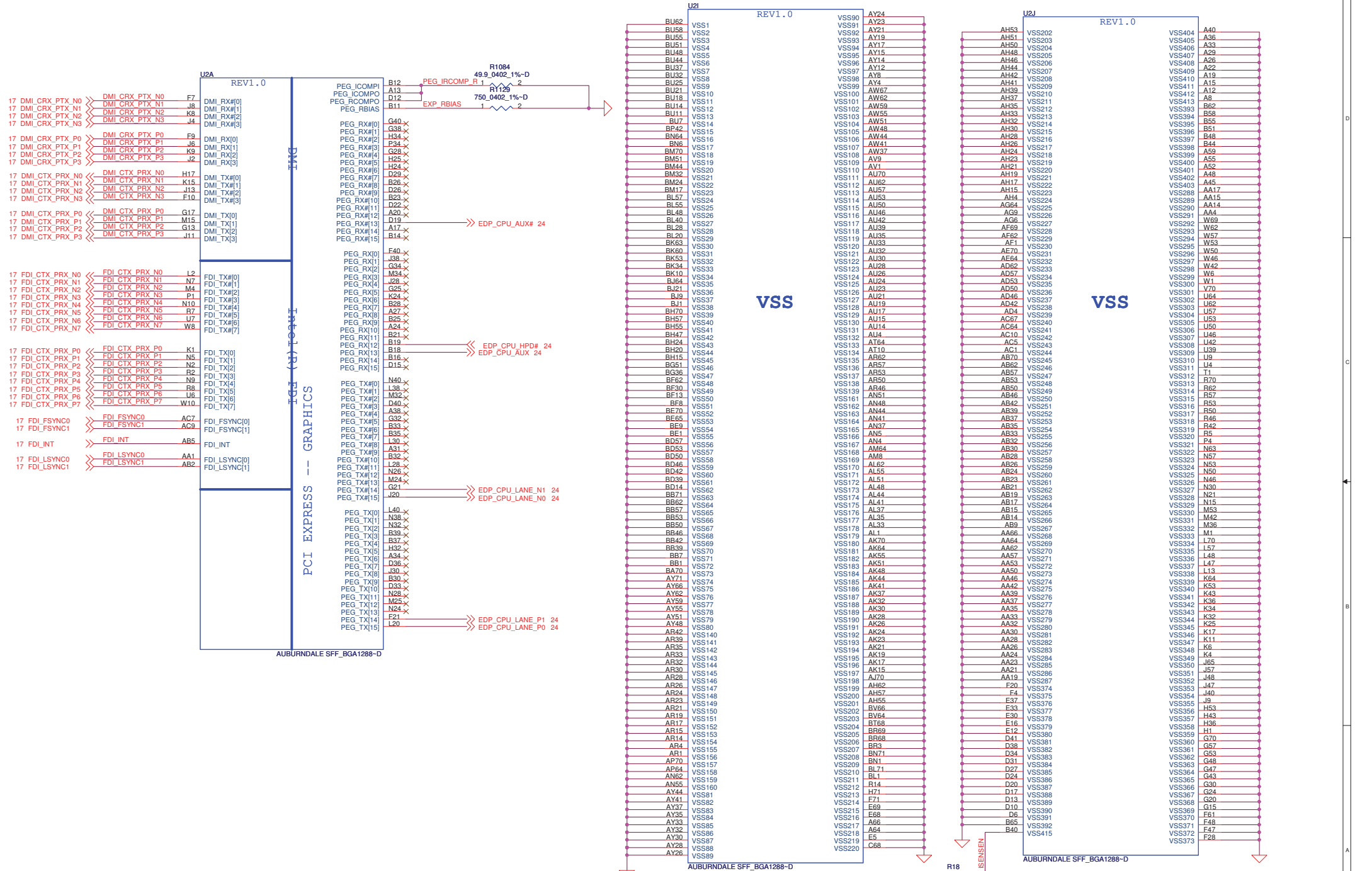
PIN	CPU0	CPU1
1 (0.7~1.5v)	100MHz	100MHz
0 (DEFAULT)	133MHz	133MHz

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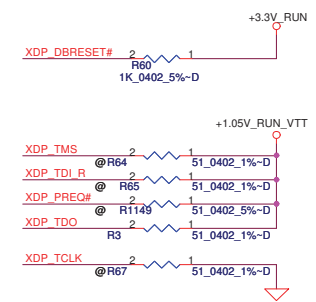
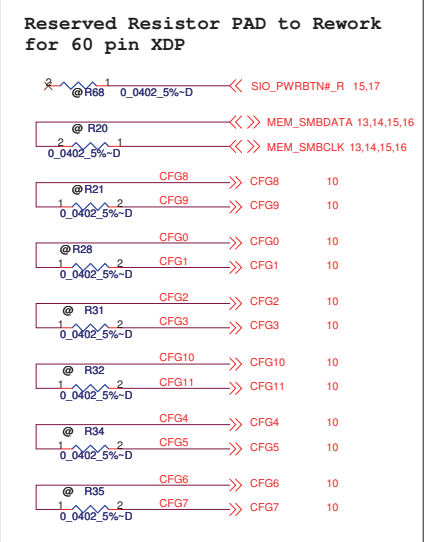
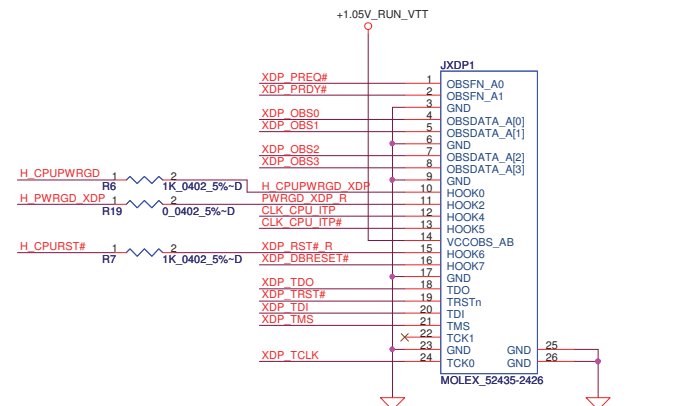
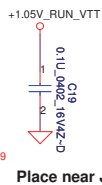
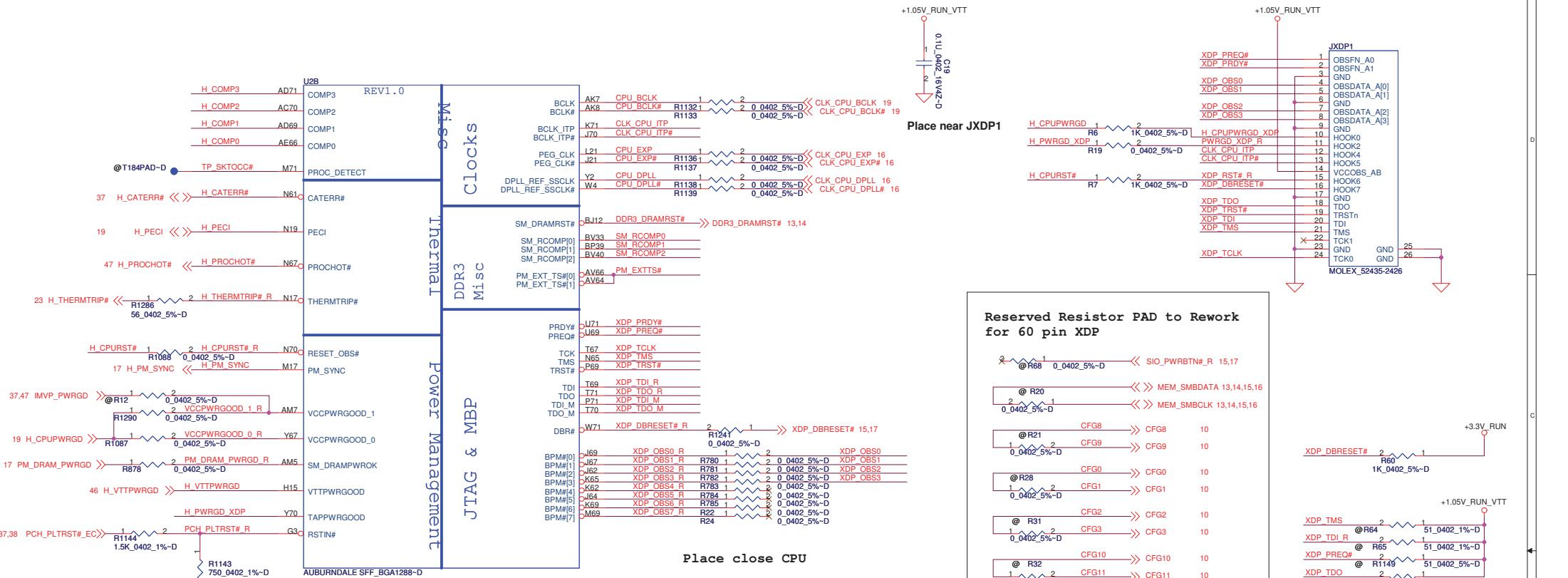
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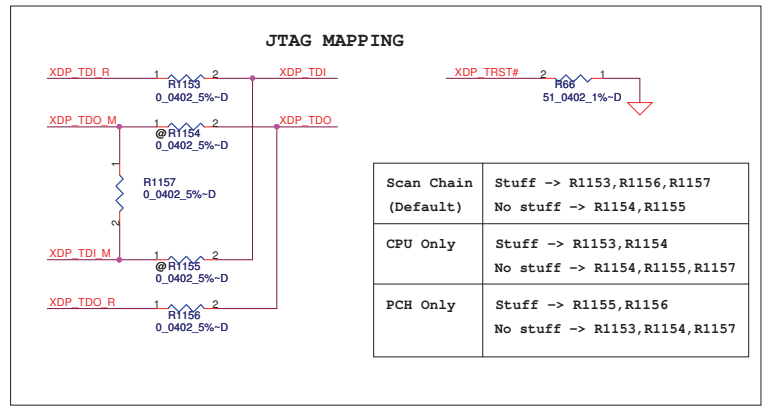
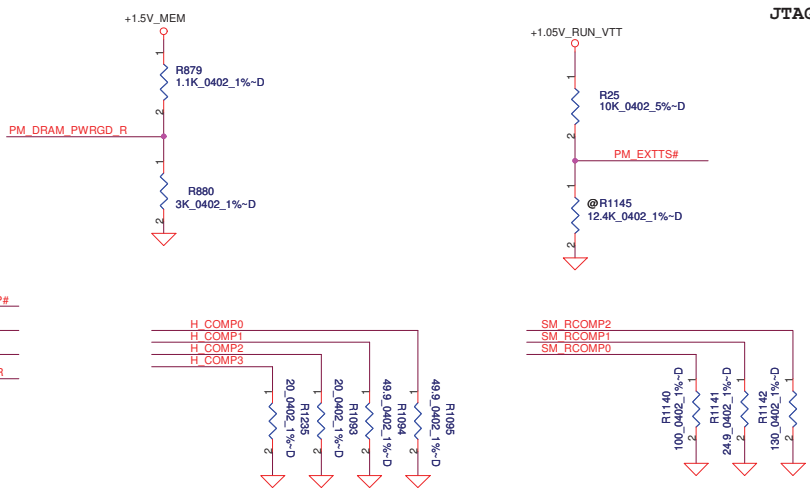
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Place close CPU

JTAG MAPPING



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**LA-5691P**

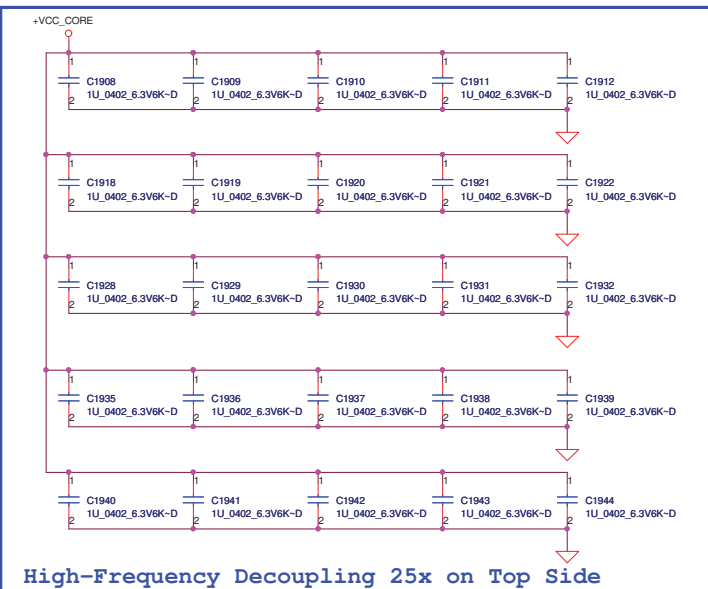
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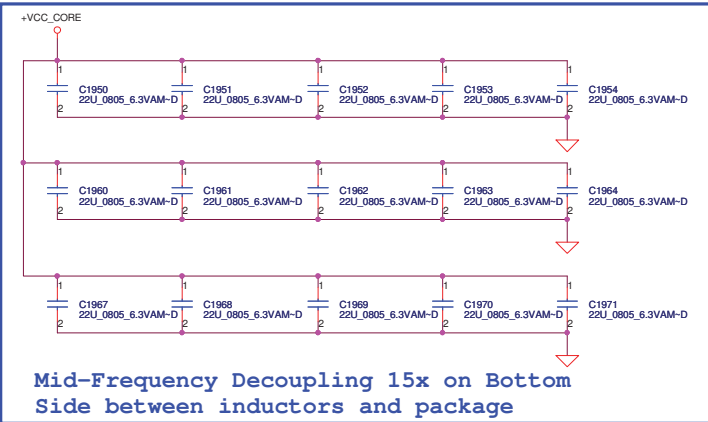




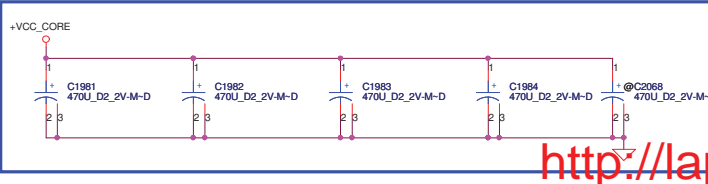




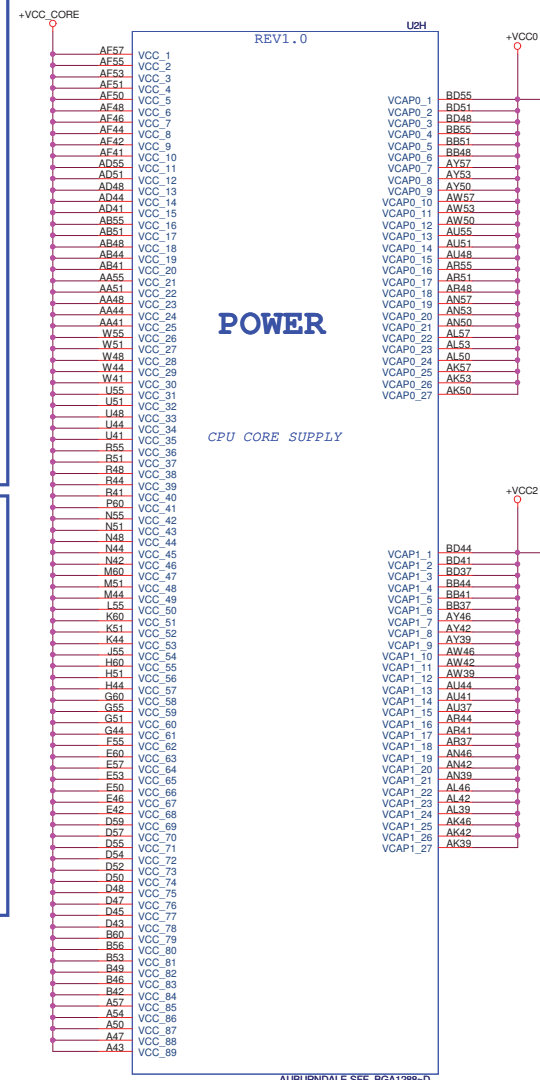
High-Frequency Decoupling 25x on Top Side



Mid-Frequency Decoupling 15x on Bottom Side between inductors and package



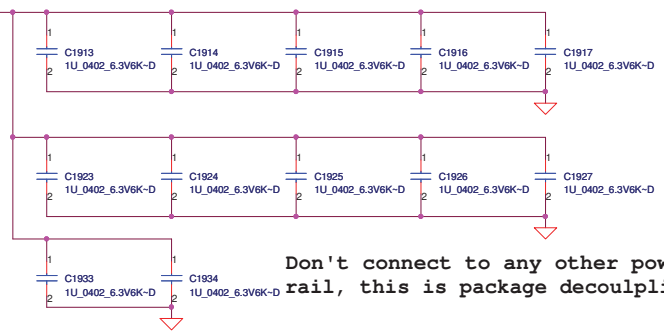
Current =48A



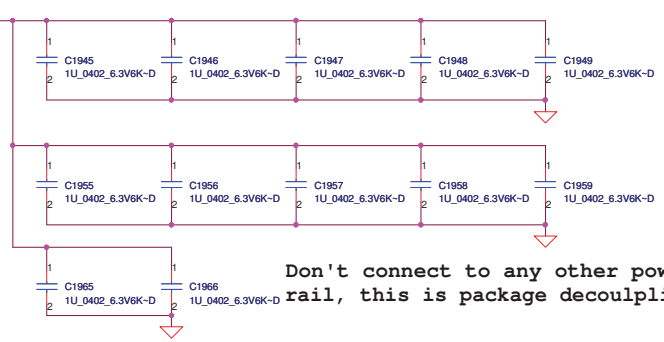
POWER

CPU CORE SUPPLY

AUBURNDALE SFF\_BGA1288-D



Don't connect to any other power rail, this is package decoupling



Don't connect to any other power rail, this is package decoupling

PROCESSOR Power Rail Table (EDS V1.0)

Voltage Rail	Voltage	S0 Iccmax Current (A)
VAXG	1.5	22
VccPLL	1.8	1.35
VCORE	0.75	48
VDDR	1.5	3
VTT	1.05	18

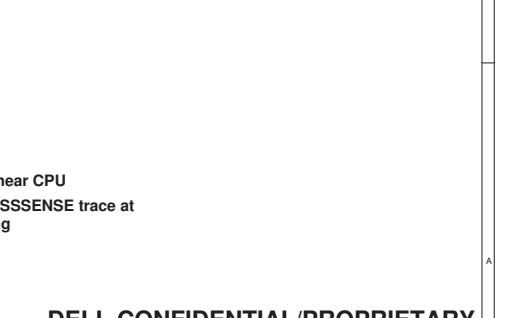
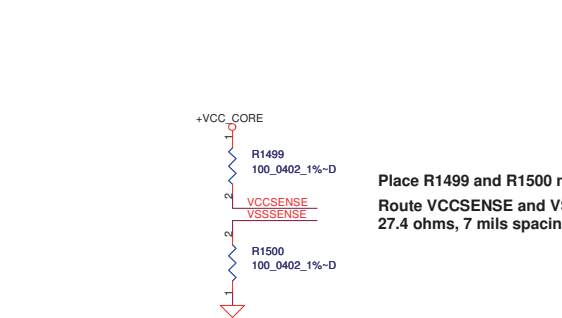
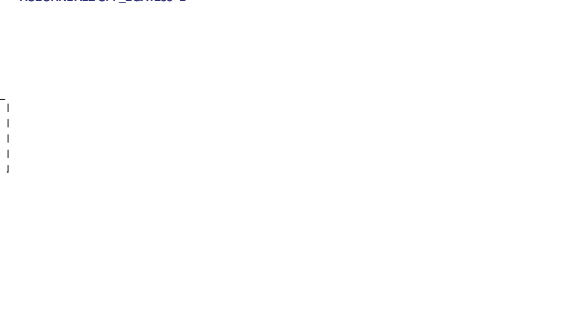
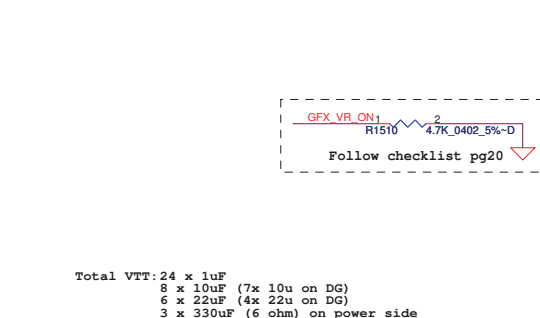
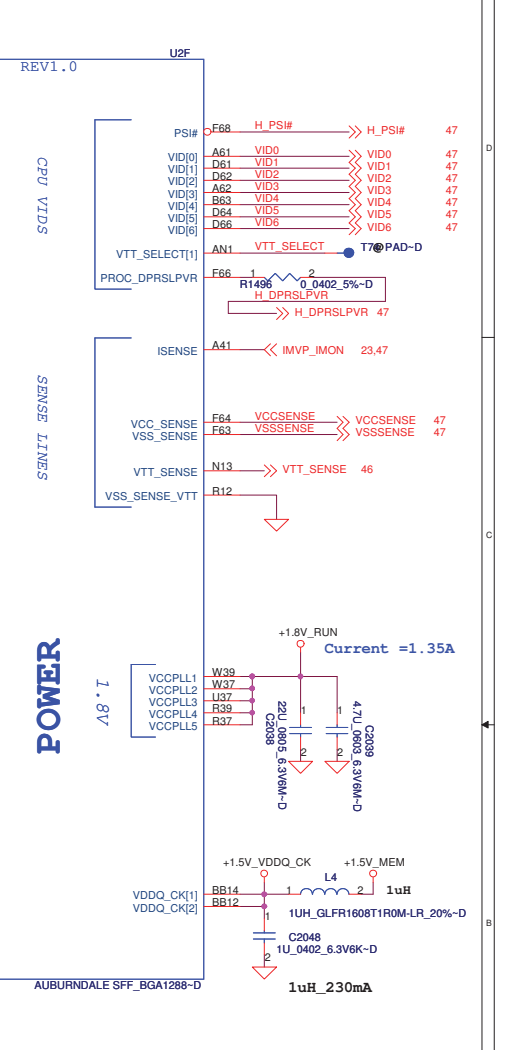
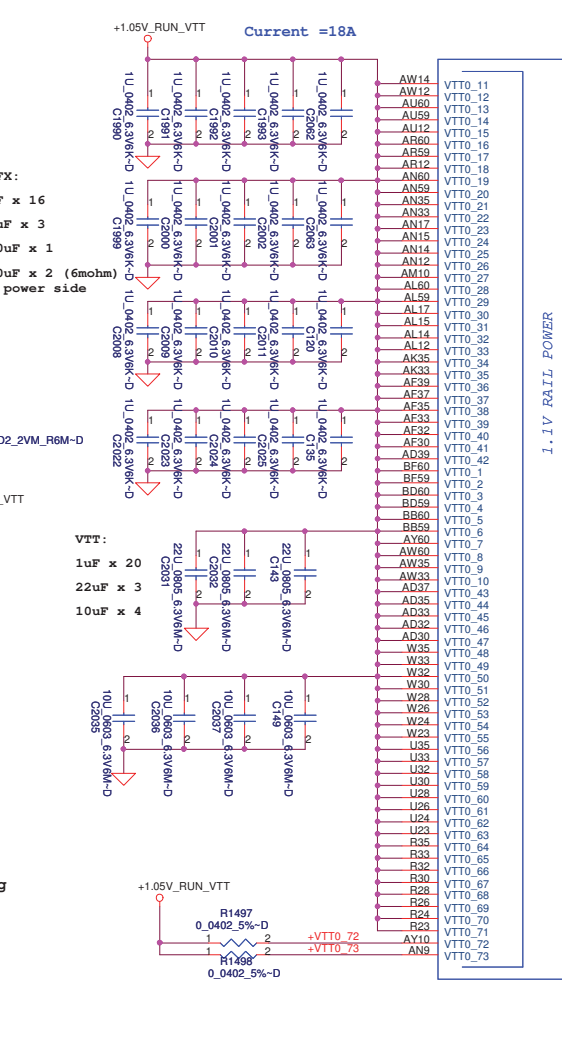
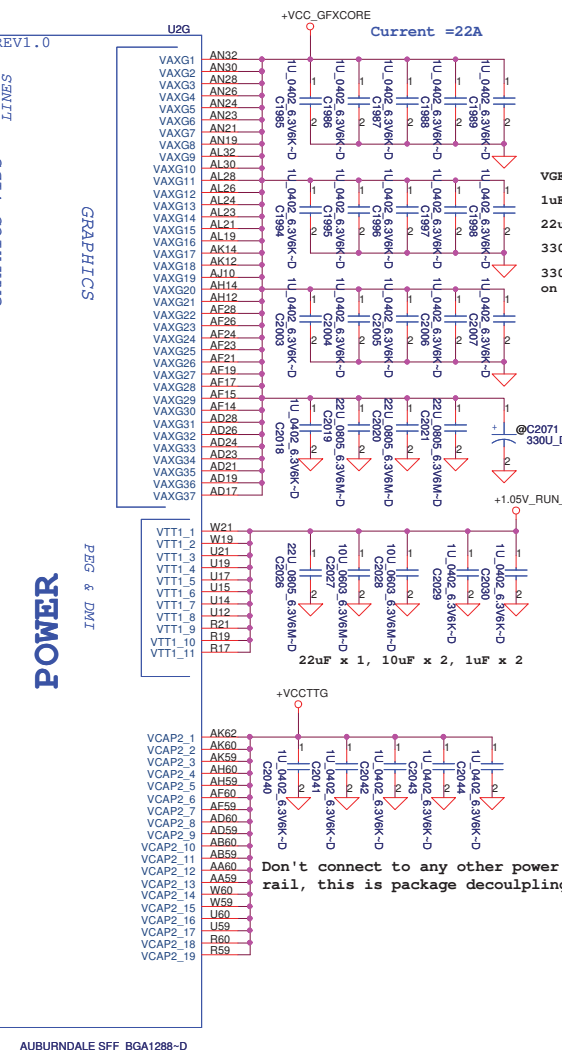
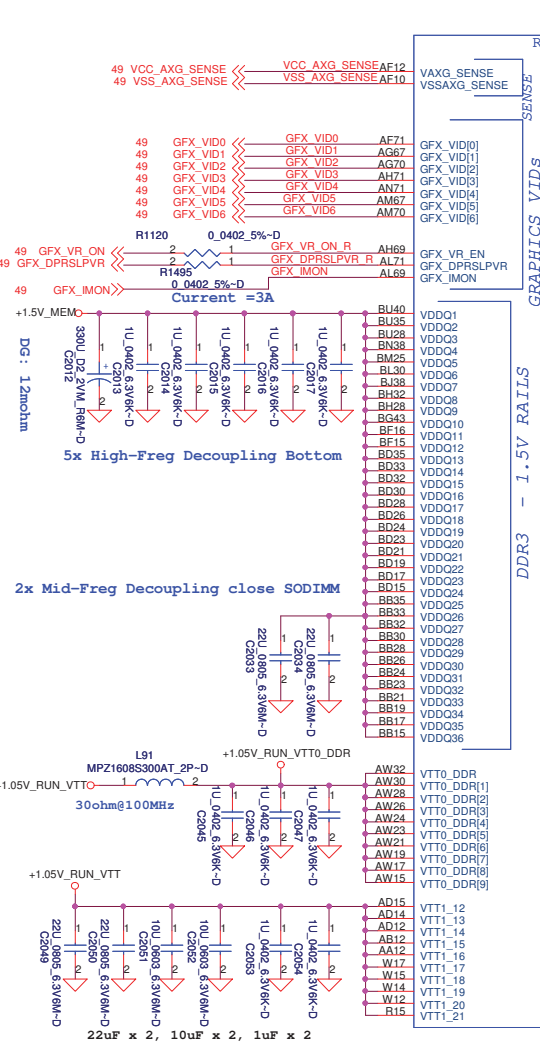
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Total VTT: 24 x 1uF  
 8 x 10uF (7x 10u on DG)  
 6 x 22uF (4x 22u on DG)  
 3 x 330uF (6 ohm) on power side

Follow checklist pg20

Place R1499 and R1500 near CPU  
 Route VCCSENSE and VSSSENSE trace at 27.4 ohms, 7 mils spacing

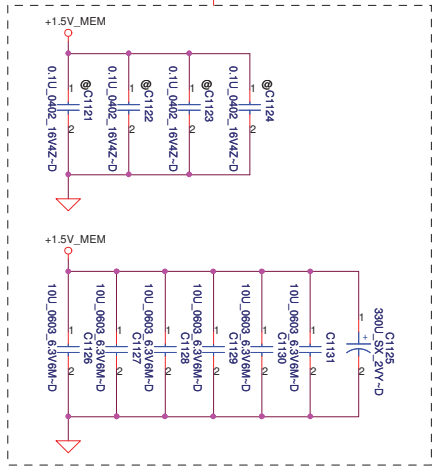
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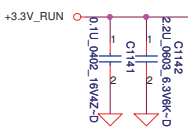
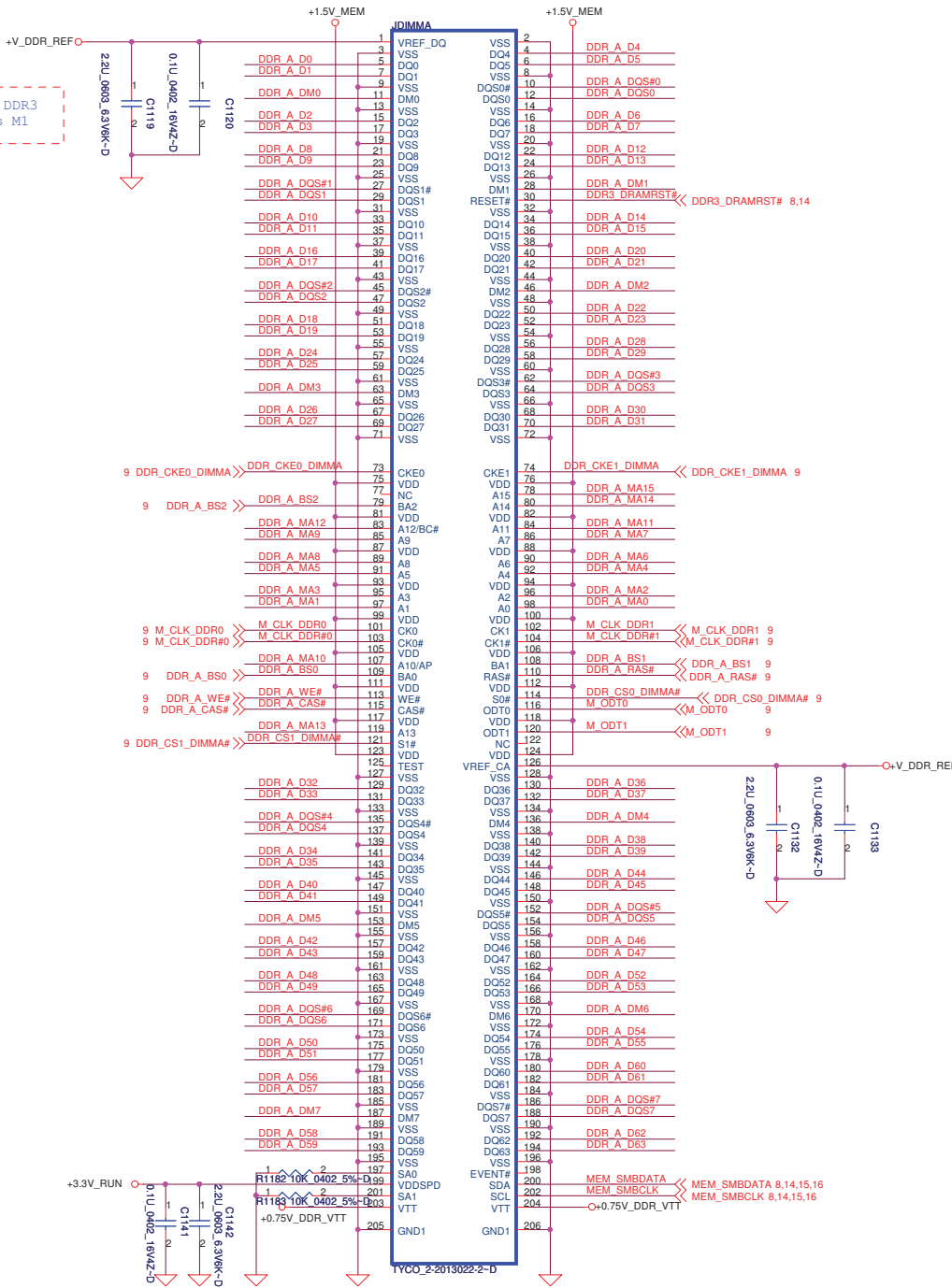
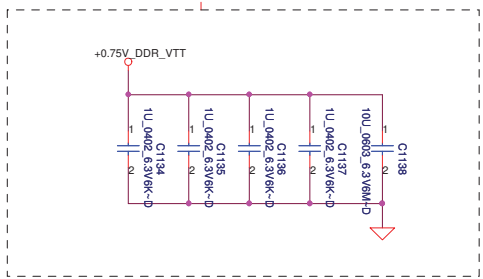
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- 9 DDR\_A\_D[0..63] <<>
- 9 DDR\_A\_DM[0..7] <<>
- 9 DDR\_A\_DQS[0..7] <<>
- 9 DDR\_A\_MA[0..15] <<>

Populate R87 for Intel DDR3  
VREFDQ multiple methods M1

Layout Note:  
Place near JDIMMA



Layout Note:  
Place near JDIMMA.203,204



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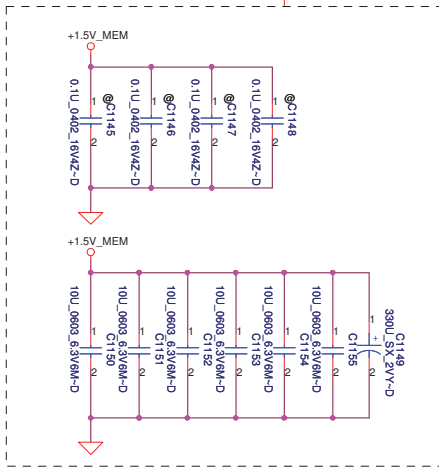


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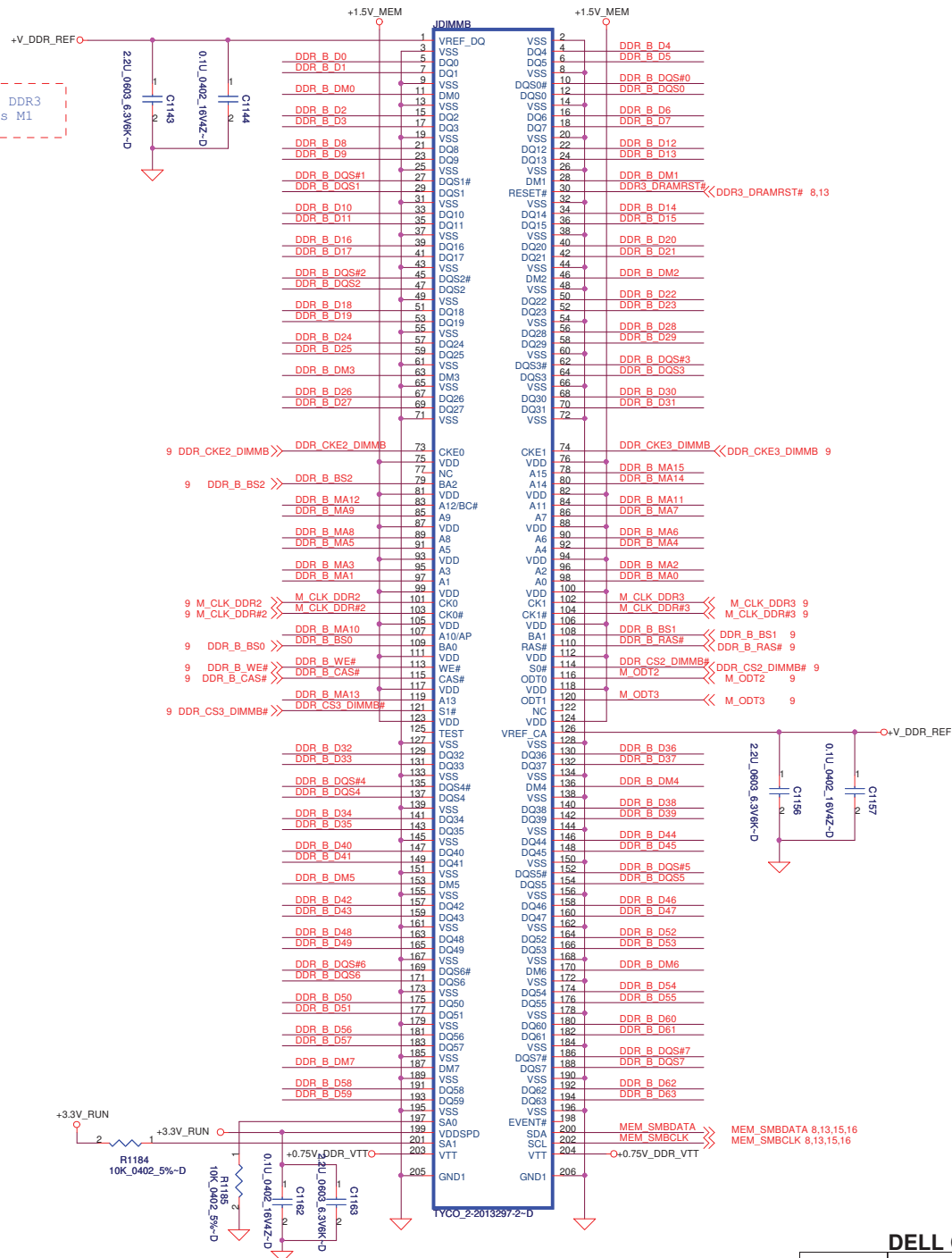
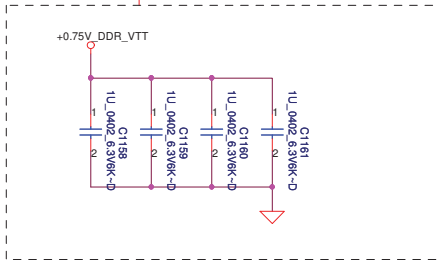
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- 9 DDR\_B\_DM[0..63] <<>
- 9 DDR\_B\_DM[0..7] <<>
- 9 DDR\_B\_DQS[0..7] <<>
- 9 DDR\_B\_MA[0..15] <<>

Populate R88 for Intel DDR3  
VREFDQ multiple methods M1

Layout Note:  
Place near JDIMMB



Layout Note:  
Place near JDIMMB.203,204



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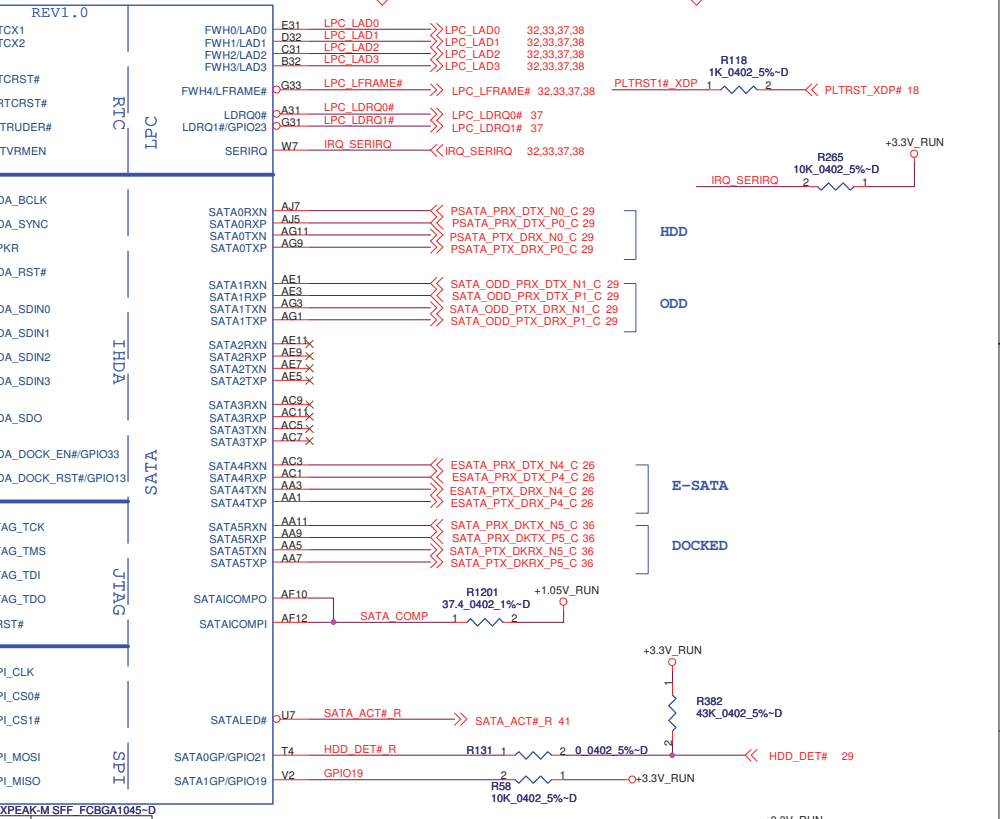
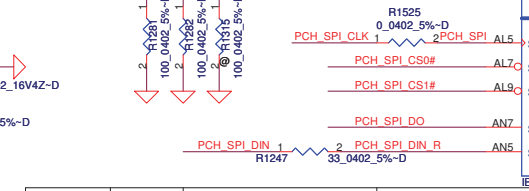
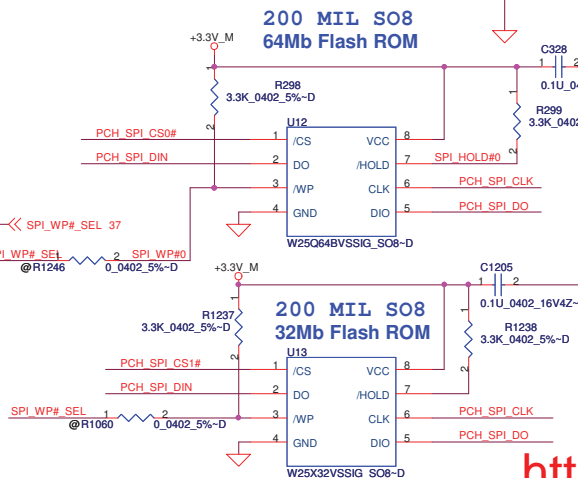
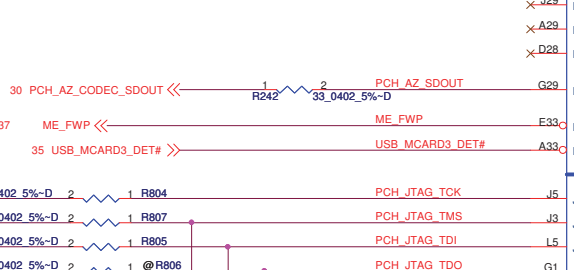
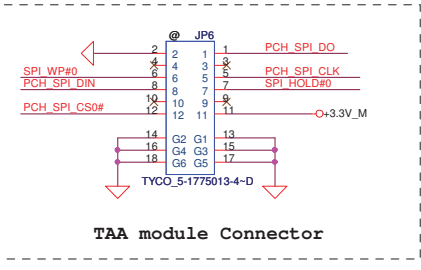
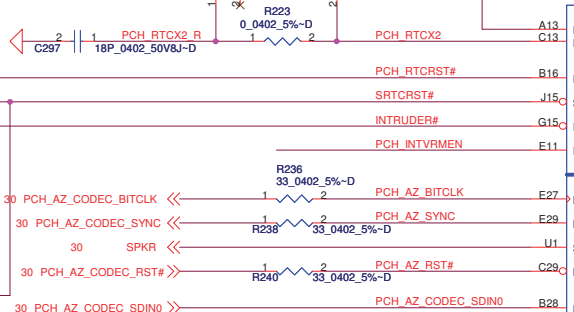
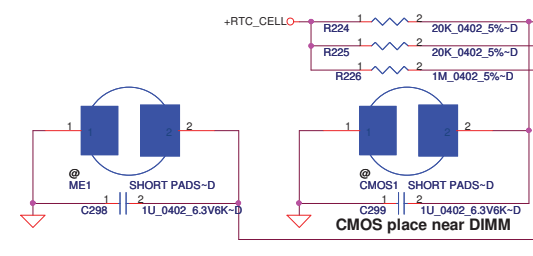
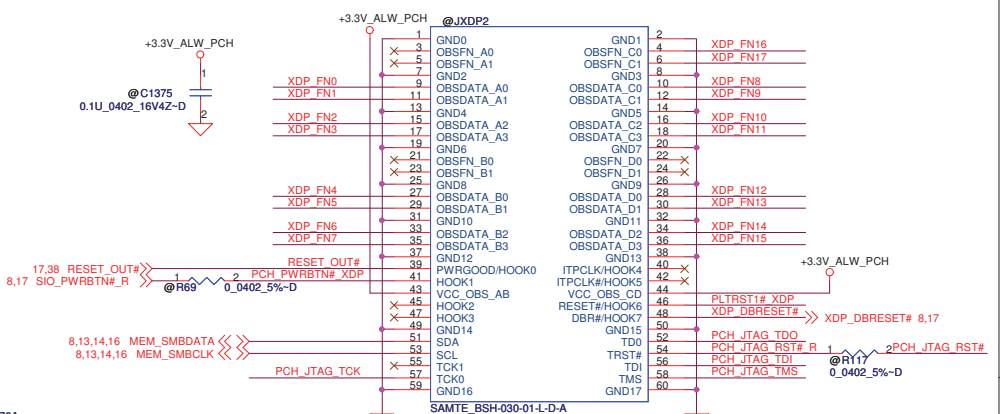
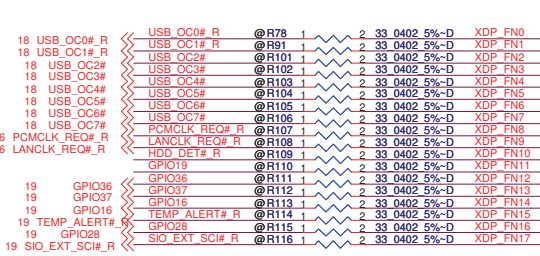
CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers



**INTVRMEN- Integrated SUS**  
 1.1V VRM Enable  
 High - Enable Internal VRs

**On Die PLL VR is supplied by**  
 1.5V when sampled high, 1.8 V  
 when sampled low



PCH Pin	Ref.	PCH JTAG Enable		PCH JTAG Disable		Production
		ES1	ES2	ES1	ES2	
TDO	R806	No Stuff	200 ohm	No Stuff	No Stuff	51 ohm
	R1315	No Stuff	100 ohm	No Stuff	No Stuff	No Stuff
TMS	R807	200 ohm	200 ohm	No Stuff	No Stuff	51 ohm
	R1281	100 ohm	100 ohm	No Stuff	No Stuff	No Stuff
TDI	R805	200 ohm	200 ohm	20K ohm	No Stuff	51 ohm
	R1282	100 ohm	100 ohm	10K ohm	No Stuff	No Stuff
TCK	R804	51 ohm	51 ohm	51 ohm	51 ohm	51 ohm
TRST#	R808	20K ohm	20K ohm	No Stuff	No Stuff	No Stuff

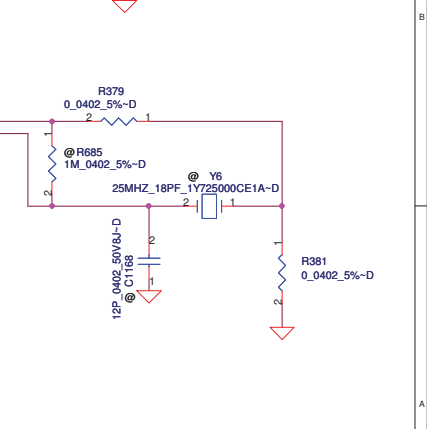
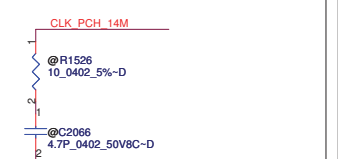
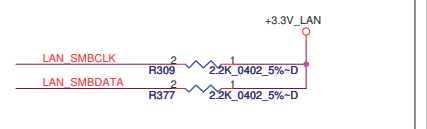
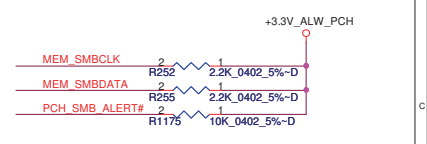
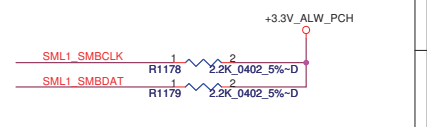
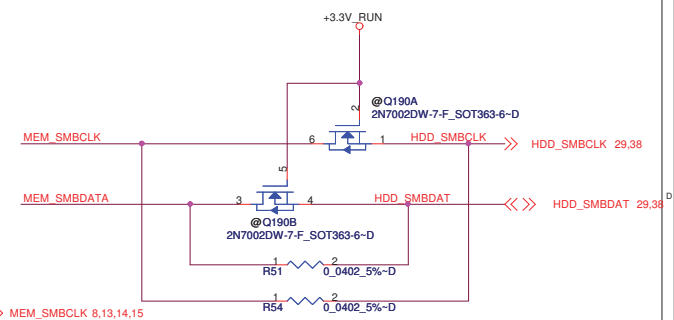
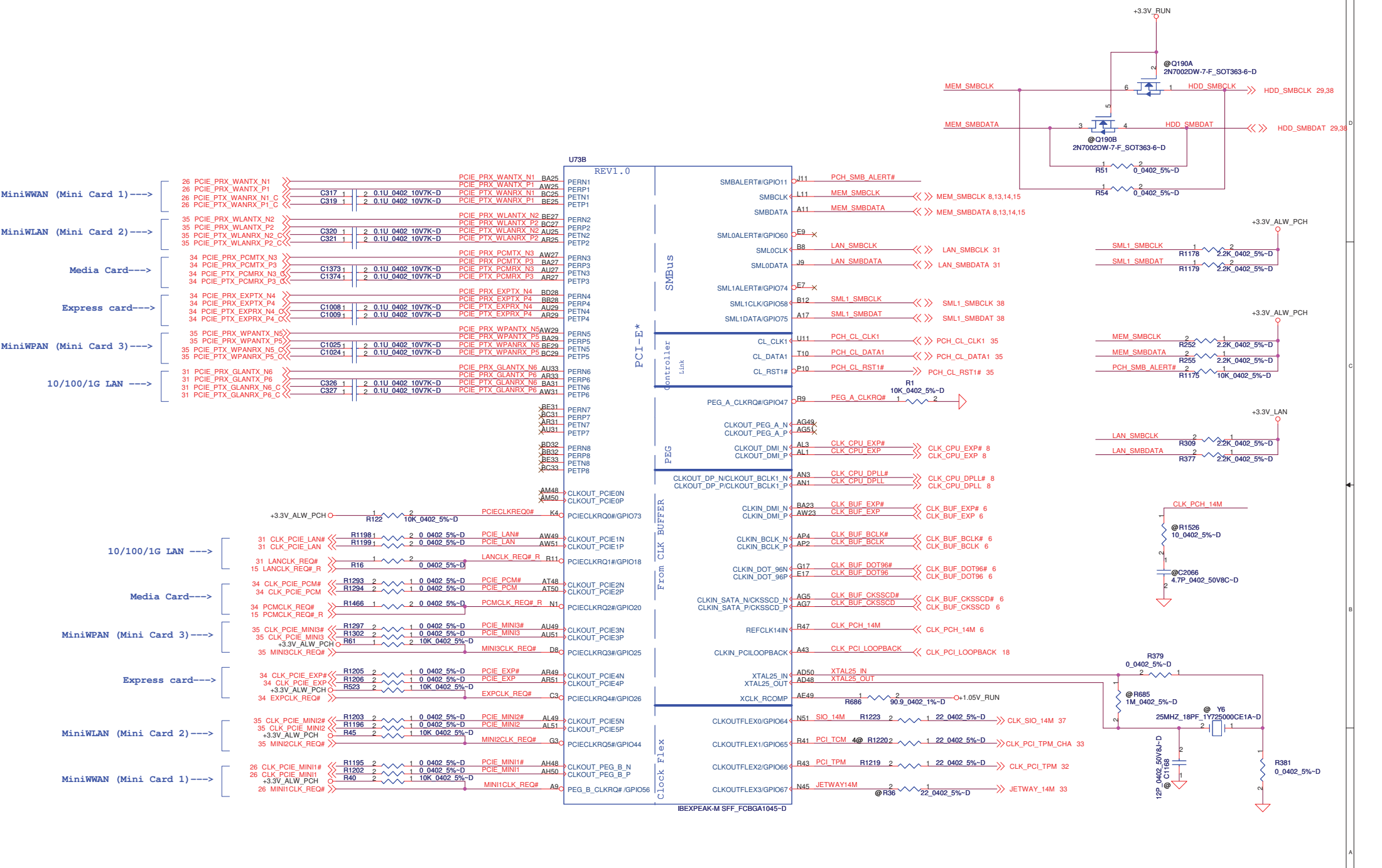
No Reboot Strap  
 Low = Default  
 High = No Reboot

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**PCH (1/8)**

Size: Document Number  
**LA-5691P**  
 Date: Monday, July 13, 2009 Sheet 15 of 51

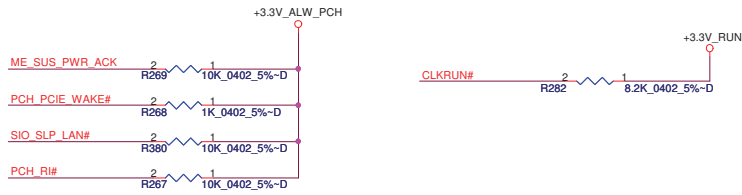


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<b>Compal Electronics, Inc.</b>		
<b>PCH (2/8)</b>		
Size	Document Number	Rev
	<b>LA-5691P</b>	<b>0.1</b>
Date:	Monday, July 13, 2009	Sheet 16 of 51

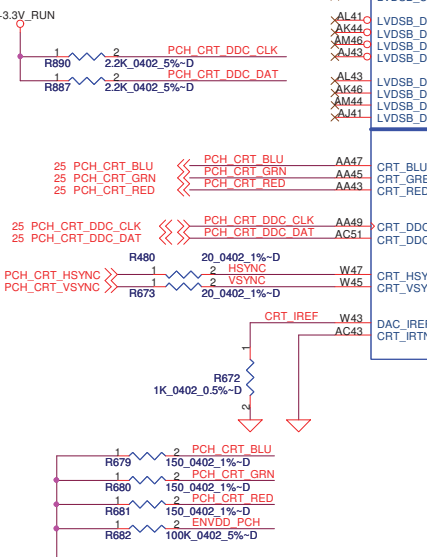
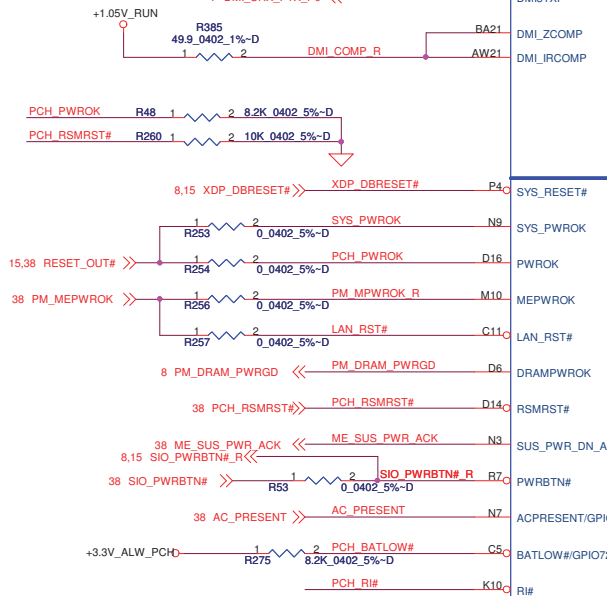
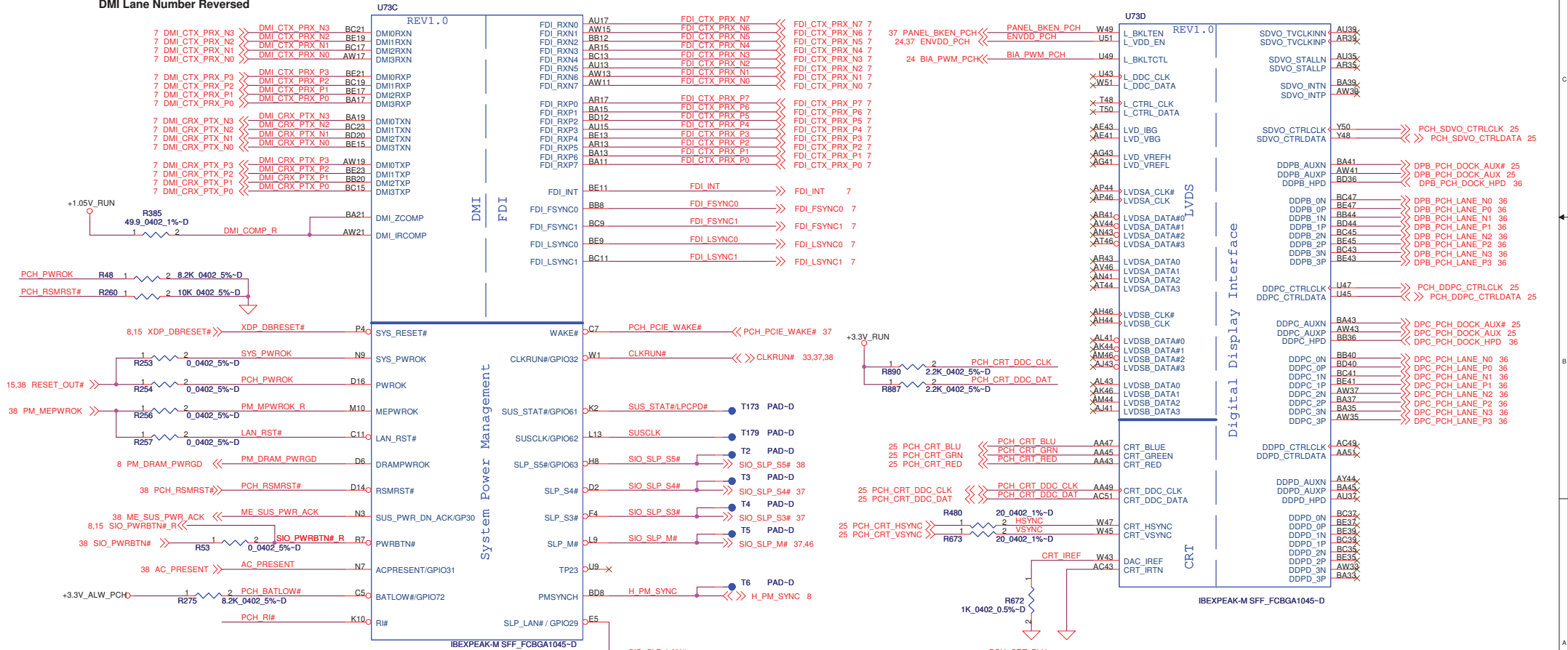
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**DMI Lane Number Reversed**

**FDI Lane Number Reversed**

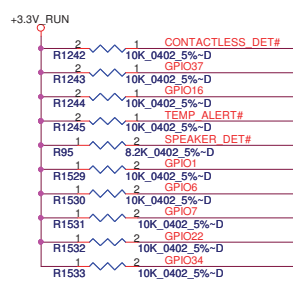
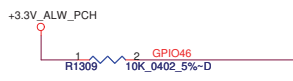
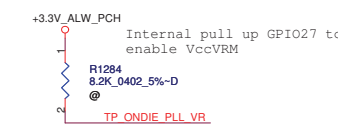
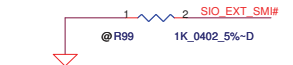
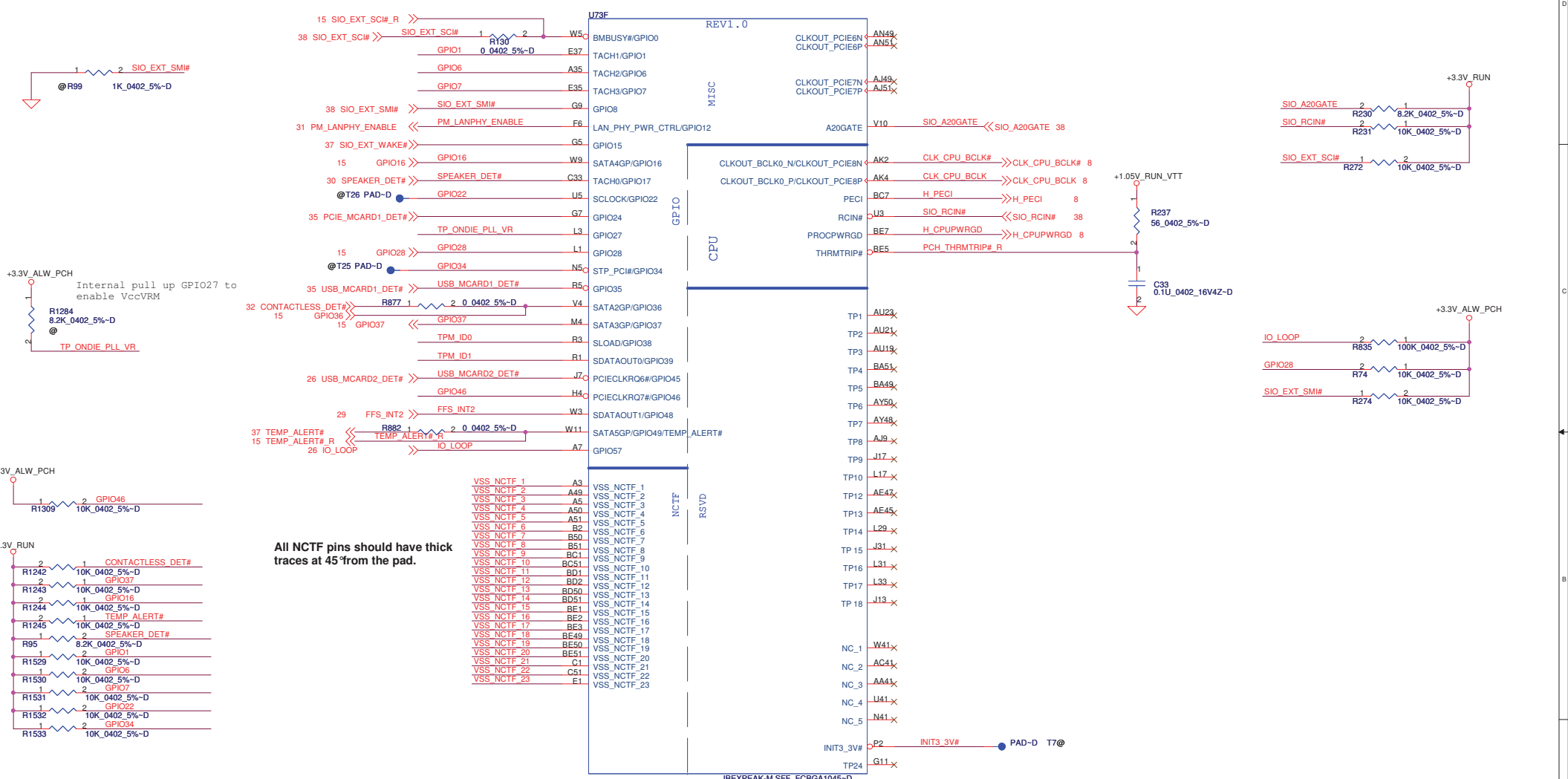


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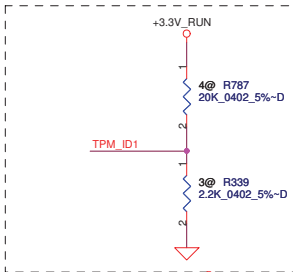
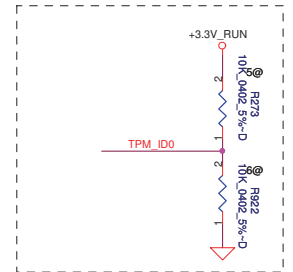


<b>Compal Electronics, Inc.</b>		
<b>PCH (3/8)</b>		
Size	Document Number	Rev
	<b>LA-5691P</b>	0.1
Date:	Monday, July 13, 2009	Sheet 17 of 51





All NCTF pins should have thick traces at 45° from the pad.



	TPM_ID0	TPM_ID1
China TPM	0	0
No TPM, No China TPM	0	1
USH1.0 (For SSI)	1	0
USH2.0	1	1

-----> will use MEMO control pop R339 & de-pop R787 when USH1.0 enable for SSI build only

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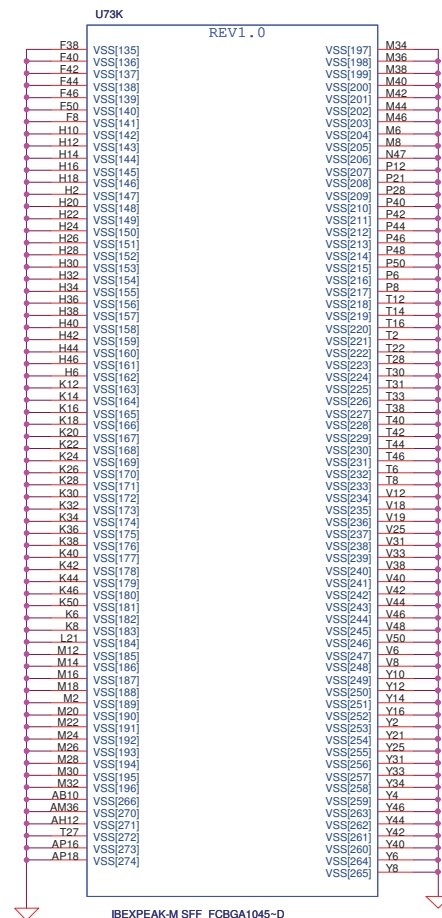
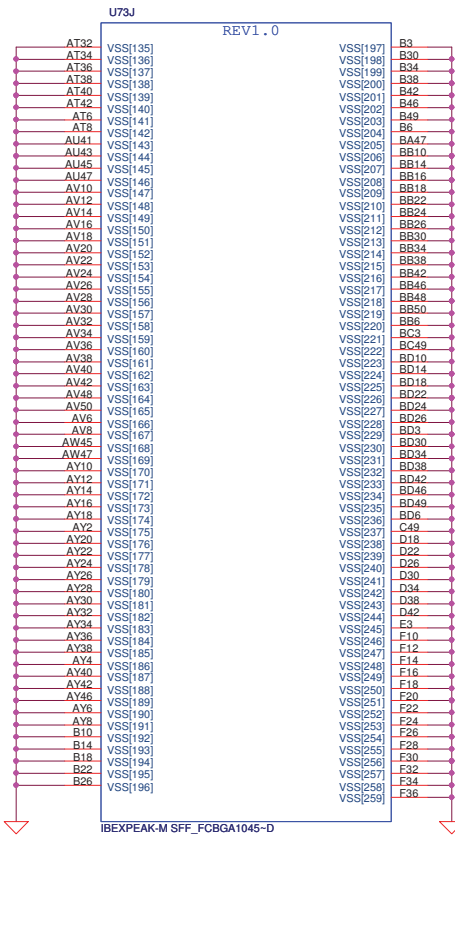
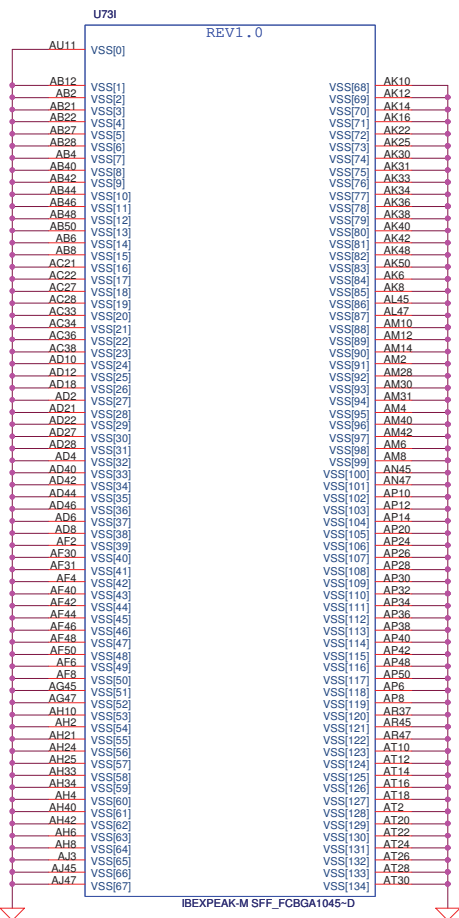
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Size: Document Number LA-5691P Rev 0.1

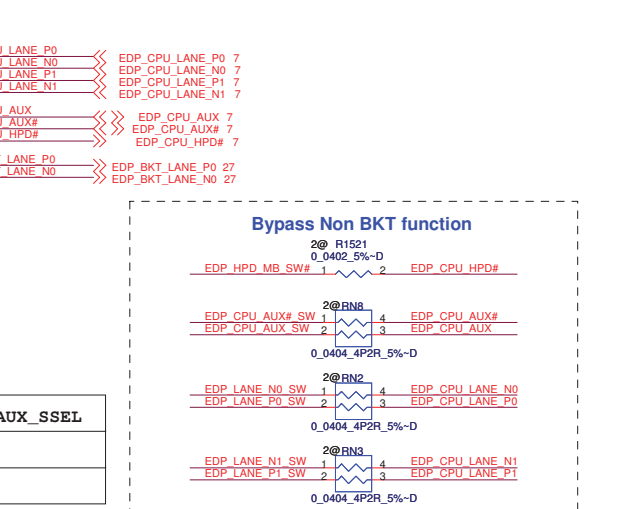
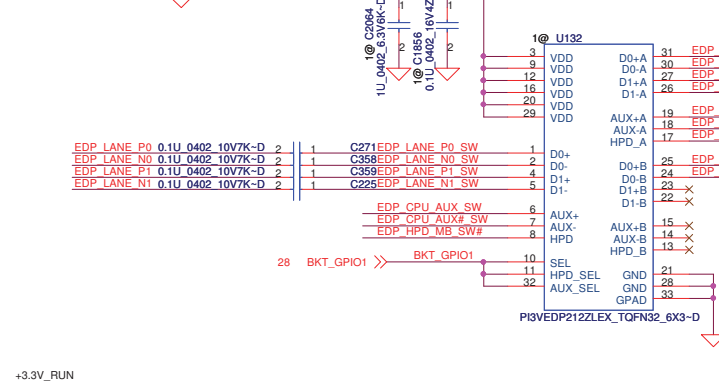
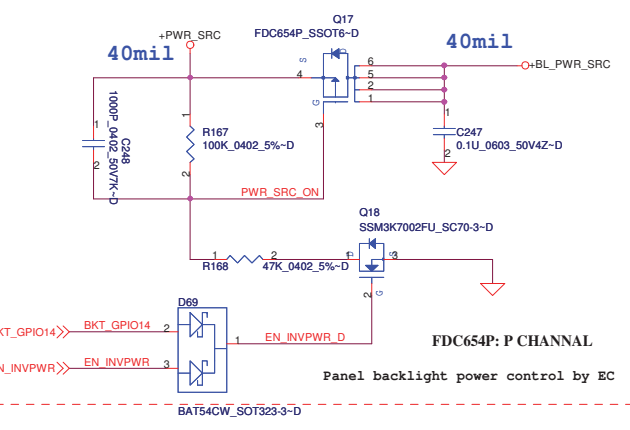
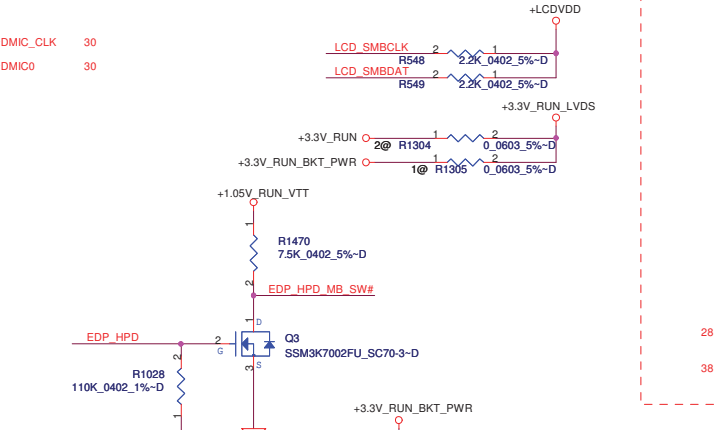
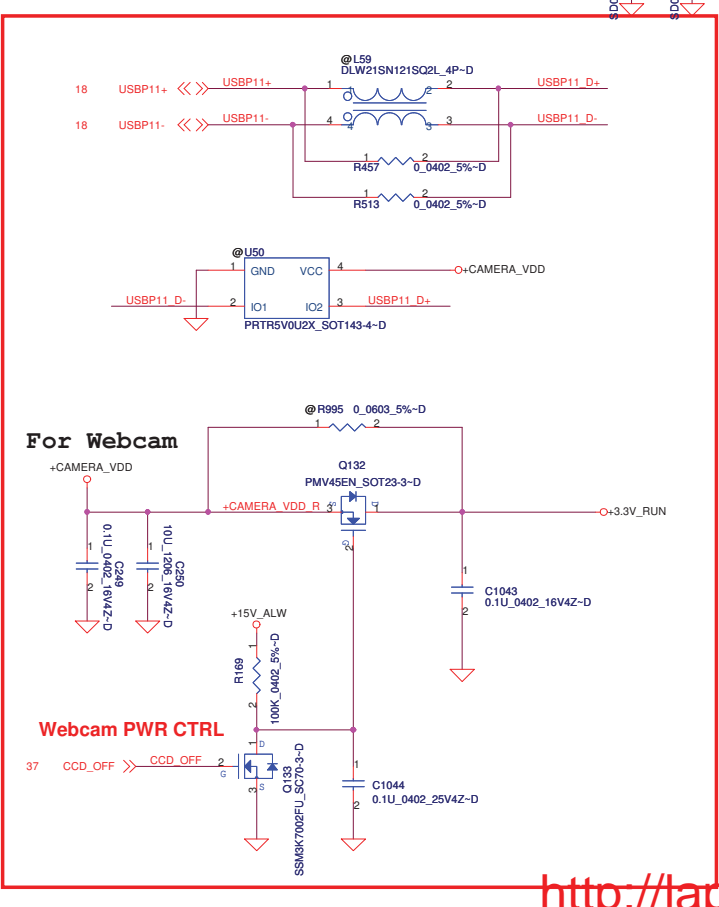
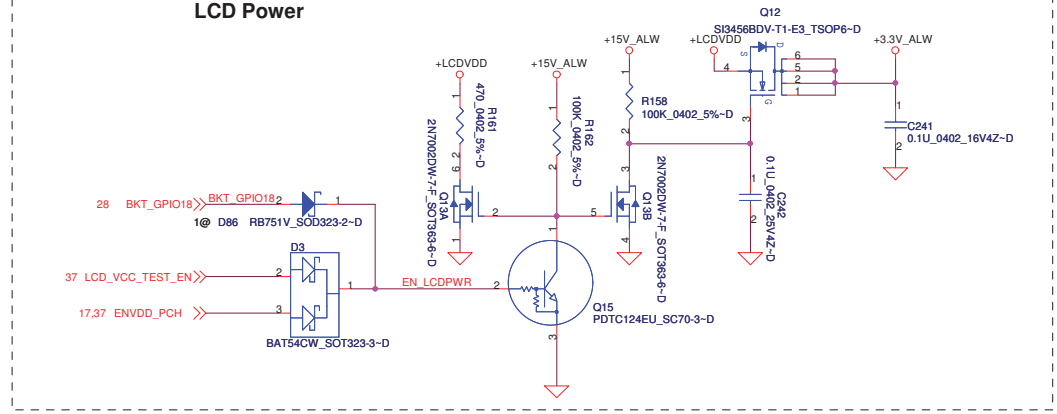
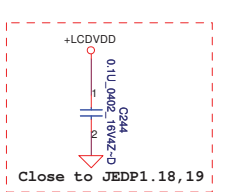
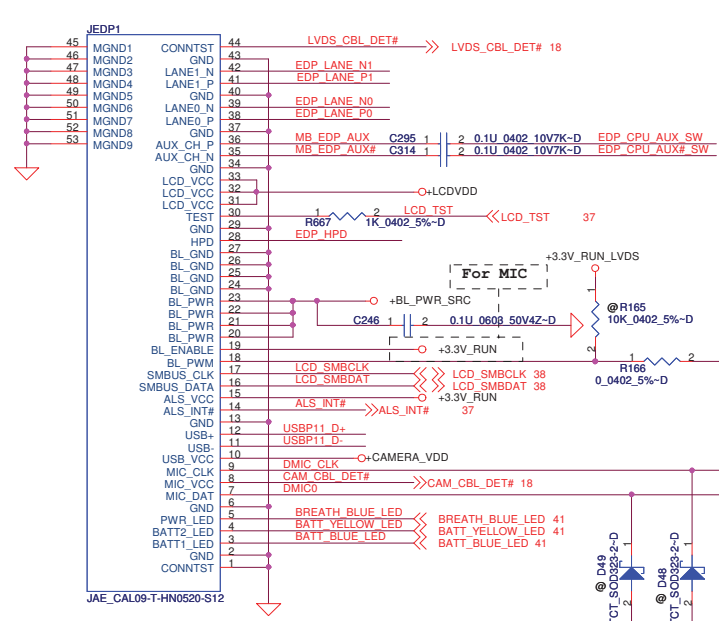
Date: Monday, July 13, 2009 Sheet 19 of 51











Function	SEL/HPD_SEL/AUX_SSEL
Port A active	L
Port B active	H

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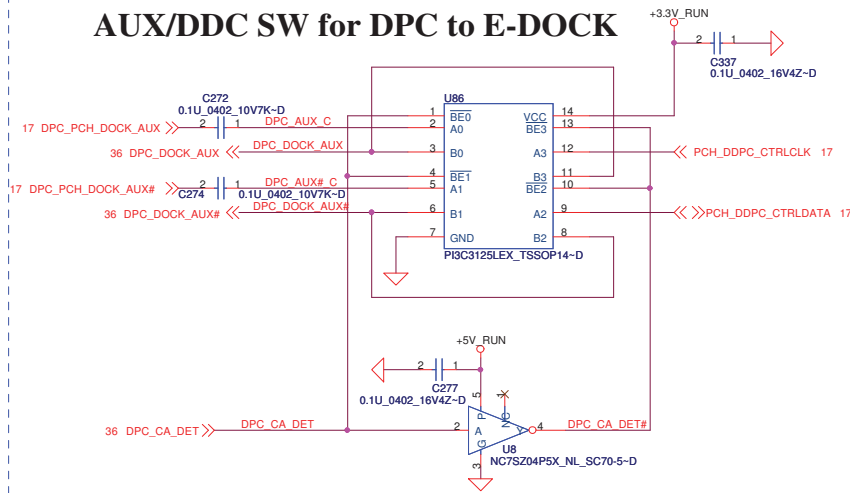
eDP & CAM Conn

LA-5691P  
Date: Monday, July 13, 2009 Sheet 24 of 51

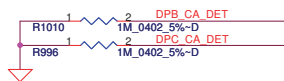
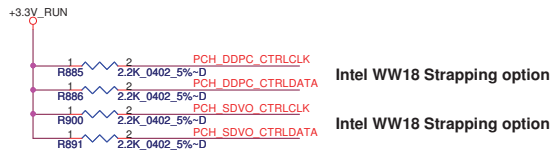
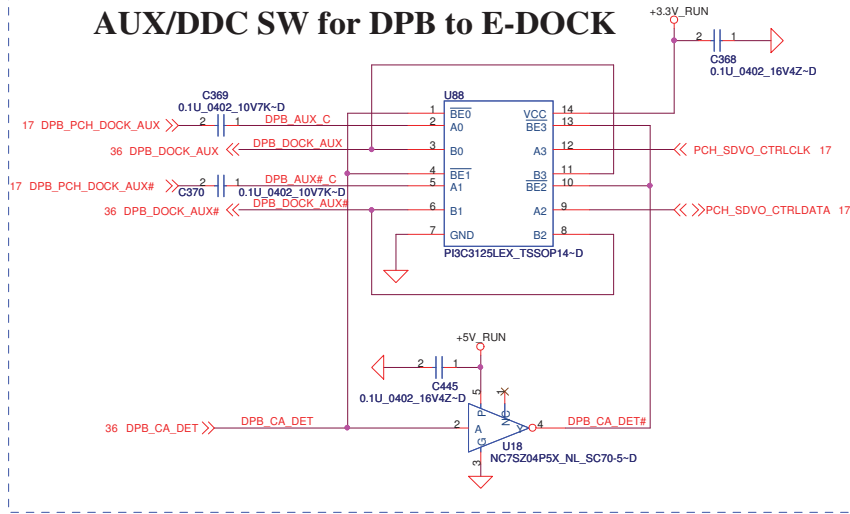
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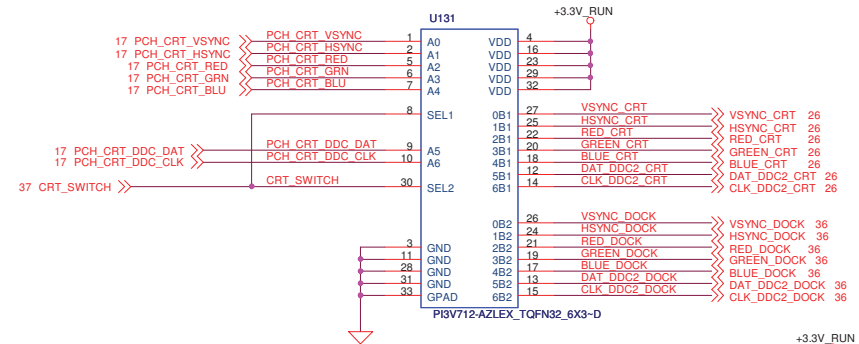
### AUX/DDC SW for DPC to E-DOCK



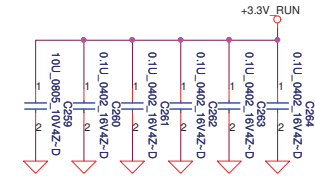
### AUX/DDC SW for DPB to E-DOCK



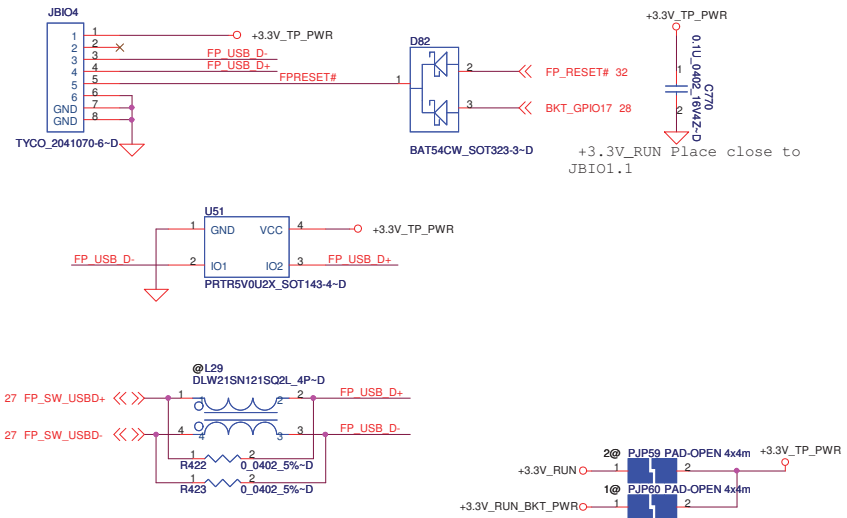
### VGA SW for MB/DOCK



SEL1/SEL2	Chanel	Source
0	A=B1	MB
1	A=B2	APR/SPR



### Fingerprint CONN.

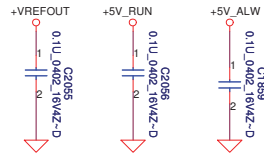


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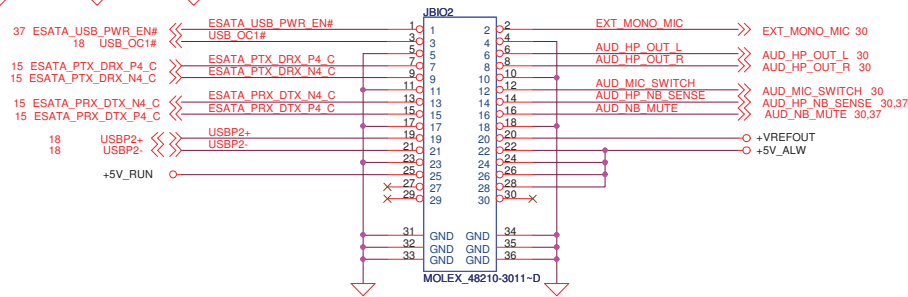
Compal Electronics, Inc.			
Title: DPC DPD SW for DOCK			
Size	Document Number	Rev	
	LA-5691P	0.1	
Date:	Monday, July 13, 2009	Sheet	25 of 51

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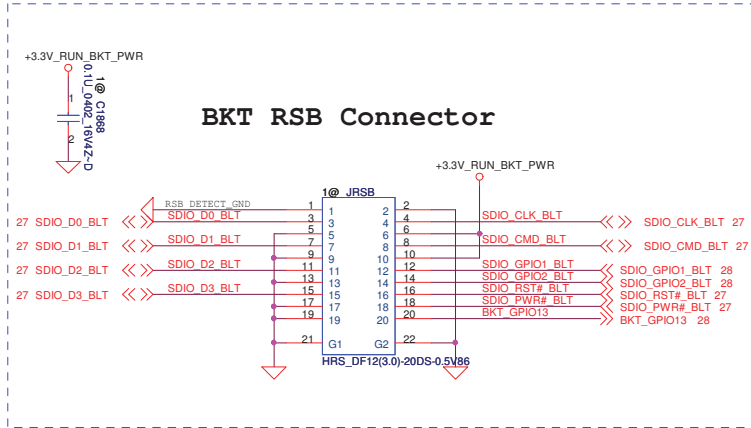
Close to JP1



E-SATA/Jack Connector

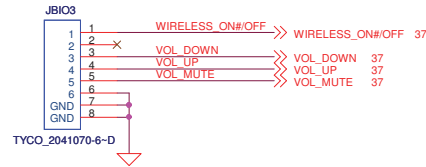


BKT RSB Connector

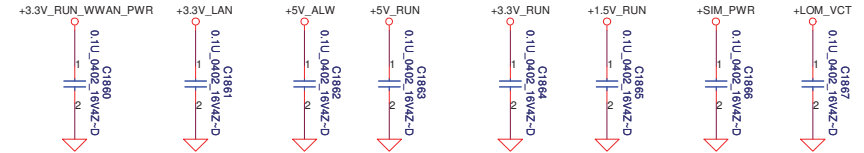
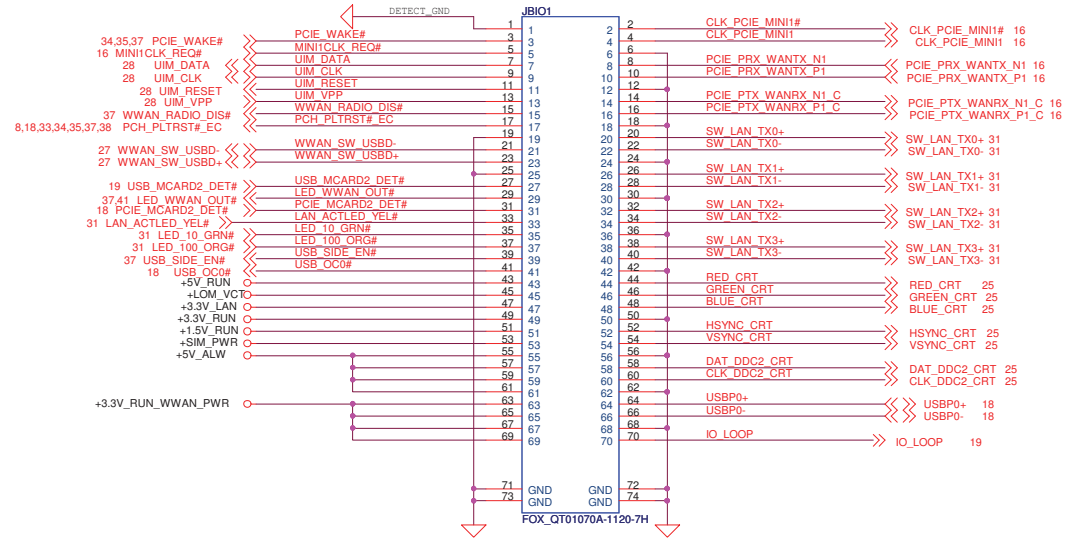


Volume + Sniffer

Change to 6 pins connector



BTB Connector



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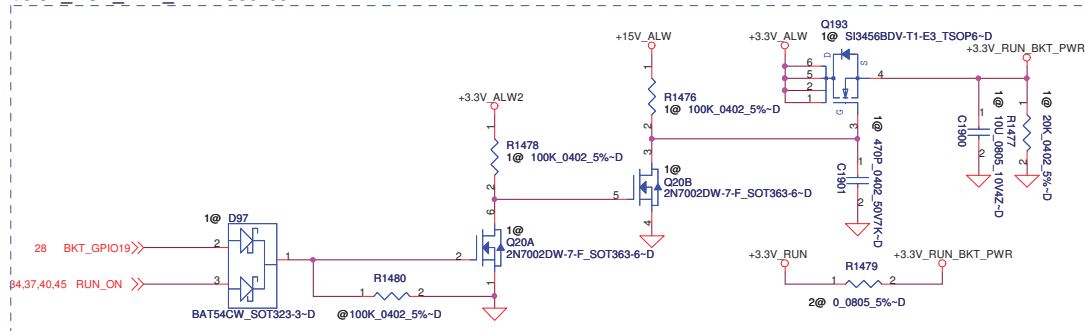
Compal Electronics, Inc.

Title			Display port		
Size	Document Number	LA-5691P		Rev	0.1
Date:	Monday, July 13, 2009	Sheet	26	of	51

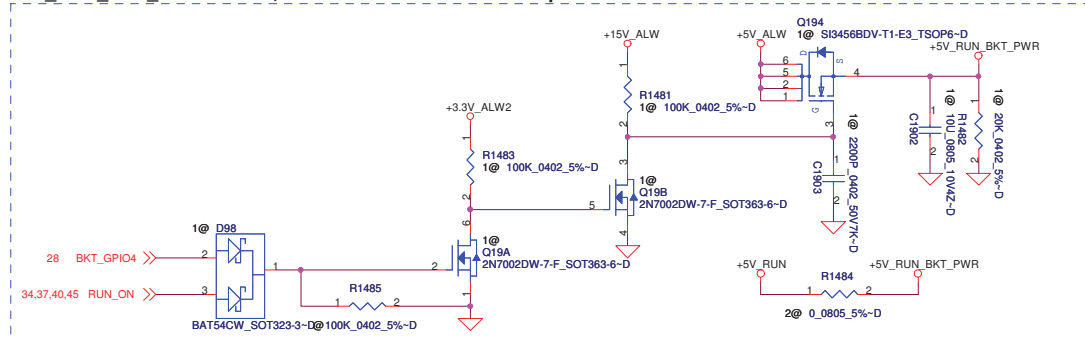
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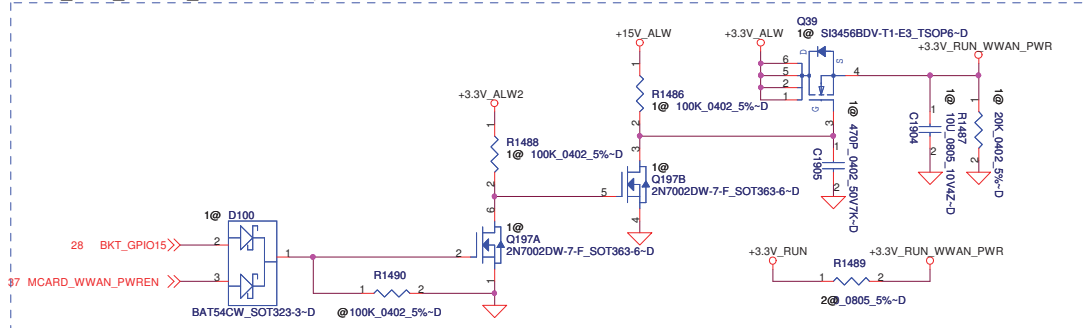
### +3.3V\_RUN\_BKT\_PWR Source



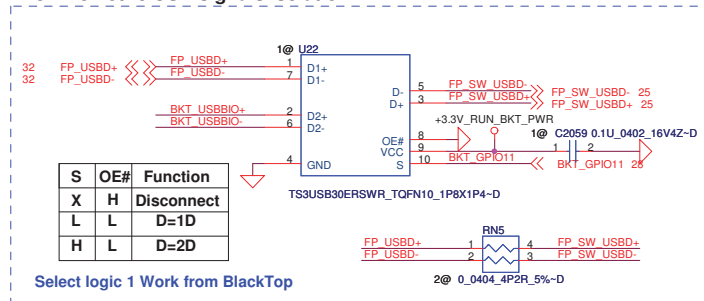
### +5V\_RUN\_BKT\_PWR Source, for Touch Pad and Audio Amplifier



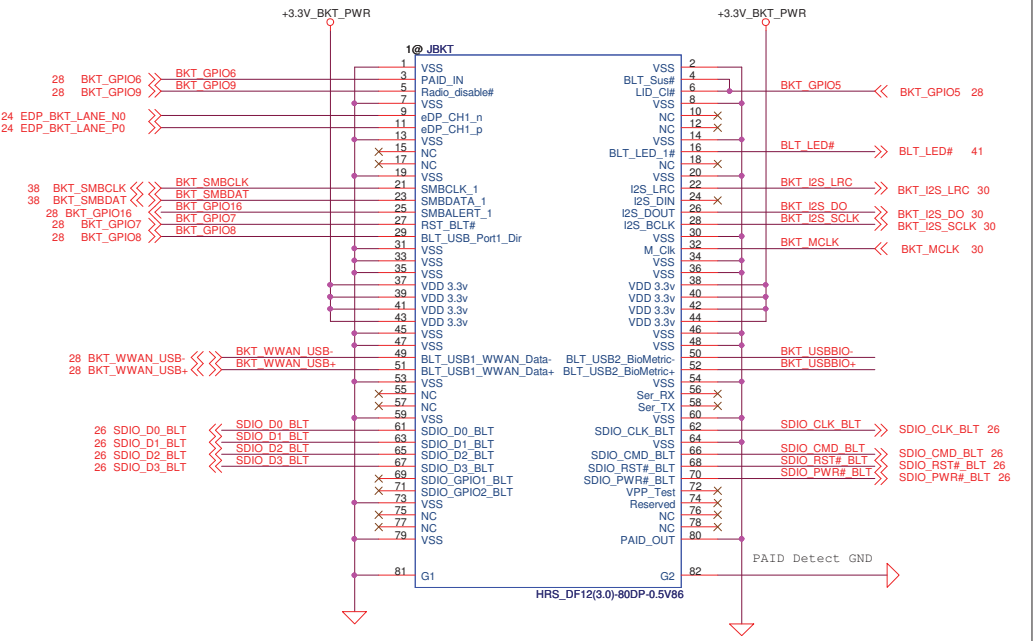
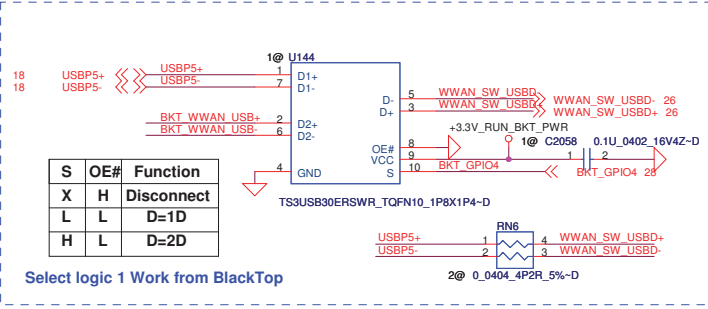
### +3.3V\_RUN\_WWAN\_PWR Source, for WWAN



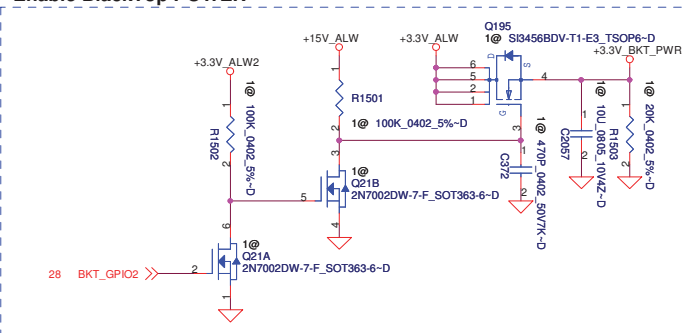
### For Biometric USB signals isolation



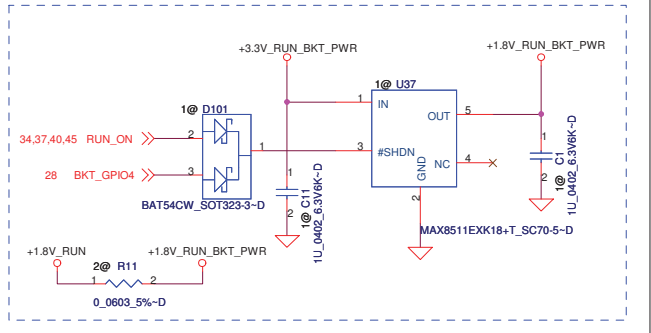
### For WWAN USB signals isolation



### Enable BlackTop POWER



### For Audio I2S



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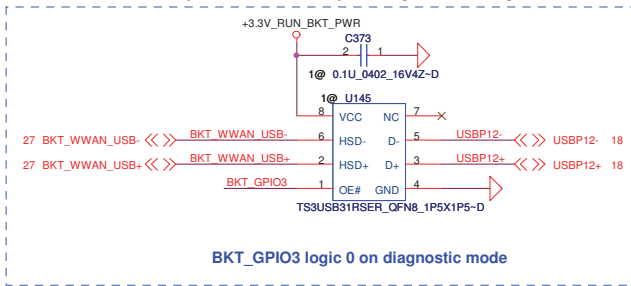
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BlackTop POWER and CONN

LA-5691P  
 Date: Monday, July 13, 2009 Sheet 27 of 51

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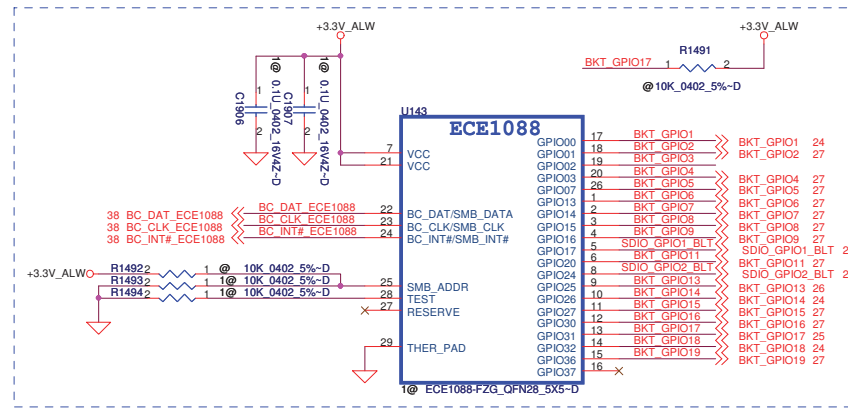
**Add BlackTop to PCH interface by USB signal when diagnostic mode**



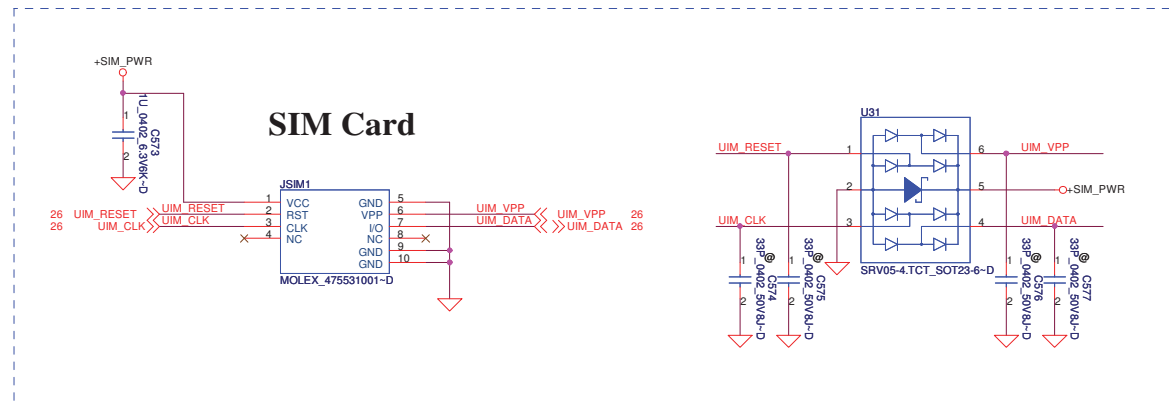
**BKT\_GPIO3 logic 0 on diagnostic mode**

- BKT\_GPIO1 → For eDP signals switch
- BKT\_GPIO2 → For BKT power switch
- BKT\_GPIO3 → For TP power switch&USB signal switch
- BKT\_GPIO4 → For AMP/TP power source&USB signal switch
- BKT\_GPIO5 → For LID\_Closed
- BKT\_GPIO6 → For PAD\_Out
- BKT\_GPIO7 → For BKT Reset
- BKT\_GPIO8 → For USB\_SEL\_BLK
- BKT\_GPIO9 → For Radio\_OFF
- BKT\_GPIO11 → Biometric mux switch
- BKT\_GPIO12 → For WLAN antenna mux control
- BKT\_GPIO13 → RSB\_DET#
- BKT\_GPIO14 → For Inverter Power
- BKT\_GPIO15 → For WWAN Power
- BKT\_GPIO16 → For SMBALERT
- BKT\_GPIO17 → For Biometric reset signal
- BKT\_GPIO18 → For LVDS Power switch
- BKT\_GPIO19 → For TP Power

**GPIO Expander for BlackTop**



**SIM Card**



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Title: **Braidwood/ SATA repeater & PCIE SATA SW**

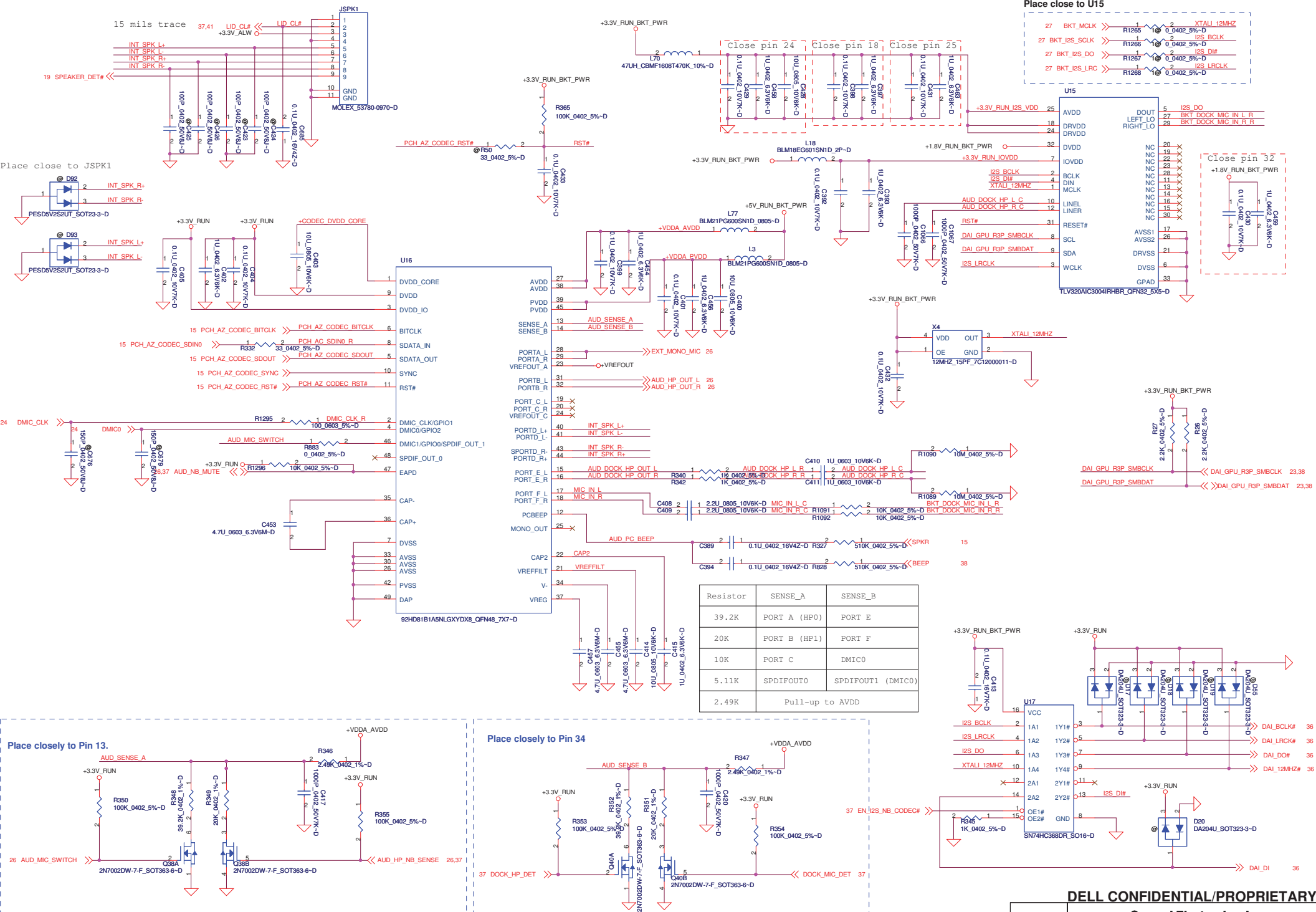
Size: **LA-5691P** Rev: **0.1**

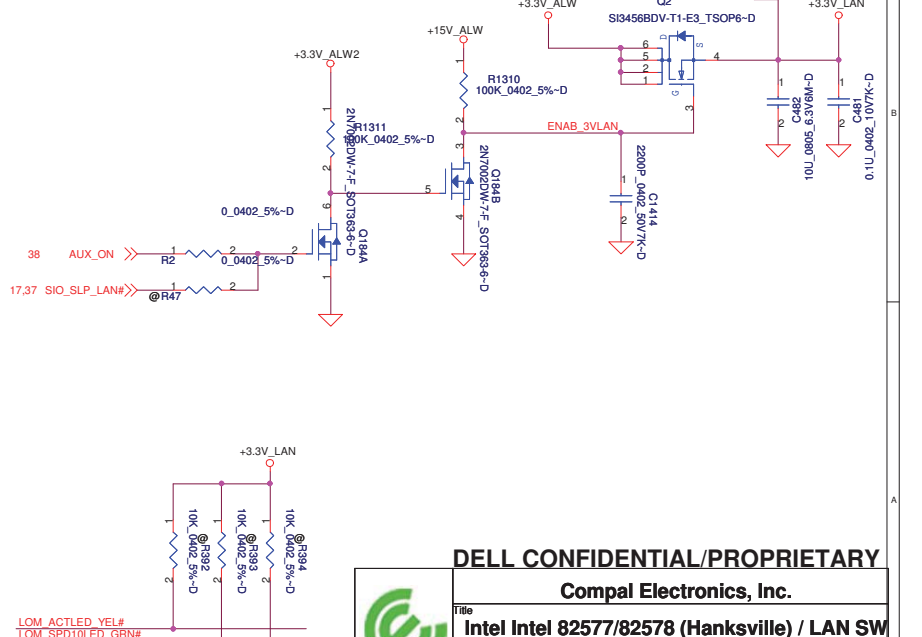
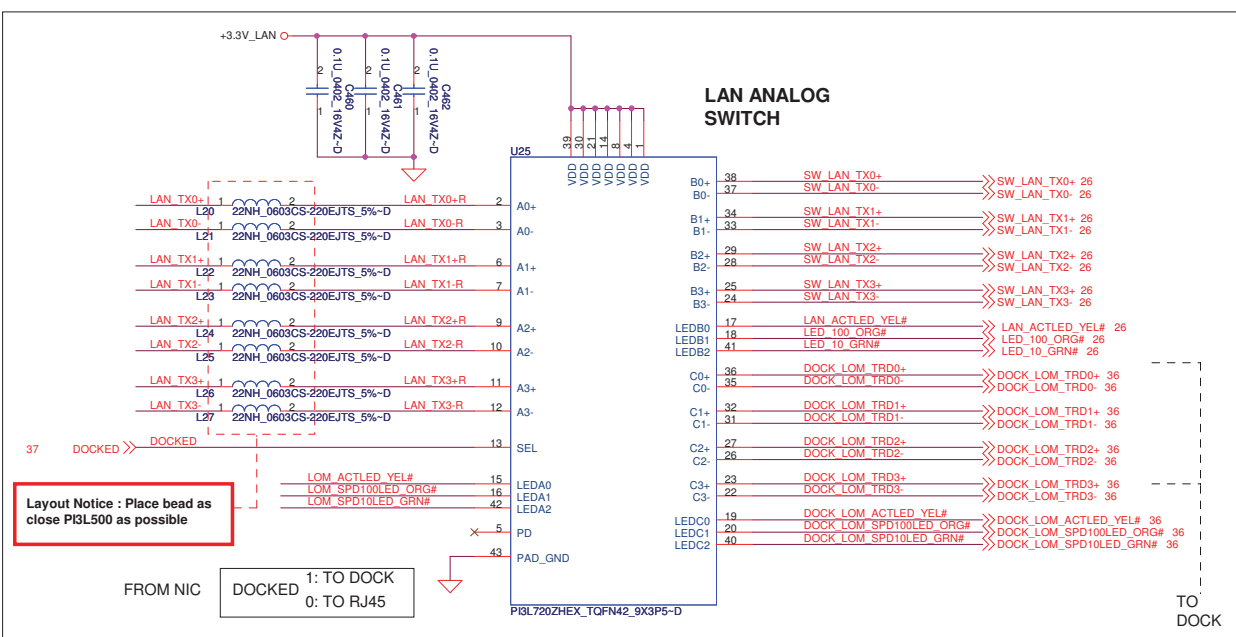
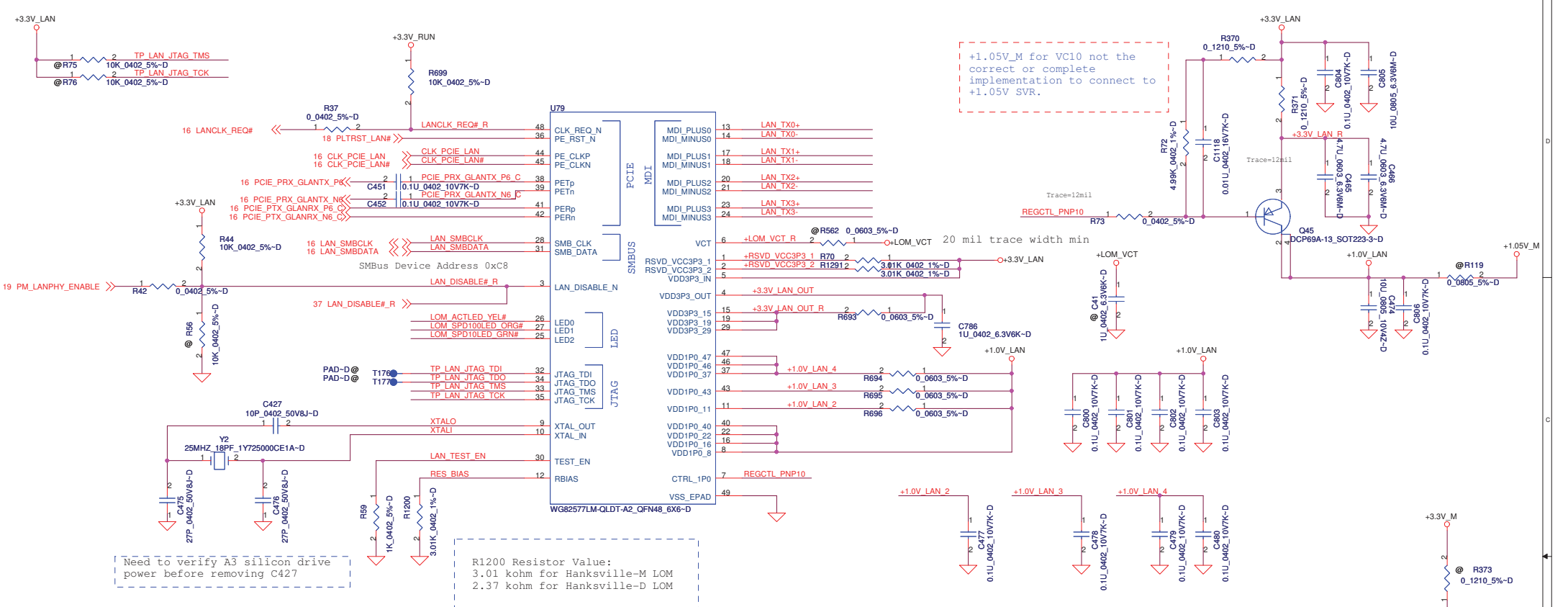
Date: **Monday, July 13, 2009** Sheet: **28** of **51**

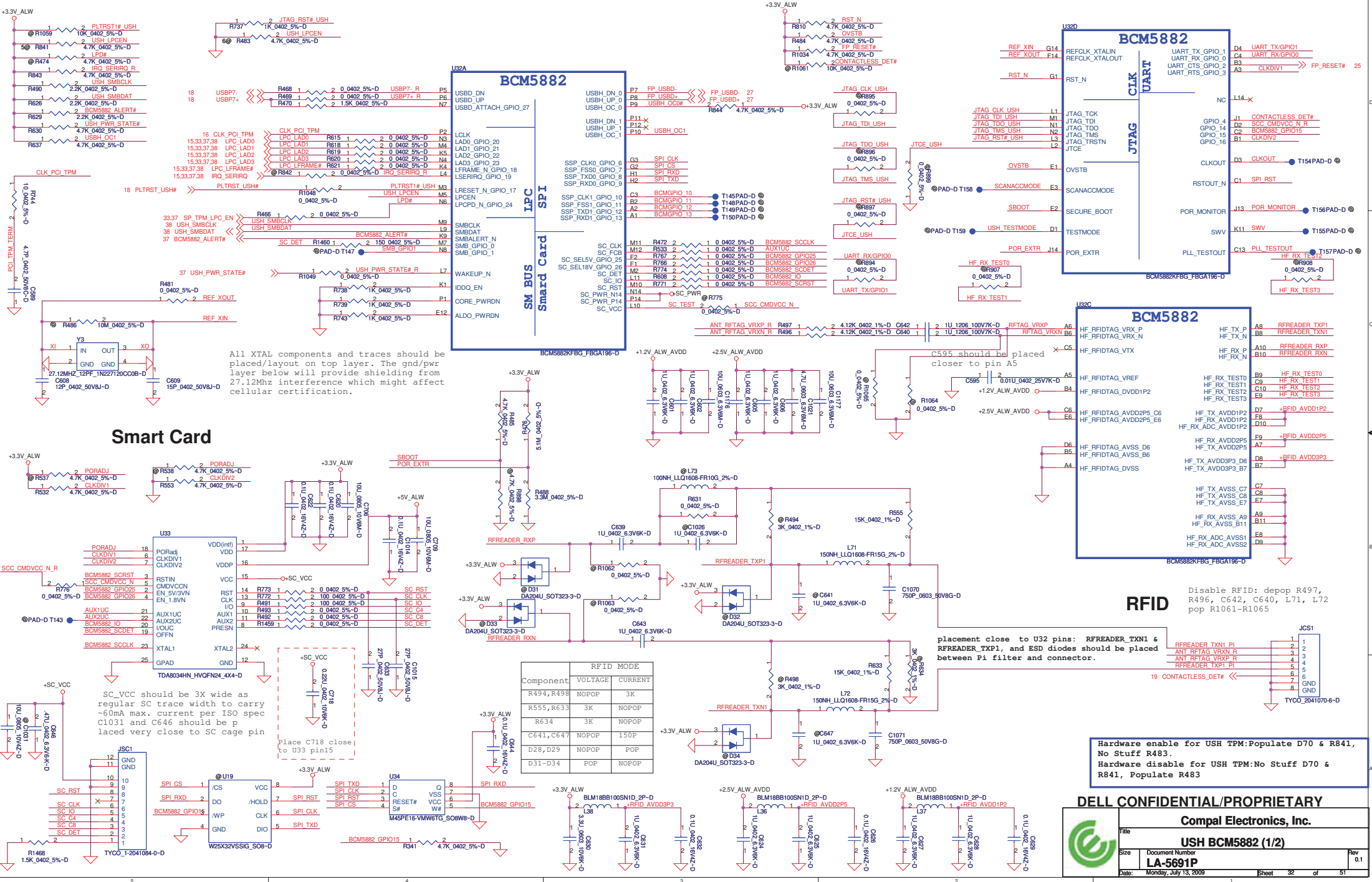
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**USH BCM5882 (1/2)**

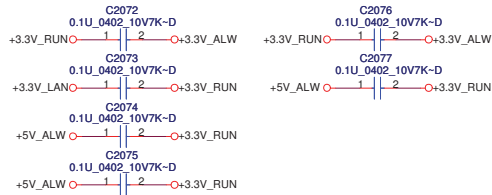
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 Size: \_\_\_\_\_ Document Number: **LA-5691P**  
 Date: Monday, July 13, 2008 Sheet 32 of 51



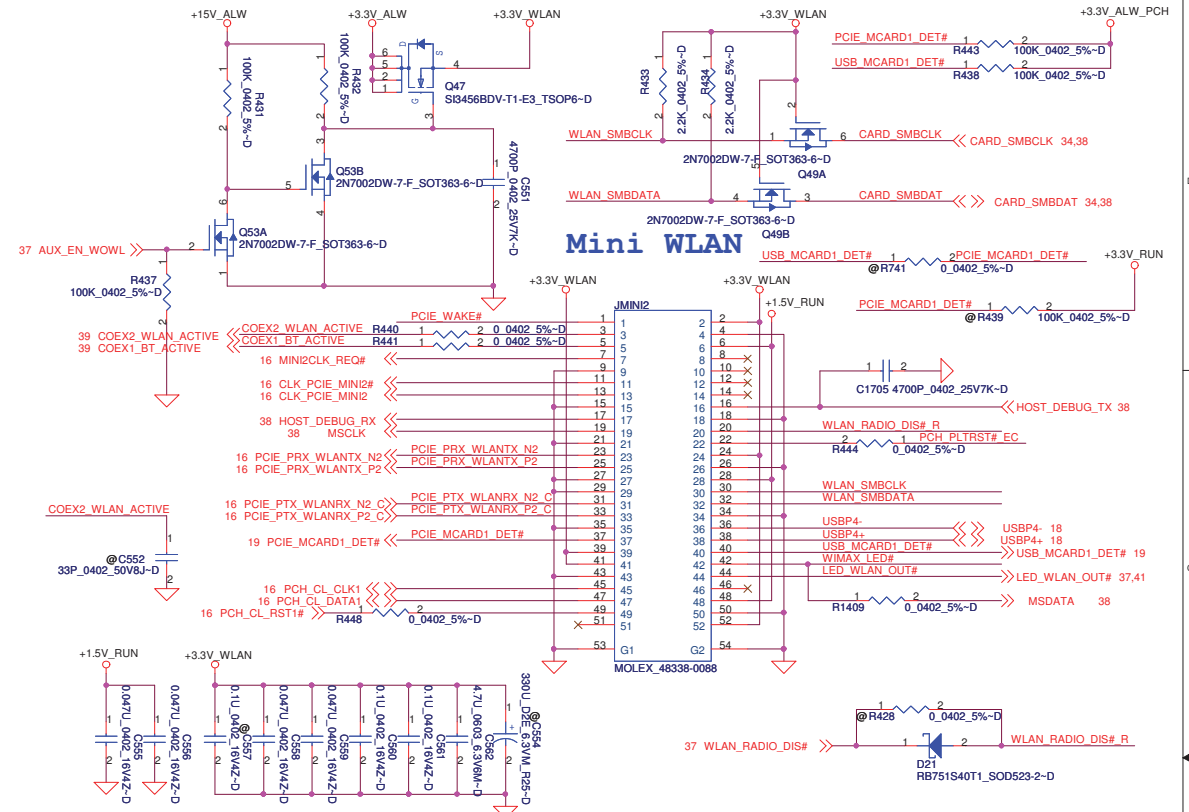




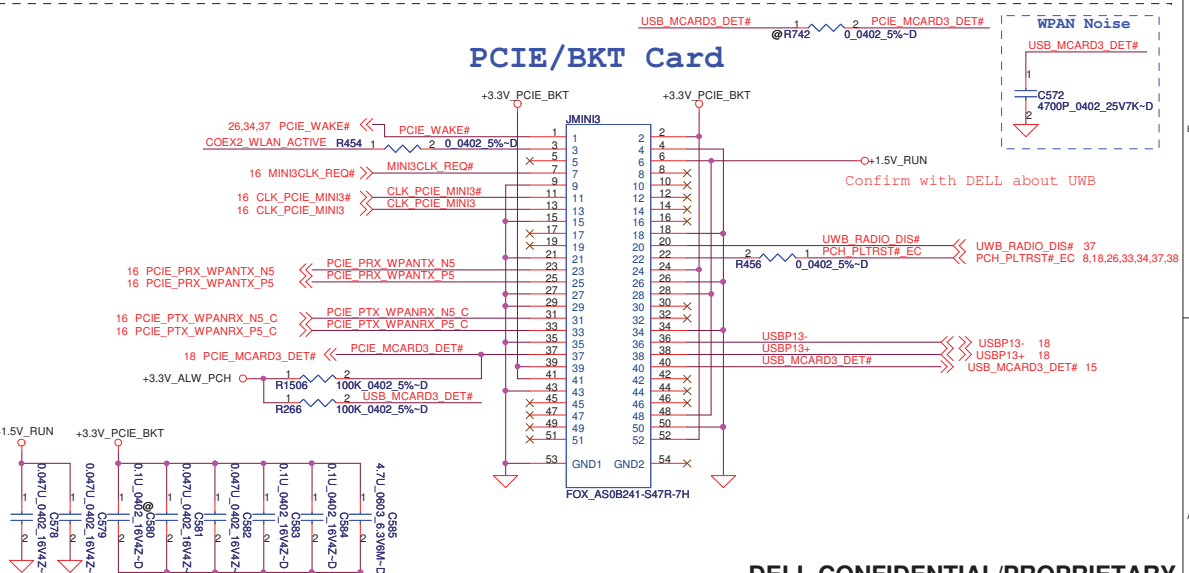
**Stitching caps for MDI**



**Stitching caps for PCIe6**



**PCIe/BKT Card**



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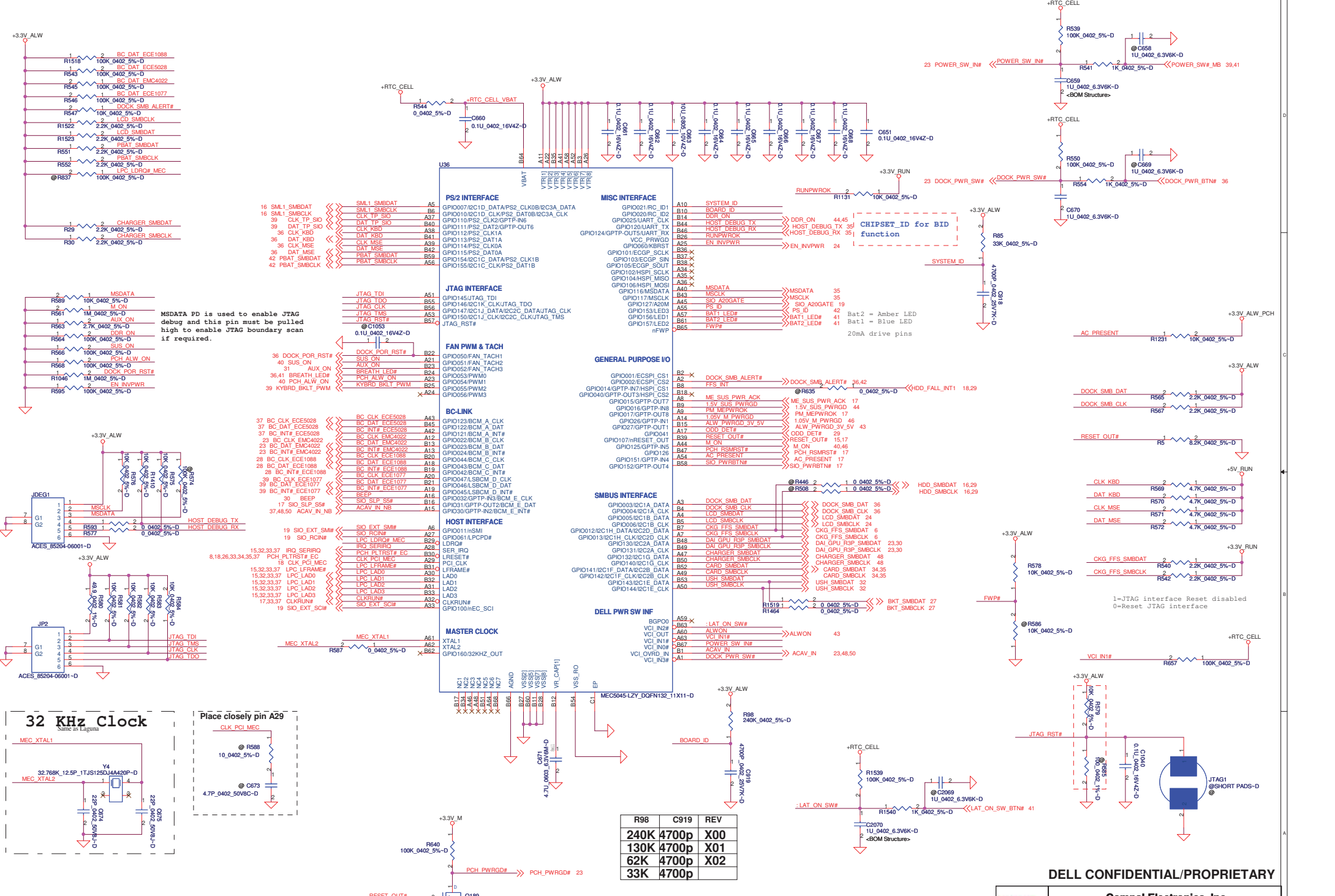
**Compal Electronics, Inc.**

Title			Mini Card		
Size			Document Number		
			LA-5691P		
Date			Monday, July 13, 2009		
Sheet			35 of 51		
Rev			0.1		

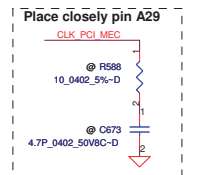
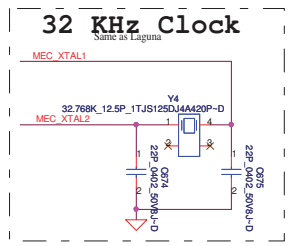
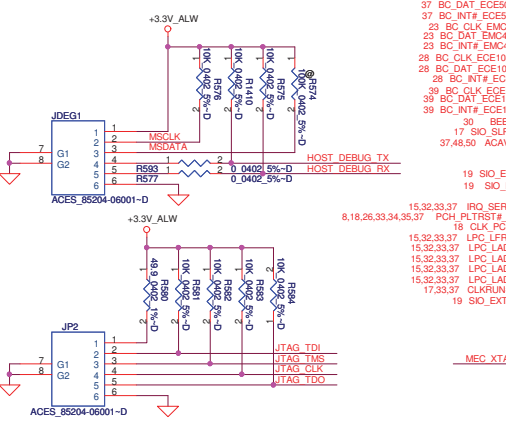
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MSDATA PD is used to enable JTAG debug and this pin must be pulled high to enable JTAG boundary scan if required.



R98	C919	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	

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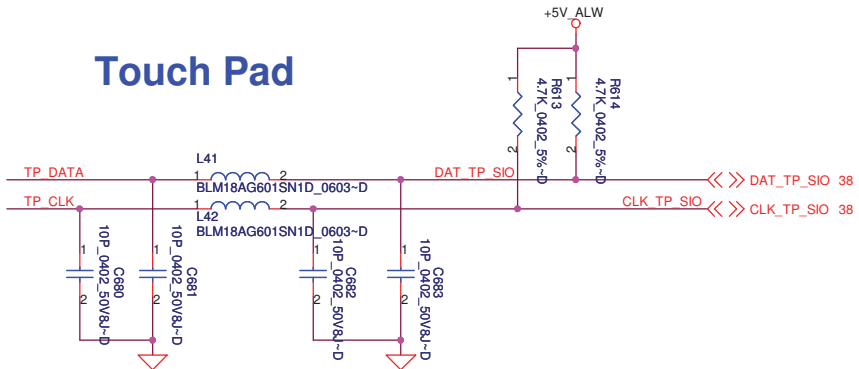
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Size: Document Number: **LA-5691P**

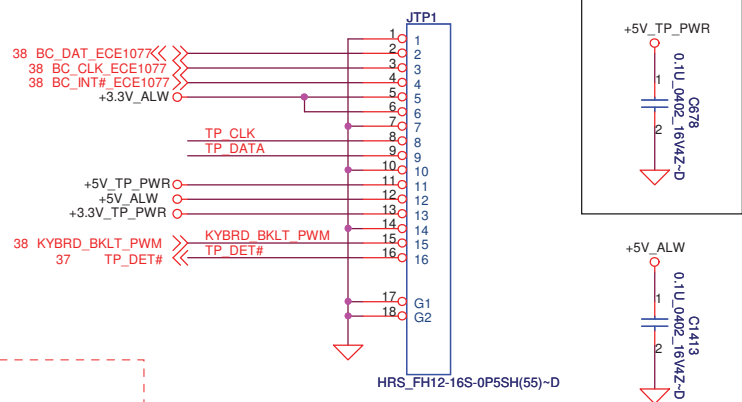
Date: Monday, July 13, 2009 Sheet 38 of 51

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# Touch Pad



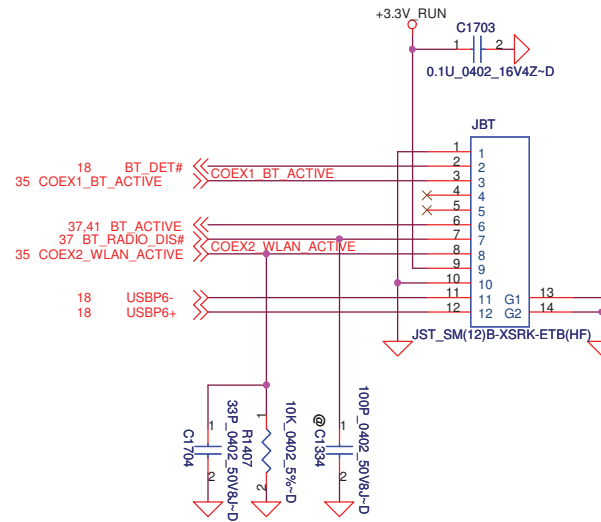
# New Keyboard connector assignment



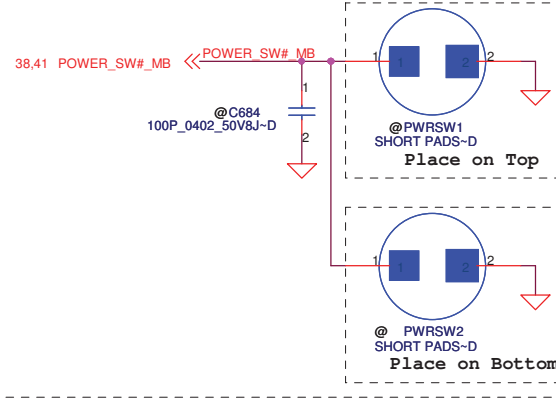
Place close to JTP1.5,6

Place close to JTP1 connector

# BlueTooth



# Power Switch for debug



@FAN

Part Number	Description
DC28A000800	FAN SET DAQ20 DC5V AB7405HB-HB3 ADDA

@Speak

Part Number	Description
PK230003Q0L	SPK PACK ZJX 2.0W 4 OHM FG

@SM CARD BODY

Part Number	Description
SP070007V0L	S SOCKET TYCO 1770551-1 10P H5.9 SMART

@PCMCIA BODY

Part Number	Description
DC000001Q0L	PCMCIA TYCO 1759096-1

@MDC wire set cable

Part Number	Description
DC02000CS0L	H-CONN SET ZGX MB-MDC

@T/P wire set cable

Part Number	Description
DC02000840L	H-CONN SET ZJX MB-B/T-TP-FP

@LVDS cable

Part Number	Description
DC020003Y0L	H-CONN SET ZJX MB-LCD 14 WXGA+(-1ch)

@LVDS cable

Part Number	Description
DC02000870L	H-CONN SET ZJX MB-LCD 14 WXGA+(-2ch)

@RTC BATT

Part Number	Description
GC20323MX00	BATT CR2032 3V 220MAH MAXELL

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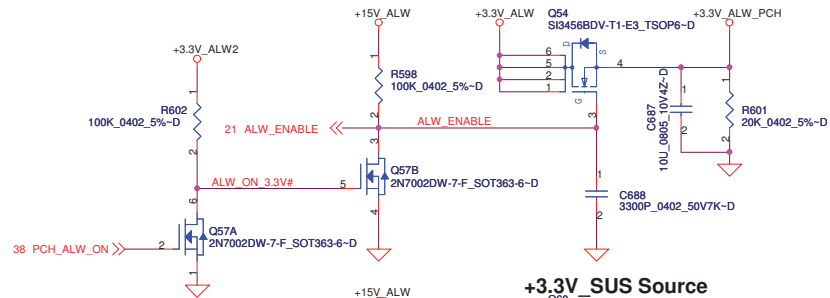
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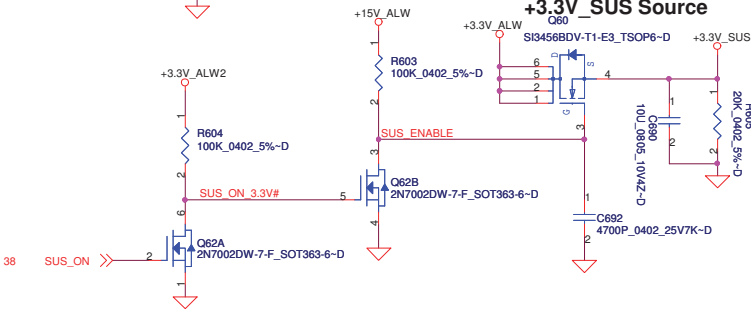
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Touch PAD/Int KB/LID		
Size	Document Number	Rev
	LA-5691P	0.1
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# DC/DC Interface

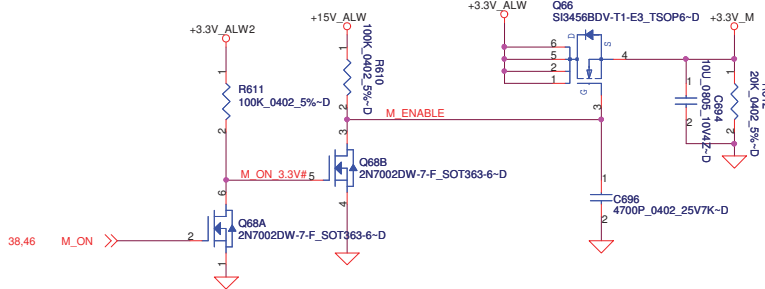
## +3.3V\_ALW\_PCH Source



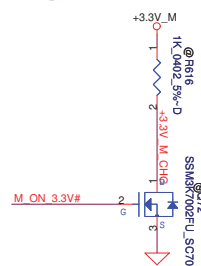
## +3.3V\_SUS Source



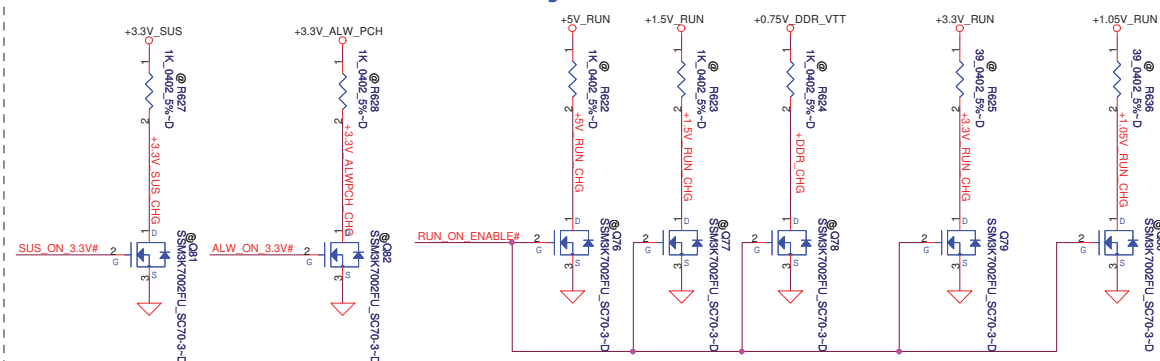
## +3.3VM Source



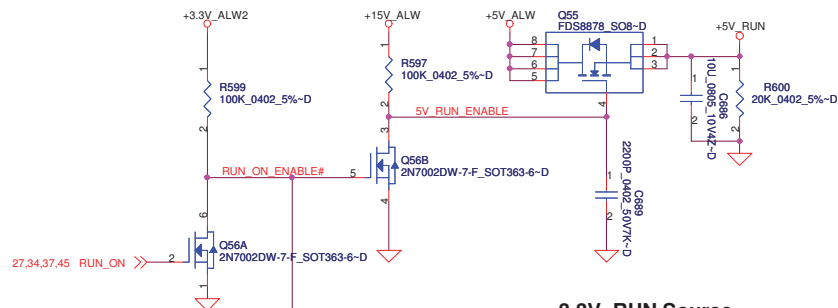
## Discharg Circuit



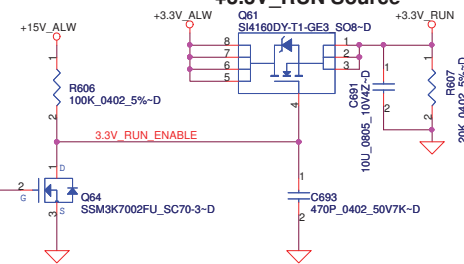
## Discharg Circuit



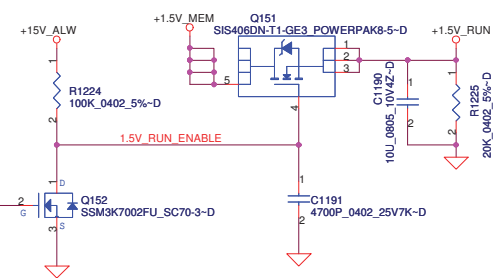
## +5VRUN Source



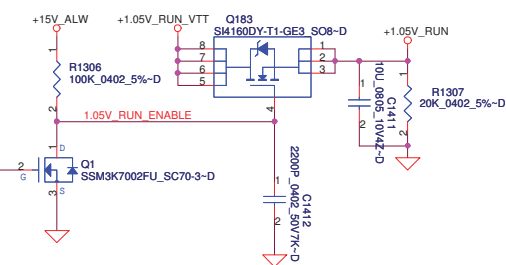
## +3.3V\_RUN Source



## +1.5V\_RUN Source



## +1.05V\_RUN Source



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POWER CONTROL

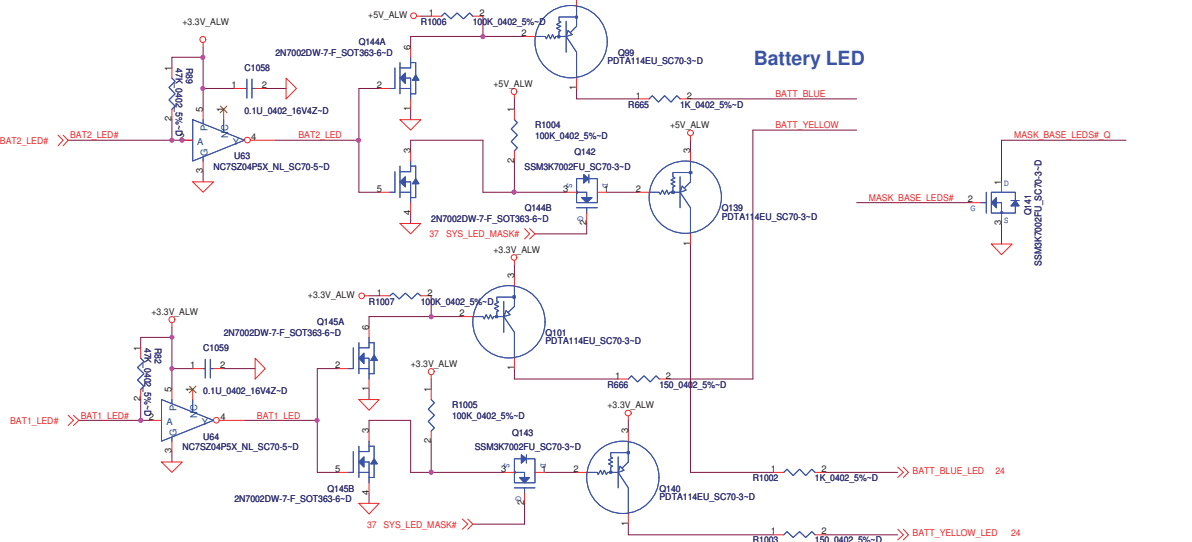
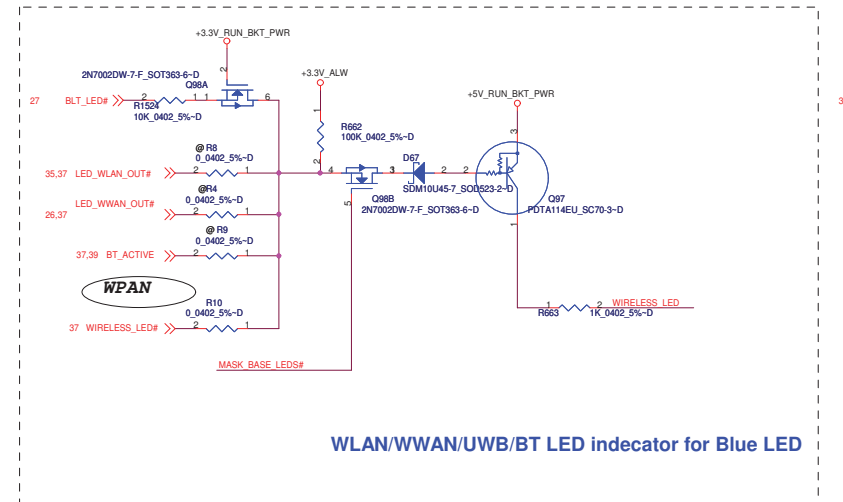
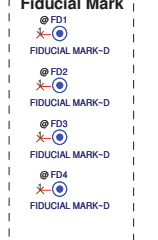
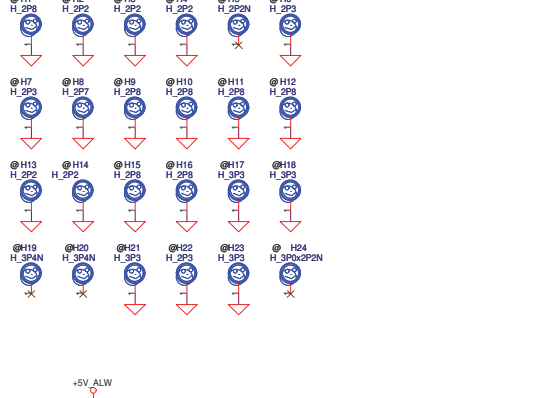
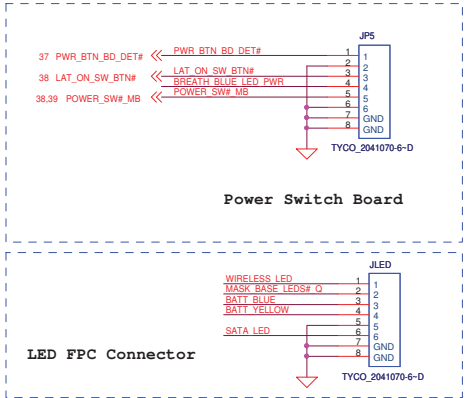
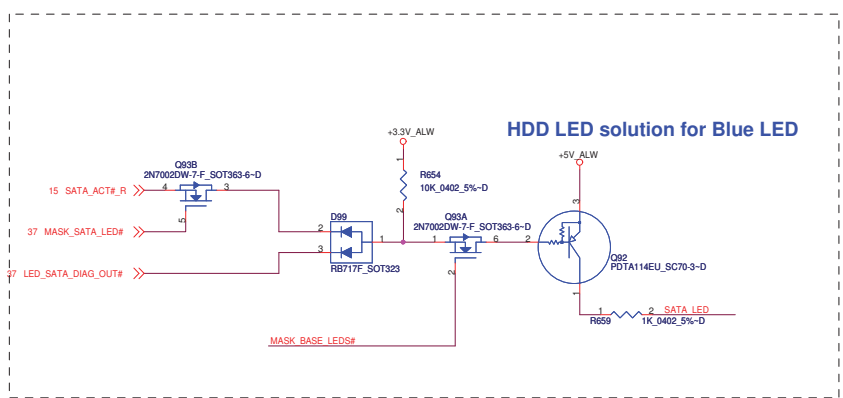
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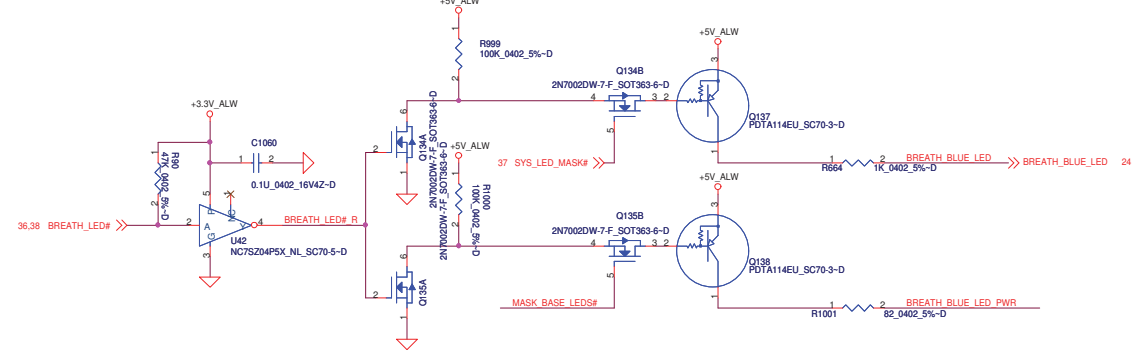
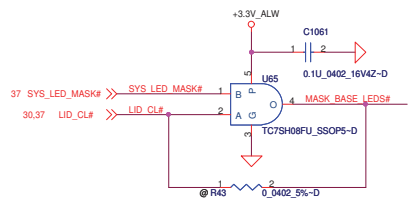
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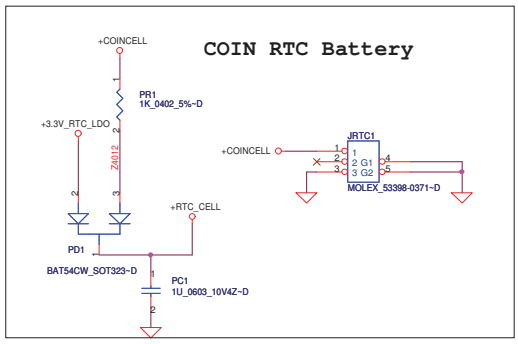
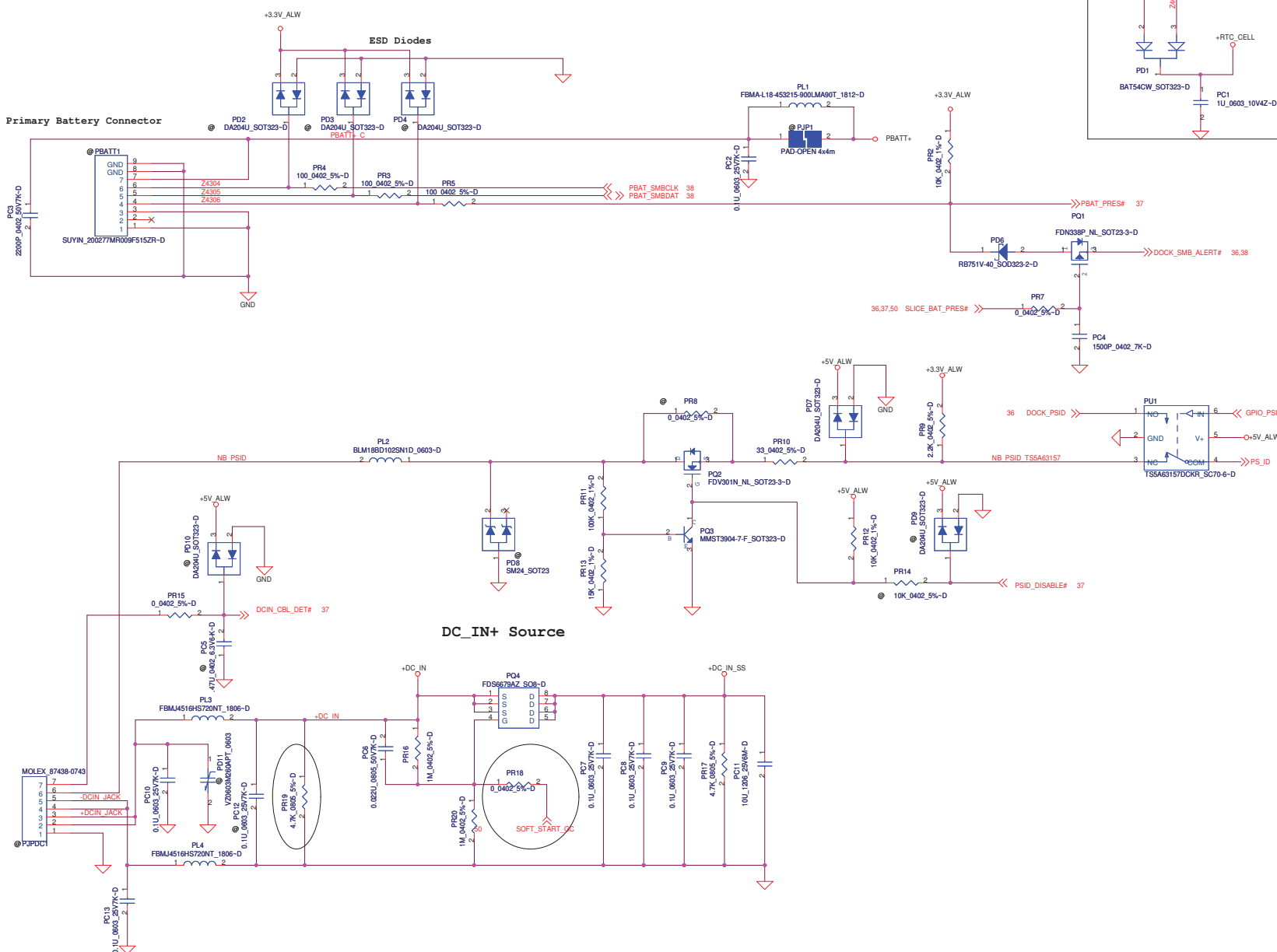
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LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1





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+DCIN

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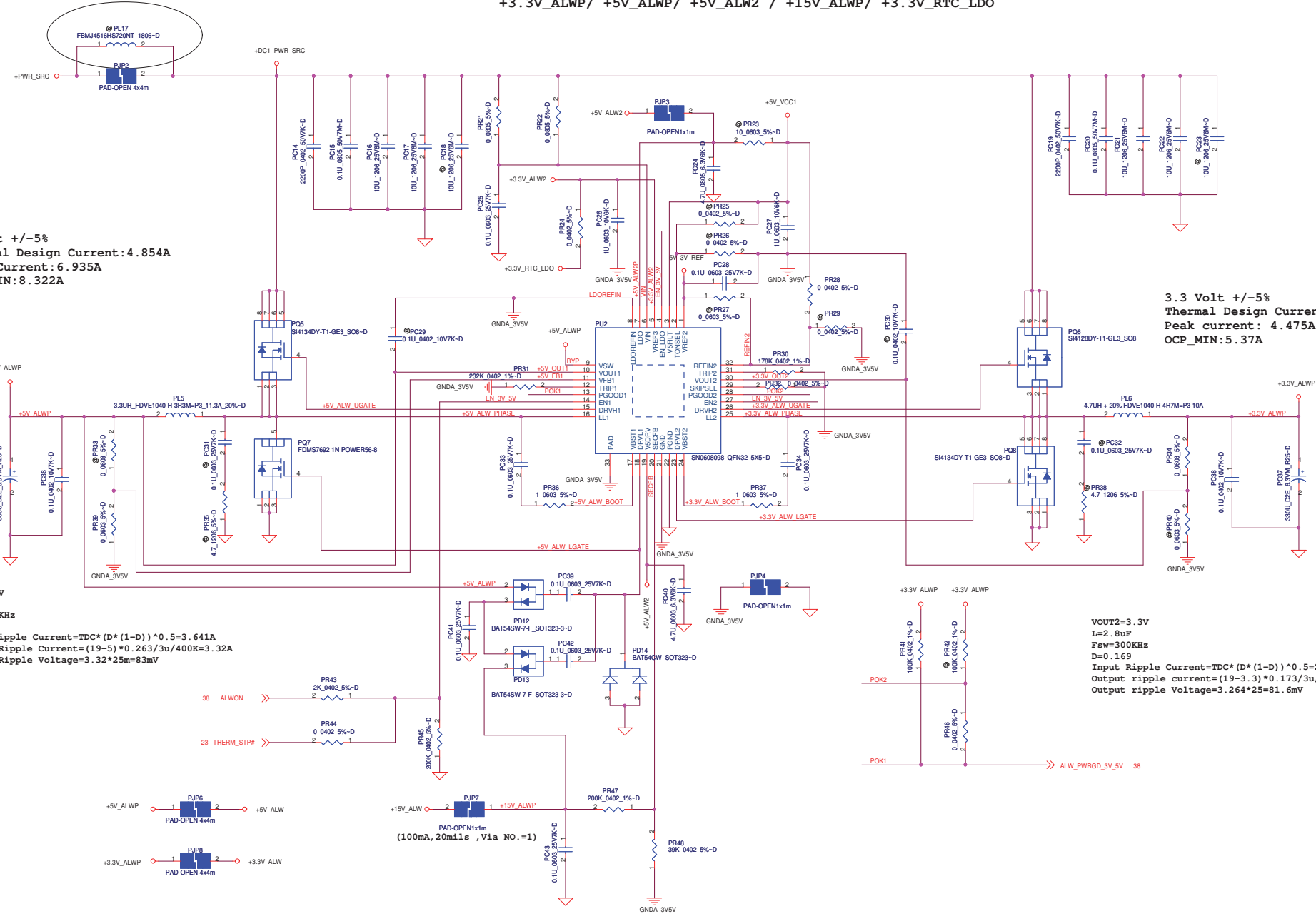
**+3.3V\_ALWP/ +5V\_ALWP/ +5V\_ALW2 / +15V\_ALWP/ +3.3V\_RTC\_LDO**

**5 Volt +/-5%**  
**Thermal Design Current: 4.854A**  
**Peak Current: 6.935A**  
**OCV\_MIN: 8.322A**

**3.3 Volt +/-5%**  
**Thermal Design Current: 3.133A**  
**Peak current: 4.475A**  
**OCV\_MIN: 5.37A**

**VOUT2=5V**  
**L=2.8uF**  
**Fsw=400KHz**  
**D=0.256**  
**Input Ripple Current=TDC\*(D\*(1-D))^0.5=3.641A**  
**Output Ripple Current=(19-5)\*0.263/3u/400K=3.32A**  
**Output Ripple Voltage=3.32\*25m=83mV**

**VOUT2=3.3V**  
**L=2.8uF**  
**Fsw=300KHz**  
**D=0.169**  
**Input Ripple Current=TDC\*(D\*(1-D))^0.5=2.051A**  
**Output ripple current=(19-3.3)\*0.173/3u/300K=3.264A**  
**Output ripple Voltage=3.264\*25m=81.6mV**



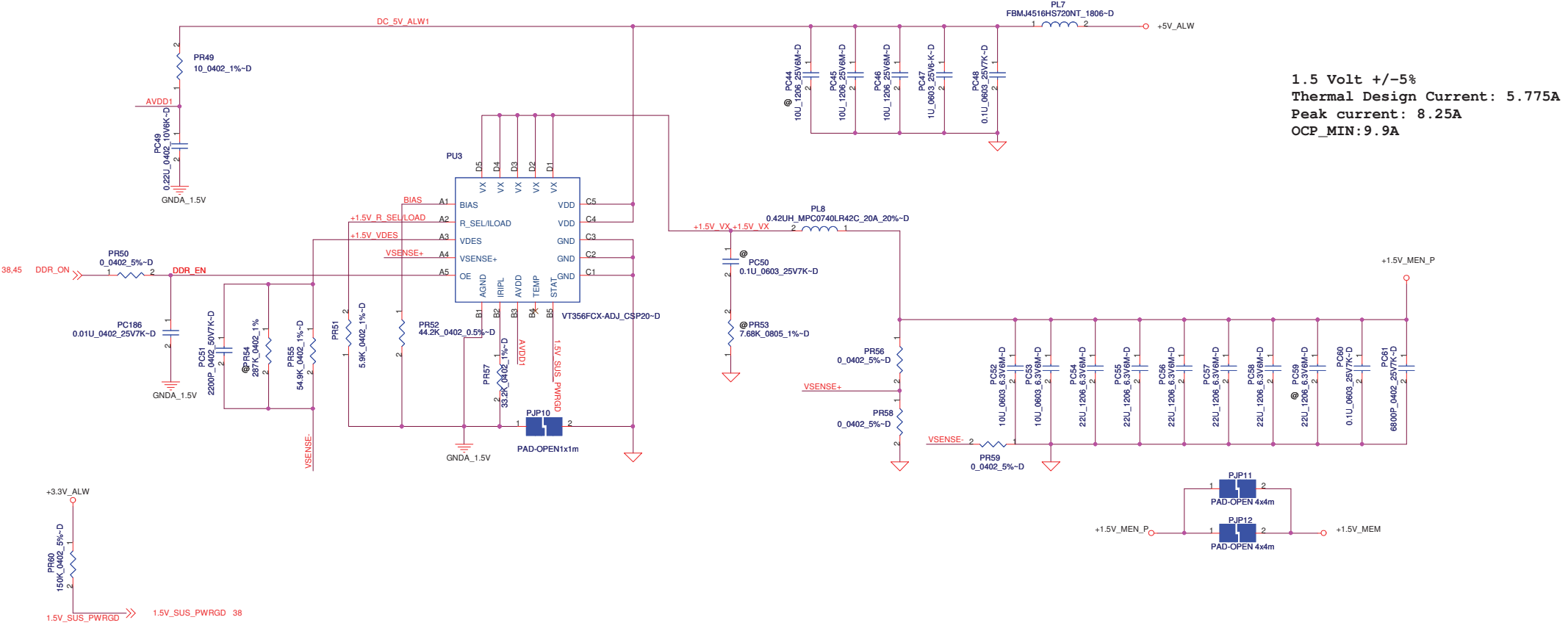
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**DC/DC +3V/ +5V**

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# +1.5V\_MEN\_P (VT356)



1.5 Volt +/-5%  
 Thermal Design Current: 5.775A  
 Peak current: 8.25A  
 OCP\_MIN:9.9A

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+1.5V\_MEM

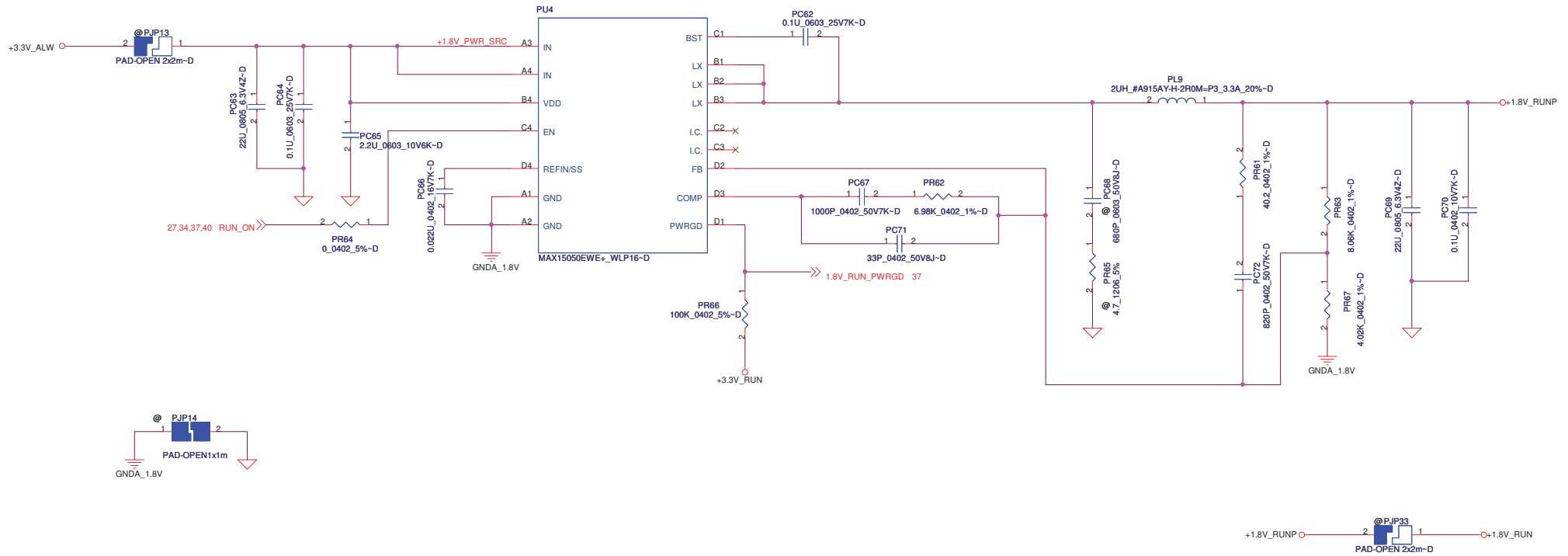
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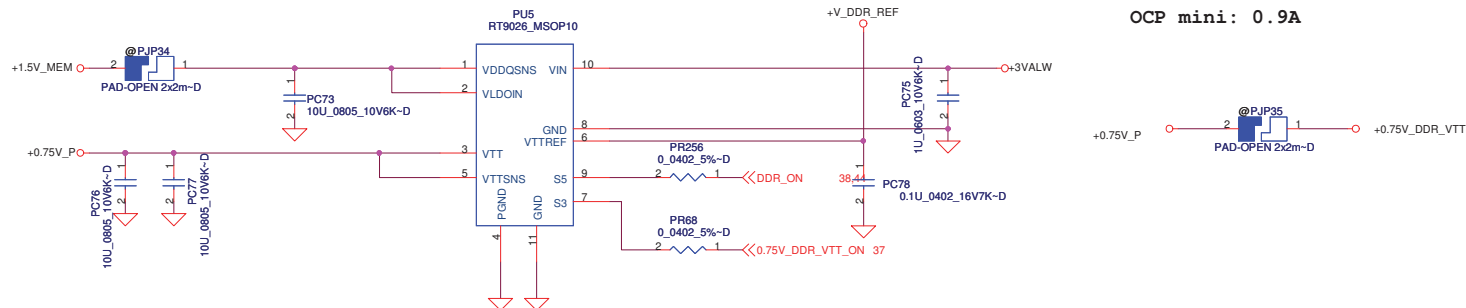
# +1.8V\_RUN

1.8 Volt +/-5%  
 Thermal Design Current: 0.894A  
 Peak current: 1.277A  
 OCP\_min:1.532A



# +0.75V\_DDR\_VTT DDR3 Termination

0.75Volt +/-5%  
 Thermal Design Current: 0.525A  
 Peak current: 0.75A  
 OCP mini: 0.9A



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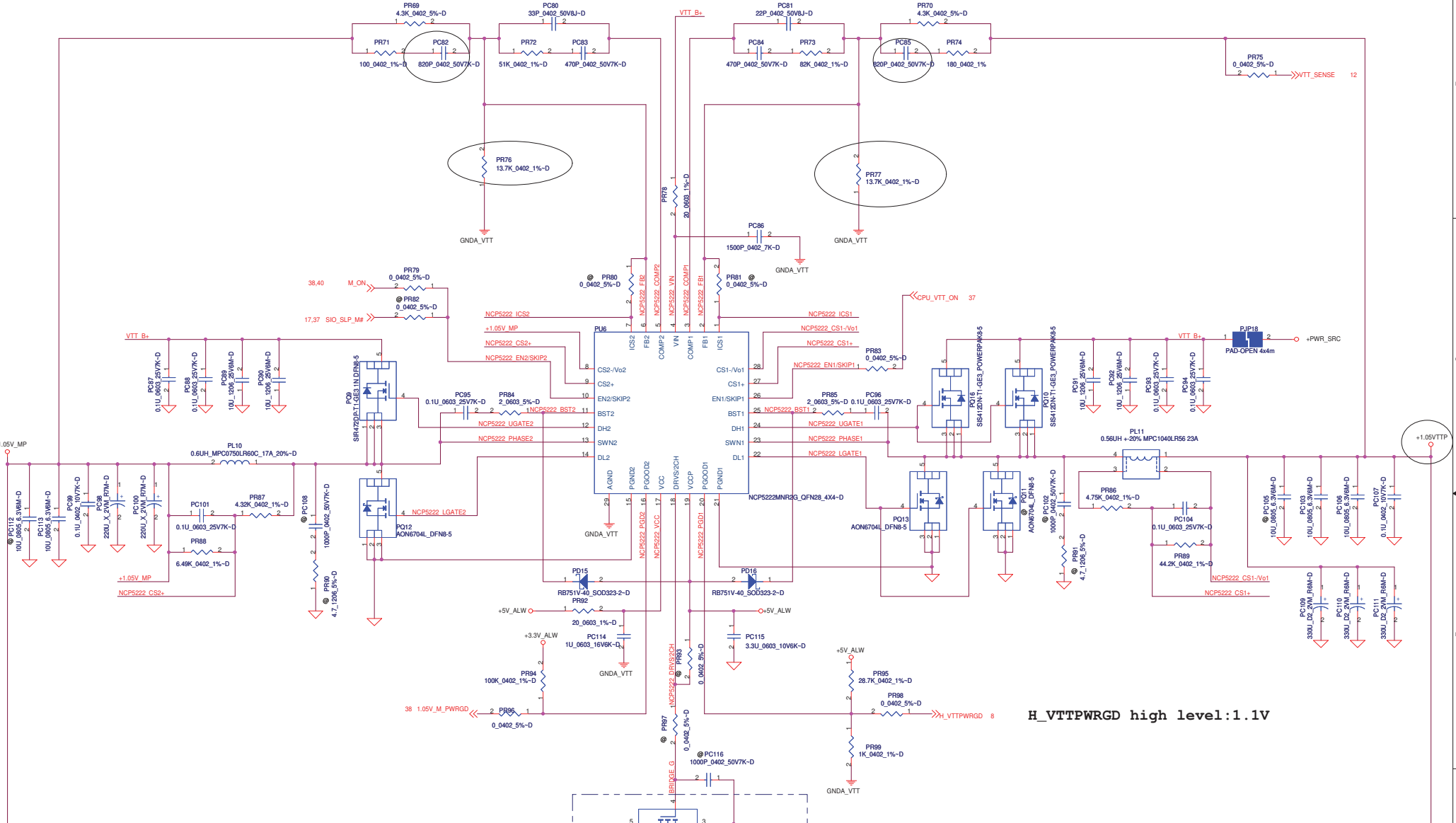
Title			
+1.8V_RUN/+0.75V_DDR_VT			
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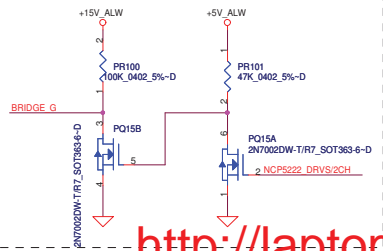
1.05 Volt +/-5%  
 Thermal Design Current: 1.51A  
 Peak current: 2.17A

+1.05V\_M/+1.05VTT\_RUN

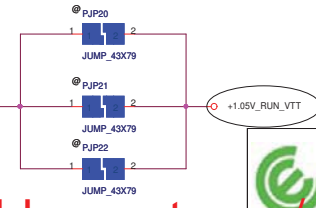
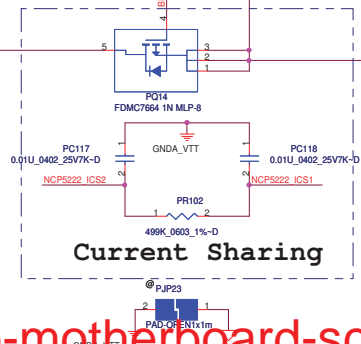
1.05 Volt +/-5%  
 Thermal Design Current: 15.9A  
 Peak current: 22.7A



Sharing MOSFET gate driver



Current Sharing

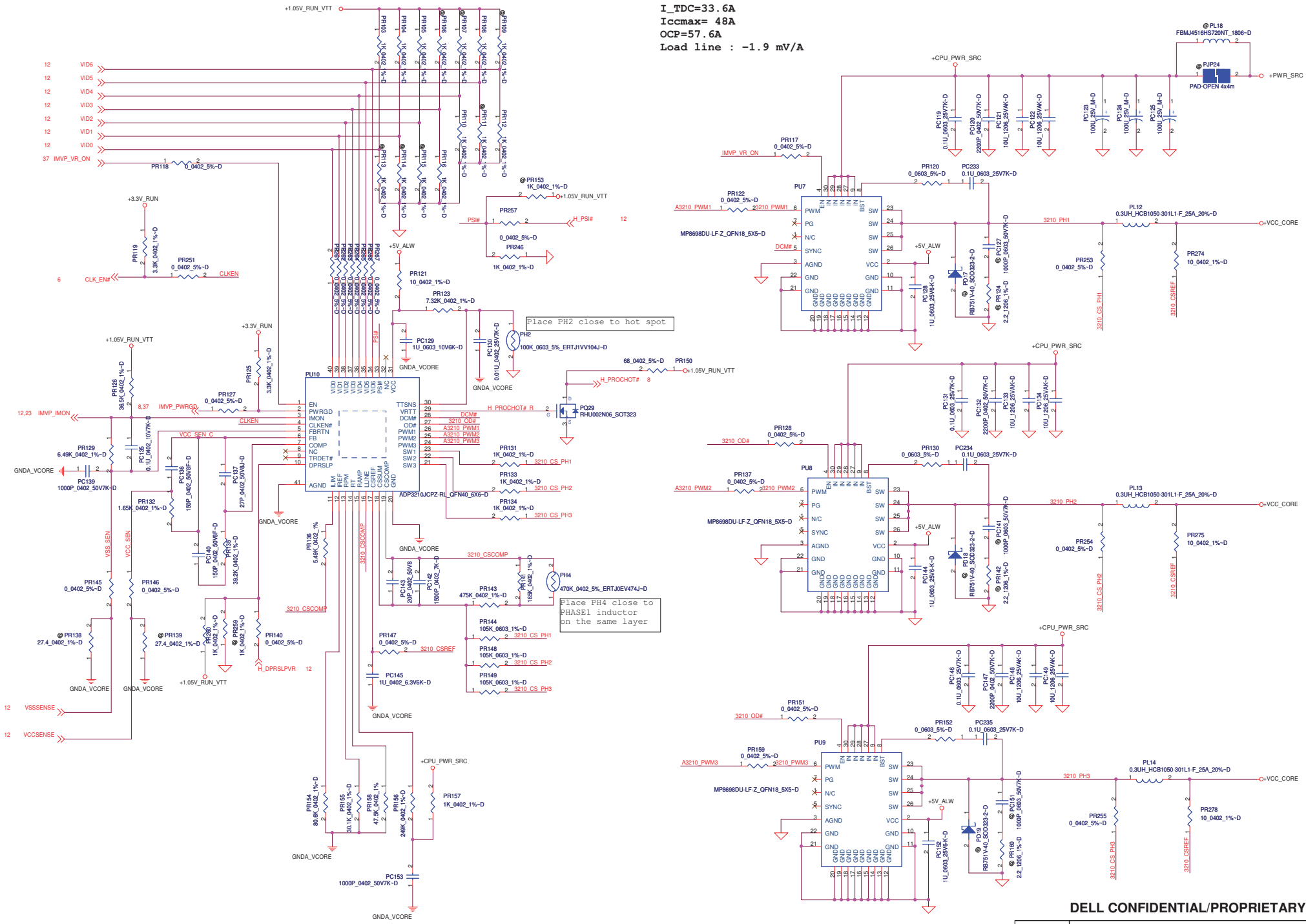


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+1.05V_M/+1.05V_RUN_VTT		
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I\_TDC=33.6A  
 Iccmax= 48A  
 OCP=57.6A  
 Load line : -1.9 mV/A



Place PH2 close to hot spot

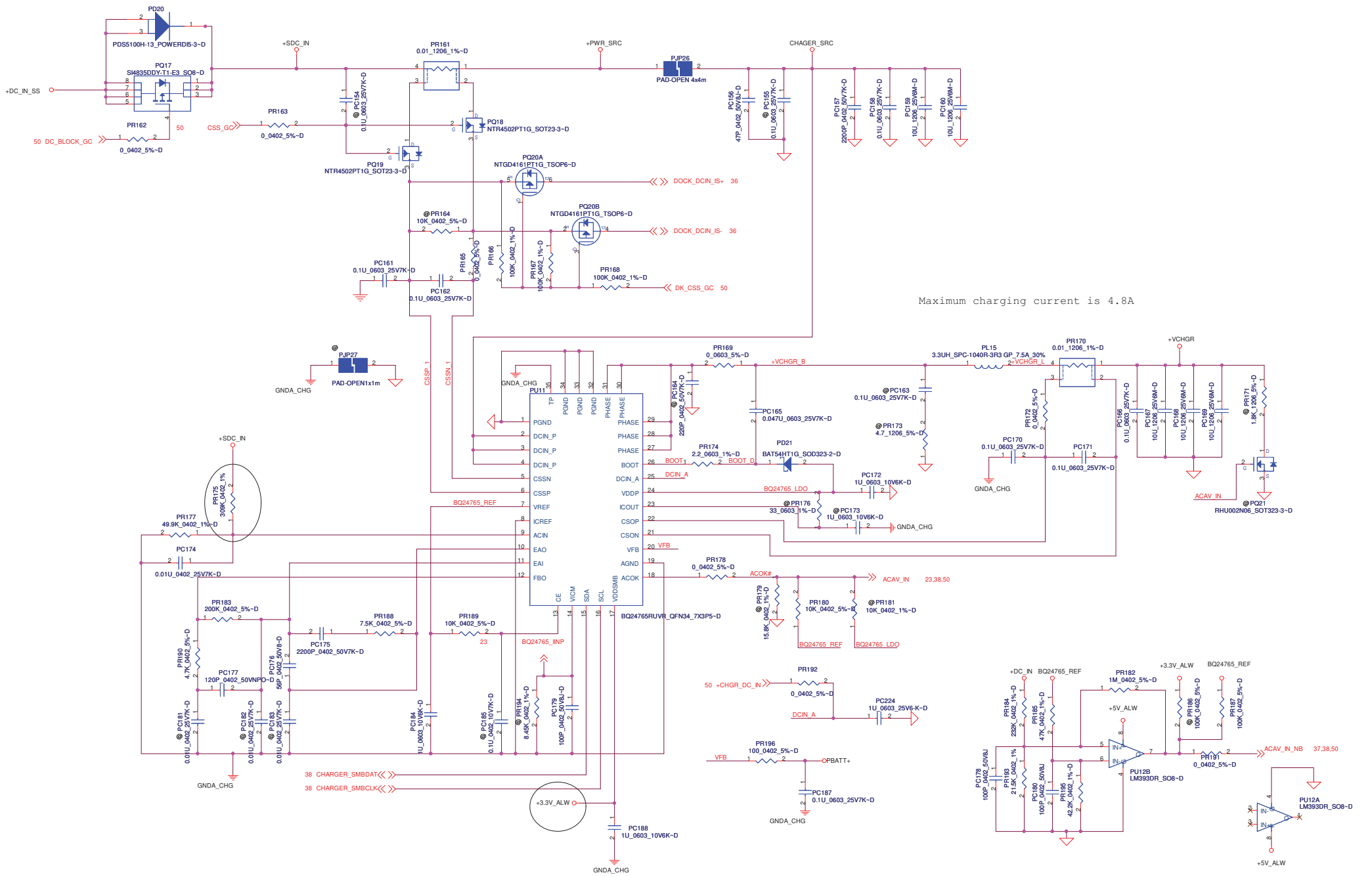
Place PH4 close to PHASE1 inductor on the same layer

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<b>+VCC CORE</b>	
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Maximum charging current is 4.8A

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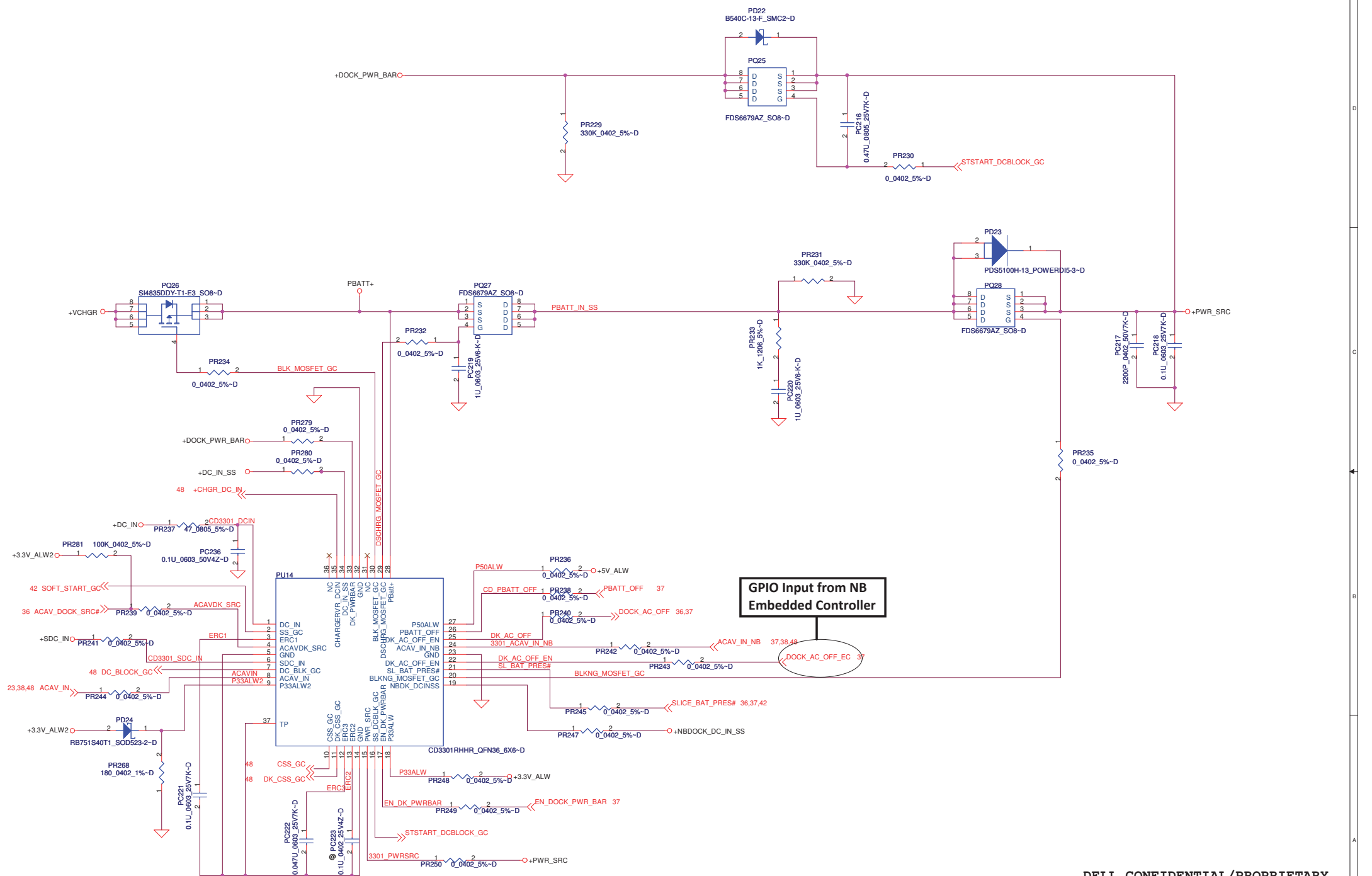
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Size:	Document Number: <b>LA-5691P</b>	Rev: <b>0.1</b>
Date: <b>Monday, July 13, 2009</b>	Sheet: <b>48</b>	of: <b>51</b>

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GPIO input from NB Embedded Controller

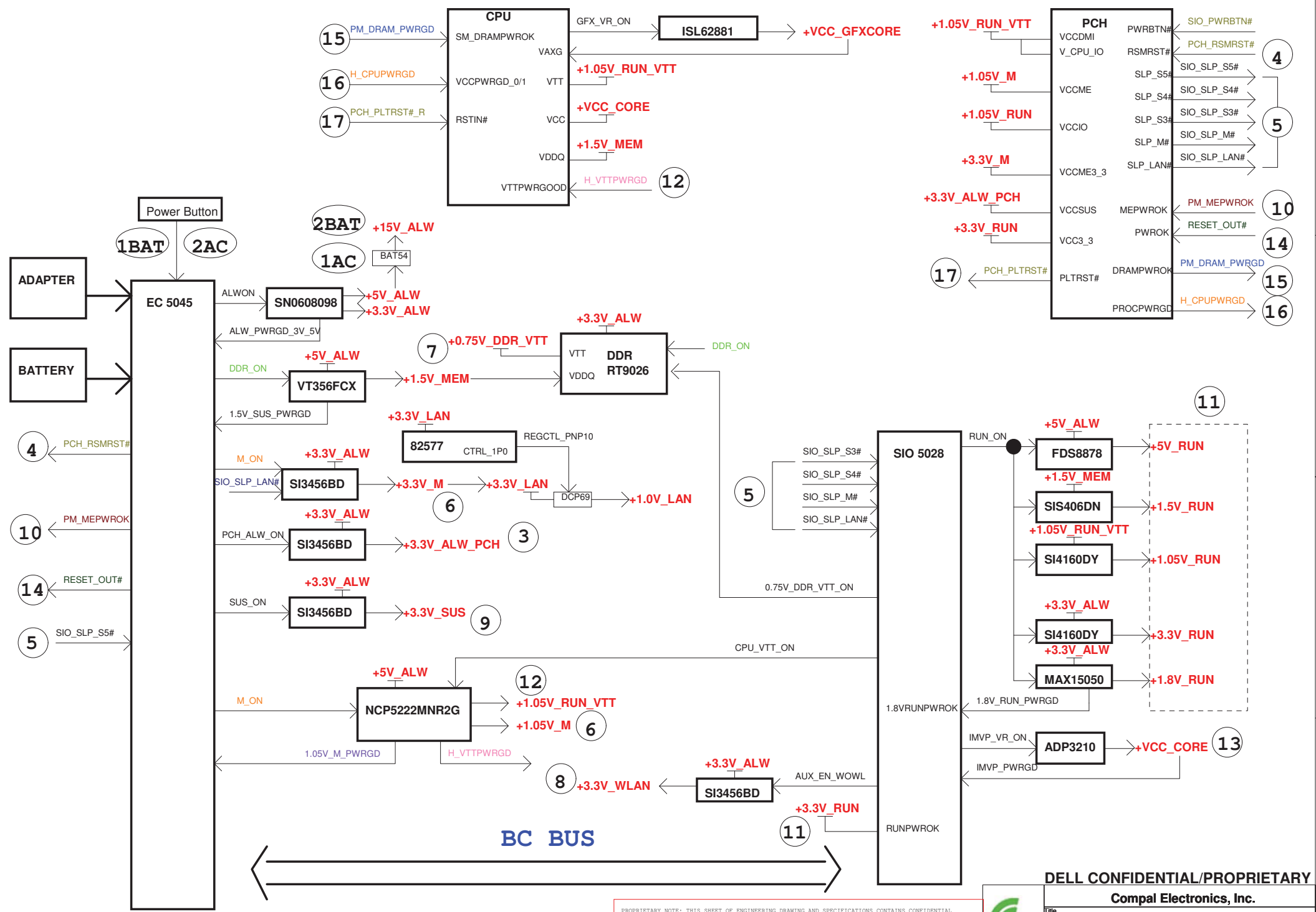
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Title Power Sequence

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