

COMPAL CONFIDENTIAL

MODEL NAME : *PLM00*

PCB NO : *LA-7161P (DAZ0I800100)*

BOM P/N : *4319AS31L01*

4319AS31L02

4319AS31L03

4319AS31L04

4319AS31L05

4319AS31L06

4319AS31L07

4319AS31L08

Andros MLK

AMD APU (Ontario/Zacate) -FT1 + FCH Hudson-M1

2011-01-05

REV : 1.0(A00)

@ : Nopop Component

WWAN@: WWAN function

CONN@: Connector only

Z@ : Zacate

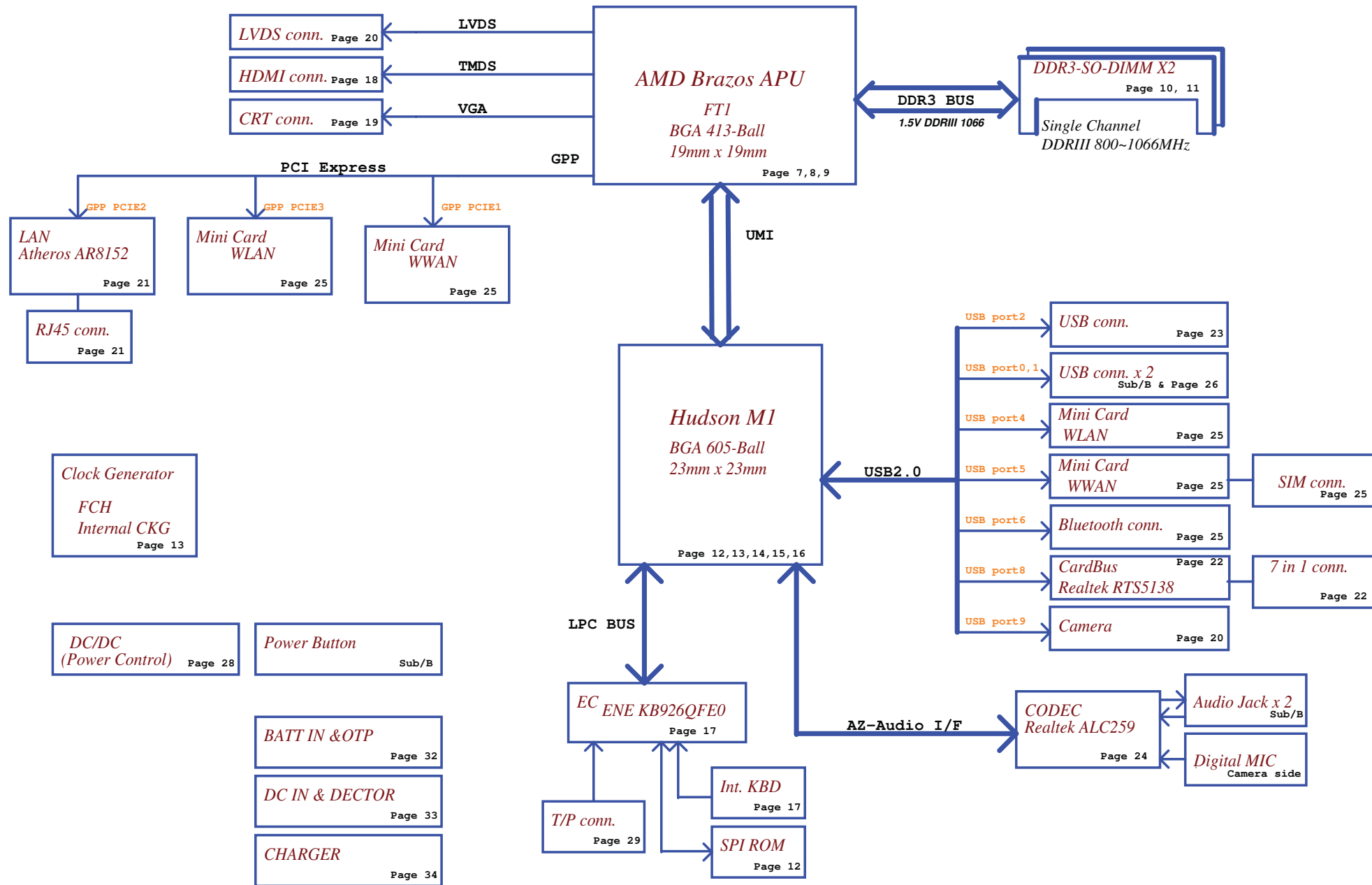
O@ : Ontario

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Compal Electronics, Inc.

Title		
Cover Sheet		
Size	Document Number	Rev
	LA-7161P	1.0
Date: Wednesday, January 05, 2011		
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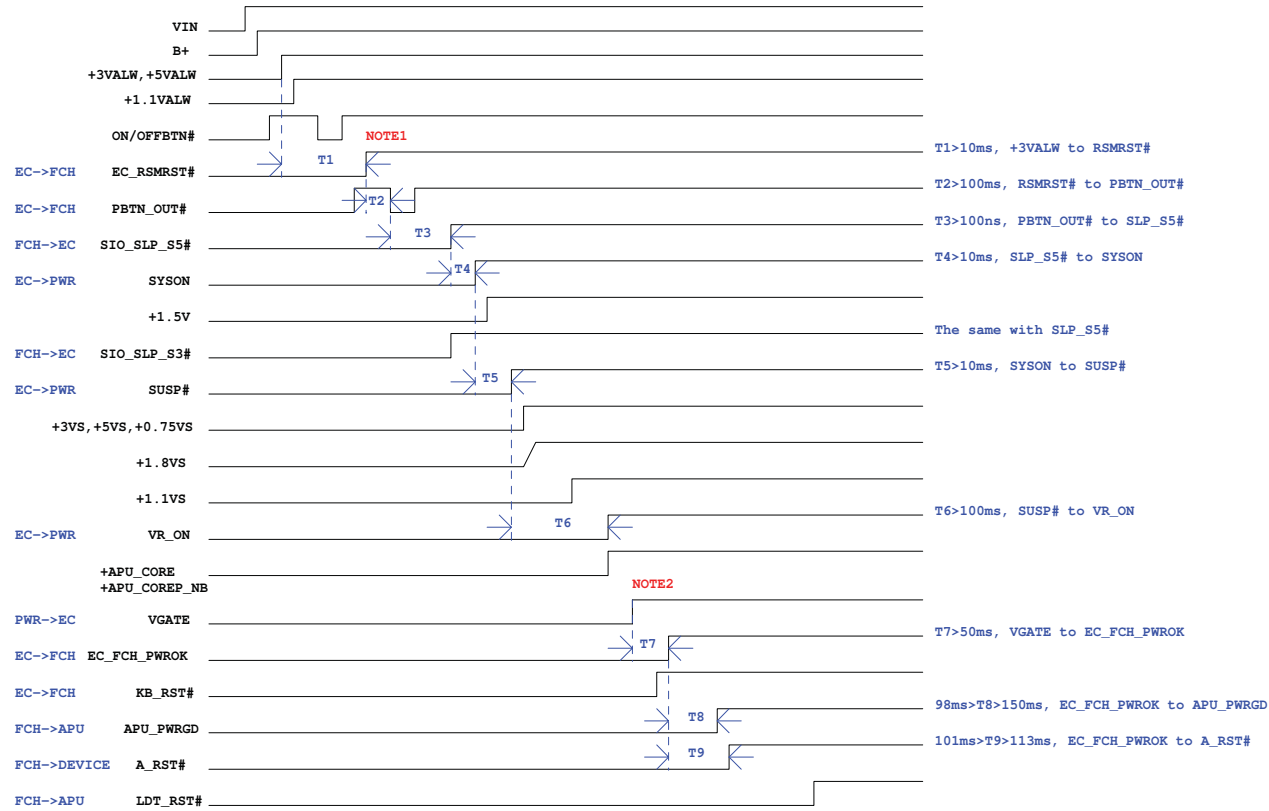
Block Diagram

LA-7161P

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POWER SEQUENCE



NOTE1: RSMRST# rise time(10% to 90%)<50ms
fail time<1ms

NOTE2: EC_FCH_PWROK rise time(10% to 90%)<50ms
fail time<1ms

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+APU_CORE_NB	1.0V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDRIII	ON	ON	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+1.1VS	1.1VS switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON(WOL)	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON
+1.1VALW	1.1V always on power rail	ON	ON	ON*

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

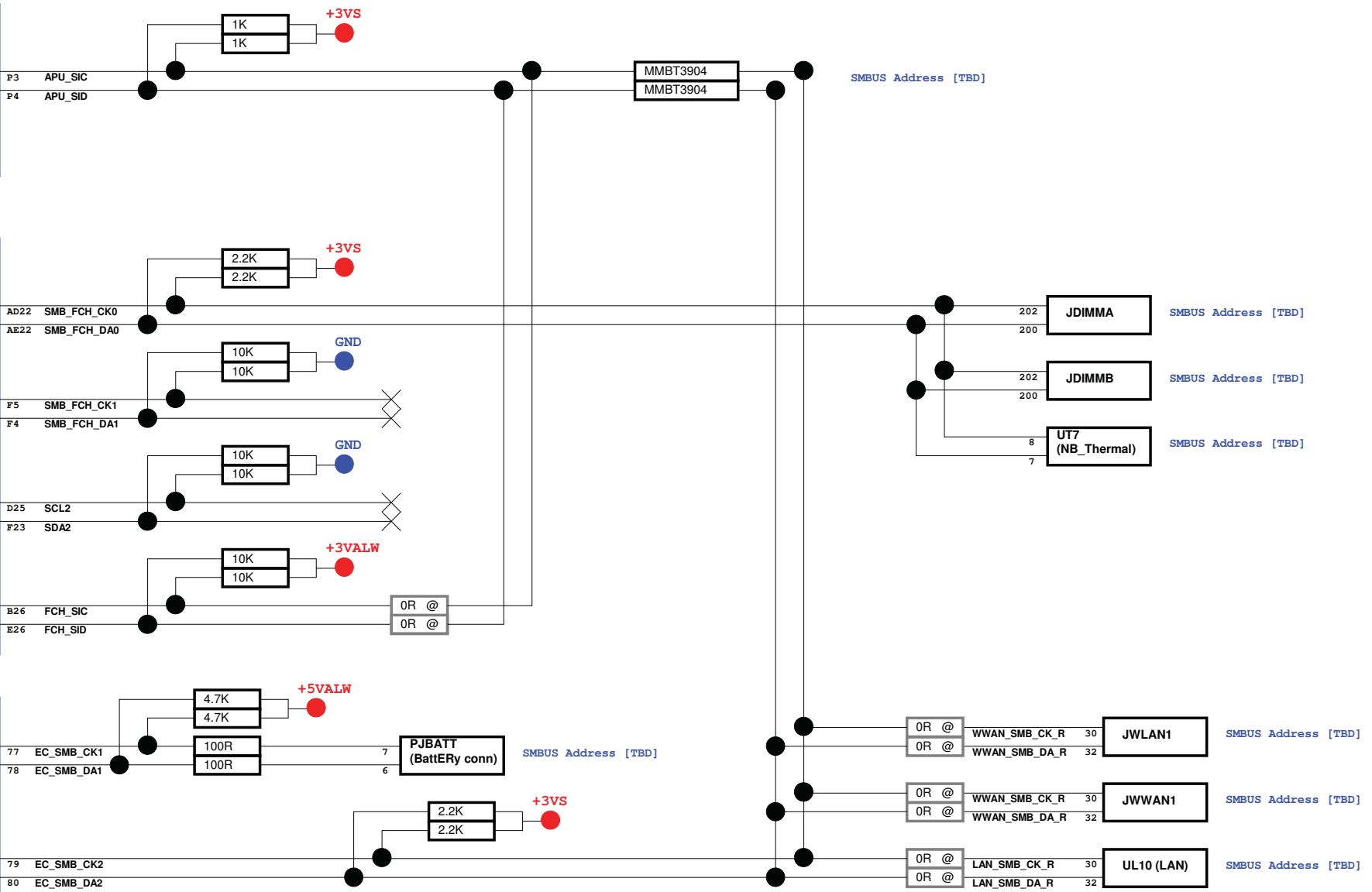
Board ID Table for AD channel

Board ID	Rb	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max	EC AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	0.5
5	
6	
7	

Title		
Power Rails		
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SMBus Topology

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Board ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	V _{AD_BID min}	V _{AD_BID typ}	V _{AD_BID max}	EC AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	0.5
5	
6	
7	

USB	USB PORT#	DESTINATION
	0	USB Port 0 (Sub-board)
	1	USB Port 1 (Sub-board)
	2	USB Port 2
	3	None
	4	MiniCard- WLAN
	5	MiniCard- WWAN
	6	None
	7	None
	8	Card Reader
	9	Camera
	10	None
	11	None
	12	None
13	None	

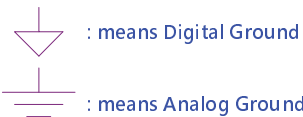
SMBUS Control Table

	SOURCE	MIINI1	BATT	MINI2	EXPRESS CARD	SODIMM
EC_SMB_CK1 EC_SMB_DA1	KB926	X	V	X	X	X
EC_SMB_CK2 EC_SMB_DA2	KB926	X	X	X	X	X
PCH_SMBCLK PCH_SMBDATA	PCH	V	X	V	V	X
MEM_SMBCLK MEM_SMBDATA	PCH	X	X	X	X	V

CLKOUT	DESTINATION
PCI0	None
PCI1	PCICLK1
PCI2	PCICLK2
PCI3	PCICLK3
PCI4	PCICLK4

CLK	DIFFERENTIAL	DESTINATION
	CLKOUT_PCIE0	10/100 LAN
	CLKOUT_PCIE1	MINI CARD- WLAN
	CLKOUT_PCIE2	MINI CARD- WWAN
	CLKOUT_PCIE3	None
	CLKOUT_PCIE4	None
	CLKOUT_PCIE5	None
	CLKOUT_PCIE6	None
	CLKOUT_PCIE7	None
CLKOUT_PCIE8	None	

Symbol Note :



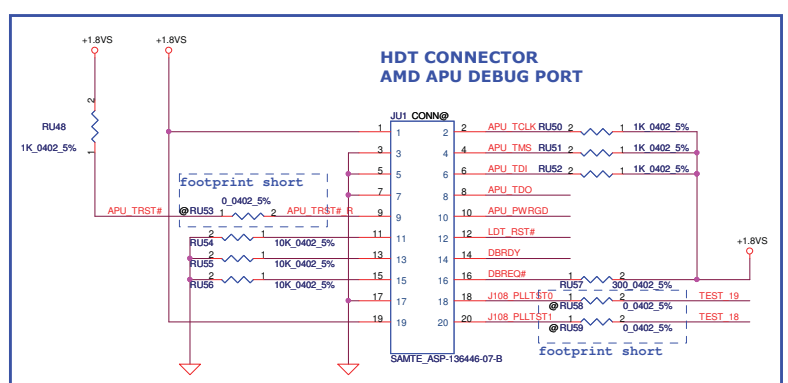
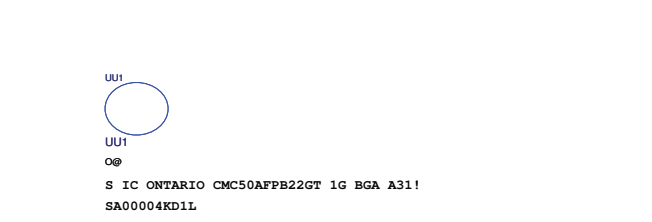
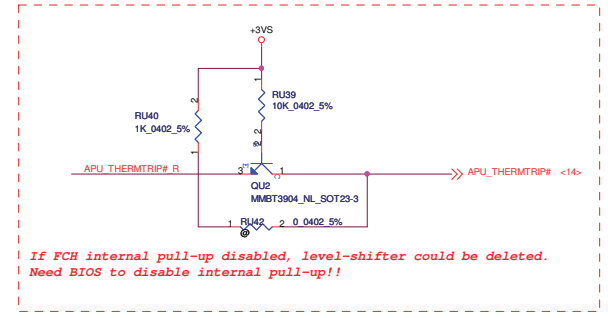
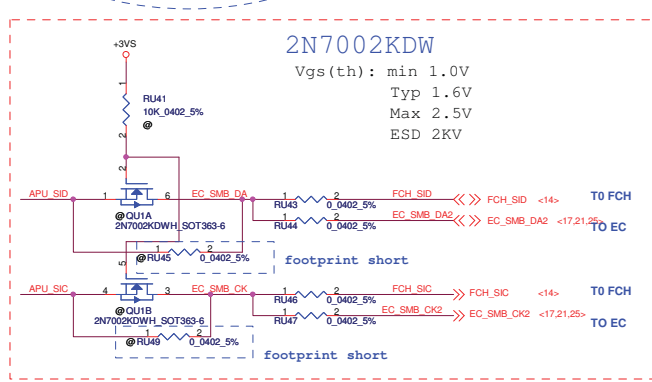
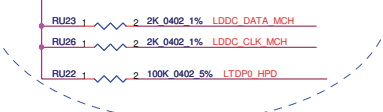
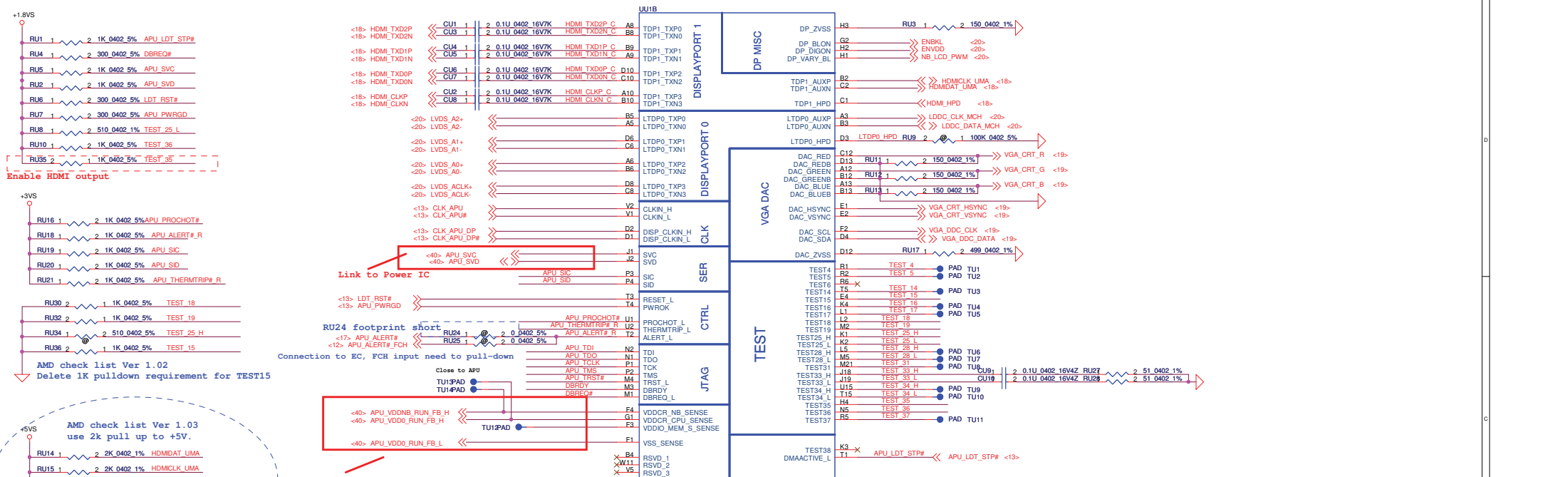
SATA	DESTINATION
SATA0	HDD1
SATA1	None
SATA2	None
SATA3	None
SATA4	None
SATA5	None

APU

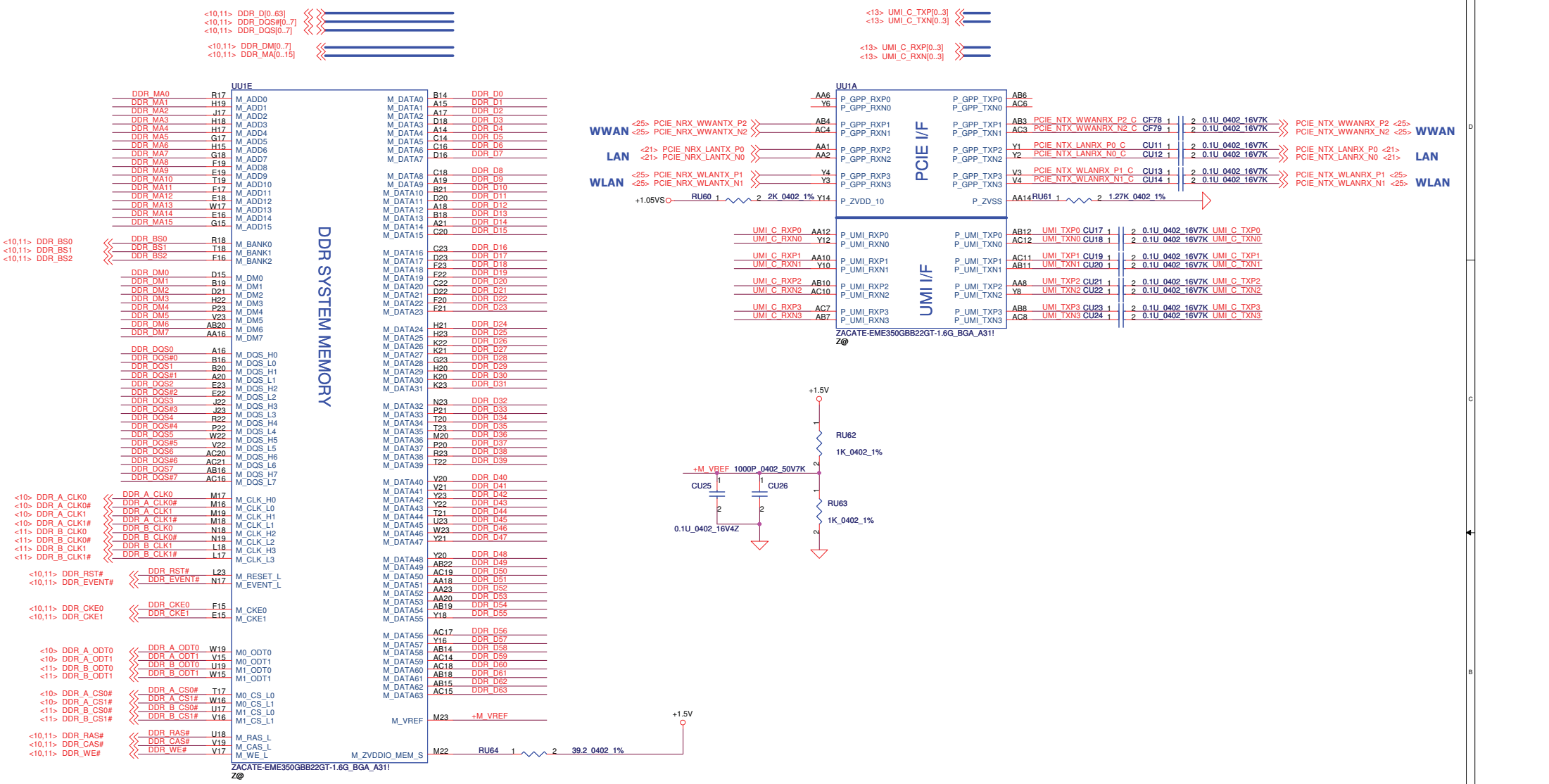
PCI EXPRESS	DESTINATION
Port0	None
Port1	WWAN
Port2	10/100
Port3	WLAN

FCH

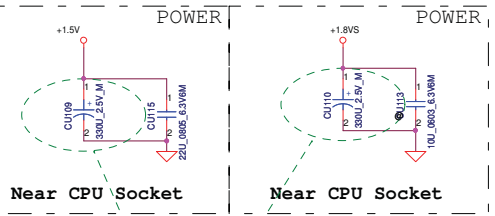
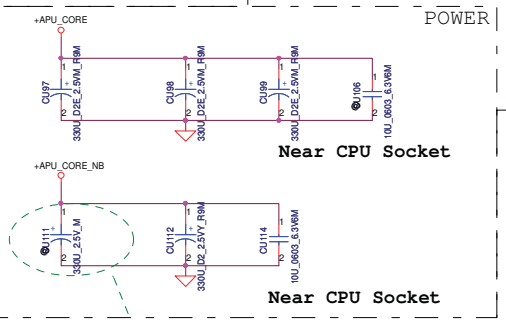
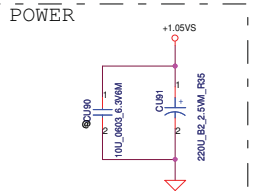
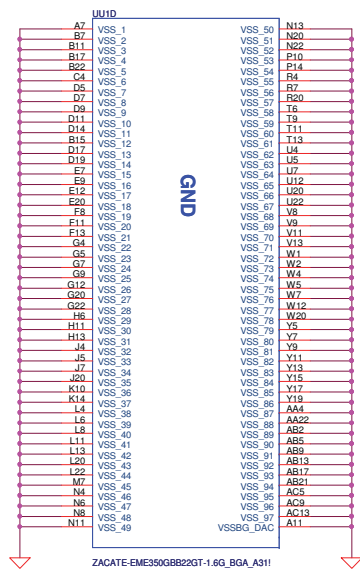
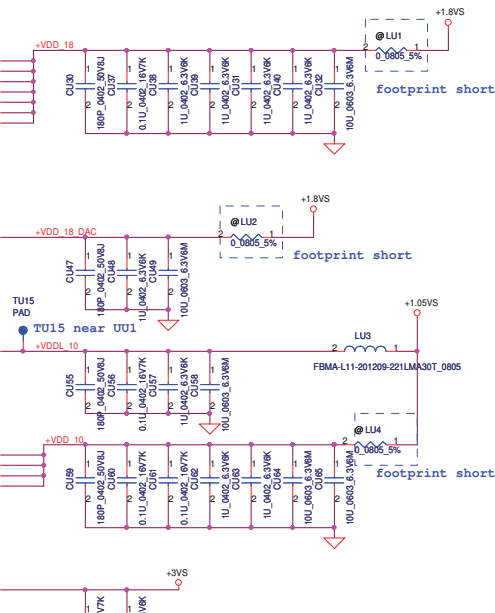
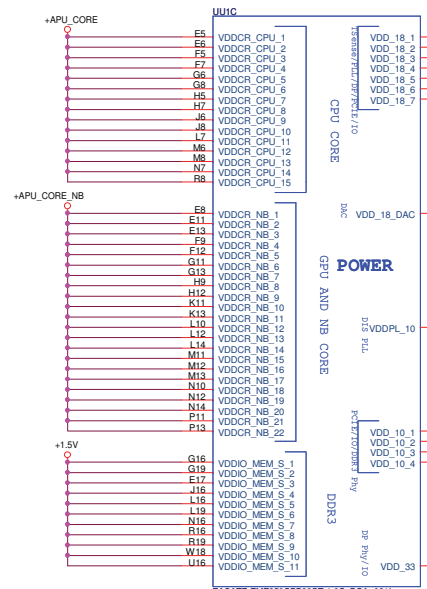
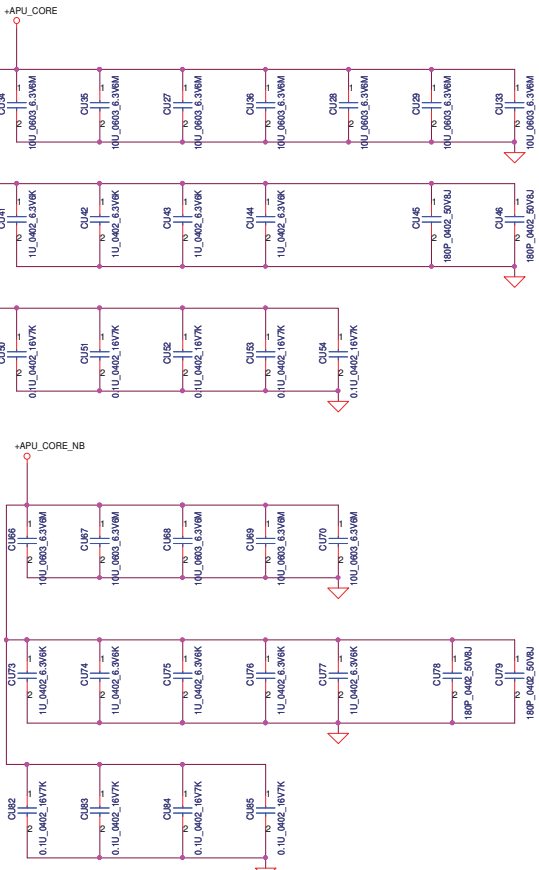
PCI EXPRESS	DESTINATION
Port0	None
Port1	None
Port2	None
Port3	None



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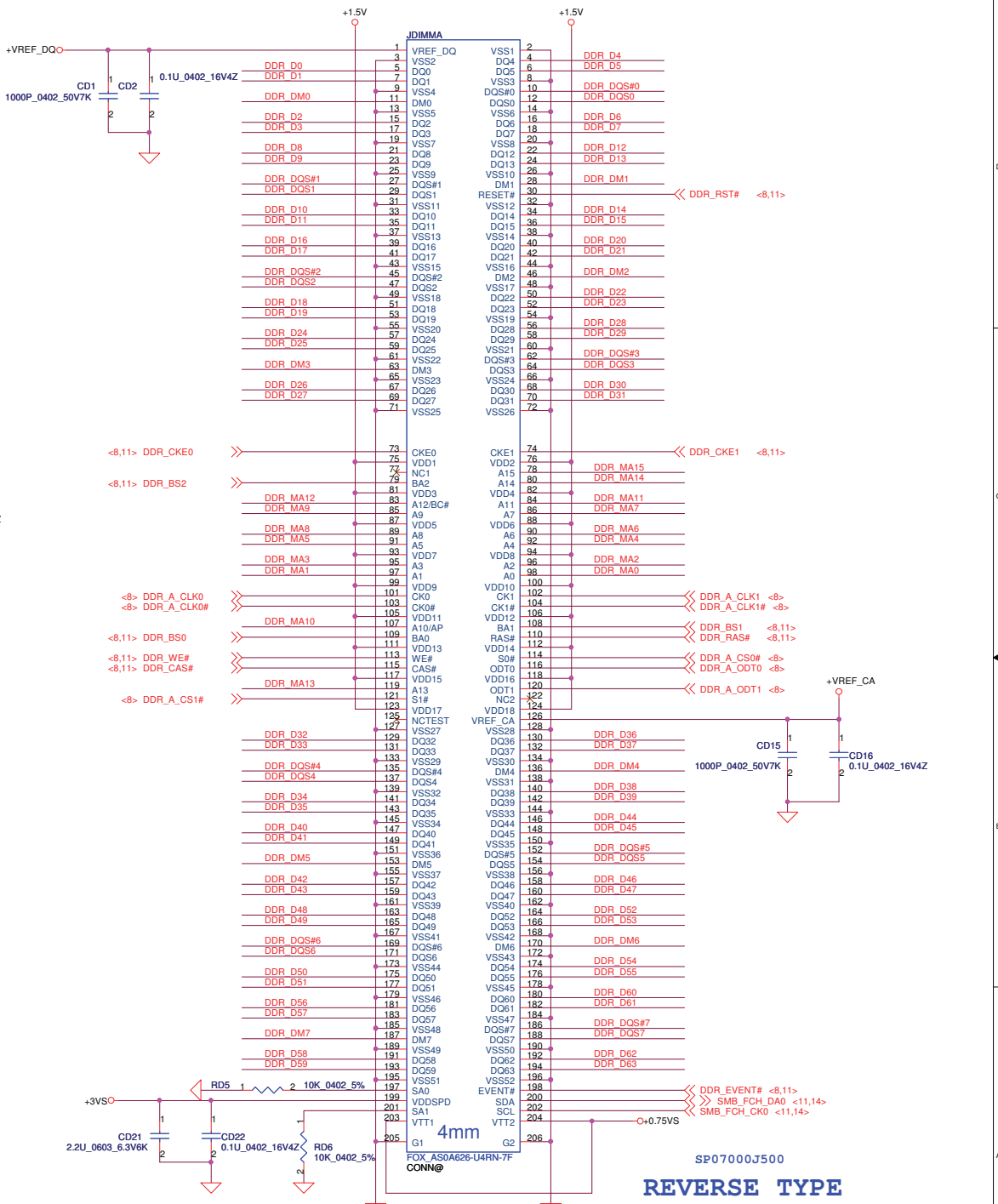
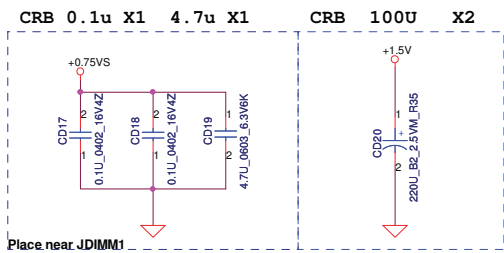
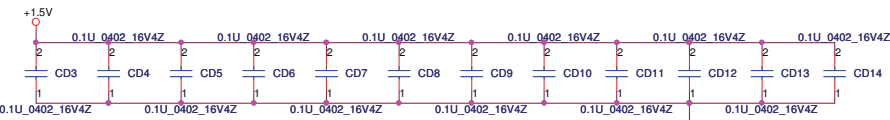
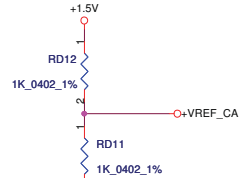
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(330uF_6.3V_4.2L_ESR17m) *1=(SF000002Z00)

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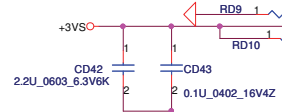
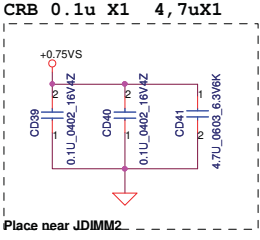
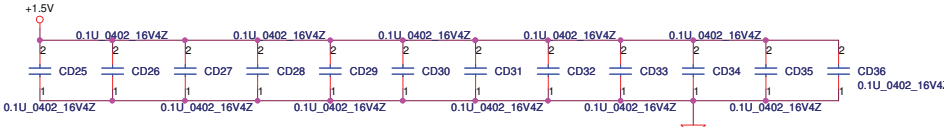
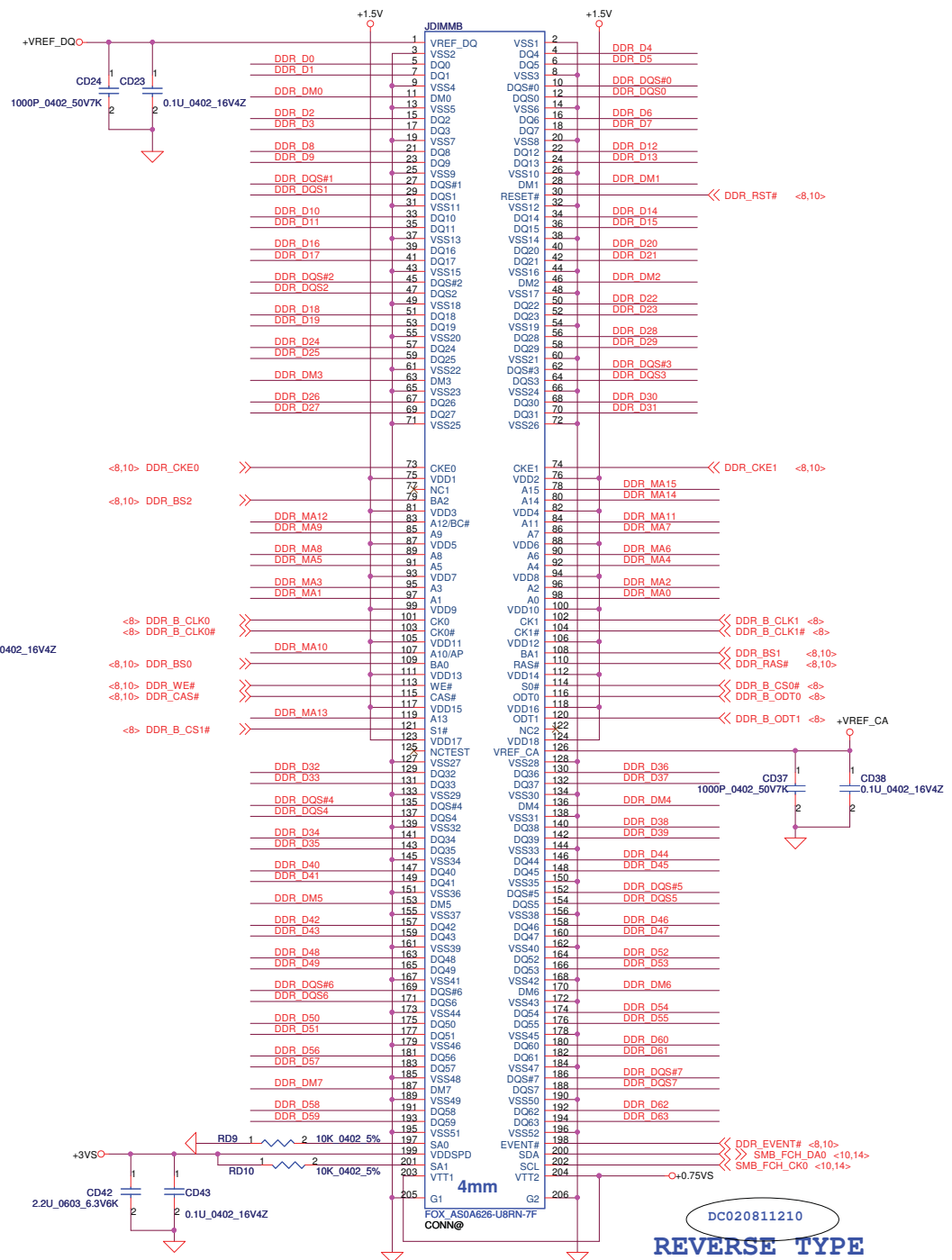
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SP07000J500
REVERSE TYPE

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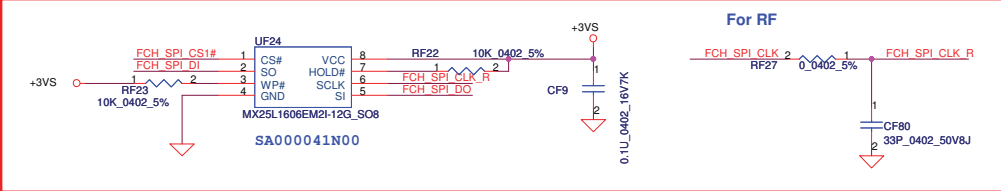
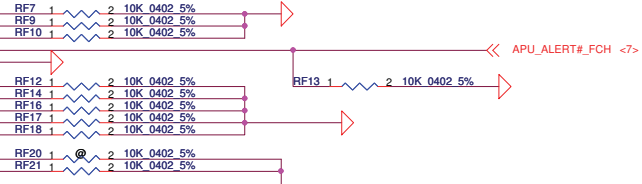
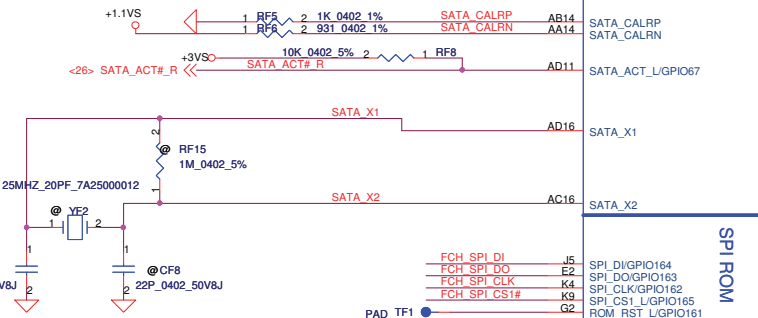
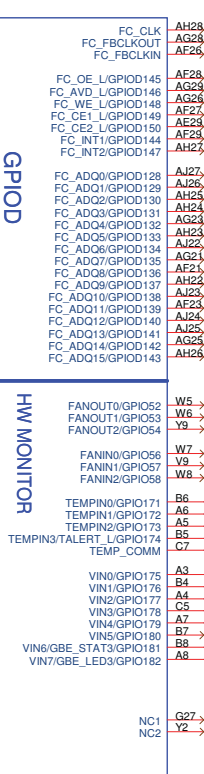
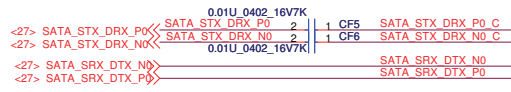
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DC020811210
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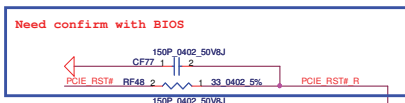
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HDD



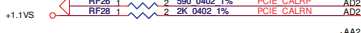
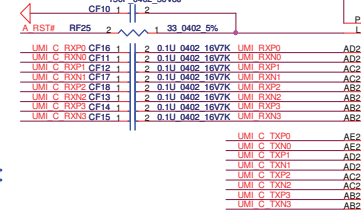
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				LA-7161P	
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<-> UMI_C_RXP0.3
<-> UMI_C_RXN0.3

<-> UMI_C_TXP0.3
<-> UMI_C_TXN0.3



<-> CLK_APU_DP
<-> CLK_APU_DP#

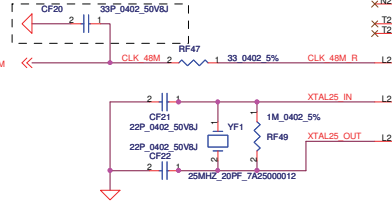
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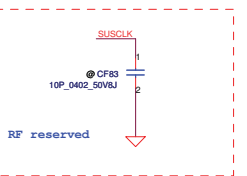
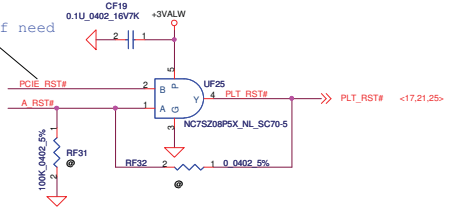
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<-25> CLK_PCIE_WWAN_N

Place close to UF1



it can be swap if need



PCI EXPRESS I/F

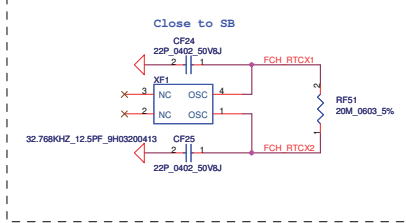
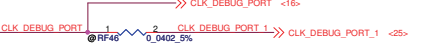
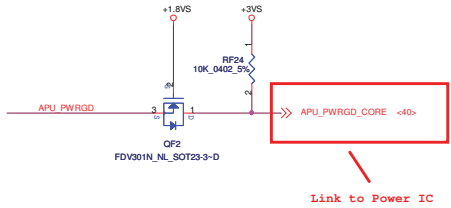
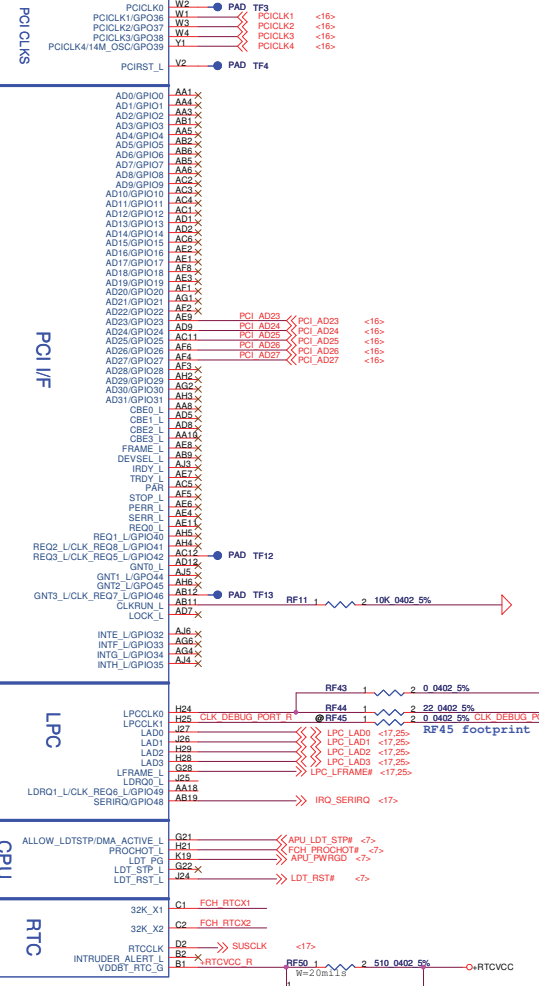
PCI I/F

CLOCK GENERATOR

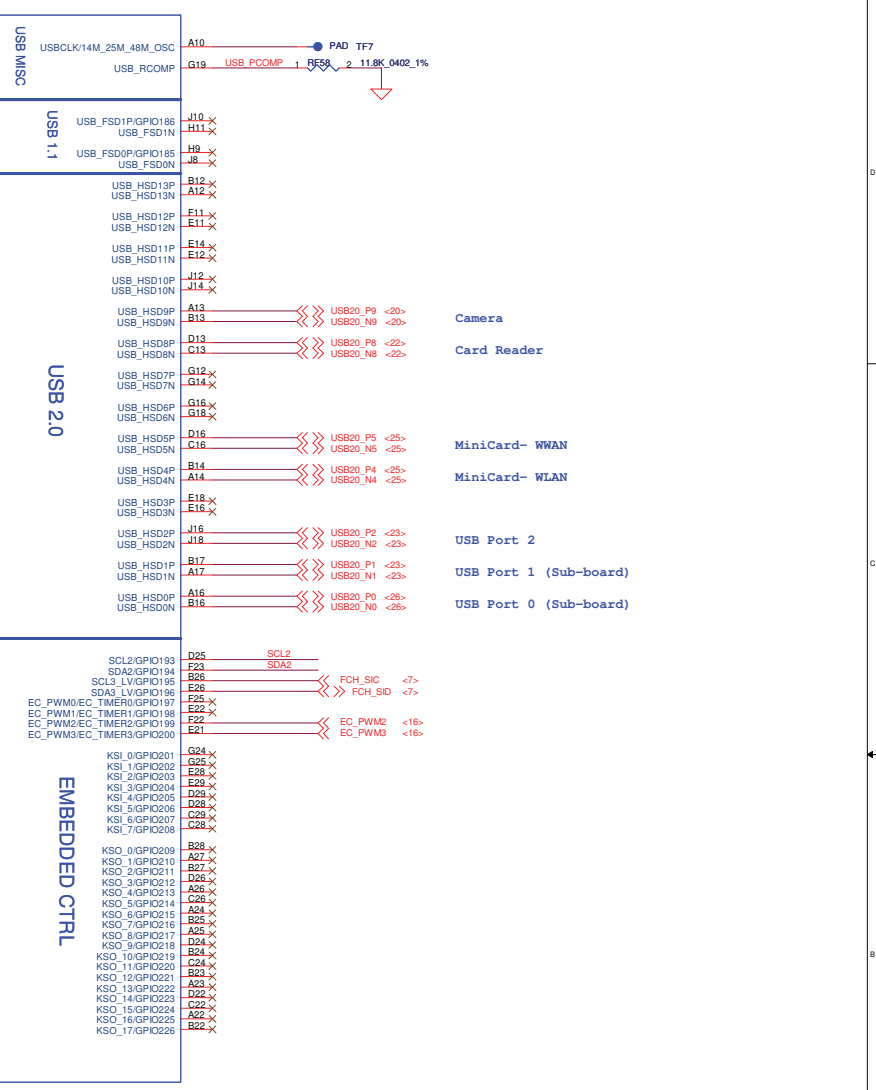
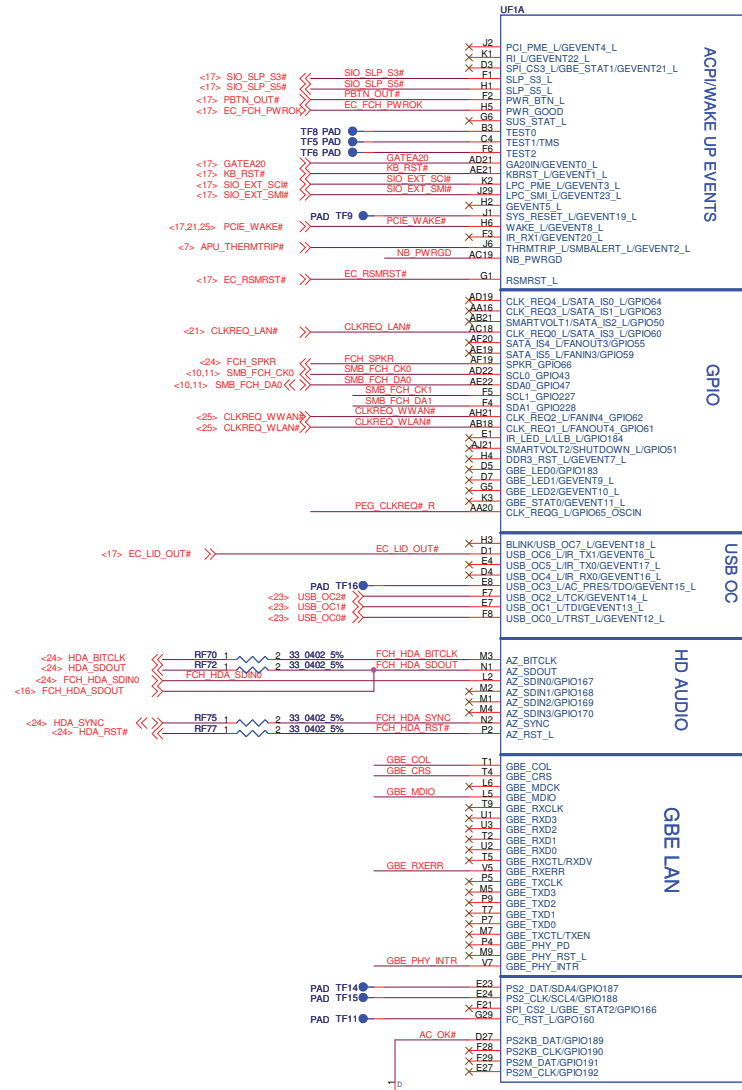
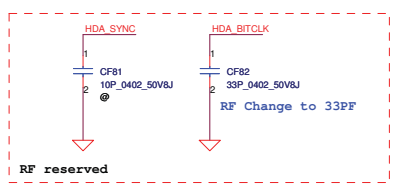
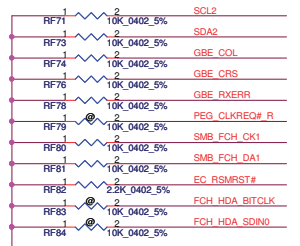
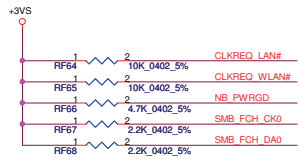
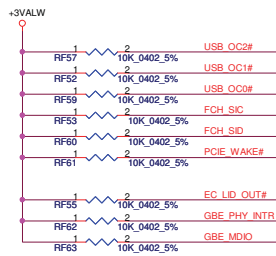
LPC

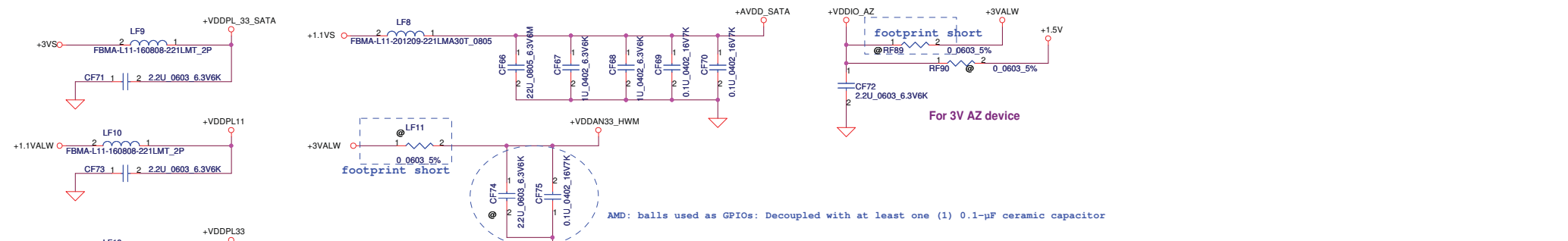
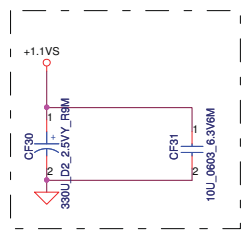
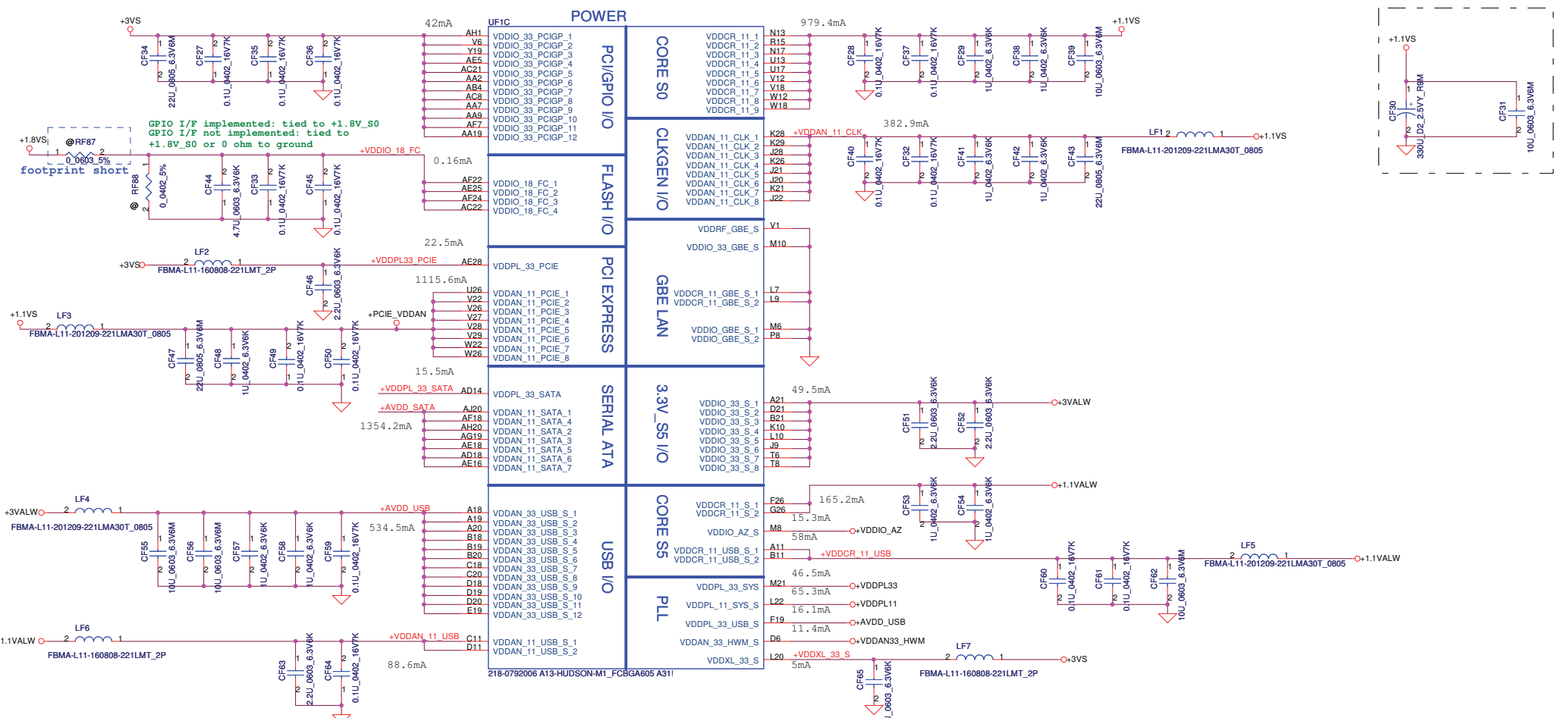
CPU

RTC



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Issued Date	2010/07/31	Deciphered Date	Title	
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Date:	Wednesday, January 05, 2011	Sheet	13	of 43



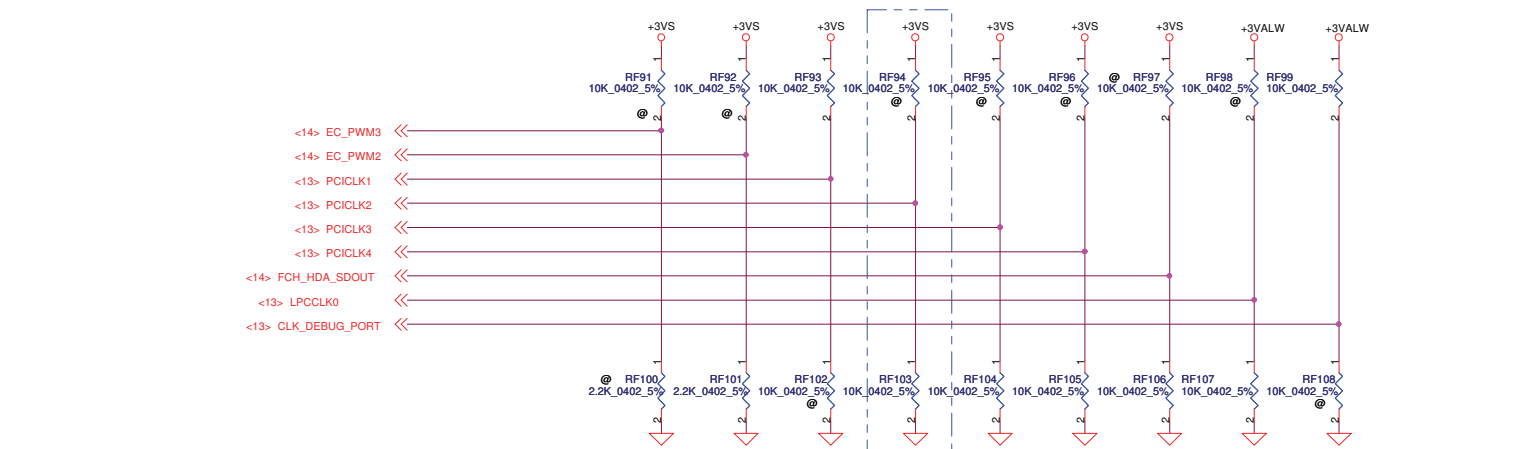
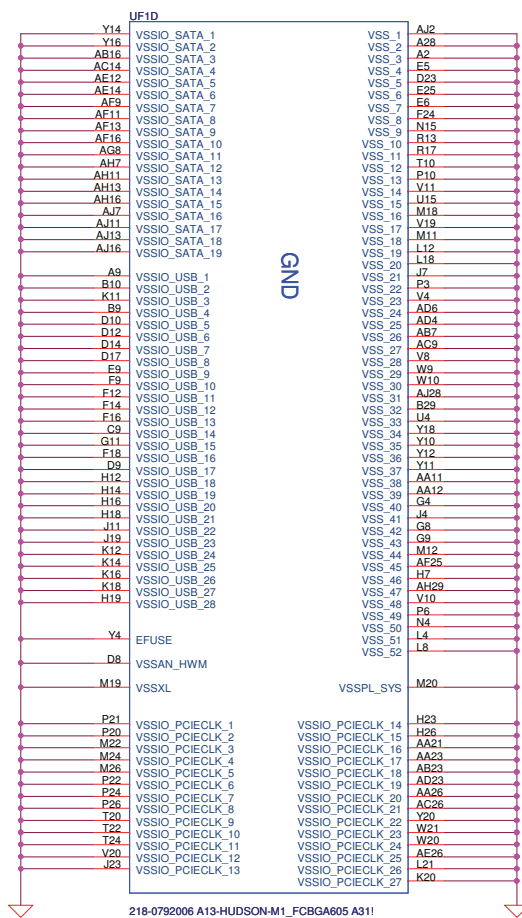


AMD: HWM not Implemented or HWM balls used as GPIOs: Bead not used.

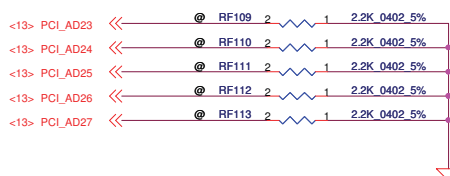
Security Classification	Compal Secret Data	
Issued Date	2010/07/31	Deciphered Date
		2011/07/31

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Title			Compal Electronics, Inc.	
Size			FCH PWR	
Custom	Document Number	LA-7161P		Rev
				1.0
Date:	Wednesday, January 05, 2011	Sheet	15	of 43

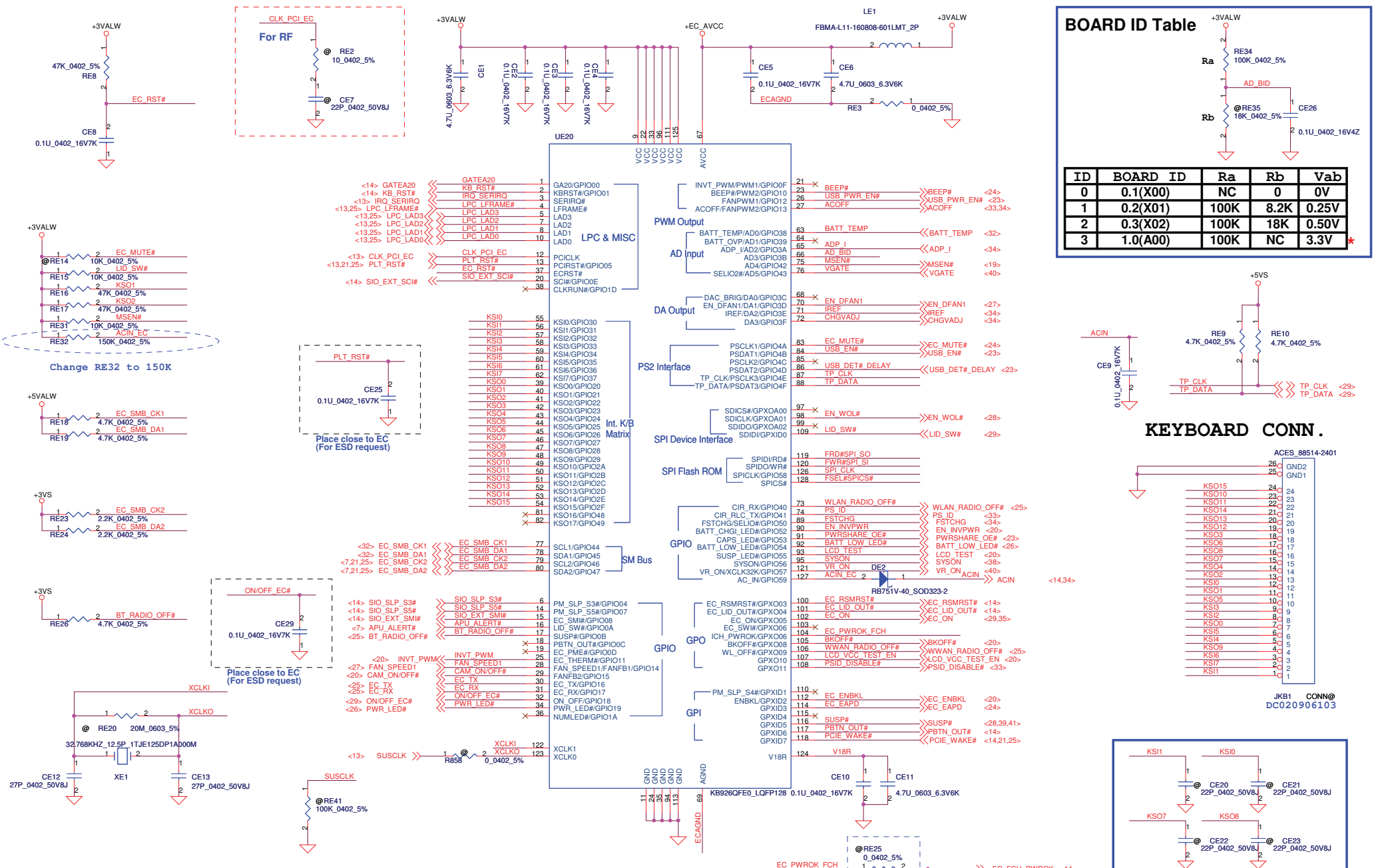


Watchdog timer on NB_PWRGD
enable for pull-up
disable for pull-down
20100527



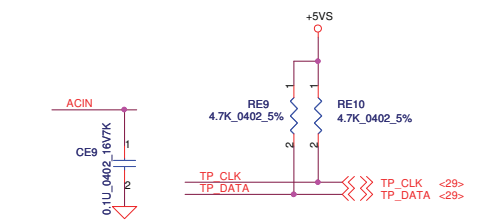
Net Name	Description
<i>PCI_AD27</i>	0 : Bypass internal PLL clock 1 : Use internal PLL-generated PLL CLK *
<i>PCI_AD26</i>	0 : ILA auto run enable 1 : ILA auto run disable *
<i>PCI_AD25</i>	0 : Bypass internal FC Clk 1 : Use internal PLL FC Clk * NEED CHECK
<i>PCI_AD24</i>	0 : Getting the value from I2C EPROM 1 : Disable I2C ROM * NEED CHECK
<i>PCI_AD23</i>	0 : Reserved 1 : Required setting (use ROMTYPE straps to determine the ROM type) *

Net Name	Description															
<i>CLK_PCI_EC_R</i>	0 : Integrated Microcontroller (IMC) Disabled * 1 : Integrated Microcontroller (IMC) Enabled															
<i>EC_PWM3</i>	<table border="1"> <thead> <tr> <th>EC_PWM3</th> <th>EC_PWM2</th> <th>ROM TYPE</th> </tr> </thead> <tbody> <tr> <td>x</td> <td>0</td> <td>SPI ROM *</td> </tr> <tr> <td>x</td> <td>x</td> <td>Reserved</td> </tr> <tr> <td>0</td> <td>0</td> <td>Reserved</td> </tr> <tr> <td>0</td> <td>x</td> <td>LPC ROM</td> </tr> </tbody> </table>	EC_PWM3	EC_PWM2	ROM TYPE	x	0	SPI ROM *	x	x	Reserved	0	0	Reserved	0	x	LPC ROM
EC_PWM3	EC_PWM2	ROM TYPE														
x	0	SPI ROM *														
x	x	Reserved														
0	0	Reserved														
0	x	LPC ROM														
<i>CLK_DEBUG_PORT</i>	0 : External clock mode. 1 : Integrated clock mode. *															
<i>PCICLK1</i>	0 : Force PCIe interface at Gen I mode. 1 : PCIe interface is at Gen II mode. *															
<i>PCICLK2</i>	0 : Disable the boot fail timer function. * 1 : Enable the boot fail timer function.															
<i>PCICLK3</i>	0 : Disable Debug Straps. * 1 : Select external Debug Straps.															
<i>PCICLK4</i>	0 : Required setting for integrated clock mode. * 1 : Reserved.															
<i>HDA_SDOOUT_R</i>	0 : Required setting for integrated clock mode. * 1 : Reserved (Hudson-1 does not support the lower power mode).															

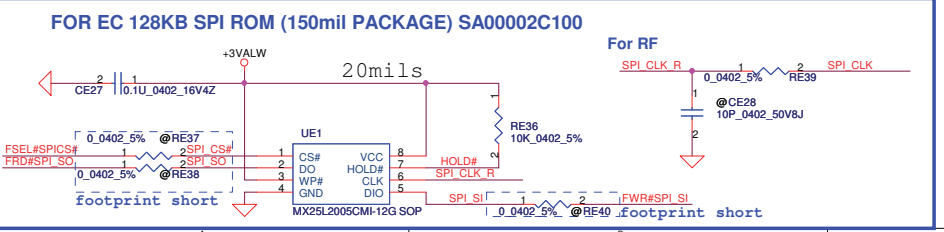
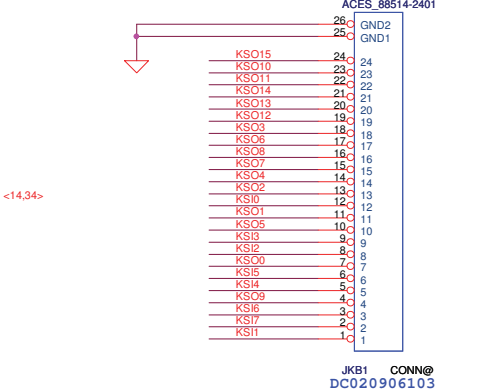


BOARD ID Table

ID	BOARD ID	Ra	Rb	Vab
0	0.1(X00)	NC	0	0V
1	0.2(X01)	100K	8.2K	0.25V
2	0.3(X02)	100K	18K	0.50V
3	1.0(A00)	100K	NC	3.3V *



KEYBOARD CONN.



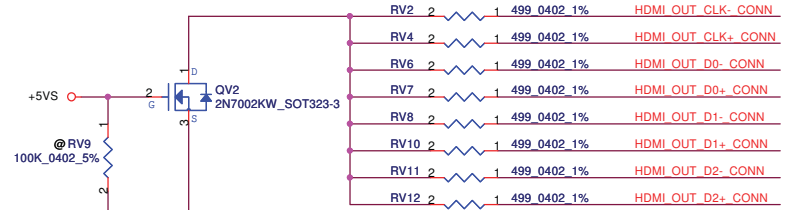
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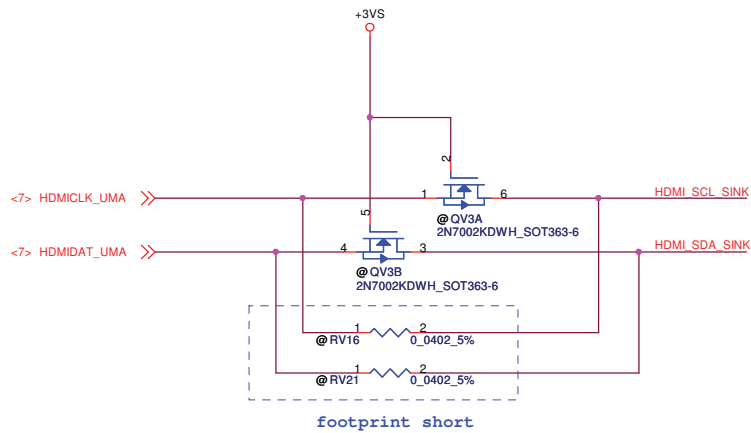
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Compal Electronics, Inc.			
Title ENE-KB926/KB Conn			
Size LA-7161P			
Date Wednesday, January 05, 2011	Document Number LA-7161P	Sheet 17	Rev 1.0

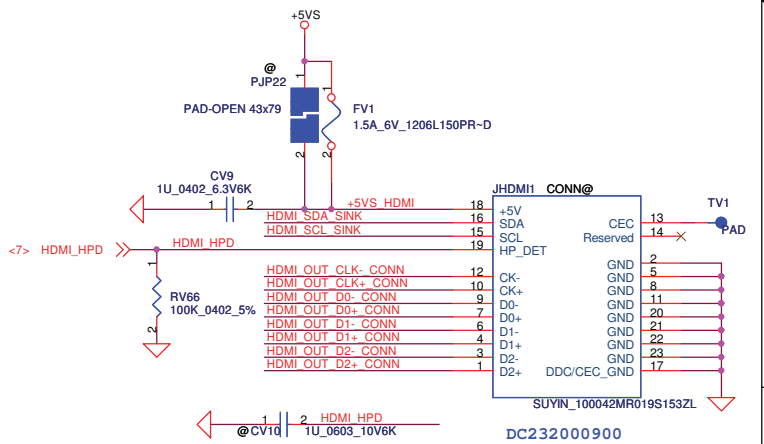
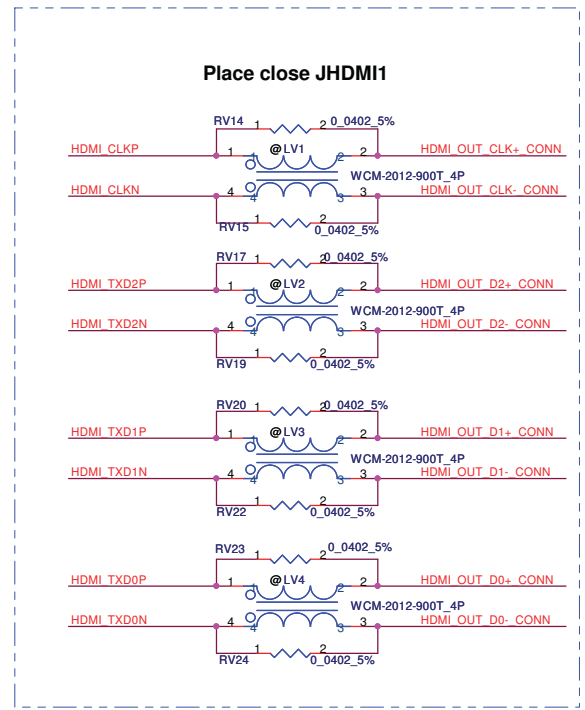
- <7> HDMI_TXD2P >> HDMI_TXD2P
- <7> HDMI_TXD2N >> HDMI_TXD2N
- <7> HDMI_TXD1P >> HDMI_TXD1P
- <7> HDMI_TXD1N >> HDMI_TXD1N
- <7> HDMI_TXD0P >> HDMI_TXD0P
- <7> HDMI_TXD0N >> HDMI_TXD0N
- <7> HDMI_CLKP >> HDMI_CLKP
- <7> HDMI_CLKN >> HDMI_CLKN



PLACE PULL DOWN RESISTORS CLOSE TO DIFFERENTIAL PAIRS CONNECTED TO SOLID GROUND FLOOD WHICH IS CONTROLLED BY THE FET
AVOID STUBS TO ALL DIFFERENTIAL TRACES



footprint short



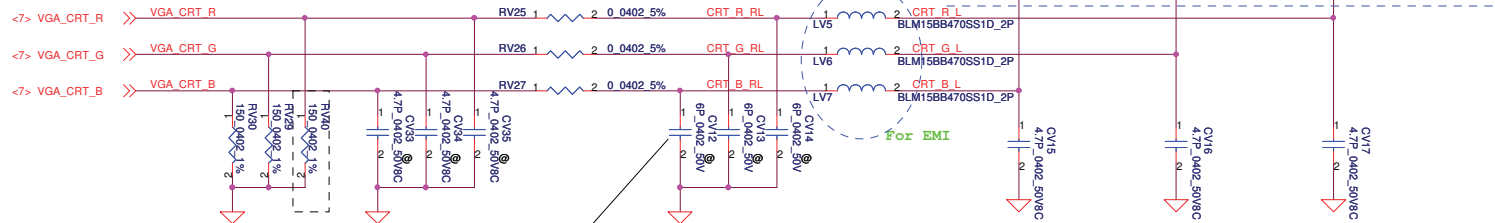
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		Compal Electronics, Inc.	
		HDMI Conn.	
Title	Document Number		Rev
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CRT

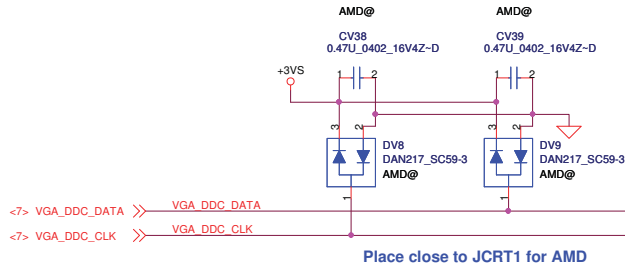
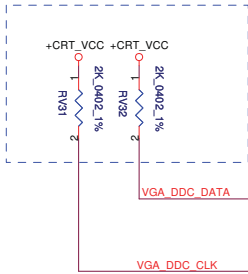
Place close to JCRT1 for AMD

Change to BLM15BB470SS1D (47 OHM BEAD)

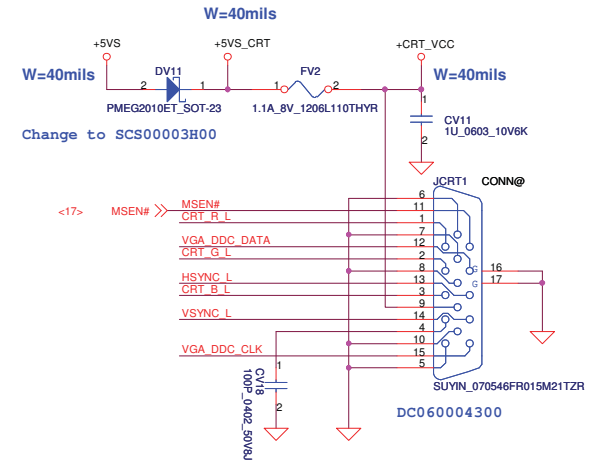


SE00000AY80
change to 6P_0402
Need apply CIS symbol

AMD check list Ver 1.03
use 2k pull up to +5V.



Place close to JCRT1 for AMD

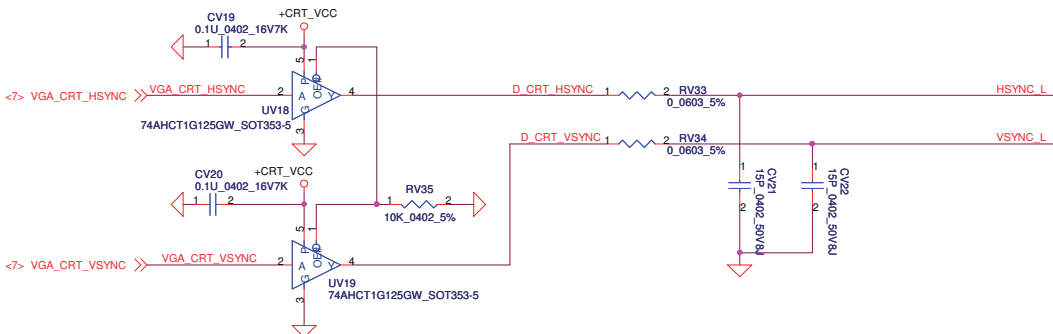


W=40mils

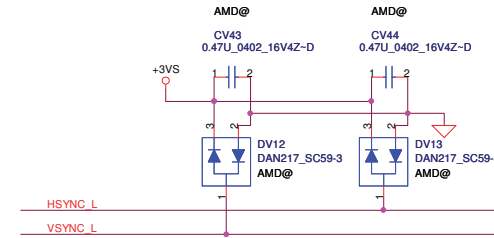
W=40mils

W=40mils

Change to SCS00003H00



Place close to JCRT1 for AMD



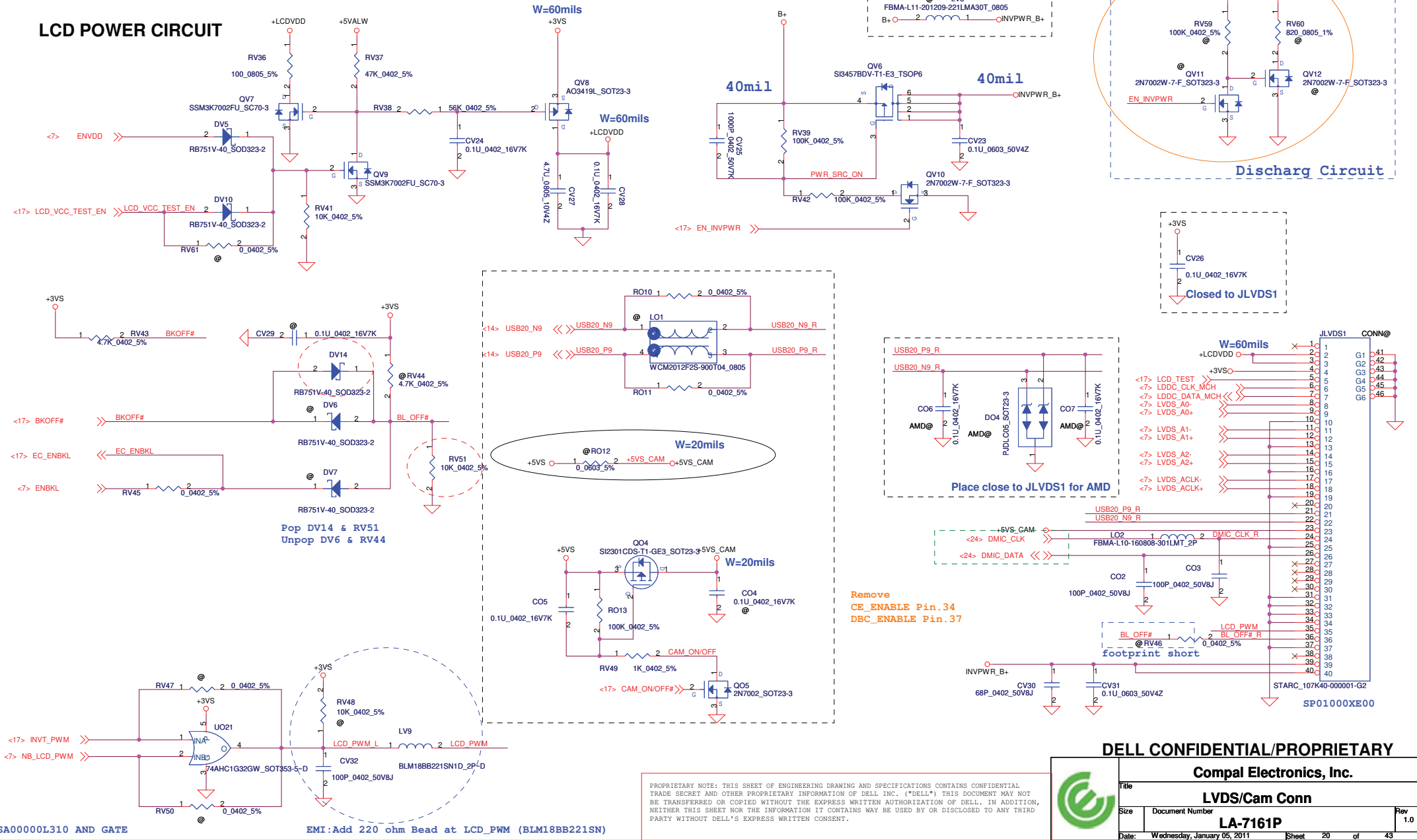
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Title VGA Conn.		
Size	Document Number LA-7161P	Rev 1.0
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LCD POWER CIRCUIT



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LVDS/Cam Conn
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SA00000L310 AND GATE

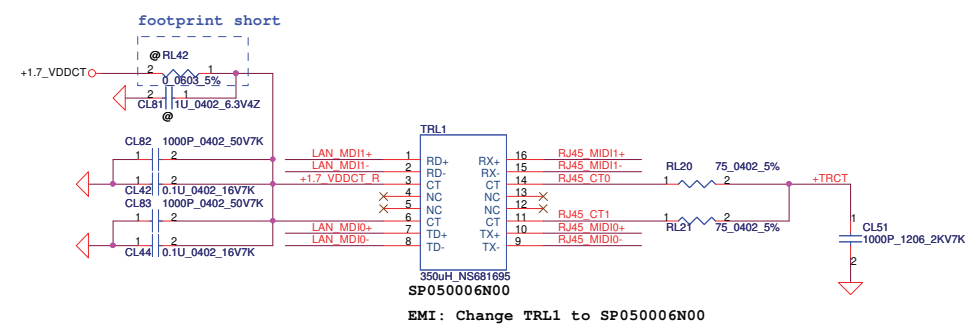
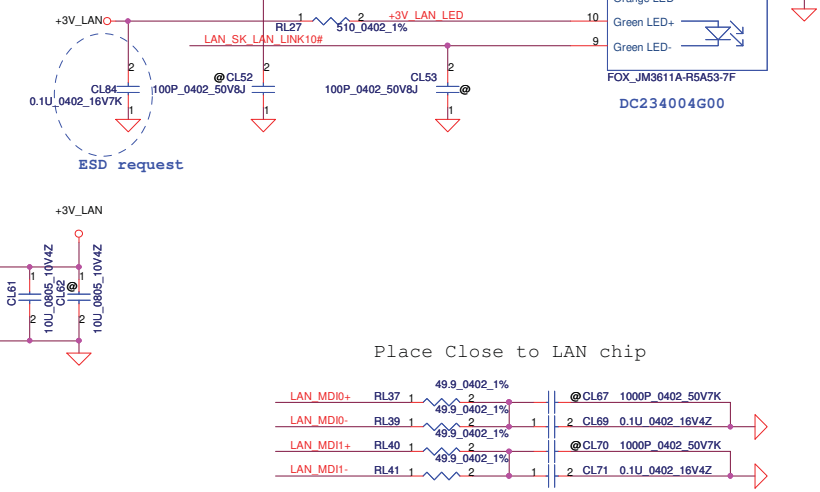
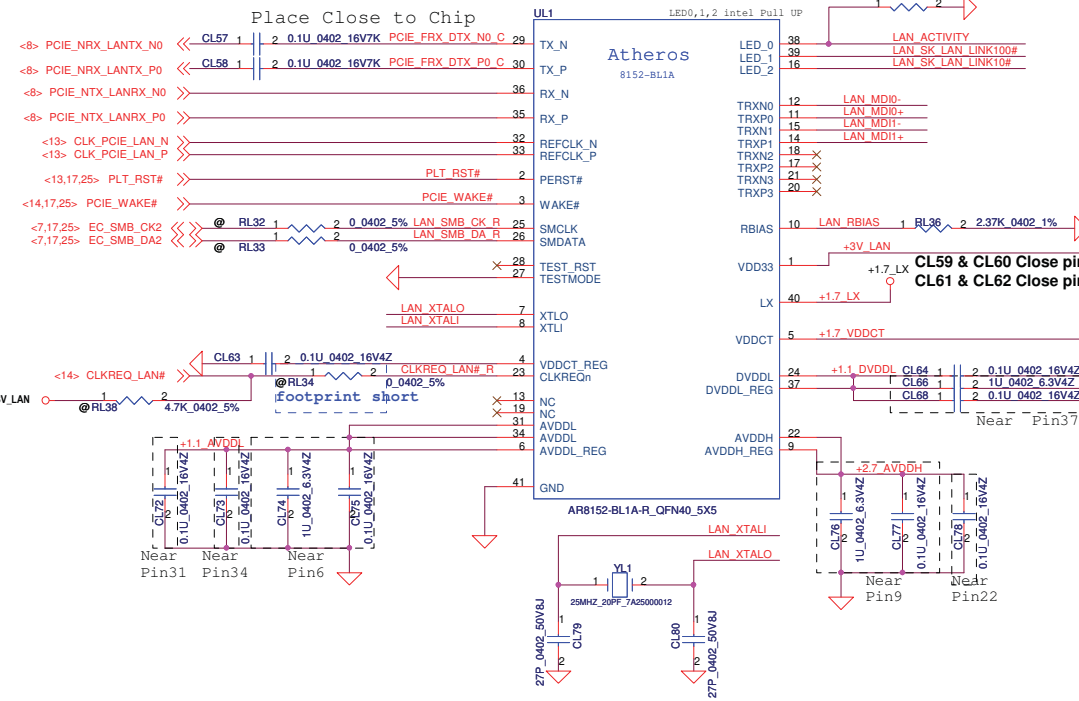
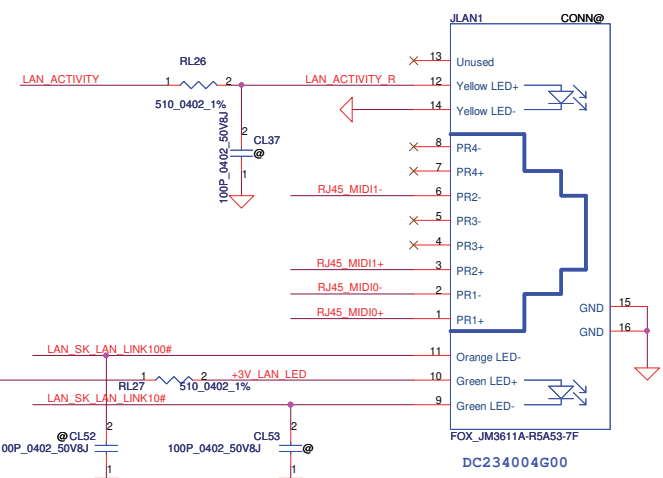
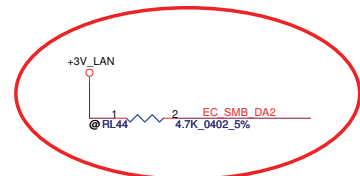
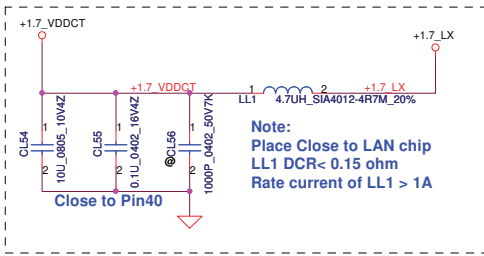
EMI:Add 220 ohm Bead at LCD_PWM (BLM18B221SN)

Remove CE_ENABLE Pin.34 DBC_ENABLE Pin.37

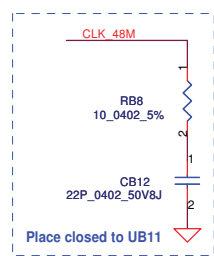
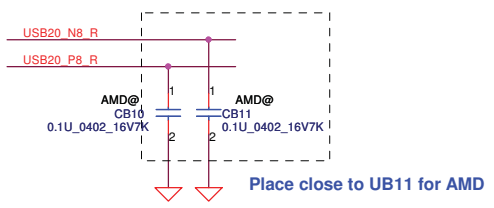
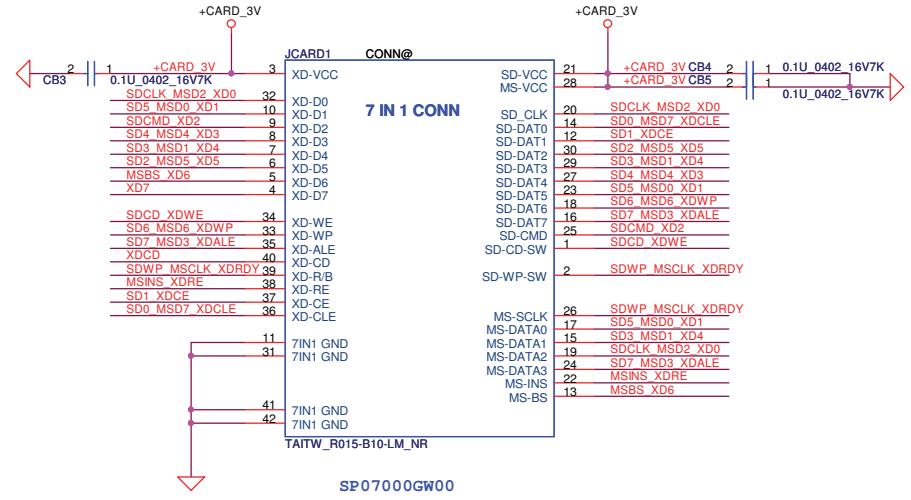
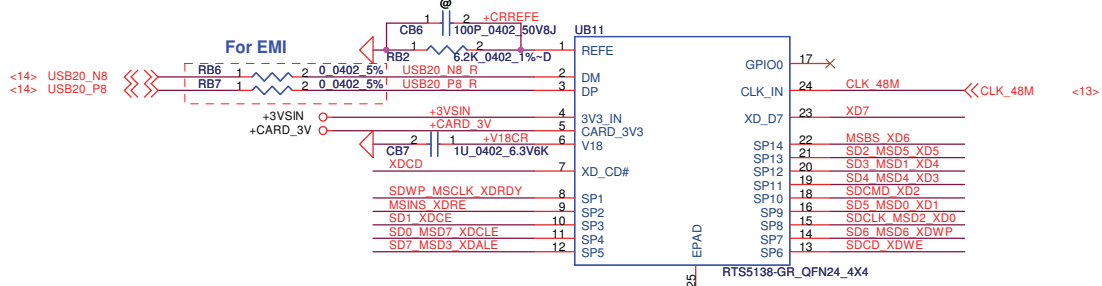
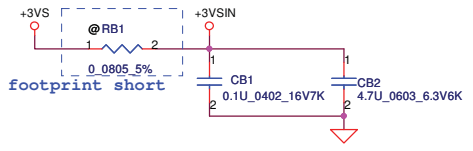
footprint short

Closed to JLVDS1

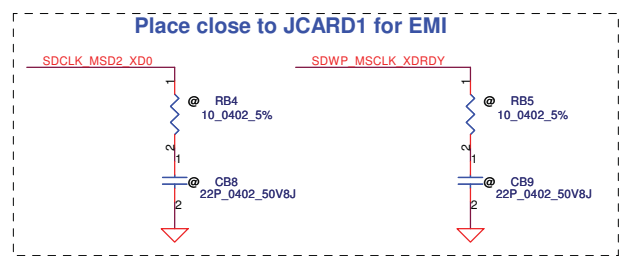
Place close to JLVDS1 for AMD



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				Sheet	21 of 43



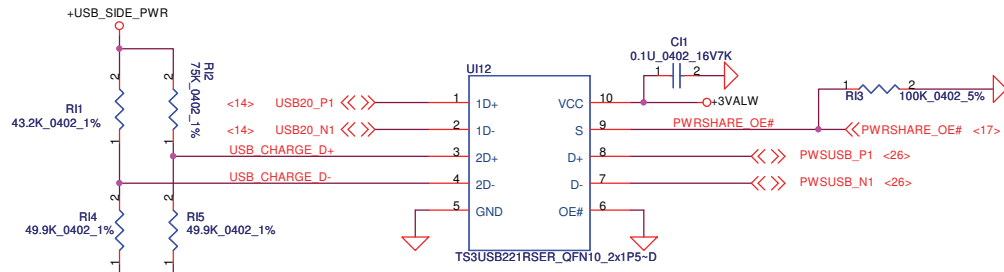
(For RF request)



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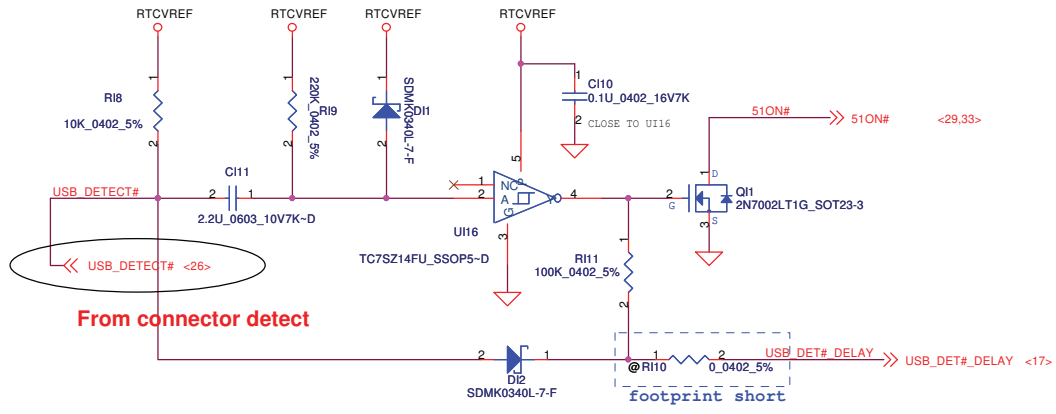
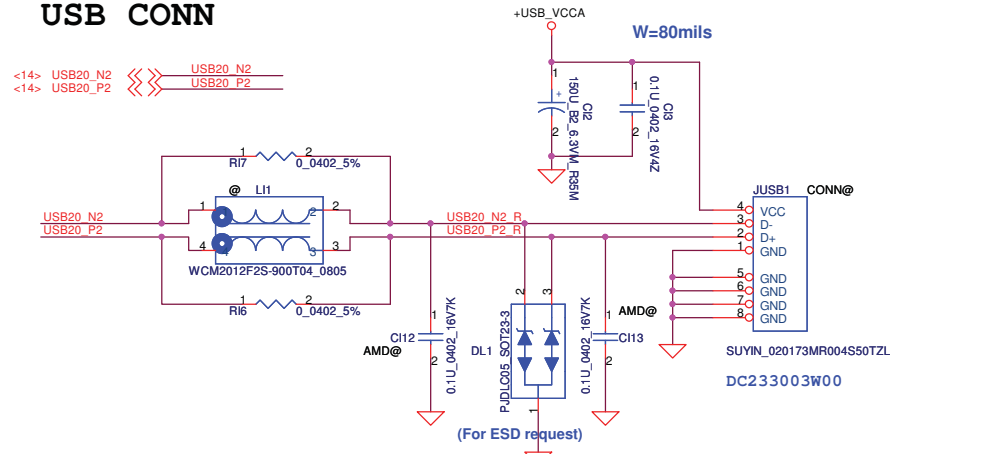
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		Card Reader RTS5138	
Title	Document Number		Rev
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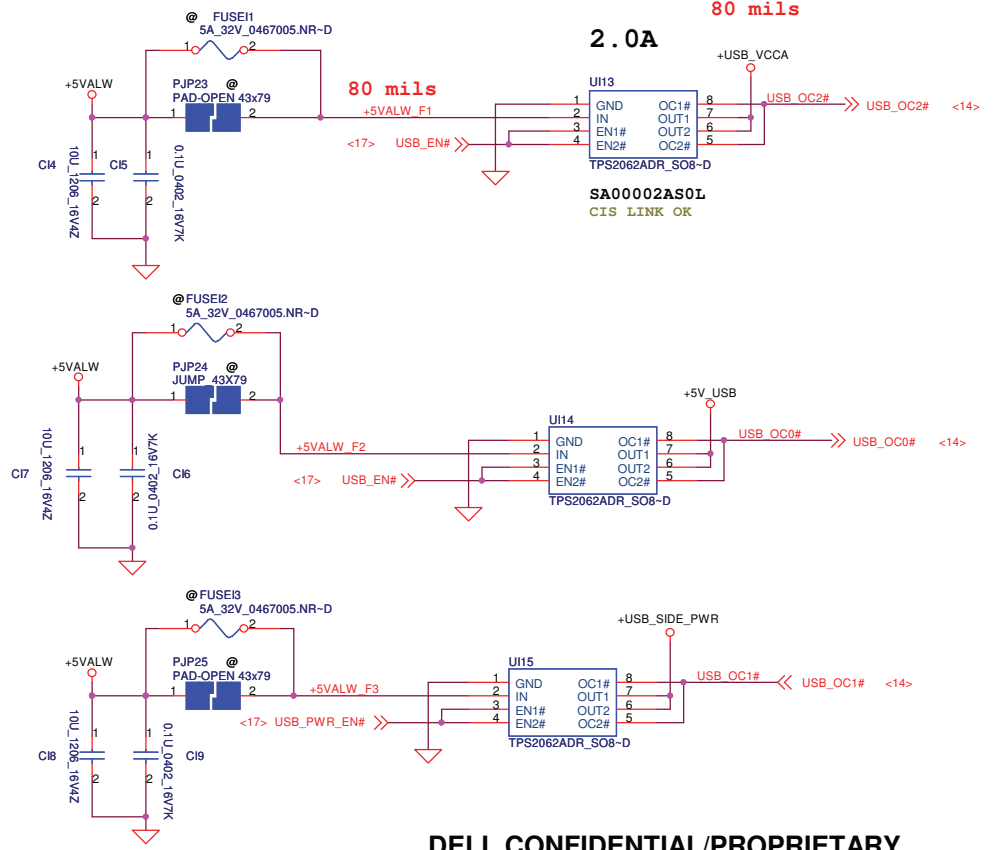


S	OE#	Function
X	H	Disconnect
L	L	D=1D
H	L	D=2D

USB CONN



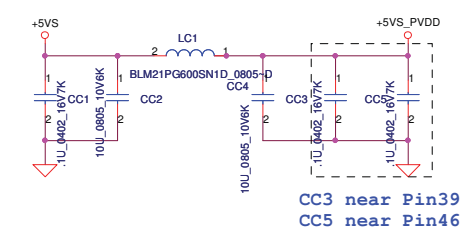
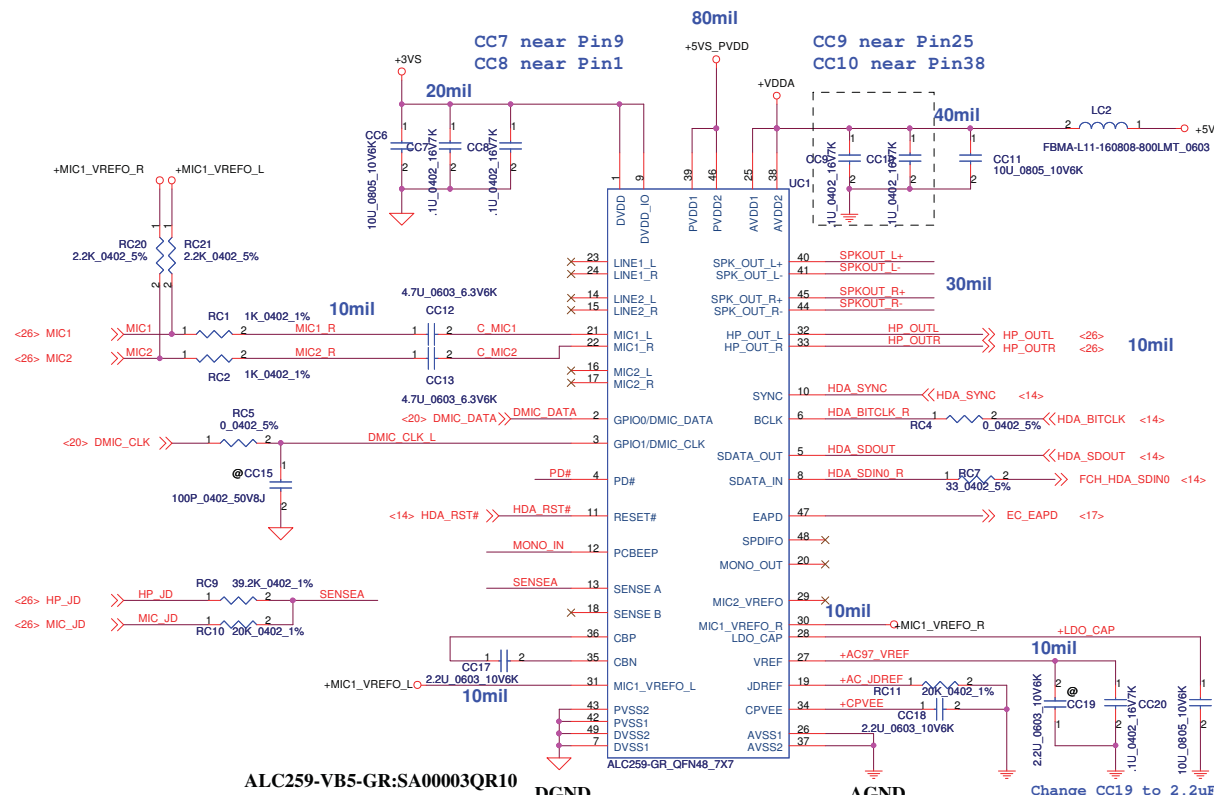
Power share



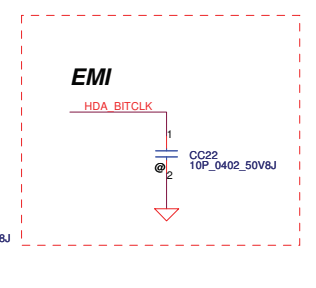
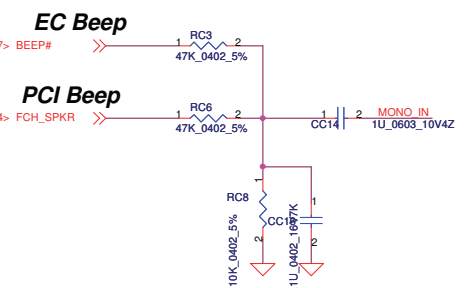
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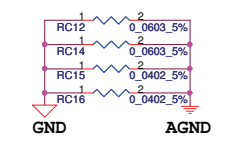
		Compal Electronics, Inc.	
		USB/POWER Share	
Size	Document Number	LA-7161P	
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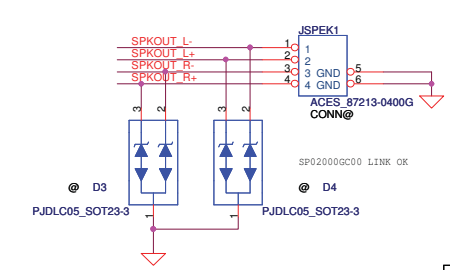
Beep sound



Change CC19 to 2.2uF for pop noise or class D noise



Speaker Connector



For Power on/off de-pop circuit and system booting warning signal:
Please system BIOS Engineer Note:
1.If you want the system make warning signal after power on
Please let EC_MUTE# high first
2.When you want to exit your BIOS programming code
Please let EC_MUTE# Low.
(The programming is difference from before)

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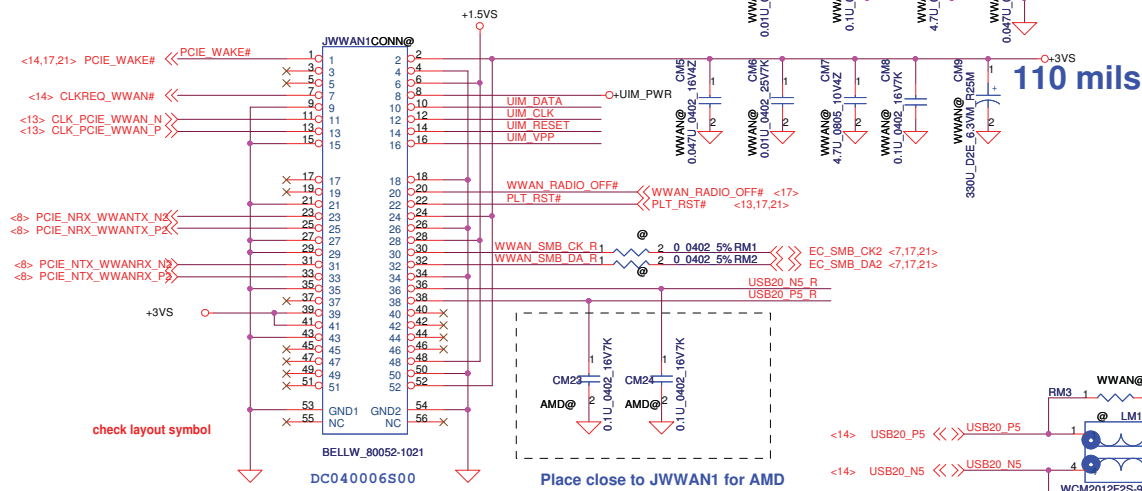


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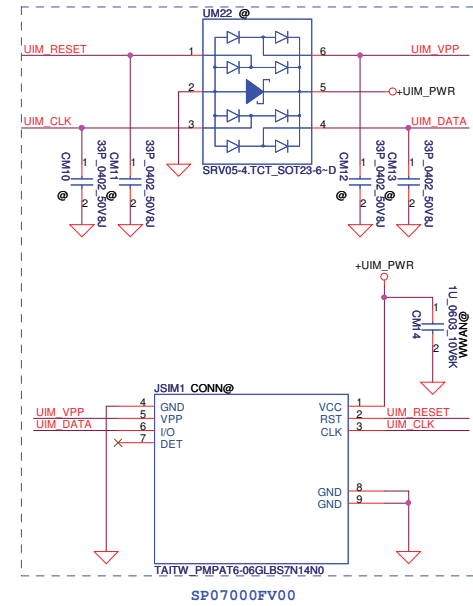
Compal Electronics, Inc.

Title			Codex ALC259		
Size	Document Number	LA-7161P		Rev	1.0
Date:	Wednesday, January 05, 2011	Sheet	24	of	43

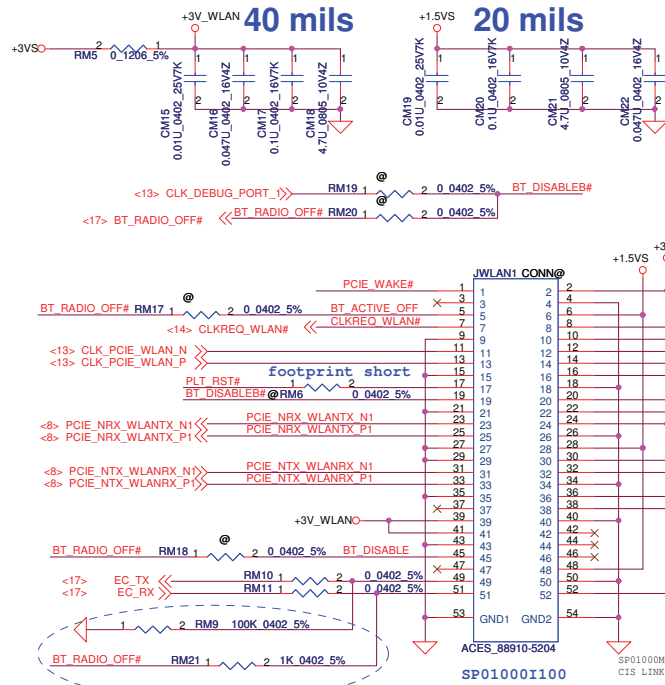
WWAN PCIE MiniCard



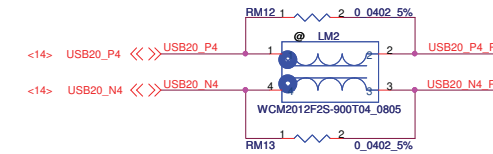
SIM Card



WLAN/WIMAX PCIE Mini Card



PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+~9%	1000	750	
+3.3Vaux	+~9%	330	250	250 (Wake enable) 5 (Not wake enable)
+1.5V	+~5%	500	375	NA

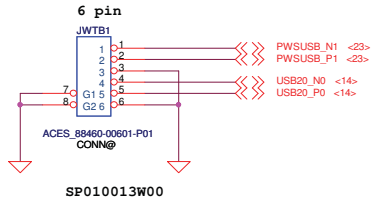


RF:Andros MLK will use DW1702 combo card

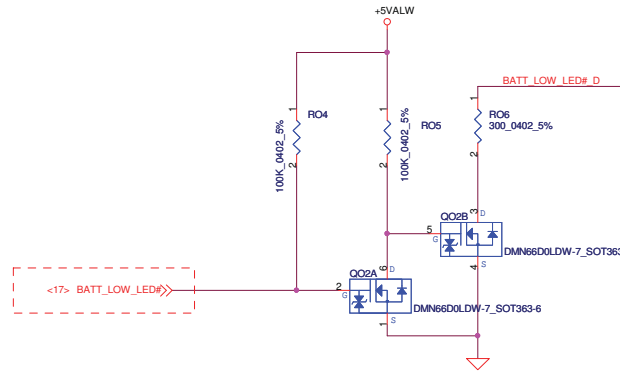
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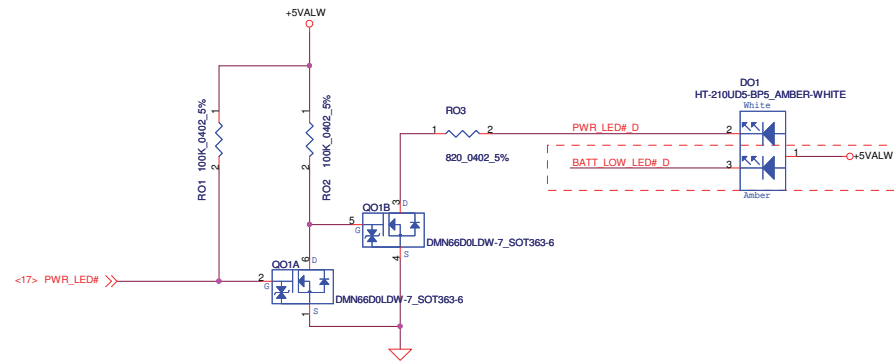
Compal Electronics, Inc.			
File: WLAN/WWAN/BT			
Size	Document Number		Rev
	LA-7161P		1.0
Date:	Wednesday, January 05, 2011	Sheet	25 of 43



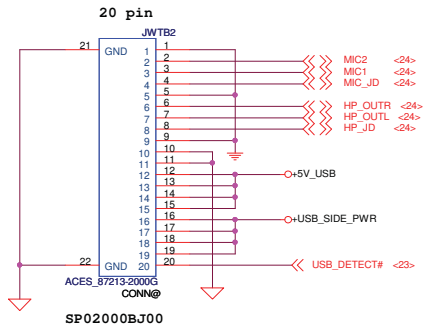
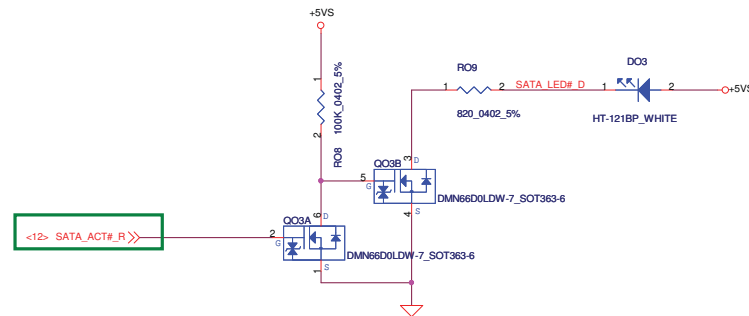
BATT CHARGE



Power LED



HD LED



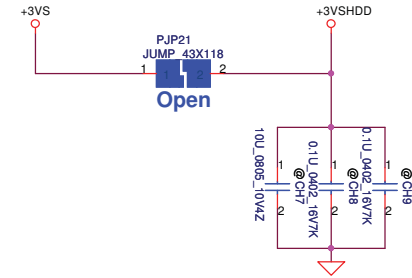
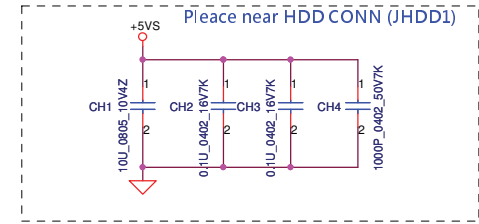
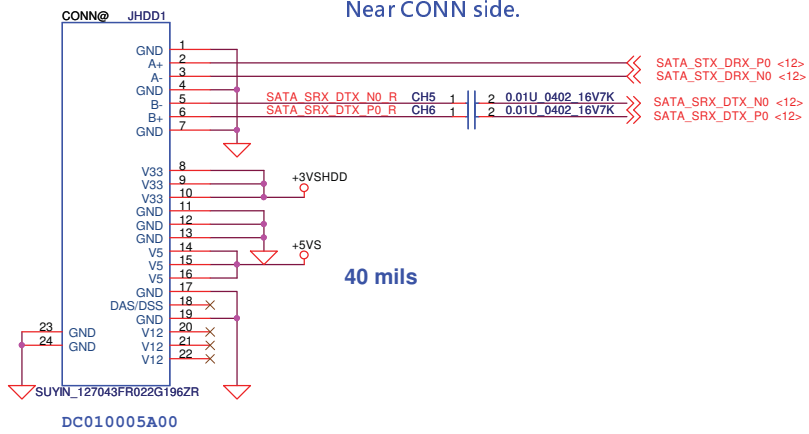
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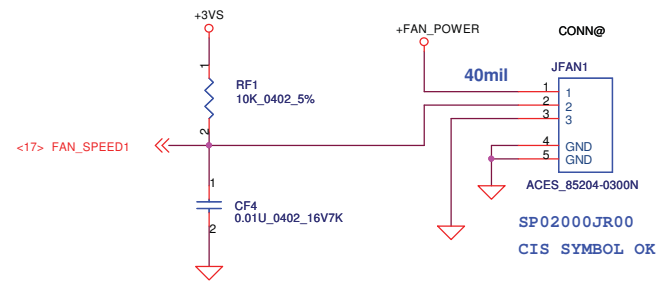
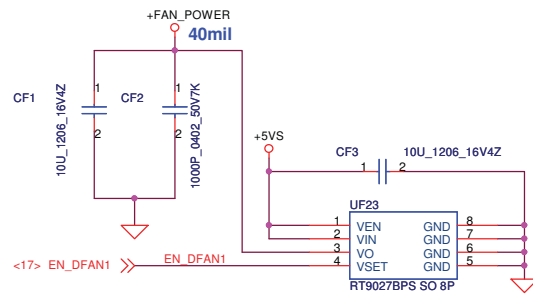
Title			WTB Conn/LED		
Size	Document Number	Rev			1.0
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HDD Connector



FAN Control circuit



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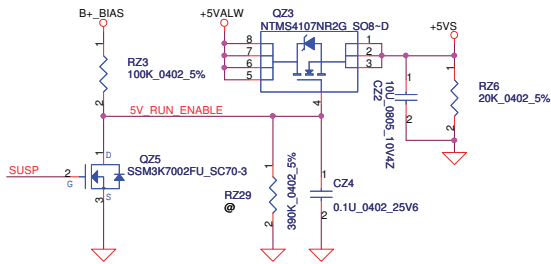
Compal Electronics, Inc.



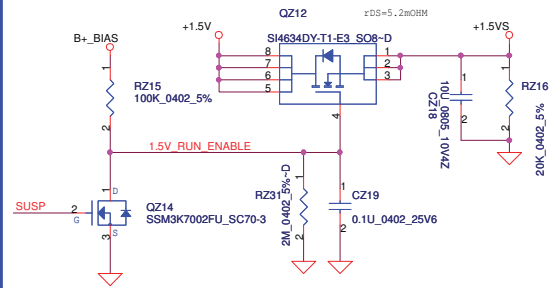
Title		FAN/HDD	
Size	Document Number	LA-7161P	
Date:	Wednesday, January 05, 2011	Sheet	27 of 43
Rev	1.0		

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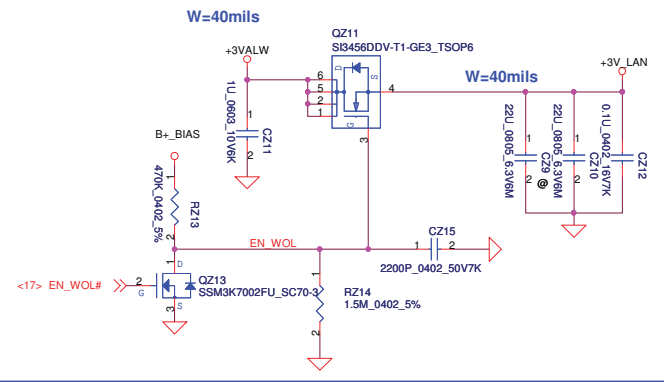
+5VALW to +5VS Transfer



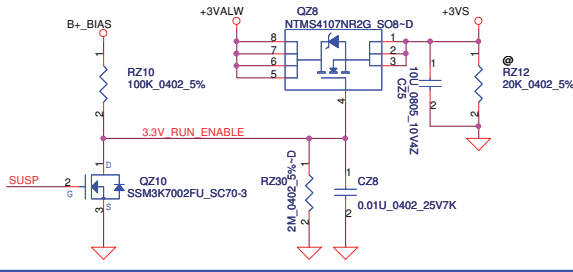
+1.5V to +1.5VS Transfer



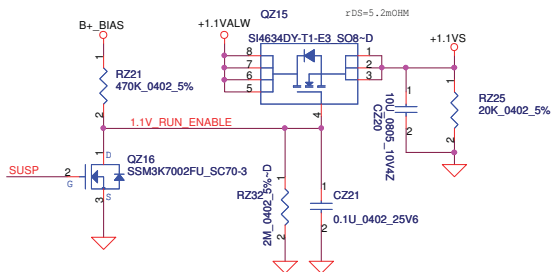
+3VALW to +3V_LAN Transfer



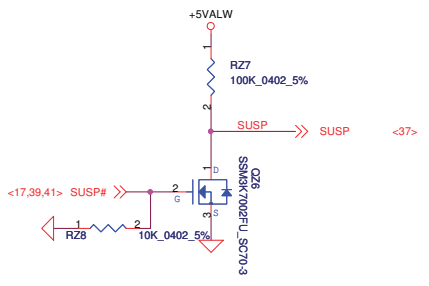
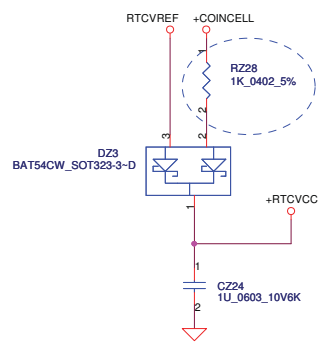
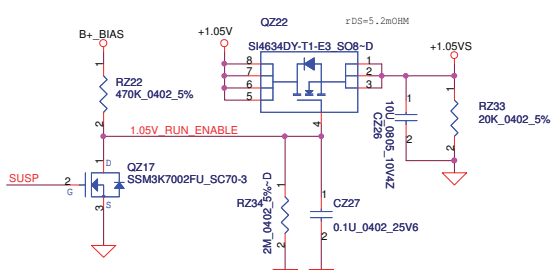
+3VALW to +3VS Transfer



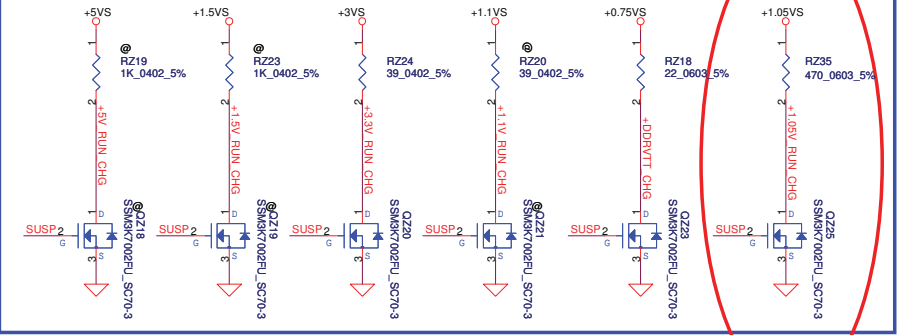
+1.1VALW to +1.1VS Transfer



+1.05V to +1.05VS Transfer



Discharg Circuit



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Compal Electronics, Inc.

Title			DC/DC (Power control)		
Size	Document Number	LA-7161P		Rev	1.0
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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
01	07	LVDS	09/28	EE	LCD Panel display abnormal	Swap LVDS Port	0.2
02	20	LVDS	09/28	EMI	LCD_PWM	Add 220 ohm Bead at LCD_PWM (BLM18BB221SN)	0.2
03	17	Board ID	09/28	EE	Change Board ID to X01	Change RE35 to 8.2K	0.2
04	17	ACIN	09/28	EE	Charge led always light when unplug AC	Change RE32 to 150K	0.2
05	29	Power Button ESD	10/08	ESD	Power Button ESD Protection	Change DZ4 to SCA00000R00	0.2
06	19	VGA	10/08	EMI	CRT EMI Noise	Change LV5;LV6;LV7 to SM01000FP00	0.2
07	21	LAN	10/08	EMI	LAN EMI Noise	Change TRL1 to SP050006N00	0.2
08	13;14	FCH	10/11	RF	RF Noise	Add CF20 & CF82 33PF	0.2
09	09	APU PWR	10/14	EE	AMD CRB Rev C update	LU1, LU2, LU4 change to 0_0805	0.2
10	07	LTDP_AUX	11/02	EE	AMD Check list update	RU14,RU15,RU23,RU26 change to 2K ohm pull up to +5VS	0.3
11	07	LTDP0_HPDP	11/02	EE	AMD Check list update	Add RU22 100k ohm pull up to +5VS	0.3
12	17	Board ID	11/17	EE	Change Board ID to X02	Change RE35 to 18K	0.3
13	10;11	DDRIII-SODIMM	11/22	EMI	DDR EMI NOISE	POP CD9,CD10,CD11,CD12,CD13,CD14,CD31,CD32,CD33,CD34,CD35,CD36	0.3
14	17	ENE-KB926	11/22	ESD	ESD	Add 0.1uF caps on CE25 & CE29	0.3
15	18	HDMI	11/22	ESD	ESD	Add 0.1uF caps CV36 on +3VS trace of top side layout.	0.3
16	21	LAN	11/22	ESD	ESD	Add 0.1uF caps CL84 on +3V_LAN trace of top side layout.	0.3
17	22	Card Reader	11/23	RF	RF Noise	Mount RB8=10,CB12=22P	0.3
18	12	FCH	11/23	RF	RF Noise	Mount CF80=33P	0.3
19	19	VGA	11/30	EE	AMD Check list update	Change RV31 & RV32 from 4.7K to 2K	0.3
20	17	Board ID	12/10	EE	Change Board ID to A00	Unpop RE35	1.0
21	19	VGA	12/10	Safety	LPS test fail	Delete RV67 . Pop FV2	1.0
22	28	DC/DC	12/16	Safety	Safety RTC battery test fail	Add RZ28 betwwn +COINCELL and DZ3 pin2	1.0
23	20	LVDS	12/23	EE	EC damage	Depop DV6 & RV44 . Pop DV14 & RV51	1.0

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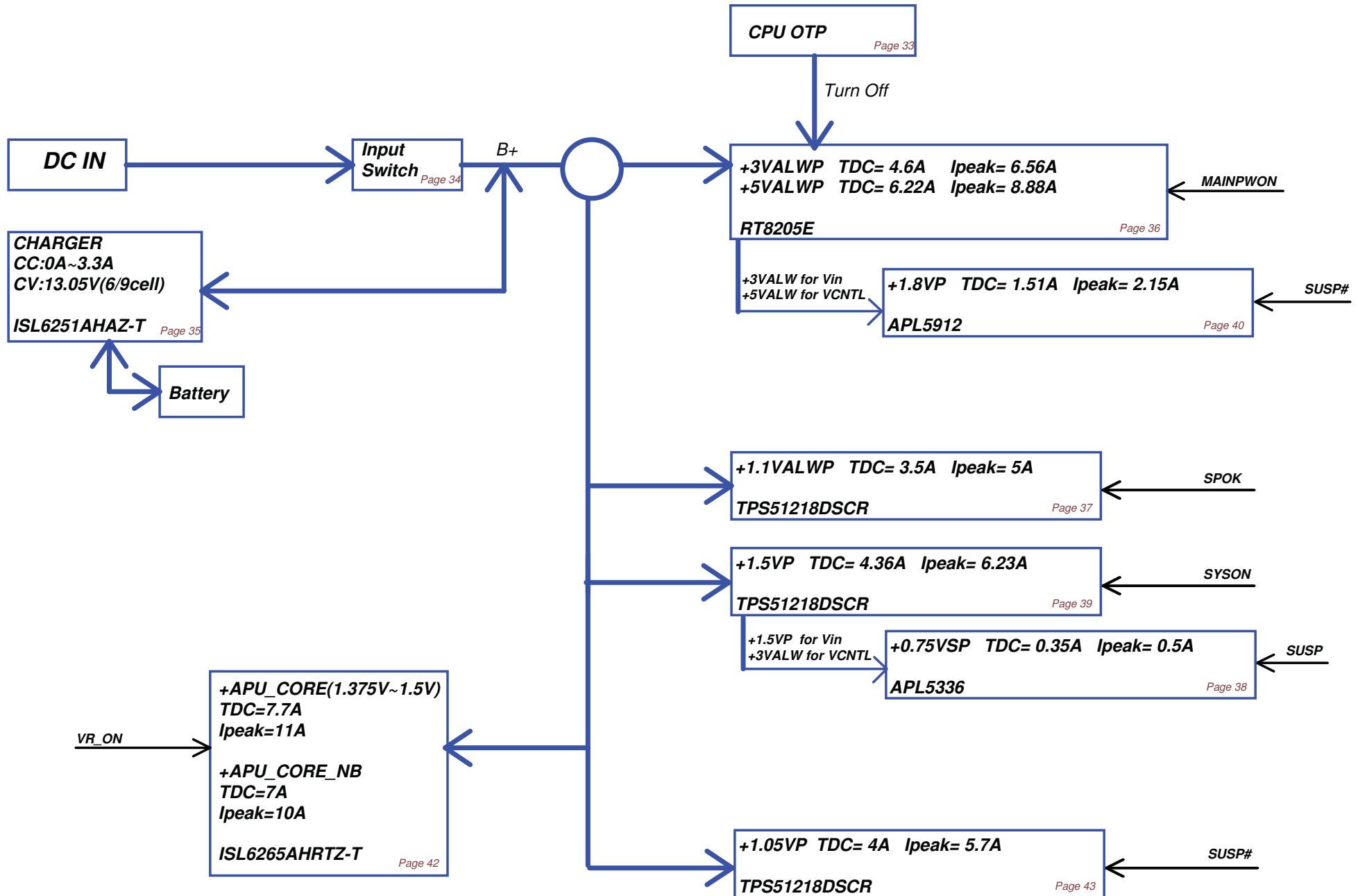
Compal Electronics, Inc.



Title		HW PIR	
Size	Document Number	Rev	
	LA-7161P	1.0	
Date:	Wednesday, January 05, 2011	Sheet	30 of 43

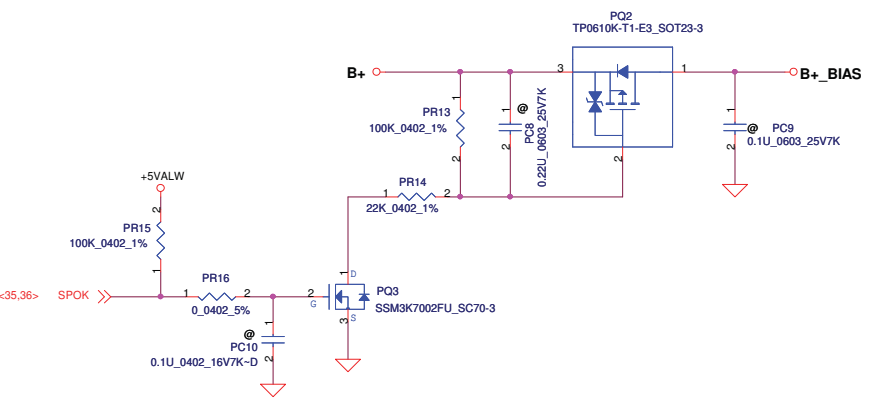
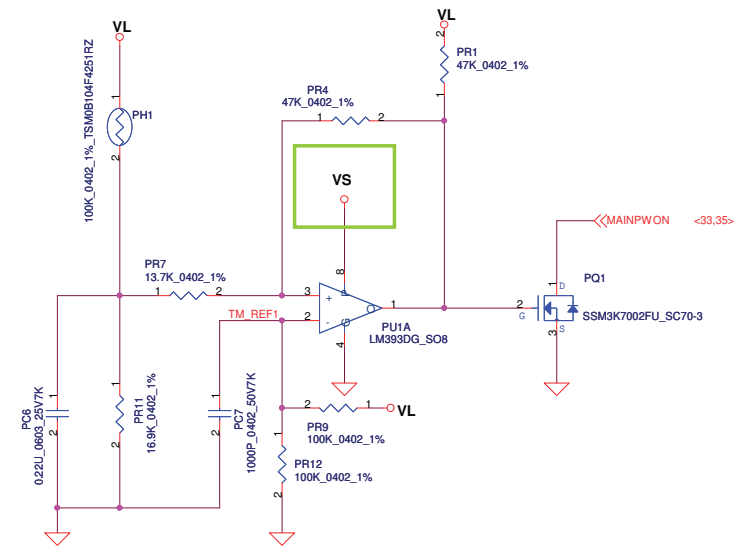
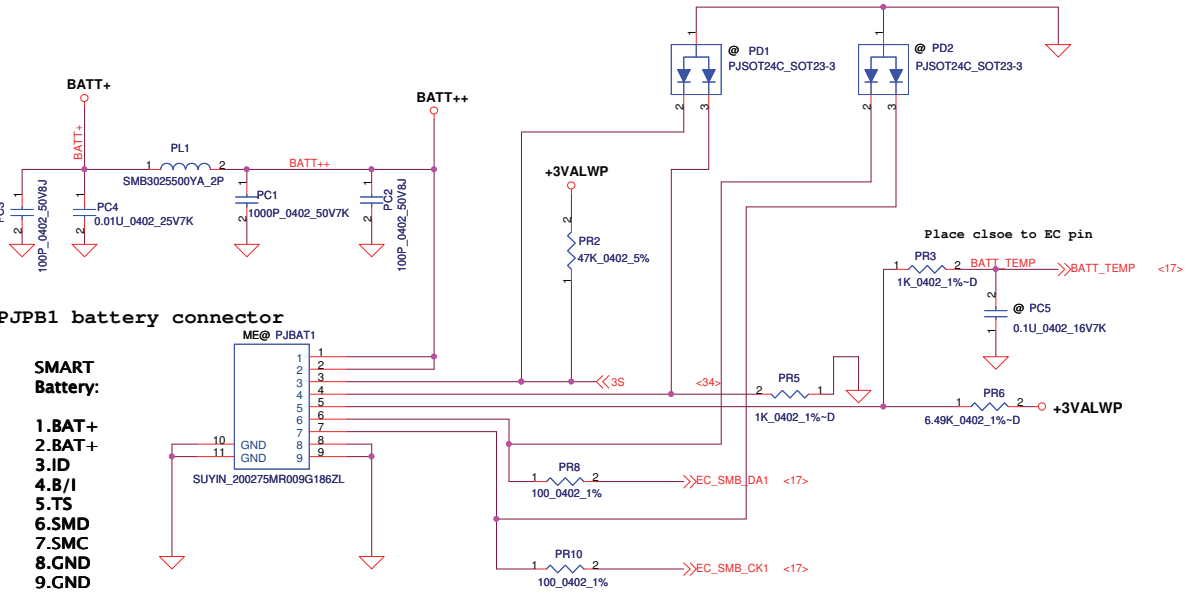
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Power block

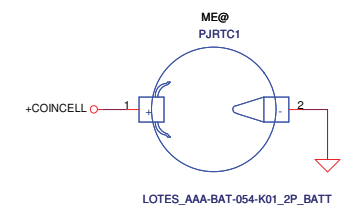


Title		
POWER BLOCK DIAGRAM		
Size	Document Number	Rev
Date: Wednesday, January 05, 2011	Sheet	31 of 43

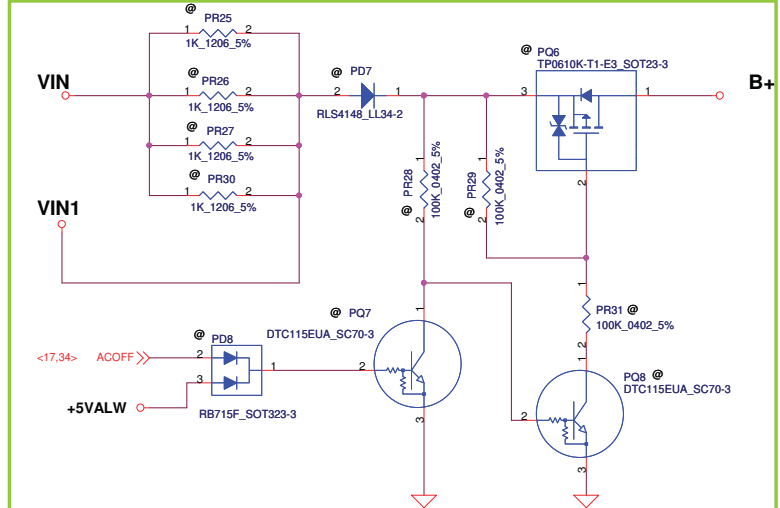
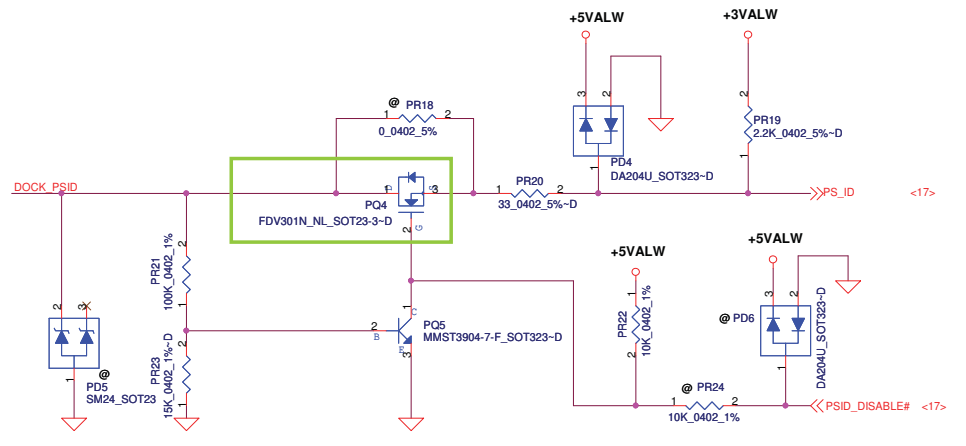
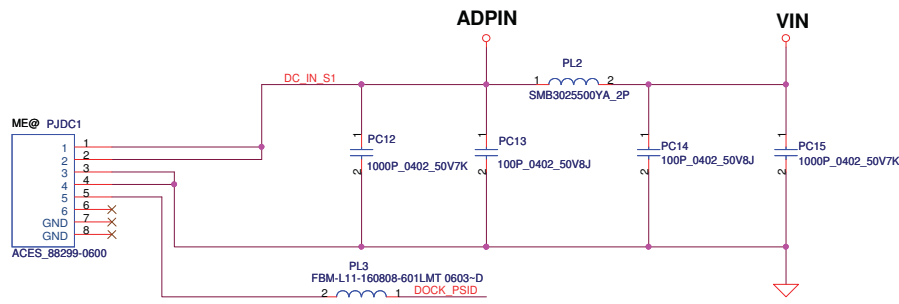
PH1 under CPU bottom side :
 CPU thermal protection at 90 +/-3 degree C
 Recovery at 50 +/-3 degree C



COIN RTC Battery



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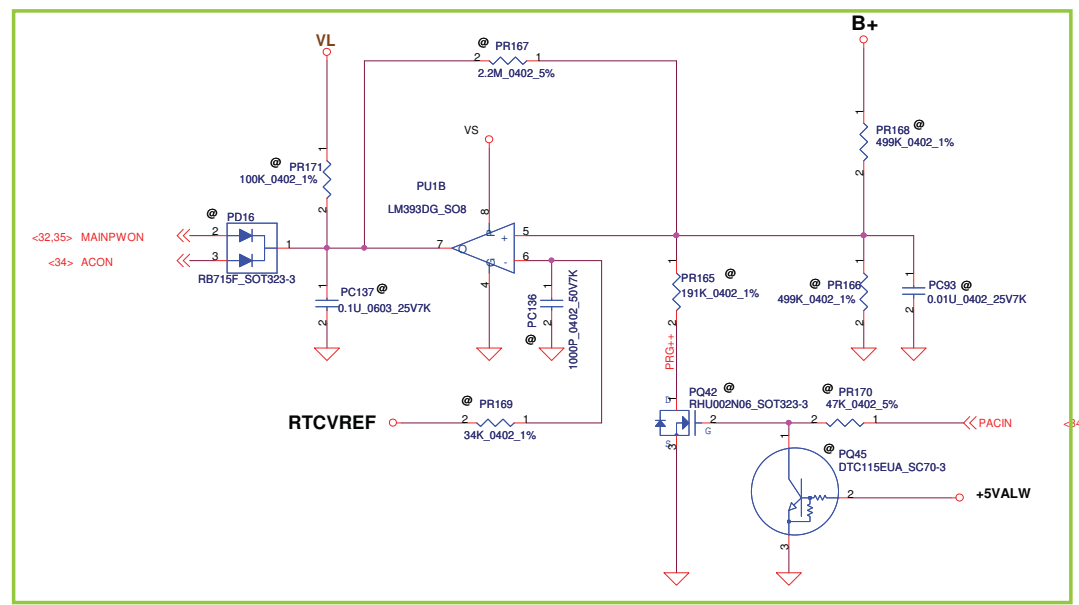
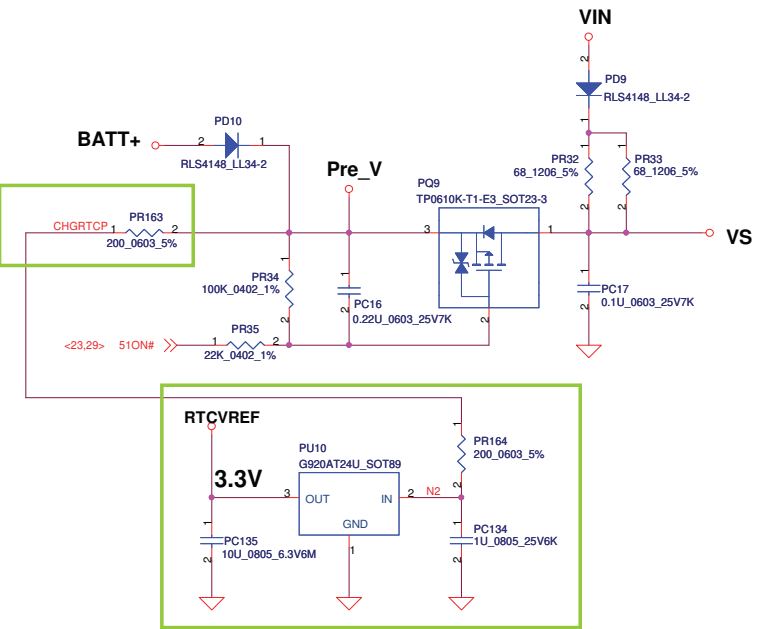


ACIN

	Precharge detector		
	Min.	typ.	Max.
H->L	14.589V	14.84V	15.243V
L->H	15.562V	15.97V	16.388V

BATT ONLY

	Precharge detector		
	Min.	typ.	Max.
H->L	6.138V	6.214V	6.359V
L->H	7.196V	7.349V	7.505V



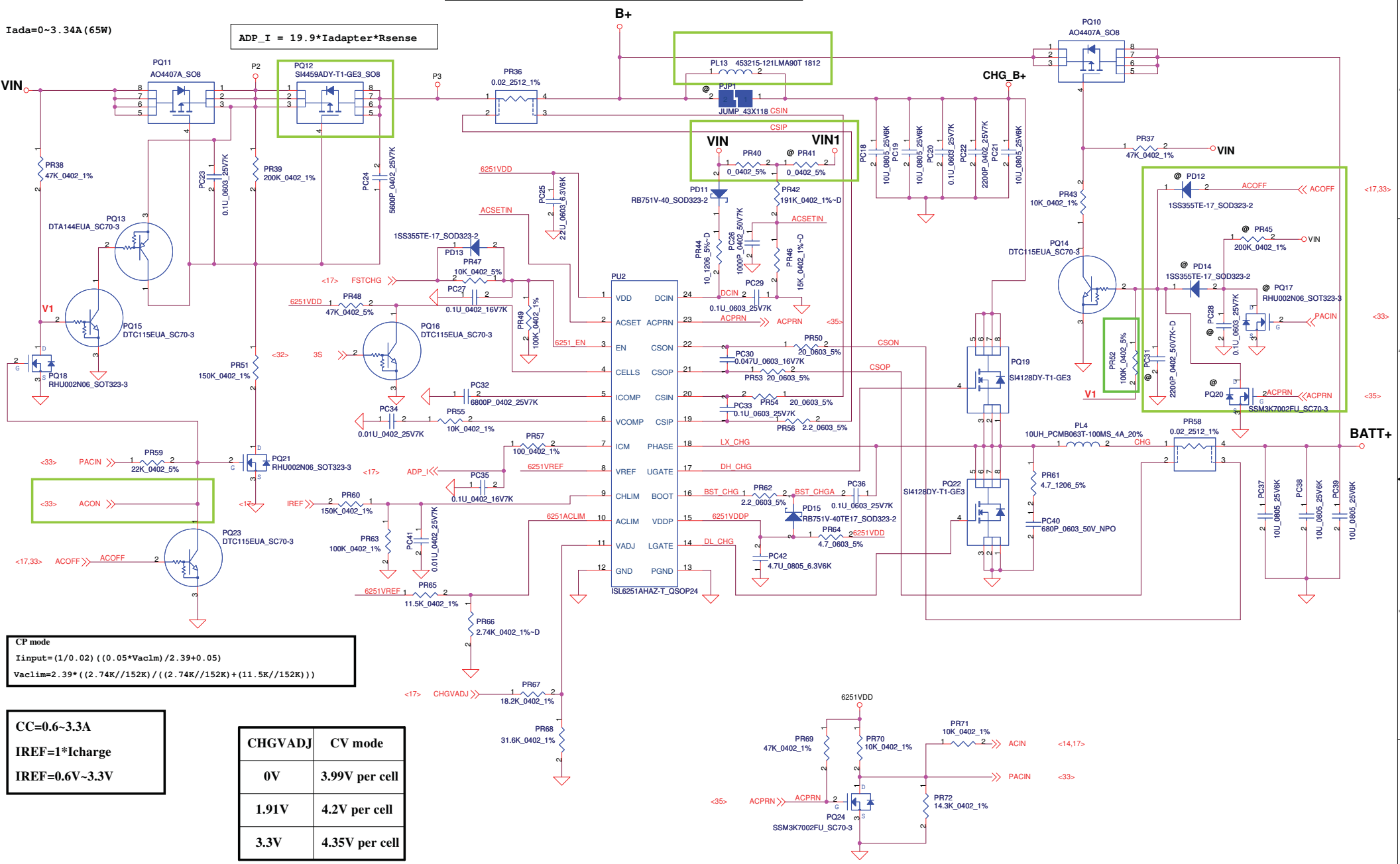
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Issued Date	2010/07/31	Deciphered Date
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Title		
DCIN & DETECTOR		
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$CP = 90\% \cdot I_{adapter} \text{ (rating)}; CP = 3.003A$

$I_{ada} = 0 \sim 3.34A \text{ (65W)}$

$ADP_I = 19.9 \cdot I_{adapter} \cdot R_{sense}$



CP mode
 $I_{input} = (1/0.02) \cdot ((0.05 \cdot V_{aclim}) / 2.39 + 0.05)$
 $V_{aclim} = 2.39 \cdot ((2.74K // 152K) / ((2.74K // 152K) + (11.5K // 152K)))$

CC=0.6-3.3A
 $I_{REF} = 1 \cdot I_{charge}$
 $I_{REF} = 0.6V \sim 3.3V$

CHGVADJ	CV mode
0V	3.99V per cell
1.91V	4.2V per cell
3.3V	4.35V per cell

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Compal Electronics, Inc.			
CHARGER			
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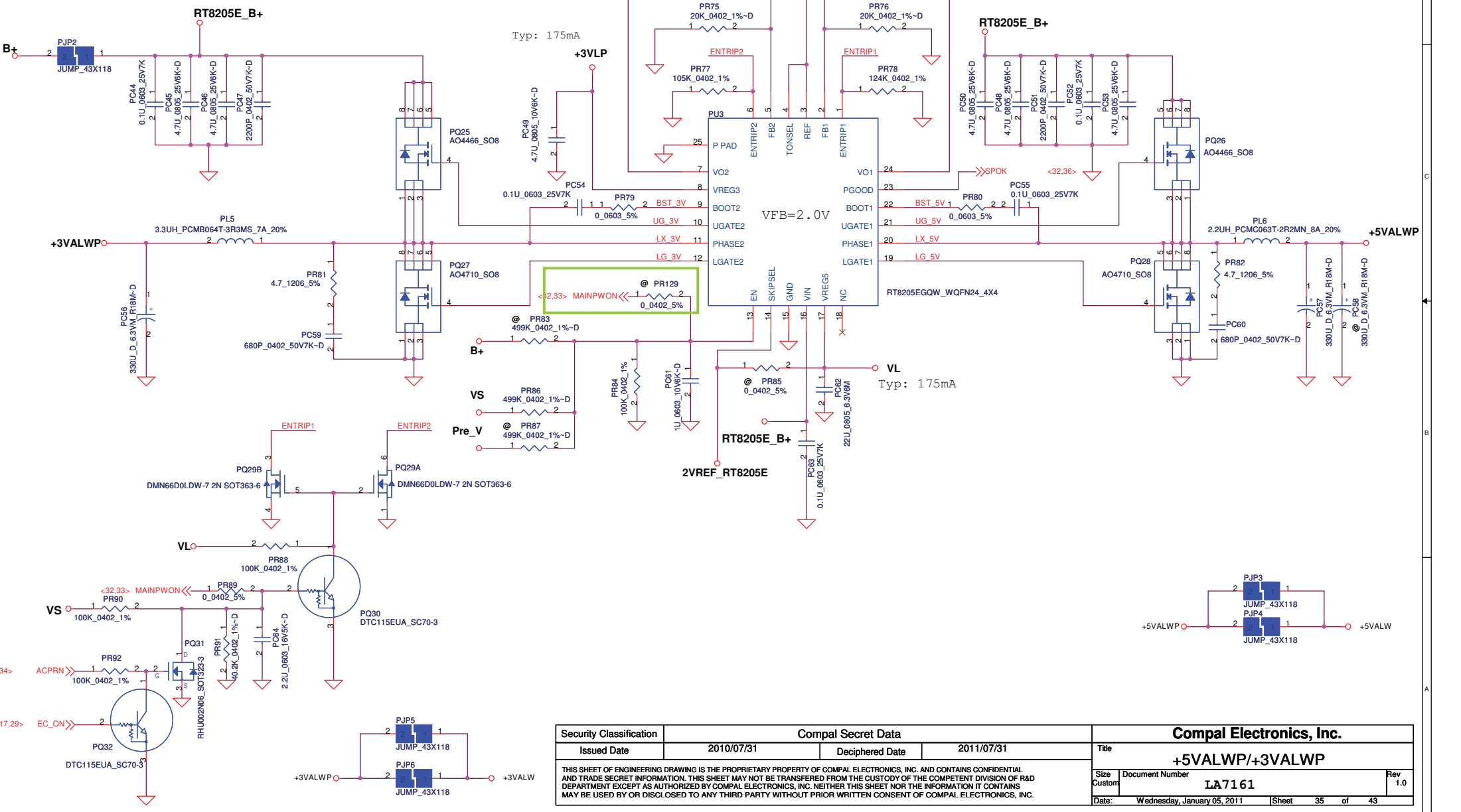
Note:
 Use RT8205E to replace TPS51125 IC can remove RTC refernece LDO
 Use RT8205E to replace TPS51427 IC must keep RTC refernece LDO

3.3VALWP

Thermal Design Current=4.6A
 Peak Current=6.56A
 OCP min=8.53A
 H/S RDS(on) 27m ohm(typ), 35m ohm(max)
 L/S RDS(on) 11.7m ohm(typ), 14.2m ohm(max)
 FSW 375KHz
 Delta I_{in}=0.8306A
 Delta I_o=2.2154A

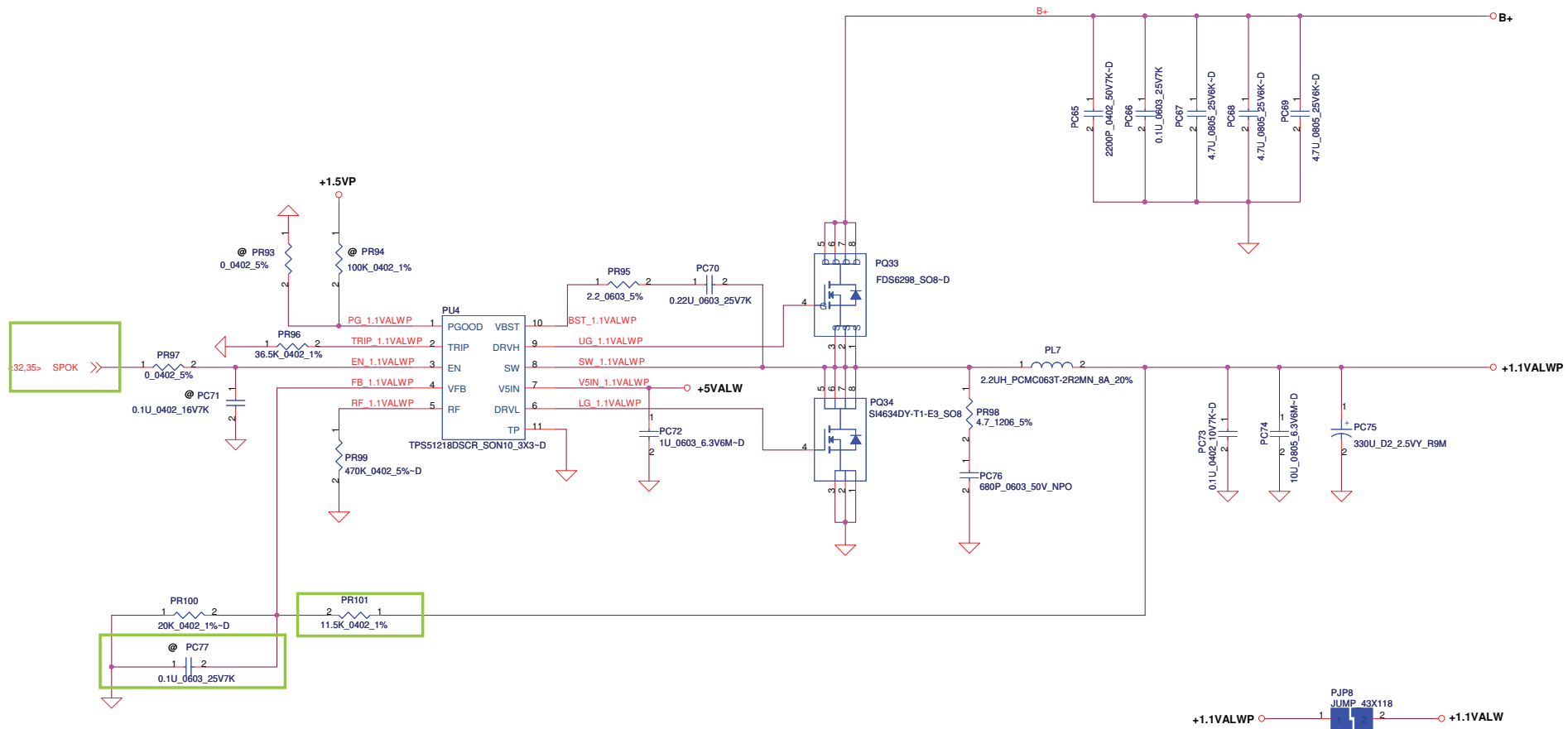
5VALWP

Thermal Design Current=6.22A
 Peak Current =8.88A
 OCP min=11.55A
 H/S RDS(on) 27m ohm(typ), 35m ohm(max)
 L/S RDS(on) 11.7m ohm(typ), 14.2m ohm(max)
 FSW 300KHz
 Delta I_{in}=2.4598A
 Delta I_o=5.6333A



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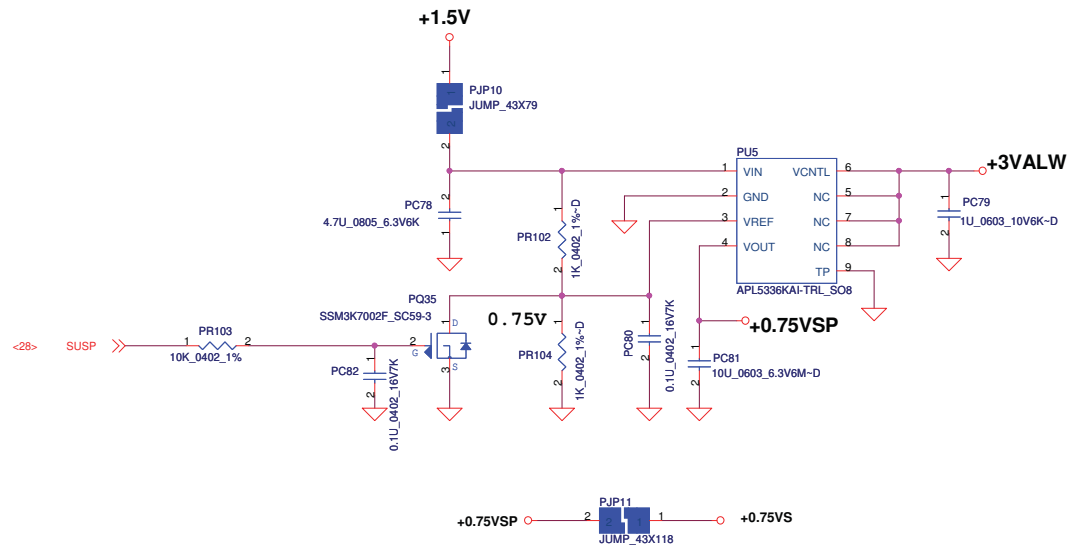
Compal Electronics, Inc.			
Title			
+5VALWP/+3VALWP			
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+1.1VALWP
 Thermal Design Current=3.5A
 Peak Current=5A
 OCP min=6.5A
 Fsw=290KHZ

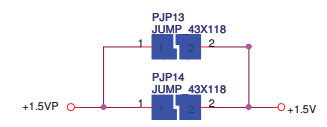
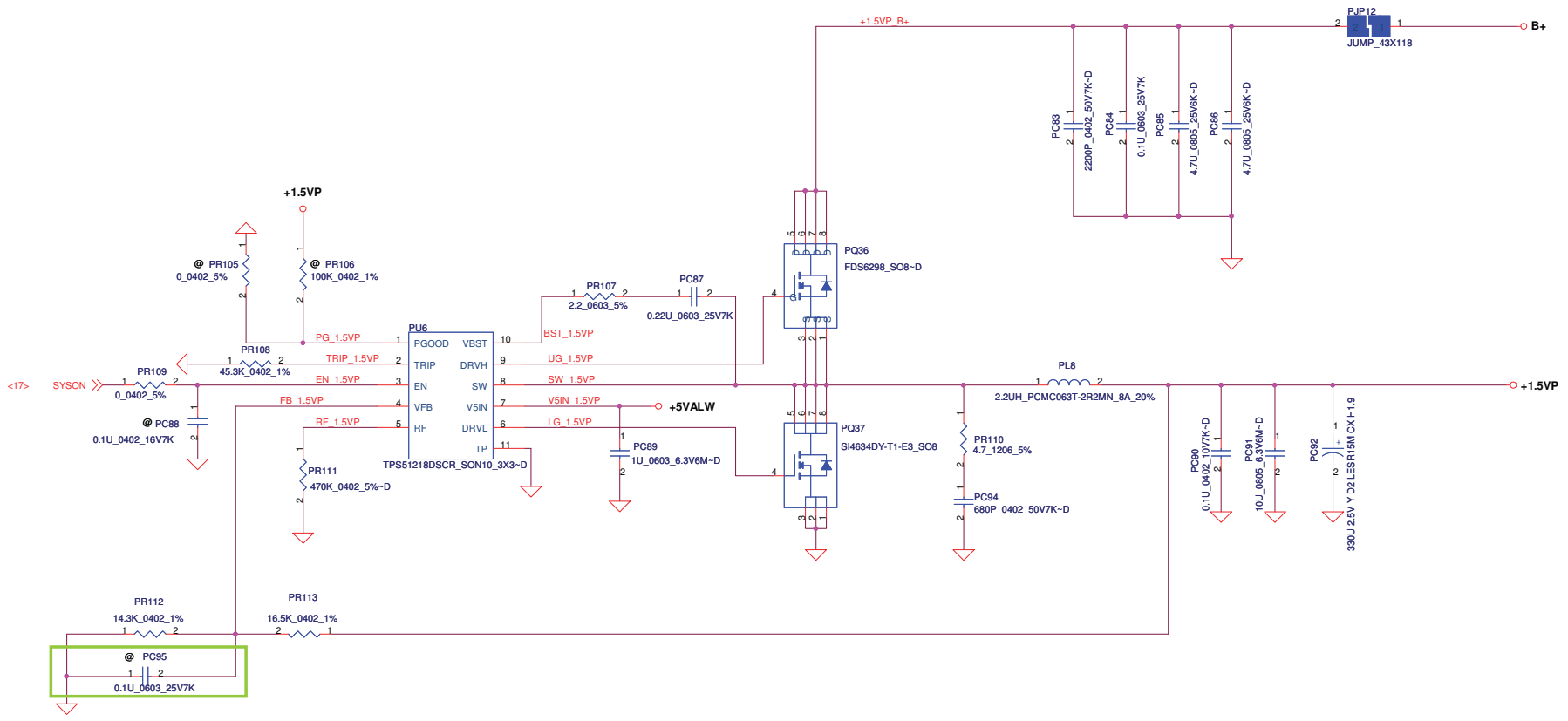
 Delta I=1.6269A
 L/S MOS Rds(on)=5.5m ohm (Typ) ; 6.7m ohm(Max)

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+0.75VSP
 Thermal Design Current=0.35A
 Peak Currnet=0.5A
 OCP min=0.65A

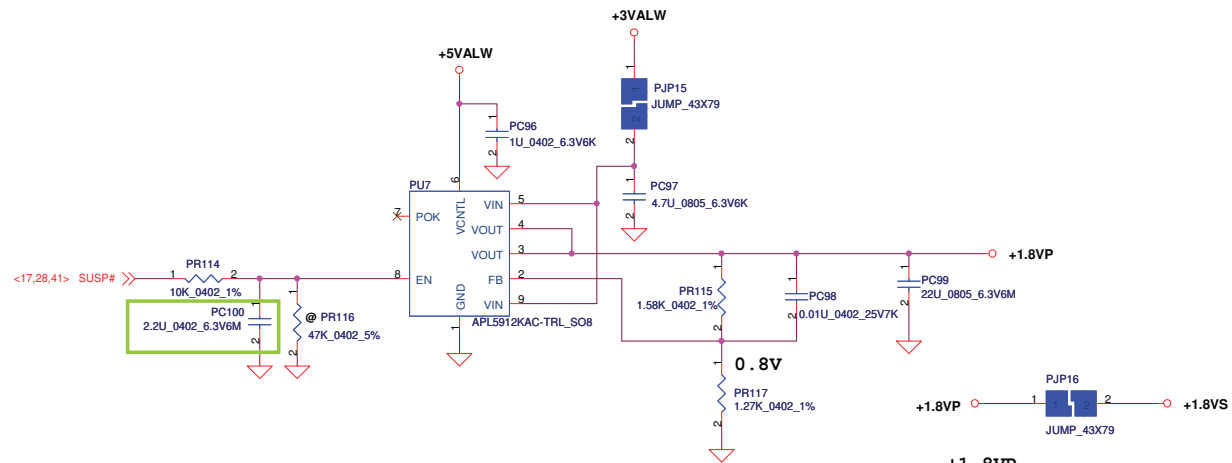
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Issued Date	2010/07/31	Deciphered Date	2011/07/31			Title
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+1.5VP
 Thermal Design Current=4.36A
 Peak Current=6.23A
 OCP min=8.1A
 Fsw=290KHZ

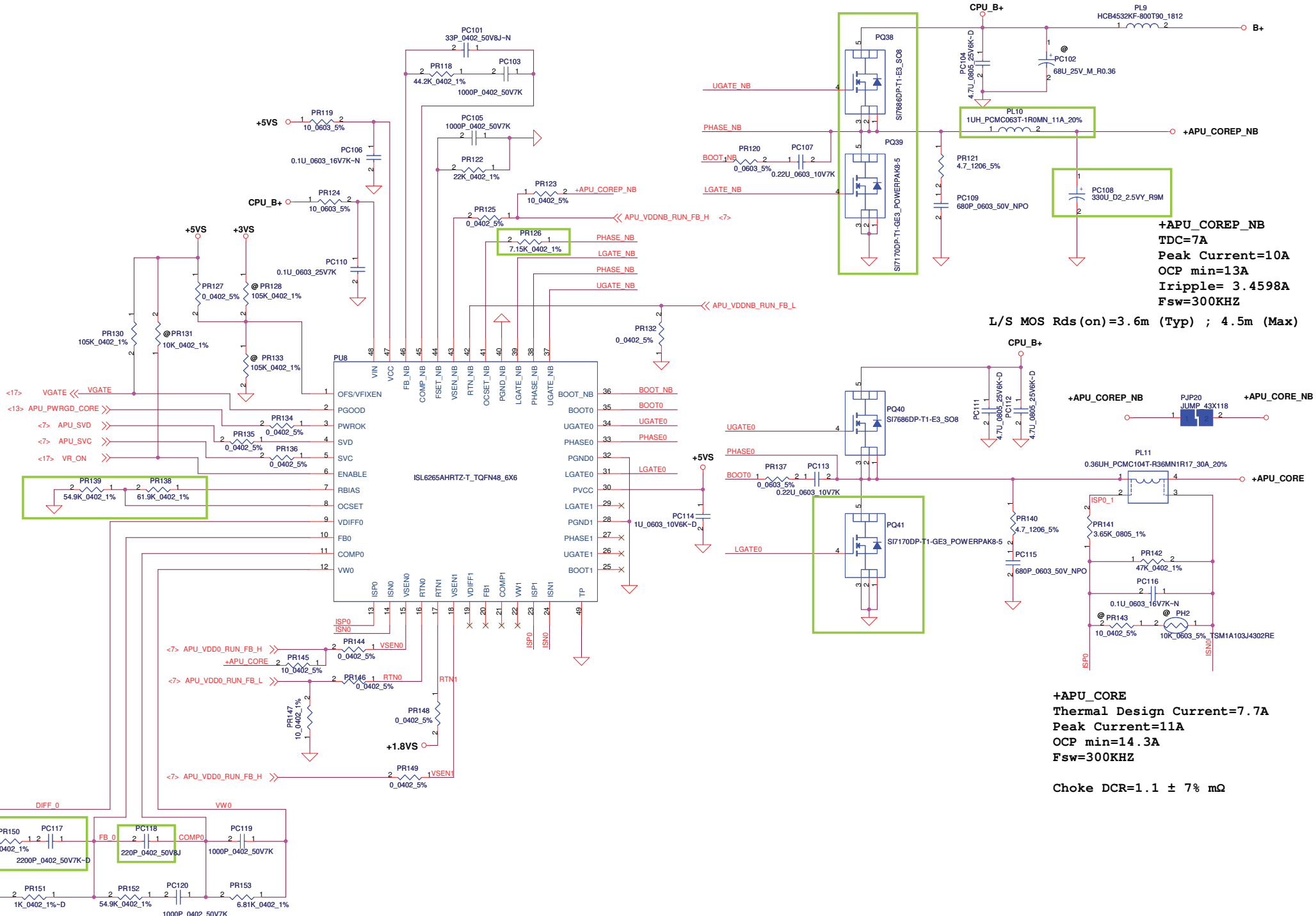
 Delta I=2.1702A
 L/S MOS Rds(on)=5.5m (Typ) ; 6.7m (Max)

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+1.8VP
 Thermal Design Current=1.51A
 Peak Current=2.15A
 OCP min=2.8A

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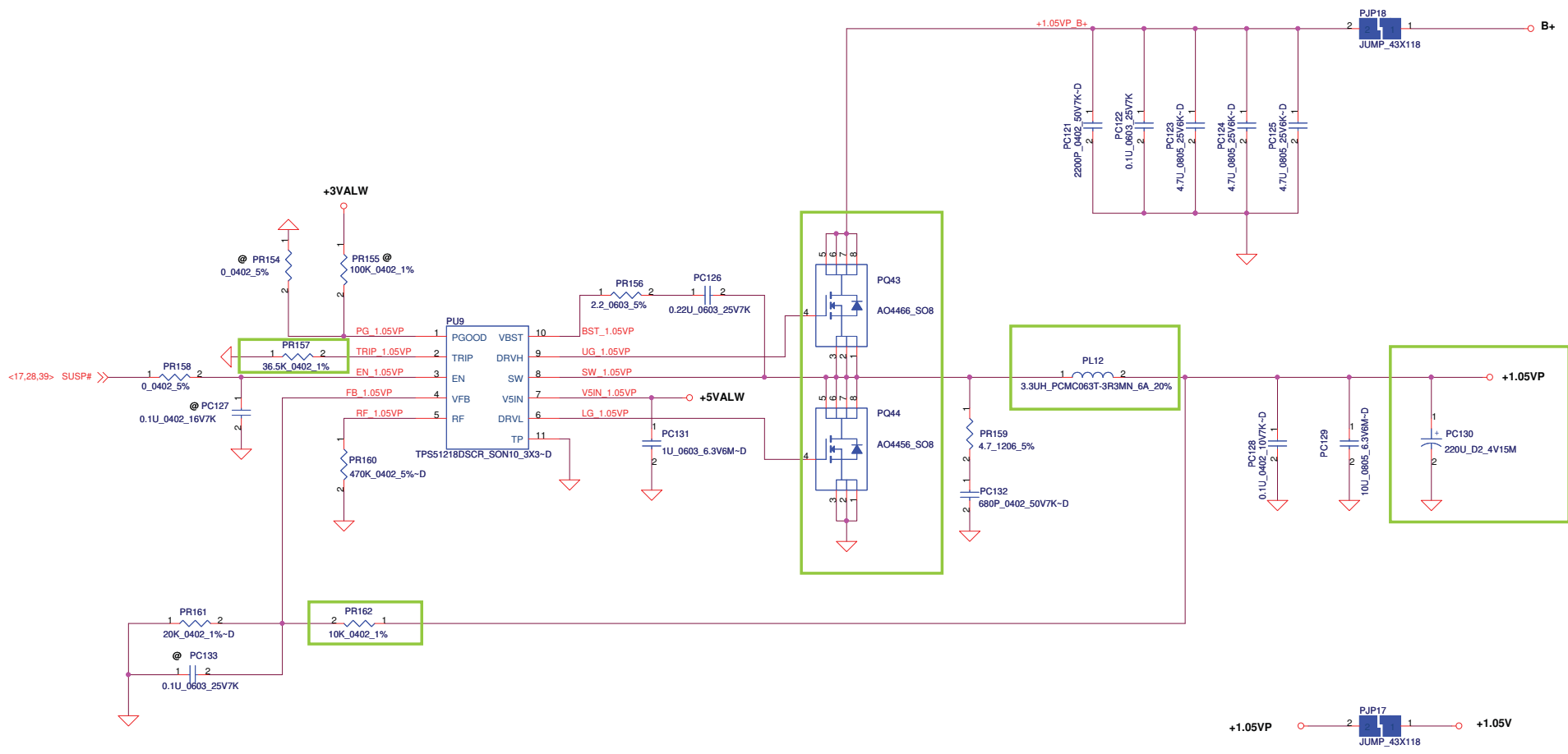
+APU_CORE_NB
TDC=7A
Peak Current=10A
OCp min=13A
Iripple= 3.4598A
Fsw=300KHZ

L/S MOS Rds (on)=3.6m (Typ) ; 4.5m (Max)

+APU_CORE
Thermal Design Current=7.7A
Peak Current=11A
OCp min=14.3A
Fsw=300KHZ

Choke DCR=1.1 ± 7% mΩ

Security Classification	Compal Secret Data		Title	
Issued Date	2010/07/31	Deciphered Date	2011/07/31	Compal Electronics, Inc.
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+1.05VP
 Thermal Design Current=4A
 Peak Current=5.7A
 OCP min=7.41A
 Fsw=290KHZ

 Delta I=1.0381A
 L/S MOS Rds (on)=4.5m (Typ) ; 5.6m (Max)

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1	40	+APU_CORE/ +APU_COREP_NB	2010/10/04	Compal	PC102(H=5.8mm) will impact ME logic lower	Depop PC102 (P/N : SF000000W00)	X01
2	33 32	DCIN BATTERY CONN /OTP/B+_BIAS	2010/10/12	Compal	HW power share no function when system at S5 ony with battery without AC.	<ol style="list-style-type: none"> Add PR163, PR164 (P/N : SD013200080) (S RES 1/10W 200 +-5% 0603); PU10 (P/N : SA009200010) (S IC G920AT24U SOT89 REG 3.3V); PC134 (P/N : SE000001380) (S CER CAP 1U 25V K X5R 0805 H1.25); PC135 (P/N : SE093106M80) (S CER CAP 10U 6.3V M X5R 0805 H1.25) Modify PD3.pin3 net name, change from +3VLP to RTCVREF Delete PD3, PR17, PC11 =>Cause HW side has alike RTC circuitry (DZ3 and CZ24) 	X01
3	32	BATTERY CONN /OTP/B+_BIAS	2010/10/18	Compal	For reduce S5,S4 power leakage when system only with battery	Change PU1A.pin8 net-name from Pre_V to VS	X01
4	32	BATTERY CONN /OTP/B+_BIAS	2010/10/18	Compal	for ME team change RTC battery connector.	Change PJRTC1 P/N from SP02000IA00(with Cable) to SP07000H700(w/o cable)	X01
5	34	CHARGER /DETECTOR	2010/10/18	Compal	follow compal power team new AC-IN, Pre-charge circuits with 連動circuits, need change design to original pre-charge design and ADP/BAT switch circuits.	<ol style="list-style-type: none"> Depop PR52 (P/N : SD02810030L), PQ20 (P/N : SB000009610) Pop item: PD12 (P/N: SC1SS355010)S DIO 1SS355TE-17 SOD323 PD14 (P/N: SC1SS355010)S DIO 1SS355TE-17 SOD323 PR45 (P/N: SD034200380)S RES 1/16W 200K +-1% 0402 PC28 (P/N: SE042104K80)S CER CAP .1U 25V K X7R 0603 PQ17 (P/N: SB502060000)S TR RHU002N06 1N SOT323 	X01
6	34	CHARGER /DETECTOR	2010/10/22	Compal	follow compal power team new AC-IN, Pre-charge circuits with 連動circuits, need change design to original pre-charge design and ADP/BAT switch circuits.	1. Pop PQ20 (P/N: SB000009610) (S TR SSM3K7002FU 1N SC70-3))	X02
7	35	+3VALWP /+5VALWP	2010/11/24	Compal	QAD team highlight BITS issue DF434417: [Rel, PT] OTP (PH1) recovery temperature can't meet spec. The recovery temperature spec is 50 +/- 3degree C.	Add @PR129 (P/N: SD028000080) (S RES 1/16W 0 +-5% 0402)	X03
8	33 34	DCIN CHARGER /DETECTOR	2010/11/24	Compal	follow compal power team new AC-IN, Pre-charge circuits with 連動circuits, need change design to original pre-charge design and ADP/BAT switch circuits.	<ol style="list-style-type: none"> Depop : PD7, PD8, PQ6, PQ7, PQ8, PR25, PR26, PR27, PR28, PR29, PR30, PR31 Add @PC93, @PC136, @PC137, @PD16, @PQ42, @PQ45, @PR165, @PR166, @PR167, @PR168, @PR169, @PR170, @PR171 Depop PR41, pop PR40 (P/N: SD028000080) (S RES 1/16W 0 +-5% 0402) Pop PR52 (P/N: SD028100380) (S RES 1/16W 100K +-5% 0402), depop PC28, PC31, PD12, PD14, PQ17, PQ20, PR45 Change PQ21.2 net name to "ACON" 	X03

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9	P35 P36 P38 P40 P41	3VALWP/5VALWP +1.1VALWP +1.5VP +APU_CORE /+APU_COREP_NB +1.05VP	2010/11/24	Compal	for support DFX team and SMT AOI detect: 較容易檢測出是否 空焊現象	follow DFX team-Chen. Daniel suggestion: to use the pad length 3.6*2.5mm PCB footprint for the PL6, PL7, PL8, PL10, PL12 material as PL5 . Change PL6 footprint from (CYNTE_PCMC063T-2R2MN_2P) to (CYNTE_PCMB064T-3R3MS_2P) PL7 footprint from (CYNTE_PCMC063T-2R2MN_2P) to (CYNTE_PCMB064T-3R3MS_2P) PL8 footprint from (CYNTE_PCMC063T-2R2MN_2P) to (CYNTE_PCMB064T-3R3MS_2P) PL10 footprint from (CYNTE_PCMC063T-1R0MN_2P) to (CYNTE_PCMB064T-3R3MS_2P) PL12 footprint from (CYNTE_PCMC063T-3R3MN_2P) to (CYNTE_PCMB064T-3R3MS_2P)	X03
0	34	CHARGER /DETECTOR	2010/11/26	Compal	Support EMC team to reduce nosie	Add @PL13 and lyaout footprint co-layout with PJP1	X03
1	34	CHARGER /DETECTOR	2010/12/14	Compal	Support EMC team to reduce nosie	1. Pop PL13 (P/N: SM01000DJ00) (S SUPPRE_ FBMA-L11-453215-121LMA90T 1812) this bead value= 120 ohm(Current rating=9A) 2. Depop PJP1	A00

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